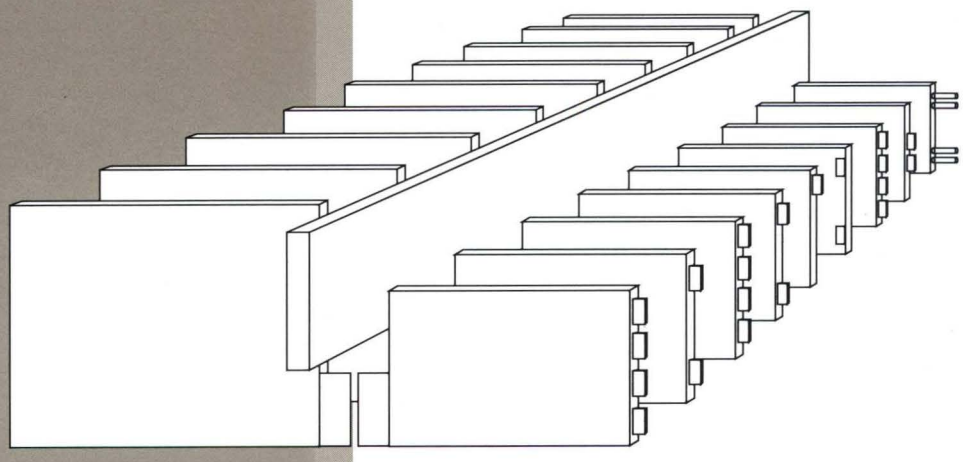
Symmetric Multiprocessor Architecture



WELLFLEET communications

Symmetric Multiprocessor Architecture

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MISSION-CRITICAL INTERNETWORKING REQUIREMENTS

All organizations depend on information to meet their revenue and/or cost control goals. An enterprise internetwork must transport mission-critical information quickly and reliably to those that require it. Consequently, an internetwork that supports the enterprise and its mission-critical applications requires routers that satisfy the following five requirements:

Connectivity, Interoperability, and Manageability

To create an enterprise internetwork, connectivity, interoperability, and manageability within a wide variety of network environments must be supported:

- LAN connectivity for Ethernet/802.3, 4 and 16 Mbps Token Ring/802.5, and FDDI
- Concurrent support of multiple protocols and bridging standards including TCP/IP with OSPF, RIP and EGP; DECnet Phase IV; OSI with ES-IS and IS-IS; Xerox XNS; Novell IPX; AppleTalk; Banyan VINES; Spanning Tree Algorithm; Source Route Bridge; Translation Bridge (FDDI-to-Ethernet); Transparent Bridge (FDDI and Ethernet); and SNA/SDLC
- Private, public or hybrid wide-area networks using low speed circuits, Fractional T1, T1/E1, T3/E3, X.25, Frame Relay, SMDS, SONET OC-1, ATM, and Point-to-Point Protocol
- Comprehensive node and SNMP-based network management

Performance

A multiprotocol internetwork requires powerful routers to concurrently handle such diverse network environments and to satisfy response time requirements. Router performance needs to be scalable to the number and type of networks supported initially and in the future. Support for newer network technologies such as FDDI, T3 and SMDS require new, much higher levels of performance.

Availability

A mission-critical internetwork cannot afford downtime. This especially true of mission-critical applications based upon IBM's SNA. The highest system reliability, availability and maintainability are critical requirements.

Broad, Scalable Product Family

An enterprise internetwork requires a family of routers that satisfy a broad spectrum of connectivity, performance and availability requirements ranging from remote site and workgroup access to high-performance, highly available backbone hubs. Scalability in network connectivity and performance are required to accommodate future internetwork expansion.

Standards Adherence

Adherence to industry standards guarantees connectivity and interoperability today and in the future. This protects an organization's investments including the investments in people trained to design and manage the internetwork.

The choice of a router architecture affects all of these requirements. However, a router architecture has the most significant impact in the areas of performance, availability and product family breadth and scalability.

ROUTER ARCHITECTURE ALTERNATIVES

EVOLUTION OF ROUTER ARCHITECTURES

The evolution of routers has resulted in three distinct architectures:

- Single processor
- Modified single processor
- Symmetric multiprocessor

All three architectures are being positioned to satisfy the requirements of enterprise internetworks supporting mission-critical applications. However, these architectures are not equal in their ability to satisfy these key requirements:

- Scalable, high performance
- High availability, including on-line operational servicing (hot swap) and no single point of system failure

The differences are highlighted in the following descriptions of each architecture.

SINGLE PROCESSOR ARCHITECTURE

The single processor architecture uses multiple network interface modules for node configuration flexibility. Network interface modules are connected to a single, central processor via a single system bus. The single processor must perform all processing tasks — filter/forward packets, modify packet headers as required, update routing and address databases, interpret management packets, respond to SNMP requests, generate management packets, and operate other services such as special packet filters implemented for enhanced network security and/or performance.

This architecture has the following impact on system performance and availability:

Performance

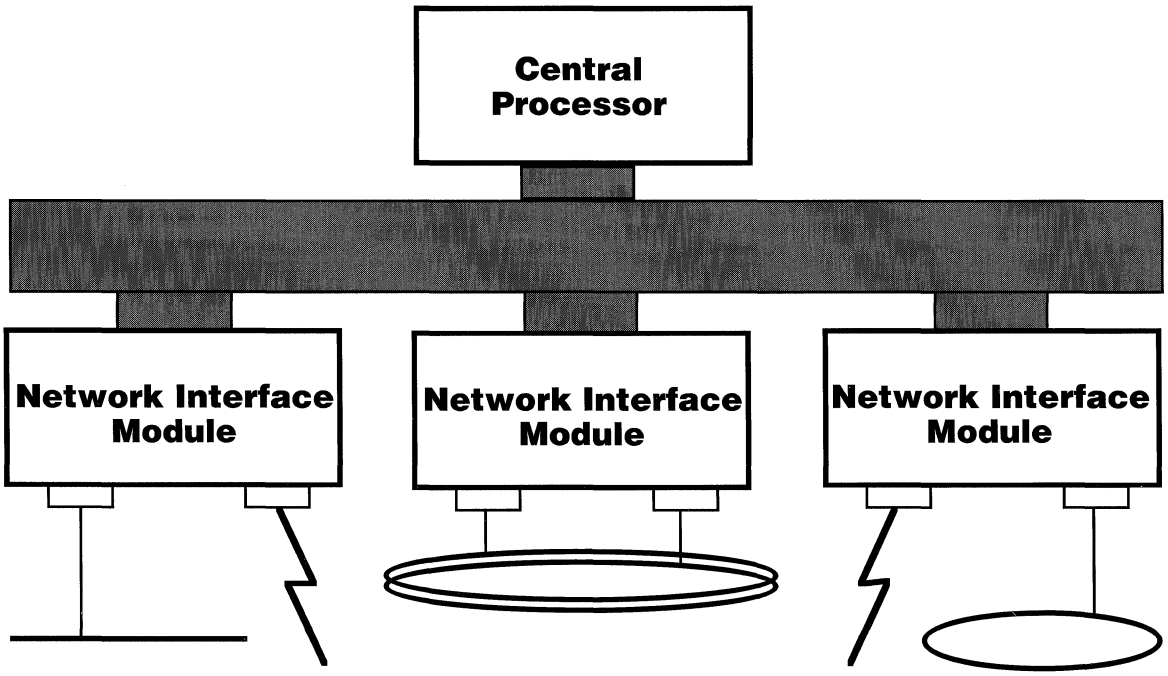
1. All packets from all network interfaces must be processed by the single central processor. This results in significant performance degradation as network interfaces are added.
2. All packets must traverse the system bus twice even when packets are destined for a network interface on the same network interface module. This also results in significant performance degradation as network interfaces are added.

Availability

3. Should the single, central processor fail, the router will fail. Additionally, complete on-line operational servicing (hot swap) cannot be performed in this architecture.

Recent implementations utilize a single RISC microprocessor and a higher speed system bus in an attempt to overcome the two performance deficiencies identified above. However, these implementations do not produce scalable system performance, but only somewhat higher aggregate system-level performance and higher initial costs. They continue to be vulnerable to failure of the single, central processor.

Single Processor Architecture



MODIFIED SINGLE PROCESSOR ARCHITECTURE

The modified single processor architecture overcomes some of the deficiencies associated with the single processor architecture. The underlying architecture is exactly the same as the single processor architecture (multiple network interface modules connected to a single, central processor via a single system bus) except that peripheral processors have also been added to each of the network interface modules in order to off-load some of the processing burden from the single, central CPU.

The peripheral processors on the network interface modules are typically bit-slice or general purpose microprocessors that usually filter and route packets destined for a network interface on the same network interface module. However, actual implementations are often tuned only for specific packet types such as Ethernet frames but not IEEE 802.3 frames.

The central processor is still responsible for those tasks which cannot be performed by the peripheral processor including intermodule routing and overall system operation (e.g. routing table updates), management and administration.

This architecture has the following impact on system performance and availability:

Performance

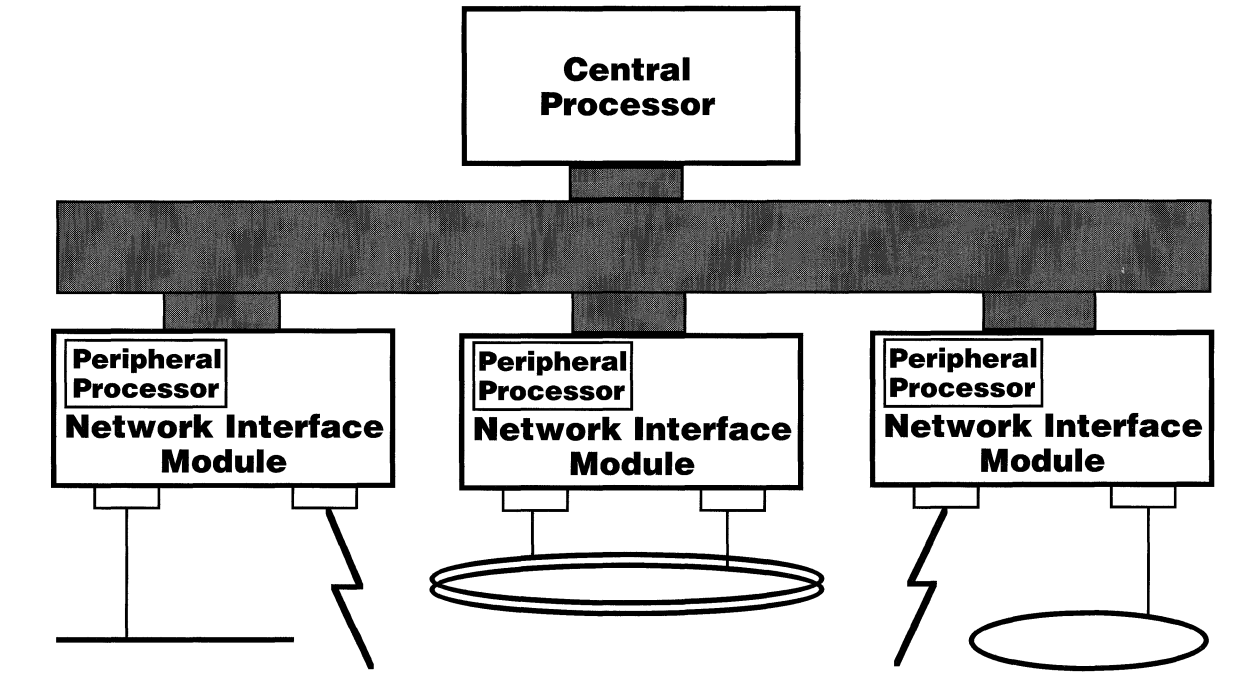
1. All packets destined for network interface(s) on other modules and overhead traffic (e.g. routing updates, management traffic,etc.) must be processed by the single, central processor. This results in serious performance degradation when there is significant traffic that must be forwarded to a different network interface module or which cannot be processed locally.

2. All packets that must be processed by the single, central processor must traverse the system bus twice. This also results in significant performance degradation as network interfaces are added.

Availability

3. Should the single, central processor fail, the router will fail. Additionally, complete on-line operational servicing (hot swap) cannot be performed in this architecture.

Modified Single Processor Architecture



SYMMETRIC MULTIPROCESSOR ARCHITECTURE

The symmetric multiprocessor architecture overcomes all of the deficiencies associated with both the single and modified single processor architectures. In this architecture, processing power is completely distributed to each network interface module.

Each network interface module has its own dedicated processor module which performs all routing processing tasks — filter/forward packets, modify packet headers as required, update routing and address databases, interpret management packets, respond to SNMP requests, generate management packets, and operate other services such as special packet filters implemented for network security and/or performance. The routing information base and protocol software is replicated on each processor module. Whenever a processor module receives routing information, it updates its own information base and distributes updates to all other processor modules.

This architecture has the following impact on system performance and availability:

Performance

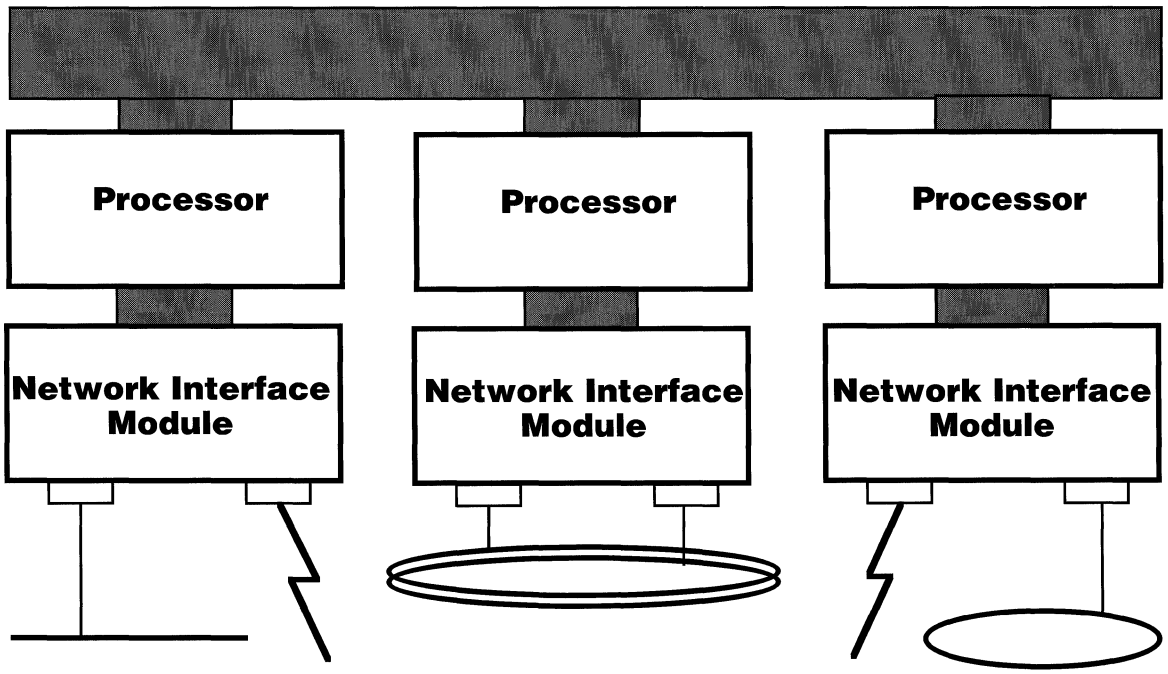
1. Network growth can be accommodated without any degradation in overall system performance since processing power is added as network interface modules are added. There is no central processor for any routing processing tasks.

2. All packets are processed by the local processor module. In addition, all outbound packets destined for a different network interface module must traverse the processor interconnect only once. This results in lower overall traffic levels over the processor interconnect.

Availability

3. The system will not fail should a single processor module fail. Only those networks connected to the failed processor module will be impacted. Additionally, complete on-line operational servicing (hot swap) can be performed in this architecture.

Symmetric Multiprocessor Architecture



WELLFLEET'S SYMMETRIC MULTIPROCESSOR ARCHITECTURE

DESIGN REQUIREMENTS

Wellfleet extensively evaluated and tested alternative router architectures supporting multiple protocols over various LAN and WAN media under varying traffic conditions (e.g. packet size, frequency, etc.). As a result of this evaluation, Wellfleet established the following ten router design requirements for routers used in building enterprise internetworks supporting mission-critical applications.

General

1. Overall requirements for scalable performance, high availability including on-line operational servicing (hot swap) and no single point of system failure, and flexible configuration capabilities dictate a symmetric multiprocessor architecture.

Performance

2. Computational requirements of multiprotocol routing (especially the use of compute-intensive link-state routing protocols such as TCP/IP's OSPF and OSI's IS-IS, and advanced filtering techniques) requires the most powerful 32-bit microprocessor. The CPU should also include integral caches and exhibit extremely low context switch latencies to enable the CPU to switch rapidly between the multiple processing tasks inherent in multiprotocol routing.

3. Storage of protocol software, routing tables, address tables, system configuration, management protocols and statistics requires a large memory space.

4. Storage of large volumes of transient user data for networks having vastly different bandwidth requires a large buffer space.

5. Maximum data transfer rates between networks and the router's processing modules requires high-performance network interface controllers and processor interconnect controllers with integrated direct memory access (DMA) capabilities.

6. Minimum delay and contention requires high bandwidth, 32-bit wide data and address paths between all resources.

Availability

7. Availability requirements including no single point of system failure require redundant power supplies, software image storage subsystems, and processor interconnects as options.

8. Reliability and maintainability requirements necessitate a design which minimizes the number of internal connectors and cables, maximizes accessibility of internal modules and components, avoids the use of ROM or PROM-based software, facilitates the visual identification of failed components, and maximizes the use of modules across a family of products.

Product Family Breadth and Scalability

9. Maximum flexibility and cost-effectiveness in connecting to the many different LAN and WAN media requires computing and storage resources and network interface resources to be located on different physical modules.

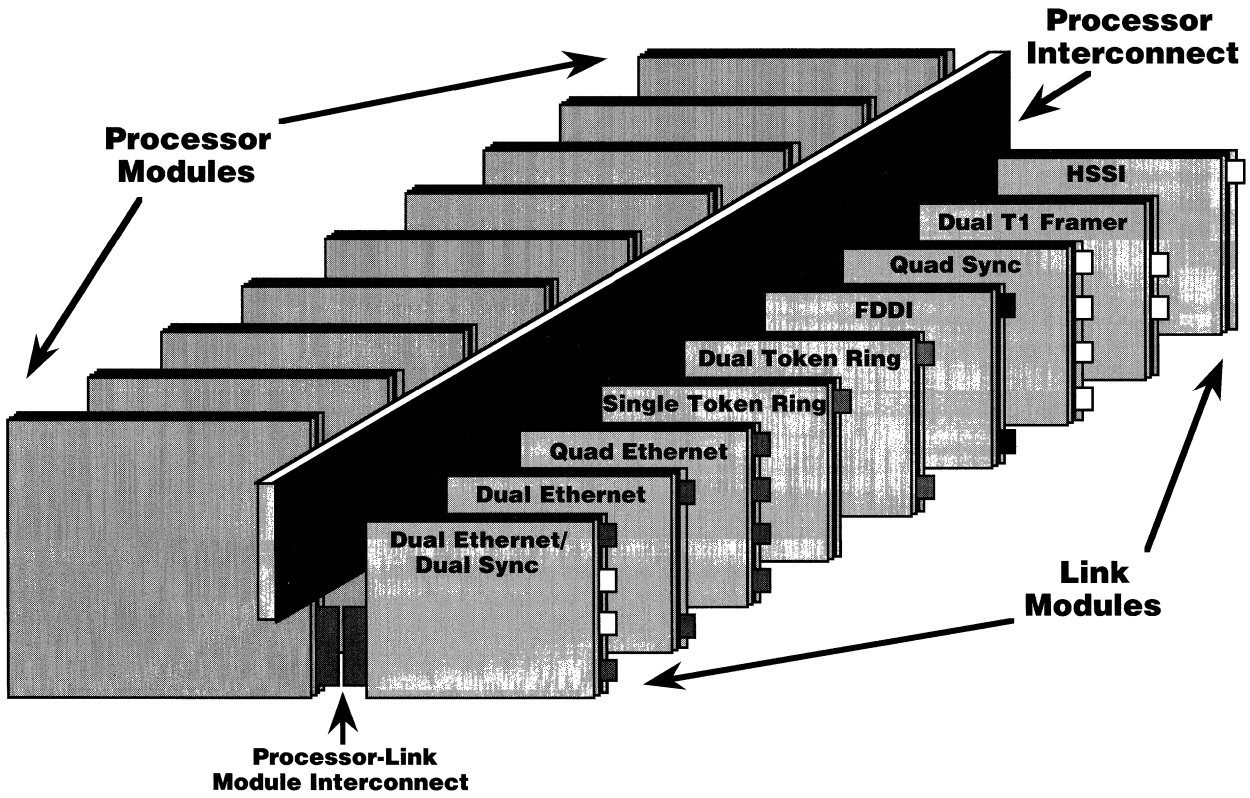
10. Requirements ranging from remote site or workgroup access to high-performance, highly available backbones require a broad range of packaging designs that support different maximum configurations of the symmetric multiprocessor architecture.

ARCHITECTURE OVERVIEW

In order to satisfy the critical need for scalable performance, high availability and flexible configuration, Wellfleet designed the symmetric multiprocessor architecture which is illustrated below. This architecture, used in all of Wellfleet's routers, employs three major architectural elements — link modules, processor modules, and processor interconnect.

Link modules provide the physical network interfaces to connect a wide variety of local and wide-area networks. Each link module is directly attached to a dedicated **processor module** to form an Intelligent Link Interface (ILI). Packets received on a link module network interface are passed to its attached processor module through a private, direct interconnect. The processor module determines the outbound network interface and either forwards the packets to another network interface on its link module or to another peer processor module via a mid-plane, high-speed **processor interconnect.** A receiving processor module then forwards the packets to the appropriate network interface on its attached link module.

Wellfleet's Symmetric Multiprocessor Architecture



ARCHITECTURE BENEFITS

The highest possible performance, availability and configurability are the advantages of this symmetric multiprocessor architecture.

Performance

Since every processor module in the system performs forwarding operations for all protocols, there is no central or master CPU resource involved in routing decisions and limiting performance as the system is expanded. Since each link module has its own dedicated processor module, aggregate system-level forwarding performance increases as the number of LAN or WAN interfaces increases.

Direct attachment of the processor module and link module further maximizes performance by ensuring that only packets traveling between different link modules traverse the processor interconnect.

Availability

If a single processor or link module fails in any system with multiple ILIs, the system continues to operate. Only those networks connected to the failed module are impacted.

The direct attachment of processor modules to link modules and to the processor interconnect in a mid-plane physical design increases system reliability by eliminating the need for internal cabling.

Lastly, the mid-plane design also allows for easy addition or removal of specific individual processor or link modules without removing others — even while the system is in operation.

Product Family Breadth and Scalability

A broad selection of link modules offers tremendous flexibility in meeting varied site-specific configuration requirements. The same link modules are supported throughout Wellfleet's product family.

ARCHITECTURE IN DETAIL

In addition to the architecture, the specific functional resources used in Wellfleet's routers also serve to maximize performance, availability and configuration.

Processor Module

The processor module includes the following major functional resources.

The CPU performs filtering/forwarding decisions, modifies packet headers as required, forwards packets to its directly attached network interfaces, updates routing and address databases, interprets management packets (e.g. IP ARP and ICMP packets, and DECnet HELLO packets), responds to SNMP requests, generates management packets, and operates other services such as special packet filters implemented for network security and/or performance. In order to support these functions, the CPU must have sufficient processing power, extremely low context switch latencies and an ability to rapidly access other processor module resources.

Local memory stores routing protocols, routing tables, address tables, management services and management information statistics used by or provided by the CPU located only on the same processor module.

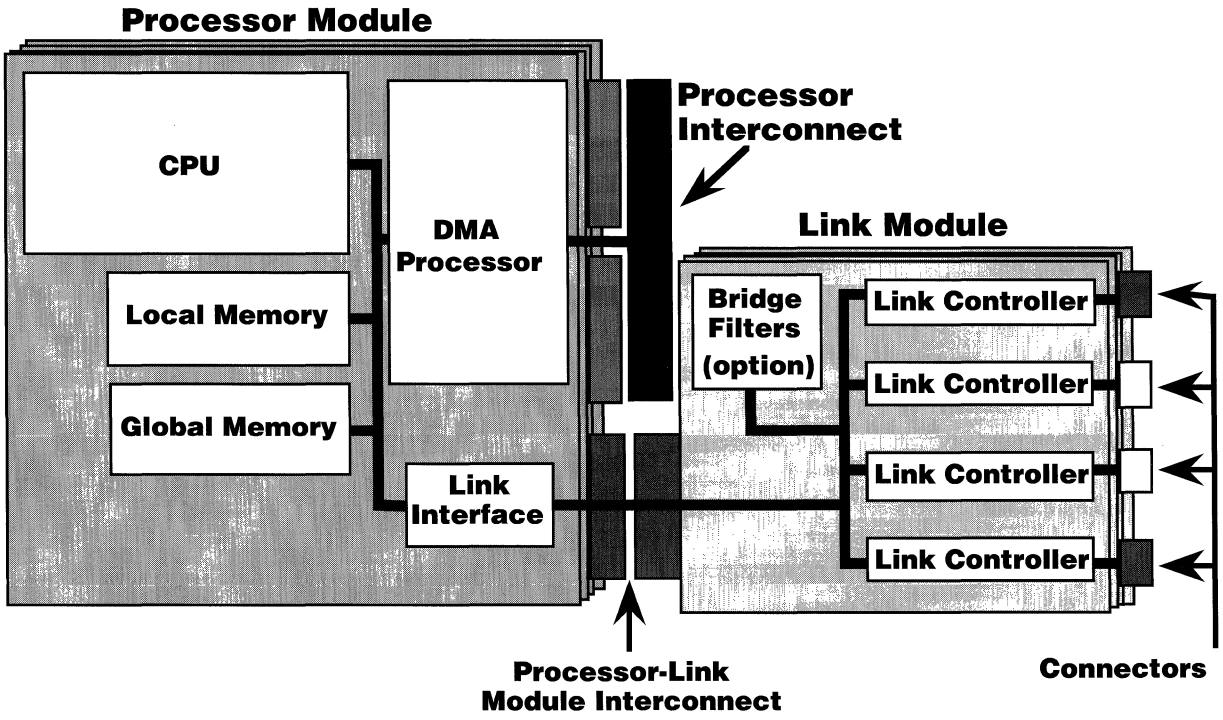
Global memory is the buffer space for transient data packets traveling from a link module to its attached processor module and between processor modules. It is called "global" because it is accessible from and visible to other processor modules. Packets are transferred (DMA'ed) into and out of global memory via link controllers (on link modules) and DMA processors — one on each of the processor modules.

The DMA processor with direct memory access capability moves forwarded packets between the global memories located on different processor modules.

The link interface provides connection to the attached link module.

Internal data paths, 32 bits wide, connect all of the above processor module resources to provide the highest possible bandwidth and lowest possible delay. Multiple paths between these resources enable concurrent operation of the resources (CPU and DMA processor for example) and ensure that there are no major gates interrupting or slowing the forwarding and processing of packets.

Intelligent Link Interface (ILI)



Link Module

The link module includes the following major resources:

Connectors provide the physical interface to specific networks (e.g. Ethernet, Token Ring, FDDI, synchronous). Cable options enable a single connector to attach to a wide variety of media standards.

Link controllers transfer packets between the physical network interface and global memory using their DMA capabilities. Link controllers are specific to the type of network interface and are capable of receiving packets at wire-speed rates.

Bridge filters, an option for Wellfleet's FDDI and Ethernet-based link modules, filter incoming packets so that CPU resources on the processor modules are preserved for packet forwarding. Wellfleet-developed gate arrays, implemented on a daughterboard, learn source addresses from incoming frames and build an address table in content addressable memory (CAM). For each incoming packet, the gate arrays consult the address table and filter (drop) those packets whose source and destination addresses reside on the same network. While many routers from other manufacturers use a shared microprocessor to both filter and forward packets, Wellfleet's Bridge Filters option offloads filtering responsibilities from the processor module. This enables the router to accommodate both large traffic bursts and sustained high-traffic loads without performance degradation.

Processor Interconnect

The processor interconnect is a high speed network which enables interprocessor communication among all processor modules in the router.

Availability, Reliability, and Maintainability Features

Availability features supporting the symmetric multiprocessor architecture include redundant power supplies, software image storage subsystems and processor interconnects. These options support no single point of system failure.

Reliability and maintainability features include module status lights, a mid-plane design with easy front and rear access (no internal cables), software upgradability via the network, a Flash EPROM card, or diskette (not ROM or PROM-based), and commonality of modules across a broad product family.

OPERATION

Inbound packets are first received from the network by a network-specific link controller. If an optional bridge filter is configured on the link module (Ethernet and FDDI only), the packets are either filtered (dropped) or accepted. Packets accepted are placed by the link controller in the global memory of its directly attached processor module. Each link controller has integrated DMA capability for rapid packet transfers.

Upon arrival in global memory, packets are retrieved by the CPU for appropriate routing. The CPU determines the outbound network interface, modifies the packet as required, and returns the packet to global memory. The result is one of the following three actions:

1. Drop packet (filter) by deleting from memory.

2. Forward packet to network interface on the directly attached link module. The link controller for the outbound network interface receives instructions from the CPU to pull the packets from global memory and send them out to the network.

3. Forward packet to network interface on a different link module. The DMA processor receives instructions from the CPU to send packets to another processor module and pushes the packets across the processor interconnect into the global memory of the processor module attached to the outbound network interface. The link controller for the outbound network interface pulls the packets from global memory and sends them out to the network.

The CPU's routing decisions are performed independently of other processor modules. Each processor module maintains independent routing and address databases for the protocols it has been configured to support in its local memory. As an individual processor module receives routing, address and management updates, it updates its own tables and then distributes the appropriate data to all other processor modules.

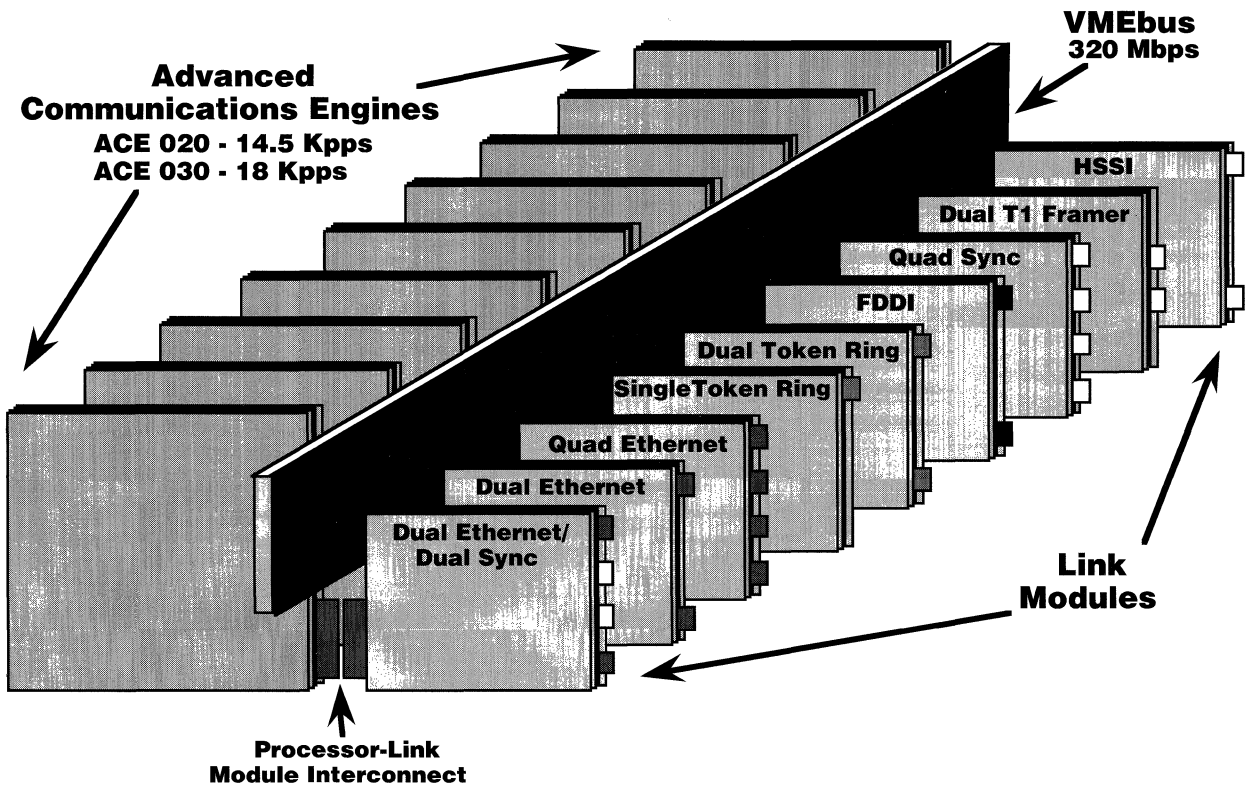
The simultaneous operation of the link controller, CPU and DMA processor optimizes overall performance. For example, the link controller places packets in global memory while the CPU updates its routing table in local memory and the DMA processor pushes a packet onto the processor interconnect. Performance is further optimized by ensuring that only packets destined for an outbound network interface on a different link module traverse the processor interconnect.

FN, LN & CN ARCHITECTURE

The Feeder Node (FN), Link Node (LN) and Concentrator Node (CN) meet user requirements for the widest range of applications including both cost-effective workgroup access and high-performance, highly available network hubs. Introduced in 1987 as the first systems to support concurrent multiprotocol routing and bridging in a single system and on a single network interface, they now support the latest network technologies such as FDDI, Frame Relay and SMDS. These systems utilize Motorola (MC) 68020 or 68030-based Advanced Communications Engine (ACE) processor modules and the standards-based VMEbus processor interconnect in their symmetric multiprocessor architecture.

The low-end FN is a cost-effective system for small network sites or workgroups. Based on a single ACE processor module, the FN supports up to four LAN/WAN interfaces and forwarding performance to 14,500 pps. The mid-range LN, an expandable platform for medium-size network sites, supports up to four ACE processor modules, 16 LAN/WAN interfaces and performance to 58,000 pps. The CN is designed for large network sites. It supports 13 ACE processor modules, 52 LAN/WAN interfaces and performance to 188,500 pps. The CN optionally supports redundant power supplies for maximum availability.

FN, LN & CN Architecture

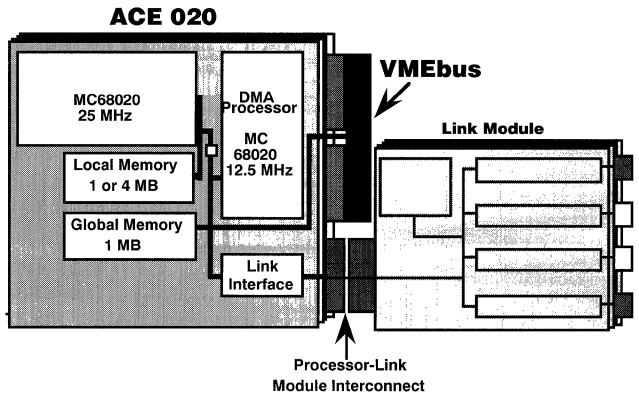


Advanced Communications Engines

ACE processor modules are available in two models – the ACE 020 and ACE 030. Both models can be used in all three systems to satisfy a range of network price and performance requirements. In the expandable LN and CN, the ACE 020 and ACE 030 can be mixed with each other in the same system to cost-effectively match forwarding performance to network bandwidth.

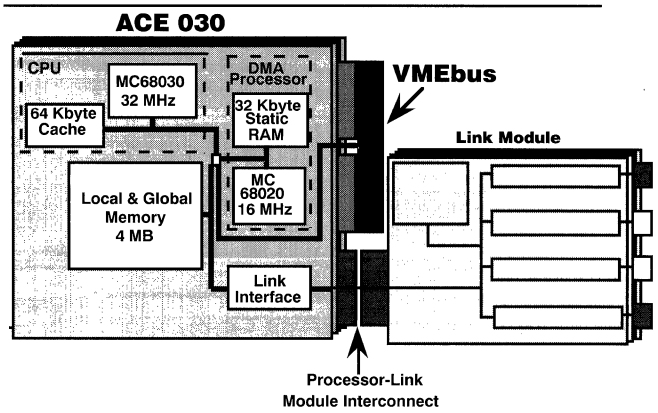
ACE 020 delivers forwarding performance of 14,500 pps. A 25 MHz MC68020 processor executes the multiprotocol router/bridge software for the network interfaces on the directly attached link module. A 12.5 MHz MC68020, operating as a high-speed DMA processor, transfers packets destined for other network interfaces across the VMEbus to other processor modules in the system. Packet buffering is performed by 1 Mbyte of global memory. Local memory, for storage of software and configuration information, is expandable from 1 to 4 Mbytes.

ACE 020



ACE 030 delivers forwarding performance of 18,000 pps. The ACE 030 employs a 32 MHz MC68030 as the routing processor and a 16 MHz MC68020 as the DMA processor. High performance is achieved through an on-board 64 Kbyte cache for instructions and data that facilitates rapid routing decisions. Additionally, the ACE 030 includes 4 Mbytes of memory for local program and global packet buffer storage.

ACE 030



VMEbus

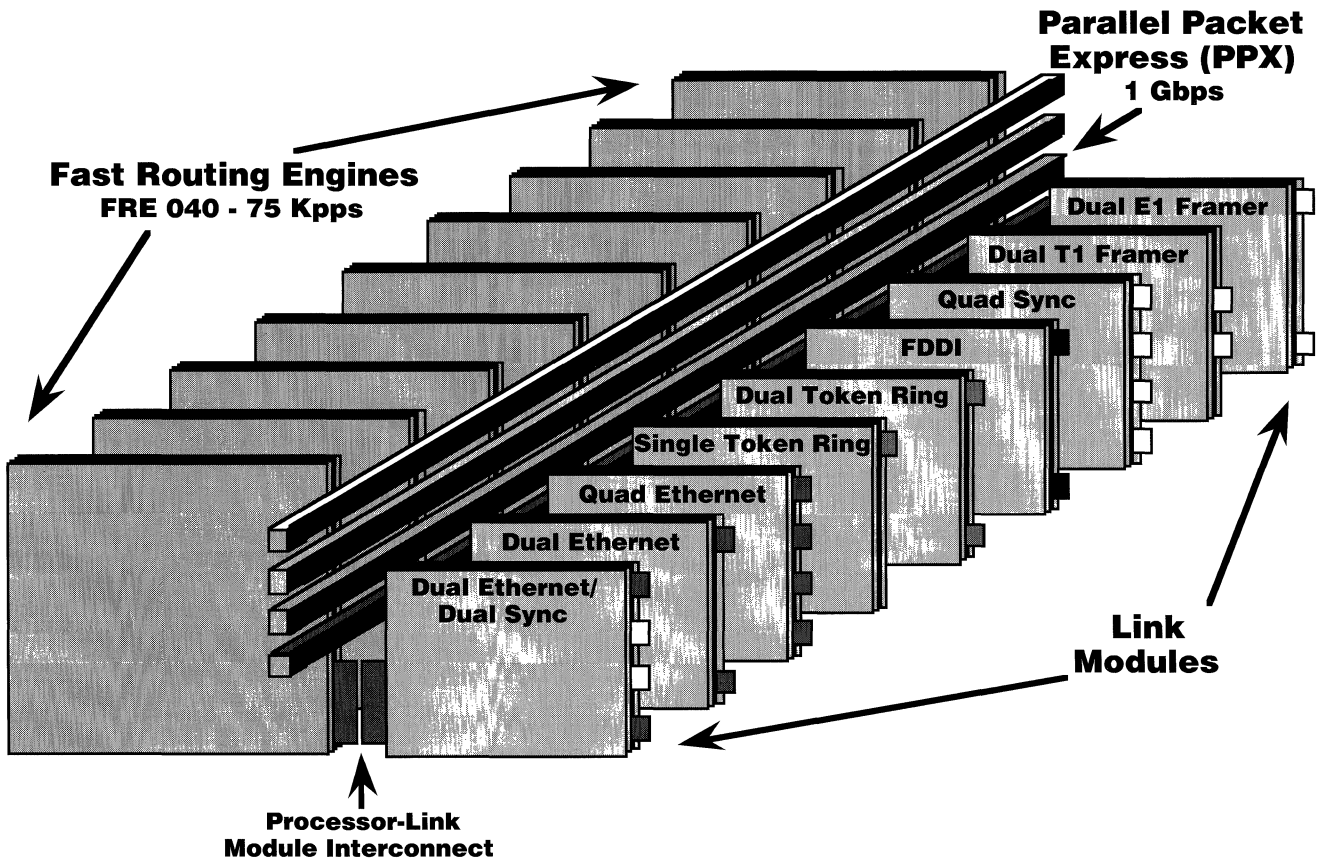
The VMEbus, an industry standard, provides aggregate bandwidth of 320 million bits per second (Mbps) to allow high-speed communication among multiple processor modules and support for high-performance network interfaces such as FDDI.

BLN AND BCN ARCHITECTURE

The Backbone Link Node (BLN) and Backbone Concentrator Node (BCN), Wellfleet's next-generation platforms, satisfy the high performance and/or availability requirements of the most demanding mission-critical backbone internetworks using, for example, FDDI, SMDS and/or SNA. Their symmetric multiprocessor architecture utilizes MC68040-based Fast Routing Engine (FRE) processor modules and Wellfleet's 1 Gbps Parallel Packet Express (PPX) processor interconnect to deliver industry leading performance and availability.

The BLN supports four FRE processor modules, 16 LAN/WAN interfaces (up to 4 FDDI) and 150,000 pps performance. The high-end BCN supports 13 FRE processor modules, 52 LAN/WAN interfaces (up to 13 FDDI) and system forwarding performance that scales to an industry-leading 480,000 pps. Several high availability features are offered for the BLN and/or BCN including redundant processor interconnects, redundant power supplies and redundant software image storage subsystems. A BCN configured with symmetric multiprocessors and all redundancy features has no single point of system failure.

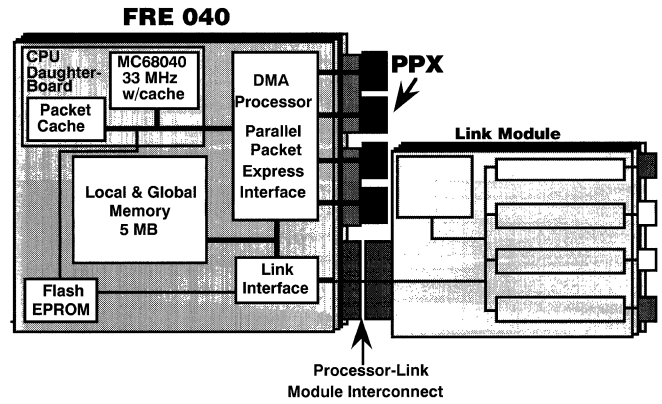
BLN & BCN Architecture



Fast Routing Engine

The Fast Routing Engine (FRE) delivers industry-leading forwarding performance of 75,000 pps. A 33 MHz MC68040 with an on-chip 4 Kbyte instruction and 4 Kbyte data cache, and a complementary, innovative, high-speed packet buffer cache is used as the routing processor. To keep pace with future microprocessor developments and protect user investments, the MC68040 is on a modular daughterboard that enables future processor upgrades. The PPXI, a patented ASIC, is the interface to the PPX processor interconnect and serves as the DMA processor. The FRE additionally includes 5 Mbytes of memory for local program and global packet buffer storage. To support rapid system re-boot and no single point of system failure, each FRE optionally supports 2 Mbytes of flash EPROM for non-volatile storage of software and configuration information.

Fast Routing Engine



Parallel Packet Express

The Parallel Packet Express (PPX), a 1 Gbps processor interconnect, uses four independent, redundant, dynamic load-sharing, 256 Mbps data paths to deliver high aggregate system performance as well as no single point of failure. Each FRE connects to all four paths and has the ability to select any of the paths. A specific path is selected randomly, on a per-packet basis, to ensure that traffic is evenly distributed across all available paths. If a single PPX data path becomes unavailable, the load is automatically distributed across the remaining paths.

LINK MODULES

Link modules provide the physical network interface to connect local and wide area networks. A broad selection of link modules offer tremendous flexibility in meeting varied site-specific configuration requirements (reference table). The same link modules are supported throughout Wellfleet's product family.

Link Modules

Ethernet-based
- Dual Ethernet*
- Quad Ethernet*
- Single Ethernet/Single Synchronous
- Single Ethernet/Dual Synchronous
- Dual Ethernet/Dual Synchronous*

Token Ring-based
- Single Token Ring
- Dual Token Ring
- Single Token Ring/Single Synchronous
- Single Token Ring/Dual Synchronous

FDDI
- Single FDDI (multi-mode)*
- Single FDDI (single-mode)*

Synchronous
- Quad Synchronous
- Single HSSI Interface
- Single Port T1 Framer (64 Kbps)
- Single Port T1 Framer (56 Kbps - DACS)
- Dual Port T1 Framer/Multiplexer (64 Kbps)
- Dual Port T1 Framer/Multiplexer (56 Kbps-DACS)
- Dual Port E1 Framer/Multiplexer

*also available with high-speed filter option

LAN Interfaces

Ethernet/802.3 interface supports IEEE 802.3 and Version 1.0/2.0 Ethernet frame formats. A unique, high-speed bridge filter option provides wire-speed filtering performance of 14,500 pps without impacting the processor module's forwarding performance. The interface includes a 15-pin AUI connector. A cable from the connector supports a variety of Ethernet media, including broadband, baseband, Starlan, fiber, 10BaseT and shielded twisted pair.

Token Ring/802.5 interface, IEEE 802.5-compatible with IEEE 802.2 Type 1 LLC support, is software-configurable to operate at 4 or 16 Mbps and offers a simple upgrade path as network performance requirements change. The interface supports IBM Type 1 and Type 3 cabling. A cable included with the interface provides a 9-pin D-subminiature connector to the Wellfleet system and a connector to either Type 1 or Type 3 cabling.

FDDI interfaces are offered for multimode or single-mode 100 Mbps FDDI LANs. The multimode interface supports 62.5/125 or 50/125 micron fiber at distances up to 2 km between stations. The single mode interface supports 9/125 micron fiber at distances up to 10 km. Both interfaces are compatible with the ANSI X3T9.5 Physical Medium Dependent (PMD), Physical Protocol (PHY), Media Access Control (MAC) and Station Management (SMT) standards. IEEE 802.1 Translation Bridging is supported for high performance communication with servers directly attached to an FDDI ring and interoperability with other 802.1-compliant bridges. FDDI-to-FDDI transparent bridging is also supported. An innovative bridge filter accelerator option provides wire-speed filtering performance of 500,000 pps. Offered without any other network interfaces, both FDDI link modules support a Class A dual attachment or a dual homing Class B single attachment. Both FDDI link modules include two Media Interface Connector (MIC) plugs as well as one RJ-11 connector for attachment to an optional external optical bypass unit.

WAN Interfaces

Synchronous interface optionally supports V.35, RS449/RS422 balanced, RS232 and X.21 connections. The specific connection is selected by using the cable option that supports the appropriate physical interface to attached DTE or DCE equipment. Both internal and external clocking are supported. A single synchronous interface operates from 1200 bps to a maximum of 52 Mbps full duplex. Aggregate bandwidth when multiple synchronous and/or LAN interfaces are operating on the same link module varies with the number and type of interfaces actually being configured.

Framed T1 interface is a 1.544 Mbps DSX-1 interface supporting D4 framing and DS-1 signaling for 64 Kbps or 56 Kbps DS-0s to access services such as Fractional T1 and Digital Access and Cross-connect System (DACS). An optional channel service unit (CSU) internal to the Wellfleet system provides direct connection to carrier-supplied circuits. The framed T1 interface can also be used to connect a D4-compatible PBX or video system to a Wellfleet system, allowing LAN, voice and video traffic to share the same backbone network.

Framed E1 interface is a 2.048 Mbps G.703 interface supporting G.704 framing and G.732 signaling for dividing an E1 circuit into its 32 component 64 Kbps channels. Supported services are comparable to those provided with the Framed T1 interface including access to available international PTT and Telecommunication Administration services and direct PBX and video system attachment.

LAN AND WAN PROTOCOLS

Every important LAN and WAN protocol is supported by Wellfleet. Complete routing and bridging support includes TCP/IP with OSPF, RIP and EGP; DECnet Phase IV; OSI with ES-IS and IS-IS; Xerox XNS; Novell IPX; Banyan VINES; AppleTalk; Transparent Bridge; Translation Bridge; Source Route Bridge; and comprehensive support for integrating IBM SNA environments. Private, public or hybrid networks can be built using X.25, Frame Relay, SMDS, and Point-to-Point Protocol.

COMPREHENSIVE NODE AND NETWORK MANAGEMENT

Comprehensive node and network management is essential to successful mission-critical internetworks. Wellfleet fully supports SNMP — the industry standard for internetwork management. Every Wellfleet node contains a MIB II-compliant SNMP agent with numerous enterprise-specific extensions. Wellfleet supports all SNMP protocol data units (PDUs) including SNMP SET for dynamic configuration and control.

Wellfleet's nodes are managed efficiently from popular general-purpose SNMP network management systems such as HP OpenView, SunNet Manager, IBM AIX NetView/6000, Cabletron Spectrum, and Digital DECmcc.

Wellfleet Site Manager is a platform-independent, SNMP-based application designed expressly for simplifying Wellfleet node management. It features an intuitive, windows-based point-and-click user interface that hides the underlying complexity of SNMP. Site Manager offers central configuration management that simplifies network setup and expansion, real-time operations and monitoring, and real-time event and fault monitoring for efficient problem identification and isolation. Site Manager operates on popular computing platforms including DOS-based 386 PCs running MS Windows, and Sun Microsystems' SPARCstations running the X Window System, OpenWindows, or Motif.

NOTES

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