ALADDiN™

M1533

Mobile Southbridge

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Please contact ALi applications department at 408-467-7456 to verify that all information is current before beginning a design using this datasheet.

M1533: PCI-to-ISA Bus Bridge

Section 1 : Introduction

1.1 Features

- **Provides a bridge between the PCI bus and ISA bus for both Pentium and Pentium Pro systems**

- **PCI interface**
  - Supports PCI Master and Slave Interface
  - Supports PCI Master and Slave Initiated Termination
  - PCI spec. 2.1 Compliant (Delayed Transaction Support)

- **Buffers Control**
  - 8-byte Bi-directional Line Buffers for DMA/ISA Memory Read/Write Cycles to PCI Bus.
  - 32-bit Posted Write Buffer for PCI Memory Write and I/O Data Write (for Sound Card) to ISA bus.

- **Provides steerable PCI interrupts for PCI device plug-and-play**
  - Up to 8 PCI Interrupts Routing
  - Level to Edge Trigger Transfer

- **Enhanced DMA Controller**
  - Provides 7 Programmable Channels, 4 for 8-bit Data Size, 3 for 16-bit Data Size
  - 32-bit Addressability
  - Provides Compatible DMA Transfers
  - Provides Type F Transfers

- **Interrupt Controller**
  - Provides 14 Interrupt Channels
  - Independent Programmable Level/Edge Triggered Channels

- **Counter/Timers**
  - Provides 8254 Compatible Timers for System Timer, Refresh Request, Speaker Output Use

- **Distributed DMA Supported**
  - 7 DMA Channels can be Arbitrarily Programmed as Distributed Channel
- **Serialized IRQ Supported**
  - Quiet/Continuous Mode
  - Programmable (Default 21) IRQ/DATA Frames
  - Programmable START Frame Pulse Width

- **Plug-and-Play Port Supported**
  - 1 Programmable Chip Select
  - 2 Steerable Interrupt Request Lines

- **Built-in Keyboard Controller**
  - Built-in PS2/AT Keyboard and PS2 Mouse Controller

- **Supports up to 256 KB ROM Size Decoding**
- **Supports Positive/Subtractive Decode for ISA Device**

- **PMU Features**
  - Full Support for ACPI and OS Directed Power Management
  - CPU SMM Legacy Mode and SMI Feature Supported
  - Supports Programmable STPCLKJ : Throttle/CKONSTP/CKOFFSTP Control
  - Supports I/O Trap for I/O Restart Feature
  - PMU Operation States :
    -- ON
    -- Standby
    -- Sleeping (Power On Suspend)
    -- Suspend (Suspend to DRAM)
    -- Suspend to HDD
    -- Soft-Off
    -- Mechanical Off
  - APM State Detection and Control Logic Supported
  - Global and Local Device Power Control Logic
  - 10 Programmable Timers : Standby/ LB/ LLB/ APMA/ APMB/ Global_Display/ Primary_IDE/ Secondary_IDE/ SIO&Audio/ Programmable IO Region
  - Provides System Activity and Display Activity Monitorings, including
    -- Video
    -- Audio
    -- Hard Disk
    -- Floppy
    -- Serial Ports
    -- Parallel Port
    -- Keyboard
    -- 6 Programmable I/O Groups
    -- 3 Programmable Memory Spaces

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- Provides Hot Plugging Events Detection
  -- CRT Connector
  -- AC Power
  -- Docking Insert
  -- Eject
  -- Setup Button
  -- Hot Key Press
- Multiple External Wakeup Events of Standby Mode
  -- Power Button
  -- Cover open
  -- Modem Ring
  -- RTC alarm
  -- EXTSW
  -- DRQ2

- Suspend Wakeup Detected
  -- Hot key
  -- Modem Ring
  -- RTC alarm
  -- Cover open
  -- Docking insert
  -- Power Button
  -- USB events
  -- IRQ
  -- EJECT
  -- ACPWR
  -- GPIO[19:16] event
- Two-Level Battery Warning Monitors
- Thermal Alarm Supported
- Clock Generator Control Logic Supported
  -- CPUCLK Stop Control
  -- PCICLK Stop Control
  -- PLL Stop Control
  -- Down Frequency Control
- L2 Cache Power Down and PCI CLKRUN Control Logic Supported
- 21 General Purpose Inputs Signals, 24 General Purpose Output Signals. 20 General Purpose Input/Output Signals
- 16 External Expandable General Purpose Inputs, 16 External Expandable General Purpose Outputs
- LCD Control
- All Registers Readable/Restorable for Proper Resume from Suspend State

- **Built-in PCI IDE Controller**
  Supports Ultra 33 Synchronous DMA Mode Transfers up to Mode 2 Timing (33 Mbytes/sec)
  Supports PIO Modes up to Mode 5 Timings, and Multiword DMA Mode 0,1,2 with Independent Timing of up to 4 Drives
  Integrated 10 x 32-bit Read Ahead & Posted Write Buffers for Each Channel (Total: 20 DWORDs)
  Dedicated Pins of ATA Interface for each Channel
  Supports Tri-state IDE Signals for Swap Bay

- **USB interface**
  One Root Hub with two USB ports based on OpenHCI 1.0a Specification
  Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) Serial Transfer
  Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse

- **SMBus Interface**
  · System Management Bus Interface which meets the V1.0 Specification

- **External APIC Interface Supported**

- **328-pin (27mmx27mm) BGA Package**

Table of Contents :

1.2 Functions

The M1533 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. The M1533 has Integrated System Peripherals (ISP) (2 x 82C59 and Serial interrupt, 1 x 82C54), advanced features (Type F and Distributed DMA) in the DMA controller (2 X 82C37), PS2 Keyboard/Mouse controller, 2-channel dedicated IDE Master Controller with Ultra-33 specification, System Management Bus (SMB), and 2 OpenHCI 1.0a USB ports. The ACPI (Advanced Configuration and Power Interface) and PCI 2.1 (Delayed Transaction & Passive Release) specification have also been implemented. Furthermore, this chip supports the Advanced Programmable Interrupt Controller (APIC) interface for Multiple-Processors system. M1533 also supports the deep flexible green function and provides the best solution for the best green system. It can connect to the ALi Pentium North Bridge (M1521/M1531/M1541) and also the ALi Pentium Pro North Bridge (M1615) to provide the best system solution.

One eight-byte bi-directional line buffer is provided for ISA/DMA Master memory read/writes. One 32-bit wide posted write buffer is provided for PCI memory write & I/O write (for Audio) cycles to the ISA bus. Provides a PCI to ISA IRQ routing table, and level to edge trigger transfer.

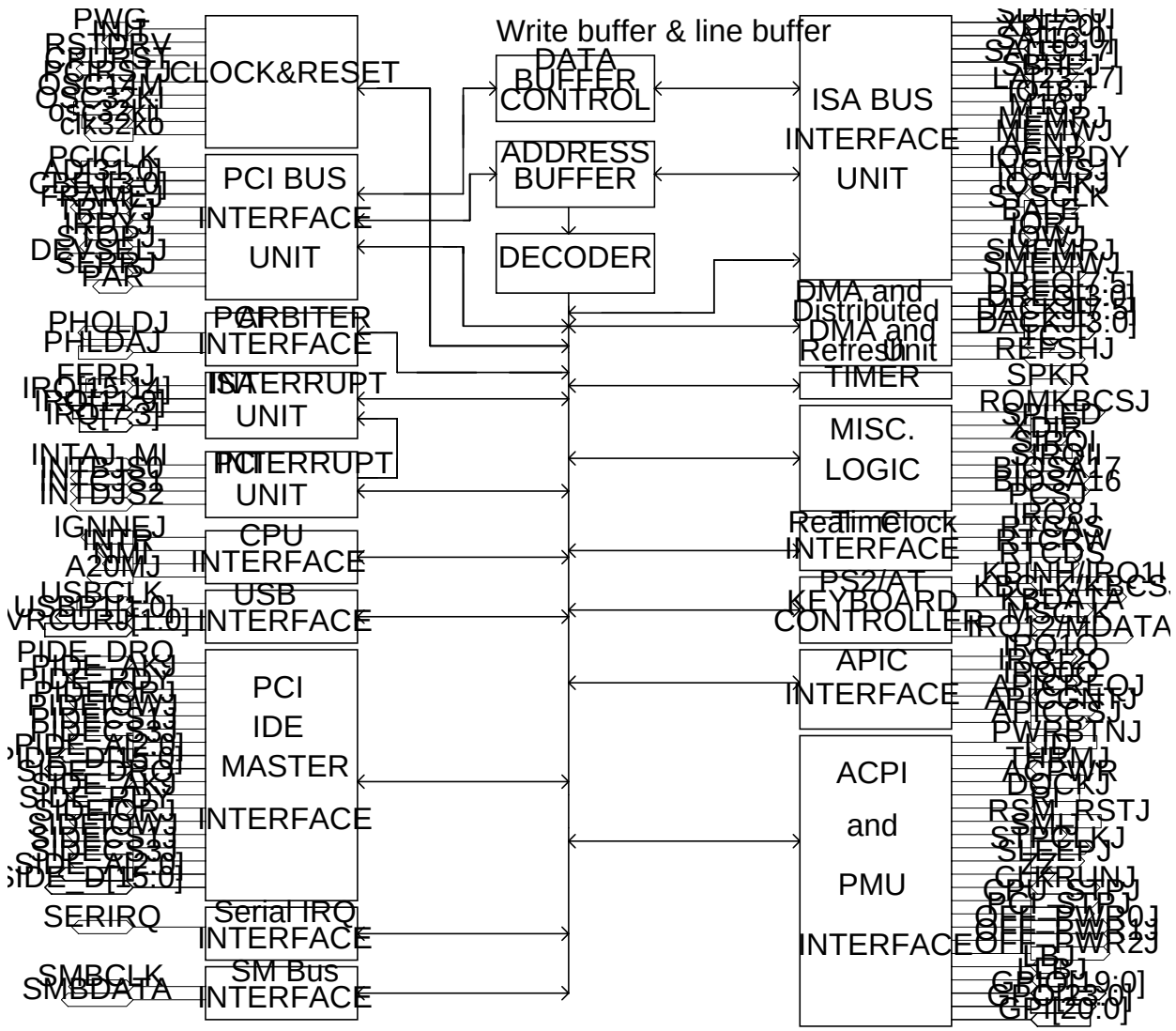
The chip provides 2 extra IRQ lines and 1 programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts.

The on-chip IDE controller supports two separate IDE connectors for up to 4 IDE devices providing an interface for IDE hard disks and CD ROMs. The Ultra 33 specification (which supports the 33M bytes per second transfer rate) has been implemented at this IDE controller. The ATA bus pins & the Buffer (Read Ahead and Posted Write) are all dedicated for separate channel to improve the performance of IDE Master.

The M1533 supports Super Green function for Intel and Intel compatible CPUs. It implements SMI or SCI (System Controller Interrupt) to meet the ACPI specification. It also meets the requirement for OnNow Design Initiative. The M1533 supports powerful power management for power saving including On, Standby, Sleeping, SoftOff, Mechanical Off State. To control the CPU power consumption, it provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control. Also, the M1533 can support the most flexible system clock design: it can be programmed to stop the CPU Clock, PCI Clock, the Clock cell, or to reduce the Clock frequency. The PBSRAM (Pipelined Burst SRAM) doze mode is also supported.

The M1533 is a highly integrated chip that includes PS2 Keyboard/Mouse controller, SMBus, 2 OpenHCI 1.0a USB ports, and dedicated GPIO (General Purpose Input/Output) pins. The Notebook or the Desktop system designer can use this chip to implement the best green and cost/performance system.

1.3 M1533 Functional Block Diagram



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Section 2 : Pin Description

2.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	AD21	AD18	CBEJ2	STOPJ	AD14	AD9	AD5	AD0	SIDED7	SIDED10	SIDED2	SIDED15	SIDEAKJ	SIDECS3J	PIDED6	PIDED10	PIDED3	NC	NC
B	NC PIDED14	AD22	AD19	AD16	**DEVSELJ**	AD15	AD10	AD6	AD1	PHLDJ	SIDED5	SIDED12	SIDED0	**SIDEIRDY**	SIDECS1J	**PIDED9**	PIDED11	PIDED13	PIDED2	
C	CBEJ3 PIDED0	AD23	AD20	AD17	TRDYJ	CBEJ1	AD11	AD7	AD2	PHLDAJ	SIDED9	SIDED3	SIDED14	SIDEIORJ	SIDEA2	PIDED5	PIDED4		PIDED1	PIDED15
D	AD26 PIDEA2	AD25	AD24	PCIRSTJ	IRDYJ	PAR	AD12	CBEJ0	AD3	CLKRUNJ	SIDED6	SIDED11	SIDED1	**SIDEIOWJ**	SIDEA0	PIDED8	PIDED12		PIDEA1	PIDEA0
E	AD29	AD28	AD27	AD30	FRAMEJ	SERRJ	AD13	AD8	AD4	PCICLK	SIDED8	SIDED4	SIDED13	**SIDEDRQ**	SIDEA1	PIDED7	PIDEAKJ	PIDECS1J	PIDECS3J	INTR
F	USBCLK	GPO8	AD31	INTAJ	INTBJ	VCC_B								VCC_D	VCC_E	PIDEIOWJ	PIDEIRDY	NMI	SMIJ	IGNNEJ
G	USBP0-	USBP0+	GPO4	INTCJ	INTDJ	VCC_B					**M1533**				VCC_3C	PIDEDRQ	PIDEIORJ	CPURST	A20MJ	INIT
H	USBP1-	USBP1+	GPI3	GPO3	GPO2											IRQ13	STPCLK	SMBDATA	SMBCLK	RI
J	SD7	RSTDRV	IOCHKJ	GPI1	GPI0					GND	GND	GND	GND			GPO1	GPO20	**GPIO19**	GPIO18	GPIO17
K	SD5	IRQ9	SD6	MSCLK	MSDATA					GND	GND	GND	GND			LLBJ	DOCKJ	GPIO16	GPIO15	GPIO14
L	SD3	DREQ2	SD4	KBCLK	KBDATA					GND	GND	GND	GND			IRQ8J	SUSTAT1J	PWRBTNJ	GPIO13	GPIO12
M	IOCHRDY	SD0	SD1	NOWSJ	SD2					GND	GND	GND	GND			PWG	HOTKEYJ	**RSMRSTJ**	LBJ	LID
N	IOWJ	SA19	**SMEMRJ**	AEN	SMEMWJ										VDD5S	SIRQI	SIRQII	OSC32KII	OSC32KI	OSC32KO
P	SA16	DACKJ3	SA17	IORJ	SA18	VCC_A									VCC_C	GPO19	GPO18	GPO23	GPO22	GPO21
R	DREQ1	SA14	**DACKJ1**	SA15	DREQ3	VDD5	VCC_A							**Vcc_3A**	VCC_A	GPO17	GPO16	GPO15	GPO14	GPO13
T	REFSHJ	SA13	IRQ6	IRQ4	**DACKJ2**	BALE	LA23	LA20	DACKJ0	MEMWJ	DREQ6	ROMKBCSJ	RTCAS	**RTCRW**	IRQ1I	GPO12	GPO11	GPO10	GPO9	GPO7
U	SA12	IRQ7	IRQ5	IRQ3	TC	OSC14M	IRQ10	IRQ15	LA17	**DREQ5**	SD10	SD12	RTCDS	XD0	XD4	EJECT	GPIO11	GPO6	GPO5	GPO0
V	SYSCLK	SA10	SA8	SA5	SA2	M16J	LA22	LA19	DREQ0	SD8	DACKJ7	SD13	SPKR	XD1	XD5	ACPWR	GPI6	GPIO8	GPIO9	GPI010
W	SA11	SA9	SA7	SA4	SA1	SBHEJ	IRQ11	IRQ14	MEMRJ	**DACKJ6**	SD11	SD14	SPLED	XD2	XD6	SETUPJ	GPI4	GPI7	GPI8	NC

TOP VIEW

Figure 2-1. M1533 Pin Diagram

Note : Please refer to p.157 for bottom view

2.2 Pin Description Table :

Pin Name	Type	Description
Clock & Reset Unit :		
PWG	I-Group C Schmitt	**Power-Good Input.** This signal comes from the power supply to indicate that power is available and stable. The de-assertion of this input will enable the leakage control circuit between Soft-off (Suspend to Disk) resume circuit and no power circuit.
PCICLK	I-Group B	**PCI Clock for Internal PCI Interface.** This is an input PCI clock, it should always be running at ON, STANDBY, SLEEP (Power-On Suspend) state. When CLKRUNJ is active, this clock should always keep on running. Internal PCI states machine and ISA state machine will use this clock.
OSC14M	I-Group A	**14.318MHz Clock Input.** This input clock will be used for Power Management timer, M8254 timer, SM bus base frequency and ISA state machine.
OSC32KI	I-Group C	**32 KHz Oscillator Input1.** This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The M1533 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a crystal is not used, an external 32 KHz clock input should connect to this pin.
OSC32KII	I-Group C	**32 KHz Oscillator Input2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The M1533 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, this pin should be floated.
CLK32KO	O-Group C 2.4/2.4 mA	**32 KHz Clock Output for DRAM Refresh.** At ON, STANDBY, SLEEP (Power On Suspend), SUSPEND (Suspend to DRAM) states, the output will send to Memory controller, to support DRAM refresh clock. At Soft off and Suspend to Disk states, the output will drive low to avoid leakage current.
USBCLK	I-Group B	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
PCI Bus Interface Unit :		
PCIRSTJ	O-Group B 12/16 mA	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.
AD[31:0]	I/O Group B 12/16 mA	**Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBEJ[3:0]	I/O Group B 12/16 mA	**Bus Command and Byte Enable.** During address phase, CBEJ[3:0] define the Bus Command. During data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	I/O Group B 12/16 mA	**Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.

Pin Description Table (continued) :

Pin Name	Type	Description
PCI Bus Interface Unit:		
TRDYJ	I/O Group B 12/16 mA	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
IRDYJ	I/O Group B 12/16 mA	**Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
STOPJ	I/O Group B 12/16 mA	**Cycle stop request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
DEVSELJ	I/O Group B 12/16 mA	**Device Select.** This signal indicates that the target device has decoded the address as its own cycle. This pin is an output pin when M1533 acts as a PCI slave has decoded address as its own cycle including subtractive decoding.
SERRJ	I-Group B	**System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERRJ is sampling low, M1533 will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O Group B 12/16 mA	**Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBEJ[3:0]. When M1533 acts as a PCI master, it drives PAR one PCI clock after address phase for read/write transaction and one PCI clock after data phase for write transaction. When the M1533 acts as a target, it drives PAR one PCI clock after data phase for PCI master read transaction.
PHLDAJ	I-Group B	**PCI Bus Ownership Acknowledge.** When PCI bus arbiter asserts this pin, M1533 has owned the PCI bus.
PHOLDJ	O-Group B 4/4 mA	**PCI Bus Ownership Request.** M1533 requests the ownership of the PCI bus from the PCI bus arbiter on the North Bridge. M1533 will assert this signal on behalf of the ISA Master, DMA Device, IDE Master, and the USB Master.
INTAJ_MI	I-Group B	**PCI INTA.** PCI interrupt input A or PCI interrupt polling input. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTAJ when 4 PCI Interrupts are supported, or connects to the 74F181 encoded output to support the 8 PCI Interrupts polling mode.
INTBJS0	I/O Group B Schmitt 4/4 mA	**PCI INTB.** PCI interrupt input B or polling select_0 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTBJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 0 to support the 8 PCI Interrupts polling mode.
INTCJS1	I/O Group B Schmitt 4/4 mA	**PCI INTC.** PCI interrupt input C or polling select_1 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTCJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 1 to support the 8 PCI Interrupts polling mode.
INTDJS2	I/O Group B Schmitt 4/4 mA	**PCI INTD.** PCI interrupt input D or polling select_2 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTDJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 2 to support the 8 PCI Interrupts polling mode.

Pin Description Table (continued) :

Pin Name	Type	Description
CPU interface :		
INIT	O-Group E 2.4/2.4 mA	**CPU Initialize Interrupt.** CPU cold & warm reset. When CPU is Pentium Pro, this signal is low active. Otherwise, this signal is high active. When power on, KBC RC, port 92 RC, shutdown all will trigger INIT active.
CPURST	O-Group E 2.4/2.4 mA	**CPU Cold Reset.** When power turn on, this reset signal will be asserted, and then will become de-asserted until 4 ms after PWG becomes high.
IGNNEJ	O-Group E 2.4/2.4 mA	**Ignore Error.** This pin is used as the Ignore Numeric coprocessor Error.
INTR	O-Group E 2.4/2.4 mA	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt.
NMI	O-Group E 2.4/2.4 mA	**Non-Maskable Interrupt to CPU.** This is generated by the ISA Parity error (IOCHKJ assertion), PCI Parity error or DRAM Parity error (SERRJ assertion), and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt.
A20MJ	O-Group E 2.4/2.4 mA	**CPU A20 Mask.** This is the CPU Address line 20 mask signal.
FERRJ/ IRQ13	I-Group E	**Floating Point Error.** FERRJ input to generate IRQ13. When Coprocessor interface is disabled through configuration register Index-43h bit 6 setting, the function of this pin is IRQ13.
ISA Bus Interface Unit :		
IRQ[15:14], IRQ[11:9], IRQ[7:3]	I/O Group A Schmitt 9.6/9.6 mA	**Interrupt Request.** The Interrupt Request lines are directly from the ISA Bus, from the PCI Interrupt Routing from serialized IRQ, or from the steerable Interrupt pins. The M1533 will also drive the interrupt pins if the source is not from the ISA bus to support the APIC interface.
RSTDRV	O-Group A 12/16 mA	**ISA Bus reset.** This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.
SD[15:8]	I/O Group A 12/12 mA	**ISA High Byte Slot Data Bus.** These pins should connect to the ISA High Byte Slot Data Bus.
XD[7:0]	I/O Group A 12/12 mA	**XD Data Bus.** When the SD[7:0] pins are defined as the GPIO[7:0] pins, these pins can be used to drive SD[7:0] if TTL LS245 is used as a buffer. M1533 signal XDIR will control this buffer.
SD[7:0]/ GPIO[7:0]	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus or General Purpose I/O.** When external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL, these pins are used as the GPIO pins for green control. Otherwise, these pins are SD[7:0]. No external LS245 is required.
SA[19:17]	O-Group A 12/12 mA	**ISA Slot Address Bus A19-A17.** These pins should connect to the ISA System Address Bus.
SA[16:0]	I/O Group A 12/12 mA	**ISA Slot Address Bus A16-A0.** These pins should connect to the ISA System Address Bus.
SBHEJ	I/O Group A 12/12 mA	**ISA Byte High Enable.** This pin should connect to the ISA System Byte High Enable pin.
LA[23:17]	I/O Group A 12/12 mA	**ISA Latched Address Bus.** They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.

Pin Description Table (continued) :

Pin Name	Type	Description
ISA Bus Interface Unit :		
IO16J	I -Group A	**ISA 16 Bit I/O Device Indicator.** This is an input and will be driven by the device if the ISA I/O cycle is a 16-bit access.
M16J	I/O Group A 12/20 mA	**ISA 16 Bit Memory Device Indicator.** This pin will be driven by the device or by the M1533 if the ISA Memory cycle is a 16-bit access.
MEMRJ	I/O Group A 12/12 mA	**ISA Memory Read.** This signal is an output when the M1533 is the ISA Bus master, or an input during ISA master cycle.
MEMWJ	I/O Group A 12/12 mA	**ISA Memory Write.** This signal is an output when the M1533 is the ISA Bus master, or an input during ISA master cycle.
AEN	O-Group A 12/12 mA	**ISA I/O Address Enable.** This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.
IOCHRDY	I/O Group A 12/20 mA	**ISA System Ready.** This signal is an output during ISA master cycle, or an input when the M1533 is the ISA Bus master.
NOWSJ	I-Group A	**ISA Zero Wait-State for Input.** This input signal will terminate the CPU to ISA command instantly.
IOCHKJ	I-Group A	**ISA Parity Error.** M1533 will generate NMI to CPU when this signal is asserted.
SYSCLK	O-Group A 12/12 mA	**ISA System Clock.** This output is generated by the PCI clock and is used as the ISA system clock.
BALE	O-Group A 12/12 mA	**Bus Address Latch Enable.** BALE will be asserted throughout DMA, ISA master , and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.
IORJ	I/O Group A 12/16 mA	**ISA I/O Read.** This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
IOWJ	I/O Group A 12/12 mA	**ISA I/O Write.** This signal is input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
SMEMRJ	O-Group A 12/12 mA	**ISA System Memory Read.** This signal indicates that the memory read command is below 1M Byte address.
SMEMWJ	O-Group A 12/12 mA	**ISA System Memory Write.** This signal indicates that the memory write command is below 1M Byte address.
DREQ[7:5], DREQ[3:0]	I-Group A Schmitt	**DMA Request Signals.** These are inputs from the DMA Device or ISA Master Request. The M1533 will combine the DMA request, ISA Master request, IDE Bus Master request, Distributed DMA controller request, and USB Master request to generate the PHOLDJ to the PCI Arbiter.
DACKJ[7:5], DACKJ[3:0]	O-Group A 9.6/9.6 mA	**DMA Acknowledge Signals.** After the M1533 has got the PCI Bus grant (PHLDAJ), the internal arbiter will assert the DMA acknowledge signal to the DMA Device Request.
TC	O-Group A 12/12 mA	**DMA End of Process.** This signal will be asserted after the DMA Device has ended the transaction.
REFSHJ	I/O Group A 12/20 mA	**ISA Refresh Cycle.** This signal is input during ISA master cycle, and an output when the M1533 is the ISA Bus master.

Pin Description Table (continued) :

Pin Name	Type	Description
Miscellaneous Logic :		
SPKR	O-Group A 4/4 mA	**Speaker Output.** This pin is used to control the Speaker Output and should connect to the Speaker.
RTCAS	O-Group A 4/4 mA	**RTC Address Strobe.** This pin is used as the RTC Address Strobe and should connect to the RTC.
RTCRW	O-Group A 4/4 mA	**RTC Write Strobe.** This pin is used as the RTC Read/Write Command and should connect to the RTC. The M1533 will drive the RTC command through dedicated pin instead of the 74F32 decode to save the system cost.
RTCDS	O-Group A 4/4 mA	**RTC Data Strobe.** This pin is used as the RTC Data Strobe and should connect to the RTC.
SPLED	O-Group A 4/4 mA	**Speed LED Output.** This pin is used to control the Speed LED Output and should connect to LED.
ROMKBCSJ	O-Group A 4/4 mA	**ROM/Keyboard Chip Select.** This pin is the ROM chip select and is the Keyboard chip select also when internal KBC is disabled.
SERIRQ/ GPI[2]	B/I Group A 12/16 mA	**Serial Interrupt Request or General Purpose Input.** This pin is used to support the serial interrupt protocol or as a General Purpose Input.
SIRQI	I-Group A Schmitt	**Steerable IRQ Input1.** This is a steerable Interrupt input; M1533 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
SIRQII	I-Group A Schmitt	**Steerable IRQ Input2.** This is a steerable Interrupt input; M1533 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
IRQ8J	I-Group C Schmitt	**RTC Interrupt Input.** This is the RTC Interrupt input. This pin belongs to the Power Group C, and it can support the RTC Alarm function during Soft-off or Suspend state.
XDIR/ GPO[12]	O-Group A 4/4 mA	**XD Bus Direction Control or General Purpose Output.** When external XD bus is designed on motherboard, this pin is X-bus direction control. Otherwise, this pin is a general purpose output. Refer to Section 2.6.
KBINH/ IRQ1I	I/O Group A Schmitt 12/24 mA	**Keyboard Inhibit or Interrupt One Input.** This pin will be the Keyboard Inhibit input when internal KBC is enabled. Otherwise, it will be the IRQ1 input.
IRQ1O/ GPO[13]	O-Group A 4/4 mA	**IRQ1 Output or General Purpose Output.** When both external APIC and internal KBC are enabled, this pin is IRQ1 output. Otherwise, it is a general purpose output.
KBCLK/ GPI[9]	I/O Group A Schmitt 12/24 mA	**Keyboard Clock or General Purpose Input.** This pin is the Keyboard interface Clock when internal KBC is enabled. Otherwise, it is a general-purpose input.
KBDATA/ GPI[10]	I/O Group A Schmitt 12/24 mA	**Keyboard data or General Purpose Input.** KB interface DATA output when internal KBC is enabled. Otherwise, this pin is a general purpose input.
MSCLK/ GPI[11]	I/O Group A Schmitt 12/24 mA	**Mouse Clock or General Purpose Input.** Mouse clock output when internal PS2 Keyboard is enabled. Otherwise, this pin is a general purpose input.

Pin Description Table (continued) :

Pin Name	Type	Description
Miscellaneous Logic :		
MSDATA/ IRQ12I	I/O Group A Schmitt 12/24 mA	**Mouse Data or Interrupt Line 12 Input.** Mouse data output when internal PS2 Keyboard is enabled. Otherwise, this pin is the IRQ12 input.
IRQ12O/ GPO[14]	O-Group A 4/4 mA	**Interrupt Line 12 Output or General Purpose Output.** When both external APIC and internal KBC are enabled, this pin is IRQ12 output. Otherwise, this pin is a general purpose output.
IRQ0/ GPO[15]	O-Group A 4/4 mA	**Interrupt Line 0 Output or General Purpose Output.** This pin is the Interrupt request 0 output when external APIC mode is enabled. Otherwise this pin is a general purpose output.
APICREQJ/ GPI[8]	I -Group A	**APIC Request Input or General Input.** This pin connects to the APIC Chip Request Line when external APIC mode is enabled. Otherwise, this pin is a general purpose input.
APICCSJ/ GPO[16]	O-Group A 4/4 mA	**APIC Chip Select or General Purpose Output.** This pin connects to the APIC Chip Select Line when external APIC mode is enabled. Otherwise, this pin is a general purpose output.
APICGNTJ/ GPO[17]	O-Group A 4/4 mA	**APIC Grant Output or General Purpose Output.** This pin connects to the APIC Chip Grant Line when external APIC mode is enabled. Otherwise, this pin is a general purpose output.
BIOSA17/ GPO[19]	O-Group A 4/4 mA	**ROM Address 17 or General Purpose Output.** This pin is the ROM A17 control when 2M ROM is used, or it is a general purpose output.
BIOSA16/ GPO[18]	O-Group A 4/4 mA	**ROM Address 17 or General Purpose Output.** This pin is the ROM A16 control when 2M ROM is used, or it is a general purpose output.
PCSJ/ GPO[0]	O-Group A 4/4 mA	**Programmable Chip Select or General Purpose Output.** This pin can be selected as a Programmable Chip Select, or as a general purpose output.
IDE interface :		
PIDE_DRQ	I-Group D	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer.
SIDE_DRQ	I-Group D	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer.
PIDE_AKJ	O-Group D 9.6/9.6 mA	**Primary IDE DACKJ for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer.
SIDE_AKJ	O-Group D 9.6/9.6 mA	**Secondary IDE DACKJ for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer.
PIDE_RDY	I-Group D	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
SIDE_RDY	I-Group D	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.

Pin Description Table (continued) :

Pin Name	Type	Description
IDE interface :		
PIDEIORJ	O-Group D 12/12 mA	**Primary IDE IORJ Command.** This is the IORJ command output pin to notify the Primary IDE device to assert the Read Data.
SIDEIORJ	O-Group D 12/12 mA	**Secondary IDE IORJ Command.** This is the IORJ command output pin to notify the Secondary IDE device to assert the Read Data.
PIDEIOWJ	O-Group D 12/12 mA	**Primary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Primary IDE device that the available Write Data is already asserted by M1533.
SIDEIOWJ	O-Group D 12/12 mA	**Secondary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Secondary IDE device that the available Write Data is already asserted by M1533.
PIDECS1J	O-Group D 9.6/9.6 mA	**IDE Chip Select 1 for Primary Channel 0.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3J	O-Group D 9.6/9.6 mA	**IDE Chip Select 3 for Primary Channel 1.** This is the Chip Select 3-command output pin to enable the Primary IDE device to watch the Read/Write Command.
SIDECS1J	O-Group D 9.6/9.6 mA	**IDE Chip Select 1 for Secondary Channel 0.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3J	O-Group D 9.6/9.6 mA	**IDE Chip Select 3 for Secondary Channel 1.** This is the Chip Select 3-command output pin to enable the Secondary IDE device to watch the Read/Write Command.
PIDE_A[2:0]	O-Group D 9.6/9.6 mA	**Primary IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
SIDE_A[2:0]	O-Group D 9.6/9.6 mA	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
PIDE_D[15:0]	I/O Group D 9.6/9.6 mA	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
SIDE_D[15:0]	I/O Group D 9.6/9.6 mA	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
Power Management Unit :		
RSM_RSTJ	I-Group C Schmitt	**Resume Circuit Initial Reset Input.** This input is used to initialize the resume circuit.
SMIJ	O-Group E 4/4 mA	**SMM Interrupt Output.** This output should be connected to CPU SMM Interrupt input.
STPCLKJ	O-Group E 4/4 mA	**Stop CPU Internal Clock Output.** This output is used to stop the CPU internal clock and should be connected to CPU STPCLKJ input.
SLEEPJ/ GPO[20]	O-Group E 4/4 mA	**Pentium PRO Sleep State or General Purpose Output.** This output will force Pentium PRO CPU to enter Sleep State, or as a general purpose output.
ZZ/ GPO[1]	O-Group E 4/4 mA	**PBSRAM Power Saving Mode or General Purpose Output.** This output is used to control L2 cache entering power saving mode, or as a general purpose output.
CLKRUNJ	I/O - Group B 12/16 mA	**PCI Clock Stop Message Control.** This pin is used to support PCI Clock Run function.
CPU_STPJ/ GPO[2]	O-Group B 4/4 mA	**Clock Cell CPU Clock Stop or General Purpose Output.** This output is used to stop the CPU Clock of the clock generator, or as a general purpose output.

Pin Description Table (continued) :

Pin Name	Type	Description
Power Management Unit :		
PCI_STPJ/ GPO[3]	O-Group B 4/4 mA	**Clock Cell PCI Clock Stop or General Purpose Output.** This output is used to stop the PCI Clock of the clock generator, or as a general purpose output.
SUSTAT1J	O-Group C 4/4 mA	**Suspend Status for North Bridge.** This output is used to notice the north bridge to control DRAM suspend refresh circuit.
SLOWDWN/ GPO[4]	O-Group B 4/4 mA	**Slow Down the Clock Generator Output or General Purpose Output.** This output is used to control the Clock Generator to slow down the clock output, or as a general purpose output.
AMSTATJ/ GPO[8]	O-Group B 4/4 mA	**APM State Control.** It is asserted when HALT or STPGNT cycle is detected.
PWRBTNJ	I-Group C Schmitt	**Power Button Input.** This input is used to support the ACPI Power Button function.
PCIREQJ/ GPI[3]	I-Group B	**PCI Bus Request Event Input or General Purpose Input.** This input comes from the North Bridge or external circuit to notice M1533 there is PCI request pending. This pin can also be programmed as a general purpose input.
POSSTA/ GPI[4]	I -Group A	**Force M1533 into Suspend Mode or General Purpose Input.** This input can be used to force M1533 entering suspend mode, or as a general purpose input.
SQWO/ GPO[9]	O-Group A 4/4 mA	**Square Wave Output or General Purpose Output.** This output can be used to output Square Wave with 1Hz or 2Hz, or as a general purpose output.
OFF_PWR0J/ GPO[21]	O-Group C 4/4 mA	**Remove Clock Generator Power Control or General Purpose Output.** This output can be used to remove the Clock Generator Power, or as a general purpose output.
OFF_PWR1/ GPO[22]	O-Group C 4/4 mA	**Remove All Circuit Power Except Internal Suspend Circuit and External DRAM or General Purpose Output.**
OFF_PWR2/ GPO[23]	O-Group C 4/4 mA	**Remove All Circuit Power Except Internal Suspend Circuit or General Purpose Output.**
RI	I -Group C Schmitt	**Ring-in or General Purpose Input.** This input connects to Modem Ring-in input to support ACPI Ring-in function, or as a general purpose input.
LBJ	I -Group C Schmitt	**First Battery Low Indication Input or General Purpose Input.** This input can be used as the first stage battery low level indication, or as a general purpose input signal.
LLBJ	I -Group C Schmitt	**Last Battery Low Indication Input or General Purpose Input.** This input can be used as the last battery low-level indication, or as a general purpose input signal.
EXTSW	I -Group A Schmitt	**External Switch Event or General Purpose Input.** EXTSW is a triggered input to the M1533 showing that an external device is requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
THRMJ	I -Group A Schmitt	**Thermal Event Input or General Purpose Input.** THRMJ is a triggered input to the M1533 showing that the external thermal detected circuits are requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
ACPWR	I - Group A Schmitt	**Detect AC Adapter Plug-in or General Purpose Input.** This is a triggered input showing that the AC adapter is plugged in or plugged out event. This triggered event can be used as a system management (or control) interrupt source. This signal also can be used optionally as a general purpose input signal.

Pin Description Table (continued) :

Pin Name	Type	Description
Power Management Unit :		
CRT	I -Group A Schmitt	**Detect CRT Connector Plug-in or General Purpose Input.** This signal represents whether the external CRT connector is plugged in/ plugged out, or used as a general purpose input.
SETUPJ	I -Group A	**Setup Switch Input or General Purpose Input.** This signal can be used as a setup switch triggered input for generating the power management interrupt event, or as a general purpose input signal.
EJECT	I -Group A	**External Eject SMIJ Trigger or General Purpose Input.** This triggered input is used as an eject (undocking) event indicator, or as a general purpose input signal.
LID	I -Group C	**Cover Switch Input or General Purpose Input.** This signal is used to indicate if the system lid is open or closed, or as a general purpose input.
HOTKEYJ	I -Group C Schmitt	**Hot Key Press Event Input or General Purpose Input.** This signal is used to indicate a hot key press event occurred or not, or as a general purpose input.
DOCKJ	I-Group C	**Docking Insert Event Input or General Purpose Input.** This triggered input is used as a docking event indicator, or as a general purpose input signal.
VCSJ/ GPI[5]	I-Group A	**VGA Activity Event Input or General Purpose Input.** The VGA chip should set this signal to active low when a VGA memory access occurs. This active signal is used by the M1533 to reload the VGA monitor timer or to generate a system management event. This signal also can be used as a general purpose input.
FPVEE/ GPI[6]	I-Group A	**LCD Back Light VEE Input or General Purpose Input.** This signal is used by the M1533 to generate DISPLAY and a programmable CCFT signal. This signal also can be used as a general purpose input.
CCFT/ GPO[5]	O-Group A 4/4 mA	**Back Light Control or General Purpose Output.** This signal can be programmed to be a periodical wave controlled by the FPVEE signal or kept to static low level. This signal also can be used as a general purpose output.
DISPLAY/ GPO[6]	O-Group A 4/4 mA	**LCD Display On/Off Control or General Purpose Output.** This signal can be programmed to be a response controlled by the FPVEE signal, or it can also be used as general purpose output.
CONTRAST/ GPO[7]	O-Group A 4/4 mA	**LCD Contrast Control or General Purpose Output.** It is a 1KHz signal with programmable duty cycle and can be used to control LCD contrast. It can also be used as general purpose output.
GPIORBJ/ GPO[10]	O-Group A 4/4 mA	**Input Event Latching into External Buffers Command or General Purpose Output.** This signal can be used as an external buffer(s) latching command for extended general inputs, or as a normal general purpose output signal.
GPIOWB/ GPO[11]	O-Group A 4/4 mA	**Output Control Signal Latching into External Buffers Command or General Purpose Output.** This signal can be used as an external buffer(s) latching command for extended general outputs, or as a normal general purpose output signal.
GPIO[19:16]	I/O, Group C Schmitt 4/4 mA	**General Purpose I/O Pins for Resume from Suspend Mode.** These signals can be programmed as the inputs or outputs for the resume triggered events from the suspend mode.
GPIO[15:12]/ BATSEL[3:0]	I/O Group C Schmitt 4/4 mA	**General Purpose I/O Pins or SM Bus Battery Select.** These signals can be used as the general purpose I/O pins, or as the external SMB battery select control signals. **GPIO[13]/BATSEL[1]** Baby AT or ATX hardware configure input. This chip supports baby AT power supply when pull high, or no pull, ATX power supply when pull low.
GPIO[11:8]	I/O Group A Schmitt 4/4 mA	**General Purpose I/O Pins for Wake-up from Stand-by Mode.** These signals can be programmed as the inputs or outputs for the wake-up triggered events from the standby mode.

Pin Description Table (continued) :

Pin Name	Type	Description
USB interface :		
USBP0+ USBP0-	I/O Group B	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USBP1+ USBP1-	I/O Group B	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
OVCRJ[1:0]/ GPI[1:0]	I -Group B	**Over Current Detect Inputs or General Purpose Inputs.** These two pins are used to monitor the USB Power Over Current, or as two general purpose inputs.
SM Bus signal :		
GPI[7]	I-Group A Schmitt	**General Purpose Input.** This signal is used as a general purpose input.
SMBCLK	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Clock.** SM Bus clock signal should be combined with SM Bus clock to carry information between the devices connected to the SM Bus.
SMBDATA	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Data Line.** SM Bus data signal should be combined with SM Bus data to carry information between the devices connected to the SM Bus.
Power Pins :		
VCC_A	P	**Vcc 3.3V or 5V for Power Group A.** This power is used for ISA interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power connects to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_3A	P	**Vcc 3.3V for Power Group A.** This power is used for ISA interface. If Vcc_A is selected as 3.3V, this power pin connects with Vcc_A to 3.3V power plane. If Vcc_A is selected as 5V, this power pin should connect to 3.3V power plane to save power consumption.
VCC_B	P	**Vcc 3.3V for Power Group B.** This power is used for PCI interface. It must be connected to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VCC_C	P	**Vcc 3.3V or 5V for Power Group C.** This power is used for resume/ suspend control interface signals during normal operation and suspend periods. If this power is connected to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power is connected to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_3C	P	**Vcc 3.3V for Power Group C.** This power is used for Resume/Suspend Control interface. If Vcc_C is selected as 3.3V, this power pin connects with Vcc_C to 3.3V power plane. If Vcc_C is selected as 5V, this power pin should connect to 3.3V power plane to save power consumption.
VCC_D	P	**Vcc 3.3V or 5V for Power Group D.** This power is used for IDE interface. If this power is connected to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power is connected to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_E	P	**Vcc 3.3V or 2.5V for Power Group E.** This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_5	P	**Vcc 5.0V for core Power.** It supplies the core power for the internal circuit except the suspend circuit.
VDD_5S	P	**Vcc 5.0V for Suspend/Resume Core Power.** It supplies the core power for the internal suspend/resume circuit.
Vss or Gnd	P	**Ground.**

2.3 Numerical Pin List

Pin no.	Pin name	Type
A1	**--**	--
A2	AD21	I/O
A3	AD18	I/O
A4	CBEJ2	I/O
A5	STOPJ	I/O
A6	AD14	I/O
A7	AD9	I/O
A8	AD5	I/O
A9	AD0	I/O
A10	SIDED7	I/O
A11	SIDED10	I/O
A12	SIDED2	I/O
A13	SIDED15	I/O
A14	SIDEAKJ	O
A15	SIDECS3J	O
A16	PIDED6	I/O
A17	PIDED10	I/O
A18	PIDED3	I/O
A19	--	-
A20	--	-
B1	**--**	-
B2	AD22	I/O
B3	AD19	I/O
B4	AD16	I/O
B5	DEVSELJ	I/O
B6	AD15	I/O
B7	AD10	I/O
B8	AD6	I/O
B9	AD1	I/O
B10	PHOLDJ	O
B11	SIDED5	I/O
B12	SIDED12	I/O
B13	SIDED0	I/O
B14	SIDERDY	I
B15	SIDECS1J	O
B16	PIDED9	I/O
B17	PIDED11	I/O
B18	PIDED13	I/O
B19	PIDED2	I/O
B20	PIDED14	I/O
C1	CBEJ3	I/O
C2	AD23	I/O
C3	AD20	I/O
C4	AD17	I/O
C5	TRDYJ	I/O

Pin no.	Pin name	Type
C6	CBEJ1	I/O
C7	AD11	I/O
C8	AD7	I/O
C9	AD2	I/O
C10	PHLDAJ	I
C11	SIDED9	I/O
C12	SIDED3	I/O
C13	SIDED14	I/O
C14	SIDEIORJ	O
C15	SIDEA2	O
C16	PIDED5	I/O
C17	PIDED4	I/O
C18	PIDED1	I/O
C19	PIDED15	I/O
C20	PIDED0	I/O
D1	AD26	I/O
D2	AD25	I/O
D3	AD24	I/O
D4	PCIRSTJ	O
D5	IRDYJ	I/O
D6	PAR	I/O
D7	AD12	I/O
D8	CBEJ0	I/O
D9	AD3	I/O
D10	CLKRUNJ	I/O
D11	SIDED6	I/O
D12	SIDED11	I/O
D13	SIDED1	I/O
D14	SIDEIOWJ	O
D15	SIDEA0	O
D16	PIDED8	I/O
D17	PIDED12	I/O
D18	PIDEA1	O
D19	PIDEA0	O
D20	PIDEA2	O
E1	AD29	I/O
E2	AD28	I/O
E3	AD27	I/O
E4	AD30	I/O
E5	FRAMEJ	I/O
E6	SERRJ	I
E7	AD13	I/O
E8	AD8	I/O
E9	AD4	I/O
E10	PCICLK	I

Numerical Pin List (continued)

Pin no.	Pin name	Type
E11	SIDED8	I/O
E12	SIDED4	I/O
E13	SIDED13	I/O
E14	SIDEDRQ	I
E15	SIDEA1	O
E16	PIDED7	I/O
E17	PIDEAKJ	O
E18	PIDECS1J	O
E19	PIDECS3J	O
E20	INTR	O
F1	USBCLK	I
F2	GPO8	O
F3	AD31	I/O
F4	INTAJ	I
F5	INTBJ	I/O
F6	VCC	P
F14	VCC	P
F15	VCC	P
F16	PIDEIOWJ	O
F17	PIDERDY	I
F18	NMI	O
F19	SMIJ	O
F20	IGNNEJ	O
G1	USBP0-	I/O
G2	USBP0+	I/O
G3	GPO4	O
G4	INTCJ	I/O
G5	INTDJ	I/O
G6	VCC	P
G15	VCC	P
G16	PIDEDRQ	I
G17	PIDEIORJ	O
G18	CPURST	O
G19	A20MJ	O
G20	INIT	O
H1	USBP1-	I/O
H2	USBP1+	I/O
H3	GPI3	I
H4	GPO3	O
H5	GPO2	O
H8	-	-
H9	-	-
H10	-	-
H11	-	-
H12	-	-
H13	-	-
H16	IRQ13	I/O
H17	STPCLK	O
H18	SMBDATA	I/O
H19	SMBCLK	I/O

Pin no.	Pin name	Type
H20	RI	I
J1	SD7	I/O
J2	RSTDRV	O
J3	IOCHKJ	I/O
J4	GPI1	I
J5	GPI0	I
J8	-	-
J9	GND	P
J10	GND	P
J11	GND	P
J12	GND	P
J13	-	-
J16	GPO1	O
J17	GPO20	O
J18	GPIO19	I/O
J19	GPIO18	I/O
J20	GPIO17	I/O
K1	SD5	I/O
K2	IRQ9	I/O
K3	SD6	I/O
K4	MSCLK	O
K5	MSDATA	I/O
K8	-	-
K9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13	-	-
K16	LLBJ	I
K17	DOCKJ	I
K18	GPIO16	I/O
K19	GPIO15	I/O
K20	GPIO14	I/O
L1	SD3	I/O
L2	DREQ2	I
L3	SD4	I/O
L4	KBCLK	I/O
L5	KBDATA	I/O
L8	-	-
L9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13	-	-
L16	IRQ8J	I
L17	SUSTAT1J	O
L18	PWRBTNJ	I
L19	GPIO13	I/O
L20	GPIO12	I/O
M1	IOCHRDY	I/O

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Numerical Pin List (continued)

Pin no.	Pin name	Type
M2	SD0	I/O
M3	SD1	I/O
M4	NOWSJ	I
M5	SD2	I/O
M8	-	-
M9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13	-	-
M16	PWG	I
M17	HOTKEYJ	I
M18	RSMRSTJ	I
M19	LBJ	I
M20	LID	I
N1	IOWJ	I/O
N2	SA19	O
N3	SMEMRJ	O
N4	AEN	O
N5	SMEMWJ	O
N8	-	-
N9	-	-
N10	-	-
N11	-	-
N12	-	-
N13	-	-
N15	VDD5S	P
N16	SIRQI	I
N17	SIRQII	I
N18	OSC32KII	I
N19	OSC32KI	I
N20	OSC32KO	O
P1	SA16	I/O
P2	DACKJ3	O
P3	SA17	O
P4	IORJ	I/O
P5	SA18	O
P6	VCC	P
P15	VCC	P
P16	GPO19	O
P17	GPO18	O
P18	GPO23	O
P19	GPO22	O
P20	GPO21	O
R1	DREQ1	I
R2	SA14	I/O
R3	DACKJ1	O
R4	SA15	I/O
R5	DREQ3	I
R6	VDD5	P
R7	VCC	P
R14	VCC	P
R15	VCC	P
R16	GPO17	O
R17	GPO16	O
R18	GPO15	O
R19	GPO14	O
R20	GPO13	O
T1	REFSHJ	I/O
T2	SA13	I/O
T3	IRQ6	I/O
T4	IRQ4	I/O
T5	DACKJ2	O
T6	BALE	O
T7	LA23	I/O
T8	LA20	I/O
T9	DACKJ0	O
T10	MEMWJ	I/O
T11	DREQ6	I
T12	ROMKBCSJ	O
T13	RTCAS	O
T14	RTCRW	O
T15	IRQ1I	I/O
T16	GPO12	O
T17	GPO11	O
T18	GPO10	O
T19	GPO9	O
T20	GPO7	O
U1	SA12	I/O
U2	IRQ7	I/O
U3	IRQ5	I/O
U4	IRQ3	I/O
U5	TC	O
U6	OSC14M	I
U7	IRQ10	I/O
U8	IRQ15	I/O
U9	LA17	I/O
U10	DREQ5	I
U11	SD10	I/O
U12	SD12	I/O
U13	RTCDS	O
U14	XD0	I/O
U15	XD4	I/O
U16	EJECT	I
U17	GPIO11	I/O
U18	GPO6	O
U19	GPO5	O
U20	GPO0	O
V1	SYSCLK	O
V2	SA10	I/O

Numerical Pin List (continued)

Pin no.	Pin name	Type
V3	SA8	I/O
V4	SA5	I/O
V5	SA2	I/O
V6	M16J	I/O
V7	LA22	I/O
V8	LA19	I/O
V9	DREQ0	I
V10	SD8	I/O
V11	DACKJ7	O
V12	SD13	I/O
V13	SPKR	O
V14	XD1	I/O
V15	XD5	I/O
V16	ACPWR	I
V17	GPI6	I
V18	GPIO8	I/O
V19	GPIO9	I/O
V20	GPIO10	I/O
W1	SA11	I/O
W2	SA9	I/O
W3	SA7	I/O
W4	SA4	I/O
W5	SA1	I/O
W6	SBHEJ	I/O
W7	IRQ11	I/O
W8	IRQ14	I/O
W9	MEMRJ	I/O
W10	DACKJ6	O
W11	SD11	I/O
W12	SD14	I/O
W13	SPLED	O
W14	XD2	I/O
W15	XD6	I/O
W16	SETUPJ	I
W17	GPI4	I
W18	GPI7	I
W19	GPI8	I
W20	--	-
Y1	**--**	-
Y2	--	-
Y3	SA6	I/O
Y4	SA3	I/O
Y5	SA0	I/O
Y6	IO16J	I
Y7	LA21	I/O
Y8	LA18	I/O
Y9	DACKJ5	O
Y10	SD9	I/O
Y11	DREQ7	I
Y12	SD15	I/O
Y13	EXTSW	I
Y14	XD3	I/O
Y15	XD7	I/O
Y16	THRMJ	I
Y17	CRT	I
Y18	GPI2	I
Y19	GPI5	I
Y20	--	-

2.4 Alphabetical Pin List

Pin no.	Pin name	Type
A1	--	-
A19	--	-
A20	--	-
B1	--	-
W20	--	-
Y1	--	-
Y2	--	-
Y20	--	-
G19	A20MJ	O
V16	ACPWR	I
A9	AD0	I/O
B9	AD1	I/O
C9	AD2	I/O
D9	AD3	I/O
E9	AD4	I/O
A8	AD5	I/O
B8	AD6	I/O
C8	AD7	I/O
E8	AD8	I/O
A7	AD9	I/O
B7	AD10	I/O
C7	AD11	I/O
D7	AD12	I/O
E7	AD13	I/O
A6	AD14	I/O
B6	AD15	I/O
B4	AD16	I/O
C4	AD17	I/O
A3	AD18	I/O
B3	AD19	I/O
C3	AD20	I/O
A2	AD21	I/O
B2	AD22	I/O
C2	AD23	I/O
D3	AD24	I/O
D2	AD25	I/O
D1	AD26	I/O
E3	AD27	I/O
E2	AD28	I/O
E1	AD29	I/O
E4	AD30	I/O
F3	AD31	I/O
N4	AEN	O
T6	BALE	O
D8	CBEJ0	I/O

Pin no.	Pin name	Type
C6	CBEJ1	I/O
A4	CBEJ2	I/O
C1	CBEJ3	I/O
D10	CLKRUNJ	I/O
G18	CPURST	O
Y17	CRT	I
T9	DACKJ0	O
R3	DACKJ1	O
T5	DACKJ2	O
P2	DACKJ3	O
Y9	DACKJ5	O
W10	DACKJ6	O
V11	DACKJ7	O
B5	DEVSELJ	I/O
K17	DOCKJ	I
V9	DREQ0	I
R1	DREQ1	I
L2	DREQ2	I
R5	DREQ3	I
U10	DREQ5	I
T11	DREQ6	I
Y11	DREQ7	I
U16	EJECT	I
Y13	EXTSW	I
E5	FRAMEJ	I/O
H10	-	
H11	-	
H12	-	
H13	-	
H8	-	
H9	-	
J10	GND	P
J11	GND	P
J12	GND	P
J13	-	
J8	-	
J9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13	-	
K8	-	
K9	GND	P
L10	GND	P
L11	GND	P

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
L12	GND	P
L13	-	-
L8	-	-
L9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13	-	-
M8	-	-
M9	GND	P
N10	-	-
N11	-	-
N12	-	-
N13	-	-
N8	-	-
N9	-	-
J5	GPI0/OVCRJ0	I
J4	GPI1/OVCRJ1	I
Y18	GPI2/SERIRQ	I
H3	GPI3/PCIREQJ	I
W17	GPI4/POSSTA	I
Y19	GPI5/VCSJ	I
V17	GPI6/FPVEE	I
W18	GPI7	I
W19	GPI8	I
V18	GPIO8	I/O
V19	GPIO9	I/O
V20	GPIO10	I/O
U17	GPIO11	I/O
L20	GPIO12/BATSEL0	I/O
L19	GPIO13/BATSEL1	I/O
K20	GPIO14/BATSEL2	I/O
K19	GPIO15/BATSEL3	I/O
K18	GPIO16	I/O
J20	GPIO17	I/O
J19	GPIO18	I/O
J18	GPIO19	I/O
U20	GPO0/PCSJ	O
J16	GPO1/ZZ	O
H5	GPO2/CPU_STPJ	O
H4	GPO3/PCI_STPJ	O
G3	GPO4/SLOWDWN	O
U19	GPO5/CCFT	O
U18	GPO6/DISPLAY	O
T20	GPO7/CONTRAST	O
F2	GPO8/AMSTATJ	O
T19	GPO9/SQWO	O
T18	GPO10/GPIORBJ	O
T17	GPO11/GPIOWB	O
T16	GPO12/XDIR	O

Pin no.	Pin name	Type
R20	GPO13/IRQ1O	O
R19	GPO14/IRQ12O	O
R18	GPO15/IRQ0	O
R17	GPO16APICCSJ	O
R16	GPO17/APICGNTJ	O
P17	GPO18/BIOSA16	O
P16	GPO19/BIOSA17	O
J17	GPO20/SLEEPJ	O
P20	GPO21/OFF_PWR0J	O
P19	GPO22/OFF_PWR1	O
P18	GPO23/OFF_PWR2	O
M17	HOTKEYJ	I
F20	IGNNEJ	O
G20	INIT	O
F4	INTAJ	I
F5	INTBJ	I/O
G4	INTCJ	I/O
G5	INTDJ	I/O
E20	INTR	O
Y6	IO16J	I
M1	IOCHRDY	I/O
J3	IOCHKJ	I/O
P4	IORJ	I/O
N1	IOWJ	I/O
D5	IRDYJ	I/O
T15	IRQ1I/KBINH	I/O
U4	IRQ3	I/O
T4	IRQ4	I/O
U3	IRQ5	I/O
T3	IRQ6	I/O
U2	IRQ7	I/O
L16	IRQ8J	I
K2	IRQ9	I/O
U7	IRQ10	I/O
W7	IRQ11	I/O
H16	IRQ13/FERRJ	I/O
W8	IRQ14	I/O
U8	IRQ15	I/O
L4	KBCLK/GPI9	I/O
L5	KBDATA/GPI10	I/O
U9	LA17	I/O
Y8	LA18	I/O
V8	LA19	I/O
T8	LA20	I/O
Y7	LA21	I/O
V7	LA22	I/O
T7	LA23	I/O
M19	LBJ	I
M20	LID	I
K16	LLBJ	I

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
V6	M16J	I/O
W9	MEMRJ	I/O
T10	MEMWJ	I/O
K4	MSCLK/GPI11	O
K5	MSDATA/IRQ12I	I/O
F18	NMI	O
M4	NOWSJ	I
U6	OSC14M	I
N19	OSC32KI	I
N18	OSC32KII	I
N20	OSC32KO	O
D6	PAR	I/O
E10	PCICLK	I
D4	PCIRSTJ	O
C10	PHLDAJ	I
B10	PHOLDJ	O
D19	PIDEA0	O
D18	PIDEA1	O
D20	PIDEA2	O
E18	PIDECS1J	O
E19	PIDECS3J	O
C20	PIDED0	I/O
C18	PIDED1	I/O
B19	PIDED2	I/O
A18	PIDED3	I/O
C17	PIDED4	I/O
C16	PIDED5	I/O
A16	PIDED6	I/O
E16	PIDED7	I/O
D16	PIDED8	I/O
B16	PIDED9	I/O
A17	PIDED10	I/O
B17	PIDED11	I/O
D17	PIDED12	I/O
B18	PIDED13	I/O
B20	PIDED14	I/O
C19	PIDED15	I/O
E17	PIDEAKJ	O
G16	PIDEDRQ	I
G17	PIDEIORJ	O
F16	PIDEIOWJ	O
F17	PIDERDY	I
M16	PWG	I
L18	PWRBTNJ	I
T1	REFSHJ	I/O
H20	RI	I
T12	ROMKBCSJ	O
M18	RSMRSTJ	I
J2	RSTDRV	O
T13	RTCAS	O
U13	RTCDS	O
T14	RTCRW	O
Y5	SA0	I/O
W5	SA1	I/O
V5	SA2	I/O
Y4	SA3	I/O
W4	SA4	I/O
V4	SA5	I/O
Y3	SA6	I/O
W3	SA7	I/O
V3	SA8	I/O
W2	SA9	I/O
V2	SA10	I/O
W1	SA11	I/O
U1	SA12	I/O
T2	SA13	I/O
R2	SA14	I/O
R4	SA15	I/O
P1	SA16	I/O
P3	SA17	O
P5	SA18	O
N2	SA19	O
W6	SBHEJ	I/O
M2	SD0/GPIO0	I/O
M3	SD1/GPIO1	I/O
M5	SD2/GPIO2	I/O
L1	SD3/GPIO3	I/O
L3	SD4/GPIO4	I/O
K1	SD5/GPIO5	I/O
K3	SD6/GPIO6	I/O
J1	SD7/GPIO7	I/O
V10	SD8	I/O
Y10	SD9	I/O
U11	SD10	I/O
W11	SD11	I/O
U12	SD12	I/O
V12	SD13	I/O
W12	SD14	I/O
Y12	SD15	I/O
E6	SERRJ	I
W16	SETUPJ	I
D15	SIDEA0	O
E15	SIDEA1	O
C15	SIDEA2	O
B15	SIDECS1J	O
A15	SIDECS3J	O
B13	SIDED0	I/O
D13	SIDED1	I/O
A12	SIDED2	I/O
C12	SIDED3	I/O

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
E12	SIDED4	I/O
B11	SIDED5	I/O
D11	SIDED6	I/O
A10	SIDED7	I/O
E11	SIDED8	I/O
C11	SIDED9	I/O
A11	SIDED10	I/O
D12	SIDED11	I/O
B12	SIDED12	I/O
E13	SIDED13	I/O
C13	SIDED14	I/O
A13	SIDED15	I/O
A14	SIDEAKJ	O
E14	SIDEDRQ	I
B14	SIDERDY	I
C14	SIDEIORJ	O
D14	SIDEIOWJ	O
N16	SIRQI	I
N17	SIRQII	I
H19	SMBCLK	I/O
H18	SMBDATA	I/O
N3	SMEMRJ	O
N5	SMEMWJ	O
F19	SMIJ	O
V13	SPKR	O
W13	SPLED	O
A5	STOPJ	I/O
H17	STPCLKJ	O
L17	SUSTAT1J	O
V1	SYSCLK	O
U5	TC	O
Y16	THRMJ	I
C5	TRDYJ	I/O
F1	USBCLK	I
G2	USBP0+	I/O
G1	USBP0-	I/O
H2	USBP1+	I/O
H1	USBP1-	I/O
F14	VCC	P
F15	VCC	P
F6	VCC	P
G15	VCC	P
G6	VCC	P
P6	VCC	P
P15	VCC	P
R14	VCC	P
R15	VCC	P
R7	VCC	P
R6	VDD5	P
N15	VDD5S	P

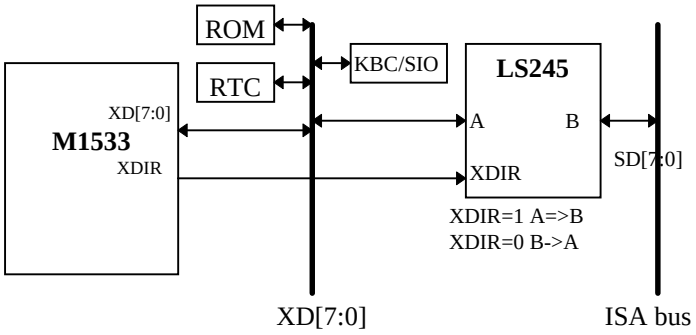
Pin no.	Pin name	Type
U14	XD0	I/O
V14	XD1	I/O
W14	XD2	I/O
Y14	XD3	I/O
U15	XD4	I/O
V15	XD5	I/O
W15	XD6	I/O
Y15	XD7	I/O

2.5 Hardware Setting Description

No.	Pin Name	Setup, Configuration
U20	PCSJ	0: Pull-low, POWER PC mode 1: Pull-high, INTEL PC mode
B10	XPHOLDJ	0: Pull-low, USB in test mode.(for test only) 1: Pull-high, USB in normal mode.
T19	SQWO	0: Pull-low, external I/O APIC is supported. 1: Pull-high, external I/O APIC is not supported.
W13	SPLED	0: Pull-low, support 256KB ROM 1: Pull-high, not support 256KB ROM
T16	XDIR	0: Pull-low, Pentium Pro CPU is used. 1: Pull-high, Pentium CPU is used.
U5	TC	0 : Pull-low, pins SD/GPIO[7:0] are SD[7:0], external LS245 is not required. 1 : Pull-high, pins SD/GPIO[7:0] are GPIO[7:0], external LS245 is required.
V13	SPKR	0: Pull-low, internal Keyboard controller is enabled. 1: Pull-high, internal Keyboard controller is disabled.
T12	ROMKBCSJ	0: Pull-low, chip test mode is enabled. (for test only) 1: Pull-high, chip test mode is disabled.

2.6 XDIR Control

When pin TC is pull high, the external LS245 is required. The connection is :



1) PCI I/O Read ISA : XDIR=0
2) PCI I/O Write ISA : XDIR=1
3) PCI Memory Read ISA : XDIR=0
4) PCI Memory Write ISA : XDIR=1
5) PCI access XD bus device (RTC,ROM,KBC) : XDIR =1
6) ISA Refresh : XDIR =1
7) ISA/DMA master MR/IOW : XDIR=1
8) ISA/DMA master MW/IOR : XDIR=0

Section 3 : Function Description

3.1 PCI Command Set

The command types the M1533 supports in Slave mode are Interrupt Acknowledge, Special cycle, I/O read, I/O write, memory read, memory write, configuration read and configuration write and other multiple memory read/write cycles.

M1533 PCI Cycle Description

CBEJ	Command Type	as Target	as Initiator
0000	Interrupt	Yes	No
0001	Special Cycle	Yes - Note.1	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes - Note.2	No
1101	Reserved	No	No
1110	Memory Read line	Yes - Note.2	No
1111	Memory Write and Invalidate	Yes - Note.3	No

Note 1 : The M1533 only decodes Stop Grant special cycle, and Halt special cycle and Shutdown special cycle. All other special cycles are ignored.
Note 2 : Treated as Memory read
Note 3 : Treated as Memory write

3.2 Description of PCI Slave

As a PCI slave, the M1533 will assert DEVSELJ signal to indicate it is the target of the PCI transaction. DEVSELJ is asserted when the M1533 positively or subtractively decodes the PCI transaction. The configuration cycle, USB programming cycle and IDE I/O cycle are positively decoded. The timer and interrupt controller programming cycles are positively or subtractively decoded via register setting. All others are subtractively decoded except for docking mode. All cycles will be positively decoded in docking mode. These cycles include PCI to ISA slave cycles. Under docking mode, M1533 only supports positive decode.

A 32-bit posted write buffer is embedded to support PCI to ISA memory write cycles and delay transaction cycle. Multiple read/write transactions are not supported. Hence, any burst cycles decoded by the M1533 will be terminated by disconnecting semantics after the first data transaction has completed. The M1533 will retry any PCI initiated cycle when its internal buffer cycle is still active.

M1533 supports delay transaction and discard counter in compliance with PCI specification 2.1.

3.2.1 Posted Write Buffer

The PCI-to-ISA memory write cycles will be posted into the write buffer when it is enabled, and the buffer is scheduled to be written to the ISA bus. Any subsequent PCI cycles to the M1533 will be retried until the posted write buffer is empty. The buffer also optionally supports data I/O posted write cycle for sound cards.

The posted write buffer must be flushed and disabled before an ISA/DMA master owns the ISA and PCI bus. This rule eliminates the possibility of a deadlock caused by a committed ISA cycle. The buffer will also be flushed before granting an external APIC request.

3.3 PCI Master

3.3.1 M1533 as PCI Master

As a PCI Master, the M1533 performs memory and I/O read/write transfers. The M1533 will assert a master abort due to DEVSELJ timeout. The M1533 acts as a PCI Master when an ISA or DMA master accesses the PCI memory. The M1533 provides an 8-byte bi-directional line buffer for ISA/DMA Master memory read from or write to PCI bus. The line buffer is used to isolate the ISA bus slower devices from the PCI. Only an ISA/DMA master memory write or read cycle to PCI bus can be assembled /disassembled into line buffer. When line buffer is enabled, the ISA/DMA master can prefetch 2 Doublewords to the line buffer for read cycle. However, only 4 bytes are used in the buffer for write cycle.

In some cases, a strong ordering must be kept due to coherency problems, the line buffer might be disabled. When the line buffer is disabled, the reorder problem caused by assembly/disassembly will be avoided and guarantees read/write ordering.

3.3.2 Posted - Write Buffer Flush

Once an ISA/ DMA master begins a cycle on the ISA bus, the cycle cannot be backed off. It can only be held in wait states via IOCHRDY. In order to avoid deadlock situations, the PCI master post write buffer needs to be flushed before an ISA/ DMA master gets the ISA bus. When the ISA/ DMA master owns the ISA bus, the post write buffer will be disabled.

3.3.3 Line Buffer Management

When an ISA /DMA master reads from PCI memory, the M1533 prefetches 8 bytes of data into the line buffer. If there is a read "hit" from the line buffer, the "hit" bytes are marked as invalid. There are 3 conditions why the line buffer needs prefetching :

1. Line buffer is "Empty" when read.
2. Read "Miss" to the line buffer.
3. Read the invalid byte from the line buffer.

When ISA/DMA master writes to PCI memory, the M1533 writes data to the line buffer. When the 4-byte buffer is full, it flushes data to the PCI bus. There are five conditions why the line buffer must flush its data :

1. Line buffer is full. Flush the line buffer and mark empty.

2. Write "Miss" to the partially full 4-byte line. Flush the partially full line and mark as empty, then write to the empty line.

3. Write "Hit" to the valid bytes. Flush it and mark as empty, then write to the empty line.

4. Read after write transaction and the line buffer is partially full. Flush the line buffer then do read prefetch.

5. Master has changed on DACKJ going inactive and last transaction is write and line buffer is partially full. Flush the line buffer.

3.4 Parity Support

As a master, the M1533 will generate address parity for read/write cycles, and data parity for write cycles. Parity check will work at read cycle. As a target, the M1533 will generate data parity for read cycles. PAR is even parity across AD[31:0] and CBEJ[3:0]. Even parity means that the number of 1's within the 36 bits and PAR is even. PAR has the same timing as AD[31:0] but delayed by one clock.

3.5 Address decoding

a. Positively decodes configuration cycle.
b. Positively or subtractively decodes interrupt acknowledge cycle.
c. Positively decodes on-chip IDE access cycle.
d. Positively decodes on-chip USB access cycle.
e. Positively or subtractively decodes internal I/O cycle (interrupt controller and timer counter).
f. Subtractively decodes DMA controller internal registers.
g. Others are subtractive decode.
h. When M1533 is programmed to be docking mode, all cycles are positively decoded including ISA-direct cycles.

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www.acerlabs.com

3.6 IDE Master Controller

a. Supports PCI bus mastering, transfer rate up to 132 Mbytes/sec. This significantly lightens the load of CPU work burden.
b. Supports IDE PIO modes 0, 1, 2, 3, 4 & 5 timing and multiword DMA modes 0,1,2 on enhanced IDE specifications. This chip is capable of accelerated PIO data transfers as well as acting as a PCI bus master on behalf of an IDE DMA slave device. The M1533 provides an interface for two dedicated IDE connectors.
c. Supports compatible and native PCI mode. Compatible mode is the default mode, native PCI mode will only be chosen by the BIOS.
d. 10 Doubleword FIFO for posted-write or read-ahead buffer for each channel (Total = 20 Doublewords). Each channel buffer is independent.
e. Programmable command and data transfer timing per drive for maximum flexibility. Operation of two hard disks is possible even if they have different PIO modes.
f. Supports concurrent operation on two ATA channels. M1533 simultaneously operates two drives.
g. Supports ATAPI CD-ROM concurrent operation. Simultaneous use of hard disks and CD-ROM is possible.
h. Dedicated ATA bus pins and dedicated buffers for each channel, no extra TTLs are needed.
i. Supports Ultra 33 high performance ATA bus for 33Mbytes transfer rate.

3.7 Distributed DMA

The Distributed DMA Hosts Controller supported by M1533 provides one way to allow the separation of the slave DMA controllers in the hardware architecture, and yet allows the OS and application base to still utilize two legacy DMA controllers.

3.8 Serialized IRQ

The serialized IRQ supported by M1533 provides one pin named IRQSER to generate IRQs event to Interrupt Controller from serialized IRQ protocol. The frame number can be programmed from 17 to 32. The Operation mode (quiet or continuous) and Start Frame Pulse width (4 to 8 pciclks) are also programmable.

3.9 Advanced Power Management

The M1533 Power management unit includes full ACPI compliance spec. and legacy power management including SMM, Stop clock control unit, APM, External SMI-switch control, Programmable counters for time-out event generation. M1533 can provide On(working)/ Sleeping (Power_on_suspend)/ Suspend_to_DRAM/ Suspend_to_Disk/Soft_Off/Mechanical_Off global system states to minimize the overall system power consumption. M1533 also provides an extra Standby state for monitoring over 16 peripheral devices activity. M1533 supports programmable Stop_Clock with throttle/ CLK_ON_STPCLK/CLK_OFF_STPCLK control for fitting the ACPI C0-C3 clock states. M1533 provides several hot plugging events detection and multiple external wake-up events for satisfying the notebook requirements. M1533 supports the battery, thermal detected logic and system/chip/devices power plane management logic. The M1533 provides full support for Advanced Configuration and Power Interface (ACPI), On-now technology and OS Directed Power Management (OSPM). M1533 also supports the legacy power management control, such as SMM and SMI features. The goal of the M1533 power management not only targets to the current desktop/ notebook satisfaction but also to the future OS driven flexible requirements.

3.10 SMBus

The M1533 SMBus has been designed based on :

System Management Bus Specification Rev 1.0
Smart Battery Data Specification Rev 1.0
Smart Battery Charger Specification Rev 1.0
System Management Bus BIOS Specification Rev 1.0
Smart Battery Selector Specification Rev 0.9

The SMBus controller also supports auto polling Battery status, remaining time and remaining capacity to reduce the CPU overhead.

The System Management Bus (SMBus) host controller in M1533 supports the ability to communicate with power-related devices by SMBus protocol. It can be a master or slave on the SMBus, providing quick/ send byte/receive byte/ write byte/write word/read word/block read/block write command with clock synchronization and arbitration functions.

3.11 USB

The M1533 USB is an implementation of the Universal Serial Bus (USB) 1.0 specification which contains PCI interface logic, Host Controller and an integrated Root Hub with two USB ports. For DOS compatibility, Keyboard and Mouse legacy are also supported.

Section 4 : Configuration Registers

4.1 Register Description

4.1.1 PCI to ISA Bridge Configuration Space (IDSEL= AD18)

The indices before 40h are read-only.
All reserved bits are read as 0's

Index-Offset **Description**

Register Index : **01h-00h**
Register Name : **Vendor ID**
Default Value : 10B9h
Attribute : RO

Register Index : **03h-02h**
Register Name : **Device ID**
Default Value : 1533h
Attribute : RO

Register Index : **05h-04h**
Register Name : **Command Byte**
Default Value : 000Fh
Attribute : RO

Bit No.	Bit Function
15-5	Reserved. Read as 0's ;
4	Caching Command Enable (always '0');
3	Special cycle Enable (always '1');
2	Bus Master Enable (always '1');
1	Memory Space Enable (always '1');
0	I/O Space Enable (always '1');

Register Index : **07h-06h**
Register Name : **Status Byte**

Bit No.	Bit Function
15	Detected Parity Error. Always '0';
14	Signal System error. Always '0' ;
13	Receive Master Abort when M1533 acts as a master. This bit is set to a '1' when M1533 generates a transaction (except for Special Cycle) is terminated with master-abort. This is a read only bit and is cleared by writing a '1' to it.
12	Receive Target Abort when M1533 acts as a master This bit is set to a '1' when M1533 encounters a target abort condition. This is a read only bit and is cleared by writing a '1' to it.
11	Signal Target Abort When M1533 acts as a slave. M1533 as a slave never generates a Target abort this bit is always 0;
10-9	M1533 DEVSELJ Timing This status of DEVSELJ decode timing as PCI specification. M1533 always generates DEVSELJ with medium timing Bit9='1',Bit10='0';
8-0	Reserved. Read as 0's;

Register Index : **08h**
Register Name : **Revision ID**.
Default Value : 00h
Attribute : Read Only

Register Index : **0B-09h**
Register Name : **Class code**.
Default Value : 0Bh=06h,0Ah=01h,09h=00h.
Attribute : Read Only

Register Index **0D-0Ch**
Register Name : **Reserved**
Attribute :

Register Index **0Eh** bit7=0 always single-function chip.
Register Name : **Device Type**
Default Value : 00h
Attribute : Read Only

Register Index : **2Bh-0Fh**
Register Name : **Reserved**
Attribute :

Register Index : **2Dh-2Ch**
Register Name : **Subsystem Vendor ID**
Default Value : 00h
Attribute : Read/Write

Register Index : **2Fh-2Eh**
Register Name : **Subsystem ID**
Default Value : 00h
Attribute : Read/Write

Register Index : **3Fh-30h**
Register Name : **Reserved**
Attribute :

M1533 PCI INTERFACE CONFIGURATIONS.
Register Index : **40h**
Register Name : **PCI Control**
Default Value : 00h

Bit No.	Bit Function
7	Reserved.
6	Sound card I/O posted-write enable/disable. 0 : Disable 1 : Enable Note: 1. When enabling this bit, D2 of cfg.40h should be enabled simultaneously. 2. This bit is a switch of cfg.50h-53h sound card I/O post write. 3. This bit has no effect on internal I/O port, e.g. 8254,8259,8237 ports.
5	Select ISA master to PCI Bus request method 0 : Bus request at each time ISA MASTER requests the bus. 1 : Bus request only MASTER assert command.
4	PCI and ISA concurrent mode enable/disable. 0 : Disable 1 : Enable
3	Delay transaction for PCI spec. 2.1 enable/disable. 0 : Disable 1 : Enable
2	PCI-to-ISA Posted Write Buffer Enable/Disable 0 : Disable 1 : Enable Note: This bit includes PCI to ISA Memory Post Write and I/O Post Write.
1	ISA Master Line Buffer Enable/Disable 0 : Disable 1 : Enable
0	DMA Line Buffer Enable/Disable 0 : Disable 1 : Enable

Register Index : **41h**
Default Value : 00h

Bit No.	Bit Function
7	PS/2 Keyboard present feature 0 : Without PS/2 keyboard(AT IRQ1) 1 : With PS/2 Keyboard Bit 7 is used to enable IRQ1 latch, when IRQ1 goes high. And IRQ1 will be released when read Port 60H. If '0', IRQ1 will be compatible to AT definition. If '1', IRQ1 will be compatible to PS/2 definition. This bit is also used to select AT/PS/2 internal Keyboard Controller.
6	PS/2 Mouse/AT Mouse select 0 : AT mouse 1 : With PS/2 mouse Bit 6 is used to enable IRQ12 latch, when IRQ12 goes high. And IRQ12 will be released when read Port 60H. If '0', IRQ12 will be compatible to AT definition. If '1', IRQ12 will be compatible to PS/2 definition.
5-2	I/O recovery period 0,0,0,0 : 0 us 0,0,0,1 : 0.25 us (2/ATCLK) 0,0,1,0 : 0.5 us (4/ATCLK) 0,0,1,1 : 0.75 us (6/ATCLK) 0,1,0,0 : 1 us (8/ATCLK) 0,1,0,1 : 1.25 us (10/ATCLK) 0,1,1,0 : 1.5 us (12/ATCLK) 0,1,1,1 : 1.75 us (14/ATCLK) 1,0,0,0 : 2 us (16/ATCLK) 1,0,0,1 : 2.25 us (18/ATCLK) 1,0,1,0 : 2.5 us (20/ATCLK) 1,0,1,1 : 2.75 us (22/ATCLK) 1,1,0,0 : 3 us (24/ATCLK) 1,1,0,1 : 3.25 us (26/ATCLK) 1,1,1,0 : 3.5 us (28/ATCLK) 1,1,1,1 : 3.75 us (30/ATCLK)
1	On-Chip I/O recovery 0 : Disable on-chip I/O recovery 1 : Enable on-chip I/O recovery Bit0 is used to enable ISA I/O recovery timer, Bit1 is used for M1533 internal I/O Port I/O recovery, but Bit0 must be 1 first.
0	ISA I/O recovery feature 0 : Disable ISA I/O recovery 1 : Enable ISA I/O recovery

Register Index : **42h**
Default Value : 00h

Bit No.	Bit Function
7	Configuration Port read data mask function. 0 : Normal I/O read/write 1 : Read from 40-FFh are all 0's
6	DMA High Page register Enable/Disable 0 : Disable. (24 bits addressing) 1 : Enable. (32 bits addressing)
5	Reserved (must be 0)
4	Reserved (must be 0)
3	Decoupled refresh control 0 : Normal refresh 1 : Decoupled refresh This bit is 0, Refresh Master will own ISA and PCI bus. When this bit is set to 1, Refresh master will only own ISA Bus.
2-0	ISA clock select 000 : 7.16 MHz 001 : PCICLK/2 010 : PCICLK/3 011 : PCICLK/4 100 : PCICLK/5 101 : PCICLK/6 110 : reserved 111 : reserved

Register Index : **43h**
Register Name : **ISA Bus cycle control**
Default Value : 00h

Bit No.	Bit Function
7	Port-92H RC/GATEA20 Selection 0 : Disable Port-92H 1 : Enable Port-92H. PORT-92H is used to start FAST RC.
6	Co-processor interface This bit is used to support the Co-processor error reporting or as an external IRQ13 for pin FERRJ. 0 : disable (Pin FERRJ as IRQ13; IGNNEJ always 1) 1 : enable (Pin FERRJ as FERRJ)
5-4	ISA Refresh period setting 0,0 : 15 us refresh period 0,1 : 30 us 1,0 : 60 us 1,1 : 120 us
3-2	16-bit ISA memory command insert wait count 0,0 : normal 16-bit access 0,1 : Insert 1 wait 1,0 : insert 2 waits 1,1 : insert 3 waits
1-0	16 bit ISA I/O command insert wait count 0,0 : normal 16-bit access 0,1 : insert 1 wait 1,0 : Insert 2 waits 1,1 : insert 3 waits

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Register Index : **44h**
Default Value : 00h

Bit No.	Bit Function
7	PCI soft reset control 0 : when CPU soft reset initialize, PCIRSTJ will not be active 1 : when CPU soft reset initialize, PCIRSTJ will be active
6	On chip I/O decode(except DMA I/O port is always subtractive) 0 : positive decode 1 : subtractive decode
5	Reserved.(must be '0')
4	On-chip IDE master Primary INTAJ level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip IDE master Primary INTAJ routing when native mode is enable. D3 D2 D1 D0 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **45h**
Default Value : 00h

Bit No.	Bit Function
7	PCI interrupt polling mode enable/disable. 0 : disable. 1 : enable.
6	ROM chip select activated when accessing 62h and 66h port. 0 : disable 1 : enable If this bit is enabled, ROM chip select will be active when accessing 60,64,62,66h ports.
5	Reserved.
4	Reserved.
3	Delay transaction timeout counter enable/disable. 0 : disable. 1 : enable.
2	Reserved.
1	Distributed DMA enable/disable 0 : disable. 1 : enable.
0	Parity check enable/disable. 0 : disable. 1 : enable.

Register Index : **46h**
Register Name : **Reserved**

Register Index : **47h**
Register Name : **BIOS chip select control**
Default Value : 00h

Bit No.	Bit Function
7	SA16 inverter control 0 : Normal SA16 1 : Invert SA16 when ROM chip select active
6	Flash ROM read/write control (write protest) 0 : disable; ROM chip select will be active only in memory read cycle. 1 : enable; ROM chip select will be active in memory read/write cycle.
5	0 : disable 1 : enable; ROMKBCSJ will be active when accessing memory 000D0000-000DFFFF.
4-3	Share memory VGA BIOS region decode.
4	0 : disable 1 : enable; ROMKBCSJ will be active when accessing memory 000C8000-000CFFFF.
3	0 : disable 1 : enable; ROMKBCSJ will be active when accessing memory 000C0000-000C7FFF.
2-1	Extended ROM region enable/disable.
2	0 : disable; 1 : enable; ROMKBCSJ will be active when accessing memory FFFC0000-FFFDFFFF. This bit will enlarge the ROM size to 256 KB.
1	0 : disable; 1 : enable; ROMKBCSJ will be active when accessing memory FFFE0000-FFFEFFFF.
0	ROM size define for ROM chip select decode 0 : 64 KB(000F0000-000FFFFF, FFFF0000-FFFFFFFF) 1 : 128KB(000E0000-000EFFFF,000F0000-000FFFFF, FFFF0000-FFFFFFFF).

Register Index : **48h**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-2 to ISA IRQ routing table Above Routing Table : D3-D0 or D7-D4 D3 D2 D1 D0 or D7 D6 D5 D4 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15 The BIOS should inhabit to set the reserved value. The reserved setting will disable the IRQ at the present design.
3-0	INT-1 to ISA IRQ routing table.

Register Index : **49h**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-4 to ISA IRQ routing table.
3-0	INT-3 to ISA IRQ routing table.

Register Index : **4Ah**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-6 to ISA IRQ routing table.
3-0	INT-5 to ISA IRQ routing table.

Register Index : **4Bh**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-8 to ISA IRQ routing table
3-0	INT-7 to ISA IRQ routing table

Register Index : **4Ch**
Register Name : **PCI INT to ISA Level to Edge transfer**
Default Value : 00h

Bit No.	Bit Function
7	INT-8 0 : disable, PCI Level trigger INT will be bypassed as level trigger to M8259. 1 : enable, PCI Level trigger INT will be transformed to be Edge trigger to M8259.
6	INT-7
5	INT-6
4	INT-5
3	INT-4
2	INT-3
1	INT-2
0	INT-1

Index 48h to 4Ch are used to define PCI INT 8 channel's routing tables for ISA system. For PCI, INT is level, not edge trigger. 4Ch index is used to enable each INT channel from level to edge transfer.

Register Index : **4Dh**
Register Name : **MBIRQ0(XSIRQI), MBIRQ1(XSIRQII) Interrupt to ISA IRQ routing table**
Default Value : 00h
Before using this register, Index 58h bit1-0 must be programmed to be SIRQI and SIRQII function.

Bit No.	Bit Function
7-4 3-0	SIRQI to ISA IRQ routing table SIRQII to ISA IRQ routing table Above Routing Table : D3-D0 or D7-D4 D3 D2 D1 D0 or D7 D6 D5 D4 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15
	The BIOS should inhabit to set the reserved value.
	The reserved setting will disable the IRQ at the present design.

Register Index : **4Eh**
Register Name : **Reserved**

Register Index : **4Fh**
Register Name : **Reserved**

Register Index : **51h-50h**
Register Name: **I/O cycle Posted-write first port definition**.
Default Value : 0000h

Bit No.	Bit Function
15	0 : disable 1 : enable
14-12	Reserved
11-0	Define the sound card first I/O port for post-write.

Register Index : **53h-52h**
Register Name : **I/O cycle posted-write second port definition**
Default Value : 0000h

Bit No.	Bit Function
15	I/O cycle posted-write second port definition. 1 : enable 0 : disable
14	On-chip USB device enable/disable. 0 : enable. 1 : disable.
13-12	Reserved.
11-0	I/O cycle posted-write second port definition. Define the sound card first I/O port for post-write.

Register Index : **54h**
Register Name : **Hardware setting status bits**
Attribute : Read only

Bit No.	Bit Function
7	PCSJ hardware setting status. 0: Pull-low, POWER PC mode 1: Pull-high, INTEL PC mode
6	PHOLDJ hardware setting status. 0: Pull-low, USB in test mode.(for test only) 1: Pull-high, USB in normal mode.
5	SQWO hardware setting status. 0: Pull-low, external I/O APIC is supported. 1: Pull-high, external I/O APIC is not supported.
4	SPLED hardware setting status. 0: Pull-low, support 256KB ROM 1: Pull-high, not support 256KB ROM
3	XDIR hardware setting status. 0: Pull-low, Pentium Pro CPU is used. 1: Pull-high, Pentium CPU is used.
2	TC hardware setting status. 0 : Pull-low, pins SD/GPIO[7:0] are SD[7:0], external LS245 is not required. 1 : Pull-high, pins SD/GPIO[7:0] are GPIO[7:0], external LS245 is required.
1	SPKR hardware setting status. 0: Pull-low, internal Keyboard controller is enabled. 1: Pull-high, internal Keyboard controller is disabled.
0	ROMKBCSJ hardware setting status. 0: Pull-low, chip test mode is enabled.(for test only) 1: Pull-high, chip test mode is disabled.

Register Index : **57h-55h**
Register Name : **Programmable chip select(pin PCSJ) address define**.
Default Value : 000002h

Bit No.	Bit Function
23	Included Port 62h, 66h in for decode PCSJ enable/disable. 0 : disable; 1 : enable.
22	The chip select qualified by ISA Bus IOWJ enable/disable. 0 : disable; 1 : enable.
21	The chip select qualified by ISA Bus IORJ enable/disable. 0 : disable; 1 : enable.
20	PCI interrupt polling mode clock select. 0 : PCICLK. 1 : 14 MHz.
19	Enable/disable system to monitor Halt cycle 0 : enable 1 : disable
18	Enable/disable break event at throttle low. 0 : enable 1 : disable
17	Enable/disable break event at throttle high. 0 : enable 1 : disable
16	Select Period of Throttle 0 : 256 us 1 : 16 us
15-2	Define the programmable I/O port address A15-A2.
1-0	00 : Compare A15-A2 for chip select signal PCSJ.(4 bytes) 01 : Compare A15-A3 for chip select signal PCSJ.(8 bytes) 10 : Disable. Chip select signal PCSJ is always inactive('1'). 11 : Compare A15-A4 for chip select signal PCSJ.(16 bytes)

Register Index : **58h**
Register Name : **IDE interface control**
Default Value : 00h

Bit No.	Bit Function
7	Reserved.(must be '0')
6	On-chip IDE controller enable/disable 0 : disable 1 : enable
5-4	IDE IDSEL Address when internal IDE is enabled : 00 : A27 (default) 01 : A26 10 : A25 11 : A24
3	IDE ATA Secondary signal bus pad control 0:disable. i.e. tri-state the secondary channel pins 1:enable. i.e. internal IDE control it.
2	IDE ATA Primary signal bus pad control 0: disable. i.e. tri-state the primary channel pins. 1: enable. i.e. internal IDE control it.
1-0	ATA bus IDE IRQ connection define (H/W connected on Mother Board). Primary IRQ Secondary IRQ 00 : SIRQI SIRQII 01 : IRQ14 IRQ15 10 : IRQ14 SIRQII 11 : IRQ14 SIRQI **Note** : IDE IRQ Hardware Connect: 1. When SIRQI is selected as IDE IRQ input, the SIRQI routing table in cfg_4dh_d[3:0] should be disabled. 2. When SIRQII is selected as IDE IRQ input, the SIRQII routing table in cfg_4dh_d[7:4] should be disabled. 3. When IDE "NATIVE" mode is enabled, "Primary" channel routing table is in cfg_44h_d[3:0]. 4. When IDE "NATIVE" mode is enabled, "Secondary" channel routing table is in cfg_75h_d[3:0].

Register Index : **59h**
Register Name : **General Purpose input multiplexed pin(GPI) select**
Default Value : 00h
These pins will be power off when entering Suspend to DRAM or Suspend to Disk.

Bit No.	Bit Function
7	SMBEVENTJ/GPI[7] select: 0=SMBEVENTJ;1=GPI[7].
6	FPVEE/GPI[6] select: 0=GPI[6];1=FPVEE.
5	VCSJ/GPI[5] select: 0=GPI[5];1=VCSJ.
4	POSSTA/GPI[4] select: 0=GPI[4];1=POSSTA.
3	PCIREQJ/GPI[3] select: 0=PCIREQJ;1=GPI[3].
2	SERIRQ/GPI[2] select: 0=GPI[2];1=SERIRQ.
1	OVCRJ[1]/GPI[1] select: 0=OVCRJ[1];1=GPI[1].
0	OVCRJ[0]/GPI[0] select: 0=OVCRJ[0];1=GPI[0].

Register Index : **5B-5Ah**
Register Name : **General Purpose Output multiplexed pin (GPO) select**.
Default Value : 0000h
These pins will be power off when entering Suspend to DRAM or Suspend to Disk.

Bit No.	Bit Function
15-12	Reserved
11	GPIOWB/GPO[11] select: 0=GPO[11]; 1=GPIOWB.
10	GPIORBJ/GPO[10] select: 0=GPO[10]; 1=GPIORBJ.
9	SQWO/GPO[9] select: 0=SQWO; 1=GPO[9].
8	AMSTATJ/GPO[8] select: 0=AMSTATJ; 1=GPO[8].
7	CONTRAST/GPO[7] select: 0=GPO[7]; 1=CONTRAST.
6	DISPLAY/GPO[6] select: 0=GPO[6]; 1=DISPLAY.
5	CCFT/GPO[5] select: 0=GPO[5]; 1=CCFT.
4	SLOWDWN/GPO[4] select: 0=SLOWDWN; 1=GPO[4].
3	PCI_STPJ/GPO[3] select: 0=PCI_STPJ; 1=GPO[3].
2	CPU_STPJ/GPO[2] select: 0=CPU_STPJ; 1=GPO[2].
1	ZZ/GPO[1] select: 0=ZZ; 1=GPO[1].
0	PCSJ/GPO[0] select: 0=PCSJ; 1=GPO[0].

Register Index : **5D-5Ch**
Default Value : 0000h

Bit No.	Bit Function
15	Enable/disable STPCLKJ mask PHOLDJ 0 : disable 1 : enable
14	On-chip PCI PMU Device enable/disable 0 : enable 1 : disable and PMU configuration register ports are mapping to M1533 registers (7Ch-FFh)
13	Self Refresh at STPCLK enable/disable 0 : enable 1 : disable
12	I/O group F positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
11	I/O group E positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
10	I/O group D positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
9	I/O group C positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
8	I/O group B positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
7	I/O group A positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
6	Parallel I/O ports positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
5	Keyboard I/O ports positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
4	Serial I/O ports positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
3	Floppy I/O ports positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
2	Video I/O ports positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
1	Audio I/O ports positive decode enable/disable when Docking mode (5Ch bit0) is enable. 0 : no response. 1 : positive decode.
0	Docking positive decode mode enable/disable. 0 : All above ports are subtractive decode, when this bit is disable. 1 : All above ports are positive decode or no response, when this bit is enable.

Register Index : **5Eh**
Default Value : 00h

Bit	Description
7	Stop USB PCICLK when entering suspend mode enable/disable. 0 : disable. USB PCICLK is still running during suspend mode. 1 : enable. USB PCICLK is stopped during suspend mode.
6	Stop ISP DMACLK when entering suspend mode enable/disable. 0 : disable. ISP DMACLK is still running during suspend mode. 1 : enable. ISP DMACLK is stopped during suspend mode.
5	Stop ISP PCICLK when entering suspend mode enable/disable. 0 : disable. ISP PCICLK is still running during suspend mode. 1 : enable. ISP PCICLK is stopped during suspend mode.
4-0	Reserved (must be "00000")

Register Index : **5Fh**
Default Value : 00h

Bit	Description
7	Output SYSCLK is stopped during suspend mode enable/disable. 0 : disable. SYSCLK is still running during suspend mode. 1 : enable. SYSCLK is stopped during suspend mode
6	Internal KB clock is stopped during suspend mode enable/disable. 0 : disable. Internal Keyboard clock is still running during suspend mode. 1 : enable. Internal Keyboard clock is stopped during suspend mode.
5	The clock of AT CLOCK DIVIDER is stopped during suspend mode enable/disable. 0 : disable. 1 : enable. All AT clock (including SYSCLK and KBCLK) is stopped during suspend mode.
4	The 14.318 MHz clock of CLKRST circuit is stopped during suspend mode enable/disable. 0 : disable 1 : enable. The 119 KHz of M8254 and cold reset counter are stopped during suspend mode.
3	Bit 9-0 of PCI-to-ISA Bridge configuration Command Register 04h lock/unlock control. 0 : Lock (cannot read/write) 1 : Unlock (can read/write)
2	On-chip arbiter control. 0 : When arbiter is disabled, chip will not mask PHOLDJ and PHLDAJ 1 : When arbiter is disabled, chip will mask PHOLDJ and PHLDAJ
1	The ROM area 4G-1 to 4G-16M(FF000000h-FFFFFFFFh) decode enable/disable. The PCSJ must be pull-low for POWER PC mode. 0 : enable. When accessing this area, pin ROMKBCSJ will be active. 1 : disable.
0	On-chip PCI device INT routing outside for POWER PC enable/disable. 0 : disable. 1 : enable. On-chip IDE INTAJ output via INTBJ/S0 pin; On-chip IDE INTBJ output via INTCJ/S1 pin; On-chip USB INTAJ output via INTDJ/S2 pin; When this bit is enabled, the cfg. 45h bit7 must be '0';

Register Index : **6Bh-60h**
Register Name : **Reserved**

Register Index : **6Ch**.
Register Name : **APIC base address relocation**
Default Value : 00h
The APIC is memory mapped at the locations FEC0_xy00h and FEC0_xy10h(x=0-Fh, y=0,4,8,Ch).

Bit No.	Bit Function
7	Enable/disable burst mode of soft STPCLK. 0 : disable 1 : enable
6	This bit selects one or two I/O APIC address ranges for APICCSJ decode. When this bit is '1', address bit 10 is ignored. When this bit is '0', address bit 10 is used to decode. For example, when bit6=1 and x=0 and y=0, APICCSJ is generated for address FEC0_0000h, FEC0_0010h,as well as FEC0_0400h, FEC0_0410h.
5-2	x address define. These four bits are compared with PCI address AD[15:12], respectively.
1-0	y address define. These two bits are compared with PCI address AD[11:10], respectively.

Register Index : **6Dh**
Default Value : 00h

Bit No.	Bit Function
7	Float ISA output pads when entering suspend mode.(isa_zj) 0 : driving. 1 : floating.
6	Reserved.
5 (0)	Release PCI Bus During ISA DMA Master Cycle Retried by North Bridge 0: Do not release 1: Release This bit is used to control the PHOLDJ assertion when ISA DMA Master cycle has been retried by North Bridge. '0' means PHOLDJ will keep assertion and North Bridge cannot grant the PCI bus to another PCI Master. '1' means M1543 will de-assert PHOLDJ and North Bridge can grant the PCI bus to another PCI Master. Set to '1' is recommended.
4	Reserved.
3-2	On-chip arbiter priority assignment. 00 : Rotate mode. ISA->USB->IDE->D_DMA->APIC->ISA.... 01 : Fixed mode. ISA is highest priority. 10 : Fixed mode. USB is highest priority. 11 : Rotate mode. ISA->USB->IDE->D_DMA->APIC->ISA....
1-0	Output Pins BIOSA17, BIOSA16 mapping when E0000-EFFFF region is accessed and ROM 256KB mode is enabled. 00 : BIOSA17=1; BIOSA16=0 (default) 01 : BIOSA17=0; BIOSA16=1 1x : BIOSA17=0; BIOSA16=0

Register Index : **6Eh**
Register Name : **ISP shadow I/O port select**
Default Value : 00h
The following is preliminary index for accessing shadow ISP ports:

Bit No.	Bit Function
7-5	Select device D7-6-5: 000 : reserved 001 : 8254 programmable timer 010 : Master 8259 011 : Slave 8259 100 : Master 8237 101 : Slave 8237 110 : reserved 111 : reserved
4-0	Select device's ports
	D4D3D2D1D0: (as below) << 8237 >> D4-3-2-1-0: 0 0 0 0 0 : master-37 channel[0] Mode register 0 0 0 0 1 : master-37 channel[1] Mode register 0 0 0 1 0 : master-37 channel[2] Mode register 0 0 0 1 1 : master-37 channel[3] Mode register 0 0 1 0 0 : master-37 Request register & Mask register combined 0 0 1 0 1 : master-37 channel[0] Base Address register Low byte 0 0 1 1 0 : master-37 channel[0] Base Address register High byte 0 0 1 1 1 : master-37 channel[0] Base Word Count register Low byte 0 1 0 0 0 : master-37 channel[0] Base Word Count register High byte 0 1 0 0 1 : master-37 channel[1] Base Address register Low byte 0 1 0 1 0 : master-37 channel[1] Base Address register High byte 0 1 0 1 1 : master-37 channel[1] Base Word Count register Low byte 0 1 1 0 0 : master-37 channel[1] Base Word Count register High byte 0 1 1 0 1 : master-37 channel[2] Base Address register Low byte 0 1 1 1 0 : master-37 channel[2] Base Address register High byte 0 1 1 1 1 : master-37 channel[2] Base Word Count register Low byte 1 0 0 0 0 : master-37 channel[2] Base Word Count register High byte 1 0 0 0 1 : master-37 channel[3] Base Address register Low byte 1 0 0 1 0 : master-37 channel[3] Base Address register High byte 1 0 0 1 1 : master-37 channel[3] Base Word Count register Low byte 1 0 1 0 0 : master-37 channel[3] Base Word Count register High byte Others: reserved

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Bit No.	Bit Function
	D4D3D2D1D0: 0 0 0 0 0 slave-37 channel[0] Mode register 0 0 0 0 1 slave-37 channel[1] Mode register 0 0 0 1 0 slave-37 channel[2] Mode register 0 0 0 1 1 slave-37 channel[3] Mode register 0 0 1 0 0 slave-37 Request register & Mask register combined 0 0 1 0 1 slave-37 channel[0] Base Address register Low byte 0 0 1 1 0 slave-37 channel[0] Base Address register High byte 0 0 1 1 1 slave-37 channel[0] Base Word Count register Low byte 0 1 0 0 0 slave-37 channel[0] Base Word Count register High byte 0 1 0 0 1 slave-37 channel[1] Base Address register Low byte 0 1 0 1 0 slave-37 channel[1] Base Address register High byte 0 1 0 1 1 slave-37 channel[1] Base Word Count register Low byte 0 1 1 0 0 slave-37 channel[1] Base Word Count register High byte 0 1 1 0 1 slave-37 channel[2] Base Address register Low byte 0 1 1 1 0 slave-37 channel[2] Base Address register High byte 0 1 1 1 1 slave-37 channel[2] Base Word Count register Low byte 1 0 0 0 0 slave-37 channel[2] Base Word Count register High byte 1 0 0 0 1 slave-37 channel[3] Base Address register Low byte 1 0 0 1 0 slave-37 channel[3] Base Address register High byte 1 0 0 1 1 slave-37 channel[3] Base Word Count register Low byte 1 0 1 0 0 slave-37 channel[3] Base Word Count register High byte Others : reserved
	<< 8259 >> D4D3D2D1D0: 0 0 0 0 0 master-59 ICW1 0 0 0 0 1 master-59 ICW2 0 0 0 1 0 master-59 ICW3 0 0 0 1 1 master-59 ICW4 0 0 1 0 0 master-59 OCW1 0 0 1 0 1 master-59 reserved (OCW2) 0 0 1 1 0 master-59 OCW3 Others: reserved
	D4D3D2D1D0: 0 0 0 0 0 slave-59 ICW1 0 0 0 0 1 slave-59 ICW2 0 0 0 1 0 slave-59 ICW3 0 0 0 1 1 slave-59 ICW4 0 0 1 0 0 slave-59 OCW1 0 0 1 0 1 slave-59 reserved (OCW2) 0 0 1 1 0 slave-59 OCW3 Others: reserved
	<< 8254 >> D4D3D2D1D0: 0 0 0 0 0 Counter[0] Low byte 0 0 0 0 1 Counter[0] High byte 0 0 0 1 0 Counter[1] Low byte 0 0 0 1 1 Counter[1] High byte 0 0 1 0 0 Counter[2] Low byte 0 0 1 0 1 Counter[2] High byte Others: reserved

Register Index : **6Fh.**
Register Name : **ISP shadow I/O select port data**
Attribute : Read only

Register Index : **70h**
Register Name : **Serial IRQ (IRQSER) Control Register**
Default Value : 12h
Attribute : Read/Write

Bit No.	Bit Function
7	Serial IRQ (IRQSER) Enable/Disable 0 : Disable 1 : Enable
6	Stop Frame Pulse Width 0 : 2 PCICLKs (Quiet mode) 1 : 3 PCICLKs (Continuous mode)
5-2(0000)	Number of IRQ/Data Frames 0000 : 17 Slots 0001 : 18 Slots 0010 : 19 Slots 0011 : 20 Slots 0100 : 21 Slots (default) 0101 : 22 Slots 0110 : 23 Slots 0111 : 24 Slots 1000 : 25 Slots 1001 : 26 Slots 1010 : 27 Slots 1011 : 28 Slots 1100 : 29 Slots 1101 : 30 Slots 1110 : 31 Slots 1111 : 32 Slots
1-0(10)	Start Frame Pulse Width 00 : 4 PCICLKs 01 : 6 PCICLKs 10 : 8 PCICLKs (default) 11 : reserved

Register Index : **71h**
Register Name : **Distributed DMA Channel on PCI or ISA side.**
Default Value : 00h

Bit No.	Bit Function
7	DMA Channel 7 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
6	DMA Channel 6 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
5	DMA Channel 5 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
4	Select de-assert time of STPCLKJ when burst mode of soft STPCLK is enabled (index 6Ch bit 7 =1) 0 : Refer to M7101 Cfg. Space index 0CCh bit2. 1 : 1 - 2 ms.
3	DMA Channel 3 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
2	DMA Channel 2 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
1	DMA Channel 1 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
0	DMA Channel 0 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot

Register Index : **72h**
Register Name : **USB IDSEL mux select**
Default Value : 00h

Bit No.	Bit Function
7	Routing table IRQ output synchronization enable/disable 0 : disable(bypass) 1 : enable (sync by PCICLK)
6	USB PWREN1J and PWREN2J output via pins GPIO[9:8] enable/disable. 0 : disable 1 : enable
5	Repeat Serial IRQ Continuous mode enable/disable. 0 : disable. 1 : enable.
4	Reserved
3-2	PMU IDSEL Address select: 00 : A28 (default) 01 : A29 10 : A30 11 : A31
1-0	USB IDSEL Address when internal USB is enabled: 00 : A31 (default) 01 : A30 10 : A29 11 : A28

Register Index : **73h**
Register Name : **Distributed DMA Base Address**
Default Value : 00h

Bit No.	Bit Function
7-0	Distributed DMA BASE Address.

Register Index : **74h**
Default Value : 00h

Bit No.	Bit Function
7	IOCHRDY driven case during DMA cycle. 0 : IOCHRDY will be driven during DMA cycle. 1 : IOCHRDY will not be driven during DMA cycle.
6	M1533 ISA Bridge Subsystem vendor ID and Subsystem ID (Offset 2F-2Ch). Read only control. 0 : Read/Write 1 : Read only
5	Reserved.
4	On-chip USB master INTAJ level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip USB master INTAJ routing table D3-2-1-0 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **75h**
Default Value : 00h

Bit No.	Bit Function
7-5	Reserved
4	On-chip IDE master Secondary INTBJ level to edge transform enable/disable. 0 : disable.(bypass) 1 : enable.(level -> edge)
3-0	On-chip IDE master Secondary INTBJ routing when native mode is enable. D3 D2 D1 D0 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **76h**
Default Value : 00h

Bit No.	Bit Function
7	SCI routing to IRQ13 enable/disable 0 : enable 1 : disable
6-5	Reserved
4	On-chip PMU system control interrupt(SCI) level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip PMU system control interrupt(SCI) routing table D3 D2 D1 D0 0 0 0 0 : IRQ13 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **77h**
Default Value : 00h

Bit No.	Bit Function
7	SMB I/O base address registers control 0 : Read/Write 1 : Read only and always '0'
6	ACPI I/O base address registers control 0 : Read/Write 1 : Read only and always '0'
5	Reserved.
4	On-chip SMB controller event interrupt level to edge transform enable/disable. 0 : disable.(bypass) 1 : enable.(level -> edge)
3-0	On-chip Smart Battery Bus(SMB) controller event interrupt routing table. D3 D2 D1 D0 0 0 0 0 : disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **FF-78h**
Register Name : **Reserved**

Note : 7Ch-FFh will be mapped by PMU configuration ports 7Ch-FFh, when PMU device is disabled.

4.1.2 IDE Master Configuration Registers (IDSEL = AD27 (default) , AD26, AD25, AD24)

Byte Index	Definition	R/W	Expected Value
1, 0	Vender ID	R	10B9H
3, 2	Device ID	R	5229H
5, 4	Command	R/W	0000H
7, 6	Status	R/W	0280H
8	Revision ID	R	20H
B, A, 9	Class Code	R	0101FAH
0EH	Header Type	R	00H
13H-10H	Base Address Registers	R/W	000001F1H
17H-14H	Base Address Registers	R/W	000003F5H
1BH-18H	Base Address Registers	R/W	00000171H
1FH-1CH	Base Address Registers	R/W	00000375H
23H-20H	Base Address Registers	R/W	0000F001H
2CH	Subsystem Vendor ID	R	00000000H
3CH	Interrupt Line	R/W	00000000H
3DH	Interrupt Pin	R/W	00000001H
3EH	Min_Gnt	R	00000002H
3FH	Max_Lat	R	00000004H

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Register Index : **4Dh**
Register Name : **Configuration register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Read Programming Interface Index 09h Class code bit 4-6 R/W or Read only. 0 : Read/Write 1 : Read Only
6-0	Reserved.

Register Index : **4Fh**
Register Name : **Configuration register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	0 : Default 1 : Master state machine resets when ATA command recommences.
5	0 : Default 1 : The FIFO threshold will be 8.
4	0 : Default 1 : FIFO reset when ATA command recommences.

Register Index : **50h**
Register Name : **Configuration register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-6	Reserved.
5	Only decodes the third byte of BASE2 and BASE4 during native mode 0 : All 4 bytes are master IDE cycle (default) 1 : Only the 3rd byte is master IDE cycle
4	Reserved.
3	CFG_BEJDEC 0 : Decode 3F6H and 376H that only uses address 1 : Use byte enable decode
2	Reserved.
1	Read programming interface index 09h class code bits 6-4 0 : programming interface bits 6-4 are reserved (always 0) 1 : normal read (default)
0	Enable internal IDE function 0 : disable(default) 1 : enable

Register Index : **51h**
Register Name : **Reset and Testing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	CFG_CHIPRST, chip reset Writing a '1' to this bit will reset the whole chip as hardware reset. It generates a one cycle pulse only.
6	CFG_SOFTRST, soft reset Writing a '1' to this bit will reset all the blocks except the configuration space. It generates a one cycle pulse only.
5	CFG_RSTCH2, soft reset Writing a '1' to this bit will reset the ATASTATE and AUTOPOL2. It generates a one cycle pulse only.
4	CFG_RSTCH1, soft reset Writing a '1' to this bit will reset the ATASTATE and AUTOPOL1. It generates a one cycle pulse only.
3	Reserved
2	CFG_ATA_TEST, auto polling Test mode enable 0 : disable(default) 1 : enable
1	CFG_LATEST, latency timer test mode enable 0 : disable(default) 1 : enable
0	CFG_FIFO_TEST, FIFO test mode enable 0 : disable(default) 1 : enable

Register Index : **52h**
Register Name : **CFG_USE_CMDT and Flexible Channel Setting**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Exchange the two hard drives 0 : Channel one is Master IDE and channel two is (Default) Slave IDE when configuring the two channels to the same channel. 1 : Channel two is Master IDE and channel one is Slave IDE when configuring the two channels to the same channel.
6	Bit 6 : Configure the two channels to secondary channel 0: Supports two channel IDE controller (Default) One is primary channel and another is secondary channel. 1: The two channels belong to primary and each channel only supports one hard drive. One channel supports Master drive and another is Slave drive. The two channels can be exchanged by Bit 7.
5	Configure the two channels to primary channel 0 : Supports two channel IDE controller (Default) One is primary channel and another is secondary channel. 1 : The two channels belong to primary and each channel only supports one hard drive. One channel supports Master drive and another is Slave drive. The two channels can be exchanged by Bit 7.
4	Exchange the Two Channels 0 : Channel one is primary channel (Default) and channel two is secondary channel. 1 : Channel two is primary channel and channel one is secondary channel.
3-0	CFG_USE_CMDT bit 0 forces the drive 0 of primary channel to use command block timing register for data transfer. bit 1 forces the drive 1 of primary channel to use command block timing register for data transfer. bit 2 forces the drive 0 of secondary channel to use command block timing register for data transfer. bit 3 forces the drive 1 of secondary channel to use command block timing register for data transfer.

Register Index: **53h**
Attribute : Read/Write

Bit	Description
7	Sub_System Vendor ID accessible or not. 0 : Read/Write 1 : Read Only
6-4, 2	Reserved.
3	Mask Base address during compatibility mode. 0 : unmask 1 : mask (return to '00000000')
1	Buffer On/Off Control 0 : Buffer On 1 : Buffer Off
0	Supports CD_ROM DMA mode 0: Disable (default) 1: Enable

Register Index : **54h**
Register Name : **FIFO threshold of primary channel drive 0 and drive 1**
Default Value : 55h
Default Value : Read/Write

Bit No.	Bit Function
7-6	Operation level. Defines the slave operation level of primary drive 1. 00 : PIO FIFO off, 01 : PIO FIFO on 10 : DMA FIFO on, 11 : Reserved
5-4	FIFO threshold register. Defines when to start master transaction of primary drive 1. 00 : 12 WORDs, 01 : 13 WORDs 10 : 14 WORDs, 11 : 15 WORDs
3-2	Operation level. Defines the slave operation level of primary drive 0. 00 : PIO FIFO off, 01 : PIO FIFO on 10 : DMA FIFO on, 11 : Reserved
1-0	FIFO threshold register. Defines when to start master transaction of primary drive 0. 00 : 12 WORDs, 01 : 13 WORDs 10 : 14 WORDs, 11 : 15 WORDs

Register Index : **55h**
Register Name : **FIFO threshold of secondary channel drive 0 and drive 1**
Default Value : 55h
Attribute : Read/Write

Bit No.	Bit Function
7-6	Operation level. Defines the slave operation level of secondary drive 1. 00 : PIO FIFO off, 01 : PIO FIFO on 10 : DMA FIFO on, 11 : Reserved
5-4	FIFO threshold register. Defines when to start master transaction of secondary drive 1. 00 : 12 WORDs, 01 : 13 WORDs 10 : 14 WORDs, 11 : 15 WORDs
3-2	Operation level. Defines the slave operation level of secondary drive 0. 00 : PIO FIFO off, 01 : PIO FIFO on 10 : DMA FIFO on, 11 : Reserved
1-0	FIFO threshold register. Defines when to start master transaction of secondary drive 0. 00 : 12 WORDs, 01 : 13 WORDs 10 : 14 WORDs, 11 : 15 WORDs

Register Index : **56h**
Register Name : **Ultra DMA /33 setting for Primary drive 0 and drive 1**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Enable Primary Device 1 for Ultra DMA/33 1: Enable 0: Disable
6-4	Ultra DMA/33 cycle time for Primary Device 1 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T
3	Enable Primary Device 0 for Ultra DMA/33 1: Enable 0: Disable
2-0	Ultra DMA/33 cycle time for Primary Device 0 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T

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Register Index : **57h**
Register Name : **Ultra DMA /33 setting for Secondary drive 0 and drive 1**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Enable Secondary Device 1 for Ultra DMA/33 1 : Enable 0 : Disable
6-4	Ultra DMA/33 cycle time for Secondary Device 1 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T
3	Enable Secondary Device 0 for Ultra DMA/33 1 : Enable 0 : Disable
2-0	Ultra DMA/33 cycle time for Secondary Device 0 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T

Register Index : **58h**
Register Name : **Primary channel address setup timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-3	Reserved
2-0	Address setup count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks

Register Index : **59h**
Register Name : **Primary channel command block timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Command active count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Command recovery count 0000 : 16 clks (Default) 0001 : 1 clk 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Ah**
Register Name : **Primary channel Drive 0 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clk 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Bh**
Register Name : **Primary channel Drive 1 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clk 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Ch**
Register Name : **Secondary channel address setup timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-3	Reserved
2-0	Address setup count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks

Register Index : **5Dh**
Register Name : **Secondary channel command block timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Command active count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Command recovery count 0000 : 16 clks (Default) 0001 : 1 clk 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

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Register Index : **5Eh**
Register Name : **Secondary channel Drive 0 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clk 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Fh**
Register Name : **Secondary channel Drive 1 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved.
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clk 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clk 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **60-61h**
Register Name: **Master byte counter for each PRD table entry**
Default Value : 00h
Attribute : Read only

Register Index : **62h**
Register Name : **Latency timer of PCI interface**
Default Value : 00h
Attribute : Read only

Register Index : **63h**
Register Name : **Latency timer expire indicator**
Default Value : 01h
Attribute : Read only

Register Index : **64-65h**
Register Name : **Byte counter for counting in ATA state machine**
Default Value : 0002h
Attribute : Read only

Register Index : **66h**
Register Name : **Sector count counter for counting in ATA state machine**
Default Value : 00h
Attribute : Read only

Register Index : **67h**
Register Name : **Block size counter for counting in ATA state machine**
Default Value : 01h
Attribute : Read only

Register Index : **68h**
Register Name : **Block size register of device 0 on primary channel**
Default Value : 00h
Attribute : read only

Register Index : **69h**
Register Name : **Block size register of device 1 on primary channel**
Default Value 00h
Attribute : read only

Register Index : **6Ah**
Register Name : **Block size register of device 0 on secondary channel**
Default Value 00h
Attribute : Read only

Register Index : **6Bh**
Register Name : **Block size register of device 1 on secondary channel**
Default Value 00h
Attribute : Read only

Register Index : **6Ch**
Register Name : **Primary channel sector count register**
This register is the duplicate of 1F2
Default Value : 00h
Attribute : Read only

Register Index : **6Dh**
Register Name : **Secondary channel sector count register**
This register is the duplicate of 172
Default Value : 00h
Attribute : Read only

Register Index : **6Eh**
Register Name : **Primary channel command register**
This register is the duplicate of 1F7
Default Value: 00h
Attribute : Read only

Register Index : **6Fh**
Register Name : **Secondary channel command register**
This register is the duplicate of 177
Default Value : 00h
Attribute : Read only

Register Index : **70h**
Register Name : **Primary channel byte count low register**.
This register is the duplicate of 1F4
Default Value : 00h
Attribute : Read only

Register Index : **71h**
Register Name : **Primary channel byte count high register**.
This register is the duplicate of 1F5
Default value : 00h
Attribute : Read only

Register Index : **72h**
Register Name : **Secondary channel byte count low register**
This register is the duplicate of 174
Default value : 00h
Attribute : Read only

Register Index : **73h**
Register Name : **Secondary channel byte count high register**
This register is the duplicate of 175
Default Value : 00h
Attribute : Read only

Register Index : **74h**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7	FIFO_OVERRD '1' means error condition occurred that FIFO is over read. This bit must be cleared by reset.
6	FIFO_OVERWR '1' means error condition occurred that FIFO is over written. This bit must be cleared by reset.
5-0	FIFO_FLAG Indicates how many words are in FIFO currently. It is binary coded.

Register Index : **75h**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
3	Secondary channel drive select (the duplicate of 176 bit 4) 0 : select drive 2 1 : select drive 3
2	Primary channel drive select (the duplicate of 1F6 bit 4) 0 : select drive 0 1 : select drive 1
1	Secondary channel interrupt status 0 : no interrupt pending 1 : interrupt pending
0	Primary channel interrupt status 0 : no interrupt pending 1 : interrupt pending

Register Index : **76h**
Register Name :
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
6-4	Secondary channel's status D4 - error D5 - DRQ D6 - busy
2-0	Primary channel's status D0 - error D1 - DRQ D2 - busy

Register Index : **78h**
Register Name :
Default Value : 21h
Attribute : Read/Write

Bit No.	Bit Function
7-0	IDE clock's frequency (default value is 33 = 21H)

4.1.3 USB PCI Configuration Register (IDSEL = AD31(default), AD30, AD29, AD28)

Register Index : **01h-00h**
Register Name : **Vendor ID Register**
Default Value : 10B9h
Attribute : Read only

Bit No.	Bit Function
15-0	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**
Register Name : **Device ID Register**
Default Value : 5237h
Attribute : Read only

Bit No.	Bit Function
15-0	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device.

Register Index **05h-04h**
Register Name : **Command Register**
Default Value 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-10(0h)	Reserved. These bits are always 0.
9(0b)	Back to Back enable. M1533's USB only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8(0b)	Enable the SERRJ driver When this bit is set, M1533's USB will enable SERRJ output driver. This bit is reset to 0 and will set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7(0b)	Wait Cycle Control - M1533's USB does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6(0b)	Respond to Parity Errors If set to 1, M1533's USB will assert PERRJ when it is the agent receiving data and it detects a data parity error. PERRJ is not asserted if this bit is 0.
5(0b)	Enable VGA Palette Snooping This bit is always 0.
4(0b)	Memory Write and Invalidate command If set to 1, M1533's USB is enabled to run Memory Write and Invalidate commands. The Memory Write and Invalidate Command will only occur if the cache line size is set to 32 bytes and the memory write is exactly one cache line.
3(0b)	Enable Special Cycle M1533's USB does not run special cycles on PCI. This bit is always 0.
2(0b)	Enable PCI Master If set to 1, M1533's USB is enabled to run PCI Master cycles.
1(0b)	Enable Response to Memory Access If set to 1, M1533's USB is enabled to respond as a target to memory cycles.
0(0b)	Enable Response to I/O Access If set to 1, M1533's USB is enabled to respond as a target to I/O cycles.

Register Index **07h-06h**
Register Name : **Status Register**
Default Value : 0280h
Attribute : Read only, Write clear

Bit No.	Bit Function
15(0b)	Detected Parity Error. This bit is set by M1533's USB to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14(0b)	SERRJ Status. This bit is set by M1533's USB to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13(0b)	Received Master Abort Status. This bit is set to 1 when M1533's USB, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12(0b)	Received Target Abort Status. This bit is set to 1 when a M1533's USB generated PCI cycle (M1533's USB is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11(0b)	Sent Target Abort Status. This bit is set to 1 when M1533's USB signals target abort. This bit is cleared (reset to 0) by writing a 1 to it.
10-9(01b)	DEVSELJ timing Read only bits indicating DEVSELJ timing when performing a positive decode. 00 : Fast 01 : Medium 10 : Slow Since DEVSELJ is asserted by M1533's USB to meet the medium timing, these bits are encoded as 01b.
8(0b)	Data Parity Reported. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and M1533's USB detects PERRJ asserted while acting as PCI master (whether PERRJ was driven by M1533's USB or not).
7(1b)	Fast Back-to-Back Capable. M1533's USB does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6-0(0h)	Reserved. These bits are always 0.

Register Index : **08h**
Register Name : **Revision ID Register**
Default Value : 03h
Attribute : Read only

Bit No.	Bit Function
7-0(03h)	Functional Revision Level (00000011b)

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Register Index **0B-09h**
Register Name : **Class Code Register**
Default Value 0C0310h
Attribute : Read only

Bit No.	Bit Function
23-0	This register identifies the generic function of M1533's USB the specific register level programming interface. The Base Class is 0Ch (Serial Bus Controller). The SubClass is 03h (Universal Serial Bus). The Programming Interface is 10h (OpenHCI).

Register Index : **0Ch**
Register Name : **Cache Line Size**
Default Value 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0(0h)	This register identifies the system cache line size in units of 32-bit words. M1533's USB will only store the value of bit 3 in this register since the cache line size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

Register Index : **0Dh**
Register Name : **Latency Timer**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0(0h)	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Register Index : **0Eh**
Register Name : **Header Type Register**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register identifies the type of predefined header in the configuration space. Since M1533's USB is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Index : **0Fh**
Register Name : **BIST**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register identifies the control and status of Built In Self Test. M1533's USB does not implement BIST, so this register is read only.

Register Index : **13-10h**
Register Name : **Base Address Register**
Default Value : 00000000h
Attribute : Read/Write

Bit No.	Bit Function
31-12(0h)	Base Address. POST writes the value of the memory base address to this register.
11-4(0h)	Always 0. Indicates a 4K byte address range is requested
3(0b)	Always 0. Indicates there is no support for pre-fetchable memory.
2-1(0h)	Always 0. Indicates that the base register is 32-bit wide and can be placed anywhere in 32-bit memory space.
0(0b)	Always 0. Indicates that the operational registers are mapped into memory space.

Register Index : **2Dh-02Ch**
Register Name : **Subsystem Vendor ID**
Default Value : 0000h
Attribute : Read/Write

Bit	Bit Function
15-0	If the Test Mode Register (index 40h) D20=0, then this register can be Read/Write. Else, this register is Read Only.

Register Index : **2Fh-02Eh**
Register Name : **Subsystem ID**
Attribute : Read/Write
Default Value : 0000h

Bit	Bit Function
15-0	If the Test Mode Register (index 40h) D20=0, then this register can be Read/Write. Else, this register is Read Only.

Register Index : **3Ch**
Register Name : **Interrupt Line Register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0(0h)	This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to M1533's USB.

Register Index : **3Dh**
Register Name : **Interrupt Pin Register**
Default Value : 01h
Attribute : Read only

Bit No.	Bit Function
7-0(01h)	This register identifies which interrupt pin a device uses. Since M1533's USB uses INTAJ, this value is set to 01h.

Register Index **3Eh**
Register Name : **Min Gnt Register**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register specifies the desired settings for how long a burst M1533's USB needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Index **3Fh**
Register Name : **Max Lat Register**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register specifies the desired settings for how often M1533's USB needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Register Index: **43h-40h**
Register Name: **Test Mode Register**
Attribute: Read/Write
Default Value: 00000000h

Bit	Bit Function
31-21	Reserved. Must always write 0's.
20	Subsystem/Vendor ID (Index 2Fh-02Ch) lock bit. 0 : Index 2Fh-02Ch can Read/Write. 1 : Index 2Fh-02Ch is Read Only.
19-0	Reserved. Must always write 0's.

4.1.4 PMU Configuration Registers Description (IDSEL=AD28(default), AD29, AD30, AD31)

All reserved bits are read as 0's

Index-Offset Description
Register Index : **01h-00h**
Register Name : **Vendor ID**
Attribute : Read Only
Default Value : 10B9h

Register Index : **03h-02h**
Register Name : **Device ID**
Attribute : Read Only
Default Value : 7101h

Register Index : **05h-004h**
Register Name : **Command Byte**
Attribute : Read Only
Default Value : 0000h

Bit	Description
15-5	Reserved. Read as 0's ;
4	Caching Command Enable (always '0');
3	Special cycle Enable (always '0');
2	Bus Master Enable (always '0');
1	Memory Space Enable (always '0');
0	I/O Space Enable(R/W). This bit controls the PMU I/O and SMB I/O space registers. The Base address I/O (CFG_10-17) must be programmed before this bit is set.

Register Index : **07h-06h**
Register Name : **Status Byte**

Bit	Description
15	Detected Parity Error. Always '0';
14	Signal System error. Always '0' ;
13	Receive Master Abort When PMU as a master. (Not Implemented, always '0')
12	Receive Target Abort When PMU as a master. (Not Implemented always '0')
11	Signal Target Abort When PMU as a slave. (Not Implemented always '0')
10-9	PMU DEVSELJ Timing. This status of DEVSELJ decode timing as PCI spec. PMU always generates DEVSELJ with medium timing Bit9='1', Bit10='0';
8-0	Reserved. Read as 0's.

Register Index : **08h**
Register Name : **Revision ID**.
Attribute : Read Only
Default Value : 00h

Register Index : **0B-009h**
Register Name : **Class code**. TBD
Attribute : Read Only

Register Index : **0D-00Ch**
Register Name : **Reserved**

Register Index : **0Eh**
Register Name : **Device Type**
Attribute : Read Only
Default Value : (00h) bit7=0 always single-function chip.

Register Index : **13h-010h**
Register Name : **Power Management I/O Base Address**
Default Value : 00000001h

Bit	Description
31-16	Reserved. Must be written as 0000h.
15-6	Corresponds to PMU I/O start address AD[15:6].(64Bytes size)
5-1	Reserved. Read as 0's
0	This bit is always '1', the PMU I/O base address in this register is indicated.

Register Index : **17h-014h**
Register Name : **SMB I/O Base Address**
Default Value : 00000001h

Bit	Description
31-16	Reserved. Must be written as 0000h.
15-5	Corresponds to SMB I/O start address AD[15:5].(32Bytes size)
4-1	Reserved. Read as 0's
0	This bit is always '1', the SMB I/O base address in this register is indicated.

Register Index : **2Bh-00Fh**
Register Name : **Reserved**

Register Index : **2Dh-02Ch**
Register Name : **Subsystem Vendor ID**
Attribute : Read/Write

Register Index : **2Fh-02Eh**
Register Name : **Subsystem ID**
Attribute : Read/Write

Register Index : **3Fh-030h**
Register Name : **Reserved**

Note : There are common status bits for ACPI and Legacy. Including ACPI released SMI.
Note : There are common enable/disable status bits for ACPI and Legacy. Including 4-resume GPSWs, HOTKEY, DOCK, COVSW, RTC, PWRBTNJ, RINGIN, USB, THERMJ, Thermal override and BUS Master.

Register Index : **41h-040h**
Register Name : **SMI enable when ON to Green**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-13	Reserved.
12	Soft SMI, caused by writing IO port 0B1h.
11	IOGP timer timeout SMI.
10	SIO & Audio timer timeout SMI.
9	HDD timer B timeout SMI.
8	HDD timer A timeout SMI.
7	LLB timer timeout SMI.
6	LB timer timeout SMI.
5	APM timer B timeout SMI.
4	APM timer A timeout SMI.
3	RTC SMI, caused by assertion of IRQ8I.
2	PWRBTNJ (Power Button) SMI.
1	Display timer timeout SMI.
0	Standby timer timeout SMI.

Register Index : **43h-042h**
Register Name : **SMI status when ON to Green**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-13	Reserved.
12	Soft SMI, caused by writing IO port 0B1h.
11	IOGP timer timeout SMI.
10	SIO & Audio timer timeout SMI.
9	HDD timer B timeout SMI.
8	HDD timer A timeout SMI.
7	LLB timer timeout SMI.
6	LB timer timeout SMI.
5	APM timer B timeout SMI.
4	APM timer A timeout SMI.
3	RTC SMI, caused by assertion of IRQ8I.
2	PWRBTNJ (Power Button) SMI.
1	Display timer timeout SMI.
0	Standby timer timeout SMI.

Register Index : **46h-044h**
Register Name : **SMI enable when Wake Up.**
Attribute : Read/Write
Default Value : 200000h

Bit	Description
23-21	Reserved.
20	SIRQ access SMI.
19	SMB bus SMI.
18	I/O group F I/O access SMI.
17	I/O group E I/O access SMI.
16	I/O group D I/O access SMI.
15	I/O group C I/O access SMI.
14	I/O group B I/O access SMI.
13	I/O group A I/O access SMI.
12	Parallel Port I/O access SMI.
11	Keyboard I/O access SMI.
10	Serial I/O access SMI.
9	Floppy I/O access SMI.
8	Video I/O access SMI.
7	Audio I/O access SMI.
6	Secondary Driver I/O access SMI.
5	Primary Driver I/O access SMI.
4	Modem RING IN SMI.
3	BUS_Master active SMI.
2	USB access SMI.
1	Display timeout activity SMI.
0	Standby to ON SMI.

Register Index : **47h**
Register Name : **Reserved**.

Register Index : **4Ah-048h**
Register Name : **SMI status when Wake Up.**
Attribute : Read/Write
Default Value : 000000h

Bit	Description
23-22	Reserved.
21	USB bus SMI status. This bit is set when USB needs CPU service.
20	SIRQ access status.
19	SMB bus status.
18	IO group F I/O access status.
17	IO group E I/O access status.
16	IO group D I/O access status.
15	IO group C I/O access status.
14	IO group B I/O access status.
13	IO group A I/O access status.
12	Parallel Port I/O access status.
11	Keyboard I/O access status.
10	Serial I/O access status.
9	Floppy I/O access status.
8	Video I/O access status.
7	Audio I/O access status.
6	Secondary Driver I/O access status.
5	Primary Driver I/O access status.
4	Modem RING IN status.
3	BUS_Master status.
2	USB access status. This bit is set when USB bus is busy.
1	Display timeout activity status.
0	Standby to ON status.

Register Index : **4Bh**
Register Name : **Reserved**.

Register Index : **4Dh-04Ch**
Register Name : **Enable of External Switch SMI.**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-11	Reserved
10	LLBJ rising/falling SMI.
9	LBJ rising/falling SMI
8	THERMALJ high/low toggle SMI.
7	EXTSW in/out SMI
6	SETUPJ in/out SMI
5	Cover Switch in/out SMI.
4	EJECTJ in/out SMI
3	CRT in/out SMI
2	DOCKJ in/out SMI.
1	HOTKEY in/out SMI.
0	AC Power in/out SMI.

Register Index : **4Fh-04Eh**
Attribute : Read/Write
Default Value : 0000h

Status of External Switches' SMI.

Bit	Description
15-11	Reserved
10	LLBJ rising/falling status.
9	LBJ rising/falling status.
8	THERMALJ high/low toggle status.
7	EXTSW in/out status.
6	SETUPJ in/out status.
5	Cover Switch in/out status.
4	EJECTJ in/out status.
3	CRT in/out status.
2	DOCKJ in/out status.
1	HOTKEY in/out status.
0	AC Power in/out status.

Register Index : **51h-050h**
Attribute : Read/Write
Default Value : 0000h

Enable of General Purpose Switches' SMI.

Bit	Description
15-12	Reserved
11	General Purpose I/O SMI 19.
10	General Purpose I/O SMI 18.
9	General Purpose I/O SMI 17.
8	General Purpose I/O SMI 16.
7	General Purpose I/O SMI 15.
6	General Purpose I/O SMI 14.
5	General Purpose I/O SMI 13.
4	General Purpose I/O SMI 12.
3	General Purpose I/O SMI 11
2	General Purpose I/O SMI 10.
1	General Purpose I/O SMI 9.
0	General Purpose I/O SMI 8.

Register Index : **53h-052h**
Register Name : **Status of General Purpose Switch SMI**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-12	Reserved
11	General Purpose I/O SMI 19.
10	General Purpose I/O SMI 18.
9	General Purpose I/O SMI 17.
8	General Purpose I/O SMI 16.
7	General Purpose I/O SMI 15.
6	General Purpose I/O SMI 14.
5	General Purpose I/O SMI 13.
4	General Purpose I/O SMI 12.
3	General Purpose I/O SMI 11
2	General Purpose I/O SMI 10.
1	General Purpose I/O SMI 9.
0	General Purpose I/O SMI 8.

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Register Index : **54h**
Register Name : **Standby timer**.
Default Value : 00h
Attribute : Read/Write
Generate Standby timer timeout SMI when it is timeout and be reset by the Standby monitor events.
Generate Standby to On SMI when the Standby monitor events occurs after timeout. The monitored events are selected at offset 060h-063h.

Bit	Description
7-0	Count. (=0, when disabled) (timebase = 1min)

Register Index : **55h**
Register Name : **APM timer A**
Default Value : 00h
Attribute : Read/Write
Generate APM timer A timeout SMI and stop when timeout. If in repeat mode, timer will be reset to count again after timeout.

Bit	Description
7	Reserved
6	Repeat mode
5-4	Timebase of APM timer A. 00 : 1ms. 01 : 1sec. 10 : 1min. 11 : reserved.
3-0	Count. (=0, when disabled)

Register Index : **56h**
Register Name : **APM timer B.**
Default Value : 00h
Attribute : Read/Write
Generate APM timer B timeout SMI and stop when timeout. If in repeat mode, timer will be reset to count again after timeout.

Bit	Description
7	Reserved.
6	Repeat mode.
5-4	Timebase of APM timer B. 00 : 1ms. 01 : 1sec. 10 : 1min. 11 : reserved.
3-0	Count. (=0, when disabled)

Register Index : **57h**
Register Name : **LB timer**
Default Value : 00h
Attribute : Read/Write
When pin LBJ is asserted, LB timer starts to count. If LBJ is de-asserted before timeout, the timer is reset and stopped. Otherwise, LB timeout SMI will be generated if this timer is timeout.

Bit	Description
7-6	Reserved.
5-4	Timebase of LB timer. 00 : 1sec. 01 : 15sec. 10 : 1min. 11 : reserved.
3-0	Count. (=0, when disabled)

Register Index : **58h**
Register Name : **LLB timer**
Default Value : 00h
Attribute : Read/Write
When pin LLBJ is asserted, LLB timer starts to count. If LLBJ is de-asserted before timeout, the timer is reset and stopped. Otherwise, LLB timeout SMI will be generated if this timer is timeout.

Bit	Description
7-6	Reserved.
5-4	Timebase of LLB timer. 00 : 1sec. 01 : 15sec. 10 : 1min. 11 : reserved.
3-0	Count. (=0, when disabled)

Register Index : **59h**
Register Name : **Global Display timer**.
Default Value : 00h
Attribute : Read/Write
Generate Display timer timeout SMI when it is timeout and be reset by the Display monitor events.
Generate Display timeout activity SMI when the Display monitor events occurs after timeout. The monitored events are selected at offset 064h-065h.

Bit	Description
7-5	Reserved.
4	Timebase of Display timer. 0 : 5sec. 1 : 1min.
3-0	Count. (=0, when disabled)

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Register Index : **5Ah**
Register Name : **HDD timer A**
Default Value : 00h
Attribute : Read/Write

Idle timer for Primary HDD access. If there is any access before timeout, then timer will be reset. Otherwise, HDD timer A timeout SMI is generated. Only writing to this timer can reset it after timeout. The timer monitors 3F6h, 1F0h-1F7h when offset 0D8h-0D9h D7=1. It also monitors internal IDE when the latter is enabled.

Bit	Description
7	Reserved.
6-5	Timebase of HDD timer A. 00 : 15sec. 01 : 30sec. 10 : 1min. 11 : reserved.
4-0	Count. (=0, when disabled)

Register Index : **5Bh**
Register Name : **HDD timer B**
Default Value : 00h
Attribute : Read/Write

Idle timer for Secondary HDD access. If there is any access before timeout, then timer will be reset. Otherwise, HDD timer B timeout SMI is generated. Only writing to this timer can reset it after timeout. The timer monitors 376h, 170h-177h when offset 0D8h-0D9h D7=1. It also monitors internal IDE when the latter is enabled.

Bit	Description
7	Reserved.
6-5	Timebase of HDD timer B. 00 : 15sec. 01 : 30sec. 10 : 1min. 11 : reserved.
4-0	Count. (=0, when disabled)

Register Index : **5Ch**
Register Name : **SIO&Audio timer A.**
Default Value : 00h
Attribute : Read/Write

Idle timer for Super I/O and Audio access. If there is any access before timeout, then timer will be reset. Otherwise, Super IO and Audio timer timeout SMI is generated. Only writing to this timer can reset it after timeout. The monitored events are selected at D0-D4 of offset 66h-67h.

Bit	Description
7	Reserved.
6-5	Timebase of SIO and Audio timer A. 00 : 1ms. 01 : 1sec. 10 : 10sec. 11 : 30sec.
4-0	Count. (=0, when disabled)

Register Index : **5Dh**
Register Name : **IOGP timer**.
Default Value : 00h
Attribute : Read/Write
Idle timer for IO Group and Memory Group Ranges access. If there is any access before timeout, then timer will be reset. Otherwise, IOGP timer timeout SMI is generated. Only writing to this timer can reset it after timeout. The monitored events are selected at D5h-DBh of offset 66h-67h.

Bit	Description
7	Reserved.
6-5	Timebase IOGP timer. 00 : 1ms. 01 : 1sec. 10 : 10sec. 11 : 30sec.
4-0	Count. (=0, when disabled)

Register Index : **05Fh-05Eh**
Register Name : **Reserved**.

Register Index : **063h-060h**
Register Name : **Enable/disable systems events monitored by Standby timer**.
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-27	Reserved.
26	BUS_ACT detected.
25	PCI_REQJ or PHOLDJ asserted.
24	IRQ3-7, IRQ9-15, NMI, INIT or SMIJ asserted.
23	IRQ1 or IRQ12 asserted.
22	IRQ0.
21	PWRBTNJ (Power Button).
20	USB.
19	I/O group F.
18	I/O group E.
17	I/O group D.
16	I/O group C.
15	I/O group B.
14	I/O group A.
13	Memory Group B.
12	Memory Group A.
11	EXTSW.
10	Cover Switch.
9	Modem RING IN.
8	RTC.
7	Parallel Ports.
6	Keyboard.
5	Serial I/O.
4	Floppy.
3	Video.
2	Audio.
1	Secondary HDD.
0	Primary HDD.

Register Index : **65h-064h**
Register Name : **Enable/disable Display events monitored by Display timer**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15	I/O group F.
14	I/O group E.
13	I/O group D.
12	I/O group C.
11	I/O group B.
10	I/O group A.
9	Memory Group B.
8	Memory Group A.
7	Parallel Ports.
6	Keyboard.
5	Serial I/O.
4	Floppy.
3	Video.
2	Audio.
1	Secondary HDD.
0	Primary HDD.

Register Index : **67h-066h**
Default Value : 0000h
Attribute : Read/Write
IDLE timer monitored events' enable/disable.

Bit	Description
15-14	Reserved.
13	I/O group F event for IOGP timer.
12	I/O group E event for IOGP timer.
11	I/O group D event for IOGP timer.
10	I/O group C event for IOGP timer.
9	I/O group B event for IOGP timer.
8	I/O group A event for IOGP timer.
7	Memory Group C event for IOGP timer.
6	Memory Group B event for IOGP timer.
5	Memory Group A event for IOGP timer.
4	Parallel Ports event for SIO and Audio timer.
3	Keyboard event for SIO and Audio timer.
2	Serial I/O event for SIO and Audio timer.
1	Floppy event for SIO and Audio timer.
0	Audio event for SIO and Audio timer.

Register Index : **68h**
Register Name : **Activity Select.**
Default Value : 00h
Attribute : Read/Write
Select the IO ports of parallel port and FDD to be monitored.

Bit	Description
7-3	Reserved.
2-1	Select DRQ of Parallel Port event. 00 : DRQ0. 01 : DRQ1. 10 : DRQ3. 11 : reserved.
0	I/O port of FDD port 0 : 3F0h-3F7h except 3F6h. 1 : 370h-377h except 376h.

Register Index : **6Bh-069h**
Register Name : **Reserved**

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Register Index : **6Fh-06Ch**
Register Name : **Enable/disable of event detected. (Part I)**
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-29	Reserved.
28	Keyboard event detect IRQ12.
27	Keyboard event detect IRQ1.
26	Floppy event detect DRQ2.
25	Video event detect Graphic IO.
24	Video event detect VCSJ pin.
23	Video event detect A-B pages.
22	Video event detect Memory Group range C.
21	Audio event detect DRQ7.
20	Audio event detect DRQ6.
19	Audio event detect DRQ5.
18	Audio event detect DRQ3.
17	Audio event detect DRQ1.
16	Audio event detect DRQ0.
15-12	I/O port of MS_Sound port.
15 14 13 12	Audio event detect F40h-F47h. Audio event detect E80h-E87h. Audio event detect 604h-60Bh. Audio event detect 530h-537h.
11-8	I/O port of SoundB-8/16 port.
11 10 9 8	Audio event detect 280h-293h. Audio event detect 260h-273h. Audio event detect 240h-253h. Audio event detect 220h-233h.
7-4	I/O port of MIDI port.
7 6 5 4	Audio event detect 330h-333h. Audio event detect 320h-323h. Audio event detect 310h-313h. Audio event detect 300h-303h.
3	Audio event detect ADLIB port, 338h-33Bh.
2	Audio event detect GAME port, 200h-207h.
1	Second drive event detect SDRQ.
0	Primary drive event detect PDRQ.

Register Index : **071h-070h**
Register Name : **Enable/disable of event detected. (Part II)**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-14	Reserved.
13-8	Select I/O port for Parallel Port event.
13	IOGPC detect I/O Group range C.
12	IOGPC detect 62h, 66h.
11	Parallel Port event detect DRQ0,1,3.
10	Parallel Port event detect 3BCh-3BEh.
9	Parallel Port event detect 278h-27Fh.
8	Parallel Port event detect 378h-37Fh.
7-0	Select I/O port for Serial port event.
7	Serial Port event detect 338h-33Fh.
6	Serial Port event detect 238h-23Fh.
5	Serial Port event detect 228h-22Fh.
4	Serial Port event detect 220h-227h.
3	Serial Port event detect 2E8h-2EFh.
2	Serial Port event detect 3E8h-3EFh.
1	Serial Port event detect 2F8h-2FFh.
0	Serial Port event detect 3F8h-3FFh.

Register Index : **073h-072h**
Register Name : **Enable/disable of event detected. (Part III)**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-12	Reserved.
11	I/O group B detect GPI(11).
10	I/O group A detect GPI(10).
9	Memory Group B detect GPI(9).
8	Memory Group A detect GPI(8).
7	Parallel Ports detect GPI(7).
6	Keyboard detect GPI(6).
5	Serial IO detect GPI(5).
4	Floppy detect GPI(4).
3	Video detect GPI(3).
2	Audio detect GPI(2).
1	Secondary HDD detect GPI(1).
0	Primary HDD detect GPI(0).

Register Index : **074h**
Register Name : **System wake up status.**
Default Value : 00h
Attribute : Read/Write

The status is set when the occurrence of the corresponding event causes a StandBy to On SMI.

Bit	Description
7-6	Reserved.
5	System wake up by RTC(IRQ8J).
4	System wake up by PWRBTNJ(Power Button).
3	System wake up by EXTSW.
2	System wake up by Cover Switch.
1	System wake up by RING IN.
0	System wake up by DRQ2.

Register Index : **075h**
Register Name : **Time interval to measure Bus activity.**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-0	Count. (timebase = PCICLK).

Register Index : **076h**
Register Name : **Threshold number of TRDYJ detected in the time interval**
Default Value : 00h
Attribute : Read/Write
If the detected number is larger than the threshold number in the time interval as set at offset 75h. Then, an BUS_ACT activity event will be generated.

Bit	Description
7	Reserved.
6	Enable/disable BUS_ACT
5-0	Threshold

Register Index : **077h**
Register Name : **SMI control register (SMI_CNTL)**
Default Value : 00h
Attribute : Read/Write
Note: Only level SMI generated.

Bit	Description
7	Select ACPI mode or M7101 mode. 0 : ACPI mode, status bit is set as soon as event occurs no matter whether the SMI is enabled or not. 1 : M7101 mode, status bit is set if and only if both events occur and the SMI is enabled.
6	SMI acknowledge control 0 : SMIACK de-asserted. 1 : SMIACK asserted.
5	Clear both ACPI and Legacy's status. 0 : Clear status bits will reset both ACPI' and Legacy' status. 1 : Clear status bits only one side.
4	Read/write clear SMI. 0 : The status bit of all status registers can only be cleared by writing '1' to it. 1 : Reading the status registers will clear the registers also.
3	Enable/disable SMI. Decides whether to generate SMI or not.
2	Enable/disable delayed Soft SMI.
1-0	SMI delay time. For AC Power, EXTSW, Cover Switch, CRT, SETUP, HOTKEY, DOCK, EJECT and Soft SMI (option). When the above SMI events occurs, SMI will be generated after the delay timer's timeout. Any monitored events set in standby monitor event en/disable register will reset this timer and delay the SMI again. Refer to Index 0D8h. 00 : no delay. 01 : 125ms. 10 : 250ms. 11 : 500ms.

*Clock management
Register Index : **079h-078h**
Register Name : **PLL timer setting**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-12	Reserved.
11-9	Selection of switching time of SUSPEND to NORMAL. When system switches from SUSPEND to NORMAL, the STPCLKJ control signal cannot de-assert until the refresh circuit is switched to normal refresh. 000 : 0. 001 : 128 us. 010 : 256 us. 011 : 512 us. 100 : 1 ms. 101 : 2 ms. 110 : 4 ms. 111 : 8 ms.
8-6	Selection of switching time of NORMAL to SUSPEND. When system switches from NORMAL to SUSPEND, the OFF_PWR1 signal cannot assert until the refresh circuit is switched to suspend refresh. 000 : 0. 001 : 128 us. 010 : 256 us. 011 : 512 us. 100 : 1 ms. 101 : 2 ms. 110 : 4 ms. 111 : 8 ms.
5-3	Selection of CPU PLL time. When CPU is from STPCLK to STPGNT, STPCLKJ signal should delay for a period of time to de-assert for the stability of internal clock of CPU. 000 : 0. 001 : 256 us. 010 : 512 us. 011 : 1 ms. 100 : 2 ms. 101 : 4 ms. 110 : 64 us. 111 : 128 us.
2-0	Selection of clock generator PLL time. When clock generator changes from off to on, CPU_STPJ and PCI_STPJ signals should delay for a period of time to deassert for the stability of clock when resumed from SLEEP. 000 : 0 ms. 001 : 1 ms. 010 : 2 ms. 011 : 4 ms. 100 : 8 ms. 101 : 16 ms. 110 : 32 ms. 111 : 64 ms.

Register Index : **07Ah**
Register Name : **Slowdown and AMSTATE control**
Default Value : 00h
Attribute : Read/Write
Transition of D0 will assert STPCLKJ first and then change SLOWDOWN after the STPGNT cycle is detected. STPCLKJ will de-assert after the CPU PLL time. If D1 is set, AMSTATJ will assert after the HALT cycle detected.

Note : SLOWDOWN and AMSTATJ always sync. by rising edge of PCICLK.

Bit	Description
7-3	Reserved.
2	Enable/disable Auto Slow Down function. 1 : Enable, when it is enabled, write D0 will not change clock. 0 : Disable.
1	Enable/disable AMSTATE
0	Transition of SLOWDN pin.

Register Index : **07Bh**
Register Name : **STPCLKJ control**
Default Value : 00h
Attribute : Read/Write.

Bit	Description
7-6	Reserved
5	Select High/Low active of Auto Thermal Throttle. 0 : high active. 1 : low active
4	Auto Thermal Throttle enabled.
3	En/disable STPCLK function. Select function when Soft STPCLK enabled(Read IO port 0B2h). When Pentium II is selected (bit 1 of this register), it is used with index CCh bit 3 to decide what CPU state to get into. 0 : Get into STPGNT state when read IO port 0B2h. 1 : Get into STPCLK state when read IO port 0B2h and Pentium selected. If Pentium II is selected and index 0CCh, bit 3=0, Sleep state is selected. If Pentium II is selected and index 0CCh, bit3=1, Deep Sleep state is selected.
2	Software STPCLK enable/disable. 0 : disable 1 : enable
1	Pentium/Pentium II 0 : Pentium 1 : Pentium II
0	Enable/disable ZZ output.

Note : When D4='1' THRMJ='0' for 2 seconds, THROTTLE function will be enabled automatically. Besides, if I/O port 10h D4 (THT_EN='1'), then THROTTLE function will be enabled, too.

	R_LVL2	R_LVL3	STPCLK_EN	Soft_STPCLK
STPGNT	1 0	0 0	X 0	0 1
STPCLK	0 0	1 0	X 1	0 1

Note : All the functions listed above runs only when I/O offset 13h-10h, D9 has enabled.

Register Index : **07Ch**
Register Name : **Break event for STPCLKJ**.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Enable/disable break event of PCI_Master.
6	Enable/disable break event of all devices.
5	Enable/disable break event of PWRBTNJ and Cover Switch.
4	Enable/disable break event of INTR.
3	Enable/disable break event of IRQ1-7, IRQ9-15, NMI, INIT and SMI.
2	Enable/disable break event of IRQ8.
1	Enable/disable break event of IRQ0.
0	Enable/disable break event of PCI Access.

Register Index : **07Dh**
Register Name : **Direction control of GPIO[7:0].**
Default Value : 00h
Attribute : Read/Write
0 : GPIO[n] is a General purpose input pin.
1 : GPIO[n] is a General purpose output pin.

Bit	Description
7	Direction of GPIO[7].
6	Direction of GPIO[6].
5	Direction of GPIO[5].
4	Direction of GPIO[4].
3	Direction of GPIO[3].
2	Direction of GPIO[2].
1	Direction of GPIO[1].
0	Direction of GPIO[0].

Register Index : **07Eh**
Register Name : **Data output to GPIO[7:0] when pin GPIO[n] is set as general purpose output pin**.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Data of GPIO[7].
6	Data of GPIO[6].
5	Data of GPIO[5].
4	Data of GPIO[4].
3	Data of GPIO[3].
2	Data of GPIO[2].
1	Data of GPIO[1].
0	Data of GPIO[0].

Register Index : **07Fh**
Register Name: **Data input from GPIO[7:0] when pin GPIO[n] is set as general purpose input pin.**
Default Value : xxh
Attribute : Read

Bit	Description
7	Data input of GPIO[7].
6	Data input of GPIO[6].
5	Data input of GPIO[5].
4	Data input of GPIO[4].
3	Data input of GPIO[3].
2	Data input of GPIO[2].
1	Data input of GPIO[1].
0	Data input of GPIO[0].

*SWITCH control
Register Index : **082h-080h**
Register Name : **Control of external SWITCH.**
Default Value : 0000_x000_x000_x000_x000_x000b
Attribute : Read/Write

Bit	Description
23-20	Reserved.
19	Status of pin LBJ.
18	Detect rising edge of LBJ.
17	Detect falling edge of LBJ.
16	Enable/disable debounce circuit of LBJ.
15	Status of pin THERMALJ.
14	Detect rising edge of THERMALJ.
13	Detect falling edge of THERMALJ.
12	Enable/disable debounce circuit of THERMALJ.
11	Status of pin EXTSW.
10	Detect rising edge of EXTSW.
9	Detect falling edge of EXTSW.
8	Enable/disable debounce circuit of EXTSW.
7	Status of pin SETUP.
6	Detect rising edge of SETUP.
5	Detect falling edge of SETUP.
4	Enable/disable debounce circuit of SETUP.
3	Status of pin CRT.
2	Detect rising edge of CRT.
1	Detect falling edge of CRT.
0	Enable/disable debounce circuit of CRT.

Register Index : **083h**
Register Name : **Reserved**.

Register Index : **084h**
Register Name : **Control of General Purpose IO 8.**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved
5	Status of pin GPIO[8].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[8]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[8].
1	Detect falling edge of GPIO[8].
0	Enable/disable debounce circuit of GPIO[8].

Register Index : **085h**
Register Name : **Control of General Purpose IO 9.**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved
5	Status of pin GPIO[9].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[9]. Direction of GPIO[9].
1	Detect falling edge of GPIO[9].
0	Enable/disable debounce circuit of GPIO[9].

Register Index : **086h**
Register Name : **Control of General Purpose IO 10**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved
5	Status of pin GPIO[10].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[10]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[10].
1	Detect falling edge of GPIO[10].
0	Enable/disable debounce circuit of GPIO[10].

Register Index : **087h**
Register Name : **Control of General Purpose IO 11**.
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[11].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[11]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[11].
1	Detect falling edge of GPIO[11].
0	Enable/disable debounce circuit of GPIO[11].

Register Index : **088h**
Register Name : **Control of General Purpose IO 12**.
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[12].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[12]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[12].
1	Detect falling edge of GPIO[12].
0	Enable/disable debounce circuit of GPIO[12].

Register Index : **089h**
Register Name : **Control of General Purpose IO 13**.
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[13].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[13]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[13].
1	Detect falling edge of GPIO[13].
0	Enable/disable debounce circuit of GPIO[13].

Register Index : **08Ah**
Register Name : **Control of General Purpose IO 14**.
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[14].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[14]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[14].
1	Detect falling edge of GPIO[14].
0	Enable/disable debounce circuit of GPIO[14].

Register Index : **08Bh**
Register Name : **Control of General Purpose IO 15.**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[15].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[15]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[15].
1	Detect falling edge of GPIO[15].
0	Enable/disable debounce circuit of GPIO[15].

Register Index : **08Eh-08Ch**
Register Name : **Control of external SWITCH. (resume**)
Default Value : x000_x000_x000_x000_x000_x000b
Attribute : Read/Write

Bit	Description
23	Status of pin LLBJ.
22	Detect rising edge of LLBJ.
21	Detect falling edge of LLBJ.
20	Enable/disable debounce circuit of LLBJ.
19	Status of pin HOTKEY.
18	Detect rising edge of HOTKEY.
17	Detect falling edge of HOTKEY.
16	Enable/disable debounce circuit of HOTKEY.
15	Status of pin Cover Switch.
14	Detect rising edge of Cover Switch.
13	Detect falling edge of Cover Switch.
12	Enable/disable debounce circuit of Cover Switch.
11	Status of pin AC Power.
10	Detect rising edge of AC Power.
9	Detect falling edge of AC Power.
8	Enable/disable debounce circuit of AC Power.
7	Status of pin EJECTJ.
6	Detect rising edge of EJECTJ.
5	Detect falling edge of EJECTJ.
4	Enable/disable debounce circuit of EJECTJ.
3	Status of pin DOCKJ.
2	Detect rising edge of DOCKJ.
1	Detect falling edge of DOCKJ.
0	Enable/disable debounce circuit of DOCKJ.

Register Index : **08Fh**
Register Name : **Reserved**.

Register Index : **090h**
Register Name : **Control of General Purpose external SWITCH A. (resume)**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[16].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[16]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[16].
1	Detect falling edge of GPIO[16].
0	Enable/disable debounce circuit of GPIO[16].

Register Index : **091h**
Register Name : **Control of General Purpose external SWITCHB. (resume)**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[17].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[17]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[17].
1	Detect falling edge of GPIO[17].
0	Enable/disable debounce circuit of GPIO[17].

Register Index : **092h**
Register Name : **Control of General Purpose external SWITCH C. (resume)**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved.
5	Status of pin GPIO[18].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[18]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[18].
1	Detect falling edge of GPIO[18].
0	Enable/disable debounce circuit of GPIO[18].

Register Index : **093h**
Register Name : **Control of General Purpose external SWITCH D**. **(resume)**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-6	Reserved
5	Status of pin GPIO[19].
4	Output level for the General Purpose Output pin when D3='1'; 0 : low. 1 : high.
3	Direction of GPIO[19]. 0 : input. The pin serves as a General Purpose Switch pin. 1 : output. The pin serves as a General Purpose Output pin.
2	Detect rising edge of GPIO[19].
1	Detect falling edge of GPIO[19].
0	Enable/disable debounce circuit of GPIO[19].

Register Index : **097h-094h**
Register Name : **Memory Group A**
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-14	Address of A[31:14].
13-4	Mask of address A[23:14].
3-0	Reserved

Register Index : **09Bh-098h**
Register Name : **Memory Group B**
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-14	Address of A[31:14].
13-4	Mask of address A[23:14].
3-0	Reserved

Register Index : **09Fh-09Ch**
Register Name : **Memory Group C** (for Video event)
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-14	Address of A[31:14].
13-4	Mask of address A[23:14].
3-0	Reserved

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Register Index : **0A1h-0A0h**
Register Name : **IO Group A**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-2	Address of A[15:2].
1-0	Mask of address A[3:2].

Register Index : **0A3h-0A2h**
Register Name : **IO Group B**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-2	Address of A[15:2].
1-0	Mask of address A[3:2].

Register Index : **0A5h-0A4h**
Register Name : **IO Group C**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-2	Address of A[15:2].
1-0	Mask of address A[3:2].

Register Index : **0A7h-0A6h**
Register Name : **IO Group D**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-2	Address of A[15:2].
1-0	Mask of address A[3:2].

Register Index : **0A9h-0A8h**
Register Name : **IO Group E**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-2	Address of A[15:2].
1-0	Mask of address A[3:2].

Register Index : **0ABh-0AAh**
Register Name : **IO Group F**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-7	Address of A[15:7].
6-2	Reserved
1-0	Mask of address A[8:7].

Register Index : **0AFh-0ACh**
Register Name : **Reserved**.

*LCD control
Register Index : **0B1h-0B0h**
Register Name : **LCD control**.
CCFT will be active if pin FPVEE is high and D6 is set.
Default Value : 0000h
Attribute : Read/Write
FPVEE, CONTRAST, DISP and CCF are enabled at M1533 CFG_59h bit 6 and CFG_5Ah bit 7-5, respectively. Besides, GPI[7] and GPI[8] are enabled by setting bit 7 of M1533 CFG_59h and pulling high of SQWO.

Bit	Description
15	Enable/disable increasing/decreasing of D13-D8 by pulse of pin INC_CONTRAST/DEC_CONTRAST. 0 : disable (default). 1 : enable. pin GPIO[10] will INC_CONTRAST and GPIO[11] be DEC_CONTRAST.
14	Enable/disable CONTRAST output.
13-8	Duty cycle of CONTRAST.
7	Enable/disable increasing/decreasing of D5-D0 by pulse of pin INC_CCFT/DEC_CCFT. 0 : disable (default). 1 : enable. pin GPI[7] will be INC_CCFT and GPI[8] be DEC_CCFT.
6	Enable/disable CCFT output.
5-0	Duty cycle of CCFT.

Register Index : **0B2h**
Register Name : The current state.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-1	Reserved
0	0 : ON. 1 : Standby

Register Index : **0B3h**
Register Name : **Speaker Control**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Reserved.
6	Enable/disable speak function. 0 : disable speak function. 1 : Enable speak function.
5-4	Latency time of write beep function when writing 0CAh. 00 : 125 ms. 01 : 62.5 ms. 10 : 31.25 ms. 11 : 15.625 ms.
3-2	4 beep function control. 00 : disable 4-beep function. 01 : 4 beeps in 1 sec. 10 : 4 beeps in 2 sec. 11 : 4 beeps in 4 sec.
1-0	Interval time of periodic 4 beep function. 00 : 60 sec. 01 : 30 sec. 10 : 15 sec. 11 : reserved.

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Register Index : **0B4h**
Register Name: **Suspend LED. (resume)**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Reserved.
6-4	Debounce clock of debounce circuits of all external pins. 000 : 128 Hz 001 : 64 Hz 010 : 32 Hz 011 : 16 Hz 100 : 8 Hz 101 : 4 Hz 110 : 2 Hz 111 : 1 Hz
3	Enable power saving of all resume switches and set GPIO 16,17,18 to be level trig. 0 : disable 1 : enable
2	Power Button Override Enable/Disable. 0 : enable 1 : disable
1-0	SUSLED control. Refer to D3h of offset C6h. 00 : low 01 : high 10 : 1 Hz 11 : 2 Hz

Register Index : **0B5h**
Register Name : **LED control**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-4	Reserved.
3-2	SQWO control. 00 : low. 01 : high. 10 : 1HZ. 11 : 2HZ.
1-0	SLED control. 00 : low. 01 : high. 10 : 1HZ. 11 : 2HZ.

Register Index : **0B6h**
Register Name : **Reserved**

Register Index : **0B7h**
Register Name : **Ring counter**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-4	Reserved.
3-0:	Count.

Register Index : **0B9h**-**0B8h**
Register Name: **GPIOW**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-0	Extended General purpose output.

Register Index : **0BBh-0BAh**
Register Name : **GPIORJ**
Default Value : 0000h
Attribute : Read only

Bit	Description
15-0	Extended General purpose input.

Register Index : **0BCh**
Register Name : **Shadow register of IO port 70h.**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-0	This register has the same value of IO port 70h. That is, writing to port 70h will writing to it, too. But, when in SMM, writing to port 70h does not change its value. And the value of port 70h will be updated as its value when exit SMM.

Register Index : **0BDh**
Default Value : 00h
Attribute : Read/Write

Bit	Description
3	PMU Class Code Writable Enable /Disable and ACPI P_CNTRL registers bit 9,13,17 control. 0 : Enable and ACPI P_CNTRL registers can read/write. 1 : Disable and ACPI P_CNTRL registers cannot read/write.
2	Select 24/32 Bits PM Timer 0 : 24 bits. 1 : 32 bits.
1-0	ACPI 24/32 bits timer test mode select (for testing).

Register Index : **0BEh**
Register Name : **Other Configuration**.
Default Value : 00h

Bit	Description
1	Enable power saving of All normal switches. 0 : disable. 1 : enable.
0	Disable internal USB SMIACKJ 0 : Enable. 1 : Disable.

Register Index : **0BFh**
Register Name : **Reserved**.

* GPO and GPI functions
Register Index : **0C2h-0C0h**
Register Name : **Data output to GPO pins.**
Default Value : 000000h
Attribute : Read/Write

Bit	Description
23-21	Reserved.
20	GPO[20]
19	GPO[19]
18	GPO[18]
17	GPO[17]
16	GPO[16]
15	GPO[15]
14	GPO[14]
13	GPO[13]
12	GPO[12]
11	GPO[11]
10	GPO[10]
9	GPO[9]
8	GPO[8]
7	GPO[7]
6	GPO[6]
5	GPO[5]
4	GPO[4]
3	GPO[3]
2	GPO[2]
1	GPO[1]
0	GPO[0]

Register Index : **0C3h**
Register Name : **Output data for GPO[23:21]. (resume)**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-3	Reserved.
2	0 : PWRBTNJ behaves as ACPI definition. 1 : Assert SMIJ are decided at rising edge of PWRBTNJ.
1	Select level/edge trigger of RI signal 0 : level trigger 1 : edge trigger
0	GPO[21].

Register Index : **0C5h-0C4h**
Register Name : **Input data of GPI[11:0].**
Default Value : 0xxxh
Attribute : Read

Bit	Description
15-12	Reserved.
11	GPI[11].
10	GPI[10].
9	GPI[9].
8	GPI[8].
7	GPI[7].
6	GPI[6].
5	GPI[5].
4	GPI[4].
3	GPI[3].
2	GPI[2].
1	GPI[1].
0	GPI[0].

Register Index : **0C6h**
Register Name : **Select Multi-function in Resume block**. **(resume)**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	GPIO[15]/BAT_SEL[3] select. 0 : GPIO[15]. 1 : BAT_SEL[0].
6	GPIO[14]/BAT_SEL[2] select. 0 : GPIO[14]. 1 : BAT_SEL[0].
5	GPIO[13]/BAT_SEL[1] select. 0 : GPIO[13]. 1 : BAT_SEL[0].
4	GPIO[12]/BAT_SEL[0] select. 0 : GPIO[12]. 1 : BAT_SEL[0].
3	GPIO[19]/SUSLED select. 0 : GPIO[19]. 1 : SUSLED.
2	OFF_PWR2/GPO[23] select. 0 : OFF_PWR2. 1 : GPO[23].
1	OFF_PWR1/GPO[22] select. 0 : OFF_PWR1. 1 : GPO[22].
0	OFF_PWR0/GPO[21] select. 0 : OFF_PWR0. 1 : GPO[21].

Register Index : **0C8h**
Register Name : **Mask monitored events of all timers**.
Default Value : 00h
Attribute : Read/Write
0 : Idle timers can be reset by its monitored event.
1 : Idle timers cannot be reset by its monitored event.

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Register Index : **0C9h**
Register Name : **Lock read/write of all configure registers**.
Default Value : 00h
Attribute : Read/Write
0 : All configuration register from offset 040h can be read/write
1 : All configuration registers from offset 040h cannot be read/write except offset 0C9h.

Register Index : **0CAh**
Register Name : **Write Beep Port**. **Write to this port will cause beep**.
Attribute : Write Only

Register Index : **0CBh**
Register Name : **CLKRUN IDLE cycle times select**.
Default Value : 00h
Attribute : Read/Write

Bit	**Description**
3	0 : NO PCI_STPJ occurred when CLKRUN active. 1 : PCI_STPJ asserted when CLKRUN active.
2	0 : Maintain M1533 internal PCICLK when CLKRUN active. 1 : Stop M1533 internal PCICLK when CLKRUN active.
1-0	00 : 26T 01 : 32T 10 : 48T 11 : 64T (T=PL2 clock period)

Register Index : **0CCh**

Bit no.	Description
5	Select de-assert time of SUSTAT1J 0 : SUSTAT1J de-asserted at the moment when CPU_STPJ de-asserted. 1 : SUSTAT1J de-asserted after CPUPLL timer is timeout.
4	Enable/Disable pin SLEEPJ or selection of Deep Sleep /Quick Start 0 : Disable. When Deep Sleep state of Pentium II is selected, CPU will get into Quick Start. 1 : Enable. Sleep/Deep Sleep states are selected.
3	Select Sleep/Deep Sleep when Pentium II is selected 0 : Read ACPI IO index 15h, CPU will get into Sleep state. When index 7Bh bit3=1 and Read IO port 0B2h, CPU will get into Sleep state, too. 1 : Read ACPI IO index 15h, CPU will get into Deep Sleep state. When index 7Bh bit3=1 and Read IO port 0B2h, CPU will get into Deep Sleep state, too.
2	Select de-assert time of STPCLKJ when burst mode is enabled. This bit is valid only when M1533 configuration register index 70h bit 12 =0. 0 : 2ms~4ms 1 : 500 us-1ms
1	0 : No effect. 1 : Any soft STPCLK instruction that occurs when GPI(9) is low will input STPGNT instead of STPCLK.
0	0 : Any soft STPCLK instruction in a master cycle and the last 20 ms will input STPGNT instead of STPCLK. 1 : Any master cycle after the previous soft STPCLK instruction will make the current soft STPCLK input STPGNT instead of STPCLK.

Register Index : **0CFh-0CEh**
Register Name : **Break Events Register**
Default Value : 00h
Attribute : Read/Write
This register is used to select break events for CPU clock control state. The selected events are 'or'ed with what selected in index 7Ch to break CPU from C2-C3 to C0.

Bit	Description
14	Select masked point of INTR/INIT/SMIJ when STPCLKJ is asserted. 0 : All of the three signals are masked as soon as STPCLKJ is asserted. 1 : They are masked after stop grant cycle is received.
15,13-9	Reserved.
8	Select GPI7 (active low) to be break events.
7	Select IRQ1 and IRQ12 to be break events.
6	Select IRQ14 and IRQ15 to be break events.
5	Reserved.
4	Select IRQ9, IRQ10 and IRQ11 to be break events.
3	Select IRQ6 and IRQ7 to be break events.
2	Select IRQ5 to be break events
1	Select IRQ3 and IRQ4 to be break events
0	Reserved

Register Index : **0D1h-0D0h, 0D7h-0D5h**
Register Name : **Reserved**.

Register Index : **0D4h**
Register Name : **Suspend TEST Mode disable/enable**.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-1	Reserved
0	0 : Disable. 1 : Enable.

Register Index : **0D9h-0D8h**
Register Name : **Dummy register**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-8	Reserved.
7	Enable/Disable HDD monitored access of 1F0-1F7h, 3F6h, 170-177h and 376h. 0 : Disable 1 : Enable
6	Enable/Disable of sleeping state stop external PCICLK. 0 : Disable 1 : Enable
5	0 : Disable. 1 : Enable dynamic clock control. When CPU reads soft STPCLK, system will input STPGNT or STPCLK depending on the asserting time of the previous STPCLKJ and PHOLDJ.
4	IRQ1/IRQ12 source select. 0 : IRQ1 & IRQ12. 1 : KBCLK & MSCLK.
3	Enable CPU_STPJ monitor PHOLDJ. 0 : Disable. 1 : Enable. CPU_STPJ will be inactive when PHOLDJ is asserted.
2	Enable delayed SMI of ACPWR and CRT. 0 : Disable. 1 : Enable.
1	Enable delayed SMI of COVSW and HOTKEY. 0 : Disable. 1 : Enable.
0	Enable delayed SMI of all external switches. Except for the following four pins. 0 : Disable. 1 : Enable.

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Register Index : **E0h**
Register Name : **SMBus Host & Slave Interface Configuration**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-2	Reserved
1	Host Slave Interface Enable
0	SMB Host Controller Interface Enable

Register Index : **E1h**
Register Name : **SMBus Host Slave Command Register** : while host being a slave device on the SMBus and the register matches the receiving command data, host generates SMI or Interrupt event.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-0	SMB Host Slave Command port.

Register Index : **E2h**
Register Name : **SMBus Host Controller Base Clock setting**
Default Value : 20h

Bit	Description
7-5	Base Clock Select [7:5] "clock" 000 OSC14M/6 : 2.39M 001 OSC14M/12 : 1.19M (default) 010 OSC14M/24 : 0.60M 100 OSC14M/4 : 3.58M 101 OSC14M/8 : 1.79M 110 OSC14M/16 : 0.89M
4-3	Idle delay setting
	[4:3] "idle time" 00 BaseClk*64 53.76 us ref. 1.19M base clock. (default) 01 BaseClk*32 10 BaseClk*128
2-0	Reserved

Register Index : **E3h**
Register Name : **Reserved**

4.2 Other I/O and Memory Spaces

4.2.1 DMA Register Description.

a. Command Register, the same as 82C37
b. DMA Channel Mode Register, the same as 82C37
c. DMA Channel Extended Mode Register,
Channels 0-3 port address - 040Bh
Channels 4-7 port address - 04D6h

Bit No.	Bit Name	Bit function	Def.
[1-0]	DMA Channel Select	00 Channel 0(4) select 01 Channel 1(5) select 10 Channel 2(6) select 11 Channel 3(7) select	XX
[3-2]	Reserved		00
[5-4]	DMA Cycle Timing Mode	00 Compatible Timing 01 Compatible Timing 10 Compatible Timing 11 Type F	00
[7-6]	Reserved		00

Compatible Timing : runs at 9 SYSCLKs (1080 nsec/ single cycle) and 8 SYSCLKs (960 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode.

Type F Timing : runs at 3 SYSCLKs (360 nsec/single cycle) and 2 SYSCLKs (240 nsec/ cycle) during the repeated portion of a BLOCK or DEMAND mode.

d. DMA Request Register, the same as 82C37
e. Mask Register-Write Single Mask Bit, the same as 82C37
f. Mask Register-Write All Mask Register Bits, the same as 82C37
g. Status Register, the same as 82C37
h. DMA Base and Current Address Register 8237 Compatible Segment
i. DMA Base and Current Byte/Word Count Register 8237 Compatible Segment
j. DMA Memory Low/High Page Register
DMA Memory Base Low Page Register
DMA Channel 0 port address - 087h
DMA Channel 1 port address - 083h
DMA Channel 2 port address - 081h
DMA Channel 3 port address - 082h
DMA Channel 5 port address - 08Bh
DMA Channel 6 port address - 089h
DMA Channel 7 port address - 08Ah
DMA Memory Base High Page Register
(Before using 32-bit addressing, index 42h bit6 must be set to '1')
DMA Channel 0 port address - 487h
DMA Channel 1 port address - 483h
DMA Channel 2 port address - 481h
DMA Channel 3 port address - 482h
DMA Channel 5 port address - 48Bh
DMA Channel 6 port address - 489h
DMA Channel 7 port address - 48Ah
These bits form the full 32-bit address for a DMA transfer.
k. Clear Byte Pointer Flip-Flop, the same as 82C37
l. Master Clear, the same as 82C37
m. Clear Mask Register, the same as 82C37

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4.2.1.2 TIMER UNIT Register Description

a. Timer Control Word Register, the same as 82C54
b. Interval Timer Read Back Command, the same as 82C54
c. Interval Timer Status Byte Format, the same as 82C54
d. Counter Latch Command Register, the same as 82C54
e. Counter Access Ports, the same as 82C54

4.2.1.3 INTERRUPT UNIT Register Description

Initialization Command Word 1 (ICW1) :

Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-5	Reserved.
4	Must be 1.
3	0 : Edge triggered interrupts for all channels 1 : Level triggered interrupts for all channels
2	Reserved
1	0 : Cascade Controller(M1533 must write 0) 1 : Single Controller
0	0 : No ICW4 needed 1 : ICW4 is needed (M1533 must write 1)

Initialization Command Word 2 (ICW2):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-3	Interrupt Vector Address
2-0	Reserved

Initialization Command Word 3 (ICW3):

Port 021h (W/O) -- INT Controller 1

M1533 must be programmed to 04h, indicating INT of CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit No.	Bit Function
7-0	0 : IR Input does not have a slave 1 : IR Input has a slave

Port 0A1h (W/O) -- INT Controller 2

M1533 must be programmed to 02h, indicating CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit No.	Bit Function
7-3	must be 0h
2-0	Slave identification code

Initialization Command Word 4 (ICW4):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-5	must be 0h
4	0 : Not Specially Fully Nested Mode 1 : Specially Fully Nested Mode
3-2	0x : Non Buffered Mode 10 : Buffer Mode/Slave 11 : Buffer Mode/Master
1	0 : Normal EOI 1 : Auto EOI
0	0 : MCS-80/85 Mode 1 : 80x86 Mode (M1533 must write 1)

Operation Command Word 1 (OCW1):

Port 021h (R/W) -- INT Controller 1
Port 0A1h (R/W) -- INT Controller 2

Bit No.	Bit Function
7-0	0 : Reset IRQ<x> mask 1 : Set IRQ<x> mask

Operation Command Word 2 (OCW2):
Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-5	EOI, SL, R 000 : Rotate in Auto EOI Command(Clear) 001 : Non Specific EOI Command 010 : Set Priority Command * L2-L0 are used 011 : * Specific EOI Command 100 : Rotate in Auto EOI Command (Set) 101 : Rotate Non Specific EOI Command 110 : * Set Priority Command 111 : * Rotate on Specific EOI Command
4-3	Must be 00b to select OCW2
2-0	L2,L1,L0 - Interrupt Level Select 000 : IRQ<0(8)> select 001 : IRQ<1(9)> select 010 : IRQ<2(10)> select 011 : IRQ<3(11)> select 100 : IRQ<4(12)> select 101 : IRQ<5(13)> select 110 : IRQ<6(14)> select 111 : IRQ<7(15)> select

Operation Command Word 3 (OCW3) :

Port 020h (R/W) -- INT Controller 1
Port 0A0h (R/W) -- INT Controller 2

Bit No.	Bit Function
7	Reserved, must be 0b.
6-5	0x : No Action 10 : Reset Special Mask Mode 11 : Set Special Mask Mode
4-3	Must be 01b to select OCW3.
2	0 : No Poll Command 1 : Poll Command
1-0	0x : No Action 10 : Read IRQ Register 11 : Read IS Register

Interrupt Unit Edge/Level Control Register (ELCR) :

Port 04D0h (R/W) -- INT Controller 1
Port 04D1h (R/W) -- INT Controller 2

Bit No.	Bit Function
7	0 : IRQ<7(15)> Edge trigger 1 : IRQ<7(15)> Level trigger
6	0 : IRQ<6(14)> Edge trigger 1 : IRQ<6(14)> Level trigger
5	0 : IRQ<5(13)> Edge trigger 1 : IRQ<5(13)> Level trigger
4	0 : IRQ<4(12)> Edge trigger 1 : IRQ<4(12)> Level trigger
3	0 : IRQ<3(11)> Edge trigger 1 : IRQ<3(11)> Level trigger
2	0 : IRQ<2(10)> Edge trigger 1 : IRQ<2(10)> Level trigger
1	0 : IRQ<1(9)> Edge trigger 1 : IRQ<1(9)> Level trigger
0	0 : IRQ<0(8)> Edge trigger 1 : IRQ<0(8)> Level trigger

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4.2.1.4 NMI Registers

NMI Enable/Disable and RTC Address register:

Port 70h, 72h
Attribute : Write Only
Default value 0xxxxxxxb

Bit No.	Bit Function
7	0 : enable NMI interrupt 1 : disable all NMI sources
6-0	RTC Memory addressing

Note : When I/O writes to port 70h or 72h, pin RTCAS will be active. Port 72h is used to support 256 byte RTC.

Port 71h, 73h
Note : When I/O writes to port 71h or 73h, pin RTCRW will be active (low). When I/O reads port 71h or 73h, pin RTCDS will be active (low).

NMI Status and Control register(Port B) :

Port 61h
Attribute : Read/Write
Default value 00h

Bit No.	Bit Function
7 (R only)	0 : No SERRJ from System Board 1 : SERRJ active, NMI requested. To reset this interrupt, set bit 2 to 1.
6 (R only)	0 : No NMI Interrupt from IOCHKJ 1 : IOCHKJ is active and NMI requested. To reset this interrupt, set bit 3 to 1.
5 (R only)	Timer Counter 2 OUT status
4 (R only)	Toggled from 0 to 1 or 1 to 0 following every refresh cycle
3 (R/W)	0 : IOCHKJ NMI enable 1 : IOCHKJ NMI disable and clear
2 (R/W)	0 : System board error enable 1 : System board error disable and clear
1 (R/W)	0 : Pin SPKR output is always '0'. 1 : Pin SPKR output is the Timer Counter 2 OUT signal value.
0 (R/W)	0 : Timer Counter 2 disable 1 : Timer Counter 2 enable

4.2.1.5 FAST RC/GATE-A20 Registers.

Port 92h
Default value : 24h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved (must be read as a 0)
6	Reserved (must be read as a 0)
5	Reserved (must be read as a 1)
4	Reserved (must be read as a 0)
3	Reserved (must be read as a 0)
2	Reserved (must be read as a 1)
1	Directly reflects the A20MJ signal 0 : A20MJ is driven inactive (low) 1 : A20MJ is driven active (high)
0	0 : allow FAST RC to be pulsed 1 : FAST RC is pulsed active

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4.2.2 USB OpenHCI Legacy Registers

Register Index **103h-100h**
Register Name : **HceControl Register**
Default Value : 00000000h
Attribute : Read/Write

Bit No.	Bit Function
31-9(0h)	Reserved. Read as 0. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.
8(0)	A20State. This bit indicates current state of Gate A20 on keyboard controller. This bit is used to compare against value written to 60h when GateA20Sequence is active.
7(0)	IRQ12Active. This bit indicates that a positive transition on IRQ12 from keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
6(0)	IRQ1Active. Indicates that a positive transition on IRQ1 from keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
5(0)	GateA20Sequence. Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC when a data value of FFh is written to I/O port 64h.
4(0)	ExternalIRQEn. When set to 1, IRQ1 and IRQ12 from the keyboard controller will cause an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
3(0)	IRQEn. When set the Host Controller will generate IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated and if it is 1, then an IRQ12 is generated.
2(0)	CharacterPending. When set, an emulation interrupt will be generated when the OutputFull bit of the HceStatus register is set to 0.
1(0)	EmulationInterrupt (Read) This bit is a static decode of the emulation interrupt condition.
0(0)	EmulationEnable. When set to 1, the Host Controller will be enabled for legacy emulation. The Host Controller will decode accesses to I/O registers 60H and 64H and generate IRQ1 and/or IRQ12 when appropriate. Additionally, the host controller will generate an emulation interrupt at appropriate times to invoke the emulation software.

Register Index : **107h-104h**
Register Name : **HceInput Register**
Default Value : 000000xxh
Attribute : Read/Write

Bit No.	Bit Function
31-8(000000h)	Reserved. Read as 0.
7-0(xxh)	InputData. This register holds data that is written to I/O ports 60h and 64h. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

Register Index : **10Bh-108h**
Register Name : **HceOutput Register**
Default Value : 000000xxh
Attribute : Read/Write

Bit No.	Bit Function
31-8(000000h)	Reserved. Read as 0. The contents of the HceStatus Register is returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Access of this register through its memory address produces no side effects.
7-0(xxh)	OutputData. This register hosts data that is returned when an I/O read of port 60h is performed by application software.

Register Index : **10Fh-10Ch**
Register Name : **HceStatus Register**
Default Value : 00000000h
Attribute : Read/Write

Bit No.	Bit Function
31-8(000000h)	Reserved. Read as 0.
7(0)	Parity. Indicates parity error on keyboard/mouse data.
6(0)	Timeout. Used to indicate a time-out
5(0)	AuxOutputFull. IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
4(0)	Inhibit Switch. This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3(0)	CmdData. The HC will set this bit to 0 on an I/O write to port 60h and on an I/O write to port 64h, the HC will set this bit to 1.
2(0)	Flag. Nominally used as a system flag by software to indicate a warm or cold boot.
1(0)	InputFull. Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0(0)	OutputFull. The HC will set this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0 then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1 then and IRQ12 will be generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.

4.2.3 Power Management I/O Space Registers

4.2.3.1 ACPI I/O Registers

The "Base" address is programmed in the PMU PCI DEVICE Configuration Space Offset 10-13h

Register Index : **01h-00h**
Register Name : **Power Management 1 Status Register(PM1_STS)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15	Wakeup Status(WAK_STS) 0 : Cleared by writing '1' to this position. 1 : An enabled resume event occurs when system is in the suspend state.
14-11	Reserved. Read as 0's
10	RTC Status(RTC_STS) 0 : Cleared by writing '1' to this position. 1 : RTC generates an alarm.(IRQ8J Assert)
9	Reserved. Read as 0's
8	Power Button Status(PWRBTN_STS) 0 : Cleared by writing '1' to this position or by Power Button Override condition. 1 : PWRBTNJ is asserted LOW.
7-6	Reserved. Read as 0's
5	Global Status(GBL_STS) 0 : Cleared by writing '1' to this position. 1 : The BIOS wanting the attention of the SCI handler (by writing a ‘1’ to the BIOS_RLS bit).
4	Bus Master Status(BM_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime a system bus master requests the system bus.
3-1	Reserved. Read as 0's
0	Power Management Timer Carry Status(PMTC_STS) 0 : Cleared by writing '1' to this position. 1 : The 22nd (30th) bit of the 24bit (32bit) PM timer goes high to low.

Register Index : **03h-02h**
Register Name : **Power Management 1 Enable Register (PM1_EN)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-11	Reserved. Read as 0's.
10	RTC Enable(RTC_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI, SMI or RSM event is generated anytime the RTC_STS bit is set.
9	Reserved. Read as 0's.
8	Power Button Enable(PWRBTN_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI, SMI or RSM event is generated anytime the PWRBTN_STS bit is set.
7-6	Reserved. Read as 0's.
5	Global Enable(GBL_EN) 0 : When reset, then no SCI event is generated. 1 : When set, then an SCI event is generated anytime the GBL_STS bit is set.
4-1	Reserved. Read as 0's.
0	Power Management Timer Carry Enable(PMTC_EN) 0 : When reset, then no SCI event is generated. 1 : When set, then an SCI event is generated anytime the PMTC_STS bit is set.

Register Index : **05h-04h**
Register Name : **Power Management 1 Control Register (PM1_CNTRL)**
Default Value : 1000h
Attribute : Read/Write

Bit No.	Bit Function
15-14	Reserved. Read as 0's
13	Suspend Enable(SLP_EN) -- Writable and Read as 0 0 : When reset, then no suspend mode is entering. 1 : When set, then causes the system to sequence into the suspend mode defined by the SLP_TYP field.
12-10	Suspend Type(SLP_TYP) This 3-bit field defines the type of hardware suspend mode. The system should enter when SLP_EN bit is set. 100 : Working 011 : Sleeping 010 : Suspend To DRAM 001 : Suspend To DISK 000 : Soft Off others : reserved The SUS_TYP field is used by the BIOS and OS code to determine the suspend mode that system is resuming from. Before entering any low state (LVL2 or LVL3), this field should be programmed to the Working mode.
9-3	Reserved. Read as 0's
2	Global Release(GBL_RLS) 0 : The resource ownership for ACPI software is not released. 1 : Set by ACPI software to raise SMI event to inform BIOS software, the resource ownership is released.
1	Bus Master Break Event Enable(BM_RLD) 0 : When reset then bus master request does not effect the processor state. 1 : When set, bus master request will transition processor from clock control state(C3) to normal state(C0).
0	SCI Enable(SCI_EN) 0 : When reset then these events will generate SMI interrupt. 1 : When set, these events will generate SCI interrupt.

Register Index : **07h-06h**
Register Name : **Reserved**

Register Index : **0Bh-08h**
Register Name : **Power Management 1 Timer Register(PM1_TMR)**
Attribute : Read Only

Bit No.	Bit Function
31-24 :	Extend Power Management Timer Value(E_PMT_VAL) Return the upper eight bits of a 32bits power management timer
23-0	Power Management Timer Value(PMT_VAL) Return the running count of the power management timer currently.

Register Index : **0Fh-0Ch**
Register Name : **Reserved**

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Register Index : **13h-10h**
Register Name : **Processor Control Register(P_CNTRL)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
31-18	Reserved. Read as 0's
17	Throttle Status(THRO_STS) -- R0 0 : The clock control state is outside throttling mode. 1 : The clock control state is in the throttling mode.
16-14	Reserved. Read as 0's
13	Clock Run Enable(CR_EN) 0 : Disable 1 : Enable the M1533 becomes a PCI CLKRUN host Programmable (IDLE CYCLE to stop PCI clock).
12-10	Reserved. Read as 0's
9	Clock Control Enable(CLK_EN) 0 : Disable the clock control function. 1 : Enable the clock control function, read to the LVL2 and LVL3 register will cause M1533 to enter the enabled clock control mode.
8-5	Reserved. Read as 0's
4	Throttle Enable(THRO_EN) 0 : Disable the CPU clock throttling function. 1 : Enable the CPU clock throttling function.
3-1	Throttle Dutysetting Values (THRO_DTY) This 3-bit duty width field (Dutyset) determines the performance of the processor by the following equation. %Performance = Dutyset/ $2^{dutywidth}$ x 100 % Dutyset : %Performance 000 : reserved 001 : 0-12.5% (about 1/8 high and 7/8 low per throttle period) 010 : 12.5-25%(about 2/8 high and 6/8 low per throttle period) 011 : 25-37.5%(about 3/8 high and 5/8 low per throttle period) 100 : 37.5-50%(about 4/8 high and 4/8 low per throttle period) 101 : 50-62.5%(about 5/8 high and 3/8 low per throttle period) 110 : 62.5-75%(about 6/8 high and 2/8 low per throttle period) 111 : 75-87.5%(about 7/8 high and 1/8 low per throttle period)
0	Reserved. Read as 0's

Register Index : **14h**
Register Name : **Processor Level 2 Register (LVL2)**
Default Value : 00h
Attribute : Read Only

Bit No.	Bit Function
7-0	Reads to this register generate an 'enter level 2 power state' to the clock control logic.

Register Index : **15h**
Register Name : **Processor Level 3 Register (LVL3)**
Default Value : 00h
Attribute : Read Only

Bit No.	Bit Function
7-0	Reads to this register generate an 'enter level 3 power state' to the clock control logic.

Register Index : **17h-16h**
Register Name : **Reserved**

Register Index : **19h-18h**
Register Name : **General Purpose Event0 Status Register (GPE0_STS)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-14	Reserved. Read as 0's.
13	HOTKEYJ Status(HOT_STS) 0 : Cleared by writing '1' to this position. 1 : The HOTKEYJ signal is asserted.
12	COVSW Status(COVSW_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the COVSW signal is asserted.
11	RI Status(RING_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the RIJ signal is asserted .
10	ACPWR Status(ACPWR_STS) 0 : Cleared by writing '1' to this position. 1 : The ACPWR signal is asserted.
9	EJECTJ Status(EJECT_STS) 0 : Cleared by writing '1' to this position. 1 : The EJECTJ signal is asserted.
8	DOCKJ Status(DOCK_STS) 0 : Cleared by writing '1' to this position. 1 : The DOCKJ signal is asserted .
7	GPIO(19) Status(GPIO19_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the GPIO19 signal is asserted.
6	GPIO(18) Status(GPIO18_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the GPIO18 signal is asserted.
5	GPIO(17) Status(GPIO17_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the GPIO17 signal is asserted.
4	GPIO(16) Status(GPIO16_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the GPIO16 signal is asserted.
3	Reserved. Read as 0's
2	USB Event Status(USBE_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the USB Event is activated.
1	Thermal Override Status(THEROR_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the THRMJ signal is driven active for greater than 2 seconds, and starts throttling the CPU's clock at the THTL_DTY ratio(when Auto Thermal Throttle Enabled)
0	Thermal Status(THER_STS) 0 : Cleared by writing '1' to this position. 1 : Anytime the THRMJ signal is driven active as defined by the THRM_POL bit.

Register Index : **1Bh-1Ah**
Register Name : **General Purpose Event0 Enable Register (GPE0_EN)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-14	Reserved. Read as 0's
13	HOTKEYJ Enable (HOT_EN) 0 : When reset, then no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the HOT_STS bit is set.
12	COVSW Enable (COVSW_EN) 0 : When reset, no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the COVSW_STS bit is set.
11	RI Enable (RING_EN) 0 : When reset, then no event is generated. 1: When set, an SCI, SMI or RSM event is generated anytime the RING_STS bit is set.
10	ACPWR Enable (ACPWR_EN) 0 : When reset, no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the ACPWR_STS bit is set.
9	EJECTJ Enable (EJECT_EN) 0 : When reset, no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the EJECT_STS bit is set.
8	DOCKJ Enable (DOCK_EN) 0 : When reset, no event is generated. 1 : When set, an SCI,SMI or RSM event is generated anytime the DOCK_STS bit is set.
7	GPIO19 Enable (GPIO19_EN) 0 : When reset, no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the GPIO19_STS bit is set.
6	GPIO18 Enable (GPIO18_EN) 0 : When reset, no event is generated. 1 : When set, an SCI,SMI or RSM event is generated anytime the GPIO18_STS bit is set.
5	GPIO17 Enable (GPIO17_EN) 0 : When reset, no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the GPIO17_STS bit is set.
4	GPIO16 Enable (GPIO16_EN) 0 : When reset, no event is generated. 1 : When set, an SCI, SMI or RSM event is generated anytime the GPIO16_STS bit is set.
3	Reserved. Read as 0's
2	USB Event Enable (USBE_EN) 0 : When reset, no event is generated. 1 : When set, an SCI,SMI or RSM event is generated anytime the USBE_STS bit is set.
1	Thermal Override Enable (THEROR_EN) 0 : When reset, no event is generated. 1 : When set, an SCI or SMI event is generated anytime the THEROR_STS bit is set.
0	Thermal Enable (THER_EN) 0 : When reset, no event is generated. 1 : When set, an SCI or SMI event is generated anytime the THER_STS bit is set.

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Register Index : **1Dh-1Ch**
Register Name : **General Purpose Event1 Status Register (GPE1_STS)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-12	Reserved. Read as 0's
11	IRQ Resume Status (IRQ_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : The IRQ(15-9,7-3,1) signal assert.
10	IRQ0 Resume Status (IRQ0_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : The IRQ0 signal assert.
9-1	Reserved. Read as 0's
0	BIOS Status(BIOS_STS) 0 : Cleared by writing '1' to this position. 1 : ACPI software requesting attention (by writing a '1' to the GBL_RLS bit).

Register Index : **1Fh-1Eh**
Register Name : **General Purpose Event1 Enable Register (GPE1_EN)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15	Low-Low Battery Enable(LLB_EN) 0 : When reset, enabled resume event will resume the system. 1 : When set, the LLBJ signal assertion will prevent the system from resuming upon any enabled resume event.
14-12	Reserved. Read as 0's
11	IRQ Resume Enable(IRQ_RSM_EN) 0 : When reset, no event is generated. 1 : When set, an RSM event is generated anytime the IRQ_RSM_STS is set. (Only in the Sleeping state)
10	IRQ0 Resume Enable(IRQ0_RSM_EN) 0 : When reset, no event is generated. 1 : When set, an RSM event is generated anytime the IRQ0_RSM_STS is set.(Only in the Sleeping state)
9-1	Reserved. Read as 0's
0	BIOS Enable(BIOS_EN) 0 : When reset, no SMI is generated. 1 : When set, the SMI is generated anytime the BIOS_STS is set.

Register Index : **27h-20h**
Register Name : **General Purpose Event1 Control Register (GPE1_CTL)**
Default Value : 0000_0000h
Attribute : Read/Write

Bit No.	Bit Function
31-2	Reserved. Read as 0's
1	BIOS Release(BIOS_RLS) -- R:0 0 : The resource ownership for BIOS software is not released. 1 : Set by BIOS software to raise SCI event to inform ACPI software, the resource ownership is released.
0	Reserved. Read as 0's

Register Index : **2Fh-28h**
Register Name : **Reserved.**

Register Index : **30h**
Register Name : **Power Management 2 Control Register (PM2_CNTRL)**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-1	Reserved. Read as 0's
0	Arbiter Disable (ARB_DIS) 0 : The arbiter is enabled. 1 : The arbiter is disabled and default CPU has ownership of the system.

Register Index : **3Fh-31h**
Register Name : **Reserved.**

4.2.3.2 Advanced Power Management Registers

Register Index : **B1h**
Register Name : **Advances Power Management Access Port (I/O)**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0	Write generates an SMI.

Register Index : **B2h**
Register Name : **Advances Power Management Access Port (I/O)**
Default Value : 00h
Attribute : Read Only

Bit No.	Bit Function
7-0	Read causes the STPCLKJ signal to be asserted.

Register Index : **B3h**
Register Name : **Advances Power Management Status Port (I/O)**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0	Pass Status information between the OS and SMI handler.

4.2.3.3 SMB I/O Space Registers

The "Base" address is programmed in the PMU PCI DEVICE Configuration Space Offset 14-17h

Register Index : **00h**
Register Name : **SMBSTS : SMBus Host/Slave Status Register**
Default Value : 00h
Attribute : (Read/Write, & write '1' clear)

Bit	Description
7	TERMINATE, "1" means the SMB host controller's interrupt (or SMI) was caused by a terminated bus transaction in response to "ABORT".
6	BUS_COLLI, Bus Collision, "1" means the SMB host controller's interrupt (or SMI) was caused by the collision of bus transaction.
5	DEVICE_ERR, Device Error, "1" means the SMB host controller's interrupt (or SMI) was caused by the SMB controller or device due to the generation of an error.
4	SMI_I_STS, "1" means that the SMB host controller's Interrupt (or SMI) was caused by the SMB controller after completing a command.
3	HST_BSY, Host Controller Busy, "1" means that the SMB host controller is going to complete a command. (RO)
2	IDL_STS, "1" means SMBus at Idle Status. (RO)
1	HSTSLV_STS, Host Slave Status, "1" means the SMB host controller's interrupt (or SMI) was caused by the host SMB slave interface.
0	HSTSLV_BSY, Host Slave Busy, "1" means that SMB slave interface is going to receive a command. (RO)

Register Index : **01h**
Register Name : **SMBCMD : SMBus Host/Slave Command**
Default Value : 00h
Attribute : Write Only

Bit	Description
7	SMB_BLK_CLR, SMB Block Register Pointer Reset, to reset block register's pointer.(WO)
6-4	SMB_COMMAND, SMB Command, indicates which kind of command is asked to perform. (R/W) [6:4] Command 000 Quick command 001 Send/Receive Byte 010 Write/Read Byte 011 Write/Read Word 100 Write/Read Block
3	T_OUT_CMD, like "Abort" command, it (WO) performs the Time Out condition on the SMBus to reset not only Host controller but also other devices on the SMBus. -->DEVICE_ERR
2	Abort, reset Host controller. --> TERMINATE (WO)
1-0	Reserved

Register Index : **02h**
Register Name : **STRT_PRT : I/O Port to Start to generate the programmed cycle on the SMBus**
Default Value : 00h
Attribute : Write

Register Index : **03h**
Register Name : **SMBus Address Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **04h**
Register Name : **SMBus DataA Register for Host Controller**
Default Value : 00h
Attribute : Read/Write
This register should be programmed with the value that will be transmitted in DataA field of the SMBus host interface transaction protocol. It means the count of block registers for a block write and read command.

Register Index : **05h**
Register Name : **SMBus DataB Register for Host Controller**
Attribute : Read/Write
Default Value : 00h
This register should be programmed with the value that will be transmitted in DataB field of the SMBus host interface transaction protocol.

Register Index : **06h**
Register Name : **SMBus Block Register for Host Controller**
Attribute : Read/Write
Default Value : 00h
This register is used to access 32-byte block data for block write and read SMBus protocol. Before reading or writing to this register, to set the block register index to 0 is needed. It is done by writing '1' to SMB_BLK_CLR in SMB I/O Space Register index 01h.

Register Index : **07h**
Register Name : **SMBus Command Register for Host Controller**
Default Value : 00h
Attribute : Read/Write
This register should be programmed with the value that will be transmitted in the command field of the SMBus host interface transaction protocol.

Register Index : **08h ~ 09h**
Register Name : **Status 1 : Polling status for battery 1**
Default Value : 00h
Attribute : Read/Write

Register Index : **0Ah ~ 0Bh**
Register Name : **Status 2 : Polling status for battery 2**
Default Value : 00h
Attribute : Read/Write

Register Index : **0Ch ~ 0Dh**
Register Name : **Status 3 : Polling status for battery 3**
Default Value : 00h
Attribute : Read/Write

Register Index : **0Eh ~ 0Fh**
Register Name : **Status 4 : Polling status for battery 4**
Default Value : 00h
Attribute : Read/Write

Register Index : **10h ~ 11h**
Register Name : **R_TIME1 : Polling remaining time for battery 1**
Default Value : 00h
Attribute : Read/Write

Register Index : **12h ~ 13h**
Register Name : **R_TIME2 : Polling remaining time for battery 2**
Default Value : 00h
Attribute : Read/Write

Register Index : **14h ~ 15h**
Register Name : **R_TIME3 : Polling remaining time for battery 3**
Default Value : 00h
Attribute : Read/Write

Register Index : **16h ~ 17h**
Register Name : **R_TIME4 : Polling remaining time for battery 4**
Default Value : 00h
Attribute : Read/Write

Register Index : **18h ~ 19h**
Register Name : **R_CAP 1 : Polling remaining capacity for battery 1**
Default Value : 00h
Attribute : Read/Write

Register Index : **1Ah ~ 1Bh**
Register Name : **R_CAP2 : Polling remaining capacity for battery 2**
Default Value : 00h
Attribute : Read/Write

Register Index : **1Ch ~ 1Dh**
Register Name : **R_CAP3 : Polling remaining capacity for battery 3**
Default Value : 00h
Attribute : Read/Write

Register Index : **1Eh ~ 1Fh**
Register Name : **R_CAP4 : Polling remaining capacity for battery 4**
Default Value : 00h
Attribute : Read/Write

4.2.3.4 PCI IDE Controller I/O Space Registers Definition.
The Primary and Secondary Channel can be disabled by setting Byte 09h.
Byte 09h - D7 - Bus master IDE
0 : No, it is not a bus master IDE.
1 : Yes, it is a Bus master IDE.

Byte 09h - D6 - Report IDE channel status
0 : No, this is the default zero value of PCI 2.1 specification.
1 : Yes, D4-5 can be queried to determine status of the IDE controller.

Byte 09h - D5 - Primary Channel
0 : No, the Primary channel is disabled.
1 : Yes, the Primary channel is enabled.

Byte 09h - D4 - Secondary Channel
0 : No, the Secondary channel is disabled.
1 : Yes, the Secondary channel is enabled.

Byte 09h - D3 - Secondary channel support
0 : compatibility only
1 : both compatibility and native mode.

Byte 09h - D2 - Operation of Secondary channel
0 : compatibility mode
1 : Native mode
Byte 09h - D1 - Primary channel support
0 : compatibility only.
1 : both compatibility and native mode.
Byte 09h - D0 - Operation of Primary channel
0 : compatibility mode
1 : Native mode

2. The PIO Mode IDE I/O Space Define.

a. Compatibility Mode.
Primary channel I/O space is from 1F0H to 1F7H and 3F6H. Secondary channel I/O space is from 170H to 177H and 376H.
b. Native Mode.
Primary Channel I/O space can be programmed at 10H and 14H. The I/O range is 8bytes described at 10H and 1 byte described at 14H. Secondary Channel I/O space can be programmed at 18H and 1CH. The I/O range is 8 bytes that are described at 18H and 1 byte is described at 1Ch.

3. Bus Master IDE Register Description.

The Bus master IDE function uses 16 bytes of I/O space. All bus master IDE I/O space can be accessed as byte, word, or Dword quantities. The description of the 16 bytes of I/O registers are as follows :

Offset from Base Address	Register	Register Access
00h	Bus Master IDE Command Register Primary	R/W
01h	Device Specific	
02h	Bus Master IDE Status Register Primary	RWC
03h	Device Specific	
04h-07h	Bus Master IDE PRD Table Address Primary	R/W
08h	Bus Master IDE Command Register Secondary	R/W
09h	Device Specific	
0Ah	Bus Master IDE Status Register Secondary	RWC
0Bh	Device Specific	
0Ch-0Fh	Bus Master IDE PRD Table Address Secondary	R/W

a. Register Name: Bus Master IDE Command register
Address Offset:
Primary Channel - Base address defined in 20H + 00H
Secondary Channel - Base address defined in 20H + 08H
Base address : F001H
Default Value : 00H
Attribute : Read/Write
Size : 8 bits

Bit	Description
7-4	Reserved. must be 0.
3	Read or Write Control. This bit sets the direction of the bus master transfer. 0 : PCI bus master read 1 : PCI bus master write. This bit must not be changed when the bus master function is active.
2-1	Reserved. must be 0.
0	Start/Stop Bus Master. Writing a '1' to this bit enables bus master operation of the controller. Bus Master operation begins when this bit is detected changing from a zero to a one. The controller will transfer data between the IDE device and memory only when this bit is set. Writing a '0' to this bit can halt master operation. All state information is lost when a '0' is written; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active and the drive has not yet finished its data transfer, the bus master command is aborted and data transferred from the drive may be discarded before being written to system memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE active bit or the interrupt bit of the Bus master IDE status register for that IDE channel being set, or both.

b. Register Name: Bus Master IDE Status Register Address Offset :
Primary Channel - Base address defined in 20H + 02H
Secondary Channel - Base address defined in 20H + 0AH
Base Address : F001H
Default Value: 00H
Attribute: Read/Write
Size: 8 bits

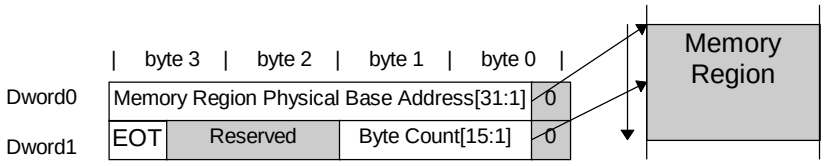
Bit	Description
D7	**Simplex Only**. (RO) This bit indicates whether or not both bus master channels (primary and secondary) can be operated at the same time. 0 : channels operate independently and can be used at a time. 1 : only one channel can be used at a time.
D6	**Drive 1 DMA capable**. (R/W) This bit is set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
D5	**Drive 0 DMA capable**. (R/W) This bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
D4-D3	Reserved. must be 0.
D2	**Interrupt**. This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a '1' is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is one, all data transferred from the drive is visible in system memory.
D1	**Error**. This bit is set when the controller encounters an error in transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a '1' is written to it by software.
D0	**Bus Master IDE active**. This bit is set when the Start bit is written to the Command Register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.

c. Register Name : Descriptor Table Pointer Register
Primary Channel - Base address defined in 20H + 04H
Secondary Channel - Base address defined in 20H + 0CH
Base address : F001H
Default Value : 00000000H
Attribute : Read/Write
Size : 32 bits

Bit	Description
D31-2	Base address of Descriptor table. Corresponds to A[31:2]
D1-0	Reserved.

4. The Physical Region Descriptor Table

Before the controller starts a master transfer it is given a pointer to a Physical Region Descriptor Table. This table contains some number of Physical Region Descriptor (PRD) which describes areas of memory that are involved in the data transfer. The PRD table must be aligned on a 4-byte boundary and the table cannot cross a 64K boundary in memory. The EOT is "END of TABLE". It means that this transaction is ending.



4.3 ISA Compatible Registers Summary :

The ISA compatible registers of the M1533 are summarized as below:

I/O Address	Attribute	Register Name
0000h	Read/Write	DMA1 (slave) CH0 Base and Current Address
0001h	Read/Write	DMA1 (slave) CH0 Base and Current Count
0002h	Read/Write	DMA1 (slave) CH1 Base and Current Address
0003h	Read/Write	DMA1 (slave) CH1 Base and Current Count
0004h	Read/Write	DMA1 (slave) CH2 Base and Current Address
0005h	Read/Write	DMA1 (slave) CH2 Base and Current Count
0006h	Read/Write	DMA1 (slave) CH3 Base and Current Address
0007h	Read/Write	DMA1 (slave) CH3 Base and Current Count
0008h	Read/Write	DMA1 (slave) Status(R)/Command(W)
0009h	Write-only	DMA1 (slave) Write Request
000Ah	Write-only	DMA1 (slave) Write Single Mask Bit
000Bh	Write-only	DMA1 (slave) Write Mode
000Ch	Write-only	DMA1 (slave) Clear Byte Pointer
000Dh	Write-only	DMA1 (slave) Master Clear
000Eh	Write-only	DMA1 (slave) Clear Mask
000Fh	Read/Write	DMA1 (slave) Read/Write All Mask Register Bits
0020h	Read/Write	INT_1 (master) Control Register
0021h	Read/Write	INT_1 (master) Mask Register
0040h	Read/Write	Timer Counter - Channel 0 Count
0041h	Read/Write	Timer Counter - Channel 1 Count
0042h	Read/Write	Timer Counter - Channel 2 Count
0043h	Read/Write	Timer Counter Command Mode Register
0060h	Read_access	Clear IRQ12 (for PS2), IRQ1 Latched Status
0060h	Read/Write	Keyboard Data Buffer
0061h	Read/Write	NMI and Speaker Status and Control
0064h	Read/Write	Keyboard Status(R)/Command(W)
0070h	Write-only	CMOS RAM Address Port and NMI Mask Register
0071h	Read/Write	CMOS Data Register Port
0081h	Read/Write	DMA Channel 2 Page Register
0082h	Read/Write	DMA Channel 3 Page Register
0083h	Read/Write	DMA Channel 1 Page Register
0087h	Read/Write	DMA Channel 0 Page Register
0089h	Read/Write	DMA Channel 6 Page Register
008Ah	Read/Write	DMA Channel 7 Page Register
008Bh	Read/Write	DMA Channel 5 Page Register
008Fh	Read/Write	Refresh Address Register for Address 23 to 17

The ISA compatible registers of M1533 (continued)

I/O Address	Attribute	Register Name
00A0h	Read/Write	INT_2 (slave) Control Register
00A1h	Read/Write	INT_2 (slave) Mask Register
00C0h	Read/Write	DMA2 (master) CH0 Base and Current Address
00C2h	Read/Write	DMA2 (master) CH0 Base and Current Count
00C4h	Read/Write	DMA2 (master) CH1 Base and Current Address
00C6h	Read/Write	DMA2 (master) CH1 Base and Current Count
00C8h	Read/Write	DMA2 (master) CH2 Base and Current Address
00CAh	Read/Write	DMA2 (master) CH2 Base and Current Count
00CCh	Read/Write	DMA2 (master) CH3 Base and Current Address
00CEh	Read/Write	DMA2 (master) CH3 Base and Current Count
00D0h	Read/Write	DMA2 (master) Status(R)/Command(W)
00D2h	Write-only	DMA2 (master) Write Request
00D4h	Write-only	DMA2 (master) Write Single Mask Bit
00D6h	Write-only	DMA2 (master) Write Mode
00D8h	Write-only	DMA2 (master) Clear Byte Pointer
00DAh	Write-only	DMA2 (master) Master Clear
00DCh	Write-only	DMA2 (master) Clear Mask
00DEh	Read/Write	DMA2 (master) Read/Write All Mask Register Bits
00F0h	Write-only	Coprocessor Error Ignored Register
040Bh	Write only	DMA1 Extended Mode Register
0481h	Read/Write	DMA CH2 High Page Register
0482h	Read/Write	DMA CH3 High Page Register
0483h	Read/Write	DMA CH1 High Page Register
0487h	Read/Write	DMA CH0 High Page Register
0489h	Read/Write	DMA CH6 High Page Register
048Ah	Read/Write	DMA CH7 High Page Register
048Bh	Read/Write	DMA CH5 High Page Register
04D0h	Read/Write	INT_1 (master) Edge/Level Control
04D1h	Read/Write	INT_2 (slave) Edge/Level Control
04D6h	Write only	DMA2 Extended Mode Register

Section 5 : Power Management Unit Programming Guide

There are two important parts in Power Management Unit of M1533. They are Legacy Power Management Unit and Advanced Configuration and Power Interface Specification (abbreviated as ACPI). The details of both are listed below.

5.1 Legacy Power Management Unit

A. Top View.
B. Timers.
C. Event Configuration.
D. External Switches.
E. Clock Control.
F. Display Control.
G. Low Battery.
H. General Purpose Input/ Output.
I. SMI control.
J. Others.

A. Top View.
The Legacy Power Management Unit based on the default functions of M7101, gives a more powerful function than the latter. It can be divided into several parts.

When talking about the traditional power management, as it is familiar to every one, the SMI or SMM. It is the major method of how the BIOS communicate with the hardware. The SMI sources are all included in Configuration Space of offset 0x40h-0x53h. ('Offset 0xxxh' means the registers of Configuration Space in Section 5.1 of this document.) There are eight idle timer timeout SMIs, two APM timer timeout SMIs, IO traps, external switches SMIs and general purpose switch SMIs. The configuration of all timers is at offset 0x54h-0x5Dh. The monitored events of the timers and the IO traps are set at offset 0x60h-0x73h. Offset 0x74h is the status bit that indicates which event resets the Standby timer when system is in Standby State. Offset 0x75h-0x76h configures the busy condition of the PCI bus. The External Switches' event is configured at offset 0x80h-0x93h. Furthermore, the programmable monitored IO/Memory range can be set at offset 0x94h-0xABh.

Besides the SMI sources and the monitored events, CPU clock control is also an important method for power saving. M1533 supports Pentium and Pentium Pro clock control. It can transfer the CPU into STPGNT or STPCLK states. Besides, system clock controls such as clock throttling and Slowdown function are also supported. Most of all, the Auto Thermal throttling can be enabled to prevent system overheat. All of the configuration registers are at 0x78h-0x7Ch. Note that some configuration registers of throttling are set at offset 0x10h-0x13h of ACPI IO space. In addition to the above listed, PCI Clock Run function can be enabled/disabled at offset 0xCBh.
Some other functions, such as Display Control and Speaker, etc., are set at offset 0B2h-0BEh.
Most important of all is the Suspend states supported. There are three states supported by M1533, namely the Power On Suspend, Suspend to DRAM and Suspend to Disk. An overview of design for suspend is introduced at ACPI.
The details of how to design the hardware or program the registers are described below.

B. Timers.

a. Standby timer and System state.
There are two states, ON & STANDBY, in this chip. The transition between both is determined by Standby timer and what events it monitors. The monitored events can be selected at offset 0x60h-0x64h and the Standby timer can be programmed at offset 0x54h. Assume Standby timer is programmed as 27 minutes and the monitored events as 01h. Then the timer begins to count immediately after being programmed. If there is any Primary HDD access (the enabled monitored event) detected before timeout, the timer will be reset. Otherwise, if it is timeout because no event occurs, it will stop and the system will transfer to STANDBY state. At the same time, the Standby timeout SMI is generated. If there is an event detected in STANDBY state, the timer will be reset to count again and a STANDBY to ON SMI will be generated. As soon as the SMI is generated, system will transfer to ON state. By the way, reading or writing at offset 0xB2h, D0, can change system states.

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b. Display timer.
This timer is similar to the Standby timer except that it has no relation with the System state. If there is an enabled Display access event detected, the timer will be reset immediately no matter what state it is in. The only difference is that the Display timeout SMI is generated when no events are detected and the timer timeout, and Display Activity SMI is generated when there is an event detected after timeout. The timer can be configured at offset 0x59h and the monitored events at offset 0x64h-0x65h.
c. Idle timers.
There are four idle timers that monitor the different group of devices. HDD A timer monitors the Primary HDD access and HDD B monitors the Secondary HDD access. SIO&AUDIO timer monitors Super IO ports and Audio ports set at offset 0x66h-0x67h, D4-D0. Moreover, IOGP timer monitors Memory Groups and IO Groups programmed at offset 094h-0ABh. All of the timers can be reset by writing the timer or occurring of its monitored events before timeout. Only writing to timer can reset it after timeout. When any one of them is timeout, its own timeout SMI will be generated. By the way, the timers can be programmed at offset 0x5Ah-0x5Dh. The events they monitor can be set at 0x66h-0x67h.
d. APM timers.
There are two APM timers that can be used for Advanced Power Management. Each has two modes. When offset 0x55h(0x56h), D6='0', the timer will generate an SMI when timeout and then stop until it is written again. When D6='1', the timer would reset to count again when timeout and generate SMI. Both timers can be programmed at offset 0x55h and 0x56h.

List of timers :

a. Standby timer - PMU Cfg. 54h
b. Display timer - PMU Cfg. 59h
c. APM timer A - PMU Cfg. 55h
d. APM timer B - PMU Cfg. 56h
e. HDD A timer - PMU Cfg. 5Ah
f. HDD B timer - PMU Cfg. 5Bh
g. SIO and Audio timer - PMU Cfg. 5Ch
h. IOGP timer - PMU Cfg. 5Dh
i. LB timer - PMU Cfg. 57h
j. LLB timer - PMU Cfg. 58h

Note : All of the events monitored by the idle timers are masked when offset 0xC8h is set.

C. Event Configuration.
There are more than twenty events that should be configured before use. Listed below are those devices. Besides, twelve devices can monitor another GPI pin as an input event. Refer to offset 0x72h-0x73h.

a. Primary HDD.
This event monitors 01F0h-01F7h and 3F6h always. When internal IDE is enabled, any IO cycle accessing it would be monitored, too. Besides, Primary DRQ can be enabled/disabled to be monitored at D0 of offset 0x6Ch.

b. Second HDD.
This event monitors 0170h-0177h and 376h always. When internal IDE is enabled, any IO cycle accessing it would be monitored, too. Besides, Secondary-DRQ can be enabled/disabled to be monitored at D1 of offset 0x6Ch.

c. Audio.
The audio access is decided by monitoring accesses to MIDI, SoundBlaster, MS_Sound, ADLIB and GAME ports which are selected at D2-D15 of offset 0x6Ch-0x6Fh. Besides, whether DRQ is monitored or not is decided at D16-D21 of offset 0x6Ch-0x6Fh.

d. Video.
There are four sources of Video Events, including MEMGPC Range, Memory access A0000-BFFFF, VCSJ and Graphic IO (3B0h-3DFh). As MEMGPC Range is a programmable memory range, it can be configured at 09Ch-09Fh. The programming steps are listed in Memory Group. VCSJ is an low active pin.

e. FDD.
The default monitor range of FDD Event is 3F0h-3F7h except 3F6h. It can be changed to 370h-377h except 376h by writing '1' to D0 of offset 0x68h. Besides, whether DRQ2 would be monitored is decided at D26 of offset 0x6Ch-0x6Fh.

f. Serial IO.
There is a maximum of eight COM ports to be monitored. They can be enable/disable individually at D0-D7 of offset 0x70h.

g. Keyboard.
IO access ports 060h and 064h will generate Keyboard Event. Moreover, enabling D27-D28 of offset 0x6Ch-0x6Fh can monitor IRQ1 or IRQ12.

h. Parallel IO.

Parallel IO Event monitors D8-D11 of offset 070h-071h. Note that only one of DRQ0, DRQ1 and DRQ3 can be monitored at once. It is selected at D1-D2 of offset 0x68h.

i. Memory Group Range.

There are three Programmable Monitored Memory ranges, MEMGPA, MEMGPB and MEMGPC. The first two are used as two single devices. MEMGPC is used as one of the Video Events. All three are programmable at offset 094h-09Fh. An example of how to program MEMGPA is shown below. The other two can be programmed similarly. Now, suppose there is a device that occupies memory range from 012340000h to 01235FFFFh. If D31-D14 of offset 0x94h-0x97h are the address bits of A[31:14], then it must be programmed as 0001_0010_0011_010X_XXb where 'X' means "don't care". Because D13-D4 are the masks of address bits A[23:14], it must be programmed as 00_0000_0111b. As a result, the written value is 012340070h.

j. IO Group Range.

There are six Programmable Monitored IO Ranges, IOGPA-IOGPF. All of them can be used similarly except for the IOGPC, which can be configured to monitor the programmed range or/and the IO ports 062h and 066h at D12-D13 of offset 070h-071h, but its range can be programmed the same way. An example of how to program IOGPA is shown below. The others can follow the steps. Suppose IO range 01230h-01237h is to be monitored. If D15-D2 of offset 0xA0h-0xA1h are the address bits of A[15:2], then it must be programmed as 0001_0010_ 0011_0Xb. Because D1-D0 are the masks of address bits A[3:2], it must be programmed as 01b. As a result, the written value is 01231h.

k. USB.

USB Event is generated when there is a device plugged in/out or the USB bus is busy.

Event	**Corresponding Register**
Primary Driver IO access	D7 of D8h-D9h Enable/Disable of internal IDE
Primary HDD event	Primary Driver IO access D0 of 6Fh-6Ch D0 of 73h-72h.
Secondary Driver IO access	D7 of D8h-D9h Enable/Disable of internal IDE
Secondary HDD event	Secondary Driver IO access D1 of 6Fh-6Ch D0 of 73h-72h
Audio IO access	D4-D15 of 6Fh-6Ch
Audio event	Audio IO access D16-D21 of 6Fh-6Ch
Video IO access	D25 of 6Fh-6Ch
Video Event	D22-D24 of 6Fh-6Ch Offset 09Fh-09Ch Video I/O access D3 of 73h-72h
Floppy IO access	D0 of 68h
Floppy Event	D26 of 6Fh-6Ch D4 of 73h-72h
Serial IO access	D0-D7 of 71h-70h
Serial Event	D5 of 73h-72h Serial IO access
Keyboard IO access	Any access to IO port 60h, 64h
Keyboard Event	Keyboard IO access. D27-D28 of 6Fh-6Ch D6 of 73h-72h
Parallel IO access	D8-D10 of 071h-070h
Parallel IO event	D11 of 71h-70h D7 of 73h-72h Parallel IO access

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IO group A IO access	Offset 0A1h-0A0h
IOGP A event	IO group A IO access. D10 of 73h-72h
IO group B IO access	Offset 0A3h-0A2h.
IOGP B event	IO group B IO access D11 of 73h-72h
IO group C IO access/ IOGP C event	Offset 0A5h-0A4h D12-D3 of 71h-70h
IO group D IO access/ IOGP D event	Offset 0A7h - 0A6h
IO group E IO access/ IOGP E event	Offset 0A9h - 0A8h
IO group F IO access/ IOGP F event	Offset 0ABh - 0AAh
Memory group A event	Offset 097h -094h
Memory group B event	Offset 09Bh - 098h
RTC event	IRQ8J asserted.
Ring IN event	Count number of Ring IN until matching offset B7h.
BUS_ACT event	Offset 076h-075h

l. BUS_ACT.

BUS_ACT event is active when the PCI bus is busy. How frequent the PCI access can be defined is indicated in offset 0x75h-0x76h. Suppose D7-D0 is written as 80h and D13-D8 as 10h. Most of all, D14 should be set to '1' in advance. Then M1533 starts to count number of TRDYJs in every period of 128 PCICLKs. If it is more than 16 TRDYJs in the period, a BUS_ACT Event will be generated.

D. External Switches.

There are 11 specified External Switches and 12 General Purpose External Switches. For the specified External Switches, they can be programmed to be sensed by rising/falling/debounce at offset 0x80h-0x82h and 0x8Ch-0x8Eh. Moreover, some specified switches are used not only to generate SMI here, but also some other functions. For example, THERMALJ pin can be used as auto thermal throttle as described in the following section. LBJ, LLBJ and ACPWR can be used as described in section of Low Battery. Besides, LLBJ can prevent system transfer from SUSPEND to ON. For the General Purpose External Switches, they can be programmed to be sensed by rising/falling/debounce, too, at offset 0x84h-0x8Bh and 0x90h-0x93h. As these pins are General Purpose IO pins, they should be configured carefully to be inputs when used as switch pins or input pins. In general, when rising(falling) is enabled and is sensed, then an SMI will be generated to inform CPU. When debounce circuit is enabled, the debounce clock of all switches can be selected at offset 0B4h, D6-D4.

List of External Switch SMIs :

CRT - PMU Cfg 80h, bit 12-15	COVSW - PMU Cfg 8Ch, bit 12-15	GPIO13 - PMU Cfg. 89h
SETUPJ - PMU Cfg 80h, bit 4-7	HOTKEY- PMU Cfg 8Ch, bit 16-19	GPIO14 - PMU Cfg. 8Ah
EXTSW - PMU Cfg 80h, bit 8-11	LLBJ - PMU Cfg 8Ch, bit 20-23	GPIO15 - PMU Cfg. 8Bh
THRMJ - PMU Cfg 80h, bit 12-15	GPIO8 - PMU Cfg. 84h	GPIO16 - PMU Cfg. 90h
LBJ - PMU Cfg 80h, bit 16-19	GPIO9 - PMU Cfg. 85h	GPIO17 - PMU Cfg. 91h
DOCKJ - PMU Cfg 8Ch, bit 0-3	GPIO10 - PMU Cfg. 86h	GPIO18 - PMU Cfg. 92h
EJECT - PMU Cfg 8Ch, bit 4-7	GPIO11 - PMU Cfg. 87h	GPIO19 - PMU Cfg. 93h
ACPWR - - PMU Cfg 8Ch, bit 8-11	GPIO12 - PMU Cfg. 88h	

E. Clock Control.

Before using any function of Clock Control, the Clock Control should be enabled first at D9 of offset 0x10h-0x13h of IO space. Every function is influenced by the Break Events selected at offset 0x7Ch of configuration space. Following are the Clock Control Functions supported by M1533.

a. Normal Throttle.

In addition to the Clock Control Enable described above, the Duty cycle should be configured in advance and then set Throttle Enable bit to start Normal Throttle. When it is enabled, the STPCLKJ de-asserted and asserted periodically with 256 us period. The Break Events can de-assert STPCLKJ immediately and reset the high/low timer. That is, STPCLKJ would start throttling again if there is no Break Event for a period of time. Only disabling the Throttle Enable bit can stop this function. By the way, all of the configured registers are at offset 0x10h-0x13h of IO space.

b. Auto Thermal Throttle.
It must be done first to program the Duty Cycle of offset 0x10h-0x13h of IO space and set D4 of offset 0x7Bh of configure space to Enable the Auto Thermal Throttle. When it is enabled and THERMALJ has asserted for 2 seconds, throttling is started. The Break Events can de-assert STPCLKJ immediately and reset the high/low timer, too. Throttling is disabled when THERMALJ has de-asserted for 2 seconds.
c. HALT
When Clock Control is enabled and the HALT special cycle is found at PCI buses, the AMSTATJ will be asserted until any Break Event occurs.
d. STPGNT
Before using STPGNT function, the D1-D0 of offset 0x7Bh of Configuration Space should be selected first. If Soft STPCLK is demanded, then D3 should be set to '0' to select STPGNT. Finally, READ offset 0xB2h of IO Space for Soft STPCLK or READ 0x14h for Processor Level 2 forces CPU input to the STPGNT state by asserting STPCLKJ. When SLEEPJ is enabled (D1 of offset 0x7Bh), timing of Pentium Pro is matched; otherwise, Pentium. Besides, ZZ is used to force L2 cache into Powerdown mode. Similar to the HALT, STPCLKJ will be de-asserted when any Break Event occurs. By the way, Soft STPCLK or READ LVL2 causes the same result.
e. STPCLK
Before using STPCLK function, the D1-D0 of offset 0x7Bh of Configure Space should be selected first. If Soft STPCLK is demanded, then D3 should be set to '1' to select STPCLK. Finally, READ offset 0xB2h of IO Space for Soft STPCLK or READ 0x15h for Processor Level 3 both forces CPU input the STPCLK state by asserting STPCLKJ, CPUSTPJ. They will be de-asserted when any Break Event occurs. By the way, Soft STPCLK or READ LVL3 causes the same result.

Note : D5-D3 of offset 0x78h-0x79h are the CPU PLL time when CPU transfers from STPCLK state to STPGNT state.

f. SLOWDOWN.
It is used to change the system clocks, which is outputted from clock generator. The programmed steps are as follows.
1. D2-D0 of offset 0x78h-0x79h are the Clock Generator PLL timer to cover the transition time of changing clock.
2. D2 of offset 0x7Ah must be enabled.
3. D0 of offset 0x7Ah reflects the status of pin SLOWDOWN. That is, any change of this bit will change SLOWDOWN in a specified sequence.

F. Display Control.
a. CCFT.
CCFT is used to control the Backlight of the LCD. When FPVEE is low, CCFT will be low, too. If FPVEE is high, then CCFT will be high or a 9.3KHz PWM output. The Duty cycle of CCFT can be configured by writing D5-D0 of offset 0xB0h or the pins of INC_CCFT and DEC_CCFT.
1. CCFT is the same as FPVEE -> D6='1' and D[5:0]=0.
2. CCFT outputs a PWM -> D6 =‘1’ and D[5:0] ≥ 10h.
3. CCFT configured by hardware pins -> D7='1'.
b. CONTRAST.
CONTRAST is used to control the contrast of the LCD. It can be programmed as 9.3KHz PWM output or HIGH. The duty cycle of CONTRAST can be configured by writing D13-D8 of offset 0xB0h-0xB1h or the pins of INC_CONTRAST and DEC_CONTRAST. Programming offset 0xB0h-0xB1h.
1. CONTRAST keeps high at -> D14='1' and D[13:8]=0.
2. CONTRAST outputs a PWM -> D14=‘1' and D[13:8] ≥ 10h.
3. CONTRAST configured by hardware pins -> D15='1'.

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G. Low Battery.

The Low battery function is active when the following occurs :

a. LBJ is low.
b. LB timer is timeout, then LB timeout SMI is generated.
c. LB timeout SMI generates periodically following the timebase set.
d. LLBJ is low.
e. LLB timer is timeout and LLB timeout SMI is generated. From now on, the LB timeout SMI will not be generated any more.
f. LLB timeout SMI generates periodically following the timebase set.
g. Any time the ACPWR is inserted, that is, asserted, both timers are disabled and reset and no SMI is generated.
h. If ACPWR is plugged out, that is, de-asserted, LLB timer will count again.
i. Only when LBJ and LLBJ are de-asserted and both timers are write reset, the Low Battery status can be cleared. Both the LB timers, LB and LLB, can be configured at offset 0x57h-0x58h.

H. General Purpose Input/Output.

There are 24 General Purpose Output pins, 12 General Purpose Inputs pins and 20 General Purpose IO pins. As most of these pins are multi-function pins, they must be enabled by programming offset 0x59h-0x5Bh of configuration space of device M1533 (not PMU) and offset 0xC6h of configuration space of device PMU.

a. GPI. The input status of GPI pins can be read from offset 0xC4h-0xC5h.
b. GPO. The output level of GPO pins can be programmed at offset 0xC0h-0xC3h.
c. GPIO[7:0].
   1. Programming the directions of GPIO[7:0] at offset 0x7Dh.
   2. Programming the output level of GPIOx at offset 0x7Eh, if it is configured as output.
   3. Read the status of GPIOx at offset 0x7Fh, if it is configured as input.
d. GPIO[19:8].
   1. Programming the direction of GPIOx at D3 of offset 0x84h-0x8Bh and offset 0x90h-0x93h.
   2. Programming the output level of GPIOx at D4 of offset 0x84h-0x8Bh and offset 0x90h-0x93h.
   3. Read the status of GPIOx at D5 of offset 0x84h-0x8Bh and offset 0x90h-0x93h.

List of GPIs, GPOs and GPIOs of M1533

GPI0(OVCRJ0)- '33 Cfg59h, bit0	GPO0(PCSJ)-'33Cfg5Ah, bit0	GPO12(XDIR)-TC pull low	GPIO0(SD0)-TC pull high	GPIO12(BATSEL0) - PMU CfgC6h, bit4
GPI1(OVCRJ1)- '33 Cfg59h, bit1	GPO1(ZZ)-'33Cfg5Ah, bit1	GPO13(IRQ1O)- SPKR & SQWO pull high	GPIO1(SD1)-TC pull high	GPIO13(BATSEL1)- PMU CfgC6h, bit5
GPI2(SERIRQ)- '33 Cfg59h, bit2	GPO2(CPU_STPJ) - '33Cfg5Ah, bit2	GPO14(IRQ12O)- SPKR & SQWO pull high	GPIO2(SD2)-TC pull high	GPIO14(BATSEL2) - PMU CfgC6h, bit6
GPI3(PCIREQJ)- '33 Cfg59h, bit3	GPO3(PCI_STPJ) - '33Cfg5Ah, bit3	GPO15(IRQ0)- SQWO pull high	GPIO3(SD3)-TC pull high	GPIO15(BATSEL3) - PMU CfgC6h, bit7
GPI4(POSSTA)- '33 Cfg59h, bit4	GPO4(SLOWDOWNJ) - '33Cfg5Ah, bit4	GPO16(APICCSJ)- SQWO pull high	GPIO4(SD4)-TC pull high	GPIO16
GPI5(VCSJ)- '33 Cfg59h, bit5	GPO5(CCFT) -'33Cfg5Ah, bit5	GPO17(APICGNTJ)- SQWO pull high	GPIO5(SD5)-TC pull high	GPIO17
GPI6(FPVEE)- '33 Cfg59h, bit6	GPO6(DISPLAY) - '33Cfg5Ah, bit6	GPO18(BIOSA16)- SPLED pull high	GPIO6(SD6)-TC pull high	GPIO18
GPI7(SMBEVENT)- '33 Cfg59h, bit7	GPO7(CONTRAST) - '33Cfg5Ah, bit7	GPO19(BIOSA17)- SPLED pull high	GPIO7(SD7)-TC pull high	GPIO19(SUSLED) - PMU CfgC6h, bit3
GPI8(APICREQJ)- SQWO pull high	GPO8(AMSTATJ) - '33Cfg5Ah, bit8	GPO20(SLEEPJ)- XDIR pull high	GPIO8	
GPI9(KBCLK)- SPKR pull high	GPO9(SQWO) - '33Cfg5Ah, bit9	GPO21(OFF_PWR0J) - '33Cfg5Ah, bit0	GPIO9	
GPI10(KBDATA)- SPKR pull high	GPO10(GPIORBJ) - '33Cfg5Ah, bit10	GPO22(OFF_PWR1) - '33Cfg5Ah, bit1	GPIO10	
GPI11(MSCLK)- SPKR pull high	GPO11(GPIOWB) - '33Cfg5Ah, bit11	GPO23(OFF_PWR2) - '33Cfg5Ah, bit2	GPIO11	

Note :

1. All GPO defaults drive low after enable.
2. All GPIO defaults are inputs after enable.
3. All GPI/GPO/GPIO pins have no pull resistors internally.
4. The comment "drive high/low before enable" is caused by the default function. For example, GPI0/OVCRJ[0] is OVCRJ[0] after reset. But it is not necessary to do if you switch it to GPI0 at booting.
5. All default values can be found at registers of "how to enable" or at '33 Cfg 54h for hardware setting pins.
6. All GPI/GPO/GPIO pins are 5V tolerance.
7. GPIO12 and GPIO14-15 should be pulled either to power of group C or to ground.

I. SMI control.

a. ACPI mode/M7101 mode.

When set as ACPI mode, the status bit of any event is set as soon as the event occurs, no matter whether its corresponding enable/disable bit is set or not. As M7101 mode, the status bit is set if and only if both event occurs and the enable/disable bit is set. Set at D7 of offset 0x77h.

b. Soft SMI.

Write offset 0xB1h of IO space will generate Soft SMI. It can be delayed to generate Soft SMI if D2 of offset 0x77h is set.

c. Read/Write clear SMI.

When set as Read Clear SMI, all status ports in configure space are cleared when read. As Write Clear SMI, writing '1' to the corresponding status bit can clear it. Set at D4 of offset 0x77h.

d. Delayed SMI.

SMI generated after a period of time when an SMI source is generated. Moreover, the SMI will be delayed again if there is any event monitored by Standby timer occurs. Only when no event occurs during that period of time, then SMI is generated.

1. Select Delayed time at D1-D0 of offset 0x77h.
2. Enable/Disable delayed SMI at D2 of offset 0x77h and D2-D0 of offset 0xD8h.

e. SMI sources

1.10 timeout timers*	6. Bus Master Active *	10. LBJ, LLBJ, EXTSW, SETUPJ, CRT input switch pins assert *	14.GPIO8-15 pins assert.*
2. Power button press	7. SMBus SMI *		15.GPIO16-19 pins assert
3.RTC alarm	8.I/O access (1st , 2nd HDD, Audio, Video, floppy, serial, parallel,	11.THRMJ, RI,LID eject, DOCKJ, Hotkey ACPWR, input switch pins assert	
4. Software SMI*	keyboard, IO group A-F*	12.Thermal override	
5.USB bus SMI*	9. Serial IRQ SMI*	13.USB activity	* (pure SMI source)

J. Others.

a. Write Beep function.

1. Enable D6 of offset 0xB3h.
2. Select Beep latency time at D5-D4 of offset 0xB3h.
3. Write 0xCAh to generate Beeps. A maximum of 3 writings are allowed at a time.

b. Periodical Beep function.

1. Enable D6 of offset 0xB3h.
2. Select Beep period at D1-D0 of offset 0xB3h.
3. Select Beep latency time at D3-D2 of offset 0xB3h.

Note : As soon as D3-D2 of offset 0xB3h are not "00", the Periodical Beep function is enabled and the first beep beeps.

c. LED control.

Three LED output controls are supported.

1. SUSLED. Always works if enabled, even when system inputs the SUSPEND. Programmed at D1-D0 of offset 0xB4h.
2. SLED and SQWO. Programmed at offset 0xB5h.

d. Extended GPI/GPO function.

Set at D2,3 of offset 0x5Bh.

1. 16 bits Writable Port Extended General Purpose Output.

When writing to offset 0xB8h with a byte or a word, a 74373 latch pulse will be generated at GPIOWB. The 74373 input should be connected to SD[15:8] and XD[7:0] if a word write command is used. The write command also writes data into the offset 0xB8h. So reading offset 0xB8h will get the data.

2. 16 bits Readable Port Extended General Purpose Input.

When reading to offset 0xBAh with a byte or a word, this will generate 74245 out of enable signal at GPIORBJ. If a word is read, the output 74245 should be connected to SD[15:8] and XD[7:0]. The read cycle can read the 74245 input word data from offset 0xBAh. When writing to offset 0xBAh, there is no meaning.

e. AT/ATX mode select (ACPI)

The GP2-13 input pin pull "high" to select legacy AT mode, pull "low" to select ATX mode. In ATX mode, the system enters soft-off state, user can use power button (PWRBTNJ) to power on system.

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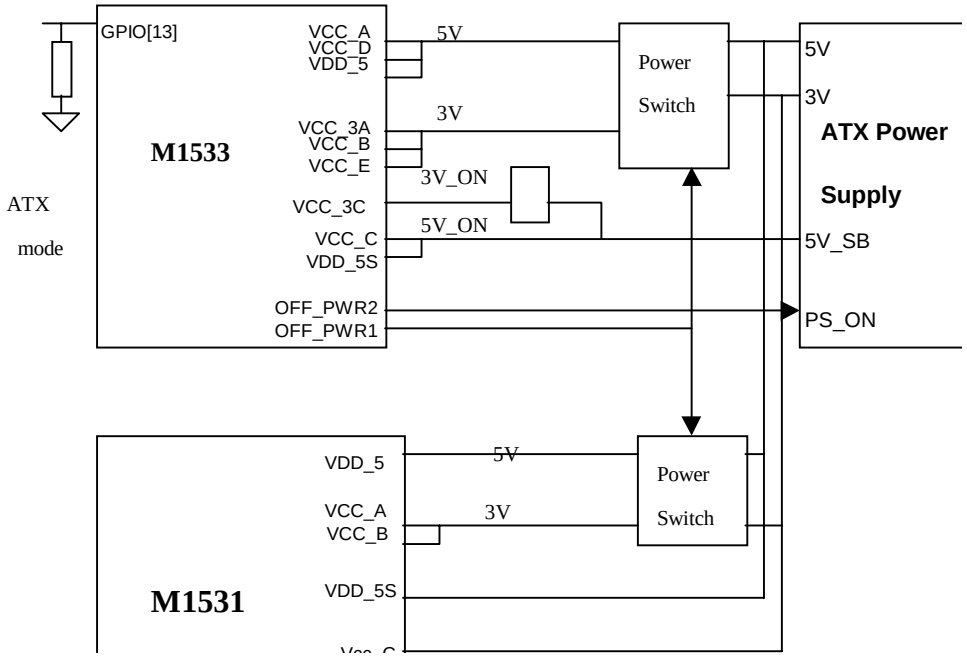
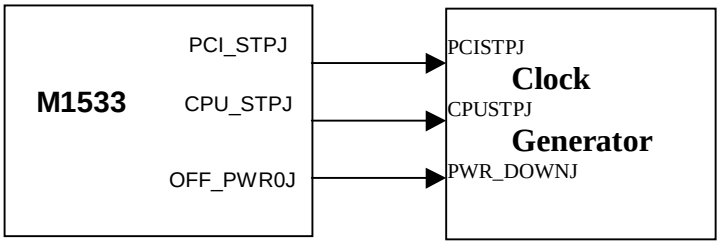
f. Supports PCI PMEJ pins (GPIO[16-18]), select GPIO[16-18] pins to level trigger (offset 0xB4h bit 3)
g. Power control connection



* If the system does not support S3 state, the power switch can be removed.

a. Clock control connection



i. Mapping PMU register 9Ch-FFh to M1533 index 9Ch-FFh when PMU device disable.

5.2 Advanced Configuration and Power Interface Specification.

A. Top View.
B. Power Management Timer.
C. SCI(SMI) Sources.
D. Suspend Modes.
E. Clock Control.
F. Resume Events.
G. Global Lock.
H. Point for Attention.

A. Top View.
The M1533 supports the ACPI(ver 1.0) specification, includes the SCI interrupt, 24/32bit Power Management Timer, System Suspend modes, CPU Power saving modes and ACPI I/O Registers.

B. Power Management Timer.
M1533 supports a 24-bit or 32-bit(PG_BD_D2) fixed rate free running count-up Power Management Timer. The ACPI uses the read-only port (IO_08_D, 32bit) to read the current value of the timer. To allow software to extend the number of bits in the timer, the Status bit(IO_00_D0) is set any time the bit-22 or bit-30 of the timer goes from HIGH to LOW. If the Enable bit (IO_02_D0) is set, then the timer generates a system control interrupt (SCI).

C. SCI(SMI) Sources.

Source	Status Register	Enable Register	Interrupt
Power Management Timer	IO_00_D0	IO_02_D0	SCI
BIOS Release	IO_00_D5	IO_02_D5	SCI
Power Button	IO_01_D0	IO_03_D0	SCI/SMI
RTC alarm	IO_01_D2	IO_03_D2	SCI/SMI
Thermal Control	IO_18_D0	IO_1A_D0	SCI/SMI
Thermal Override	IO_18_D1	IO_1A_D1	SCI/SMI (THRMJ assert > 2sec)
USB Event	IO_18_D2	IO_1A_D2	SCI/SMI
GPIO16-19	IO_18_D4-7	IO_1A_D4-7	SCI/SMI
Docking	IO_19_D0	IO_1B_D0	SCI/SMI
Eject	IO_19_D1	IO_1B_D1	SCI/SMI
AC Adapter	IO_19_D2	IO_1B_D2	SCI/SMI
Ring	IO_19_D3	IO_1B_D3	SCI/SMI
Lid Switch	IO_19_D4	IO_1B_D4	SCI/SMI
Hot Key	IO_19_D5	IO_1B_D5	SCI/SMI
ACPI Release	IO_1C_D0	IO_1E_D0	SMI

Some sources can be enabled to generate the ACPI interrupt, SCI or an SMI. (SCI_EN, IO_04_D0)

D. Suspend Modes.
The M1533 supports five types of system suspend modes.
1)S0: Working
2)S1: Sleeping(Sleeping with Processor Context Maintained)
- .CPU enters the STOP CLOCK state (using STPCLKJ, CPU_STPJ)
- .SRAM Power Saving Mode (using ZZ, PG_7B_D0)
- .Pentium Pro Sleep Mode (using SLEEPJ, PG_7B_D1, Hardware Setting)
- .Inform M1531 to switch to Suspend Refresh mode (using SUSTAT1J)
- .PAD enters Power Saving Mode
- .Stop Internal PCICLK (PG_CB_D2) Option:
  - .Stop ISP PCICLK (CFG_5E_D5)
  - .Stop ISP DMACLK (CFG_5E_D6)
  - .Stop USB PCICLK (CFG_5E_D7)

.Stop 119 KHz clock of M8254 and cold reset counter clock (CFG_5F_D4)
.Stop All AT clocks, including SYSCLK and KB CLK (CFG_5F_D5)
.Stop Internal Keyboard clock (CFG_5F_D6)
.Stop SYSCLK (CFG_5F_D7)
.Stop External PCI Device PCICLK (using PCI_STPJ)
.Stop M1533 PCICLK, OSC14M (PG_D8_D6, using OFF_PWR0J)
.Run M1533 CLK32O
.Run M1533 CLK32I

3)S3: Suspend To DRAM (Sleeping with Processor Context Lost)
.Inform M1531 to switch to Suspend Refresh mode (using SUSTAT1J)
.All Power Off except Resume Block
.Stop M1533 PCICLK
.Stop M1533 OSC14M
.Run M1533 CLK32O
.Run M1533 CLK32I

4)S4: Suspend To DISK(Non_volatile storage)
.All Power Off except Resume Block
.Stop M1533 PCICLK
.Stop M1533 OSC14M
.Stop M1533 CLK32O
.Run M1533 CLK32I

5)S5: Soft Off
.The same as S4

Using CPU_STPJ to control clock generator to stop CPU clock and M1531 host clock
Using PCI_STPJ to control clock generator to stop PCI slots clock and M1531 PCI clock
Using OFF_PWR0J to control clock generator to stop all clocks, except for 32 KHz.
Using OFF_PWR1 to control power plane to stop M1531, M1533 off-power and on-board devices (except RAM) power regions
Using OFF_PWR2 to control power plane to stop M1531 total_power, M1533 off_power and on-board devices power regions.

How to enter S1 state :
.Set CLK_EN='1' (IO_11_D1)
.Program the time of Switch Normal to Suspend Refresh
(PG_78_D6-8,suggest 128 us)
.Program the stable time of Clock Generator PLL, when system is from S1 to s0
(PG_78_D0-2,suggest 1 ms)
.Program the stable time of CPU PLL, when system is from S1 to s0
(PG_78_D3-5,0,suggest 4 ms)
.Program the time of Switch Suspend to Normal Refresh
(PG_78_D9-11,suggest 128 us)
.Set SLP_EN='1', SLP_TYP="011" (IO_05_D5, IO_05_D2-4)

How to enter S3 state:
.Set SLP_EN='1', SLP_TYP="010" (IO_05_D5, IO_05_D2-4)

How to enter S4 state:
.Set SLP_EN='1', SLP_TYP="001" (IO_05_D5, IO_05_D2-4)

How to enter S5 state:
.Set SLP_EN='1', SLP_TYP="000" (IO_05_D5, IO_05_D2-4) or
.Power Button Override Event (PWRBTNJ Assert > 4 sec, PG_B4_D2)

E. Clock Control.

.CPU Clock Control(set CLK_EN='1')
.THROTTLE (THRO_EN=>IO_10_D4, THRO_DTY=>IO_10_D1-3)
.STOP GRANT STATE (Read LVL2,IO_14_D7-0)
.STOP CLOCK STATE (Read LVL3,IO_15_D7-0)
.PCI Clock Control
.Supports CLKRUN function (set CR_EN=>IO_11_D5='1')
.Idle times select (PG_CB_D0-1)
.Stop Device PCICLK (PG_CB_D3)

F. Resume Events.

Event	Status Register	Enable Register	Resume from
Power Button	IO_01_D0	IO_03_D0	S1/S3/S4/S5
RTC alarm	IO_01_D2	IO_03_D2	S1/S3/S4/S5
USB Event	IO_18_D2	IO_1A_D2	S1
GPIO 16-19	IO_18_D4-7	IO_1A_D4-7	S1/S3/S4/S5
Docking	IO_19_D0	IO_1B_D0	S1/S3/S4/S5
Eject	IO_19_D1	IO_1B_D1	S1
AC Adapter	IO_19_D2	IO_1B_D2	S1
Ring	IO_19_D3	IO_1B_D3	S1/S3/S4/S5
Lid Switch	IO_19_D4	IO_1B_D4	S1/S3/S4/S5
Hot Key	IO_19_D5	IO_1B_D5	S1/S3/S4/S5
IRQ0 assert	IO_1D_D2	IO_1F_D2	S1
IRQ assert	IO_1D_D3	IO_1F_D3	S1

The LLBJ assertion will prevent the system from waking-up any Enabled Resume Event, when the LLB_EN Bit is set (IO_1F_D7).
(SCI_EN,IO_04_D0)

G. Global Lock.

M1533 supports two sets of Registers :
a. BIOS_RLS(IO_20_D1), GLB_STS(IO_00_D5), GLB_EN(IO_02_D5)
b. GLB_RLS(IO_04_D2), BIOS_STS(IO_1C_D0), BIOS_EN(IO_1E_D0)

In the event of a resource conflict, the Global Lock is used by the ACPI driver to inform the BIOS driver that it is finished using a shared resource, or by the BIOS driver to inform the ACPI driver.

H. Point of Attention.

.The ACPI Status Registers only support "write '1'" clear method
.The Legacy Status Registers support "write '1'" clear or "Read Clear" method (PG_77_D4)
.The ACPI and Legacy Common Status Registers can clear both or one side. (PG_77_D5)
.The ACPI and Legacy SMI method can select ACPI or 7101 mode. (PG_77_D7)
.CFG represents the M1533 Configuration Space Register
.PG represents the PMU Configuration Space Register
.IO represents the ACPI I/O Space Register

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I. ACPI Programming Guide

ACPI BIOS initialize chipset registers :

1) Program ACPI/SMB IO address to DF00h/DF80h

Chip	Space	Offset	Value
PMU	CFG	10h	00h
PMU	CFG	11h	DFh
PMU	CFG	14h	80h
PMU	CFG	15h	DFh
PMU	CFG	04h	01h(Bit0)->Enable IO command

2) Reset PMU clock control circuit.

PMU	CFG	7Ch	12h(bit4,1)
PMU	CFG	7ch	00h ->must set 'high' to 'low'

3) Program North Bridge arbiter control IO address to DF30h and pass to PCI bus.

Chip	Space	Offset	Value
M1531	CFG	70h(E8h)	30h
M1531	CFG	71h(E9h)	F1h
M1531	CFG	72h(EAh)	01h(bit1-0)-> pass to PCI bus
M1531	CFG	77h(EBh)	80h(bit7)-> Enable memory data bus gated clock during S1.

4) Program South Bridge

M1533	CFG	57h	06h(bit2-1) -> disable event to break throttle
M1533	CFG	5Eh	E0h (bit7-5) -> Stop USB, ISP, clock during S1.
M1533	CFG	5Fh	F4h(bit7-4)-> Stop SYSCLK, KBC, AT, 14M clock during S1. (bit2) -> disable South Bridge arbiter, when ACPI disable arbiter.
M1533	CFG	76h	81h(bit7) -> disable SCI routing to IRQ13. (bit4-0) -> SCI routing to IRQ9and level trigger.

5) Program PMU

PMU	CFG	78h	69h-> a.bit8-6- 128us normal to suspend switch time.
PMU	CFG	79h	02h Suspend switch time b. bit2-0 =1ms clock generator PLL time. c. bit 5-3 = 4ms CPU PLL time d. bit 11-9 =128us Suspend to normal switch time
PMU	CFG	7Ch	92h(bit7,4,1)-> Set PCI master, INTR,IRQ0,as break event.
PMU	CFG	BDh	04h(bit2) -> Set ACPI free run 32-bit timer.
PMU	CFG	D8h	40h(bit6) -> Stop south bridge PCI clock during S1.

6) Enable clock control function

ACPI	IO	DF11h	02h(bit1) -> Enable clock control

7) Initialize the ACPI event features.

ACPI	IO	DF00h	FFh->Clear ACPI event status.
ACPI	IO	DF01h	FFh-> Clear ACPI event status.
ACPI	IO	DF18h	FFh-> Clear ACPI event status.
ACPI	IO	DF19h	FFh-> Clear ACPI event status.
ACPI	IO	DF1Ch	FFh-> Clear ACPI event status.
ACPI	IO	DF1Dh	FFh-> Clear ACPI event status.
ACPI	IO	DF02h	00h-> Disable ACPI event.
ACPI	IO	DF03h	00h-> Disable ACPI event.
ACPI	IO	DF1Ah	00h-> Disable ACPI event.
ACPI	IO	DF1Bh	00h-> Disable ACPI event.
ACPI	IO	DF1Eh	00h-> Disable ACPI event.
ACPI	IO	DF1Fh	00h-> Disable ACPI event.

ACPI compatible OS initialization :
1. Scanning memory for ACPI tables.
2. Turn on ACPI
   . Write ACPI_Enable value to SMI_CMD port ->described in the FACP table, ex. 0 AA B1
   . Hardware assert software SMI to BIOS.
   . BIOS check port value, if ACPI_ENABLE:
   1) ACPI IO DF04h 01h(bit0) -> Enable SCI
   2) M1533 CFG 5Dh 40h(bit6) -> Disable PMU device and mapping 7Ch-FFh to M1533.

5.3 System Management Bus Host Controller Programming Example

Programming Guide for SMBus
* if PMU(M7101) register index 14h-17h set to be 00003A81h
* For SMB Host Controller to be a master only, just set M7101's register index E0h = "01h" & E2h = "20h".
* then below Example's index "03h" will be "00003A80h+03h" that is 'I/O address of SMB Host Controller' = "00003A83h".

Example:
1. A "Write Byte" cycle for Smart Battery Selector (address="14h"), and the write data is 3Ah (DataA="3Ah") with "Command Reg" being "22h".
   => write '1' clear to let read index 00h to be "04h" (Idle).
   => write index 03h "14h"(address="14h" and write cycle).
   => write index 01h "20h"(Write/Read Byte command).
   => write index 04h "3Ah"(DataA is for Byte data use).
   => write index 07h "22h"(Command Reg = "22h").
   => write index 02h "XXh"(write any data for index 02h to start).
   => wait SMI (or Interrupt).
   => read index 00h, if bit4='1' it means complete successfully.
   => else then write '1' clear and restart the protocol.

2. A "Write Word" cycle for Smart Battery (address="16h"), and the write data is Low Byte=27h (DataA="27h"), and High Byte=D1h (DataB="D1h") with "Command Reg" being "33h".
   => write '1' clear to let read index 00h to be "04h" (Idle).
   => write index 03h "16h"(address="16h" and write cycle).
   => write index 01h "30h"(Write/Read Word command).
   => write index 04h "27h"(DataA is for Low Byte data use).
   => write index 05h "D1h"(DataB is for High Byte data use).
   => write index 07h "33h"(Command Reg = "33h").
   => write index 02h "XXh"(write any data for index 02h to start).
   => wait SMI (or Interrupt).
   => read index 00h, if bit4='1' it means complete successfully.
   => else then write '1' clear and restart the protocol.

3. A "Read Word" cycle for Thermal (address="90h"-"9Eh"), this procedure is based on the address="92h" with "Command Reg" being "45h".
   => write '1' clear to let read index 00h to be "04h" (Idle).
   => write index 03h "93h"(address="92h" and read cycle).
   => write index 01h "30h"(Write/Read Word command).

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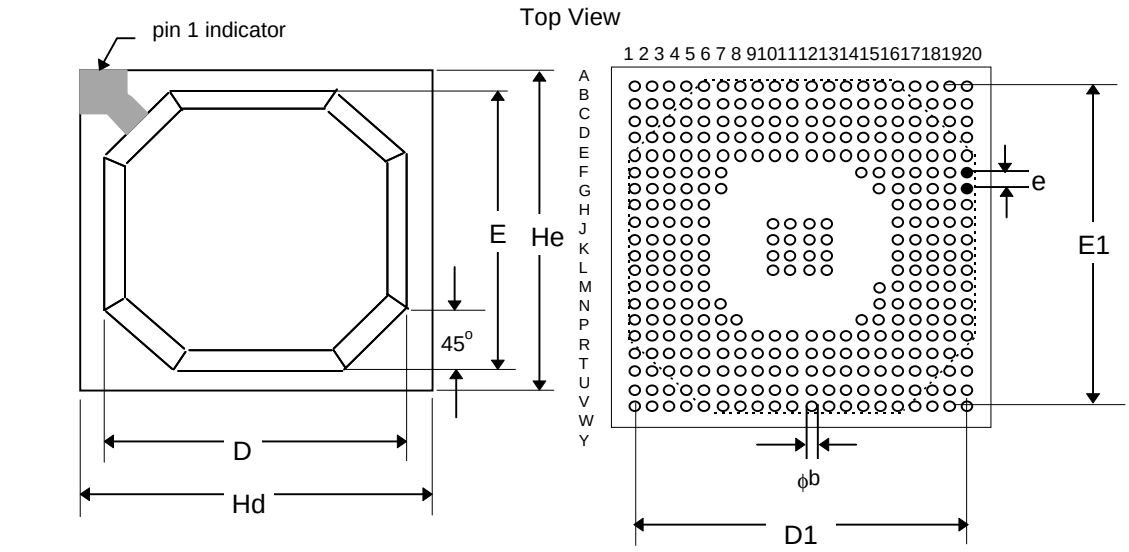
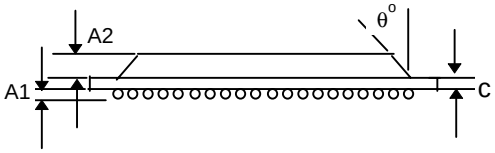
=> write index 07h "45h"(Command Reg = "45h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully.
=> else then write '1' clear and reinitialize the procedure.
=> if succeed, read index 04h for Low Byte (DataA), and index 05h for High Byte (DataB).

4. A "Write Block" cycle for Clock Synthesizer (address="D2h"). It has a total of 6 bytes data, for example, to send and the write data is "07h", "2A", "51h", "D0h", "46h" and "38h" with "Command Reg" being "77h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "D2h"(address="D2h" and write cycle).
=> write index 01h "C0h"(Write/Read Block command and reset Block Register Pointer).
=> write index 04h "06h"(DataA is for Block Byte number).
=> write index 06h "07h"(Block Data).
=> write index 06h "2Ah"(Block Data).
=> write index 06h "51h"(Block Data).
=> write index 06h "D0h"(Block Data).
=> write index 06h "46h"(Block Data).
=> write index 06h "38h"(Block Data).
=> write index 07h "77h"(Command Reg = "77h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully.
=> else then write '1' clear and restart the protocol.

Section 6 : Packaging Information

328L BGA Dimension Spec (27 x 27 mm)





Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	23.80	24.00	24.20
D1	23.93	24.13	24.33
E	23.80	24.00	24.20
E1	23.93	24.13	24.33
e		1.27	
Hd	26.80	27.00	27.20
He	26.80	27.00	27.20
θ°	23°	30°	37°
Y (radius of ball)			0.25

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Section 7 : Revision History

i.v. 10/22/96
p.7-16 Pin Type (with Drive Current)
p.57 bits 7-6
p.95 bits 8-6
p.110 bits 2-0 Index 0C6h
p.13 SMIJ, STPCLKJ, SLEEPJ, ZZ belong to Group E
p.134 PCI IDE Registers
p.80 Indices 41h-40h, 43h-42h bit 12 & bit 3
p.85 Index 54h
p.86 Index 59h
p.87 Index 5Ah, 5Bh, 5Ch, 5Dh
p.89 Index 67-66h
p.92 Index 71-70h
p.94 Index 76h
p.95 Index 79h-78h
p.99 Index 84h,85h,86h,87h,88h,89h,8Ah,8Bh
p.110 Index 0C6h
p.112 0D9h-0D8h bits 7-6
p.106 Index 0B1h-0B0h
Index 0B3h bits 5-4,1-0
p.107 Index 0B4h, 0B5h
p.132 Index B1h, B2h
p.141 Table inserted.
p.24 2.5 Hardware Setting Table
p.47 Index 6Dh bit 7

p.41,45,52,55,76,77,79,95,97,109,112 04/11/97
p.57, 59 04/25/97
p.57,119 06/11/97
p.117,127 07/22/97
p.13,25,43,46,80,127,142,144 08/05/97
p.4,5,9,10,16,26,28,50,133-135,149 08/08/97
p.59 11/27/97

p.14,15,22,42,45-47,90,97,107-109,111,141,143,145-153 02/12/98
Appendix A 02/12/98

p.47,51 03/11/98

p.157,134 03/12/98

p.47,51,95,97,105,109,111,112 09/19/98 v1.56 tss

Pinout Diagram (bottom view)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	PIDED3	PIDED10	PIDED6	SIDECS3J	SIDEAKJ	SIDED15	SIDED2	SIDED10	SIDED7	AD0	AD5	AD9	AD14	STOPJ	CBEJ2	AD18	AD21	NC
B	PIDED14	PIDED2	PIDED13	PIDED11	**PIDED9**	SIDECS1J	**SIDEIRDY**	SIDED0	SIDED12	SIDED5	PHLDJ	AD1	AD6	AD10	AD15	**DEVSELJ**	AD16	AD19	AD22	NC
C	PIDED0	PIDED15	PIDED1	PIDED4	PIDED5	SIDEA2	SIDEIORJ	SIDED14	SIDED3	SIDED9	PHLDAJ	AD2	AD7	AD11	CBEJ1	TRDYJ	AD17	AD20	AD23	CBEJ3
D	PIDEA2	PIDEA0	PIDEA1	PIDED12	PIDED8	SIDEA0	**SIDEIOWJ**	SIDED1	SIDED11	SIDED6	CLKRUNJ	AD3	CBEJ0	AD12	PAR	IRDYJ	PCIRSTJ	AD24	AD25	AD26
E	INTR	PIDECS3J	PIDECS1J	PIDEAKJ	PIDED7	SIDEA1	**SIDEDRQ**	SIDED13	SIDED4	SIDED8	PCICLK	AD4	AD8	AD13	SERRJ	FRAMEJ	AD30	AD27	AD28	AD29
F	IGNNEJ	SMIJ	NMI	PIDEIRDY	PIDEIOWJ	VCC_E	VCC_D								VCC_B	INTBJ	INTAJ	AD31	GPO8	USBCLK
G	INIT	A20MJ	CPURST	PIDEIORJ	PIDEDRQ	VCC_3C				M1533					VCC_B	INTDJ	INTCJ	GPO4	USBP0+	USBP0-
H	RI	SMBCLK	SMBDATA	STPCLK	IRQ13											GPO2	GPO3	GPI3	USBP1+	USBP1-
J	GPIO17	GPIO18	**GPIO19**	GPO20	GPO1				GND	GND	GND	GND				GPI0	GPI1	IOCHKJ	RSTDRV	SD7
K	GPIO14	GPIO15	GPIO16	DOCKJ	LLBJ				GND	GND	GND	GND				MSDATA	MSCLK	SD6	IRQ9	**S**D5
L	GPIO12	GPIO13	PWRBTNJ	SUSTAT1J	IRQ8J				GND	GND	GND	GND				KBDATA	KBCLK	SD4	DREQ2	SD3
M	LID	LBJ	**RSMRSTJ**	HOTKEYJ	PWG				GND	GND	GND	GND				SD2	NOWSJ	SD1	SD0	IOCHRDY
N	OSC32KO	OSC32KI	OSC32KII	SIRQII	SIRQI	VDD5S										SMEMWJ	AEN	**SMEMRJ**	SA19	IOWJ
P	GPO21	GPO22	GPO23	GPO18	GPO19	VCC_C									VCC_A	SA18	IORJ	SA17	DACKJ3	SA16
R	GPO13	GPO14	GPO15	GPO16	GPO17	VCC_A	**Vcc_3A**							VCC_A	VDD5	DREQ3	SA15	**DACKJ1**	SA14	DREQ1
T	GPO7	GPO9	GPO10	GPO11	GPO12	IRQ1I	**RTCRW**	RTCAS	ROMKBCSJ	DREQ6	MEMWJ	DACKJ0	LA20	LA23	BALE	**DACKJ2**	IRQ4	IRQ6	SA13	REFSHJ
U	GPO0	GPO5	GPO6	GPIO11	EJECT	XD4	XD0	RTCDS	SD12	SD10	**DREQ5**	LA17	IRQ15	IRQ10	OSC14M	TC	IRQ3	IRQ5	IRQ7	SA12
V	GPI010	GPIO9	GPIO8	GPI6	ACPWR	XD5	XD1	SPKR	SD13	DACKJ7	SD8	DREQ0	LA19	LA22	M16J	SA2	SA5	SA8	SA10	SYSCLK
W	NC	GPI8	GPI7	GPI4	SETUPJ	XD6	XD2	SPLED	SD14	SD11	**DACKJ6**	MEMRJ	IRQ14	IRQ11	SBHEJ	SA1	SA4	SA7	SA9	SA11
Y	NC	GPI5	GPI2	CRT	THRMJ	XD7	XD3	EXTSW	SD15	DREQ7	SD9	DACKJ5	LA18	LA21	IO16J	SA0	SA3	SA6	NC	NC

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Appendix A : Chip Specification Change Table

Rev.	Sample Date	Specification Change
E	04/18/97	Provide M1533 register index 53h bit 6=1 to disable USB device
F	06/27/97	
G	07/17/97	
H	09/15/97	1.Provide M1533 register index 57h bit 1 or bit2=1 to disable throttle break event. 2.Assert DS when read RTC IO port 70/72h (M1533 register index 53h bit 5) 3.Provide M1533 register index 57h bit 3=0 to monitor halt cycle.
I	11/07/97	1.Provide M7101 register index B4h bit 3=1to enable PMEs(GPIO[18:16])as level sensitive.
J	02/06/98	1.Add stop clock burst mode (M1533 register index 6Ch bit7=1) 2.Add interrupt polling mode clock select(M1533 register index 57h bit 4, 0=>PCICLK, 1=>14MHz) 3.Add AT/ATX mode hardware setting (AT mode =>GPIO[13] is pull “H”, ATX mode =>GPIO[13] is pull “L” 4.M7101 register index 7Ch-FFh will be mapped to M1533 register index 7Ch-FFh when PMU device is disable. 5.M1533 arbiter disable function for ACPI (M1533 register index 5Fh bit 2)

This material is recyclable.

Please contact ALi applications department at 408-467-7456 to verify that all information is current before beginning a design using this datasheet.