ALTERA

Data Book

August 1993

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About this Data Book

August 1993

This data book provides comprehensive information about Altera's FLEX 8000, MAX 7000, MAX 5000/EPS464, Classic, Configuration EPROM, and EPS448 devices and MAX+PLUS II development tools. For information on Micro Channel EPLDs and the MCMap development system, refer to the Altera ***Micro Channel Adapter Handbook***.

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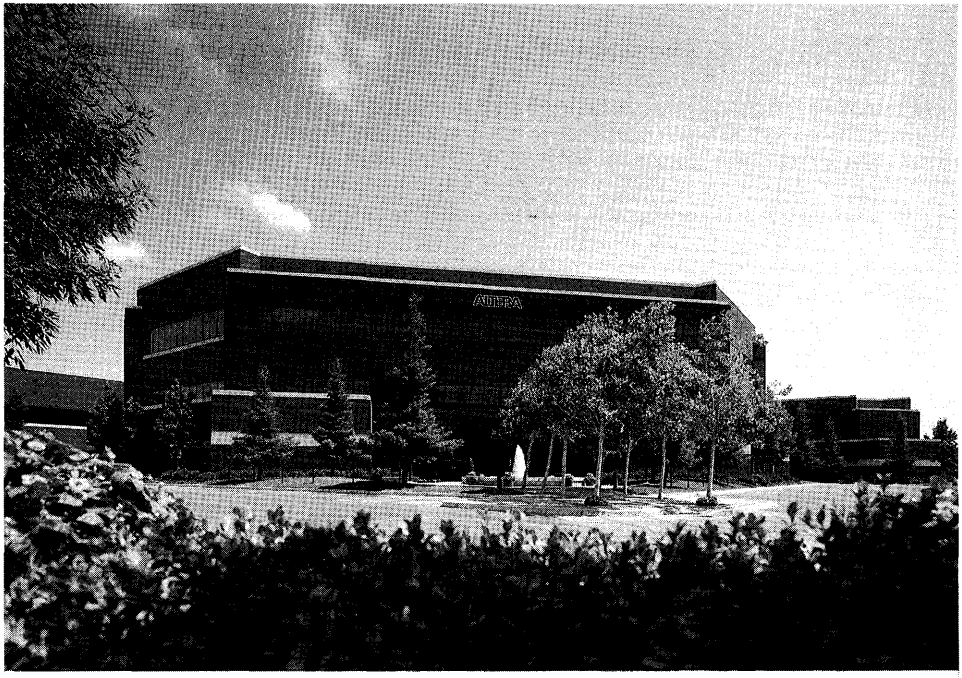
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Introduction

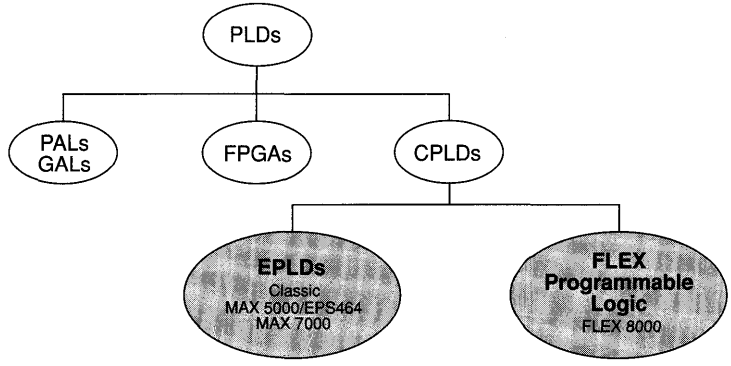
August 1993, ver. 1 Data Sheet

Programmable Logic Devices (PLDs) are digital, user-configurable integrated circuits (ICs) used to implement custom logic functions. PLDs implement any Boolean expression or registered function using the generic logic structures in the devices. In contrast, off-the-shelf logic ICs, such as TTL devices, provide a specific logic function and cannot be modified to meet individual circuit-design requirements.

PLDs were once viewed only as an alternative to discrete logic and custom or semi-custom devices such as ASICs and gate arrays. In recent years, however, PLDs have become the preferred choice. As PLD costs have decreased through high-volume manufacturing and the use of aggressive process technologies, PLD manufacturers have been able to offer devices with higher integration, higher performance, and lower cost per function than most discrete and custom devices.

Programmable logic encompasses all digital logic circuits configured by the end-user, including simple 20-pin PAL/GAL devices, Field Programmable Gate Arrays (FPGAs), function-specific PLDs, Complex PLDs (CPLDs), and Erasable Programmable Logic Devices (EPLDs). PLDs are offered in many different architectures, and a variety of memory technologies for configuring the devices. Figure 1 shows where Altera's general-purpose devices fit into the programmable logic device market.

Figure 1. Altera General-Purpose Logic Devices



Altera PLDs

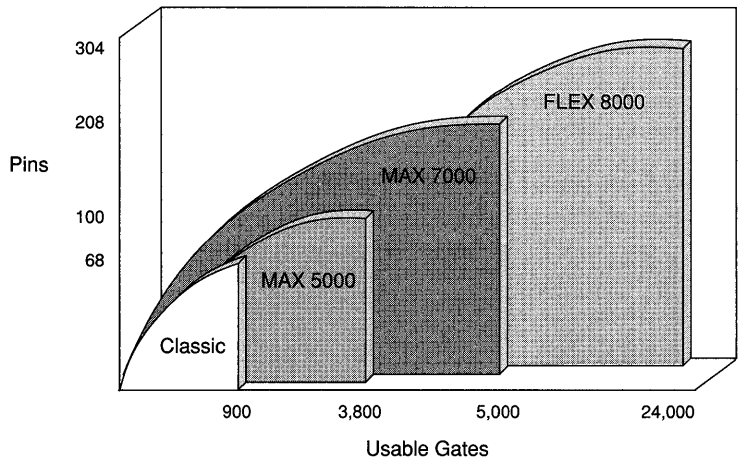
Altera offers four families of general-purpose PLDs: FLEX 8000, MAX 7000, MAX 5000/EPS464, and Classic. These families use either sum-of-products architecture or look-up table (LUT) architecture. Each architecture offers advantages for implementing and fitting logic into a device and for meeting performance requirements. Altera uses three different memory technologies in its devices: EPROM, EEPROM, and SRAM. The Classic, MAX 5000/ EPS464, and MAX 7000 families use sum-of-products architecture and EPROM or EEPROM technologies. The FLEX 8000 family uses an LUT architecture and SRAM technology. See Table 1.

Table 1. Altera Device Architecture & Technology

Device Family	Architecture	Technology
FLEX 8000	Look-Up Table	SRAM
MAX 7000	Sum-of-Products	EPROM, EEPROM
MAX 5000/EPS464	Sum-of-Products	EPROM
Classic	Sum-of-Products	EPROM, EEPROM

MAX 7000, MAX 5000/EPS464, and Classic devices are targeted for combinatorially intensive logic designs. These families provide logic densities ranging from 150 to 5,000 usable gates, and pin counts ranging from 20 to 208 pins. The FLEX 8000 family provides logic density from 2,500 to 24,000 usable gates and pin counts from 84 to 304 pins (see Figure 2). In FLEX 8000 devices, the high performance, predictable interconnect delays and ease-of-use of EPLDs are combined with the high

Figure 2. Pin Count & Density in Altera Device Families



register counts, low standby power, and in-circuit reconfigurability of FPGAs, making these devices the ideal solution for high-density, register-intensive designs.

The EPROM- and EEPROM-based Classic and Multiple Array MatriX (MAX) devices are non-volatile erasable devices. EPROM devices are erased with UV light, while EEPROM devices are erased electrically. SRAM-based FLEX 8000 devices can be configured in-circuit during power-up. They consume low power and offer a high degree of flexibility to support different application requirements.

All Altera device families use CMOS process technology, which provides lower power dissipation and greater reliability than bipolar technology. To facilitate continual improvement, Altera migrates products to advanced process technologies as soon as these technologies become viable and can support reliable manufacturing. Currently, Altera offers devices built on an advanced 0.65-micron technology.

For high-volume production, Altera offers Mask-Programmed Logic Devices (MPLDs) as low-cost alternatives to high-density PLDs. MPLDs, which are masked versions of programmable logic devices, offer a unique turn-key approach that eliminates the engineering-intensive tasks required for custom and semi-custom devices. The quick turn-around for MPLD conversion guarantees fast time-to-market.

Altera Device Architectures

The following descriptions of Altera's device families identify the key features and benefits of each family.

Classic Family

Industry Standard, Low Density

Altera's original family of EPLDs is the Classic family, with densities up to 900 usable gates and pin counts up to 68 pins. Composed of single arrays of globally interconnected logic, the industry-standard Classic family offers a low-cost solution for low-density applications. Some devices in the Classic family offer a unique "zero-power mode," which allows these devices to draw only microamps of current at standby, making them ideal for low-power applications.

MAX 5000/EPS464 Family

Lowest Cost, Medium Density

MAX 5000/EPS464 EPLDs provide a comprehensive, cost-effective solution for designs intensive in combinatorial logic. The MAX 5000 architecture uses several Logic Array Blocks (LABs) connected by a Programmable Interconnect Array (PIA) to pack up to 3,750 usable gates and 100 pins into a single device. This family also features a high logic-to-pin ratio, making it ideal for buried-logic-intensive designs, such as state machines.

MAX 7000 Family

Highest Performance, High Density

The MAX 7000 family is the fastest, high-density programmable logic family in the industry, with up to 5,000 usable gates. Based on a second-generation MAX architecture, these devices support counter frequencies as high as 125 MHz and propagation delays as fast as 7.5 ns. With pin counts up to 208 pins, MAX 7000 devices offer a high pin-to-logic ratio, making them ideal for I/O-intensive designs. MAX 7000 devices also offer a programmable speed/power control, so that each macrocell can be configured for high-speed or low-power operation. Thus, speed-critical sections of a design can be programmed to run at the fastest speed, while the remainder operates at low power.

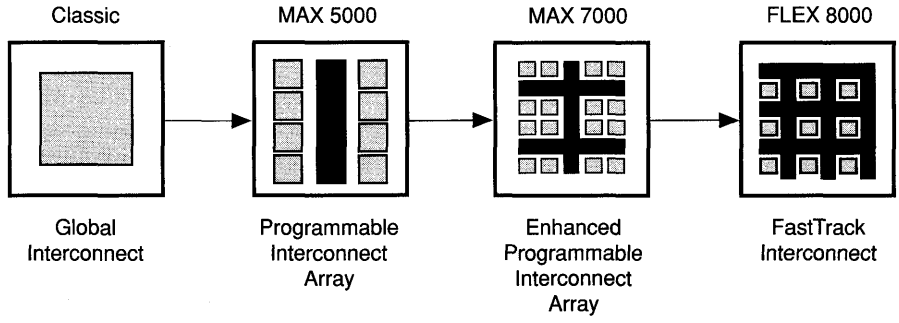
FLEX 8000 Family

Highest Density, Register-Intensive

FLEX 8000 programmable logic represents a new type of programmable logic architecture, combining the high register counts of FPGAs with the fast, predictable interconnect of EPLDs. FLEX 8000 devices provide up to 24,000 usable gates, 2,266 flipflops, and 304 pins. The SRAM-based FLEX 8000 family features low standby power and in-circuit reconfigurability, making it ideal for such applications as PC add-on cards, battery-powered instruments, and multi-purpose telecommunication cards.

Figure 3 shows the architecture evolution of Altera devices and illustrates how the interconnect structure has evolved to maintain high performance at even the highest densities.

Figure 3. Altera Architecture Evolution



Advantages of Programmable Logic

Designers generally develop a logic circuit with three distinctly different device options: discrete logic devices (TTL, CMOS, etc.), custom or semi-custom devices (gate arrays and ASICs), or programmable logic devices. The best choice is the option that can meet the most design requirements. Table 2 lists a number of important requirements, and ranks the three device options according to how effectively they meet these requirements.

Table 2. Device Options Ranking

Requirement	PLD	Discrete Logic	Custom Device
Speed	●	○	●
Density	●	○	●
Cost	●	○	● *(1)*
Development Time	●	◗	○
Prototyping & Simulation Time	●	○	○
Manufacturing Time	●	◗	○
Ease of Use	●	◗	○
Future Modification	●	◗	○
Inventory Risk	●	●	○
Development Tool Support	●	○	●

Notes:
(1) Cost-effective only in high-volume production
● = very effective
◗ = adequate
○ = poor

Advantages of Altera Programmable Logic

Altera programmable logic devices not only offer the general benefits of PLD technology, but other advantages as well. These advantages—based on innovative architectures, aggressive technologies, and the MAX+PLUS II programmable logic development environment—are:

- ❑ Higher performance
- ❑ High-density logic integration
- ❑ Greater cost-effectiveness
- ❑ Shorter development cycles

Higher Performance

Performance is a function of process and architecture. Altera devices are manufactured on state-of-the-art CMOS processes, which offer the fastest possible delays. Altera devices are also designed with continuous interconnection schemes, which provide fast, consistent signal delays throughout the device.

High-Density Logic Integration

Designers often seek the highest possible logic integration for the designs they develop, usually to reduce board space and cost. Also, existing designs often undergo secondary development cycles that aim to reduce cost by integrating more logic into fewer devices. In both cases, programmable logic devices with high logic integration capability offer an excellent solution. Altera devices, which range in density from 300 to 24,000 usable gates, can easily integrate existing logic, whether it be a few or a few hundred discrete logic devices, PLDs, FPGAs, or even custom devices. This high integration capability provides higher performance and reliability, as well as lower system cost.

Greater Cost-Effectiveness

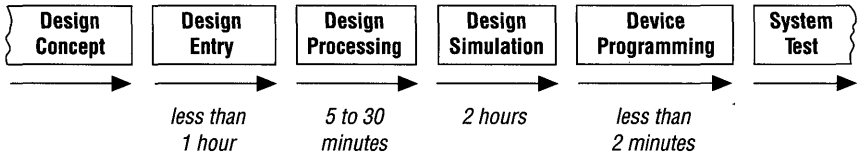
Altera continually strives to refine product development and manufacturing processes. The expertise accumulated over more than a decade of leadership has made both process technologies and the manufacturing flow highly efficient, and has enabled the company to offer the most cost-effective, highest-performance programmable logic available.

Short Development Cycles with MAX+PLUS II Software

Time is the most precious resource for many design engineers. Large sums of money are wasted on projects that are not completed on schedule and therefore miss a window of opportunity. Consequently, the shorter the development cycle, the better. Altera's fast, intuitive, and easy-to-use MAX+PLUS II software can shorten the development cycle considerably. Design entry, processing, verification, and device programming together take only a few hours, potentially allowing several complete design iterations in one day. Figure 4 illustrates a typical PLD development cycle in the MAX+PLUS II development environment. Times shown are representative of a relatively sophisticated 10,000-gate logic design.

MAX+PLUS II enables designers to target different Altera device families without further modification to a design. The software automatically partitions and optimizes the design for the selected architecture. See "MAX+PLUS II Development Tools" later in this data sheet.

Figure 4. Development Cycle for Altera Devices



Architecture Basics

The basic building block of all Altera general-purpose devices is the logic cell. It contains combinatorial logic and a programmable flipflop that can emulate D, T, JK, and SR functionality or can be bypassed for purely combinatorial operation. Logic cells in Classic, MAX 5000/EPS464, and MAX 7000 devices are called macrocells; in FLEX 8000 devices, they are called logic elements (LEs). Complete details on macrocells and logic elements are available in the individual device family data sheets in this data book.

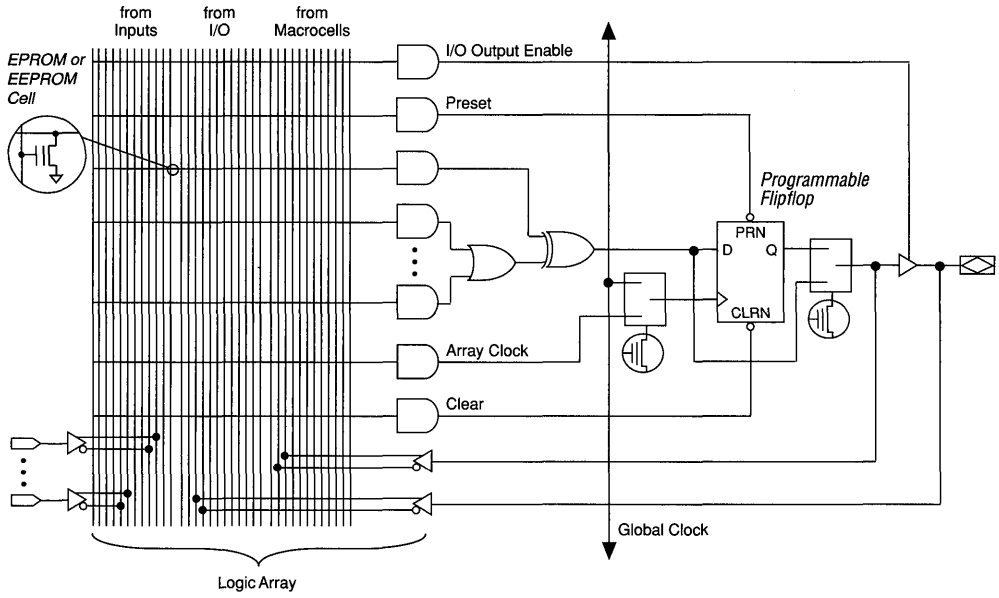
Signals enter the device via dedicated inputs or I/O pins configured as inputs. Inputs to each logic cell are supplied by the input pins and other logic cells. Signals drive out of the device via the I/O pins. Outputs of logic cells are available as inputs to other logic cells, or may be driven out of the device via I/O pins. A continuous interconnect structure provides connections between logic cells and between pins and logic cells. This structure ensures consistent, predictable delays across all densities and architectures.

Altera device data sheets contain timing models for precise calculation of all worst-case timing delays. This calculation is possible because of the continuous routing structure of the devices. In contrast, a segmented routing structure, such as that found in FPGAs, provides connections by linking a series of short routing segments. This series of connections introduces unpredictable delays and signal skew, preventing the use of timing models for device performance estimates.

EPLD Architecture

Altera Classic, MAX 5000/EPS464, and MAX 7000 EPLDs implement logic using a sum-of-products structure. Each macrocell contains a set of wide-input AND-gates (called product terms or p-terms), an OR-gate, and a programmable register for sequential functions (see Figure 5). For specific details on each EPLD family's macrocell structure, refer to the appropriate data sheet in this data book.

Figure 5. Typical EPLD Macrocell



Combinatorial Functions

A product term is an *n*-input AND gate, where *n* is the number of possible inputs. Figure 6 shows three different representations of the same logic function: Circuit A is presented in traditional logic notation; Circuit B has been modified to a sum-of-products notation; and Circuit C is written in AND-array notation.

Figure 6. AND-Array Notation (Part 1 of 2)

EPLD schematics frequently use a 1-input AND-gate notation as shorthand for n-input AND gates. A dot represents a connection between an input (vertical wire) and one of the inputs to an n-input AND gate. The absence of any dots on the input to the AND gate indicates an unused AND gate whose output is at a logic 0.

Circuit A: Typical Circuit

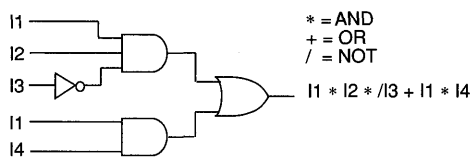
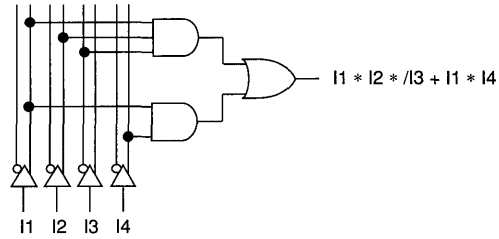
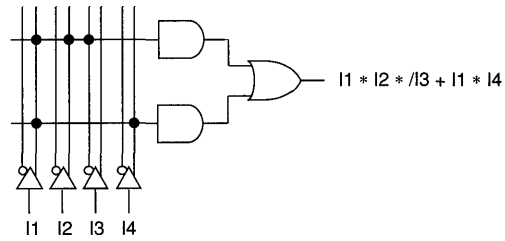


Figure 6. AND-Array Notation (Part 2 of 2)

Circuit B: Circuit A with Complementary Output Buffers



Circuit C: Circuit B with 8-Input AND Gates in AND-Array Notation



Outputs of the product terms are tied to the inputs of an OR gate to compute the sum. Since all combinatorial logic can be reduced to a sum-of-products expression, the generic AND-OR array of Circuit C can produce any Boolean function. (The actual product terms in Altera devices are much wider than the 8 inputs shown.)

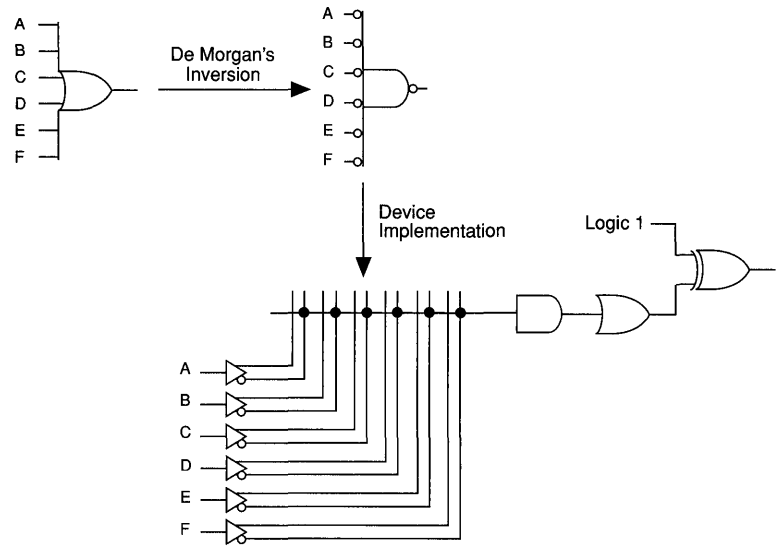
Product terms can also be used to generate complex control signals for use with the programmable register (Clock, Clear, Preset, and Clock Enable) or the Output Enable signal for the I/O pins. These signals are called array control signals.

To support programmable inversion and complex functions, the output of the OR gate feeds one input to a two-input XOR gate (see Figure 5). This architectural feature allows the software to generate inversions wherever necessary, without wasting macrocells for simple functions. Figure 7 shows an OR function that requires six product terms in its current form. By using the programmable XOR gate and De Morgan's inversion, the OR function can be transformed into a NAND function using a single product term:

```
A+B+C+D+E+F = /(/A*/B*/C*/D*/E*/F)
```

This inversion from OR to AND translates the equation and reduces the number of fixed OR terms required in the logic array. MAX+PLUS II software automatically applies De Morgan's inversion and other logic synthesis techniques to optimize the use of the logic array.

Figure 7. Logic Minimization with De Morgan's Inversion



MAX 5000 and MAX 7000 macrocells support very complex combinatorial functions. They provide allocatable product terms, called expander product terms, that can be used for functions requiring more product terms than are normally found in a macrocell. The MAX 5000 architecture supports shareable expander product terms, called shared expanders, that feed back into the logic array to support two levels of logic. The MAX 7000 architecture provides shareable expanders as well as parallel expanders. Parallel expanders are product terms that are shared between adjacent macrocells. They allow the MAX+PLUS II software to increase the effective number of inputs to the OR gate in the sum-of-products. See the family device data sheets in this data book for more detailed information on shared and parallel expanders.

Sequential Functions

Programmable flipflops in the macrocells are used to implement sequential functions. MAX 5000 EPLD flipflops can also be configured as flow-through latches. If the flipflop is not required for macrocell logic, it can be bypassed. Most macrocell flipflops also have an asynchronous Clear and Preset that allows emulation of most TTL functions.

In all Altera EPLDs except the EP330, each internal flipflop can be clocked from a dedicated global Clock pin (i.e., a Clock pin whose signal does not pass through the logic array), any input or I/O pin, or any internal logic

function. For each flipflop, a multiplexer selects either a pin or product-term source for the Clock.

EPLD flipflops are positive-edge-triggered with data transitions that occur on the rising edge of the dedicated global Clock. When the Clock is driven by a product term, flipflops can be configured for either positive- or negative-edge-triggered operation. In addition, product-term Clocks allow gated Clock and Clock Enable logic to be implemented. Global Clock signals have faster Clock-to-output delay times than internally generated product-term Clock signals. In MAX 7000 devices, a Clock Enable signal can synchronize groups of registers on asynchronous control signals.

I/O Pins

The EPLD I/O control block contains a tri-state buffer controlled either by a macrocell product term or by a dedicated input pin. The I/O pins can be configured as inputs, outputs, or bidirectional pins. Most EPLDs have dual feedback, i.e., the macrocell feedback is decoupled from the I/O pin feedback. With the dual feedback feature, a buried function can be implemented in the macrocell while the I/O pin is used simultaneously as an input. This ability ensures that logic in an EPLD is not wasted due to I/O pin requirements. Applications that require bus-oriented functions or many buried flipflops—such as counters, shift registers, and state machines—are easily accommodated by the programmable I/O control block.

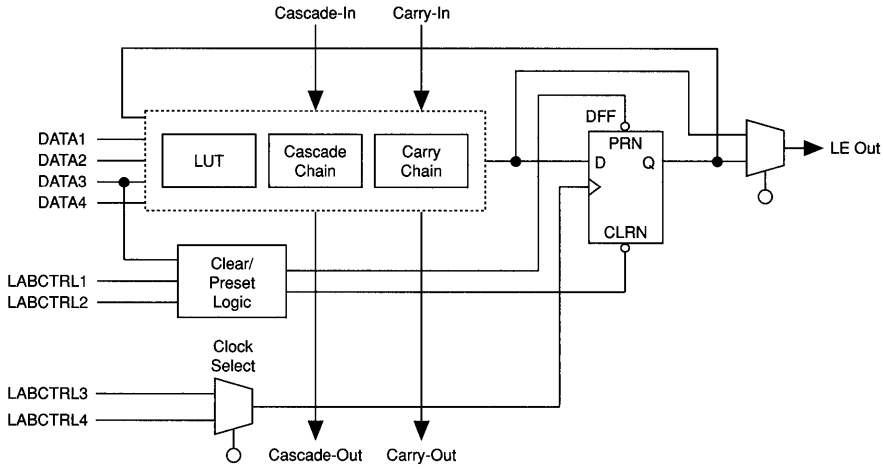
Routing

Routing resources in product-term-based devices connect the input and I/O pins to macrocells and also provide a macrocell-to-macrocell path. Most of the Classic devices and the smallest MAX 5000 devices are fully interconnected, ensuring a global routing path for all signals. Higher-density EPLDs use a Programmable Interconnect Array (PIA) that routes only the signals necessary for a specific function. By providing optimized routing resources, Altera's high-density EPLDs do not suffer the speed and die-size penalty typically incurred in globally routed high-density devices.

FLEX Architecture

The FLEX 8000 architecture implements logic with a large matrix of logic elements (LEs). Each LE contains a four-input look-up table (LUT) to compute any function of four variables, and dedicated carry and cascade chains to support complex combinatorial functions. The LE also contains a programmable register for sequential logic functions (see Figure 8). The fine-grained structure of the LE makes FLEX 8000 devices ideal for register-intensive applications.

Figure 8. FLEX 8000 Device Logic Element Architecture



Combinatorial Functions

Combinatorial functions are implemented with the four-input LUT and two dedicated high-speed data paths (carry chain and cascade chain) in the LE. The carry chain supports very fast carry generation for arithmetic functions and counters, while the cascade chain supports wider-input functions such as multiplexers and decoders.

Sequential Functions

Programmable flipflops are used for sequential functions such as counters, state machines, and shift registers. Flipflops can be clocked from a dedicated global Clock pin, any input or I/O pin, or any internal logic function. Although flipflops in FLEX 8000 devices are positive-edge-triggered, the FLEX architecture supports programmable inversion on all control signals that allows negative-edge triggering for any Clock source.

I/O Pins

I/O pins can be configured as input, output, or bidirectional pins. A register associated with each I/O pin can be used as an input or output register. The FLEX architecture also provides a tri-state buffer associated with each I/O pin that can be controlled by a dedicated input pin, any I/O pin, or internal logic.

Routing

Routing in the FLEX architecture is provided by the FastTrack Interconnect, a continuous interconnect structure consisting of horizontal and vertical routing paths. This global routing structure allows LEs to communicate with each other and with a wide variety of I/O pins, providing high performance and low-skew interconnect of all signals in FLEX 8000 devices.

MAX+PLUS II Development Tools

Altera achieves maximum device performance and density not only with advanced processes and innovative logic architectures, but also through state-of-the-art design tools. The MAX+PLUS II programmable logic development software provides an architecture-independent design environment that supports designs for Altera's general-purpose programmable logic device families, ensuring easy design entry, quick processing, and uncomplicated device programming.

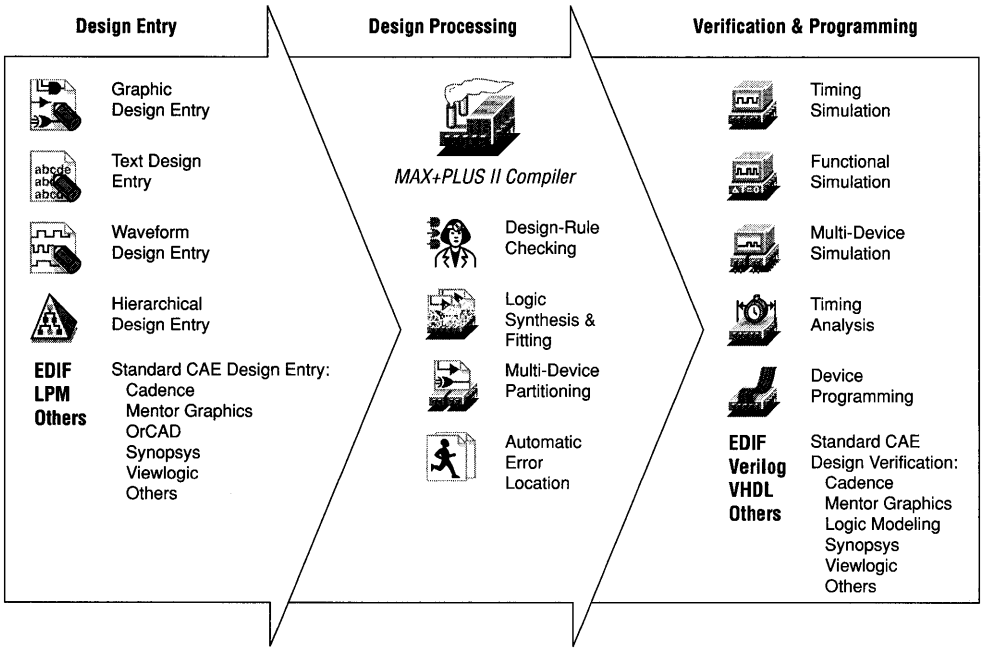
Using MAX+PLUS II, designers no longer need to master the complexities of device architectures. MAX+PLUS II translates their design—created with familiar design entry tools, such as schematic capture or a high-level behavioral language—into the format required by the target architecture.

Since intimate architectural knowledge is built into Altera development tools, designers do not need to manually optimize their design, and are thus able to complete their designs much more rapidly. With MAX+PLUS II, users can take a logic circuit from design entry to device programming in a matter of hours. Design processing is typically completed in minutes, allowing several complete design iterations in a single day.

Design Entry, Design Processing & Device Programming

MAX+PLUS II offers a full spectrum of logic design capabilities (see Figure 9). Designers are free to combine text, graphic, and waveform design entry methods while creating single- or multi-device hierarchical designs. The MAX+PLUS II Compiler performs minimization and logic synthesis, fits the design into one or more devices, and generates programming data. Design verification with functional and timing simulation and delay prediction for speed-critical paths is available, as well as multi-device simulation across multiple device families. Altera and a number of programming hardware manufacturers offer hardware for programming the devices.

Figure 9. MAX+PLUS II Design Environment



Access to Various Platforms & Other CAE Tools

Altera is committed to enable designers to work in the logic development environments most familiar to them. MAX+PLUS II interfaces to a wide variety of other CAE tools—provided by companies such as Cadence, Mentor Graphics, OrCAD, Synopsys, and Viewlogic—via EDIF, LPM, Verilog, and VHDL. The MAX+PLUS II Compiler runs on both PC and workstation platforms, making MAX+PLUS II the industry's only platform-independent, architecture-independent programmable logic design environment. The ACCESS alliance, which Altera has formed with many CAE tool vendors, guarantees smooth interfaces between Altera products and the products of the ACCESS partners, and ensures timely support of Altera devices with these tools.

The Logical Alternative

The advanced architectures and processing technologies used in Altera devices provide the greatest performance and highest density available in programmable logic devices. The sophisticated, highly integrated MAX+PLUS II development environment gives the designer the tools with which to extract this superior performance and density. Together, Altera devices and Altera development tools are the logical choice for all programmable logic designs.

Component Selection Guide

August 1993, ver. 1 Data Sheet

Introduction

This selection guide lists devices available from Altera:

- FLEX 8000 devices
- Configuration EPROMs
- MAX 7000 devices
- MAX 5000/EPS464 devices
- Classic devices
- 3.3-Volt devices
- Function-specific devices
  - SAM devices
  - Micro Channel devices
- Military-qualified devices
  - Classic devices
  - MAX 5000 devices
  - MAX 7000 devices
  - FLEX 8000 devices

For detailed information on these products, refer to the appropriate sections in this data book. For a list of all Altera products, refer to the *Product Index*. For information on Altera's programmable logic development systems, see the *MAX+PLUS II Selection Guide*.

FLEX 8000 Devices

Table 1 provides information on the FLEX 8000 family of register-intensive, high-density, programmable logic devices. These devices combine the fine-grained architecture and high register count of FPGAs with the high speed, predictable interconnect delays, and ease-of-use of EPLDs. FLEX 8000 devices are fabricated on CMOS SRAM technology.

Table 1. FLEX 8000 Devices *See Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Technology	Flipflops	Logic Elements	Dedicated Inputs	I/O	Number of Pins
EPF8282	L, T	C	-2	SRAM	282	208	4	64, 74	84, 100
EPF8282	L, T	C, I	-3	SRAM	282	208	4	64, 74	84, 100
EPF8452	L, G, Q	C	-2	SRAM	452	336	4	64, 116	84, 160
EPF8452	L, G, Q	C, I, M	-3	SRAM	452	336	4	64, 116	84, 160
EPF8820	G, R, B	C	-2	SRAM	820	672	4	116, 148	160, 192, 208, 225 *(4)*
EPF8820	G, R, B	C, I	-3	SRAM	820	672	4	116, 148	160, 192, 208, 225
EPF81188	G, R	C,	-2	SRAM	1188	1008	4	180	232, 240
EPF81188	G, R	C, I, M	-3	SRAM	1188	1008	4	180	232, 240
EPF81500	G, R	C	-2	SRAM	1500	1296	4	177, 204	240, 288, 304 *(5)*
EPF81500	G, R	C, I	-3	SRAM	1500	1296	4	177, 204	240, 288, 304

Notes to tables 1 through 8 are listed on page 23.

Configuration EPROMs

Table 2 provides information on Configuration EPROMs, which are serial EPROMs that are used to configure FLEX 8000 devices.

Table 2. Configuration EPROMs for FLEX 8000 Devices

Device	Package (2)	Temp. (3)	Description	Number of Pins
EPC1064	P, L, T	C, I, M	64K × 1-bit serial EPROM for configuring FLEX 8000 devices	8, 20, 32
EPC1213	P, L	C, I, M	213K × 1-bit serial EPROM for configuring FLEX 8000 devices	8, 20

Notes to tables 1 through 8 are listed on page 23.

MAX 7000 Devices

Table 3 provides information on the MAX 7000 family of high-density, high-speed, I/O-intensive, general-purpose programmable logic devices. These devices range from fast 7.5-ns PAL/GAL integrators to high-speed programmable alternatives to gate arrays. MAX 7000 devices are fabricated on CMOS EPROM and EEPROM technologies.

Table 3. MAX 7000 Devices *See Note (1)*

Device	Package *(2)*	Temp. *(3)*	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Technology	MCells (FFs)	Ded. Inputs	I/O	Number of Pins
EPM7032	L, Q, T	C	-7	7.5	125.0	EEPROM	32	4	32	44
EPM7032	L, Q, T	C	-10	10	100.0	EEPROM	32	4	32	44
EPM7032	L, Q, T	C, I	-12	12	90.9	EEPROM	32	4	32	44
EPM7032	L, Q, T	C, I	-15	15	76.9	EEPROM	32	4	32	44
EPM7032	L	C	-15T	15	76.9	EEPROM	32	4	32	44
EPM7064	L, G, Q	C	-7	7.5	125.0	EEPROM	64	4	48, 64	68, 84, 100 *(6)*
EPM7064	L, G, Q	C	-10	10	100.0	EEPROM	64	4	48, 64	68, 84, 100
EPM7064	L, G, Q	C	-12	12	90.9	EEPROM	64	4	48, 64	68, 84, 100
EPM7064	L, G, Q	C, I	-15	15	76.9	EEPROM	64	4	48, 64	68, 84, 100
EPM7096	L, G, Q	C	-7	7.5	125.0	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	L, G, Q	C	-10	10	100.0	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	L, G, Q	C	-12	12	90.9	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	L, G, Q	C, I	-15	15	76.9	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	J, L, G, Q	C	-2	15	71.4	EPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	J, L, G, Q	C	-3	20	62.5	EPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	J, L, G, Q	C, I		25	50.0	EPROM	96	4	48, 60, 72	68, 84, 100
EPM7128	L, G, Q	C	-10	10	100.0	EEPROM	128	4	48, 64, 80, 96	68, 84, 100, 160
EPM7128	L, G, Q	C	-12	12	90.9	EEPROM	128	4	48, 64, 80, 96	68, 84, 100, 160
EPM7128	L, G, Q	C	-15	15	76.9	EEPROM	128	4	48, 64, 80, 96	68, 84, 100, 160
EPM7128	L, G, Q	C, I	-20	20	62.5	EEPROM	128	4	48, 64, 80, 96	68, 84, 100, 160
EPM7160	L, G, Q	C	-12	12	90.9	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7160	L, G, Q	C	-15	15	76.9	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7160	L, G, Q	C, I	-20	20	62.5	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7192	G, Q	C	-12	12	90.9	EEPROM	192	4	120	160
EPM7192	G, Q	C	-15	15	76.9	EEPROM	192	4	120	160
EPM7192	G, Q	C, I, M	-20	20	62.5	EEPROM	192	4	120	160
EPM7256	G, W, M	C	-20	20	62.5	EPROM	256	4	128, 160	160, 192, 208 *(7)*
EPM7256	G, W, M	C, I, M	-25	25	50.0	EPROM	256	4	128, 160	160, 192, 208

Notes to tables 1 through 8 are listed on page 23.

MAX 5000/ EPS464 Devices

Table 4 provides information on the MAX 5000/EPS464 family of low-cost programmable logic devices for tasks ranging from 20-pin address decoders to 100-pin custom LSI peripherals. These devices combine the speed, ease-of-use, and familiarity of PAL devices with the density of programmable gate arrays. MAX 5000/EPS464 devices are fabricated on CMOS EPROM technology.

Table 4. MAX 5000/EPS464 Devices *See Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Technology	Macrocells (Flipflops)	Dedicated Inputs	I/O	Number of Pins
EPM5016	D, P, S	C	-15	15	100.0	EPROM	16	8	8	20
EPM5016	D, P, S	C, I	-17	17	83.3	EPROM	16	8	8	20
EPM5016	D, P, S	C, I	-20	20	62.5	EPROM	16	8	8	20
EPM5032	D, P, J, L	C	-15	15	76.9	EPROM	32	8	16	28
EPM5032	D, P, J, L	C	-17	17	71.4	EPROM	32	8	16	28
EPM5032	D, P, J, L	C, I	-20	20	62.5	EPROM	32	8	16	28
EPM5032	D, P, J, L	C, I, M	-25	25	50.0	EPROM	32	8	16	28
EPS464	J, L, Q	C	-20	20	66.7	EPROM	64	4	32	44
EPS464	J, L, Q	C	-25	25	50.0	EPROM	64	4	32	44
EPM5064	J, L	C	-1	25	50.0	EPROM	64	8	28	44
EPM5064	J, L	C, I	-2	30	40.0	EPROM	64	8	28	44
EPM5064	J, L	C, I, M		35	33.3	EPROM	64	8	28	44
EPM5128	J, L, G	C	-1	25	50.0	EPROM	128	8	52	68
EPM5128	J, L, G	C, I	-2	30	40.0	EPROM	128	8	52	68
EPM5128	J, L, G	C, I, M		35	33.3	EPROM	128	8	52	68
EPM5128A	J, L, G	C	-12	12	111.1	EPROM	128	8	52	68
EPM5128A	J, L, G	C	-15	15	83.3	EPROM	128	8	52	68
EPM5128A	J, L, G	C	-20	20	66.7	EPROM	128	8	52	68
EPM5130	J, L, G, Q, W	C	-1	25	50.0	EPROM	128	20	48, 64	84, 100
EPM5130	J, L, G, Q, W	C	-2	30	40.0	EPROM	128	20	48, 64	84, 100
EPM5130	J, L, G, Q, W	C, I, M		35	33.3	EPROM	128	20	48, 64	84, 100
EPM5192	J, L, G	C	-1	25	50.0	EPROM	192	8	64	84
EPM5192	J, L, G	C	-2	30	40.0	EPROM	192	8	64	84
EPM5192	J, L, G	C, I, M		35	33.3	EPROM	192	8	64	84
EPM5192A	J, L, G, Q	C	-15	15	83.3	EPROM	192	8	64	84, 100
EPM5192A	J, L, G, Q	C	-20	20	66.7	EPROM	192	8	64	84, 100

Notes to tables 1 though 8 are listed on page 23.

Classic Devices

Table 5 provides information on the Classic family of programmable logic devices, which offer the industry's most comprehensive solution to high-speed, low-power logic integration. These devices provide t_{PD} as low as 7.5 ns and internal counter rates as high as 125 MHz. Classic devices are fabricated on CMOS EPROM and EEPROM technologies.

Table 5. Classic Devices *See Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Technology	Macrocells (Flipflops)	Dedicated Inputs	I/O	Number of Pins
EP330	P, S	C	-12	12	100.0	EPROM	8	10	8	20
EP330	P, S	C	-15	15	83.3	EPROM	8	10	8	20
EP610	P, L, S	C	-15	15	83.3	EPROM	16	4	16	24, 28
EP610	P, L, S	C, I	-20	20	62.5	EPROM	16	4	16	24, 28
EP610	D, P, L, S	C	-25	25	40.0	EPROM	16	4	16	24, 28
EP610	D, P, L, S	C, I	-30	30	33.3	EPROM	16	4	16	24, 28
EP610	D, P, L, S	C, I, M	-35	35	28.6	EPROM	16	4	16	24, 28
EP610A	P, L, S	C	-7	7.5	125.0	EEPROM	16	4	16	24, 28
EP610A	P, L, S	C	-10	10	100.0	EEPROM	16	4	16	24, 28
EP610A	P, L, S	C	-12	12	83.3	EEPROM	16	4	16	24, 28
EP610A	P, L, S	C	-15	15	71.4	EEPROM	16	4	16	24, 28
EP610T	P, L, S	C	-15	15	83.3	EPROM	16	4	16	24, 28
EP610T	P, L, S	C	-20	20	62.5	EPROM	16	4	16	24, 28
EP610T	P, L, S	C	-25	25	40.0	EPROM	16	4	16	24, 28
EP910	D, P, J, L	C	-30	30	33.3	EPROM	24	12	24	40, 44
EP910	D, P, J, L	C, I	-35	35	28.6	EPROM	24	12	24	40, 44
EP910	D, P, J, L	C, I, M	-40	40	25.0	EPROM	24	12	24	40, 44
EP910A	L	C	-10	10	100.0	EEPROM	24	12	24	44
EP910A	L	C	-12	12	83.3	EEPROM	24	12	24	44
EP910A	L	C	-15	15	71.4	EEPROM	24	12	24	44
EP910T	P, L	C	-30	30	33.3	EPROM	24	12	24	40, 44
EP1810	L	C	-20	20	50.0	EPROM	48	16	48	68
EP1810	L	C, I	-25	25	40.0	EPROM	48	16	48	68
EP1810	J, L, G	C	-35	35	28.6	EPROM	48	16	48	68
EP1810	J, L, G	C, I, M	-45	45	22.2	EPROM	48	16	48	68
EP1810T	L	C	-20	20	50.0	EPROM	48	16	48	68
EP1810T	L	C, I	-25	25	40.0	EPROM	48	16	48	68
EP1810T	L	C	-35	35	28.6	EPROM	48	16	48	68

Notes to tables 1 though 8 are listed on page 23.

3.3-Volt Devices

Table 6 provides information on Altera's general-purpose programmable logic devices for 3.3-V applications. These devices are ideal for low-power systems, such as battery-operated instruments and notebook computers. The 3.3-V devices are fabricated on CMOS EEPROM and SRAM technologies.

Table 6. 3.3-Volt Devices *See Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Technology	Flipflops	Logic Cells	Dedicated Inputs	I/O	Number of Pins
EPM7032V (8)	L, T	C	-12	EEPROM	32	32	4	32	44
EPM7032V	L, T	C	-15	EEPROM	32	32	4	32	44
EPM7032V	L, T	C, I	-20	EEPROM	32	32	4	32	44
EPF8282V (9)	L, T	C	-3	SRAM	282	208	4	64, 74	84, 100
EPF8282V	L, T	C, I	-4	SRAM	282	208	4	64, 74	84, 100

Function-Specific Devices

Table 7 provides information on the user-configurable Stand-Alone Microsequencer (SAM) devices, ideal for implementing high-performance controllers. SAM devices feature 448 words of on-chip reprogrammable microcode EPROM, a 15 × 8 stack, a loop counter, and prioritized multi-way control branching. SAM devices are based on CMOS EPROM technology.

Table 7. SAM Devices

Device	Package (2)	Temp. (3)	Speed Grade	f_{CYC} (MHz)	Technology	Microcode EPROM	Branch EPLD (P-Terms)	Stack	Inputs	Outputs	Number of Pins
EPS448	D, P, L	C	-25A	25	EPROM	448 × 36	768	15 × 8	10	16	28
EPS448	D, P, L	C	-25	25	EPROM	448 × 36	768	15 × 8	10	16	28
EPS448	D, P, L	C, I, M	-20	20	EPROM	448 × 36	768	15 × 8	10	16	28
EPS448	D, P, L	C	-16	16	EPROM	448 × 36	768	15 × 8	10	16	28

Table 8 gives information on the Micro Channel programmable logic device, which provides a user-configurable interface for PS/2 Micro Channel Bus adapter cards. Basic interface functions are integrated into the EPB2001, which is 100% compatible with Micro Channel AC timing and DC output drive specifications. The EPB2001 is based on CMOS EPROM technology.

Table 8. Micro Channel Device

Device	Package (2)	Temp. (3)	Technology	Description	Number of Pins
EPB2001	L	C	EPROM	Single-chip interface adapter for PS/2 Micro Channel	84

Notes to Tables 1 though 8:

(1) Preliminary data is shown for some parameters. Consult individual device data sheets in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for current availability of device package options):
- D: Ceramic dual in-line package (CerDIP)
- P: Plastic dual in-line package (PDIP)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- G: Ceramic pin-grid array (PGA)
- S: Plastic small-outline integrated circuit (SOIC)
- Q: Plastic quad flat pack (PQFP)
- W: Windowed ceramic quad flat pack (CQFP).
- T: Plastic thin quad flat pack (TQFP)
- M: Metal quad flat pack (MQFP)
- R: Power quad flat pack (RQFP)
- B: Ball-grid array (BGA)

(3) Operating temperature:
- C : Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)
- M: Military (–55° C to 125° C)

(4) The 192-, 208-, and 225-pin package options of the EPF8820 provide 148 I/O pins.

(5) The 288- and 304-pin package options of the EPF81500 provide 204 I/O pins.

(6) The 84- and 100-pin package options for the EPM7064 provide 64 I/O pins.

(7) The 192- and 208-pin package options for the EPM7256 provide 160 I/O pins.

(8) The EPM7032V is a 3.3-V version of the EPM7032.

(9) The EPF8282V is a 3.3-V version of the EPF8282.

Military-Qualified Devices

Tables 9 though 12 provide information on Altera's military-qualified Classic, MAX 5000, MAX 7000, and FLEX 8000 devices. For more information on Altera's military-qualified devices, consult *Military Products* in this data book.

Table 9. Military-Qualified Classic Devices *See Note (1)*

Device	Package (2)	Assurance Level (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Technology	Macrocells (Flipflops)	Dedicated Inputs	I/O	Number of Pins	Altera Military Drawing (4)
EP610	D	883B	35	28.6	EPROM	16	4	16	24	02D-00522
8947601LA	D	DESC	35	28.6	EPROM	16	4	16	24	
EP1810	G	883B	45	25.0	EPROM	48	16	48	68	02D-00782
8946901YC	G	DESC	45	25.0	EPROM	48	16	48	68	

Table 10. Military-Qualified MAX 5000 Devices *See Note (1)*

Device	Package (2)	Assurance Level (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Technology	Macrocells (Flipflops)	Dedicated Inputs	I/O	Number of Pins	Altera Military Drawing (4)
EPM5032	D	883B	25	50.0	EPROM	32	8	16	28	02D-00828
9061102XA	D	DESC	25	50.0	EPROM	32	8	16	28	–
EPM5128	G	883B	30	40.0	EPROM	128	8	52	68	02D-01015
EPM5128	G	883B	35	33.3	EPROM	128	8	52	68	02D-01015
8946801XC	G	DESC	35	33.3	EPROM	128	8	52	68	–
EPM5130	G, W	883B	30	40.0	EPROM	128	20	64	100	02D-01413
EPM5130	G, W	883B	35	33.3	EPROM	128	20	64	100	02D-01413
9314402MZC	G	DESC	30	40.0	EPROM	128	20	64	100	–
9314401MZC	G	DESC	35	33.3	EPROM	128	20	64	100	–
9314402MYA	W	DESC	30	40.0	EPROM	128	20	64	100	–
9314401MYA	W	DESC	35	33.3	EPROM	128	20	64	100	–
EPM5192	G	883B	35	33.3	EPROM	192	8	64	84	02D-01359
9206202MZC	G	DESC	30	40.0	EPROM	192	8	64	84	–
9206201MZC	G	DESC	40	33.3	EPROM	192	8	64	84	–

Table 11. Military-Qualified MAX 7000 Devices (Under Development) *See Note (1)*

Device	Package (2)	Assurance Level (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Technology	Macrocells (Flipflops)	Dedicated Inputs	I/O	Number of Pins
EPM7192	G	883B	20	66.6	EEPROM	192	4	120	160

Table 12. Military-Qualified FLEX 8000 Devices (Under Development) *See Note (1)*

Device	Package (2)	Assurance Level (3)	Speed Grade	Technology	Flipflops	Logic Elements	Dedicated Inputs	I/O	Number of Pins
EPF8452	G	883B	-3	SRAM	452	336	4	116	160
EPF81188	G	883B	-3	SRAM	1188	1008	4	180	232

Notes to Tables 9 though 12:

(1) All military-qualified devices are rated to military temperatures (–55° C to 125° C). Preliminary data is shown for some other parameters. Consult individual device data sheets in this data book for more information, or contact Altera for the most current device information.

(2) Package configurations:
- D: Ceramic dual in-line package (CerDIP)
- G: Ceramic pin-grid array (PGA)
- W: Ceramic quad flat pack (CQFP)

(3) Product assurance levels:
- 883B: Processed to MIL-STD-883, current revision.
- DESC: DESC Standard Military Drawing (SMD). Consult Altera or DESC for availability.

(4) All Military Product Drawings (MPDs) are prepared in accordance with the appropriate military specification format. When a Source Control Drawing (SCD) is necessary, the appropriate MPD is required for proper SCD preparation.

Notes:

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FLEX™
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FLEX 8000

Programmable Logic Device Family

August 1993, ver. 3 | Data Sheet

Features

- High-density, register-rich programmable logic device family
  - 2,500 to 24,000 usable gates
  - 282 to 2,252 registers
- Fabricated on a 0.8-micron CMOS SRAM technology
- In-circuit reconfigurable
- FastTrack continuous routing structure for fast, predictable interconnect delays
- Available in a variety of packages with 84 to 304 pins (see Table 1)
- Input/output registers on all I/O pins
- Dedicated carry chain that can implement fast adders and counters
- Dedicated cascade chain for efficient implementation of high-speed, high-fan-in logic functions
- Low power consumption (less than 1 mA in standby mode)
- Programmable output slew-rate control to reduce switching noise
- Built-in Joint Test Action Group (JTAG) Boundary-Scan test circuitry on selected devices
- 3.3-V operation provided by EPF8282V devices (see the *3.3-Volt Programmable Logic Devices Data Sheet* in this data book)
- Software design support and automatic place-and-route with Altera's MAX+PLUS II development system for PC, Sun SPARCstation, and HP 9000 Series 700 platforms

Table 1. FLEX 8000 Device Features

Feature	EPF8282 EPF8282V	EPF8452	EPF8820	EPF81188	EPF81500
Available Gates *(1)*	5,000	8,000	16,000	24,000	31,000
Usable Gates *(1)*	2,500	4,000	8,000	12,000	15,500
Flipflops	282	452	820	1,188	1,500
Logic Elements	208	336	672	1,008	1,296
Maximum User I/O	78	120	152	184	208
JTAG BST Circuitry	Yes	No	Yes	No	Yes
Packages *(2)*	84-pin PLCC 100-pin TQFP	84-pin PLCC 160-pin PQFP 160-pin PGA	160-pin RQFP 192-pin PGA 208-pin RQFP 225-pin BGA	232-pin PGA 240-pin RQFP	240-pin RQFP 288-pin PGA 304-pin RQFP

Notes:
(1) Devices with 24,000 usable gates (48,000 available gates) are under development.
(2) Contact Altera for information on package availability. Ball-grid array (BGA) packages are under development.

General Description

Altera's Flexible Logic Element MatriX (FLEX) family combines the benefits of both EPLDs and FPGAs. The fine-grained architecture and high register count of FPGAs are combined with the high speed and predictable interconnect delays of EPLDs to make FLEX 8000 the ideal programmable logic family for a wide range of applications. Logic is implemented in FLEX 8000 devices with compact 4-input look-up tables (LUTs) and programmable registers, while high performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing, wide data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 2 shows typical functions and performance for FLEX 8000 devices.

Table 2. FLEX 8000 Performance

Application	Logic Elements Used	-2 Speed Grade	-3 Speed Grade
16-bit prescaled counter	24	133 MHz	115 MHz
16-bit loadable counter	16	68 MHz	45 MHz
16-bit up/down counter	16	68 MHz	45 MHz
24-bit accumulator	24	48 MHz	32 MHz
16-line-to-1-line multiplexer	10	14 ns	17 ns

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. When used as outputs, these registers provide fast Clock-to-output times; as inputs, they provide quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM cells. FLEX 8000 devices are configured at system power-up, with data stored in a configuration EPROM device or provided by a system controller. Altera offers the EPC1213 and EPC1064 serial Configuration EPROMs, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32K × 8-bit or larger EPROM or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because the reconfiguration requires less than 100 ms, real-time changes can be made during system operation.

Altera's MAX+PLUS II development system can be used to create FLEX 8000 logic designs with any combination of graphic, text, and waveform design entry. Full simulation, worst-case timing analysis, and functional testing are available for design verification. MAX+PLUS II also provides an EDIF 2 0 0 and EDIF 2 9 0 netlist interface for additional design entry and simulation support with industry-standard CAE tools. In addition, MAX+PLUS II can export Verilog and VHDL netlist files.

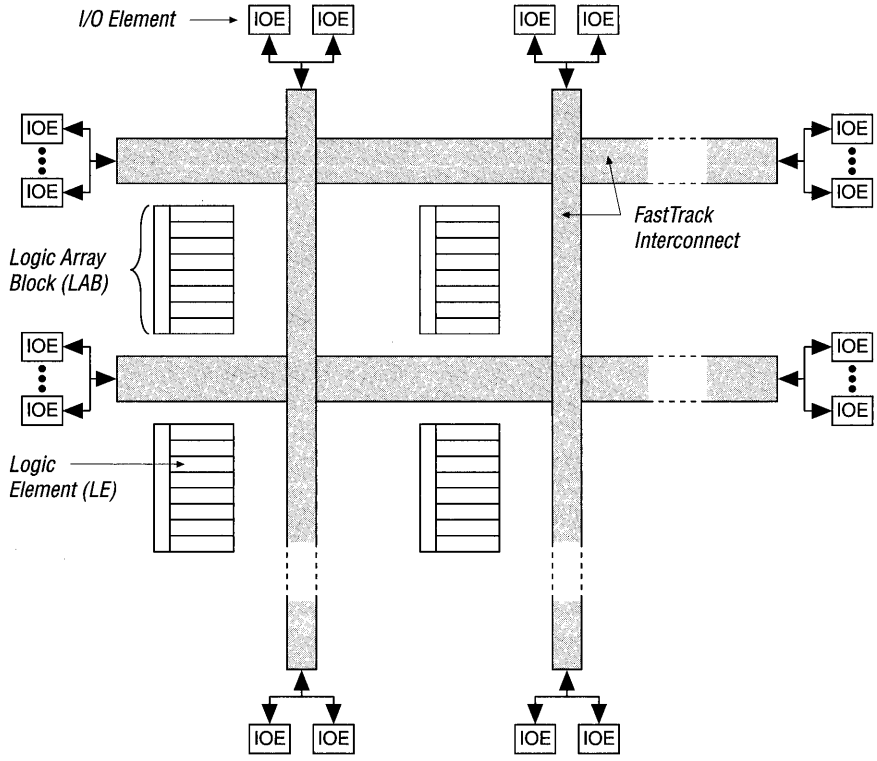
Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

LEs are grouped into sets of eight to create Logic Array Blocks (LABs). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram

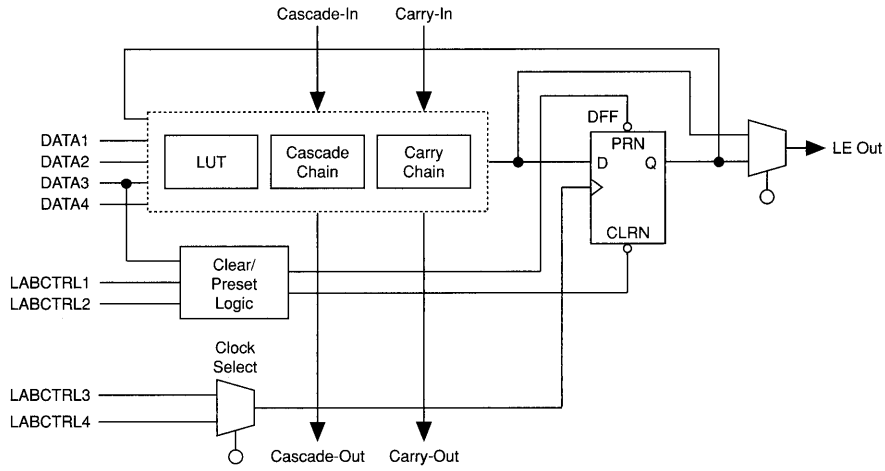


Signal interconnections within FLEX 8000 devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous lines that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input look-up table (LUT), a programmable flipflop, a carry chain, and a cascade chain. Figure 2 shows a block diagram of the LE.

Figure 2. FLEX 8000 Logic Element (LE)



The LUT is a function generator that can compute any function of four variables. The programmable flipflop in the LE can be configured to emulate D, T, JK, or SR operation. The Clock, Clear, and Preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

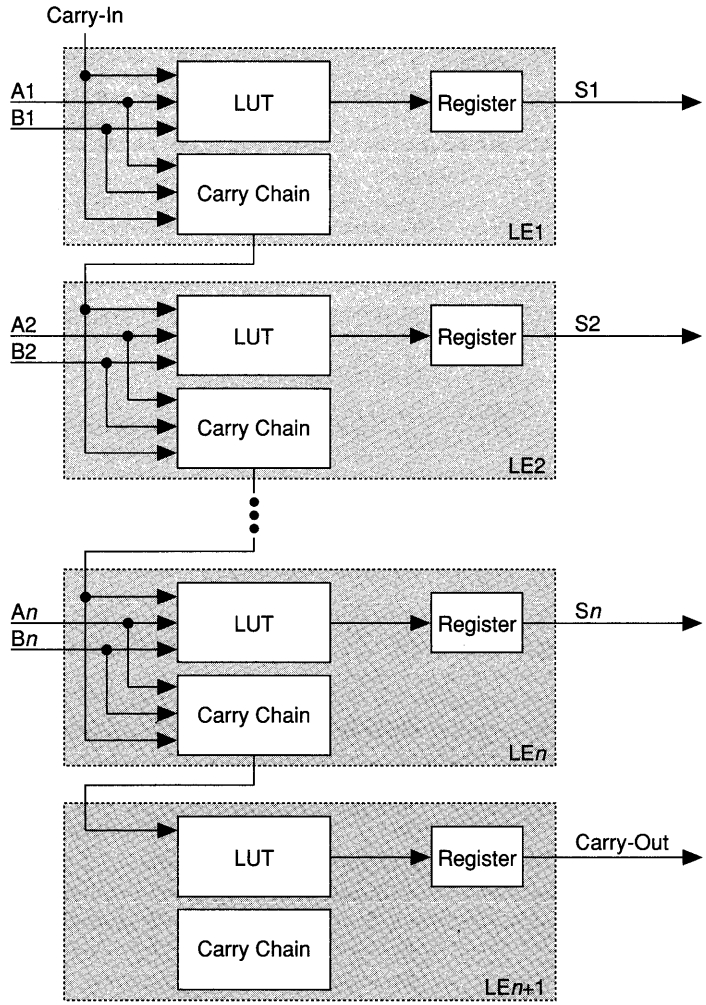
The FLEX 8000 architecture provides two dedicated high-speed data paths, the carry and cascade chains, that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Cascade and carry chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce the routing resources available for implementing other logic. Therefore, carry and cascade chains are recommended only for use in speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also specify carry chain logic manually during design entry.

Figure 3 shows how an *n*-bit full adder can be implemented in *n*+1 LEs by using the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal. In addition to mathematical functions, the carry chain logic supports very fast counters and comparators.

Figure 3. Carry Chain Operation

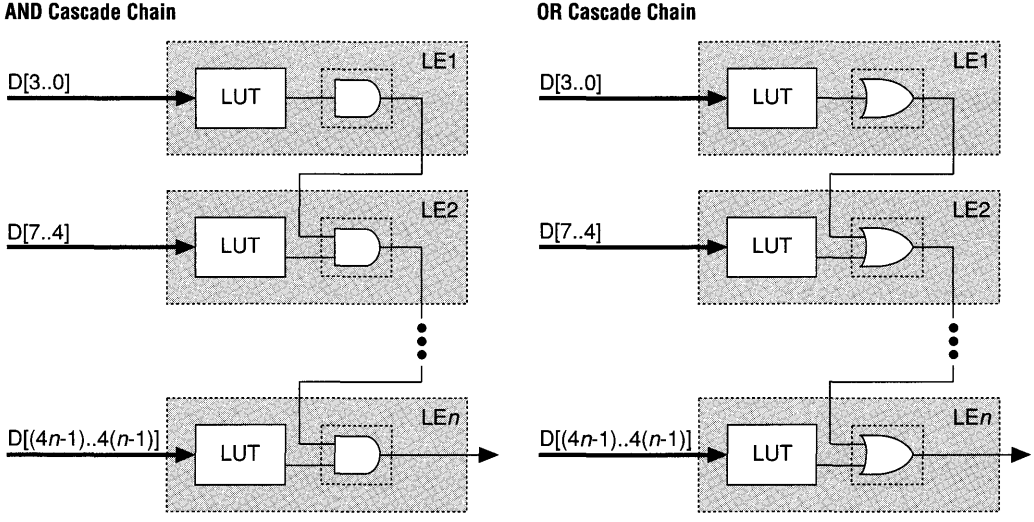


Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay of approximately 1 ns per LE. The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also specify cascade chain logic manually during design entry.

Figure 4 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. The LE delay is approximately 6 ns; the cascade chain delay is 1 ns. With the cascade chain, 9 ns is needed to decode a 16-bit address.

Figure 4. Cascade Chain Operation



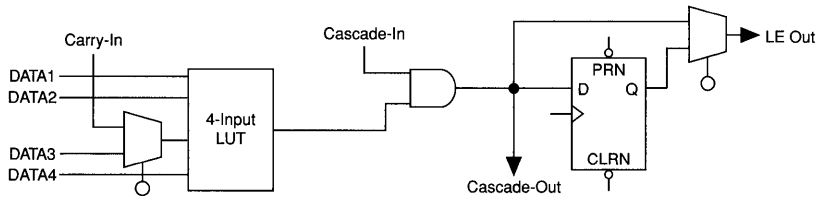
Logic Element Operating Modes

The FLEX 8000 logic element can operate in one of four modes, shown in Figure 5, each of which uses LE resources differently. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining

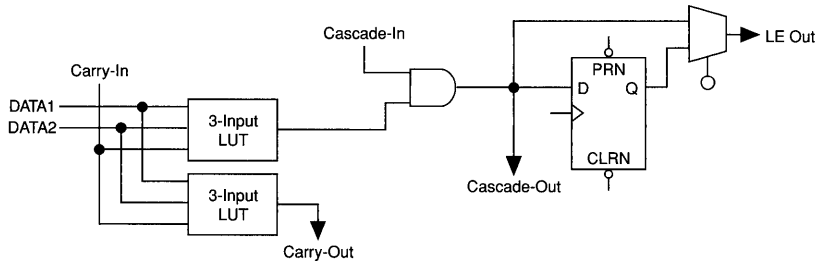
inputs to the LE provide Clock, Clear, and Preset control for the register. MAX+PLUS II software automatically chooses the best mode for each application. Design performance can also be enhanced by structuring designs for the appropriate operating mode.

Figure 5. FLEX 8000 Logic Element Operating Modes

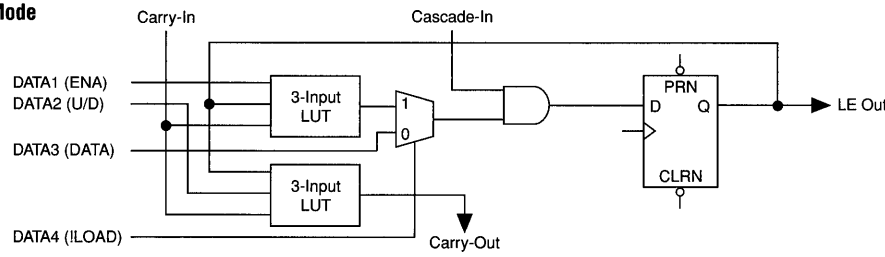
Normal Mode



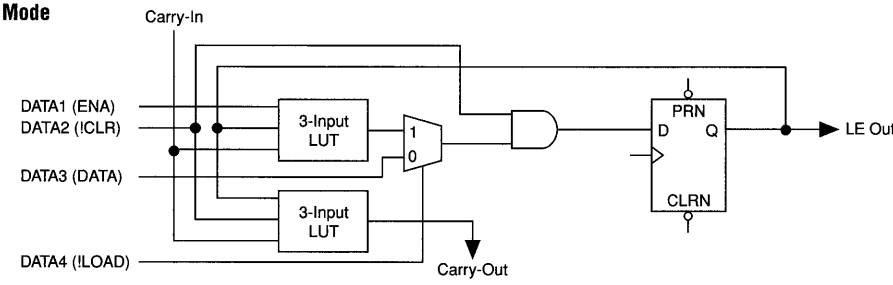
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The Normal mode is suitable for general logic applications and wide decode functions that can take advantage of a cascade chain. In Normal mode, four data inputs from the LAB local interconnect and the carry-in are the inputs to a 4-input LUT. The MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input that is physically controlled by a configurable SRAM bit. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE Out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the Q output of the programmable register.

Arithmetic Mode

The Arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 5, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output would be the sum of three bits: A, B, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The Arithmetic mode also supports a cascade chain.

Up/Down Counter Mode

The Up/Down Counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry look-ahead bit. A 2-line-to-1-line multiplexer provides synchronous loading. Data can also be loaded asynchronously with the Clear and Preset register control signals, without using the LUT resources.

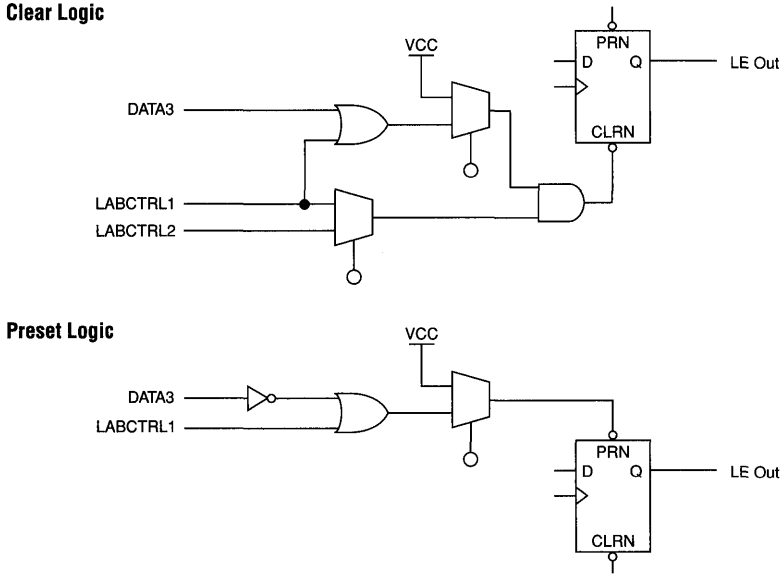
Clearable Counter Mode

The Clearable Counter mode is similar to the Up/Down Counter mode, but supports a synchronous Clear instead of the up/down control. The Clear function is substituted for the cascade-in signal in the Up/Down Counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry look-ahead bit. Synchronous loading is provided by a 2-line-to-1-line multiplexer, the output of which is ANDed with a synchronous Clear. This Clear function is substituted for the cascade-in signal that is available in the Up/Down Counter mode.

Clear/Preset Logic Control

Logic for the programmable register's Clear and Preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. See Figure 6. The Clear function is controlled by DATA3, LABCTRL1, and LABCTRL2; the Preset function is controlled by DATA3 and LABCTRL1. The MAX+PLUS II Compiler automatically selects the best control signal implementation during compilation. Since the Clear and Preset functions are active low, the Compiler automatically assigns a logic high to an unused Clear and/or Preset. Preset control can also be provided by using a Clear and inverting the output of the register. Inversion control is available for the inputs to both LEs and IOEs; therefore, if a register is cleared by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used to implement other logic.

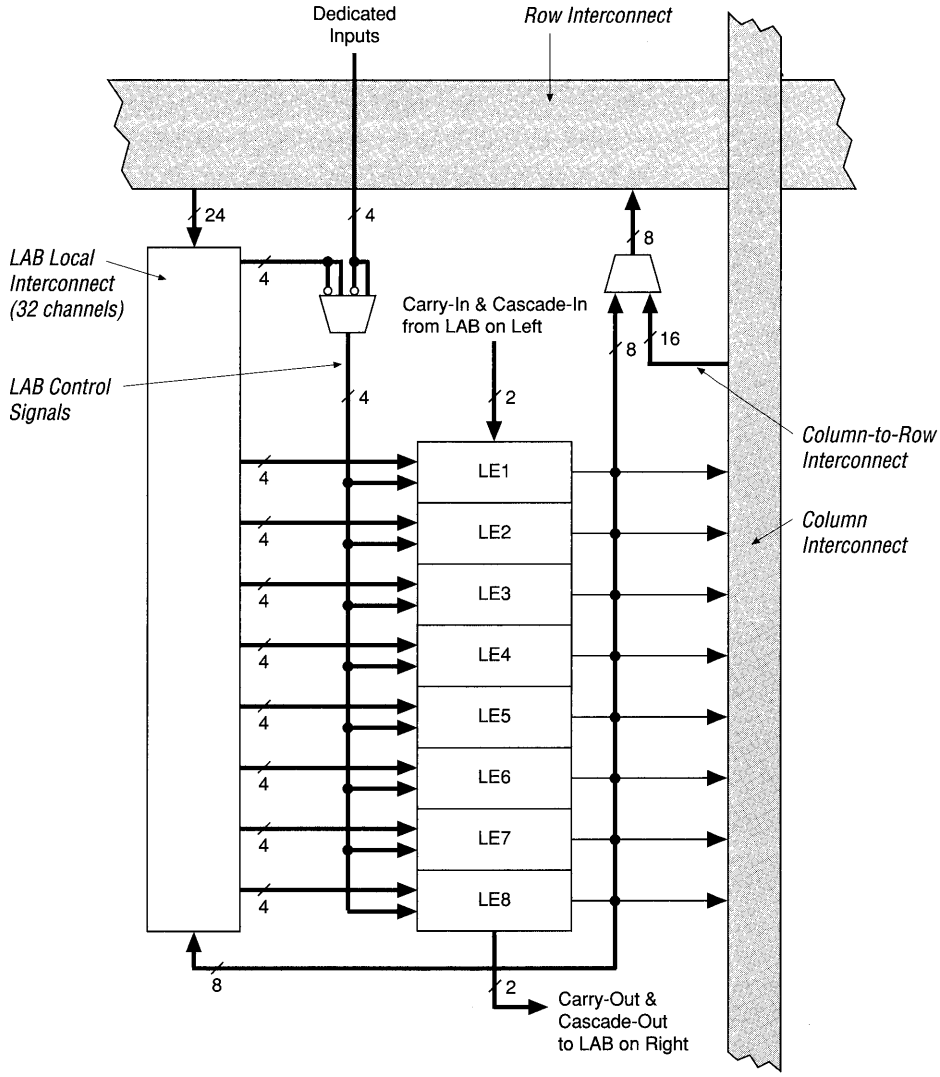
Figure 6. Logic Element Clear & Preset Logic



Logic Array Block

A Logic Array Block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture for efficient routing with high device utilization and high performance. Figure 7 shows a block diagram of the FLEX 8000 LAB.

Figure 7. Logic Array Block (LAB)



Data signals enter the LAB local interconnect from either the row interconnect or the dedicated inputs. The outputs of all eight LEs are also driven back into the LAB local interconnect via local feedback lines. Each LE in the LAB can drive signals out to the rest of the device via both row and column interconnect paths.

Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as Clocks, the other two for Clear/Preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global Clock, Clear, or Preset signals because they provide synchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. Programmable inversion is available for all four LAB control signals.

FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing paths that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each column of LABs has a dedicated column interconnect that routes signals out of the LABs in the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 3 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

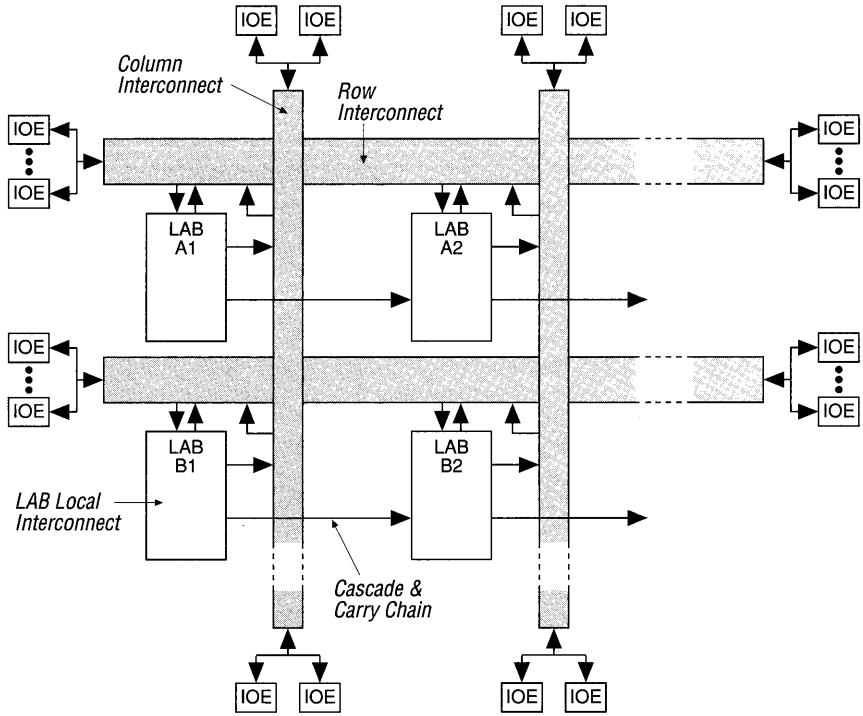
Table 3. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282, EPF8282V	2	168	13	16
EPF8452	2	168	21	16
EPF8820	4	168	21	16
EPF81188	6	168	21	16
EPF81500	6	216	27	16

Figure 8 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 8. FLEX 8000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



Dedicated Inputs

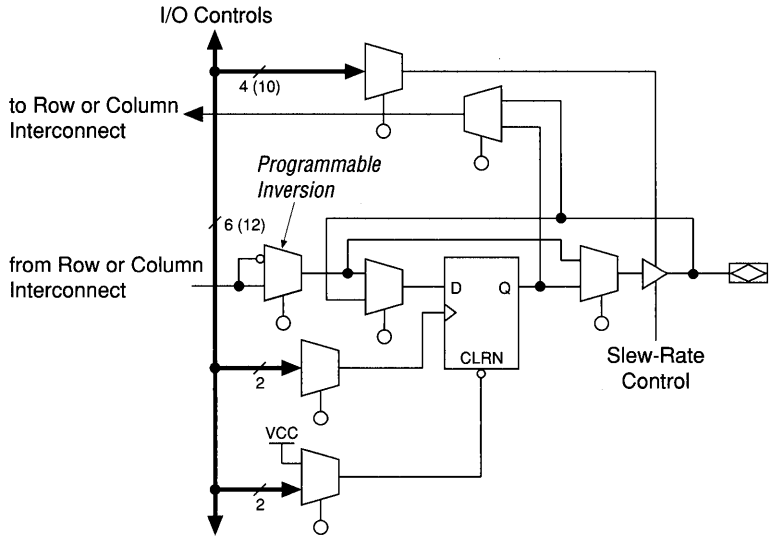
In addition to the general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew device-wide signal distribution, and are typically used for global Clock, Clear, and Preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs for nets with large fan-outs because they can feed the local interconnect of each LAB in the device.

I/O Element

Figure 9 shows the I/O element (IOE) block diagram. Signals enter the FLEX 8000 device from either the I/O pins that provide general-purpose input capability or the four dedicated inputs that are typically used for fast, global control signals. The IOEs are located at the ends of the row and column interconnect.

Figure 9. I/O Element (IOE)

Numbers in parentheses are for the EPF81500 device.



I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast Clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect when appropriate.

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides a speed increase of up to 1 ns, but may introduce more noise into a system than a slow slew rate. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

The Clock, Clear, and Output Enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. The I/O control signals can be configured to provide up to four Output Enable signals (ten in the EPF81500), and up to two Clock or Clear signals.

JTAG Boundary-Scan Testing

The Joint Test Action Group (JTAG) Boundary-Scan Test (BST) architecture in the EPF8282, EPF8282V, EPF8820, and EPF81500 FLEX devices makes it possible to isolate a device's internal circuitry from its I/O circuitry. The JTAG boundary-scan testing offers the capability to efficiently test components on circuit boards with tight lead spacing.

Only five device pins are needed to either force or observe data signals on the I/O pins of FLEX 8000 devices that comply with the JTAG IEEE Std 1149.1-1990 specification. Serial data is shifted into boundary-scan cells in the device; observed data is shifted out and externally compared to expected results. Boundary-scan testing offers efficient PC board testing, providing an electronic substitute for the traditional "bed of nails" test fixture. The JTAG BST architecture also supports interconnect fault testing and device functionality testing that are not available in other test systems. For detailed information on JTAG boundary-scan testing, refer to the JTAG IEEE Std 1149.1-1990 specification.

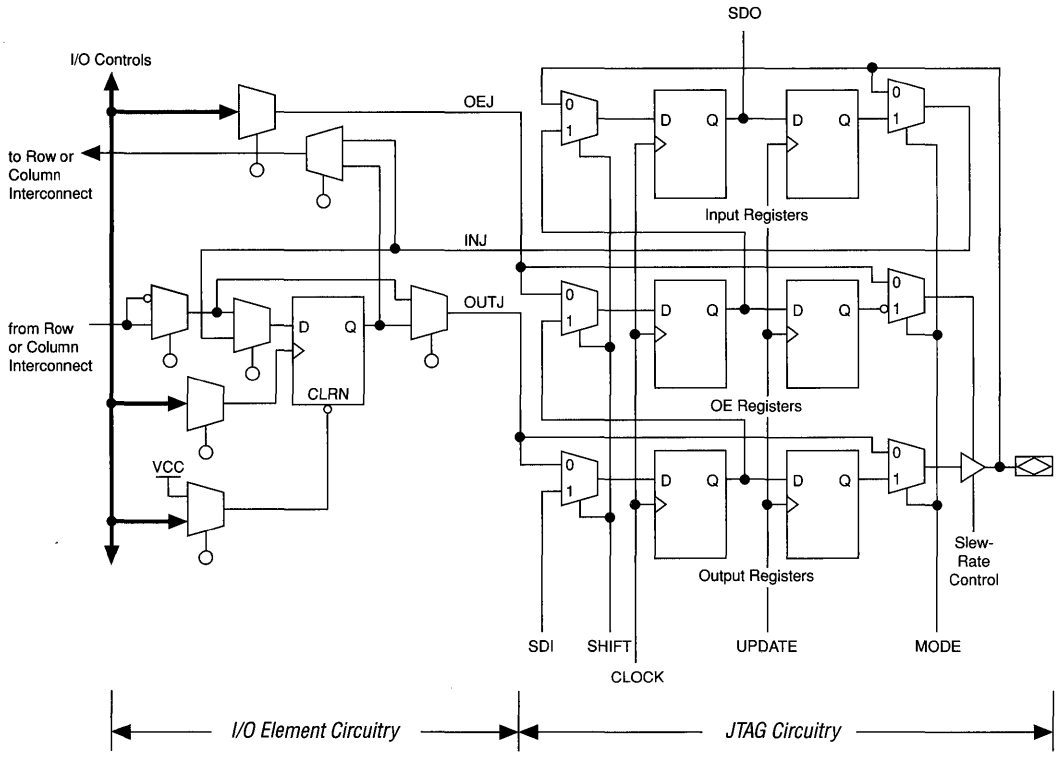
The JTAG BST-capable FLEX 8000 devices implement the mandatory SAMPLE, EXTEST, and BYPASS JTAG BST instructions. When a device is operating in JTAG BST mode, four I/O pins are used as the TDI, TDO, TMS, and TCLK JTAG pins. A dedicated active-low Reset pin, nTRST, initializes the JTAG BST circuitry. When the nTRST pin is driven low, the JTAG BST circuitry is reset and the device functions normally. Table 4 summarizes the functions of each of the JTAG BST pins.

Table 4. JTAG Pin Descriptions

Pin	Name	Description
TDI	Test data input	Serial input pin for instructions and test data.
TDO	Test data output	Serial data output pin for instructions and test data. The signal is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Serial input pin to select the JTAG instruction mode. TMS should be driven high during user-mode operation.
TCLK	Test clock input	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively. TCLK is also used to shift serial instruction data into the TMS pin.
nTRST	Test reset input	Active-low input to asynchronously initialize or reset the boundary-scan circuit. When nTRST is driven low, the boundary-scan circuit is reset, and the device operates in user mode.

Figure 10 shows the IOE of FLEX 8000 devices with JTAG BST registers. Each IOE has six registers that connect to internal data signals via the OUTJ, INJ, and OEJ signals. In an IOE that does not have JTAG BST registers (as shown in Figure 9), these signals are connected to the tri-state buffer's input, output, and Output Enable controls, respectively. The control signals for the JTAG BST registers are generated internally from the TMS and TCLK inputs.

Figure 10. I/O Element with JTAG Architecture



The JTAG BST registers shown in Figure 10 also exist for dedicated input and configuration pins in FLEX 8000 devices. However, only some of these pins provide output and Output Enable signals.

JTAG boundary-scan testing can be used either before or immediately after a FLEX 8000 device is configured. An Enable/Disable option bit for JTAG BST operation is set during device configuration.

The JTAG BST operation is controlled by a Test Access Port (TAP) Controller that drives three registers: a 3-bit instruction register that directs the flow of test data; a 1-bit bypass register; and a large boundary register located among the IOEs on the periphery of the FLEX 8000 device. The boundary registers for the EPF8282 and EPF8282V devices contain 273 bits; for the EPF8820, 465 bits; and for the EPF81500, 645 bits.

Figure 11 illustrates the JTAG BST register control functions. The instruction register is loaded and data is serially clocked through the TDI and TDO pins to perform testing.

Figure 11. JTAG Register Control

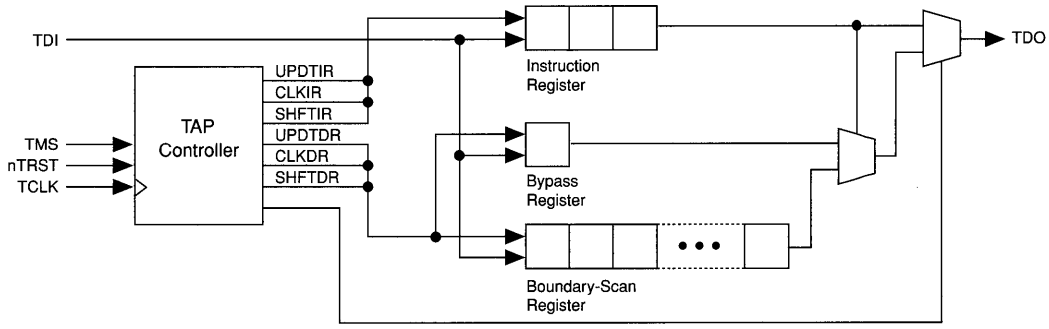


Table 5 describes the SAMPLE, EXTEST, and BYPASS test instruction modes. For additional information on JTAG boundary-scan testing for FLEX 8000 devices, contact Altera Applications at (800) 800-EPLD.

Table 5. JTAG Boundary-Scan Instruction Modes

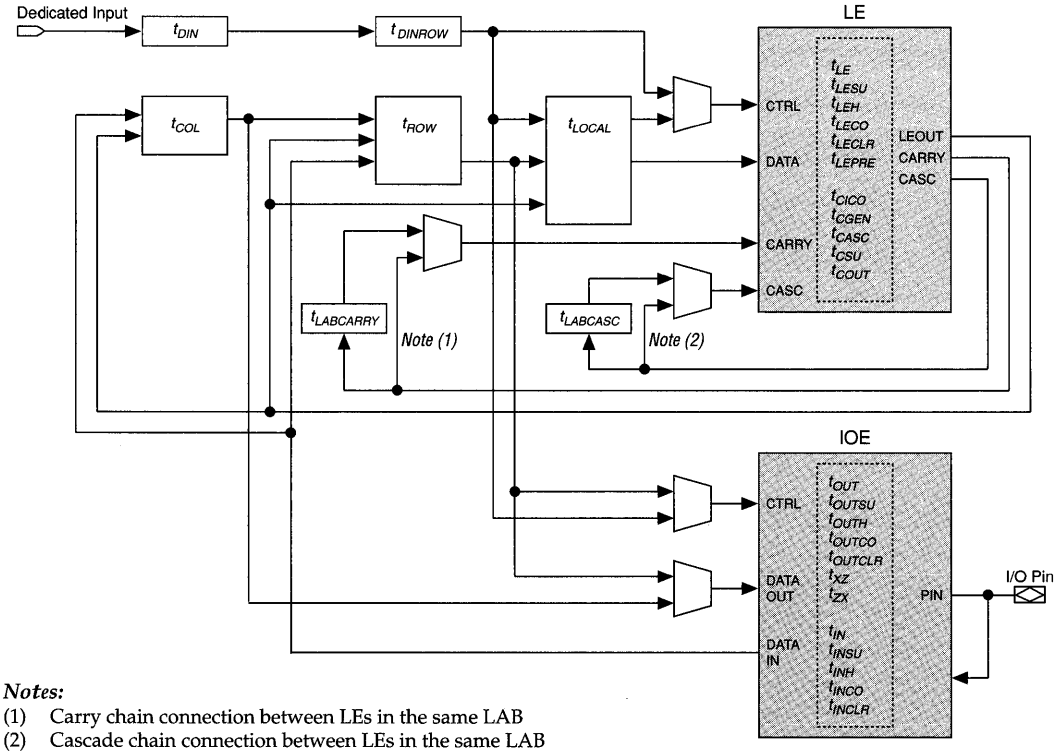
Mode	Opcode	Description
SAMPLE	101	Allows a snapshot of the signals at the device pins to be captured and examined while the device is operating normally. This mode also allows data to be loaded into update registers while the device is operating normally.
EXTEST	000	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	111	Enables the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass through the selected device synchronously to adjacent devices while the device is operating normally.

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation analysis. This predictable performance stands in marked contrast to that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard CAE tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and system-level performance analysis.

The FLEX 8000 timing model in Figure 12 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and

Figure 12. FLEX 8000 Timing Model



Notes:
(1) Carry chain connection between LEs in the same LAB
(2) Cascade chain connection between LEs in the same LAB

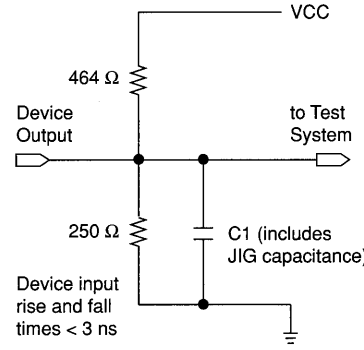
cascade interconnect paths. Each parameter shown in Figure 12 is expressed as a worst-case value in the "Internal Timing Characteristics" tables in this data sheet. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine final worst-case performance.

Generic Testing

Each FLEX 8000 device is functionally tested and guaranteed. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 13. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 13. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Symbol	Parameter	EPF81500	EPF81188	EPF8820	EPF8452	EPF8282	Unit
I_{MAX}	Maximum DC V_{CC} or GND current	1250	1000	850	500	400	mA
P_D	Maximum Power dissipation	6.9	5.5	4.7	2.75	2.2	W

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Ambient temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (3)*		500		µA

Capacitance *Note (4)*

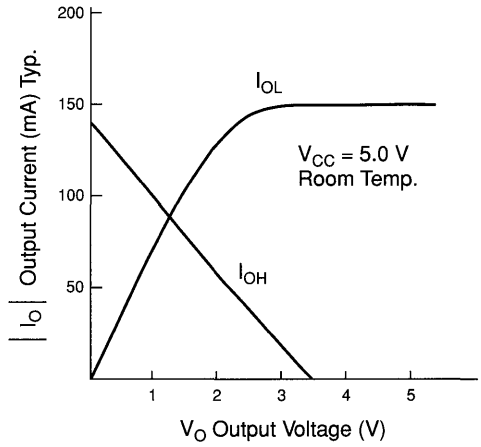
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(4) Capacitance is sample-tested only.

Figure 14 shows the maximum output drive characteristics of FLEX 8000 I/O pins.

Figure 14. FLEX 8000 Maximum Output Drive Characteristics



EPF81500 Internal Timing Characteristics *Note (1)*

EPF81500 I/O Element Output Timing Parameters			EPF81500-2		EPF81500-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OUTSU}	Setup time for output register		2.0		2.0		ns
t_{OUTH}	Hold time for output register		0		0		ns
t_{OUTCO}	Clock-to-output time for output register	C1 = 35 pF		4.0		5.0	ns
t_{OUT}	Combinatorial time for I/O output			3.0		4.0	ns
t_{OUTCLR}	Clear time for output register			4.2		5.2	ns
t_{XZ}	Valid to Z time for IOE	C1 = 5 pF		3.0		4.0	ns
t_{ZX}	Z to valid time for IOE	C1 = 35 pF		3.0		4.0	ns

EPF81500 I/O Element Input Timing Parameters			EPF81500-2		EPF81500-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{INSU}	Setup time for input register		2.8		2.8		ns
t_{INH}	Hold time for input register		0		0		ns
t_{INCO}	Clock-to-output time for input register			2.0		3.0	ns
t_{IN}	Input pad and buffer delay			1.8		2.8	ns
t_{INCLR}	Clear time for input register			2.2		3.2	ns

EPF81500 Logic Element Timing Parameters			EPF81500-2		EPF81500-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LESU}	Setup time for LE register		2.8		3.7		ns
t_{LEH}	Hold time for LE register		0		0		ns
t_{LECO}	Clock-to-output time for LE			3.7		4.0	ns
t_{LE}	Combinatorial time for LE			5.6		6.0	ns
t_{LECLR}	Clear time for LE register			4.0		4.3	ns
t_{LEPRE}	Preset time for LE register			4.0		4.3	ns
t_{CICO}	Carry-in to carry-out time			0.7		1.1	ns
t_{CGEN}	Carry generation time			2.6		3.3	ns
t_{CASC}	Cascade-in to cascade-out time			1.1		2.0	ns
t_{CSU}	Carry-in to register setup time		1.8		2.7		ns
t_{COUT}	Carry-in to LE out delay			4.6		5.0	ns

EPF81500 Interconnect Timing Parameters			EPF81500-2		EPF81500-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade time between LEs in different LABs			0.5		0.9	ns
$t_{LABCARRY}$	Carry time between LEs in different LABs			0.5		0.6	ns
t_{COL}	Column interconnect routing delay			3.0		3.0	ns
t_{DIN}	Dedicated input pad delay			3.0		4.0	ns
t_{LOCAL}	LAB local interconnect delay			1.0		1.0	ns
t_{DINROW}	Dedicated input routing delay	*Note (2)*		4.0		5.0	ns
t_{ROW}	Row interconnect routing delay			5.0		5.0	ns

EPF81500 External Reference Timing Characteristics *Note (3)*

			EPF81500-2		EPF81500-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	I/O pin to I/O pin via row, LE, and column	C1 = 35 pF		19		22	ns
t_2	I/O pin to I/O pin via row, LE, and row			20		24	ns

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) The t_{ROW} and t_{DINROW} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(3) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

EPF81188 Internal Timing Characteristics *Note (1)*

EPF81188 I/O Element Output Timing Parameters			EPF81188-2		EPF81188-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OUTSU}	Setup time for output register		2.0		2.0		ns
t_{OUTH}	Hold time for output register		0		0		ns
t_{OUTCO}	Clock-to-output time for output register	C1 = 35 pF		4.0		5.0	ns
t_{OUT}	Combinatorial time for I/O output			3.0		4.0	ns
t_{OUTCLR}	Clear time for output register			4.2		5.2	ns
t_{XZ}	Valid to Z time for IOE	C1 = 5 pF		3.0		4.0	ns
t_{ZX}	Z to valid time for IOE	C1 = 35 pF		3.0		4.0	ns

EPF81188 I/O Element Input Timing Parameters			EPF81188-2		EPF81188-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{INSU}	Setup time for input register		2.8		2.8		ns
t_{INH}	Hold time for input register		0		0		ns
t_{INCO}	Clock-to-output time for input register			2.0		3.0	ns
t_{IN}	Input pad and buffer delay			1.8		2.8	ns
t_{INCLR}	Clear time for input register			2.2		3.2	ns

EPF81188 Logic Element Timing Parameters			EPF81188-2		EPF81188-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LESU}	Setup time for LE register		2.8		3.7		ns
t_{LEH}	Hold time for LE register		0		0		ns
t_{LECO}	Clock-to-output time for LE			3.7		4.0	ns
t_{LE}	Combinatorial time for LE			5.6		6.0	ns
t_{LECLR}	Clear time for LE register			4.0		4.3	ns
t_{LEPRE}	Preset time for LE register			4.0		4.3	ns
t_{CICO}	Carry-in to carry-out time			0.7		1.1	ns
t_{CGEN}	Carry generation time			2.6		3.3	ns
t_{CASC}	Cascade-in to cascade-out time			1.1		2.0	ns
t_{CSU}	Carry-in to register setup time		1.8		2.7		ns
t_{COUT}	Carry-in to LE out delay			4.6		5.0	ns

EPF81188 Interconnect Timing Parameters			EPF81188-2		EPF81188-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade time between LEs in different LABs			0.5		0.9	ns
$t_{LABCARRY}$	Carry time between LEs in different LABs			0.5		0.6	ns
t_{COL}	Column interconnect routing delay			3.0		3.0	ns
t_{DIN}	Dedicated input pad delay			3.0		4.0	ns
t_{LOCAL}	LAB local interconnect delay			1.0		1.0	ns
t_{DINROW}	Dedicated input routing delay	*Note (2)*		4.0		5.0	ns
t_{ROW}	Row interconnect routing delay			5.0		5.0	ns

EPF81188 External Reference Timing Characteristics *Note (3)*

			EPF81188-2		EPF81188-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	I/O pin to I/O pin via row, LE, and column	C1 = 35 pF		19		22	ns
t_2	I/O pin to I/O pin via row, LE, and row			20		24	ns

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) The t_{ROW} and t_{DINROW} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(3) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

EPF8820 Internal Timing Characteristics *Note (1)*

EPF8820 I/O Element Output Timing Parameters			EPF8820-2		EPF8820-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OUTSU}	Setup time for output register		2.0		2.0		ns
t_{OUTH}	Hold time for output register		0		0		ns
t_{OUTCO}	Clock-to-output time for output register	C1 = 35 pF		4.0		5.0	ns
t_{OUT}	Combinatorial time for I/O output			3.0		4.0	ns
t_{OUTCLR}	Clear time for output register			4.2		5.2	ns
t_{XZ}	Valid to Z time for IOE	C1 = 5 pF		3.0		4.0	ns
t_{ZX}	Z to valid time for IOE	C1 = 35 pF		3.0		4.0	ns

EPF8820 I/O Element Input Timing Parameters			EPF8820-2		EPF8820-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{INSU}	Setup time for input register		2.8		2.8		ns
t_{INH}	Hold time for input register		0		0		ns
t_{INCO}	Clock-to-output time for input register			2.0		3.0	ns
t_{IN}	Input pad and buffer delay			1.8		2.8	ns
t_{INCLR}	Clear time for input register			2.2		3.2	ns

EPF8820 Logic Element Timing Parameters			EPF8820-2		EPF8820-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LESU}	Setup time for LE register		2.8		3.7		ns
t_{LEH}	Hold time for LE register		0		0		ns
t_{LECO}	Clock-to-output time for LE			3.7		4.0	ns
t_{LE}	Combinatorial time for LE			5.6		6.0	ns
t_{LECLR}	Clear time for LE register			4.0		4.3	ns
t_{LEPRE}	Preset time for LE register			4.0		4.3	ns
t_{CICO}	Carry-in to carry-out time			0.7		1.1	ns
t_{CGEN}	Carry generation time			2.6		3.3	ns
t_{CASC}	Cascade-in to cascade-out time			1.1		2.0	ns
t_{CSU}	Carry-in to register setup time		1.8		2.7		ns
t_{COUT}	Carry-in to LE out delay			4.6		5.0	ns

EPF8820 Interconnect Timing Parameters			EPF8820-2		EPF8820-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade time between LEs in different LABs			0.5		0.9	ns
$t_{LABCARRY}$	Carry time between LEs in different LABs			0.5		0.6	ns
t_{COL}	Column interconnect routing delay			3.0		3.0	ns
t_{DIN}	Dedicated input pad delay			3.0		4.0	ns
t_{LOCAL}	LAB local interconnect delay			1.0		1.0	ns
t_{DINROW}	Dedicated input routing delay	*Note (2)*		4.0		5.0	ns
t_{ROW}	Row interconnect routing delay			5.0		5.0	ns

EPF8820 External Reference Timing Characteristics *Note (3)*

			EPF8820-2		EPF8820-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	I/O pin to I/O pin via row, LE, and column	C1 = 35 pF		19		22	ns
t_2	I/O pin to I/O pin via row, LE, and row			20		24	ns

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) The t_{ROW} and t_{DINROW} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(3) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

EPF8452 Internal Timing Characteristics *Note (1)*

EPF8452 I/O Element Output Timing Parameters			EPF8452-2		EPF8452-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OUTSU}	Setup time for output register		2.0		2.0		ns
t_{OUTH}	Hold time for output register		0		0		ns
t_{OUTCO}	Clock-to-output time for output register	C1 = 35 pF		4.0		5.0	ns
t_{OUT}	Combinatorial time for I/O output			3.0		4.0	ns
t_{OUTCLR}	Clear time for output register			4.2		5.2	ns
t_{XZ}	Valid to Z time for IOE	C1 = 5 pF		3.0		4.0	ns
t_{ZX}	Z to valid time for IOE	C1 = 35 pF		3.0		4.0	ns

EPF8452 I/O Element Input Timing Parameters			EPF8452-2		EPF8452-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{INSU}	Setup time for input register		2.8		2.8		ns
t_{INH}	Hold time for input register		0		0		ns
t_{INCO}	Clock-to-output time for input register			2.0		3.0	ns
t_{IN}	Input pad and buffer delay			1.8		2.8	ns
t_{INCLR}	Clear time for input register			2.3		3.3	ns

EPF8452 Logic Element Timing Parameters			EPF8452-2		EPF8452-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LESU}	Setup time for LE register		2.8		3.7		ns
t_{LEH}	Hold time for LE register		0		0		ns
t_{LECO}	Clock-to-output time for LE			3.7		4.0	ns
t_{LE}	Combinatorial time for LE			5.6		6.0	ns
t_{LECLR}	Clear time for LE register			4.0		4.3	ns
t_{LEPRE}	Preset time for LE register			4.0		4.3	ns
t_{CICO}	Carry-in to carry-out time			0.7		1.1	ns
t_{CGEN}	Carry generation time			2.6		3.3	ns
t_{CASC}	Cascade-in to cascade-out time			1.1		2.0	ns
t_{CSU}	Carry-in to register setup time		1.8		2.7		ns
t_{COUT}	Carry-in to LE out delay			4.6		5.0	ns

EPF8452 Interconnect Timing Parameters			EPF8452-2		EPF8452-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade time between LEs in different LABs			0.5		0.9	ns
$t_{LABCARRY}$	Carry time between LEs in different LABs			0.5		0.6	ns
t_{COL}	Column interconnect routing delay			3.0		3.0	ns
t_{DIN}	Dedicated input pad delay			3.0		4.0	ns
t_{LOCAL}	LAB local interconnect delay			1.0		1.0	ns
t_{DINROW}	Dedicated input routing delay	*Note (2)*		4.0		5.0	ns
t_{ROW}	Row interconnect routing delay			5.0		5.0	ns

EPF8452 External Reference Timing Characteristics *Note (3)*

			EPF8452-2		EPF8452-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	I/O pin to I/O pin via row, LE, and column	C1 = 35 pF		19		22	ns
t_2	I/O pin to I/O pin via row, LE, and row			20		24	ns

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) The t_{ROW} and t_{DINROW} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(3) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

EPF8282 Internal Timing Characteristics *Note (1)*

EPF8282 I/O Element Output Timing Parameters			EPF8282-2		EPF8282-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OUTSU}	Setup time for output register		2.0		2.0		ns
t_{OUTH}	Hold time for output register		0		0		ns
t_{OUTCO}	Clock-to-output time for output register	C1 = 35 pF		4.5		6.0	ns
t_{OUT}	Combinatorial time for I/O output			3.5		5.0	ns
t_{OUTCLR}	Clear time for output register			4.8		6.3	ns
t_{XZ}	Valid to Z time for IOE	C1 = 5 pF		3.5		5.0	ns
t_{ZX}	Z to valid time for IOE	C1 = 35 pF		3.5		5.0	ns

EPF8282 I/O Element Input Timing Parameters			EPF8282-2		EPF8282-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{INSU}	Setup time for input register		2.8		2.8		ns
t_{INH}	Hold time for input register		0		0		ns
t_{INCO}	Clock-to-output time for input register			2.0		3.0	ns
t_{IN}	Input pad and buffer delay			1.8		2.8	ns
t_{INCLR}	Clear time for input register			2.3		3.3	ns

EPF8282 Logic Element Timing Parameters			EPF8282-2		EPF8282-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LESU}	Setup time for LE register		2.5		3.7		ns
t_{LEH}	Hold time for LE register		0		0		ns
t_{LECO}	Clock-to-output time for LE			3.3		4.0	ns
t_{LE}	Combinatorial time for LE			5.0		6.0	ns
t_{LECLR}	Clear time for LE register			3.6		4.3	ns
t_{LEPRE}	Preset time for LE register			3.6		4.3	ns
t_{CICO}	Carry-in to carry-out time			0.7		1.1	ns
t_{CGEN}	Carry generation time			2.3		3.3	ns
t_{CASC}	Cascade-in to cascade-out time			1.1		2.0	ns
t_{CSU}	Carry-in to register setup time		1.6		2.7		ns
t_{COUT}	Carry-in to LE out delay			4.1		5.0	ns

EPF8282 Interconnect Timing Parameters			EPF8282-2		EPF8282-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade time between LEs in different LABs			0.5		0.9	ns
$t_{LABCARRY}$	Carry time between LEs in different LABs			0.5		0.6	ns
t_{COL}	Column interconnect routing delay			2.5		2.5	ns
t_{DIN}	Dedicated input pad delay			3.0		4.0	ns
t_{LOCAL}	LAB local interconnect delay			1.0		1.0	ns
t_{DINROW}	Dedicated input routing delay	*Note (2)*		3.0		3.5	ns
t_{ROW}	Row interconnect routing delay			4.2		4.2	ns

EPF8282 External Reference Timing Characteristics *Note (3)*

			EPF8282-2		EPF8282-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	I/O pin to I/O pin via row, LE, and column	C1 = 35 pF		17		20	ns
t_2	I/O pin to I/O pin via row, LE, and row			18		22	ns

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) The t_{ROW} and t_{DINROW} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(3) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

Calculating FLEX 8000 Supply Current

The V_{CC} supply current for FLEX 8000 devices, I_{CC}, can be calculated with the following equation:

$$I_{CC} = I_{CCSTANDBY} + I_{CCOUTPUT} + I_{CCACTIVE}$$

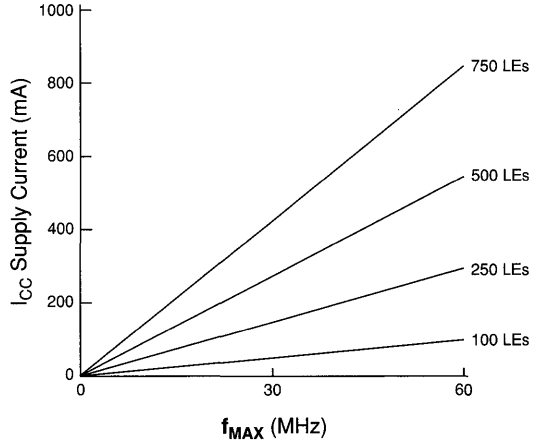
Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "DC Operating Conditions" table earlier in this data sheet. The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated on the basis of the relationship that each LE typically consumes 150 µA/MHz. The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = 150\frac{\mu A}{MHz \bullet LE} \times F \times N \times s$$

In this equation, F is the maximum operating frequency in MHz; N is number of LEs used in the device; and s is the percentage of LEs that switch on each Clock edge. Altera recommends that designers use a value of 12.5% for s (s = 0.125), which is based on a 16-bit counter in which 2 out of 16 (12.5%) of the bits switch on each Clock edge.

Figure 15 shows the relationship between I_{CC} and operating frequency for LE utilization values ranging from 100 to 750 LEs.

Figure 15. FLEX 8000 I_{CC} vs. Operating Frequency



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This data sheet summarizes the device operating modes and available device configuration schemes; refer to *Application Note 33 (Configuring FLEX 8000 Devices)* in this data book for detailed descriptions of device configuration options, device configuration pins, and information on configuring FLEX 8000 devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 8000 architecture uses SRAM technology that requires configuration data to be loaded whenever the circuit powers up and begins operation. The process of physically loading the SRAM programming data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The configuration and initialization processes together are called "command mode"; normal device operation is called "user mode."

The SRAM technology allows FLEX 8000 devices to be reconfigured in-circuit by loading new programming data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external EPROM devices, and completing the loading process. The Clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates at up to 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device, which operates as a slave. Table 6 shows the source of data for each of the six configuration schemes.

Table 6. Configuration Schemes

Configuration Scheme	Acronym	Data Source
Active Serial	AS	Altera Configuration EPROM
Active Parallel Up	APU	Parallel EPROM
Active Parallel Down	APD	Parallel EPROM
Passive Serial	PS	Serial data path
Passive Parallel Synchronous	PPS	Intelligent host
Passive Parallel Asynchronous	PPA	Intelligent host

MAX+PLUS II Development System

FLEX 8000 devices are supported by Altera's MAX+PLUS II development system. MAX+PLUS II also supports the Altera Classic, MAX 5000/EPS464, and MAX 7000 device families.

Designs can be entered as logic schematics with the Graphic Editor; as state machines, truth tables, conditional logic, and Boolean equations with the Altera Hardware Description Language (AHDL); or as waveforms with the Waveform Editor. Logic synthesis and minimization automatically optimize the logic of a design. MAX+PLUS II also provides automatic design partitioning into multiple devices from the same family. Design verification and timing analysis are performed with the built-in Simulator and Timing Analyzer. Errors in a design can be automatically located and highlighted in the original design files.

MAX+PLUS II software runs on 386- and 486-based PCs, as well as Sun SPARCstations and HP 9000 Series 700 workstations. It gives designers the tools to create complex logic designs quickly and efficiently. MAX+PLUS II provides an EDIF netlist interface for additional design entry and simulation support with popular CAE tools from Cadence, Intergraph, Logic Modeling, Mentor Graphics, Synopsys, Viewlogic, and others. MAX+PLUS II also exports Verilog and VHDL netlist files for use with other industry-standard design verification tools.

Altera's FLEX 8000-compatible programming hardware includes the Altera Logic Programmer card, the Master Programming Unit (MPU), and various device adapters. The MPU supports continuity checking to ensure adequate electrical contact between the adapter and the device. Configuration EPROM device adapters are shipped with a special downloading cable that allows users to configure FLEX 8000 devices in-circuit with Altera programming hardware and the MAX+PLUS II Programmer. For more information on programming hardware, see *Altera Programming Hardware* in this data book. Further details about the MAX+PLUS II development system are available in the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Device Pin-Outs

Tables 7 and 8 show the pin names and numbers for each device package.

Table 7. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	84-Pin PLCC EPF8452	84-Pin PLCC EPF8282	100-Pin TQFP EPF8282	160-Pin PGA EPF8452	160-Pin PQFP EPF8452
nSP *(1)*	75	75	75	R1	120
MSEL0 *(1)*	74	74	74	P2	117
MSEL1 *(1)*	53	53	51	A1	84
nSTATUS *(1)*	32	32	24	C13	37
nCONFIG *(1)*	33	33	25	A15	40
nWS	30	30	22	F13	30
nRS	48	48	42	C6	71
RDCLK	49	49	45	B5	73
DCLK *(1)*	10	10	100	P14	1
nCS	29	29	21	D15	29
CS	28	28	19	E15	27
RDYnBUSY	77	77	77	P3	125
CLKUSR	50	50	47	C5	76
CONF_DONE *(1)*	11	11	1	N13	4
ADD17	51	51	49	B4	78
ADD16	55	36	28	E2	91
ADD15	56	56	55	D1	92
ADD14	57	57	57	E1	94
ADD13	58	58	58	F3	95
ADD12	60	60	59	F2	96
ADD11	61	61	60	F1	97
ADD10	62	62	61	G2	98
ADD9	63	63	62	G1	99
ADD8	64	64	64	H1	101
ADD7	65	65	65	H2	102
ADD6	66	66	66	J1	103
ADD5	67	67	67	J2	104
ADD4	69	69	68	K2	105
ADD3	70	70	69	K1	106
ADD2	71	71	71	K3	109
ADD1	72	76	76	M1	110
ADD0	76	78	78	N3	123

Table 7. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	84-Pin PLCC EPF8452	84-Pin PLCC EPF8282	100-Pin TQFP EPF8282	160-Pin PGA EPF8452	160-Pin PQFP EPF8452
DATA7	2	3	90	P8	144
DATA6	4	4	91	P10	150
DATA5	6	6	92	R12	152
DATA4	7	7	95	R13	154
DATA3	8	8	97	P13	157
DATA2	9	9	99	R14	159
DATA1	13	13	4	N15	11
DATA0	14	14	5	K13	12
TDI *(2)*	–	55	54	–	–
TDO *(2)*	–	27	18	–	–
TCLK *(2)*	–	72	72	–	–
TMS *(2)*	–	20	11	–	–
nTRST *(1)*	–	52	50	–	–
Dedicated Inputs	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	C3, D14, N2, R15	5, 36, 85, 116
VCC	17, 38, 52, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155
No Connect (N.C.)	–	–	–	–	2, 3, 38, 39, 70, 82, 83, 118, 119, 148
Total User I/O Pins	64	64	74	116	116

Notes:
(1) Dedicated configuration pin (not available as a user I/O pin).
(2) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.

Table 8. FLEX 8000 192-, 208-, 232- & 240-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	192-Pin PGA EPF8820	208-Pin QFP EPF8820	232-Pin PGA EPF81188	240-Pin QFP EPF81188
nSP *(1)*	R15	207	C14	237
MSEL0 *(1)*	T15	4	G15	21
MSEL1 *(1)*	T3	49	L15	40
nSTATUS *(1)*	B3	108	L3	141
nCONFIG *(1)*	C3	103	R4	117
nWS	C5	114	P1	133
nRS	B5	116	N1	137
RDCLK	C11	137	G2	158
DCLK *(1)*	C15	158	C4	184
nCS	B13	145	E2	166
CS	A16	148	E3	169
RDYnBUSY	A8	127	K2	146
CLKUSR	A10	134	H2	155
CONF_DONE *(1)*	B15	153	G3	160
ADD17	R5	43	R15	58
ADD16	U3	42	T17	56
ADD15	T5	41	P15	54
ADD14	U4	40	M14	47
ADD13	R6	39	M15	45
ADD12	T6	35	M16	43
ADD11	R7	33	K15	36
ADD10	T7	31	K17	34
ADD9	T8	29	J14	32
ADD8	U9	25	J15	29
ADD7	U10	23	H17	27
ADD6	U11	21	H15	25
ADD5	U12	19	F16	18
ADD4	R12	14	F15	16
ADD3	U14	13	F14	14
ADD2	U15	11	D15	7
ADD1	R13	10	B17	5
ADD0	U16	9	C15	3

Table 8. FLEX 8000 192-, 208-, 232- & 240-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	192-Pin PGA EPF8820	208-Pin QFP EPF8820	232-Pin PGA EPF81188	240-Pin QFP EPF81188
DATA7	H17	178	A7	205
DATA6	G17	176	D8	203
DATA5	F17	174	B7	200
DATA4	E17	172	C7	198
DATA3	G15	171	D7	196
DATA2	F15	167	B5	194
DATA1	E16	165	A3	191
DATA0	C16	162	A2	189
TDI *(2)*	R11	20	–	–
TDO *(2)*	B9	129	–	–
TCLK *(2)*	U8	30	–	–
TMS *(2)*	U7	32	–	–
nTRST *(1)*	R3	54	–	–
Dedicated Inputs	A5, U5, U13, A13	17, 36, 121, 140	C1, C17, R1, R17	10, 51, 130, 171
VCC	C8, C9, C10, D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14, R8, R9, R10, R14	5, 6, 26, 27, 48, 55, 69, 87, 102, 119, 131, 141, 159, 173, 191, 206	E4, E8, E10, E14, F5, F13, H4, H5, H13, H14, K5, K13, L4, L14, M5, M13, N8, N10, P12, R14, U1	19, 20, 41, 42, 64, 65, 66, 81, 99, 114, 116, 128, 140, 150, 162, 172, 186, 202, 220, 235, 236
GND	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229
No Connect (N.C.)	–	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	–	61, 62, 119, 120, 181, 182, 239, 240
Total User I/O Pins	148	148	180	180

Notes:
(1) Dedicated configuration pin (not available as a user I/O pin).
(2) Available as a user I/O pin if device is not configured to use JTAG BST circuitry.

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ALTERA

MAX 7000

Programmable Logic Device Family

August 1993, ver. 1 | Data Sheet

Features...

- High-performance, erasable CMOS devices based on second-generation Multiple Array MatriX (MAX) architecture
- Complete EPLD family with logic densities up to 10,000 available gates (5,000 usable gates). See Table 1.
- Fast, 7.5-ns pin-to-pin logic delays with up to 125-MHz counter frequencies (including interconnect)
- Programmable power-saver mode for up to 50% power reduction in each macrocell
- Programmable Security Bit for total protection of proprietary designs
- Configurable expander product-term distribution allowing up to 32 product terms in each macrocell
- 44 to 208 pins available in J-lead, pin-grid array (PGA), and quad flat pack (QFP) packages, including 1-mm thin quad flat pack (TQFP)
- High pin-to-logic ratio with user-defined I/O options for pin-intensive applications such as 32-bit microprocessor interface logic
- Enhanced Programmable Interconnect Array (PIA) that provides a fast, fixed delay from any internal source to any destination in the device
- Advanced macrocell to efficiently place logic for optimum speed and density
- Programmable flipflops providing individual Clear, Preset, Clock, and Clock Enable controls
- Independent clocking of all registers from array or global Clock signals
- 3.3-V operation and advanced power management features provided by EPM7032V device

Table 1. MAX 7000 Device Features

Feature	EPM7032	EPM7032V	EPM7064	EPM7096	EPM7128	EPM7160	EPM7192	EPM7256
Available Gates	1,200	1,200	2,500	3,600	5,000	6,400	7,500	10,000
Usable Gates	600	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	32	64	96	128	160	192	256
Max. User I/O	36	36	68	76	100	104	124	164
t_{PD} (ns)	7.5	12	7.5	7.5	10	12	12	20
t_{ASU} (ns)	3	4	3	3	3	4	4	4
t_{CO} (ns)	4.5	7	4.5	4.5	5	6	6	12
f_{CNT} (MHz)	125	90.9	125	125	100	90.9	90.9	62.5

...and More Features

- Software design support featuring Altera's MAX+PLUS II development system on 386- or 486-based PCs, Sun SPARCstations, or HP 9000 Series 700 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers
- EDIF, Verilog, VHDL, and other interfaces providing additional design entry and simulation support with popular CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic

General Description

The MAX 7000 family of high-density, high-performance CMOS EPLDs is based on Altera's second-generation MAX architecture. Fabricated on advanced 0.8-micron CMOS EEPROM and EPROM technologies, the MAX 7000 family provides 600 to 5,000 usable gates, pin-to-pin delays as low as 7.5 ns, and counter speeds up to 125 MHz.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000 EPLDs are also ideal for gate-array prototyping. MAX 7000 EPLDs are available in a wide range of packages, including plastic J-lead chip carrier (PLCC); ceramic pin-grid array (PGA); and the following quad flat pack (QFP) packages: ceramic (CQFP), metal (MQFP), plastic (PQFP), or thin (TQFP). See Table 2.

Table 2. MAX 7000 Pin Count & Package Options *Note (1)*

Pin Count	EPM7032	EPM7032V	EPM7064	EPM7096	EPM7128	EPM7160	EPM7192	EPM7256
44	PLCC, PQFP, TQFP	PLCC, TQFP	–	–	–	–	–	–
68	–	–	PLCC	PLCC	–	–	–	–
84	–	–	PLCC	PLCC	PLCC	PLCC	–	–
100	–	–	PQFP	PQFP	PQFP	PQFP	–	–
160	–	–	–	–	PQFP	PQFP	PQFP, PGA	–
192	–	–	–	–	–	–	–	PGA
208	–	–	–	–	–	–	–	CQFP, MQFP

Note:
(1) Contact Altera for information on available device packages.

MAX 7000 EPLDs use CMOS EEPROM or EPROM cells to implement logic functions within the device. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. EPLDs can be reprogrammed for quick and efficient iterations during design development and debug cycles. Each EEPROM-based device is guaranteed for 100 program and erase cycles. Each EPROM-based device is guaranteed for 25 program and erase cycles.

MAX 7000 EPLDs contain from 32 to 256 macrocells that are combined into groups called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides independent programmable Clock, Clock Enable, Clear, and Preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remainder runs at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay.

The MAX 7000 EPLD family is supported by Altera's MAX+PLUS II development system, a single integrated package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and programming software. MAX+PLUS II provides EDIF, VHDL, Verilog, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. MAX+PLUS II runs on 386- and 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations.

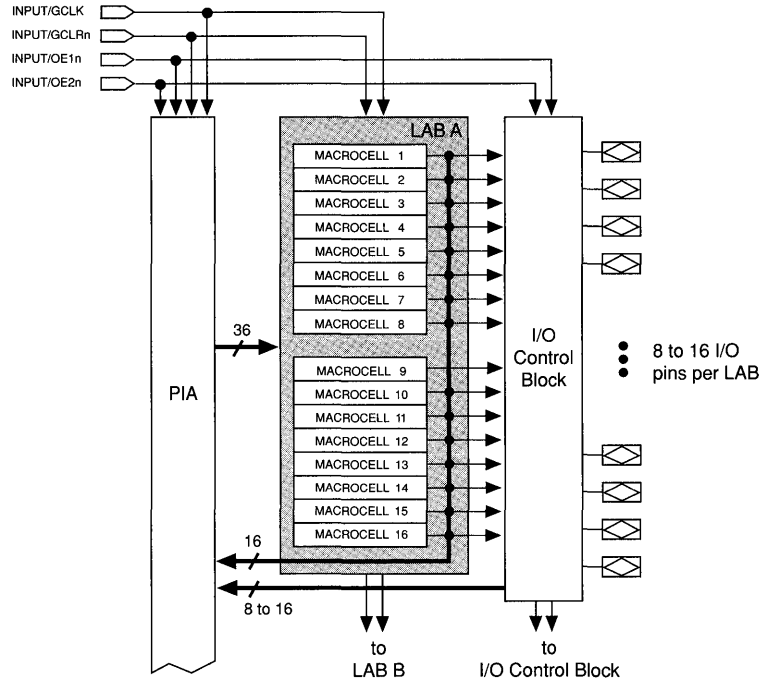
Functional Description

The MAX 7000 architecture includes the following elements:

- Logic Array Blocks
- Macrocells
- Expander product terms (shared and parallel)
- Programmable Interconnect Array
- I/O control blocks

In addition to these basic elements, the MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (Clock, Clear, and two Output Enable signals) for each macrocell and I/O pin. Figure 1 shows a portion of the MAX 7000 architecture.

Figure 1. MAX 7000 Architecture



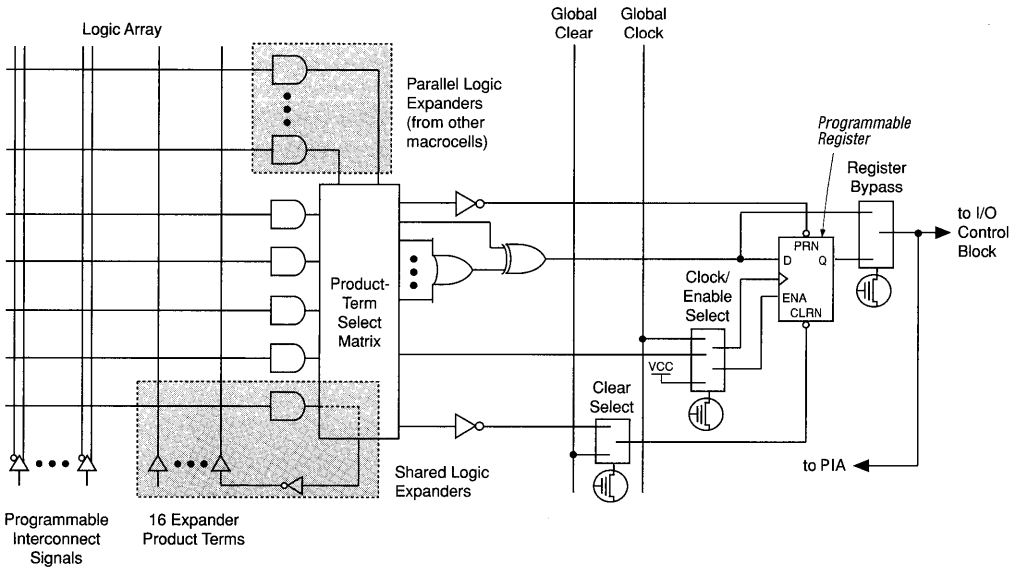
Logic Array Blocks

MAX 7000 architecture is based on the concept of linking small, high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked together via the Programmable Interconnect Array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells. All inputs to each LAB, except the global control signals, are fed by 36 signals from the PIA. LABs consist of macrocell arrays, as shown in Figure 1.

Macrocells

The MAX 7000 macrocell, shown in Figure 2, can be individually configured for both sequential and combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Figure 2. MAX 7000 Macrocell



Combinatorial logic is implemented in the logic array, which contains five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. One product term per macrocell can be inverted and directly fed back into the logic array. This "shareable" product term can be connected to any other product term within the LAB. Based on the logic requirements of the design, MAX+PLUS II automatically optimizes product-term allocation.

In registered functions, each macrocell flipflop can be individually programmed to emulate D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the user specifies the desired flipflop type and MAX+PLUS II selects the most efficient flipflop operation for each registered function to minimize the resources needed by the design.

Three clocking modes are available for each programmable register:

- A register can be clocked by the dedicated global Clock pin (GCLK). In this mode, the flipflop is positive-edge-triggered, and offers the fastest Clock-to-output performance.
- A register can be clocked by an array Clock implemented with a product term. In this mode, the flipflop can be configured for positive- or negative-edge-triggered operation. Array Clocks allow any signal source within the device or gated logic functions to clock the flipflop.
- A register can be clocked by a global Clock pin and enabled by a product term. The register is enabled when the Clock Enable (ENA) input is high. Each flipflop can be activated individually while taking advantage of the fast Clock-to-output delay of the global Clock pin.

Each register also supports asynchronous Preset and Clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product terms that drive the Preset and Clear are active-high, active-low control is provided when the signal is inverted within the logic array. In addition, each register Clear function can be individually driven by the active-low dedicated global Clear pin (GCLRn).

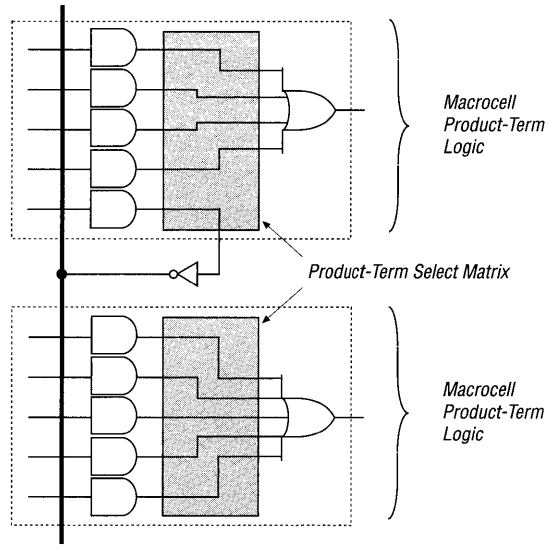
Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using another macrocell to supply the needed logic resources, the MAX 7000 architecture offers both shared and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has up to 16 shareable expanders, which can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders can also be cross-coupled to build additional buried flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



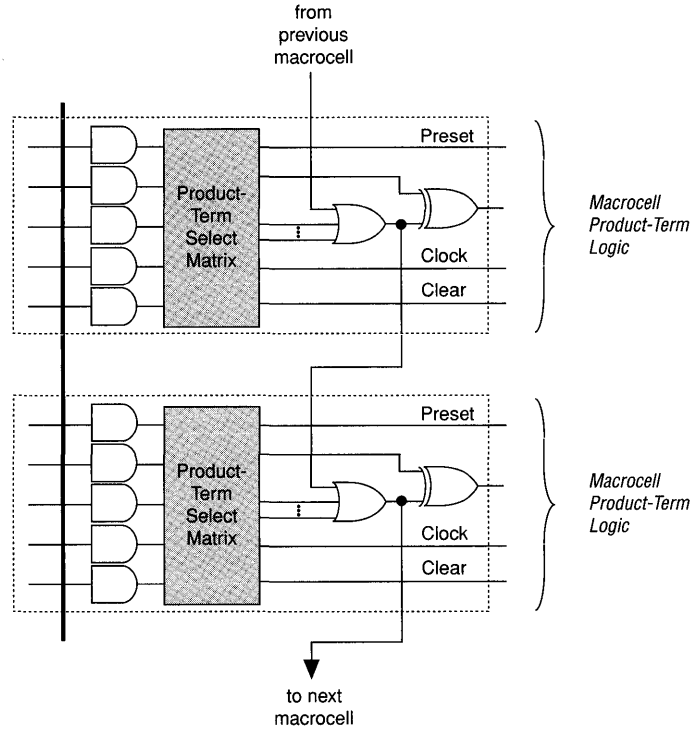
Parallel expanders are unused product terms from macrocells that can be allocated to a neighboring macrocell to implement fast, complex logic functions. With parallel expanders, up to 20 product terms can directly feed the macrocell OR logic—5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically route a set of up to 5 parallel expanders to the necessary macrocells. Up to 3 sets of 5 parallel expanders can be routed to a single macrocell. Each set of 5 expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within the LAB (macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders, and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. Parallel Logic Expanders

These unused product terms in a macrocell can be allocated to a neighboring macrocell.

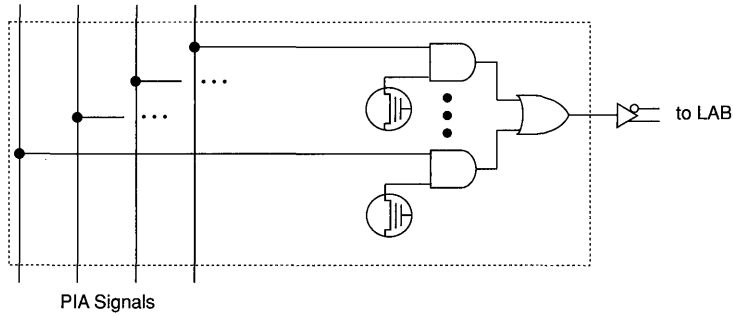


Programmable Interconnect Array

Logic is routed between LABs on the Programmable Interconnect Array (PIA). This global bus is a programmable path that routes any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pin feedbacks, and macrocell feedbacks feed the PIA and route across the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EPROM or EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals, and makes timing performance easy to predict.

Figure 5. PIA Routing

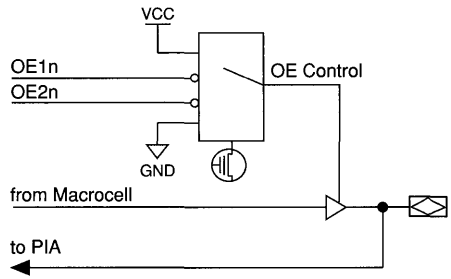


I/O Control Blocks

The I/O control block, shown in Figure 6, allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is controlled by one of two global active-low Output Enable pins (OE1n and OE2n) or directly connected to GND or VCC. When the tri-state buffer control is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to VCC, the output is enabled.

MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Figure 6. I/O Control Block



Programmable Speed/Power Control

The MAX 7000 family offers a power-saver mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by up to 50%, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 EPLD for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal additional timing delay (t_{LPA}) for the t_{LAD}, t_{IC}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

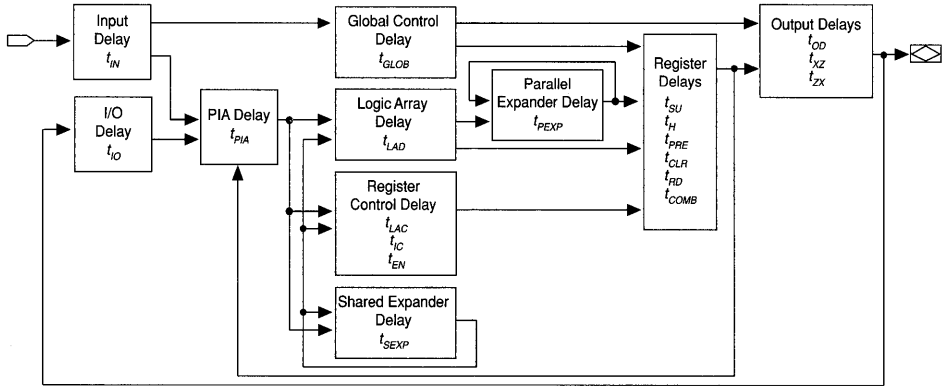
Design Security

All MAX 7000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM or EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

Timing Model

MAX 7000 EPLD timing can be analyzed with MAX+PLUS II software, with a variety of popular industry-standard CAE simulators and timing analyzers, or with the timing model shown in Figure 7. MAX 7000 devices have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 7. Timing Model



Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters can be calculated from the sum of internal parameters and represent pin-to-pin timing delays. Figure 8 shows the internal timing relationship for internal and external delay parameters. See *Application Brief 100 (Understanding EPLD Timing)* in this data book for more information.

Figure 8. Switching Waveforms (Part 1 of 2)

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

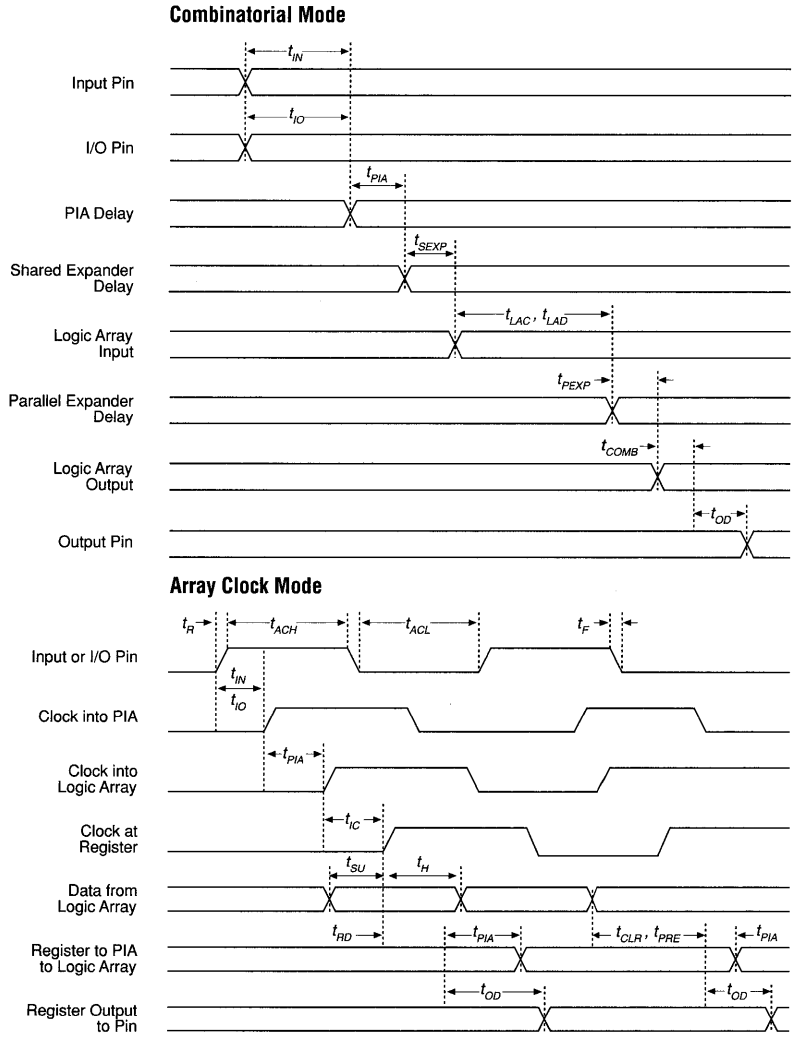
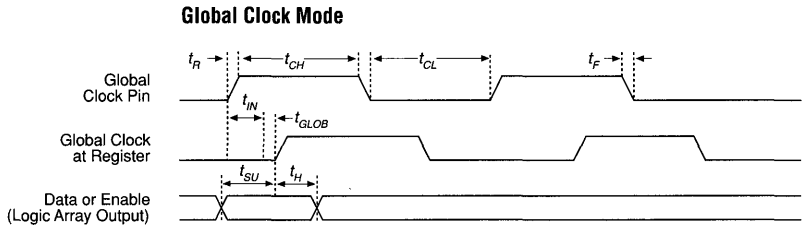


Figure 8. Switching Waveforms (Part 2 of 2)



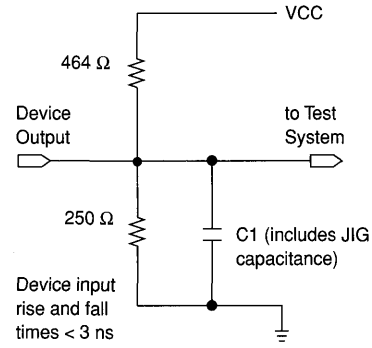
Generic Testing

MAX 7000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EEPROM or EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9.

Test patterns can be used and then erased during early stages of the device production flow. EPROM-based EPLDs in one-time-programmable windowless packages also contain on-board logic circuitry to allow verification of function and AC specifications during this production flow.

Figure 9. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



MAX+PLUS II Development System

MAX 7000 EPLDs are supported by the MAX+PLUS II development system, a completely integrated environment for design entry, compilation, verification, and programming. MAX+PLUS II software is available for 386- and 486-based PCs, as well as Sun SPARCstations and HP 9000 Series 700 workstations. All platforms include more than 300 74-series macrofunctions and the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, conditional logic, and truth table entry methods. MAX+PLUS II also provides highly automated compilation, automatic multi-device partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a comprehensive on-line help system.

In addition, MAX+PLUS II imports and exports industry-standard EDIF 2 0 0 and 2 9 0 netlist files for a convenient interface to industry-standard PC- and workstation-based CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic. MAX+PLUS II also exports Verilog or VHDL netlist files to support simulation with the Cadence Verilog-XL simulator or various VHDL simulators. For further details about MAX+PLUS II and other CAE tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and *CAE Software Support* in this data book.

Device Programming

All MAX 7000 EPLDs can be programmed on 386- or 486-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. See *Altera Programming Hardware* in this data book for more information.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 EPLD with the results of simulation. This feature requires a device adapter with the "PLM-" prefix.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

QFP Carrier & Development Socket

MAX 7000 devices in 100-plus pin QFP packages are shipped in special plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet* in this data book.

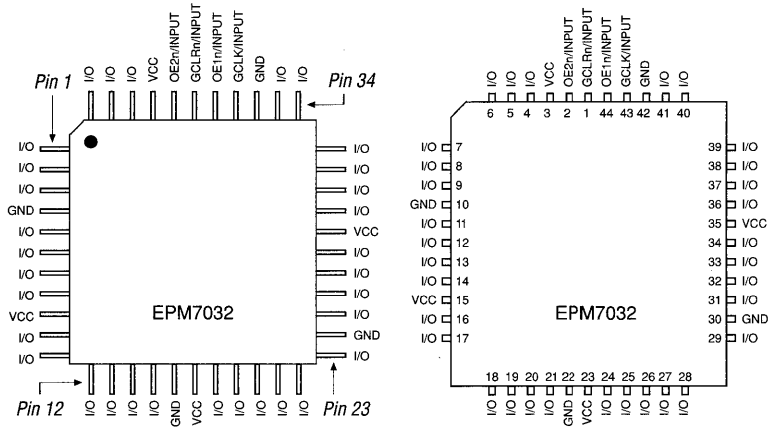
Notes:

Features

- High-performance, erasable CMOS EPLD based on second-generation MAX architecture
  - 600 usable gates
  - Combinatorial speeds with t_{PD} = 7.5 ns
  - Counter frequencies up to 125 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 36 inputs or 32 outputs
- 32 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing 32 product terms in a single macrocell
- Available in 44-pin packages (see Figure 10):
  - EIAJ-standard plastic quad flat pack (PQFP)
  - 1.0-mm thin quad flat pack (TQFP)
  - Plastic J-lead chip carrier (PLCC)
- Low-cost "T" version available (See "EPM7032-15T EPLD" in this data sheet).

Figure 10. EPM7032 Package Pin-Out Diagrams

Package outlines not drawn to scale.



44-Pin QFP

44-Pin J-Lead

General Description

The Altera EPM7032 is a high-performance, high-density CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 11. Fabricated on a 0.8-micron EEPROM technology, the EPM7032 provides in-system speeds of 125 MHz and propagation delays of 7.5 ns. The EPM7032 architecture supports 100% TTL emulation and allows the

integration of SSI, MSI, and custom logic functions. It can replace multiple 20- and 24-pin PLDs. The EPM7032 can accommodate designs with up to 36 inputs or 32 outputs.

Figure 11. EPM7032 Block Diagram

Pin numbers without parentheses are for the PLCC packages. Pin numbers in parentheses are for QFP packages.

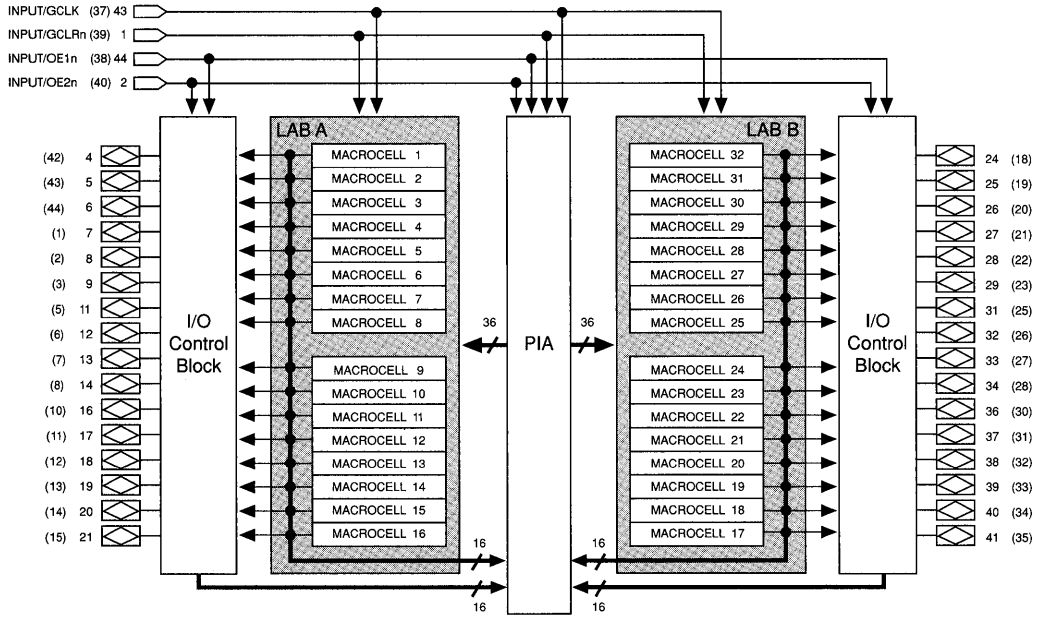


Figure 12 shows the output drive characteristics of EPM7032 I/O pins.

Figure 12. Typical EPM7032 Output Drive Characteristics

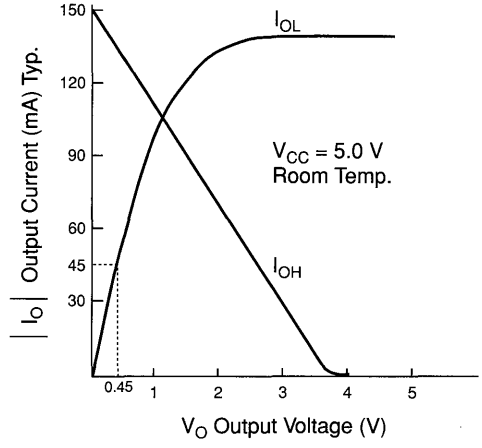


Figure 13 shows typical supply current versus frequency for the EPM7032.

Figure 13. EPM7032 I_{CC} vs. Frequency

I_{CC} for the EPM7032-12 and EPM7032-15 is calculated with the following equation:

$$I_{CC} = (0.9 \times MC_{TON}) + (0.55 \times MC_{TOFF}) + [(0.018 \times MC) \times f_{MAX}]$$

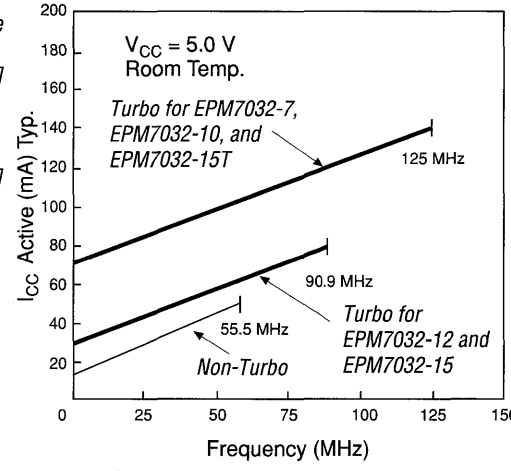
I_{CC} for the EPM7032-7, EPM7032-10, and EPM7032-15T is calculated with the following equation:

$$I_{CC} = (2.2 \times MC_{TON}) + (0.55 \times MC_{TOFF}) + [(0.018 \times MC) \times f_{MAX}]$$

The parameters for this equation are:

- MC_{TON} = *number of macrocells used with Turbo Bit on*
- MC_{TOFF} = *number of macrocells used with Turbo Bit off*
- MC = *total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)*
- f_{MAX} = *highest Clock frequency to the device*

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB and no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC				0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND		–40		40	µA
I_{CC1}	V_{CC} supply current	V_I = GND, No load	-12, -15		24	35	mA
	(low-power mode, standby)	*Note (4)*	-7, -10, -15T		35	70	mA
I_{CC2}	V_{CC} supply current	V_I = GND, No load,	-12, -15		30	40	mA
	(low-power mode, active)	f = 1.0 MHz, *Note (4)*	-7, -10, -15T		45	100	mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7032-7		EPM7032-10		EPM7032-12		EPM7032-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10		12		15	ns
t_{PD2}	I/O input to non-registered output			7.5		10		12		15	ns
t_{SU}	Global clock setup time		6		8		10		11		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.5		5		6		8	ns
t_{CH}	Global clock high time		3		4		4		5		ns
t_{CL}	Global clock low time		3		4		4		5		ns
t_{ASU}	Array clock setup time		3		3		4		4		ns
t_{AH}	Array clock hold time		2		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.5		10		12		15	ns
t_{ACH}	Array clock high time		3		4		5		6		ns
t_{ACL}	Array clock low time		3		4		5		6		ns
t_{CNT}	Minimum global clock period			8		10		11		13	ns
f_{CNT}	Max. int. global clock freq.	*Note (4)*	125.0		100		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			8		10		11		13	ns
f_{ACNT}	Max. int. array clock freq.	*Note (4)*	125.0		100		90.9		76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	166.7		125		125		100		MHz

Internal Timing Parameters			EPM7032-7		EPM7032-10		EPM7032-12		EPM7032-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.5		1		2		2	ns
t_{IO}	I/O input pad and buffer delay			0.5		1		2		2	ns
t_{SEXP}	Shared expander delay			4		5		7		8	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		1		1	ns
t_{LAD}	Logic array delay			3		5		5		6	ns
t_{LAC}	Logic control array delay			3		5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		2		3		4	ns
t_{ZX}	Output buffer enable delay			4		5		6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		5		6		6	ns
t_{SU}	Register setup time		3		3		4		4		ns
t_{H}	Register hold time		2		3		4		4		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			3		5		5		6	ns
t_{EN}	Register enable time			3		5		5		6	ns
t_{GLOB}	Global control delay			1		1		0		1	ns
t_{PRE}	Register preset time			2		3		3		4	ns
t_{CLR}	Register clear time			2		3		3		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		1		1		2	ns
t_{LPA}	Low power adder	*Note (7)*		10		11		12		13	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7032-7, EPM7032-10, EPM7032-12, EPM7032-15
Industrial Temp.	(–40° C to 85° C)	EPM7032-12, EPM7032-15
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7032 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7032-1	EPM7032-10
EPM7032-2	EPM7032-12
EPM7032-3	EPM7032-15

Features

- ❑ Low-cost version of the EPM7032. See "EPM7032" in this data sheet for more information.
- ❑ High performance 32-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15ns.
  - Counter frequency as high as 76.9 MHz
- ❑ Pin, function, and programming-file compatible with the EPM7032.

AC Operating Conditions (Part 1 of 2)

External Timing Parameters *Note (1)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15	ns
t_{PD2}	I/O input to non-registered output			15	ns
t_{SU}	Global clock setup time		11		ns
t_{H}	Global clock hold time		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8	ns
t_{CH}	Global clock high time		6		ns
t_{CL}	Global clock low time		6		ns
t_{ASU}	Array clock setup time		4		ns
t_{AH}	Array clock hold time		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15	ns
t_{ACH}	Array clock high time		6.5		ns
t_{ACL}	Array clock low time		6.5		ns
t_{CNT}	Minimum global clock period			13	ns
f_{CNT}	Max. internal global clock frequency	*Note (3)*	76.9		MHz
t_{ACNT}	Minimum array clock period			13	ns
f_{ACNT}	Max. internal array clock frequency	*Note (3)*	76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	83.3		MHz

AC Operating Conditions (Part 2 of 2)

Internal Timing Parameters Note (1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2	ns
t_{IO}	I/O input pad and buffer delay			2	ns
t_{SEXP}	Shared expander delay			10	ns
t_{PEXP}	Parallel expander delay			1	ns
t_{LAD}	Logic array delay			6	ns
t_{LAC}	Logic control array delay			6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4	ns
t_{ZX}	Output buffer enable delay			6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6	ns
t_{SU}	Register setup time		4		ns
t_{H}	Register hold time		4		ns
t_{RD}	Register delay			1	ns
t_{COMB}	Combinatorial delay			1	ns
t_{IC}	Array clock delay			6	ns
t_{EN}	Register enable time			6	ns
t_{GLOB}	Global control delay			1	ns
t_{PRE}	Register preset time			4	ns
t_{CLR}	Register clear time			4	ns
t_{PIA}	Prog. Interconnect Array delay			2	ns
t_{LPA}	Low-power adder	*Note (5)*		15	ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5.0\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
(2) Typical values are for $T_A = 25°\ C$ and $V_{CC} = 5.0\ V$.
(3) Measured with a device programmed as a 16-bit counter in each LAB. I_{CC} is measured at 0° C.
(4) The f_{MAX} values represent the highest frequency for pipelined data.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, t_{IC}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7032-15T

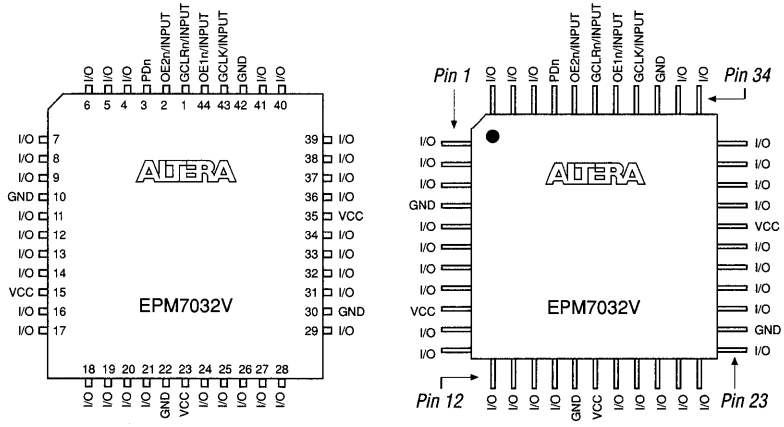
Features

For detailed information, refer to "EPM*7032V*" in the *3.3-Volt Devices Data Sheet* in this data book.

- 3.3-V version of the popular EPM7032 EPLD
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 90.9 MHz
- Innovative power-saving features
  - 30% to 50% power savings over 5-V operation
  - Power-down mode controlled by a power-down pin to allow zero power consumption during periods of inactivity
  - Programmable power-saver mode for up to 50% power reduction during active operation, configurable for each macrocell
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture allowing up to 36 inputs or 32 outputs
- 32 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Independent clocking of all registers from array or global Clock signals
- Available in 44-pin plastic reprogrammable packages (see Figure 14):
  - 1.0-mm thin quad flat pack (TQFP)
  - J-lead chip carrier (PLCC)

Figure 14. EPM7032V Package Pin-Out Diagrams

Package outlines not drawn to scale.



44-Pin J-Lead

44-Pin QFP

Notes:

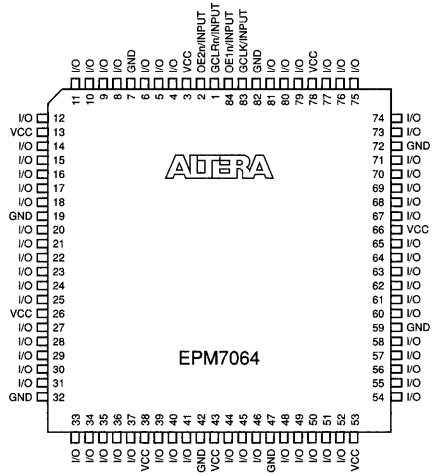
Features

Preliminary Information

- High-performance, erasable CMOS EPLD based on second-generation MAX architecture
  - 1,250 usable gates
  - Combinatorial speeds with t_{PD} = 7.5 ns
  - Counter frequencies up to 125 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 68 inputs or 64 outputs
- 64 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing 32 product terms in a single macrocell
- Available in the following packages (see Figure 15):
  - 84-pin plastic J-lead chip carrier (PLCC)
  - 100-pin EIAJ-standard plastic quad flat pack (PQFP)

Figure 15. EPM7064 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 3 and 4 in this data sheet for pin-out information.



General Description

The Altera EPM7064 is a high-performance, high-density CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 16. Fabricated on a 0.8-micron EEPROM technology, the EPM7064 provides counter speeds of 125 MHz and propagation delays of 7.5 ns. The EPM7064 architecture supports 100% TTL emulation and allows the integration of

SSI, MSI, and custom logic functions. It can replace multiple 20- and 24-pin PLDs. The EPM7064 can accommodate designs with up to 68 inputs or 64 outputs.

Figure 16. EPM7064 Block Diagram

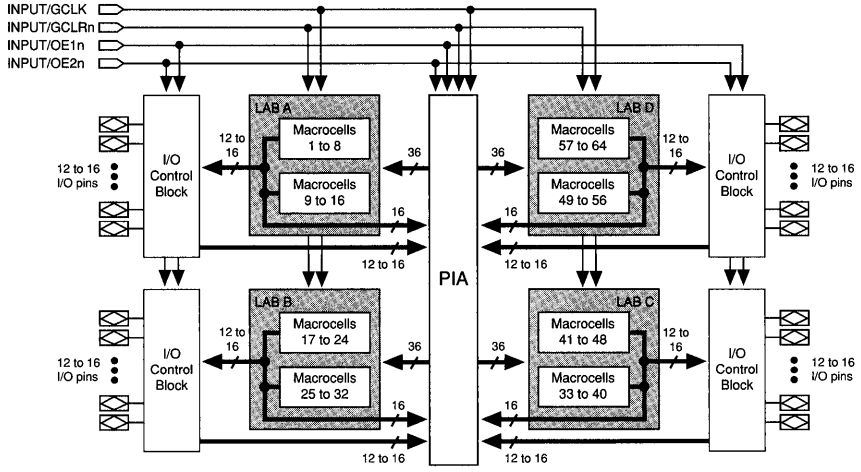
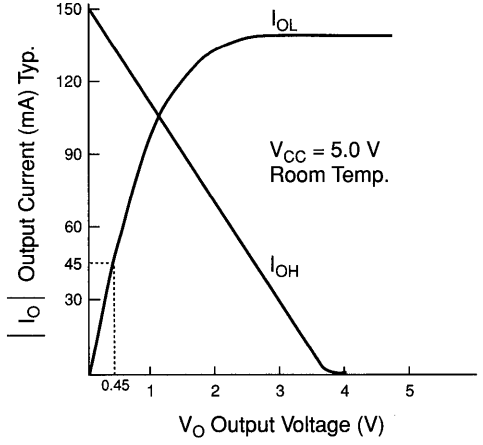


Figure 17 shows the output drive characteristics of EPM7064 I/O pins.

Figure 17. Typical EPM7064 Output Drive Characteristics



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		40		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		45		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10		12		15	ns
t_{PD2}	I/O input to non-registered output			7.5		10		12		15	ns
t_{SU}	Global clock setup time		6		8		10		11		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.5		5		6		8	ns
t_{CH}	Global clock high time		3		4		4		5		ns
t_{CL}	Global clock low time		3		4		4		5		ns
t_{ASU}	Array clock setup time		3		3		4		4		ns
t_{AH}	Array clock hold time		2		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.5		10		12		15	ns
t_{ACH}	Array clock high time		3		4		5		6		ns
t_{ACL}	Array clock low time		3		4		5		6		ns
t_{CNT}	Minimum global clock period			8		10		11		13	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	125.0		100		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			8		10		11		13	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	125.0		100		90.9		76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	166.7		125		125		100		MHz

Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.5		1		2		2	ns
t_{IO}	I/O input pad and buffer delay			0.5		1		2		2	ns
t_{SEXP}	Shared expander delay			4		5		7		8	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		1		1	ns
t_{LAD}	Logic array delay			3		5		5		6	ns
t_{LAC}	Logic control array delay			3		5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		2		3		4	ns
t_{ZX}	Output buffer enable delay			4		5		6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		5		6		6	ns
t_{SU}	Register setup time		3		3		4		4		ns
t_{H}	Register hold time		2		3		4		4		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			3		5		5		6	ns
t_{EN}	Register enable time			3		5		5		6	ns
t_{GLOB}	Global control delay			1		1		0		1	ns
t_{PRE}	Register preset time			2		3		3		4	ns
t_{CLR}	Register clear time			2		3		3		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		1		1		2	ns
t_{LPA}	Low power adder	*Note (7)*		10		11		12		13	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Device Qualification		Availability
Commercial Temp.	(0° C to 70° C)	EPM7064-10, EPM7064-12, EPM7064-15
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7064 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7064-1	EPM7064-10
EPM7064-2	EPM7064-12
EPM7064-3	EPM7064-15

Pin-Out Information

Tables 3 and 4 provide pin-out information for the EPM7064 packages.

Table 3. EPM7064 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP
GCLK	83	89
GCLRn	1	91
OE1n	84	90
OE2n	2	92
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93
No Connect (N.C.)	–	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80

Table 4. EPM7064 I/O Pin-Outs

MC	LAB	84-Pin J-Lead	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP
1	A	22	16	17	B	41	39
2	A	21	15	18	B	40	38
3	A	20	14	19	B	39	37
4	A	18	12	20	B	37	35
5	A	17	11	21	B	36	34
6	A	16	10	22	B	35	33
7	A	15	8	23	B	34	32
8	A	14	6	24	B	33	31
9	A	12	4	25	B	31	27
10	A	11	3	26	B	30	25
11	A	10	100	27	B	29	23
12	A	9	99	28	B	28	22
13	A	8	98	29	B	27	21
14	A	6	96	30	B	25	19
15	A	5	95	31	B	24	18
16	A	4	94	32	B	23	17
33	C	44	42	49	D	63	65
34	C	45	43	50	D	64	66
35	C	46	44	51	D	65	67
36	C	48	46	52	D	67	69
37	C	49	47	53	D	68	70
38	C	50	48	54	D	69	71
39	C	51	49	55	D	70	73
40	C	52	50	56	D	71	75
41	C	54	54	57	D	73	77
42	C	55	56	58	D	74	78
43	C	56	58	59	D	75	81
44	C	57	59	60	D	76	82
45	C	58	60	61	D	77	83
46	C	60	62	62	D	79	85
47	C	61	63	63	D	80	86
48	C	62	64	64	D	81	87

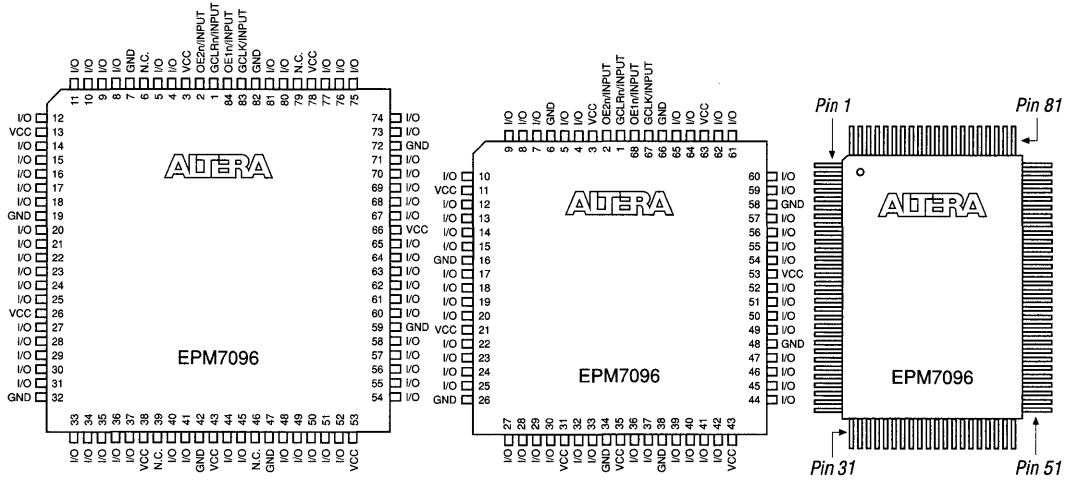
Features

Preliminary Information

- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 1,800 usable gates
  - Combinatorial speeds with t_{PD} = 7.5 ns
  - Counter frequencies up to 125 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture providing up to 76 inputs or 72 outputs
- 96 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in the following packages (see Figure 18):
  - 68- and 84-pin plastic J-lead chip carrier (PLCC)
  - 100-pin EIAJ-standard plastic quad flat pack (PQFP)

Figure 18. EPM7096 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 5 and 6 in this data sheet for pin-out information.



84-Pin J-Lead 68-Pin J-Lead 100-Pin QFP

General Description

The Altera EPM7096 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 19. Fabricated on a 0.8-micron EEPROM technology, the EPM7096 provides 1,800 usable gates, counter speeds of 125 MHz, and propagation delays of 7.5 ns. The EPM7096 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and

22V10s to MACH devices and FPGAs. The EPM7096 can accommodate designs with up to 76 inputs or 72 outputs.

Figure 19. EPM7096 Block Diagram

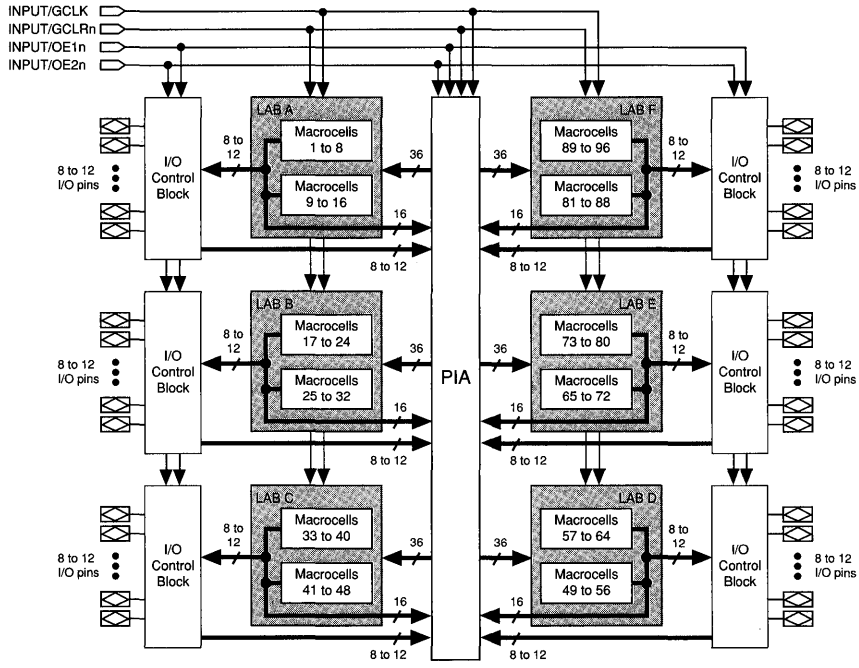


Figure 20 shows the output drive characteristics of EPM7096 I/O pins.

Figure 20. EPM7096 Output Drive Characteristics

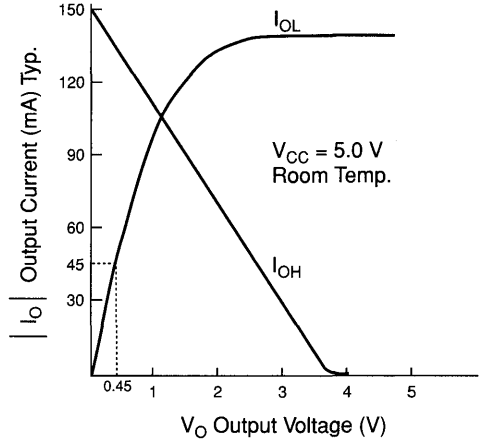


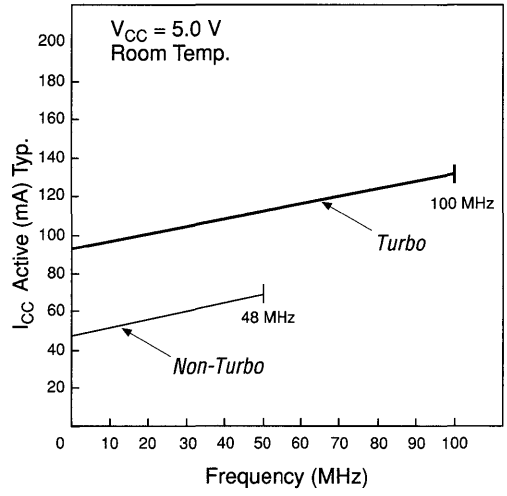
Figure 21 shows typical supply current versus frequency for the EPM7096.

Figure 21. EPM7096 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.91 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0053 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		50		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		55		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7096-7		EPM7096-10		EPM7096-12		EPM7096-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10		12		15	ns
t_{PD2}	I/O input to non-registered output			7.5		10		12		15	ns
t_{SU}	Global clock setup time		6		8		10		11		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.5		5		6		8	ns
t_{CH}	Global clock high time		3		4		4		5		ns
t_{CL}	Global clock low time		3		4		4		5		ns
t_{ASU}	Array clock setup time		3		3		4		4		ns
t_{AH}	Array clock hold time		2		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.5		10		12		15	ns
t_{ACH}	Array clock high time		3		4		5		6		ns
t_{ACL}	Array clock low time		3		4		5		6		ns
t_{CNT}	Minimum global clock period			8		10		11		13	ns
f_{CNT}	Max. int. global clock frequency	*Note (4)*	125.0		100		90.9		76.9		MHz
t_{ACNT}	Minimum array clock period			8		10		11		13	ns
f_{ACNT}	Max. int. array clock frequency	*Note (4)*	125.0		100		90.9		76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	166.7		125		125		100		MHz

Internal Timing Parameters			EPM7096-7		EPM7096-10		EPM7096-12		EPM7096-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.5		1		2		2	ns
t_{IO}	I/O input pad and buffer delay			0.5		1		2		2	ns
t_{SEXP}	Shared expander delay			4		5		7		8	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		1		1	ns
t_{LAD}	Logic array delay			3		5		5		6	ns
t_{LAC}	Logic control array delay			3		5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2		2		3		4	ns
t_{ZX}	Output buffer enable delay			4		5		6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		5		6		6	ns
t_{SU}	Register setup time		3		3		4		4		ns
t_{H}	Register hold time		2		3		4		4		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			3		5		5		6	ns
t_{EN}	Register enable time			3		5		5		6	ns
t_{GLOB}	Global control delay			1		1		0		1	ns
t_{PRE}	Register preset time			2		3		3		4	ns
t_{CLR}	Register clear time			2		3		3		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		1		1		2	ns
t_{LPA}	Low power adder	*Note (7)*		10		11		12		13	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7096-10, EPM7096-12, EPM7096-15
Industrial Temp.	(–40° C to 85° C)	EPM7096-15
Military Temp.	(–55° C to 125° C)	Consult factory

Product Replacement Guide

The following table shows which EEPROM EPM7096 devices should be used as replacements for the earlier EPROM EPM7096 devices.

EPROM Device	EEPROM Device
EPM7096	EPM7096-15
EPM7096-2	EPM7096-15
EPM7096-3	EPM7096-15

Pin-Out Information

Tables 5 and 6 provide pin-out information for the EPM7096 packages.

Table 5. EPM7096 Dedicated Pin-Outs

Dedicated Pin	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
`GCLK`	67	83	89
`GCLRn`	1	1	91
`OE1n`	68	84	90
`OE2n`	2	2	92
`GND`	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
`VCC`	3, 11, 21, 31, 35, 43, 53, 63	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93
No Connect (N.C.)	–	6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96

Table 6. EPM7096 I/O Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
1	A	13	16	8	17	B	23	28	23
2	A	–	–	–	18	B	–	–	–
3	A	–	15	7	19	B	22	27	22
4	A	12	14	6	20	B	–	–	21
5	A	–	–	4	21	B	20	25	19
6	A	10	12	3	22	B	–	24	18
7	A	–	–	–	23	B	–	–	–
8	A	9	11	2	24	B	19	23	17
9	A	8	10	1	25	B	18	22	16
10	A	–	–	–	26	B	–	–	–
11	A	–	9	100	27	B	17	21	15
12	A	7	8	99	28	B	–	20	14
13	A	–	–	98	29	B	15	18	12
14	A	5	5	95	30	B	–	–	11
15	A	–	–	–	31	B	–	–	–
16	A	4	4	94	32	B	14	17	10
33	C	33	41	39	49	D	36	44	42
34	C	–	–	–	50	D	–	–	–
35	C	32	40	38	51	D	37	45	43
36	C	–	–	35	52	D	–	–	46
37	C	30	37	34	53	D	39	48	47
38	C	–	36	33	54	D	–	49	48
39	C	–	–	–	55	D	–	–	–
40	C	29	35	32	56	D	40	50	49
41	C	28	34	31	57	D	41	51	50
42	C	–	–	–	58	D	–	–	–
43	C	27	33	30	59	D	42	52	51
44	C	–	–	29	60	D	–	–	52
45	C	25	31	27	61	D	44	54	54
46	C	–	30	26	62	D	–	55	55
47	C	–	–	–	63	D	–	–	–
48	C	24	29	25	64	D	45	56	56

Table 6. EPM7096 I/O Pin-Outs (Part 2 of 2)

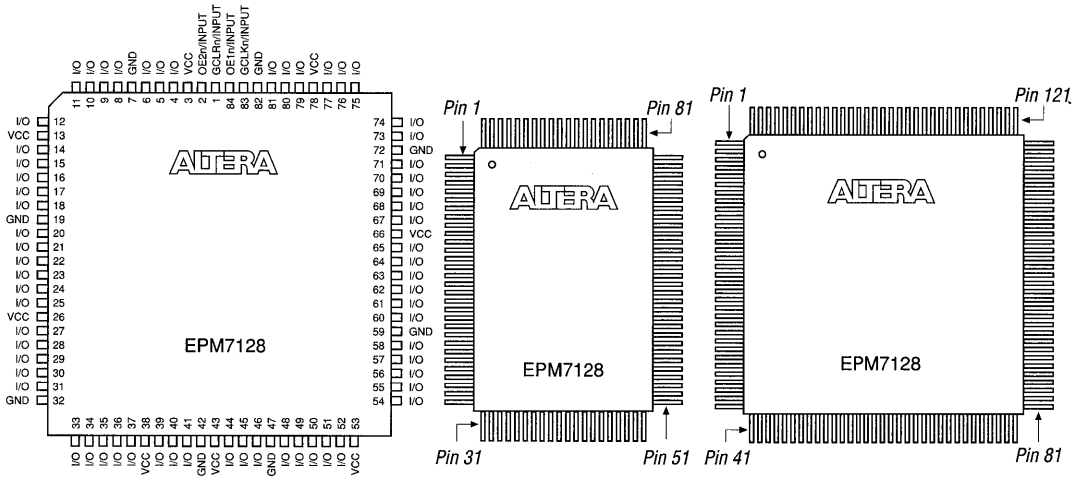
MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
65	E	46	57	58	81	F	56	69	73
66	E	–	–	–	82	F	–	–	–
67	E	47	58	59	83	F	–	70	74
68	E	–	–	60	84	F	57	71	75
69	E	49	60	62	85	F	–	–	77
70	E	–	61	63	86	F	59	73	78
71	E	–	–	–	87	F	–	–	–
72	E	50	62	64	88	F	60	74	79
73	E	51	63	65	89	F	61	75	80
74	E	–	–	–	90	F	–	–	–
75	E	52	64	66	91	F	–	76	81
76	E	–	65	67	92	F	62	77	82
77	E	54	67	69	93	F	–	–	83
78	E	–	–	70	94	F	64	80	86
79	E	–	–	–	95	F	–	–	–
80	E	55	68	71	96	F	65	81	87

Features

- High-density CMOS EPLD based on second-generation MAX architecture
  - 2,500 usable gates
  - Combinatorial speeds with t_{PD} = 10 ns
  - Counter frequencies up to 100 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 100 inputs or 96 outputs
- 128 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in the following packages (see Figure 22):
  - 84-pin plastic J-lead chip carrier (PLCC)
  - 100- and 160-pin plastic quad flat pack (PQFP)

Figure 22. EPM7128 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 7 and 8 in this data sheet for pin-out information.



General Description

The Altera EPM7128 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 23. Fabricated on a 0.8-micron EEPROM technology, the EPM7128 provides 2,500 usable gates, counter speeds of 100 MHz, and propagation delays of 10 ns. The EPM7128 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 128 macrocells,

the EPM7128 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. With its high performance and density, the EPM7128 provides FPGA density with PAL performance. The high density and high I/O pin count make the EPM7128 appropriate for prototyping gate arrays. The EPM7128 can also accommodate both logic- and I/O-intensive designs.

Figure 23. EPM7128 Block Diagram

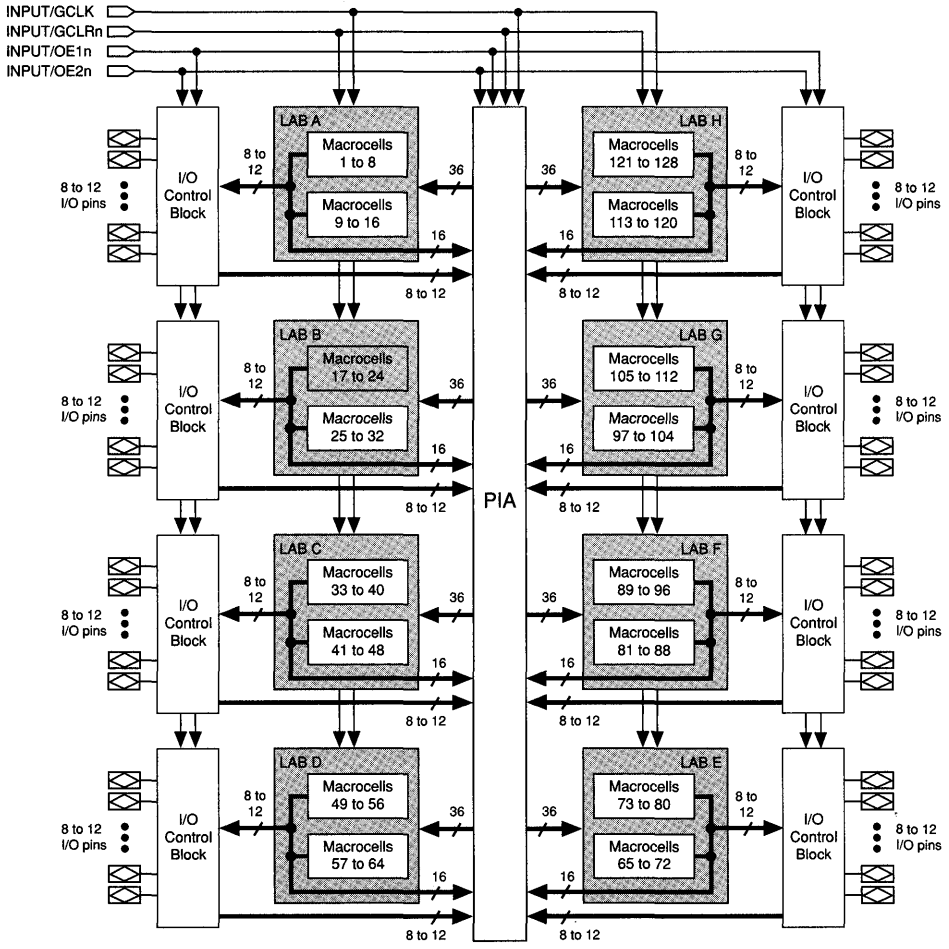


Figure 24 shows the output drive characteristics of EPM7128 I/O pins.

Figure 24. EPM7128 Output Drive Characteristics

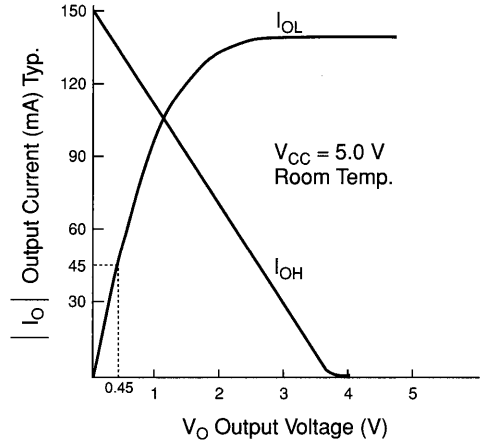


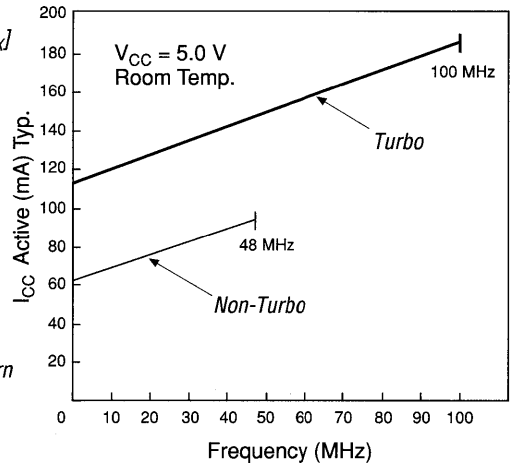
Figure 25 shows typical supply current versus frequency for the EPM7128.

Figure 25. EPM7128 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.91 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0053 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Rating See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	-40	85	° C
T_C	Case temperature	For military use	-55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		90		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		100		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7128-10		EPM7128-12		EPM7128-15		EPM7128-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-reg. output	C1 = 35 pF		10		12		15		20	ns
t_{PD2}	I/O input to non-reg. output			10		12		15		20	ns
t_{SU}	Global clock setup time		8		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		6		8		12	ns
t_{CH}	Global clock high time		4		4		5		6		ns
t_{CL}	Global clock low time		4		4		5		6		ns
t_{ASU}	Array clock setup time		3		4		4		5		ns
t_{AH}	Array clock hold time		3		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12		15		20	ns
t_{ACH}	Array clock high time		4		5		6		8		ns
t_{ACL}	Array clock low time		4		5		6		8		ns
t_{CNT}	Minimum global clock period			10		11		13		16	ns
f_{CNT}	Max. int. global clock freq.	*Note (4)*	100		90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			10		11		13		16	ns
f_{ACNT}	Max. int. array clock freq.	*Note (4)*	100		90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		125		100		83.3		MHz

Internal Timing Parameters			EPM7128-10		EPM7128-12		EPM7128-15		EPM7128-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad & buffer delay			1		2		2		3	ns
t_{IO}	I/O input pad & buffer delay			1		2		2		3	ns
t_{SEXP}	Shared expander delay			5		7		8		9	ns
t_{PEXP}	Parallel expander delay			0.8		1		1		2	ns
t_{LAD}	Logic array delay			5		5		6		8	ns
t_{LAC}	Logic control array delay			5		5		6		8	ns
t_{OD}	Output buffer & pad delay	C1 = 35 pF		2		3		4		5	ns
t_{ZX}	Output buffer enable delay			5		6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		6		6		9	ns
t_{SU}	Register setup time		3		4		4		4		ns
t_{H}	Register hold time		3		4		4		5		ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{IC}	Array clock delay			5		5		6		8	ns
t_{EN}	Register enable time			5		5		6		8	ns
t_{GLOB}	Global control delay			1		0		1		3	ns
t_{PRE}	Register preset time			3		3		4		4	ns
t_{CLR}	Register clear time			3		3		4		4	ns
t_{PIA}	Prog. Interconn. Array delay			1		1		2		3	ns
t_{LPA}	Low power adder	*Note (7)*		11		12		13		15	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7128-10, EPM7128-12, EPM7128-15, EPM7128-20
Industrial Temp.	(–40° C to 85° C)	EPM7128-20
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7128 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7128-1	EPM7128-10
EPM7128-2	EPM7128-12
EPM7128-3	EPM7128-15
EPM7128-4	EPM7128-20

Pin-Out Information

Tables 7 and 8 provide pin-out information for the EPM7128 packages.

Table 7. EPM7128 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
GCLK	83	89	139
GCLRn	1	91	141
OE1n	84	90	140
OE2n	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	8, 26, 55, 61, 79, 104, 133, 143
No Connect (N.C.)	–	–	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157

Table 8. EPM7128 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	–	4	160	17	B	22	16	21
2	A	–	–	–	18	B	–	–	–
3	A	12	3	159	19	B	21	15	20
4	A	–	–	158	20	B	–	–	19
5	A	11	2	153	21	B	20	14	18
6	A	10	1	152	22	B	–	12	16
7	A	–	–	–	23	B	–	–	–
8	A	9	100	151	24	B	18	11	15
9	A	–	99	150	25	B	17	10	14
10	A	–	–	–	26	B	–	–	–
11	A	8	98	149	27	B	16	9	13
12	A	–	–	147	28	B	–	–	12
13	A	6	96	146	29	B	15	8	11
14	A	5	95	145	30	B	–	7	10
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	14	6	9
33	C	–	27	41	49	D	41	39	59
34	C	–	–	–	50	D	–	–	–
35	C	31	26	33	51	D	40	38	58
36	C	–	–	32	52	D	–	–	57
37	C	30	25	31	53	D	39	37	56
38	C	29	24	30	54	D	–	35	54
39	C	–	–	–	55	D	–	–	–
40	C	28	23	29	56	D	37	34	53
41	C	–	22	28	57	D	36	33	52
42	C	–	–	–	58	D	–	–	–
43	C	27	21	27	59	D	35	32	51
44	C	–	–	25	60	D	–	–	50
45	C	25	19	24	61	D	34	31	49
46	C	24	18	23	62	D	–	30	48
47	C	–	–	–	63	D	–	–	–
48	C	23	17	22	64	D	33	29	43

Table 8. EPM7128 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	44	42	62	81	F	–	54	80
66	E	–	–	–	82	F	–	–	–
67	E	45	43	63	83	F	54	55	88
68	E	–	–	64	84	F	–	–	89
69	E	46	44	65	85	F	55	56	90
70	E	–	46	67	86	F	56	57	91
71	E	–	–	–	87	F	–	–	–
72	E	48	47	68	88	F	57	58	92
73	E	49	48	69	89	F	–	59	93
74	E	–	–	–	90	F	–	–	–
75	E	50	49	70	91	F	58	60	94
76	E	–	–	71	92	F	–	–	96
77	E	51	50	72	93	F	60	62	97
78	E	–	51	73	94	F	61	63	98
79	E	–	–	–	95	F	–	–	–
80	E	52	52	78	96	F	62	64	99
97	G	63	65	100	113	H	–	77	121
98	G	–	–	–	114	H	–	–	–
99	G	64	66	101	115	H	73	78	122
100	G	–	–	102	116	H	–	–	123
101	G	65	67	103	117	H	74	79	128
102	G	–	69	105	118	H	75	80	129
103	G	–	–	–	119	H	–	–	–
104	G	67	70	106	120	H	76	81	130
105	G	68	71	107	121	H	–	82	131
106	G	–	–	–	122	H	–	–	–
107	G	69	72	108	123	H	77	83	132
108	G	–	–	109	124	H	–	–	134
109	G	70	73	110	125	H	79	85	135
110	G	–	74	111	126	H	80	86	136
111	G	–	–	–	127	H	–	–	–
112	G	71	75	112	128	H	81	87	137

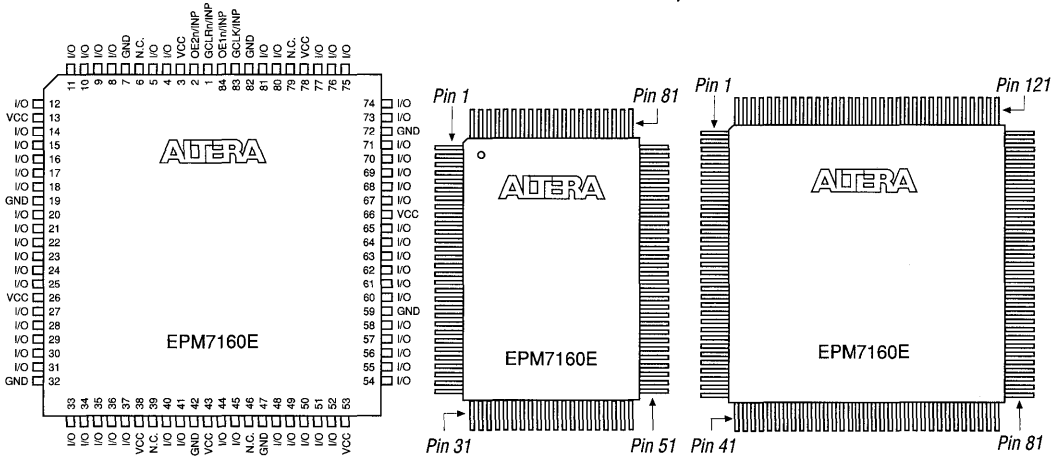
Notes:

Features

- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 3,200 usable gates
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 104 inputs or 100 outputs
- 160 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in plastic packages (see Figure 26):
  - 84-pin plastic J-lead chip carrier (PLCC)
  - 100- and 160-pin plastic quad flat pack (PQFP)

Figure 26. EPM7160 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 9 and 10 in this data sheet for pin-out information.



84-Pin J-Lead 100-Pin QFP 160-Pin QFP

General Description

The Altera EPM7160 is a high-density, high-performance CMOS device based on Altera's second-generation MAX architecture. See Figure 27. Fabricated on a 0.8-micron EEPROM technology, the EPM7160 provides 3,200 usable gates, counter speeds of 90.9 MHz, and propagation delays of 12 ns. The EPM7160 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 160 macrocells, the EPM7160 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. With its high performance and density, the EPM7160 provides FPGA

density with PAL performance. The high density and high I/O pin count also make the EPM7160 appropriate for prototyping gate arrays. The EPM7160 can accommodate both logic- and I/O-intensive designs.

Figure 27. EPM7160 Block Diagram

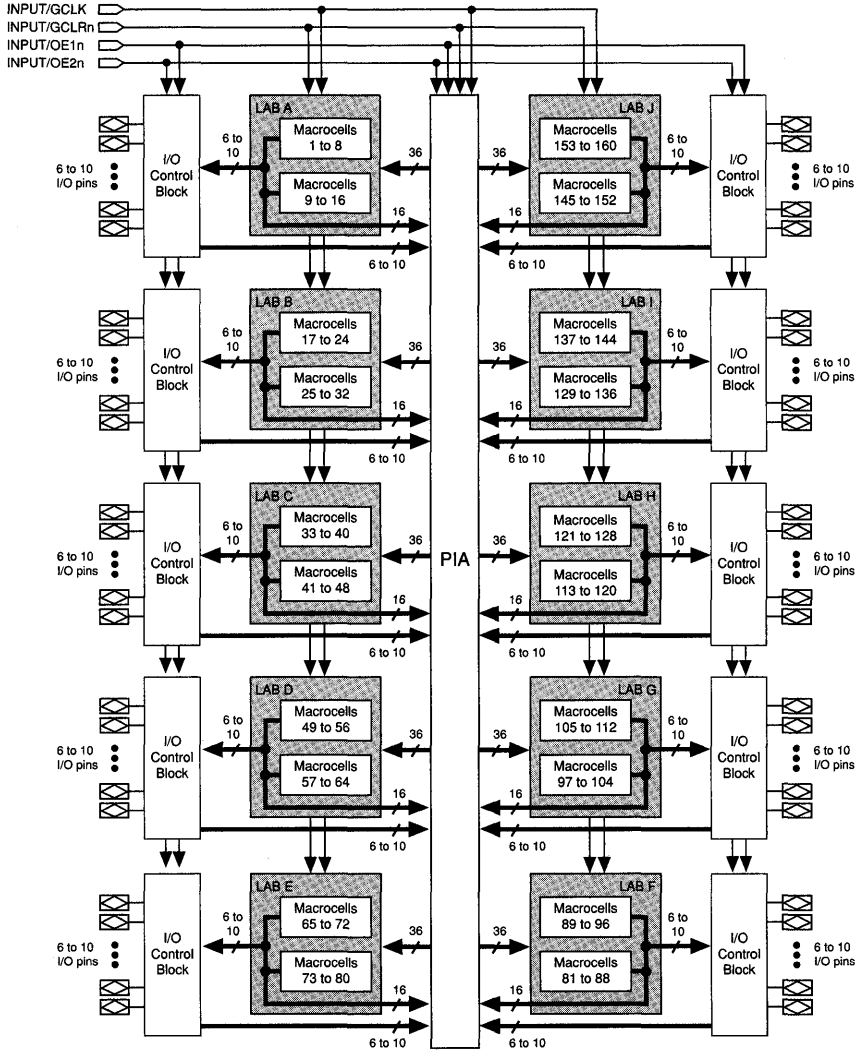


Figure 28 shows the output drive characteristics of EPM7160 I/O pins.

Figure 28. EPM7160 Output Drive Characteristics

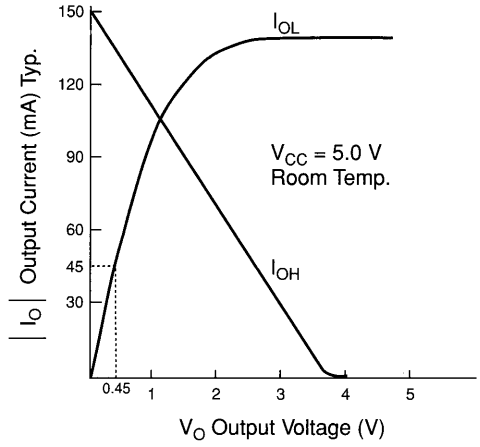


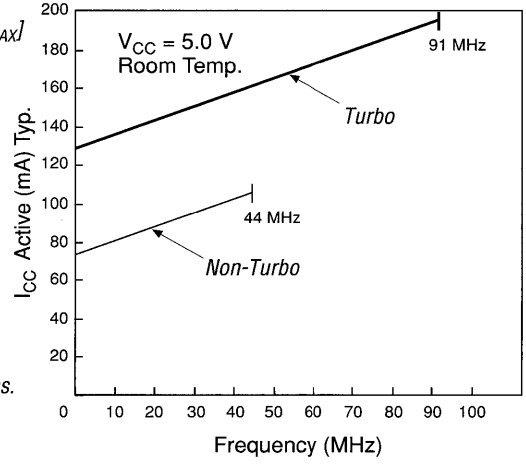
Figure 29 shows typical supply current versus frequency for the EPM7160.

Figure 29. EPM7160 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.82 \times MC_{TON}) + (0.43 \times MC_{TOFF}) + [(0.0046 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with an output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		110		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		115		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (2)*

External Timing Parameters			EPM7160-12		EPM7160-15		EPM7160-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		9		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		5		5		ns
t_{AH}	Array clock hold time		4		5		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7160-12		EPM7160-15		EPM7160-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3		3	ns
t_{IO}	I/O input pad and buffer delay			2		3		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		2		2	ns
t_{LAD}	Logic array delay			5		5		8	ns
t_{LAC}	Logic control array delay			5		5		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		4		5		4		ns
t_{H}	Register hold time		4		5		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		8	ns
t_{EN}	Register enable time			5		5		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*Note (7)*		12		13		15	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample tested only. `OE1n` (high-voltage pin during programming) has a capacitance of 25 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, and t_{ACL} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7160-12, EPM7160-15, EPM7160-20
Industrial Temp.	(–40° C to 85° C)	EPM7160-20
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7128 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7160-1	EPM7160-12
EPM7160-2	EPM7160-15
EPM7160-3	EPM7160-20

Pin-Out Information

Tables 9 and 10 provide pin-out information for the EPM7160 packages.

Table 9. EPM7160 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
GCLK	83	89	139
GCLRn	1	91	141
OE1n	84	90	140
OE2n	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	8, 26, 55, 61, 79, 104, 133, 143
No Connect (N.C.)	6, 39, 46, 79	–	1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157

Table 10. EPM7160 I/O Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	11	2	158	17	B	18	11	15
2	A	–	–	–	18	B	–	–	–
3	A	10	1	153	19	B	17	10	14
4	A	–	–	–	20	B	–	–	–
5	A	–	–	152	21	B	–	–	13
6	A	–	100	151	22	B	–	9	12
7	A	–	–	–	23	B	–	–	–
8	A	9	99	150	24	B	16	8	11
9	A	8	98	149	25	B	15	7	10
10	A	–	–	–	26	B	–	–	–
11	A	5	96	147	27	B	14	6	9
12	A	–	–	–	28	B	–	–	–
13	A	–	–	146	29	B	–	–	7
14	A	–	95	145	30	B	–	4	160
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	12	3	159
33	C	–	21	27	49	D	–	–	48
34	C	–	–	–	50	D	–	–	–
35	C	25	19	25	51	D	33	30	44
36	C	–	–	–	52	D	–	–	–
37	C	–	–	24	53	D	–	29	43
38	C	24	18	23	54	D	31	27	41
39	C	–	–	–	55	D	–	–	–
40	C	23	17	22	56	D	30	26	33
41	C	–	12	16	57	D	–	–	32
42	C	–	–	–	58	D	–	–	–
43	C	20	14	18	59	D	29	25	31
44	C	–	–	–	60	D	–	–	–
45	C	–	–	19	61	D	–	24	30
46	C	21	15	20	62	D	28	23	29
47	C	–	–	–	63	D	–	–	–
48	C	22	16	21	64	D	27	22	28

Table 10. EPM7160 I/O Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	–	–	59	81	F	–	–	62
66	E	–	–	–	82	F	–	–	–
67	E	41	39	58	83	F	44	42	63
68	E	–	–	–	84	F	–	–	–
69	E	–	38	57	85	F	–	43	64
70	E	40	37	56	86	F	45	44	65
71	E	–	–	–	87	F	–	–	–
72	E	37	35	54	88	F	48	46	67
73	E	–	–	53	89	F	–	–	68
74	E	–	–	–	90	F	–	–	–
75	E	36	34	52	91	F	49	47	69
76	E	–	–	–	92	F	–	–	–
77	E	–	33	51	93	F	–	48	70
78	E	35	32	50	94	F	50	49	71
79	E	–	–	–	95	F	–	–	–
80	E	34	31	49	96	F	51	50	72
97	G	–	–	73	113	H	–	60	94
98	G	–	–	–	114	H	–	–	–
99	G	52	51	77	115	H	60	62	96
100	G	–	–	–	116	H	–	–	–
101	G	–	52	78	117	H	–	–	97
102	G	54	54	80	118	H	61	63	98
103	G	–	–	–	119	H	–	–	–
104	G	55	55	88	120	H	62	64	99
105	G	–	–	89	121	H	–	69	105
106	G	–	–	–	122	H	–	–	–
107	G	56	56	90	123	H	65	67	103
108	G	–	–	–	124	H	–	–	–
109	G	–	57	91	125	H	–	–	102
110	G	57	58	92	126	H	64	66	101
111	G	–	–	–	127	H	–	–	–
112	G	58	59	93	128	H	63	65	100

Table 10. EPM7160 I/O Pin-Outs (Part 3 of 3)

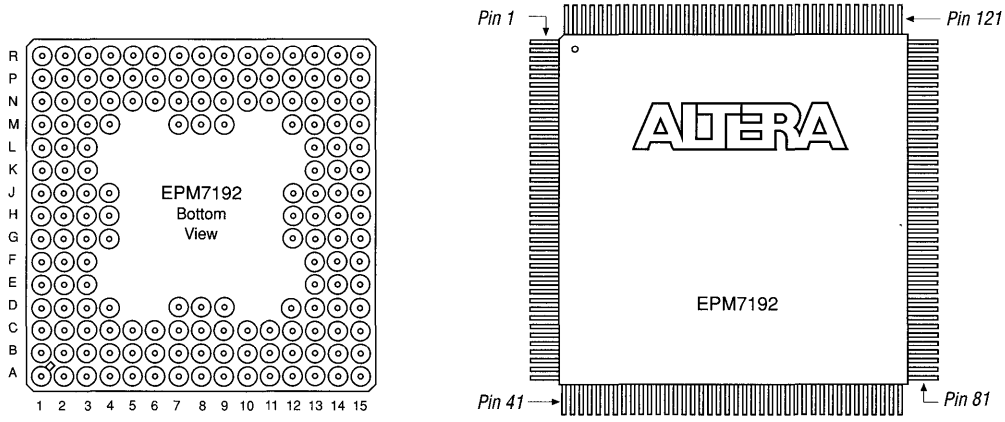
MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
129	I	67	70	106	145	J	74	79	123
130	I	–	–	–	146	J	–	–	–
131	I	68	71	107	147	J	75	80	128
132	I	–	–	–	148	J	–	–	–
133	I	–	–	108	149	J	–	–	129
134	I	–	72	109	150	J	–	81	130
135	I	–	–	–	151	J	–	–	–
136	I	69	73	110	152	J	76	82	131
137	I	70	74	111	153	J	77	83	132
138	I	–	–	–	154	J	–	–	–
139	I	71	75	112	155	J	80	85	134
140	I	–	–	–	156	J	–	–	–
141	I	–	–	114	157	J	–	–	135
142	I	–	77	121	158	J	–	86	136
143	I	–	–	–	159	J	–	–	–
144	I	73	78	122	160	J	81	87	137

Features

- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 3,750 usable gates
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture providing up to 124 inputs or 120 outputs
- 192 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 160-pin packages (see Figure 30):
  - Pin-grid array (PGA)
  - Plastic quad flat pack (PQFP)

Figure 30. EPM7192 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 11 and 12 in this data sheet for pin-out information.



160-Pin PGA

160-Pin QFP

General Description

The Altera EPM7192 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 31. Fabricated on a 0.8-micron EEPROM technology, the EPM7192 provides 3,750 usable gates, counter speeds of 90.9 MHz and propagation delays of 12 ns. The EPM7192 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 192 macrocells, the EPM7192 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s.

The high density and high I/O pin count make the EPM7192 appropriate for prototyping gate arrays. The EPM7192 can accommodate both logic- and I/O-intensive designs.

Figure 31. EPM7192 Block Diagram

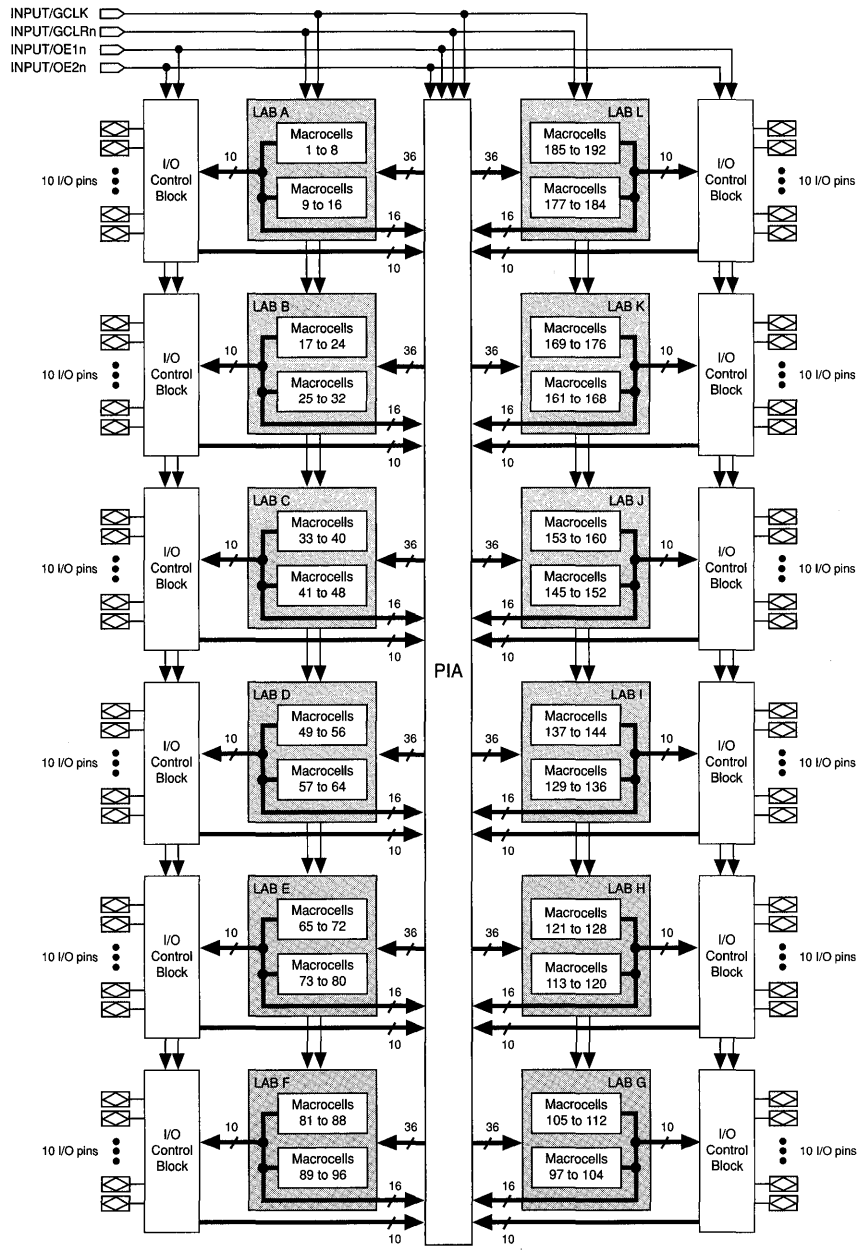


Figure 32 shows the output drive characteristics of EPM7192 I/O pins.

Figure 32. EPM7192 Output Drive Characteristics

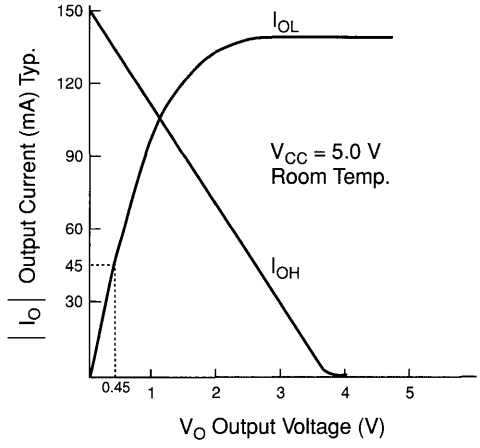


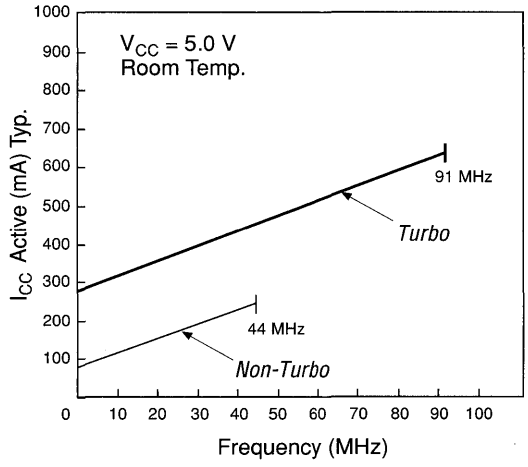
Figure 33 shows typical supply current versus frequency for the EPM7192.

Figure 33. EPM7192 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (1.5 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0088 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		130		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		135		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7192-12		EPM7192-15		EPM7192-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		9		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		5		5		ns
t_{AH}	Array clock hold time		4		5		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7192-12		EPM7192-15		EPM7192-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3		3	ns
t_{IO}	I/O input pad and buffer delay			2		3		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		2		2	ns
t_{LAD}	Logic array delay			5		5		8	ns
t_{LAC}	Logic control array delay			5		5		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		4		5		4		ns
t_{H}	Register hold time		4		5		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		8	ns
t_{EN}	Register enable time			5		5		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*Note (7)*		12		13		15	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7192-12, EPM7192-15, EPM7192-20
Industrial Temp.	(–40° C to 85° C)	EPM7192-20
Military Temp.	(–55° C to 125° C)	Consult factory
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7192 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7192-1	EPM7192-12
EPM7192-2	EPM7192-15
EPM7192-3	EPM7192-20

Pin-Out Information

Tables 11 and 12 provide pin-out information for the EPM7192 packages.

Table 11. EPM7192 Dedicated Pin-Outs

Dedicated Pin	160-Pin PGA	160-Pin QFP
GCLK	M8	139
GCLRn	N8	141
OE1n	P8	140
OE2n	R8	142
GND	C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148
VCC	C5, C7, C9, C10, C12, D3, G12, H4, J12, M3, N5, N7, N9, N12	10, 25,40,55, 56, 65, 74, 89, 103, 118, 133, 137, 144, 155
No Connect (N.C.)	A1, A2, A14, A15, R1, R2, R14, R15	1, 11, 39,54, 67, 82, 110, 120

Table 12. EPM7192 I/O Pin-Outs (Part 1 of 2)

MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP
1	A	M12	156	17	B	L14	8	33	C	H14	21
2	A	–	–	18	B	–	–	34	C	–	–
3	A	P11	154	19	B	M14	7	35	C	J13	20
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P12	153	21	B	M15	6	37	C	H15	19
6	A	P10	152	22	B	N14	5	38	C	J15	17
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R12	151	24	B	N15	4	40	C	J14	16
9	A	N10	150	25	B	P15	2	41	C	K15	15
10	A	–	–	26	B	–	–	42	C	–	–
11	A	R11	149	27	B	N13	160	43	C	K13	14
12	A	–	–	28	B	–	–	44	C	–	–
13	A	R10	147	29	B	P14	159	45	C	L15	13
14	A	P9	146	30	B	P13	158	46	C	K14	12
15	A	–	–	31	B	–	–	47	C	–	–
16	A	R9	145	32	B	R13	157	48	C	L13	9
49	D	D15	33	65	E	B12	45	81	F	D8	60
50	D	–	–	66	E	–	–	82	F	–	–
51	D	E15	31	67	E	B13	44	83	F	A9	59
52	D	–	–	68	E	–	–	84	F	–	–
53	D	E14	30	69	E	C13	43	85	F	C8	58
54	D	F15	29	70	E	B14	42	86	F	B9	53
55	D	–	–	71	E	–	–	87	F	–	–
56	D	F13	28	72	E	C14	41	88	F	A10	52
57	D	G14	27	73	E	D12	38	89	F	B10	51
58	D	–	–	74	E	–	–	90	F	–	–
59	D	F14	26	75	E	B15	37	91	F	A11	50
60	D	–	–	76	E	–	–	92	F	–	–
61	D	G13	24	77	E	D14	36	93	F	B11	49
62	D	G15	23	78	E	C15	35	94	F	A12	48
63	D	–	–	79	E	–	–	95	F	–	–
64	D	H13	22	80	E	E13	34	96	F	A13	46

Table 12. EPM7192 I/O Pin-Outs (Part 2 of 2)

MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP
97	G	A8	61	113	H	A3	76	129	I	E3	88
98	G	–	–	114	H	–	–	130	I	–	–
99	G	B8	62	115	H	B4	77	131	I	F3	90
100	G	–	–	116	H	–	–	132	I	–	–
101	G	A7	63	117	H	B3	78	133	I	E2	91
102	G	A6	68	118	H	C3	79	134	I	F2	92
103	G	–	–	119	H	–	–	135	I	–	–
104	G	B7	69	120	H	B2	80	136	I	E1	93
105	G	A5	70	121	H	B1	83	137	I	G3	94
106	G	–	–	122	H	–	–	138	I	–	–
107	G	B6	71	123	H	C2	84	139	I	F1	95
108	G	–	–	124	H	–	–	140	I	–	–
109	G	A4	72	125	H	C1	85	141	I	G1	97
110	G	B5	73	126	H	D2	86	142	I	G2	98
111	G	–	–	127	H	–	–	143	I	–	–
112	G	D4	75	128	H	D1	87	144	I	H1	99
145	J	H2	100	161	K	L2	113	177	L	R3	125
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J1	101	163	K	N1	114	179	L	R4	127
148	J	–	–	164	K	–	–	180	L	–	–
149	J	H3	102	165	K	L3	115	181	L	M4	128
150	J	J3	104	166	K	P1	116	182	L	R5	129
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K1	105	168	K	M2	117	184	L	P5	130
153	J	J2	106	169	K	N2	119	185	L	R6	131
154	J	–	–	170	K	–	–	186	L	–	–
155	J	K2	107	171	K	P2	121	187	L	P6	132
156	J	–	–	172	K	–	–	188	L	–	–
157	J	K3	108	173	K	N3	122	189	L	N6	134
158	J	L1	109	174	K	P3	123	190	L	R7	135
159	J	–	–	175	K	–	–	191	L	–	–
160	J	M1	112	176	K	P4	124	192	L	P7	136

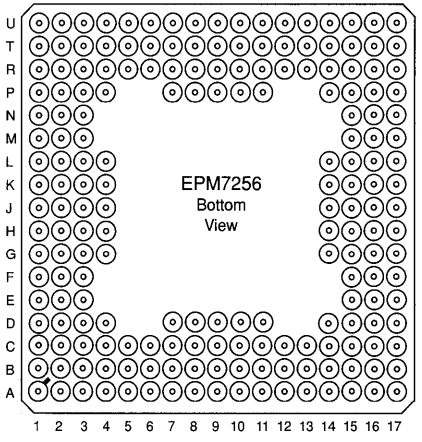
Notes:

Features

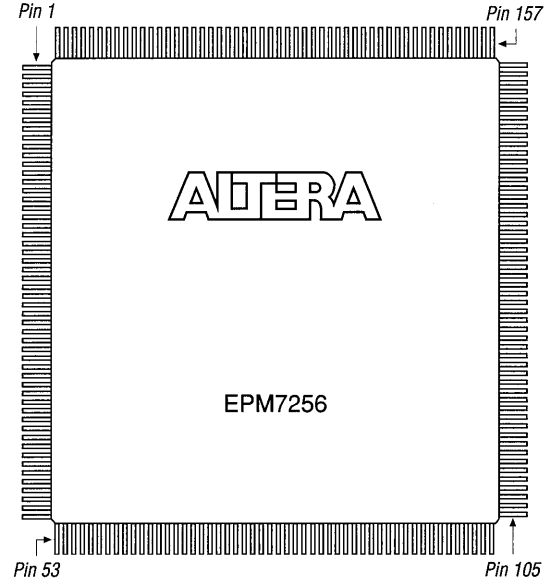
- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 5,000 usable gates
  - Combinatorial speeds with t_{PD} = 20 ns (Higher speed versions under development)
  - Counter frequencies up to 62.5 MHz
- Advanced 0.8-micron CMOS EPROM technology
- Programmable I/O architecture with up to 164 inputs or 160 outputs
- 256 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in the following packages (see Figure 34):
  - 192-pin pin-grid array (PGA)
  - 208-pin power quad flat pack (RQFP)
  - 208-pin metal quad flat pack (MQFP)

Figure 34. EPM7256 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 13 and 14 in this data sheet for pin-out information.



192-Pin PGA



208-Pin QFP

General Description

The Altera EPM7256 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 35. Fabricated on a 0.8-micron EPROM technology, the EPM7256 provides 5,000 usable gates, counter speeds of 62.5 MHz and propagation delays of

20 ns. The EPM7256 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 256 macrocells, the EPM7256 implements complete system-level designs. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH devices and FPGAs. The high density and high I/O pin count make the EPM7256 appropriate for prototyping gate arrays. The EPM7256 can accommodate both logic- and I/O-intensive designs.

Figure 35. EPM7256 Block Diagram

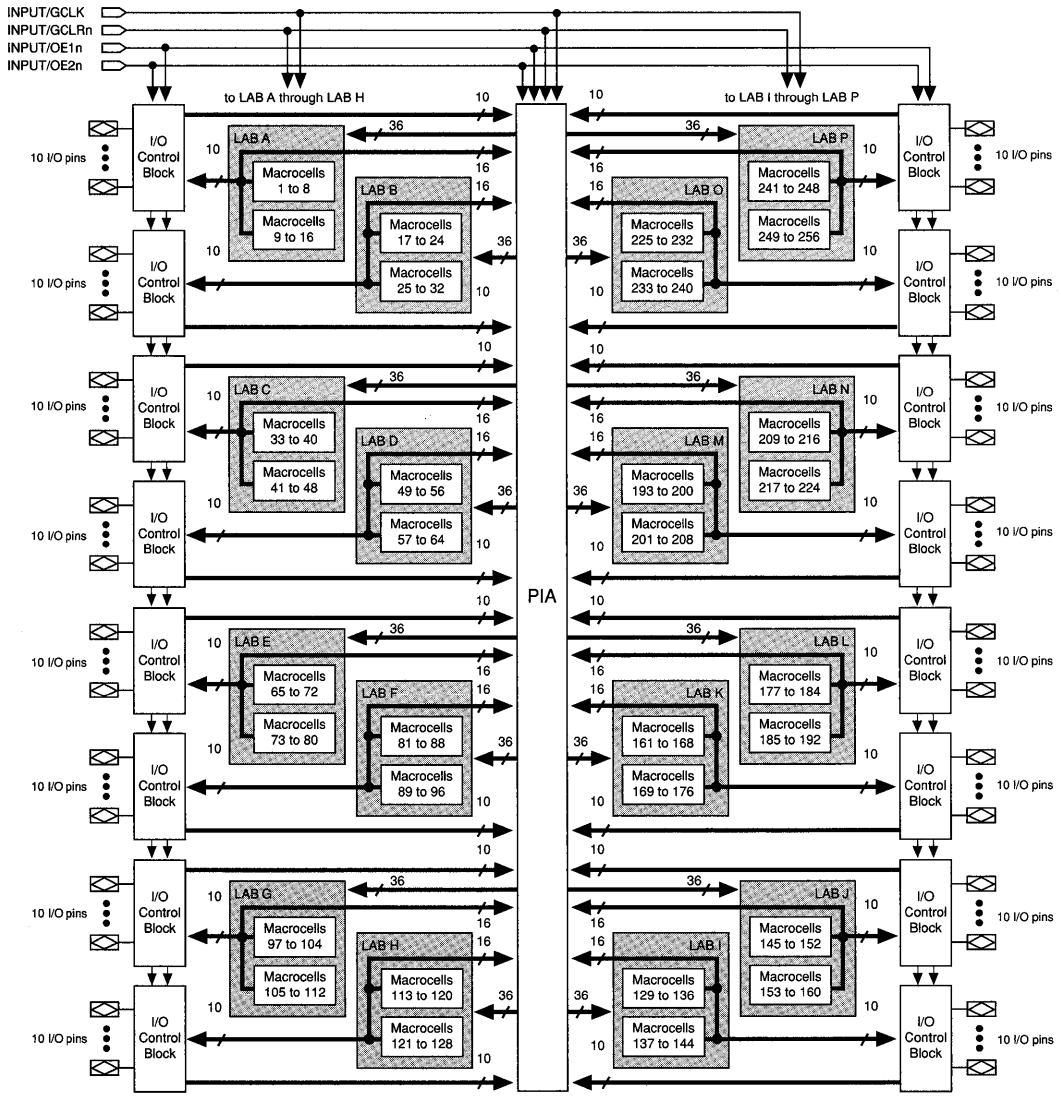


Figure 36 shows the output drive characteristics of EPM7256 I/O pins.

Figure 36. EPM7256 Output Drive Characteristics

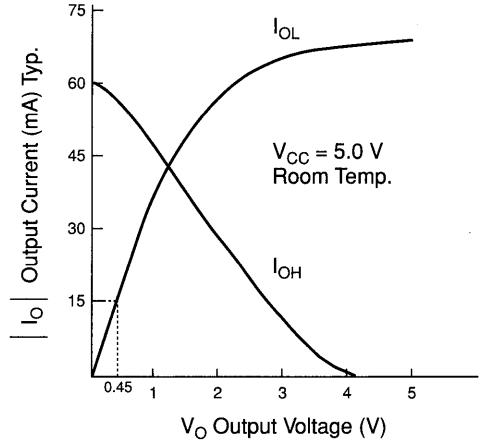


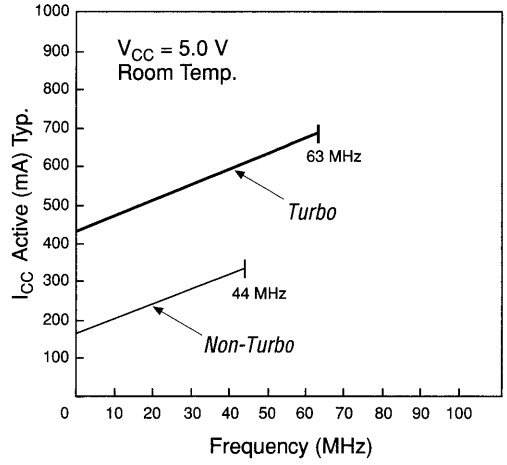
Figure 37 shows typical supply current versus frequency for the EPM7256.

Figure 37. EPM7256 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (1.7 \times MC_{TON}) + (0.59 \times MC_{TOFF}) + [(0.015 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		150		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		155		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7256-20		EPM7256-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		6		8		ns
t_{CL}	Global clock low time		6		8		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	ns
t_{ACH}	Array clock high time		8		12.5		ns
t_{ACL}	Array clock low time		8		12.5		ns
t_{CNT}	Minimum global clock period			16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	62.5		50		MHz
t_{ACNT}	Minimum array clock period			16		25	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	62.5		40		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	83.3		62.5		MHz

Internal Timing Parameters			EPM7256-20		EPM7256-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Shared expander delay			8		10	ns
t_{PEXP}	Parallel expander delay			2		3	ns
t_{LAD}	Logic array delay			8		10	ns
t_{LAC}	Logic control array delay			8		10	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		6	ns
t_{ZX}	Output buffer enable delay			9		12	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		9		12	ns
t_{SU}	Register setup time		4		5		ns
t_{H}	Register hold time		5		6		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{IC}	Array clock delay			8		10	ns
t_{EN}	Register enable time			8		10	ns
t_{GLOB}	Global control delay			3		4	ns
t_{PRE}	Register preset time			4		4	ns
t_{CLR}	Register clear time			4		4	ns
t_{PIA}	Prog. Interconnect Array delay			3		4	ns
t_{LPA}	Low power adder	*Note (7)*		7		8	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7256-20, EPM7256-25
Industrial Temp.	(–40° C to 85° C)	EPM7256-25
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7256 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7256-2	EPM7256-20
EPM7256	EPM7256-25

Pin-Out Information

Tables 13 and 14 provide pin-out information for the EPM7256 packages.

Table 13. EPM7256 Dedicated Pin-Outs *Note (1)*

Dedicated Pin	192-Pin PGA	208-Pin MQFP, RQFP
GCLK	P9	184
GCLRn	R9	182
OE1n	T9	183
OE2n	U9	181
GND	C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11	14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200
VCC	C5, C11, D7, D11, D14, G4, H14, K4, L14, P3, P7, P11, R5, R14	5, 23, 41, 63, 74, 83, 85, 107, 125, 143, 165, 179, 186, 191
No Connect (N.C.)	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208

Note to tables:

(1) CQFP pin-out information differs from the MQFP and RQFP pin-out information given in this table. Contact Altera Applications for CQFP pin-out information.

Table 14. EPM7256 I/O Pin-Outs (Part 1 of 3)

MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP
1	A	U17	153	17	B	N17	141	33	C	B17	108
2	A	–	–	18	B	–	–	34	C	–	–
3	A	R16	154	19	B	M16	142	35	C	C15	109
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P14	159	21	B	M15	144	37	C	C17	110
6	A	U16	160	22	B	P17	145	38	C	C16	111
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R15	161	24	B	N16	146	40	C	D17	112
9	A	U15	162	25	B	R17	147	41	C	D15	113
10	A	–	–	26	B	–	–	42	C	–	–
11	A	T15	163	27	B	P16	148	43	C	E17	114
12	A	–	–	28	B	–	–	44	C	–	–
13	A	U14	164	29	B	T17	149	45	C	D16	115
14	A	U13	166	30	B	N15	150	46	C	E15	117
15	A	–	–	31	B	–	–	47	C	–	–
16	A	T14	167	32	B	T16	151	48	C	F16	118
49	D	A14	92	65	E	U12	168	81	F	J16	130
50	D	–	–	66	E	–	–	82	F	–	–
51	D	B12	93	67	E	R13	169	83	F	J15	131
52	D	–	–	68	E	–	–	84	F	–	–
53	D	B13	95	69	E	U11	170	85	F	K17	132
54	D	A15	96	70	E	T13	171	86	F	J14	133
55	D	–	–	71	E	–	–	87	F	–	–
56	D	B14	97	72	E	T11	172	88	F	K16	135
57	D	A16	98	73	E	T12	173	89	F	K15	136
58	D	–	–	74	E	–	–	90	F	–	–
59	D	C14	99	75	E	R12	175	91	F	L17	137
60	D	–	–	76	E	–	–	92	F	–	–
61	D	B16	100	77	E	U10	176	93	F	L16	138
62	D	B15	101	78	E	R10	177	94	F	M17	139
63	D	–	–	79	E	–	–	95	F	–	–
64	D	A17	102	80	E	T10	178	96	F	L15	140

Table 14. EPM7256 I/O Pin-Outs (Part 2 of 3)

MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP
97	G	E16	119	113	H	C9	79	129	I	U6	197
98	G	–	–	114	H	–	–	130	I	–	–
99	G	F17	120	115	H	D9	80	131	I	T5	196
100	G	–	–	116	H	–	–	132	I	–	–
101	G	F15	121	117	H	C10	81	133	I	U7	195
102	G	G16	122	118	H	A10	84	134	I	T6	194
103	G	–	–	119	H	–	–	135	I	–	–
104	G	G15	123	120	H	A11	86	136	I	T7	193
105	G	G17	124	121	H	B10	87	137	I	R6	192
106	G	–	–	122	H	–	–	138	I	–	–
107	G	H17	126	123	H	A12	88	139	I	R7	190
108	G	–	–	124	H	–	–	140	I	–	–
109	G	H15	127	125	H	B11	89	141	I	U8	189
110	G	J17	128	126	H	A13	90	142	I	R8	188
111	G	–	–	127	H	–	–	143	I	–	–
112	G	H16	129	128	H	C12	91	144	I	T8	187
145	J	J2	27	161	K	F3	38	177	L	B9	78
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J3	26	163	K	F1	37	179	L	C8	77
148	J	–	–	164	K	–	–	180	L	–	–
149	J	K1	25	165	K	E2	36	181	L	A9	76
150	J	J4	24	166	K	G2	35	182	L	A8	73
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K2	22	168	K	G3	34	184	L	A7	71
153	J	K3	21	169	K	G1	33	185	L	B8	70
154	J	–	–	170	K	–	–	186	L	–	–
155	J	L1	20	171	K	H1	31	187	L	A6	69
156	J	–	–	172	K	–	–	188	L	–	–
157	J	L2	19	173	K	H3	30	189	L	B7	68
158	J	M1	18	174	K	J1	29	190	L	A5	67
159	J	–	–	175	K	–	–	191	L	–	–
160	J	L3	17	176	K	H2	28	192	L	C6	66

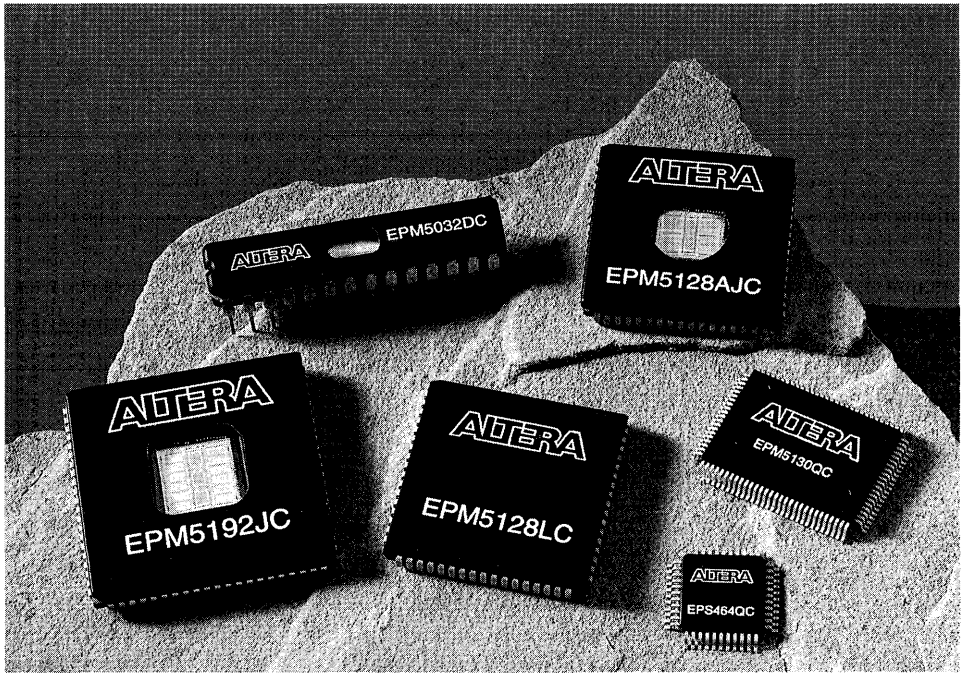
Table 14. EPM7256 I/O Pin-Outs (Part 3 of 3)

MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP
193	M	U1	4	209	N	N1	16
194	M	–	–	210	N	–	–
195	M	R2	3	211	N	M2	15
196	M	–	–	212	N	–	–
197	M	R3	206	213	N	M3	13
198	M	U2	205	214	N	P1	12
199	M	–	–	215	N	–	–
200	M	P4	204	216	N	N2	11
201	M	U3	203	217	N	R1	10
202	M	–	–	218	N	–	–
203	M	T3	202	219	N	P2	9
204	M	–	–	220	N	–	–
205	M	U4	201	221	N	T1	8
206	M	U5	199	222	N	N3	7
207	M	–	–	223	N	–	–
208	M	T4	198	224	N	T2	6
225	O	B1	49	241	P	A4	65
226	O	–	–	242	P	–	–
227	O	C3	48	243	P	B6	64
228	O	–	–	244	P	–	–
229	O	C1	47	245	P	B5	62
230	O	D3	46	246	P	A3	61
231	O	–	–	247	P	–	–
232	O	D1	45	248	P	B4	60
233	O	C2	44	249	P	A2	59
234	O	–	–	250	P	–	–
235	O	E1	43	251	P	C4	58
236	O	–	–	252	P	–	–
237	O	E3	42	253	P	B2	57
238	O	D2	40	254	P	B3	56
239	O	–	–	255	P	–	–
240	O	F2	39	256	P	A1	55

Contents

August 1993

Section 4 MAX 5000/EPS464


ALTERA
EPM5032DC
ALTERA
EPM5128AJC
ALTERA
EPM5192JC
ALTERA
EPM5128LC
ALTERA
EPM5130QC
ALTERA
EPS464QC

MAX 5000/EPS464

Programmable Logic Device Family

August 1993, ver. 1 | Data Sheet

Features

- Advanced Multiple Array MatriX (MAX) 5000/EPS464 architecture combining speed and ease-of-use of PAL devices with density of programmable gate arrays
- Complete family of high-performance, erasable 0.8-micron CMOS EPROM EPLDs for designs ranging from fast 20-pin address decoders to 100-pin LSI custom peripherals (see Table 1)
- Second-generation MAX 5000A devices on 0.65-micron CMOS EPROM process providing higher performance
- Fast, 12-ns combinatorial delays and 111.1-MHz counter frequencies
- Configurable expander product-term distribution allowing more than 32 product terms in a single macrocell
- 20 to 100 pins available in DIP, J-lead, PGA, SOIC, and QFP packages
- Programmable registers providing D, T, JK, and SR flipflop functionality with individual Clear, Preset, and Clock controls
- Programmable Security Bit for total protection of proprietary designs
- Software design support featuring Altera's MAX+PLUS II development system on 386- or 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations
- Programming support with Altera's Master Programming Unit (MPU) or programming hardware from other manufacturers
- EDIF, Verilog, VHDL and other interfaces providing additional design entry and simulation support with popular CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic

Table 1. MAX 5000/EPS464 Device Features

Feature	EPM5016	EPM5032	EPS464	EPM5064	EPM5128	EPM5128A	EPM5130	EPM5192	EPM5192A
Avail. Gates	600	1,200	2,500	2,500	5,000	5,000	5,000	7,500	7,500
Usable Gates	300	600	1,250	1,250	2,500	2,500	2,500	3,750	3,750
Macrocells	16	32	64	64	128	128	128	192	192
LABs	1	1	1	4	8	8	8	12	12
Expanders	32	64	256	128	256	256	256	384	384
Routing	global	global	global	PIA	PIA	PIA	PIA	PIA	PIA
Max. User I/O	16	24	36	36	60	60	68, 84	72	72
t_{PD} (ns)	15	15	20	25	25	12	25	25	15
t_{ASU} (ns)	5	7	6	5	5	4	5	5	5
t_{CO} (ns)	9	10	12	14	14	6	14	14	7
f_{CNT} (MHz)	100	76.9	66.7	50	50	111.1	50	50	83.3

General Description

The MAX 5000/EPS464 family combines innovative architecture and advanced process technologies to offer optimum performance, flexibility, and the highest logic-to-pin ratio of any general-purpose programmable logic device family. Fabricated on an advanced CMOS EPROM technology, the MAX 5000/EPS464 family includes three types of devices—MAX 5000, MAX 5000A, and EPS464—each described in this data sheet.

The MAX 5000/EPS464 architecture supports 100% TTL emulation and high-density integration of multiple SSI, MSI, and LSI logic functions. For example, an EPM5192 can replace over 100 7400-series devices; it can integrate complete subsystems into a single package, saving board area and reducing power consumption. MAX 5000/EPS464 EPLDs are available in a wide range of packages: windowed ceramic and plastic dual in-line (CerDIP and PDIP), windowed ceramic and plastic J-lead chip carrier (JLCC and PLCC), windowed ceramic pin-grid array (PGA), plastic small-outline integrated circuit (SOIC), and windowed ceramic and plastic quad flat pack (CQFP and PQFP) packages. See Table 2.

MAX 5000/EPS464 EPLD densities range from 16 to 192 macrocells that are combined into groups called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable Clock, Clear, and Preset functions. To build complex logic functions, each macrocell

Table 2. MAX 5000/EPS464 Device Pin Count & Package Options *Note (1)*

Pin Count	EPM5016	EPM5032	EPS464	EPM5064	EPM5128	EPM5128A	EPM5130	EPM5192	EPM5192A
20	CerDIP PDIP SOIC	–	–	–	–	–	–	–	–
28	–	CerDIP PDIP JLCC/PLCC	–	–	–	–	–	–	–
44	–	–	JLCC PLCC PQFP	JLCC PLCC	–	–	–	–	–
68	–	–	–	–	JLCC/PLCC PGA	JLCC/PLCC PGA	–	–	–
84	–	–	–	–	–	–	JLCC/PLCC	JLCC/PLCC PGA	JLCC/PLCC PGA
100	–	–	–	–	–	–	PGA CQFP PQFP		PQFP

Note:
(1) Contact Altera for information on available device packages.

can be supplemented with shareable expander product terms ("expanders") to provide more than 32 product terms per macrocell.

The MAX 5000/EPS464 family is supported by Altera's MAX+PLUS II development system, a single integrated package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and programming software. MAX+PLUS II provides EDIF, VHDL, Verilog, and other netlist interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. MAX+PLUS II runs on 386- and 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations.

MAX 5000 EPLDs

Developed on a 0.8-micron CMOS EPROM process, these first-generation MAX EPLDs offer pin-to-pin logic delays as fast as 15 ns and counter frequencies as high as 100 MHz. MAX 5000 devices range from the 16-macrocell EPM5016 to the 192-macrocell EPM5192.

MAX 5000A EPLDs

MAX 5000A EPLDs are developed on an advanced 0.65-micron CMOS EPROM technology. Produced on a state-of-the-art process, MAX 5000A devices offer pin-to-pin delays as fast as 12 ns and counter frequencies as high as 111 MHz. MAX 5000A EPLDs are fully pin-, function-, and programming-file-compatible with their MAX 5000 counterparts.

EPS464 EPLDs

The EPS464 is an advanced general-purpose EPLD based on the MAX 5000 architecture. It has 64 enhanced macrocells and 256 shared expanders, all of which are routed globally to implement complex projects. Full global routing makes the EPS464 a high-performance device, capable of 66-MHz counter frequencies. The programmable I/O pins and dedicated inputs can implement up to 36 inputs or 32 outputs. The EPS464 is available in 44-pin JLCC, PLCC, and PQFP packages. For a functional description and other information, see "EPS464 EPLD" later in this section.

Functional Description

This section provides a functional description of MAX 5000 and MAX 5000A EPLDs, which have the same architecture. MAX 5000 devices have the following architectural features:

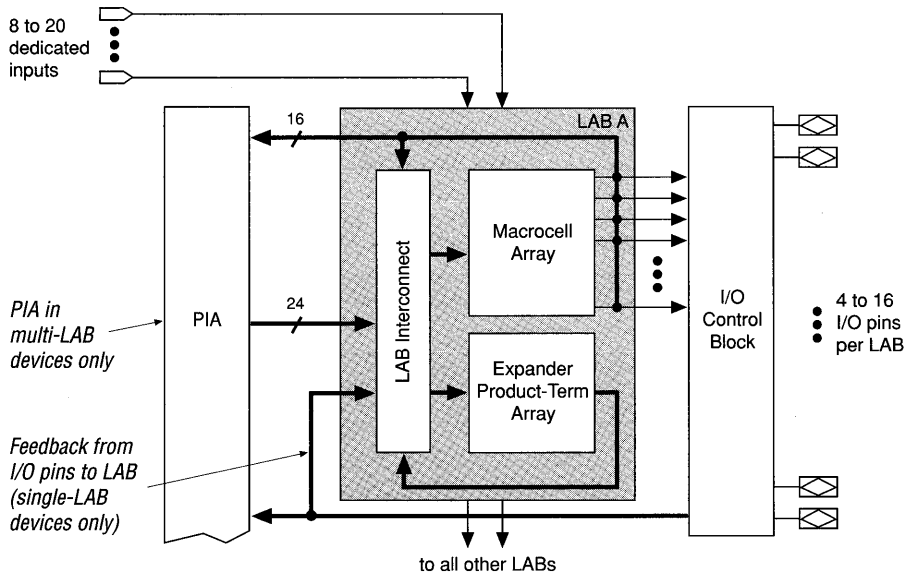
- ❑ Logic Array Blocks
- ❑ Macrocells
- ❑ Clocking options
- ❑ Expander product terms
- ❑ Programmable Interconnect Array
- ❑ I/O control blocks

MAX 5000 architecture is based on the concept of linking high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked together via the Programmable Interconnect Array (PIA), a global bus that is fed by all I/O pins and macrocells. In addition to these basic elements, the MAX 5000 architecture includes 8 to 20 dedicated inputs, each of which can be used as a high-speed, general-purpose input, or one of which can be used as a high-speed global Clock for registers.

Logic Array Blocks

MAX 5000 EPLDs contain 1 to 12 LABs. The EPM5016 and EPM5032 have a single LAB, while the EPM5064, EPM5128, EPM5128A, EPM5130, EPM5192, and EPM5192A contain multiple LABs. Each LAB consists of a macrocell array and an expander product-term array. See Figure 1. The number of macrocells and expanders in the arrays varies with each device.

Figure 1. MAX 5000 Architecture

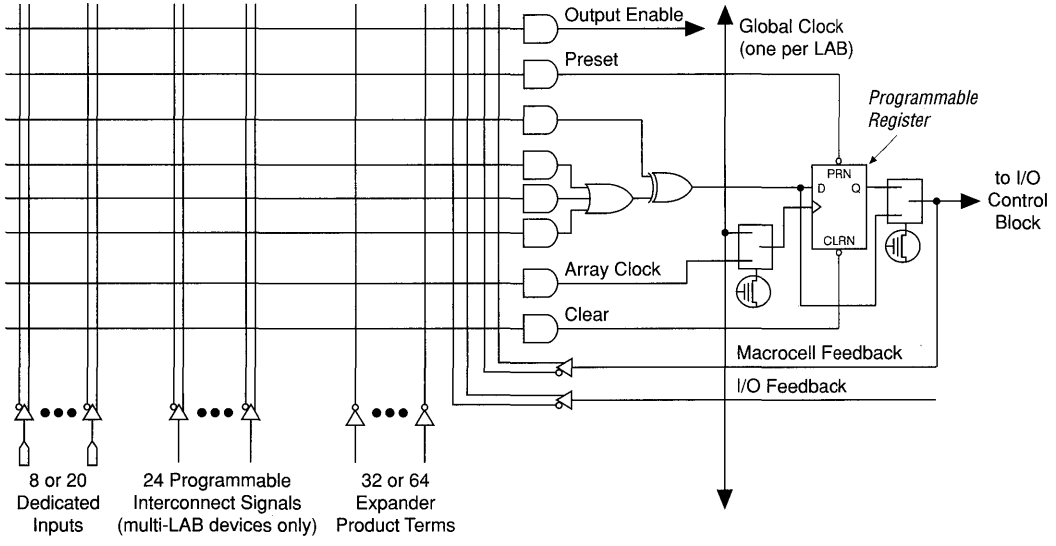


Macrocells are the primary resource for logic implementation. Additional logic capability is available from expanders, which can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. These flexible macrocells and shareable expanders facilitate variable product-term designs without the inflexibility of fixed product-term architectures. All macrocell outputs are globally routed within an LAB via the LAB interconnect, and also feed the PIA to provide efficient routing for high-fan-in designs. The outputs of the macrocells also feed the I/O control block, which consists of groups of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5128A, EPM5130, EPM5192, and EPM5192A, multiple LABs are connected by a Programmable Interconnect Array (PIA).

Macrocells

The MAX 5000 macrocell consists of a programmable logic array and an independently configurable register (see Figure 2). The register can be programmed to emulate D, T, JK, or SR operation, as a flow-through latch, or bypassed for purely combinatorial operation. Combinatorial logic is implemented in the programmable logic array, in which three product terms that are ORed together feed one input to an XOR gate. The second input to the XOR gate is controlled by a single product term that can implement active-high or active-low logic. The XOR gate is also used for complex XOR arithmetic logic functions and for De Morgan's inversion.

Figure 2. MAX 5000 Macrocell



The output of the XOR gate feeds the programmable register or bypasses it for combinatorial operation.

Additional product terms—called secondary product terms—are used to control the Output Enable, Preset, Clear, and Clock signals. Preset and Clear product terms drive the active-low asynchronous Preset and asynchronous Clear inputs to the configurable flipflop. The Clock product term allows each register to have an independent Clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin can use the Output Enable product term to control the active-high tri-state buffer in the I/O control block. These secondary product terms allow exact emulation of 74-series macrofunctions.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device.

Clocking Options

Each LAB supports either global or array clocking. Global clocking is provided by a dedicated Clock signal (CLK) that offers fast Clock-to-output delay times. Since each LAB has one global Clock, all flipflop Clocks within the LAB can be positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global Clock, it can be used as a high-speed dedicated input.

In the array clocking mode, each flipflop is clocked by a product term. Any input pin or internal logic can be used as a Clock source. Array clocking allows each flipflop to be configured for positive- or negative-edge-triggered operation, giving the macrocell increased flexibility. Systems that require multiple Clocks are easily integrated into MAX 5000 EPLDs.

Each flipflop in an LAB can be clocked by a different array-generated Clock; however, global and array clocking modes cannot be mixed in the same LAB.

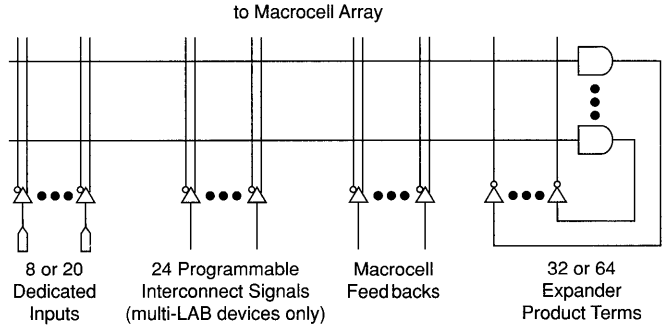
Expander Product Terms

While most logic functions can be implemented with the product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using additional macrocells to supply the needed logic resources, the MAX 5000 architecture uses shared expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has 32 shared expanders (except for the EPM5032 LAB, which has 64). The expanders can be viewed as a pool of uncommitted product terms. The expander product-term array (see Figure 3) contains unallocated, inverted product terms that feed the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs for MAX 5000 EPLDs.

Figure 3. Expander Product Terms

Expander product terms are unallocated logic that can be used and shared by all macrocells in an LAB. Sharing allows efficient integration of complex combinatorial functions.



Expanders are fed by all signals in the LAB. One expander can feed all macrocells in the LAB or multiple product terms in the same macrocell. Since expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. Expanders can also be cross-coupled to build additional flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shared expanders are used.

Programmable Interconnect Array

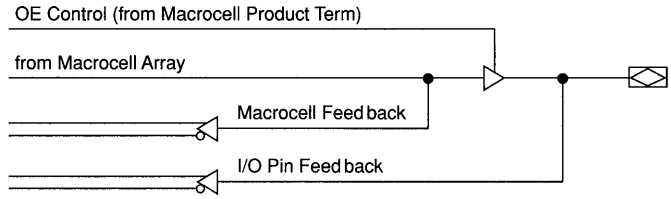
The higher-density MAX 5000 devices—EPM5064, EPM5128, EPM5128A, EPM5130, EPM5192, and EPM5192A—use a Programmable Interconnect Array (PIA) to route signals between the various LABs. The PIA, which is fed by all macrocell and I/O pin feedbacks, routes only the signals required for implementing logic in an LAB. While the routing delays of channel-based routing schemes in masked or field programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 5000 PIA has a fixed delay. The PIA thus eliminates skew between signals, and makes timing performance easy to predict.

I/O Control Blocks

Each LAB has an I/O control block that allows each I/O pin to be individually configured for input, output, or bidirectional operation. See Figure 4. The I/O control block is fed by the macrocell array. A dedicated macrocell product term controls a tri-state buffer, which drives the I/O pad.

Figure 4. I/O Control Block

The decoupled I/O control block features dual feedback to maximize flexibility of device pins.



Each I/O pin in a MAX 5000 device provides dual feedback, i.e., a feedback path both before and after the tri-state buffer. Since the tri-state buffer decouples the I/O pins from the macrocells, all registers within the LAB can be "buried." Thus, I/O pins can be configured as dedicated input, output, or bidirectional pins. Using an I/O pin as an input in single-LAB devices reduces the number of available expanders by two. In multi-LAB devices, I/O pins feed the PIA directly.

Design Security

All MAX 5000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

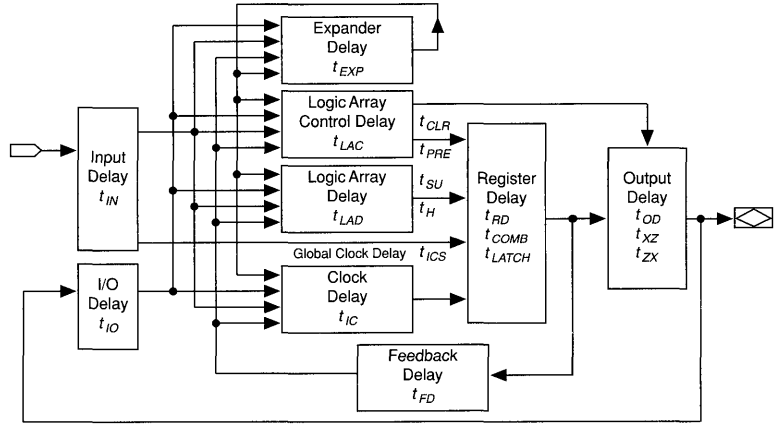
Timing Model

MAX 5000 EPLD timing can be analyzed with MAX+PLUS II software, with a variety of other industry-standard CAE simulators and timing analyzers, or with the timing model shown in Figure 5. MAX 5000 EPLDs have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis.

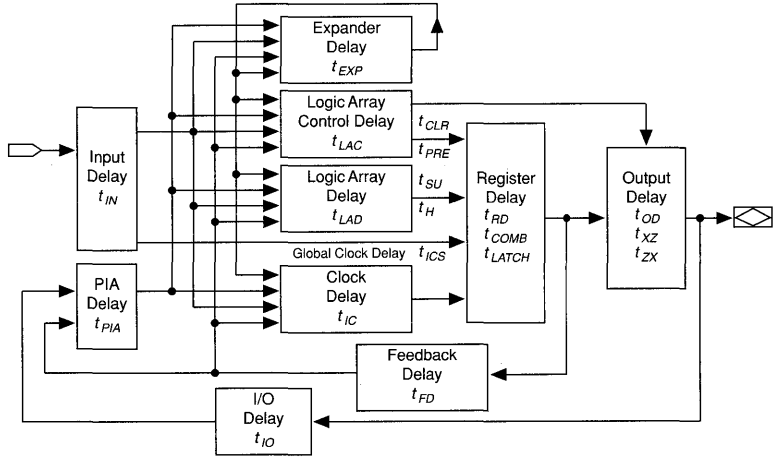
Figure 5. Timing Models

Design performance can be predicted with these timing models and the device performance specifications.

Single-LAB EPLDs



Multi-LAB EPLDs

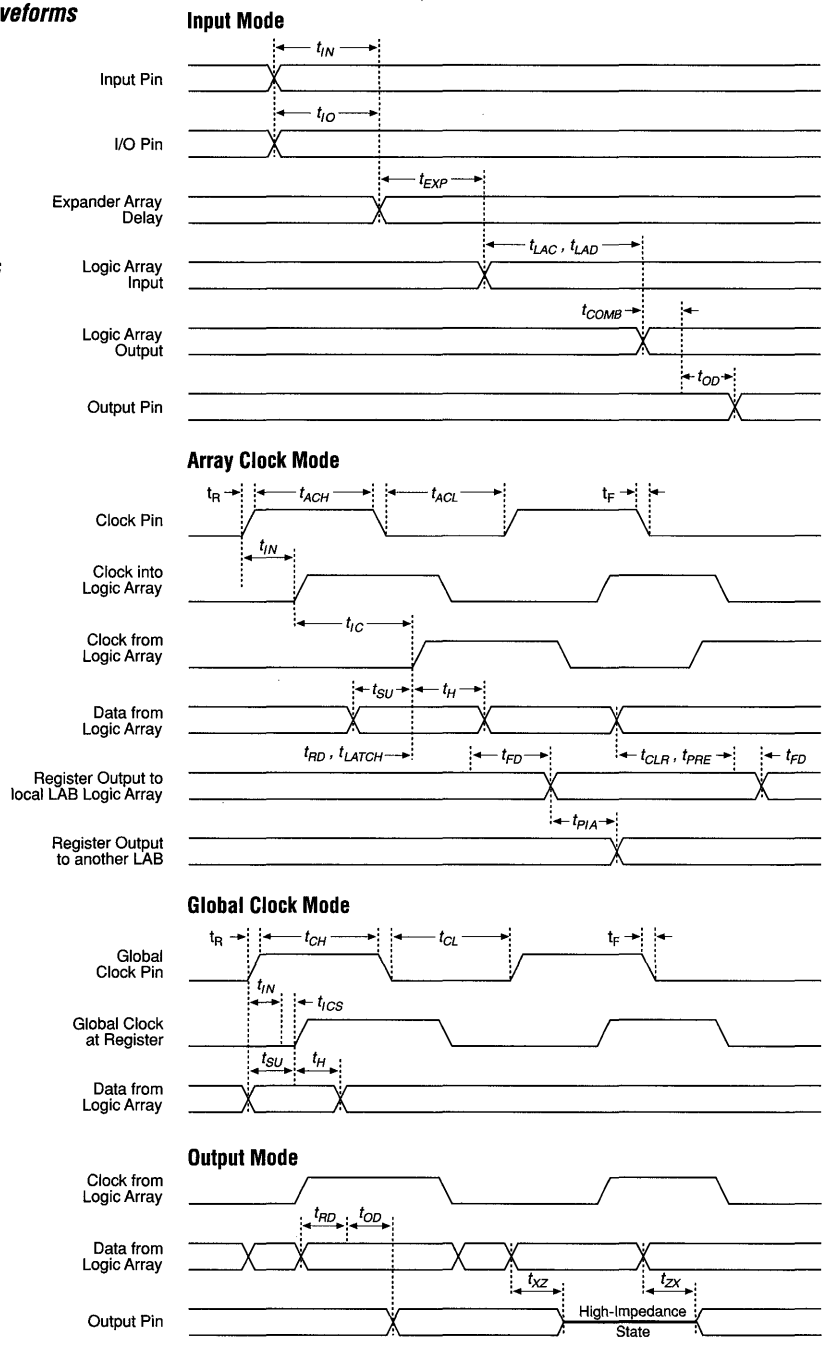


Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters are calculated with the sum of internal parameters and represent pin-to-pin timing delays. Figure 6 shows the internal timing relationship for internal and external delay parameters. For more information on EPLD timing, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Figure 6. Switching Waveforms

In multi-LAB EPLDs, I/O pins that are used as inputs traverse the PIA.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



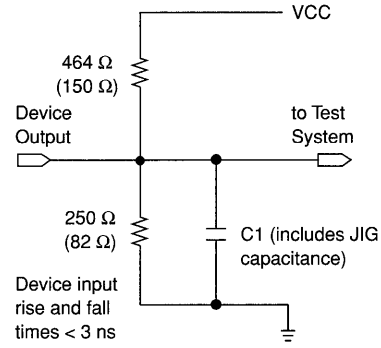
Generic Testing

MAX 5000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those in Figure 7.

Figure 7. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Numbers in parentheses are for the EPM5016.



Test patterns can be used and then erased during early stages of the device production flow. EPROM-based EPLDs in one-time-programmable windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during this production flow.

MAX+PLUS II Development System

MAX 5000 EPLDs are supported by the MAX+PLUS II development system, a completely integrated environment for design entry, compilation, verification, and programming. MAX+PLUS II software is available for 386- and 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations. MAX+PLUS II provides more than 300 74-series macrofunctions and the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, conditional logic, and truth table entry methods. MAX+PLUS II also provides highly automated compilation, automatic multi-device partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a comprehensive on-line help system.

In addition, MAX+PLUS II imports and exports industry-standard EDIF 2 0 0 and EDIF 2 9 0 netlist files for a convenient interface to industry-standard CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic. MAX+PLUS II also exports Verilog and VHDL netlist files that support simulation with other industry-standard simulators. For further details

about MAX+PLUS II and other CAE tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and *CAE Software Support* in this data book.

Device Programming

All MAX 5000 EPLDs can be programmed on 386- and 486-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera Programming Hardware.*

MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 5000 EPLD to the results of simulation. (This feature requires a device adapter with the "PLM-" prefix.)

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices. For more information, see *Programming Hardware Manufacturers.*

QFP Carrier & Development Socket

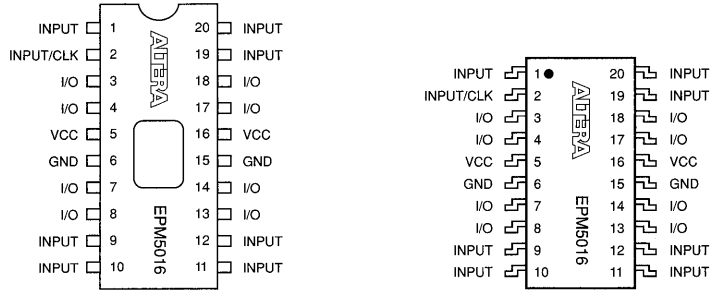
MAX 5000 devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the fragile QFP leads. Each carrier can be used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram devices without exposing the leads to mechanical stress. For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet.*

Features

- High-speed, single-LAB MAX 5000 EPLD
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- 16 individually configurable macrocells
- 32 shareable expander product terms ("expanders") allowing 36 product terms in a single macrocell
- 24-mA output drivers to allow direct interfacing to system buses
- Programmable I/O architecture allowing up to 16 inputs or 8 outputs
- Available in 20-pin, windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 8):
  - Dual in-line (CerDIP and PDIP)
  - Small-outline integrated circuit (plastic SOIC only)

Figure 8. EPM5016 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



General Description

The Altera EPM5016 is a MAX 5000 EPLD optimized for speed. It can integrate multiple SSI and MSI TTL and CMOS logic devices. In addition, the EPM5016 can replace any 20-pin PAL or PLA device with logic left over for further integration. The EPM5016 contains 16 macrocells; the expander product-term array provides 32 expanders. The I/O control block contains 8 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility. See Figure 9.

Figure 9. EPM5016 Block Diagram

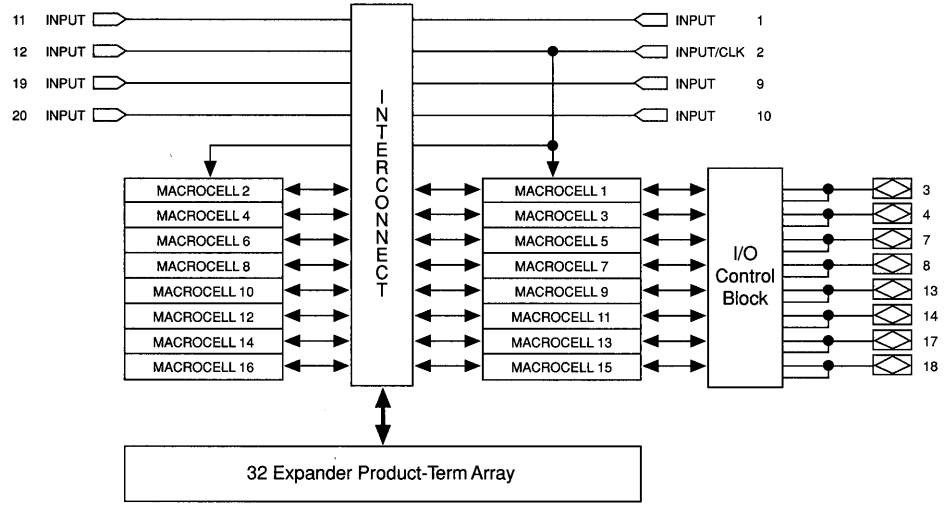
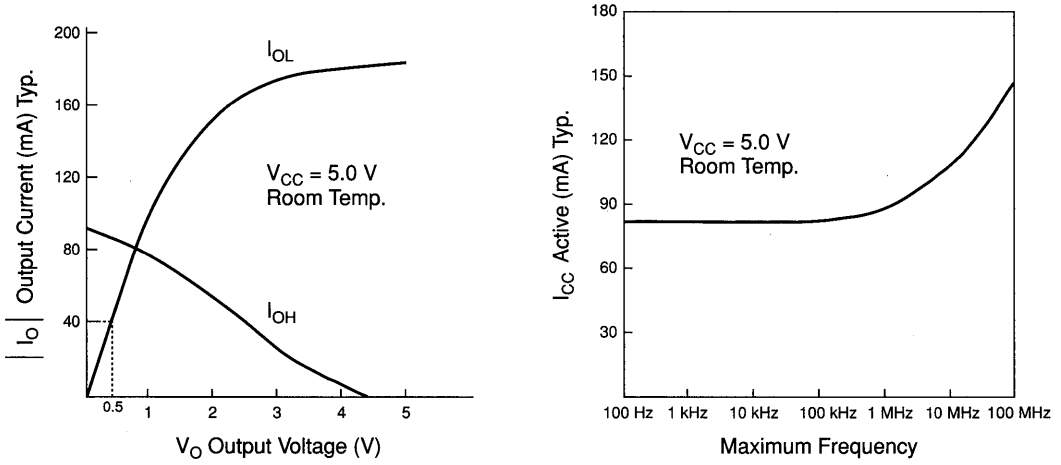


Figure 10 shows the output drive characteristics of EPM5016 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5016.

Figure 10. EPM5016 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			200	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (2), (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Note (5)*		80	110 (150)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Note (5)*		85	115 (175)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20	ns
t_{PD2}	I/O input to non-registered output			15		17		20	ns
t_{SU}	Global clock setup time		6		8		11		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		9		11		13	ns
t_{CH}	Global clock high time		5		6		8		ns
t_{CL}	Global clock low time		5		6		8		ns
t_{ASU}	Array clock setup time		4		5		6		ns
t_{AH}	Array clock hold time		4		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		13		15		18	ns
t_{ACH}	Array clock high time	*Note (6)*	4		5		7		ns
t_{ACL}	Array clock low time		6		7		9		ns
t_{CNT}	Minimum global clock period			10		12		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	100		83.3		62.5		MHz
t_{ACNT}	Minimum array clock period			10		12		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	100		83.3		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	100		83.3		62.5		MHz

Internal Timing Parameters *Note (8)*			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		4		4	ns
t_{IO}	I/O input pad and buffer delay			2		4		4	ns
t_{EXP}	Expander array delay			5		8		10	ns
t_{LAD}	Logic array delay			8		8		10	ns
t_{LAC}	Logic control array delay			4		5		7	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		5	ns
t_{ZX}	Output buffer enable delay			7		7		8	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		8	ns
t_{SU}	Register setup time		0		2		4		ns
t_{LATCH}	Flow-through latch delay			1		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{H}	Register hold time		6		6		7		ns
t_{IC}	Array clock delay			6		6		8	ns
t_{ICS}	Global clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		1	ns
t_{PRE}	Register preset time			5		6		6	ns
t_{CLR}	Register clear time			5		6		6	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.
(6) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5016-15, EPM5016-17, EPM5016-20
Industrial Temp.	(–40° C to 85° C)	EPM5016-20
Military Temp.	(–55° C to 125° C)	Consult factory

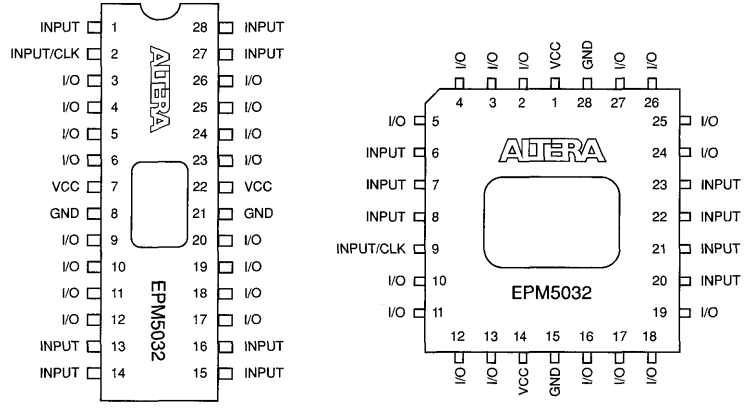
Notes:

Features

- High-speed, single-LAB MAX 5000 EPLD
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 77 MHz
  - Pipelined data rates up to 83 MHz
- 32 individually configurable macrocells
- 64 shareable expander product terms ("expanders") allowing 68 product terms on a single macrocell
- Programmable I/O architecture allowing up to 24 inputs or 16 outputs
- Available in 28-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 11):
  - Dual in-line (CerDIP and PDIP)
  - J-lead chip carrier (JLCC and PLCC)

Figure 11. EPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



General Description

The Altera EPM5032 EPLD is a MAX 5000 EPLD optimized for speed. It can integrate multiple SSI and MSI TTL and CMOS logic devices. In addition, the EPM5032 can replace multiple 20-pin PAL or PLA devices with logic left over for further integration. The EPM5032 contains 32 macrocells; the expander product-term array provides 64 expanders. The I/O control block contains 16 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility. See Figure 12.

Figure 12. EPM5032 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

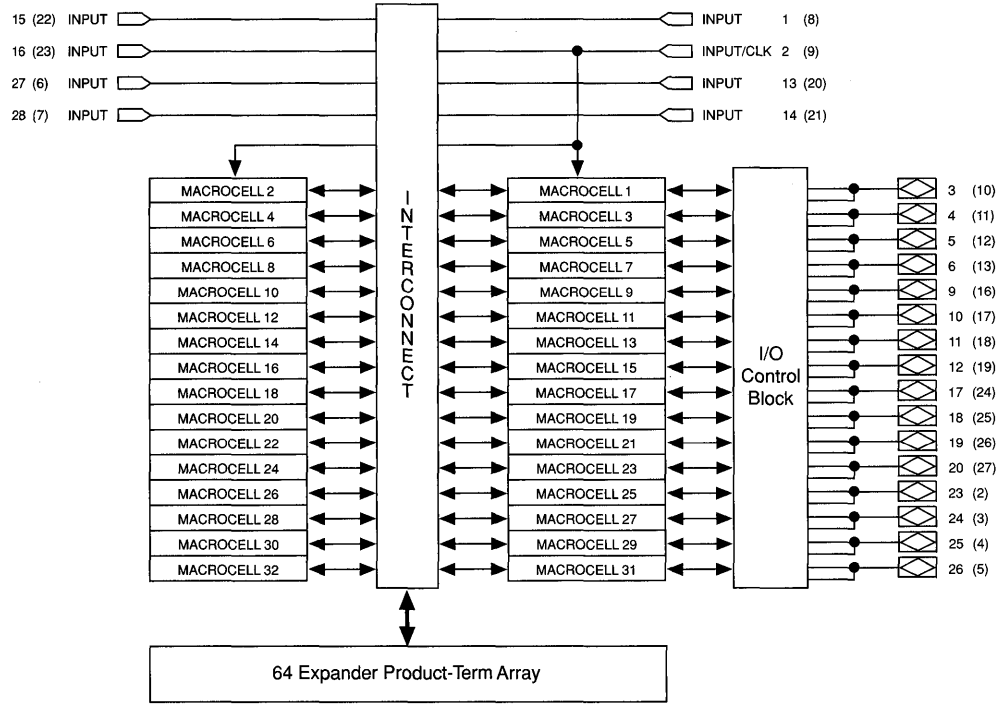
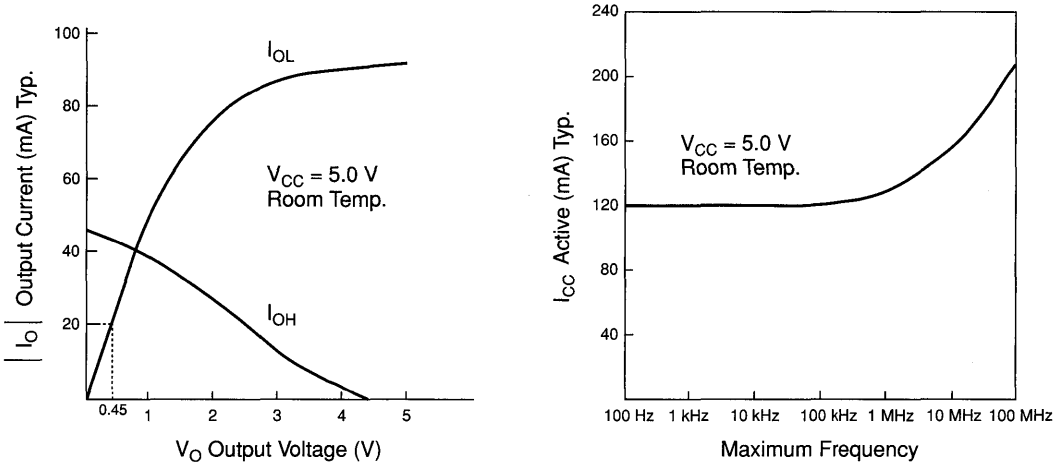


Figure 13 shows the output drive characteristics of EPM5032 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5032.

Figure 13. EPM5032 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	150 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, *Notes (3), (6)*		120	150 (200)	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (3), (6)*		125	155 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{PD2}	I/O input to non-registered output			15		17		20		25	ns
t_{SU}	Global clock setup time		9		10		12		15		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		10		12		15	ns
t_{CH}	Global clock high time		6		6		7		8		ns
t_{CL}	Global clock low time		6		6		7		8		ns
t_{ASU}	Array clock setup time		5		5		6		8		ns
t_{AH}	Array clock hold time		5		5		6		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		18		22	ns
t_{ACH}	Array clock high time	*Note (7)*	6		6		7		9		ns
t_{ACL}	Array clock low time		7		8		9		11		ns
t_{CNT}	Minimum global clock period			13		14		16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	76.9		71.4		62.5		50		MHz
t_{ACNT}	Minimum array clock period			13		14		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	76.9		71.4		62.5		50		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	83.3		83.3		71.4		62.5		MHz

Internal Timing Parameters *Note (9)*			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		3		5		7	ns
t_{IO}	I/O input pad and buffer delay			3		3		5		7	ns
t_{EXP}	Expander array delay			8		8		10		15	ns
t_{LAD}	Logic array delay			7		9		10		13	ns
t_{LAC}	Logic control array delay			4		4		4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		4		4	ns
t_{ZX}	Output buffer enable delay			7		7		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		7		7	ns
t_{SU}	Register setup time		4		3		4		5		ns
t_{LATCH}	Flow-through latch delay			1		1		1		1	ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{H}	Register hold time		5		7		8		10		ns
t_{IC}	Array clock delay			7		7		8		10	ns
t_{ICS}	Global clock delay			2		2		2		3	ns
t_{FD}	Feedback delay			1		1		1		1	ns
t_{PRE}	Register preset time			5		5		6		9	ns
t_{CLR}	Register clear time			5		5		6		9	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) Measured with a device programmed as a 32-bit counter. I_{CC} measured at 0° C.
(7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(8) The f_{MAX} values represent the highest frequency for pipelined data.
(9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5032-15, EPM5032-17, EPM5032-20, EPM5032-25
Industrial Temp.	(–40° C to 85° C)	EPM5032-25
Military Temp.	(–55° C to 125° C)	EPM5032-25
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

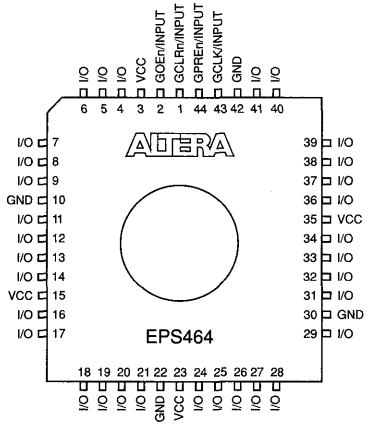
Features

For detailed information, refer to "EPS464 EPLD" in this data sheet.

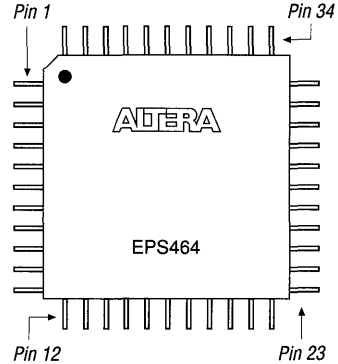
- High-performance, globally-routed, general-purpose EPLD
  - Combinatorial speeds as fast as 20 ns
  - Counter frequencies up to 67 MHz
  - Pipelined data rates up to 71 MHz
- 64 enhanced macrocells and 256 shared expander product terms ("expanders"); ideal for custom waveform generation and state machine designs
- Programmable registers providing D, T, JK, and SR flipflops with individual Clear, Preset, and Clock controls
- Powerful macrocell architecture optimized for:
  - Modulo-*n* binary and Gray-code counters
  - Complex state machines
  - Multiple product-term JK flipflops for waveform generation
  - Phase comparator and Clock oscillator functions
- Noise-resistant input buffers with 250-mV hysteresis and quiet output buffers for noise immunity and reliable operation
- Programmable Security Bit for total protection of proprietary designs
- Programmable I/O support for up to 36 inputs or 32 outputs
- Available in 44-pin windowed ceramic and one-time-programmable (OTP) packages (see Figure 14):
  - J-lead chip carrier (JLCC and PLCC)
  - Quad flat pack (plastic PQFP only)

Figure 14. EPS464 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 11 in this data sheet for QFP pin-out information. Windows in ceramic packages only.



44-Pin J-Lead



44-Pin QFP

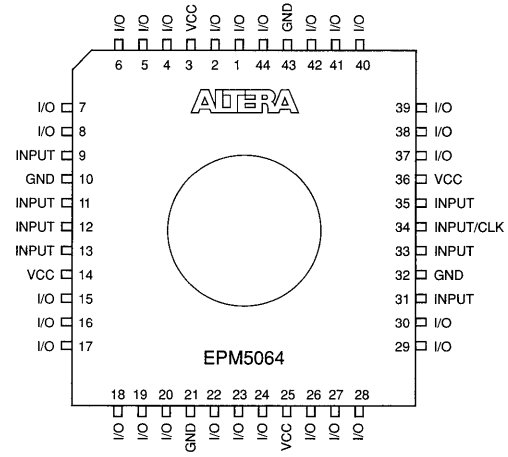
Notes:

Features

- High-density, 64-macrocell, general-purpose MAX 5000 EPLD
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 63 MHz
- 128 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 36 inputs or 28 outputs
- Available in 44-pin windowed ceramic and one-time-programmable (OTP) J-lead chip carrier packages (JLCC and PLCC). See Figure 15.
- Easy integration of 10 standard PALs in ½ square inch of board space

Figure 15. EPM5064 Package Pin-Out Diagram

Package outline not drawn to scale. Windows in ceramic packages only.



44-Pin J-Lead

General Description

The Altera EPM5064 EPLD is a user-configurable, high-performance MAX 5000 EPLD that serves as a high-density replacement for 74-series SSI and MSI TTL and CMOS logic. In addition, the EPM5064 can integrate multiple 20- and 24-pin low-density PLDs. For example, the EPM5064 can integrate the logic contained in over 10 standard 20-pin PALs.

The EPM5064 consists of 64 macrocells equally divided into 4 Logic Array Blocks (LABs) with 16 macrocells. Each LAB also contains 32 expander product terms. The EPM5064 has 8 dedicated input pins, one of which can be used as a global system Clock that provides enhanced Clock-to-output

delays. The device has 28 I/O pins that can be configured for input, output, or bidirectional operation. All I/O pins feature dual-feedback for maximum pin flexibility. Two of the LABs have 8 I/O pins, ensuring high speed for 8-bit bus functions; the other two LABs have 6 I/O pins. See Figure 16.

Figure 16. EPM5064 Block Diagram

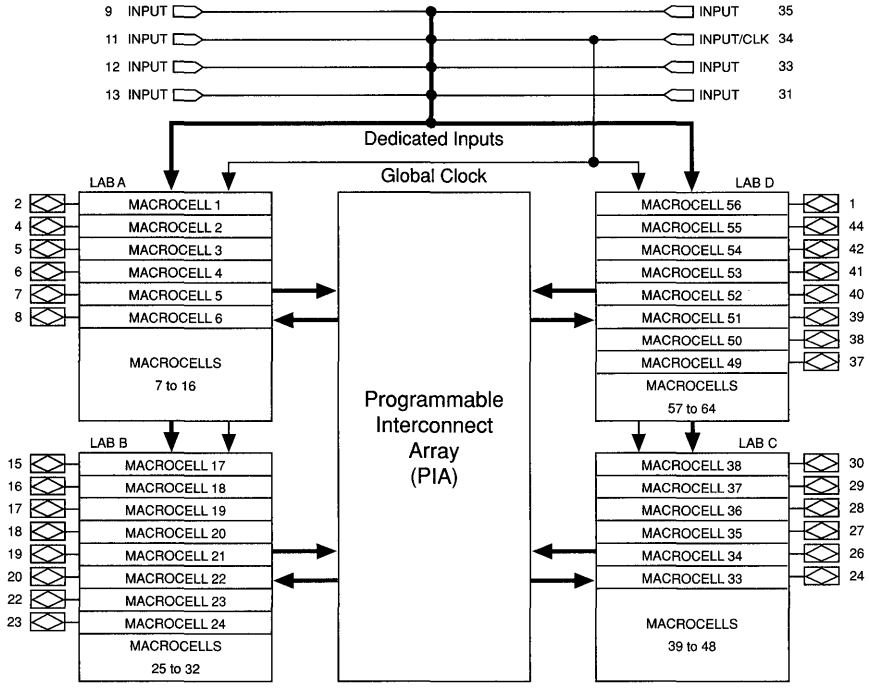
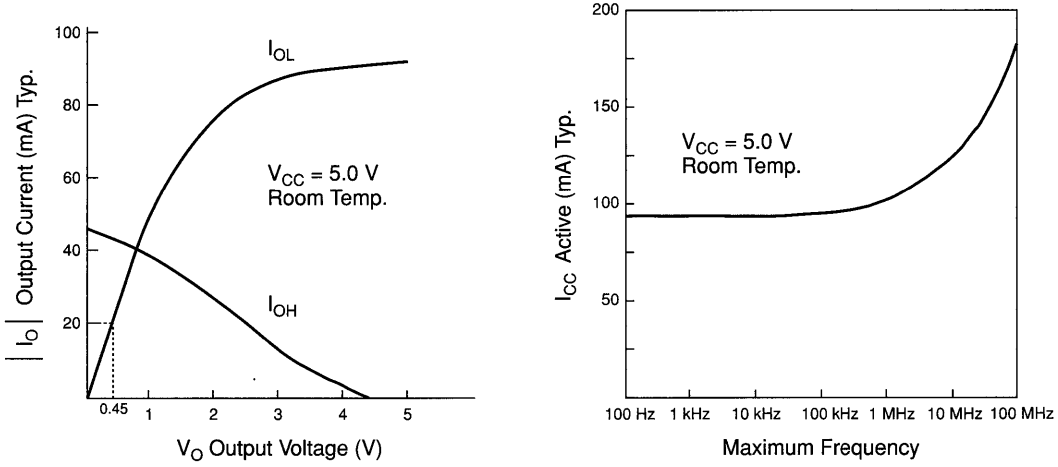


Figure 17 shows the output drive characteristics of EPM5064 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5064. The high integration density of the EPM5064 can greatly reduce system power requirements.

Figure 17. EPM5064 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, *Notes (2), (5)*		90	125 (200)	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (2), (5)*		95	135 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (6)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (7)*	62.5		50		40		MHz

Internal Timing Parameters *Note (8)*			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(6) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

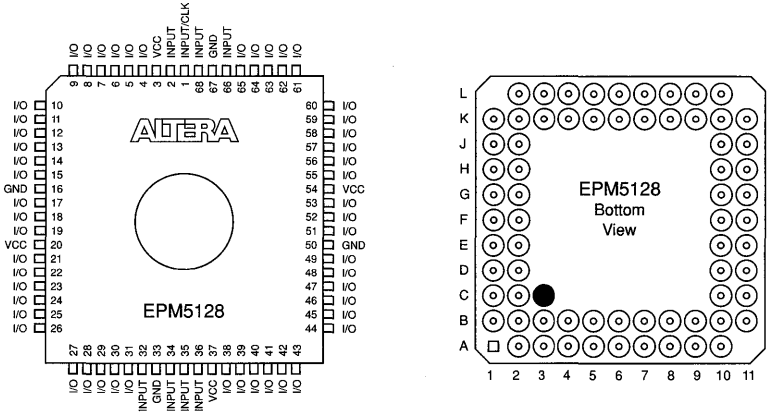
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5064-1, EPM5064-2, EPM5064
Industrial Temp.	(–40° C to 85° C)	EPM5064
Military Temp.	(–55° C to 125° C)	EPM5064

Features

- High-density, 128-macrocell, general-purpose MAX 5000 EPLD
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- 256 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in 68-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 18):
  - J-lead chip carrier (JLCC and PLCC)
  - Pin-grid array (ceramic PGA only)

Figure 18. EPM5128 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 3 and 4 in this data sheet for pin-out information. Windows in ceramic packages only.



68-Pin J-Lead 68-Pin PGA

General Description

The Altera EPM5128 EPLD is a user-configurable, high-performance MAX 5000 EPLD that provides a high-density replacement for 74-series SSI and MSI TTL and CMOS logic. For example, a `74161` counter uses only 3% of the EPM5128 EPLD. The EPM5128 can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs.

The EPM5128 consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs) with 16 macrocells. Each LAB also contains 32 expander product terms. The EPM5128 has 8 dedicated input pins, one of which can be used as a global system Clock. The EPM5128 contains 52 I/O pins that

can be configured for input, output, or bidirectional operation. Four of the LABs have 8 I/O pins; the other 4 have 5 I/O pins. See Figure 19.

Figure 19. EPM5128 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages.

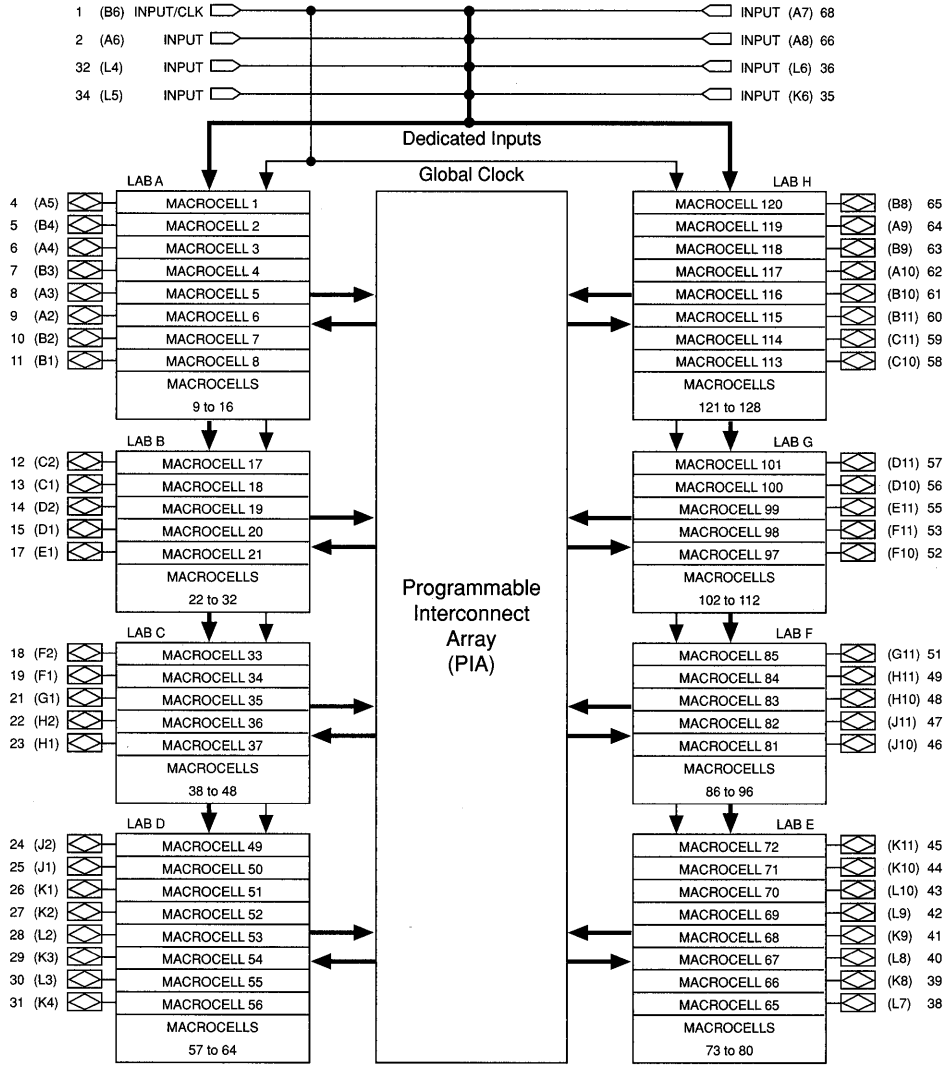
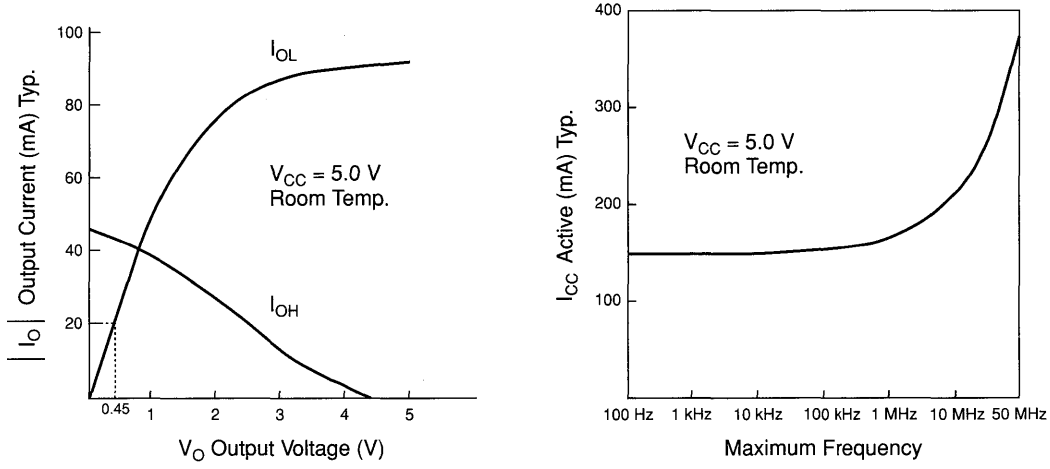


Figure 20 shows the output drive characteristics of EPM5128 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5128.

Figure 20. EPM5128 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (6)*		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (3), (6)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (7)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	62.5		50		40		MHz

Internal Timing Parameters *Note (9)*			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(8) The f_{MAX} values represent the maximum frequency for pipelined data.
(9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5128-1, EPM5128-2, EPM5128
Industrial Temp.	(–40° C to 85° C)	EPM5128
Military Temp.	(–55° C to 125° C)	EPM5128
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Tables 3 and 4 provide pin-out information for the EPM5128.

Table 3. EPM5128 Dedicated Pin-Outs

Dedicated Pin	68-Pin J-Lead	68-Pin PGA
INPUT/CLK	1	B6
INPUT	2, 32, 34, 35, 36, 66, 68	A6, L4, L5, L6, K6, A8, A7
GND	16, 33, 50, 67	B7, E2, G10, K5
VCC	3, 20, 37, 54	B5, E10, G2, K7

Table 4. EPM5128 I/O Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
1	A	4	A5	17	B	12	C2
2	A	5	B4	18	B	13	C1
3	A	6	A4	19	B	14	D2
4	A	7	B3	20	B	15	D1
5	A	8	A3	21	B	17	E1
6	A	9	A2	22	B	–	–
7	A	10	B2	23	B	–	–
8	A	11	B1	24	B	–	–
9	A	–	–	25	B	–	–
10	A	–	–	26	B	–	–
11	A	–	–	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	–	–	30	B	–	–
15	A	–	–	31	B	–	–
16	A	–	–	32	B	–	–
33	C	18	F2	49	D	24	J2
34	C	19	F1	50	D	25	J1
35	C	21	G1	51	D	26	K1
36	C	22	H2	52	D	27	K2
37	C	23	H1	53	D	28	L2
38	C	–	–	54	D	29	K3
39	C	–	–	55	D	30	L3
40	C	–	–	56	D	31	K4
41	C	–	–	57	D	–	–
42	C	–	–	58	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	–	–	62	D	–	–
47	C	–	–	63	D	–	–
48	C	–	–	64	D	–	–

Table 4. EPM5128 I/O Pin-Outs (Part 2 of 2)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
65	E	38	L7	81	F	46	J10
66	E	39	K8	82	F	47	J11
67	E	40	L8	83	F	48	H10
68	E	41	K9	84	F	49	H11
69	E	42	L9	85	F	51	G11
70	E	43	L10	86	F	–	–
71	E	44	K10	87	F	–	–
72	E	45	K11	88	F	–	–
73	E	–	–	89	F	–	–
74	E	–	–	90	F	–	–
75	E	–	–	91	F	–	–
76	E	–	–	92	F	–	–
77	E	–	–	93	F	–	–
78	E	–	–	94	F	–	–
79	E	–	–	95	F	–	–
80	E	–	–	96	F	–	–
97	G	52	F10	113	H	58	C10
98	G	53	F11	114	H	59	C11
99	G	55	E11	115	H	60	B11
100	G	56	D10	116	H	61	B10
101	G	57	D11	117	H	62	A10
102	G	–	–	118	H	63	B9
103	G	–	–	119	H	64	A9
104	G	–	–	120	H	65	B8
105	G	–	–	121	H	–	–
106	G	–	–	122	H	–	–
107	G	–	–	123	H	–	–
108	G	–	–	124	H	–	–
109	G	–	–	125	H	–	–
110	G	–	–	126	H	–	–
111	G	–	–	127	H	–	–
112	G	–	–	128	H	–	–

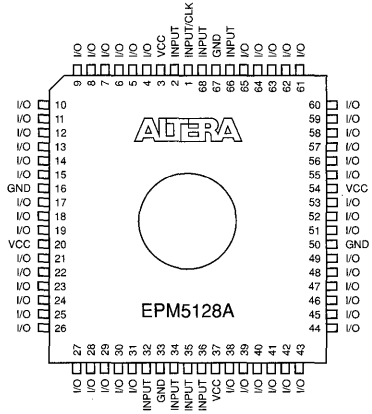
Features

Preliminary Information

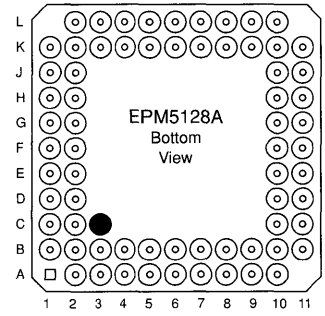
- High-density, second-generation MAX 5000 EPLD developed on an advanced 0.65-micron CMOS EPROM process
- Higher-speed upgrade for existing EPM5128 designs
- High-speed multi-LAB architecture
  - t_{PD} as fast as 12 ns
  - Counter frequencies up to 111 MHz
- 256 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- High-density replacement for 74-series SSI and MSI TTL and CMOS logic
- Available in 68-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 21):
  - J-lead chip carrier (JLCC and PLCC)
  - Pin-grid array (ceramic PGA only)

Figure 21. EPM5128A Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 3 and 4 in this data sheet for package pin-out information. Windows in ceramic packages only.



68-Pin J-Lead



68-Pin PGA

General Description

The Altera EPM5128A EPLD is a user-configurable, high-performance MAX 5000 EPLD that is pin-, function- and programming-file-compatible with the EPM5128. For a description of the device architecture, see "EPM5128 EPLD" in this data sheet.

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (2), (5)*		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (2), (5)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM5128A-12		EPM5128A-15		EPM5128A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			20		25		33	ns
t_{SU}	Global clock setup time		8		10		13		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		7		8	ns
t_{CH}	Global clock high time		4.5		5		7		ns
t_{CL}	Global clock low time		4.5		5		7		ns
t_{ASU}	Array clock setup time		4		5		6		ns
t_{AH}	Array clock hold time		4		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		11		13		16	ns
t_{ACH}	Array clock high time		4.5		5		7		ns
t_{ACL}	Array clock low time		4.5		5		7		ns
t_{CNT}	Minimum global clock period			9		12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	111.1		83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			9		12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	111.1		83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	111.1		100.0		71.4		MHz

Internal Timing Parameters *Note (7)*			EPM5128A-12		EPM5128A-15		EPM5128A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2.5		3		4	ns
t_{IO}	I/O input pad and buffer delay			2.5		3		4	ns
t_{EXP}	Expander array delay			6		8		10	ns
t_{LAD}	Logic array delay			6		8		12	ns
t_{LAC}	Logic control array delay			5		5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3		3	ns
t_{ZX}	Output buffer enable delay			5		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5		5	ns
t_{SU}	Register setup time		2		2		1		ns
t_{LATCH}	Flow-through latch delay			0.5		1		1	ns
t_{RD}	Register delay			0.5		1		1	ns
t_{COMB}	Combinatorial delay			0.5		1		1	ns
t_{H}	Register hold time		5		7		10		ns
t_{IC}	Array clock delay			5		6		8	ns
t_{ICS}	Global clock delay			0		0		0	ns
t_{FD}	Feedback delay			0.5		1		1	ns
t_{PRE}	Register preset time			3		3		3	ns
t_{CLR}	Register clear time			3		3		3	ns
t_{PIA}	Prog. Interconnect Array delay			8		10		13	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(6) The f_{MAX} values represent the maximum frequency for pipelined data.
(7) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	Consult factory
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

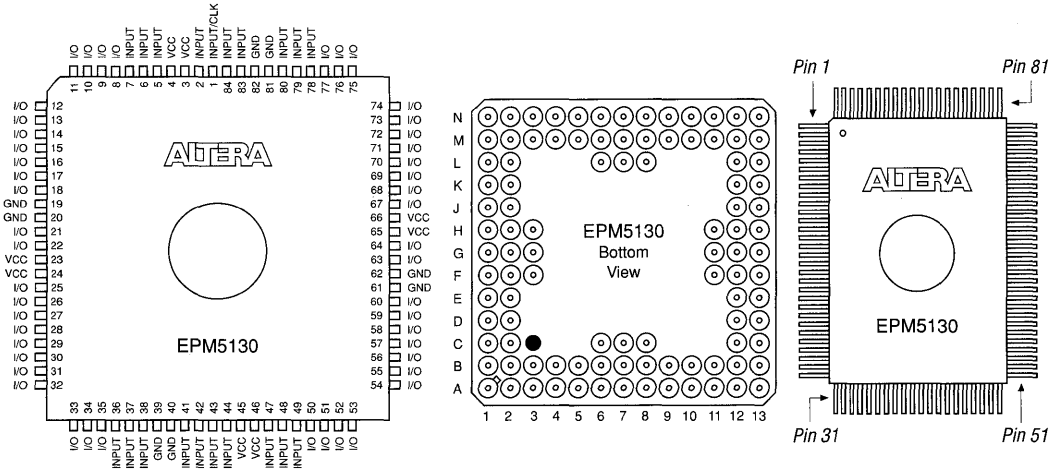
(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Features

- High-density, 128-macrocell, general-purpose MAX 5000 EPLD
- 128 macrocells optimized for pin-intensive applications, easily integrating over 60 TTL MSI and SSI components
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- High pin count for 16- or 32-bit data paths
- 256 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- 20 high-speed dedicated inputs for fast latching of 16-bit functions
- Fast Clock-to-output delays for bus-oriented functions
- Programmable I/O architecture allowing up to 84 inputs or 64 outputs in 100-pin packages, or up to 68 inputs or 48 outputs in 84-pin packages
- Available in windowed ceramic and one-time-programmable (OTP) packages (see Figure 22):
  - 84-pin J-lead chip carrier (JLCC and PLCC)
  - 100-pin pin-grid array (ceramic PGA only)
  - 100-pin quad flat pack (CQFP and PQFP)

Figure 22. EPM5130 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 5 and 6 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead 100-Pin PGA 100-Pin QFP

General Description

The Altera EPM5130 EPLD is a user-configurable, high-performance MAX 5000 EPLD optimized for pin-intensive designs. It provides a high-density replacement for 74-series SSI and MSI TTL and CMOS logic. A single EPM5130 EPLD can quickly integrate multiple 20- and 24-pin low-density PLDs and high-pin-count subsystems, such as custom DMA controllers. In addition, it can handle a 32-bit data path application with enough I/O to allow the required control signals to be implemented.

The EPM5130 consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs), each containing 16 macrocells and 32 expander product terms. Expander product terms can be used and shared by all macrocells in the device to ensure efficient use of device resources. Because the LAB is very compact, the high speeds required by most I/O subsystems are maintained. See Figure 23.

The EPM5130 has 20 dedicated input pins that allow high-speed input latching of 16-bit functions. One of these inputs can be configured as a global Clock to provide enhanced Clock-to-output delays for bus-oriented functions. The EPM5130 also has 64 I/O pins, 8 in each LAB, that can be configured for input, output, or bidirectional operation. Dual feedback on the I/O pins provides the most efficient use of device pin resources.

Figure 23. EPM5130 Block Diagram

Numbers without parentheses are for J-lead packages; numbers in parentheses are for PGA packages; numbers in brackets are for QFP packages.

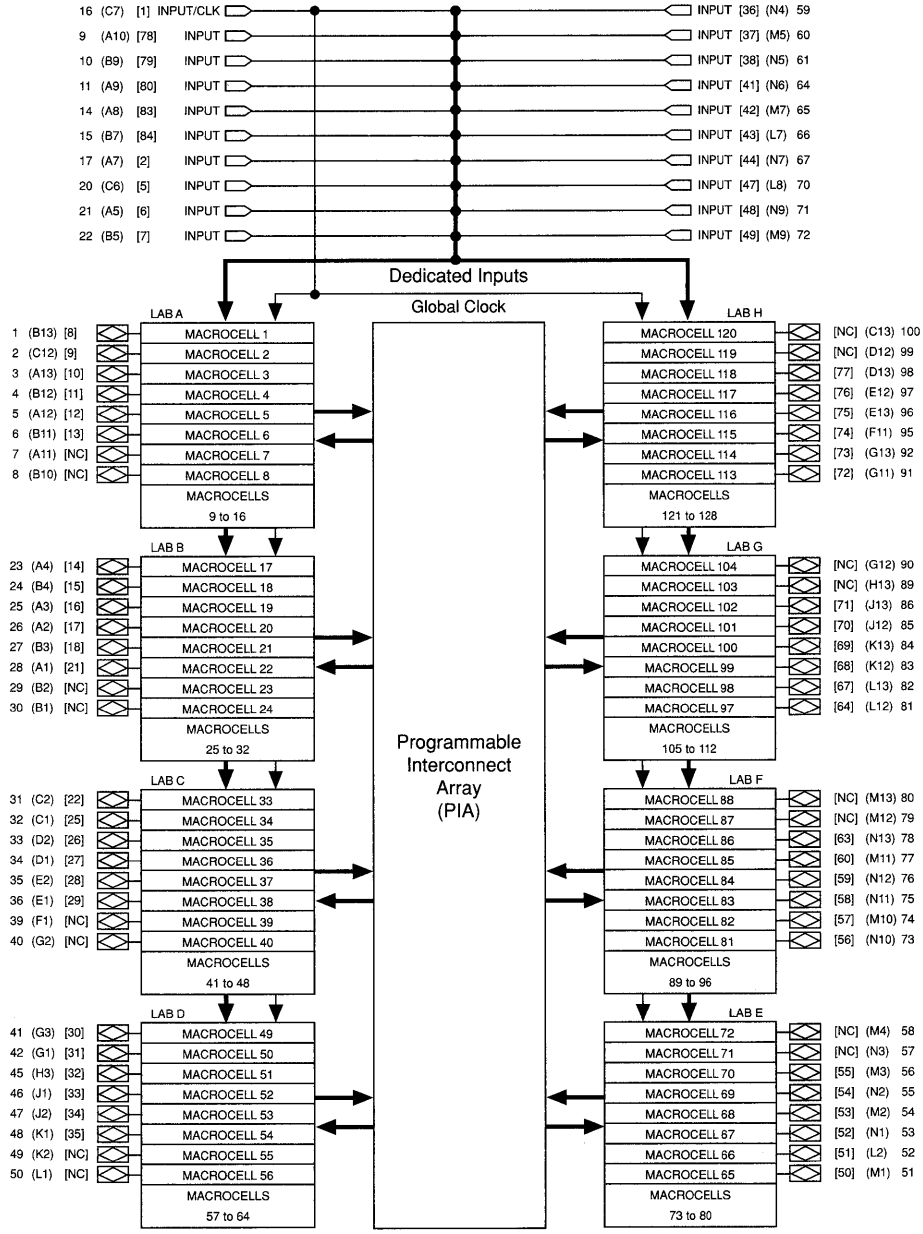
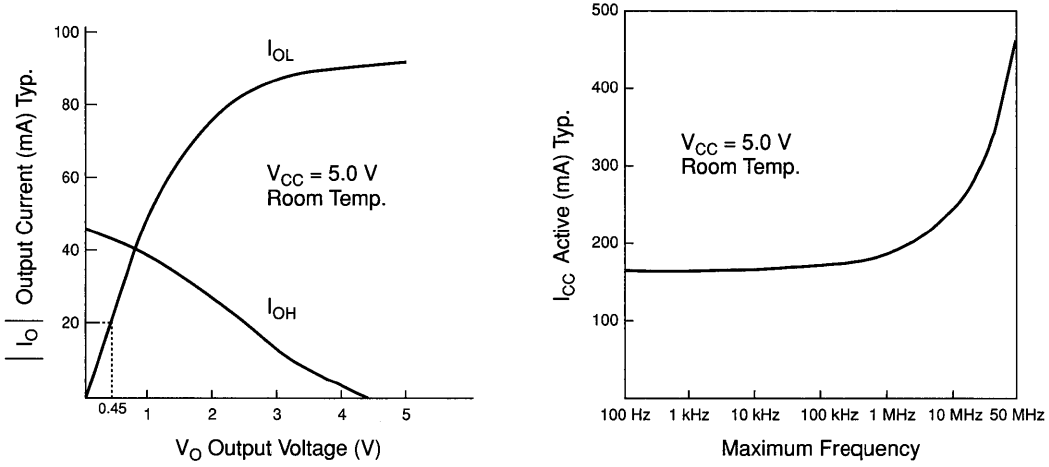


Figure 24 shows the output drive characteristics of EPM5130 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5130.

Figure 24. EPM5130 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (6)*		175	250 (325)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (3), (6)*		180	275 (375)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (7)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	62.5		50		40		MHz

Internal Timing Parameters *Note (9)*			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(8) The f_{MAX} values represent the highest frequency for pipelined data.
(9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5130-1, EPM5130-2, EPM5130
Industrial Temp.	(–40° C to 85° C)	EPM5130
Military Temp.	(–55° C to 125° C)	EPM5130
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Tables 5 and 6 provide pin-out information for the EPM5130.

Table 5. EPM5130 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
INPUT/CLK	1	C7	16
INPUT	2, 5, 6, 7, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 78, 79, 80, 83, 84	A5, A7, A8, A9, A10, B5, B7, B9, C6, L7, L8, M5, M7, M9, N4, N5, N6, N7, N9	9, 10, 11, 14, 15, 16, 17, 20, 21, 22, 59, 60, 61, 64, 65, 66, 67, 70, 71, 72
GND	19, 20, 39, 40, 61, 62, 81, 82	B8, C8, F2, F3, H11, H12, L6, M6	12, 13, 37, 38, 62, 63, 87, 88
VCC	3, 4, 23, 24, 45, 46, 65, 66	A6, B6, F12, F13, H1, H2, M8, N8	18, 19, 43, 44, 68, 69, 93, 94

Table 6. EPM5130 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
1	A	8	B13	1	17	B	14	A4	23
2	A	9	C12	2	18	B	15	B4	24
3	A	10	A13	3	19	B	16	A3	25
4	A	11	B12	4	20	B	17	A2	26
5	A	12	A12	5	21	B	18	B3	27
6	A	13	B11	6	22	B	21	A1	28
7	A	–	A11	7	23	B	–	B2	29
8	A	–	B10	8	24	B	–	B1	30
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	22	C2	31	49	D	30	G3	41
34	C	25	C1	32	50	D	31	G1	42
35	C	26	D2	33	51	D	32	H3	45
36	C	27	D1	34	52	D	33	J1	46
37	C	28	E2	35	53	D	34	J2	47
38	C	29	E1	36	54	D	35	K1	48
39	C	–	F1	39	55	D	–	K2	49
40	C	–	G2	40	56	D	–	L1	50
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

Table 6. EPM5130 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
65	E	50	M1	51	81	F	56	N10	73
66	E	51	L2	52	82	F	57	M10	74
67	E	52	N1	53	83	F	58	N11	75
68	E	53	M2	54	84	F	59	N12	76
69	E	54	N2	55	85	F	60	M11	77
70	E	55	M3	56	86	F	63	N13	78
71	E	–	N3	57	87	F	–	M12	79
72	E	–	M4	58	88	F	–	M13	80
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	64	L12	81	113	H	72	G11	91
98	G	67	L13	82	114	H	73	G13	92
99	G	68	K12	83	115	H	74	F11	95
100	G	69	K13	84	116	H	75	E13	96
101	G	70	J12	85	117	H	76	E12	97
102	G	71	J13	86	118	H	77	D13	98
103	G	–	H13	89	119	H	–	D12	99
104	G	–	G12	90	120	H	–	C13	100
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

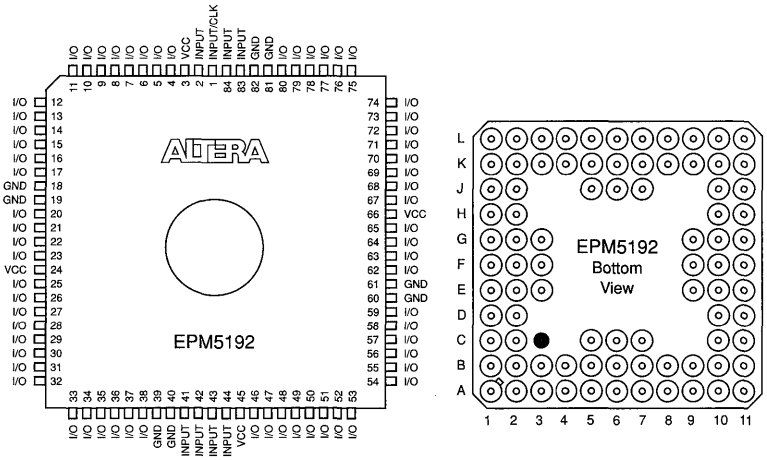
Notes:

Features

- High-density, 192 macrocell, general-purpose MAX 5000 EPLD, easily integrating complete logic boards into a single package
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- 384 shareable expander product terms ("expanders") offering flexibility for register and combinatorial logic expansion
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs, and I/O tri-state buffers that facilitate connections to system buses
- Available in 84-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 25):
  - J-lead chip carrier (JLCC and PLCC)
  - Pin-grid array (ceramic PGA only)

Figure 25. EPM5192 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 7 and 8 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead

84-Pin PGA

General Description

The Altera EPM5192 is a user-configurable, high-performance MAX 5000 EPLD that provides a high-density replacement for 74-series SSI and MSI TTL and CMOS logic. It can replace over 100 TTL SSI and MSI components and integrate the logic of over 20 22V10 devices. The EPM5192 consists of 192 macrocells equally divided into 12 Logic Array Blocks (LABs), each with 16 macrocells and 32 expanders. These compact LABs maintain high performance and efficient use of device resources. The EPM5192 has 8 dedicated input pins, one of which can be used as a global Clock. It can mix global and array clocking, facilitating easy integration of multiple subsystems. The EPM5192 contains 64 I/O pins that can be configured for input, output, or bidirectional operation, providing an interface to high-speed, bus-oriented applications. See Figure 26.

Figure 26. EPM5192 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages. Numbers in brackets are for EPM5192A QFP packages.

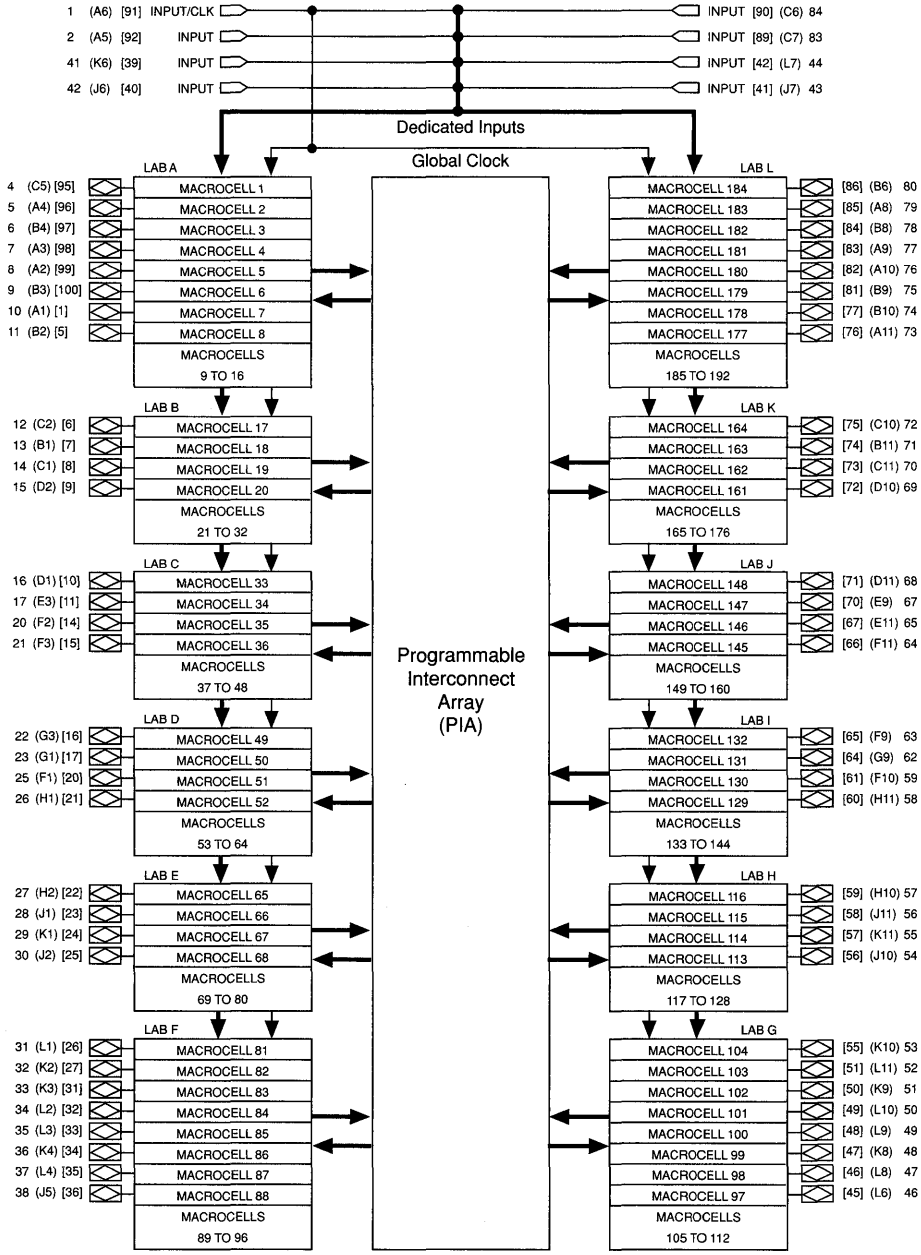
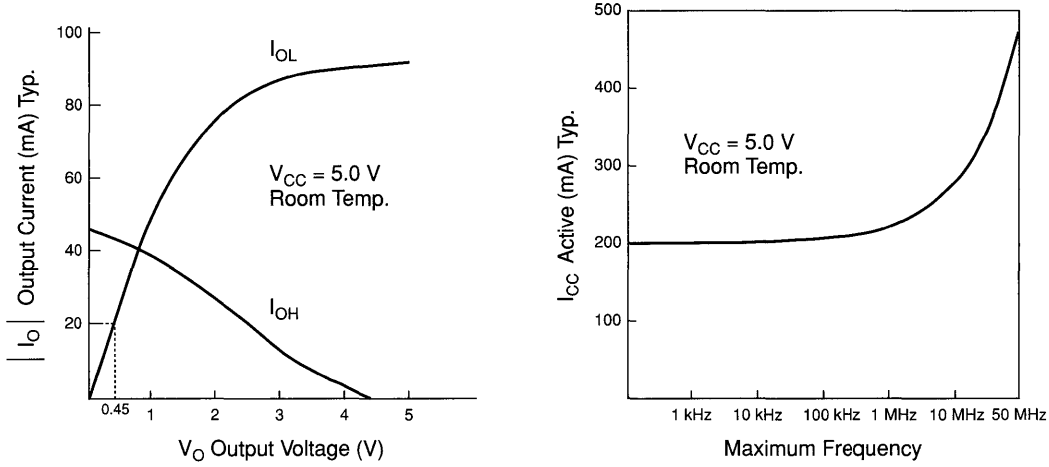


Figure 27 shows the output drive characteristics of EPM5192 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5192.

Figure 27. EPM5192 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	4.75 (5.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (6)*		250	360 (435)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (3), (6)*		270	380 (480)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (7)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	62.5		50		40		MHz

Internal Timing Parameters *Note (9)*			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(8) The f_{MAX} values represent the highest frequency for pipelined data.
(9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5192-1, EPM5192-2, EPM5192
Industrial Temp.	(–40° C to 85° C)	EPM5192
Military Temp.	(–55° C to 125° C)	EPM5192
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Tables 7 and 8 provide pin-out information for the EPM5192.

Table 7. EPM5192 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	84-Pin PGA
INPUT/CLK	1	A6
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5
VCC	3, 24, 45, 66	B5, E10, G2, K7

Table 8. EPM5192 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
1	A	4	C5	17	B	12	C2	33	C	16	D1
2	A	5	A4	18	B	13	B1	34	C	17	E3
3	A	6	B4	19	B	14	C1	35	C	20	F2
4	A	7	A3	20	B	15	D2	36	C	21	F3
5	A	8	A2	21	B	–	–	37	C	–	–
6	A	9	B3	22	B	–	–	38	C	–	–
7	A	10	A1	23	B	–	–	39	C	–	–
8	A	11	B2	24	B	–	–	40	C	–	–
9	A	–	–	25	B	–	–	41	C	–	–
10	A	–	–	26	B	–	–	42	C	–	–
11	A	–	–	27	B	–	–	43	C	–	–
12	A	–	–	28	B	–	–	44	C	–	–
13	A	–	–	29	B	–	–	45	C	–	–
14	A	–	–	30	B	–	–	46	C	–	–
15	A	–	–	31	B	–	–	47	C	–	–
16	A	–	–	32	B	–	–	48	C	–	–
49	D	22	G3	65	E	27	H2	81	F	31	L1
50	D	23	G1	66	E	28	J1	82	F	32	K2
51	D	25	F1	67	E	29	K1	83	F	33	K3
52	D	26	H1	68	E	30	J2	84	F	34	L2
53	D	–	–	69	E	–	–	85	F	35	L3
54	D	–	–	70	E	–	–	86	F	36	K4
55	D	–	–	71	E	–	–	87	F	37	L4
56	D	–	–	72	E	–	–	88	F	38	J5
57	D	–	–	73	E	–	–	89	F	–	–
58	D	–	–	74	E	–	–	90	F	–	–
59	D	–	–	75	E	–	–	91	F	–	–
60	D	–	–	76	E	–	–	92	F	–	–
61	D	–	–	77	E	–	–	93	F	–	–
62	D	–	–	78	E	–	–	94	F	–	–
63	D	–	–	79	E	–	–	95	F	–	–
64	D	–	–	80	E	–	–	96	F	–	–

Table 8. EPM5192 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
97	G	46	L6	113	H	54	J10	129	I	58	H11
98	G	47	L8	114	H	55	K11	130	I	59	F10
99	G	48	K8	115	H	56	J11	131	I	62	G9
100	G	49	L9	116	H	57	H10	132	I	63	F9
101	G	50	L10	117	H	–	–	133	I	–	–
102	G	51	K9	118	H	–	–	134	I	–	–
103	G	52	L11	119	H	–	–	135	I	–	–
104	G	53	K10	120	H	–	–	136	I	–	–
105	G	–	–	121	H	–	–	137	I	–	–
106	G	–	–	122	H	–	–	138	I	–	–
107	G	–	–	123	H	–	–	139	I	–	–
108	G	–	–	124	H	–	–	140	I	–	–
109	G	–	–	125	H	–	–	141	I	–	–
110	G	–	–	126	H	–	–	142	I	–	–
111	G	–	–	127	H	–	–	143	I	–	–
112	G	–	–	128	H	–	–	144	I	–	–
145	J	64	F11	161	K	69	D10	177	L	73	A11
146	J	65	E11	162	K	70	C11	178	L	74	B10
147	J	67	E9	163	K	71	B11	179	L	75	B9
148	J	68	D11	164	K	72	C10	180	L	76	A10
149	J	–	–	165	K	–	–	181	L	77	A9
150	J	–	–	166	K	–	–	182	L	78	B8
151	J	–	–	167	K	–	–	183	L	79	A8
152	J	–	–	168	K	–	–	184	L	80	B6
153	J	–	–	169	K	–	–	185	L	–	–
154	J	–	–	170	K	–	–	186	L	–	–
155	J	–	–	171	K	–	–	187	L	–	–
156	J	–	–	172	K	–	–	188	L	–	–
157	J	–	–	173	K	–	–	189	L	–	–
158	J	–	–	174	K	–	–	190	L	–	–
159	J	–	–	175	K	–	–	191	L	–	–
160	J	–	–	176	K	–	–	192	L	–	–

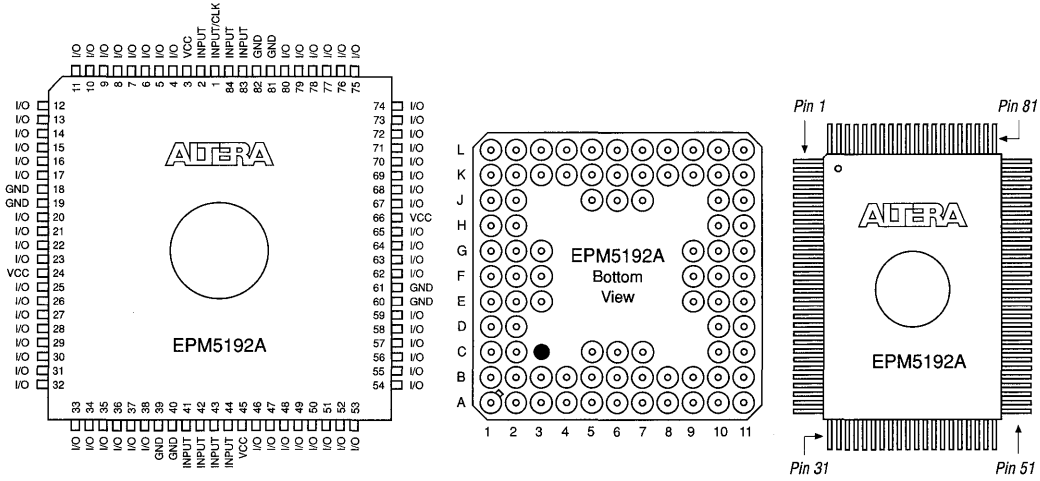
Features

Preliminary Information

- High-performance, second-generation MAX 5000 EPLD developed on an advanced 0.65-micron CMOS EPROM process
- High-speed upgrade for existing EPM5192 designs
- High-speed multi-LAB architecture
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 83.3 MHz
- 384 shareable expander product terms ("expanders") offering flexibility for register and combinatorial logic expansion
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs
- High-density replacement for 74-series SSI and MSI TTL and CMOS logic
- Available in windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 28):
  - 84-pin J-lead chip carrier (JLCC and PLCC)
  - 84-pin pin-grid array (ceramic PGA only)
  - 100-pin quad flat pack (plastic PQFP only)

Figure 28. EPM5192A Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 9 and 10 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead 84-Pin PGA 100-Pin QFP

General Description

The Altera EPM5192A EPLD is a user-configurable, high-performance MAX 5000 EPLD that is pin-, function- and programming-file-compatible with the EPM5192. For a description of the device architecture, see "EPM5192 EPLD" in this data sheet.

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Note (5)*		180	225	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Note (5)*		200	245	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EPM5192A-15		EPM5192A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output			25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		7		8	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		13		16	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (5)*	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (5)*	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	100.0		71.4		MHz

Internal Timing Parameters *Note (7)*			EPM5192A-15		EPM5192A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{EXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay			5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Prog. Interconnect Array delay			10		13	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(5) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(6) The f_{MAX} values represent the maximum frequency for pipelined data.
(7) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	Consult factory
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Tables 9 and 10 provide pin-out information for the EPM5192A.

Table 9. EPM5192A Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
INPUT/CLK	1	A6	91
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6	39, 40, 41, 42
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5	2, 3, 4, 12, 13, 28, 29, 30, 37, 38, 52, 53, 54, 62, 63, 78, 79, 80, 87, 88
VCC	3, 24, 45, 66	B5, E10, G2, K7	18, 44, 68, 69, 93, 94

Table 10. EPM5192A I/O Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
1	A	4	C5	95	17	B	12	C2	6
2	A	5	A4	96	18	B	13	B1	7
3	A	6	B4	97	19	B	14	C1	8
4	A	7	A3	98	20	B	15	D2	9
5	A	8	A2	99	21	B	–	–	–
6	A	9	B3	100	22	B	–	–	–
7	A	10	A1	1	23	B	–	–	–
8	A	11	B2	5	24	B	–	–	–
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	16	D1	10	49	D	22	G3	16
34	C	17	E3	11	50	D	23	G1	17
35	C	20	F2	14	51	D	25	F1	20
36	C	21	F3	15	52	D	26	H1	21
37	C	–	–	–	53	D	–	–	–
38	C	–	–	–	54	D	–	–	–
39	C	–	–	–	55	D	–	–	–
40	C	–	–	–	56	D	–	–	–
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

Table 10. EPM5192A I/O Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
65	E	27	H2	22	81	F	31	L1	26
66	E	28	J1	23	82	F	32	K2	27
67	E	29	K1	24	83	F	33	K3	31
68	E	30	J2	25	84	F	34	L2	32
69	E	–	–	–	85	F	35	L3	33
70	E	–	–	–	86	F	36	K4	34
71	E	–	–	–	87	F	37	L4	35
72	E	–	–	–	88	F	38	J5	36
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	46	L6	45	113	H	54	J10	56
98	G	47	L8	46	114	H	55	K11	57
99	G	48	K8	47	115	H	56	J11	58
100	G	49	L9	48	116	H	57	H10	59
101	G	50	L10	49	117	H	–	–	–
102	G	51	K9	50	118	H	–	–	–
103	G	52	L11	51	119	H	–	–	–
104	G	53	K10	55	120	H	–	–	–
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

Table 10. EPM5192A I/O Pin-Outs (Part 3 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
129	I	58	H11	60	145	J	64	F11	66
130	I	59	F10	61	146	J	65	E11	67
131	I	62	G9	64	147	J	67	E9	70
132	I	63	F9	65	148	J	68	D11	71
133	I	–	–	–	149	J	–	–	–
134	I	–	–	–	150	J	–	–	–
135	I	–	–	–	151	J	–	–	–
136	I	–	–	–	152	J	–	–	–
137	I	–	–	–	153	J	–	–	–
138	I	–	–	–	154	J	–	–	–
139	I	–	–	–	155	J	–	–	–
140	I	–	–	–	156	J	–	–	–
141	I	–	–	–	157	J	–	–	–
142	I	–	–	–	158	J	–	–	–
143	I	–	–	–	159	J	–	–	–
144	I	–	–	–	160	J	–	–	–
161	K	69	D10	72	177	L	73	A11	76
162	K	70	C11	73	178	L	74	B10	77
163	K	71	B11	74	179	L	75	B9	81
164	K	72	C10	75	180	L	76	A10	82
165	K	–	–	–	181	L	77	A9	83
166	K	–	–	–	182	L	78	B8	84
167	K	–	–	–	183	L	79	A8	85
168	K	–	–	–	184	L	80	B6	86
169	K	–	–	–	185	L	–	–	–
170	K	–	–	–	186	L	–	–	–
171	K	–	–	–	187	L	–	–	–
172	K	–	–	–	188	L	–	–	–
173	K	–	–	–	189	L	–	–	–
174	K	–	–	–	190	L	–	–	–
175	K	–	–	–	191	L	–	–	–
176	K	–	–	–	192	L	–	–	–

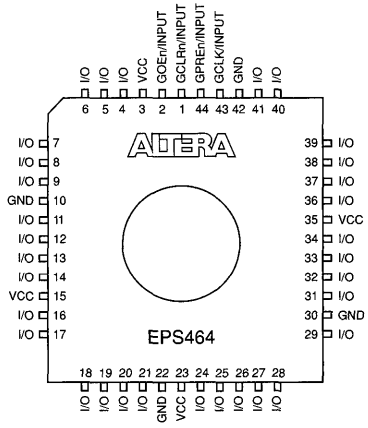
Notes:

Features

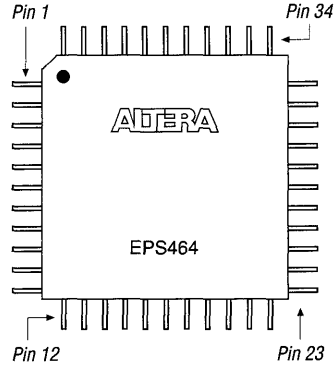
- High-performance, globally-routed, general-purpose EPLD
  - Combinatorial speeds as fast as 20 ns
  - Counter frequencies up to 67 MHz
  - Pipelined data rates up to 71 MHz
- 64 enhanced macrocells and 256 shared expander product terms ("expanders"); ideal for custom waveform generation and state machine designs
- Programmable registers providing D, T, JK, and SR flipflops with individual Clear, Preset, and Clock controls
- Powerful macrocell architecture optimized for:
  - Modulo-*n* binary and Gray-code counters
  - Complex state machines
  - Multiple product-term JK flipflops for waveform generation
  - Phase comparator and Clock oscillator functions
- Noise-resistant input buffers with 250-mV hysteresis and quiet output buffers for noise immunity and reliable operation
- Programmable Security Bit for total protection of proprietary designs
- Programmable I/O support for up to 36 inputs or 32 outputs
- Available in 44-pin windowed ceramic and one-time-programmable (OTP) packages (see Figure 29):
  - J-lead chip carrier (JLCC and PLCC)
  - Quad flat pack (plastic PQFP only)

Figure 29. EPS464 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 11 in this data sheet for QFP pin-out information. Windows in ceramic packages only.



44-Pin J-Lead



44-Pin QFP

General Description

The EPS464 is an general-purpose EPLD based on the MAX 5000 architecture. It combines innovative architecture and an advanced fabrication process to offer optimum performance and flexibility. Fabricated on a 0.8-micron CMOS EPROM technology, the EPS464 has 64 enhanced macrocells and 256 shared expanders, all of which are globally routed to implement complex designs.

The EPS464 provides an integrated solution for a wide range of applications. Because the EPS464 architecture supports 100% TTL emulation, it can integrate multiple SSI, MSI, and LSI logic functions into one device. It is also ideal for synchronous timing and waveform-generation applications, such as TV/video synchronization signals (e.g., NTSC, PAL, SECAM, HDTV), CCD timing controllers, high-performance state machines, and memory controllers. Each output can generate customized waveforms to meet various system requirements.

The EPS464 has 32 I/O pins that can be independently configured for input, output, or bidirectional operation. It also has 4 dedicated input pins that can be programmed as general-purpose inputs or as system-wide control signals (Clock, Clear, Preset, and Output Enable) for each macrocell and I/O pin. The EPS464 input pins have input protection circuitry to prevent electrostatic discharge (ESD) damage and to reduce the possibility of latch-up. The input pins also provide input hysteresis to prevent spurious switching due to noisy inputs. The outputs are designed to minimize output switching noise, offering quiet and reliable operation.

The EPS464 advanced macrocell structure can integrate complex logic functions, with over 100 product terms available to any one macrocell. Each of the 64 internal flipflops can be programmed for D, T, JK, or SR operation. JK and SR flipflops are well-suited for pattern-generation applications, since simple set and reset operations can be used to define the transitions of output waveforms.

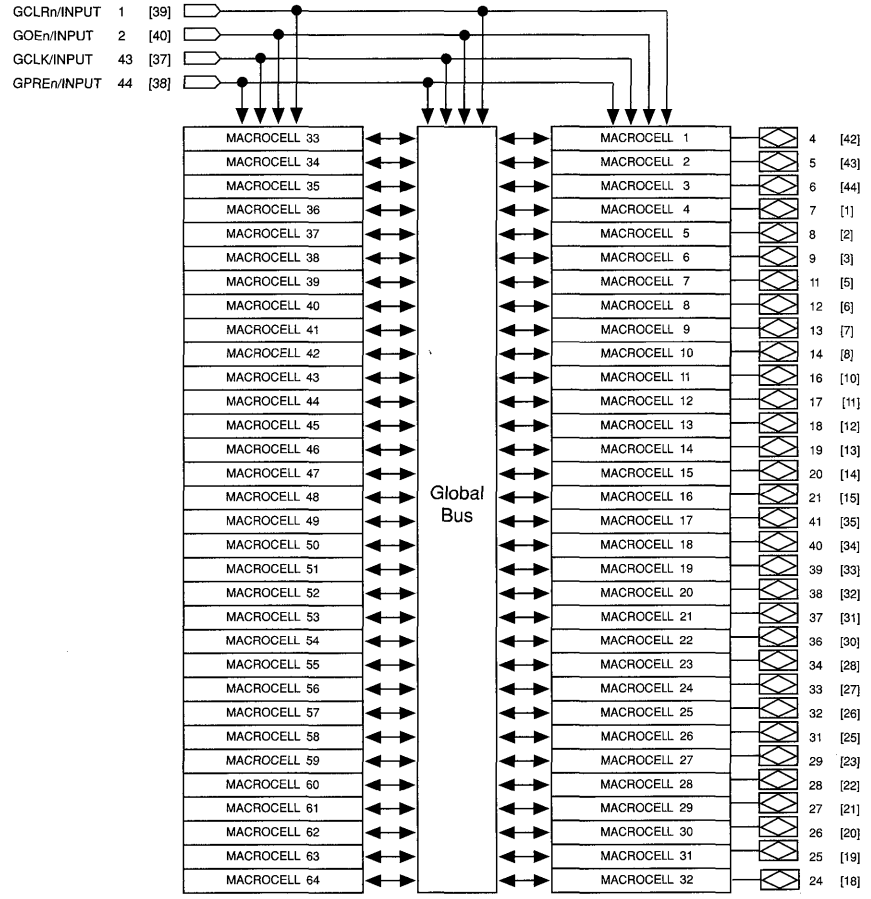
The EPS464 is supported by Altera's MAX+PLUS II development system, a single integrated package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and programming. MAX+PLUS II provides EDIF, VHDL, Verilog and other netlist interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. The system runs on 386- and 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations.

Functional Description

The EPS464 is a 64-macrocell EPLD optimized for timing and waveform synthesis applications. Thirty-two macrocells are connected to I/O pins; the other 32 macrocells are available for buried logic and state machine registers (see Figure 30). The high logic density and large number of macrocells allow designers to create multiple counters inside the EPS464 and to add state machines and combinatorial logic to enhance design integration.

Figure 30. EPS464 Block Diagram

Numbers without brackets are for J-lead packages. Numbers in brackets are for QFP packages.



All EPS464 macrocells are fed by a global bus, which supports 66-MHz system speeds and eliminates placement-dependent interconnect delays between device resources.

The EPS464 uses CMOS EPROM cells to configure all combinatorial and sequential logic functions in the device. It is user-configurable to accommodate a variety of independent logic blocks typically used in waveform generation and random-logic integration applications. The EPLDs can be erased for quick and efficient iterations during development and debug cycles.

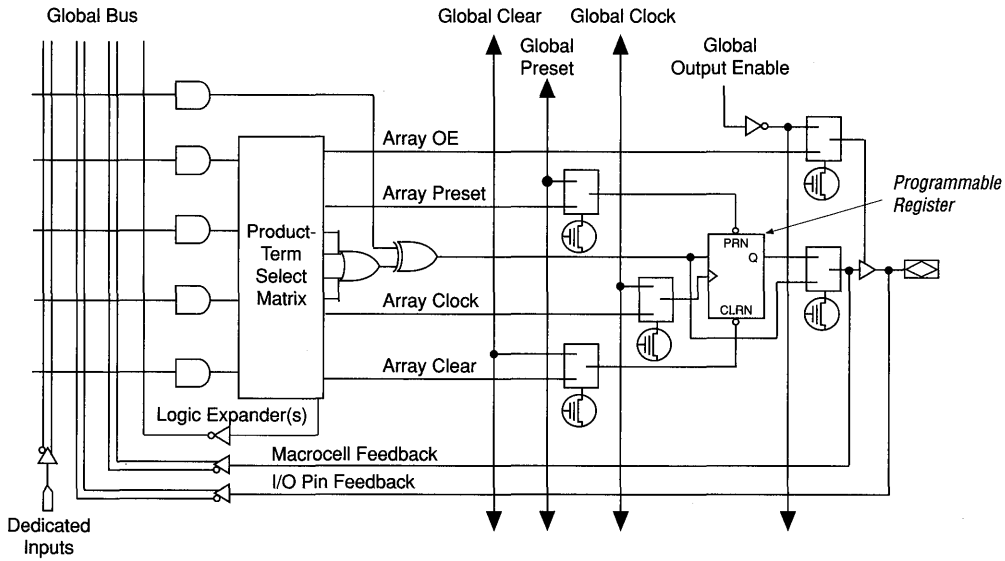
EPS464 architecture includes the following elements:

- Macrocells
- Expander product terms
- I/O control block

Macrocells

The EPS464 macrocell, shown in Figure 31, consists of three functional blocks: a product-term array, a product-term select matrix, and a programmable register.

Figure 31. EPS464 Macrocell



Combinatorial logic is implemented in the product-term array, which consists of five product terms. Four product terms feed the product-term select matrix; the fifth feeds one input of an XOR gate, making it possible to implement active-high or active-low logic. The XOR gate is also used to build complex arithmetic logic functions and to perform De Morgan's

inversion, which reduces the number of product terms required for a design.

Based on the logic requirements of the design, the product-term select matrix individually directs the macrocell's product-term resources to the four-input OR gate, the Clock, Clear, or Preset controls on the programmable register, the Output Enable controls on the I/O pins, or up to four expander product terms. The product-term select matrix can also connect VCC or GND to the control resources to permanently enable or disable logic functions.

Each programmable register can be configured as a D, T, JK, or SR flipflop and is positive-edge-triggered. Register types can be specified by the designer or by the MAX+PLUS II software, which automatically selects the most efficient flipflop type to implement a given logic function. The register can also be bypassed for fast combinatorial operation.

The macrocell's register control functions (Clock, Clear, and Preset) can be driven from product terms or from the dedicated input pins. Selection is made on an individual basis, ensuring efficient macrocell resource utilization. Connecting these control functions directly to the dedicated input pins GPREn, GCLRn, and GCLK guarantees fast operation. These control functions can also be generated with product terms to provide additional design flexibility.

Expander Product Terms

Although most logic functions can be implemented with the product terms available in each macrocell, some complex logic functions may require additional product terms. Rather than using additional macrocells to supply the needed logic resources, the EPS464 architecture uses shared expander product terms to provide additional product terms directly to any macrocell. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

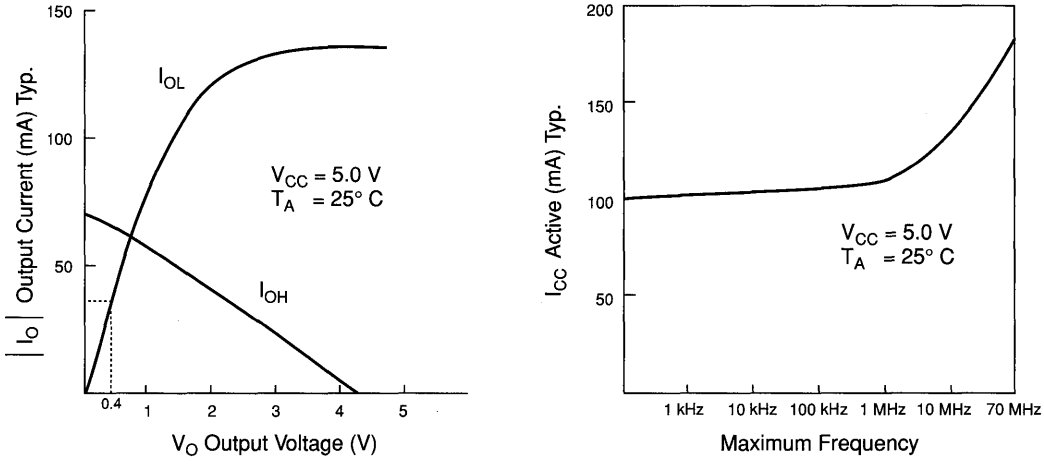
The EPS464 provides up to 256 logic expanders, which are inverted product terms that feed back into the global bus. Expanders are fed by all signals in the EPS464. Expanders can be used and shared by all product terms in the EPS464 to build complex logic functions, allowing the software to factor logic expressions and combine product terms efficiently. If the expanders are not used for combinatorial logic, they can be cross-coupled to build additional flipflops, latches, or input registers. This flexibility allows designers to fully use the silicon resources packed into each EPS464 device. A small delay (t_{SEXP}) is incurred when shared expanders are used.

I/O Control Block

The I/O control block consists of a user-configurable I/O control function for each I/O pin. The EPS464 has 32 I/O pins, each of which can be configured for input, output, or bidirectional operation. Each macrocell that feeds an I/O pin has a tri-state buffer between the macrocell output and the I/O pin. The EPS464 provides dual feedback, with feedback paths before and after the tri-state buffer; if an I/O pin is configured as an input, the associated macrocell is not wasted and can be used for buried logic. The Output Enable for each tri-state buffer can be controlled by the dedicated active-low global Output Enable input (GOEn), or by a product term within the macrocell.

Figure 32 shows the output drive characteristics of EPS464 I/O pins and typical supply current (I_{CC}) versus frequency for the EPS464 EPLD.

Figure 32. EPS464 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Design Security

The EPS464 contains a programmable Security Bit that controls access to the data programmed into the device. If the Security Bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when the device is erased.

Timing Model

Timing in the EPS464 EPLD can be analyzed with MAX+PLUS II software, with a variety of popular industry-standard CAE simulators and timing analyzers, or with the timing model shown in Figure 33. The actual values for each parameter given in the "AC Operating Conditions" table in this

data sheet. The EPS464 has fixed internal delays that allow the user to determine the worst-case timing for any design. The individual delays are predetermined and are not dependent on routing or layout considerations. For complete timing information, MAX+PLUS II provides a timing simulator with 0.1-ns resolution, delay prediction for point-to-point delay calculation, and a detailed timing analyzer.

Figure 33. EPS464 Timing Model

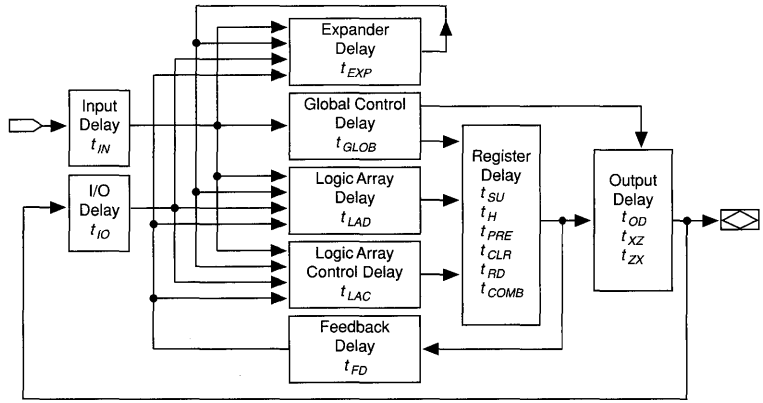
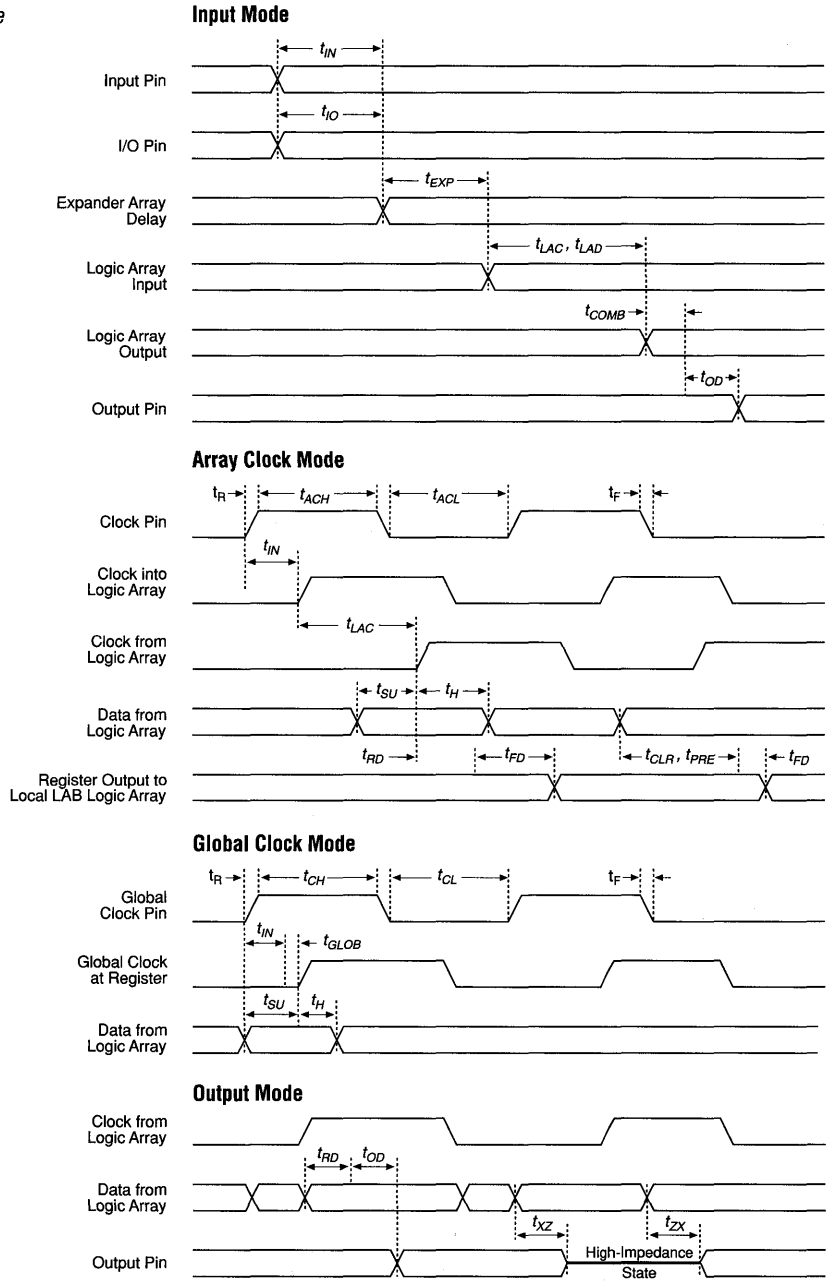


Figure 34 shows the switching waveforms for EPS464 devices.

For more information, see *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Figure 34. EPS464 Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

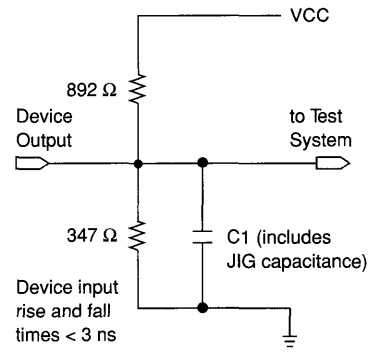


Generic Testing

EPS464 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are performed under conditions equivalent to those shown in Figure 35.

Figure 35. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



MAX+PLUS II Development System

EPS464 EPLDs are supported by the MAX+PLUS II development system, a completely integrated environment for design entry, compilation, verification, and programming. MAX+PLUS II software is available for 386- and 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations. All platforms include more than 300 74-series macrofunctions and the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, conditional logic, and truth table entry methods. MAX+PLUS II also provides highly automated compilation, automatic multi-device partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a comprehensive on-line help system.

In addition, MAX+PLUS II imports and exports industry-standard EDIF 2 0 0 and 2 9 0 and other netlist files for a convenient interface to industry-standard CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic. MAX+PLUS II also exports Verilog and VHDL netlist files that support simulation with other industry-standard simulators. For further details about MAX+PLUS II and other CAE tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and *CAE Software Support* in this data book.

Device Programming

EPS464 EPLDs can be programmed on an IBM PS/2, PC-AT, or compatible computer with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a EPS464 to the results of simulation. To use this feature, you must use the device adapter with the "PLM-" prefix.

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices. For more information, see *Programming Hardware Manufacturers.*

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–0.5	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–1.0	13.0	V
V_I	DC input voltage		–0.5	5.5	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–55	125	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.4	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Note (4)*		100	120	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Note (4)*		105	125	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPS464-20		EPS464-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		7		10		ns
t_{CL}	Global clock low time		7		10		ns
t_{ASU}	Array clock setup time		4		5		ns
t_{AH}	Array clock hold time		8		10		ns
t_{ACO1}	Array clock to output delay			20		25	ns
t_{ACH}	Array clock high time		7		10		ns
t_{ACL}	Array clock low time		7		10		ns
t_{CNT}	Minimum global clock period			15		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	66.7		50		MHz
t_{ACNT}	Minimum array clock period			15		20	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	66.7		50		MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	71.4		50		MHz

Internal Timing Parameters *Note (6)*			EPS464-20		EPS464-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		6	ns
t_{IO}	I/O input pad and buffer delay			5		6	ns
t_{EXP}	Expander array delay			13		15	ns
t_{LAD}	Logic array delay			9		13	ns
t_{LAC}	Logic control array delay			9		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5	ns
t_{ZX}	Output buffer enable delay			6		6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6	ns
t_{SU}	Register setup time		4		5		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		8		10		ns
t_{GLOB}	Global control delay			1		3	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			4		4	ns
t_{CLR}	Register clear time			4		4	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C, V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Measured with a device programmed as four 16-bit counters. I_{CC} measured at 0° C.
(5) The f_{MAX} values represent the highest frequency for pipelined data.
(6) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPS464-20, EPS464-25
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

Pin-Out Information

Table 11 provides pin-out information for the EPS464 QFP package.

Table 11. EPS464 QFP Pin-Outs

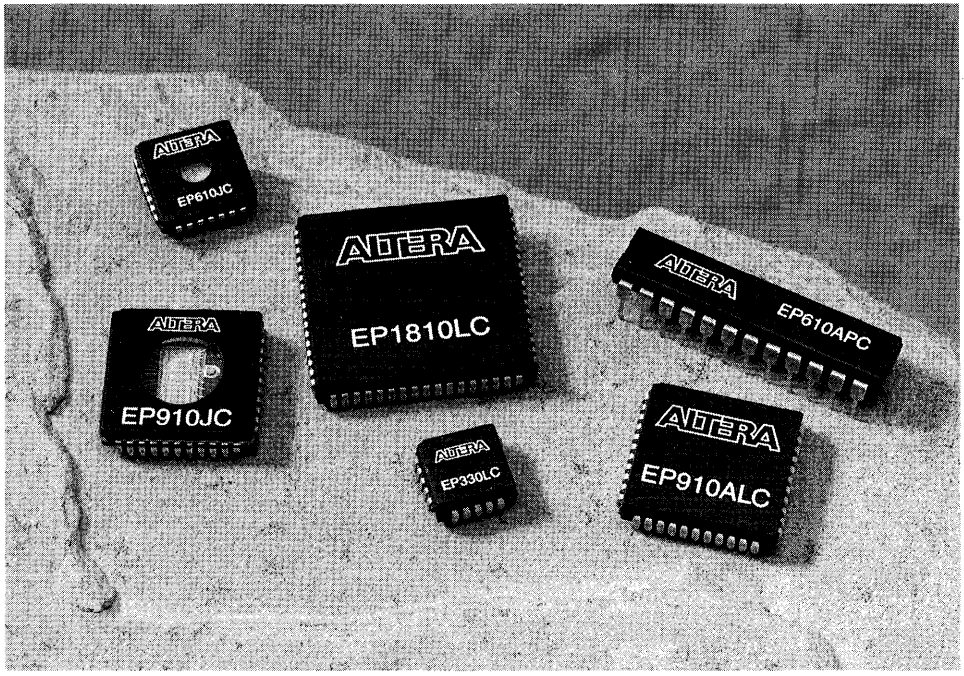
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	12	I/O	23	I/O	34	I/O
2	I/O	13	I/O	24	GND	35	I/O
3	I/O	14	I/O	25	I/O	36	GND
4	GND	15	I/O	26	I/O	37	INPUT/GCLK
5	I/O	16	GND	27	I/O	38	INPUT/GPREn
6	I/O	17	VCC	28	I/O	39	INPUT/GCLRn
7	I/O	18	I/O	29	VCC	40	INPUT/GOEn
8	I/O	19	I/O	30	I/O	41	VCC
9	VCC	20	I/O	31	I/O	42	I/O
10	I/O	21	I/O	32	I/O	43	I/O
11	I/O	22	I/O	33	I/O	44	I/O

Notes:

Contents

August 1993

Section 5 Classic


ALTERA
EP610JC
ALTERA
EP1810LC
ALTERA
EP610APC
ALTERA
EP910JC
ALTERA
EP330LC
ALTERA
EP910ALC

Classic

Programmable Logic Device Family

August 1993, ver. 1 | Data Sheet

Features

- Complete EPLD family with logic densities up to 1,800 available gates (900 usable gates). See Table 1.
- Multiple 20-pin PAL and GAL replacement and integration
- Device erasure and reprogramming with advanced, non-volatile EEPROM and EPROM technology
- Fast pin-to-pin logic delays as low as 7.5 ns and internal counter frequencies as high as 125 MHz
- 20 to 68 pins available in DIP, J-lead, PGA, and SOIC packages
- Programmable Security Bit for total protection of proprietary designs
- 100% generically testable to provide 100% programming yield
- Programmable registers providing D, T, JK, and SR flipflops with individual Clear and Clock controls
- Software design support featuring Altera's MAX+PLUS II development system on 386- and 486-based PC, Sun SPARCstation, and HP 9000 Series 700 workstation platforms
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers
- EDIF, Verilog, VHDL, and other interfaces available for additional design entry and simulation support from other standard CAE tools

Table 1. Classic Device Features

Feature	EP330	EP610, EP610T *(1)*	EP610A	EP910, EP910T	EP910A	EP1810, EP1810T *(1)*
Available Gates	300	600	600	900	900	1,800
Usable Gates	150	300	300	450	450	900
Macrocells	8	16	16	24	24	48
Max. User I/O	18	20	20	36	36	64
t_{PD} (ns)	12	15 (35)	7.5	30	10	20 (45)
f_{CNT} (MHz)	100	83.3 (28.6)	125	33.3	100	50 (22.2)

Note:

(1) Numbers in parentheses are for MIL-STD-883B-compliant versions of the EP610 and EP1810. For more information, refer to the *EP610 MIL-STD-883B-Compliant EPLD* and *EP1810 MIL-STD-883B-Compliant EPLD* data sheets in this data book.

General Description

The Altera Classic family offers the industry's most comprehensive solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technologies, these devices also have turbo-only and high-performance versions, all of which are described in this data sheet.

Classic EPLDs support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 150 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 7.5 ns and counter frequencies as high as 125 MHz. Classic EPLDs are available in a wide range of packages, including ceramic and plastic dual in-line (CerDIP & PDIP), ceramic and plastic J-lead chip carrier (JLCC & PLCC), ceramic pin-grid array (PGA), and plastic small-outline integrated circuit (SOIC) packages.

The Classic family uses sum-of-products logic, which provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The basic building block of the Classic EPLD, the macrocell, can be individually programmed for D, T, SR, or JK flipflop operation or for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global Clock or by any input or feedback path to the AND array in all Classic devices except the EP330. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to simultaneously implement a variety of logic functions.

In comparison to equivalent bipolar devices, the CMOS EEPROM and EPROM technologies of Classic EPLDs can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well-suited for a wide range of low-power applications. Classic devices are 100% generically tested and are easily erased electrically or with ultraviolet light. Designs and design changes can be implemented quickly, eliminating the need for post-programming testing.

The Classic family is supported by Altera's MAX+PLUS II development system, an integrated software package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and programming capabilities. MAX+PLUS II provides EDIF, VHDL, Verilog, and other netlist interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. The MAX+PLUS II development system runs on 386- and 486-based PCs, Sun SPARCstations, and HP 9000 Series 700 workstations.

Turbo-Only "T" EPLDs

Altera offers Classic EPLDs in which the Turbo Bit is permanently turned on (designated by a "T" suffix in the ordering code). These devices are available in plastic one-time-programmable (OTP) packages and provide a low-cost, high-speed solution to logic designs. They are completely pin-, function-, and programming file-compatible with their non-turbo counterparts. "T" devices have no non-Turbo mode.

High-Performance "A" EPLDs

For the highest performance in the Classic family, Altera offers the EP610A and EP910A. Fabricated on a 0.8-micron CMOS EEPROM process, these devices offer t_{PD} delays as low as 7.5 ns and counter frequencies as high as 125 MHz. These EPLDs are reprogrammable, plastic-packaged devices that are completely pin-, function-, and programming file-compatible with their EPROM counterparts. "A" devices have no zero-power option.

Functional Description

The Classic EPLD architecture consists of the following elements:

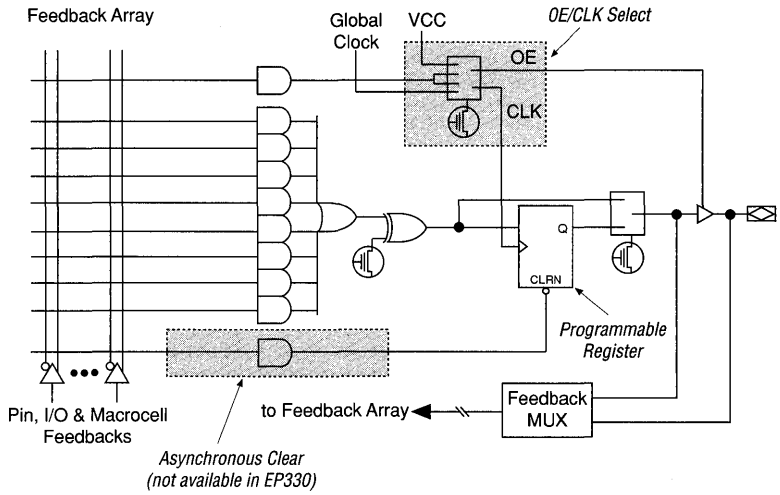
- Macrocells
- Programmable registers
- Output Enable/Clock selection
- Feedback selection

Macrocells

The Classic macrocell, shown in Figure 1, can be individually configured for both sequential and combinatorial logic operation. Eight product terms form a programmable-AND array that feeds an OR gate for combinatorial logic implementation. An additional product term is used for asynchronous Clear control of the internal register (asynchronous Clear is not available in the EP330); another product term implements either an Output Enable or a logic-array-generated Clock. Inputs to the programmable-AND array come from both the true and complement signals of the dedicated inputs, feedbacks from I/O pins that are configured as inputs, and feedbacks from macrocell outputs. Signals from dedicated inputs are globally routed and can feed the inputs of all device macrocells. The routing of feedback signals from macrocells and I/O pins configured as inputs is controlled by the feedback multiplexer (feedback MUX).

Figure 1. Classic Macrocell

For additional information on feedback MUX configurations, see Figure 3.



The eight product terms of the programmable-AND array feed the 8-input OR gate, which then feeds one input to an XOR gate. The other input to the XOR gate is connected to a programmable bit that allows the array output to be inverted. Altera's MAX+PLUS II software uses the XOR gate to implement active-high or active-low logic, or uses De Morgan's inversion to reduce the number of product terms to implement a function.

Programmable Registers

To implement registered functions, each macrocell flipflop can be individually programmed for D, T, JK, or SR operation (EP330 EPLDs have D flipflops only). If necessary, the flipflop can be bypassed for combinatorial operation. During design compilation, MAX+PLUS II selects the most efficient flipflop operation for each registered function to minimize the logic resources needed by the design. Registers have an individual asynchronous Clear function controlled by a dedicated product term (asynchronous Clear is not available in the EP330). Registers are cleared automatically during power-up.

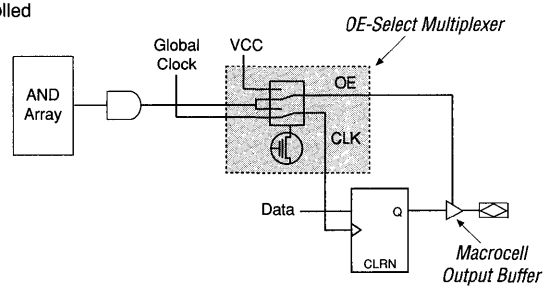
Output Enable/Clock Selection

Figure 2 shows the two operating modes (Mode 0 and 1) provided by the Output Enable/Clock selection multiplexer (OE/CLK MUX). This multiplexer, which is controlled by a single programmable bit, can be

Figure 2. OE/CLK Select Multiplexer

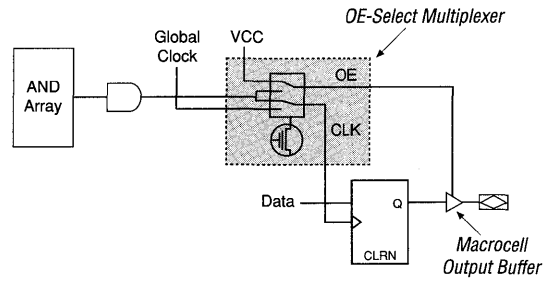
In Mode 0, the register is clocked by the global Clock signal. The output is enabled by the logic from the product term.

Mode 0:
OE = Product-Term-Controlled
CLK = Global



In Mode 1, the output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated. (Not available in EP330 EPLDs.)

Mode 1:
OE = Enabled
CLK = Product Term



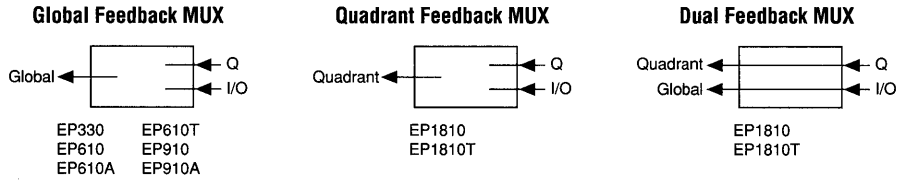
individually configured for each macrocell. In Mode 0, the tri-state output buffer is controlled by a single product term. If the output of the AND gate is high, the output buffer is enabled. If the output is low, the output buffer has a high-impedance value. In this mode, the macrocell flipflop is clocked by its global Clock input signal. (The EP330 supports only Mode 0.)

In Mode 1, the Output Enable buffer is always enabled, so the macrocell flipflop can be triggered by an array Clock signal generated by the OE/CLK product term. This mode allows flipflops to be individually clocked by any of the terms on the AND array. With both true and complement signals in the AND array, the flipflop can be configured to trigger on a rising or falling edge. This product-term-controlled Clock configuration also supports gated Clock structures.

Feedback Selection

Each macrocell in a Classic EPLD provides array feedback selection that is controlled by the feedback MUX. This feedback selection allows the user to feed either the macrocell output or the I/O pin input associated with the macrocell back into the AND array. The macrocell output can be either the Q output of the programmable register or the combinatorial output of the macrocell. Different Classic EPLDs have different feedback MUX configurations. See Figure 3. The EP330, EP610, EP610A, EP910, and EP910A have a global feedback configuration: either the macrocell output (Q) or the I/O pin input (I/O) can feed back to the AND array so that it is accessible to all other macrocells.

Figure 3. Feedback MUX Configurations



EP1810 EPLDs have two feedback configurations: quadrant and dual. Most macrocells in EP1810 EPLDs have a quadrant feedback configuration: either the macrocell output or I/O pin input can feed back to other macrocells in the same quadrant. Selected macrocells in EP1810 EPLDs have a dual feedback configuration: the output of the macrocell feeds back to other macrocells in the same quadrant, and the I/O pin input feeds back to all macrocells in the device. If the associated I/O pin is not used, the macrocell output can optionally feed all macrocells in the device. In this case, the output of the macrocell passes through the tri-state buffer and uses the feedback path between the buffer and the I/O pin.

Design Security

Classic EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM or EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

Turbo Bit

Many Classic EPLDs contain a programmable Turbo Bit to control the automatic power-down feature that enables the low-standby-power mode (I_{CC1}). When the Turbo Bit is turned on, the low-standby-power mode is disabled. All AC values are tested with the Turbo Bit turned on. When the device is operating with the Turbo Bit turned off (non-turbo mode), a non-

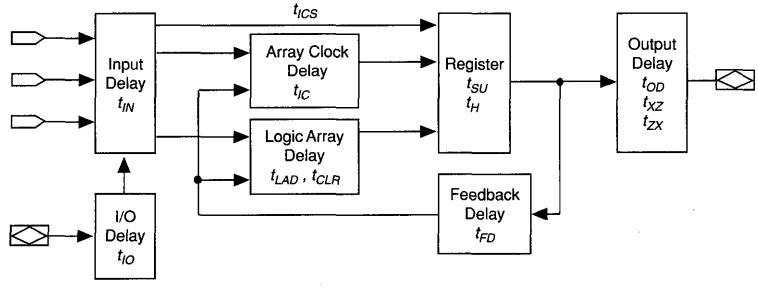
turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-turbo adder is specified in the "AC Operating Conditions" tables for each Classic device that supports the turbo mode.

Timing Model

Classic EPLD timing can be analyzed with MAX+PLUS II software, with a variety of popular industry-standard CAE simulators and timing analyzers, or with the timing model shown in Figure 4. Classic EPLDs have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 4. Timing Model

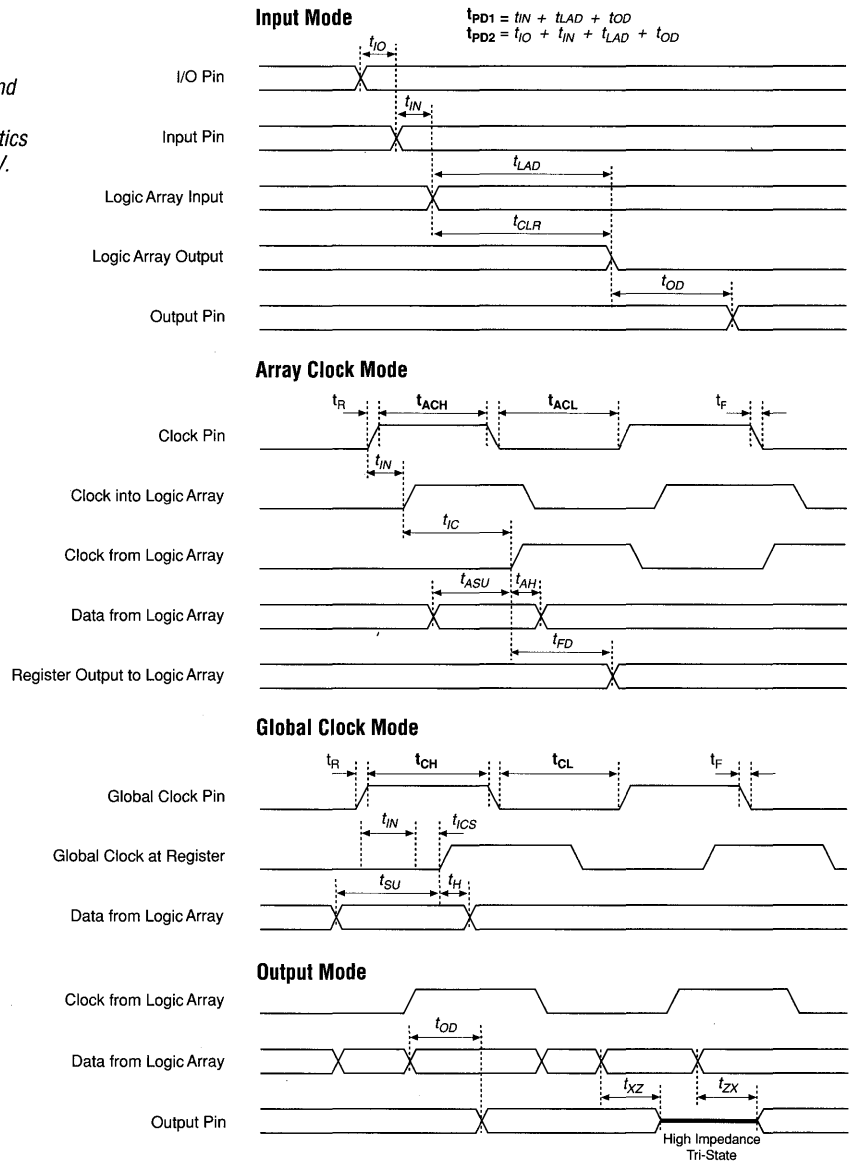
If the register is bypassed, the delay between the logic array and the output buffer is zero.



Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters can be calculated from the sum of internal parameters and represent pin-to-pin timing delays. Figure 5 shows the internal timing relationship for internal and external delay parameters. For more information on EPLD timing, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Figure 5. Switching Waveforms

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low.
All timing characteristics are measured at 1.5 V.



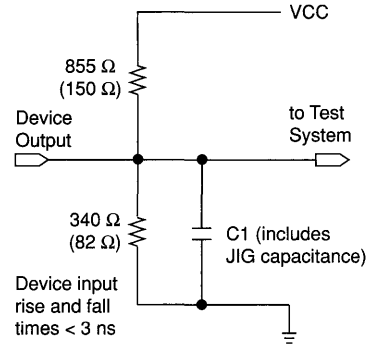
Generic Testing

Classic EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM or EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 6.

Test programs can be used and then erased during early stages of the device production flow. EPROM-based EPLDs in one-time programmable windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during this production flow.

Figure 6. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Numbers in parentheses are for the EP330.

MAX+PLUS II Development System

Classic EPLDs are supported by the MAX+PLUS II development system, a completely integrated environment for design entry, compilation, verification, and programming. MAX+PLUS II software is available for 386- and 486-based PCs, as well as Sun SPARCstations and HP 9000 Series 700 workstations. All platforms include more than 300 74-series macrofunctions and the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, conditional logic, and truth table entry methods. MAX+PLUS II also provides highly automated compilation, automatic multi-device partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a comprehensive on-line help system.

In addition, MAX+PLUS II imports and exports industry-standard EDIF 2 0 0 and EDIF 2 9 0 netlist files for a convenient interface to industry-standard CAE tools from vendors such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic. MAX+PLUS II also exports Verilog and VHDL netlist files for use with other CAE simulation tools such as the Cadence Verilog-XL simulator. For more details, see the *MAX+PLUS II Programmable Logic Development System & Software* and *CAE Software Support* data sheets in this data book.

Device Programming

Classic EPLDs can be programmed on 386- and 486-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

The MAX+PLUS II software can use waveform- or text-format test vectors created with the MAX+PLUS II Waveform or Text Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a Classic EPLD to the results of simulation. (This feature requires a device adapter with the "PLM-" prefix.) See the *Altera Programming Hardware Data Sheet* for more information.

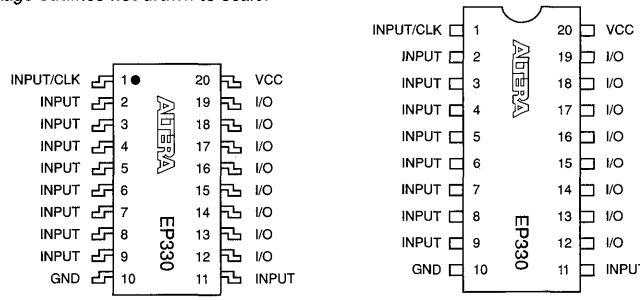
Data I/O and other programming hardware manufacturers also offer programming support for Altera devices. See the *Programming Hardware Manufacturers* data sheet in this data book for more information.

Features

- High-performance, 8-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 125 MHz
- Low power; I_{CC} = 45 mA (typical)
- Macrocell flipflops can be individually programmed for registered or combinatorial operation
- Available in 20-pin, one-time-programmable (OTP) plastic packages (see Figure 7):
  - Small-outline integrated circuit (SOIC)
  - Dual in-line package (PDIP)
- Direct replacement for 20-pin PAL/GAL devices

Figure 7. EP330 Package Pin-Out Diagrams

Package outlines not drawn to scale.



General Description

The Altera EP330 EPLD is a high-speed, low-power device that is a direct replacement for GAL 16V8 and most 20-pin PAL programmable logic devices. The EP330 has 8 macrocells, 10 dedicated input pins, and 8 I/O pins (see Figure 8). Each macrocell can access signals from the global bus. The global bus consists of the true and complement forms of the device inputs and the macrocell outputs. Pin 1 can be used as the global Clock for registers in the device or as a dedicated input for combinatorial logic.

Figure 8. EP330 Block Diagram

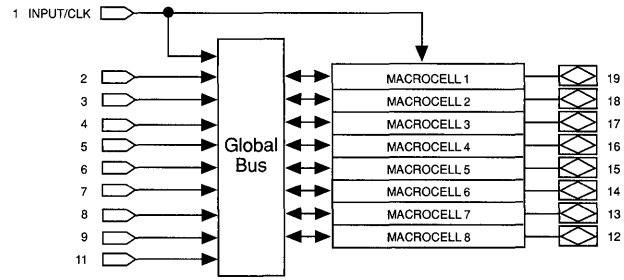
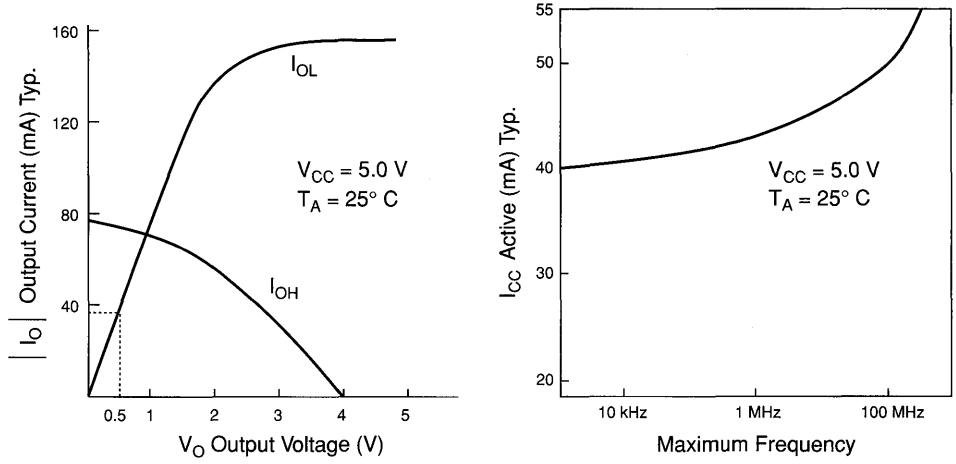


Figure 9 shows the maximum output drive characteristics of EP330 I/O pins and typical supply current (I_{CC}) versus frequency for the EP330 EPLD.

Figure 9. EP330 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–160	160	mA
I_{OUT}	DC output current, per pin		–50	50	mA
P_D	Power dissipation			800	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*Note (2)*		20	ns
t_F	Input fall time	*Note (2)*		20	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load, *Note (5)*		40	75	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (5)*		45	75	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF

AC Operating Conditions *Note (4)*

			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15	ns
t_{PD2}	I/O input to non-registered output			13		16	ns
t_{PZX}	Input to output enable			12		15	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		12		15	ns
t_{IO}	I/O input pad and buffer delay			1		1	ns

Global Clock Mode			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	125		100		MHz
t_{SU}	Setup time		6		8		ns
t_H	Hold time		0		0		ns
t_{CH}	Clock high time		4		5		ns
t_{CL}	Clock low time		4		5		ns
t_{CO1}	Clock to output delay			8		10	ns
t_{CNT}	Minimum clock period			10		12	ns
f_{CNT}	Internal maximum frequency	*Note (5)*	100		83.3		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all Clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) Measured with a device programmed as an 8-bit counter. I_{CC} measured at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. Pin 11 (high-voltage pin during programming) has maximum capacitance of 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

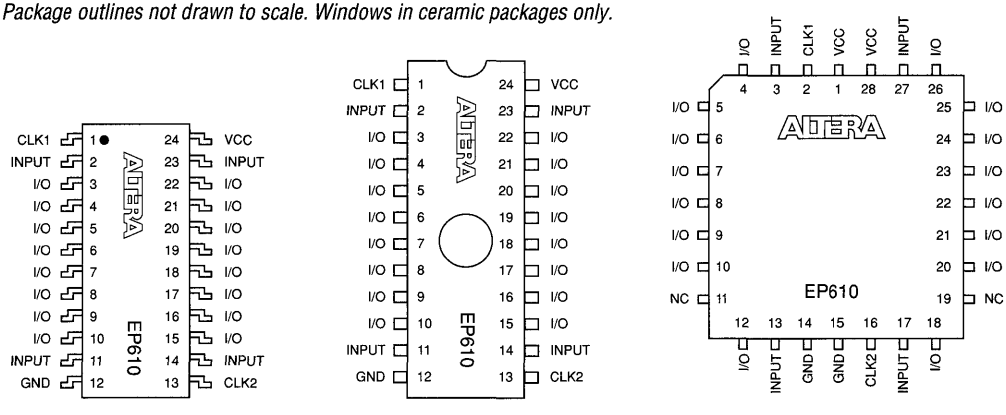
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP330-12, EP330-15
Industrial Temp.	(–40° C to 85° C)	EP330-15

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs
- Pin-, function-, and programming file-compatible with Altera's EP610A, EP610T, and EP610 MIL-STD-883-compliant devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 10):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

Figure 10. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



General Description

The EP610 has 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global Clock pins (see Figure 11). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLOCK1 is a dedicated Clock input for the registers in macrocells 9 through 16. CLOCK2 is a dedicated Clock input for registers in macrocells 1 through 8.

5 Classic

Figure 11. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

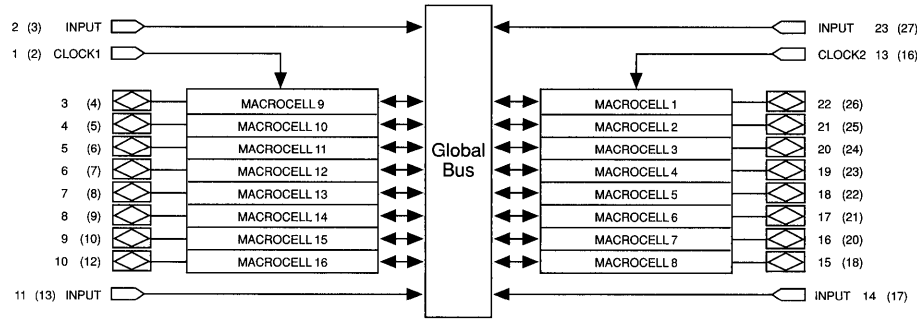
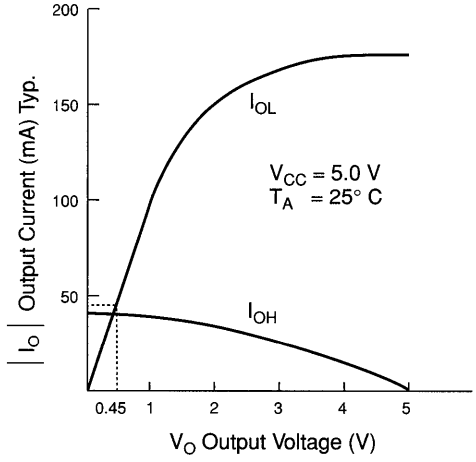


Figure 12 shows the maximum output drive characteristics of EP610 I/O pins.

Figure 12. EP610 Maximum Output Drive Characteristics

EP610-15 & EP610-20 EPLDs



EP610-25, EP610-30 & EP610-35 EPLDs

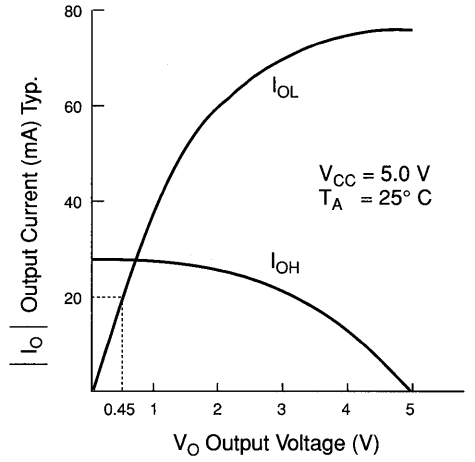
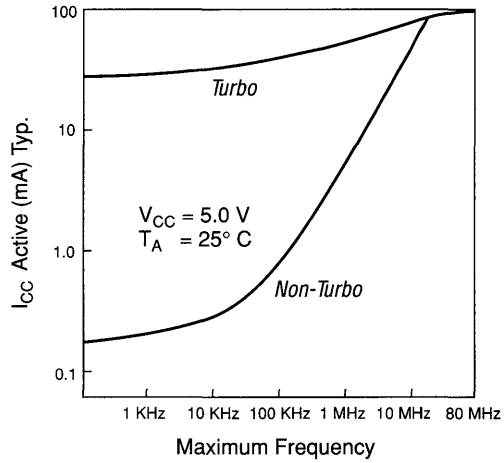


Figure 13 shows the typical supply current (I_{CC}) versus frequency of all EP610 devices.

Figure 13. EP610 I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (3)*		100 (50)	ns
t_F	Input fall time			100 (50)	ns

DC Operating Conditions *Notes (2), (4), (5)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Notes (6), (7)*			20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz			5	10 (15)	mA
I_{CC3}	V_{CC} supply current (turbo, active)	*Note (7)*	-15, -20		60	90 (115)	mA
			-25, -30, -35		45	60 (75)	mA

Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions: EP610-15 and EP610-20 *Note (5)*

			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_{H}	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*Note (7)*	83.3		62.5		0	MHz

Array Clock Mode			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	71.4		55.6		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*Note (7)*	71.4		55.6		0	MHz

AC Operating Conditions: EP610-25, EP610-30, and EP610-35 *Note (5)*

			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns

Global Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	47.6		41.7		37.0		0	MHz
t_{SU}	Input setup time		21		24		27		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		10		11		12		0	ns
t_{CL}	Clock low time		10		11		12		0	ns
t_{CO1}	Clock to output delay			15		17		20	0	ns
t_{CNT}	Minimum clock period			25		30		35	0	ns
f_{CNT}	Internal maximum frequency	*Note (7)*	40.0		33.3		28.6		0	MHz

Array Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	47.6		41.7		37.0		0	MHz
t_{ASU}	Input setup time		8		8		8		30	ns
t_{AH}	Input hold time		12		12		12		0	ns
t_{ACH}	Clock high time		10		11		12		0	ns
t_{ACL}	Clock low time		10		11		12		0	ns
t_{ACO1}	Clock to output delay			27		32		37	30	ns
t_{ACNT}	Minimum clock period			25		30		35	0	ns
f_{ACNT}	Internal maximum frequency	*Note (7)*	40.0		33.3		28.6		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15 and EP610-20 EPLDs: maximum V_{PP} is 14.0 V.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns. For EP610-15 and EP610-20 Clocks: t_R and t_F = 20 ns.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When the Turbo Bit is not set (non-turbo mode), an EP610 EPLD will enter standby mode if no logic transitions occur for 100 ns (after the last transition).
(7) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP610-25, EP610-30, and EP610-35 EPLDs: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP610-15, EP610-20, EP610-25, EP610-30, EP610-35
Industrial Temp.	(–40° C to 85° C)	EP610-20, EP610-30, EP610-35
Military Temp.	(–55° C to 125° C)	EP610-35 *Note (1)*

Note:

(1) Only military-temperature-range devices are listed. MIL-STD-883-compliant product specifications are provided in the *EP610 MIL-STD-883-Compliant EPLD Data Sheet* in this data book and in Military Product Drawings (MPDs). However, MPDs should be used to prepare Source Control Drawings (SCDs) and are available from Altera Marketing at (408) 894-7000. (For more information on MPDs and SCDs, see the *Military Products Data Sheet* in this data book.)

Notes:

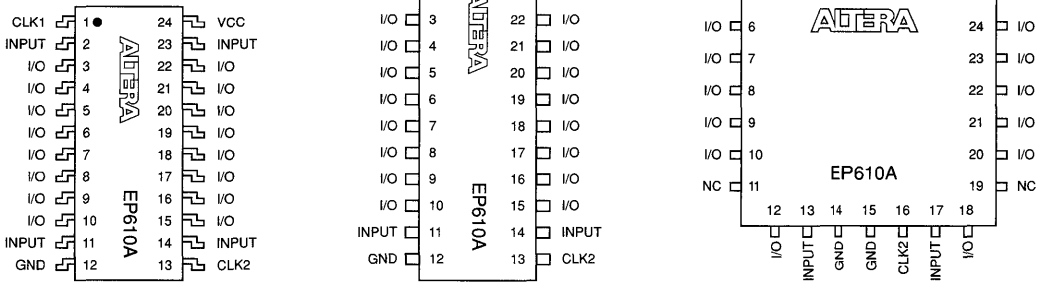
Features

Preliminary Information

- Highest-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 7.5 ns
  - Counter frequencies up to 125 MHz
  - Pipelined data rates up to 142.9 MHz
- Fabricated on advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 20 inputs or 16 outputs
- Pin-, function-, and programming file-compatible with Altera's EP610, EP610T, EP610 MIL-STD-883-compliant, and EP630 devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in reprogrammable plastic packages (see Figure 14):
  - 24-pin small-outline integrated circuit (SOIC)
  - 24-pin dual in-line package (PDIP)
  - 28-pin J-lead chip carrier (PLCC)

Figure 14. EP610A Package Pin-Out Diagrams

Package outlines not drawn to scale.



24-Pin SOIC | 24-Pin DIP | 28-Pin J-Lead

General Description

The Altera EP610A EPLD is a high-speed, EEPROM-based version of the EP610 device. Fully compatible with EP610 devices, the EP610A offers enhanced performance for existing EP610 designs with no additional design modifications. For information on EP610A architecture, refer to Figure 11 earlier in this data sheet.

5 Classic

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			25	ns
t_F	Input fall time			25	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (4), (5)*		105	130 (180)	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

			EP610A-7		EP610A-10		EP610A-12		EP610A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10		12		15	ns
t_{PD2}	I/O input to non-registered output			7.5		10		12		15	ns
t_{PZX}	Input to output enable			7.5		10		12		16	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		7.5		10		12		16	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		7.5		10		12		16	ns

Global Clock Mode			EP610A-7		EP610A-10		EP610A-12		EP610A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	142.9		125		100		83.3		MHz
t_{SU}	Input setup time		6		7		8		10		ns
t_{H}	Input hold time		0		0		0		0		ns
t_{CH}	Clock high time		3.5		4		5		6		ns
t_{CL}	Clock low time		3.5		4		5		6		ns
t_{CO1}	Clock to output delay			5		6		7		8	ns
t_{CNT}	Minimum clock period			8		10		12		14	ns
f_{CNT}	Internal maximum frequency	*Note (4)*	125.0		100		83.3		71.4		MHz

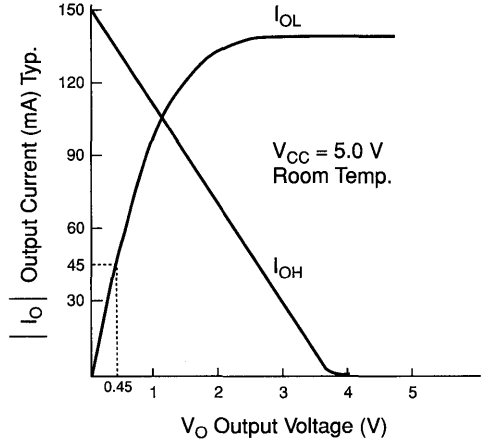
Array Clock Mode			EP610A-7		EP610A-10		EP610A-12		EP610A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	142.9		125		100		83.3		MHz
t_{ASU}	Input setup time		3		3		4		5		ns
t_{AH}	Input hold time		3		3		4		5		ns
t_{ACH}	Clock high time		3.5		4		5		6		ns
t_{ACL}	Clock low time		3.5		4		5		6		ns
t_{ACO1}	Clock to output delay			8		10		12		14	ns
t_{ACNT}	Minimum clock period			8		10		12		14	ns
f_{ACNT}	Internal maximum frequency	*Note (4)*	125.0		100		83.3		71.4		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use; V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use; V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C. Actual I_{CC} should be verified during operation because this measurement is sensitive to the operating conditions and the actual pattern in the device.
(5) Numbers in parentheses are for military and industrial temperature versions.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. CLK2 (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 15 shows the output drive characteristics of EP610A I/O pins.

Figure 15. EP610A Maximum Output Drive Characteristics



Product Availability

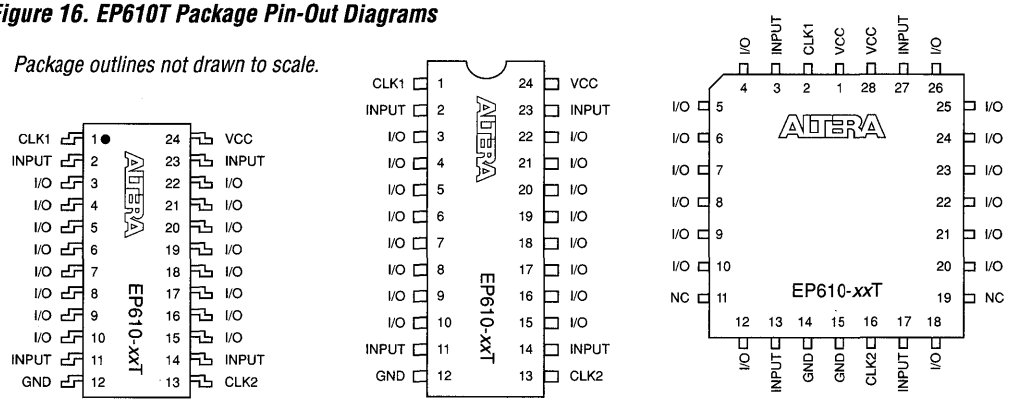
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP610A-7, EP610A-10, EP610A-12, EP610A-15
Industrial Temp.	(–40° C to 85° C)	EP610A-15
Military Temp.	(–55° C to 125° C)	Consult factory

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs
- Pin-, function-, and programming file-compatible with Altera's EP610, EP610A, and EP610 MIL-STD-883-compliant devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in low-cost, one-time-programmable (OTP) packages (see Figure 16):
  - 24-pin small-outline integrated circuit (SOIC)
  - 24-pin dual in-line package (PDIP)
  - 28-pin J-lead chip carrier (PLCC)

Figure 16. EP610T Package Pin-Out Diagrams

Package outlines not drawn to scale.



24-Pin SOIC | 24-Pin DIP | 28-Pin J-Lead

General Description

The Altera EP610T EPLD is a low-cost, high-performance version of the EP610 device. This device operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device, which is preset at the factory, is permanently turned on. For information on EP610T architecture, refer to Figure 11 earlier in this data sheet.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*Note (2)*		100	ns
t_F	Input fall time	*Note (2)*		100	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load, *Note (5)*		60	90	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (5)*		60	90	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (4)*

			EP610-15T		EP610-20T		EP610-25T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{PD2}	I/O input to non-registered output			17		22		27	ns
t_{PZX}	Input to output enable			15		20		25	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		15		20		25	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20		27	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	ns

Global Clock Mode			EP610-15T		EP610-20T		EP610-25T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	83.3		62.5		47.6		MHz
t_{SU}	Input setup time		9		11		21		ns
t_{H}	Input hold time		0		0		0		ns
t_{CH}	Clock high time		6		8		10		ns
t_{CL}	Clock low time		6		8		10		ns
t_{CO1}	Clock to output delay			11		13		15	ns
t_{CNT}	Minimum clock period			12		16		25	ns
f_{CNT}	Internal maximum frequency	*Note (5)*	83.3		62.5		40.0		MHz

Array Clock Mode			EP610-15T		EP610-20T		EP610-25T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	71.4		55.6		47.6		MHz
t_{ASU}	Input setup time		6		8		8		ns
t_{AH}	Input hold time		6		8		12		ns
t_{ACH}	Clock high time		7		9		10		ns
t_{ACL}	Clock low time		7		9		10		ns
t_{ACO1}	Clock to output delay			15		20		27	ns
t_{ACNT}	Minimum clock period			14		18		25	ns
f_{ACNT}	Internal maximum frequency	*Note (5)*	71.4		55.6		40.0		MHz

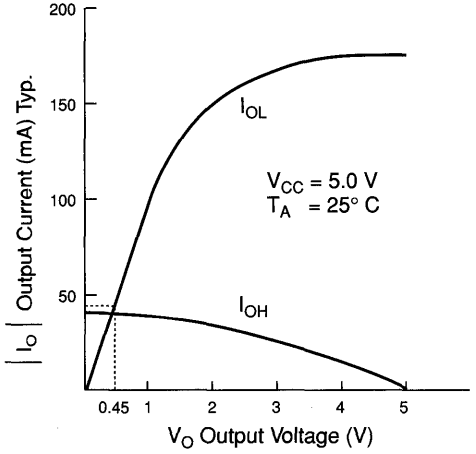
Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15T and EP610-20T EPLDs: maximum V_{PP} is 14.0 V.
(2) For EP610-15T and EP610-20T EPLDs: t_R and t_F = 40 ns. For EP610-15T and EP610-20T Clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. For EP610-25T EPLDs: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

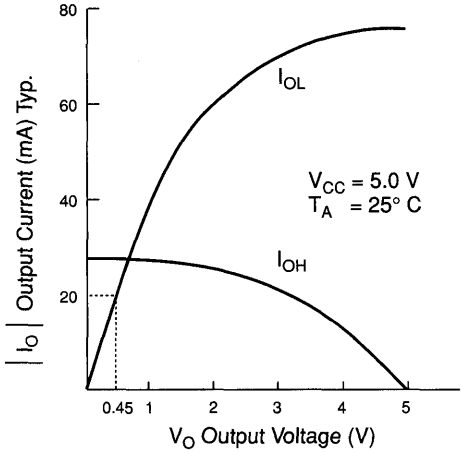
Figure 17 shows the output drive characteristics for EP610T I/O pins and the typical supply current (I_{CC}) versus frequency for the EP610T EPLD.

Figure 17. EP610T Maximum Output Drive Characteristics & I_{CC} vs. Frequency

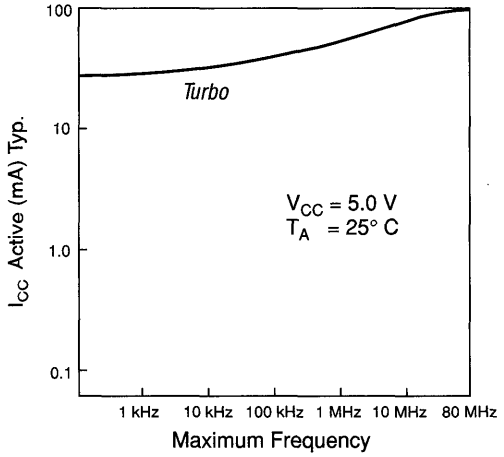
Output Drive Characteristics of EP610-15T & EP610-20T EPLDs



Output Drive Characteristics of EP610-25T EPLDs



I_{CC} vs. Frequency of All EP610T EPLDs



Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP610-15T, EP610-20T, EP610-25T
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

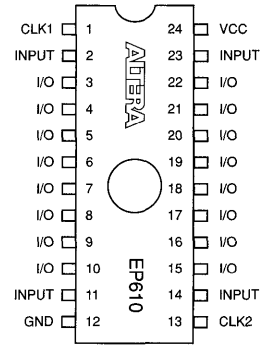
EP610 MIL-STD-883-Compliant EPLD

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 35 ns
  - Counter frequencies up to 28.5 MHz
  - Pipelined data rates up to 37 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs
- Pin-, function-, and programming file-compatible with Altera's EP610 devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 24-pin windowed ceramic dual in-line packages (CerDIP) (see Figure 18)

Figure 18. EP610 MIL-STD-883-Compliant Package Pin-Out Diagram

Package outlines not drawn to scale.



24-Pin DIP

General Description

The Altera EP610 MIL-STD-883-compliant EPLD can implement up to 600 equivalent gates of SSI and MSI logic functions. This device complies with the military standard operating requirements listed in MIL-STD-883B. For information on the device architecture, output drive characteristics, and supply current versus frequency graphs, refer to Figures 11, 12, and 13, respectively, earlier in this data sheet.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage		–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–55	125	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			50	ns
t_F	Input fall time			50	ns

DC Operating Conditions *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (3)*	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (3)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (3)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10	10	µA
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Note (4)*		900	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (4)*		25	mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (4)*		140	mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		35	ns
t_{PD2}	I/O input to non-registered output	*Notes (6), (7)*		37	ns
t_{PZX}	Input to output enable			35	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Notes (2), (6), (7), (8)*		35	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF, *Notes (6), (7)*		37	ns

Global Clock Mode					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Notes (6), (9), (10)*	37.0		MHz
t_{SU}	Input setup time	*Notes (6), (7)*	27		ns
t_{H}	Input hold time	*Note (6)*	0		ns
t_{CH}	Clock high time	*Note (2)*	12		ns
t_{CL}	Clock low time		12		ns
t_{CO1}	Clock to output delay			20	ns
t_{CNT}	Minimum clock period	*Notes (2), (11)*		35	ns
f_{CNT}	Internal maximum frequency	*Note (11)*	28.5		MHz

Array Clock Mode					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Notes (6), (9), (10)*	37.0		MHz
t_{ASU}	Input setup time	*Notes (2), (6), (7)*	8		ns
t_{AH}	Input hold time		12		ns
t_{ACH}	Clock high time	*Notes (2), (7)*	12		ns
t_{ACL}	Clock low time		12		ns
t_{ACO1}	Clock to output delay	*Notes (6), (7)*		37	ns
t_{ACNT}	Minimum clock period	*Notes (2), (11)*		35	ns
f_{ACNT}	Internal maximum frequency		28.6		MHz

Notes to tables:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: V_{CC} = 5 V DC ± 10%, T_C = –55° C to 125° C
(2) These devices may not be tested, but are guaranteed to the limits specified in the Absolute Maximum Ratings table.
(3) Tested at maximum operating temperature only.
(4) Tested with non-output loading using a data pattern specified by the device manufacturer. Data path is correlated to a 16-bit counter.
(5) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated inputs only. Pin 13 (high voltage pin during programming) has a capacitance of 50 pF.
(6) All array-dependent delays are specified for an XOR pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM pull-down. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an XOR-like pattern in which only one pure input switches at a time.
(7) When in non-turbo mode, a non-turbo adder of 30 ns (maximum) is added to this parameter to determine worst-case timing. Parameters may not be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.
(8) Not tested directly, but guaranteed by testing t_{PD}.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) Not tested directly, but derived from t_{SU}.
(11) Specified with device programmed as a 16-bit counter with no output loading.

Product Availability

Product Grade	Availability
MIL-STD-883-Compliant (–55° C to 125° C)	EP610 MIL-STD-883, *Note (1)*

Note:

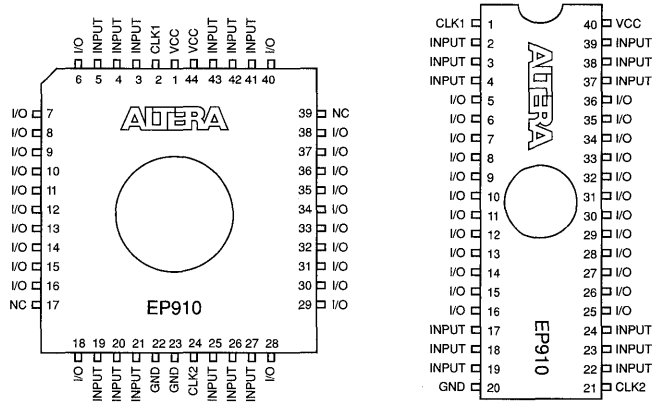
(1) Only military-temperature-range devices are listed. MIL-STD-883-compliant product specifications are provided in this data sheet and in Military Product Drawings (MPDs). However, MPDs should be used to prepare Source Control Drawings (SCDs) and are available from Altera Marketing at (408) 894-7000. (For more information on MPDs and SCDs, see the *Military Products Data Sheet* in this data book.)

Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 30, 35, and 40 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Pin-, function-, and programming file-compatible with Altera's EP910A and EP910T EPLDs
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 21):
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)

Figure 21. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



44-Pin J-Lead 40-Pin DIP

General Description

The Altera EP910 EPLD can implement up to 900 equivalent gates of SSI and MSI logic functions. The EP910 has 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global Clock pins (see Figure 22). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLOCK1 and CLOCK2 are the dedicated Clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

5 Classic

Figure 22. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

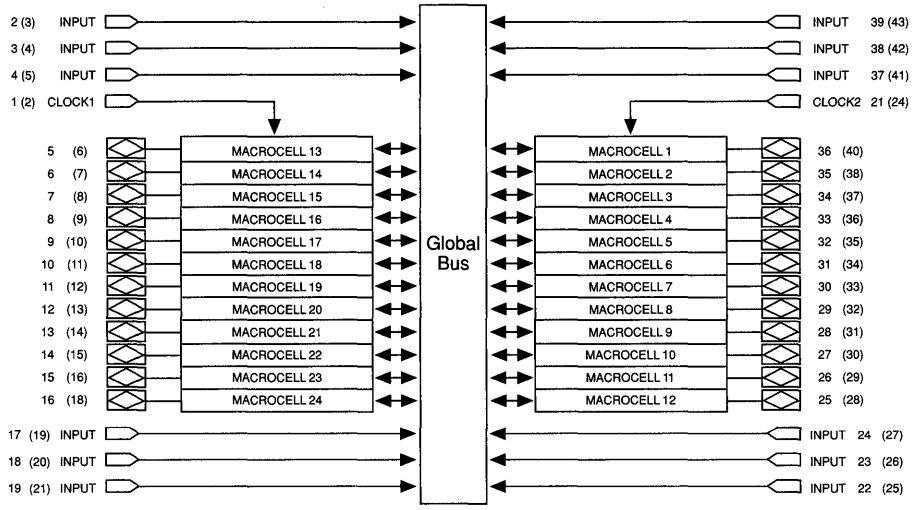
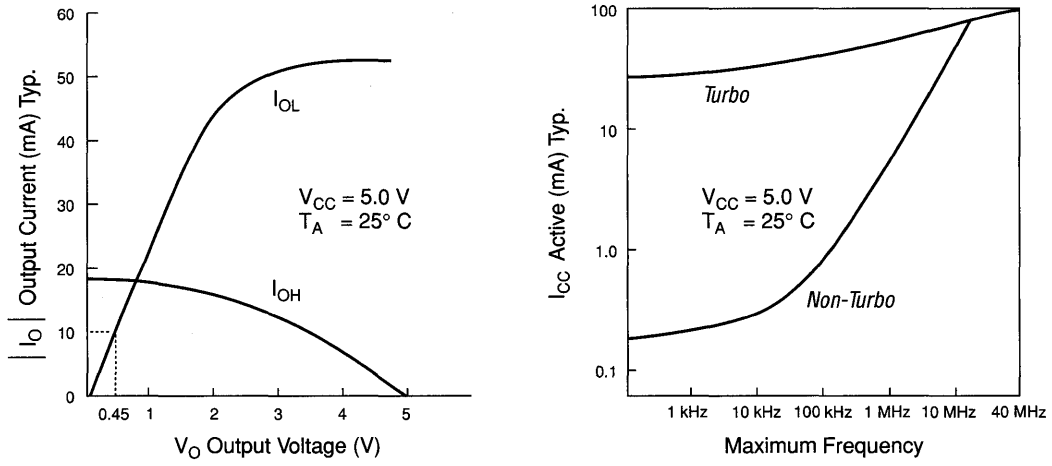


Figure 23 shows the output drive characteristics of EP910 I/O pins and typical supply current (I_{CC}) versus frequency for the EP910 EPLD.

Figure 23. EP910 Maximum Output Drive Characteristics and I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (3)*		100 (50)	ns
t_F	Input fall time			100 (50)	ns

DC Operating Conditions *Notes (2), (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Notes (6), (7)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (7)*		6	20	mA
I_{CC3}	V_{CC} supply current (turbo, active)			45	80 (100)	mA

5 Classic

Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
t_{PD2}	I/O input to non-registered output			33		38		43	30	ns
t_{PZX}	Input to output enable			30		35		40	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		30		35		40	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
t_{IO}	I/O input pad and buffer delay			3		3		3	0	ns

Global Clock Mode			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	41.7		37.0		32.3		0	MHz
t_{SU}	Input setup time		24		27		31		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		12		13		15		0	ns
t_{CL}	Clock low time		12		13		15		0	ns
t_{CO1}	Clock to output delay			18		21		24	0	ns
t_{CNT}	Minimum clock period			30		35		40	0	ns
f_{CNT}	Internal maximum frequency	*Note (7)*	33.3		28.6		25.0		0	MHz

Array Clock Mode			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	33.3		31.3		29.4		0	MHz
t_{ASU}	Input setup time		10		10		10		30	ns
t_{AH}	Input hold time		15		15		15		0	ns
t_{ACH}	Clock high time		15		16		17		0	ns
t_{ACL}	Clock low time		15		16		17		0	ns
t_{ACO1}	Clock to output delay			33		38		43	30	ns
t_{ACNT}	Minimum clock period			30		35		40	0	ns
f_{ACNT}	Internal maximum frequency	*Note (7)*	33.3		28.6		25.0		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For all Clocks: t_R and t_F = 100 ns (50 ns for military and industrial temperature versions).
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When the Turbo Bit is not set (non-turbo mode), an EP910 EPLD will enter standby mode if no logic transitions occur for 100 ns (after the last transition).
(7) Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0° C.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP910-30, EP910-35, EP910-40
Industrial Temp.	(–40° C to 85° C)	EP910-35, EP910-40
Military Temp.	(–55° C to 125° C)	Consult factory

Notes:

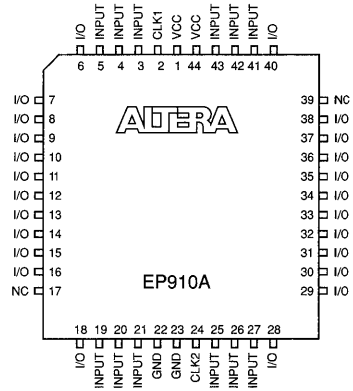
Features

Preliminary Information

- Highest-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 10 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 125 MHz
- Fabricated on advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Pin-, function-, and programming file-compatible with Altera's EP910 and EP910T EPLDs
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in a reprogrammable plastic 44-pin J-lead chip carrier (PLCC) package (see Figure 24)

Figure 24. EP910A Package Pin-Out Diagram

Package outline not drawn to scale.



44-Pin J-Lead

General Description

The Altera EP910A EPLD is a high-speed, EEPROM-based version of the EP910 device. Fully compatible with EP910 devices, the EP910A offers enhanced performance for existing EP910 designs with no additional design modifications. For information on the device architecture, refer to Figure 22 earlier in this data sheet.

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			25	ns
t_F	Input fall time			25	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (4), (5)*		120	180 (255)	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

			EP910A-10		EP910A-12		EP910A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12		15	ns
t_{PD2}	I/O input to non-registered output			10		12		15	ns
t_{PZX}	Input to output enable			11		13		16	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		11		13		16	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		11		13		16	ns

Global Clock Mode			EP910A-10		EP910A-12		EP910A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	125		100.0		83.3		MHz
t_{SU}	Input setup time		7		8		10		ns
t_{H}	Input hold time		0		0		0		ns
t_{CH}	Clock high time		4		5		6		ns
t_{CL}	Clock low time		4		5		6		ns
t_{CO1}	Clock to output delay			6		7		8	ns
t_{CNT}	Minimum clock period			10		12		14	ns
f_{CNT}	Internal maximum frequency	*Note (4)*	100		83.3		71.4		MHz

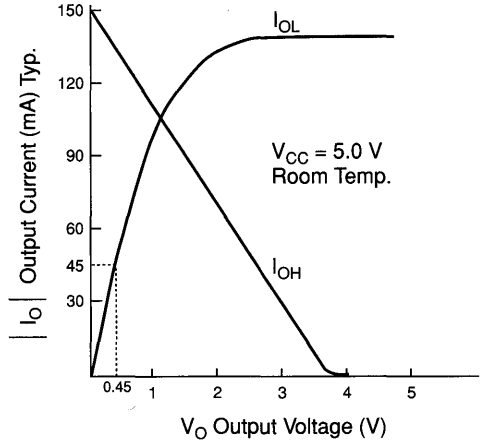
Array Clock Mode			EP910A-10		EP910A-12		EP910A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	125		100		83.3		MHz
t_{ASU}	Input setup time		3		4		5		ns
t_{AH}	Input hold time		3		4		5		ns
t_{ACH}	Clock high time		4		5		6		ns
t_{ACL}	Clock low time		4		5		6		ns
t_{ACO1}	Clock to output delay			10		12		14	ns
t_{ACNT}	Minimum clock period			10		12		14	ns
f_{ACNT}	Internal maximum frequency	*Note (4)*	100		83.3		71.4		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0° C. Actual I_{CC} should be verified during operation because this measurement is sensitive to the operating conditions and the actual pattern in the device.
(5) Numbers in parentheses are for military and industrial temperature versions.
(6) Capacitance measured at 25° C. Sample-tested only. CLK2 (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 25 shows the maximum output drive characteristics of EP910A I/O pins.

Figure 25. EP910A Maximum Output Drive Characteristics



Product Availability

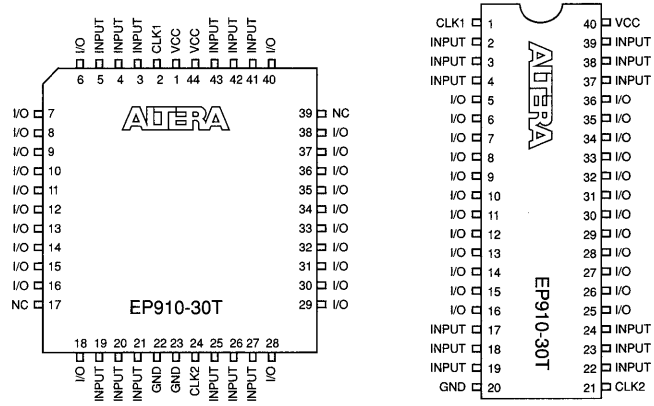
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP910A-10, EP910A-12, EP910A-15
Industrial Temp.	(–40° C to 85° C)	EP910A-15
Military Temp.	(–55° C to 125° C)	Consult factory

Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 30 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Pin-, function-, and programming file-compatible with Altera's EP910 and EP910A EPLDs
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Available in low-cost, one-time-programmable (OTP) plastic packages (See Figure 26):
  - 44-pin J-lead chip carrier (PLCC)
  - 40-pin dual in-line package (PDIP)

Figure 26. EP910T Package Pin-Out Diagrams

Package outlines not drawn to scale.



44-Pin J-Lead 40-Pin DIP

General Description

Altera's EP910T EPLD is a low-cost, high-performance version of the EP910 device. The EP910T operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device, which is preset at the factory, is permanently turned on. For information on EP910T architecture, refer to Figure 22 earlier in this data sheet.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*Note (2)*		100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load, *Note (5)*		80	115	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Note (5)*		80	115	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (4)*

			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30	ns
t_{PD2}	I/O input to non-registered output			33	ns
t_{PZX}	Input to output enable			30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33	ns
t_{IO}	I/O input pad and buffer delay			3	ns

Global Clock Mode			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	41.7		MHz
t_{SU}	Input setup time		24		ns
t_{H}	Input hold time		0		ns
t_{CH}	Clock high time		12		ns
t_{CL}	Clock low time		12		ns
t_{CO1}	Clock to output delay			18	ns
t_{CNT}	Minimum clock period			30	ns
f_{CNT}	Internal maximum frequency	*Note (5)*	33.3		MHz

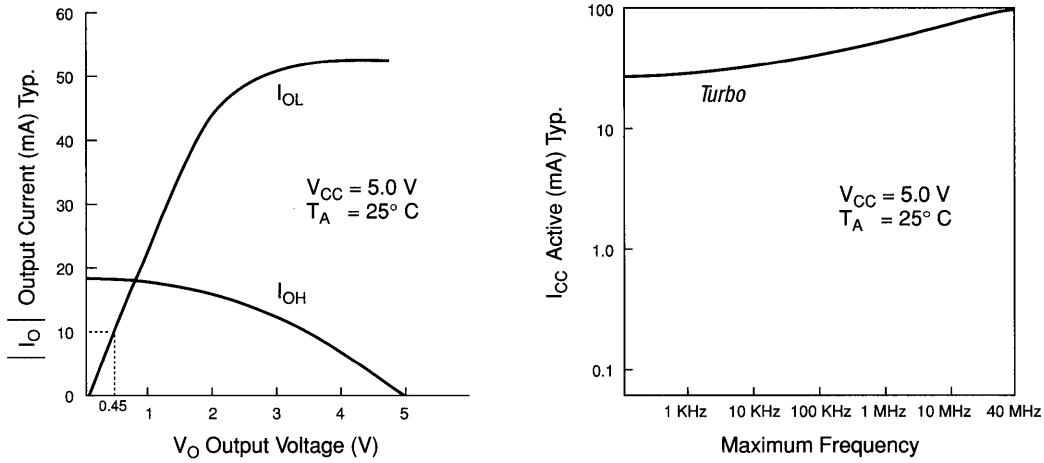
Array Clock Mode			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	33.3		MHz
t_{ASU}	Input setup time		10		ns
t_{AH}	Input hold time		15		ns
t_{ACH}	Clock high time		15		ns
t_{ACL}	Clock low time		15		ns
t_{ACO1}	Clock to output delay			33	ns
t_{ACNT}	Minimum clock period			30	ns
f_{ACNT}	Internal maximum frequency	*Note (5)*	33.3		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all Clocks: t_R and t_F = 100 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 27 shows the maximum output drive characteristics of EP910T I/O pins and typical supply (I_{CC}) current versus frequency for the EP910T EPLD.

Figure 27. EP910T Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Product Availability

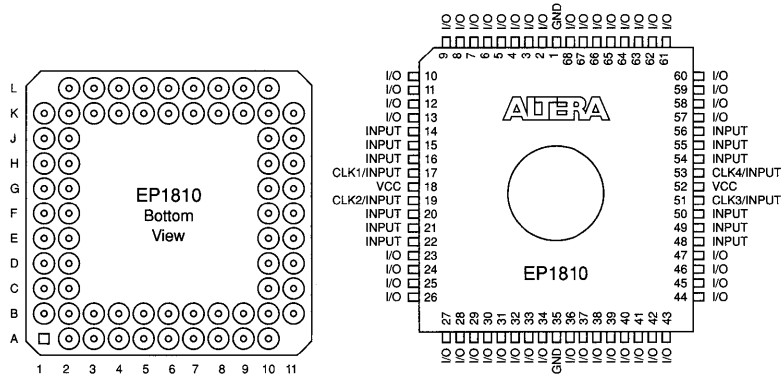
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP910-30T
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 20, 25, 35, and 45 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- Pin-, function-, and programming file-compatible with Altera's EP1810T and EP1810 MIL-STD-883-compliant devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin windowed ceramic and one-time-programmable plastic packages (see Figure 28):
  - Pin-grid array package (ceramic PGA only)
  - J-lead chip carrier (JLCC and PLCC)

Figure 28. EP1810 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 2 in this data sheet for PGA package pin-out information. Windows in ceramic packages only.

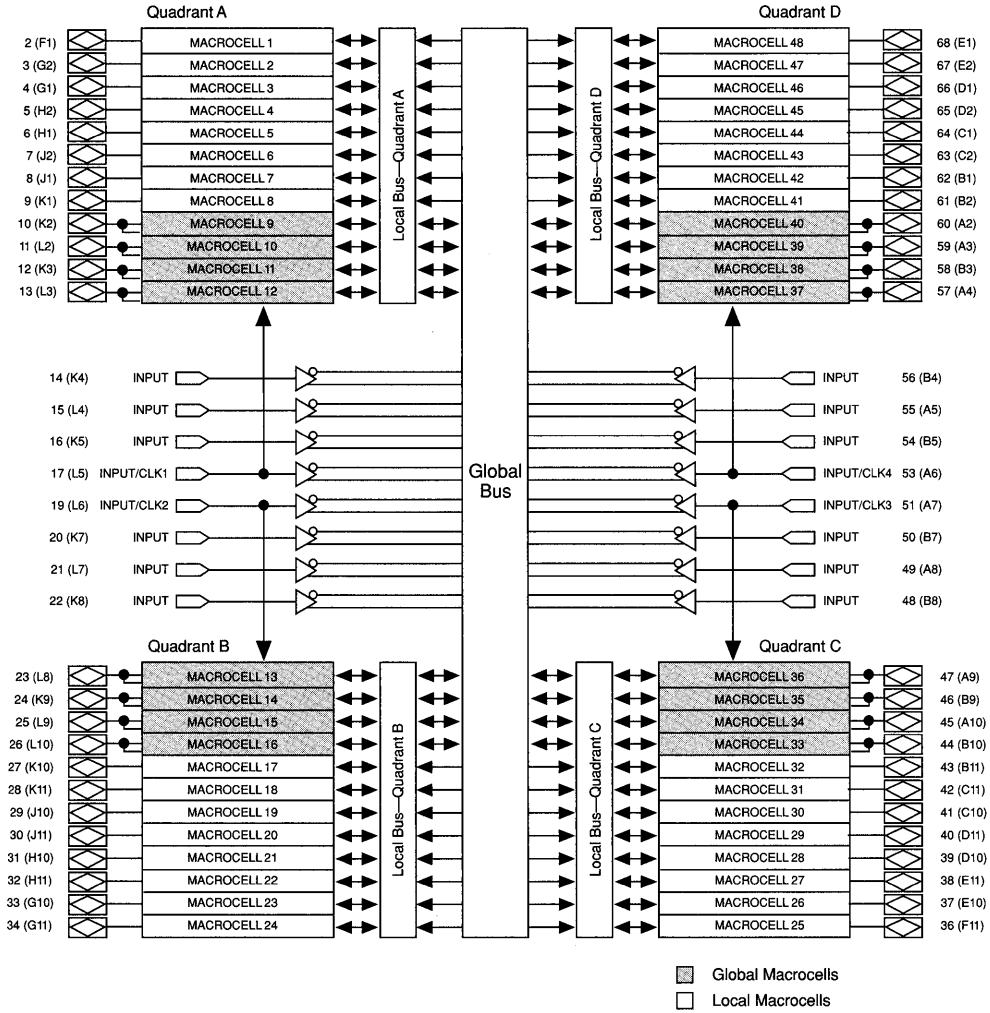


General Description

The Altera EP1810 EPLD offers LSI density, TTL-equivalent speed, and low power consumption. The EP1810 has 48 macrocells, 16 dedicated input pins, and 48 I/O pins (see Figure 29). The EP1810 is divided into four quadrants, each containing 12 macrocells. Of the twelve macrocells in each quadrant, 8 have quadrant feedback and are "local" macrocells. (See "Feedback Selection" earlier in this data sheet for more information.) The remaining 4 macrocells in the quadrant are "global" macrocells. Both local and global macrocells can access signals from the global bus, which consists

Figure 29. EP1810 Block Diagram

Numbers in parentheses are for J-lead packages. Numbers without parentheses are for PGA packages.



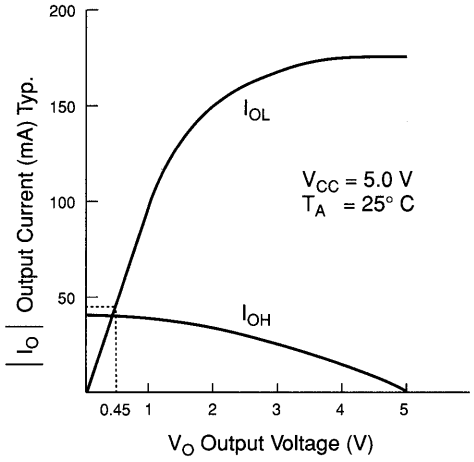
of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

The EP1810 also has four dedicated inputs (one in each quadrant) that can be used as quadrant Clock inputs. If the dedicated input is used as a Clock pin, the input feeds the Clock input of all registers in that particular quadrant.

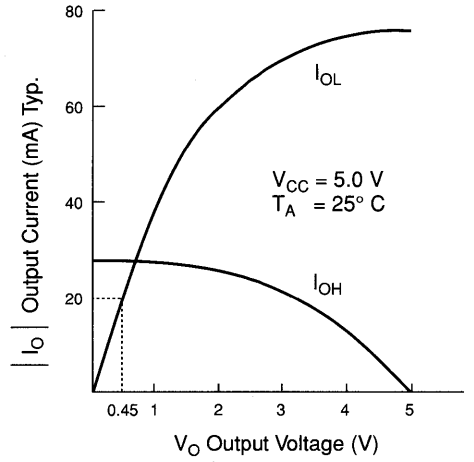
Figure 30 shows the output drive characteristics of EP1810 I/O pins and typical supply current (I_{CC}) versus frequency for the EP1810 EPLDs.

Figure 30. EP1810 Maximum Output Drive Characteristics & I_{CC} vs. Frequency

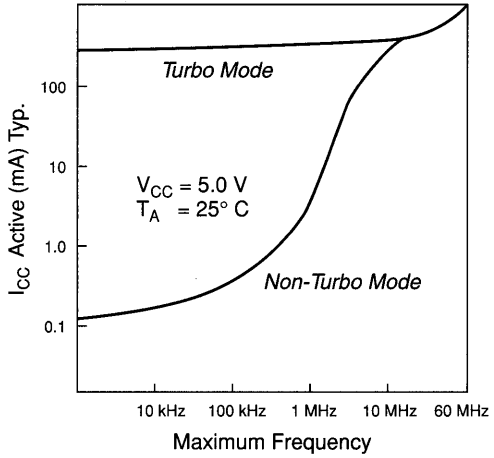
Output Drive Characteristics of EP1810-20 and EP1810-25 EPLDs



Output Drive Characteristics of EP1810-35 & EP1810-45 EPLDs



I_{CC} vs. Frequency of EP1810 EPLDs



5 Classic

Absolute Maximum Rating See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (3)*		50	ns
t_F	Input fall time			50	ns

DC Operating Conditions *Note (2), (4), (5)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current	V_I = V_{CC} or GND, I_O = 0,	-20, -25		50	150	µA
	(non-turbo, standby)	*Notes (6), (7)*	-35, -45		35	150	µA
I_{CC2}	V_{CC} supply current	V_I = V_{CC} or GND, No load,	-20, -25		20	40	mA
	(non-turbo, active)	f = 1.0 MHz, *Note (7)*	-35, -45		10	30 (40)	mA
I_{CC3}	V_{CC} supply current	V_I = V_{CC} or GND, No load,	-20, -25		180	225 (250)	mA
	(turbo, active)	f = 1.0 MHz, *Note (7)*	-35, -45		100	180 (240)	mA

Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions: EP1810-20, EP1810-25 *Note (5)*

External Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output			22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Maximum internal frequency	*Note (7)*	50		40		0	MHz
f_{MAX}	Maximum clock frequency	*Note (10)*	62.5		50		0	MHz

Internal Timing Parameters			EP1810-20		EP1810-25		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay			6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (11)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		8		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

AC Operating Conditions: EP1810-35, EP1810-45 *Note (5)*

External Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		35		45	30	ns
t_{PD2}	I/O input to non-registered output			40		50	30	ns
t_{SU}	Global clock setup time		25		30		30	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20		25	0	ns
t_{CH}	Global clock high time		12		15		0	ns
t_{CL}	Global clock low time		12		15		0	ns
t_{ASU}	Array clock setup time		10		11		30	ns
t_{AH}	Array clock hold time		15		18		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35		45	30	ns
t_{CNT}	Minimum global clock period			35		45	0	ns
f_{CNT}	Maximum internal frequency	*Note (7)*	28.6		22.2		0	MHz
f_{MAX}	Maximum clock frequency	*Note (10)*	40		33.3		0	MHz

Internal Timing Parameters			EP1810-35		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{IN}	Input pad and buffer delay			7		6	0	ns
t_{IO}	I/O input pad and buffer delay			5		5	0	ns
t_{LAD}	Logic array delay			19		28	30	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9		11	0	ns
t_{ZX}	Output buffer enable delay			9		11	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (11)*		9		11	0	ns
t_{SU}	Register setup time		10		10		0	ns
t_{H}	Register hold time		15		18		0	ns
t_{IC}	Array clock delay			19		28	30	ns
t_{ICS}	Global clock delay			4		8	0	ns
t_{FD}	Feedback delay			6		7	–30	ns
t_{CLR}	Register clear time			24		32	30	ns

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For all Clocks: t_R and t_F = 100 ns (50 ns for military and industrial temperature versions).
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When the Turbo Bit is not set (non-turbo mode), an EP910 EPLD enters standby mode if no logic transitions occur for 100 ns (after the last transition).
(7) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP1810-20, EP1810-25, EP1810-35, EP1810-45
Industrial Temp.	(–40° C to 85° C)	EP1810-25, EP1810-45
Military Temp.	(–55° C to 125° C)	EP1810-45, *Note (1)*

Note:

(1) Only military-temperature-range devices are listed. MIL-STD-883-compliant product specifications are provided in "EP1810 MIL-STD-883-Compliant EPLD" in this data sheet and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Table 2 provides pin-out information for EP1810 devices in the PGA package.

Table 2. EP1810 PGA Pin-Outs

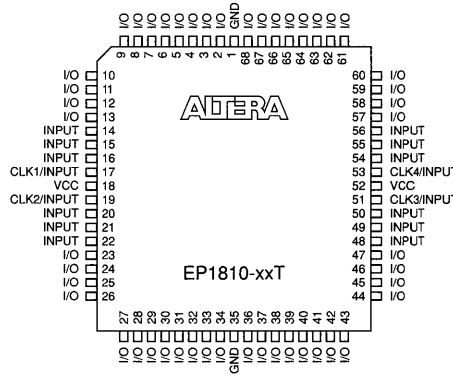
Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 20 ns, 25 ns, and 35 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- Pin-, function-, and programming file-compatible with Altera's EP1810 and EP1810 MIL-STD-883-compliant devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin one-time-programmable (OTP) plastic J-lead chip carrier (PLCC) (see Figure 31)

Figure 31. EP1810T Package Pin-Out Diagram

Package outline not drawn to scale.



68-Pin J-Lead

General Description

The Altera EP1810T EPLD is a low-cost, high-performance version of the EP1810 device. The EP1810T operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device, which is preset at the factory, is permanently turned on. For information on EP1810T architecture, refer to Figure 29 earlier in this data sheet.

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300	300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*Note (2)*		50	ns
t_F	Input fall time			50	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load, *Note (5)*	-20T, -25T		180	250	mA
			-35T		120	215	mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (5)*	-20T, -25T		180	250	mA
			-35T		120	215	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions *Note (4)*

External Timing Parameters			EP1810-20T		EP1810-25T		EP1810-35T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25		35	ns
t_{PD2}	I/O input to non-registered output			22		28		40	ns
t_{SU}	Global clock setup time		13		17		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18		20	ns
t_{CH}	Global clock high time		8		10		12		ns
t_{CL}	Global clock low time		8		10		12		ns
t_{ASU}	Array clock setup time		8		10		10		ns
t_{AH}	Array clock hold time		8		10		15		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25		35	ns
t_{CNT}	Minimum global clock period			20		25		35	ns
f_{CNT}	Internal maximum frequency	*Note (5)*	50		40		28.6		MHz
f_{MAX}	Maximum frequency	*Note (7)*	62.5		50		40		MHz

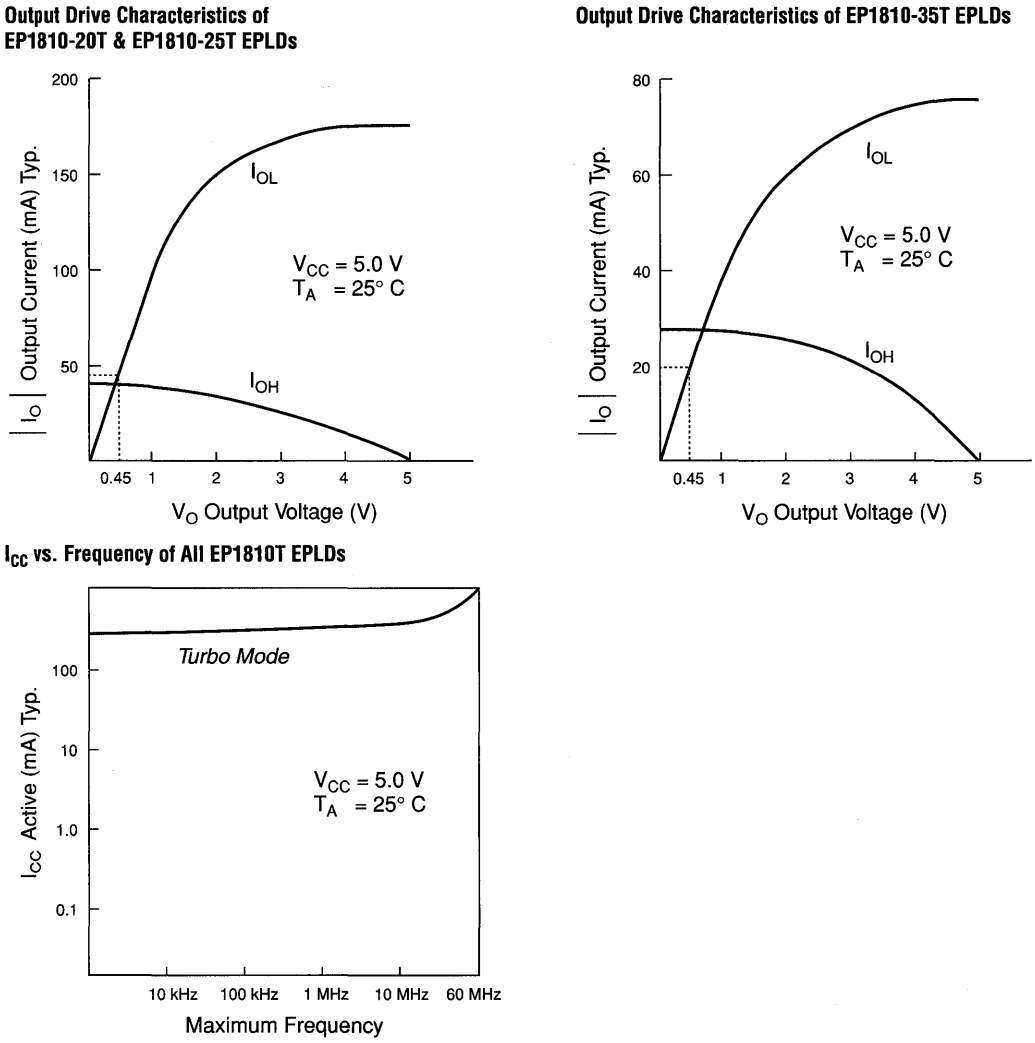
Internal Timing Parameters			EP1810-20T		EP1810-25T		EP1810-35T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		7	ns
t_{IO}	I/O input pad and buffer delay			2		3		5	ns
t_{LAD}	Logic array delay			9		12		19	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6		9	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (8)*		6		6		9	ns
t_{SU}	Register setup time		8		10		10		ns
t_{H}	Register hold time		8		10		15		ns
t_{IC}	Array clock delay			9		12		19	ns
t_{ICS}	Global clock delay			4		5		4	ns
t_{FD}	Feedback delay			3		3		6	ns
t_{CLR}	Register clear time			9		12		24	ns

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20T and EP1810-25T EPLDs: maximum V_{PP} is 14.0 V.
(2) For EP1810-20T and EP1810-25T Clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. For EP1810-35T EPLDs: Pin 19 (high-voltage pin during programming) has a maximum capacitance of 160 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) Sample-tested only for an output change of 500 mV.

Figure 32 shows the output drive characteristics of EP1810T I/O pins and typical supply current (I_{CC}) versus frequency for the EP1810T EPLD.

Figure 32. EP1810T Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP1810-20T, EP1810-25T, EP1810-35T
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

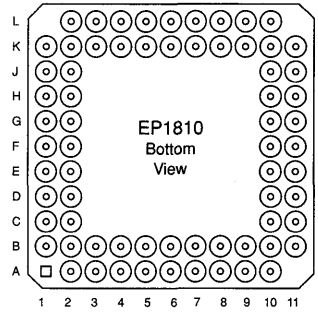
EP1810 MIL-STD-883-Compliant EPLD

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 45 ns
  - Counter frequencies up to 22.2 MHz
  - Pipelined data rates up to 33.3 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs
- Pin-, function-, and programming file-compatible with Altera's EP1810 and EP1810T devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin windowed ceramic pin-grid array (PGA) packages (see Figure 33):

Figure 33. EP1810 Package Pin-Out Diagram

Package outline not drawn to scale. See Table 3 in this data sheet for PGA package pin-out information.



68-Pin PGA

General Description

The Altera EP1810 MIL-STD-883-compliant EPLD offers LSI density, TTL-equivalent speed, and low power consumption. This device is a version of the EP1810 that complies with the military standard operating requirements listed in MIL-STD-883B. For information on the device architecture, output drive characteristics, and supply current versus frequency graphs, refer to Figures 29 and 30 earlier in this data sheet.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–0.5	7.0	V
V_{PP}	Programming supply voltage		–0.5	13.5	V
V_I	DC input voltage		–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or GND current		–400	400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–55	125	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			50	ns
t_F	Input fall time			50	ns

DC Operating Conditions *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (2)*	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (2)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (2)*		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10	10	µA
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Note (3)*		900	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (3), (4)*		40	mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (4)*		240	mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

AC Operating Conditions *Note (1)*

External Timing Parameters					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF, *Notes (6), (7)*		45	ns
t_{PD2}	I/O input to non-registered output			55	ns
t_{SU}	Global clock setup time	*Notes (6), (7)*	30		ns
t_{H}	Global clock hold time	*Note (4)*	0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF, *Note (7)*		25	ns
t_{CH}	Global clock high time		15		ns
t_{CL}	Global clock low time		15		ns
t_{ASU}	Array clock setup time	*Notes (6), (7)*	13		ns
t_{AH}	Array clock hold time	*Notes (6), (7)*	18		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF, *Notes (6), (7)*		50	ns
t_{CNT}	Minimum global clock period	*Note (7)*		45	ns
f_{CNT}	Maximum internal frequency	*Note (8)*	22.2		MHz
f_{MAX}	Maximum clock frequency	*Notes (6), (7), (9), (10)*	33.3		MHz
t_{PZX}	Input to output enable	*Notes (6), (7)*		45	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Notes (6), (7), (11), (12)*		45	ns

Notes to tables:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: V_{CC} = 5 V DC ± 10%, T_C = –55° C to 125° C
(2) Tested at 25° C and 125° C only.
(3) Tested at 25° C only.
(4) Tested with non-output loading using a data pattern specified by the device manufacturer. Data path is correlated to four 12-bit counters.
(5) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated inputs only. Pin 13 (high voltage pin during programming) has a capacitance of 50 pF.
(6) All array-dependent delays are specified for an XOR pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM pull-down. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an XOR-like pattern in which only one pure input switches at a time.
(7) When in non-turbo mode, a non-turbo adder of 30 ns maximum (40 ns for t_{ASU}) is applied. Parameters may not be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.
(8) Not tested directly, but guaranteed by testing t_{CNT} or t_{ACNT}.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) Not tested directly, but derived from t_{SU}.
(11) May not be tested, but is guaranteed to the limits specified in the table under Absolute Maximum Ratings.
(12) Sample tested only for an output change of 500 mV.

Product Availability

Product Grade	Availability
MIL-STD-883-Compliant (–55° C to 125° C)	EP1810 MIL-STD-883, *Note (1)*

Note:

(1) Only military-temperature-range devices are listed. MIL-STD-883-compliant product specifications are provided in this data sheet and in Military Product Drawings (MPDs). However, MPDs should be used to prepare Source Control Drawings (SCDs) and are available from Altera Marketing at (408) 894-7000. (For more information on MPDs and SCDs, see the *Military Products Data Sheet* in this data book.)

Pin-Out Information

Table 3 provides pin-out information for the EP1810 Military-STD-883-Compliant EPLD.

Table 3. EP1810 MIL-STD-883-Compliant PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O

Contents

August 1993

Section 6 **3.3-Volt**


ALTERA
EPM7032VLC44
ALTERA
FLEX™
EPF8282VLC84
ALTERA
EPM7032VTC44
ALTERA
FLEX™
EPF8282VTC100

3.3-Volt Programmable Logic Devices

August 1993, ver. 1 Data Sheet

Introduction

Many circuit designs demand not only higher performance and higher integration, but also lower power consumption. This requirement is especially important in electronics products such as notebook computers and personal communicators, which must consume less power to extend the life of a battery. The recent proliferation of 3.3-V microprocessors and support hardware also illustrate the need for low-power ICs.

Altera has long been a pioneer in providing low-power programmable logic. The Classic family provided the first "zero-power" EPLDs, and MAX 7000 devices offered the first user-programmable power-saver mode.

Altera remains at the forefront of the low-power programmable logic field by offering new 3.3-V programmable logic devices. This data sheet provides information on Altera's 3.3-V devices:

- EPM7032V (MAX 7000 device family)
- EPF8282V (FLEX 8000 device family)

Notes:

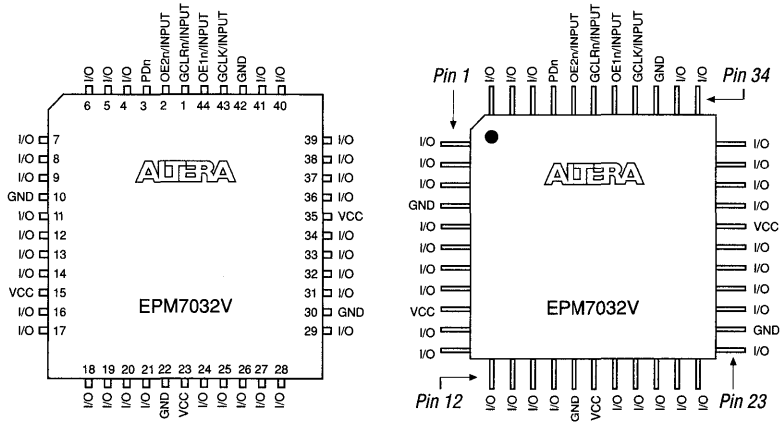
Features...

Preliminary Information

- 3.3-V version of the popular EPM7032 EPLD
  - Combinatorial speeds with t_{PD} = 12 ns
  - Clock frequencies up to 90.9 MHz
- Innovative power-saving features
  - 30% to 50% power savings over 5-V operation
  - Power-down mode controlled by a power-down pin to allow zero power consumption during periods of inactivity
  - Programmable power-saver mode for up to 50% power reduction during active operation, configurable for each macrocell
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture allowing up to 36 inputs or 32 outputs
- 32 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Programmable registers configurable as D, T, JK, and SR flipflops with individual Clear, Preset, Clock, and Clock Enable controls
- Independent clocking of all registers from array or global Clock signals
- Available in 44-pin plastic packages (see Figure 1):
  - J-lead chip carrier (PLCC)
  - 1.0-mm thin quad flat pack (TQFP)

Figure 1. EPM7032V Package Pin-Out Diagrams

Package outlines not drawn to scale.



...and More Features

- Pin-, function-, and programming-file-compatible with 5-V EPM7032 devices
- Software design support featuring Altera's MAX+PLUS II development system on PC, Sun SPARCstation, and HP 9000 Series 700 platforms
- Programming support from Altera's Master Programming Unit (MPU) or programming hardware from other manufacturers

General Description

The general characteristics of the EPM7032V are identical to those of the 5-V EPM7032, with the exceptions noted in this data sheet. See the *MAX 7000 Programmable Logic Device Family Data Sheet* in this data book for complete information on MAX 7000 EPLDs.

The EPM7032V is a high-performance MAX 7000 EPLD that meets the low power and voltage requirements of 3.3-V applications ranging from notebook computers to battery-operated, hand-held equipment. Fabricated on a 0.8-micron EEPROM technology, the EPM7032V provides in-system speeds up to 125 MHz and propagation delays of 12 ns. Its architecture supports 100% TTL emulation and can integrate SSI, MSI, and custom logic functions. The EPM7032V can replace multiple 20- and 24-pin PLDs. It is available in 44-pin reprogrammable PLCC or TQFP packages and can accommodate designs with up to 36 inputs and 32 outputs.

The EPM7032V provides a unique power-down mode that is ideal for power-sensitive applications. A dedicated power-down pin allows the device to be powered down to a near-zero-power consumption level. While in power-down mode, all internal logic and external I/O signals of the EPM7032V maintain the state just prior to the assertion of the power-down pin. When this pin is released, the device resumes normal operation.

The EPM7032V also provides programmable speed and power optimization. Speed-critical portions of a design can run at high speed and full power, while the remainder runs at reduced speed and low power. This feature enables the user to configure individual macrocells to operate at up to 50% less power while adding only a nominal timing delay.

Power Management

The 3.3-V operation of the EPM7032V offers power savings of 30% to 50% over the 5-V operation of the EPM7032. Power-saving features of the EPM7032V include a programmable power-saver mode and a power-down mode.

Programmable Speed/Power Control

All MAX 7000 devices, including the EPM7032V, offer a power-saver mode that supports low-power operation across user-defined signal paths or the entire device. This feature can reduce total power dissipation by up to 50%, since most logic applications require only a fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in the EPM7032V for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal additional timing delay (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

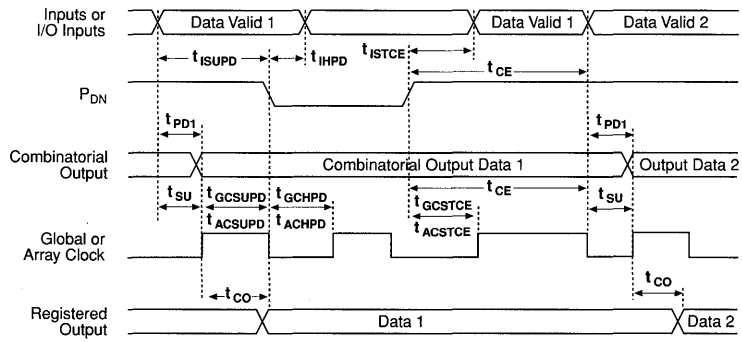
Power-Down Mode

The EPM7032V provides a power-down mode that allows the device to consume near-zero power (typically 50 µA). The power-down mode is controlled externally by the dedicated power-down pin (PDn). When PDn is asserted (i.e., brought to ground), the power-down sequence latches all inputs, internal logic, and output pins of the EPM7032V, preserving their present state. Output pins maintain their present low, high, or tri-state (high-impedance) value while in power-down mode. Once in power-down mode, any or all of the inputs, including Clocks, can be toggled without affecting the frozen state of the device. Since internal latches are used to ensure that the proper state exists during power-down mode, the external inputs and Clocks must meet certain setup and hold time requirements. See Figure 2 and the "Power-Down Timing Parameters and Chip-Enable Timing Parameters" tables, later in this data sheet.

Figure 2. Power-Down Mode Switching Waveforms

The switching waveforms for the EPM7032V are identical to those of the 5-V EPM7032 in all modes except for the additional power-down mode shown here.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



When the PDn signal is brought high, the device is enabled, and the combinatorial outputs respond to the present input conditions within the specified chip-enable delay (t_{CE}). Registered outputs respond to Clock transitions within t_{CE}. Clocking the device during the chip-enable sequence can cause the data to change internal to the chip if a Clock transition occurs during certain intervals of the chip-enable or chip-disable sequences. All Clocks should be gated to prevent Clock transitions during the Clock setup time (t_{GCSUPD} or t_{ACSUPD}) and during the chip-enable setup time (t_{GCSTCE} or t_{ACSTCE}), as shown in Figure 2. All registers in the EPM7032V provide Clock Enable control for simple access to disable Clocks. If output signals must be frozen in a high-impedance state during power-down, the associated Output Enable signal must be asserted, the system Clock must be removed, and the PDn pin must be asserted. To reactivate the device, the sequence is reversed. For some systems, it may be more appropriate to switch the order of the Clock and Output Enable controls.

All power-down/chip-enable timing parameters are computed from external input or I/O pins, with the macrocell Turbo Bit turned on, and without the use of parallel expanders. For macrocells in low-power mode (Turbo Bit off), the low-power adder t_{LPA} must be added to the power-down/chip-enable timing parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH}, and t_{SEXP}. For macrocells that use parallel expanders, t_{PEXP} must be added. For data or Clock paths that use more than one logic array delay, the worst-case data or Clock delay also must be added to the respective power-down/chip-enable parameters. Actual worst-case timing for data and Clock paths can be calculated with the MAX+PLUS II Simulator or Timing Analyzer, or other industry-standard CAE verification tools.

Design Security

All MAX 7000 devices, including the EPM7032V, contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when the device is erased.

Generic Testing

The EPM7032V is functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under the conditions equivalent to those shown in Figure 3.

Test patterns can be used and then erased in the EPLD during early stages of the device production flow.

Figure 3. EPM7032V AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.

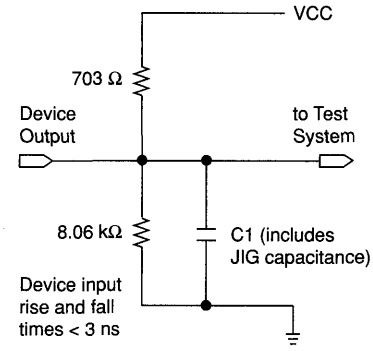


Figure 4 shows the output drive characteristics of EPM7032V I/O pins.

Figure 4. Typical EPM7032V Output Drive Characteristics

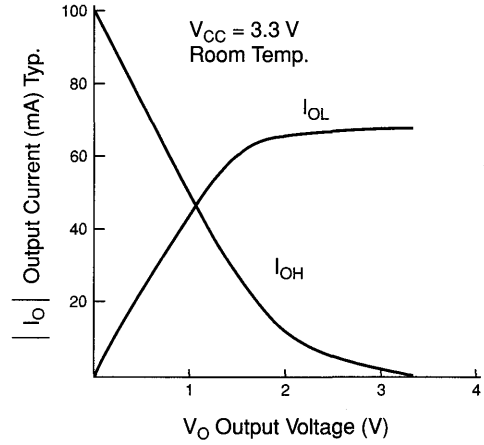
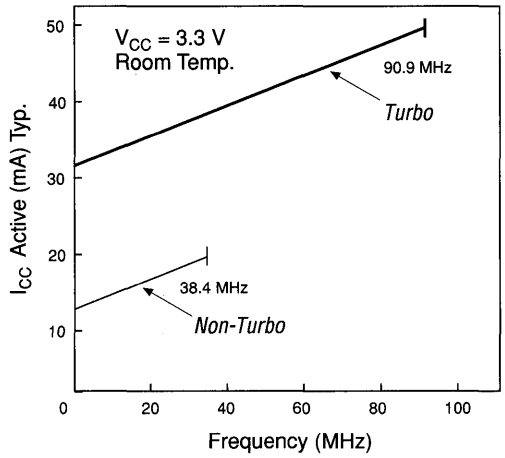


Figure 5 shows typical supply current versus frequency for the EPM7032V.

Figure 5. EPM7032V I_{CC} vs. Frequency



I_{CC} is calculated with the following equation:
$I_{CC} = (0.98 \times MC_{TON}) + (0.42 \times MC_{TOFF}) + [(0.006 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 3.3V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB and no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	5.6	V
V_I	DC input voltage	*Note (1)*	–2.0	5.6	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –0.1 mA DC	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC0}	V_{CC} supply current (standby, power-down mode)	*Note (4)*		20	150	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load, *Note (4)*		10	20	mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		15	25	mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		7		8		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		4		5		ns
t_{AH}	Array clock hold time		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		2		3	ns
t_{IO}	I/O input pad and buffer delay			3		2		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		1		2	ns
t_{LAD}	Logic array delay			4		6		8	ns
t_{LAC}	Logic control array delay			4		6		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		5		4		4		ns
t_{H}	Register hold time		4		4		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			4		6		8	ns
t_{EN}	Register enable time			4		6		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*Note (7)*		15		17		20	ns

Power-Down/Chip-Enable Timing Parameters

Power-Down Timing Parameters		EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISUPD}	Input or I/O input setup time before power down	30		30		35		ns
t_{IHPD}	Input or I/O input hold time after power down	0		0		0		ns
t_{GCSUPD}	Global clock setup time before power down	20		20		25		ns
t_{GCHPD}	Global clock hold time after power down	0		0		0		ns
t_{ACSUPD}	Array clock setup time before power down	30		30		35		ns
t_{ACHPD}	Array clock hold time after power down	0		0		0		ns
t_{HPD}	Minimum high pulse width of power-down pin	800		800		900		ns
t_{LPD}	Minimum low pulse width of power-down pin	800		800		900		ns
t_{PDOWN}	Power down delay		800		800		900	ns

Chip Enable Timing Parameters		EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**		**Max**		**Max**		**Max**	**Unit**
t_{ISTCE}	Input or I/O input stable after chip enable		60		60		70	ns
t_{GCSTCE}	Global clock stable after chip enable		60		60		70	ns
t_{ACSTCE}	Array clock stable after chip enable		60		60		70	ns
t_{CE}	Data stable after chip enable		700		700		800	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to V_{CC} + 2 V for periods shorter than 20 ns under no-load conditions during normal operation.

(2) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.

(3) Operating conditions: V_{CC} = 3.3 V ± 10%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 3.3 V ± 10%, T_A = –40° C to 85° C for industrial use.

(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C .

(5) Capacitance measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

(6) The f_{MAX} values represent the highest frequency for pipelined data.

(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

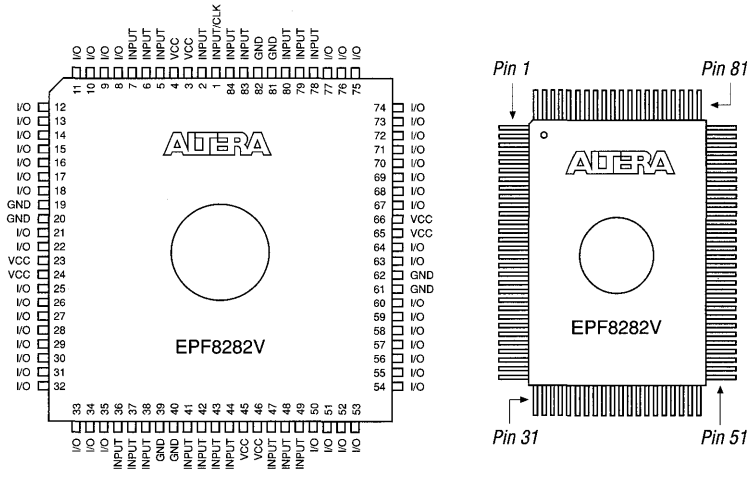
Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7032V-12, EPM7032V-15, EPM7032V-20
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

Notes:

Features

- 3.3-V version of the EPF8282 device
- High-density, register-rich programmable logic device
  - 1,250 gates, 282 registers
  - 78 I/O pins and 4 dedicated inputs
- Fabricated on a 0.8-micron CMOS SRAM technology
- In-circuit reconfigurable
- FastTrack continuous routing structure for fast, predictable interconnect delays
- Available in plastic packages (see Figure 6):
  - 84-pin J-Lead chip carrier (PLCC)
  - 100-pin thin quad flat pack (TQFP)
- Input/output registers on all I/O pins
- Dedicated carry chain that can implement fast adders and counters
- Built-in cascade chain for efficient implementation of high-speed, high-fan-in logic functions
- Low power consumption (less than 1 mA in standby mode)
- Programmable output slew-rate control to reduce switching noise
- Built-in Joint Test Action Group (JTAG) Boundary-Scan test circuitry
- Software design support and automatic place-and-route with Altera's MAX+PLUS II development system for PC, Sun SPARCstation, and HP 9000 Series 700 platforms
- Pin-, function-, and programming-file-compatible with 5-V EPF8282 devices

Figure 6. EPF8282V Package Pin-Out Diagrams



84-Pin J-Lead

100-Pin QFP

General Description

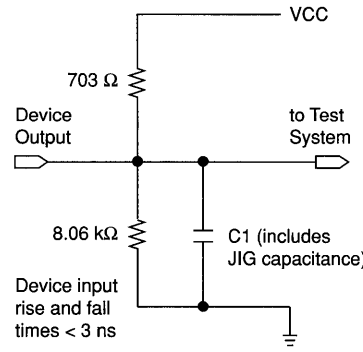
The general characteristics of the EPF8282V are identical to those of the 5-V EPF8282, with the exceptions noted in this data sheet. For detailed information on FLEX 8000 devices, refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book.

Generic Testing

Each FLEX 8000 device is functionally tested and guaranteed. Complete testing of each configurable SRAM bit and all internal logical elements ensures 100% configuration yield. AC test measurements for 3.3-V FLEX 8000 devices are made under conditions equivalent to those shown in Figure 7. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 7. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			600	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2.2	W
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Ambient temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = 0.1 mA DC	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (3)*		300		µA

Capacitance *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Internal Timing Characteristics *Note (5)*

I/O Element (IOE) Output Timing Parameters			EPF8282V-3		EPF8282V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OUTSU}	Setup time for output register		3.0		3.0		ns
t_{OUTH}	Hold time for output register		0		0		ns
t_{OUTCO}	Clock-to-output time for output register	C1 = 35 pF		8.1		10.8	ns
t_{OUT}	Combinatorial time for I/O output			6.3		9.0	ns
t_{OUTCLR}	Clear time for output register			8.4		11.1	ns
t_{XZ}	Valid to Z time for IOE	C1 = 5 pF		6.3		9.0	ns
t_{ZX}	Z to valid time for IOE	C1 = 35 pF		6.3		9.0	ns

I/O Element (IOE) Input Timing Parameters			EPF8282V-3		EPF8282V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{INSU}	Setup time for input register		4.5		4.5		ns
t_{INH}	Hold time for input register		0		0		ns
t_{INCO}	Clock-to-output time for input register			3.0		4.5	ns
t_{IN}	Input pad and buffer delay			2.7		4.2	ns
t_{INCLR}	Clear time for input register			3.3		4.8	ns

Logic Element (LE) Timing Parameters			EPF8282V-3		EPF8282V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LESU}	Setup time for LE register		3.8		5.6		ns
t_{LEH}	Hold time for LE register		0		0		ns
t_{LECO}	Clock-to-output time for LE			5.0		6.0	ns
t_{LE}	Combinatorial time for LE			7.5		9.0	ns
t_{LECLR}	Clear time for LE register			5.4		6.5	ns
t_{LEPRE}	Preset time for LE register			5.4		6.5	ns
t_{CICO}	Carry-in to carry-out time			1.1		1.7	ns
t_{CGEN}	Carry generation time			3.5		5.0	ns
t_{CASC}	Cascade-in to cascade-out time			1.7		3.0	ns
t_{CSU}	Carry-in to register setup time		2.4		3.6		ns
t_{COUT}	Carry-in to LE out delay			6.1		7.0	ns

Interconnect Timing Parameters			EPF8282V-3		EPF8282V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade time between LEs in different LABs			0.8		1.4	ns
$t_{LABCARRY}$	Carry time between LEs in different LABs			0.8		0.9	ns
t_{COL}	Column interconnect routing delay			3.8		3.8	ns
t_{DIN}	Dedicated input pad delay			4.5		6.0	ns
t_{LOCAL}	LAB local interconnect delay			1.5		1.5	ns
t_{DINROW}	Dedicated input routing delay	*Note (6)*		4.5		5.3	ns
t_{ROW}	Row interconnect routing delay			6.3		6.3	ns

External Reference Timing Characteristics *Note (7)*

			EPF8282V-3		EPF8282V-4		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	I/O pin to I/O pin via row, LE, and column	C1 = 35 pF		27		32	ns
t_2	I/O pin to I/O pin via row, LE, and row			29		35	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Operating conditions: $V_{CC} = 3.3\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.

(3) Typical values are for $T_A = 25°\ C$ and $V_{CC} = 3.3\ V$.

(4) Capacitance is sample-tested only.

(5) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(6) The t_{ROW} and t_{DINROW} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(7) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

Notes:

Contents

August 1993

Section 7 **Function-Specific**

EPS448 SAM EPLD

Stand-Alone Microsequencer

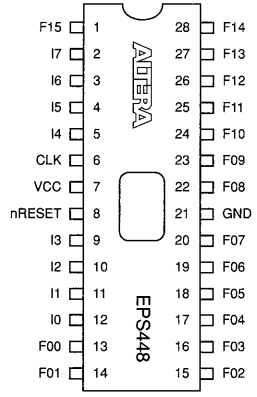
August 1993, ver. 4 | Data Sheet

Features

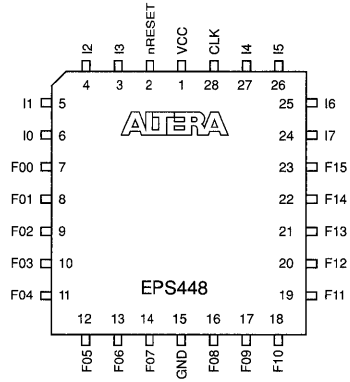
- User-configurable Stand-Alone Microsequencer (SAM) EPLD for implementing high-performance controllers
- On-chip reprogrammable microcode EPROM up to 448 words deep
- 15 × 8-bit stack
- Loop counter
- Prioritized multiway control branching
- 8 general-purpose branch-control inputs and 16 general-purpose control outputs
- Cascadable to expand the number of outputs or states
- Low-power CMOS technology
- Available in 28-pin windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 1):
  - Dual in-line (CerDIP and PDIP)
  - J-lead chip carrier (plastic PLCC only)
- Clock frequencies up to 25 MHz
- High-level support with SAM+PLUS design tools that include Altera State Machine Input Language (ASMILE), Assembly Language (ASM), SAM Design Processor (SDP), and SAMSIM functional simulator

Figure 1. EPS448 Package Pin-Out Diagrams

Package outlines not drawn to scale.
Windows in ceramic packages only.



28-Pin DIP



28-Pin J-Lead

General Description

The EPS448 EPLD is a function-specific, user-configurable Stand-Alone Microsequencer (SAM). The on-chip EPROM (up to 448 words) of the EPS448 is integrated with branch-control logic, a pipeline register, a stack,

and a loop counter. This generic microcoded architecture can efficiently implement a broad range of high-performance controllers, from state machines to waveform-generation applications.

The 1.2-micron CMOS EPROM technology allows the EPS448 EPLD to operate at 25-MHz Clock frequency while still benefitting from low CMOS power consumption. This technology also facilitates 100% generic testability, which eliminates the need for post-programming testing.

Altera's SAM+PLUS software provides design entry, logic optimization, and functional simulation for EPS448 designs. With SAM+PLUS, designs are entered in either state machine or microcode format. The software automatically performs logic minimization and design fitting. The designer can then simulate the design or program it directly to create customized working silicon. Programming takes only a few minutes with standard Altera programming hardware and MAX+PLUS II software. For more information, see the *Altera Programming Hardware Data Sheet* in this data book.

Applications

Applications ideally suited for the EPS448 include programmable sequence generators (i.e., state machines), bus and memory control functions, graphics and DSP algorithm controllers, and other high-performance control logic. EPS448 devices can be cascaded horizontally for greater output capabilities and vertically for deeper microcode memory. See *Application Brief 65 (Vertical Cascading of EPS448 SAM EPLDs)* in the Altera 1992 ***Applications Handbook***.

State Machines

EPS448 architecture easily implements synchronous state machines. The device's internal EPROM memory and pipeline register allow up to 448 unique states to be specified. Its branch-control logic allows single-Clock, multiway branching based on the eight inputs, the current device state, and the user-defined transition conditions. Design entry is simplified with the Altera State Machine Input Language (ASMILE), which is supported by SAM+PLUS software. This high-level language uses `IF-THEN` statements to define state transitions and truth tables to define or tri-state the outputs on a state-by-state basis.

Microcoded Controllers

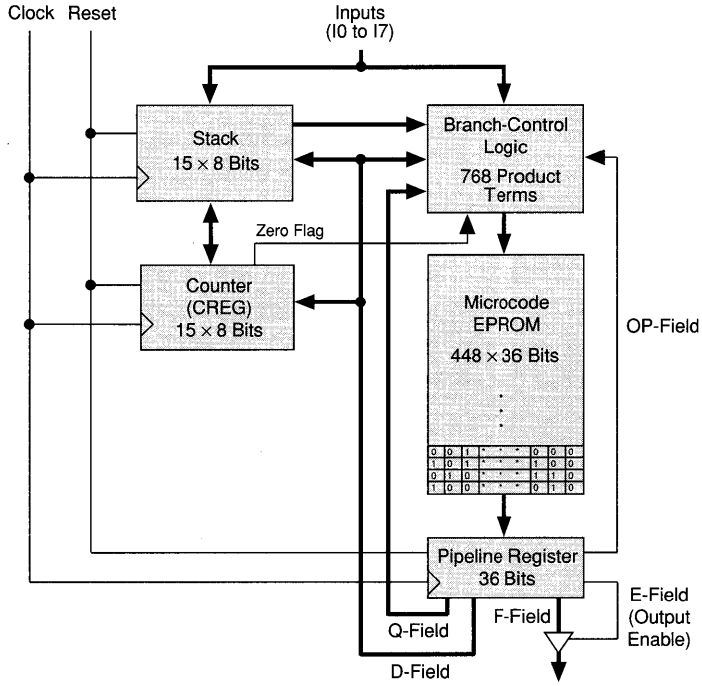
EPS448 architecture provides advanced features that make it suitable for use as a complex microcoded controller. The 448-word on-chip EPROM is integrated with a microcode sequencer consisting of branch-control logic, a stack, and a loop counter. The branch-control logic—fed by the 8 general-purpose inputs, counter, stack, and pipeline register—provides flexible, multiway microcode branch capability in a single Clock cycle, enhancing throughput beyond that of conventional controllers or sequencers.

For microcoded controllers, SAM+PLUS software offers the high-level Assembly Language (ASM) design entry format. This language consists of powerful instructions (i.e., opcodes) that easily implement conditional branches, subroutine calls, multi-level FOR-NEXT loops, and dispatch functions (i.e., branching to an externally specified address). For more information, see "Instruction Set" later in this data sheet.

Functional Description

The EPS448 EPLD consists of a microcode EPROM, a 36-bit pipeline register, branch-control logic, a 15 × 8-bit stack, and an 8-bit loop counter. See Figure 2.

Figure 2. EPS448 Block Diagram



The branch-control logic generates the address of the next state and applies it to the microcode memory. The outputs of the microcode memory represent user-defined outputs and internal control values associated with the next state. These new values are clocked into the pipeline register on the leading edge of the Clock and become the current state. The branch-control logic uses the new values in the pipeline register—along with the counter, stack, and inputs—to generate the new next-state address.

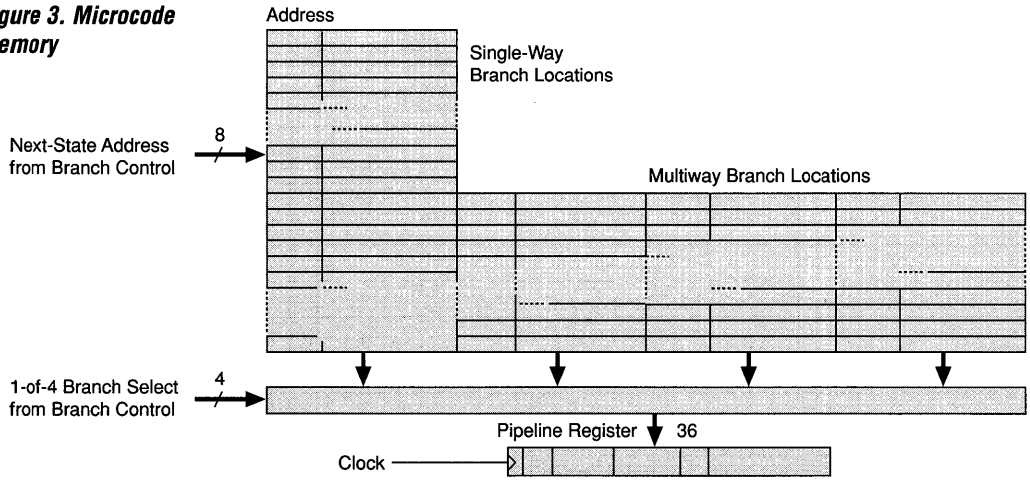
Microcode EPROM & Pipeline Register

The microcode EPROM is organized into 448 36-bit words, each of which can be viewed as a single state location. Each of the 36 bits is divided into the following categories:

Field:	Size:	Description:
F-field	16 bits	Consists of user-defined outputs at device pins.
Q-field	8 bits	Provides the next-state address.
D-field	8 bits	General-purpose field used either as a constant or as an alternative next-state address.
OP-field	3 bits	Contains the instruction (opcode).
E-field	1 bit	Enables or tri-states the device outputs.

As shown in Figure 3, the microcode memory is organized as 256 addresses. Addresses 0 through 191 contain a single 36-bit word, which is associated with the desired next state. This state information is clocked into the pipeline register on the rising edge of the Clock, and the outputs become valid one Clock-to-output delay (t_{CO}) later.

Figure 3. Microcode Memory



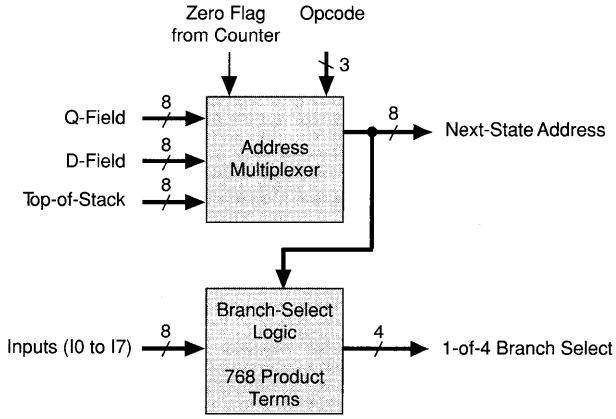
Each address location between 192 and 255 accesses 4 unique 36-bit instructions. Each of these four instructions corresponds to a different possible next state. (The extensions `.0`, `.1`, `.2`, and `.3` are added to distinguish the four states.) These 64 addresses make up the multiway branch locations, and are used to perform single-Clock, 4-way branching. Whenever the next-state address falls within the multiway branch locations, the branch-control logic makes the necessary 1-of-4 selection based on the next-state address and user-defined input conditions.

Branch-Control Logic Block

The branch-control logic block is the key to the high-performance sequencing ability of the EPS448 EPLD. This block determines the next state to be clocked into the pipeline register, based on the current status of the pipeline register, the counter, the stack, and the eight input pins.

The branch-control logic is divided into two segments: the address multiplexer and the branch-select logic. See Figure 4.

Figure 4. Branch-Control Logic



The address multiplexer provides the next-state address to the microcode memory. The next-state address can come from the Q-field, the D-field, or the top-of-stack. The selection is based on the instruction in the pipeline register and the condition of the zero flag from the counter.

The branch-select logic is a programmable logic block with 768 product terms, 16 inputs, and 4 outputs. It is used to perform a 2-, 3-, or 4-way branch based on user-defined input conditions. When the next-state address falls within the multiway branch range of memory—i.e., any address greater than 191—the branch-select logic performs the necessary 1-of-4 selection. When the next-state address is less than 192, no selection is required and the branch-select logic is turned off.

The conditions controlling the multiway branch are defined by the user in a simple `IF-THEN-ELSE` format, as shown in the following example:

```
IF       (cond3)    THEN   select 201.3
ELSEIF   (cond2)    THEN   select 201.2
ELSEIF   (cond1)    THEN   select 201.1
ELSE                       select 201.0
```

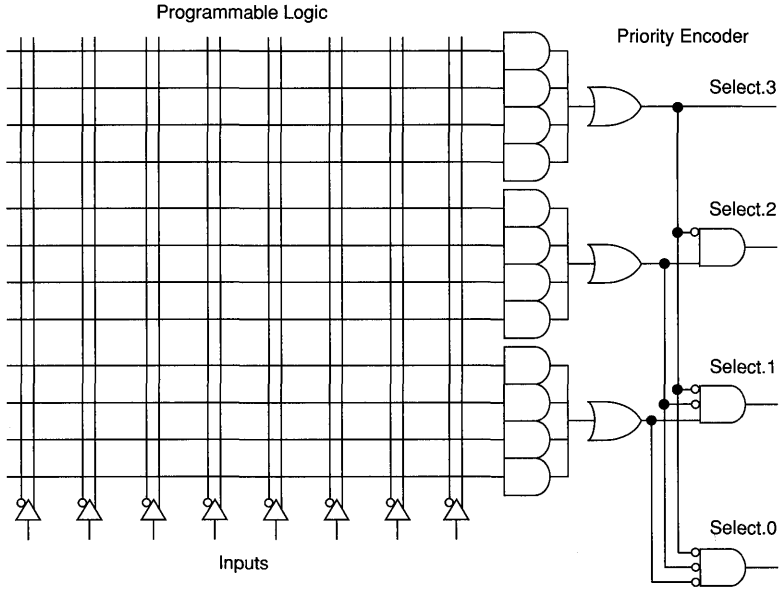
The conditions are prioritized so that if the first condition (i.e., cond3) is met, then microword 201.3 is selected and clocked into the pipeline register, regardless of the results of cond2 and cond1. If no conditions are met, then microword 201.0 is clocked into the pipeline resister.

The three conditional expressions are user-defined. They can contain any logical equation that is based on the inputs and can be reduced to four product terms, as shown in the following example:

```
cond1  =   I1 * /I2 * /I4
         + I3 * /I4 * /I5 * /I6 * /I7
         + I0
         + I2 * /I4 * /I5
```

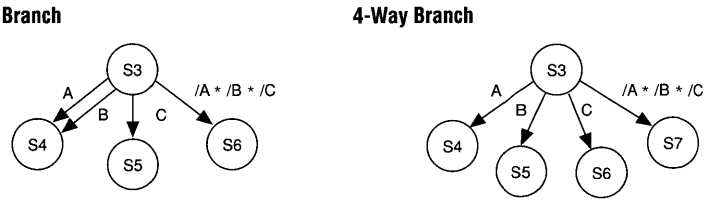
A unique set of 12 product terms is present in each of the 64 available multiway branch locations for a total of 768 product terms. Figure 5 shows how each set is used to select the appropriate instruction.

Figure 5. Branch Logic in a Multiway Branch Location



The EPS448 EPLD is designed so that the number of available product terms is always sufficient for a design. Prioritization provides an effective product-term count of more than 12 per location. A tradeoff between the number of product terms and the number of possible branches can be made simply by placing identical state information in 2 locations, as shown in Figure 6.

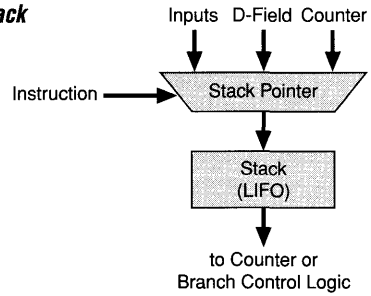
Figure 6. Multiway Branching vs. Product-Term Needs



Stack

The EPS448 stack is a Last-In First-Out (LIFO) arrangement that consists of 15 × 8-bit words. The top of stack can be selected by the branch-control logic as the next-state address or popped into the counter. Values can be pushed onto the stack from either the D-field in the pipeline register or from the counter. Therefore, subroutines, nested loops, and other iterative structures can be implemented efficiently. The logic levels on the 8 dedicated input pins can also be pushed onto the stack to allow external address specification in a dispatch function or to externally load the counter. See Figure 7.

Figure 7. Stack

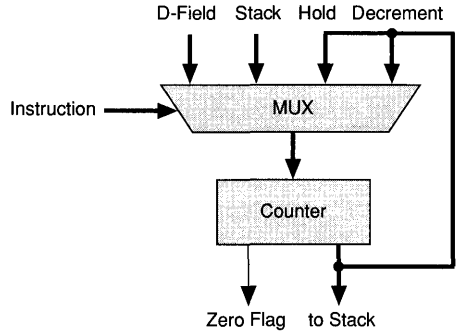


The pushing or popping of the stack occurs on the leading edge of the Clock. The stack is "zero-filled" so that a pop from an empty stack resets all 8 bits to zero. On the other hand, a push to a full stack writes over the top-of-stack, leaving the other 14 values unchanged.

Loop Counter

The EPS448 EPLD contains an 8-bit loop counter, called count register (CREG), that is useful for controlling timing loops and determining branch-control functions. The CREG is a down counter that can be loaded directly from the D-field of the pipeline register or from the top-of-stack. The value of the CREG can be saved and restored by pushing and popping it to and from the stack. See Figure 8.

Figure 8. Loop Counter (CREG)



The CREG is loaded or decremented on the leading edge of the Clock. It stops decrementing once it reaches zero, thereby preventing roll-over. A zero flag indicates when the counter has reached zero. This flag is used with the LOOPNZ command to control program flow. (See "Instruction Set" later in this data sheet.) Single-instruction delay loops are easily constructed, and nested loops or delays of arbitrary length can be generated in combination with the stack.

Output Enable Control

Each microcode word contains an Output Enable bit (i.e., the E-field) that enables all outputs when E = 1, and causes high impedance when E = 0. This bit is accessible through instruction set commands provided with SAM+PLUS software. This Output Enable capability allows EPS448 EPLDs to be vertically cascaded to increase the number of states.

nRESET Pin

The nRESET pin acts as a master Reset for the EPS448 EPLD, causing it to empty the stack, clear the counter, and load the microword at address 0 into the pipeline register. The nRESET signal is useful for system reset or for synchronizing several horizontally or vertically cascaded EPS448 devices.

The nRESET signal must be held low for at least three rising Clock edges to reset the EPS448 EPLD. Allowing nRESET to go high before the third rising Clock edge causes the EPS448 device to enter an undefined state.

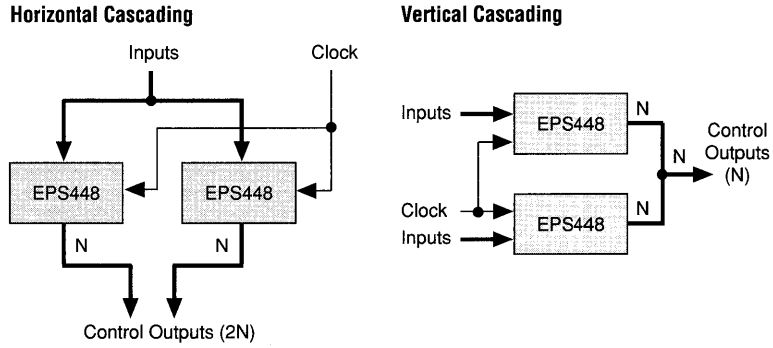
The outputs of the startup address (00 Hex) appear at the pins after the fourth rising Clock edge after nRESET goes low, and are maintained until the third rising Clock edge after nRESET returns to high.

When the EPS448 EPLD is operating in noisy environments, a glitch on the nRESET pin during one setup cycle (t_{SUR}) before the Clock edge may cause it to enter an undefined state. To prevent this effect, a capacitor of at least 0.1 µF should be connected from the nRESET input to GND.

Horizontal & Vertical Cascading

EPS448 EPLDs, like memory- and bit-slice devices, can be cascaded to provide greater functionality (see Figure 9). If an application requires more output lines, two or more EPS448 devices can be cascaded horizontally. Likewise, if an application requires more states, two or more EPS448 EPLDs can be cascaded vertically. In either case, no delay is incurred. The user can also simultaneously cascade EPS448 devices horizontally and vertically. The SAM+PLUS development software automatically implements horizontal cascading when a design specifies more than the 16 available outputs. However, vertical cascading requires the designer to make certain tradeoffs to split the design. Refer to *Application Brief 65 (Vertical Cascading of EPS448 SAM EPLDs)* in the 1992 ***Applications Handbook*** for more information.

Figure 9. Horizontal and Vertical Cascading



Instruction Set

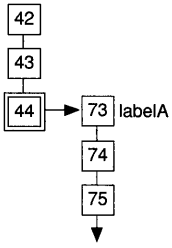
The instruction set used to enter designs for the EPS448 EPLD consists of a compact assortment of powerful commands for efficient implementation of multiway branching, subroutines, nested `FOR-NEXT` loops, and dispatch functions. These instructions are used only with Assembly Language (ASM) design entry.

Each command in the instruction set is described and illustrated in this section. In the following descriptions, `labelA` and `labelB` represent arbitrary labels located in the ASM file. These symbolic labels are converted into 8-bit absolute addresses by the SAM+PLUS software. (SAM+PLUS allows the designer to use the high-level Assembly Language without worrying about the actual values that are placed in the various fields.) The parameter constant is any 8-bit number (0 to 255 decimal, 0 to FF hexadecimal) that represents an address, a mask, or a constant.

For simplicity, it is assumed that the sample destination labels in the following descriptions are not in the multiway branch block. See "Multiway Branching" later in this data sheet.

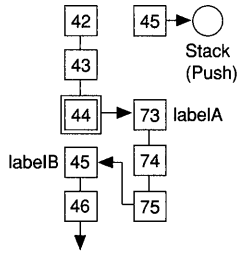
CONTINUE

This command causes execution to continue with the next sequential instruction in the ASM file. In this example, the current address is 44, and CONTINUE instructs SAM+PLUS to go to address 45 in the ASM file.



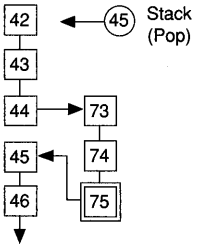
JUMP labelA

This instruction causes execution to branch to the indicated location. In this example, address 44 contains the instruction JUMP labelA; labelA is located at address 73. The next instruction comes from labelA.



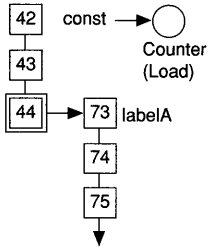
CALL labelA RETURNTO labelB

This instruction pushes the address of labelB onto the stack and makes labelA the next-state address. CALL labelA without the RETURNTO command makes labelB default to the next instruction in the ASM file. In this example, the address location 44 contains the instruction CALL labelA; labelA is located at address 73. The instruction pushes the address of the next instruction (45) onto the stack and causes the next instruction to come from address 73. The RETURN instruction at address 75 returns the execution to address 45. The CALL command is typically used to call a subroutine.



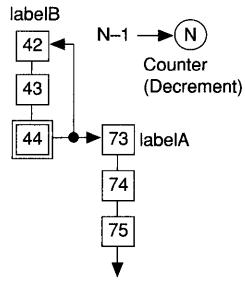
RETURN

This command causes the address of the next instruction to come from the top-of-stack and pops that value off the stack. In this example, the instruction at address 44 calls the subroutine at address 73 and pushes the value 45 onto the stack. The RETURN instruction at address 75 pops the value 45 off of the top-of-stack and causes execution to continue with address 45. RETURN is most frequently used to return from a subroutine.



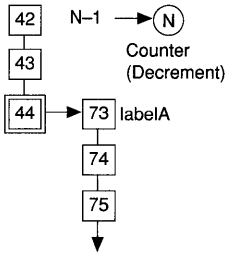
LOADC constant GOTO labelA

This command loads the counter with the specified value and then executes the instruction at labelA. If GOTO is not included in the instruction, labelA defaults to the next instruction in the ASM file. In this example, the instruction LOADC 173D GOTO labelA is located at address 44. This command specifies that the decimal value 173 is loaded into the counter and that the next state comes from labelA at address 73. LOADC is typically used to load the counter before entering a FOR-NEXT loop or a wait-state generator.



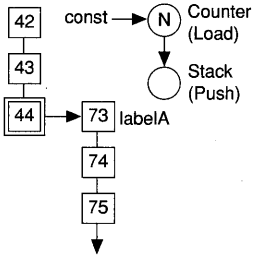
LOOPNZ labelB ONZERO labelA

This instruction jumps to one of two addresses based on the value of the zero flag, and decrements the counter if it is not already zero. If it is zero (i.e., zero flag = 1), the next instruction comes from labelA. If it is not zero (i.e., zero flag = 0), the next instruction comes from labelB. If the ONZERO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is LOOPNZ labelB ONZERO labelA, where labelB is located at address 42 and labelA at address 73. If the counter is not at zero, the instruction at address 42 is executed and the counter is decremented. If the counter is already at zero, the instruction at address 73 is executed and the counter remains at zero. LOOPNZ is typically used to implement FOR–NEXT loops.



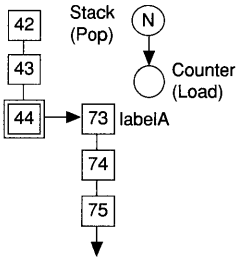
DECNZ GOTO labelA

This command decrements the counter if it is not zero and then jumps to the instruction specified at labelA. If GOTO is not included in the instruction, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is DECNZ GOTO labelA, where labelA is located at address 73. The counter is decremented if it is not zero and the next instruction comes from address 73. DECNZ is typically used to conditionally decrement the counter.



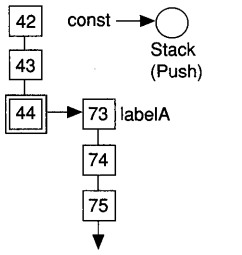
PUSHLOADC constant GOTO labelA

This instruction pushes the current value of the counter onto the stack, loads a new value into the counter, and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is PUSHLOADC 153D GOTO labelA, where labelA is located at address 73. The value in the counter is pushed onto the stack, the decimal value 153 is loaded into the counter, and the next instruction comes from address 73. PUSHLOADC is useful for implementing FOR–NEXT loops.



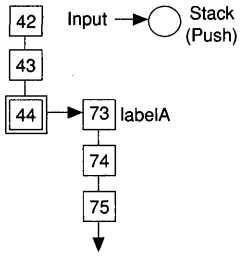
POPC GOTO labelA

This command pops the top-of-stack into the counter and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is POPC GOTO labelA, where labelA is located at address 73. The current value at the top-of-stack is removed from the stack (i.e., popped) and loaded into the counter. The next instruction comes from address 73. POPC is typically used with the PUSHLOADC instruction to implement nested FOR–NEXT loops.



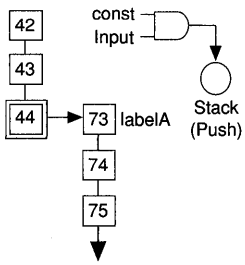
PUSH constant GOTO labelA

This command pushes the value of the constant onto the stack and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is PUSH 34D GOTO labelA, where labelA is located at address 73. The decimal value 34 is pushed onto the stack and the next instruction comes from address 73. PUSH is typically used to store a value on the stack.



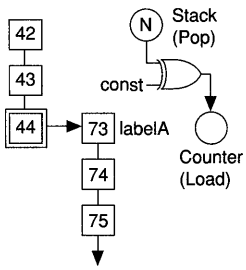
PUSHI GOTO labelA

This instruction pushes the eight inputs (I7 to I0) onto the stack. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is PUSHI GOTO labelA, where labelA is located at address 73. At the leading edge of the Clock, the eight inputs are pushed onto the stack. Typically, address 73 would have a RETURN instruction that would cause execution to jump to the address represented by the recently pushed input pins, implementing a dispatch function. This instruction can also be used to load the counter with an externally specified variable. To do so in this example, address 73 would have a POPC instruction.



ANDPUSHI constant GOTO labelA

This command pushes the eight inputs (I7 to I0) onto the stack. It is identical to the PUSHI GOTO labelA command, except that the inputs are first bit-wise ANDed with a constant to allow the masking of irrelevant inputs. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is ANDPUSHI 34D GOTO labelA, where labelA is located at address 73. At the leading edge of the Clock, the eight inputs are masked with the decimal constant 34 and pushed onto the stack. The next instruction comes from address 73. ANDPUSHI is an advanced instruction typically used to branch to an externally specified resource or to externally load the counter.



POPXORC constant GOTO labelA

This instruction pops the top-of-stack, bit-wise XORs it with a constant, loads the results into the counter, and jumps to labelA. If the GOTO instruction is not included, labelA defaults to the next instruction in the ASM file. In this example, the instruction at address 44 is POPXORC 25D GOTO labelA, where labelA is located at address 73. The top-of-stack is popped off the stack, XORed with decimal 25, and the result is loaded into the counter. The next state comes from address 73. POPXORC is an advanced instruction typically used to compare the inputs against a known value and then branch on the basis of the result.

Table 1 summarizes the effects of each instruction on the address multiplexer, the stack, and the counter.

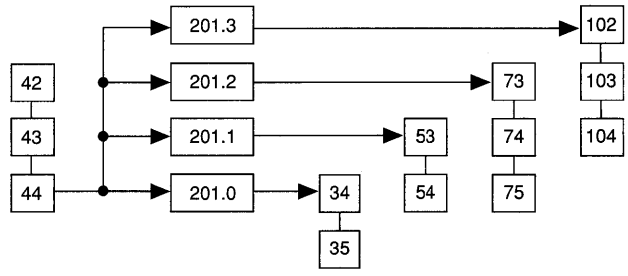
Table 1. Instruction Set Summary

Instruction	Definition	Next-State Address	Effect on Stack	Effect on Counter
CONTINUE	Continue with next instruction	labelA	None	Hold
JUMP	Jump to a label	labelA	None	Hold
CALL	Call subroutine	labelA	labelB	Hold
RETURN	Return from subroutine	labelA	Pop	Hold
LOADC	Load CREG	labelA	None	Constant
LOOPNZ	Loop/decrement CREG on non -zero value	labelA *or* labelB	None	Decrement
DECNZ	Decrement CREG on non-zero value	labelA	None	Decrement
PUSHLOADC	Push CREG to stack and load CREG	labelA	CREG	Constant
POPC	Pop stack to CREG	labelA	Pop	Stack
PUSH	Push constant to stack	labelA	Push	Hold
PUSHI	Push inputs to stack	labelA	Inputs	Hold
ANDPUSHI	Push masked inputs to stack	labelA	Inputs (ANDed) Constant	Hold
POPXORC	XOR stack with constant and send result to CREG	labelA	Pop	Stack XOR Constant

Multiway Branching

Multiway branching provides an added dimension to the capabilities of the instruction set. For example, a JUMP labelA to an address within the multiway branch block forces the branch-select logic to decide which of the four words to send to the pipeline register. This selection is based on user-defined functions of the inputs. See Figure 10.

Figure 10. Jumping to a Multiway Branch Address



Any of the 13 available commands can be enhanced with multiway branching. For example, location 44 in Figure 10 can be a CALL to a subroutine, and address 201 can contain the starting instruction for 4 unique subroutines. The routine that is actually executed depends on the user-defined condition of the inputs. The following ASM code can be used to implement this example:

```
44D:     [Output Spec] CALL ROUTINE1;
201D:
ROUTINE1:   IF            cond1    THEN    [out 1]    JUMP 102D;
                ELSEIF    cond2    THEN    [out 2]    JUMP 73D;
                ELSEIF    cond3    THEN    [out 3]    JUMP 53D;
                ELSE                       [out 4]    JUMP 34D;
```

Design Security

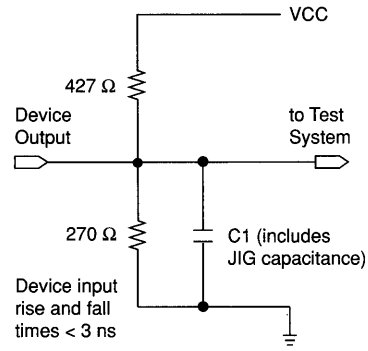
The EPS448 EPLD contains a programmable design Security Bit that controls access to the data programmed into the EPLD. If this Security Bit is used, a proprietary design implemented in the EPLD cannot be copied or retrieved. It provides a high level of design control because programmed data within EPROM cells is invisible. The Security Bit, along with all other program data, is reset by erasing the EPLD.

Functional Testing

The EPS448 EPLD is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. AC test measurements are performed under the conditions shown in Figure 11.

Figure 11. EPS448 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable input noise immunity can result.



Since the EPS448 EPLD is erasable, Altera can use and then erase test programs during early stages of production flow. This ability to use application-independent, general-purpose tests is called generic testing and is unique among user-defined LSI logic devices. EPS448 EPLDs also contain on-board test circuitry to allow verification of function and AC specifications after they are packaged in windowless packages.

Figure 12 shows the output drive characteristics of EPS448 I/O pins and typical supply current versus frequency for the EPS448 EPLD.

Figure 12. EPS448 Output Drive Characteristics and I_{CC} vs. Frequency

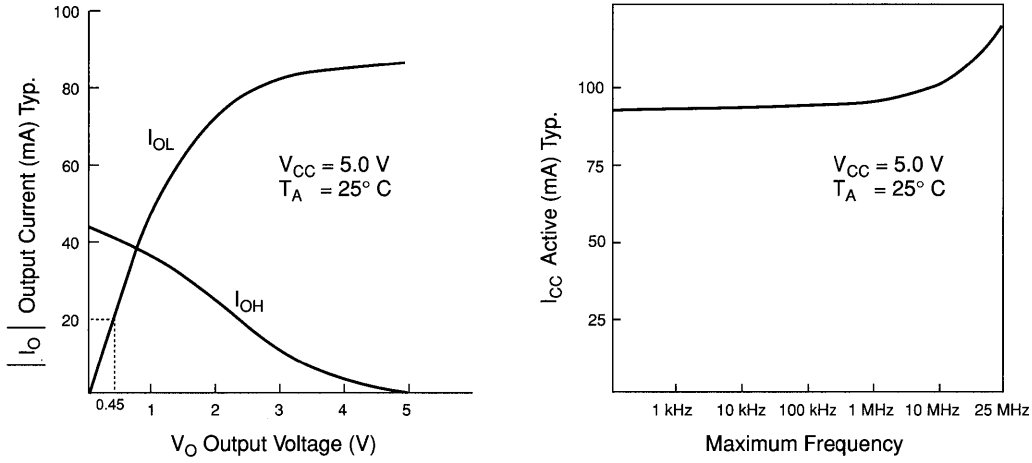
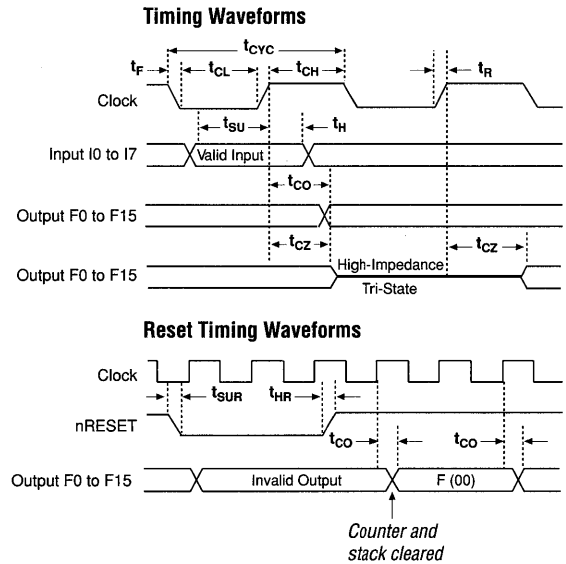


Figure 13 shows EPS448 timing and reset timing waveforms.

Figure 13. EPS448 Switching Waveforms

If nRESET is held low for more than three Clock edges, then the outputs associated with the boot address (00 Hex) will remain at the pins until the third Clock after nRESET goes high.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–10	85	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			500 (100)	ns
t_F	Input fall time			500 (100)	ns

DC Operating Conditions *Notes (2), (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –8 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –4 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 8 (4) mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND, *Note (5)*	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	No load, V_I = V_{CC} or GND, *Note (6)*		60	95 (120)	mA
I_{CC3}	V_{CC} supply current (active)	No load, 50% duty cycle, f = 1.0 MHz, V_I = V_{CC} or GND, *Note (6)*		90	140 (200)	mA

Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{RST}	nRESET pin capacitance			75	pF

AC Operating Conditions *Note (3)*

			EPS448-25A		EPS448-25		EPS448-20		EPS448-16		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
f_{CYC}	Maximum frequency	C1 = 35 pF	25		25		20		16		MHz
t_{CYC}	Minimum clock cycle			40		40		50		62.5	ns
t_{SU}	Input setup time		16.5		20		22		22		ns
t_H	Input hold time		0		0		0		0		ns
t_{CO}	Clock to output delay	C1 = 35 pF		16.5		20		22		22	ns
t_{CZ}	Clock to output disable or enable			16.5		20		22		22	ns
t_{CL}	Global clock low time		11		12		15		15		ns
t_{CH}	Global clock high time		11		12		15		15		ns
t_{SUR}	nRESET setup time		16.5		18		18		18		ns
t_{HR}	nRESET hold time		5		5		5		5		ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.

(2) Numbers in parentheses are for military and industrial temperature versions.

(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.

(4) Typical values are for T_A = 25° C, V_{CC} = 5 V.

(5) For 1.0 < V_I < 3.8, the nRESET pin can supply up to 200 µA.

(6) This condition applies when the present state is a single-way branch location.

(7) Capacitance is measured at 25° C. Sample-tested only.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPS448-16, EPS448-20, EPS448-25, EPS448-25A
Industrial Temp.	(–40° C to 85° C)	EPS448-20
Military Temp.	(–55° C to 125° C)	EPS448-20

Notes:

Micro Channel EPLD

User-Configurable Micro Channel Interface

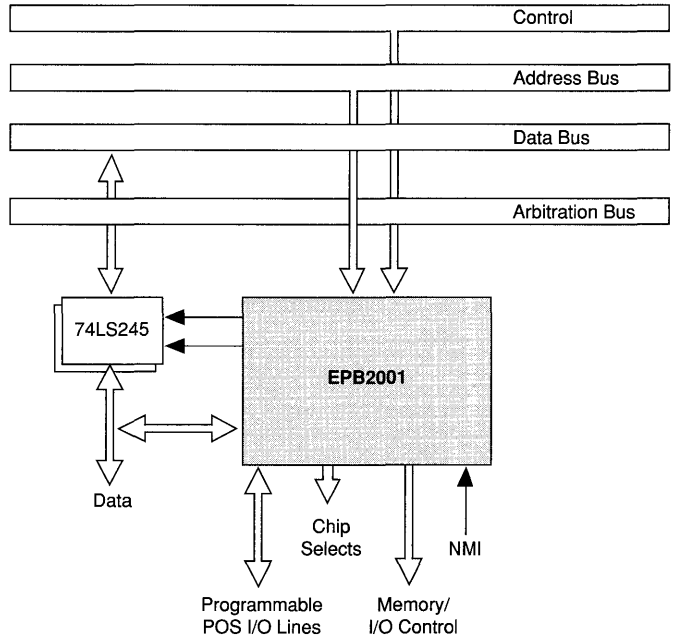
August 1993, ver. 2 | Data Sheet

Features ...

- ❑ 100% Micro Channel-compatible architecture eliminates design debug problems and allows faster board design time.
- ❑ 30-mA power-supply current conserves limited board power for memory, I/O, and other essential ICs.
- ❑ 25-ns address decoding supports high-speed, zero "wait-state" data transfers.
- ❑ Programmable POS register I/O gives the designer a choice of POS bits accessible on board.
- ❑ Multiple I/O or address decode ranges (up to 8 per chip-select output) provide multiple addressing options for the designer's board.

See Figure 1.

Figure 1. Micro Channel Bus



...and More Features

- 8 programmable chip-select outputs eliminate the need for extra address decoder PLDs and glue logic ICs.
- 24 Micro Channel address inputs support full address decoding from the Micro Channel bus.
- 24-mA current drive outputs eliminate extra buffer ICs.
- Channel-check interrupt support enables the board to use bus Non-Maskable Interrupts for fast CPU interrupt response.
- Altera's MCMap Development System simplifies Micro Channel design and eliminates design errors.

See the ***Micro Channel Adapter Handbook*** for more information.

Configuration EPROMs
for FLEX 8000 Devices

August 1993, ver. 2 Data Sheet

Features

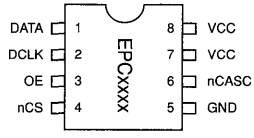
- Family of serial EPROMs designed to configure FLEX 8000 devices
- Available in compact, one-time programmable (OTP) 8-pin plastic dual in-line (PDIP) and 20-pin plastic J-lead chip carrier (PLCC) packages (see Figure 1); 32-pin thin quad flat pack (TQFP) packages under development
- Simple 4-wire interface to FLEX 8000 devices for ease of use
- Low current during configuration (15 mA) and near-zero standby current (100 µA)
- Software design support with Altera's MAX+PLUS II development system for IBM PC, Sun SPARCstation, and HP 9000 Series 700 platforms
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers, including Data I/O

Functional Description

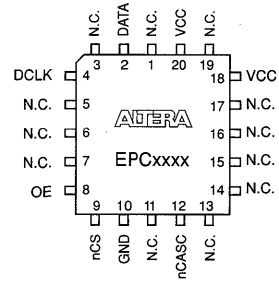
In SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is desired. Altera's serial-memory Configuration EPROMs store configuration data for the SRAM-based Altera FLEX 8000 devices.

Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



8-Pin DIP



20-Pin J-Lead

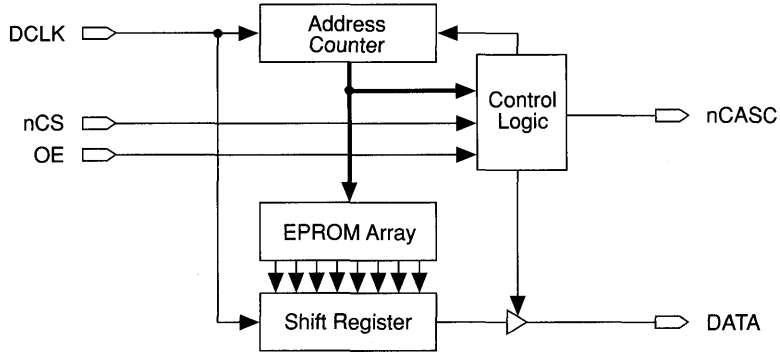
Table 1 shows the size of each Altera Configuration EPROM and indicates which FLEX 8000 device is typically configured by each.

Table 1. Typical Application for Altera Configuration EPROMs

Device	Device Size	Typical FLEX 8000 Device Configured
EPC1064	65,536 × 1 bit	EPF8282, EPF8282V, EPF8452
EPC1213	212,992 × 1 bit	EPF8820, EPF81188

Figure 2 shows a block diagram of the Configuration EPROM. Configuration data is stored in the EPROM array and clocked out serially by the DCLK input. The Output Enable (OE), Chip-Select (nCS), and Clock (DCLK) pins supply the control signals for the address counter and the output tri-state. The device presents the configuration data as a serial bit stream on the DATA pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC pin provides handshaking between multiple Configuration EPROMs, so that a set of devices can be linked together to serially configure a large FLEX 8000 device. Refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* and *Application Note 33 (Configuring FLEX 8000 Devices)* in this data book for more information on FLEX architecture and configuration.

Figure 2. Configuration EPROM Functional Block Diagram



The control signals for Configuration EPROMs (DCLK, nCS, OE) interface directly to the FLEX 8000 device control signals. A FLEX 8000 device can control the entire configuration process by retrieving the configuration data from the Configuration EPROM without an external intelligent controller. Configuration usually occurs automatically at system power-up.

The OE and nCS pins work together to control the tri-state buffer on the DATA output pin, and to enable the address counter in the Configuration EPROM. When OE is driven low, the device resets the address counter and tri-states the DATA pin. When the OE pin is driven high again, the device is

controlled by the nCS pin. If nCS is held high after the OE reset pulse, the counter is disabled, and the DATA output pin is tri-stated. When nCS is driven low, the counter is enabled and the DATA output pin is enabled. The nCS pin can then be held either high or low to control the output and counter. When OE is driven low again, regardless of the state of nCS, the address counter is reset and the DATA output pin is tri-stated. Upon power-up, the address counter is automatically reset. Table 2 describes the pin functions of Altera Configuration EPROMs.

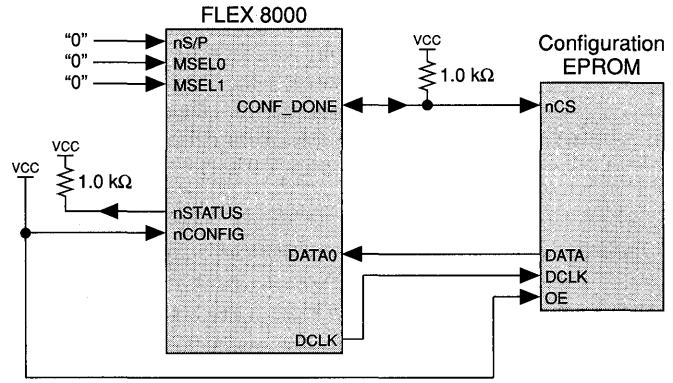
Table 2. Configuration EPROM Pin Functions

Pin Name	8-Pin PDIP Pin Number	20-Pin PLCC Pin Number	Pin Type	Description
DATA	1	2	Output	Serial data output.
DCLK	2	4	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	Input	Output Enable (active high) and Reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	Input	Chip-Select output (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	Output	Cascade-Select output (active low). This output goes low when the address counter has reached its maximum value. nCASC is usually connected to the nCS input of the next Configuration EPROM in a daisy-chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	Power	Power pin

Single-Device Configuration

The active serial (AS) configuration scheme uses a serial Configuration EPROM (e.g., EPC1213) as a data source for a FLEX 8000 device. The Configuration EPROM presents its data to the FLEX 8000 device in a serial bit-stream. Figure 3 shows a typical circuit in which the FLEX 8000 device controls the configuration process and uses a serial Configuration EPROM as the data source. For additional information, refer to *Application Note 33 (Configuring FLEX 8000 Devices).*

Figure 3. Active Serial Configuration



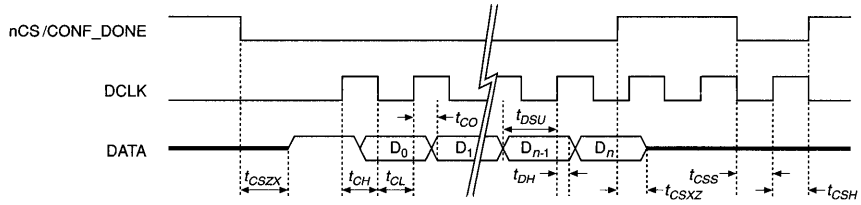
The nCONFIG pin on the FLEX 8000 device in Figure 3 is connected to V_{CC}, so the device automatically configures itself at system power-up. The system can monitor the nSTATUS pin to ensure that configuration occurs correctly. Immediately after power-up, the FLEX 8000 device pulls the nSTATUS pin low and releases it within 100 ms. Once released, the open-drain nSTATUS pin is pulled up to V_{CC} by an external 1.0-kΩ pull-up resistor. If an error occurs during configuration, the FLEX 8000 device pulls the nSTATUS pin low, indicating that configuration was unsuccessful.

The DCLK signal, which is driven by the FLEX 8000 device, clocks sequential data bits from the Configuration EPROM. While the SRAM data is being loaded, the FLEX 8000 device holds the open-drain CONF_DONE pin at GND, indicating that data is loading. A 24-bit program-length counter within the FLEX 8000 device stores the program length, i.e., the total number of configuration bits. Once the terminal count value for the configuration data (i.e., the last configuration data bit) has been reached, the FLEX 8000 device releases the CONF_DONE pin, which is subsequently pulled up to V_{CC} by an external 1.0-kΩ pull-up resistor. The resulting high input on the nCS pin causes the Configuration EPROM to tri-state its DATA output, electrically removing the Configuration EPROM from the circuit.

After it releases the CONF_DONE pin, the FLEX 8000 device uses it as an input for monitoring the configuration process. When the FLEX 8000 device senses a high logic level on CONF_DONE, it completes the initialization process and enters user mode. Figure 4 shows the timing associated with the AS configuration process and the order of transitions on the control signals.

Worst-case values for the timing parameters shown in Figure 4 are given in the "Timing Parameters" table later in this data sheet.

Figure 4. Single-Device Configuration Timing Waveforms

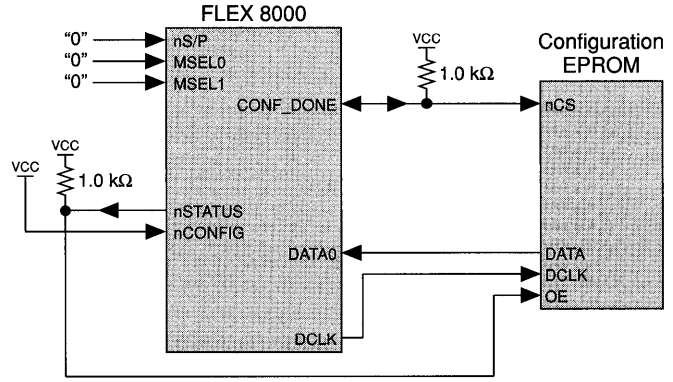


In the circuit shown in Figure 3, the nCONFIG pin on the FLEX 8000 device is tied to the Output Enable (OE) input of the Configuration EPROM; both are tied to V_{CC}. A high logic level on the nCONFIG input automatically starts the configuration. The output of the serial Configuration EPROM is enabled by a high input on its OE pin. If an error occurs during circuit configuration, the FLEX 8000 device pulls and holds the nSTATUS pin low, indicating a configuration error. External circuitry is used to monitor the nSTATUS pin and take appropriate action if configuration fails. This circuitry must assert a high-low-high pulse on the nCONFIG pin to reconfigure the device after the error. The same circuitry can also be used to begin reconfiguring the FLEX 8000 device at any time after system power-up.

The FLEX 8000 device's built-in *Auto-Restart Configuration on Frame Error* option bit allows the device to automatically reconfigure itself if it encounters an error during configuration. If this option bit is turned on, a configuration error causes the FLEX 8000 device to pull the nSTATUS pin low for 10 internal Clock cycles and then release it. This 1- to 3-µs pulse on the nSTATUS pin provides an external indication that reconfiguration is about to begin. It also can be used to reset the Altera Configuration EPROM.

Figure 5 shows a circuit that uses the *Auto-Restart Configuration on Frame Error* option. The nSTATUS pin is connected to the OE input on the Altera Configuration EPROM so that the error-reset pulse on nSTATUS resets the internal address counter on the Configuration EPROM and prepares it to reconfigure the FLEX 8000 device. The nCONFIG input is also available to initiate a reconfiguration cycle externally. Since the nSTATUS pin is pulled low and then released whenever configuration begins, it resets the Configuration EPROM before reconfiguration. During device operation, if V_{CC} drops below the power-on reset (POR) threshold for the FLEX 8000 device, nSTATUS is pulsed and the Configuration EPROM is reset in the same way to provide automatic reconfiguration. Timing for the circuit in Figure 5 is identical to the timing shown in Figure 4 for the AS configuration scheme (the error-reset pulse on nSTATUS is not shown).

Figure 5. Active Serial Device Configuration with Automatic Reconfiguration on Error



MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. MAX+PLUS II software automatically generates a Programmer Object File (**.pof**) for every FLEX 8000 device in a project. By default, each FLEX 8000 device in a multi-device project has a dedicated serial Configuration EPROM. MAX+PLUS II selects the appropriate Configuration EPROM to most efficiently store the data for each FLEX 8000 device.

The POF includes a preamble, cyclic redundancy check (CRC), and synchronization data that allow it to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with MAX+PLUS II and a Configuration EPROM programming adapter. A number of other programming hardware manufacturers, including Data I/O, support programming of Configuration EPROMs. See the *Altera Programming Hardware* and *Programming Hardware Manufacturers* data sheets in this data book.

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	4.75	5.25	V
V_I	Input voltage	*Note (1)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10	10	µA

Supply Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 8 MHz		10		mA

Capacitance *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Timing Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled			50	ns
t_{CSZX}	nCS low to DATA output enabled			50	ns
t_{CSXZ}	nCS high to DATA output disabled			50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		100		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		ns
t_{DSU}	Data setup time before rising edge on DCLK		50		ns
t_{DH}	Data hold time after rising edge on DCLK		0		ns
t_{CO}	DCLK to DATA out delay, *Note (5)*			75	ns
t_{CK}	Clock period		160		ns
f_{CK}	Clock frequency			6	MHz
t_{CL}	DCLK low time		80		ns
t_{CH}	DCLK high time		80		ns
t_{XZ}	OE low or nCS high to DATA output disabled			50	ns
t_{OEW}	OE pulse width to guarantee counter reset		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			60	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			50	ns
t_{CEOUT}	nCS high to nCASC high delay			100	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Capacitance is sample-tested only.
(5) Eight Clock cycles are required after the t_{CSS} setup time has been met to clock out the first eight bits. These bits are all high and are used to synchronize the configuration process. The ninth Clock cycle presents the first configuration data bit.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPC1213, EPC1064
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

Package Outlines

See the *Package Outlines Data Sheet* in this data book for dimensions of the Configuration EPROM 8-pin PDIP and 20-pin PLCC packages. For package outlines of the 32-pin TQFP Configuration EPROM, contact Altera Applications at (800) 800-EPLD.

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8 Military


ALTERA
EPF81188GM883B
ALTERA
EPM7192GM883B
ALTERA
EP1810GM883B
ALTERA
EPM5130WM883B

Military Products

August 1993, ver. 3 | Data Sheet

Introduction

Altera's military devices are manufactured in proven EPROM, EEPROM, and SRAM technologies, providing an optimum combination of reliability, speed, density, and low power consumption. Altera offers military devices that meet military-temperature-range, MIL-STD-883B, and DESC requirements. This data sheet discusses the following topics:

- Product availability
- MIL-STD-883B qualification flow
- Source control drawings

Product Availability

Tables 1 and 2 provide information on military-temperature-range, MIL-STD-883B-qualified, and DESC devices. For more information on Altera's military products, contact Altera Marketing at (408) 894-7000. For detailed device information, refer to the appropriate data sheets in this data book.

Table 1. Altera Military-Temperature-Range Devices

Device	Package *(1)*	Symbol	Max	Unit
EP610	D, J	t_{PD1}	35	ns
EP910	D, J	t_{PD1}	40	ns
EP1810	G, J	t_{PD1}	45	ns
EPM5032	D, J	t_{PD1}	25	ns
EPM5064	J	t_{PD1}	30, 35	ns
EPM5128	G, J	t_{PD1}	30, 35	ns
EPM5130	G, J, W	t_{PD1}	30, 35	ns
EPM5192	G, J	t_{PD1}	35	ns
EPM7192	G	t_{PD1}	15, 20	ns
EPF8452	G	t_1	22	ns
EPF81188	G	t_1	22	ns
EPS448	D, J	f_{MAX}	20	MHz

Note:

(1) Package configurations:
- D: Ceramic dual in-line package (CerDIP)
- J: Ceramic J-lead chip carrier (JLCC)
- G: Ceramic pin-grid array (PGA)
- W: Ceramic quad flat pack (CQFP) in QFP carrier

Table 2. Altera MIL-STD-883B-Qualified & DESC Devices

Device	Package *Note (1)*	Symbol	Max	Unit	Altera Military Drawing	DESC Order Number
EP610	D	t_{PD1}	35	ns	02D-00522	5962-8947601LA
EP1810	G	t_{PD1}	45	ns	02D-00782	5962-8946901YC
EPM5032	D	t_{PD1}	25	ns	02D-00828	5962-9061102XA
EPM5128	G	t_{PD1}	30	ns	02D-01015	*Note (2)*
EPM5128	G	t_{PD1}	35	ns	02D-01015	5962-8946801XC
EPM5130	G	t_{PD1}	30	ns	02D-01413	5962-9314402MZC
EPM5130	G	t_{PD1}	35	ns	02D-01413	5962-9314401MZC
EPM5130	W	t_{PD1}	30	ns	02D-01413	5962-9314402MYA
EPM5130	W	t_{PD1}	35	ns	02D-01413	5962-9314401MYA
EPM5192	G	t_{PD1}	30	ns	02D-01359	5962-9206202MZC
EPM5192	G	t_{PD1}	40	ns	02D-01359	5962-9206201MZC
EPM7192	G	t_{PD1}	15, 20	ns	C.F.	–
EPF8452	G	t_1	22	ns	C.F.	–
EPF81188	G	t_1	22	ns	C.F.	–

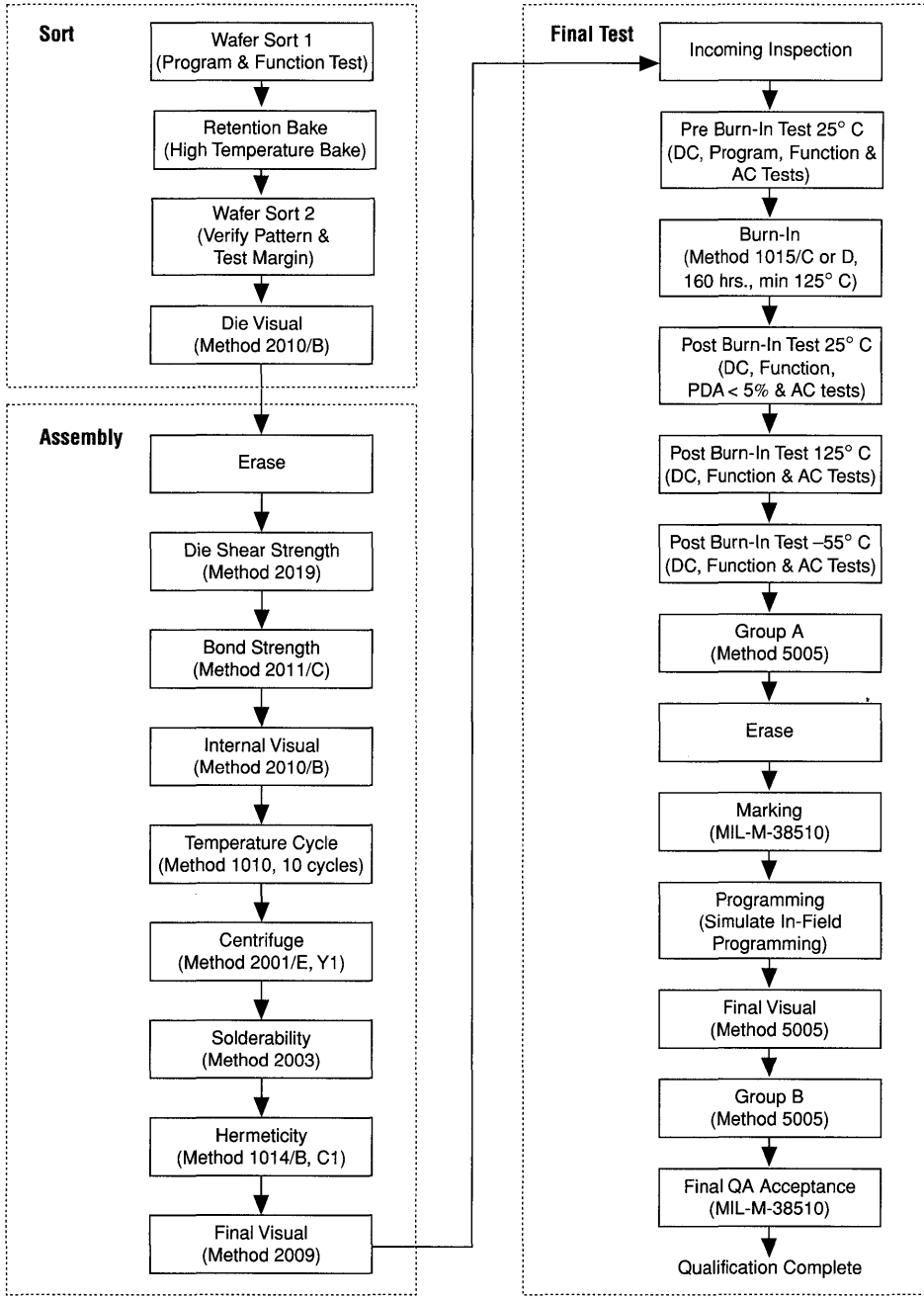
Notes:
(1) Package configurations:
D: Ceramic dual in-line package (CerDIP)
G: Ceramic pin-grid array (PGA)
W: Ceramic quad flat pack (CQFP) in QFP carrier
(2) DESC number pending

MIL-STD-883B Qualification Flow

Figure 1 shows the process flow for qualifying Altera devices to MIL-STD-883B specifications.

MIL-STD-883B-compliant device specifications are provided in Military Product Drawings (MPDs) that are available on request from Altera Marketing. An MPD is prepared in accordance with the appropriate military specification format and is used for preparing Source Control Drawings (SCDs).

Figure 1. MIL-STD-883B Qualification Flow

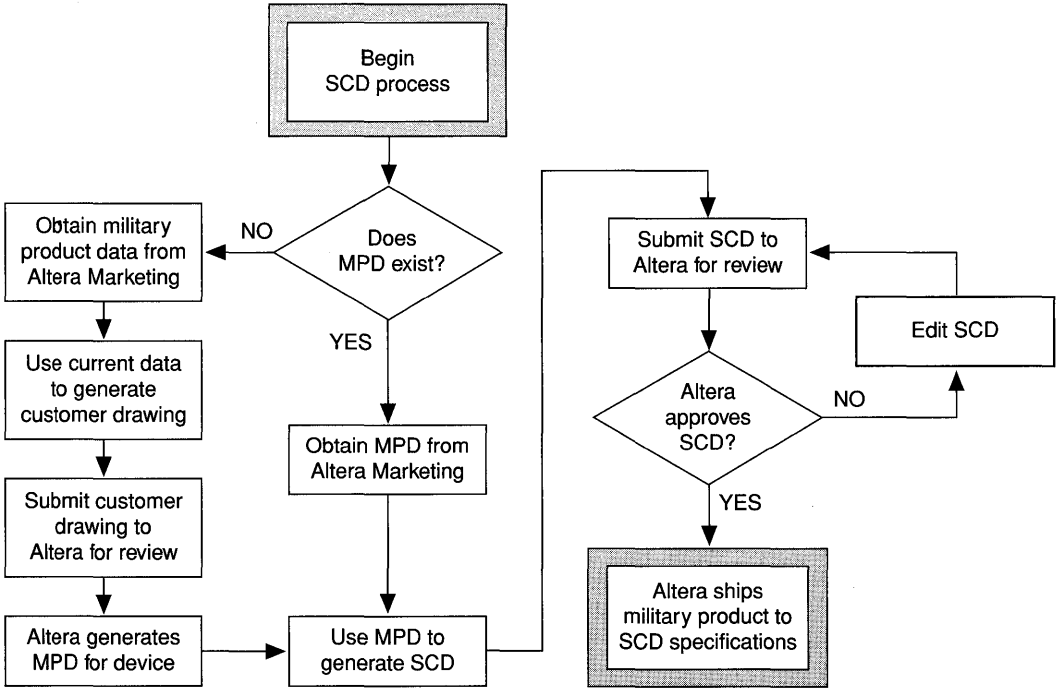


Source Control Drawings

Source Control Drawings (SCDs) are generated for Altera's commercial devices that are or will be qualified for MIL-STD-883B. SCDs are also used for document control. An SCD should be based on a Military Product Drawing (MPD) provided by Altera. When an MPD is not available, the user should contact Altera's Marketing Department for current data. Altera MPDs contain information on the scope, reference documents, MIL-STD-883B requirements, quality assurance provisions, and preparation of delivery for devices. Characteristics of device screening—such as burn-in testing, AC/DC electrical properties, timing waveforms, and package dimensions—are also detailed in MPDs. These specifications may differ from those for Altera's commercially rated devices. Altera will not approve an SCD until the described MPD requirements are met.

Figure 2 shows the process flow for generating an SCD for Altera's military products.

Figure 2. Source Control Drawing (SCD) Generation Flow



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ALTERA
FLEX™
MPF81188QC240
ALTERA
MPM7192GC160
ALTERA
MPN21QC240
ALTERA
MPM7256QC208
ALTERA
MPN21QC208

MPLDs
Mask-Programmed Logic Devices

August 1993, ver. 2 | Data Sheet

Features

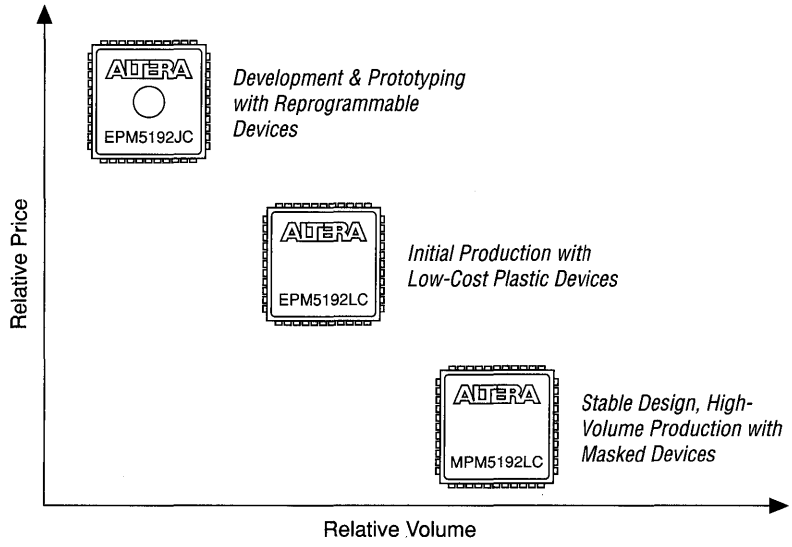
- Masked versions of Altera programmable logic devices
- Reduced cost for high-volume production
- Available for high-density MAX 5000 devices, MAX 7000 devices, and FLEX 8000 devices
- Pin-, function-, and timing-compatible with original device
- Conversion process handled by Altera
- Fast turn-around to reduce time-to-market
- Test vectors generated by Altera
- Low power consumption
- *N*-to-1 option combines multiple Altera programmable devices into a single MPLD

General Description

Altera Mask-Programmed Logic Devices (MPLDs) provide a masked alternative to programmable logic devices. By using a generic CMOS process and removing all programmable cells, Altera passes considerable savings on to customers who anticipate high-volume production. The combination of Altera programmable logic devices and MPLDs provides the best of both worlds: the fast time-to-market offered by programmable devices, and the low cost and low risk offered by MPLDs. See Figure 1.

Figure 1. MPLD Economics

As volumes increase during production, a design can move from erasable/reconfigurable devices to MPLDs.



9 MPLD

Altera handles the programmable logic device-to-MPLD conversion so that no redesign effort is required. Altera guarantees that the MPLD meets the worst-case AC and DC parameters of the original Altera programmable logic device. In addition, Altera automatically generates test vectors with 98% fault coverage.

MPLD Compatibility

An Altera MPLD is guaranteed to be pin-, function-, and timing-compatible with the original programmable logic device. This guarantee ensures that the MPLD can replace the original Altera device, while providing lower cost and maintaining the production flow.

Pin compatibility guarantees that both the pin-out and DC specifications of the MPLD match those of the original device. In addition, the MPLD typically consumes less power than the equivalent programmable device, depending on the design and operating conditions.

Functional compatibility is ensured because the logic within the programmable logic device (e.g., product terms, programmable flipflops, etc.) is mapped directly to specially designed elements within the MPLD. Altera employs a proprietary logic synthesis program that uses the Simulator Netlist File (**.snf**) generated by Altera's MAX+PLUS II software. The SNF describes the final synthesis, placement, and routing of the original design. The conversion process pays special attention to the wide fan-in of product terms and the wide fan-out of registers commonly found in programmable logic applications.

An MPLD is guaranteed to meet the worst-case timing parameters of the corresponding programmable logic device, as specified in the device data sheet. If a worst-case analysis of the design implementation in the programmable has been performed, the same analysis will hold for the MPLD. Therefore, the timing of the original design and the overall system are maintained when the programmable device is replaced with an MPLD.

Design for Testability

Unlike ASIC designs, which require time-consuming test vector generation, Altera programmable logic devices do not require test vectors: the devices are fully tested before they are shipped and are verified at programming time.

MPLD designs include a scan-based testing method that parallels the testability of Altera programmable logic devices. This patented test methodology allows Altera to create test vectors with 98% fault coverage for all "stuck-at" and open faults. This high fault coverage is maintained regardless of whether synchronous or asynchronous design techniques are used.

The built-in design-for-testability in MPLDs frees the design engineer from the burden of creating a testable design and test vectors. In fact, customer-provided simulation vectors are optional for MPLD conversions.

N-to-1 MPLD Conversion Option

Many applications use multiple Altera programmable logic devices on a single board for both prototyping and production. In some applications, it may be desirable to perform prototyping with multiple programmable devices, then shift to a single-device implementation for high-volume production. Altera's MPLD conversion program provides this capability with the "*N*-to-1" conversion option, which combines a multi-device design into a single MPLD. The *N*-to-1 conversion offers the benefits of developing with multiple programmable logic devices, even when production constraints require a high-density, single-device solution.

The *N*-to-1 MPLD conversion works in conjunction with the design partitioning feature in MAX+PLUS II software. Partitioning allows a design engineer to create a large design without concern for design size or fitting constraints. MAX+PLUS II automatically partitions the design and fits each portion into a separate programmable device. Multiple programmable devices can be used for design prototyping while simulation and timing analysis can be completed on the top-level design.

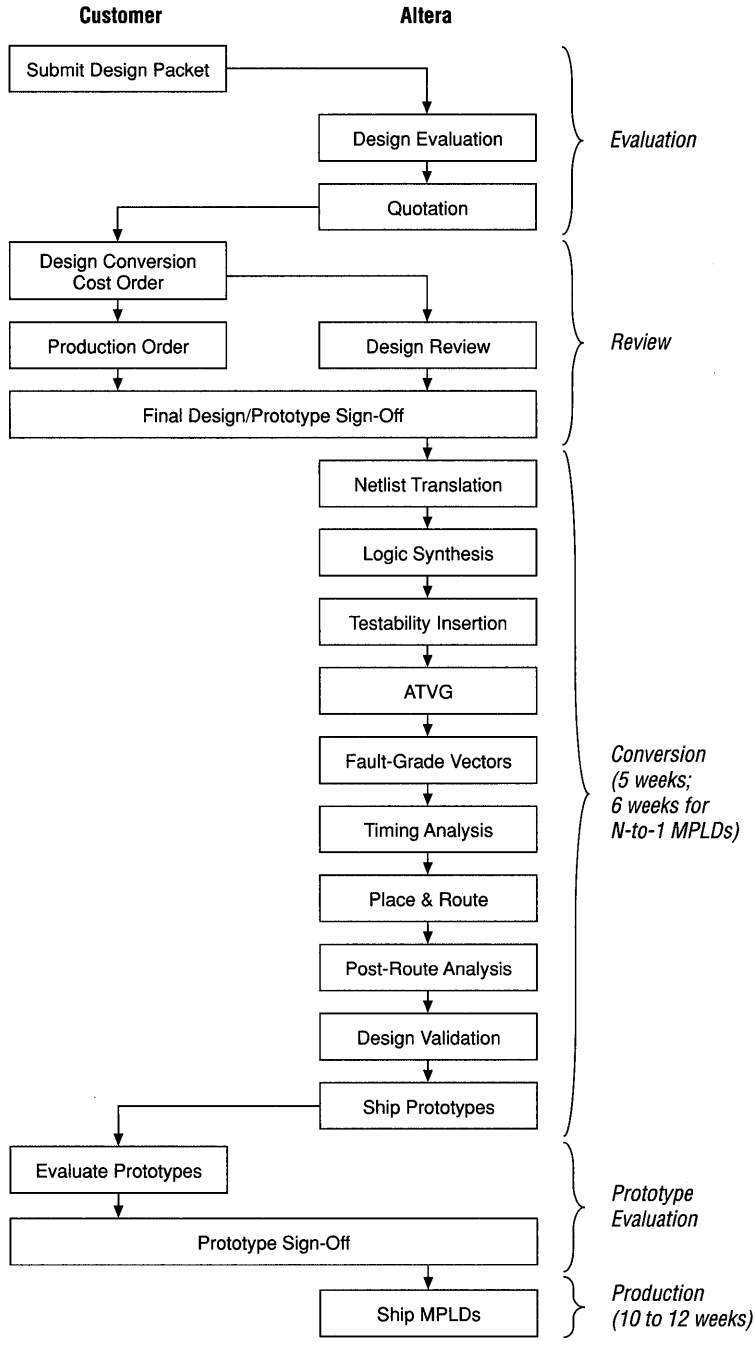
The *N*-to-1 MPLD option provides a single MPLD that is function- and timing-compatible with the original multi-device solution. The package type and pin-out are determined by the application's requirements. A wide range of packages is available.

Quick, Seamless Conversion

One of the principal objectives of Altera's MPLD conversion program is to minimize the design engineer's time and resource investment in the conversion. The engineer simply submits design files created with MAX+PLUS II software and Altera delivers MPLDs within weeks of the design sign-off.

The MPLD conversion flow chart (see Figure 2) shows how easily a programmable Altera device can be converted into an MPLD. The ***MPLD Conversion Information & Order Forms*** workbook, which can be obtained from an Altera representative, provides the instructions and forms needed to submit a design for quotation. The design engineer submits the design files and the workbook's *Checklist*, *Information Form*, and *Questionnaire* to Altera. Altera then performs a design evaluation and returns a price quote for the conversion.

Figure 2. MPLD Conversion Flow



After the customer submits an order for the Design Conversion Cost (DCC), an Altera engineer reviews the design and submits a *Final Design Sign-Off Form* for customer approval. This form describes the specifications of the MPLD in detail. After the final design has been signed off, Altera begins the design conversion.

The design conversion includes netlist translation, logic synthesis, testability insertion, Automatic Test Vector Generation (ATVG), fault grading, timing analysis, place-and-route, post-route timing analysis, design validation, and the prototype manufacturing. The entire conversion process, from final design sign-off to prototype delivery, takes less than 5 weeks (6 weeks for *N*-to-1 conversion). Production quantities are delivered 10 to 12 weeks after the customer returns the *Prototype Sign-Off Form.*

Conclusion

The two most important design goals faced by engineers today are reducing time-to-market and minimizing system cost. The combination of Altera programmable logic devices and MPLDs provides a solution that fills these needs, allowing a company to take a product to market quickly, lower the end-product cost, and reduce the risks associated with ASIC design.

Notes:

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Section 10 Device Operation

Operating Requirements for Altera Devices

August 1993, ver. 5 Data Sheet

Introduction

Altera devices combine unique programmable logic architectures with advanced CMOS processes to provide exceptional performance and reliability. To maintain the highest possible performance and reliability of Altera devices, system designers must consider the following operating requirements:

- Operating conditions
- Pin voltage levels
- Output loading
- Power-supply management
- Thermal analysis
- Reduction of heat build-up
- Device erasure

Operating Conditions

Altera devices are rated according to a set of defined parameters, which must be considered when a device is implemented in a system. These parameters are provided in each device data sheet and include absolute maximum ratings, recommended operating conditions, and DC and AC operating conditions.

Absolute Maximum Ratings

Absolute maximum ratings define the limits of the conditions that a particular Altera device can withstand. These values are based on experimental evidence of device behavior, as well as theoretical modeling of breakdown and damage mechanisms. These ratings are stress ratings only. Functional operation of the device at these conditions or at conditions above those indicated in the "Recommended Operating Conditions" table in a device data sheet is not implied. For example, I_{OUT} is the absolute current capacity and not the drive capability of an output pin. The output source and sink currents are given as I_{OH} and I_{OL} in the "DC Operating Conditions" section of each data sheet.

Operating an Altera device at conditions listed in the "Absolute Maximum Ratings" table in a device data sheet for extended periods of time may impair device reliability. Operating the device at conditions that exceed these ratings may cause permanent damage to the device.

Recommended Operating Conditions

The functional operation limits for an Altera device, given in the "Recommended Operating Conditions" table in a device data sheet, specify limits under which all AC and DC parameters are guaranteed. These parameters may also be expressed differently in other rating sections. For example, the V_{CC} range specified in this table is the range over which the AC and DC operating conditions are guaranteed. The V_{CC} range specified in the "Absolute Maximum Ratings" table is the power-supply level beyond which the device will be damaged.

DC Operating Conditions

The steady-state voltage and current values expected from an Altera device are provided in the "DC Operating Conditions" table in a device data sheet. This information includes input voltage sensitivities (V_{IH}, V_{IL}), output voltage (V_{OH}, V_{OL}), current capability (I_{OH}, I_{OL}), and input and output leakage currents (I_I, I_{OZ}). The values are guaranteed for DC operation under the conditions specified in each device data sheet.

AC Operating Conditions

The external and internal timing parameters for an Altera device are given in the "AC Operating Conditions" table(s) in a device data sheet. These parameters are determined under the conditions specified in the "Recommended Operating Conditions" table. The external timing parameters are guaranteed pin-to-pin delays when the device is operating under these conditions.

Timing parameters are specified as either maximum or minimum values. A maximum value indicates that the delay will not exceed the specified time. Setup, hold, and pulse width times are expressed as minimum values that the system must provide to ensure reliable device operation.

Pin Voltage Levels

Device pins can be exposed to dangerous voltages during handling or device operation. During handling, pins can be exposed to high-voltage static discharges that cause electrostatic discharge (ESD) damage. During operation, power-supply spikes on the VCC and GND pins or errant logic levels elsewhere in the system can produce logic level stress with voltages on the order of magnitude of V_{CC} (0 V to 15 V). To minimize these hazards, the user must observe the precautions specified for the following conditions:

- Pin connections
- Latch-up
- Hot-socketing
- Electrostatic discharge

Pin Connections

During project compilation, MAX+PLUS II software generates a device utilization report, called a Report File (**.rpt**), that provides information on the pin-outs and connectivity of the device(s) used in the project. The Report File includes a pin-out diagram that shows the user signal pins, VCC and GND pins, and reserved pins.

The VCC and GND pins should be tied to the V_{CC} or GND planes on the printed circuit board (PCB) respectively. Dedicated input pins used in a design and I/O pins configured as inputs should always be driven by an active source. I/O pins configured as bidirectional pins should always be driven whenever the I/O pin is used as an input.

Unused dedicated input and I/O pins are marked in the Report File as GND and RESERVED, respectively. Unused dedicated inputs should be tied to the GND plane. Otherwise, these pins may "float" in an indeterminate state, possibly increasing DC current in the device and introducing noise into the system. Since reserved I/O pins are driven by active signals representing the buried logic present in the logic cell associated with that particular pin, reserved I/O pins should remain unconnected. Tying a reserved I/O pin to either V_{CC} or GND creates contention that may damage the output driver on the device.

For proper operation, signals on the input and output pins must be in the following range:

$$GND \leq (V_{IN} \textit{ or } V_{OUT}) \leq V_{CC}$$

Latch-Up

Parasitic bipolar transistors, which are present in the fundamental structure of CMOS devices, may be paths for dangerous currents in the device. Typically, the base-emitter and base-collector junctions of these transistors are not forward-biased, so the transistors are not turned on. Figure 1 shows a cross-section of a CMOS wafer and primary parasitic transistors. To ensure that all junctions remain reverse-biased, the P-type substrate is connected to the most negative voltage available on-chip (GND), and the N-type well structure is connected to the most positive voltage on-chip (V_{CC}).

Figure 1. Parasitic Bipolar Transistors in CMOS

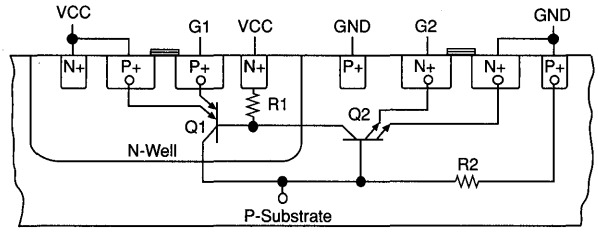


Figure 1 also shows the parasitic resistors that occur in the CMOS structure. Generally, these resistors are of no concern as long as currents do not flow through the structure laterally. However, I-R drops may occur in the structure if any of the associated diodes turn on. These diodes may be initially turned on by power-supply or I/O pin transients that exceed the limits of GND and V_{CC}. These transients can be induced by signal ringing and other inductive effects in the system.

Catastrophic failure can occur if these parasitic structures begin to conduct, since the effect is regenerative and reinforces itself until potentially destructive currents flow. This silicon-controlled rectifier (SCR) effect is called "latch-up." As the current flows through the parasitic transistor, the I-R drop through the resistor increases, further forward-biasing the base-emitter junction. The cycle continues until the current is limited by drops in the primary current path. At this point, this current may have reached a level that permanently damages internal circuitry.

Altera devices have been designed to minimize the effects of latch-up, caused by power-supply and I/O pin transients. Under recommended operating conditions, all devices are guaranteed to withstand input voltage extremes of between GND – 1 V and V_{CC} + 1 V, as well as input currents of 100 mA or less that are forced through the device pins.

To minimize the chances of inducing latch-up during power-up, GND should be applied to the device first, then V_{CC}, and finally the inputs. The power should be removed from the device in the reverse order: first, the inputs are removed, then V_{CC}, and finally GND.

Simultaneous application of inputs and V_{CC} to the device, which may occur as a power supply rises during power up, should be safe as long as V_{CC} meets the maximum rise time. The designer should ensure that the inputs cannot rise faster than the supply at the V_{CC} pin(s).

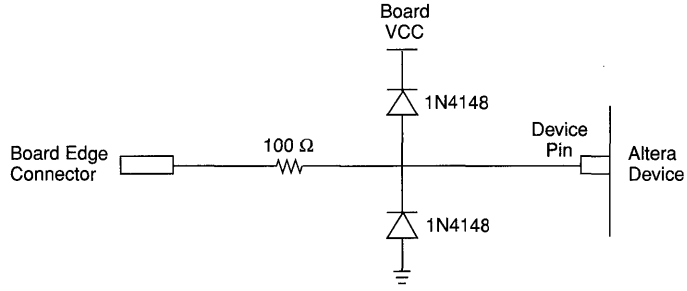
Hot-Socketing

Latch-up frequently occurs when electrical subsystems are plugged into active hardware, i.e., "hot-socketed." When a subsystem is plugged into active hardware, the logic levels often appear at the subsystem's logic devices before the power supply can provide current to the V_{CC} and GND grid of the subsystem board. This condition may lead to latch-up.

Increasing the length of the V_{CC} and GND connections can reduce the chances of latch-up during hot-socketing. If metal "fingers" are used for the board connection, the V_{CC} and GND fingers at the card edge should be longer than the logic connections. This difference in length causes the power supply to appear at the device before the logic levels, and is usually sufficient to prevent latch-up. Off-the-shelf connectors with longer V_{CC} and GND connections can provide similar results.

Implementing the circuitry shown in Figure 2 also provides protection against latch-up during hot-socketing. The diode structure provides a "clamp" level on the input voltage, preventing it from swinging more than one diode-drop away from a power-rail (–0.6 V to V_{CC} + 0.6 V). The series resistor also reduces the possibility of latch-up by restricting the current to the device input and clamp diodes. This circuitry provides the maximum protection against latch-up, but is usually required only if the input on the device is tied directly to the edge connector. Device inputs that are driven by other circuit elements in the subsystem are generally safe from latch-up, since these elements provide a natural delay before the logic levels are established.

Figure 2. Hot-Socket Protection



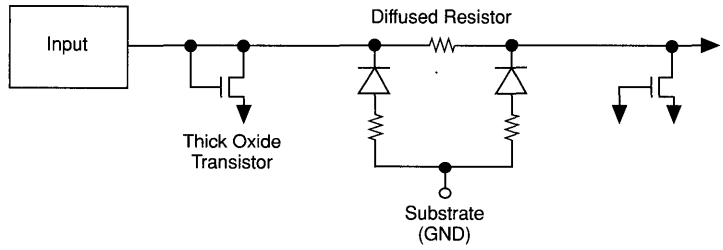
Electrostatic Discharge

Electrostatic discharge (ESD) resulting from improper device handling can cause device failure that may not manifest itself for a long period of time. Although ESD damage may result in immediate device failure, it more frequently affects the long-term reliability of the device.

Device handling during the programming cycle increases exposure to potential static-induced failure. During normal activity, the human body can generate voltages of up to tens of kilovolts (kV). Wearing ground straps during device handling and grounding all surfaces that come in contact with components reduces the likelihood of damage. Synthetic materials used in clothing can store large amounts of static electricity and may also cause ESD.

Altera devices include special structures that reduce the effects of ESD at the pins. Figure 3 shows a typical input structure for an Altera device. Diode structures and specialized field-effect transistors shunt harmful voltages to ground before destructive currents can flow. Most Altera devices can withstand ESD voltages greater than 2 kV, but all devices are guaranteed to withstand ESD voltages greater than 1 kV.

Figure 3. Altera Device Input Protection Structure



Output Loading

Output loading is typically resistive and/or capacitive. During development, the designer should ensure that the target device can supply both the current and speed necessary for the loads.

Resistive Loading

Resistive loading exists whenever a device output sinks or sources a current in a steady state. Examples of resistive loading include devices with TTL inputs, terminated buses, and discrete bipolar transistors.

Output current capabilities (I_{OH} and I_{OL}), which are functions of output voltages (V_{OH} and V_{OL}), are given in the data sheet for each device. In a DC condition, output current capabilities determine the maximum resistivity

of a load while still maintaining the necessary output voltage. If the system requires higher currents, such as those necessary to drive an LED or a relay, a high-current buffer or a discrete current switch must be used.

Short-circuit conditions—where I_{OH} and I_{OL} exceed the absolute maximum rating (I_{OUT})—can permanently damage the device.

Capacitive Loading

The "AC Operating Conditions" table in a device data sheet specifies an output capacitance condition (C1) for parameters relating to external performance. For most Altera devices, C1 is 35 pF for active signals and 5 pF for high-impedance parameters.

Device packages and board-level trace capacitance contribute the majority of loading capacitance. (An insignificant amount of the total capacitance on output buffers is attributable to the gate capacitance of CMOS device inputs.) The specified 35-pF load condition is a representative value for most CMOS circuits. For applications in which a device drives a higher capacitance, performance decreases as the capacitive load increases.

Device sockets are a source of both capacitive and inductive loading. Once a system is finalized for production, sockets should be removed if possible, and the devices should be mounted directly onto the PCB. Direct board mounting reduces both the capacitive load and noise from socket contacts.

To ensure the highest circuit performance, the capacitance on device outputs should be minimized. Since wiring traces on the PCB, device input pins, and device packaging all contribute to the total capacitance, the following guidelines should be observed:

- Board layout should ensure that signals run perpendicular to each other to provide a minimum capacitive coupling effect. Also, signal traces should be kept as short as possible.
- A high-current buffer should be used to speed the signal to all destinations for networks in which a single source drives many loads.

The lack of V_{CC} and GND planes or excessive trace lengths may cause problems with radiated coupling of noise into logic signals and transmission-line effects on signal quality. These ringing and noise elements on logic levels can lead to circuit reliability problems. When recommended layout practices cannot be implemented to prevent transmission-line problems, a small series resistance (10 Ω to 30 Ω) can be used to reduce the magnitude of undershoot and overshoot on signal edges. This resistance dampens the ringing that can occur on long board traces and prevents false triggering.

Power-Supply Management

Although Altera devices are designed to minimize noise generation and susceptibility, they—like all CMOS devices—can be sensitive to fluctuations in power supply and input lines. To minimize the effect of these fluctuations, the system designer must pay special attention to:

- V_{CC} and GND planes
- Decoupling capacitors
- V_{CC} rise time
- Current dissipation

V_{CC} & GND Planes

The system designer can minimize power-supply noise or "ground bounce" by providing separate V_{CC} and GND planes for every PCB, thus ensuring a near-infinite current-sink capability, noise protection, and shielding for logic signals on the board. If an entire plane cannot be provided, the widest possible GND and V_{CC} traces should be created throughout the entire board. Logic-width traces should not be used to carry the power supply. Although V_{CC} and GND planes tend to increase the capacitive load of the traces, they significantly reduce system noise, and dramatically increase system reliability.

Decoupling Capacitors

Each VCC and GND pin should be connected directly to the V_{CC} and GND planes in the PCB. Each pair of VCC and GND pins should be decoupled with a 0.2-µF power-supply decoupling capacitor, located as close as possible to the Altera device. For devices with a very large number of VCC and GND pins—i.e., more than 8 pairs of each—it may not be necessary to provide a decoupling capacitor for every pair. Decoupling requirements are based on the amount of logic used in the device, the frequency of operation, and the output switching requirements. As the number of I/Os and the switching frequency increase, more decoupling capacitance is required. The ideal solution is to provide a capacitor for every VCC/GND pair, which will decouple the device for any logic utilization or operating frequency. For less dense or slower designs, a reduction in the number of capacitors may be acceptable. For example, the EPM7192 has 14 VCC/GND pairs. In general, 8 decoupling capacitors are sufficient for most designs. Decoupling capacitors should have a good frequency response, like that in monolithic-ceramic capacitors.

Every PCB should also have a large-capacity, general-purpose, electrolytic capacitor network to stabilize the power supply. A 100-µF capacitor should be placed immediately adjacent to the location where the power-supply lines come into the PCB. If a transformer or regulator is used to change the voltage level, the capacitor should be placed immediately after the final stage that develops the device's V_{CC} supply. This capacitor provides a

beneficial leveling effect that supplies extra current when a large number of nodes switch simultaneously in a circuit. However, the larger the power supply capacitor, the longer the time required to bring the maximum V_{CC} to the operating level. The size of the capacitor must not force the V_{CC} rise time to violate the maximum rise time discussed next in "V_{CC} Rise Time."

V_{CC} Rise Time

When power is applied to an Altera device (with the exception of the EPS448 device), the device initiates a Power-On Reset (POR), typically as V_{CC} approaches 1.5 V to 2.0 V. The POR event occurs only if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). Slower rise times can cause incorrect device initialization and functional failure. The maximum V_{CC} rise times for Altera devices are provided in Table 1.

Table 1. Maximum V_{CC} Rise Time for Altera Devices

Device Family	Time
Classic	50 ms
MAX 5000/EPS464	10 ms
MAX 7000	10 ms
FLEX 8000	10 ms
EPS448	50 ms

The POR time is the time required after V_{CC} reaches the recommended operating range to clear device registers, configure I/O pins, and release tri-states. Once this initialization is complete, the device is ready to begin logic operation. The POR time is typically no more than 50 ms.

Current Dissipation

Every Altera device is designed to consume the least possible amount of power while providing high performance. Since these two design goals can conflict with each other, Altera devices and software tools allow designers to monitor and control the current with built-in device features.

MAX 7000 macrocells can be individually configured for high performance or low power during design entry. Turning the macrocell's Turbo Bit on allows the macrocell to function in a high-performance mode at the specified device ratings. If the Turbo Bit is turned off, the macrocell's built-in power-saving mode trades higher performance for lower current consumption.

MAX 7000 devices operating in low-power mode consume less current. The supply current (I_{CC}) can be reduced by as much as 50%, depending on

the design and operating frequency. Most MAX 7000 device data sheets provide a graph that shows the relationship between I_{CC} and frequency. For a device with the Turbo Bit option, the graph provides two curves; one showing I_{CC} versus frequency when all macrocells have their Turbo Bits turned on, the other when all macrocells have the Turbo Bits off. Since most designs use a combination of Turbo and non-Turbo macrocells, a formula that accounts for this ratio and the frequency of operation is also provided with the graph. The values shown in the graph and formula are measured with no output loads and represent only the current necessary for device operation.

Many Classic devices also have a Turbo Bit option. A Classic device operating in low-power mode enters a standby mode after 100 ns of inactivity (i.e., when no inputs or outputs have changed). An input signal transition "wakes" the device, which then performs normally until the next standby mode period. However, the signal incurs an additional delay—specified as the non-Turbo delay adder in device data sheets—as it wakes and propagates through the device.

Thermal Analysis

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

Thermal analysis should be completed early in the design process to help identify potential heat-related problems in the system and prevent the system from exceeding the device's maximum allowed junction temperature. To perform a thermal analysis, the designer must:

1. Estimate power consumption of the application.
2. Calculate the maximum allowed power for the device and package.
3. Compare the estimated and maximum allowed power values.

In most applications, the power dissipated is significantly lower than the maximum allowed. However, this type of analysis should be performed for all projects. Several steps that can correct temperature-related problems are described later in this data sheet.

Estimating Power Consumption

The following formula should be used to estimate the maximum supply current (I_{CC}):

Estimated maximum I_{CC} = no-load $I_{CC} + DC_{OUT} + AC_{OUT}$

The no-load I_{CC} can be obtained from the I_{CC}-versus-frequency graph provided in the device data sheet. Since this value is "unloaded," it is necessary to add the DC_{OUT} from steady-state outputs and the AC_{OUT} current from frequently switching outputs. DC_{OUT} depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output, as shown in the following formula:

$$DC_{OUT} = \sum_{n=1}^{d} \frac{V_{On}}{R_n}$$

In this formula, d is the number of DC outputs, V_{On} is the DC output voltage of output n, R_n is the resistive load driven by output n.

AC_{OUT} depends on the capacitive load on each output and the frequency at which each output switches, as shown in the following formula:

$$AC_{OUT} = \sum_{n=1}^{a} C_n V_n f_n$$

In this formula, a is the number of AC outputs, C_n is the capacitive load on output n, V_n is the voltage swing of output n, and f_n is the switching frequency of output n.

The estimated maximum I_{CC} is used together with the following formula to estimate the maximum power (P_{EST}):

P_{EST} = estimated maximum $I_{CC} \times V_{CC}$

☞ The actual I_{CC} should be measured after the project is completed to verify P_{EST}.

Calculating Maximum Allowed Power for the Device & Package

The following formulas are used to calculate the maximum allowed power (P_{MAX}) for a device:

$$P_{MAX} = \frac{150^\circ C - T_{AMB}}{\theta_{JA}} \quad or \quad P_{MAX} = \frac{150^\circ C - T_{CASE}}{\theta_{JC}}$$

The maximum allowable power is dependent on the maximum allowable junction temperature of the silicon, the ambient temperature of operation, and the package's thermal resistance (θ) when configured in the system. The maximum junction temperature is specified as 150° C. The ambient temperature depends on the application. The worst-case P_{MAX} value is

estimated using the formula with θ_{JA}, the junction-to-ambient thermal resistance. θ_{JA} is a measure of the worst-case thermal resistance for a device in still air, with convection cooling only. If forced-air flow and heat-sinking are used to dissipate heat, the designer should use the junction-to-case thermal resistance, θ_{JC}, to calculate P_{MAX} for a device. θ_{JC} is a measure of the lowest possible thermal resistance.

Tables 2 through 5 provide θ_{JA} and θ_{JC} values for Altera devices.

Table 2. Thermal Resistance of Classic Devices

Device	Pin Count	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EP330	20	PDIP	68	19
		SOIC	88	17
EP610	24	CerDIP	60	10
EP610A		PDIP	55	18
EP610T		SOIC	77	17
	28	JLCC	90	12
		PLCC	74	13
EP910	40	CerDIP	40	12
EP910A		PDIP	49	23
EP910T	44	JLCC	67	5
		PLCC	58	10
EP1810	68	JLCC	47	12
EP1810T		PLCC	44	13
		PGA	38	6

Table 3. Thermal Resistance of MAX 5000/EPS464 Devices

Device	Pin Count	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EPM5016	20	CerDIP	62	10
		PDIP	61	27
		PLCC	C.F.	C.F.
		SOIC	C.F.	C.F.
EPM5032	28	CerDIP	44	12
		PDIP	48	19
		JLCC	69	9
		PLCC	59	10
		SOIC	C.F.	C.F.
EPM5064	44	JLCC	62	15
		PLCC	52	9
EPM5128	68	JLCC	39	11
		PLCC	44	12
		PGA	32	2
EPM5128A	68	JLCC	C.F.	C.F.
		PLCC	C.F.	C.F.
EPM5130	84	JLCC	30	C.F.
		PLCC	35	11
	100	CQFP	50	11
		PQFP	50	10
		PGA	26	4
EPM5192	84	JLCC	30	4
		PLCC	35	11
		PGA	27	2
EPM5192A	84	JLCC	C.F.	C.F.
		PLCC	C.F.	C.F.
EPM5192A	100	CQFP	C.F.	C.F.
		PQFP	C.F.	C.F.
EPS464	44	JLCC	68	5
		PLCC	52	9
		PQFP	C.F.	C.F.

Note:
C.F. Consult Factory

Table 4. Thermal Resistance of MAX 7000 Devices

Device	Pin Count	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EPM7032	44	PLCC	52	9
		PQFP	C.F.	C.F.
		TQFP	C.F.	C.F.
EPM7032V	44	PLCC	C.F.	C.F.
		TQFP	C.F.	C.F.
EPM7064	68	PLCC	44	12
	84	PLCC	35	11
	100	PQFP	50	10
EPM7096	68	JLCC	48	12
		PLCC	44	12
	84	JLCC	30	C.F.
		PLCC	55	11
	100	CQFP	50	11
		PQFP	50	10
EPM7128	84	PLCC	35	11
	100	PQFP	C.F.	C.F.
	160	PQFP	40	7
EPM7160	84	PLCC	35	11
	100	PQFP	50	10
	160	PQFP	40	7
EPM7192	160	PGA	20	7
		PQFP	40	7
EPM7256	192	PGA	16	6
	208	CQFP	20	6
		MQFP	17	8
		RQFP	C.F.	C.F.

Note:
C.F. Consult Factory

Table 5. Thermal Resistance of FLEX 8000 Devices

Device	Pin Count	Package	θ_{JA} (° C/W)	θ_{JC} (° C/W)
EPF8282	84	PLCC	35	11
	100	TQFP	C.F.	C.F.
EPF8282V	100	PGA TQFP	C.F. C.F.	C.F. C.F.
EPF8452	84	PLCC	35	11
	160	PQFP PGA	40 20	7 6
EPF8820	160	PQFP PGA	40 C.F.	7 C.F.
	192	PGA	16	6
	208	PQFP RQFP	40 C.F.	7 C.F.
EPF81188	232	PGA	16	6
	240	MQFP RQFP	20 C.F.	2 C.F.

Note:
C.F. Consult Factory

Comparing Maximum Allowed Power & Estimated Power

To avoid reliability problems, the system designer should compare the values calculated for maximum allowed power and estimated power. The estimated power should be the smaller of the two values. If the estimated power exceeds the maximum allowed power, refer to "Reduction of Heat Build-Up" next in this data sheet for suggestions on how to reduce power requirements for a design.

Reduction of Heat Build-Up

The following actions reduce power dissipation, and thus heat build-up, for an application.

1. *Use available low-power features of the device.* Classic devices and individual MAX 7000 macrocells can be configured for low-power operation, with only a nominal increase in propagation delay, by turning the Turbo Bit off. All macrocells in the MAX 7000 device that do not need to run in high-performance mode should be set to low-power mode.

2. *Choose a different device package.* A ceramic or higher-pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connection to the PCB.

3. *Use forced-air cooling and/or heat-sinking.* Forced-air cooling improves the efficiency of convection cooling, reducing the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.

4. *Slow the operation in portions of the circuit.* I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array Clock sources for all registers. Signals that do not require high-speed operation can use a slower array Clock that significantly reduces the system power consumption.

5. *Reduce the number of outputs.* DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the project, and thereby reduce the power.

6. *Reduce the amount of circuitry in the device.* Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.

7. *Choose a different device family.* The MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features at low density.

8. *Modify the design to reduce power.* Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact Altera Applications at (800) 800-EPLD.

Device Erasure

Altera Classic, MAX 5000/EPS464, EPS448, and MAX 7000 devices use non-volatile, reprogrammable EPROM or EEPROM memory cells to retain the configuration data so that the configuration data does not need to be reloaded when the system powers up. EPROM and EEPROM memory-cell technologies have similar programming characteristics, but different erasure mechanisms.

Altera's EPROM-based devices are available in both plastic and ceramic packages. Plastic packages for EPROM devices are one-time-programmable (OTP) devices; windowed ceramic packages allow erasure by exposure to UV light. Altera EPROM-based devices begin to erase when exposed to lights with wavelengths shorter than 4,000 Å. Since fluorescent lighting and sunlight fall into this range, an opaque label must be placed over the device window to ensure long-term reliability. To completely erase a device, it must be exposed to UV light with a wavelength of 2,540 Å. Devices should be erased for one hour by an eraser system with a power rating of 12,000 $\mu W/cm^2$. Altera devices may be damaged by long-term exposure to high-intensity UV light.

Altera guarantees that its EPROM-based devices can be programmed and erased at least 25 times, provided the recommended erasure exposure levels are used. Most devices can be reliably erased and reprogrammed many more times beyond this guaranteed minimum.

Altera's EEPROM-based devices are available in reprogrammable plastic packages. (The EPM7192 is also available in a windowless ceramic PGA package.) EEPROM cells are electrically erasable and therefore do not have an erasure window. These EEPROM-based devices are erased immediately before being programmed, and can be erased and reprogrammed at least 100 times. Most devices can be reliably erased and reprogrammed many more times beyond this guaranteed minimum.

Notes:

Configuring FLEX 8000 Devices

August 1993, ver. 2 Application Note 33

Introduction

The architecture of Altera's Flexible Logic Element MatriX (FLEX) devices supports several different configuration schemes for loading a design into one or more devices on the circuit board. This application note provides complete details on all aspects of FLEX 8000 device configuration, including sample schematics and timing information.

This application note should be used together with the *FLEX 8000 Programmable Logic Device Family Data Sheet* and the *Configuration EPROMs for FLEX 8000 Devices Data Sheet* in this data book. If appropriate, illustrations in this application note show devices with generic "FLEX 8000" and "Configuration EPROM" labels to indicate that they are valid for all FLEX 8000 devices and Altera Configuration EPROMs. All timing parameters shown in figures and tables apply to all FLEX 8000 device speed grades.

The following topics are discussed:

FLEX 8000 Device Operating Modes

The FLEX architecture uses SRAM cells to store the configuration data for the device. These SRAM cells must be loaded each time the circuit powers up and begins operation. The process of physically loading the SRAM programming data into the FLEX 8000 device is called *configuration*. After configuration, the FLEX 8000 device resets its registers, enables its I/O pins, and begins operation as a logic device. This reset operation is called *initialization*. Together, the configuration and initialization processes are called *command mode*; normal in-circuit device operation is called *user mode*.

SRAM technology allows FLEX 8000 devices to be reconfigured in-circuit by loading new configuration data. Real-time reconfiguration can be performed by forcing the device into command mode with a dedicated device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire process requires less than 100 ms, and can be used to dynamically reconfigure FLEX 8000 devices during system operation.

Existing systems that incorporate FLEX 8000 devices can be updated by installing new data in the system. Such in-field upgrades can be as simple as copying a new configuration file to a hard disk, or inserting an EPROM programmed with new configuration data into the circuit.

Device configuration can occur either automatically at system power-up or under the control of external logic. Initialization can be controlled by the internal oscillator in the FLEX 8000 device or by an external Clock signal. Dedicated device configuration pins can be used to control when configuration and initialization begin. This range of command-mode control features provides excellent flexibility for designs implemented in FLEX 8000 devices.

Overview of Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, which you choose on the basis of the target application. Both active and passive schemes are available. In an active configuration scheme, the FLEX device guides the configuration operation, controlling external memory devices and the initialization process. The Clock source for all active configuration schemes is an internal oscillator in the FLEX 8000 device that typically operates in the range of 2 to 6 MHz. In a passive configuration scheme, an external controller guides the configuration of the FLEX 8000 device, which operates as a slave. Table 1 shows the source of data for each of the six configuration schemes.

Table 1. Configuration Schemes

Configuration Scheme	Acronym	Data Source
Active Serial	AS	Altera Configuration EPROM
Active Parallel Up	APU	Parallel EPROM
Active Parallel Down	APD	Parallel EPROM
Passive Serial	PS	Serial data path
Passive Parallel Synchronous	PPS	Intelligent host
Passive Parallel Asynchronous	PPA	Intelligent host

Each FLEX 8000 device has a different size requirement for its configuration data, based on the number of SRAM cells in the device. Table 2 shows the amount of data, expressed in both bits and Kbytes, necessary to configure each FLEX 8000 device. You can use this table to calculate the data space (i.e., data storage resources) required in a parallel or serial data source for a system that incorporates FLEX 8000 devices.

Table 2. FLEX 8000 Device Data-Size Spaces

Device	Data Size (bits)	Data Size (Kbytes)
EPF8282, EPF8282V	40,000	5
EPF8452	64,000	8
EPF8820	128,000	16
EPF81188	192,000	24
EPF81500	250,000	31

Active Configuration

In an active configuration scheme, the FLEX 8000 device controls the entire configuration process and generates the synchronization and control signals necessary to configure and initialize itself from an external memory. The active serial (AS) configuration scheme uses an Altera Configuration EPROM to store the configuration data. The active parallel up (APU) and active parallel down (APD) configuration schemes use a parallel-format memory such as a 32K × 8-bit EPROM as the data source.

Passive Configuration

In a passive configuration scheme, the FLEX 8000 device is incorporated into a system with an intelligent host that controls the configuration process. The intelligent host transparently selects a serial or parallel data source, and the data is presented to the FLEX 8000 device on a common data bus. In this type of system, the configuration data can be stored in a mass-storage medium, such as a hard disk. With passive configuration schemes, new configuration data is easily installed by supplying a new configuration file on a diskette or tape.

Choosing a Configuration Scheme

The best configuration scheme for a particular application depends on many factors, such as the presence of an intelligent host in the system, the need to reconfigure in real-time, and the need to periodically install new configuration data. Available board space is also a consideration for configuration schemes that use parallel or serial EPROMs to store configuration data.

The following guidelines can help you decide which configuration scheme is most appropriate for your application:

- For fast time-to-market, the easiest and quickest configuration schemes to implement are the three active configuration schemes: active serial (AS), active parallel up (APU), and active parallel down (APD). These configuration schemes require no external intelligence. The FLEX 8000 device is typically configured automatically at system power-up. If the FLEX 8000 device senses a power failure, it automatically triggers a reconfiguration cycle.

- For fast prototyping and development work, the passive serial (PS) configuration scheme, together with the FLEX Download Cable, provides the quickest means of iterative design analysis. The MAX+PLUS II Programmer can directly download configuration data to a FLEX 8000 device on the prototype circuit board.

- If a FLEX 8000 device is incorporated into a system with an intelligent host, you can use this host to control the configuration process in one of the passive configuration schemes: passive parallel asynchronous (PPA), passive parallel synchronous (PPS), or passive serial (PS). The configuration data can be stored in a mass-storage medium, such as a hard disk, thereby reducing the number of ICs required for the system. The FLEX 8000 device configuration can also be synchronized with any other system resources that must be initialized.

- In applications that require real-time device reconfiguration—such as data transformation filters, video formatters, and encryption/decryption circuits—the best choice is one of the passive configuration schemes. Reconfigurability allows you to reuse the logic resources within the FLEX 8000 device, instead of designing redundant or duplicate circuitry into your systems. Passive configuration schemes easily support the multiple sources of configuration data that may be required for real-time configuration. However, these schemes require more external circuitry. The FLEX 8000 device must rely on an intelligent host to retrieve and load new configuration data, and cannot perform any of the tasks required for reconfiguration.

- If field upgrades are anticipated, passive configuration schemes offer the ability to easily install new configuration data. New configuration files can be supplied to end users on diskette or tape. (In active schemes, a new EPROM must be inserted into the system.)

You can also use multiple configuration schemes during system operation. If you choose a single configuration scheme, you can simply hard-wire the three configuration scheme selection pins (nSP, MSEL1, and MSEL0) to their necessary levels (V_{CC} or GND). If you use multiple configuration

schemes, you can drive these selection pins with some controlling logic or connect them to a port on an intelligent host. For example, you can configure a FLEX 8000 device with an AS configuration scheme to load its "start-up" configuration data, then dynamically change the configuration scheme selection bits to select a different configuration scheme, and provide a different configuration data source.

FLEX 8000 Device Configuration Schemes

The following sections describe each configuration scheme in detail:

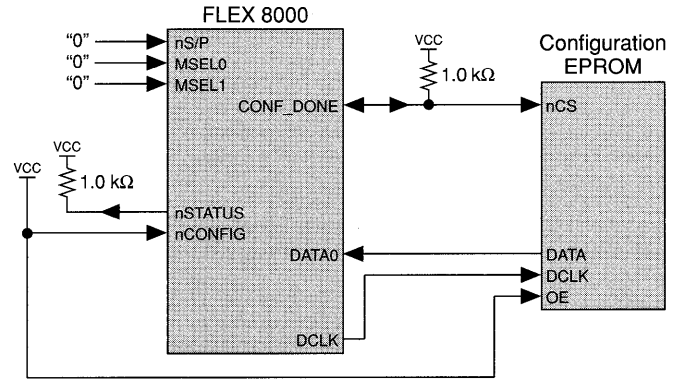
- Active serial (AS)
- Active parallel up (APU)
- Active parallel down (APD)
- Passive parallel synchronous (PPS)
- Passive parallel asynchronous (PPA)
- Passive serial (PS)

In-circuit reconfiguration, device configuration option bits, device configuration pins, and the source of data for each configuration scheme are described later in this application note.

Active Serial Configuration

The active serial (AS) configuration scheme uses an Altera-supplied serial Configuration EPROM (e.g., EPC1213) as a data source for FLEX 8000 devices. The Configuration EPROM presents its data to the FLEX 8000 device in a serial bit-stream. Figure 1 shows a typical circuit in which the FLEX 8000 device controls the configuration process and uses a serial Configuration EPROM as the data source.

Figure 1. Active Serial Device Configuration



The nCONFIG pin on the FLEX 8000 device in Figure 1 is connected to V_{CC}, so the device automatically configures itself at system power-up. The system can monitor the nSTATUS pin to ensure that configuration occurs correctly. Immediately after power-up, the FLEX 8000 device pulls the nSTATUS pin low and releases it within 100 ms. Once released, the open-drain nSTATUS pin is pulled up to V_{CC} by an external 1.0-kΩ pull-up resistor. If an error occurs during configuration, the FLEX 8000 device pulls the nSTATUS pin low, indicating that configuration was unsuccessful.

The DCLK signal, which is driven by the FLEX 8000 device, clocks sequential data bits from the Configuration EPROM. While the SRAM data is being loaded, the FLEX 8000 device holds the open-drain CONF_DONE pin at GND, indicating that data is loading. A 24-bit program-length counter within the FLEX 8000 device stores the program length, i.e., the total number of configuration bits. Once the terminal count value for the configuration data (i.e., the last configuration data bit) has been reached, the FLEX 8000 device releases the CONF_DONE pin, which is subsequently pulled up to V_{CC} by an external 1.0-kW pull-up resistor. The resulting high input on the nCS pin causes the Configuration EPROM to tri-state its DATA output, electrically removing the Configuration EPROM from the circuit.

After it releases the CONF_DONE pin, the FLEX 8000 device uses it as an input for monitoring the configuration process. When the FLEX 8000 device senses a high logic level on CONF_DONE, it completes the initialization process and enters user mode. Figure 2 shows the timing associated with the AS configuration process and the order of transitions on the control signals.

Figure 2. Active Serial Configuration Timing Waveforms

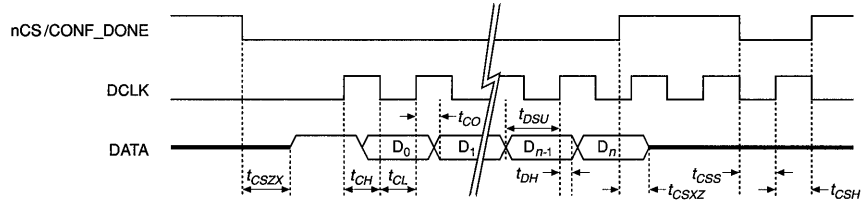


Table 3 provides values for the AS timing parameters.

Table 3. Active Serial Configuration Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled		50	ns
t_{CSZX}	nCS low to DATA output enabled		50	ns
t_{CSXZ}	nCS high to DATA output disabled		50	ns
t_{CH}	DCLK high time	80	250	ns
t_{CL}	DCLK low time	80	250	ns
t_{DSU}	Data setup time before rising edge on DCLK	50		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CO}	DCLK to DATA out		75	ns
t_{OEW}	OE low pulse width to guarantee counter reset	100		ns
t_{CSS}	nCS low to first DCLK rising edge	100		ns
t_{CSH}	nCS low hold time after DCLK rising edge	0		ns

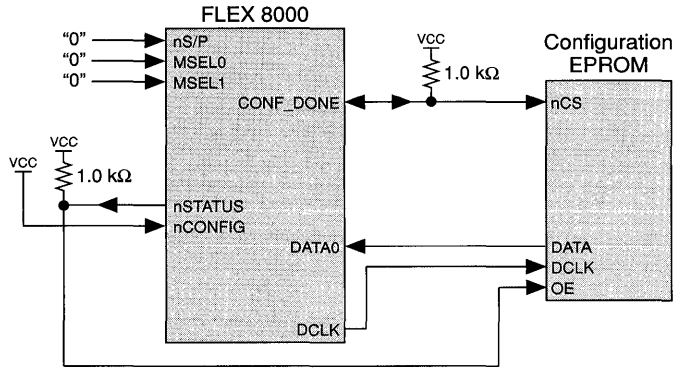
In the circuit shown in Figure 1, the nCONFIG pin on the FLEX 8000 device is tied to the Output Enable (OE) input of the Configuration EPROM; both are tied to V_{CC}. A high logic level on the nCONFIG input automatically starts the configuration. The output of the serial Configuration EPROM is enabled by a high input on its OE pin. If an error occurs during circuit configuration, the FLEX 8000 device pulls and holds the nSTATUS pin low, indicating a configuration error. External circuitry is used to monitor the nSTATUS pin and take appropriate action if configuration fails. This circuitry must assert a high-low-high pulse on the nCONFIG pin to reconfigure the device after the error. The same circuitry can also be used to begin reconfiguring the FLEX 8000 device at any time after system power-up.

The FLEX 8000 device's built-in *Auto-Restart Configuration on Frame Error* option bit allows the device to automatically reconfigure itself if it encounters an error during configuration. If this option bit is turned on, a configuration error causes the FLEX 8000 device to pull the nSTATUS pin low for 10 internal Clock cycles and then release it. This 1- to 3-µs pulse on the nSTATUS pin provides an external indication that reconfiguration is about to begin. It also can be used to reset the Altera Configuration EPROM.

Figure 3 shows a circuit that uses the *Auto-Restart Configuration on Frame Error* option. The nSTATUS pin is connected to the OE input on the Altera serial Configuration EPROM so that the error-reset pulse on nSTATUS resets the internal address counter on the Configuration EPROM and prepares it to reconfigure the FLEX 8000 device. The nCONFIG input is also available to initiate a reconfiguration cycle externally. Since the nSTATUS pin is pulled low and then released whenever configuration begins, it

resets the Configuration EPROM before reconfiguration. If V_{CC} drops below the power-on reset (POR) threshold for the FLEX 8000 device during device operation, nSTATUS is pulsed and the Configuration EPROM is reset in the same way to provide automatic reconfiguration. Timing for the circuit in Figure 3 is identical to the timing shown in Figure 2 for the AS configuration scheme (the error-reset pulse on nSTATUS is not shown).

Figure 3. Active Serial Device Configuration with Automatic Reconfiguration on Error



The Altera serial Configuration EPROMs are designed for performance that is compatible with the setup and hold time requirements of FLEX 8000 devices. Refer to the *Configuration EPROMs for FLEX 8000 Devices Data Sheet* in this data book for complete details on timing and circuitry. Details on device programming are given in "Programming a Serial Configuration EPROM" later in this application note.

Active Parallel Up & Active Parallel Down Configuration

In the active parallel up (APU) and active parallel down (APD) configuration schemes, the FLEX 8000 device generates sequential addresses that drive the address inputs to an external PROM. The PROM then returns the appropriate byte of data on the data pins DATA[7..0]. Sequential addresses are generated until the FLEX 8000 device has been completely loaded. The CONF_DONE pin is then released and pulled high externally, indicating that configuration has been completed. The counting sequence can be ascending (00000H to 3FFFFH) for APU configuration or descending (3FFFFH to 00000H) for APD configuration.

Figure 4 shows a typical circuit with a FLEX 8000 device and a parallel EPROM for APU or APD configuration. In this circuit, the nCONFIG input to the FLEX 8000 device is connected to a system-wide, active-low Reset

signal. The nCONFIG pin can be tied to V_{CC} (as shown in Figure 1) to start configuration automatically at system power-up; however, the system-wide Reset allows you to explicitly control the time at which configuration begins. The nCONFIG pin must be held low to meet the minimum low pulse width requirement for t_{CFG} (see Table 4 later in this application note).

Figure 4. Active Parallel Device Configuration with a 256-Kbyte EPROM

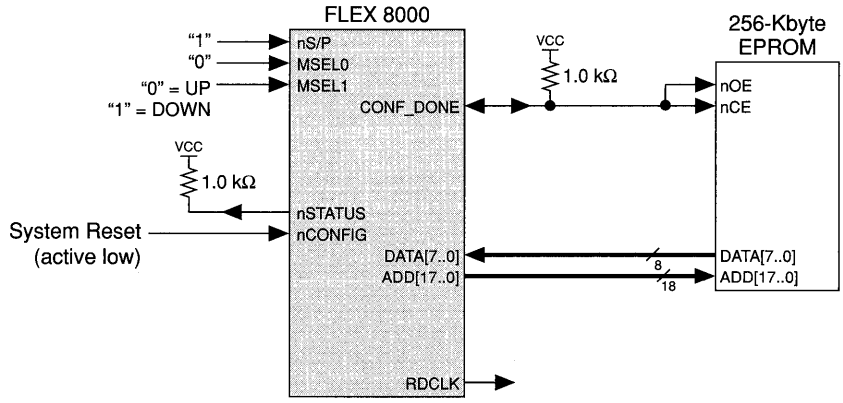
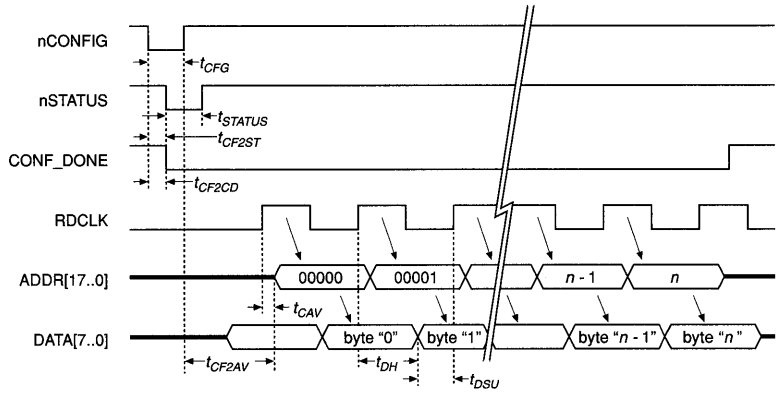


Figure 5 shows the timing associated with the circuit in Figure 4. The high-low-high pulse on the nCONFIG pin starts the configuration process. The nSTATUS pin is pulled low for up to 100 ms, and the CONF_DONE pin is pulled down to GND. Once the CONF_DONE pin is low, address generation begins. The low logic level on the CONF_DONE pin also enables the output of the EPROM. In an APU configuration scheme, the first address generated is 00000H; in an APD configuration scheme, it is 3FFFFH.

The configuration events in Figure 5 are based on the RDCLK signal rather than the DCLK signal. The RDCLK signal, a Clock signal that is generated by dividing the DCLK signal by eight, is used to frame the data bytes supplied by the parallel EPROM. In the APU and APD configuration schemes, the FLEX 8000 device generates the DCLK signal internally and uses it to serialize the incoming data words. On each pulse of the RDCLK signal, the FLEX 8000 device latches an 8-bit byte, and the following eight pulses on DCLK convert that 8-bit value into a serial data stream. The RDCLK signal is available as an output pin during configuration. (In user mode, the RDCLK pin is available as an I/O pin.) You can monitor this signal to ensure that the parallel EPROM observes the data setup and hold time requirements for the FLEX 8000 device.

Figure 5. Active Parallel Up Configuration Timing Waveforms

A rising edge on RDCLK increments the address counter ADDR[17..0], which is driven out to the parallel EPROM. The parallel EPROM then sends the addressed byte of configuration data to the FLEX 8000 device.



A new address is presented on the ADD[17..0] pins a short time (t_{CAV}) after a rising edge on RDCLK. Table 4 shows the timing parameters for the APU and APD configuration in Figure 4. Before the subsequent rising edge on RDCLK, the external parallel EPROM must present valid data soon enough to meet the t_{DSU} setup time for the data. This subsequent rising edge on RDCLK latches data, based on the address generated by the previous Clock cycle. EPROMs with access times faster than 500 ns should be used to guarantee the data setup time.

Table 4. Active Parallel Up & Down Configuration Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{CF2ST}	nCONFIG low to nSTATUS low		1	µs
t_{CFG}	nCONFIG low pulse width	2		µs
t_{STATUS}	nSTATUS low pulse width	2.5		µs
t_{CF2CD}	nCONFIG low to CONF_DONE low		1	µs
t_{CF2AV}	nCONFIG high to first valid address		3.5	µs
t_{CAV}	RDCLK rising edge to address valid		1	µs
t_{DH}	Data hold time after rising clock edge (RDCLK)	0		ns
t_{DSU}	Data setup time before rising clock edge (RDCLK)	50		ns

Once the terminal count value for the FLEX 8000 device configuration data is reached, the FLEX 8000 device releases the CONF_DONE pin. The CONF_DONE

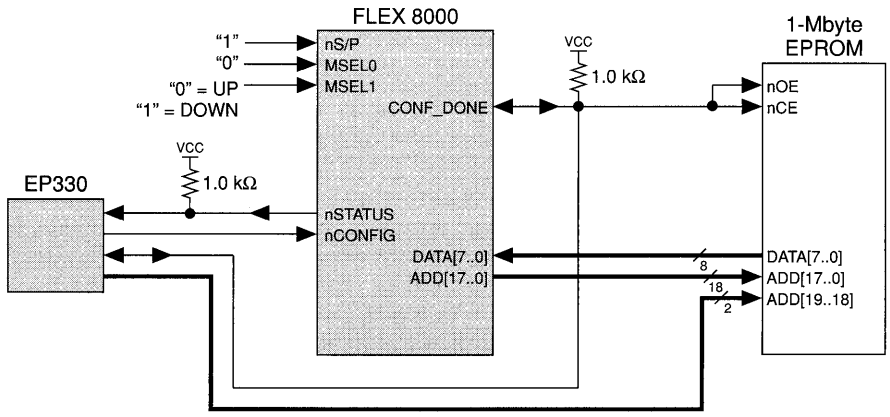
pin is pulled up to V_{CC} via the pull-up resistor, and the FLEX 8000 device disables the output on the EPROM. Since the DATA[7..0] pins on the EPROM are tri-stated after configuration, the corresponding DATA[7..0] pins on the FLEX 8000 device are available as I/O pins during user-mode operation.

All FLEX 8000 devices provide 18 address lines, which are sufficient to uniquely decode up to 256 Kbytes of data, much more than the largest FLEX 8000 device requires. See Table 2.

Although the 18 address lines limit FLEX 8000 devices to addressing 256 Kbytes of data, you can use a larger EPROM device (e.g., 512 Kbytes, 1 Mbyte, 2 Mbytes, etc.) by masking in the necessary offset addresses. In larger EPROMs, the FLEX 8000 device configuration information is treated as a separate "page" in the EPROM, and can be placed on any convenient boundary. However, some additional logic is required to provide the offset address.

Figure 6 shows how you can use an Altera EP330 device as a decoder that asserts the necessary page-offset address onto the address bus during configuration. The EP330 allows the 18-bit address generated by the FLEX 8000 device to select one of four 256-Kbyte "pages" in the EPROM. The EP330 should monitor the nSTATUS and CONF_DONE signals to ensure that errors are handled correctly. The inputs to the EP330 must be system-level control signals that select the appropriate page in the EPROM to be loaded into the FLEX 8000 device, and control when the configuration actually occurs. Timing for the circuit in Figure 6 is identical to the timing shown in Figure 5.

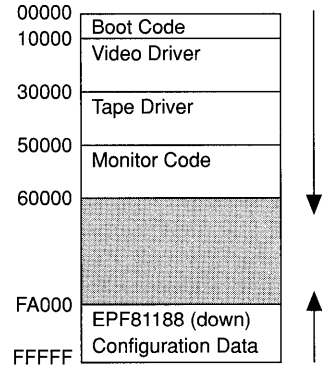
Figure 6. Active Parallel Device Configuration with Offset Address Generation Circuitry



The active parallel configuration schemes can generate addresses in either an ascending or descending order, depending on your system requirements. Counting up (APU configuration) is appropriate if the FLEX 8000 configuration data is stored at the beginning of an EPROM, or if the configuration data has been placed at some known offset in an EPROM larger than 256 Kbytes. Counting down (APD configuration) is appropriate if the low addresses are not available, e.g., if the CPU code must use the beginning of the EPROM or if the EPROM is also used to store other information that is expected to increase as an application evolves. The changing nature of the data size is characteristic of basic I/O system (BIOS) and boot PROMs.

Figure 7 shows an example of a BIOS EPROM memory map, in which the FLEX 8000 configuration data is placed at the top of the memory space in an APD configuration.

Figure 7. Typical BIOS EPROM Memory Map



Passive Parallel Synchronous Configuration

In a passive parallel synchronous (PPS) configuration scheme, the FLEX 8000 device is tied to an intelligent host. With PPS configuration, data can be driven directly onto a common data bus between the host and the FLEX 8000 device. The DCLK, CONF_DONE, nCONFIG, and nSTATUS signals are connected to a port on the host. Although you can drive the DCLK signal from the system Clock, you must have precise control of any interrupts that can influence the internal counting of the FLEX 8000 devices. This precise control is required because the FLEX 8000 device latches data on the rising edge of the DCLK signal, and the next eight falling edges of the DCLK signal serialize the latched data. New data is latched on every eighth rising edge of the DCLK signal until the FLEX 8000 device is completely configured.

Figure 8 illustrates PPS configuration of a FLEX 8000 device. In this circuit, the CPU generates a byte of configuration data and directs the FLEX 8000

device to latch and serialize the data by strobing a high pulse on the DCLK input. In Figure 8, no specific source is shown for the data bus DATA[7..0], which is typically driven by a dedicated data latch. A microcontroller host usually has byte-wide ports that can be used for this data bus. If the host is a CPU or intelligent logic, a dedicated data register can be implemented with an octal latch. Depending on the capability of the host and the memory space implementation in the system, you can use an external memory instead to drive the data onto the system data bus. This type of external memory usage requires the memory to hold the data on the bus while the host executes the commands to direct the FLEX 8000 device to latch and serialize the data. However, not all processors can accommodate this type of operation.

Figure 8. Passive Parallel Synchronous Device Configuration

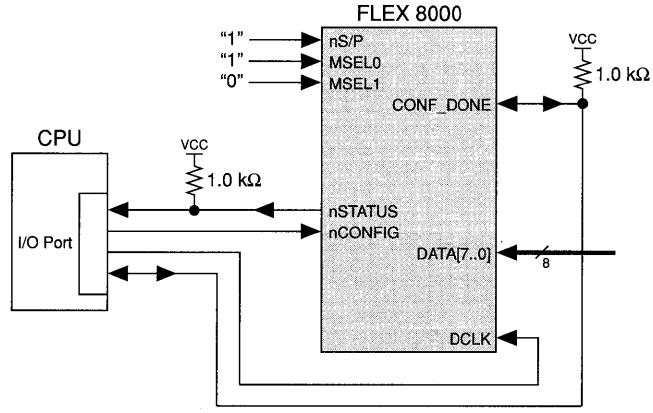


Figure 9 shows the timing for the PPS configuration scheme. The CPU generates Clock cycles and data; eight DCLK cycles are required to latch and serialize each 8-bit data word. A new data word must be present at the DATA[7..0] inputs upon every eighth DCLK cycle.

Figure 9. Passive Parallel Synchronous Configuration Timing Waveforms

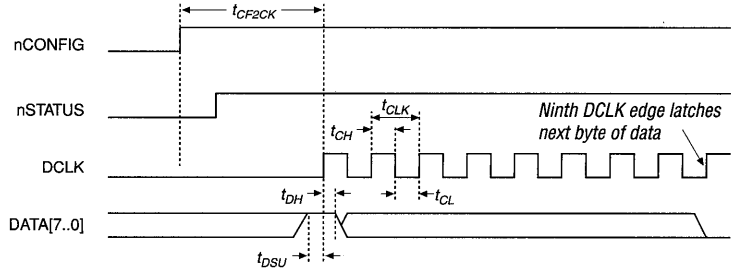


Table 5 shows the timing parameters associated with PPS configuration.

Table 5. Passive Parallel Synchronous Configuration Timing Parameters

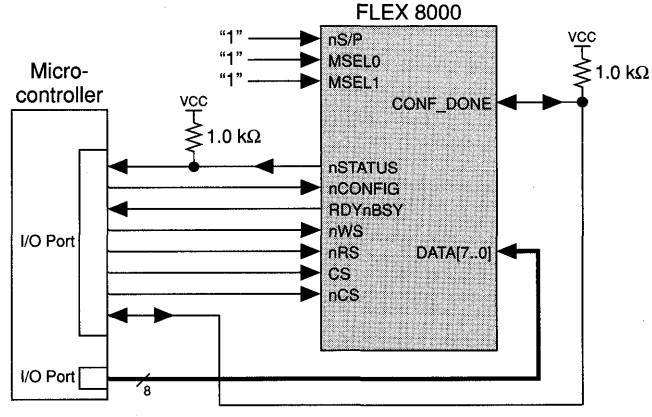
Symbol	Parameter	Min	Max	Unit
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	5		µs
t_{DSU}	Data setup time before rising edge on DCLK	50		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CH}	DCLK clock high time	80		ns
t_{CL}	DCLK clock low time	80		ns
t_{CLK}	DCLK period	160		ns
f_{MAX}	DCLK maximum frequency		6	MHz

Passive Parallel Asynchronous Configuration

With the passive parallel asynchronous (PPA) configuration scheme, a FLEX 8000 device in a system can be configured in parallel with the rest of a board. The FLEX 8000 device accepts a parallel byte of input data, then serializes the data with its internal synchronization Clock. The device is selected with the nCS and CS chip select pins, so multiple devices can reside on the same data bus. The ability to select individual FLEX 8000 devices allows multiple devices to be configured in parallel by a single intelligent host.

This efficient handshaking allows an intelligent host to simultaneously configure multiple FLEX 8000 devices or other configurable portions of the system. Figure 10 illustrates PPA configuration of a FLEX 8000 device. A

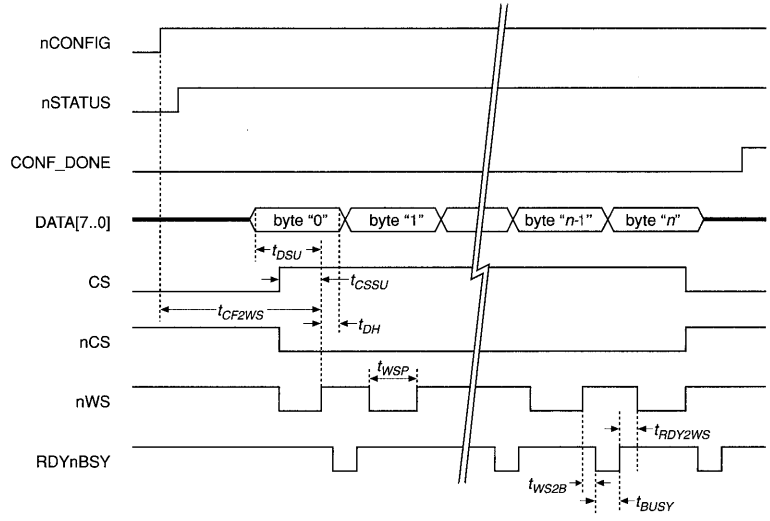
Figure 10. Passive Parallel Asynchronous Device Configuration with Dedicated Ports



microcontroller is used as the intelligent host to ensure that sufficient dedicated I/O ports are available to drive all control signals and the data bus to the FLEX 8000 device. The chip select signals CS and nCS are both used to select the device. However, you can also tie nCS to GND and control chip selection with the CS pin only (or vice-versa), thus saving one bit in the I/O port.

Figure 11 shows the timing for the PPA configuration scheme. The CPU presents an 8-bit data word to the FLEX 8000 device, and indicates that the word is valid by strobing a low pulse on the nWS input. The FLEX 8000 device senses the rising edge of the nWS signal, latches the data on the DATA[7..0] inputs, and uses its internal oscillator to serialize the 8-bit data word.

Figure 11. Passive Parallel Asynchronous Timing Waveforms



The CPU must poll the RDYnBUSY signal to establish when the FLEX 8000 device is ready to receive more data. RDYnBUSY falls immediately after the rising edge of the DCLK signal that latches data, indicating that the device is busy. While the FLEX 8000 device processes the data byte, RDYnBUSY remains low. On the eighth falling edge of DCLK, RDYnBUSY returns to V_{CC}, indicating that another byte of data can be latched. Table 6 shows the timing parameters associated with PPA configuration.

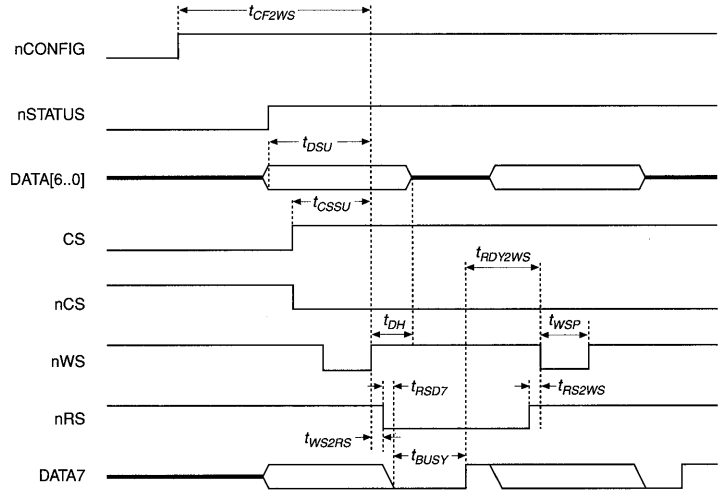
As an alternative to polling the RDYnBUSY signal, the CPU can determine the status of the FLEX 8000 device by strobing a low pulse on the nRS input to the FLEX 8000 device. This strobe causes the FLEX 8000 device to present the RDYnBUSY status on the bidirectional pin DATA7 so that the CPU

Table 6. Passive Parallel Asynchronous Configuration Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{CF2WS}	nCONFIG high to first nWS rising edge	5		µs
t_{DSU}	Data setup time before rising edge on nWS	50		ns
t_{DH}	Data hold time after rising edge on nWS	0		ns
t_{CSSU}	Chip selected delay before rising edge on nWS	50		ns
t_{WSP}	nWS low pulse width	500		ns
t_{WS2B}	nWS rising edge to RDYnBSY low		50	ns
t_{BUSY}	RDYnBSY low pulse width		4	µs
t_{RDY2WS}	RDYnBSY rising edge to nWS falling edge	50		ns
t_{WS2RS}	nWS rising edge to nRS falling edge	500		ns
t_{RS2WS}	nRS rising edge to nWS falling edge	500		ns
t_{RSD7}	nRS falling edge to DATA7 valid with RDYnBSY signal		50	ns

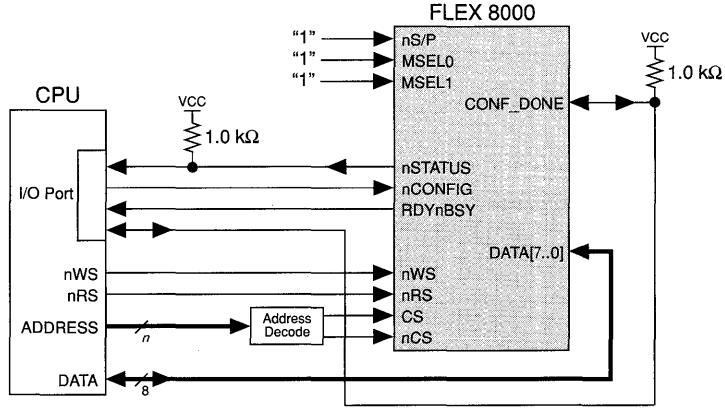
can determine device status from the data bus, instead of using an additional port on the CPU for the RDYnBUSY signal. This low pulse on nRS must occur only during the corresponding high pulse (inactive) on the nWS signal. The timing waveforms in Figure 12 show how the nRS pin can be used to poll the status of the device with the bidirectional pin DATA7 of the circuit shown in Figure 10. The timing parameters given in Table 6 also apply to Figure 12.

Figure 12. Passive Parallel Asynchronous Timing Waveforms Using nRS & DATA7



The circuit in Figure 10 takes advantage of the architecture of a microcontroller host. Figure 13 shows an alternative to this circuit, in which a CPU serves as the intelligent host and the FLEX 8000 device is treated more as a memory than as a port. The nWS and nRS inputs to the FLEX 8000 device are driven by the CPU's memory read/write control pins; the DATA[7..0] inputs to the FLEX 8000 device are driven directly by the system data bus. As in Figure 10, the nSTATUS and nCONFIG control signals must be driven by an intelligent I/O port, but the CS and nCS chip select signals are decoded from the address bus and not driven from an I/O port on the CPU. This address decoding scheme allows the CPU to write to the FLEX 8000 device as a memory. A small programmable logic device, such as the Altera EPM7032, is ideal for quickly decoding a wide address and selecting the FLEX 8000 device.

Figure 13. Passive Parallel Asynchronous Device Configuration with Address Decoding



PPA configuration is useful when multiple FLEX 8000 devices are configured simultaneously. The CPU reads a byte of configuration data from the disk or from memory, and then writes it to the FLEX 8000 device. The CPU then polls the RDYnBUSY signal (or the DATA7 pin via the nRS input) to determine when another data byte can be written. Timing for this circuit is identical to the timing shown in Figure 12, although t_{CSSU}, the minimum chip select delay before the rising edge of nWS, must increase to account for the time required to decode the address.

The configuration process is generally controlled with a precise order of steps, so the timing constraints are minimal. The following steps show the typical control sequence executed by the CPU:

1. Pull the nCONFIG pin to GND, hold it for 10 µs, then pull it up to V_{CC}.
2. Read the next byte of configuration data from an EPROM or a mass storage device such as a hard disk.
3. Generate the address of the FLEX 8000 device.
4. Perform a memory write cycle to the FLEX 8000 device address using the stored configuration data byte.
5. Poll the RDYnBUSY signal. When it goes high, transfer the next byte of configuration data by repeating steps 2 through 4.
6. Repeat steps 2 through 5 until the FLEX 8000 device pulls the CONF_DONE net high, which indicates that configuration is complete.

Passive Serial Configuration

The passive serial (PS) configuration scheme uses an external controller to configure the FLEX 8000 device with a serial bit-stream. The FLEX 8000 device is treated as a slave device with a 5-wire interface to the external controller. The external controller can be one of the following:

- The MAX+PLUS II Programmer, used together with the PL-MPU Master Programming Unit, an appropriate device adapter, and the FLEX Download Cable.

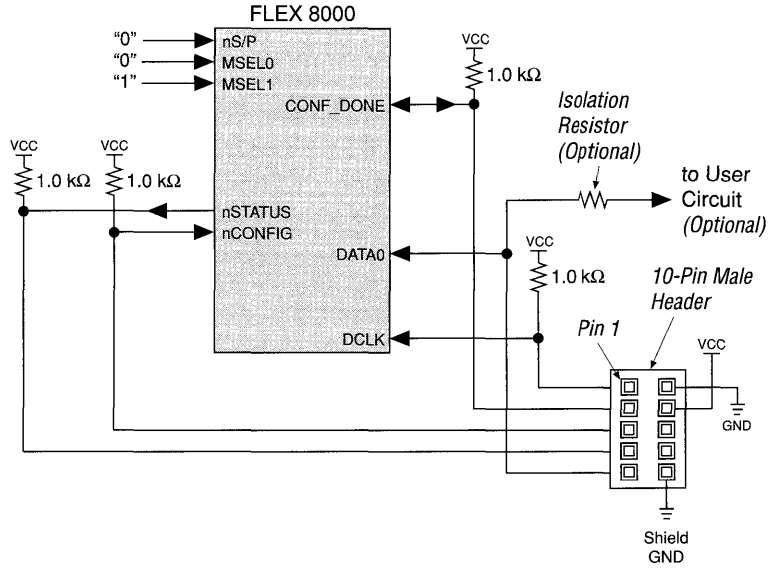
- An intelligent host such as a microcontroller or a CPU. This type of PS configuration is similar to the PPA and PPS configuration schemes, but uses a bit-wide serial data path instead of a byte-wide parallel data path.

Passive Serial Configuration with the FLEX Download Cable

Passive serial (PS) configuration uses the MAX+PLUS II Programmer and Altera programming hardware as the external controller. The Altera FLEX Download Cable can connect any Configuration EPROM programming adapter, which is installed on the PL-MPU Master Programming Unit, to a single target FLEX 8000 device in the prototype system. The FLEX Download Cable provides a 5-wire connection between the FLEX 8000 device and the programming adapter. Configuration data is taken from the SRAM Object File (**.sof**) generated automatically during project compilation and downloaded by the MAX+PLUS II Programmer. Once the device is configured, the programming hardware is tri-stated and electrically removed from the circuit. This type of PS configuration allows you to perform multiple design iterations rapidly.

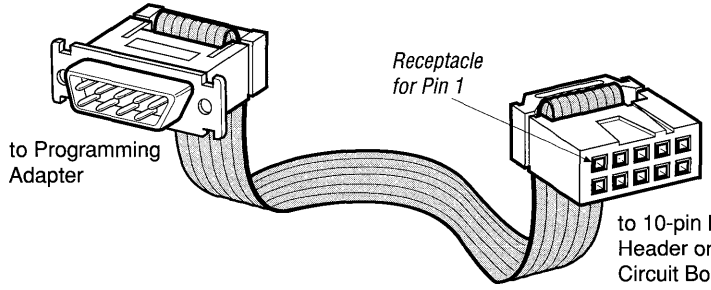
Figure 14 shows how the FLEX Download Cable interfaces to the target FLEX 8000 device. The 10-pin male header on the circuit board has two rows of five pins, spaced on 0.1-inch centers, that connect to the configuration pins on the FLEX 8000 device. Standard 10-pin IDS-type male headers are readily available to provide the target board connections.

Figure 14. Passive Serial Device Configuration with the FLEX Download Cable



A 10-pin female plug on one end of the FLEX Download Cable is connected to the 10-pin male header on the circuit board; the other end of the FLEX Download Cable is connected to a Configuration EPROM programming adapter. See Figure 15. Timing for PS configuration is identical to the timing for bit-wide PS configuration shown later in this application note.

Figure 15. FLEX Download Cable Signals & Positions



Header Pin Connections:

DCLK	CONF_DONE	nCONFIG	nSTATUS	DATA0
GND	VCC	N.C.	N.C.	GND

When a FLEX 8000 device is configured via the FLEX Download Cable, the DCLK, CONF_DONE, nCONFIG, DATA0, and nSTATUS pins on the cable are connected directly to the pins of the same names on the FLEX 8000 device. The VCC and GND pins must be tied to the system power planes. These VCC and GND pins supply power to the optical isolation circuitry in the programming adapter; they do not supply power to the target FLEX 8000 device. Refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for device pin numbers.

The DCLK, CONF_DONE, nCONFIG, and nSTATUS pins on the FLEX 8000 device are dedicated configuration pins. Since they are not available as user I/O pins, they do not require isolation from the rest of the circuit. However, a system must include pull-up resistors that pull these pins up to V_{CC}, as shown in Figure 14. These resistors allow you to remove the FLEX Download Cable after configuration is complete without introducing any noise from floating inputs.

The DATA0 pin is available as an I/O pin during user-mode operation, and may require isolation, depending on how it is used. During configuration, the DATA0 pin on the FLEX 8000 device acts as an input, and is driven by the programming hardware. If the DATA0 pin is an output pin during user mode, the signal that it drives does not need to be buffered. However, if the DATA0 pin is an input or bidirectional pin during user mode, contention may occur between the user-mode signal and the FLEX Download Cable during configuration.

If the signal that drives the DATA0 pin during user mode is tri-stated during configuration and initialization, no conflict occurs. However, if this signal is active during configuration, the DATA0 input pin must be isolated from the active source. You can isolate the DATA0 pin by inserting a tri-state buffer between the DATA0 pin and the rest of the network that it drives. This tri-state buffer must be controlled by external logic.

If you cannot use active isolation, placing a 550-Ω resistor between the user-mode signal and the DATA0 pin should provide adequate isolation. The FLEX Download Cable is driven by 12-mA drivers, which supply sufficient current to mask any signals that may be present at the other end of the resistor. Resistive isolation may not be suitable for very-high-speed circuits. Actual in-circuit performance should be evaluated in the laboratory to ensure that this isolation scheme does not affect other portions of the circuit.

The No Connect (N.C.) pins shown in Figure 15 are reserved, and should not be tied to any data or power signals. The header should be placed as close as possible to the FLEX 8000 device.

For additional information on passive serial configuration with the FLEX Download Cable, refer to "Configuring a FLEX 8000 Device In-System

with MAX+PLUS II & the FLEX Download Cable" later in this application note.

Bit-Wide Passive Serial Configuration

The passive serial (PS) configuration scheme provides a bit-wide passive interface for device configuration. No handshaking is provided in any PS configuration. Therefore, the FLEX 8000 device must be configured at 2 MHz or less. Figure 16 shows how a bit-wide PS configuration is implemented. Data bits are presented on the DATA0 input, with the least significant bit of each byte of data presented first. The DCLK is strobed with a high pulse to latch the data. This serial data loading continues until the CONF_DONE pin goes high, indicating that the device is fully configured. The data source can be any source that the host can address.

Figure 16. Bit-Wide Passive Serial Device Configuration

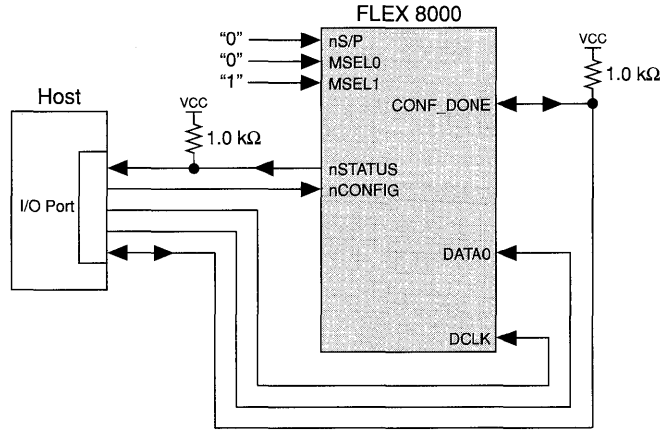


Figure 17 shows the timing for bit-wide PS configuration.

Figure 17. Bit -Wide Passive Serial Timing Waveforms

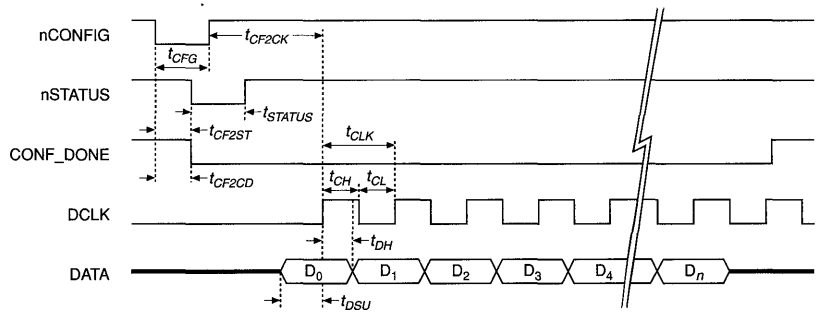


Table 7 gives the timing parameters for bit-wide PS configuration.

Table 7. Passive Serial Configuration Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low		1	µs
t_{CF2ST}	nCONFIG low to nSTATUS low		1	µs
t_{CFG}	nCONFIG low pulse width	2		µs
t_{STATUS}	nSTATUS low pulse width	2.5		µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	5		µs
t_{DSU}	Data setup time before rising edge on DCLK	50		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CH}	DCLK high time	250		ns
t_{CL}	DCLK low time	250		ns
t_{CLK}	DCLK period	500		ns

In-Circuit Reconfiguration

After a FLEX device has entered the user mode, you can choose to replace the configuration data pattern inside a FLEX 8000 device at any time. In this process, called *in-circuit reconfiguration*, new configuration data is selected using one of three methods, depending on the configuration scheme:

- In a passive configuration scheme, a different file can be downloaded from a mass-storage system.
- In the AS configuration scheme, multiple sets of configuration data can be stored in one or more serial Configuration EPROMs. Each set of data is used in succession.
- In the APU and APD configuration schemes, new configuration data is selected by externally multiplexing a different EPROM source onto the data path or by providing offset address generation circuitry to select a different page within the same EPROM.

Because the SRAM cells used to configure the functionality of the FLEX architecture are volatile, they can be reprogrammed without removing the FLEX 8000 device from the circuit board.

The nCONFIG input controls device reconfiguration. In the active configuration schemes shown in Figures 1 and 3, the nCONFIG pin is tied to V_{CC} to force the FLEX 8000 device to automatically configure itself at system power-up. In the PPA and PPS configuration schemes, controlling logic is used on the nCONFIG input to determine when the configuration starts, as shown in Figures 8, 10, and 13. However, all configuration

schemes allow you to connect the nCONFIG pin to a port on an intelligent host, which can be used to control the configuration process. If nCONFIG is held low, the configuration process can be delayed as necessary. For example, the nCONFIG pin can be held low during system initialization and then pulled high when it is appropriate to configure the FLEX 8000 device.

At any time during system operation, regardless of the current state of the FLEX 8000 device, the nCONFIG pin can be used to restart the configuration process. When nCONFIG is driven low and then high again, the device resets itself and prepares for configuration. In an active configuration scheme, the FLEX 8000 device immediately starts retrieving data from the external EPROM; in a passive configuration scheme, it prepares to receive the data from the intelligent host. An example of a reset pulse on nCONFIG in an APU configuration scheme is shown in Figure 5 earlier in this application note. This nCONFIG timing applies to all configuration schemes whenever the device is reconfigured.

All latched and registered data in the device is lost during reconfiguration, so any counter values or the current state of the device should be stored either in the intelligent host's storage system or in some external circuitry, such as an Altera EPLD. The entire reconfiguration process requires about 100 ms. The system resumes normal operation after the FLEX 8000 device releases the CONF_DONE pin, indicating that initialization is complete.

Configuration Control Features

Within a FLEX 8000 device, the configuration and initialization processes can be controlled with two types of built-in resources:

- Device configuration option bits
- Device configuration pins

This section provides detailed information on configuration option bits and pins. The usage of various options and pins is discussed in the descriptions of individual configuration schemes earlier in this application note. Some configuration pins and options can also be used together to provide additional configuration and initialization control.

Device Configuration Option Bits

FLEX 8000 devices have device configuration option bits that allow you to control device behavior during configuration. Table 8 describes all FLEX 8000 device option bits and their availability in different configuration schemes. You can set these options on a device-by-device basis during design entry in the MAX+PLUS II Graphic, Text, or Waveform Editor with the **FLEX 8000 Individual Device Options** dialog box, which is accessible from the **Chip to Device** dialog box on the Assign menu. (In MAX+PLUS II for workstations, the **Chip to Device** dialog box is available on the Compiler's Device menu.) You can also enter default device option settings

for an entire project in the MAX+PLUS II Compiler with the **FLEX 8000 Device Options** dialog box, which is accessible from the **Device Options** dialog box (Device menu).

Table 8. FLEX 8000 Device Configuration Option Bits (Part 1 of 2)

Device Option	Configuration Scheme	Option Usage	Default Configuration (Option Off)	Modified Configuration (Option On)
User-Supplied Start-Up Clock	All	After a FLEX 8000 device is configured, it must be initialized over the course of 10 Clock cycles. The user can choose the source of the Clock.	In the AS, APU, APD, and PPA configuration schemes, the internal FLEX 8000 device oscillator supplies the initialization Clock. In the PS and PPS configuration schemes, the internal oscillator is disabled, so external circuitry must provide the initialization Clock on the DCLK pin.	The user provides the Clock on the CLKUSR pin. This type of Clock can be used to fully synchronize initialization for multiple FLEX 8000 devices. The maximum user-supplied Clock frequency is 6 MHz, and the Clock should have a 50% duty cycle.
Auto-Restart Configuration on Frame Error	AS, APU, APD AS	If a data error occurs when a FLEX 8000 device is configured with an active configuration scheme, the user can choose how to restart the configuration.	The configuration process halts and the user must externally direct the device to restart the configuration process. If a configuration error occurs, the nSTATUS pin is driven and held low until the nCONFIG pin is externally pulled low and then high again. In an AS configuration scheme, the external nCONFIG reset pulse resets the Configuration EPROM if the nCONFIG pin on the FLEX 8000 device is tied to the Output Enable pin on the Configuration EPROM.	Directs the device to automatically restart the configuration process. The nSTATUS pin is driven and held low for 10 Clock cycles and is then released. The nSTATUS pin subsequently pulls up to V_{CC}, indicating to any external circuitry that the reconfiguration process has started. In an AS configuration scheme, the nSTATUS reset pulse automatically resets the Configuration EPROM if the nSTATUS pin on the FLEX 8000 device is tied to the Output Enable pin on the Configuration EPROM.
Release Clears Before Tri-States	All	During configuration, the I/O pins on the device are tri-stated by an Output Enable override. The user can choose the order in which the tri-states are released and the registered logic cells and peripheral registers are cleared during initialization.	Directs the device to release the Output Enable override on the tri-state buffer before releasing the Clear signal on registered logic cells and peripheral registers during initialization.	Directs the device to release the Clear signal on registered logic cells and peripheral registers before releasing the Output Enable override on the tri-state buffer during initialization.
Enable DCLK Output In User Mode	AS, APU, APD, PPA	FLEX 8000 devices drive the DCLK signal during configuration in all active configuration schemes and the PPA configuration scheme. The DCLK signal can range from 2 to 6 MHz in frequency. The user can choose whether to enable the DCLK signal during user mode. The duty cycle and frequency of the DCLK signal are not guaranteed.	Disables the DCLK pin when the device operates in user mode after device configuration and initialization have been completed.	Enables the DCLK pin when the device operates in user mode after device configuration and initialization have been completed.

Table 8. FLEX 8000 Device Configuration Option Bits (Part 2 of 2)

Device Option	Configuration Scheme	Option Usage	Default Configuration (Option Off)	Modified Configuration (Option On)
Disable Start-Up Time-Out	All	The CONF_DONE pin, a bidirectional open-drain pin, is held at GND by the FLEX 8000 device during configuration. Once configuration is complete, the CONF_DONE pin is released and the FLEX 8000 device treats the pin as an input pin. In most applications, the CONF_DONE pin is pulled up to V_{CC} via a 1.0-kΩ resistor. This low-to-high transition directs the FLEX 8000 device to begin initialization. The user can enable or disable the time-out error checking that determines whether CONF_DONE goes high within 10 Clock cycles.	If the CONF_DONE pin does not go high within 10 Clock cycles after being released by the device, the device drives the nSTATUS pin low at the end of the configuration cycle, indicating an error condition.	If the CONF_DONE pin does not go high within 10 Clock cycles after being released by the device, the device continues to wait for CONF_DONE to go high. To delay initialization, the CONF_DONE node can be held low externally after the FLEX 8000 device has released the CONF_DONE pin, if, for example, the user wishes to control the time required for the FLEX 8000 device to enter user mode.

Device Configuration Pins

FLEX 8000 devices include control pins that modify the sequence and timing of the configuration and initialization processes, and provide a variety of configuration options. Some configuration pins have the same effect regardless of the selected configuration scheme; others are specific to a particular configuration scheme. Table 9 summarizes the functionality of each configuration pin.

Table 9. Pin Functions (Part 1 of 2) *Note (1)*

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nSP	n/a	All	Input	Serial/Parallel selection input. A low input selects a serial configuration scheme; a high input selects a parallel configuration scheme.
MSEL1 MSEL0	n/a	All	Input	2-bit configuration scheme selection inputs that are used in conjunction with nSP to select the configuration scheme. The bit patterns of nSP:MSEL1:MSEL0 are associated with the following configuration schemes: 000 = AS 100 = APU 001 = Reserved 101 = PPS 010 = PS 110 = APD 011 = Reserved 111 = PPA
nSTATUS	n/a	All	Bidirectional Open Drain	Command mode status output. The FLEX 8000 device drives the nSTATUS pin low immediately after power-up, then releases it within 100 ms. The nSTATUS pin must be pulled up to V_{CC} with a 1.0-kΩ resistor. If an error occurs during configuration, nSTATUS is pulled low again by the FLEX 8000 device.

Table 9. Pin Functions (Part 2 of 2)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCONFIG	n/a	All	Input	Configuration control input. A low input resets the FLEX 8000 device. A low-to-high transition starts a configuration cycle.
nWS	I/O	PPA	Input	Write Strobe input. A low-to-high transition causes the FLEX 8000 device to latch a byte of data on the DATA[7..0] pins.
nRS	I/O	PPA	Input	Read Strobe input. A low input directs the FLEX 8000 device to place the RDYnBUSY signal on the DATA7 pin.
RDCLK	I/O	APD, APU	Output	Divide-by-8 of DCLK output. Used internally to serialize an 8-bit data stream in the byte-wide APU or APD configuration scheme.
DCLK	*(2)* *(3)*	AS PPS, PS	Output Input	Clock source for external PROM devices. Clock input from external host.
nCS CS	I/O	PPA	Input	Chip Select inputs. A low input on nCS and a high input on CS selects a specific FLEX 8000 device for configuration. If only one of the chip selects is used, the other must be tied to its active level (e.g., nCS would be tied to GND).
RDYnBUSY	I/O	PPA	Output	Ready output. A high output indicates that the FLEX 8000 device is ready to accept another byte of data. A low output indicates that the device is not ready to receive data.
CLKUSR	I/O	All	Input	Optional user-supplied Clock input. Synchronizes the initialization process.
CONF_DONE	n/a	All	Bidirectional Open Drain Input	Status output. Driven low by the FLEX 8000 device during the configuration process. Status input. A high input directs the device to execute the initialization process and enter user mode. The CONF_DONE net must be pulled up to V_{CC} with a 1.0-kΩ resistor. The CONF_DONE pin may be actively driven low by an external source to delay the FLEX 8000 device initialization process. This feature is useful when the configuration process will be completed some time before actual operation is necessary.
ADD17 to ADD0	I/O	APD, APU	Outputs	Address outputs. Driven by the FLEX 8000 device to uniquely address up to 256 Kbytes of external configuration memory devices.
DATA7 to DATA0	I/O	APD, APU, PPA, PPS	Inputs	Data inputs. Byte-wide configuration data is presented to the FLEX 8000 device on all 8 data pins.
DATA0		AS, PS	Input	Data input. Bit-wide configuration data is presented to the FLEX 8000 device on the DATA0 pin.
DATA7		PPA	Output	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the device receives an nRS strobe. Using the DATA7 pin may be more convenient than using the RDYnBSY output pin.

Notes:

(1) The maximum number of dual-purpose configuration pins that can be used as I/O pins in user mode varies in different configuration schemes:
AS: 3 pins APU: 29 pins APD: 29 pins
PS: 2 pins PPS: 9 pins PPA: 15 pins

(2) The internally-generated DCLK signal used to configure FLEX 8000 devices with the AS, APU, APD, and PPA configuration schemes is available during user-mode operation if the *Enable DCLK Output in User Mode* configuration option bit is turned on. The DCLK signal can range from 2 to 6 MHz in frequency; the duty cycle and frequency are not guaranteed.

(3) An externally-generated DCLK signal is used to configure FLEX 8000 devices with the PS and PPS configuration schemes. After configuration has finished, the external host can continue to drive the DCLK signal during user-mode operation.

Seven of the device pins are dedicated to the configuration process and cannot be used as I/O pins in user mode. Other configuration pins are dual-purpose pins that also can be used as I/O pins when the device operates in user mode. You can choose whether to use each dual-purpose pin as an I/O pin in user mode, and whether to force a dual-purpose pin to tri-state (i.e., drive a high-impedance logic level).

You can specify these settings for each pin on a device-by-device basis during design entry in the MAX+PLUS II Graphic, Text, or Waveform Editor with the **FLEX 8000 Individual Device Options** dialog box that is accessible via the **Chip to Device** dialog box on the Assign menu. (In MAX+PLUS II for workstations, the **Chip to Device** dialog box is available on the Compiler's Device menu.) You can also enter default pin settings for an entire project in the MAX+PLUS II Compiler with the **FLEX 8000 Device Options** dialog box that is accessible via the **Device Options** dialog box (Device menu). Turning on the *Reserve* option for a specified pin in either dialog box prevents the pin from being used as an I/O pin during user mode; turning on the *Tri-State* option forces the pin to tri-state. A reserved pin should not be connected to any circuitry on the target board unless it is also tri-stated. Otherwise, the reserved pin will drive an unknown logic level that may cause logic contention with other signals on the board.

The nSTATUS, nCONFIG, CONF_DONE, and CLKUSR device configuration pins are available to monitor the configuration process and control how the device loads data, initializes, and enters user-mode operation. These pins can be used together with configuration option bits to provide additional configuration and initialization control.

nSTATUS Pin

The nSTATUS pin is an open-drain bidirectional pin. When the FLEX 8000 device powers up, it pulls this pin low and then releases it within 100 ms. During configuration, the nSTATUS pin can be polled externally to verify that the FLEX 8000 device is being configured. If an error occurs during configuration, the nSTATUS pin is pulled and held low. After the pin is pulled low, configuration must be restarted.

Configuration is restarted with a high-low-high pulse on the nCONFIG pin. As an alternative, if the *Auto-Restart Configuration on Frame Error* option bit is turned on, the FLEX 8000 device can restart the configuration automatically when an error is detected. If this option bit is turned on, the nSTATUS pin is pulled low for a few microseconds and then released, indicating that the reconfiguration cycle has started. See Figure 3 earlier in this application note for an example of an AS configuration scheme that supports auto-reconfiguration.

If V_{CC} falls below an acceptable level during user-mode operation, the nSTATUS pin is pulled and held low, indicating an error condition. See "Configuration Reliability" later in this application note for more details.

nCONFIG Pin

The nCONFIG pin is a dedicated input that is used to start a configuration cycle. In most applications, the nCONFIG pin is tied to V_{CC}, directing the FLEX 8000 device to immediately start configuration in an active configuration scheme, or to prepare immediately for configuration in a passive configuration scheme.

When the nCONFIG pin is held at GND, the FLEX 8000 device is reset and ready to start configuration. Configuration begins only after the pin is pulled up to V_{CC}. The nCONFIG pin can thus be held low to delay the configuration process, and prevent data from loading until the desired time.

If an application requires a FLEX 8000 device to be reconfigured after system power-up, the nCONFIG pin must be tied to some external intelligent circuitry that monitors and controls that configuration process, as described in "In-Circuit Reconfiguration" earlier in this application note.

CONF_DONE Pin

The CONF_DONE pin is an open-drain bidirectional pin that reflects the configuration status. When a FLEX 8000 device is ready to begin loading data, the CONF_DONE pin is pulled to GND and remains at GND while the data is loading, indicating that the FLEX 8000 device is being configured. After the last configuration data byte has been read, the CONF_DONE pin is released and pulled to V_{CC} by an external pull-up resistor, indicating that configuration is finished. The FLEX 8000 device interprets this low-to-high transition on the CONF_DONE signal as the command to initialize and enter the user mode.

If the CONF_DONE pin does not pull up to V_{CC} within ten Clock cycles of the final configuration data byte, the FLEX 8000 device detects an error condition, aborts the initialization process, and drives and holds the nSTATUS pin low. If the nSTATUS pin is low, it indicates either that an error has occurred in the application circuit, or that the configuration data-stream is corrupt.

The CONF_DONE pin can also be used to control the initialization process. You can disable error checking on the CONF_DONE net by turning on the device's *Disable Start-Up Time-Out* configuration option bit, so that the failure of CONF_DONE to pull to V_{CC} does not cause an error condition. The CONF_DONE network can then be driven by some external logic, and held low until initialization is desired.

CLKUSR Pin

The CLKUSR pin can coordinate the initialization of multiple FLEX 8000 devices or synchronize the configuration of a FLEX 8000 device with other application logic in the system. In most applications, the FLEX 8000 device uses its internal oscillator (available externally as DCLK) to complete the initialization. After ten Clock cycles, the device enters user mode. You can turn on the *User-Supplied Start-Up Clock* configuration option bit and supply these ten Clock cycles on the CLKUSR pin to ensure that the device enters the user mode precisely when desired. Since the internal oscillators on all FLEX 8000 devices are not guaranteed to have the same frequency, you can use the CLKUSR pin to synchronize multiple FLEX 8000 devices in the same system.

MAX+PLUS II Configuration & Programming Support

The MAX+PLUS II software can generate four different types of configuration files for FLEX 8000 devices, as shown in Table 10. During project compilation, MAX+PLUS II automatically generates a POF and an SOF for each FLEX 8000 device. If necessary, you can generate a TTF or Hex File, as well as different POF(s), after compilation with the **Combine Programming Files** command (File menu) in the MAX+PLUS II Programmer or Compiler.

Table 10. FLEX 8000 Device Programming Files

File Type	Filename Extension	File Format	File Utilization
SRAM Object File	**.sof**	Binary	Downloaded directly into the FLEX 8000 device with the MAX+PLUS II Programmer using the FLEX 8000 Download Cable and Altera programming hardware.
Programmer Object File	**.pof**	Binary	Programmed into an Altera Configuration EPROM. The POF contains the configuration data, as well as the header, CRC, and pad bytes for configuring the FLEX 8000 device in an AS configuration scheme.
Hexadecimal (Intel-Format) File	**.hex**	ASCII text	Programmed into an industry-standard parallel EPROM. The Hex File contains the configuration data, as well as the header, CRC, and pad bytes for programming a parallel EPROM that configures a FLEX 8000 device in an APU or APD configuration scheme.
Tabular Text File	**.ttf**	ASCII text	A comma-separated version of the Hex File, used as source code in high-level programming languages. The TTF can be included in the source code for an intelligent host that configures the FLEX 8000 device in a PPA, PPS, or bit-wide PS configuration scheme. It can also be converted into an equivalent binary format that is directly loaded (LSB first) into the FLEX 8000 device.

Together, the MAX+PLUS II Programmer and Altera programming hardware provide the following capabilities:

- A POF can be programmed into an Altera serial Configuration EPROM for an AS configuration scheme.
- An SOF can be downloaded via the FLEX Download Cable for in-circuit PS configuration of a FLEX 8000 device.

Programming & Configuration Files

This section provides information on the characteristics of each type of configuration file. The process of creating different configuration files is described in "Combining & Converting Programming Files" later in this application note.

SRAM Object File

The SRAM Object File (**.sof**) is used during passive serial configuration when the data is downloaded directly into the FLEX 8000 device in-system with the MAX+PLUS II Programmer, the FLEX Download Cable, and Altera programming hardware. MAX+PLUS II automatically inserts the necessary header, formatting, and synchronization bits into the data stream when it downloads an SOF into a FLEX 8000 device. See "Configuring a FLEX 8000 Device In-System with MAX+PLUS II & the FLEX Download Cable" later in this application note for more information.

If configuration files are needed for other configuration schemes, MAX+PLUS II uses the data in SOF(s) to generate the appropriate POF(s), a TTF, or a Hex File.

Programmer Object File

The Programmer Object File (**.pof**) is used to program Altera serial Configuration EPROMs for an AS configuration scheme. MAX+PLUS II automatically generates a POF for every FLEX 8000 device in a project. In a multi-device project, each FLEX 8000 device has a dedicated serial Configuration EPROM. MAX+PLUS II selects the appropriate Configuration EPROM to most efficiently store the data for each FLEX 8000 device.

Hexadecimal (Intel-Format) File

The Hexadecimal File (**.hex**) is an ASCII file in the Intel Hex format. This file contains the configuration and formatting data for an industry-standard byte-wide parallel EPROM that is used to configure a FLEX 8000 device in an APU or APD configuration scheme. The data in the Hex File is interpreted

by the programming software when it is programmed into a parallel EPROM.

The usual base address for FLEX 8000 configuration data is the origin of the EPROM. In some applications, the origin of the EPROM is required by other system resources, so some offset is necessary. In an APU configuration scheme, the FLEX 8000 device generates ascending addresses starting at 00000H; in an APD configuration scheme, it generates descending addresses starting at 3FFFFH. The FLEX 8000 device provides these base addresses for the configuration data during configuration, but any needed offset address must be generated externally, as shown earlier in Figure 6. The APU scheme is appropriate if the FLEX 8000 configuration data can be stored at the beginning of an EPROM or at some known offset in an EPROM larger than 256 Kbytes. The APD scheme is appropriate if the FLEX 8000 configuration data is placed in an EPROM in which the low addresses are not available (as shown in Figure 7), or in an EPROM that also stores other information that is expected to increase as an application evolves.

Tabular Text File

The Tabular Text File (**.ttf**) is a tabular ASCII file that provides a comma-separated version of the configuration data for the PPA, PPS, and bit-wide PS configuration schemes. In some applications, the storage device that contains the FLEX 8000 configuration data is neither dedicated to nor connected directly to the FLEX 8000 device. For example, an EPROM can also contain executable code for a system (e.g., BIOS routines) and other data. The TTF allows you to include the FLEX 8000 configuration data as part of the source code for the intelligent host (using "include" or "source" commands). The host can access this data from an EPROM or a mass-storage device and load it into the FLEX 8000 device.

A TTF can be imported into nearly any Assembly Language or high-level language compiler. Consult the documentation for your compiler or assembler for information on including other source files.

If you do not include the TTF in the source code for an intelligent host, the file's comma-separated ASCII representation of the binary data must be converted into its equivalent 8-bit binary format (e.g., 85 would become 01010101) before it is loaded into the FLEX 8000 device. Data must be stored so that the least significant bit (LSB) of each byte of data is loaded first. You can convert the ASCII decimal values into a binary image and store it on a mass storage device. The intelligent host can then read data from the binary file and load it into the FLEX 8000 device. You can also use the intelligent host to perform real-time conversion during configuration. In the PPA and PPS configuration schemes, the FLEX 8000 device receives its information in parallel from the data bus, a data port on the CPU, or

some other byte-wide channel. In the bit-wide PS configuration scheme, the data is shifted in serially.

Programming a Serial Configuration EPROM

You can program Altera Configuration EPROMs with MAX+PLUS II, the PL-MPU Master Programming Unit, and the appropriate Configuration EPROM programming adapter. The PLMJ1213 adapter programs Configuration EPROMs in 8-pin plastic dual in-line package (PDIP) and 20-pin plastic J-lead chip carrier (PLCC) packages; the PLMT1064 adapter programs Configuration EPROMs in 32-pin thin quad flat pack (TQFP) adapters.

To program an Altera serial Configuration EPROM:

1. Choose the **Programmer** command (MAX+PLUS II menu) to open the Programmer window.
2. By default, the Programmer loads the POF for the current project. If necessary, load a different POF with the **Select Programming File** command (File menu). The appropriate device for the current programming file is displayed in the Device field.
3. Insert a blank Configuration EPROM into the 8-pin DIP, 20-pin J-lead, or 32-pin QFP socket on the programming adapter. The socket for the FLEX 8000 device (if any) must be empty.
4. Choose the **Program** button.

After successful programming, you can place the Configuration EPROM on the target board to configure a FLEX 8000 device in the AS configuration scheme.

Configuring a FLEX 8000 Device In-System with MAX+PLUS II & the FLEX Download Cable

To configure a FLEX 8000 device with the FLEX Download Cable:

1. Connect the FLEX Download Cable to the 9-pin D-type connector on a Configuration EPROM programming adapter.
2. Connect the other end of the FLEX Download Cable to the 10-pin male header on the target board.
3. Start MAX+PLUS II and choose the **Programmer** command (MAX+PLUS II menu) to open the Programmer window.
4. Choose the **Select Programming File** command (File menu).
5. Select the desired SOF filename in the *Files* box or type a name in the *File Name* box. If you choose a programming file from another project, you are asked if you wish to change the current project name.
6. Choose **OK**.
7. Choose the **Program** button to configure the device.

After the device is configured and initialized, it enters user mode and operates as a logic device. The FLEX Download Cable is electrically removed from the circuit and does not influence circuit operation. You can also physically disconnect the FLEX Download Cable without disturbing the FLEX 8000 configuration data or device operation.

Combining & Converting Programming Files

MAX+PLUS II automatically generates a POF and an SOF for every FLEX 8000 device in a project, as described earlier in this application note. The POF can be programmed into an Altera serial Configuration EPROM used in an AS configuration scheme; by default, each FLEX 8000 device has one dedicated Configuration EPROM.

You may wish to combine and/or convert the automatically generated SOFs into a different format for the following purposes:

- To use a configuration scheme other than AS. You must convert an SOF into a Hex File or a TTF for programming a parallel EPROM, BIOS EPROM, or another data source.
- To combine multiple sets of configuration data to be used for in-circuit reconfiguration in any configuration scheme.

To convert an SOF into a Hex File or TTF:

1. Refer to Table 2 to calculate the required data space in a parallel or serial data source.
2. Choose the **Combine Programming Files** command (File menu) in the MAX+PLUS II Programmer or Compiler.
3. Select the desired SOF name in the *Files* box or type a name in the *File Name* box under *Input Files*. Choose the **Add** button to add it to the *Selected Files* box.
4. Specify information for the desired configuration scheme:

   - If the FLEX 8000 device will be configured with a parallel EPROM in the APU or APD configuration scheme, select *.hex (Active Parallel)* in the *File Format* drop-down list box under *Output File*.

     In addition, if the FLEX 8000 configuration data will not start at the origin of the EPROM, specify the base address for the configuration data in the *Address* box under *Input Files*. Choose *Up* or *Down* under *Count* to specify whether the FLEX 8000 device should count up or down. The counting sequence can be either ascending (00000H to 3FFFFH) for APU configuration or descending (3FFFFH to 00000H) for APD configuration, as described in "Hexadecimal (Intel-Format) File" earlier in this application note.

or:

- If the FLEX 8000 device will be configured with a PPA, PPS, or bit-wide PS scheme, select *.ttf (Passive Parallel)* in the *File Format* drop-down list box under *Output File*. The TTF can be incorporated as source code for a data structure in a high-level programming language. Otherwise, the TTF data must be converted into its equivalent 8-bit binary format before it is loaded into the FLEX 8000 device, as described in "Tabular Text File" earlier in this application note.

5. The default name for the output file is the current project name plus the extension **.hex** or **.ttf**. To give a different name to the file, type a name in the *File Name* box under *Output File*.
6. Choose **OK** to generate the Hex File or TTF. The file is placed in the current project directory.

You can use in-circuit reconfiguration to load multiple sets of configuration data into the FLEX 8000 device in a system. The following procedure describes how to combine SOFs for in-circuit reconfiguration of a FLEX 8000 device.

To combine SOFs for in-circuit reconfiguration with multiple sets of configuration data:

1. Refer to Table 2 to calculate the required data space in a parallel or serial data source.
2. Choose the **Combine Programming Files** command (File menu) in the MAX+PLUS II Programmer or Compiler.
3. Select the SOF with the first set of configuration data and choose the **Add** button to add it to the *Selected Files* box.
4. Repeat step 3 until all SOFs have been added to the *Selected Files* box.
5. Arrange the selected files in the order in which the different sets of configuration data will be used by selecting each SOF filename and choosing the **Up** or **Down** button under *Order*.
6. Specify information for the desired configuration scheme, select the output filename, and choose **OK**. (The default name for the output file is the current project name plus the extension **.hex**, **.ttf**, or **.pof**. To give a different name to the file, type a name in thge *File Name* box under *Output File*. If multiple POFs are generated, they are uniquely identified by a sequence number appended to the filename (e.g., the first is **device.pof**, the second is **device1.pof**, etc. You can specify an output filename that has less than the maximum of eight characters to leave room for the numerical index; otherwise, the last character(s) are truncated to include it.)

Configuration Reliability

The FLEX architecture has been designed to minimize the effects of power supply and data noise in a system, and to ensure that the configuration data is not corrupted during configuration or normal user-mode operation. A number of circuit design features are provided to ensure the highest possible level of reliability from this SRAM technology.

Cyclic redundancy check (CRC) circuitry is used to validate every data frame (i.e., sequence of data bits) as it is loaded into the FLEX 8000 device. If the CRC generated by the FLEX 8000 device does not match the data stored in the data stream, the configuration process is halted, and the nSTATUS pin is pulled and held low to indicate an error condition. This CRC circuitry ensures that noisy systems will not cause errors that yield an incorrect or incomplete configuration.

The FLEX architecture also provides a very high level of reliability in low-voltage brown-out conditions. The SRAM cells require a certain V_{CC} level to maintain accurate data. Since this voltage threshold is significantly lower than that required to activate the power-on reset (POR) circuitry in the FLEX 8000 device, the FLEX 8000 device stops operating if the V_{CC} starts to fail, and indicates an operation error by pulling and holding the nSTATUS pin low. The device must then be reconfigured before it can resume operation as a logic device. In active configuration schemes, reconfiguration begins as soon as V_{CC} returns to an acceptable level if the nCONFIG pin is tied to V_{CC}. Otherwise, the host system must start the reconfiguration process.

These device features ensure that FLEX 8000 devices have the highest possible reliability in a wide variety of environments, and provide the same high level of system reliability that exists in other families of Altera programmable logic devices.

Notes:

Understanding EPLD Timing

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Introduction

Altera EPLDs provide device performance that is consistent from simulation to application. Before programming a device, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer or with the timing models given in this application brief and the timing parameters listed in individual device data sheets. Both methods yield the same results.

This application brief defines device internal delay parameters and AC timing characteristics, and illustrates the timing models for the Classic, MAX 5000/EPS464, and MAX 7000 device families. For information on FLEX 8000 timing, refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book.

Familiarity with EPLD architecture and characteristics is assumed. Refer to individual device data sheets in this data book for complete descriptions of the architectures.

Internal EPLD Delay Parameters

Within an EPLD, timing delays contributed by individual architectural elements are called microparameters. The following list defines microparameters for Classic, MAX 5000/EPS464, and MAX 7000 EPLDs. Individual device data sheets for MAX 5000/EPS464 and MAX 7000 EPLDs give the values for these parameters; microparameters for Classic EPLDs are listed in this application brief.

t_{IN} Input pad and buffer delay. In Classic and MAX 5000/EPS464 EPLDs, it is the time required for a dedicated input pin to drive the true and complement data input signal into the logic array(s). In MAX 7000 devices, it is the time required for a dedicated input pin to drive the input signal into the Programmable Interconnect Array (PIA) or into the global control array.

t_{IO} I/O input pad and buffer delay. This delay applies to I/O pins used as inputs. In Classic EPLDs, it is the delay added to t_{IN}. In MAX 5000/EPS464 EPLDs with a single Logic Array Block (LAB), it is the delay from the I/O pin to the logic arrays. In MAX 7000 and multi-LAB MAX 5000 EPLDs, it is the delay from the I/O pin to the PIA.

t_{PIA} Programmable Interconnect Array delay. The delay incurred by signals that require routing through the PIA. MAX 7000 and multi-LAB MAX 5000 EPLDs only.

t_{EXP} Expander array delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the logic array. MAX 5000/EPS464 EPLDs only.

t_{SEXP} Shared expander array delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the logic array. MAX 7000 EPLDs only.

t_{PEXP} Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. For each group of up to five parallel expanders added to a single function, an additional t_{PEXP} delay is added to the timing path. MAX 7000 EPLDs only.

t_{ICS} Global Clock delay. The delay from the dedicated Clock pin to a register's Clock input. Classic and MAX 5000 EPLDs only.

t_{GLOB} Global control delay. The delay from a dedicated input pin to any global control function in a macrocell or I/O control block. EPS464 and MAX 7000 EPLDs only.

t_{LAC} Logic array control delay. The AND array delay for register control functions such as Preset, Clear, and Output Enable. MAX 5000/EPS464 and MAX 7000 EPLDs only.

t_{IC} Array Clock delay. The delay through a macrocell's Clock product term to the register's Clock input.

t_{EN} Register Enable delay. The register AND array delay from the PIA to the register Enable input. MAX 7000 EPLDs only.

t_{CLR} Register Clear time. The delay from the time when the register's asynchronous Clear input is asserted to the time the register output stabilizes at logical low.

t_{PRE} Register Preset time. The delay from the time when the register's asynchronous Preset input is asserted to the time the register output stabilizes at logical high.

t_{LAD} Logic array delay. The time a logic signal requires to propagate through a macrocell's AND-OR-XOR structure.

t_{RD} Register delay. The delay from the rising edge of the register's Clock to the time the data appears at the register output. MAX 5000/EPS464 and MAX 7000 EPLDs only.

t_{SU} Register setup time. The time required for a signal to be stable at the register input before the Clock's rising edge to ensure that the register correctly stores the input data.

t_H Register hold time. The time required for a signal to be stable at the register input after the register Clock's rising edge to ensure that the register correctly stores the input data.

t_{COMB} Combinatorial buffer delay. The delay from the time when a combinatorial logic signal bypasses the programmable register to the time it becomes available at the macrocell output. MAX 5000/EPS464 and MAX 7000 EPLDs only.

t_{LATCH} Latch delay. The propagation delay through the programmable register when it is configured as a flow-through latch. MAX 5000 EPLDs only.

t_{FD} Feedback delay. In Classic EPLDs, it is the delay of a macrocell output fed back into the logic array. In single-LAB MAX 5000/EPS464 EPLDs, it is the delay of a macrocell output fed back into the logic array. In multi-LAB MAX 5000 EPLDs, it is the delay of a macrocell output fed back into the LAB's logic array or to a PIA input.

t_{OD} Output buffer and pad delay. The delay from the macrocell output, through the tri-state output buffer, to the output pin.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's Enable control is disabled.

t_{ZX} Output buffer enable delay. The delay required for the macrocell output to appear at the output pin after the output buffer's Enable control is enabled.

t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA} must be added to the logic array delay (t_{LAD}), register control delay (t_{LAC}, t_{IC}, t_{ACL}, or t_{EN}), and the shared expander delay (t_{SEXP}) paths. MAX 7000 EPLDs only.

AC Timing Characteristics

AC timing characteristics, called macroparameters, represent actual pin-to-pin timing characteristics. Each macroparameter consists of a combination of internal delay elements (microparameters). The data sheet for each EPLD gives timing macroparameters that characterize the AC operating specifications. These are worst-case values, derived from extensive performance measurements and guaranteed by testing. The following list defines macroparameters for Classic, MAX 5000/EPS464, and MAX 7000 EPLDs.

t_{PD1} Dedicated input pin to non-registered output delay. The time required for a signal on any dedicated input pin to propagate through the combinatorial logic in a macrocell and appear at an external EPLD output pin.

t_{PD2} I/O pin input to non-registered output delay. The time required for a signal on any I/O pin input to propagate through the combinatorial logic in a macrocell and appear at an external EPLD output pin.

t_{PZX} Tri-state to active output delay. The time required for an input transition to change an external output from a tri-state (high-impedance) logic level to a valid high or low logic level.

t_{PXZ} Active output to tri-state delay. The time required for an input transition to change an external output from a valid high or low logic level to a tri-state (high-impedance) logic level.

t_{CLR} Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.

t_{SU} Global Clock setup time. The time data must be present at the input pin before the global (synchronous) Clock signal is asserted at the Clock pin.

t_{H} Global Clock hold time. The time the data must be present at the input pin after the global Clock signal is asserted at the Clock pin.

t_{CO1} Global Clock to output delay. The time required to obtain a valid output after the global Clock is asserted at the Clock pin.

t_{CNT} Minimum global Clock period. The minimum period maintained by a globally clocked counter.

t_{ASU} Array Clock setup time. The time data must be present at the input pin before an array (asynchronous) Clock signal is asserted at an input pin.

t_{AH} Array Clock hold time. The time data must be present at the input pin after an array Clock signal is asserted at an input pin.

t_{ACO1} Array Clock to output delay. The time required to obtain a valid output after an array Clock signal is asserted at an input pin.

t_{ACNT} Minimum array Clock period. The minimum period maintained by a counter when it is clocked by a signal from the array.

EPLD Timing Models

Timing models are simplified block diagrams that illustrate propagation delays through Altera EPLDs. Logic can be implemented in different paths. You can trace the actual paths used in your Altera device design by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for

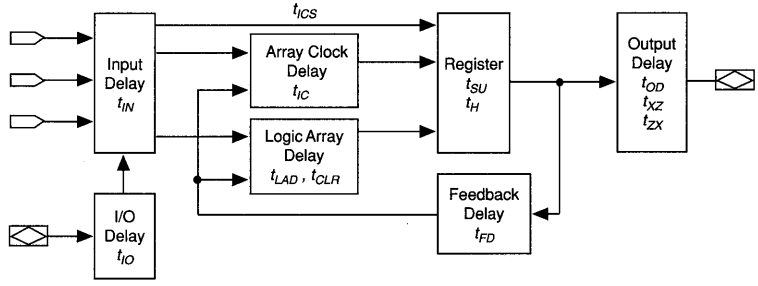
the project. You then add up the appropriate microparameters to calculate the propagation delays through the EPLD.

Classic EPLDs

The Classic architecture provides registered and combinatorial capabilities. Registers can be clocked from a global Clock or through an array (product-term) Clock, and can be asynchronously cleared. When the global Clock is used, the Output Enable can be controlled by a product term. Figure 1 shows the timing model for Classic devices.

Figure 1. Classic EPLD Timing Model

If the register is bypassed, the delay between the logic array and the output buffer is zero.



Tables 1 through 6 show the internal delay parameters for all Classic EPLDs.

Table 1. EP330 Timing Parameters (in ns)

Parameter	EP330-12	EP330-15
t_{IN}	2	3
t_{IO}	1	1
t_{LAD}	7	8
t_{OD}	3	4
t_{ZX}	3	4
t_{XZ}	3	4
t_{SU}	2	3
t_H	4	5
t_{IC}	n/a	n/a
t_{ICS}	3	3
t_{FD}	1	1
t_{CLR}	n/a	n/a

Table 2. EP610 Timing Parameters (in ns)

Parameter	EP610-15	EP610-20	EP610-25	EP610-30	EP610-35
t_{IN}	4	4	8	9	11
t_{IO}	2	2	2	2	2
t_{LAD}	6	11	11	14	15
t_{OD}	5	5	6	7	9
t_{ZX}	5	5	6	7	9
t_{XZ}	5	5	6	7	9
t_{SU}	5	4	11	11	12
t_{H}	4	7	10	10	10
t_{IC}	6	11	13	16	17
t_{ICS}	2	4	1	1	0
t_{FD}	1	1	3	5	8
t_{CLR}	6	11	13	16	17

Table 3. EP610A Timing Parameters (in ns)

Parameter	EP610A-7	EP610A-10	EP610A-12	EP610A-15
t_{IN}	3	2	1	2
t_{IO}	0	0	0	0
t_{LAD}	3.5	6	8	10
t_{OD}	1	2	3	3
t_{ZX}	1	2	3	4
t_{XZ}	1	2	3	4
t_{SU}	3.5	3	3	3
t_{H}	2.5	3	4	6
t_{IC}	4	6	8	9
t_{ICS}	1	2	3	3
t_{FD}	1	1	1	1
t_{CLR}	3.5	6	8	11

Table 4. EP910 Timing Parameters (in ns)

Parameter	EP910-30	EP910-35	EP910-40
t_{IN}	9	10	13
t_{IO}	3	3	3
t_{LAD}	14	16	17
t_{OD}	7	9	10
t_{ZX}	7	9	10
t_{XZ}	7	9	10
t_{SU}	12	13	15
t_{H}	12	12	12
t_{IC}	17	19	20
t_{ICS}	2	2	1
t_{FD}	4	6	8
t_{CLR}	17	19	20

Table 5. EP910A Timing Parameters (in ns)

Parameter	EP910A-10	EP910A-12	EP910A-15
t_{IN}	2	1	2
t_{IO}	0	0	0
t_{LAD}	6	8	10
t_{OD}	2	3	3
t_{ZX}	3	4	4
t_{XZ}	3	4	4
t_{SU}	3	3	3
t_{H}	3	4	6
t_{IC}	6	8	9
t_{ICS}	2	3	3
t_{FD}	1	1	1
t_{CLR}	7	9	11

Table 6. EP1810 Timing Parameters (in ns)

Parameter	EP1810-20	EP1810-25	EP1810-35	EP1810-45
t_{IN}	5	7	7	6
t_{IO}	2	3	5	5
t_{LAD}	9	12	19	28
t_{OD}	6	6	9	11
t_{ZX}	6	6	9	11
t_{XZ}	6	6	9	11
t_{SU}	8	10	10	10
t_{H}	5	7	15	18
t_{IC}	9	12	19	28
t_{ICS}	4	5	4	8
t_{FD}	3	3	6	7
t_{CLR}	9	12	24	32

MAX 5000/EPS464 EPLDs

The MAX 5000 architecture supports many functions. The macrocell array provides registered, combinatorial, or flow-through latch operation. The registers can be clocked from a global Clock or through product-term array Clocks, and can be asynchronously preset and cleared. Separate product terms control the Output Enable and logic inversion. The array of shared expander product terms provides additional product terms to implement complex logic.

The EPS464 is an advanced general-purpose EPLD based on the MAX 5000 architecture. It has 64 enhanced macrocells and 256 shared expanders, all of which are routed globally to implement complex projects.

MAX 5000 EPLDs are divided into two categories: single- and multi-LAB EPLDs. Figure 2 shows the timing model for the single-LAB EPM5016 and EPM5032 EPLDs.

Figure 2. Single-LAB MAX 5000 EPLD Timing Model

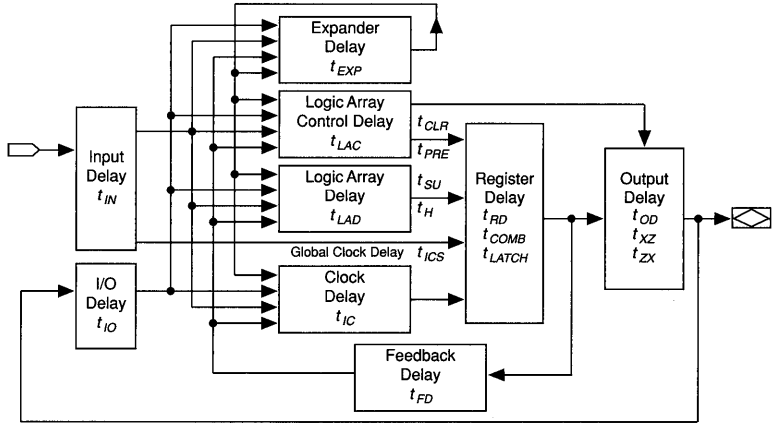
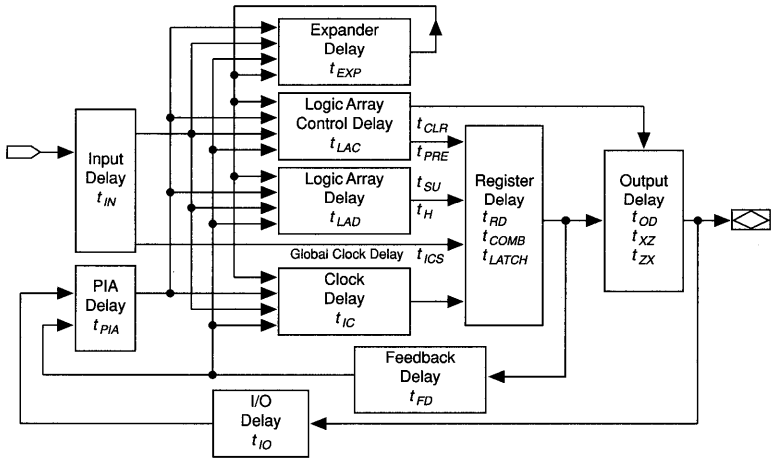


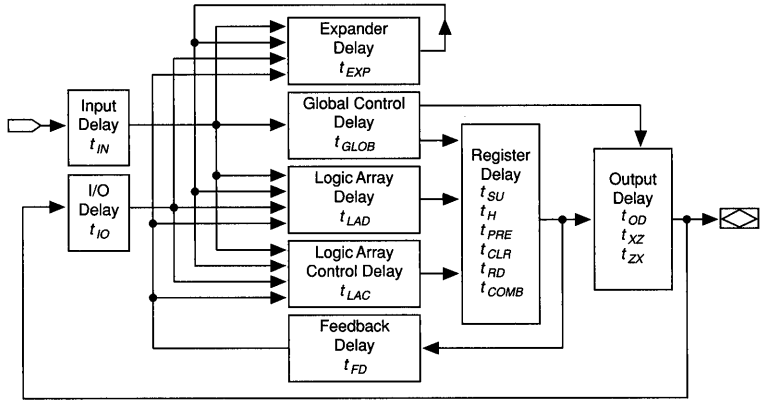
Figure 3 shows the timing model for the multi-LAB MAX 5000 EPLDs: the EPM5064, EPM5128, EPM5128A, EPM5130, EPM5192, and EPM5192A EPLDs. In multi-LAB devices, the Programmable Interconnect Array (PIA) routes signals between different LABs. All I/O inputs come into the logic array through the PIA. Signals routed through the PIA incur an additional delay.

Figure 3. Multi-LAB MAX 5000 EPLD Timing Model



The timing model for the EPS464 EPLD is shown in Figure 4.

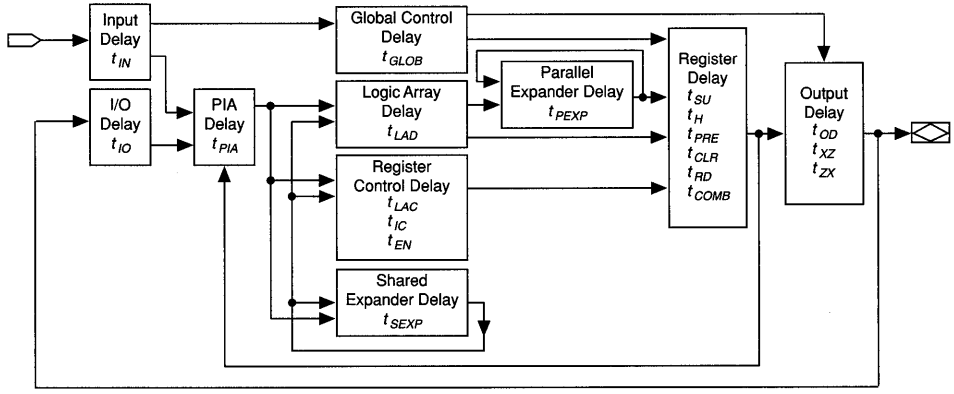
Figure 4. EPS464 EPLD Timing Model



MAX 7000 EPLDs

The MAX 7000 architecture differs from the MAX 5000 architecture in several ways. MAX 7000 architecture has globally routed register Clock and Clear and tri-state buffer Output Enable signals. Two types of expander product terms—shared and parallel—can be used to implement complex logic. Each macrocell can be set for low-power operation to reduce power dissipation in the EPLD. Figure 5 shows the timing model for MAX 7000 EPLDs.

Figure 5. MAX 7000 EPLD Timing Model

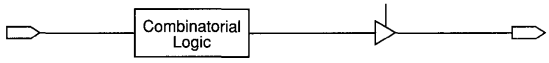


Calculating Timing Delays

You can calculate pin-to-pin timing delays for any device with the appropriate timing model and internal delay parameters. Each AC timing macroparameter is calculated from a combination of internal delays. Figure 6 illustrates the various macroparameters. To calculate the delay for a signal that follows a different path through the EPLD, refer to the timing models shown in Figures 1 through 5 to determine which microparameters to add together.

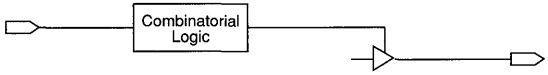
Figure 6. AC Timing Parameters (Part 1 of 3)

Combinatorial Delay

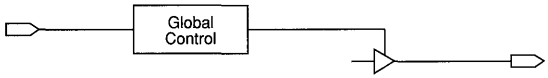


Classic	t_{PD1}	=	$t_{IN} + t_{LAD} + t_{OD}$
	t_{PD2}	=	$t_{IO} + t_{IN} + t_{LAD} + t_{OD}$
MAX 5000	t_{PD1}	=	$t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$
(single-LAB)	t_{PD2}	=	$t_{IO} + t_{LAD} + t_{COMB} + t_{OD}$
MAX 5000	t_{PD1}	=	$t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$
(multi-LAB)	t_{PD2}	=	$t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$
EPS464	t_{PD1}	=	$t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$
	t_{PD2}	=	$t_{IO} + t_{LAD} + t_{COMB} + t_{OD}$
MAX 7000	t_{PD1}	=	$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$
	t_{PD2}	=	$t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$

Tri-State Enable/Disable Delay



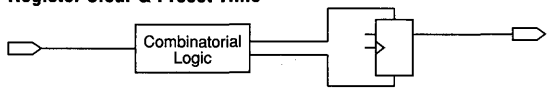
Classic	t_{PXZ}, t_{PZX}	=	$t_{IN} + t_{LAD} + (t_{XZ}$ or $t_{ZX})$
MAX 5000	t_{PXZ}, t_{PZX}	=	$t_{IN} + t_{LAC} + (t_{XZ}$ or $t_{ZX})$
EPS464	t_{PXZ}, t_{PZX}	=	$t_{IN} + t_{LAC} + (t_{XZ}$ or $t_{ZX})$



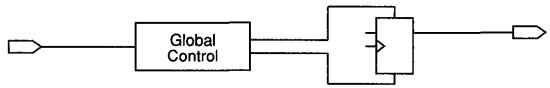
MAX 7000	t_{PXZ}, t_{PZX}	=	$t_{IN} + t_{GLOB} + (t_{XZ}$ or $t_{ZX})$
EPS464	t_{PXZ}, t_{PZX}	=	$t_{IN} + t_{GLOB} + (t_{XZ}$ or $t_{ZX})$

Figure 6. AC Timing Parameters (Part 2 of 3)

Register Clear & Preset Time

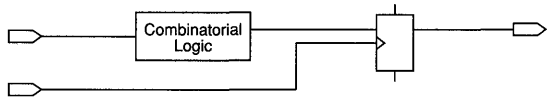


Classic	t_{CLR}	=	$t_{IN} + t_{CLR} + t_{OD}$
MAX 5000	t_{PRE}, t_{CLR}	=	$t_{IN} + t_{LAC} + (t_{PRE}$ or $t_{CLR}) + t_{OD}$
EPS464	t_{PRE}, t_{CLR}	=	$t_{IN} + t_{LAC} + (t_{PRE}$ or $t_{CLR}) + t_{OD}$
MAX 7000	t_{PRE}, t_{CLR}	=	$t_{IN} + t_{PIA} + t_{LAC} + (t_{PRE}$ or $t_{CLR}) + t_{OD}$



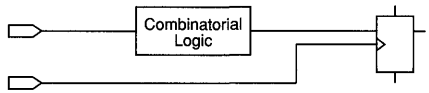
MAX 7000	t_{GCLR}	=	$t_{IN} + t_{GLOB} + t_{CLR} + t_{OD}$
EPS464	t_{GPRE}, t_{GCLR}	=	$t_{IN} + t_{GLOB} + (t_{PRE}$ or $t_{CLR}) + t_{OD}$

Setup Time



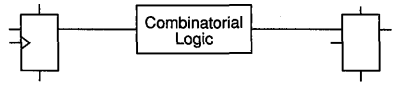
Classic	t_{SU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{ICS}) + t_{SU}$
MAX 5000	t_{SU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{ICS}) + t_{SU}$
EPS464	t_{SU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{GLOB}) + t_{SU}$
MAX 7000	t_{SU}	=	$(t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{GLOB}) + t_{SU}$

Hold Time



Classic	t_{H}	=	$(t_{IN} + t_{ICS}) - (t_{IN} + t_{LAD}) + t_{H}$
MAX 5000	t_{H}	=	$(t_{IN} + t_{ICS}) - (t_{IN} + t_{LAD}) + t_{H}$
EPS464	t_{H}	=	$(t_{IN} + t_{GLOB}) - (t_{IN} + t_{LAD}) + t_{H}$
MAX 7000	t_{H}	=	$(t_{IN} + t_{GLOB}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_{H}$

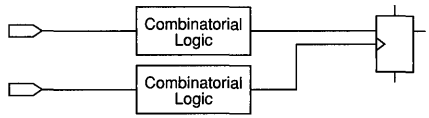
Counter Frequency



Classic	t_{CNT}	=	$t_{FD} + t_{LAD} + t_{SU}$
MAX 5000	t_{CNT}	=	$t_{RD} + t_{FD} + t_{LAD} + t_{SU}$
EPS464	t_{CNT}	=	$t_{RD} + t_{FD} + t_{LAD} + t_{SU}$
MAX 7000	t_{CNT}	=	$t_{RD} + t_{PIA} + t_{LAD} + t_{SU}$

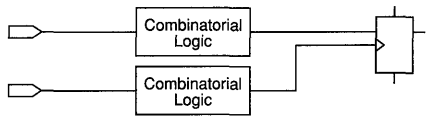
Figure 6. AC Timing Parameters (Part 3 of 3)

Asynchronous Setup Time



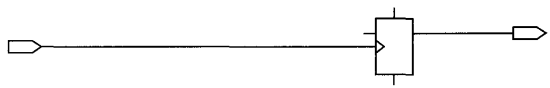
Classic	t_{ASU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$
MAX 5000	t_{ASU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$
EPS464	t_{ASU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$
MAX 7000	t_{ASU}	=	$(t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{PIA} + t_{IC}) + t_{SU}$

Asynchronous Hold Time



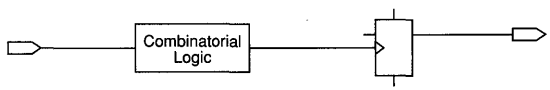
Classic	t_{AH}	=	$(t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_H$
MAX 5000	t_{AH}	=	$(t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_H$
EPS464	t_{AH}	=	$(t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_H$
MAX 7000	t_{AH}	=	$(t_{IN} + t_{PIA} + t_{IC}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_H$

Clock-to-Output Delay



Classic	t_{CO1}	=	$t_{IN} + t_{ICS} + t_{OD}$
MAX 5000	t_{CO1}	=	$t_{IN} + t_{ICS} + t_{RD} + t_{OD}$
EPS464	t_{CO1}	=	$t_{IN} + t_{GLOB} + t_{RD} + t_{OD}$
MAX 7000	t_{CO1}	=	$t_{IN} + t_{GLOB} + t_{RD} + t_{OD}$

Array Clock-to-Output Delay



Classic	t_{ACO1}	=	$t_{IN} + t_{IC} + t_{OD}$
MAX 5000	t_{ACO1}	=	$t_{IN} + t_{IC} + t_{RD} + t_{OD}$
EPS464	t_{ACO1}	=	$t_{IN} + t_{IC} + t_{RD} + t_{OD}$
MAX 7000	t_{ACO1}	=	$t_{IN} + t_{PIA} + t_{IC} + t_{RD} + t_{OD}$

Examples

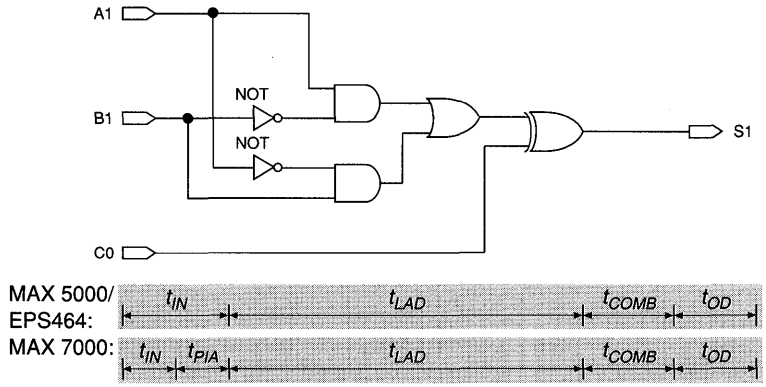
The following examples show how to use microparameters to calculate the delays for real applications.

Example 1: 7483 TTL Macrofunction

You can analyze the timing delays for macrofunctions that have been subjected to minimization and logic synthesis. A MAX+PLUS II Report File that includes the optional Equations Section lists the synthesized logic equations. These equations are structured so that you can quickly determine the logic configuration. For example, Figure 7 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The Report File gives the following equations for S1, the least significant bit of the adder:

```
S1      = OUTPUT ( _LC021 , VCC );
_LC021 = LCELL   ( _EQ026 $ C0  );
_EQ026 = B1   & !A1
       # !B1 &  A1;
```

Figure 7. Adder Logic Timing for MAX 5000/EPS464 & MAX 7000 Architecture



S1 is the output of macrocell 21 (_LC021), which contains combinatorial logic. The combinatorial logic LCELL(_EQ026 $ C0) represents the XOR of the intermediate equation _EQ026 and the carry-in C0. In turn, _EQ026 is logically equivalent to the XOR of inputs B1 and A1. Therefore:

Timing delay for S1 in MAX 5000/EPS464 EPLDs:

$$t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$$

Timing delay for S1 in MAX 7000 EPLDs:

$$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$$

Example 2: S2 Adder Bit

For complex logic that requires expanders (represented as _X<*number*> in Report Files), the expander array delay, t_{EXP} (or t_{SEXP} for MAX 7000 EPLDs), is added to the delay element. The second bit of the 7483 adder macrofunction, S2, requires shared expanders. The equations are:

```
S2      =  _LC019;
_LC019  =  LCELL( _EQ023  $  _EQ024 );
_EQ023  =  _X029  &  _X030  &  _X031;
_X029   =  EXP( !B1  &  !A1 );
_X030   =  EXP( !B1  &  !C0 );
_X031   =  EXP( !A1  &  !C0 );
_EQ024  =  _X032  &  _X033;
_X032   =  EXP( !B2  &  A2  );
_X033   =  EXP(  B2  &  A2  );
```

Figure 8 shows how you can map the logic structure onto the MAX 5000/ EPS464 and MAX 7000 architectures with these equations. Therefore:

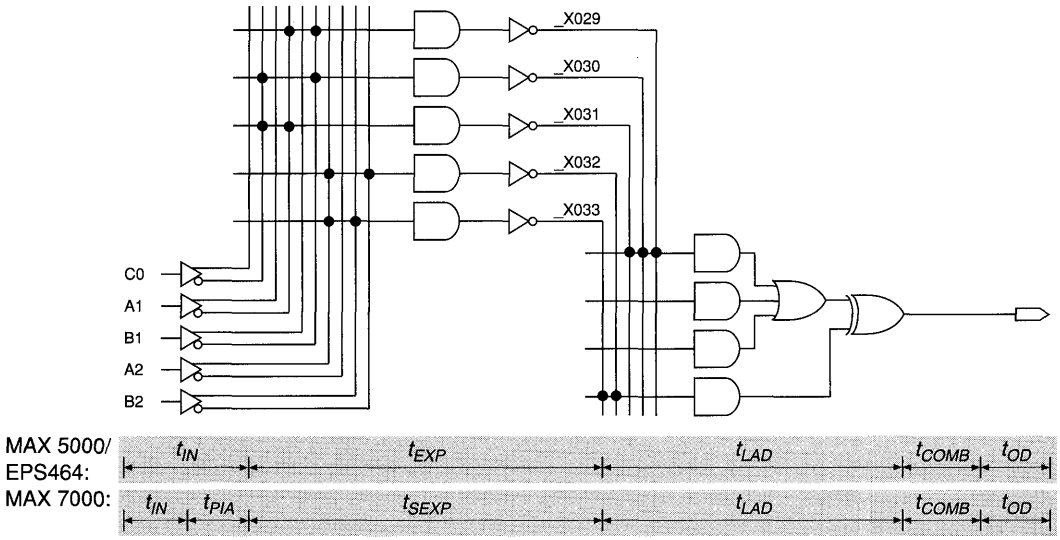
Timing delay for S2 in MAX 5000/EPS464 EPLDs:

$$t_{IN} + t_{EXP} + t_{LAD} + t_{COMB} + t_{OD}$$

Timing delay for S2 in MAX 7000 EPLDs:

$$t_{IN} + t_{PIA} + t_{SEXP} + t_{LAD} + t_{COMB} + t_{OD}.$$

Figure 8. Adder Equations Mapped to MAX 5000/EPS464 & MAX 7000 Architecture



Example 3: S2 Adder Bit With Parallel Expanders (MAX 7000)

The Compiler uses parallel expanders if the Parallel Expanders logic synthesis option is turned on when a project is compiled for MAX 7000 EPLDs. When parallel expanders are used, no shareable expanders are used, and the timing delay for the S2 bit of the 7483 becomes:

$t_{IN} + t_{PIA} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{OD}$

Example 4: S1 Adder Bit in Low-Power Mode (MAX 7000)

If a macrocell in a MAX 7000 EPLD is set for low-power mode, then you must add the low-power adder delay to the total delay through that macrocell. In Figure 7, the S1 delay thus becomes:

$t_{IN} + t_{PIA} + t_{LPA} + t_{LAD} + t_{COMB} + t_{OD}$

Conclusion

The architectures of Altera EPLDs have fixed internal timing delays that are independent of routing. You can determine the worst-case timing delays for any design before programming a device. Total delay paths (macroparameters) can be expressed as the sums of internal timing delays (microparameters). Timing models illustrate the internal delay paths for EPLDs and show how these microparameters affect each other. You can use MAX+PLUS II development tools to automatically calculate delay paths, or hand-calculate delay paths by adding the microparameters for an appropriate timing model. With this ability to predict worst-case timing delays, you can be confident of a design's in-system timing performance.

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Programmable Logic Development System & Software

August 1993, ver. 4 Data Sheet

Introduction

A programmable logic design environment ideally satisfies a large variety of design requirements: it should support devices with different architectures, run on multiple platforms, provide an easy-to-use interface, and offer a broad range of features. Moreover, the design environment should give designers the freedom to use the tools of their choice. The Altera MAX+PLUS II development system, a fully integrated programmable logic design environment, meets all of these requirements.

The MAX+PLUS II design environment offers unmatched flexibility and performance. The rich graphical user interface is complemented by complete and instantly accessible on-line documentation, which makes learning and using MAX+PLUS II quick and easy.

- *Modular Tools* Designers can customize their development environment by choosing from a variety of design entry, design processing, and design verification options, all of which are described in this data sheet. New features can be added as they are needed, preserving the initial tools investment. Since MAX+PLUS II supports multiple device families, designers can add support for new architectures without having to learn new tools.

- *Architecture-Independence* The MAX+PLUS II Compiler, the heart of the MAX+PLUS II system, supports Altera's Classic, MAX 5000/ EPS464, MAX 7000, and FLEX 8000 programmable logic device families, offering the industry's only truly architecture-independent programmable logic design environment. The Compiler also provides powerful logic synthesis and minimization to efficiently fit designs with minimal user effort.

- *Multiple Platforms* MAX+PLUS II runs under Microsoft Windows on 386- or 486-based PCs and under X Windows on Sun SPARCstations and HP 9000 Series 700 workstations.

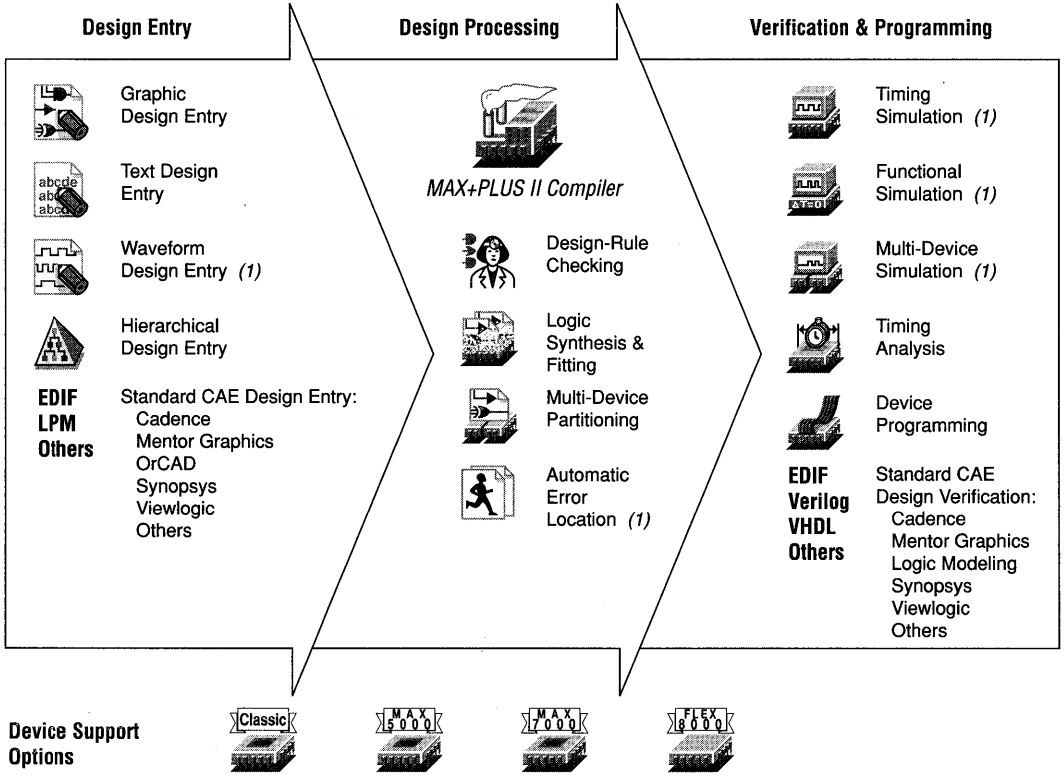
- *Open Interfaces* Altera works closely with CAE manufacturers to link MAX+PLUS II with other industry-standard design entry, synthesis, and verification tools. The interfaces to CAE tools comply with EDIF 2 0 0 or 2 9 0, library of parameterized modules (LPM), Verilog, VHDL, and other standards. They allow designers to create a logic design with Altera or standard CAE design entry tools, compile the design for an Altera device with the MAX+PLUS II Compiler, and

perform device- or board-level simulation with Altera or other CAE verification tools. MAX+PLUS II currently supports interfaces to tools from Cadence, Exemplar, Data I/O, Intergraph, Mentor Graphics, Minc, OrCAD, Synopsys, Viewlogic, and others.

- *Full Integration* Together, the MAX+PLUS II design entry, processing, and verification features offer the most fully integrated suite of programmable logic development tools available, allowing faster debug and shorter development cycles.

The MAX+PLUS II design process, shown in Figure 1, consists of four phases: design entry, design processing, design verification, and device programming.

Figure 1. MAX+PLUS II Design Environment



Note:
(1) Available only in the PC-based version of MAX+PLUS II.

Design Entry

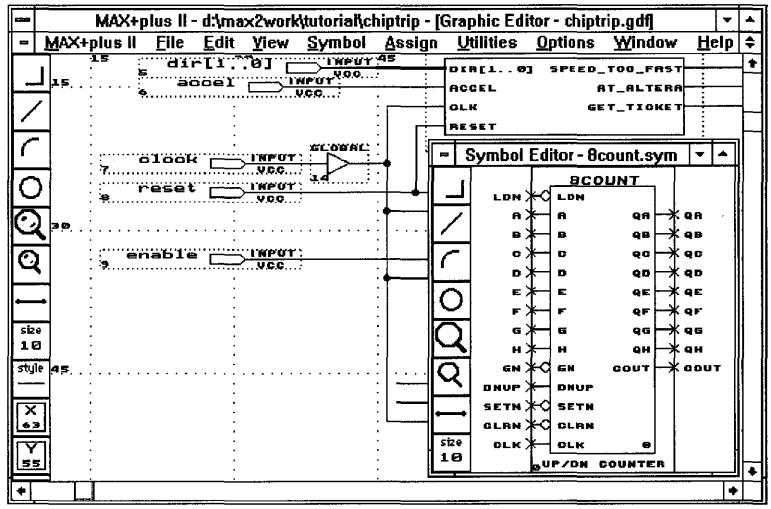
MAX+PLUS II can integrate design files—generated with the MAX+PLUS II design entry tools or with a variety of other industry-standard CAE design entry tools—into a single design hierarchy. The high degree of integration between MAX+PLUS II applications allows information to flow freely to and from each application. For example, errors identified during compilation, simulation, and timing analysis can be automatically located and highlighted in the original design file. If a design (called a project in MAX+PLUS II) consists of two or more hierarchical levels, the designer can go from one design file directly to all other design files in the hierarchy, regardless of whether they are graphic-, text-, or waveform-based.

Schematic Capture & Symbol Editing

The MAX+PLUS II Graphic Editor (shown in Figure 2) makes schematic design entry fast and easy. Drag-and-drop editing quickly moves one or more objects or an entire area. During a move, a net can be preserved with the rubberbanding feature. The designer can also make a design more compact by connecting primitives with buses to create arrays of symbols. Over 300 74-series and other macrofunctions are available.

MAX+PLUS II can automatically create a symbol for any design file. With the Symbol Editor (also shown in Figure 2), the designer can modify a symbol to customize its appearance, or create an entirely new symbol.

Figure 2. MAX+PLUS II Graphic & Symbol Editors



Text Design Entry

With the MAX+PLUS II Text Editor, the designer can view and edit any ASCII text file, including EDIF netlists. The Text Editor is ideal for entering and editing design files written in the Altera Hardware Description Language (AHDL).

AHDL

The Altera Hardware Description Language (AHDL) is a high-level modular language used to create logic designs for Altera devices. It can implement state machines, truth tables, conditional logic, and Boolean equations. AHDL syntax supports arithmetic and relational operations such as addition, subtraction, equality, and magnitude comparisons. Standard Boolean functions (e.g., AND, OR, NAND, NOR, XOR, and XNOR) are also available. Since AHDL supports groups, operations can be performed on a byte- or word-wide basis as well as on single variables. Together, these features make it easy to implement complex projects in a concise, high-level description.

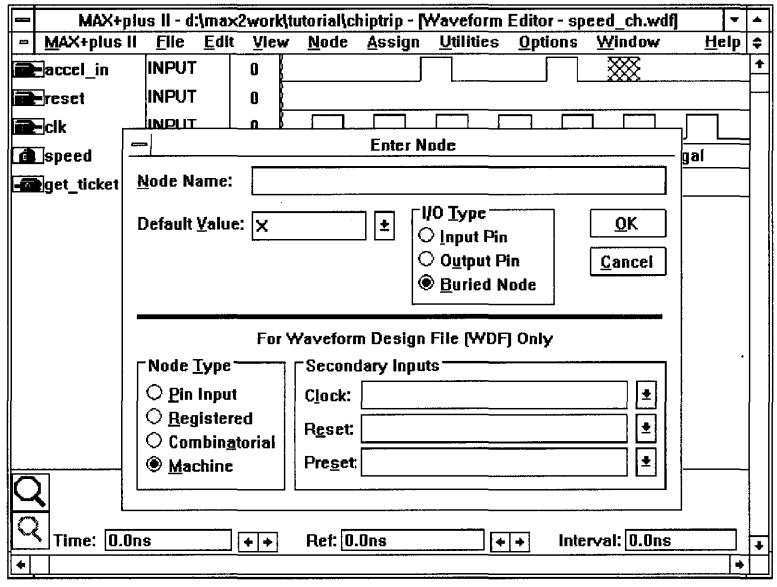
Waveform Design Entry

The MAX+PLUS II Waveform Editor (shown in Figure 3) is used to create and edit waveform design files, as well as input vectors for simulation and functional testing. The Waveform Editor also functions as a logic analyzer that allows the designer to view simulation results.

Waveform design entry is best suited for sequential and repeating functions. The Compiler's advanced waveform synthesis algorithms automatically generate logic from user-defined input and output waveforms that represent registered, combinatorial, and state machine logic. The Compiler automatically assigns state bits and state variables for state machines.

Waveform Editor features allow the designer to copy, cut, paste, repeat, and stretch waveforms; to create design files with internal nodes, flipflops, and state machines; to combine waveforms into groups that display binary, octal, decimal, or hexadecimal values; and to compare two sets of simulation results by superimposing one set of waveforms on another.

Figure 3. MAX+PLUS II Waveform Editor



Industry-Standard CAE Design Entry

The MAX+PLUS II Compiler can interface with other standard CAE tools that generate EDIF 2 0 0 and EDIF 2 9 0 netlist files. The Compiler uses Library Mapping Files (**.lmf**) to map proprietary symbol and pin names from other CAE tools to MAX+PLUS II macrofunction and basic-gate library elements. Altera provides LMFs for over 100 74-series and custom macrofunctions for files generated by tools from companies such as Cadence, Mentor Graphics, Minc, OrCAD, and Viewlogic. VHDL and Verilog design support is also available through Cadence, Exemplar, Intergraph, Mentor Graphics, Racal-Redac, Synopsys, and Viewlogic. For more information on other industry-standard design entry tools, see *CAE Software Support* in this data book.

MAX+PLUS II also supports design entry using the Library of Parameterized Modules (LPM). The LPM standard is built upon and follows the syntax for the EDIF 2 0 0 standard. The Compiler processes LPM netlists automatically, translating them into a MAX+PLUS II-compatible format. All LPM gate, arithmetic, and storage components are supported.

MAX+PLUS II can also read OrCAD Schematic Files (**.sch**) and Xilinx Netlist Format Files (**.xnf**) for compilation or integration into designs for Altera devices.

Hierarchical Design Entry

Hierarchical designs can consist of design files created with several different formats, including schematic capture, text design entry (with AHDL), waveform design entry, and EDIF. MAX+PLUS II supports multiple levels of hierarchy in a single design. This flexibility allows designers to use the design entry method best suited to each portion of the design. The MAX+PLUS II Hierarchy Display, which displays the hierarchy of the project, allows designers to easily traverse the hierarchy, automatically opening the appropriate editor for each design file.

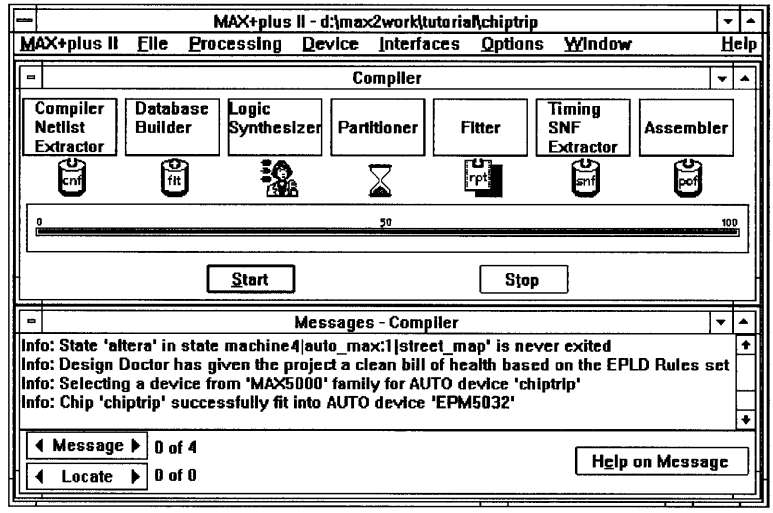
Design Processing

When MAX+PLUS II processes a design, the Compiler reads in design files and produces programming and simulation files, the Timing Analyzer analyzes the timing of a design, and the Message Processor automatically locates errors.

Automatic Error Location

The MAX+PLUS II Message Processor communicates with all MAX+PLUS II applications, recording error, information, and warning messages for problems such as connection and syntax errors. Designers can use the Message Processor to automatically open the file that contains the source of an error and highlight its location. See Figure 4.

Figure 4. MAX+PLUS II Compiler & Message Processor



Logic Synthesis & Fitting

The Compiler's Logic Synthesizer module supports both synthesized and what-you-see-is-what-you-get (WYSIWYG) design implementation. It selects appropriate logic reduction algorithms to minimize and remove redundant logic, ensuring that the device logic resources are used as efficiently as possible for a specified device architecture. It also removes unused logic from the project.

Logic synthesis options help the designer guide the outcome of logic synthesis. Altera provides three "ready-made" synthesis styles, which specify the settings for multiple logic synthesis options. The designer can apply a style to set default synthesis options, create custom styles, and specify individual synthesis options on selected logic functions. Synthesis options can be tailored for a specific device family to take advantage of its architecture. A number of advanced logic options further expand the designer's ability to influence logic synthesis.

The Compiler's Fitter module applies heuristic rules to select the best possible implementation for the synthesized project in one or more devices. This automatic fitting relieves the designer of tedious place-and-route tasks. The Fitter generates a Report File (**.rpt**) that shows project implementation as well as any unused resources in the device(s).

Design-Rule Checking

The MAX+PLUS II Compiler includes the Design Doctor, a design-rule-checker utility. This utility checks each design file for logic that may cause system-level reliability problems usually discovered only *after* a design has entered production. The user can choose one of three predefined sets of design rules with increasingly thorough design-rule checking, or create a custom set of rules.

Design rules are based on reliability guidelines that cover logic containing features such as asynchronous inputs, ripple Clocks, multi-level logic on Clocks, Preset and Clear configurations, and race conditions. Rule violations are explained to help the designer determine which edits are needed in the design files.

Multi-Device Partitioning

If a project does not fit into a single device, the Compiler's Partitioner module divides it into multiple devices from the same device family. It attempts to split the project into the smallest possible number of devices while minimizing the number of pins used for inter-device communication. The Fitter automatically fits the logic into the specified devices.

Partitioning can be totally automatic, partially user-controlled, or fully user-controlled. If a project is too large to fit into a specified device, the designer can specify the type and number of additional devices.

Industry-Standard Output Formats

The Compiler provides netlist writers that can create netlists that can be used in a variety of simulation environments. These netlists contain post-synthesis functional and timing information that can be used with other standard design verification tools for device- or board-level simulation. The following interfaces are available:

- *EDIF Interface* Creates EDIF 2 0 0 and EDIF 2 9 0 netlists.
- *Verilog Interface* Creates Verilog netlists that can be used with Verilog-XL simulators.
- *VHDL Interface* Creates VHDL netlists that can be used with VHDL simulators.

Programming File Generation

The Assembler module creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), and/or JEDEC Files (**.jed**) for a compiled project. The MAX+PLUS II Programmer uses these files and standard Altera hardware to program the desired devices. Device programming is also available with other industry-standard programming equipment. In addition, MAX+PLUS II can generate Intel-format Hexadecimal Files (**.hex**) and Tabular Text Files (**.ttf**) for configuring FLEX 8000 devices. See *Application Note 33 (Configuring FLEX 8000 Devices)* in this data book for more information.

Design Verification

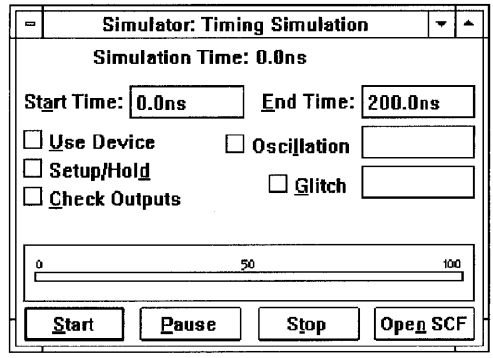
Design verification processes include design simulation and timing analysis to test the logical operation and internal timing of a design. Design verification is available from Altera and from a variety of CAE vendors.

Simulation

The MAX+PLUS II Simulator provides flexibility and control for modeling single- or multi-device projects. The Simulator uses the Simulator Netlist File (**.snf**) generated during compilation to perform functional, timing, or combined linked multi-device simulation for a project. Figure 5 shows the Simulator window.

The designer either defines input stimuli with a straightforward vector input language or draws waveforms directly with the MAX+PLUS II Waveform Editor. Simulation results can be viewed in the Waveform Editor or Text Editor and printed as waveform or text files.

Figure 5. MAX+PLUS II Simulator



The designer specifies commands either interactively or in a Command File (**.cmd**) to perform a variety of tasks, such as monitoring the project for glitches, oscillation, and register setup and hold time violations; halting the simulation when user-defined conditions are met; forcing flipflops high or low; and performing functional testing. If a setup or hold time, minimum pulse width, or oscillation period is violated, the Message Processor reports the problem. The designer can then use the Message Processor to locate the time at which the problem occurred in the Waveform Editor and to locate the error in the original design file.

For easy comparison, the designer can superimpose the results of two simulations in the Waveform Editor.

Functional Simulation

The MAX+PLUS II Simulator supports functional simulation that tests the logical operation of a project before it is synthesized, allowing the designer to quickly identify and correct logical errors. The MAX+PLUS II Waveform Editor displays the results of functional simulation and provides easy access to all nodes in the project, including combinatorial functions.

Timing Simulation

In a timing simulation, the MAX+PLUS II Simulator tests the project after it has been fully synthesized and optimized. Timing simulation is performed at 0.1-ns resolution.

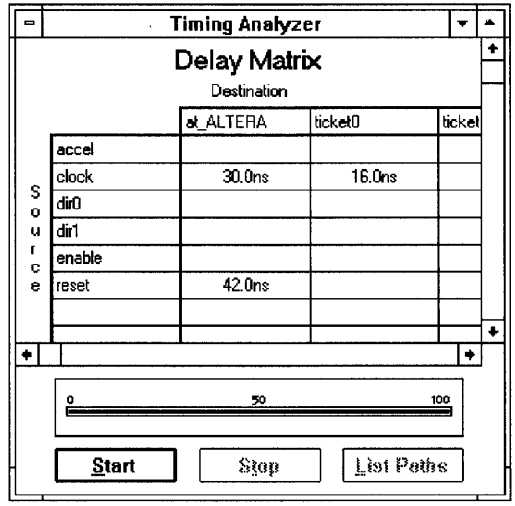
Multi-Device Simulation

MAX+PLUS II can combine the timing and/or functional information from multiple Altera devices, allowing the designer to simulate several devices operating together. These projects can be implemented in different device families.

Timing Analysis

The MAX+PLUS II Timing Analyzer can calculate a matrix of point-to-point device delays, determine setup and hold time requirements at device pins, and calculate maximum Clock frequency. MAX+PLUS II design entry tools are integrated with the Timing Analyzer, allowing the designer to simply tag start and end points in the design to determine the shortest and longest propagation delays. In addition, the Message Processor can locate critical paths identified by the Timing Analyzer in the design files and display them in the appropriate design editor. See Figure 6.

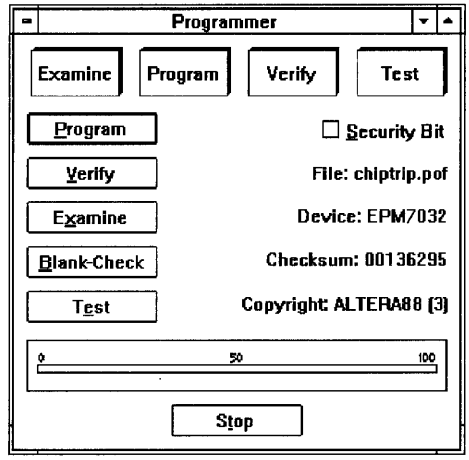
Figure 6. MAX+PLUS II Timing Analyzer



Device Programming

The MAX+PLUS II Programmer, shown in Figure 7, uses programming files generated by the Compiler to program Altera devices. It allows the designer to program, verify, examine, blank-check, and functionally test devices. The programming hardware includes an add-on Logic Programmer card (for PC-AT, PS/2, or compatible computers) that drives the Altera Master Programming Unit (MPU). The MPU performs continuity checking to ensure adequate electrical contact between the programming adapter and the device. With the appropriate programming adapter, the MPU also

Figure 7. MAX+PLUS II Programmer



supports functional testing, so that vectors created for simulation can be applied to a programmed device to verify its functionality.

All hardware and software necessary for programming and verifying devices is available from Altera (see *Altera Programming Hardware* in this data book). Programming support is also available from many other programming hardware manufacturers (see *Programming Hardware Manufacturers* in this data book).

On-Line Help

On-line help provides access to all information on MAX+PLUS II. It includes complete, up-to-date documentation on all MAX+PLUS II applications, causes and suggested actions for messages, references to related Altera documentation, text file formats (e.g., AHDL), and information on Altera devices and adapters.

On-line help is only a keystroke or a mouse click away. The F1 key provides instant access to information on a dialog box, highlighted menu command, or pop-up message. Typing Shift+F1 turns the mouse pointer into a question mark pointer that allows the designer to click on any item on the screen—including primitives, macrofunctions, and AHDL keywords—for context-sensitive help on that item.

Software Maintenance Agreement

To guarantee timely upgrades to software and documentation, Altera offers a Software Maintenance Agreement that entitles the customer to software updates, discounts on selected software products, Applications Engineering support, and access to Altera's electronic bulletin board service (BBS).

Recommended System Configurations

To run MAX+PLUS II with optimum results, Altera recommends the following system configurations:

PC System Configuration

- ❑ 386- or 486-based PC-AT, PS/2 Model 70 or higher, or compatible computer
- ❑ 16 Mbytes of RAM
- ❑ DOS version 5.0 or higher
- ❑ Microsoft Windows version 3.1
- ❑ Microsoft Windows-compatible graphics card and monitor
- ❑ 35 Mbytes free disk space
- ❑ 1.44-Mbyte 3 ½-inch floppy disk drive
- ❑ 2- or 3-button mouse compatible with Microsoft Windows 3.1
- ❑ Full-length 8-bit ISA or Micro Channel Adapter slot for Logic Programmer card
- ❑ Parallel port

Sun Workstation System Configuration

- ❑ Sun SPARC2 workstation with color or monochrome monitor
- ❑ 32 Mbytes of RAM
- ❑ Sun OS 4.1.2 (or Solaris 1.0), *Note (1)*
- ❑ Sun OpenWindows 3.0 (or Solaris 1.0), *Note (1)*
- ❑ 50 Mbytes free disk space
- ❑ 30 Mbytes swap space
- ❑ ISO 9660-compatible CD-ROM drive

Hewlett-Packard Workstation System Configuration

- ❑ HP 9000 Series 700 workstation with color or monochrome monitor
- ❑ HP-UX 8.07, *Note (1)*
- ❑ HP-VUE
- ❑ 50 Mbytes free disk space
- ❑ 32 Mbytes of RAM
- ❑ ISO 9660-compatible CD-ROM drive

Note:
(1) Contact Altera Applications for information on current operating system support.

Package Options

Altera offers a variety of tool configurations and migration products for PC- and workstation-based versions of MAX+PLUS II. For up-to-date information on MAX+PLUS II software packages and development systems, refer to *Ordering Information* in this data book or contact Altera Marketing at (408) 894-7000. For detailed information on package options, refer to the *MAX+PLUS II Selection Guide* in this section.

MAX+PLUS II Selection Guide

August 1993, ver. 1

Development Systems & Add-On Products

Altera offers a variety of system configurations and add-on products for MAX+PLUS II. MAX+PLUS II supports all of Altera's general-purpose programmable logic devices, including EPROM-, EEPROM- and SRAM-based devices, for true technology-independent design. Once designers purchase a device support option, they can add to it at any time. Four device support options are available:

- *Classic+Plus* Supports the low-power Classic family, and the EPM5016, EPM5032, EPM7032, and EPM7032V devices.
- *MAX 5000/EPS464* Supports the mid-range MAX 5000/EPS464 family.
- *MAX 7000* Supports the high-performance MAX 7000 family.
- *FLEX 8000* Supports the register-intensive, high-gate-count, SRAM-based FLEX 8000 family.

The first decision to make in selecting a MAX+PLUS II system is to determine the device support needed. The second is to select the desired features. Table 1 shows the available features and Altera device support provided by each MAX+PLUS II configuration. Refer to the Device Support columns in this table, and then use the Design Entry and Compilation and Verification columns to select the configuration with the appropriate design development features. The Ordering Codes column provides the necessary codes for ordering MAX+PLUS II systems and add-on products that provide features not included in the initial package purchased by the user.

For up-to-date information on available features and device support, contact Altera Marketing at (408) 894-7000 for a copy of the most current MAX+PLUS II selection guide.

For a detailed description of MAX+PLUS II development software, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Table 1. Altera Development Systems, Software & Device Support

Ordering Codes	Design Entry				Compilation & Verification									Device Support		
	Schematic Capture	Waveform Design Entry	Text Design Entry	EDIF Interface	Design-Rule Checking	Functional Simulation	Timing Simulation	Multi-Device Simulation	Multi-Device Partitioning	Logic Synthesis & Fitting	Timing Analysis	Waveform Editing	Programming Hardware	FLEX 8000	MAX 7000	MAX 5000/EPS464	Classic-Plus
Base Systems (PC Platform)																	
PLS-ES	✓		✓	✓						✓	✓						✓
PLS-STD	✓		✓	✓						✓	✓					✓	✓
PLS-ADV	✓		✓	✓						✓	✓				✓	✓	✓
PLS-FLEX8	✓		✓	✓						✓	✓			✓		✓	✓
PLS-HPS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓
PLDS-HPS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
Add-On Products (PC Platform)																	
PLSM-5K																✓	
PLSM-7K															✓		
PLSM-8K														✓			
PLSM-ADE		✓			✓	✓	✓	✓	✓			✓					
Base Systems (Workstation Platform)																	
PLS-WS/HP			✓	✓	✓					✓				✓	✓	✓	✓
PLS-WS/SN			✓	✓	✓					✓				✓	✓	✓	✓
Add-On Products (Workstation Platform)																	
PLSM-WS/SN			✓	✓	✓					✓				✓	✓	✓	✓
PLSM-WS/HP			✓	✓	✓					✓				✓	✓	✓	✓
PLSM-TA											✓						

MAX+PLUS II Package Options

This section describes the various MAX+PLUS II products shown in Table 1, as well as software maintenance products that provide registered users with regular upgrades to software and documentation. For information on ordering Altera products, see *Ordering Information* in this data book.

PC-Based System Configurations

PLS-ES

Contains logic synthesis and fitting support for the Classic family and the EPM5016, EPM5032, EPM7032, and EPM7032V devices. Also includes schematic capture, text design entry with AHDL, interface through EDIF 2 0 0 and 2 9 0 input and output files, LPM netlist reader, hierarchical

design management, on-line help, automatic error location, and timing analysis.

PLS-STD
Contains logic synthesis and fitting support for the MAX 5000/EPS464 and Classic families, and the EPM7032 and EPM7032V devices. Also includes schematic capture, text design entry with AHDL, interface through EDIF 2 0 0 and 2 9 0 input and output files, LPM netlist reader, hierarchical design management, on-line help, automatic error location, and timing analysis.

PLS-ADV
Contains logic synthesis and fitting support for the MAX 7000, MAX 5000/EPS464, and Classic families. Also includes schematic capture, text design entry with AHDL, interface through EDIF 2 0 0 and 2 9 0 input and output files, LPM netlist reader, hierarchical design management, on-line help, automatic error location, and timing analysis.

PLS-FLEX8
Contains logic synthesis and fitting support for the FLEX 8000, MAX 5000/EPS464, and Classic families, and the EPM7032 and EPM7032V devices. Also includes schematic capture, text design entry with AHDL, interface through EDIF 2 0 0 and 2 9 0 input and output files, LPM netlist reader, hierarchical design management, on-line help, automatic error location, and timing analysis.

PLS-HPS/PLDS-HPS
Contains all features and device support of PLS-ADV, plus waveform design entry, design-rule checking, multi-device partitioning, timing simulation, multi-device simulation, functional simulation, and waveform editing. PLDS-HPS also includes selected programming hardware, including the Altera Master Programming Unit (MPU).

PC-Based Add-On Products

PLSM-5K
Adds compilation support for the Altera MAX 5000/EPS464 family to PLS-ES.

PLSM-7K
Adds compilation support for the Altera MAX 7000 family to PLS-ES, PLS-STD, and PLS-FLEX8.

PLSM-8K
Adds compilation support for the Altera FLEX 8000 family to PLS-ES, PLS-STD, PLS-ADV, PLS-HPS, and PLDS-HPS.

PLSM-ADE
Adds waveform design entry/editing; design-rule checking; functional, timing, and multi-device simulation; and multi-device partitioning to PLS-ES, PLS-STD, PLS-ADV, and PLS-FLEX8.

PLAESW-xxx
Software maintenance products for PC-based MAX+PLUS II. Software Maintenance Agreements ensure that registered users receive all upgrades to software and documentation when development software is upgraded or modified to provide new features and/or to support new devices. To order a Software Maintenance Agreement, use the PLAESW- prefix followed by the appropriate product extension (e.g., PLAESW-HPS).

Workstation-Based System Configurations

PLS-WS/SN and PLS-WS/HP
Contains logic synthesis and fitting support for the Classic, MAX 5000/ EPS464, MAX 7000, and FLEX 8000 families. Interface provided to Mentor Graphics, Cadence, Synopsys, Viewlogic, Intergraph, and other CAE environments through EDIF 200 and 290 input and output files. Workstation support also includes text design entry with AHDL, design-rule checking, and multi-device partitioning. PLS-WS/SN supports appropriately configured Sun Sparcstations; PLS-WS/HP supports appropriately configured HP 9000 Series 700 workstations.

PLAESW-WS
Software maintenance product for workstation-based MAX+PLUS II.

Workstation-Based Add-On Products

PLSM-TA
Adds timing analysis capabilities to MAX+PLUS II for workstations. The MAX+PLUS II Timing Analyzer can calculate a matrix of point-to-point device delays, determine set-up and hold-time requirements at device pins, and calculate maximum Clock frequency.

PLSM-WS/SN and PLSM-WS/HP
Provides additional floating node licenses for workstation-based MAX+PLUS II.

Altera Programming Hardware

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General Description

Altera offers a variety of programming hardware to program and configure Altera devices. The following products are available:

- Logic Programmer Cards
- Master Programming Unit
- Programming Adapters & FLEX Download Cable
- Altera Stand-Alone Programmer

Logic Programmer Cards

Logic Programmer cards generate programming waveforms and voltages for the Master Programming Unit (MPU). Two Logic Programmer cards are available: the LP5 and LP6. The LP6 card interfaces with IBM PC-AT and compatible computers; the LP5 card interfaces with IBM PS/2 Model 50, 60, 70, and 80 and compatible Micro Channel computers. Both cards are software-controlled and can be installed into any full-length expansion slot in a computer.

Ordering Codes: PLP5, PLP6

Master Programming Unit

The Master Programming Unit (MPU) is a hardware module that is used together with an appropriate adapter to program Altera devices. The MPU connects to a Logic Programmer card via a 25-pin ribbon cable. The MPU receives power from the Logic Programmer card and does not require an external power supply. Programming and functional test information is transmitted from the Logic Programmer card through the ribbon cable to the MPU. A programming indicator LED on the MPU lights up when the unit is active.

When used with the appropriate adapter, the MPU automatically tests for continuity between the device leads and the programming socket before programming. It can also apply test vectors to functionally test and verify programmed Altera devices. Test vectors can be created in waveform or text format in the MAX+PLUS II Waveform Editor or Text Editor and applied to the device; results can be viewed in waveform or text format.

Ordering Code: PL-MPU

Altera Stand-Alone Programmer

The Altera Stand-Alone Programmer, PL-ASAP2, provides the hardware and software needed for programming all Altera devices. PL-ASAP2 includes an LP6 Logic Programmer card, an MPU, MAX+PLUS II Programmer software (which requires Microsoft Windows version 3.1 or higher), and complete documentation.

Ordering Code: PL-ASAP2

Programming Adapters & FLEX Download Cable

Altera provides programming adapters for all Altera devices. Two types of adapters plug directly into the MPU: PLM-prefix and PLAD3-12 adapters. PLM-prefix programming adapters contain a socket that supports a specific device package. The PLAD3-12 compatibility adapter allows PLE-prefix programming adapters to be used with the MPU. The PLAD3-12 adapter also directly supports programming of the EP330.

Adapters for Configuration EPROMs (PLMJ1213 and PLMT1064) program the Configuration EPROMs used to configure FLEX 8000 devices. These adapters are also used to download configuration data directly to FLEX 8000 devices via the FLEX Download Cable, which is provided with Configuration EPROM adapters.

Each adapter contains a zero-insertion-force dual in-line package (DIP), J-lead, pin-grid array (PGA), small-outline integrated circuit (SOIC), or quad flat pack (QFP) socket. The adapters for QFP devices with 100 or more pins support Altera's QFP carrier technology. See the *QFP Carrier & Development Socket Data Sheet* in this data book for more information.

All PLM-prefix adapters, except the Configuration EPROM adapters, allow functional test vectors to be applied to and read from programmed Altera devices. Both PLM- and PLE-prefix adapters support open-circuit testing.

Table 1 lists Altera devices, package options, and required adapters.

Ordering Codes: PLExxxx, PLMxxxx, PLAD3-12

Table 1. Device Adapter Support (Part 1 of 2)

Device	Package	Adapter
EP330	DIP J-Lead SOIC	PLAD3-12 PLEJ330 PLES330
EP600/610/610A/610T	DIP J-lead SOIC	PLED610 PLEJ610 PLES610
EP900/910/910A/910T	DIP J-lead	PLED910 PLEJ910
EP1800/1810/1810T	J-lead PGA	PLMJ1810 PLEG1810
EPB2001	J-lead	PLEJ2001
EPM5016	DIP J-lead SOIC	PLED5016 PLEJ5016 PLES5016
EPM5032	DIP J-lead SOIC	PLMD5032 PLMJ5032 PLES5032
EPM5064	J-lead	PLMJ5064
EPM5128/5128A	J-lead PGA	PLMJ5128A PLMG5128A
EPM5130	J-lead PGA QFP	PLMJ5130 PLEG5130 PLMQ5130
EPM5192/5192A	J-lead PGA QFP (EPM5192A only)	PLMJ5192 PLMG5192 PLMQ5192A
EPM7032, EPM7032V	J-lead QFP TQFP	PLMJ7032-44 PLMQ7032-44 PLMT7032-44
EPM7064	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) QFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128	J-lead (68-pin) J-lead (84-pin) QFP (100-pin) QFP (160-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100 PLMQ7128-160

Table 1. Device Adapter Support (Part 2 of 2)

Device	Package	Adapter
EPM7160	J-lead QFP (100-pin) QFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7160-160
EPM7192	PGA QFP	PLMG7192-160 PLMQ7192-160
EPM7256	PGA QFP (160-pin) QFP (208-pin)	PLMG7256-192 PLMQ7256-160 PLMQ7256-208
All FLEX 8000 devices	all	*Note (1)*
EPC1064	DIP J-lead TQFP	PLMJ1213 PLMJ1213 PLMT1064
EPC1213	DIP J-lead	PLMJ1213 PLMJ1213
EPS448	DIP J-lead	PLED448 PLEJ448
EPS464	J-lead QFP	PLMJ464 PLMQ464

Note to table:
(1) Configuration of FLEX 8000 devices is supported by Configuration EPROMs and the FLEX Download Cable.

Programming Support

Altera customers can obtain or increase device support with the hardware shown in Table 2. By matching his or her current programming hardware setup with the desired device support, the designer can determine additional programming hardware that is required for device programming.

Table 2. Programming Hardware Requirements (Part 1 of 2)

Current Programming Hardware	Desired Device Support	Additional Programming Hardware Required	
		IBM PC-AT & Compatible	IBM PS/2 & Compatible
None	All Altera devices	PL-ASAP2; Appropriate programming adapters	PLP5; PL-MPU; Appropriate programming adapters
LP5 or LP6 Logic Programmer card	All Altera devices	PL-MPU; Appropriate programming adapters	PL-MPU; Appropriate programming adapters

Table 2. Programming Hardware Requirements (Part 2 of 2)

Current Programming Hardware	Desired Device Support	Additional Programming Hardware Required	
		IBM PC-AT & Compatible	IBM PS/2 & Compatible
LP5 or LP6 Logic Programmer card; PLE3-12A or PLE3-12, programming unit or PL-MPU programming unit (with PLAD3-12 adapter)	All Classic devices EPM5016 EPM5032 (SOIC) EPM5130 EPS448 EPB2001	Appropriate programming adapters	Appropriate programming adapters
LP5 or LP6 Logic Programmer card; PL-MPU programming unit	EPM5032 (DIP & J-lead) EPM5064 EPM5128 EPM5128A EPS464 EPM5192 EPM5192A All MAX 7000 devices All Configuration EPROMs	Appropriate programming adapters	Appropriate programming adapters
LP5 or LP6 Logic Programmer card; PL-MPU programming unit (no PLAD3-12 adapter)	All Classic devices EPM5016 EPM5032 (SOIC) EPM5130 EPS448 EPB2001	PLAD3-12 adapter; Appropriate programming adapters	PLAD3-12 adapter; Appropriate programming adapters
LP5 or LP6 Logic Programmer card; PLE3-12A or PLE3-12 Programming unit	EPM5032 (DIP & J-lead) EPM5064 EPM5128 EPM5128A EPS464 EPM5192 EPM5192A All MAX 7000 devices All Configuration EPROMs	PL-MPU; Appropriate programming adapters	PL-MPU; Appropriate programming adapters

Notes:

CAE Software Support

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Introduction

Altera recognizes the importance of supporting other industry-standard design tools, and works closely with leading CAE software manufacturers to provide high-quality development support for Altera programmable logic devices. To ensure strategic partnerships with CAE tool manufacturers, Altera has established the ACCESS program. Through this program, Altera and its CAE partners work together to develop either direct support for Altera devices or seamless integration with Altera's MAX+PLUS II development software.

Table 1 summarizes each company's design entry, compilation/synthesis, and simulation/verification products that support Altera devices directly or provide an interface to MAX+PLUS II. As shown in Table 1, Altera also supplies design interface kits for several CAE tools. Altera recommends contacting CAE software manufacturers directly for details on product features, specific device support, and product availability. While Altera provides technical assistance to these companies, final responsibility for the quality and accuracy of these products rests with these manufacturers.

☞ Contact the Altera Applications Department by telephone at (800) 800-EPLD or by fax at (408) 954-0348 for the most up-to-date information on CAE support.

Table 1. Standard CAE Support for Altera Devices (Part 1 of 2)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Accel Technologies, Inc. TEL: (619) 554-1000 FAX: (619) 554-1019	Tango-PLD Tango-Schematic	✓ ✓	✓	✓ ✓
Acugen Software, Inc. TEL: (603) 881-8821 FAX: (603) 881-8906	AADELAY AAMAX ATGEN			✓ ✓ ✓
Aldec, Inc. TEL: (805) 499-6867 FAX: (805) 498-7945	Susie			✓
Cadence Design Systems, Inc. TEL: (408) 943-1234 FAX: (408) 943-0402	Composer *(1)* Concept *(1)* RapidSIM *(1)* SystemPGA Synergy *(2)* Verilog, Verilog-XL *(1)* Leapfrog *(2)*	✓ ✓ ✓ ✓ 	 ✓ ✓ 	 ✓ ✓ ✓
Data I/O Corp. TEL: (800) 247-5700 FAX: (206) 882-1043	ABEL-FPGA ABEL FutureNet	✓ ✓ ✓	✓ ✓	✓ ✓
Exemplar Logic, Inc. TEL: (510) 849-0937 FAX: (510) 849-9935	CORE Solution		✓	
Flynn Systems Corp. TEL: (603) 891-1111 FAX: (603) 891-1074	FS-High Density FS-PALibrary			✓ ✓
GenRad (U.K.) TEL: 329 822240 FAX: 329 822305	Hilo			✓
Intergraph Corp. TEL: (800) 239-4111 FAX: (303) 581-9972	ACEPlus AdvanSIM-1076 DLAB Synovation	✓	 ✓	 ✓ ✓
ISDATA GmbH (Germany) TEL: 0721/75 10 87 FAX: 0721/75 26 34	LOG/ic	✓	✓	✓
Logic Modeling Corp. TEL: (503) 690-6900 FAX: (503) 690-6906	SmartModels			✓

Table 1. Standard CAE Support for Altera Devices (Part 2 of 2)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Logical Devices, Inc. TEL: (800) 331-7766 FAX: (305) 428-1811	CUPL	✓	✓	✓
Mentor Graphics Corp. TEL: (503) 626-7000 FAX: (503) 685-1268	AutoLogic *(1)* Design Architect *(1)* PLD Synthesis QuickSim II *(1)*	✓ ✓	✓ ✓	 ✓
Minc Inc. TEL: (719) 590-1155 FAX: (719) 590-7330	PLDesigner-XL	✓	✓	✓
OrCAD Systems Corp. TEL: (503) 690-9881 FAX: (503) 690-9891	PLD MOD SDT VST	✓ ✓	✓	✓ ✓ ✓
Quad Design TEL: (800) 988-8250 FAX: (805) 988-8259	Motive			✓
Racal-Redac TEL: (201) 848-8000 FAX: (201) 848-7953	Cadat System Expert Visula	 ✓ ✓	 ✓	✓
Synopsys, Inc. TEL: (415) 962-5000 FAX: (415) 694-4249	FPGA Compiler *(1)* DC/Pro DC/Expert VSS Simulator		✓ ✓ ✓	 ✓
Viewlogic Systems, Inc. TEL: (800) 422-4600 FAX: (508) 480-0882	Viewdraw *(1)* ViewPLD Viewsim *(1)* VHDL Designer	✓ ✓ ✓	 ✓ ✓	 ✓

Notes:
(1) Interface design kits are available from Altera.
(2) Interface under development. Contact Altera Corporation for more information.

Notes:

Programming Hardware Manufacturers

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Introduction

Table 1 lists the manufacturers that offer programming hardware support for Altera devices. These companies are continually developing support for Altera programmable logic and configuration devices. Altera recommends contacting manufacturers directly for details on product features, specific device support, and product availability. While Altera provides technical assistance to these companies, final responsibility for the quality and accuracy of these products rests with these manufacturers.

Table 1. Programming Hardware Manufacturers (Part 1 of 2)

Manufacturer	Country	Telephone	Fax
Advantech	U.S.A.	(408) 245-6678	(408) 245-8268
Advin Systems, Inc.	U.S.A.	(408) 243-7000	(408) 736-2503
Ando Electric Co. Ltd.	Japan	3 3733 1161	3 3739 7310
Aval Data Corp.	Japan	3 5375 7321	3 5375 7717
B&C Microsystems, Inc.	U.S.A.	(408) 730-5511	(408) 730-5521
BP Microsystems	U.S.A.	(713) 688-4600	(713) 688-0920
Bytek Corporation	U.S.A.	(407) 994-3520	(407) 994-3615
Celectronic GmbH	Germany	30 4 13 6075	30 4 13 6078
Cornelius Consult	Germany	234 361206	234 356698
DATA I/O	U.S.A.	(206) 881-6444	(206) 882-1043
Elan Digital Systems Limited, U.K.	U.K.	(489) 579799	(489) 577516
ertec GmbH	Germany	9 131 75570	9 131 7557 10
HAMIS Haase, Menrad & Co. GmbH	Germany	531 70231	531 74020
ICE Technical Ltd.	U.K.	226 767 404	226 370 434
Instronic Peripherals & Systems	India	812 324967	812 324848
Leap Electronic Co., Ltd.	Taiwan	2 999 1860	2 999 0015
Link Computer Graphics, Inc.	U.S.A.	(201) 808-8990	(201) 808-8786
Logical Devices, Inc.	U.S.A.	(305) 428-6868	(305) 428-1811
Micro EDA	U.S.A.	(818) 912-7617	(818) 964-4989
MicroPross	France	20 47 9040	20 47 9369
Owen Electronic GmbH	Germany	6381 4202 0	6381 4202 85
Prologic Systems	U.S.A.	(303) 460-0103	(303) 469-5565
SMS Micro Systems	U.S.A.	(206) 883-8447	(206) 883-8601

Table 1. Programming Hardware Manufacturers (Part 2 of 2)

Manufacturer	Country	Telephone	Fax
Stag Microsystems	U.S.A.	(408) 988-1118	(408) 988-1232
Sunrise Electronic Inc.	U.S.A.	(818) 914-1926	(818) 914-1583
Sunshine Electronics Co., Ltd.	Taiwan	2 7633732	2 7654065
System General	U.S.A.	(408) 263-6667	(408) 262-9220
Tribal Microsystems/HiLo Systems	U.S.A.	(510) 623-8859	(510) 623-9925
Xeltek	U.S.A.	(408) 524-1935	(408) 295-7084

Contents

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Section 12 General Information

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Introduction

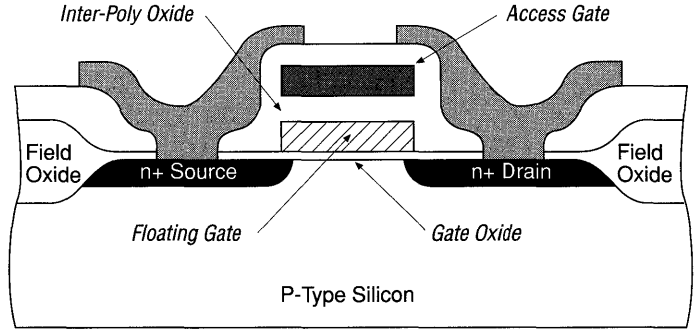
Altera's broad range of programmable logic devices incorporates three memory technologies: EPROM, EEPROM, and SRAM. To ensure the highest level of device performance and reliability, Altera maintains a comprehensive testing program that carefully monitors the factors affecting the basic programming elements of each device technology. Altera maintains rigorous quality standards both before a device technology is put into production and throughout the manufacturing process.

EPROM Technology

The EPROM transistor is a modified NMOS transistor in which the threshold voltage is easily changed between a low voltage (near V_{SS}) and a high voltage (greater than V_{CC}). The different threshold voltages represent the EPROM cell in the on and off states.

The EPROM transistor has a floating polysilicon gate between the access gate and the substrate, as shown in Figure 1. The floating gate is electrically isolated from the substrate by a thin-gate oxide that is approximately 200 Å thick, and from the access gate by a thicker dielectric inter-poly oxide that typically consists of oxides and/or nitrides.

Figure 1. EPROM Cell Construction



EPROM transistors are programmed to a high-threshold voltage with hot electron injection. When a programming voltage V_{PP} (normally 12.5 V) is applied to the access gate of an EPROM cell and a slightly lower voltage is applied to its drain, electrons flow from the source to the drain. As these electrons pick up kinetic energy, their path is altered by an electric field located between the access gate and substrate. This electric field is generated

by the potential difference between V_{PP} on the access gate and the slightly lower drain voltage. Electrons that achieve a kinetic energy of 3.2 eV or more, accelerate vertically toward the floating gate, pass through the gate oxide, and are trapped on the floating-gate electrode. These excess electrons create a net negative voltage on the floating gate that opposes the electrical field created by the positive voltage on the access gate. The result is a substantial increase in the threshold voltage required to change the EPROM cell into a conducting state. See Figure 2.

Figure 2. EPROM Cell Programming

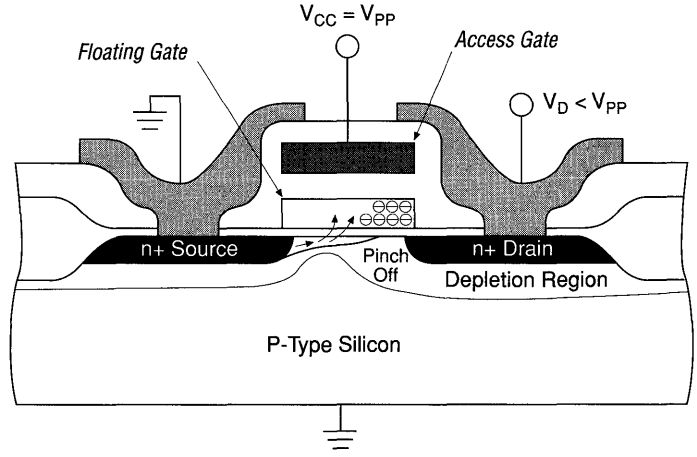
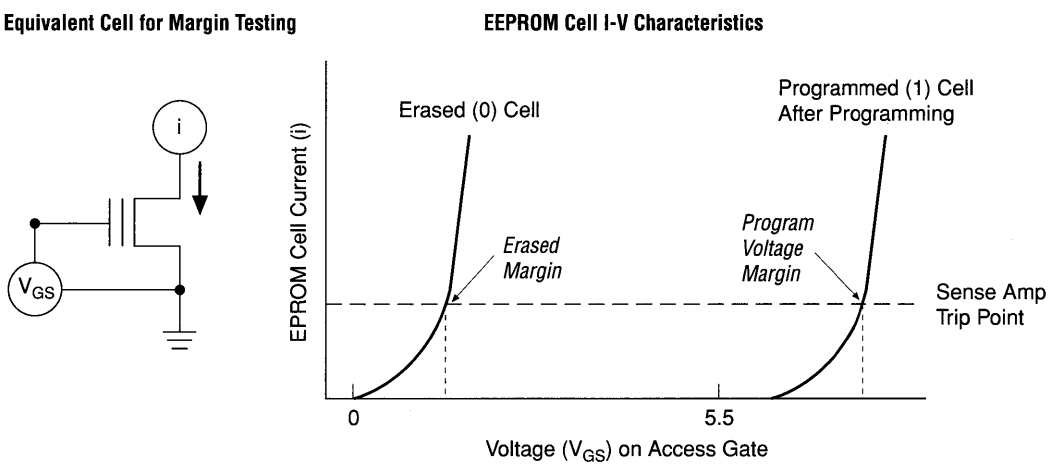


Figure 3 shows the current-voltage (I-V) relationships for programmed (high-threshold voltage) and erased (low-threshold voltage) EPROM cells. The programmed EPROM cell behaves as a transistor that is turned off, since source-drain current does not flow for access-gate voltages ranging from 0 to V_{CC}. In contrast, an erased cell produces source-drain current when its access gate is brought to approximately 1 V (on).

Programmed EPROM cells in the off state are erased by exposing the device to ultraviolet (UV) radiation with wavelengths of 2,540 Å. The excess electrons on the floating gate absorb radiant energy from this UV exposure, raising their energy levels above the 3.2-eV barrier. The increased energy levels enable the electrons to overcome the oxide-silicon potential barrier and migrate into the substrate, where they are neutralized.

Figure 3. Current vs. Voltage Relationships of Erased & Programmed EPROM Cells



EEPROM Technology

Like the EPROM transistor, the EEPROM transistor is an MOS transistor that is either on or off, depending on the threshold voltage. Unlike EPROM devices, however, EEPROM devices can be electrically erased. The EEPROM cell consists of a single floating polysilicon gate structure that is used to change the threshold voltage of the transistor. See Figure 4. The threshold voltage is changed when a tunneling mechanism traps an excess of electrons on the floating gate. Fowler-Nordheim tunneling occurs when the floating gate is raised to a high voltage (12 V to 13 V) via capacitive coupling to the N+ implant region. Once the electrons have been trapped on the floating gate, they present a negative shielding voltage and increase the threshold voltage of the transistor, making it impossible to turn the transistor on under normal operating voltages. This process allows the floating gate to act as an on/off switch for the read transistor.

The EEPROM cell is erased with the same tunneling mechanism. Since the electrons are removed from the floating gate, the gate has a net positive charge that allows the EEPROM transistor to be turned on or off, depending on the voltage on the control gate.

For a complete operational description of the EEPROM cell, see the *EPM7032 Process, Assembly, and Reliability Information Package*, available from Altera or from an Altera sales representative.

Figure 4. EEPROM Cell Construction

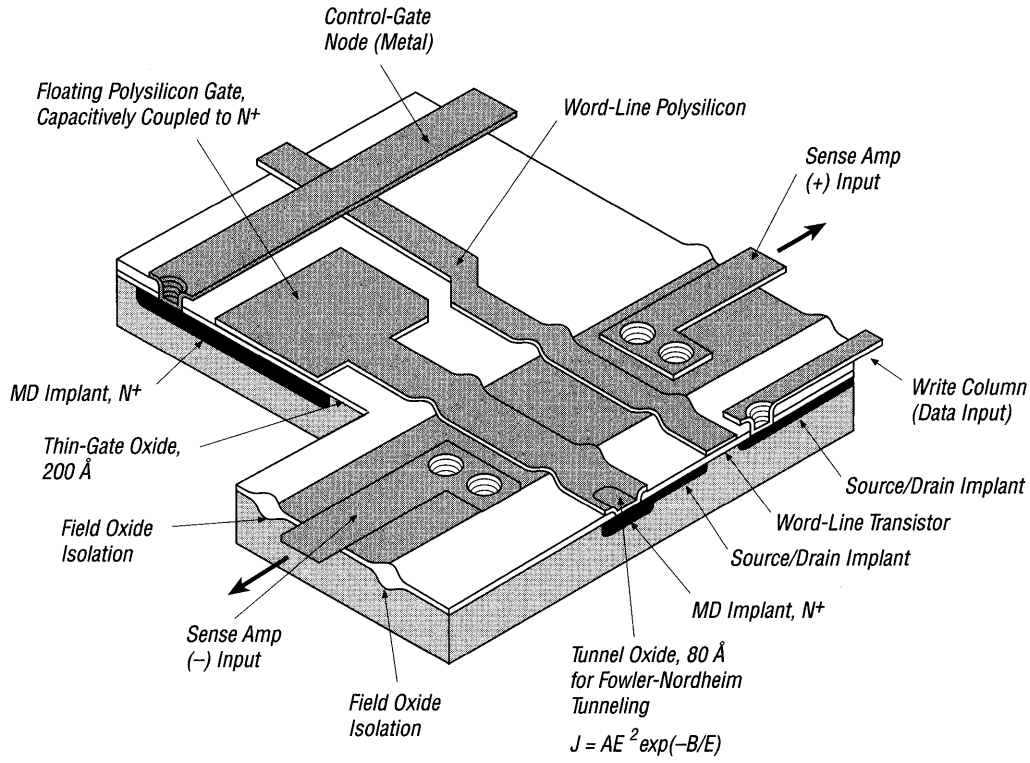
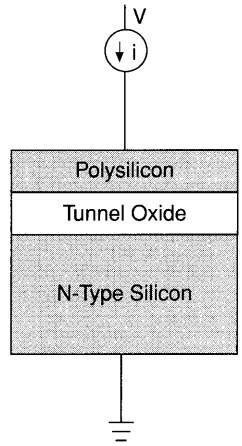


Figure 5 shows a 2-electrode structure in which one electrode is formed by polysilicon and another is formed by a heavily doped N-type silicon diffusion. These electrodes are separated by a tunnel oxide that is approximately 80 Å thick. When typical operating voltages of 5 V or less are applied across the tunnel oxide, it acts as a dielectric and does not conduct electricity. When 12 V to 14 V are applied, however, electrons tunnel through the oxide. This process is characterized by an extremely small tunneling current (less than 10^{-20} A) at typical operating voltages of 5 V or less. At higher voltages that are used to erase or program the cell (i.e., charge or discharge the floating gate), the exponential rise in current produces approximately 1 µA of current flow through the tunnel oxide. Depending on the voltage's polarity, this current is sufficient to charge or discharge the cell within a few milliseconds.

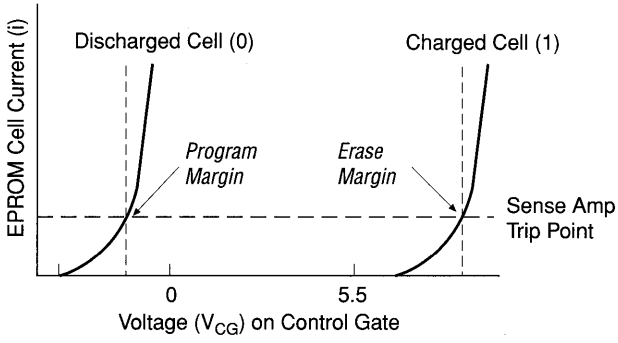
Figure 5. EEPROM Floating-Gate Electrode, Tunnel Oxide & Heavily Doped Diffusion Electrode



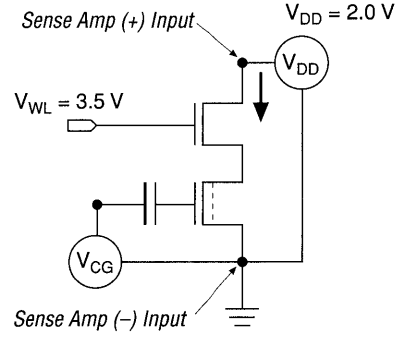
The I-V relationships for programmed and erased EEPROM cells are similar to those of EPROM cells (see Figure 6). Unlike the EPROM cell, however, the threshold voltage of a discharged EEPROM cell is negative (less than 0 V) because electrons are removed from the floating gate. Electron removal gives the floating gate a net positive charge.

Figure 6. Current vs. Voltage Relationships of an Erased & of a Programmed EEPROM Cell

EEPROM Cell I-V Characteristics



Equivalent Circuit for Margin Testing

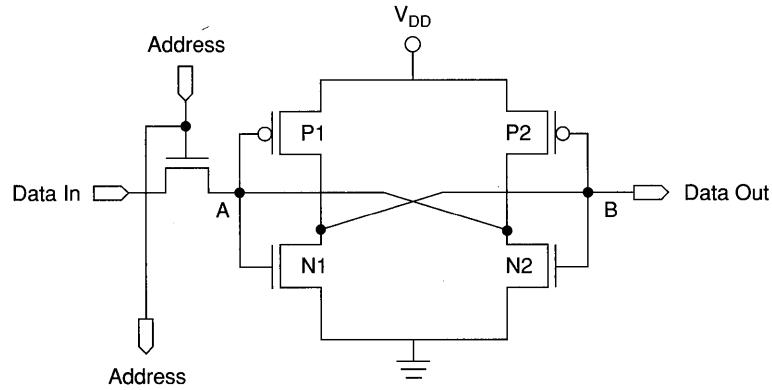


SRAM Technology

Altera's FLEX 8000 programmable logic devices use static RAM (SRAM) memory cells as the basic programming element. Figure 7 shows the standard CMOS five-transistor cell that comprises the memory element.

The process used to manufacture FLEX 8000 devices is a subset of the EEPROM fabrication process. Therefore, all process development and reliability enhancements used to manufacture EEPROM devices also apply to SRAM-based devices.

Figure 7. SRAM Memory Cell



Failure Mechanisms & Reliability Screens

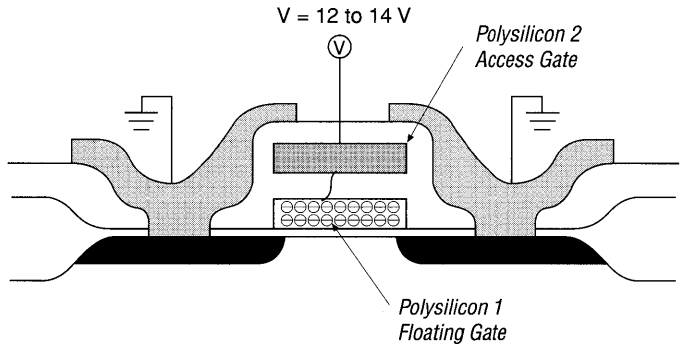
Both EPROM and EEPROM cells function through a change in threshold voltage. Reliable EPROM and EEPROM cells maintain their charge by holding excess electrons placed on the floating gate over the expected life of the device, thus maintaining a high-threshold voltage (off state). Discharged cells maintain a low-threshold voltage (on state) in which no electrons move onto the floating gate over the life of the device.

Voltage Margin Testing

Voltage margin testing is used to measure the threshold voltage of EPROM or EEPROM cells. This testing is essential for monitoring the programmability and erasability of a device, as well as its long-term stability after programming or erasure. Altera devices incorporate special test-mode circuitry that enables the threshold voltage (i.e., voltage margin) of each EPROM or EEPROM cell on a device to be measured. (Since SRAM cells are configured at system power-up by a Configuration EPROM or an external host, voltage margin testing does not apply.) This circuitry is used to measure the programmability of all devices and to implement screens that detect charge loss from programmed devices. During this screening process, any degradation of the threshold voltage is measured for each cell as a function of time, temperature, and voltage.

The first voltage margin test is performed during wafer sort. Wafer testing at Altera consists of multiple wafer sort operations. At Wafer Sort 1, devices are tested for combinatorial and registered logic functionality and cell programming to ensure that all EPROM or EEPROM cells are fully programmable. Each cell is "voltage-margined" to ensure that its threshold voltage exceeds 5.5 V, which is the maximum V_{CC} value encountered during normal operation. After this process, each cell's access gate is raised to a high voltage (12 V) to pull electrons off the floating gate through any defects in the inter-poly oxide between the floating and access gates. See Figure 8.

Figure 8. DC Erase Stress for an EPROM Cell

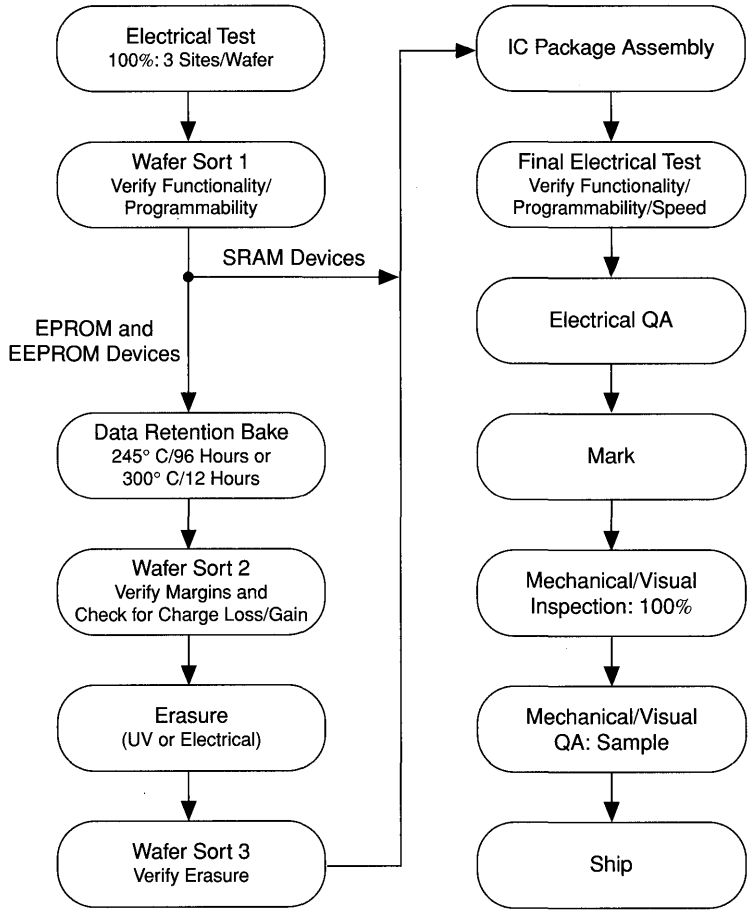


As shown in Figures 1 and 2, the floating gate is completely surrounded by oxide. Any defect in the oxide or contamination by mobile ionic charges such as Na^+ can cause electrons to migrate off the gate. This "cell stress," or DC erase stress, lowers the threshold voltage of any cell with a defective oxide. A cell's base threshold voltage is determined by performing a voltage margin test immediately after programming and before the DC erase stress. After the DC erase stress is applied, each cell's voltage margin is tested again. If any cell shows a significant reduction in threshold voltage, the device is rejected from the manufacturing flow.

Thermally activated charge-loss mechanisms are also reliability hazards. To detect material defects, every device is baked at a high temperature with all cells in the charged state after Wafer Sort 1. Depending on the device, this bake is performed at 300° C for 12 hours or 245° C for 96 hours. After the bake, the threshold voltage for each cell is remeasured during Wafer Sort 2 and compared to its pre-bake values. Devices with cells that exhibit a reduced threshold voltage are rejected from the manufacturing flow. Additional margin testing is performed on packaged devices after assembly.

Figure 9 shows a typical wafer-sort process.

Figure 9. Wafer-Sort, Assembly & Final Test Flow for Altera Devices



Reliability Screening

The various wafer-sort operations also include reliability screening. Voltage and temperature-accelerated stresses are applied to activate potential charge-loss failure mechanisms within the device. Reliability testing is an integral part of the standard production test flow for all Altera devices. To ensure the effectiveness of Altera's testing program, test results are continuously verified.

After the IC package assembly operation, during which the individual dice are removed from the wafers and placed into packages, each device is tested, and the results are compared against data-sheet specifications. This test is performed at elevated temperatures to ensure that specifications are

met for the maximum guaranteed operating temperature: 70° C for commercial, 85° C for industrial, and 125° C for military devices.

Altera Reliability Program

Altera's integrated circuits must meet rigorous reliability standards. Altera uses a two-phase approach to ensure a consistent high level of reliability from its manufacturing processes and devices:

- ❑ New product/production process qualification
- ❑ Reliability monitoring

New Product/Production Process Qualification

Altera performs rigorous reliability tests on new devices and subjects new or substantially modified processes to a rigorous series of reliability tests before production. Tests are perfomed to Altera, industry, and MIL-STD-883 (rev. C) standards. This qualification procedure ensures that all manufacturing processes and products meet Altera's minimum reliability requirements. Tables 1 and 2 show the reliability tests for hermetic and plastic package devices, respectively.

Table 1. Hermetic Package Qualification Requirements

Sequence	Test	MIL-STD-883 (Rev. C) Method	Goal LTPD *Note (1)*	Sample Size	Rejects Allowed	Assembly Plant	New Leadframe	New Package	New Lead Finish	Wafer Fabrication Process	Full Qualification
	ESD sensitivity	3015.7	–	4	0					✓	✓
	Latch-up		–	5	0					✓	✓
	Retention bake		5	77	1					✓	✓
B2	Mark permanency	2015	–	4	0	✓	✓		✓		✓
B3	Solderability	2003	10	22	0	✓	✓	✓	✓		✓
B5	Bond strength	2011	15	15	0	✓	✓	✓			✓
C1	Lifetest 1,000/2,000 hours	1005 (125° C)	5	77	1					✓	✓
D1	Physical dimensions	2016	15	0	0	✓	✓	✓			✓
D2	Lead fatigue	2004 B2	15	15	0	✓	✓	✓	✓		✓
	Fine & gross leak	1014									
D3	Thermal shock	1011.7 B	5	77	1	✓	✓	✓		✓	✓
	Temperature cycle	1010.7 C									
	Moisture resistance										
	Fine & gross leak	1014									
	External visual	1004									
	End point electrical	Altera									
D4	Mechanical shock	2002 B	15	15	0	✓	✓		✓		✓
	Vibration variable	2007 A									
	Frequency										
	Constant acceleration	2001 E (30 kg)									
	Fine & gross leak	1014									
	External visual										
	End point electrical	Altera									
D4	Internal water vapor	1018 (5000 ppm maximum)	–	3/5	0/1	✓	✓	✓	✓	✓	✓
D8	Lid torque	2024	–	15	0	✓	✓	✓	✓		✓

Note:
(1) LTPD: Lot Tolerance Percent Defective

Table 2. Plastic Package Qualification Requirements

Sequence		Test	MIL-STD-883 (Rev. C) Method	Requirements									
				Goal LTPD Note (1)	Sample Size	Rejects Allowed	Assembly Plant	New Package	New Leadframe	New Lead Finish	Wafer Fabrication Process	New Molding Compound	Full Qualification
B1	Physical dimension	2016	–	2	0	✓	✓	✓			✓	✓
B2	Mark permanency	2015	–	4	0	✓	✓		✓		✓	✓
B3	Solderability	2003	10	22	0	✓	✓	✓	✓		✓	✓
B4	Autoclave 121° C/100% rh 15 psi, unbiased: 168 hours		5	77	1	✓	✓	✓	✓	✓	✓	✓
B5	Bond strength	2011	15	15	0	✓	✓	✓			✓	✓
C1	Lifetest 1,000/2,000 hours	1005 (125° C)	5	77	1	✓	✓			✓	✓	✓
C2	85/85 with bias: 1,000 hours	85° C/85% relative humidity	5	77	1					✓	✓	✓
D1	Lead integrity	2004.5	15	15	0	✓	✓	✓			✓	✓
D2	Resistance to solder heat: 260° C for 10 seconds		10	22	0	✓	✓	✓	✓		✓	✓
D3	Thermal shock –55° C to +125° C, 100 cycles	1011.7 B	5	77	1	✓	✓	✓		✓	✓	✓
D4	Temperature cycle –65° C to +125° C, 1,000 cycles	1010.7 C	5	77	1	✓	✓	✓	✓	✓	✓	✓

Note:
(1) LTPD: Lot Tolerance Percent Defective

Reliability Monitoring

Once a device or process is qualified for production, Altera routinely conducts reliability tests throughout its manufacturing life cycle. Reliability tests are conducted under the careful supervision of trained reliability engineers and technicians, and are perfomed to Altera, industry, and MIL-STD-883 (rev. C) standards. Table 3 describes the reliability tests and shows how often they are performed.

Table 3. Reliability Test Program

Test Type	MIL-STD-883C Method/Condition	Test Frequency	Plastic Package	Hermetic Package
Lifetest	2,000 hours at 125° C at rated voltages	1 time per month per process	✓	✓
Data retention bake	1,000 hours (minimum) at 170° C	1 time per month per process	✓	✓
Temperature cycling	1,000 cycles 1010.7, condition C –55° C to +150° C (plastic) –65° C to +150° C (hermetic)	1 time per month per process	✓	✓
Thermal shock	1011.7, condition B –55° C to +125° C	2 times per year per package	✓	✓
Constant acceleration	2001E, 30,000G force, Y1 only	2 times per year per package	–	✓
Mechanical shock	2002B, 1500G force, 0.5-ms pulse peak	2 times per year per package	–	✓
Lid torque	2024	1 time per month per package	–	✓
Lead integrity	2004 B2	2 times per year per package	✓	✓
Internal water vapor content	1018, 5000 ppm maximum at 100° C	1 time per month per package	–	✓
Temperature/humidity/bias	85° C/85% relative humidity, 5 V, 1,000 hours minimum	1 time per month per package	✓	–
Autoclave (pressure cooker)	121° C, 2 atm, 96 hours minimum	1 time per month per package	✓	–

Altera's Reliability Engineering Lab uses the latest equipment for reliability testing, allowing Altera engineers and technicians to perform accurate reliability qualifications and monitoring on a timely basis. This equipment provides engineers and technicians with the control and precision required to perform rigorous semiconductor stress tests.

Results from Altera's reliability monitoring program are published several times each year in the *Altera Reliability Report*. This report summarizes the test results for all Altera devices over a 15-month period. It includes detailed descriptions of the reliability tests, their implementation, and useful information about semiconductor reliability. For a copy of the *Altera Reliability Report*, contact the Altera Literature Department at (408) 894-7134.

QFP Carrier & Development Socket

August 1993, ver. 5 Data Sheet

Features

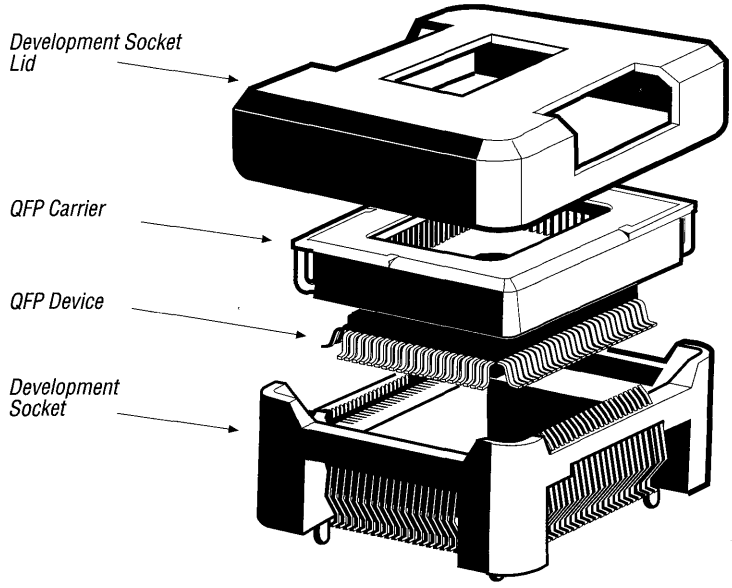
- Quad flat pack (QFP) carriers protect fragile leads on Altera QFP devices.
- Development socket allows on-board electrical and mechanical prototype testing with QFP packages.
- QFP carriers eliminate damage to leads caused by device handling.
- Carriers and sockets are available in 100-, 160-, and 208-pin counts.
- Development socket footprints match QFP footprints, making migration to production easier.

General Description

The Altera QFP carrier and development socket protect the fragile leads on QFP devices during shipping and throughout the development cycle. The socket has the same lead footprint as the device, so it can be used both during mechanical and electrical prototyping.

The material used in the carrier and development socket helps prevent electrostatic damage to the devices while providing excellent AC circuit performance. QFP carriers and development sockets are currently available for 100-, 160-, and 208-pin QFP packages. Figure 1 shows the 100-pin QFP carrier and development socket.

Figure 1. 100-Pin QFP Carrier & Development Socket



QFP Carrier

The carrier is a static-dissipative, molded plastic shell that holds the device and leads in a secure frame to prevent mechanical damage. The device is held in the carrier by recessed plastic clips (2 clips on the 100-pin carrier and 4 clips on the 160-pin and 208-pin carriers).

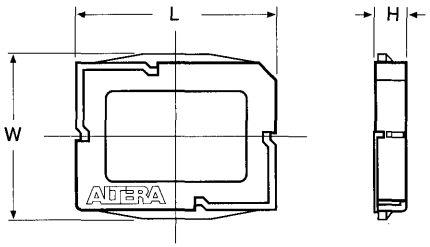
All MAX 5000 and MAX 7000 QFP devices with 100 or more pins are shipped from the factory in carriers, thus eliminating the need to handle the delicate device leads. The carriers are packaged either in anti-static rails or strip packs. Devices can be programmed and erased while in the carrier. EPROM-based QFP devices are erased with a UV lamp; EEPROM-based QFP devices are erased in the programming adapter. Figure 2 shows the dimensions of the QFP carriers.

☞ QFP devices without protective carriers should be handled with a vacuum wand at an electrostatically protected workplace to reduce the possibility of mechanical or electrical device damage.

Figure 2. QFP Carrier Dimensions

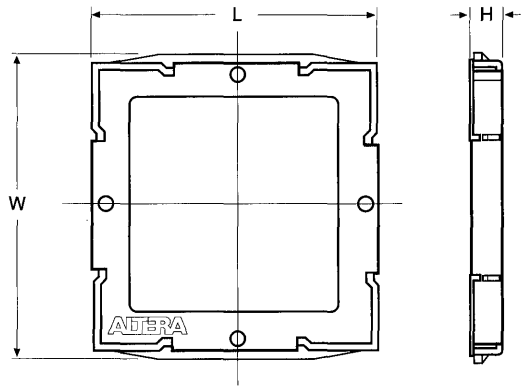
Dimensions are shown in millimeters.

100-Pin QFP Carrier



Pin Count	L	W	H
100	25.2	21.2	4.2
160	33.2	35.2	5.1
208	33.2	35.2	5.1

160- and 208-Pin QFP Carrier

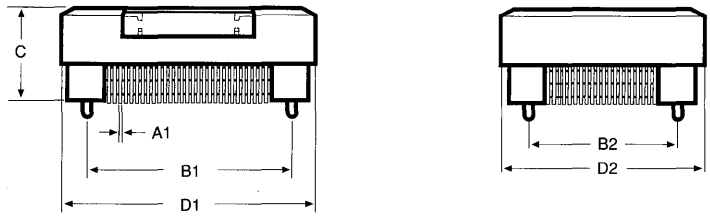


QFP Development Socket

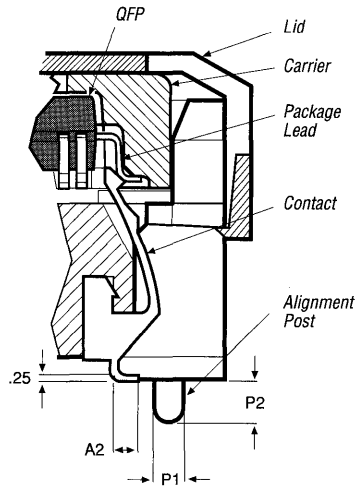
The QFP development socket footprint is compatible with the lead footprint of the QFP device. It ensures the device's electrical connection to the printed circuit board and provides excellent AC circuit performance: low noise, low capacitance, and low inductance. (A device mounted directly on the printed circuit board will provide better interconnect capacitance and inductance than a device loaded into the carrier/socket.) See Figure 3.

Figure 3. QFP Development Socket Dimensions

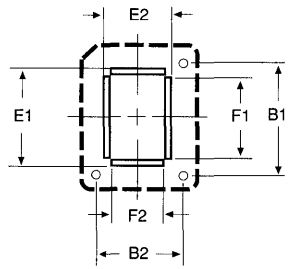
Dimensions are shown in millimeters.



Contact & Lid Detail



Board Layout



Pin Count	A1	A2	B1	B2	C	D1	D2	E1	E2	F1	F2	P1	P2
100	0.20	0.93	25.0	19.0	12.0	31.51	25.54	23.30	17.30	30 Pads @ 0.65	20 Pads @ 0.65	1.0	1.5
160	0.20	0.93	33.8	33.8	12.8	39.60	39.60	32.08	32.08	40 Pads @ 0.65	40 Pads @ 0.65	1.0	1.5
208	0.20	0.93	33.8	33.8	12.8	39.60	39.60	31.68	31.68	52 Pads @ 0.50	52 Pads @ 0.50	1.0	1.5
Tolerance	±0.02	±0.12	±0.12	±0.12	±0.40	±0.20	±0.20	±0.12	±0.12			±0.03	±0.12

☞ To ensure correct board layout, pad sizes must be compatible with the development socket and the QFP device leads.

The development socket withstands the temperatures required by reflow technology. With the appropriate solder mask, multiple development sockets can be closely spaced on the board. Three alignment posts ensure correct orientation and provide sufficient registration for reflow soldering. When other components must be placed near the development socket, the designer must ensure that component leads do not conflict with the outline of the development socket.

The QFP carrier is held in the development socket by the socket lid, which braces the carrier against the electrical contacts in the socket. These contacts connect the device leads to the development socket, ensuring a positive electrical connection that is not susceptible to mechanical interruption caused by jarring or impulsive shocks. The carrier design ensures that the pressure of the socket contacts does not significantly affect the coplanarity of the device leads. This carrier/socket combination allows the designer to perform mechanical analysis during the functional prototyping cycle.

Altera also provides a tool to extract the QFP device from the carrier. Although it is possible to extract a QFP device from the carrier without the tool, Altera recommends using the tool for QFP devices with 160 or more pins. Two extraction tools are available: one for 100-pin QFPs and one for 160- and 208-pin QFPs. See "Extracting a Device with the Extraction Tool" later in this data sheet for complete details.

Step-by-Step Instructions

The following step-by-step instructions describe how to:

1. Insert the QFP carrier into the development socket
2. Remove the QFP carrier from the development socket
3. Program a device in the QFP carrier
4. Extract a device from the QFP carrier
5. Extract a device from the QFP carrier with the extraction tool
6. Insert a device into the QFP carrier

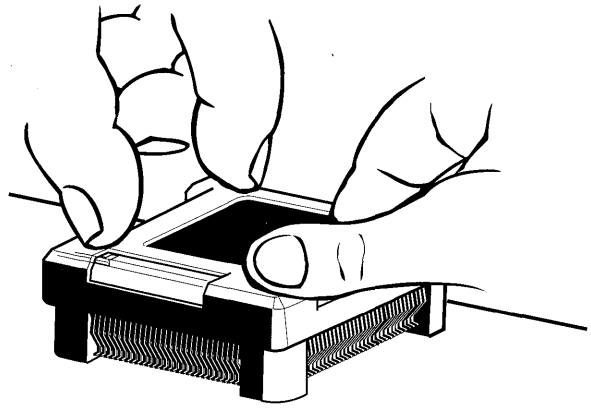
☞ The device should be removed from the QFP carrier only *after* it has been programmed and is ready to be soldered onto the board.

Inserting the QFP Carrier into the Development Socket

To insert the QFP carrier into the development socket:

1. Align the QFP carrier on the development socket by matching the beveled corner of the carrier to the beveled corner of the socket and aligning the alignment dots.
2. Place the socket lid over the socket *and press down firmly on all four corners of the lid.* Clicking sounds will be clearly audible. See Figure 4.

Figure 4. Inserting the QFP Carrier into the Development Socket



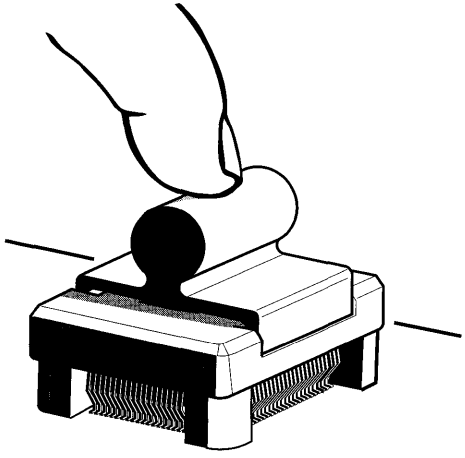
Removing the QFP Carrier from the Development Socket

To remove the QFP carrier from the development socket:

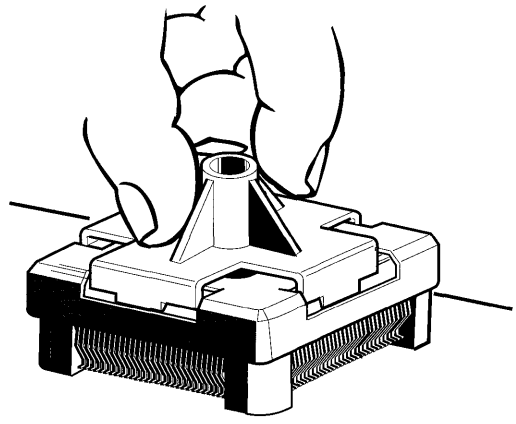
1. Place the removal tool over the QFP socket lid, as shown in Figure 5.
2. Gently press down, making sure that the edges of the tool fit into the slots on the top of the lid. Clicking sounds will be clearly audible.
3. While maintaining pressure, lift the lid and removal tool together.
4. Remove the carrier.

Figure 5. Removing the QFP Carrier from the Development Socket

100-Pin Carrier



160- and 208-Pin Carrier



Programming a Device in the QFP Carrier

QFP devices that are shipped in the protective QFP carriers are ready to be programmed with the Altera Master Programming Unit (MPU) and the appropriate PLMQ-type programming adapter. With Altera programming software and hardware, test vectors can be directly applied to the device for programming verification and functional testing. Devices in QFP packages can also be programmed with industry-standard programming hardware from other manufacturers (e.g., Data I/O).

To program a device in the QFP carrier:

1. Place the QFP carrier with the device into the programming adapter, making sure that carrier and adapter are aligned correctly.
2. Close the retaining latch by pressing the latch against the socket. A clicking sound is clearly audible as the latch fastens over the socket.

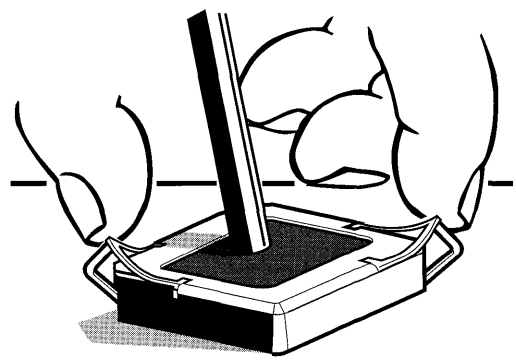
☞ The retaining latch on the clamshell-style programming adapter socket ensures good electrical contact between the device leads and the socket. The retaining latch must be shut after the QFP carrier is placed into the programming adapter; otherwise, programming problems may occur.

Extracting a Device from the QFP Carrier

Altera recommends using the extraction tool to extract QFP devices with more than 160 pins from the QFP carriers. To extract a device from the QFP carrier:

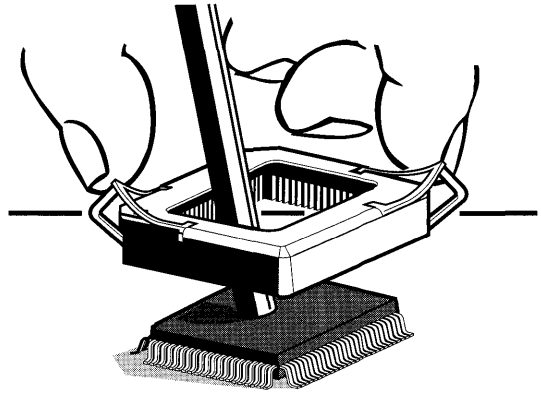
1. Place the QFP carrier against a flat surface.
2. Without applying pressure, hold down the device with the blunt end of a pencil or another similar tool.
3. Bend up the yellow retaining clips located on diagonal corners of the QFP carrier. See Figure 6.

Figure 6. Bending the Retaining Clips to Extract the QFP Device from the QFP Carrier



4. Lift the QFP carrier straight up. See Figure 7.

Figure 7. Lifting the QFP Carrier to Extract the QFP Device



Extracting a Device from the QFP Carrier with the Extraction Tool

The QFP carrier extraction tool has a floating platform set into the base of the tool. The QFP device rests on this platform. The lever is connected to a shaft whose head pushes the device out of the carrier. The shaft is mounted on a vertical support that can be rotated to permit easy insertion and removal of the device. The shaft mount incorporates a carrier holder that secures the carrier after it has been extracted from the QFP device. See Figure 8.

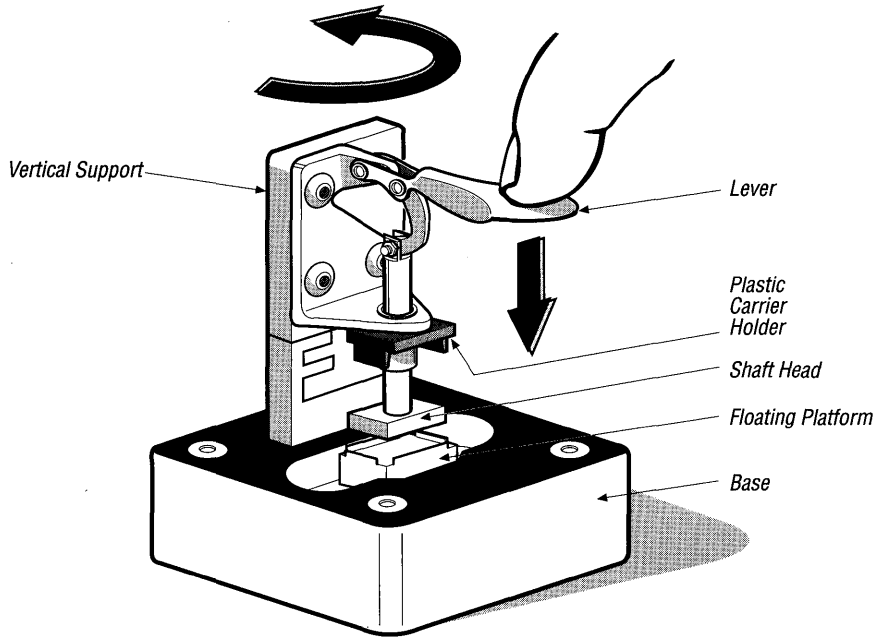
To extract a QFP device from the carrier:

1. Place the tool on a flat surface with the lever facing you.
2. Rotate the vertical support so that it does not block access to the device platform.
3. Place the QFP device in the carrier on the floating platform (the Altera logo on the carrier should be located in the upper right hand corner). The carrier will not fit into the tool if it is inserted improperly.
4. Rotate the vertical support back over the QFP until the shaft head is positioned directly over the QFP in the carrier. A click is clearly audible.
5. Press down the lever so that the shaft head pushes the QFP out of the carrier. *Keep the lever down.*
6. Pull the carrier straight up until it snaps onto the black plastic carrier holder.
7. Pull the lever up to disengage the shaft head from the QFP device.
8. Rotate the vertical support away from the base.

9. With a vacuum wand or another handling device, pick up the device. *Do not handle the device with your fingers to avoid damage to the leads.*

☞ A QFP device should not be re-inserted into the QFP carrier with the extraction tool.

Figure 8. Extracting the QFP Device from the Carrier with the Extraction Tool



Inserting a Device into the QFP Carrier

To insert a QFP device into the QFP carrier:

1. Hold the carrier bottom side up.
2. With thumb and forefinger, bend the yellow retaining clips outward.
3. Place the device into the carrier so that the device leads fit into the molded channels. The beveled corner of the device must be aligned with the beveled corner of the QFP carrier. When the device is securely seated in the carrier, the clips will snap back over the corners of the device and hold it in place.

The yellow plastic clips hold the device securely in place without hindering access to the leads. The open carrier top allows the EPROM-based QFP device to be placed under a UV lamp for device erasure.

☞ Altera recommends that the QFP device not be re-inserted into the QFP carrier once it has been removed.

Ordering Information

QFP carriers and development sockets are rated from –65° C to 155° C, and are qualified to handle commercial, industrial, and military operating temperatures. For up-to-date information on available QFP carriers and development sockets, refer to *Ordering Information* in this data book.

Notes:

Altera Device Package Outlines

August 1993, ver. 4 | Data Sheet

Introduction

This data sheet provides package outlines for all Altera devices. Table 1 shows the type of packages, lead materials, and lead finishes available.

Table 1. Altera Device Packages

Package Type	Package Code	Lead Material	Lead Finish
Ceramic dual in-line	D	Alloy 42	Solder dip
Plastic dual in-line	P	Copper	Solder dip (60/40)
Ceramic J-lead	J	Alloy 42	Solder dip (60/40)
Plastic J-lead	L	Copper	Solder plate (60/40)
Ceramic pin-grid array	G	Alloy 42	Gold over nickel plate
Plastic small-outline IC	S	Copper	Solder plate (80/20)
Ceramic quad flat pack	W	Alloy 42	Matte tin plate
Plastic quad flat pack	Q	Copper	Solder plate (80/20)
Metal quad flat pack	M	Copper	Solder plate (80/20)
Plastic thin quad flat pack	T	Copper	Solder plate (80/20)
Power quad flat pack	R	Copper	Solder plate (80/20)

Package outlines are listed here in ascending pin count order. Maximum lead coplanarity is 0.004 in. (0.10 mm). For information on device package ordering codes, see *Ordering Information* in this data book. Package outline dimensions are shown in the following formats:

$$\frac{\textit{min. inches (min. millimeters)}}{\textit{max. inches (max. millimeters)}}$$

or:

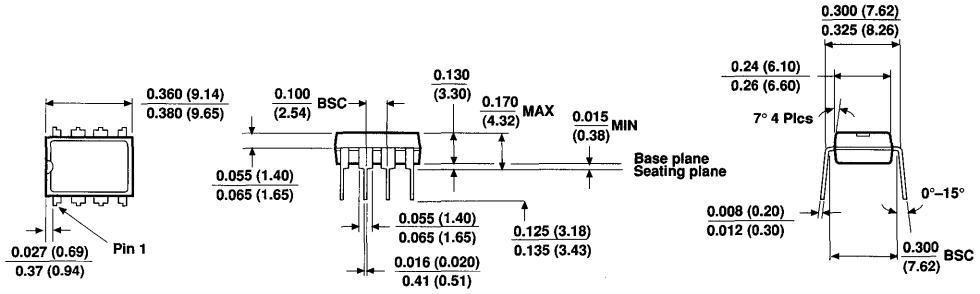
$$\frac{\textit{nominal inches} \pm \textit{tolerance}}{\textit{(nominal millimeters} \pm \textit{tolerance)}}$$

or:

$$\frac{\textit{inches}}{\textit{(millimeters)}}\ \text{BSC, Min., Max., Ref.}$$

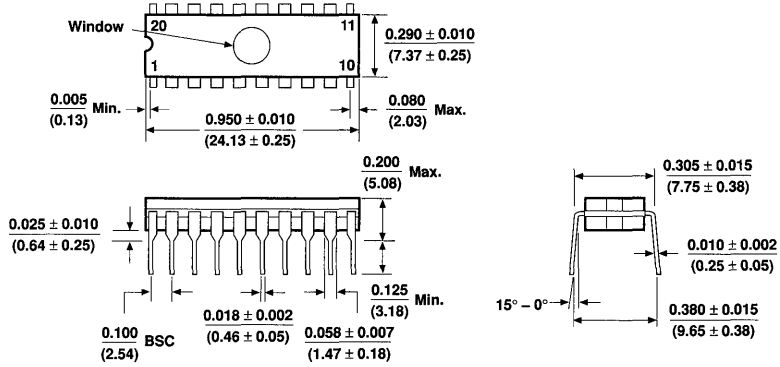
20-Pin Plastic Dual In-Line Package (PDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



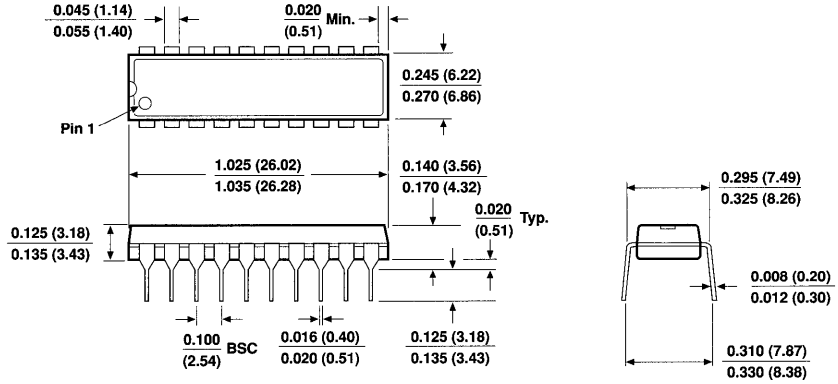
20-Pin Ceramic Dual In-Line Package (CerDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



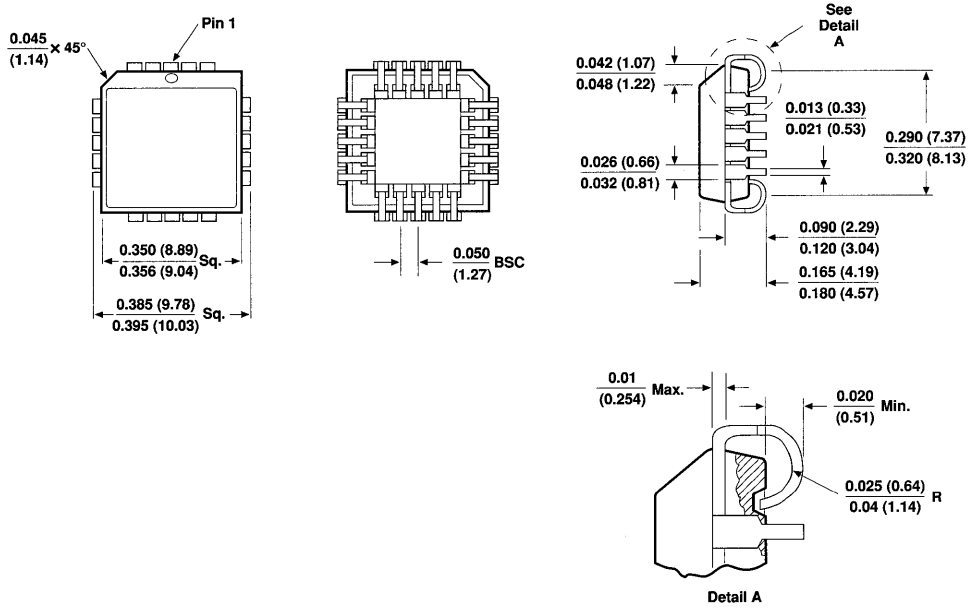
20-Pin Plastic Dual In-Line Package (PDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



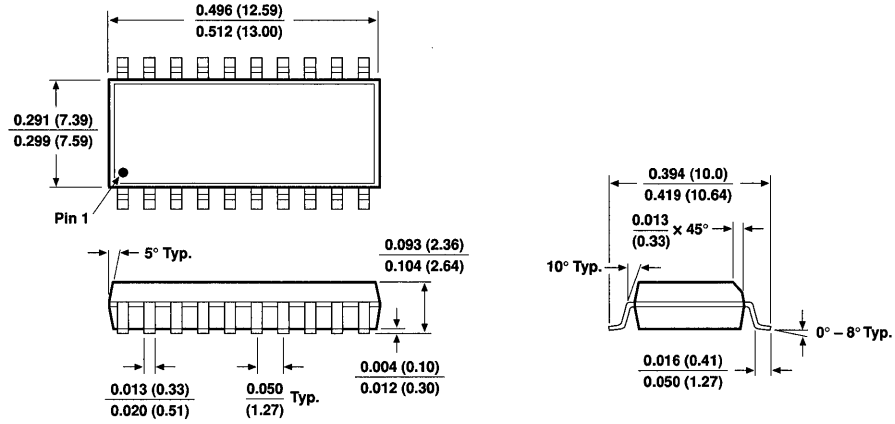
20-Pin Plastic J-Lead Chip Carrier (PLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



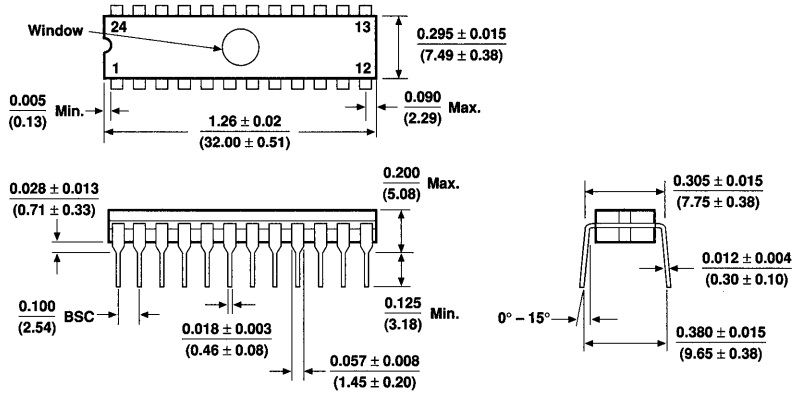
20-Pin Plastic Small-Outline Integrated Circuit (SOIC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



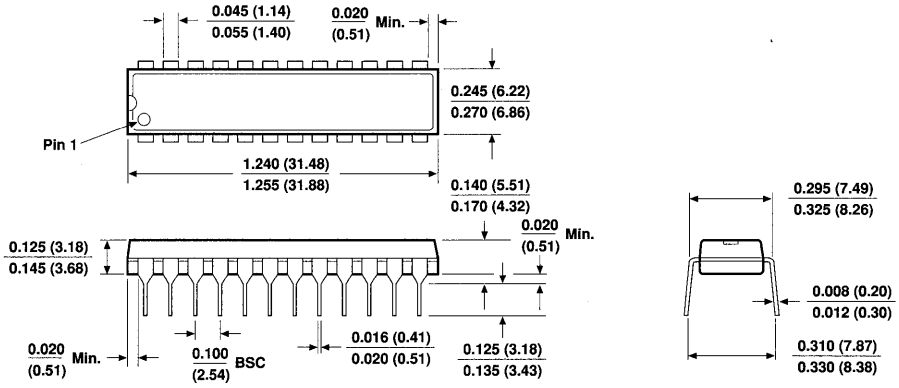
24-Pin Ceramic Dual In-Line Package (CerDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



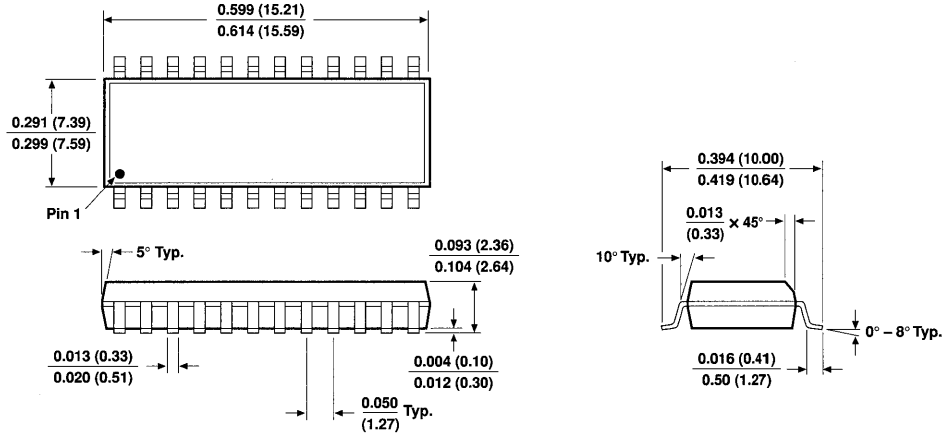
24-Pin Plastic Dual In-Line Package (PDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



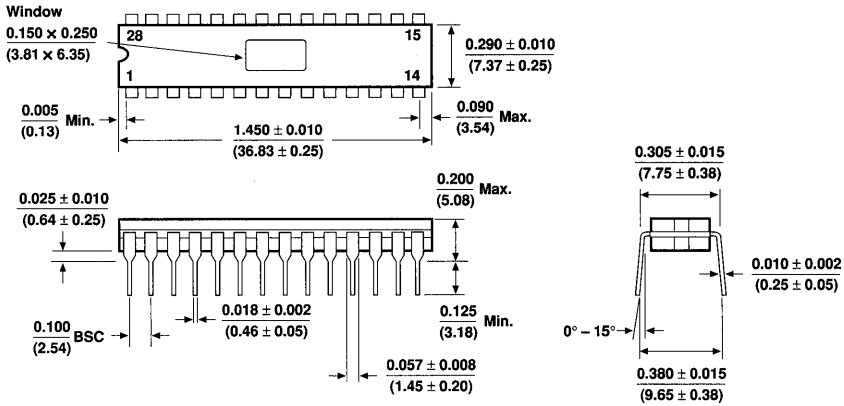
24-Pin Plastic Small-Outline Integrated Circuit (SOIC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



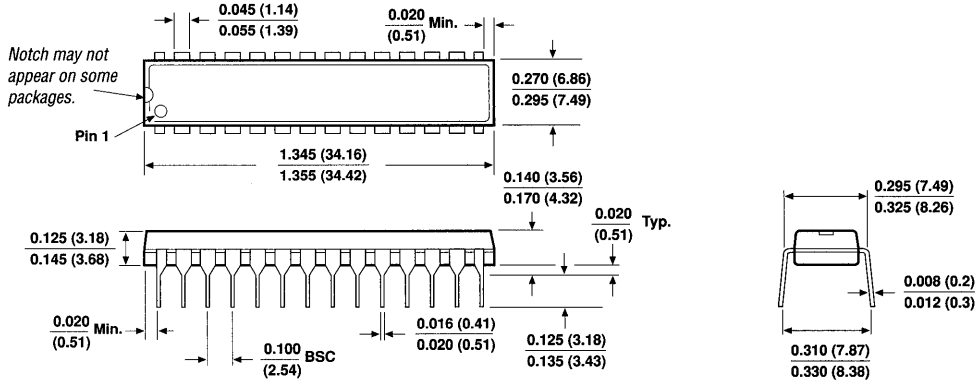
28-Pin Ceramic Dual In-Line Package (CerDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



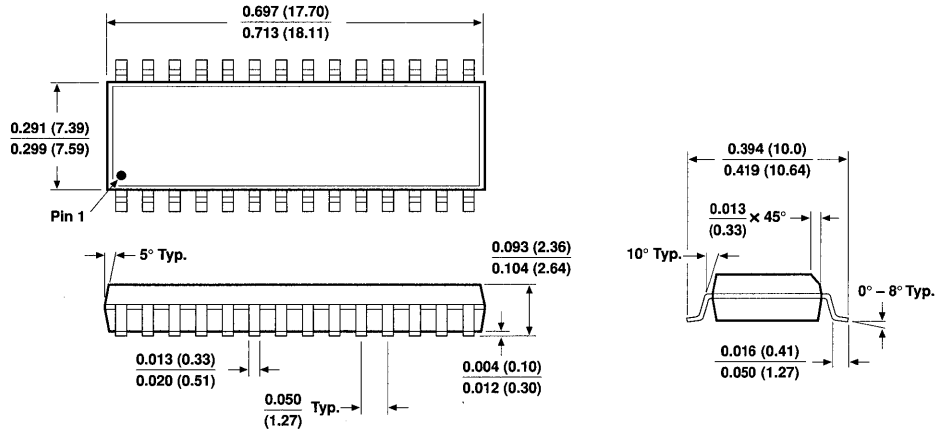
28-Pin Plastic Dual In-Line Package (PDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



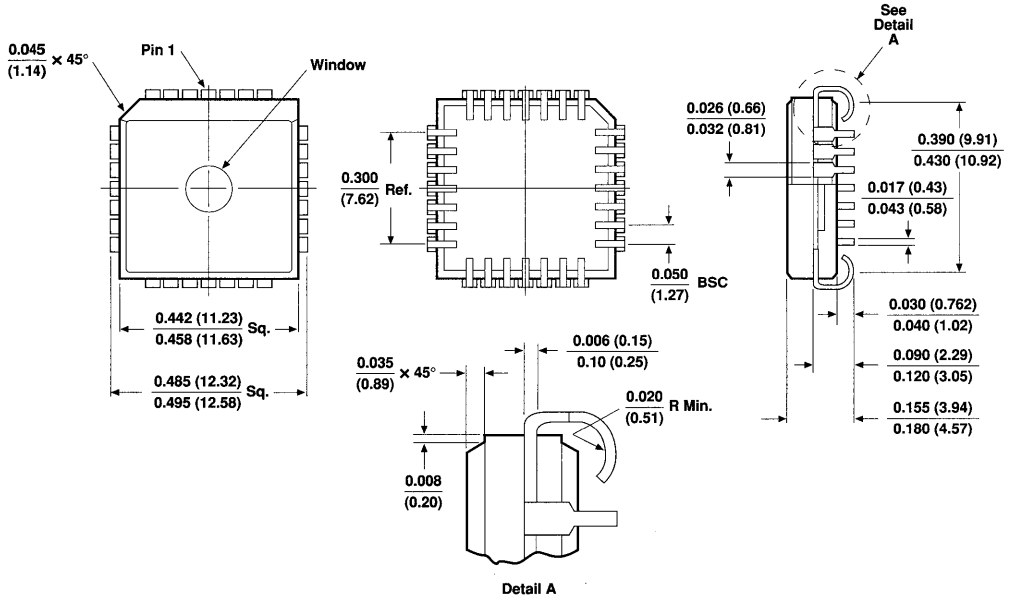
28-Pin Plastic Small-Outline Integrated Circuit (SOIC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



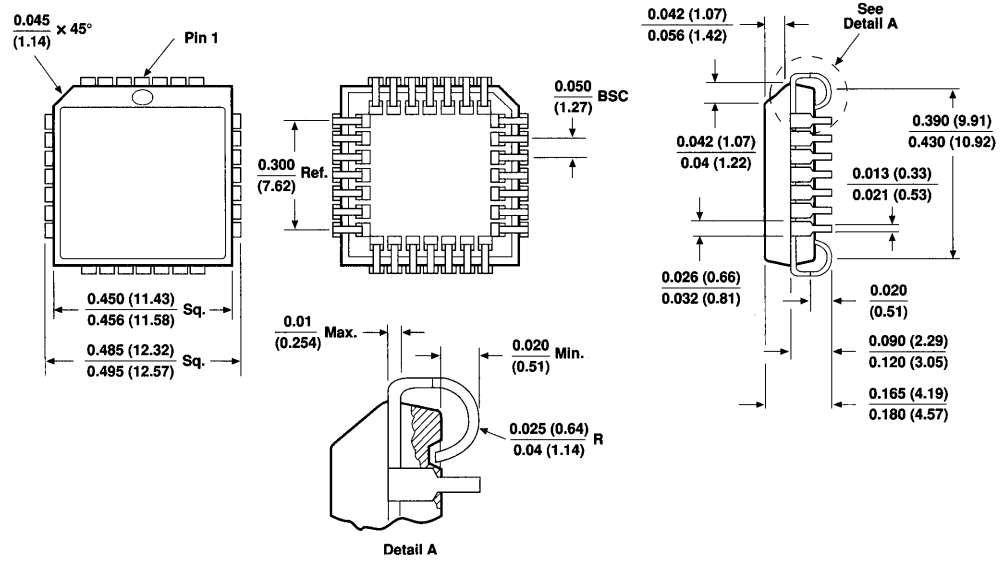
28-Pin Ceramic J-Lead Chip Carrier (JLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in Altera Military Product Drawing 02D-00194.



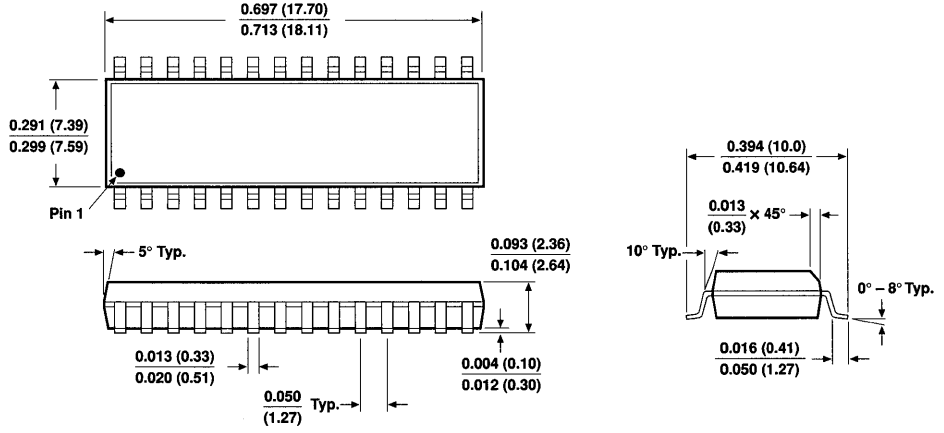
28-Pin Plastic J-Lead Chip Carrier (PLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



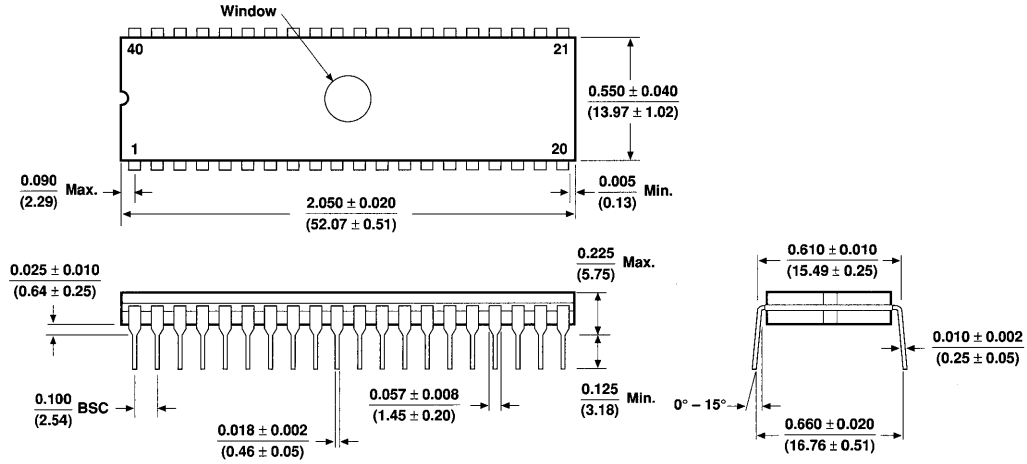
28-Pin Plastic Small-Outline Integrated Circuit (SOIC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



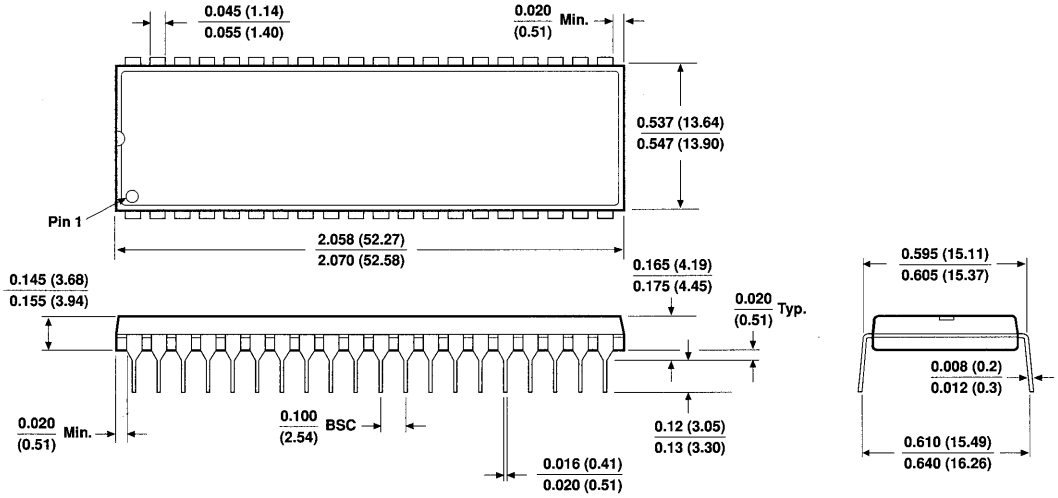
40-Pin Ceramic Dual In-Line Package (CerDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



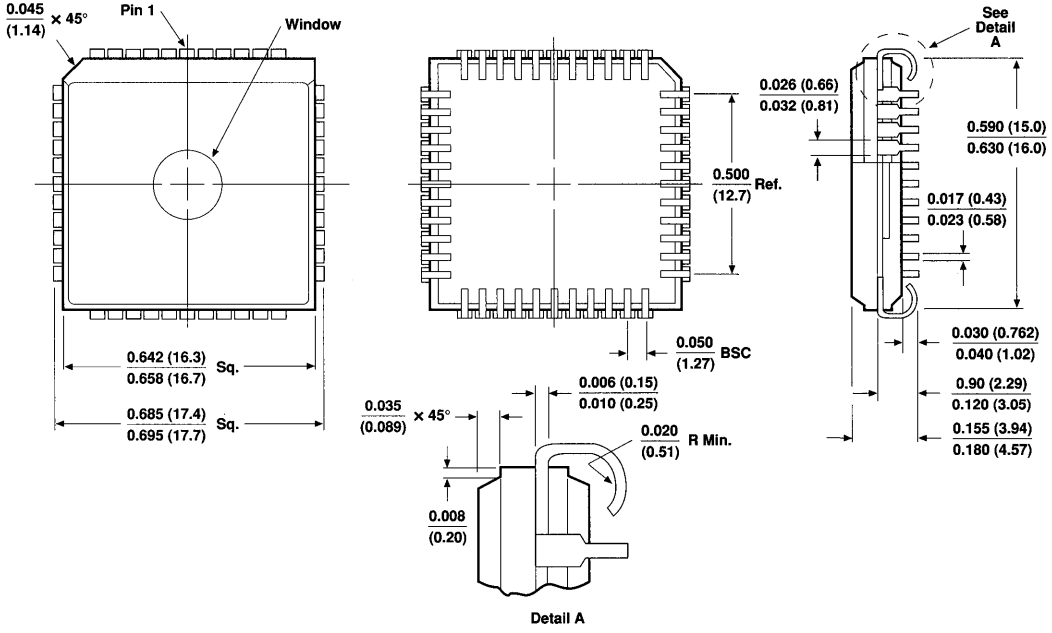
40-Pin Plastic Dual In-Line Package (PDIP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



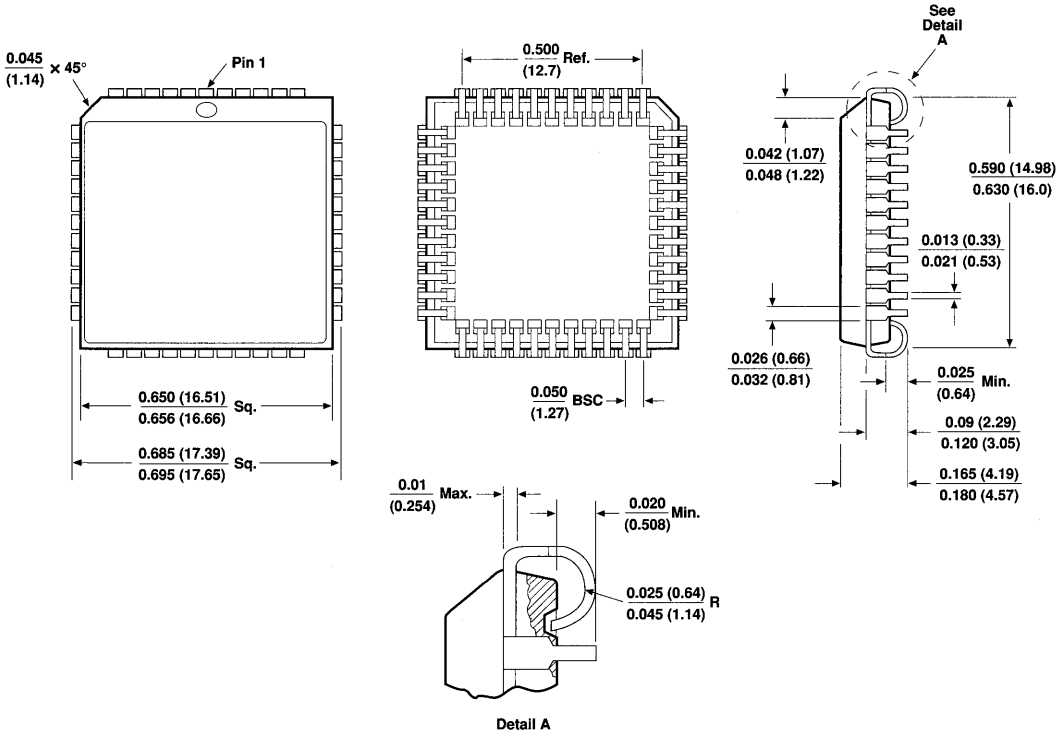
44-Pin Ceramic J-Lead Chip Carrier (JLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



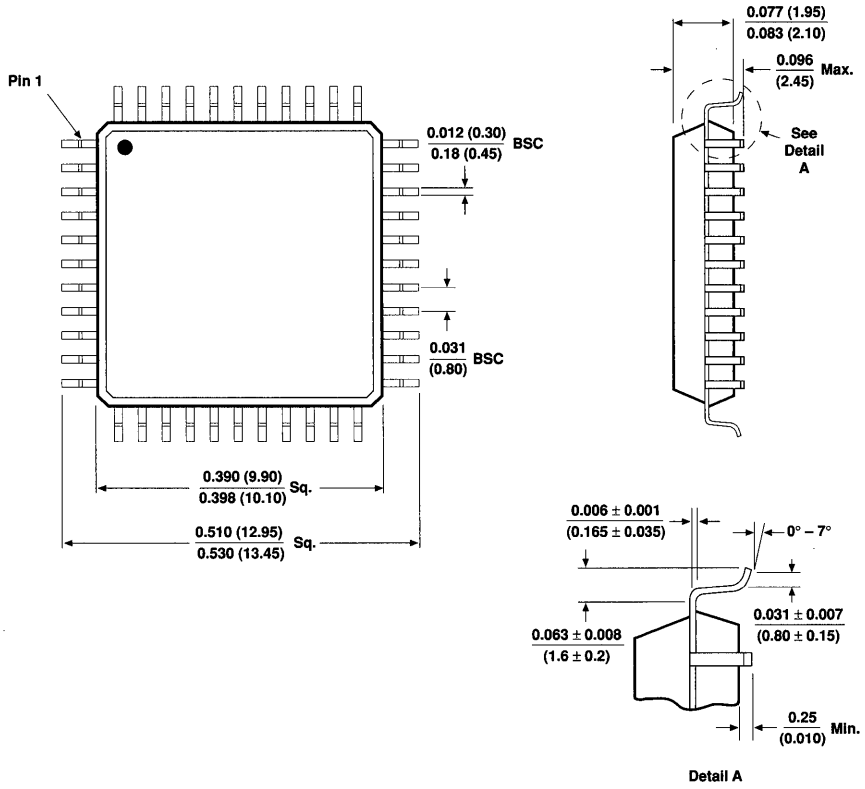
44-Pin Plastic J-Lead Chip Carrier (PLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



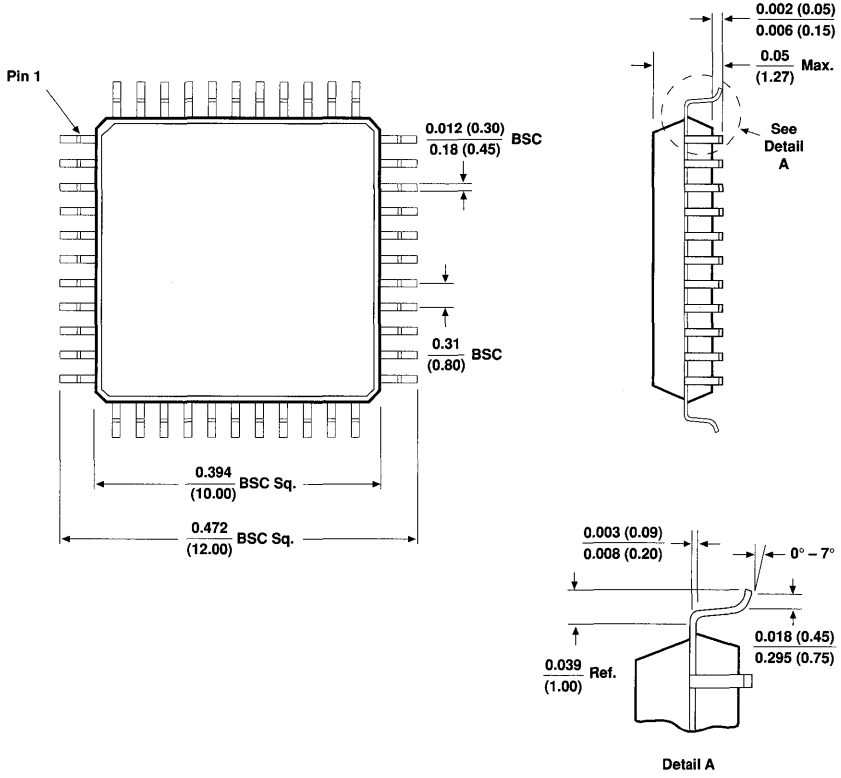
44-Pin Plastic Quad Flat Pack (PQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



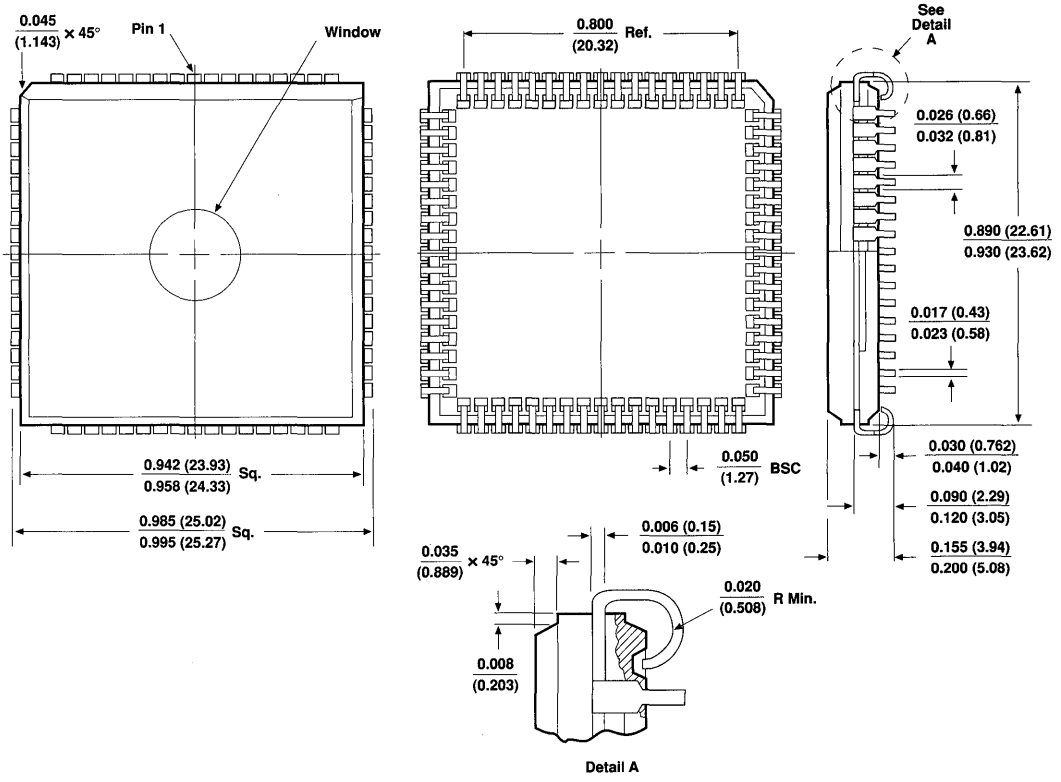
44-Pin Thin Plastic Quad Flat Pack (TQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



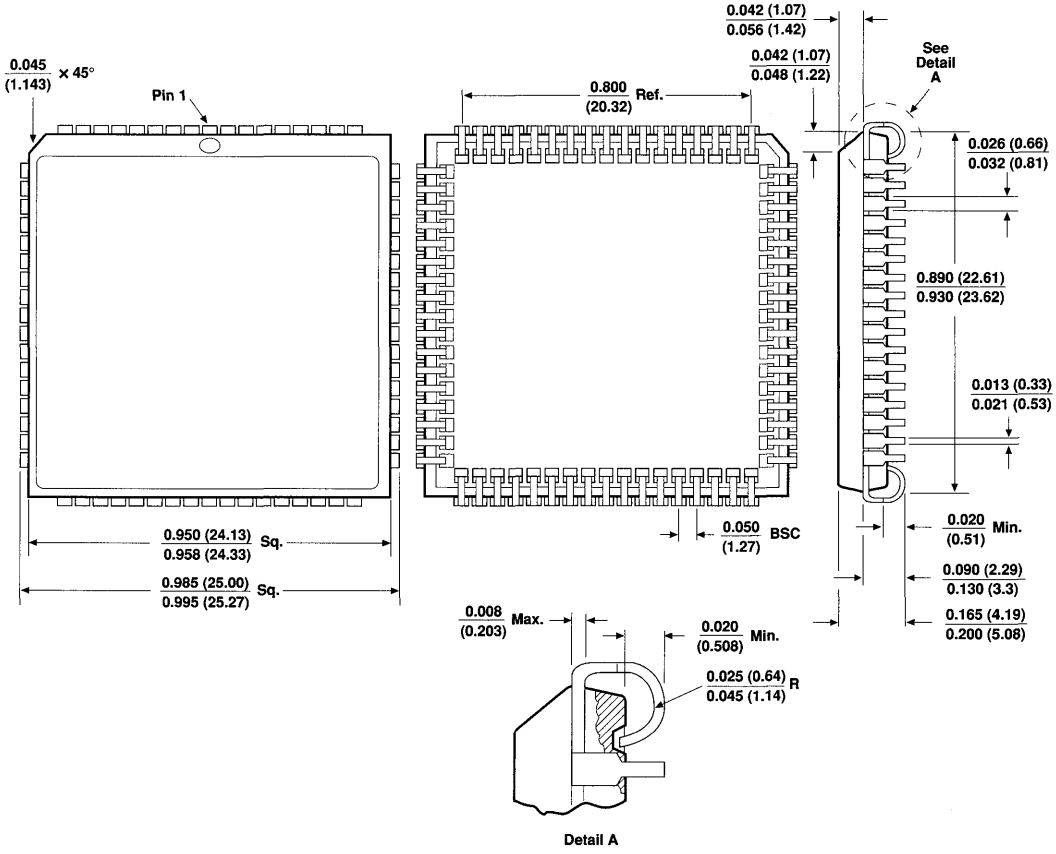
68-Pin Ceramic J-Lead Chip Carrier (JLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline C-J2 in Appendix C of MIL-M-38510.



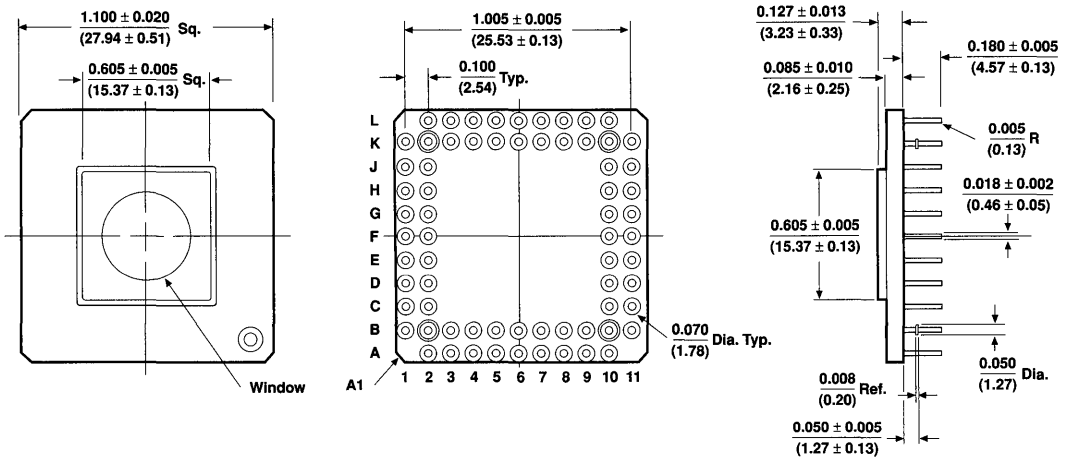
68-Pin Plastic J-Lead Chip Carrier (PLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



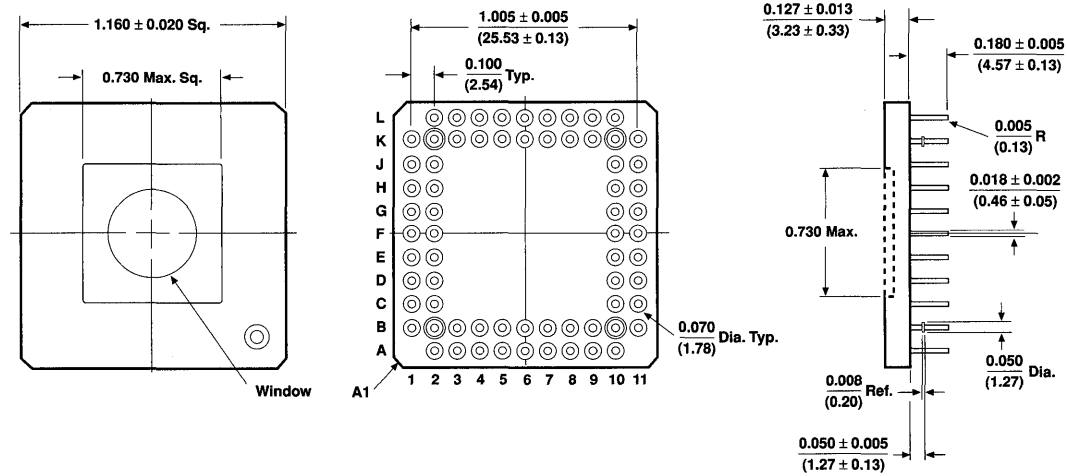
68-Pin Small Outline Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in Altera Military Product Drawing 02D-00205.



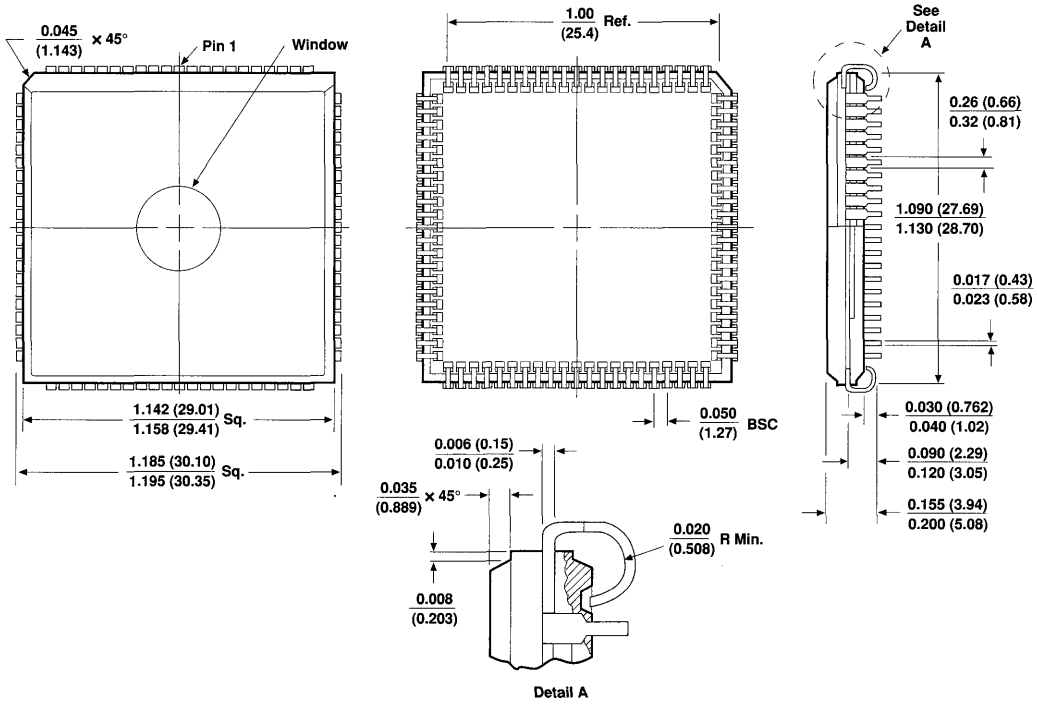
68-Pin Large Outline Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



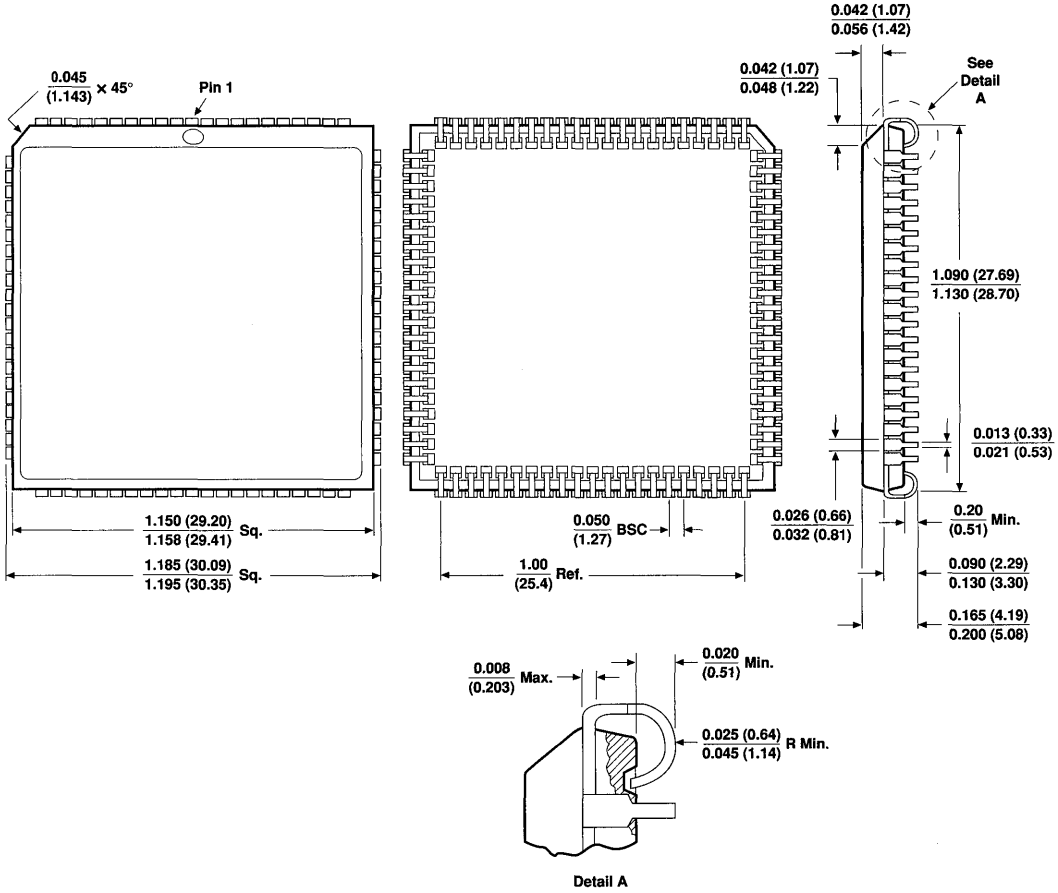
84-Pin Ceramic J-Lead Chip Carrier (JLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



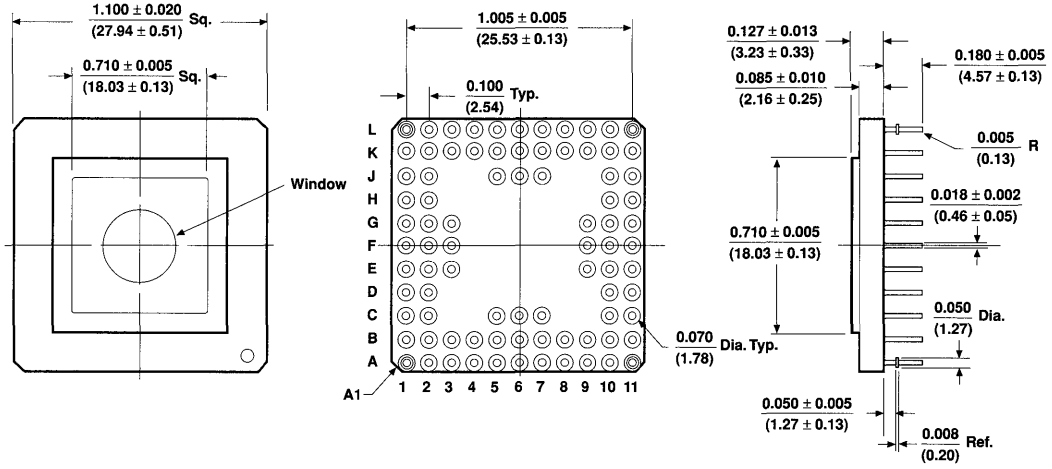
84-Pin Plastic J-Lead Chip Carrier (PLCC)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



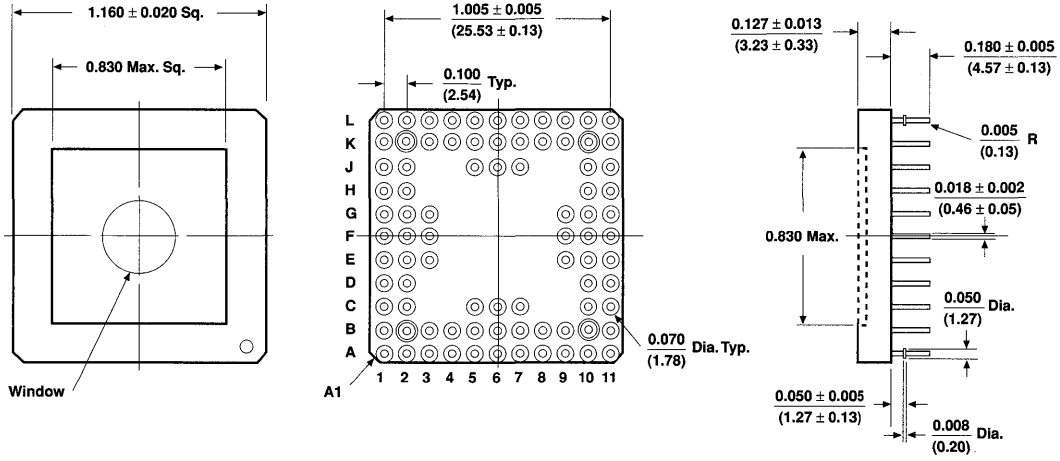
84-Pin Small Outline Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



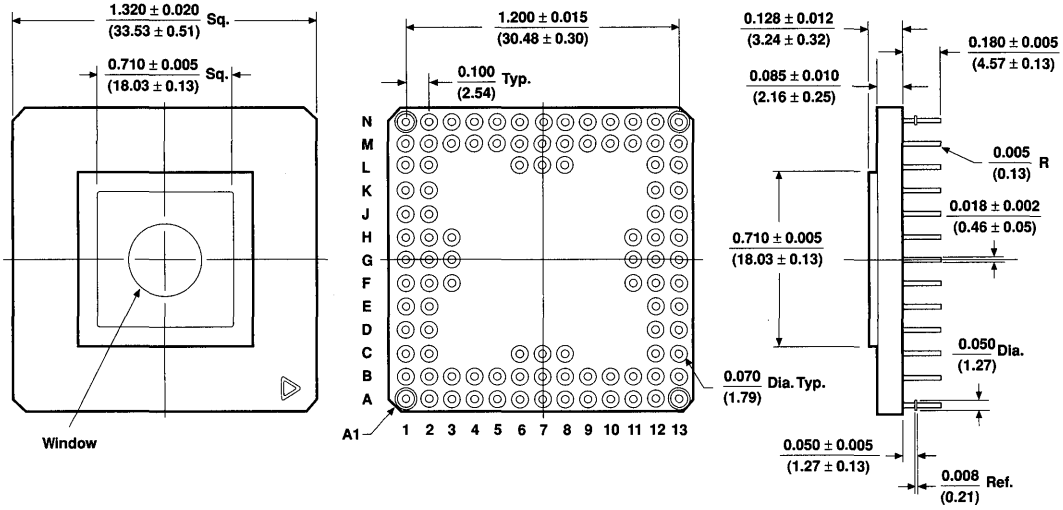
84-Pin Large Outline Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



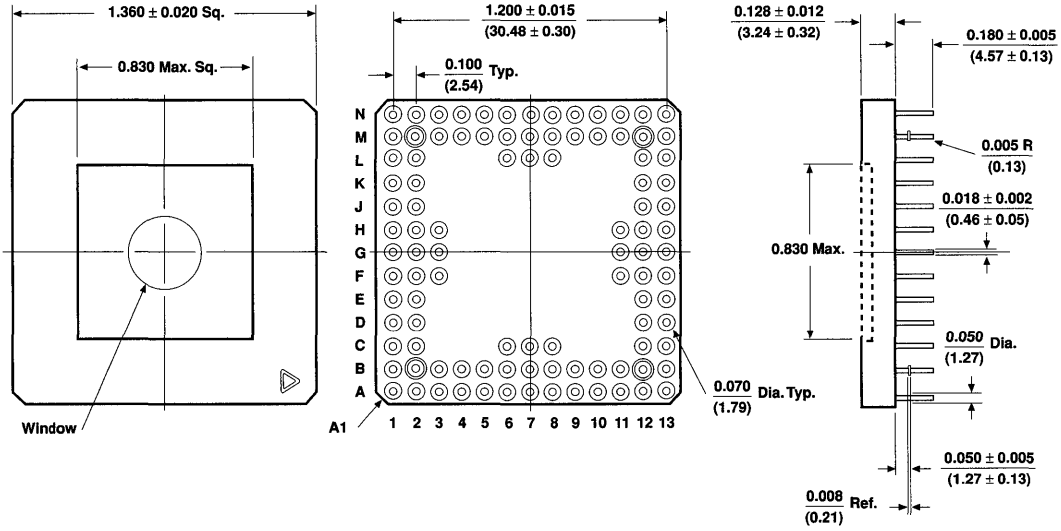
100-Pin Small Outline Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



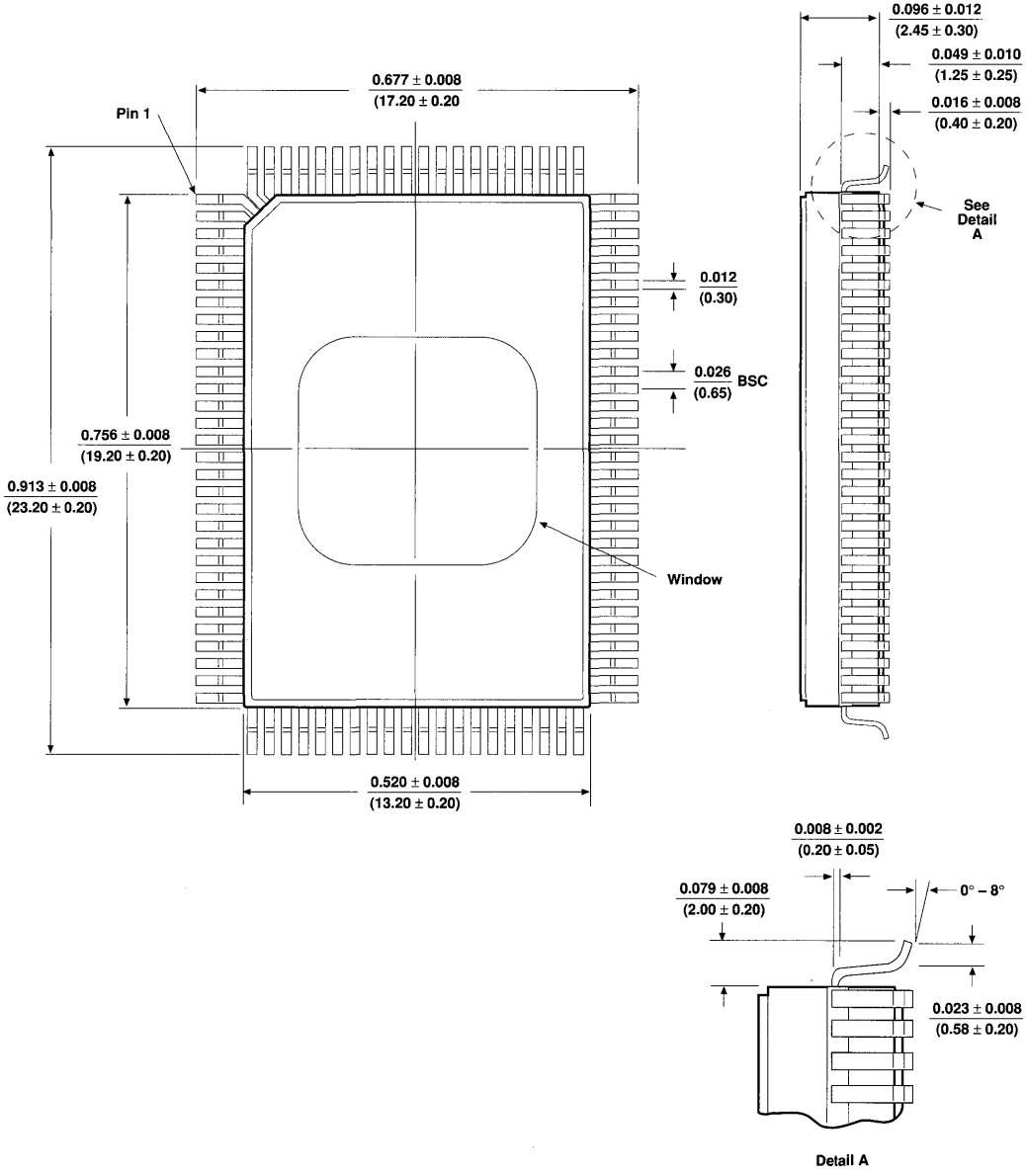
100-Pin Large Outline Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches. For military-qualified product, see case outline in MIL-STD-1835.



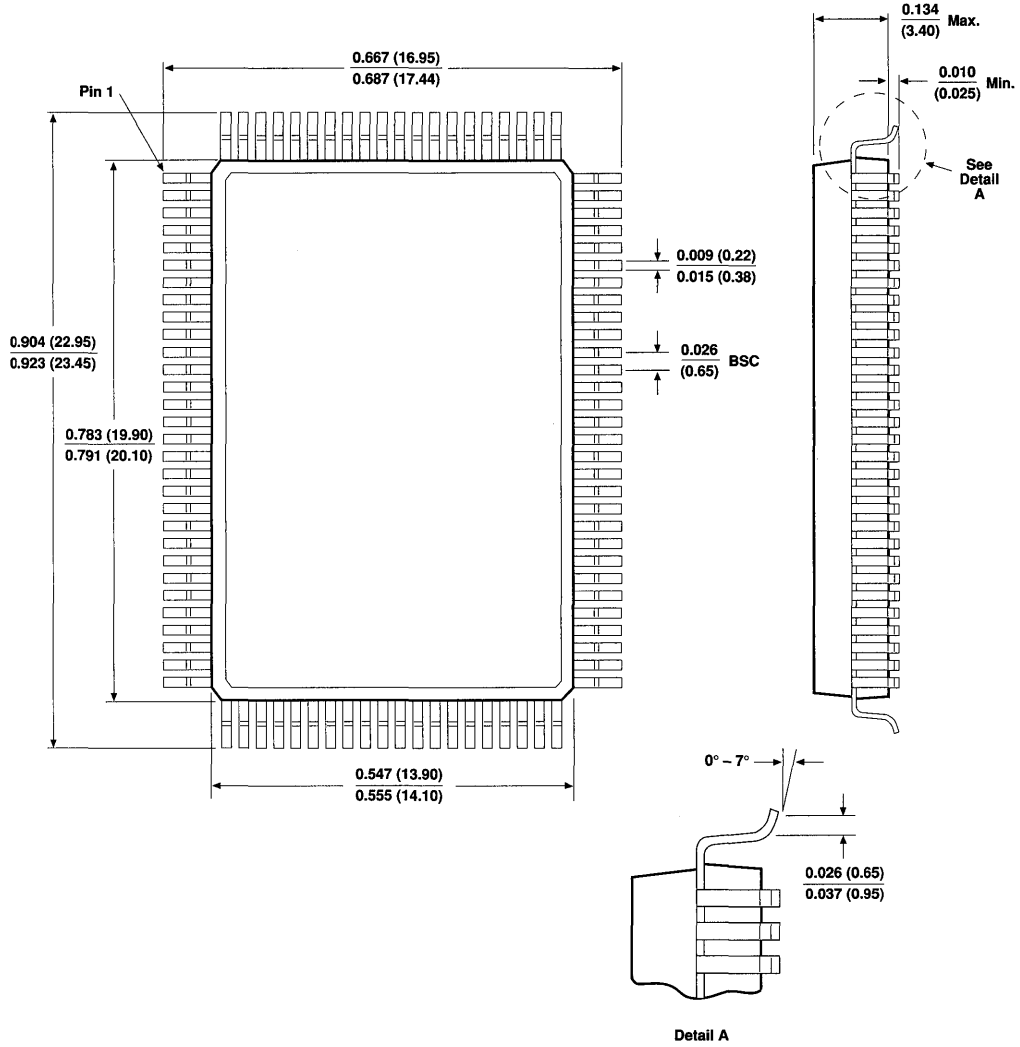
100-Pin Ceramic Quad Flat Pack (CQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



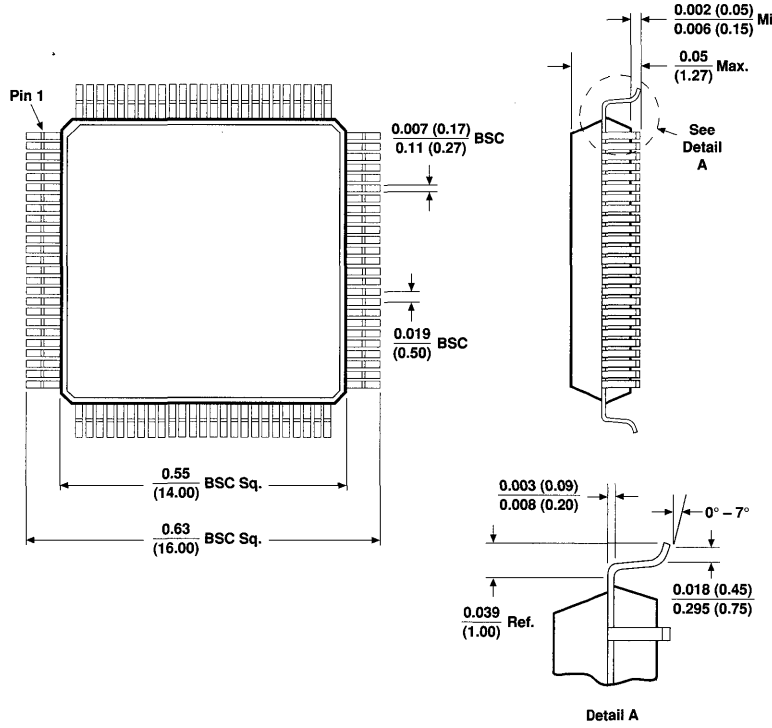
100-Pin Plastic Quad Flat Pack (PQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



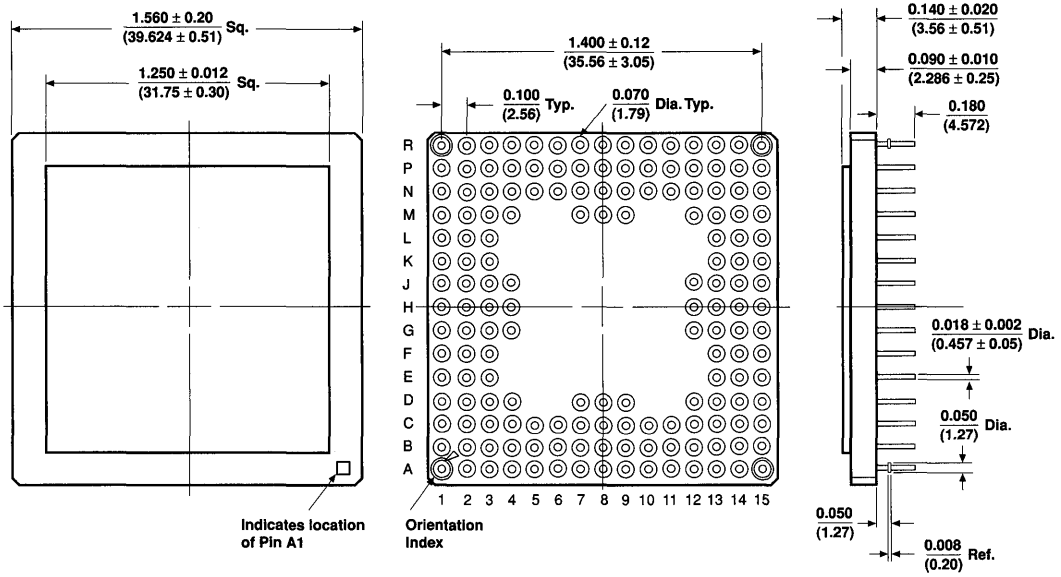
100-Pin Thin Plastic Quad Flat Pack (TQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



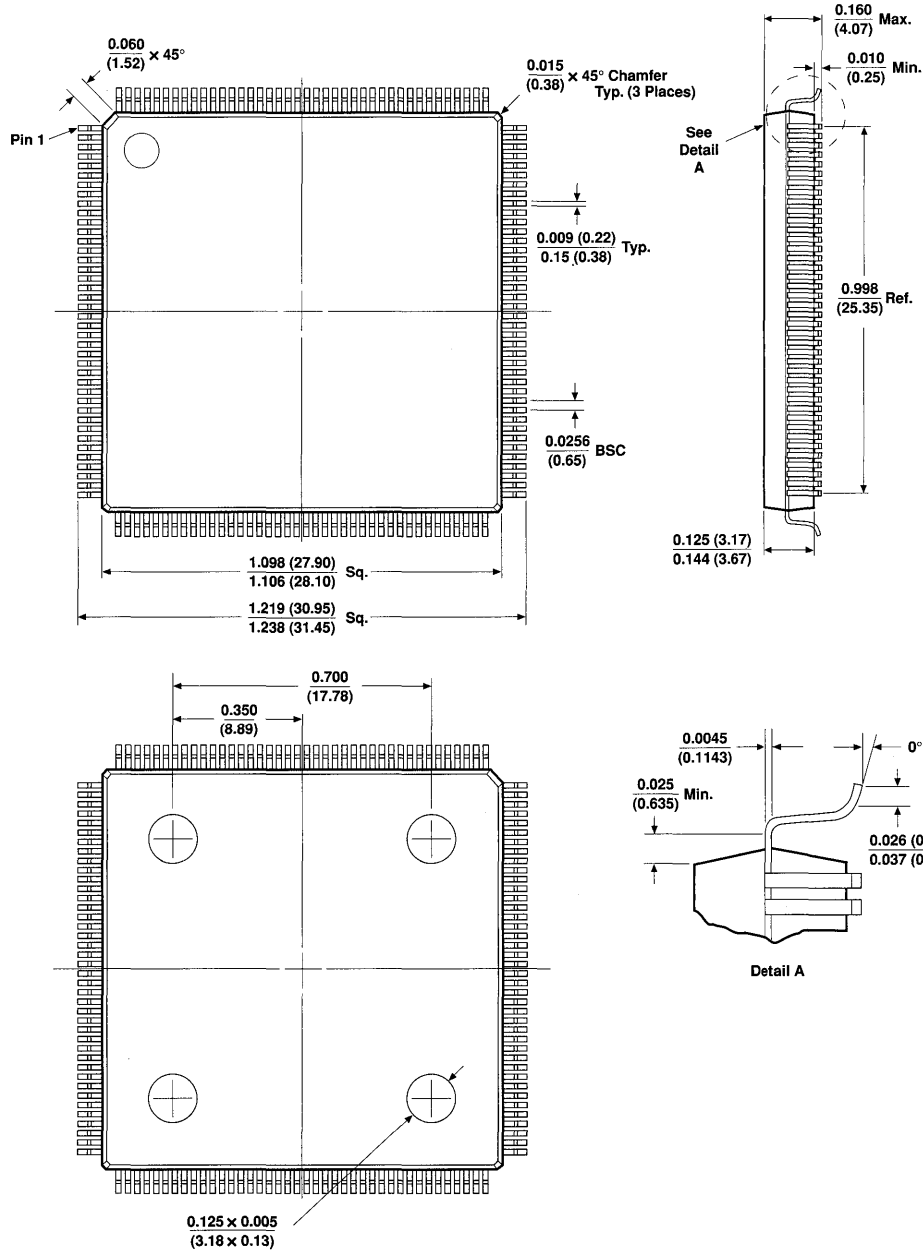
160-Pin Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



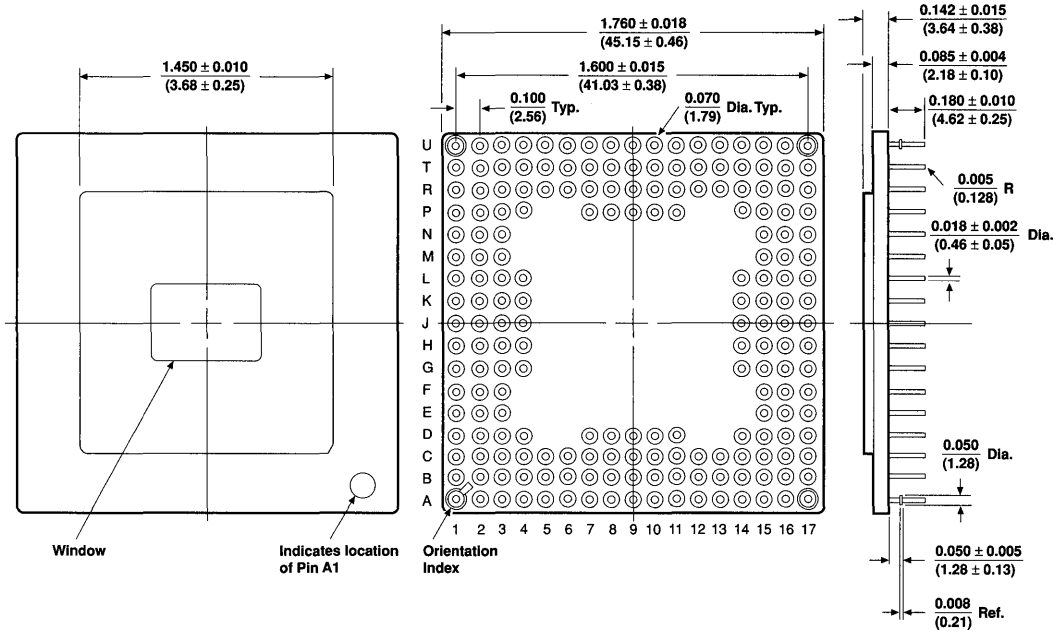
160-Pin Plastic Quad Flat Pack (PQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



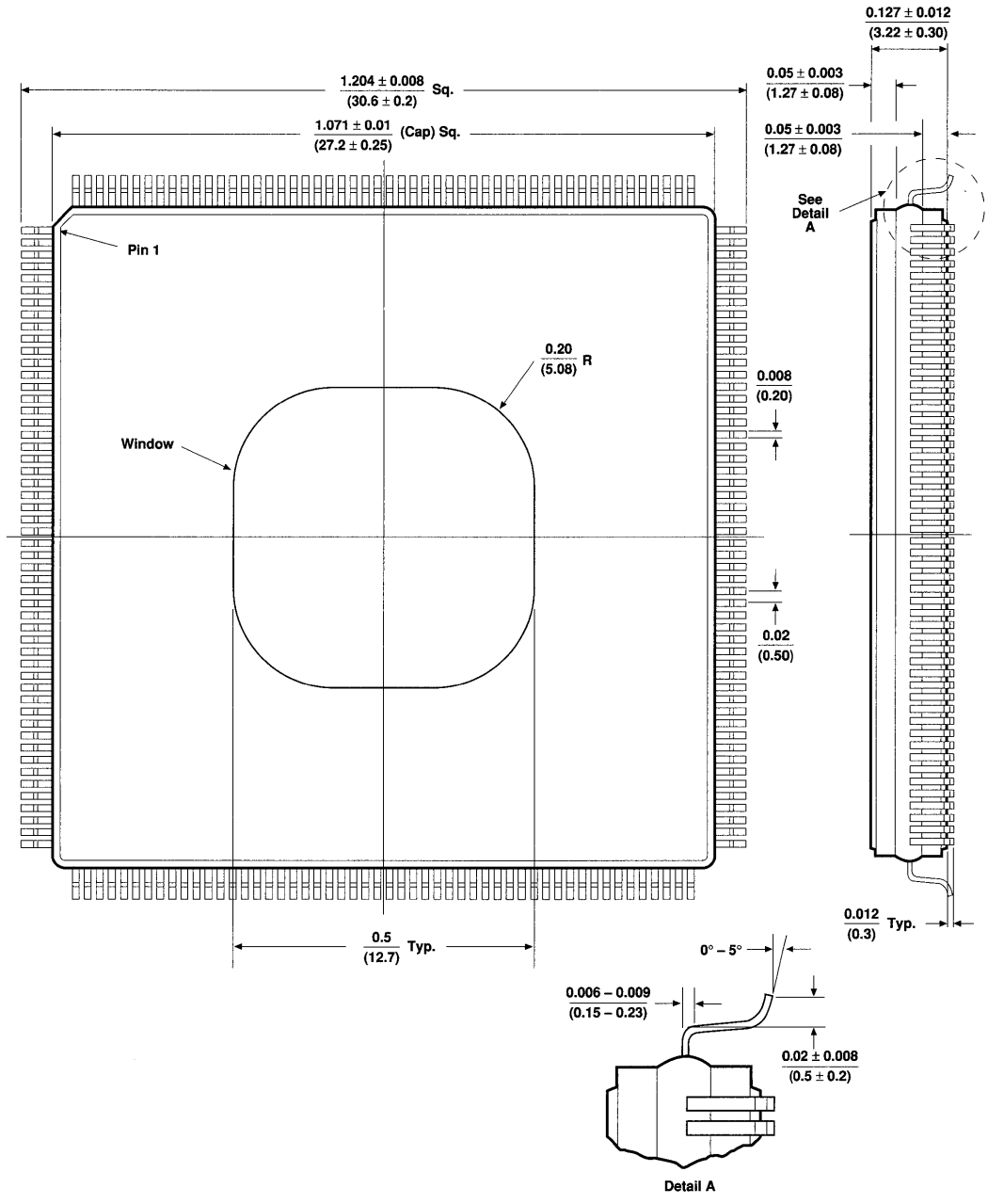
192-Pin Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



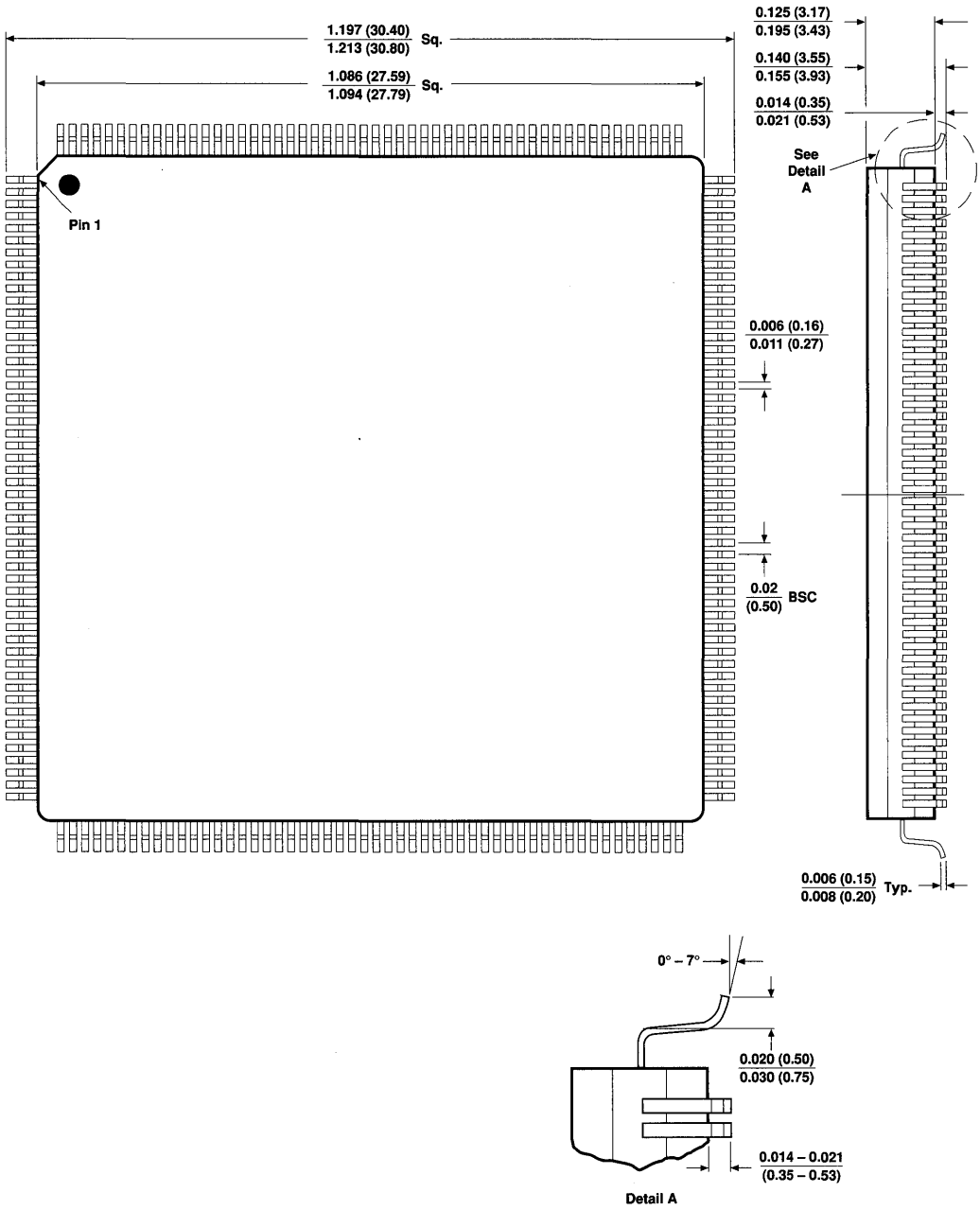
208-Pin Ceramic Quad Flat Pack (QFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



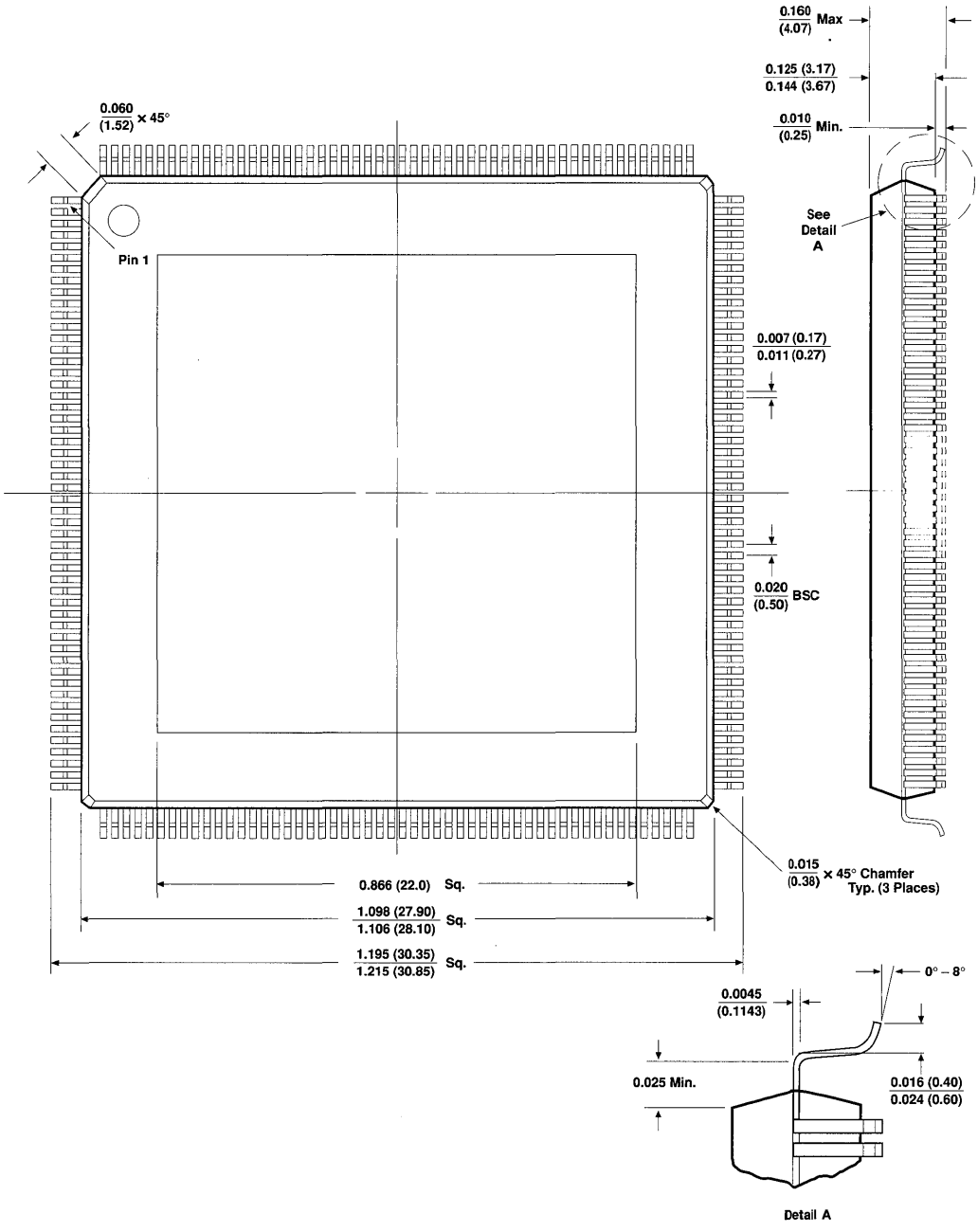
208-Pin Metal Quad Flat Pack (MQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



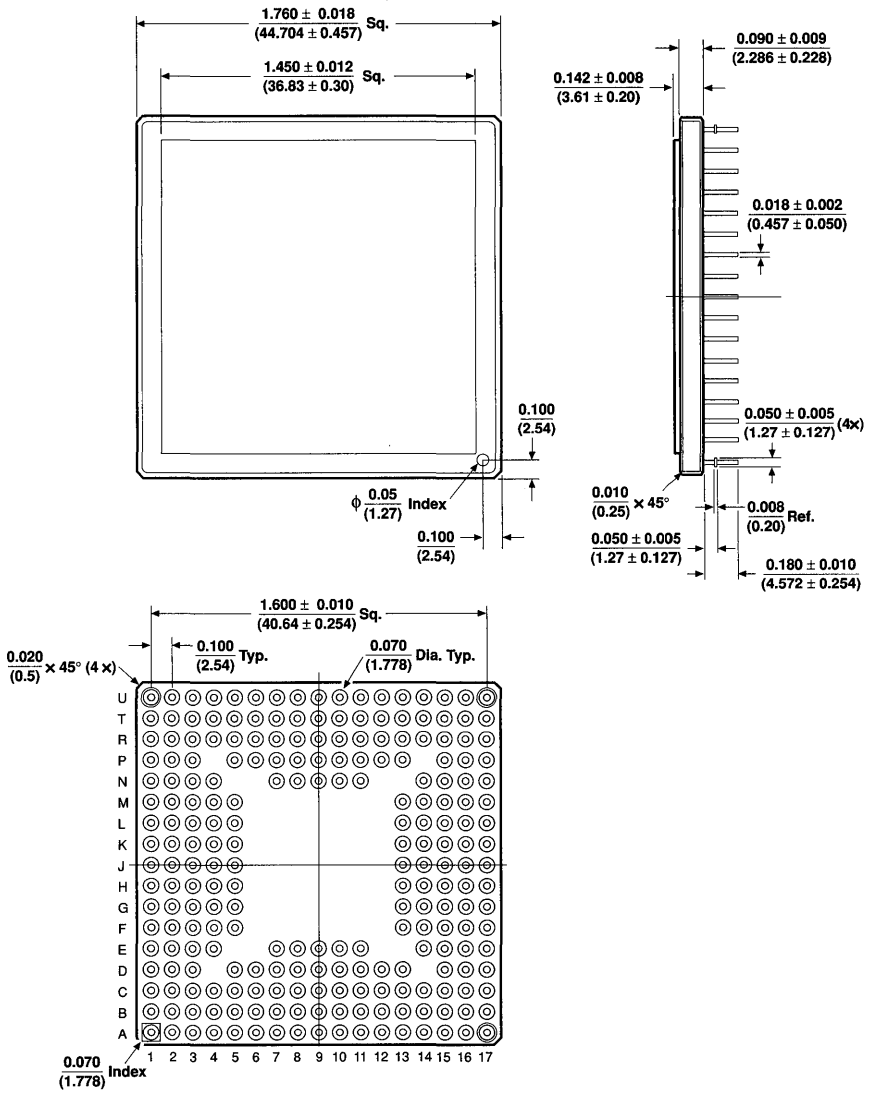
208-Pin Power Quad Flat Pack (RQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



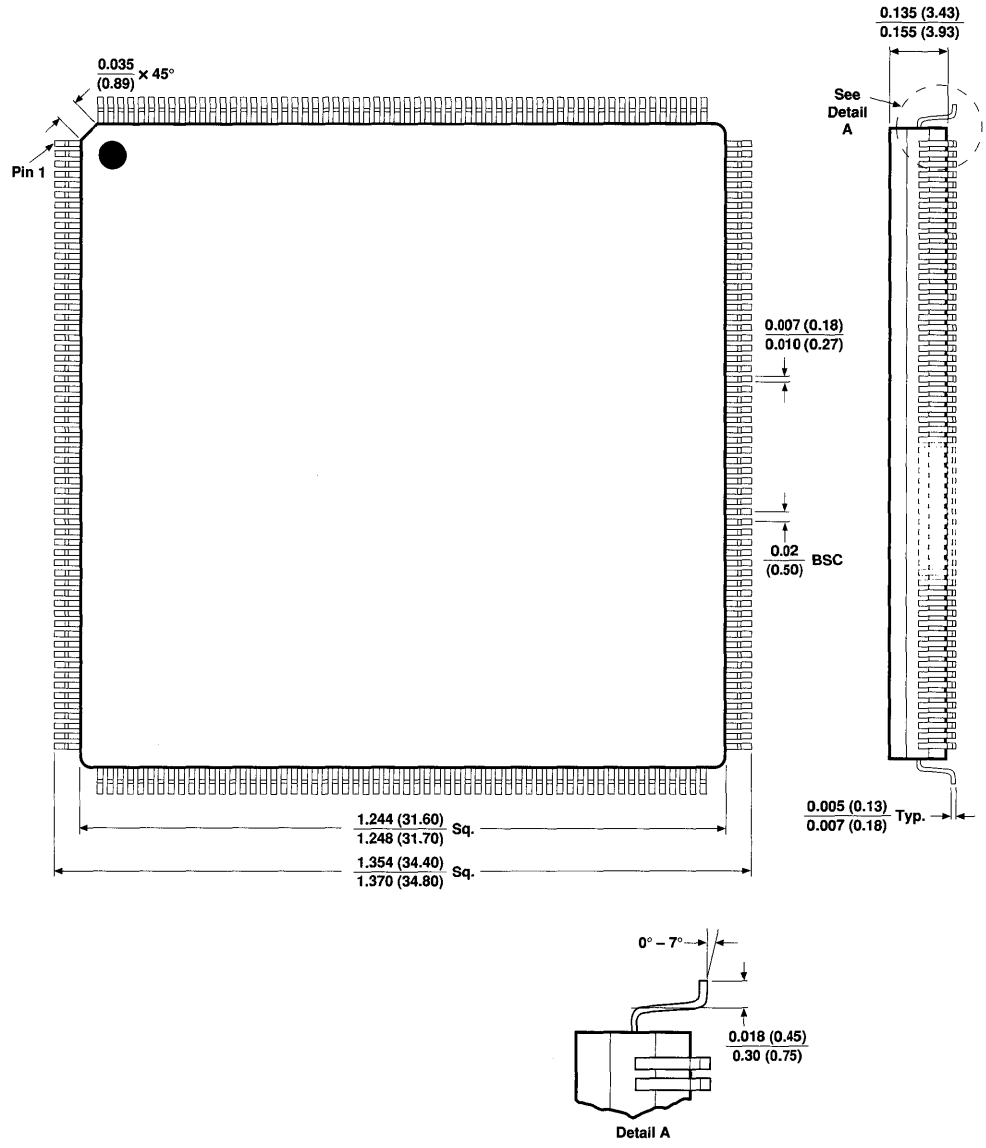
232-Pin Ceramic Pin-Grid Array (PGA)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in inches.



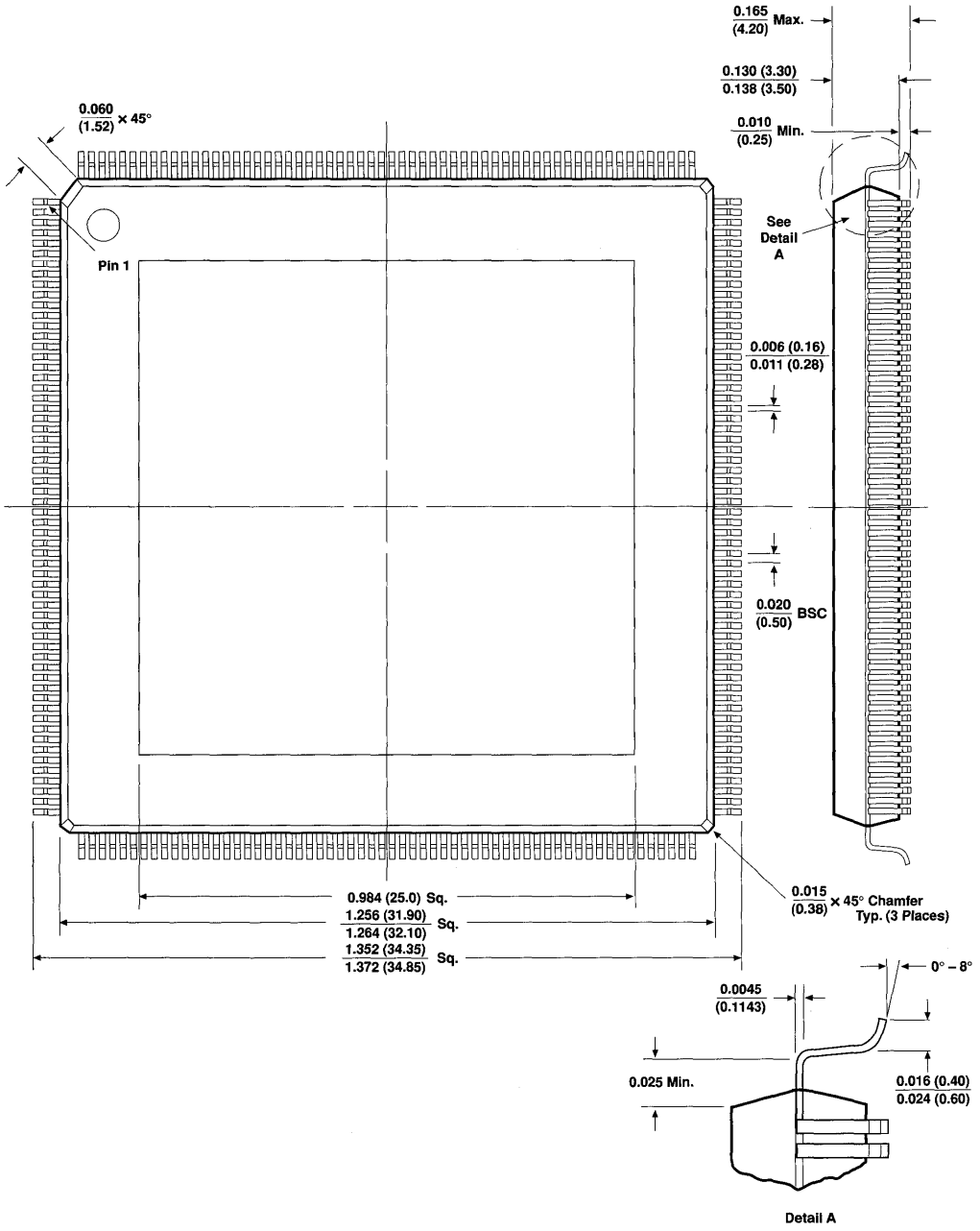
240-Pin Metal Quad Flat Pack (MQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



240-Pin Power Quad Flat Pack (RQFP)

See "Introduction" in this data sheet for dimension formats. Controlling measurement is in millimeters.



Ordering Information

August 1993, ver. 6

Altera Devices

Figure 1 explains the ordering codes for Altera devices. Since many devices are available with different pin counts for the same package type, many of the the ordering codes include pin count. Some devices use relative numbers (e.g., -1, -2) to designate speed grades, while others use actual propagation delay times (e.g., -15, -20). For information on specific package, speed grade, and operating temperature combinations, refer to individual device data sheets in this data book, or contact Altera Marketing at (408) 894-7000.

Figure 1. Device Package Ordering Codes

EPM 7032 L C 44 -7

Family Signature:
EP: Classic device
EPM: MAX 5000 or MAX 7000 device
EPF: FLEX 8000 device
EPC: Configuration EPROM device
EPS: EPS464 or SAM device
EPB: Micro Channel device

Device Type:
EP: 330, 610, 610A, 910, 910A, 1810
EPM: 5016, 5032, 5064, 5128, 5128A, 5130, 5192, 5192A, 7032, 7032V, 7064, 7096, 7128, 7160, 7192, 7256
EPF: 8282, 8282V, 8452, 8820, 81188, 81500
EPC: 1064, 1213
EPS: 448, 464
EPB: 2001

Package Type:
D: Ceramic dual in-line package (CerDIP)
P: Plastic dual in-line package (PDIP)
J: Ceramic J-lead chip carrier (JLCC)
L: Plastic J-lead chip carrier (PLCC)
G: Ceramic pin-grid array (PGA)
B: Ball-grid array (BGA)
S: Plastic small-outline integrated circuit (SOIC)
W: Ceramic quad flat pack (CQFP), *Note (1)*
M: Metal quad flat pack (MQFP), *Note (1)*
Q: Plastic quad flat pack (PQFP), *Note (1)*
T: Thin plastic quad flat pack (TQFP), *Note (1)*
R: Power quad flat pack (RQFP), *Note (1)*

Speed Grade:
See individual data sheets in this data book for speed/product relationships (e.g., -2, -15T, or blank).

Pin Count:
Number of pins for devices with different pin-count options (MAX 7000, FLEX 8000, and Configuration EPROM devices only).

Operating Temperature/Military Processing:
C: Commercial temperature (0° C to 70° C)
I: Industrial temperature (–40° C to 85° C)
M: Military temperature (–55° C to 125° C)
M883B Processed to MIL-STD-883, current revision
M883BX: Processed to MIL-STD-883, current revision with modified J-lead package dimension
MB: Fully compliant with deviation to MIL-STD-883, current revision (consult Altera for specific deviations)
5962: DESC Standard Military Drawing (SMD)

Examples:

EPF81188GC232-3	EPF81188 in a ceramic 232-pin PGA package, commercial temperature range, -3 speed grade
EPM5130GM883B	EPM5130 in a ceramic 100-pin PGA package, MIL-STD-883B-qualified

Note:
(1) MAX 5000 and MAX 7000 devices in QFP packages with 100 or more pins are shipped in QFP carriers. For more information on QFP carriers, see the *QFP Carrier & Development Socket Data Sheet* in this data book.

MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs) available from Altera Marketing. These MPDs should be used to prepare Source Control Drawings (SCDs).

Development Tools

Table 1 provides ordering codes for Altera's MAX+PLUS II development systems and software and lists the Altera devices supported by each configuration. Refer to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* for details on each package. To order add-on products, the base system must be covered by a current software maintenance agreement.

Table 1. Altera Development Systems, Software & Device Support

Development System & Software Features					Device Compilation Support *(1)*			
Ordering Codes	**Base Design Environment** *(2)*	**Advanced Design Environment** *(3)*	**Workstation Design Environment** *(4)*	**Programming Hardware**	**FLEX 8000**	**MAX 7000**	**MAX 5000 EPS464**	**Classic EPM5016 EPM5032 EPM7032 EPM7032V**
MAX+PLUS II Base Systems (PC Platform)								
PLS-ES	✓							✓
PLS-STD	✓						✓	✓
PLS-ADV	✓					✓	✓	✓
PLS-FLEX8	✓				✓		✓	✓
PLS-HPS	✓	✓				✓	✓	✓
PLDS-HPS	✓	✓		✓		✓	✓	✓
MAX+PLUS II Add-On Products (PC Platform)								
PLSM-5K							✓	
PLSM-7K						✓		
PLSM-8K					✓			
PLSM-ADE		✓						
MAX+PLUS II Base Systems (Workstation Platform)								
PLS-WS/HP			✓		✓	✓	✓	✓
PLS-WS/SN			✓		✓	✓	✓	✓
MAX+PLUS II Add-On Products (Workstation Platform)								
PLSM-TA *(5)*			✓					

Notes to table:

(1) Device compilation support includes logic synthesis and fitting.

(2) The base design environment includes the following features:
- Schematic capture
- Text design entry with the Altera Hardware Description Language (AHDL)
- Bidirectional EDIF 2 0 0 and EDIF 2 9 0 interface
- LPM input
- Hierarchical design management
- Automatic error location
- Timing analysis
- Extensive on-line help

(3) The advanced design environment includes the following additional features:
- Waveform design entry and editing
- Design-rule checking
- Multi-device partitioning within a device family
- Functional, timing, and multi-device simulation across device families
- Timing analysis across device families

(4) The workstation design environment includes the following features:
- Text design entry with AHDL
- Bidirectional EDIF 2 0 0 and EDIF 2 9 0 interface
- LPM input
- Multi-device partitioning within a device family
- Standard CAE interfaces
- Extensive on-line help

(5) This add-on product provides timing analysis across device families for MAX+PLUS II for workstations.

Floating Node Licenses for Workstations

In addition to the base system, users can purchase floating nodes that are tied to a license manager on a workstation network. These extra nodes can be obtained by purchasing one or more floating node licenses (see Table 2). Each floating node includes a unique Altera identification number that is associated with the original base system purchased. To purchase a floating node, the original base system must be covered by a current software maintenance agreement.

Table 2. Floating Node Licenses for Workstations

Product	Ordering Code
PLS-WS/SN	PLSM-WS/SN
PLS-WS/HP	PLSM-WS/HP

Software Maintenance Agreement

Renewable, one-year software maintenance agreements for development products provide software and documentation updates for all registered users of Altera development systems. Table 3 shows the codes for ordering software maintenance agreements.

Table 3. Software Maintenance Agreement

Product	Ordering Code
PLS-ES	PLAESW-ES
PLS-STD	PLAESW-STD
PLS-ADV	PLAESW-ADV
PLS-FLEX8	PLAESW-FLEX8
PLS-HPS, PLDS-HPS	PLAESW-HPS
PLSM-5K	PLAESW-5K
PLSM-7K	PLAESW-7K
PLSM-8K	PLAESW-8K
PLSM-ADE	PLAESW-ADE
PLS-WS/SN, PLSM-WS/SN, PLS-WS/HP, PLSM-WS/HP	PLAESW-WS
PLSM-TA	PLAESW-TA

Programming Hardware & Adapters

This section provides the ordering codes for Altera programming hardware. Table 4 lists the ordering codes for the programming card and units. For complete information on programming hardware and adapters, see the *Altera Programming Hardware Data Sheet* in this data book.

Table 4. Programming Hardware

Product	Ordering Code	Description
LP6 Logic Programmer Card	PLP6	Interfaces with IBM PC-AT or compatible computer.
LP5 Logic Programmer Card	PLP5	Interfaces with IBM PS/2 or compatible Micro Channel computer.
Master Programming Unit (MPU)	PL-MPU	Programs all Altera devices (with the appropriate device adapter).
Compatibility Adapter	PLAD3-12	Interfaces PLE- prefix adapters to MPU. Together with MPU, directly supports EP330 devices.
Altera Stand-Alone Programmer	PL-ASAP2	Includes programming software, a Logic Programmer card, and the MPU.

Table 5 lists the ordering codes for programming adapters. PLAD3-12 and PLM-prefix programming adapters plug directly into the Master Programming Unit (MPU). PLM-prefix adapters provide programming support, device-to-socket continuity testing, and device functional testing (except for FLEX 8000 and Configuration EPROM devices). PLAD3-12 compatibility adapters allow PLE-prefix adapters, which provide programming support, to be used with the MPU.

Table 5. Device Adapter Support (Part 1 of 2)

Device	Package	Adapter
EP330	DIP J-Lead SOIC	PLAD3-12 PLEJ330 PLES330
EP600/610/610A/610T	DIP J-lead SOIC	PLED610 PLEJ610 PLES610
EP900/910/910A/910T	DIP J-lead	PLED910 PLEJ910
EP1800/1810/1810T	J-lead PGA	PLMJ1810 PLEG1810
EPB2001	J-lead	PLEJ2001
EPM5016	DIP J-lead SOIC	PLED5016 PLEJ5016 PLES5016
EPM5032	DIP J-lead SOIC	PLMD5032 PLMJ5032 PLES5032
EPM5064	J-lead	PLMJ5064
EPM5128/5128A	J-lead PGA	PLMJ5128A PLMG5128A
EPM5130	J-lead PGA QFP	PLMJ5130 PLEG5130 PLMQ5130
EPM5192/5192A	J-lead PGA QFP (EPM5192A only)	PLMJ5192 PLMG5192 PLMQ5192A
EPM7032, EPM7032V	J-lead QFP TQFP	PLMJ7032-44 PLMQ7032-44 PLMT7032-44
EPM7064	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 5. Device Adapter Support (Part 2 of 2)

Device	Package	Adapter
EPM7096	J-lead (68-pin) J-lead (84-pin) QFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128	J-lead (68-pin) J-lead (84-pin) QFP (100-pin) QFP (160-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100 PLMQ7128-160
EPM7160	J-lead QFP (100-pin) QFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7160-160
EPM7192	PGA QFP	PLMG7192-160 PLMQ7192-160
EPM7256	PGA QFP (160-pin) QFP (208-pin)	PLMG7256-192 PLMQ7256-160 PLMQ7256-208
All FLEX 8000 devices	all	*Note (1)*
EPC1064	DIP J-lead TQFP	PLMJ1213 PLMJ1213 PLMT1064
EPC1213	DIP J-lead	PLMJ1213 PLMJ1213
EPS448	DIP J-lead	PLED448 PLEJ448
EPS464	J-lead QFP	PLMJ464 PLMQ464

Note:

(1) Configuration of FLEX 8000 devices is supported by Configuration EPROMs and the FLEX Download Cable, which is provided with Configuration EPROM adapters.

Development Sockets for QFP Carriers

Table 6 shows the ordering codes for QFP device development sockets. All MAX 5000/EPS464 and MAX 7000 QFP devices with 100 or more pins are shipped in QFP carriers. QFP carriers and development sockets are rated from –65° C to 155° C and are qualified to handle commercial (C), industrial (I), and military (M) operating temperatures.

Table 6. QFP Device Sockets

Product	Ordering Code
100-pin development socket (includes removal tool)	PL-SKT/Q100
160-pin development socket (includes removal tool)	PL-SKT/Q160
208-pin development socket (includes removal tool)	PL-SKT/Q208

Table 7 shows the ordering codes for the QFP carrier extraction tools.

Table 7. QFP Carrier Extraction Tools

Product	Ordering Code
100-pin QFP carrier extraction tool	PL-EXT1
160- and 208-pin QFP carrier extraction tool	PL-EXT2

Notes:

Technical Support from Altera Applications

August 1993, ver. 1

Introduction

Altera's technical support team includes over 30 Applications Engineers dedicated to promptly resolving customers' technical issues. These Applications Engineers are located at Altera's headquarters in San Jose, California, and at several locations around the world.

In addition, Altera Applications offers the following services:

- Training courses
- Electronic bulletin board service
- Applications publications
- Design evaluations
- Technical support hotline

Training Courses

Altera provides a variety of training courses that help customers efficiently use Altera products. With these courses, customers can fine-tune their skills with Altera development tools or simply learn more about Altera products. Courses include device architectures, MAX+PLUS II demonstrations, and how-to sessions. All training courses can be tailored to fit customer needs.

Training courses are held at Altera in San Jose; in some cases, they can be held at customer sites. For more information, contact Altera Applications at (408) 894-7000.

Electronic Bulletin Board Service

Altera maintains a 24-hour electronic bulletin board service (BBS) for instant access to the latest Altera product information. On-line versions of Altera application notes and briefs, as well as recent quarterly newsletters, are available from the BBS. Software utility programs are also available.

The telephone number for the BBS is (408) 249-1100. To connect to the BBS via modem, the following equipment and configuration is required:

- 1200 or 2400 baud rate
- Bell Standard 212A or compatible modem
- 8 data bits, 1 stop bit, no parity

The following file transfer protocols are supported:

- ASCII (non-binary)
- Xmodem (checksum)
- Xmodem-CRC (CRC)
- Ymodem-G (1K-Xmodem-G)
- Ymodem (1K-Xmodem)
- Kermit

Applications Publications

Altera Applications produces technical application notes and briefs to help customers select and use programmable logic. All technical literature currently available from Altera is listed in the Applications quarterly customer newsletter, *News & Views*. The *News & Views* newsletter also includes technical articles written by Altera Applications engineers, a question and answer section that addresses many commonly asked questions, and the latest information on Altera products. All registered users of Altera products receive *News & Views* each quarter.

Design Evaluations

If customers are considering using Altera devices, Altera Applications Engineers can evaluate their designs and recommend a device that will best fit their needs. Applications engineers will also estimate device performance. For more information, contact your local Altera sales office.

Technical Support Hotline

From 7:30 a.m. to 5:00 p.m. Pacific Standard Time, customers can talk directly to Applications Engineers when they call (800) 800-EPLD. Questions are handled promptly and completely, ensuring that the design process keeps moving forward. If customers are outside of the United States, they can contact their local Altera distributor or sales office, or send a fax to (408) 954-0348.

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August 1993

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Glossary

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A

Active Parallel Down (APD) A configuration scheme in which a byte-wide parallel PROM loads the design data into a FLEX 8000 device. The FLEX 8000 device first generates an address; the PROM subsequently returns the next byte of data. Addresses are generated by the FLEX 8000 device sequentially in descending order (3FFFFh to 00000h). MAX+PLUS II can generate Hexadecimal (Intel-Format) Files (**.hex**) that contain the data for configuring FLEX 8000 devices in an APD configuration scheme.

Active Parallel Up (APU) A configuration scheme in which a byte-wide parallel PROM loads the design data into a FLEX 8000 device. The FLEX 8000 device first generates an address; the PROM subsequently returns the next byte of data. Addresses are generated by the FLEX 8000 device sequentially in ascending order (00000h to 3FFFFh). MAX+PLUS II can generate Hexadecimal (Intel-Format) Files (**.hex**) that contain the data for configuring FLEX 8000 devices in an APU configuration scheme.

Active Serial (AS) A configuration scheme in which a serial EPROM loads the design data into a FLEX 8000 device. The MAX+PLUS II Compiler automatically generates a Programmer Object File (**.pof**) for programming serial EPROM devices, e.g., the EPC1213 Configuration EPROM, whenever a FLEX 8000 project is compiled.

Altera Hardware Description Language (AHDL) Altera's design entry language. AHDL is completely integrated into MAX+PLUS II, and allows the designer to enter and edit Text Design Files (**.tdf**) with the MAX+PLUS II Text Editor or any standard text editor, then compile, simulate, and program projects within MAX+PLUS II. AHDL supports Boolean equation, state machine, conditional, and decode logic. AHDL also provides access to all Altera macrofunctions.

array Clock A Clock signal that passes through the logic array of a device before arriving at the Clock input of a register.

Assembler The Compiler module that creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), and optional JEDEC Files (**.jed**) for programming Altera devices.

authorization code A code that enables MAX+PLUS II applications and features. This code, provided by Altera, is shown on the Altera Registration card shipped with new MAX+PLUS II systems.

C

Carry Chain option A FLEX 8000 logic synthesis option that controls the use of carry chain logic. When this option is set to AUTO, it directs the Compiler's Logic Synthesizer module to insert carry chain logic—i.e., insert CARRY buffers—wherever it is useful. When defining a logic synthesis style, designers can specify the maximum allowable length of a chain of these synthesized CARRY buffers. The AUTO setting does not force the Logic Synthesizer to use carry logic and has no effect on CARRY primitives that have been entered in design files.

When the Carry Chain option is set to IGNORE, it directs the Logic Synthesizer to ignore CARRY buffers that have been entered manually in design files. When this option is set to MANUAL, the Logic

Synthesizer uses only the CARRY primitives that have been manually entered in design files.

Cascade Chain option A FLEX 8000 logic synthesis option that controls the use of cascade chain logic. When this option is set to AUTO, it directs the Compiler's Logic Synthesizer module to insert cascade logic—i.e., insert CASCADE buffers—wherever it is useful. When defining a logic synthesis style, designers can specify the maximum allowable length of a chain of these synthesized CASCADE buffers. The AUTO setting does not force the Logic Synthesizer to use cascade logic and has no effect on CASCADE primitives that have been entered in design files.

When the Cascade Chain option is set to IGNORE, it directs the Logic Synthesizer to ignore CASCADE buffers that have been entered manually in design files. When this option is set to MANUAL, the Logic Synthesizer uses only the CASCADE primitives that have been manually entered in design files.

CerDIP Ceramic Dual In-Line Package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

Classic An Altera device family based on Altera's original EPLD architecture. This EEPROM- and EPROM-based family includes EP330, EP610, EP610A, EP910, EP910A, and EP1810 devices.

Compiler Netlist Extractor The MAX+PLUS II Compiler module that creates Compiler Netlist Files (**.cnf**), Hierarchy Interconnect Files (**.hif**), and Symbol Files (**.sym**) from the design files for a project. This module includes built-in EDIF and Xilinx Netlist Readers that convert EDIF Netlist Files (**.edf**) and Xilinx Netlist Format Files (**.xnf**) created with industry-standard CAE software. The Compiler Netlist Extractor also checks each design file in a project for problems such as duplicate node names, missing inputs and outputs, and outputs that are tied together.

Configuration EPROM A serial EPROM supplied by Altera for configuring FLEX 8000 devices.

configuration scheme The method used to load data into a FLEX 8000 device. Six configuration schemes are available:

Active Serial (AS)
Active Parallel Up (APU)
Active Parallel Down (APD)
Passive Parallel Asynchronous (PPA)
Passive Parallel Synchronous (PPS)
Passive Serial (PS)

For complete information on FLEX 8000 configuration schemes, see *Application Brief 33 (Configuring FLEX 8000 Devices)*.

continuity checking A test for open circuits between device pins and programming adapter sockets. This test verifies that a device is properly seated in the socket of the adapter.

CQFP Ceramic Quad Flat Pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

D

Database Builder The MAX+PLUS II Compiler module that builds a single, fully flattened database that integrates all files in a project hierarchy. It also examines the logical completeness and consistency of the project and checks for boundary connectivity and syntactical errors.

dedicated input pin A pin that may only be used as an input to the device.

device An Altera programmable logic device, including Classic, MAX 5000/EPS464, MAX 7000, FLEX 8000, EPS448, EPB2001, and Configuration EPROM devices.

device family A group of Altera programmable logic devices with the same fundamental architecture. Altera device families are the Classic, MAX 5000/EPS464, MAX 7000, FLEX 8000, and Configuration EPROM families.

E

EDIF Electronic Design Interchange Format. An industry-standard format for transmitting design data. AN EDIF 2 0 0 or 2 9 0 netlist filke is generated from a schematic design or a VHDL or Verilog design that has been processed with an industry-standard synthesis tool. The netlist file is then imported into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can generated one or more EDIF Output Files (**.edo**) in EDIF 2 0 0 or 2 9 0 format that contain functional and timing information for simulation with a standard EDIF simulator.

EEPROM Electrically Erasable Programmable Read-Only Memory. A form of reprogrammable semiconductor memory in which the contents can be erased by subjecting the device to appropriate electrical signals.

EPLD Erasable Programmable Logic Device, i.e., an Altera device that is a member of the Classic, MAX 5000/EPS464, or MAX 7000 family.

EPROM Erasable Programmable Read-Only Memory. A form of reprogrammable semiconductor memory whose contents can be erased by subjecting the device to ultraviolet light of the proper wavelength. See *Operating Requirements for Altera Devices* and *Technology & Reliability* for more information.

expander product term A single product term with an inverted output that feeds back into the Logic Array Block (LAB) of a MAX 5000/EPS464 or MAX 7000 device. An uncommitted expander product term that can be shared with other logic cells in the same LAB is called a shareable expander; a product term that has been shared in this manner is called a shared expander. In MAX 7000 devices only, an expander product term borrowed from an adjacent logic cell in the same LAB is called a parallel expander.

external timing parameters Factory-tested, guaranteed worst-case values. Examples: t_{PD1}, t_{CO1}, f_{CNT}. In FLEX 8000 device data sheets, external timing parameters are listed under "External Reference Timing Characteristics."

extraction tool A tool to extract QFP devices from QFP carriers. Two extraction tools are available from Altera: one for 100-pin QFPs and one for 160- and 208-pin QFPs.

F

family-specific macrofunction An Altera-provided macrofunction that contains logic optimized for the architecture of a specific device family. The functionality of a family-specific macrofunction is always the same, regardless of the device family for which it is designed. However, primitives and nodes used within the macrofunction file can vary from family to family to take advantage of different device architectures, providing higher performance and more efficient implementation.

FastTrack Interconnect Dedicated connection paths that span the entire width and height of a FLEX 8000 device. These connection paths allow signals to travel between all Logic Array Blocks (LABs) in a device.

Fitter The MAX+PLUS II Compiler module that fits a project into one or more devices. The Fitter selects appropriate interconnection paths, and pin and logic cell assignments. It also creates a Report File (**.rpt**) and Fit File (**.fit**) for the project.

FLEX Download Cable A cable used to download SRAM Object File (**.sof**) data in a passive serial (PS) configuration scheme to a FLEX 8000 device in an in-system circuit. FLEX 8000 devices can be configured with the FLEX Download Cable to allow functional testing and prototyping on the circuit board.

FLEX 8000 An Altera device family based on Flexible Logic Element MatriX architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices. The family includes the EPF8282, EPF8282V, EPF8452, EPF8820, EPF81188, and EPF81500 devices.

flipflop or **register** An edge-triggered, clocked storage unit that stores a single bit of data. A low-to-high transition on the Clock signal changes the output of the flipflop, based on the value of the data input(s). This value is maintained until the next low-to-high transition of the Clock, or until the flipflop is preset or cleared. Depending on the architecture of the device family, a register can be programmed as a level-sensitive flow-through latch or as an edge-triggered D,T, JK, or SR flipflop.

functional simulation A MAX+PLUS II Simulator mode that uses a functional Simulator Netlist File (**.snf**) to simulate the logical performance of a project without timing information.

Functional SNF Extractor The MAX+PLUS II Compiler module that creates the functional Simulator Netlist File (**.snf**) required for functional simulation.

G

global Clear A signal from a dedicated input pin that does not pass through the logic array before arriving at the Clear input of a register. In FLEX 8000 devices, a global Clear can come from any of the dedicated inputs. MAX 7000 devices have input pins that can be used either as global Clear sources or dedicated inputs to the device.

global Clock A signal from a dedicated input pin that does not pass through the logic array before arriving at the Clock input of a register. In FLEX 8000 devices, a global Clock can come from any of the four dedicated input pins. MAX 7000, MAX 5000, EPS464, and EP1810 devices have input pins that can be used either as global Clock sources or dedicated inputs to the device. EP910, EP910A, EP610, EP610A, and EP330 devices have dedicated Clock iput pins.

H

Hexadecimal (Intel-Format) File (.hex) A hexadecimal file that supports the Active Parallel Up (APU) and Active Parallel Down (APD) configuration schemes for FLEX 8000 devices.

I

interconnect timing parameters Internal timing parameters for the interconnect in FLEX 8000 devices.

internal timing parameters Worst-case delays based on external timing parameters. Internal timing parameters cannot be measured explicitly, and should be used only for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance. Examples: t_{LAD}, t_{CGEN}, t_{CLR}. In FLEX 8000 device data sheets, internal timing parameters are listed under "Internal Timing Characteristics."

J

JEDEC File (.jed) An ASCII file that contains programming information. JEDEC Files provide an industry-standard format for transferring information between a data preparation system and a logic device programmer. The MAX+PLUS II Programmer can optionally save programming data in JEDEC File format and use a JEDEC File to program the following Altera devices: EP330, EP610, EP610A, EP910, EP910A, EP1810, EPM5016, and EPM5032 devices.

The Programmer can also use JEDEC Files generated by A+PLUS software to program Classic devices.

JLCC Ceramic J-Lead Chip Carrier. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

JTAG Joint Test Action Group. A set of specifications that enables board- and chip-level functional verification of a board during production.

L

library of parameterized modules (LPM) A technology-independent library of logic functions. The LPM standard is built upon and follows the syntax of the EDIF 2 0 0 standard. Parameterized modules from the LPM support architecture-independent design entry for Altera Classic, MAX 5000/EPS464, MAX 7000, and FLEX 8000 devices. The MAX+PLUS II Compiler's EDIF Netlist Reader module includes built-in compilation support for many parameterized modules in the LPM.

linked simulation A MAX+PLUS II Simulator mode that uses a linked Simulator Netlist File (**.snf**) to simulate the logical performance of a project consisting of multiple, linked individual projects. A linked simulation uses the timing and/or functional netlist information from the combined SNFs of these individual projects.

Linked SNF Extractor The MAX+PLUS II Compiler module that creates the linked Simulator Netlist File (**.snf**) required for multi-project simulation.

Logic Array Block (LAB) A physically grouped set of logic resources in an Altera device. The LAB consists of a logic cell array and, in some device families, an expander product term array. Any signal that is available to any one logic cell in the LAB is available to the entire LAB. In Classic devices, the logic in the LAB shares a global Clock signal. The LAB is fed by a global bus and a dedicated input bus. (In the *EP1810 Data Sheet*, a LAB is called a quadrant.) In MAX 5000 and MAX 7000 devices, the LAB is fed by a Programmable Interconnect Array (PIA) and a dedicated input bus; in FLEX 8000 devices, the LAB is fed by row interconnect paths and a dedicated input bus.

logic cell The generic term for a basic building block of an Altera general-purpose logic device. In EPLDs (Classic, MAX 5000/EPS464, and MAX 7000 devices), the logic cell is called a macrocell. In FLEX 8000 devices, the logic cell is called a logic element.

logic element (LE) A basic building block of an Altera FLEX 8000 device. A logic element consists of a look-up table (LUT)—i.e., a function generator that quickly computes any function of four variables—and a programmable register to support sequential functions. The register can be programmed to emulate a flow-through latch; a D, T, JK, or SR flipflop; or it can be bypassed entirely for pure combinatorial logic. The register can feed other logic elements or feed back to the logic element itself. Some logic elements feed output or bidirectional I/O pins on the device.

Logic elements have "numbers" of the format LC<*number*>_<*LAB name*>, where <*number*> ranges from 1 to 8 and <*LAB name*> consists of the row letter and column number of the Logic Array Block (LAB).

logic element timing parameters Internal timing parameters for the logic elements in FLEX 8000 devices.

Logic Programmer card The LP4, LP5, or LP6 expansion card required to run the MAX+PLUS II Programmer and program Altera devices.

Logic Synthesizer The Compiler module that uses several algorithms to minimize gate count, remove redundant logic, and utilize the device architecture as efficiently as possible.

look-up table (LUT) A function that generates outputs based on inputs and a set of stored data. The logic element of FLEX 8000 devices includes a four-input LUT that can be configured to emulate any logical function of four inputs.

M

macrocell A basic building block in Altera Classic, MAX 5000/EPS464, and MAX 7000 devices. A macrocell consists of two parts: combinatorial logic and a configurable register. The combinatorial logic allows a wide variety of logic functions. Depending on the architecture of the device family, the register can be programmed to emulate a flow-through latch; a D, T, JK, or SR

flipflop; or it can be bypassed entirely for pure combinatorial logic. The register can feed other macrocells or feed back to the macrocell itself. Some macrocells feed output or bidirectional I/O pins on the device. Macrocells have numbers of the format LC<*number*>.

Master Programming Unit (MPU) A logic device programming box. The MPU works with zero-insertion-force sockets and individual adapters to program and test Altera devices. The PL-MPU base unit and adapters with the prefix "PLM" support both device programming and device testing. The PLE3-12A unit and other adapters (e.g., adapters with the prefix "PLE" and the PLAD3-12 adapter) support device programming only.

MAX 5000/EPS464 An Altera device family based on the first generation of Multiple Array MatriX architecture. This EPROM-based device family includes EPM5016, EPM5032, EPM5064, EPS464, EPM5128, EPM5128A, EPM5130, EPM5192, and EPM5192A devices.

MAX 7000 An Altera device family based on the second generation of Multiple Array MatriX architecture. These EPROM- and EEPROM-based devices include EPM7032, EPM7032V, EPM7064, EPM7096, EPM7128, EPM7160, EPM7192, and EPM7256 devices.

MAX+PLUS II Altera's Multiple Array MatriX Programmable Logic User System. MAX+PLUS II is a set of computer programs and hardware support products that allow design and implementation of custom logic circuits with Classic, MAX 5000/EPS464, MAX 7000, and FLEX 8000 devices.

MPLD Mask-Programmed Logic Device, i.e., a custom Altera device created by converting a design originally created for an EPLD or FLEX 8000 device. Altera offers a program for converting customer designs into MPLDs, which are cost-effective alternatives for high-volume production.

MQFP Metal Quad Flat Pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

P

parallel expander An expander product term that is borrowed from an adjacent logic cell in the same MAX 7000 Logic Array Block (LAB). Parallel Expanders is also a logic option that can be applied to a logic function to allow it to borrow such parallel expanders. This option can reduce the number of expander product terms required in a project and increase the speed of the project. However, the project may use additional logic cells, and may be more difficult to fit.

Passive Parallel Asynchronous (PPA) A configuration scheme in which a CPU loads the FLEX 8000 device via a common data bus. This configuration scheme is used for a system in which multiple devices require initialization. In this scheme, the FLEX 8000 device accepts a parallel byte of input data, and then serializes that byte using its internal synchronization Clock. Intelligent handshaking between the CPU and the FLEX 8000 device allows the CPU to configure multiple FLEX 8000 devices simultaneously. MAX+PLUS II can generate Tabular Text Files (**.ttf**) that contain the data for configuring FLEX 8000 devices in an PPA configuration scheme.

Passive Parallel Synchronous (PPS) A configuration scheme in which a CPU loads the FLEX 8000 device via a common data bus. Data is latched by the FLEX 8000 device on the first rising edge of a CPU-driven Clock signal. The next eight Clock pulses serialize this latched data within the FLEX 8000 device. The tenth rising edge of the Clock signal causes the FLEX 8000 to latch the next 8-bit byte of data. MAX+PLUS II can generate Tabular Text Files (**.ttf**) that contain the data for configuring FLEX 8000 devices in a PPS configuration scheme.

Passive Serial (PS) A configuration scheme in which an external controller is used to configure a FLEX 8000 device with a serial bit-stream. The external controller can be the MAX+PLUS II Programmer or an intelligent host, such as a microcontroller or a CPU.

PDIP Plastic Dual In-Line Package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

peripheral register A register that exists on the periphery of a FLEX 8000 device. Peripheral Register is also a logic option that specifies that a register should be implemented in a peripheral register.

PGA Ceramic Pin-Grid Array. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

PLAD3-12 An adapter that plugs into the Master Programming Unit (MPU). It allows the designer to use adapters with the prefix "PLE" designed for use with the PLE3-12A programming unit. It also directly supports programming of EP330 devices in DIP packages.

PLCC Plastic J-Lead Chip Carrier. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

Programmable Interconnect Array (PIA) The portion of a MAX 5000 or MAX 7000 device that routes signals between different Logic Array Blocks (LABs).

Programmer Object File (.pof) A binary file generated by the Compiler's Assembler module. It contains the data used by the MAX+PLUS II Programmer to program an Altera device.

PQFP Plastic Quad Flat Pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

product term Two or more factors in a Boolean expression combined with an AND operator constitute a product term, where "product" means "logic product."

programming file A file containing data for programming Altera devices. Both the MAX+PLUS II Compiler and Programmer can generate programming files. The following programming file formats are available in MAX+PLUS II:

Hexadecimal (Intel-Format) File (**.hex**)
JEDEC File (**.jed**)
Programmer Object File (**.pof**)
SRAM Object File (**.sof**)
Tabular Text File (**.ttf**)

POFs, SOFs, and JEDEC Files are used to program devices with the MAX+PLUS II Programmer. Hex files and TTFs are used to configure FLEX 8000 devices by other means. JEDEC Files generated by A+PLUS software can also be used to program Classic devices. The Programmer can save data read from an examined device in POF or JEDEC File format.

project A project consists of all files that are associated with a particular design, including all subdesign files and related ancillary files created by the user or by MAX+PLUS II software. The project name is the same as the name of the top-level design file in the project. MAX+PLUS II performs compilation, simulation, timing analysis, and programming on only one project at a time.

R

removal tool A tool to remove a QFP device in a carrier from a development socket. Two removal tools are available from Altera: one for 100-pin QFPs and one for 160- and 208-pin QFPs.

RQFP Power Quad Flat Pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

S

SAM+PLUS Altera's Stand-Alone Micro-sequencer (SAM) Programmable Logic User System. SAM+PLUS is a set of computer programs and hardware support products that facilitate design and implementation of custom logic circuits with the EPS448 device.

Security Bit A bit that prevents an Altera device from being interrogated or inadvertently reprogrammed. It can be turned on or off for each device in a project, or for the entire project.

shared expanders and **shareable expanders** A feature of MAX 5000/EPS464 and MAX 7000 device architecture that allows logic cells to use uncommitted product terms within the same Logic Array Block (LAB). A product term that can be shared in this manner is called a shareable expander; a product term that is shared in this manner is called a shared expander. The MAX+PLUS II Compiler automatically allocates shareable expanders when a project is compiled. A shared expander can be allocated with an EXP primitive.

software guard A device that attaches to the parallel printer port on a computer. It is required to run MAX+PLUS II software.

SOIC Plastic Small-Outline Integrated Circuit. A device package offered by Altera. See *Altera Device Package Outlines and Ordering Information* for more information.

SRAM Static Read-Only Memory. A read-write memory that stores data in integrated flipflops. See *Technology & Reliability* for more information.

SRAM Object File (.sof) A binary file, generated by MAX+PLUS II, that contains the data for configuring an Altera FLEX 8000 device via the FLEX Download Cable.

T

Tabular Text File (.ttf) An ASCII text file in tabular format that supports the Passive Parallel Synchronous (PPS) and Passive Parallel Asynchronous (PPA) configuration schemes for configuring FLEX 8000 devices.

timing simulation A MAX+PLUS II Simulator mode that uses a timing Simulator Netlist File (**.snf**) to simulate the logical and timing performance of a project. Since the timing SNF is generated after logic synthesis, partitioning, and fitting are performed, only the nodes that have not been removed by logic optimization are simulated.

Timing SNF Extractor The Compiler module that creates the timing Simulator Netlist File (**.snf**), which contains the functional and timing data for the fully optimized project. This file is used for timing simulation and timing analysis. The Compiler's EDIF Netlist Writer module also uses timing SNFs to generate EDIF Output Files (**.edo**).

TQFP Thin Quad Flat Pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* for more information.

Turbo Bit A control bit for choosing speed and power characteristics of Altera Classic and MAX 7000 devices. If the Turbo Bit is on, the speed increases; if it is off, the power consumed decreases. The Turbo Bit may be turned on or off in a design file or the Compiler. In Classic devices, the Turbo Bit applies to the entire device. In MAX 7000 devices, it applies to individual logic cells within a device. The Turbo Bit is not available in MAX 5000/EPS464 and FLEX 8000 devices.

U

user I/O The total number of I/O pins and dedicated inputs on a device.

V

Verilog A hardware description language from Cadence. You can generate an EDIF 2 0 0 or 2 9 0 netlist file from a Verilog design that has been processed with a Verilog synthesis tool, then import the file into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a Verilog Output File (**.vo**) that contains functional and timing information for simulation with a standard Verilog simulator.

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language. You can generate an EDIF 2 0 0 or 2 9 0 netlist file from a VHDL design that has been processed with a VHDL synthesis tool, then import the file into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a VHDL Output File (**.vho**) that contains functional and timing information for simulation with a standard VHDL simulator.

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