Spring 1994

AMCC
Applied Micro Circuits Corporation

Computer Products Data Book

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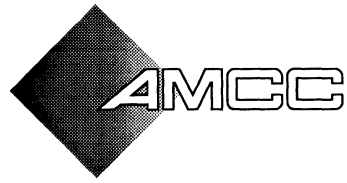

Computer Products Databook

For Marketing and Application Information Contact:

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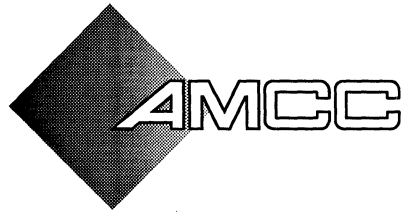
The material in this document supersedes all previous documentation issued for any of the products included herein.



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			Number	Type	Max Freq.			
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Q20004	1 Micron Bipolar	671	28	None	8-3
Q20010	1 Micron Bipolar	1469	66	None	8-3
Q20P010	1 Micron Bipolar	928	34	1 GHz PLL	8-15
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Q24008	1 Micron BiCMOS	760	44	None	8-25
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Q24021	1 Micron BiCMOS	2160	80	None	8-25
Q24060	1 Micron BiCMOS	5760	132	None	8-25
Q24091	1 Micron BiCMOS	9072	160	None	8-25
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NOTES

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Corporate Summary 2

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Company Overview

AMCC defines, develops, manufactures and markets high performance application specific standard products (ASSPs) and application specific integrated circuits (ASICs).

AMCC has over ten years of specific expertise in bipolar and BiCMOS semicustom design methodologies and process technologies, and extensive knowledge of the semiconductor industry. This expertise, when combined with a focus on systems level problem solving, enables AMCC to rapidly design, prototype and produce in volume, targeted high performance, systems oriented integrated logic circuits (ICs).

Since 1982, AMCC has designed and produced five generations of semicustom bipolar ECL logic arrays and two generations of BiCMOS logic arrays. AMCC ASIC expertise includes its mixed ECL/TTL interface, phase-locked loop (PLL), precision vernier, "Turbo" drivers, skew control, high-speed VCO and controlled edge rate output. AMCC uses its ASIC methodology to quickly and cost effectively implement standard products—the ASSPs. ASSPs include precision clock and timing and telecom/datacom high performance network products.

AMCC's long-standing focus on high performance semicustom ICs has enabled the Company to cement long-lasting relationships with many industry leaders. Through these relationships, AMCC has developed extensive systems expertise in data communications, telecommunications, computers and computer support, bus interface and test and instrumentation. AMCC has earned a reputation for producing high quality products.

Strategic Partnerships

AMCC manufactures its own 1.0 micron BiCMOS and Bipolar wafers using proven processes. The Company follows a "semi-fabbed" manufacturing strategy. AMCC has reciprocal foundry relationships in place with major domestic and international semiconductor partners that provide for significant additional production capacity. Wafer purchases from strategic foundry partners both expand capacity and provide alternate sources.

Additional high-volume assembly and test facilities are located offshore.

AMCC's "quick turn, semi-fabbed" manufacturing approach blends together the strengths of both the "fabbed" and "fabless" semiconductor strategies. Fabbed advantages include the security of total in-house control and time to market. Fabless advantages include multiple sourcing and allows the company to focus investment on new high performance products.

AMCC has long recognized that in an increasingly competitive semiconductor marketplace, no one company can excel in every discipline. As a result, the Company has a successful history of strategic partnerships in both process and product development that continues today. Many of the Company's ASSPs have been co-developed through partnership agreements.

Network Products

High performance networking encompasses a wide range of applications, all requiring data transmission rates from > 100 Mbit per second to 1 Gbit per second, and beyond. These applications include computer data transmission, fiber-optic telecommunications transmission systems, digital video broadcasting and many more.

AMCC's network products are designed in tandem with emerging industry standards. AMCC has introduced more than 15 ASSP products designed to implement ANSI or CCITT approved communications standards such as the High Performance Parallel Interface (**HIPPI**), **Fibre Channel,** the Synchronous Optical Network (**SONET**) and Asynchronous Transfer Mode (**ATM**) telecommunications standards.

AMCC's close working relationship with the companies developing and proposing these standards has helped AMCC to garner an excellent position in the high-speed networking arena. AMCC's HIPPI chipset, for example, was the industry's first complete implementation of the HIPPI specification. The Fibre Channel and SONET chip sets provide a highly integrated, rapidly implemented interface solution. These joint projects allow AMCC to remain at the forefront of the emerging network technologies.

Computer Products

AMCC provides a growing line of precision clock and timing standard products for exacting system designs. AMCC has also tailored clock and timing devices to specific customer needs for high performance clock generation and distribution, clock synchronization and de-skewing, frequency synthesis, and pulse shaping applications. Offerings include low jitter, low skew clock drivers and clock generators aimed at high performance workstation applications.

AMCC computer products provide high performance while minimizing emission through noise reduction. They fulfill the designer's requirements of low-skew, high speed and low-noise.

Military

AMCC has provided high performance integrated circuits to the military market since it was founded in 1979. AMCC's familiarity with the military's unique requirements and the company's flexibility to meet these requirements have been instrumental in its success in this market.

NOTES

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AMCC Commitment to Quality

Quality is the degree to which a product meets a customer's expectations with regard to delivery time, cost, and performance to the requirements of the application.

Reliability is "...the probability of a product performing, without failure, a specified function under given conditions for a specified period of time".[1]

AMCC is committed to achieving the highest quality and reliability level in the integrated circuit products we provide. Every year for over a decade we have established industry-leading reliability and outgoing quality targets and then beat them.

The quality and reliability philosophy at AMCC starts with the premise that for AMCC to continue to excel in the ever expanding market place, the quality expectations of customers must be met or exceeded.

Our team operating philosophy is to:

1) design in manufacturability and reliability during the new product development phase;

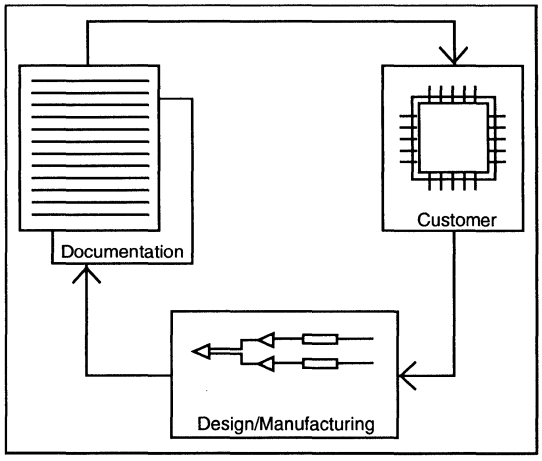
2) build in quality at all manufacturing steps;

3) execute thorough product inspections and reliability confirmation;

4) incorporate feedback from internal and external sources into continuous quality improvement programs.

Reliability and Manufacturability - Designed In From The Start

Reliability and manufacturability are designed in through active participation in product reviews by design, manufacturing, and reliability engineering. This is followed by extensive characterization and qualification testing of the new products and processes.



QA gates and subsequent feedback ensures quality confirmation of AMCC's final product in a continuous improvement program

Quality Built In During Wafer Fabrication and Manufacturing

AMCC's manufacturing and quality teams employ in-process inspections and the SPC methodology to provide assurance of continued process control and compliance to specification.

Inspection And Reliability Confirmation

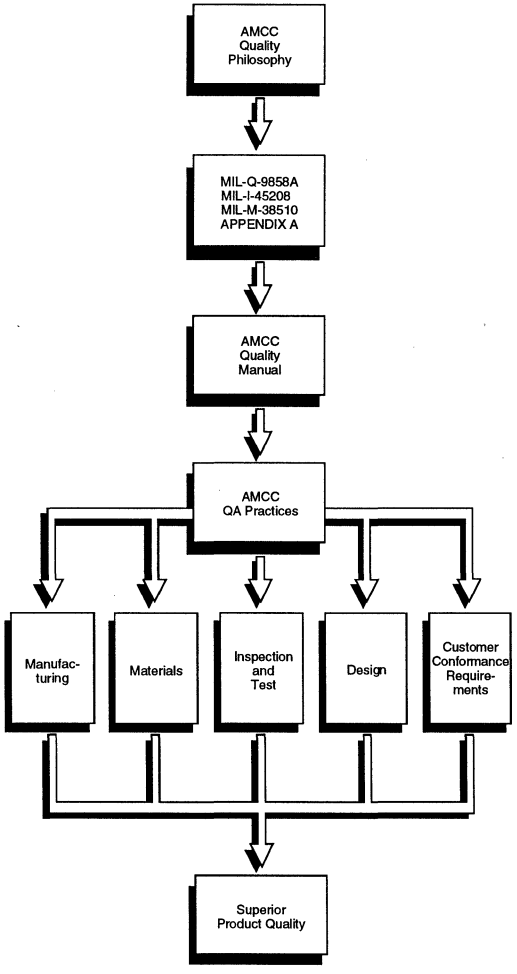
- IPQC (In-Process Quality Control) gates strategically placed to verify customer requirements and to provide feedback data for process monitoring and improvement
- Final outgoing inspection gate
- MIL-STD-105D sampling program
- Group A and B testing
- Reliability monitors

[1] JURAN

QUALITY SYSTEM OVERVIEW

Continuous Quality Improvement Program

- Corporate-wide commitment driven by the Executive Staff
- A program plan that is flexible enough to comprehend dynamic customer inputs
- Statistical tools in place for analysis and action planning
- Weekly and monthly review meetings to share performance data
- Self examination consistent with elements in the Malcolm Baldridge National Quality Award



AMCC QUALITY SYSTEM

The Quality System at AMCC is modeled on the most stringent of military requirements. Elements of MIL-Q-9858A, MIL-STD-883, and MIL-M-38510 Appendix A have been combined with a baseline MIL-I-45208 Quality program to achieve the overall corporate philosophy.

AMCC's Quality System has the following components integrated throughout the factory to meet or exceed the above requirements.

- Quality Organization
- Quality Planning
- Work Instructions
- Record Maintenance and Storage
- Corrective Action
- Cost-of-Quality Reporting
- Non-Conforming Material Control
- Statistical Quality Control
- Inspection Status System
- Vendor Control
- Document Change Control System
- Calibration Purchase Control
- Material Control
- Production Processing and Fabrication Auditing System
- Inspection and Test
- ESD Safe Handling Control
- Training/ Certification
- Shelf Life Storage Control

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PRODUCT QUALIFICATIONS

A qualification is a sequence of tests in which all parameters, including the reliability of the device are tested. It is this sequence of tests which **initially qualifies** the part to be released for production.

For the military, it is typically required that parts pass stringent qualification procedures before production is started or product is shipped.

AMCC provides MIL-STD-883 Methods 5005, 5008, and 5010 testing for our military customers on contract.

MIL-STD-883 Method 5005

"Qualification And Quality Conformance Procedures"

Method 5005 establishes qualification and quality-conformance inspection procedures for semiconductors to ensure that the quality of devices and lot conform with the requirements of the applicable procurement document. The full requirements of Group A, B, C, D, and E test and inspections are intended for use in initial device qualification - or requalification in the event of product or process change - and in periodic testing for retaining qualification.

Group A consists of electrical tests performed on an inspection lot which has already passed the 100% screening requirements. After a lot has passed the 100% screen tests, a random sample of parts is selected from the total population of devices to form the inspection lot. The inspection lot is then subjected to these Group A electrical tests.

Group B inspection tests are used to monitor the fabrication and assembly processes performed on each inspection lot.

Group C consists of a 1000-hour life test conducted to verify die integrity.

Group D verifies the material integrity and the reliability of the package.

Group E demonstrates the radiation hardness capability of the device. Performed on a generic basis by device type or as required for an application.

MIL-STD-883 Method 5010

"Test Procedures For Custom Monolithic Microcircuits"

This method establishes screening and quality conformance procedures for the testing of custom and semicustom monolithic semiconductors to verify Class B or Class S quality and reliability levels. Testing is performed in conjunction with other documentation such as MIL-M-38510 and an applicable detail specification. It establishes the design, material, performance, control, and documentation requirements needed to achieve prescribed levels of device quality and reliability. AMCC can support qualification using this method.

Until August of 1983, the qualification most commonly used was Method 5005. Since that time, the newer revision of MIL-STD-883 includes Method 5010, which is better suited for semicustom devices (logic arrays included). Either qualification is adequate, but it is desirable to use the 5010 qualification procedure in qualifying custom or semicustom devices.

Qualification Method 5005 VS. 5010

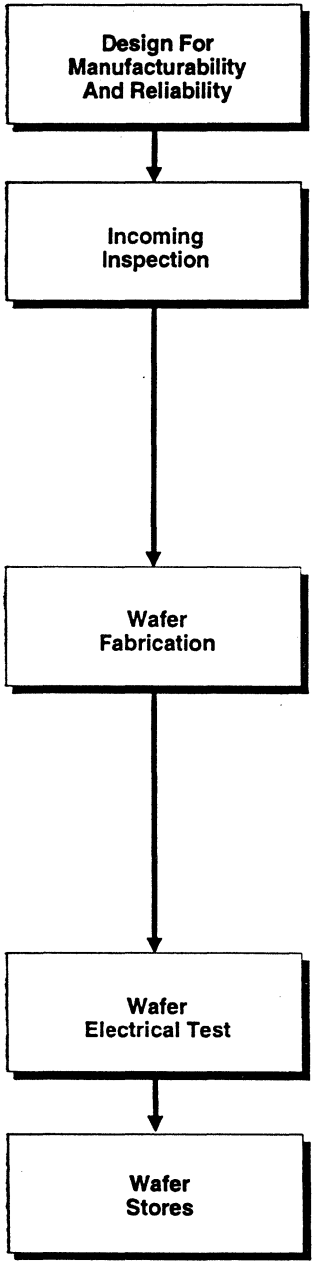
The primary difference between the two methods is in the Group D test. Method 5005 uses electrically-good devices, where method 5010 uses electrical rejects and package-only parts for environmental tests. In addition, Method 5010 is designed for smaller production releases (i.e., 2000 devices/year) while Method 5005 is designed for large production releases.

Generic Data

Under the provision of MIL-STD 38510 a customer can elect to qualify using generic data (similar device/ family). However, the provisions of the applicable contract should be reviewed. In most cases generic data will satisfy full qualification requirements.

Since many of the qualifications at AMCC are on-going, generic data may be available for this purpose.

AMCC Product Assurance Product Flow Detail



- Component Selection
  - Definition - Specification
  - Vendor: Selection - Qualification - Approval
  - Qualified Vendors List (QVL)

- Acceptance Documents and Operating Procedures
  - Purchase Order
  - Component/Material Specifications
  - Product Assurance and General Procedures
  - QVL
  - Inspection of All Direct Materials

- Class 10 Clean Room - FED-STD-209
- Measurements in Adherence with MIL-STD-977
- SPC:
  - In-process Monitors
  - PCM Electricals
- SEM Inspection on All Military Lots
- QA Audits:
  - CV Plots - Weekly (minimum)
  - DI Water - Weekly
    - Particle Counts
    - Bacteria Count
  - Airborne Particle Count - Weekly
  - LTO Tests - Weekly
    - % Phosporous
    - Pinholes
    - Uniformity
- IPQC
  - Base and Metal Final
- IPQC
  - Product Assurance Specifications
  - Manufacturing Test Procedures

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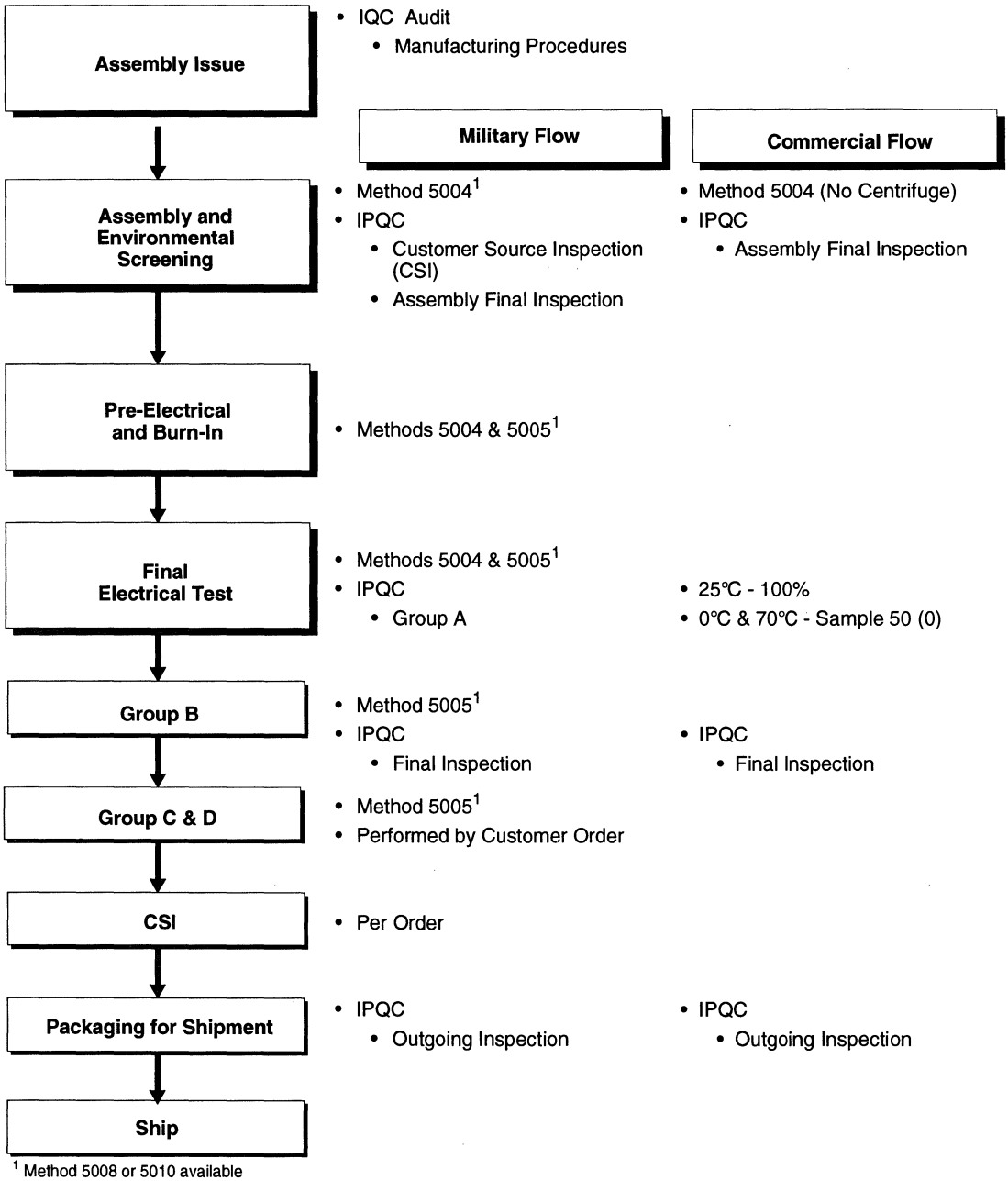
AMCC Product Assurance Product Flow Detail



[1] Method 5008 or 5010 available

- New/changed processes and material qualifications
- In-process Quality monitors
- Periodic operating life and environmental testing

New/Changed Wafer Processes and Material Qualifications

In order to initially release a device to production a standard set of MIL-STD-883 tests must be completed successfully. These tests include:

Wafer Process and Design

- Operating LifeMethod 1005
- ESD CharacterizationMethod 3015
- Wire Bond PullMethod 2011
- Thermal Shock or Method 1011 or 1010 Temperature Cycling

Package and Related Materials

- Selected Subgroups of MIL-STD-883, Method 5005, Group B and D

AMCC adheres to MIL-M-38510 with regards to changes.

If changes to production released devices are determined to be major, the appropriate qualification testing must be successfully completed prior to change approval.

In-Process Quality Monitors

- CV plots
- Airborne particle count
- Bacteria, particle count, and resistivity on DI water
- ESD work stations and procedures
- In-line testing of process gases
- In-line testing of LTO
- Temperature and humidity control
- SPC in wafer fabrication
- SEM of all military lots

Periodic Operating Life and Environmental Testing

- Performed on a product from each process family twice per year.
- 1000 hour operating life test (minimum), Method 5005, Group C.
- Temperature cycling per Method 1010, 100 cycles, condition C: -65°C / 150°C

Final Measure and Assurance of Quality

The cost of defects depends on when the failure occurs. For example, costs rise significantly as undetected defective ICs are integrated into systems. High quality parts cut costs substantially, and the extra quality built into every AMCC device means added value to our customers.

To achieve maximum quality, AMCC employs 100% testing of all devices, followed by stringent QA sampling.

AMCC performs QA sampling measurements at *full specification temperature, both DC and AC*, to achieve the tightest AQLs in the industry.

RADIATION HARDNESS

High energy radiation can cause structural changes in the silicon and silicon dioxide crystal lattice by displacing atoms from their normal crystal sites. These changes can be responsible for increased junction leakage, degraded transistor current gain (β), and increased parasitic Si/SiO2 interface leakage currents. The damage is generally induced by neutrons, X-rays, and gamma rays. The effects of the damage induced by this radiation can change both AC and DC parameters, affect functional performance, and, in severe cases, destroy the device.

Certain of AMCC's high performance products are inherently radiation resistant. The radiation resistance of AMCC IC's is the result of the small geometries, the structure of the fabrication process itself, and the use of ECL logic within the device. Contact your AMCC representative regarding radiation resistance characteristics associated with a specific product.

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Clock Drivers 3

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The design of high speed TTL/CMOS systems is often made more challenging and more difficult than their ECL and GaAs counterparts due to the poor transmission line behavior of the TTL device inputs. Since inputs from either TTL or CMOS devices provide essentially no termination to a given signal path (transmission line), reflections at the end of the line are a certainty. Nowhere in a system is this more noticeable and disastrous than when it occurs on the system's clock. It is here that the wrong choice for the clock driver can cripple the chance for success of a design.

There are many contradictions imposed on the "ideal" TTL clock driver. For example, slower edge rates reduce undershoot, ringing and plateau effects at the expense of duty cycle, frequency and clock skew; while faster edge rates cause overshoot, noise injection, and greater EMI radiation while trying to improve frequency, duty cycle and clock skew.

AMCC has solved this dilemma with an output driver circuit that is best described as having two modes for controlling the clock edges. This patented method produces a fast, crisp edge during the transition phase of the output waveform and then immediately slows the edge and becomes a closer match to the impedance of the external PC board. Figure 1 shows the representative effect of the "dual slope" on the falling edge of the clock. The output driver circuit actually uses the reflected wave to determine the appropriate inflection point for the slope and virtually eliminates "ground bounce".

Figure 1. "Dual Sloped" Output Driver Eliminates "Ground Bounce"

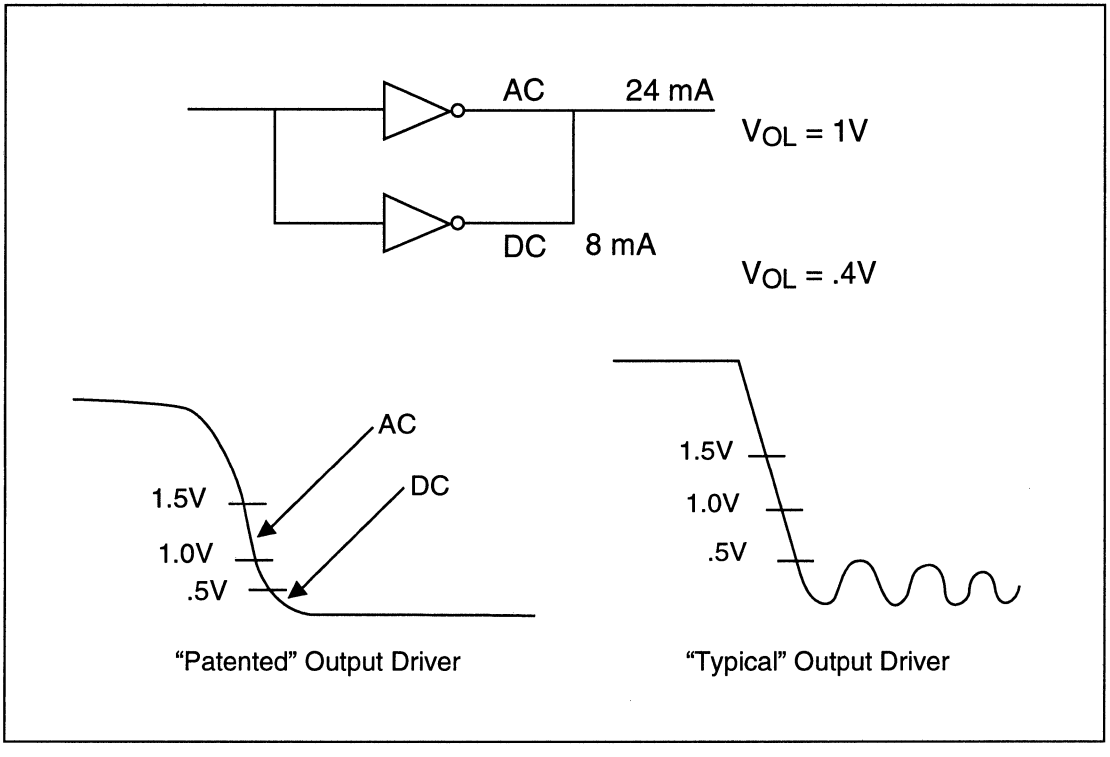


Figure 2 shows the representative effect of dynamically adjusting source series termination on the rising edge. By adjusting the built-in termination to individual loading environments, AMCC's clock drivers prevent "ringing" without the use of any additional on-board termination.

Figure 3 shows an unterminated 66MHz output of an SC35XX Series Driver. Conventional TTL output stages, with or without serial termination resistors, cannot attain both the **edge rates** *and* the **impedance matching** qualities achieved with the AMCC method.

Figure 2. Built-in, On-Chip Source (Series) Termination Minimizes "Overshoot"

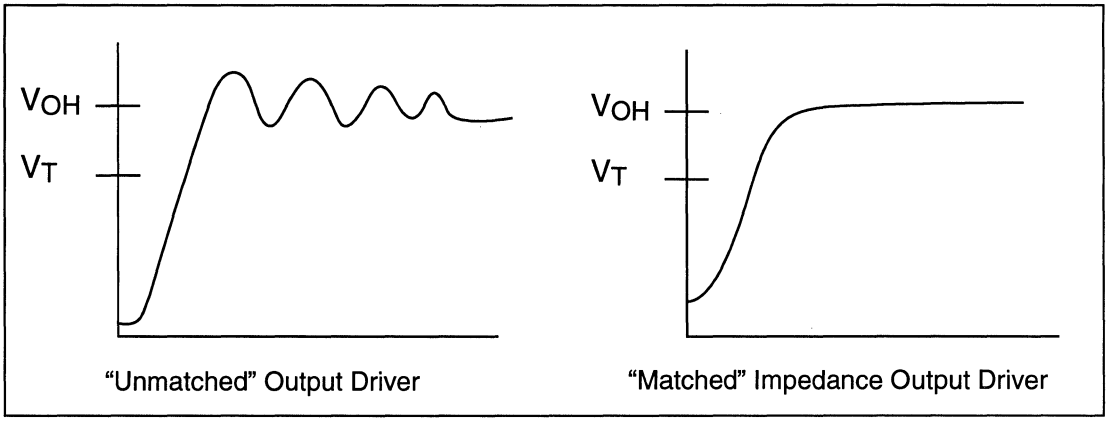
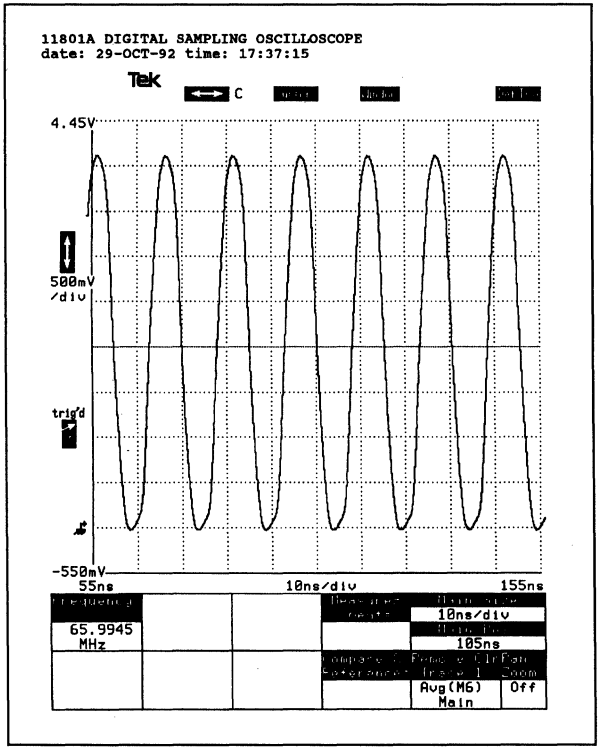


Figure 3. SC35XX Driver with 20pf Load and 8" of Trace



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20–OUTPUT CLOCK DRIVER SC3500

GENERAL DESCRIPTION

The SC3500 is a precision clock fan out driver. It requires a 2X frequency clock input from either a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20-clock outputs are divided into three groups. The first group of ten (10) outputs are unconditionally at the primary frequency, "Fa" = F input/2. The second group, "Fb", of five outputs can be selected to be either identical to "Fa" or at 1/2 the frequency of "Fa". The third group, "Fc", of five outputs, must be selected to be at either 1/2 or 1/4 of "Fa".

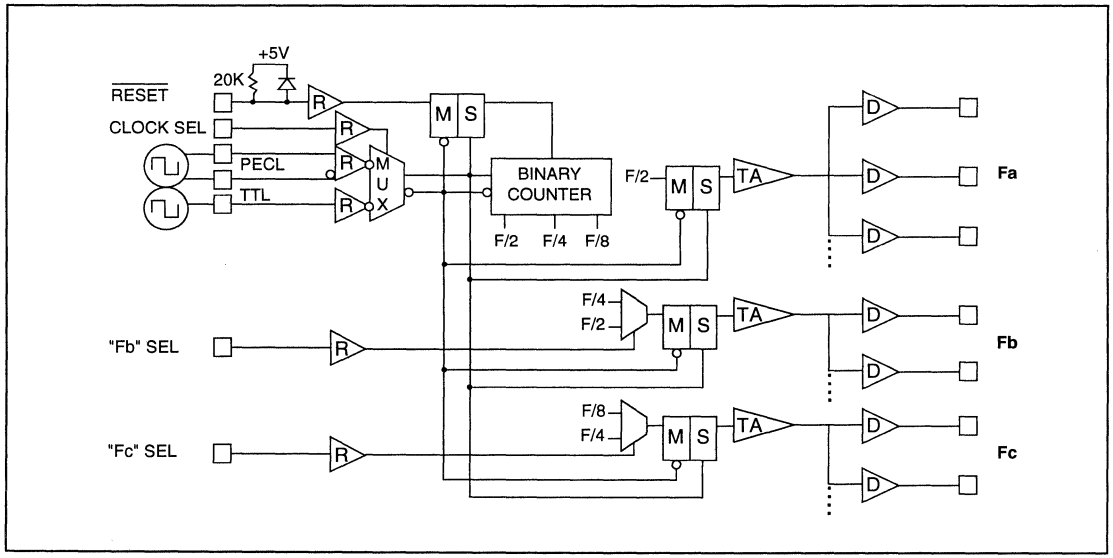
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs:**
  - Ten (10) outputs at primary frequency, up to 80 MHz
  - Five (5) outputs at primary or 1/2 primary frequency
  - Five (5) outputs at either 1/2 or 1/4 primary frequency
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground–bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground .....-0.5V to +7.0V
Input Voltage .....-0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature .....+140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

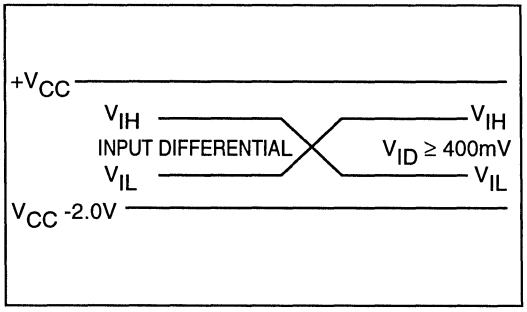
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-11)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL, CSEL, BSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		50	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL, CSEL, BSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-9 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3500 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3500 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3500 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications—Using AC Test Circuit (Page 3-11)

V_{CC} = +5.0V ± 5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3500–2	SC3500–1	SC3500	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	2.0	—	ns
Maximum Skew Across Fa Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	160	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

Notes:
1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 1.0 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip twenty output fan-out device using AMCC's advanced BiCMOS process. This design has optimized the device for clock symmetry and absolute minimum skew across all twenty outputs. Three harmonic clock frequency groups are provided that are user selectable.

For highest performance this approach requires a 2X clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator operating between +5V and ground can provide either differential ECL inputs (referenced to +5V - PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This 2X input clock will be fanned out to a divide down counter and to master-slave flip-flops for synchronization, refer to the logic diagram preceding. Using this methodology the output duty cycle asymmetry becomes largely a function of output driver slew rate into the AC load.

Two user select pins, "B select" and "C select", provide the "Fb" and "Fc" output (sub-harmonic) frequencies by way of multiplexor selection into the final resynchronizing flip-flops. The divide down counter outputs are 50% duty cycle decoded. The output resynchronizing flip-flops are keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated TTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset" — a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following five falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after five falling edge clock inputs, from a high (leading edge) count origin (see "Relative Output Timing", Page 3-10, and "Reset To Output Timing", in Clock Driver Application Note #1).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current.

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Clock Driver Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3500 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa	Fb	Fc
LO	LO	F	F/2	F/4	F/8
HI	LO	F	F/2	F/2	F/8
LO	HI	F	F/2	F/4	F/4
HI	HI	F	F/2	F/2	F/4

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non–crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3500 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3500 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-11 for complete load definition).

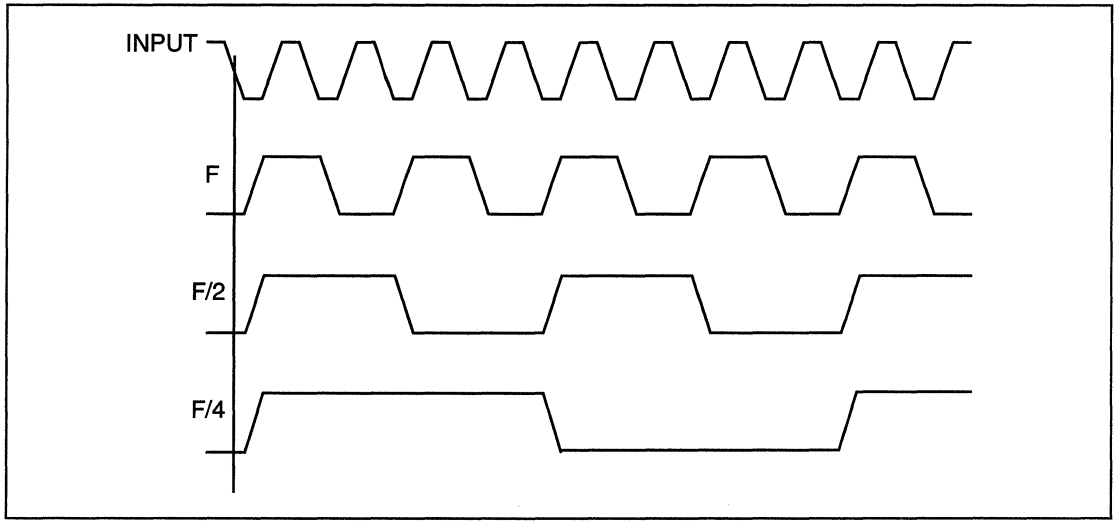
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3500 to determine the total power being dissipated by the SC3500. This total power is then multiplied by the SC3500's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3500. For greatest reliability, this junction temperature should not exceed 140°C.

	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: You have a SC3500 with 8 of the Fa outputs running at 66 MHz with 10 pF loads (8 x 47 = 376 mW + 2 x 16 = 32 mW for an Fa Total of 408 mW), 3 of the Fb outputs are running at 33 MHz with 5 pF loads (3 x 19 = 57 mW + 2 x 12 = 24 mW for an Fb Total of 81 mW), and 2 Fc outputs running at 33 MHz with 15 pF loads (2 x 24 = 48 mW + 3 x 12 = 36 mW for an Fc Total of 84 mW). The Total Chip Power is Core Power (400 mW) + Fa Power (408 mW) + Fb Power (81 mW) + Fc Power (84 mW) = 973 mW. Your design calls for a 70°C Still Air ambient. The SC3500's junction temperature would then be: 70°C + (.973 Watts x 50°C/Watt = 49°C) = 119°C, below the 140°C maximum.

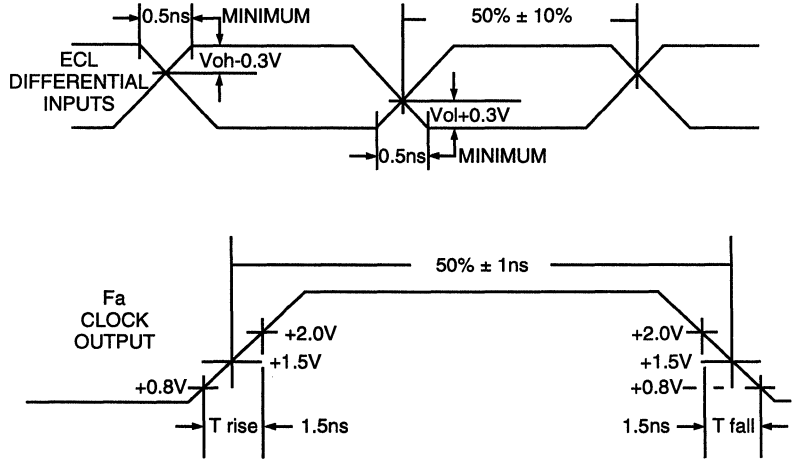
Relative Output Timing



Symmetry

The outputs of the SC3500 are nominally centered to provide a clean 50% duty cycle, symmetrical waveform at the +1.5V threshold reference. (See Threshold Crossing Characteristics diagram below for the conditions.)

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

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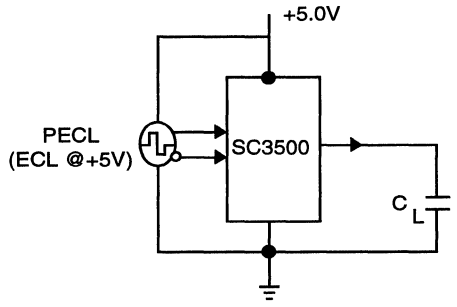
AC Test Circuit



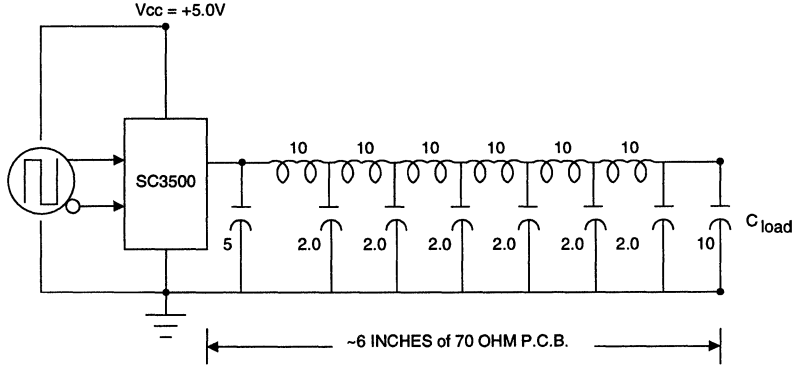
Designing the SC3500 for "Real Loads"

While the AC Test Circuit presented above can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3500 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3500 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz.

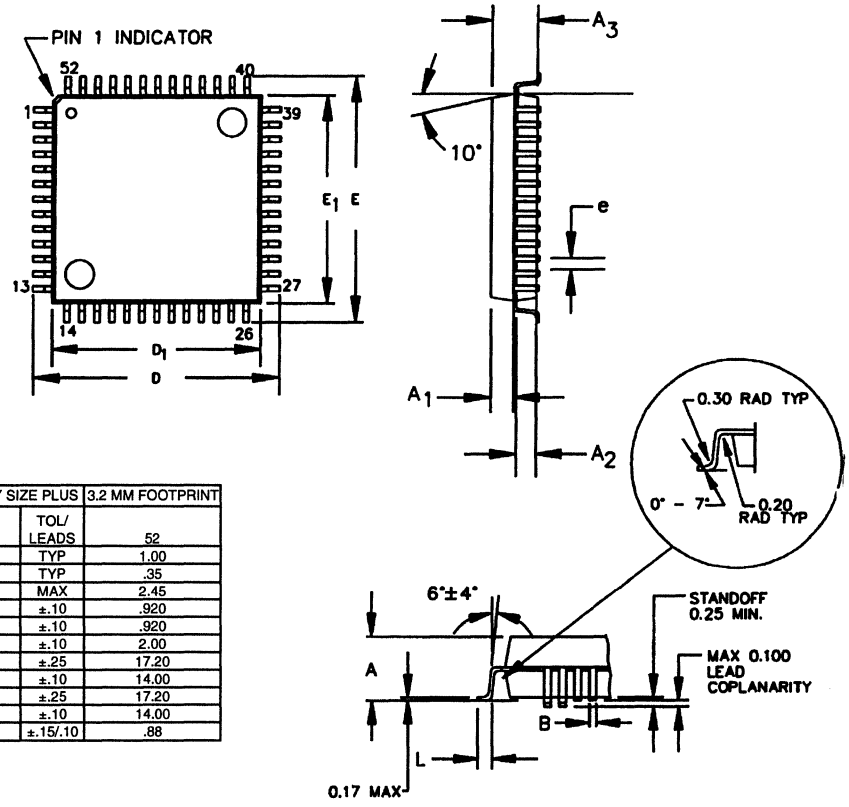
Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

52-Pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	14	CSEL	27	NC	40	TTL OSC
2	GND	15	GND	28	NC	41	GND
3	FB4	16	FA0	29	FC0	42	FA9
4	GND	17	VCC	30	GND	43	VCC
5	FB3	18	FA1	31	FC1	44	FA8
6	VCC	19	GND	32	VCC	45	GND
7	FB2	20	FA2	33	FC2	46	FA7
8	GND	21	VCC	34	GND	47	VCC
9	FB1	22	FA3	35	FC3	48	FA6
10	VCC	23	GND	36	VCC	49	GND
11	FB0	24	FA4	37	FC4	50	FA5
12	VCC	25	VCC	38	PECL OSCN	51	VCC
13	BSEL	26	NC	39	PECL OSCP	52	CLK SEL

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Ordering Information

Package Type	Max Skew Across All Outputs	Max Skew Chip-to-Chip	Part Number
52 Lead Quad Flat Pack	0.5 ns	1.0 ns	SC3500Q-2
52 Lead Quad Flat Pack	0.5 ns		SC3500Q–1
52 Lead Quad Flat Pack	1.0 ns		SC3500Q

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20-OUTPUT CLOCK DRIVER / INVERTER SC3502

GENERAL DESCRIPTION

The SC3502 is a precision clock fan-out driver. It requires a 2X frequency clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20-clock outputs are divided into four groups. The first group of five (5) outputs are unconditionally at the primary frequency, "Fa" =F input/2. The second group of five (5) outputs, "$\overline{Fa}$", are set at the same frequency, but are inverted. The third group of five (5) outputs, "Fb", can be selected to be either identical to "Fa" or at 1/2 the frequency of "Fa". The fourth group of five (5) outputs, "Fc", are inverted and can be selected to be at either 1/2 or 1/4 of "Fa".

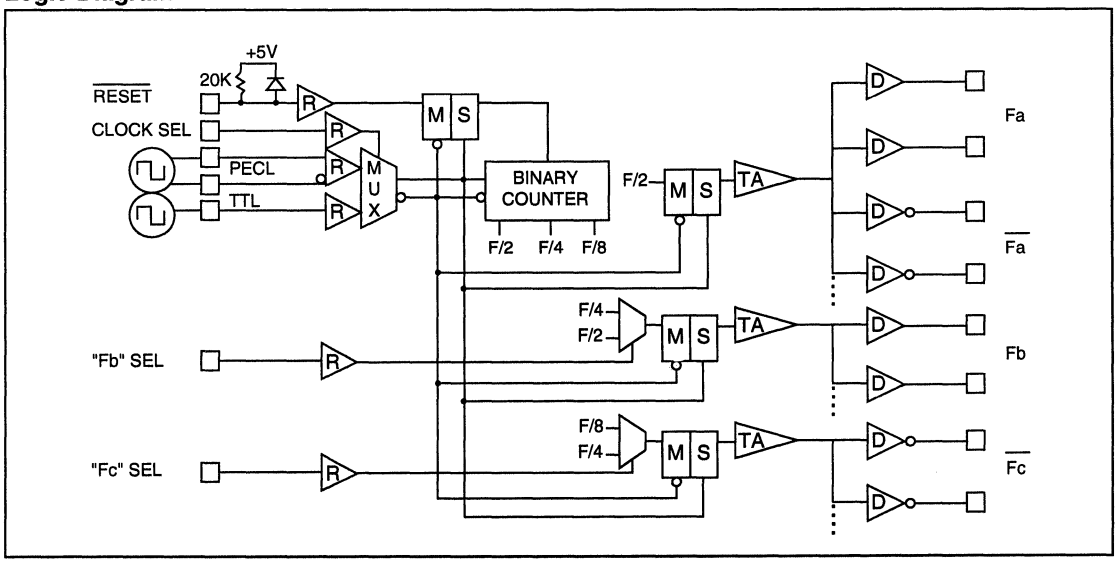
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize overshoot and undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs:**
  - Five (5) outputs at primary frequency, up to 80 MHz
  - Five (5) inverted outputs at the primary frequency, up to 80 MHz
  - Five (5) outputs at primary or 1/2 primary frequency
  - Five (5) inverted outputs at either 1/2 or 1/4 primary frequency
- **Leading edge skew for all outputs ≤1.0 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

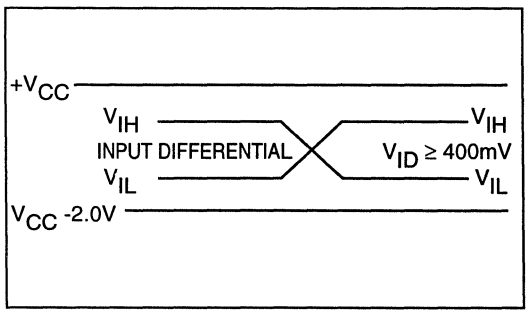
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-21)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including Clock	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including Clock	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-250	uA
	TTL, CSEL, BSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		50	uA
	Reset	V_{IN} = 0.5V		-375	uA
	TTL, CSEL, BSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-19 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3502 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



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AC Specifications - Using AC Test Circuit (Page 3-21)

Vcc = +5.0V ±5%, Ta = 0°C to +70°C, C_{LOAD} = 10pF

Parameter	SC3502-1	SC3502	UNITS
Maximum Skew Across All Outputs	1.0	1.5	ns
Maximum Skew Chip To Chip	2.0	—	ns
Maximum Skew Across Fa Outputs	0.25	0.25	ns
Maximum Skew Across $\overline{Fa}$ Outputs	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Skew Across $\overline{Fc}$ Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	MHz
Maximum Rising/Falling Edge Rates	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all non-inverted copies and the falling edge of all inverted copies
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
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For highest performance this approach requires a 2X clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V - PECL) to AMCC's Clock Driver or TTL (CMOS) levels. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This 2X input clock will be fanned out to a divide down counter and to master-slave flip-flops for synchronization, refer to the logic diagram preceding. Using this methodology the output duty cycle asymmetry becomes largely a function of output driver slew rate into the AC load.

Two user select pins, "B select" and "C select", provide the "Fb" and "Fc" output (sub-harmonic) frequencies by way of multiplexor selection into the final resynchronizing flip-flops. The divide down counter outputs are 50% duty cycle decoded. The output resynchronizing flip-flops are keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated TTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. On the first falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low, it is held low). When RESET is released (high), the outputs will resume counting, after five falling edge clock input delays, from their low state (see "Relative Output Timing", Page 3-20 and "Reset To Output Timing", in Clock Driver Application Note #1).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current.

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The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3502 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa	$\overline{Fa}$	Fb	$\overline{Fc}$
LO	LO	F	F/2	F/2	F/4	F/8
HI	LO	F	F/2	F/2	F/2	F/8
LO	HI	F	F/2	F/2	F/4	F/4
HI	HI	F	F/2	F/2	F/2	F/4

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non–crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3502 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3502 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-21 for complete load definition).

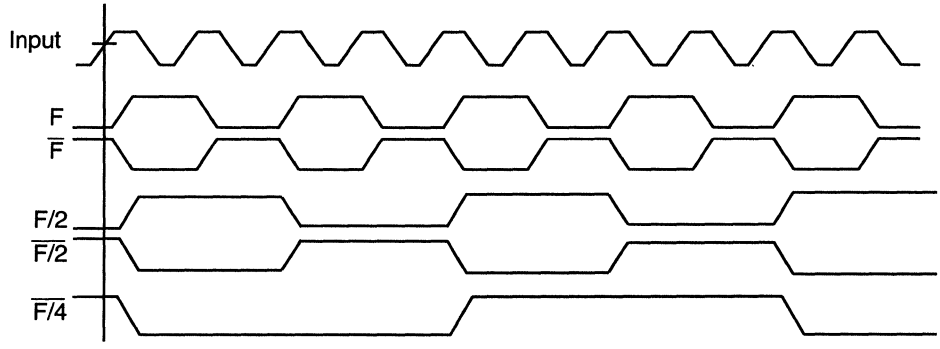
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3502 to determine the total power being dissipated by the SC3502. This total power is then multiplied by the SC3502's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3502. For greatest reliability, this junction temperature should not exceed 140°C.

	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: You have a SC3502 with 4 of the Fa and 4 of the $\overline{Fa}$ outputs running at 66 MHz with 10 pF loads (8 x 47 = 376 mW + 2 x 16 = 32 mW for an Fa and $\overline{Fa}$ Total of 408 mW), 3 of the Fb outputs are running at 33 MHz with 5 pF loads (3 x 19 = 57 mW + 2 x 12 = 24 mW for an Fb Total of 81 mW), and 2 $\overline{Fc}$ outputs running at 33 MHz with 15 pF loads (2 x 24 = 48 mW + 3 x 12 = 36 mW for an $\overline{Fc}$ Total of 84 mW). The Total Chip Power is Core Power (400 mW) + Fa and $\overline{Fa}$ Power (408 mW) + Fb Power (81 mW) + $\overline{Fc}$ Power (84 mW) = 973 mW. Your design calls for a 70°C Still Air ambient. The SC3502's junction temperature would then be: 70°C + (.973 Watts x 50°C/Watt = 49°C) = 119°C, below the 140°C maximum.

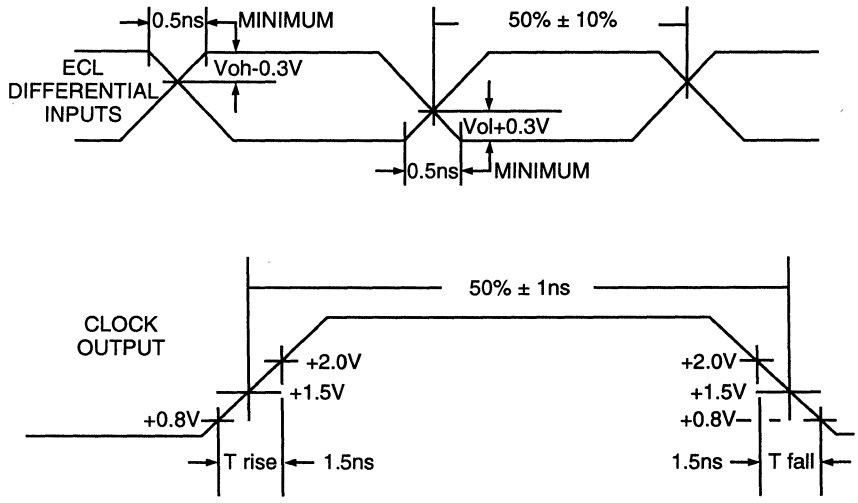
Relative Output Timing



Symmetry

The outputs of the SC3502 are nominally centered to provide a clean 50% duty cycle, symmetrical waveform at the +1.5V threshold reference. (See Threshold Crossing Characteristics diagram below, for the conditions.)

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

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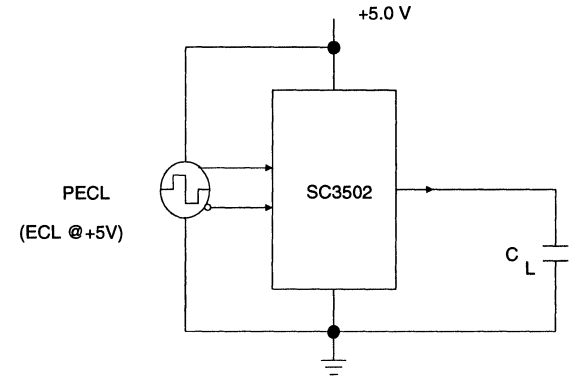
AC Test Circuit



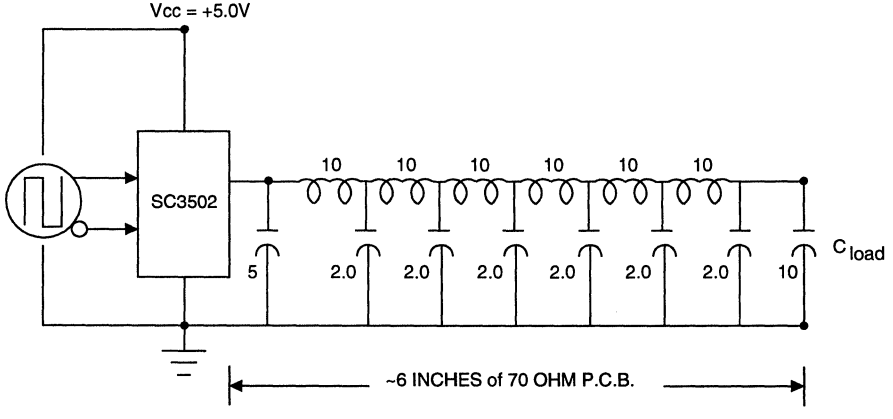
Designing the SC3502 for "Real Loads"

While the AC Test Circuit presented above be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3502 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3502 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz.

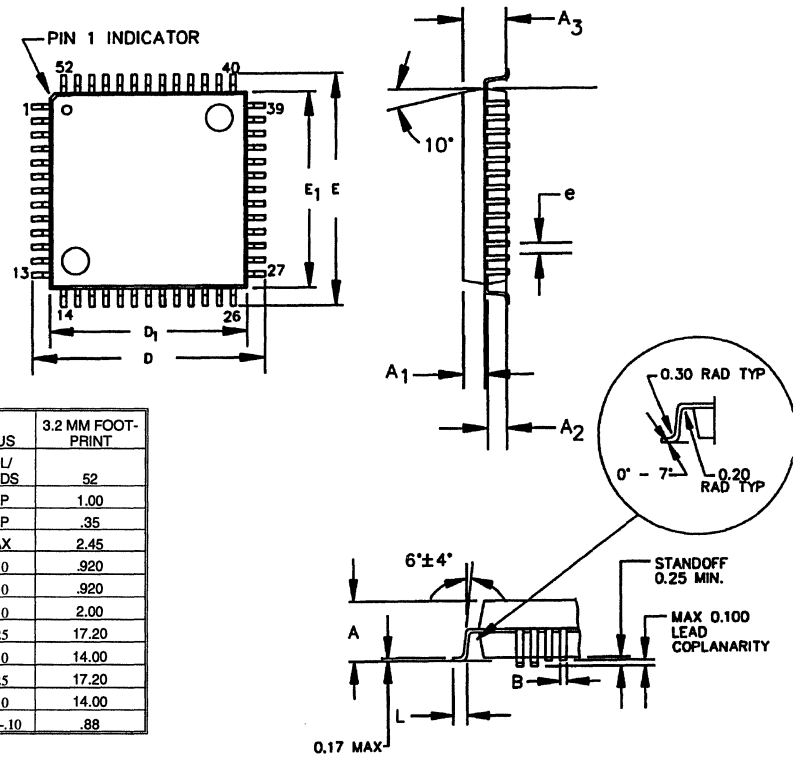
Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

52–Pin PQFP Package



BODY SIZE PLUS		3.2 MM FOOT-PRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	+.15/-.10	.88

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	14	"C" SEL	27	NC	40	TTL OSC
2	GND	15	GND	28	NC	41	GND
3	FB4	16	FA0	29	$\overline{\text{FC0}}$	42	$\overline{\text{FA9}}$
4	GND	17	VCC	30	GND	43	VCC
5	FB3	18	FA1	31	$\overline{\text{FC1}}$	44	$\overline{\text{FA8}}$
6	VCC	19	GND	32	VCC	45	GND
7	FB2	20	FA2	33	$\overline{\text{FC2}}$	46	$\overline{\text{FA7}}$
8	GND	21	VCC	34	GND	47	VCC
9	FB1	22	FA3	35	$\overline{\text{FC3}}$	48	$\overline{\text{FA6}}$
10	VCC	23	GND	36	VCC	49	GND
11	FB0	24	FA4	37	$\overline{\text{FC4}}$	50	$\overline{\text{FA5}}$
12	VCC	25	VCC	38	PECL OSCN	51	VCC
13	"B" SEL	26	NC	39	PECL OSCP	52	CLK SEL

Ordering Codes

Package Type	Max Skew Across All Outputs	Part Number
52 Lead Plastic Quad Flat Pack	1.0 ns	SC3502Q-1
52 Lead Plastic Quad Flat Pack	1.5 ns	SC3502Q

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20-OUTPUT CLOCK DRIVER SC3506

GENERAL DESCRIPTION

The SC3506 is a precision low skew clock driver with 20 outputs. It employs a clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The twenty outputs are divided into two groups: group Fb is at the primary frequency, equal to the input; group Fa is at one half of the primary input frequency.

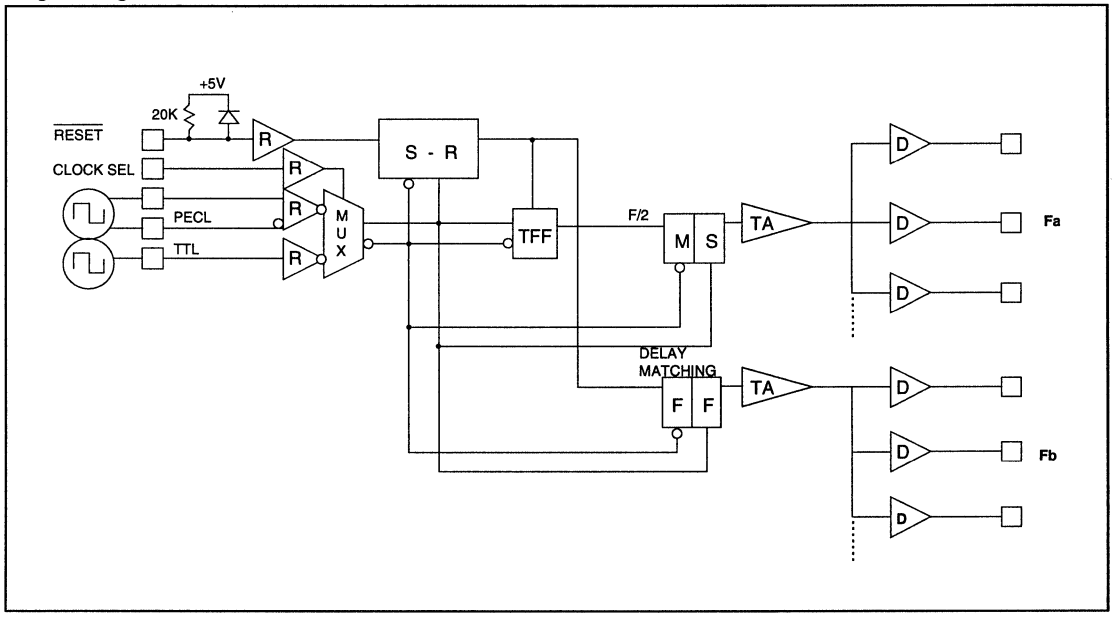
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs:**
  - Ten (10) outputs at primary frequency, up to 80 MHz
  - Ten (10) outputs at 1/2 primary frequency
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **Compatible with Intel's Pentium™ processor**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

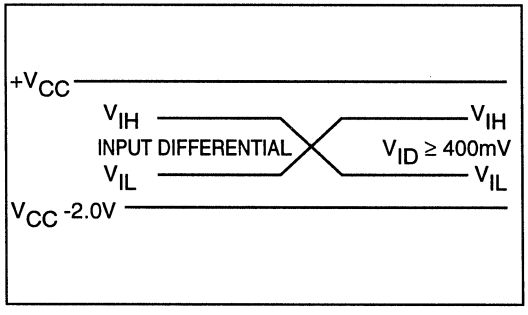
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-28)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-27 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3506 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3506 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3506 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using AC Test Circuit (Page 3-28)

V_{CC} = +5.0V ±5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3506-2	SC3506-1	SC3506	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	2.0	—	ns
Maximum Skew Across Fa Outputs	0.25	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum Differential PECL Input Frequency	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip twenty output fan-out device using AMCC's advanced BiCMOS process. This design has optimized the device for clock symmetry and absolute minimum skew across all twenty outputs. Two harmonic clock frequency groups are provided.

For highest performance this approach requires a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V - PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization, refer to the logic diagram preceding. Using this methodology, the output duty cycle for the F/2 or Fa group becomes largely a function of output driver slew rate into the AC load.

The Fb group duty cycle is governed by the input source clock. The output flip-flops are reset keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated TTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high), the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin (see "Relative Output Timing", Page 3-28, and "Reset To Output Timing",in the Application Note #1).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Application Note #1).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3506 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Power Management

The overall goal of managing the power dissipated by the SC3506 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3506 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-29 for complete load definition).

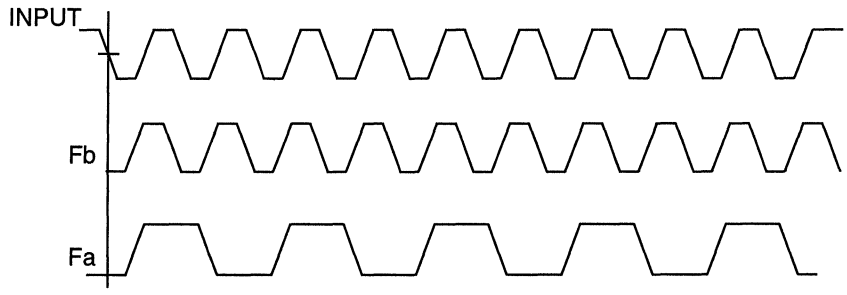
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3506 to determine the total power being dissipated by the SC3506. This total power is then multiplied by the SC3506's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3506. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3506 is as follows:

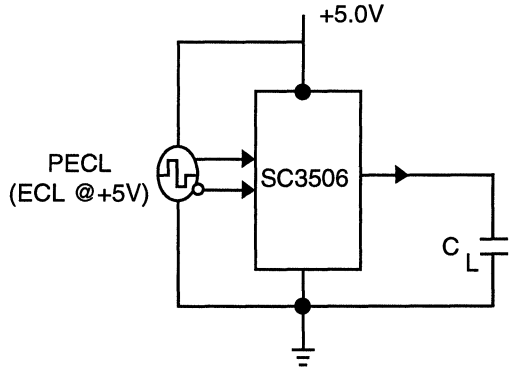
	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: An SC3506 with 8 of the Fb outputs running at 66 MHz with 10 pF loads (8 x 47 = 376 mW + 2 x 16 = 32 mW for an Fb Total of 408 mW), 3 of the Fa outputs are running at 33 MHz with 5 pF loads (3 x 19 = 57 mW), and 2 Fa outputs running at 33 MHz with 15 pF loads (2 x 24 = 48 mW + 5 x 12 = 60 mW for an Fa Total of 165 mW). The Total Chip Power is Core Power (400 mW) + Fb Power (408 mW) + Fa Power (165 mW) = 973 mW. Your design calls for a 70°C Still Air ambient. The SC3506's junction temperature would then be: 70°C + (.973 Watts x 50°C/Watt = 49°C) = 119°C, below the 140°C maximum.

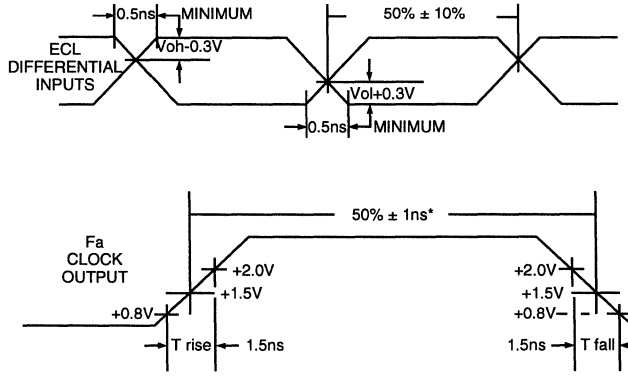
Relative Output Timing



AC Test Circuit



Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

*Applies only to divide-by-two outputs.

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Designing the SC3506 for "Real Loads"

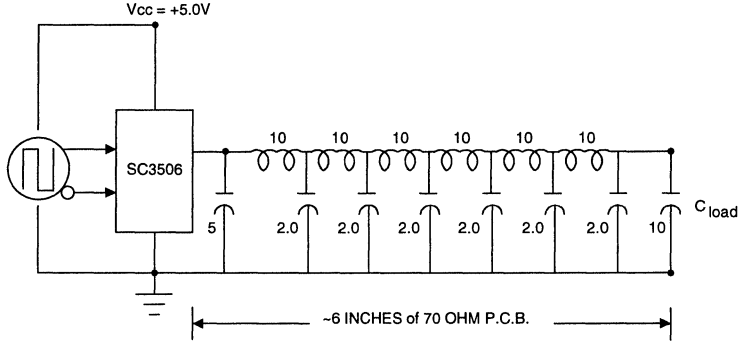
While the AC Test Circuit presented on Page 3-28 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3506 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3506 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note #1.

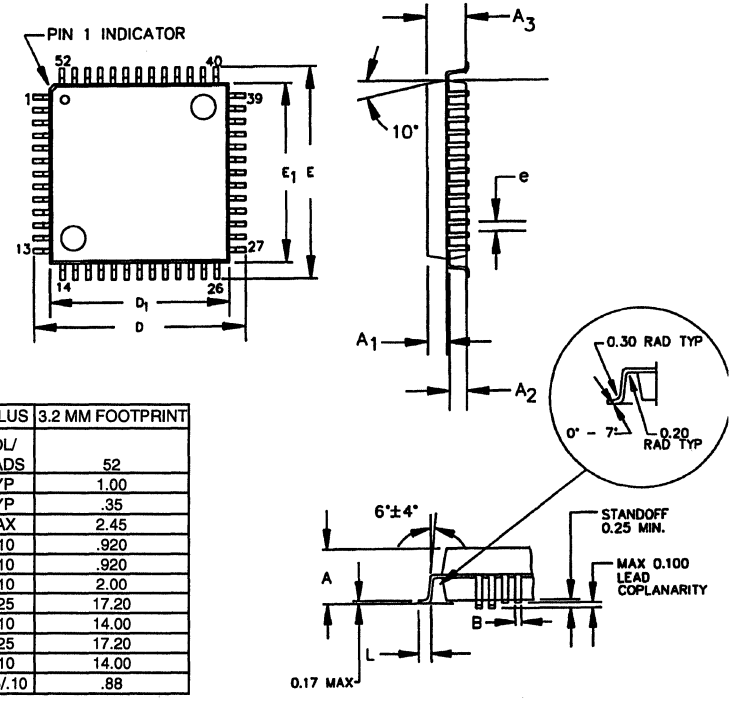
3

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

52–Pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT	
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	14	VCC	27	NC	40	TTL OSC
2	GND	15	GND	28	NC	41	GND
3	FB4	16	FA0	29	FB5	42	FA9
4	GND	17	VCC	30	GND	43	VCC
5	FB3	18	FA1	31	FB6	44	FA8
6	VCC	19	GND	32	VCC	45	GND
7	FB2	20	FA2	33	FB7	46	FA7
8	GND	21	VCC	34	GND	47	VCC
9	FB1	22	FA3	35	FB8	48	FA6
10	VCC	23	GND	36	VCC	49	GND
11	FB0	24	FA4	37	FB9	50	FA5
12	VCC	25	VCC	38	PECL OSCN	51	VCC
13	VCC	26	NC	39	PECL OSCP	52	CLK SEL

Ordering Codes

Package Type	Max Skew Across All Outputs	Max Skew Chip-to-Chip	Part Number
52 Lead Plastic Quad Flat Pack	0.5 ns	1.0 ns	SC3506Q-2
52 Lead Plastic Quad Flat Pack	0.5 ns	2.0 ns	SC3506Q-1
52 Lead Plastic Quad Flat Pack	1.0 ns	—	SC3506Q

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20-OUTPUT CLOCK DRIVER SC3507

GENERAL DESCRIPTION

The SC3507 is a precision low skew driver with 20 outputs. It requires a 2X frequency clock input from either a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The 20-clock outputs are divided into three groups. The first group of ten (10) outputs are unconditionally at the primary frequency, "Fa"= F input/2. The second group, "Fb", of five outputs can be selected to be either identical to "Fa" or at 1/2 the frequency of "Fa". Similarly, the third group, "Fc", of five outputs, can be selected to be at either equal to or 1/2 of "Fa".

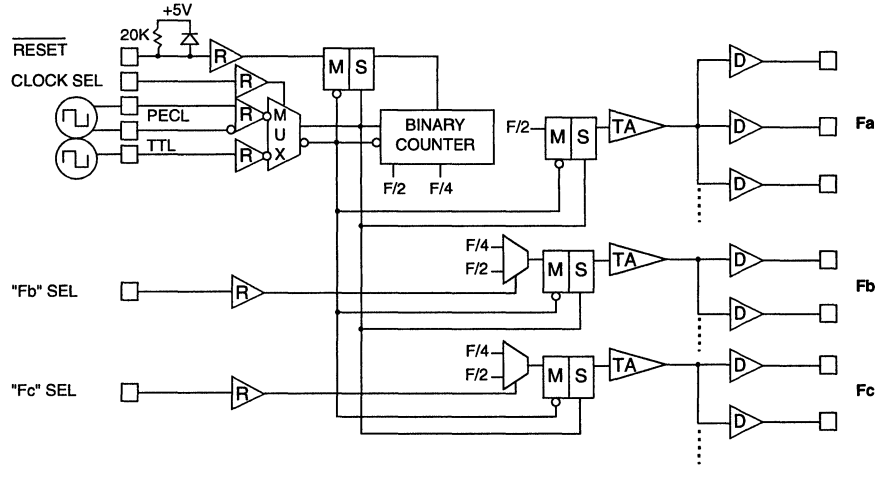
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs:**
  - Ten (10) outputs at primary frequency, up to 80 MHz
  - Ten (10) outputs at primary or 1/2 primary frequency, in two groups of five outputs
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

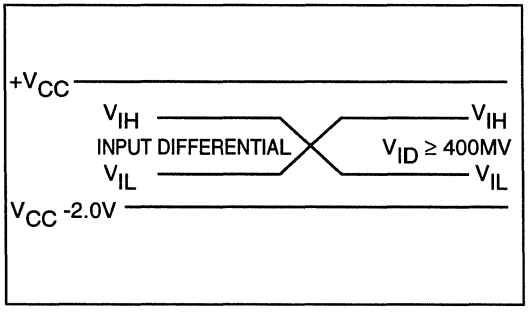
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-36)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL, CSEL, BSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL, CSEL, BSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-35 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3507 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3507 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3507 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using Evaluation Circuit (Page 3-37)

Vcc = +5.0V ±5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3507-1	SC3507	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Chip to Chip	2.0	—	ns
Maximum Skew Across Fa Outputs	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	MHz
Maximum Rising/Falling Edge Rates	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output Duty Cycle asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip clock driver with twenty outputs using AMCC's advanced BiCMOS process. This design was optimized for minimum skew across all twenty outputs.

For best performance this approach requires a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator operating between +5V and ground can provide either differential ECL inputs (referenced to +5V - PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization, (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. On the first falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low, it is held low). When RESET is released (high), the outputs will resume counting, after five falling edge clock input delays, from their low state (see "Relative Output Timing", Page 3-36, and "Reset To Output Timing" in the Application Note #1).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Application Note #1).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3507 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa	Fb	Fc
LO	LO	F	F/2	F/4	F/4
HI	LO	F	F/2	F/2	F/4
LO	HI	F	F/2	F/4	F/2
HI	HI	F	F/2	F/2	F/2

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non–crystal oscillator sources may be used at the user's discretion. See Application Note #1.

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Power Management

The overall goal of managing the power dissipated by the SC3507 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3507 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-37 for complete load definition).

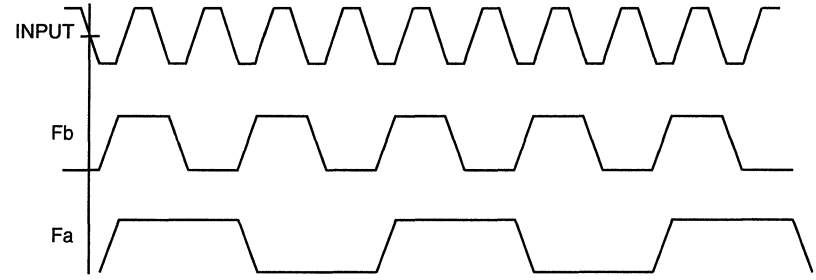
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3507 to determine the total power being dissipated by the SC3507. This total power is then multiplied by the SC3507's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3507. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3507 is as follows:

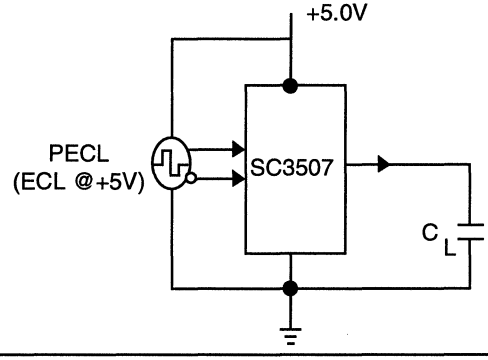
	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: An SC3507 with 8 of the Fa outputs running at 66 MHz with 10 pF loads (8 x 47 = 376 mW + 2 x 16 = 32 mW for an Fa Total of 408 mW), 3 of the Fb outputs are running at 33 MHz with 5 pF loads (3 x 19 = 57 mW + 2 x 12 = 24 mW for an Fb Total of 81 mW), and 2 Fc outputs running at 33 MHz with 15 pF loads (2 x 24 = 48 mW + 3 x 12 = 36 mW for an Fc Total of 84 mW). The Total Chip Power is Core Power (400 mW) + Fa Power (408 mW) + Fb Power (81 mW) + Fc Power (84 mW) = 973 mW. Your design calls for a 70°C Still Air ambient. The SC3507's junction temperature would then be: 70°C + (.973 Watts x 50°C/Watt = 49°C) = 119°C, below the 140°C maximum.

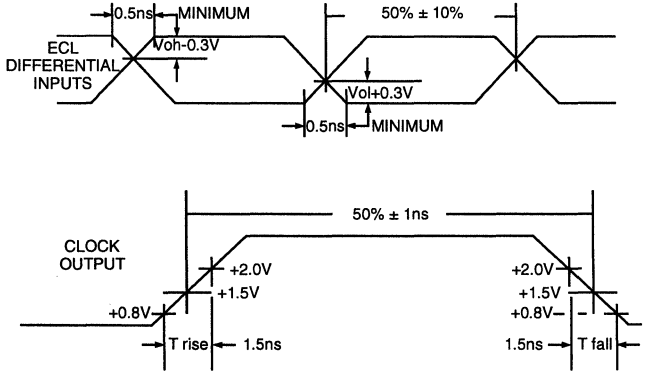
Relative Output Timing



AC Test Circuit



Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

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Designing the SC3507 for "Real Loads"

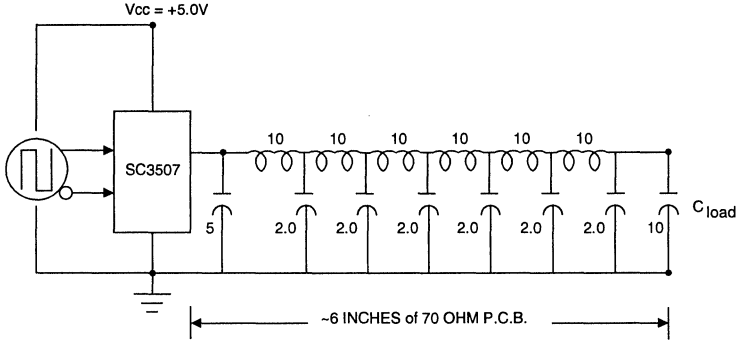
While the AC Test Circuit presented on Page 3-36 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3507 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3507 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use.

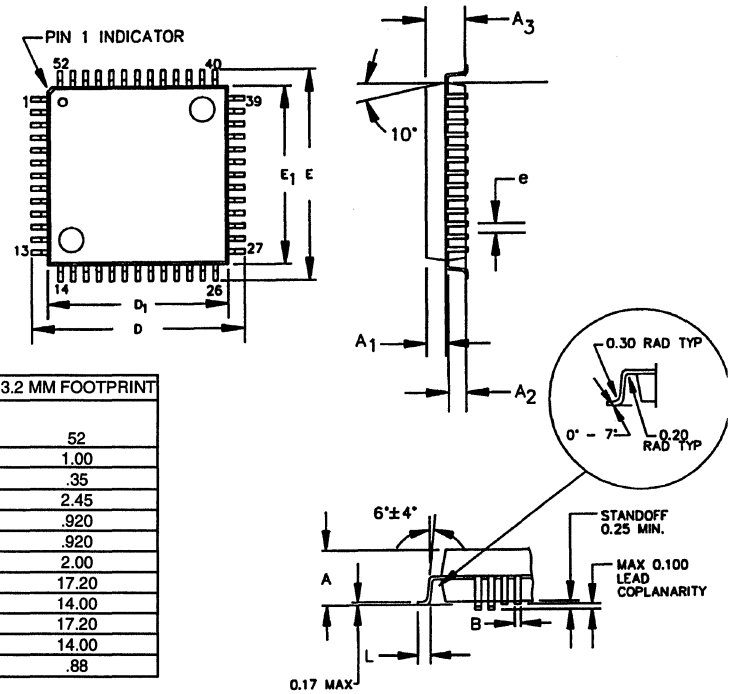
3

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

52–Pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	14	"C" SEL	27	NC	40	TTL OSC
2	GND	15	GND	28	NC	41	GND
3	FB4	16	FA0	29	FC0	42	FA9
4	GND	17	VCC	30	GND	43	VCC
5	FB3	18	FA1	31	FC1	44	FA8
6	VCC	19	GND	32	VCC	45	GND
7	FB2	20	FA2	33	FC2	46	FA7
8	GND	21	VCC	34	GND	47	VCC
9	FB1	22	FA3	35	FC3	48	FA6
10	VCC	23	GND	36	VCC	49	GND
11	FB0	24	FA4	37	FC4	50	FA5
12	VCC	25	VCC	38	PECL OSCN	51	VCC
13	"B" SEL	26	NC	39	PECL OSCP	52	CLK SEL

Ordering Codes

Package Type	Max Skew Across All Outputs	Part Number
52 Lead Plastic Quad Flat Pack	0.5 ns	SC3507Q-1
52 Lead Plastic Quad Flat Pack	1.0 ns	SC3507Q

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20-OUTPUT CLOCK DRIVER SC3508

GENERAL DESCRIPTION

The SC3508 is a minimum skew clock driver with 20 outputs. It can employ a clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

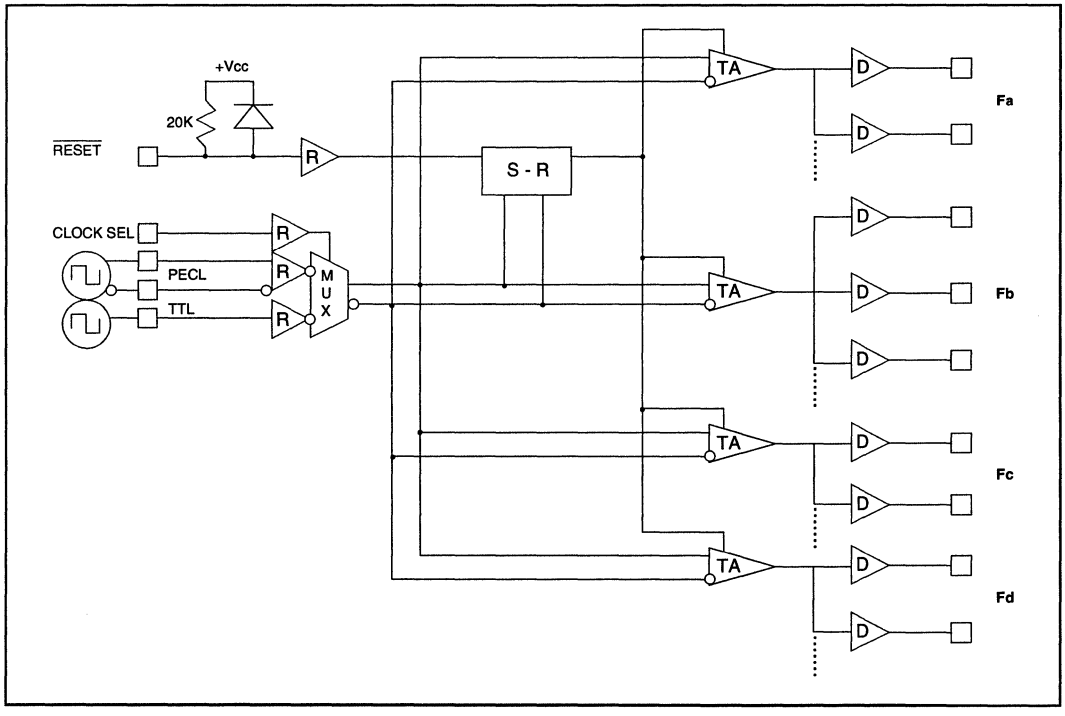
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs at primary frequency up to 80 MHz**
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **Compatible with Intel's Pentium™ processor**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

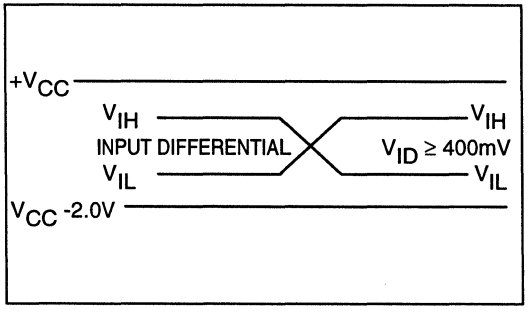
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-43)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including Clock	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including Clock	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-43 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3508 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3508 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3508 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC SPECIFICATIONS–USING AC TEST CIRCUIT (Page 3-43)

V_{CC} = +5.0V ± 5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

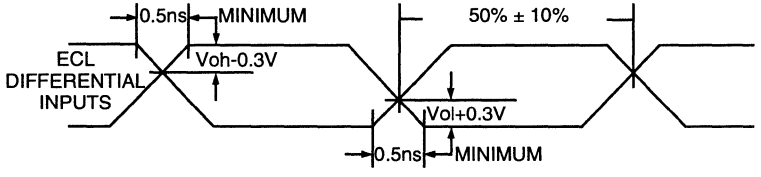
Parameter	SC3508-2	SC3508-1	SC3508	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	2.0	—	ns
Maximum Skew Across Fa, Fb, Fc, or Fd Outputs	0.25	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

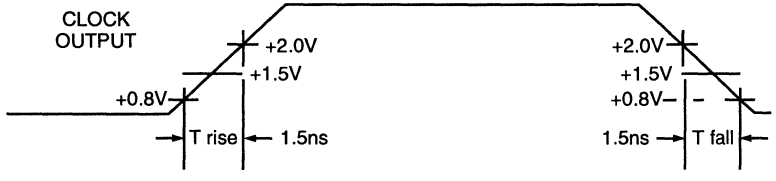
Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. The SC3508 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

3

Threshold Crossing Characteristics





NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip clock buffer and twenty output fan-out driver using AMCC's advanced BiCMOS process. This design is optimized the device for absolute minimum skew across all twenty outputs.

For best performance, this approach will require a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V—PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to translation amplifiers and output drivers, (refer to the preceding logic diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Clock Driver Application Note #1).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see clock Driver Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3508 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Power Management

The overall goal of managing the power dissipated by the SC3508 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3508 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-44 for complete load definition).

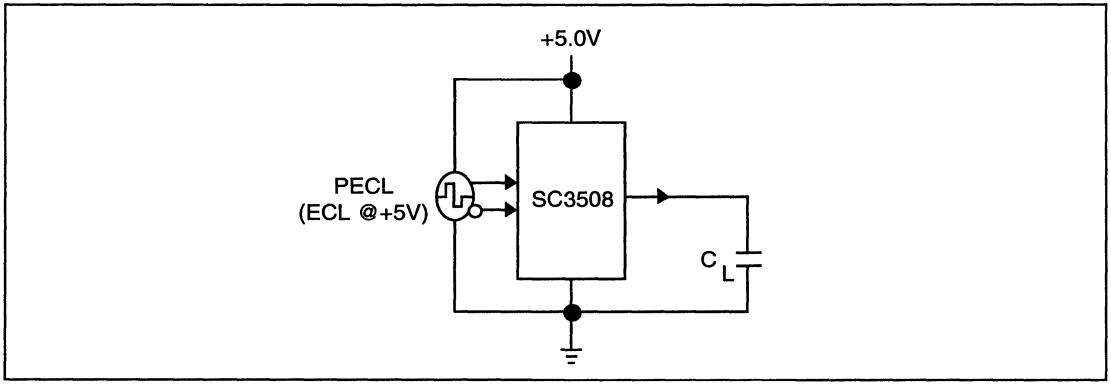
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3508 to determine the total power being dissipated by the SC3508. This total power is then multiplied by the SC3508's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3508. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3508 is as follows:

	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: An SC3508 with 12 of the outputs running at 50 MHz with 15 pF loads (12 x 39 = 468 mW + 8 x 14 = 112 mW for a Total of 580 mW). The Total Chip Power is Core Power (400 mW) + F_0 Power (580 mW) = 980 mW. Your design calls for a 70°C Still Air ambient. The SC3508's junction temperature would then be: 70°C + (.98 Watts x 50°C/Watt = 49°C) = 119°C, which is below the 140°C maximum junction temperature.

AC Test Circuit



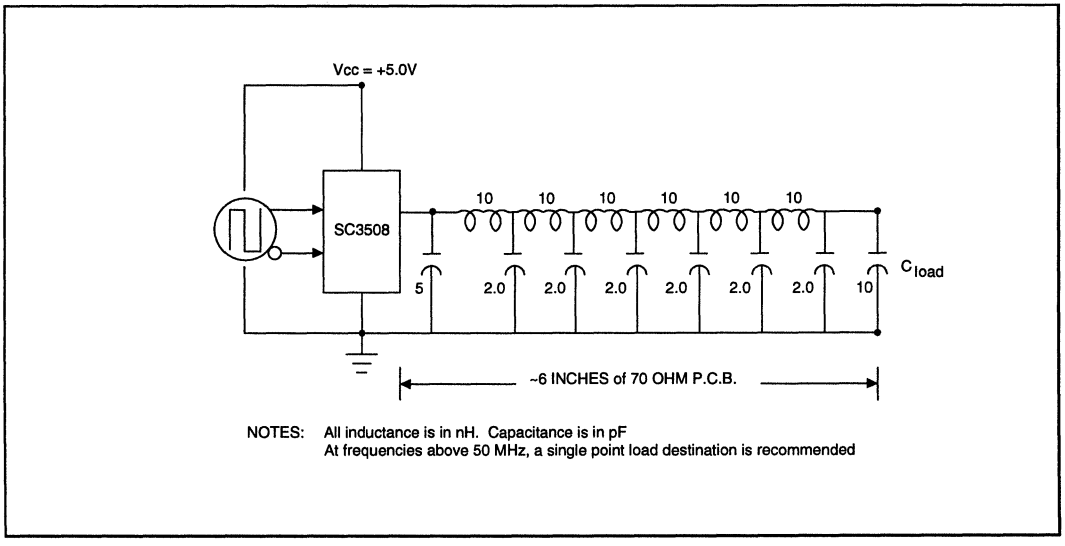
Designing the SC3508 for "Real Loads"

While the AC Test Circuit presented on Page 3-43 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3508 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3508 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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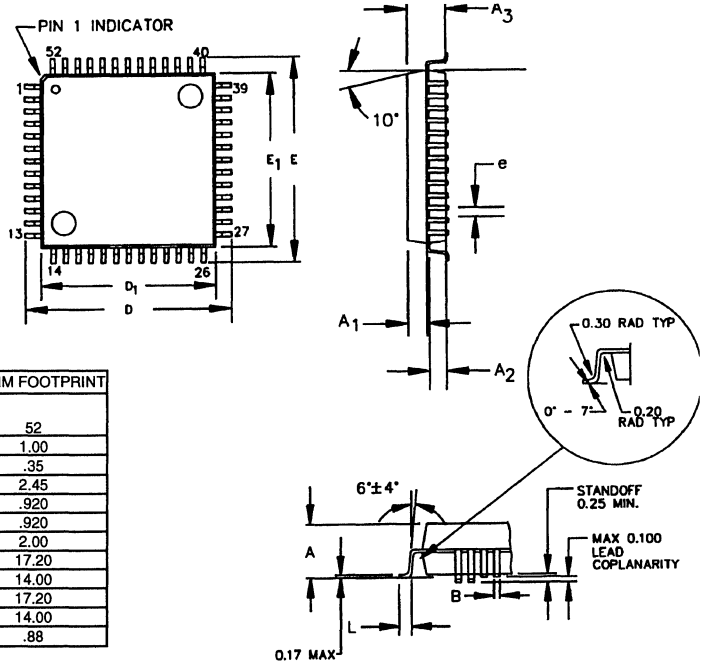
52–Pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	14	VCC	27	NC	40	TTL OSC
2	GND	15	GND	28	NC	41	GND
3	FA0	16	FB0	29	FC0	42	FD0
4	GND	17	VCC	30	GND	43	VCC
5	FA1	18	FB1	31	FC1	44	FD1
6	VCC	19	GND	32	VCC	45	GND
7	FA2	20	FB2	33	FC2	46	FD2
8	GND	21	VCC	34	GND	47	VCC
9	FA3	22	FB3	35	FC3	48	FD3
10	VCC	23	GND	36	VCC	49	GND
11	FA4	24	FB4	37	FC4	50	FD4
12	VCC	25	VCC	38	PECL OSCN	51	VCC
13	VCC	26	NC	39	PECL OSCP	52	CLK SEL

Ordering Codes

Package Type	Max Skew Across All Outputs	Max Skew Chip to Chip	Part Number
52 Lead Plastic Quad Flat Pack	0.5 ns	1.0 ns	SC3508Q-2
52 Lead Plastic Quad Flat Pack	0.5 ns	2.0 ns	SC3508Q-1
52 Lead Plastic Quad Flat Pack	1.0 ns	—	SC3508Q

NOTES

10-OUTPUT CLOCK DRIVER SC3517

GENERAL DESCRIPTION

The SC3517 is a precision low skew clock driver with ten outputs. It requires a 2X frequency clock input from a single ended TTL or an ECL differential source operating between +5V and ground. This 2X reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers.

The ten (10)-clock outputs are divided into two groups. The first group of five (5) outputs are unconditionally at the primary frequency, "Fb"= F input/2. The second group, "Fc", of five outputs can be selected to be either identical to "Fb" or at 1/2 the frequency of "Fb". There are no "Fa" outputs on the SC3517.

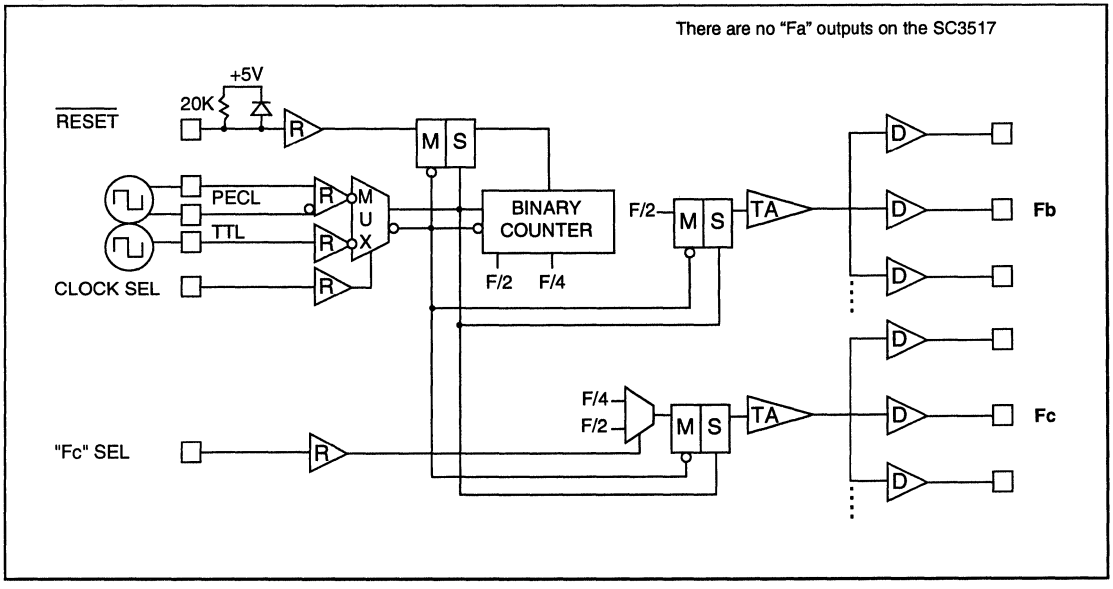
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Ten (10) clock outputs:**
  - Five (5) outputs at primary frequency, up to 80 MHz
  - Five (5) outputs at primary or 1/2 primary frequency
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

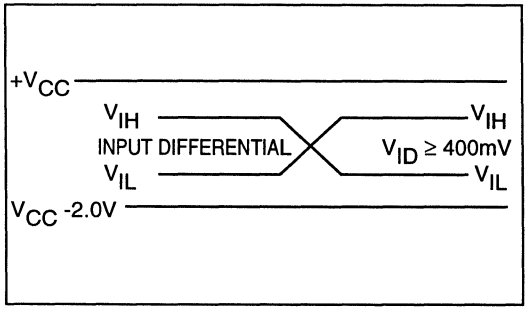
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-53)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL, CSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL, CSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-51 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3517 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3517 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3517 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using AC Test Circuit (Page 3-53)

Vcc = +5.0V ±5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3517-1	SC3517	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Chip to Chip	2.0	—	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Skew Across Fc Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	160	160	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip clock driver with ten outputs using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all ten outputs.

For best performance this approach will require a 2X clock source input. This input frequency source, operating between +5V and ground, can provide either differential ECL inputs (referenced to +5V , PECL) or single ended TTL (CMOS) input level to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") select TTL and logic HIGH selects PECL. This 2X input clock will be fanned out to a divide counter and to flip-flops for synchronization, then to the translation amplifiers and output drivers (refer to the preceding logic diagram) . The output duty cycle asymmetry is largely a function of the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. On the first falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low, it is held low). When RESET is released (high) the outputs will resume counting, after five falling edge clock input delays, from their low state (see "Relative Output Timing", Page 3-52 and "Reset To Output Timing", in the Application Note).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two I.C. input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Application Note #1).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3517 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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Output Clock Frequency Selection

"C" SEL	XCO FREQ	Fb	Fc
LO	F	F/2	F/4
HI	F	F/2	F/2

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non–crystal oscillator sources may be used at the user's discretion. See Application Note #1.

Power Management

The overall goal of managing the power dissipated by the SC3517 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3517 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-53 for complete load definition).

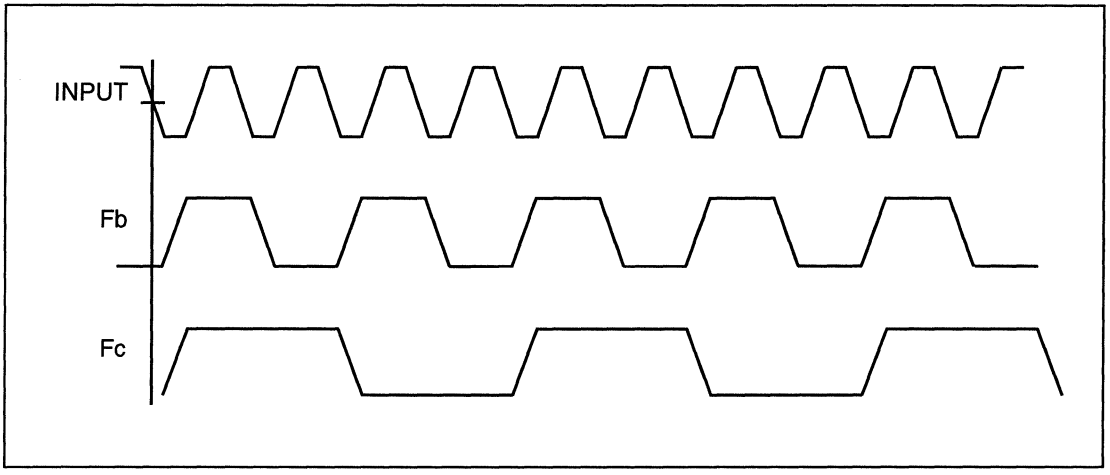
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3517 to determine the total power being dissipated by the SC3517. This total power is then multiplied by the SC3517's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3517. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3517 is as follows:

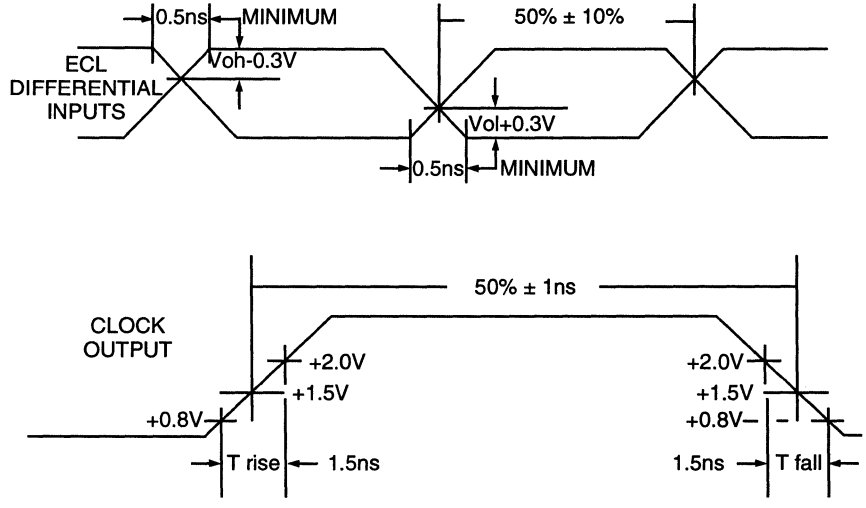
	STILL AIR
THERMAL RESISTANCE	50°C/WATT

The outputs of the SC3517 are nominally centered to provide a clean 50% duty cycle, symmetrical waveform at the +1.5V threshold reference (see Threshold Crossing Characteristics diagram below for the conditions).

Relative Output Timing



Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

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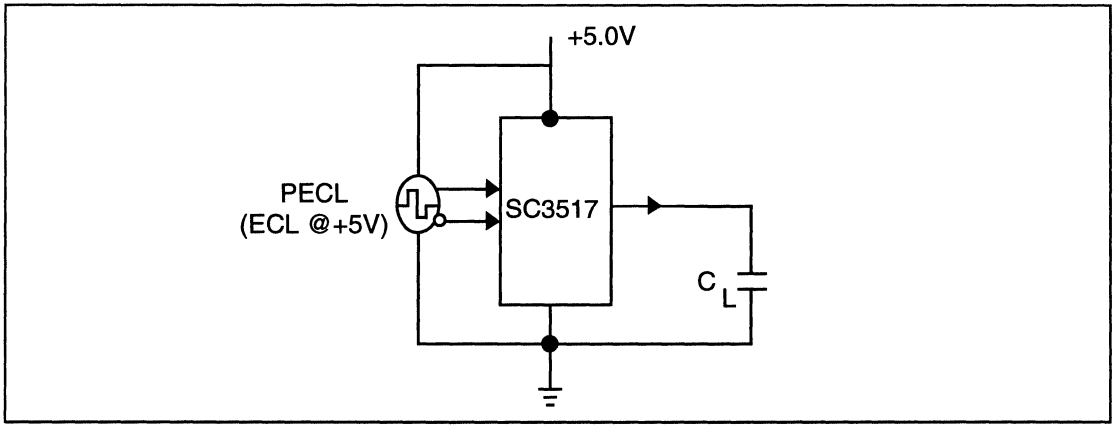
AC Test Circuit



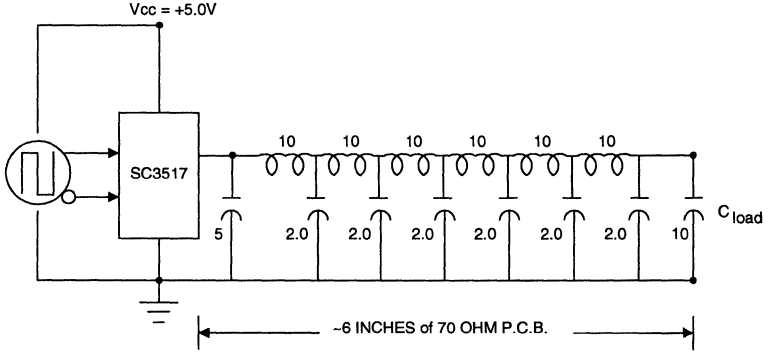
Designing the SC3517 for "Real Loads"

While the AC Test Circuit presented above can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3517 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3517 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

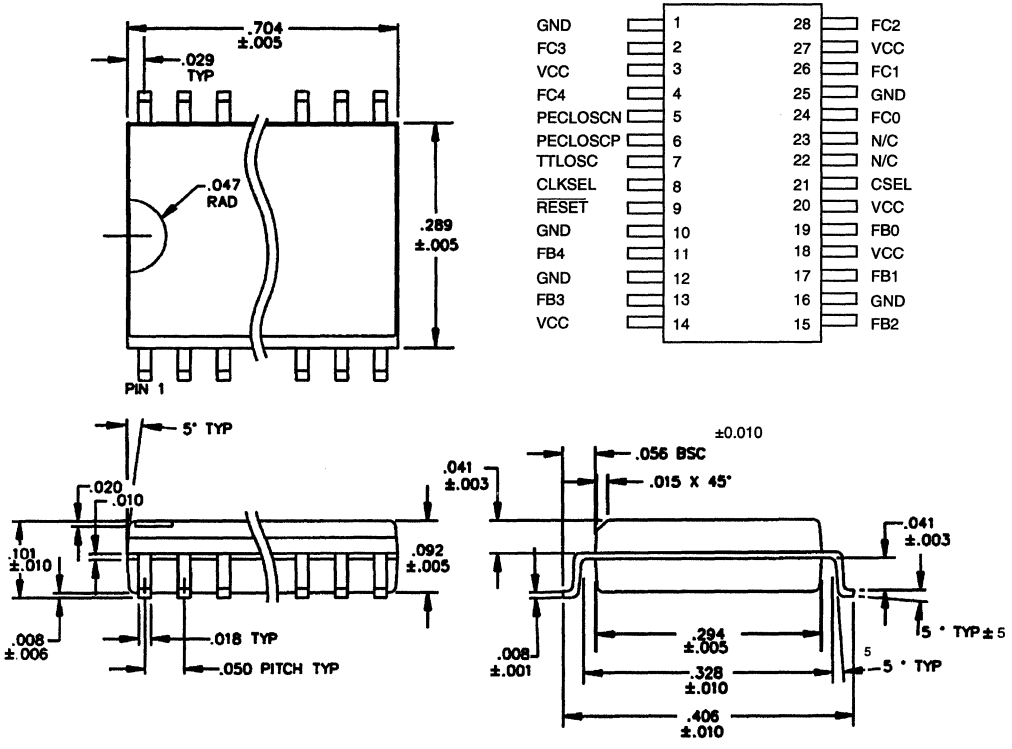
Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

28–Lead Small Outline Integrated Circuit Plastic Package (SOIC)



Dimensions nominal in inches.

Ordering Codes

Package Type	Max Skew Across All Outputs	Part Number
28 Lead Small Integrated Circuit Plastic Package	0.5 ns	SC3517S-1
28 Lead Small Integrated Circuit Plastic Package	1.0 ns	SC3517S

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10-OUTPUT CLOCK DRIVER SC3518

GENERAL DESCRIPTION

The SC3518 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to the clock output drivers.

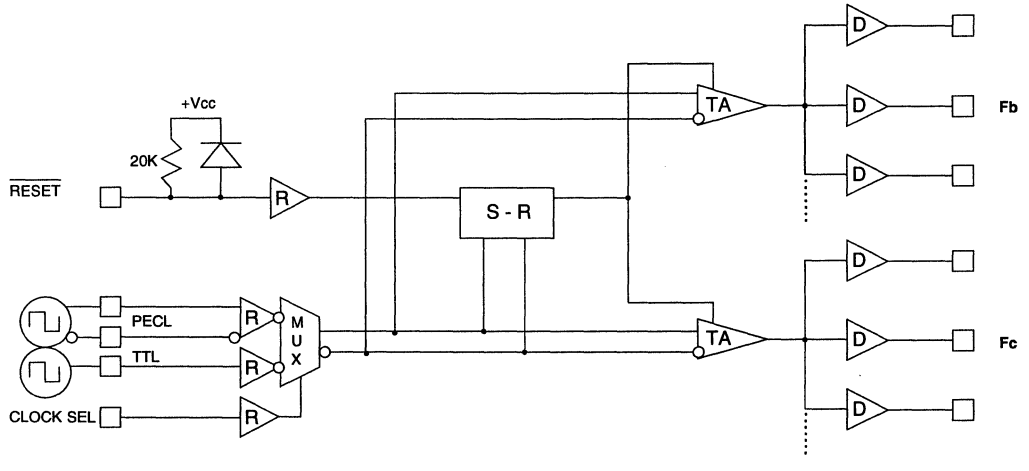
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Ten (10) clock outputs at primary frequency up to 80 MHz**
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **Compatible with Intel's Pentium™ processor**

3

Logic Diagram



There are no "Fa" outputs on the SC3518

Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

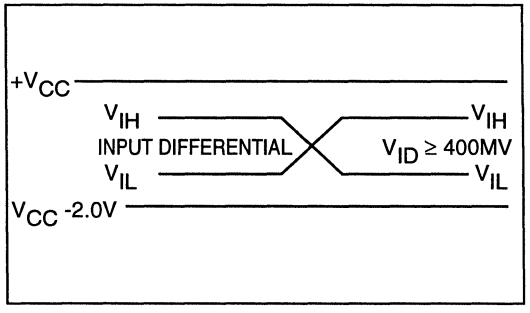
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-60)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 3-59 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3518 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3518 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3518 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using AC Test Circuit (Page 3-60)

V_{CC} = +5.0V ±5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3518-2	SC3518-1	SC3518	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	2.0	—	ns
Maximum Skew Across Fb or Fc Outputs	0.25	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum Differential PECL Input Frequency	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

*Notes:

1. Skew is referenced to the rising edges of all outputs
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C Chip to chip skew tested at 70°C.
3. The SC3518 output symmetry follows input symmetry. Output duty cycle will also be affected by voltage and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip ten output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all ten outputs.

The clock source input for this device may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V , PECL) or single ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Clock Driver Application Note #1).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3518 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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Power Management

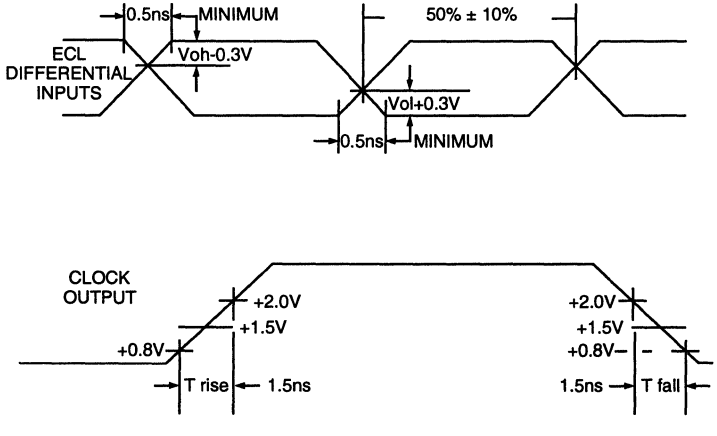
The overall goal of managing the power dissipated by the SC3518 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3518 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-60 for complete load definition).

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (400 mW) of the SC3518 to determine the total power being dissipated by the SC3518. This total power is then multiplied by the SC3518's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3518. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3518 is as follows:

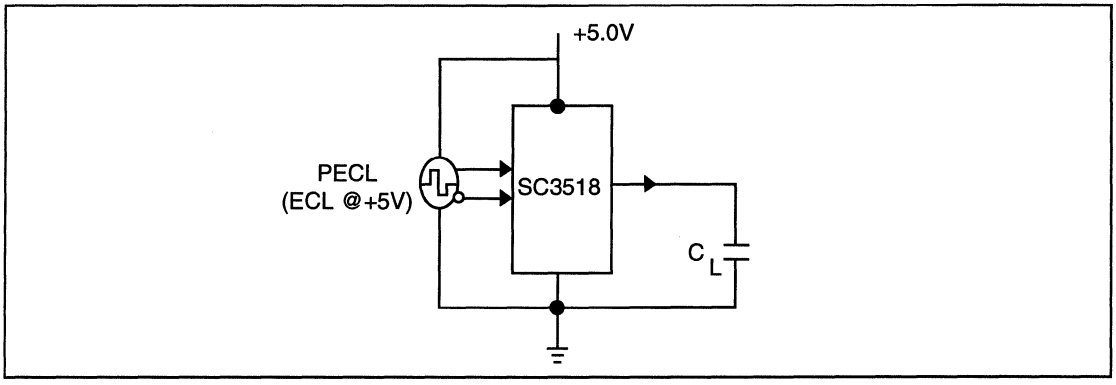
	STILL AIR
THERMAL RESISTANCE	50°C/WATT

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

AC Test Circuit



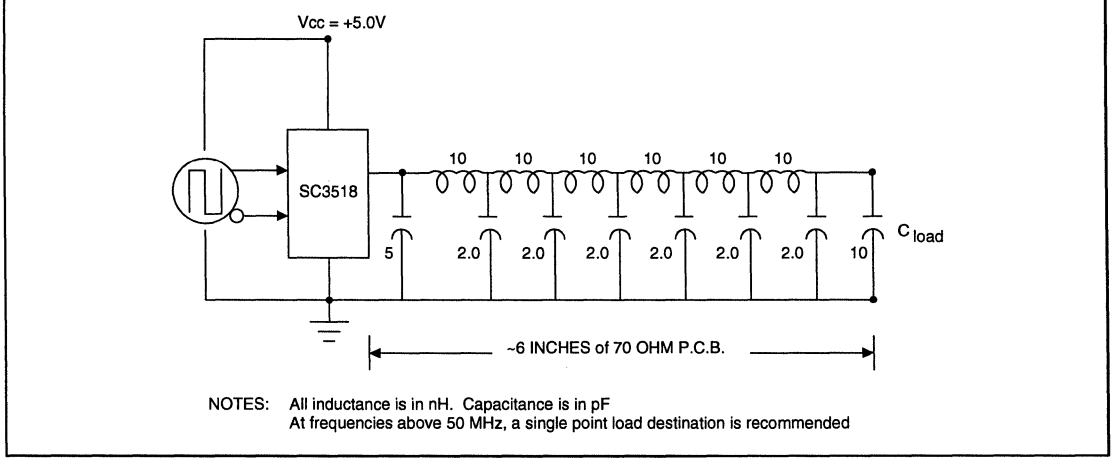
Designing the SC3518 for "Real Loads"

While the AC Test Circuit presented above can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3518 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3518 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use. AMCC will Spice model any reasonable load presented at customer request, driven by our output drivers. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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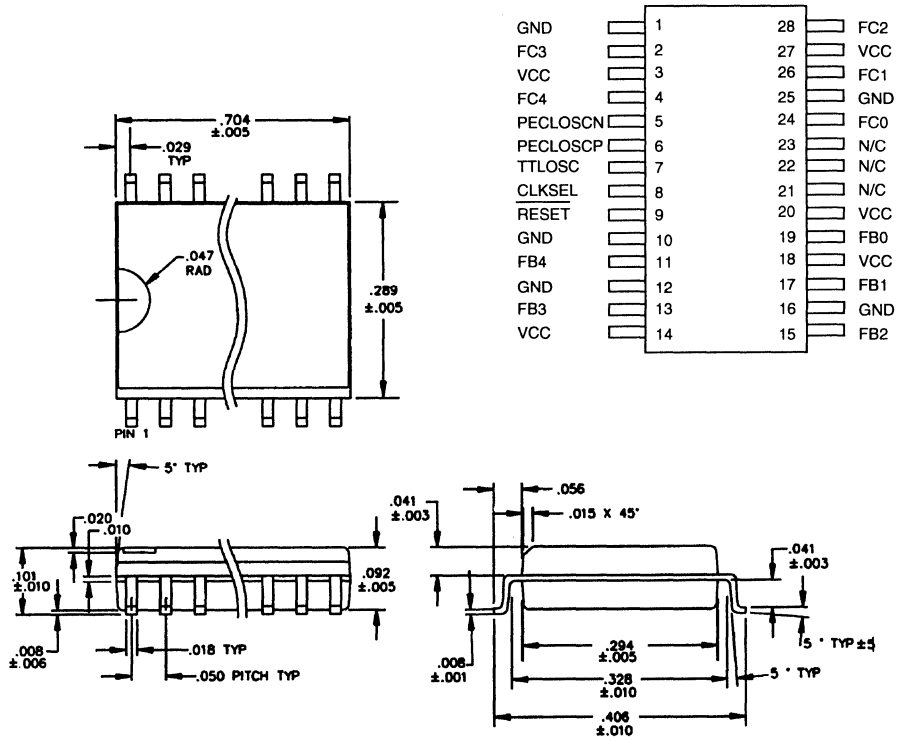
28-Lead Small Outline Integrated Circuit Package (SOIC)



All dimensions in inches.

Ordering Codes

Package Type	Max Skew Across All Outputs	Max Skew Chip-to-Chip	Part Number
28 Lead Small Integrated Circuit Plastic Package	0.5 ns	1.0 ns	SC3518S-2
28 Lead Small Integrated Circuit Plastic Package	0.5 ns	2.0 ns	SC3518S-1
28-Lead Small Integrated Circuit Plastic Package	1.0 ns	—	SC3518S

NOTES

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9–OUTPUT CLOCK DRIVER SC3526

GENERAL DESCRIPTION

The SC3526 is a low skew clock driver with nine outputs. Five outputs operate at the primary reference frequency and four outputs operate at half the primary reference frequency. A synchronous reset ensures proper phase of the half frequency outputs. It can employ a clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise, distortion, and EMI.

APPLICATIONS

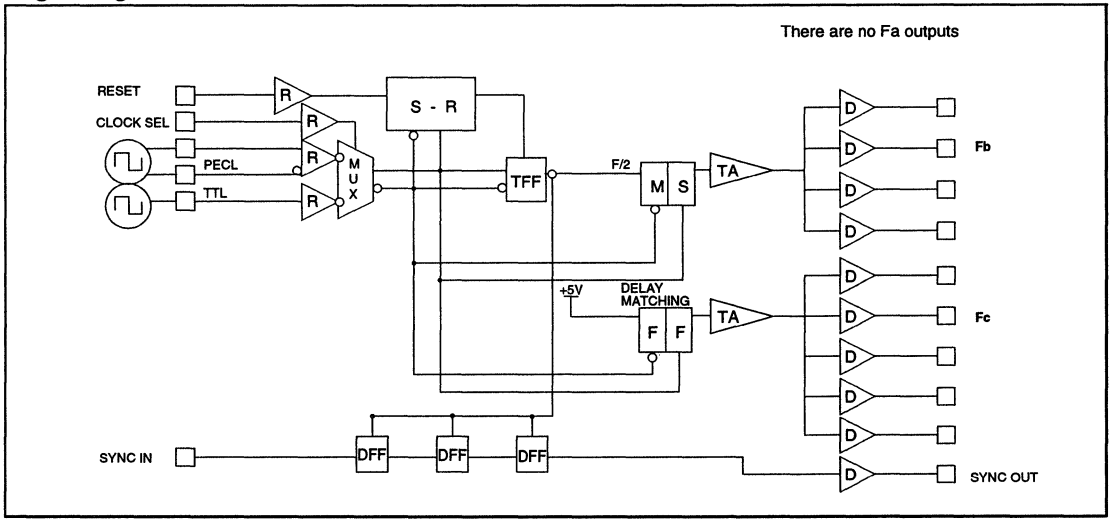
- **High speed clock distribution where signal fidelity and low noise are key requirements**
- **High-performance 80486 and Pentium™-based systems**

FEATURES

- **Five (5) clock outputs at reference frequency up to 66 Mhz**
- **Four (4) clock outputs at half reference frequency up to 33 Mhz**
- **Leading edge skew for all outputs <700 ps**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω equivalent source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

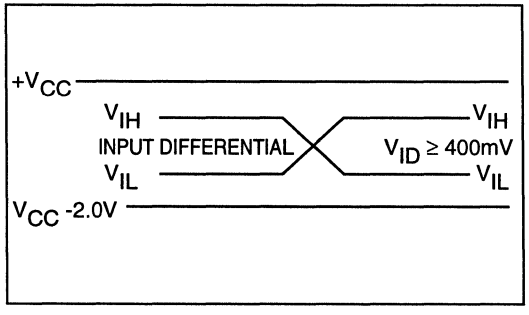
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-67)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including clock	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including clock	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 66MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 66MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-64		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	64		mA
PWR	Power Dissipation	Reference Page 3-67		250	mW

1. Maximum test duration, one second.

The SC3526 features source series termination Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3526 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3526 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using AC Test Circuit (Page 3-67)

V_{CC} = +5.0V ±5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

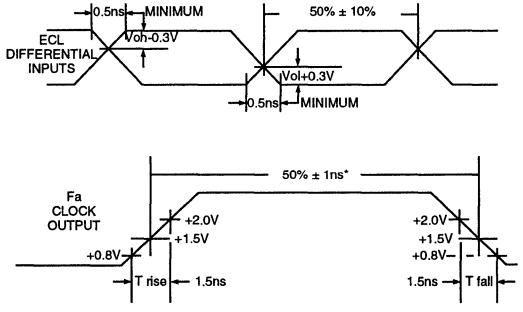
Parameter	SC3526	Units
Maximum Skew Across All Outputs	700	ps
Maximum Output Duty Cycle Asymmetry	±1.0	ns
Maximum TTL Input Frequency	66	MHz
Maximum Differential PECL Input Frequency	66	MHz
Maximum Rising/Falling Edge Rate	1.5	ns
Maximum TTL Output Frequency	66	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3526 output symmetry follows input symmetry for Fc outputs.
3. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

3

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

*Applies only to divide-by-two outputs.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip nine output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all nine outputs.

The clock source input for this device can provide either differential ECL inputs (referenced to +5V, PECL) or single ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The synchronization circuit provides three serial flip flops clocked by the internally generated F/2 (half reference frequency) clock which can be used to provide a three–stage metastability filter or a three–cycle delay of the F/2 outputs. The circuit receives its input from the SYNCIN input and feeds the D–input to the first flip–flop; the Q output of the flip–flop feeds the D–input of the second flip–flop which, in turn, feeds the third flip–flop. The Q output of the third flip–flop drives the SYNCOUT pin.

When the RESET input is held high (active), the FC0–4 outputs will continue to run while the FB0–3 outputs will be driven high. When RESET is de–asserted, the FB0–3 outputs will be active after a fixed three–input clock delay, from a leading edge count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Clock Driver Application Note #1 for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3526 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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Power Management

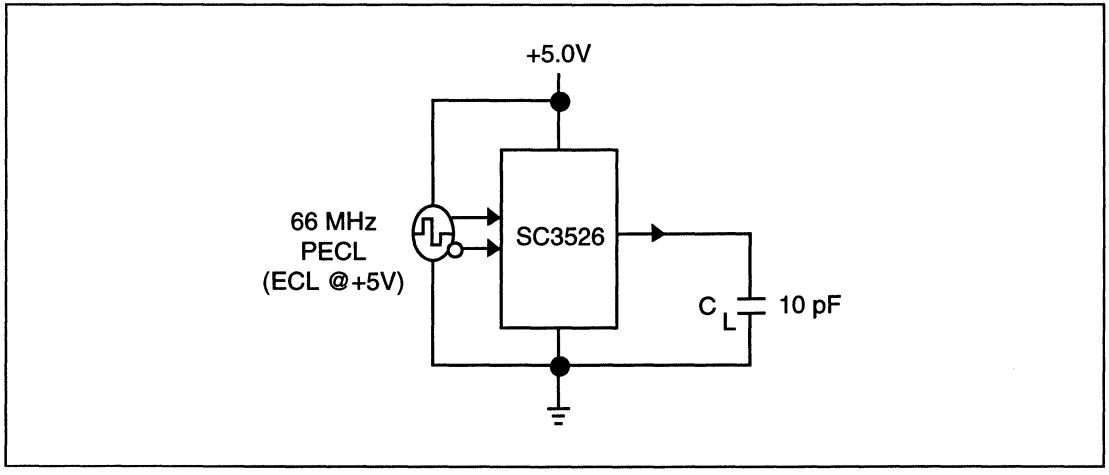
The overall goal of managing the power dissipated by the SC3526 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3526 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-68 for complete load definition). Per output:

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The individual output power must then be added to the static core power (250 mW) of the SC3526 to determine the total power being dissipated by the SC3526. This total power is then multiplied by the SC3526's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3526. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3526 is as follows:

	STILL AIR
THERMAL RESISTANCE	50°C/WATT

AC Test Circuit



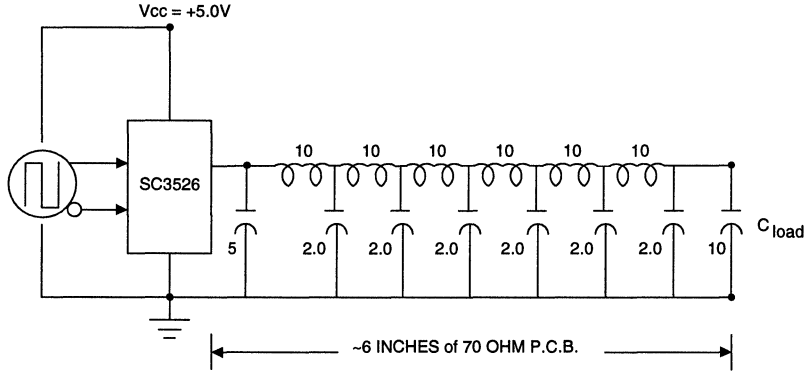
Designing the SC3526 for "Real Loads"

While the AC Test Circuit presented on Page 3-67 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3526 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3526 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 66 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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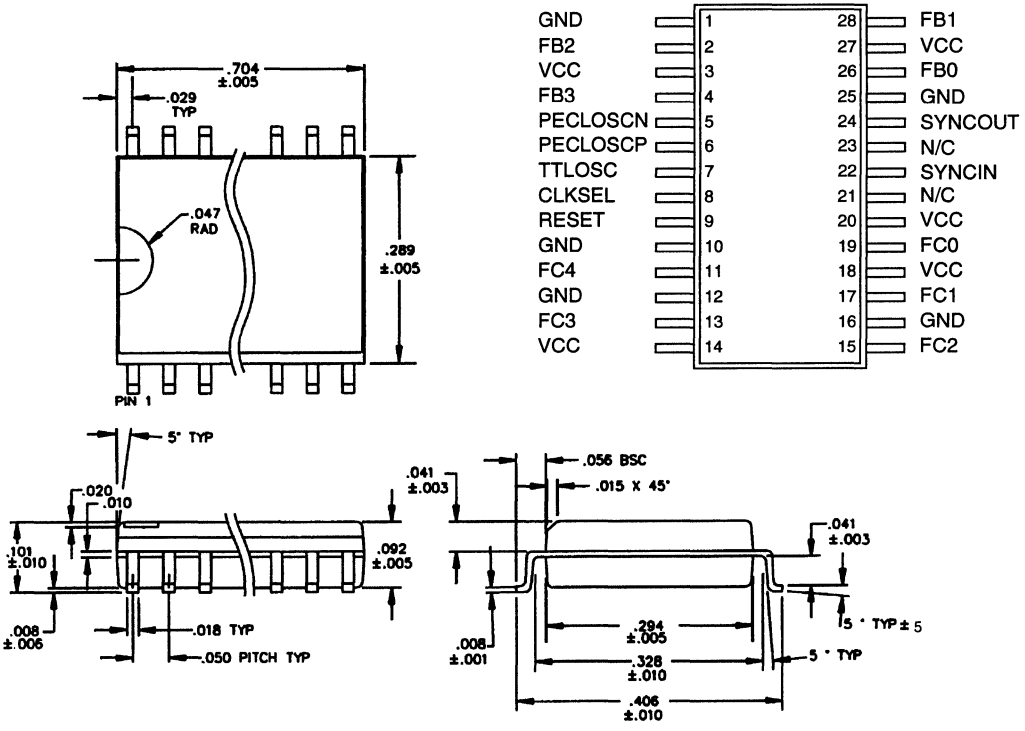
28-Lead Small Outline Integrated Circuit Plastic Package (SOIC)



Dimensions nominal in inches.

Ordering Codes

Package Type	Part Number
28-Lead Small Integrated Circuit Plastic Package	SC3526S

NOTES

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GENERAL DESCRIPTION

The SC3528 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise, distortion, and EMI.

APPLICATIONS

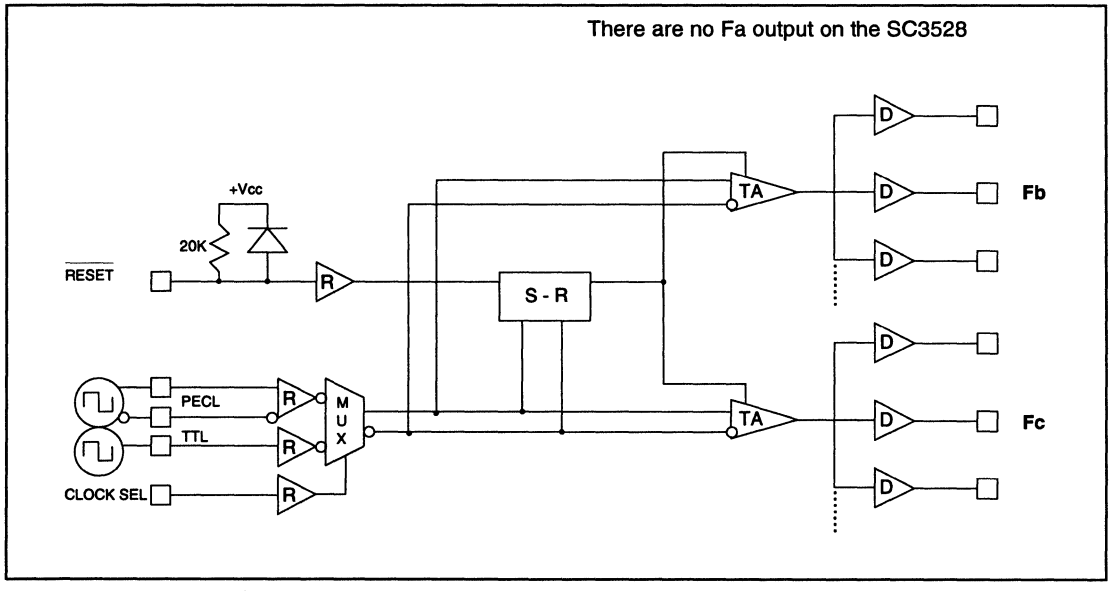
- **High speed clock distribution where signal fidelity and low noise are key requirements**
- **High-performance 80486 and Pentium™-based systems**

FEATURES

- **Ten (10) clock outputs at up to 66 MHz**
- **Leading edge skew for all outputs <700 ps**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω equivalent source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

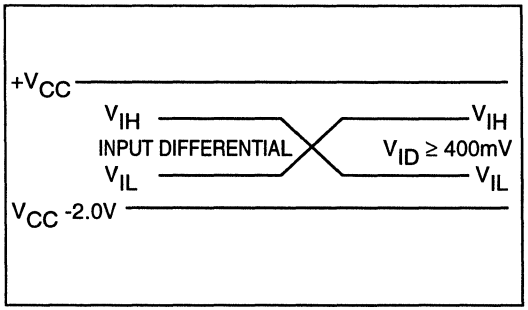
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-75)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including clock	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including clock	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 66MHz max C_L = 10pF	2.6		V
V_{OL}	Output LOW Voltage	F_{OUT} = 66MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-64		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	64		mA
PWR	Static Power Dissipation	Reference Page 3-75		250	mW

1. Maximum test duration, one second.

The SC3528 features source series termination to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3528 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3528 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.6V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using AC Test Circuit (page 3-75)

V_{CC} = +5.0V ±5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

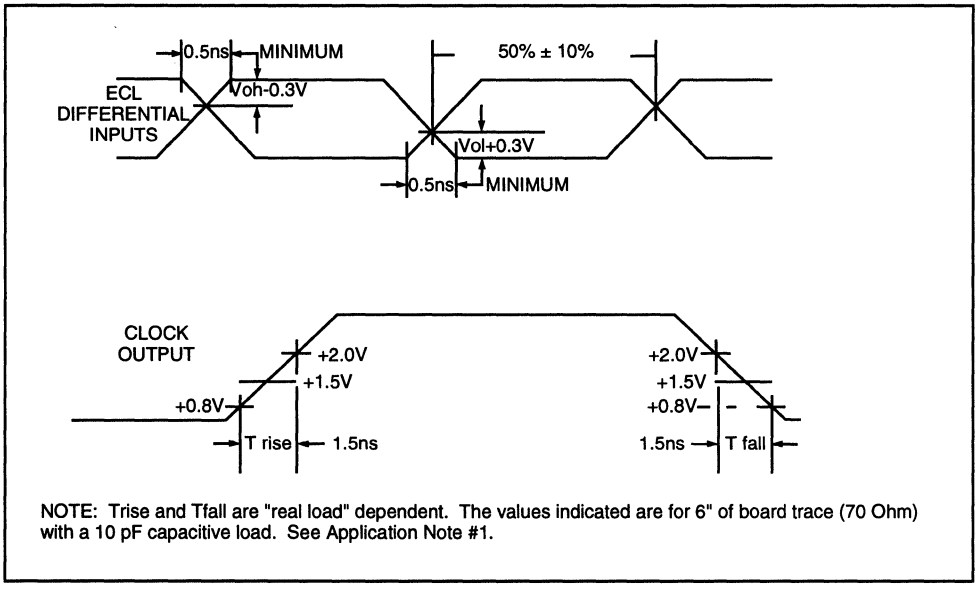
Parameter	SC3528	Units
Maximum Skew Across All Outputs	700	ps
Maximum TTL Input Frequency	66	MHz
Maximum Differential PECL Input Frequency	66	MHz
Maximum Rising/Falling Edge Rate	1.5	ns
Maximum TTL Output Frequency	66	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3528 output symmetry follows input symmetry. Output duty will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

3

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip ten output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all ten outputs.

The clock source input for this device can provide either differential ECL inputs (referenced to +5V, PECL) or single ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. On the fourth falling edge clock input after RESET goes low, the outputs will go low in sequence (the output divide count continues, but once an output goes low it is held low). When RESET is released (high), the outputs will resume counting, after four falling edge clock input delays, from their low state.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Clock Driver Application Note #1 for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3528 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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Power Management

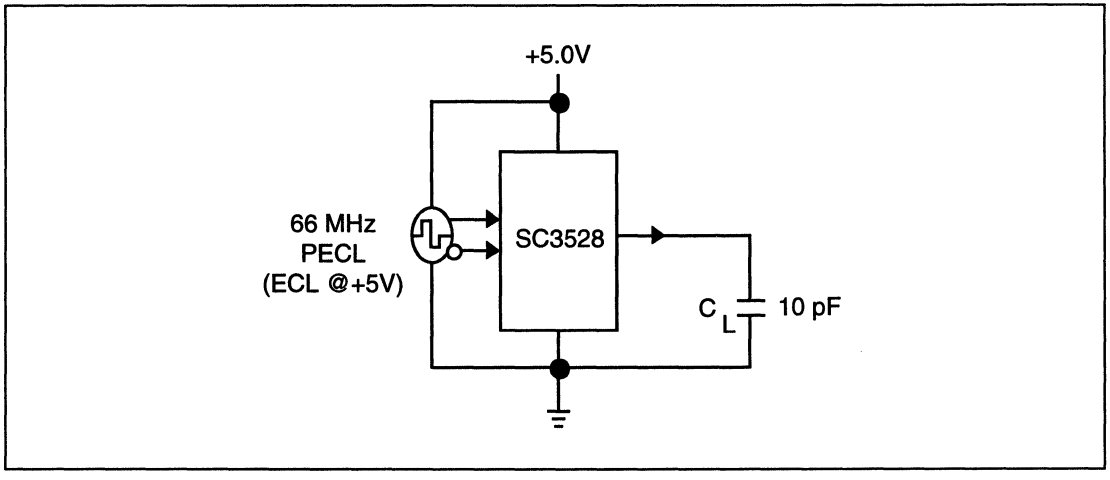
The overall goal of managing the power dissipated by the SC3528 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3528 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-76 for complete load definition). Per output:

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The individual output power must then be summed and added to the static core power (250 mW) of the SC3528 to determine the total power being dissipated by the SC3528. This total power is then multiplied by the SC3528's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3528. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3528 is as follows:

	STILL AIR
THERMAL RESISTANCE	50°C/WATT

AC Test Circuit



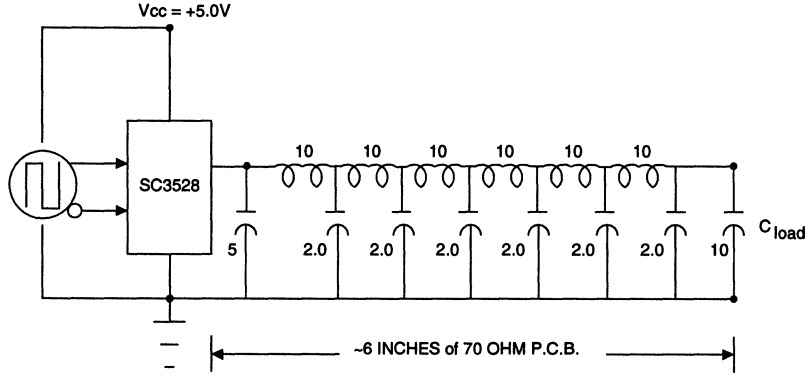
Designing the SC3528 for "Real Loads"

While the AC Test Circuit presented on page 3-75 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3528 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3528 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 66 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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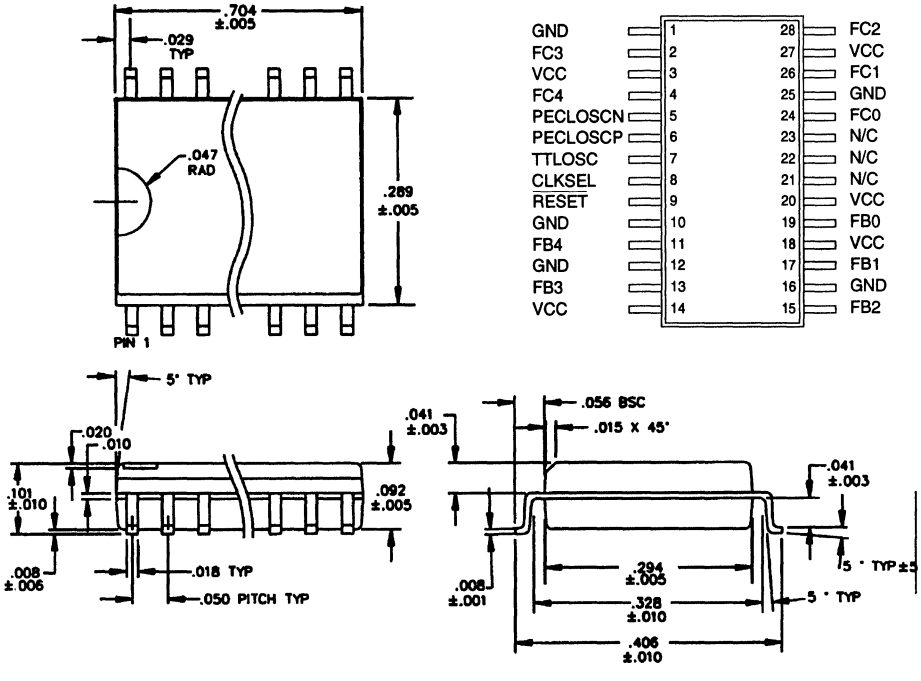
Package 28 Lead Small Outline Integrated Circuit Plastic Package (SOIC)



Dimensions nominal in inches.

Ordering Codes

Package Type	Part Number
28 Lead Small Integrated Circuit Plastic Package	SC3528S

NOTES

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10–OUTPUT CLOCK DRIVER WITH POWER–DOWN FEATURE SC3529

GENERAL DESCRIPTION

The SC3529 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single–ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Power down circuitry is included that allows the disabling of two, five, or all outputs. The two control signals are synchronized to the reference to prevent duty–cycle distortion during power up or power down sequencing.

Applied Micro Circuits Corporation (AMCC) uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise, distortion, and EMI.

APPLICATIONS

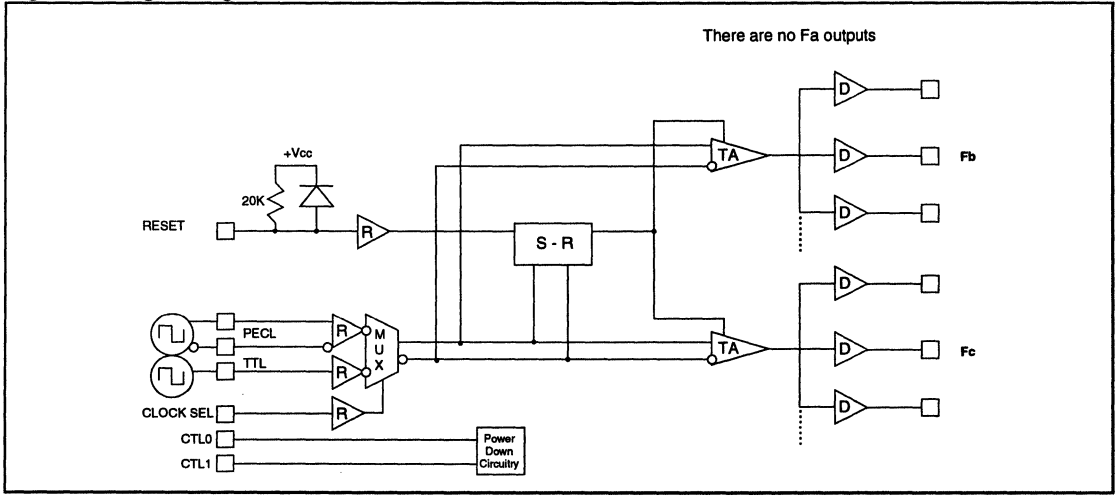
- **High speed clock distribution where signal fidelity and low noise are key requirements**
- **High-performance 80486 and Pentium™-based systems**

FEATURES

- **Ten (10) clock outputs at up to 66 MHz**
- **Two control pins enable power down feature on two, five, or all outputs**
- **Leading edge skew for all outputs <700 ps**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω equivalent source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

3

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

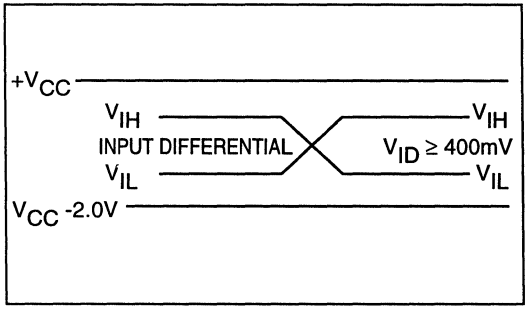
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 3-83)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including clock	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including clock	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL, CTL0, CTL1	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL, CTL0, CTL1	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 66MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 66MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-64		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	64		mA
PWR	Disabled Power Dissipation	Reference Page 3-83 (Outputs High)		250	mW

1. Maximum test duration, one second.

The SC3529 features source series termination to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3529 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3529 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications - Using AC Test Circuit (Page 3-83)

V_{CC} = +5.0V ±5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

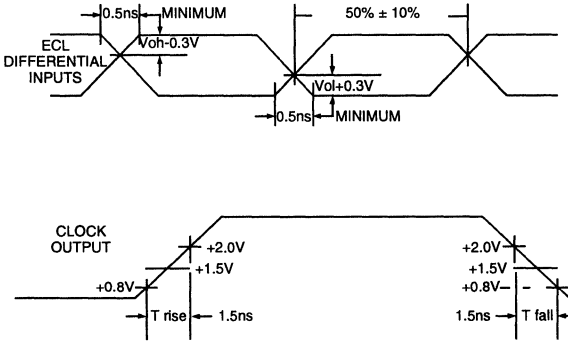
Parameter	SC3529	Units
Maximum Skew Across All Outputs	700	ps
Maximum TTL Input Frequency	66	MHz
Maximum Differential PECL Input Frequency	66	MHz
Maximum Rising/Falling Edge Rate	1.5	ns
Maximum TTL Output Frequency	66	MHz

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. The SC3529 output symmetry follows input symmetry. Output duty cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

3

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip ten output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for minimum skew across all ten outputs.

The clock source input for this device can provide either differential ECL inputs (referenced to +5V, PECL) or single ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The CTL0 and CTL1 inputs can be used to "power down" two, five, or ten of the SC3529's outputs. The control circuitry is designed to be synchronous with the reference clock to prevent duty cycle distortion during power–up or power–down sequencing.

When the inputs are configured per the table below, the appropriate outputs are driven to the minimum power state (LOW). With all outputs disabled, the power of the device is equal to its static dissipation of 200 mW.

CTL0	CTL1	FUNCTION
0	0	All outputs enabled
0	1	FC0–FC4 enabled
1	0	FB0–FB1 enabled
1	1	All outputs disabled

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset" – a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 100 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Clock Driver Application Note #1 for simulation results).

To lower noise and maintain signal fidelity, power and ground pins are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3529 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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Power Management

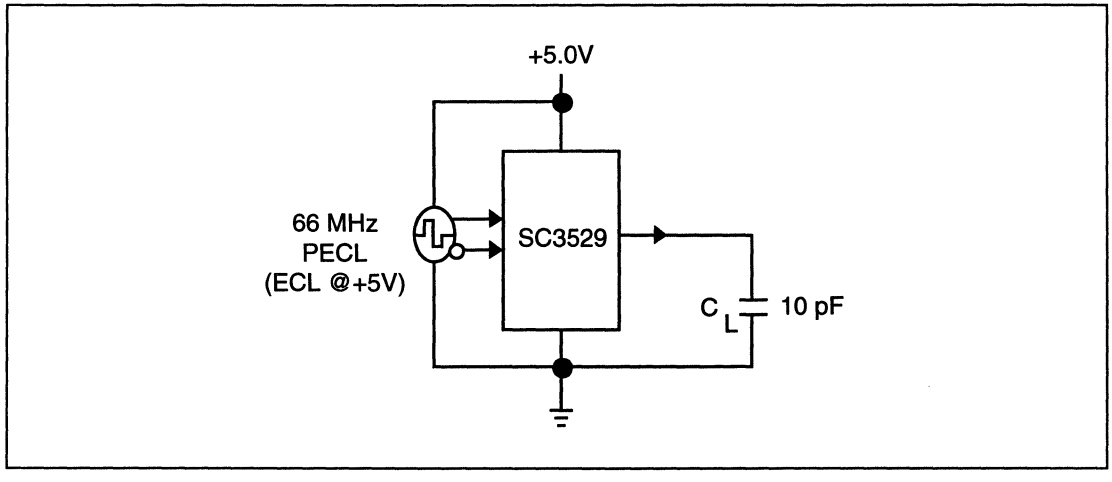
The overall goal of managing the power dissipated by the SC3529 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3529 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 3-84 for complete load definition). Per output:

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
66 MHz	38 mW	47 mW	55 mW	75mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	60 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	52 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The individual output power must then be summed and added to the static core power (250 mW) of the SC3529 to determine the total power being dissipated by the SC3529. This total power is then multiplied by the SC3529's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3529. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3529 is as follows:

	STILL AIR
THERMAL RESISTANCE	50°C/WATT

AC Test Circuit



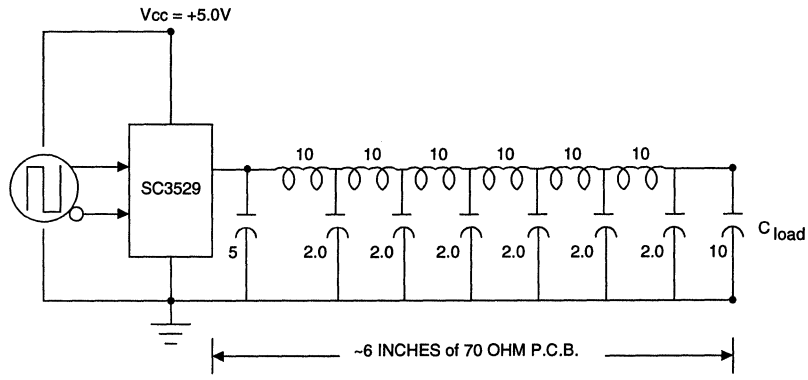
Designing the SC3529 for "Real Loads"

While the AC Test Circuit presented on Page 3-83 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3529 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3529 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 66 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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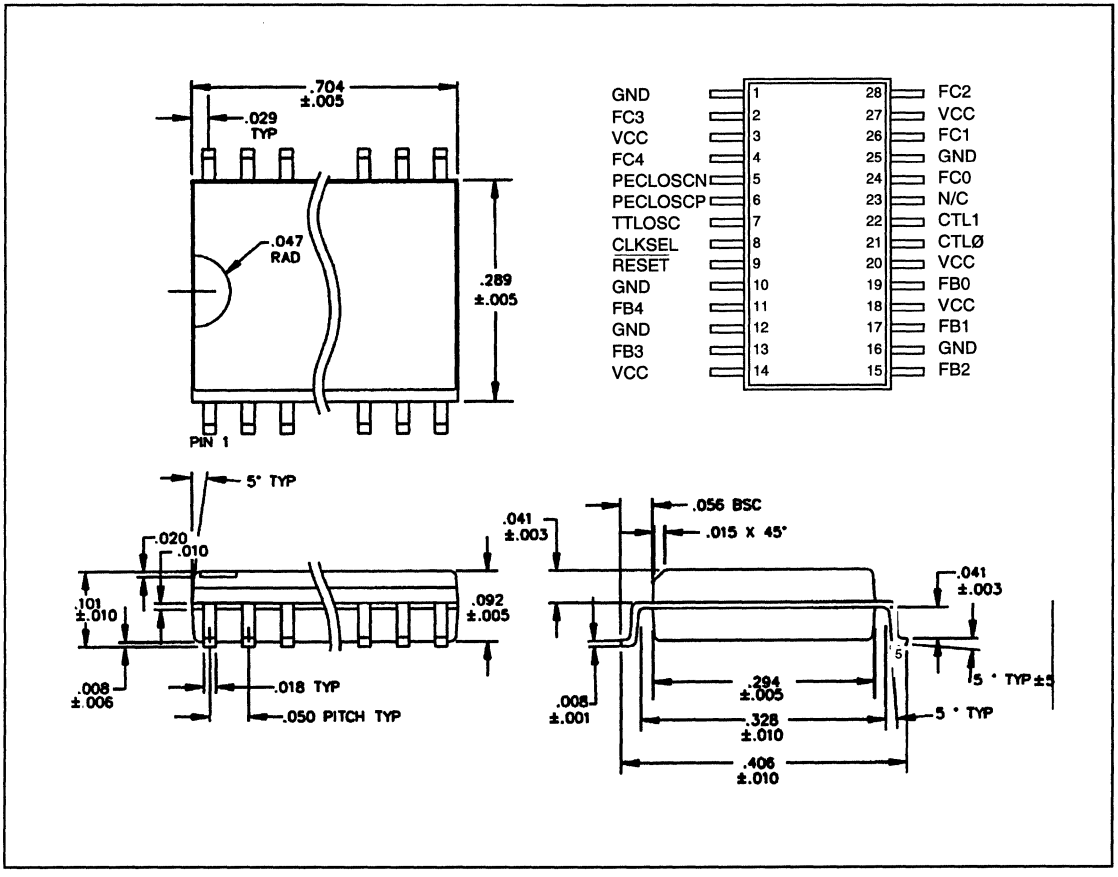
28–Lead Small Outline Integrated Circuit Package (SOIC)



Ordering Codes

Package Type	Part Number
28 Lead Small Integrated Circuit Plastic Package	SC3529S

NOTES

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3V Compatible Clock Drivers

4

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20–OUTPUT LVTTL CLOCK DRIVER

GENERAL DESCRIPTION

The SC3306 is a precision low skew clock driver with 20 outputs. It employs a clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to symmetrical, divide-by-two master-slave flip-flops. The resultant output is distributed to the clock output drivers. All outputs conform with JEDEC LVTTL levels.

The twenty outputs are divided into two groups: group Fb is at the primary frequency, equal to the input; group Fa is at one half of the primary input frequency.

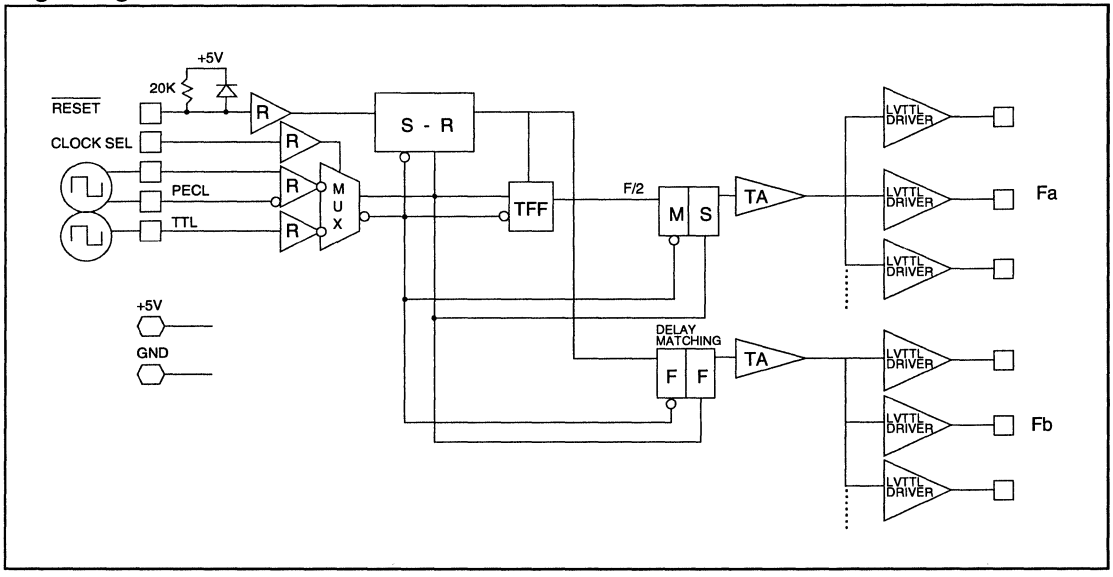
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs:**
  - Ten (10) outputs at primary frequency, up to 80 MHz
  - Ten (10) outputs at 1/2 primary frequency
- **All outputs are leading edge synchronized to within ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **Compatible with Intel's Pentium™ processor**

4

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

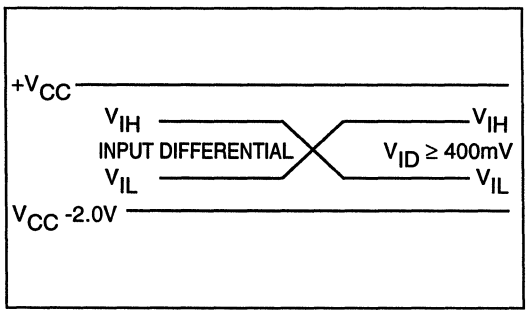
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 4-8)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.4	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 4-7 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3306 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3306 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3306 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

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AC Specifications - Using AC Test Circuit (page 4-8)

V_{CC} = +5.0V ±5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3306-1	SC3306	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Chip to Chip	2.0	—	ns
Maximum Skew Across Fa Outputs	0.25	0.25	ns
Maximum Skew Across Fb Outputs	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry @ 1.5V	±1.0	±1.0	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum Differential PECL Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. Output symmetry follows input symmetry for the 1X outputs.
4. Asymmetry is defined as the deviation from a 50% duty cycle measured at 1.5V. Asymmetry will be effected by voltage, temperature, and load (including the length of the PC trace).
5. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
6. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a twenty output fan-out device using an advanced BiCMOS process. This design has optimized the device for clock symmetry and absolute minimum skew across all twenty outputs. Two harmonic clock frequency groups are provided.

For highest performance this approach requires a clock source input from a crystal controlled oscillator (XCO) located adjacent to the clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V - PECL) or TTL (CMOS) input levels to the clock driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and to output flip-flops for synchronization, refer to the preceeding logic diagram. Using this methodology, the output duty cycle for the F/2 or Fa group becomes largely a function of output driver slew rate into the AC load.

The Fb group duty cycle is governed by the input source clock. The output flip-flops are reset keyed for leading edge alignment. These outputs are amplified to fan out to AMCC's complementary source terminated LVTTL output drivers.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin (see "Relative Output Timing", pg. 4-8, and "Reset To Output Timing",in the Application Note #1).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50-75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Application Note #1 for Spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to simultaneously switching outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3306 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Power Management

The overall goal of managing the power dissipated by the SC3306 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3306 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 4-9 for complete load definition).

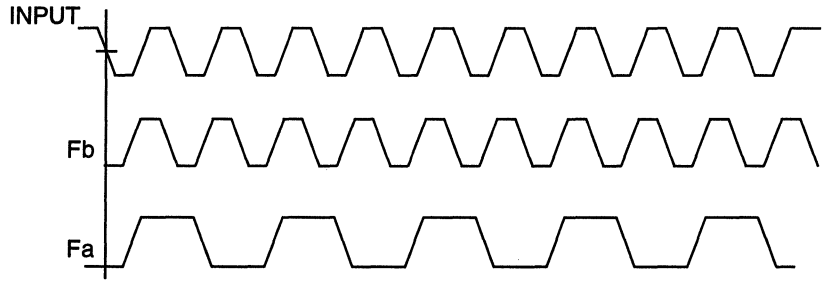
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	92 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	77 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	60 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	49 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	42 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	36 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	31 mW	7 mW

The above output power must then be added to the core power (400 mW) of the SC3306 to determine the total power being dissipated by the SC3306. This total power is then multiplied by the SC3306's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3306. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3306 is as follows:

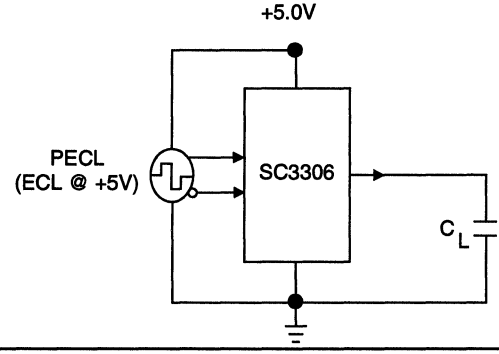
	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: AN SC3306 with 8 of the Fb outputs running at 66 MHz with 10 pF loads (8 x 33 = 264 mW + 2 x 11 = 22 mW for an Fb Total of 286 mW), 3 of the Fa outputs are running at 33 MHz with 5 pF loads (3 x 13 = 39 mW), and 2 Fa outputs running at 33 MHz with 15 pF loads (2 x 17 = 34 mW + 5 x 8 = 40 mW for an Fa Total of 113 mW). The Total Chip Power is Core Power (400 mW) + Fb Power (286 mW) + Fa Power (113 mW) = 799 mW. Your design calls for a 70°C Still Air ambient. The SC3306's junction temperature would then be: 70°C + (.799 Watts x 50°C/Watt = 40°C) = 110°C, below the 140°C maximum.

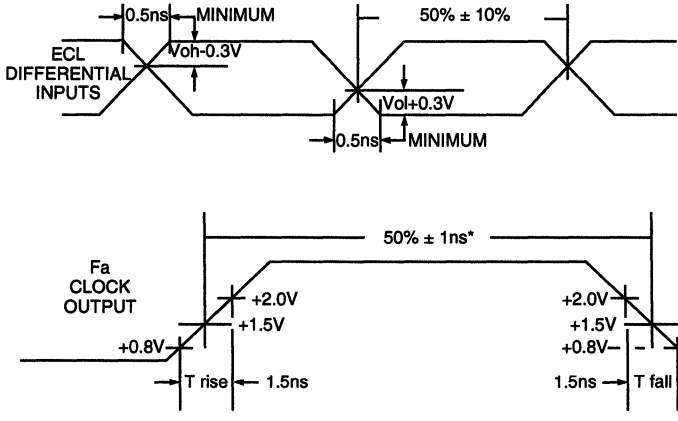
Relative Output Timing



AC Test Circuit



Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

*Applies only to divide-by-two outputs.

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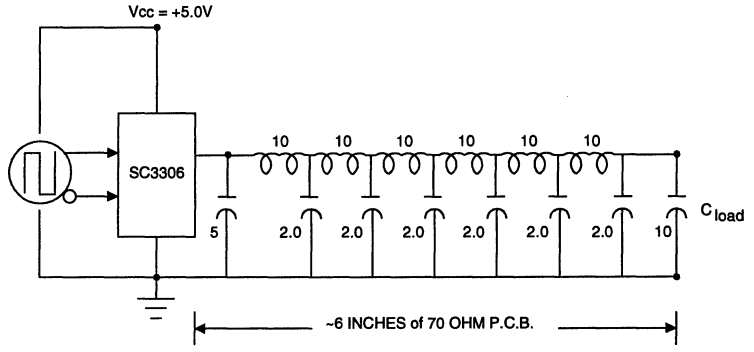
Designing the SC3306 for "Real Loads"

While the AC Test Circuit presented on Page 4-8 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3306 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3306 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note #1.

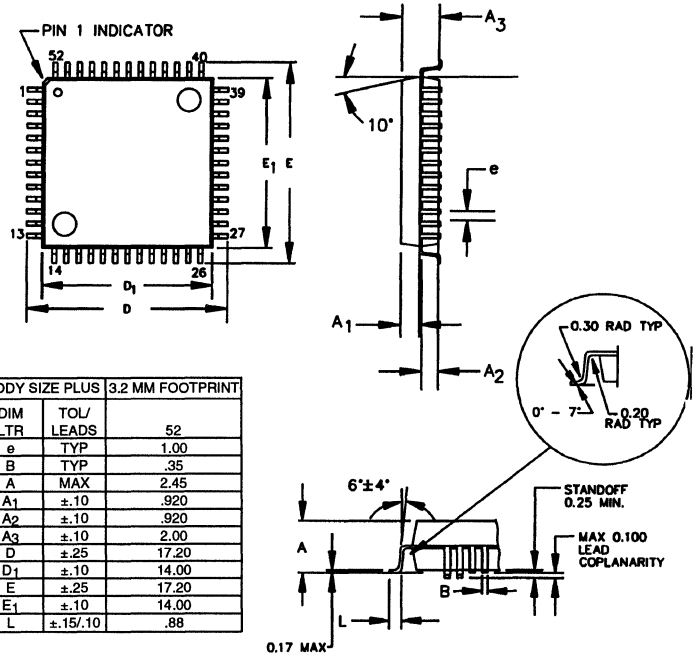
Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

52–Pin Plastic Quad Flat Pack

PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	27	NC
2	GND	28	NC
3	FB4	29	FB5
4	GND	30	GND
5	FB3	31	FB6
6	VCC	32	VCC
7	FB2	33	FB7
8	GND	34	GND
9	FB1	35	FB8
10	VCC	36	VCC
11	FB0	37	FB9
12	VCC	38	PECL OSCN
13	VCC	39	PECL OSCP
14	VCC	40	TTL OSC
15	GND	41	GND
16	FA0	42	FA9
17	VCC	43	VCC
18	FA1	44	FA8
19	GND	45	GND
20	FA2	46	FA7
21	VCC	47	VCC
22	FA3	48	FA6
23	GND	49	GND
24	FA4	50	FA5
25	VCC	51	VCC
26	NC	52	CLK SEL



BODY SIZE PLUS	3.2 MM FOOTPRINT	
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

All dimensions in mm.

Ordering Codes

Package Type	Max Skew Across All Outputs	Part Number
52 Lead Plastic Quad Flat Pack	0.5 ns	SC3306Q-1
52 Lead Plastic Quad Flat Pack	1.0 ns	SC3306Q

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20–OUTPUT LVTTL CLOCK DRIVER SC3308

GENERAL DESCRIPTION

The SC3308 is a minimum skew clock driver with 20 outputs. It can employ a clock input from a single ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTL levels.

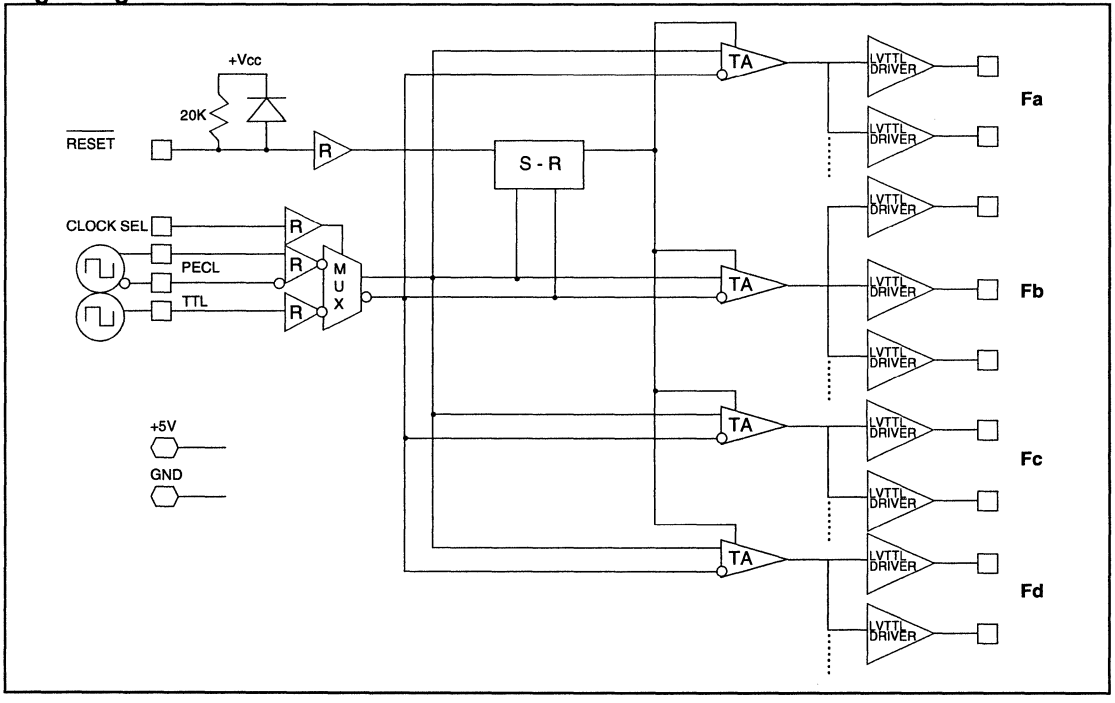
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Twenty (20) clock outputs at primary frequency up to 80 MHz**
- **All outputs are leading edge synchronized to within ≤0.5ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **Compatible with Intel's Pentium™ Processor**

4

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

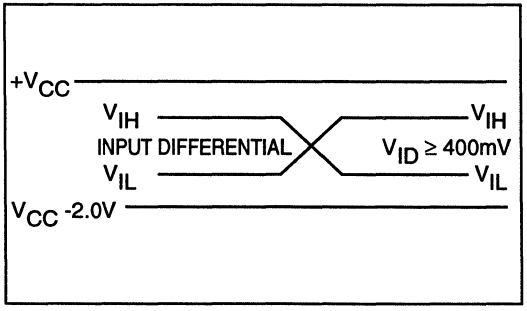
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 4-15)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.4	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 4-15 @ 70°C		400	mW

1. Maximum test duration, one second.

The SC3308 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3308 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3308 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

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AC Specifications - Using AC Test Circuit (Page 4-15)

Vcc = +5.0V ±5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

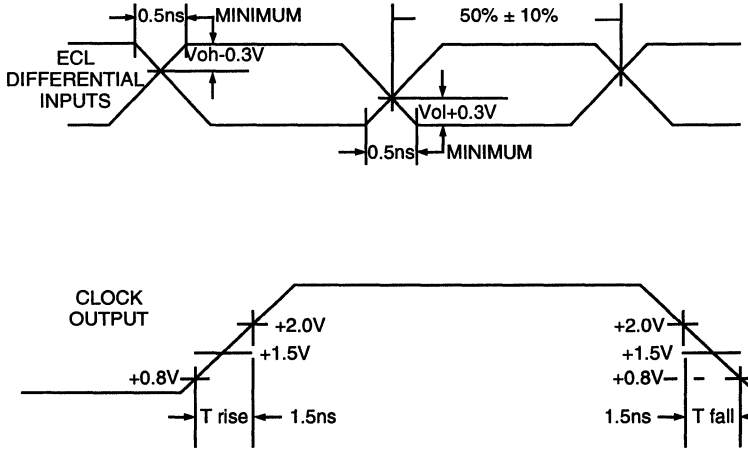
Parameter	SC3308-1	SC3308	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Chip to Chip	2.0	—	ns
Maximum Skew Across Fa, Fb, Fc, or Fd Outputs	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rates	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. SC3308 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.

4

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm). with a 10 pF capacitive load. See Application Note #1.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip clock buffer and twenty output fan-out driver using AMCC's advanced BiCMOS process. This design is optimized the device for absolute minimum skew across all twenty outputs.

For best performance this approach will require a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V - PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to translation amplifiers and output drivers, (refer to the preceding logic diagram). The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Clock Driver Application Note #1 for spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to simultaneously switching outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Clock Driver Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3308 will exhibit skews less than the specified maximum. A plastic 52 lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Power Management

The overall goal of managing the power dissipated by the SC3308 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3308 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 4-16 for complete load definition).

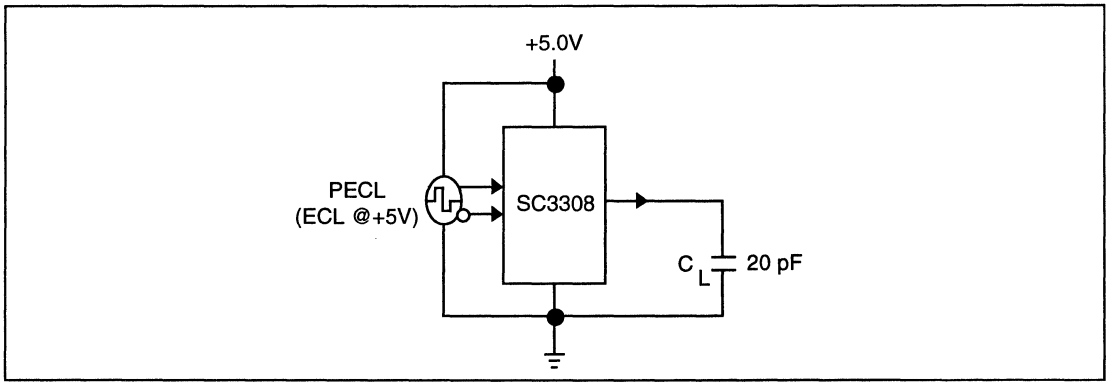
FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	92 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	77 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	60 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	49 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	42 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	36 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	31 mW	7 mW

The above output power must then be added to the core power (400 mW) of the SC3308 to determine the total power being dissipated by the SC3308. This total power is then multiplied by the SC3308's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3308. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3308 is as follows:

	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	50°C/WATT	40°C/WATT	35°C/WATT

For example: You have a SC3308 with 12 of the outputs running at 50 MHz with 15 pF loads (12 x 27 = 324 mW + 8 x 10 = 80 mW for a Total of 404 mW). The Total Chip Power is Core Power (400 mW) + output Power (404 mW) = 804 mW. Your design calls for a 70°C Still Air ambient. The SC3308's junction temperature would then be: 70°C + (.804 Watts x 50°C/Watt = 40°C) = 110°C, which is below the 140°C maximum junction temperature.

AC Test Circuit



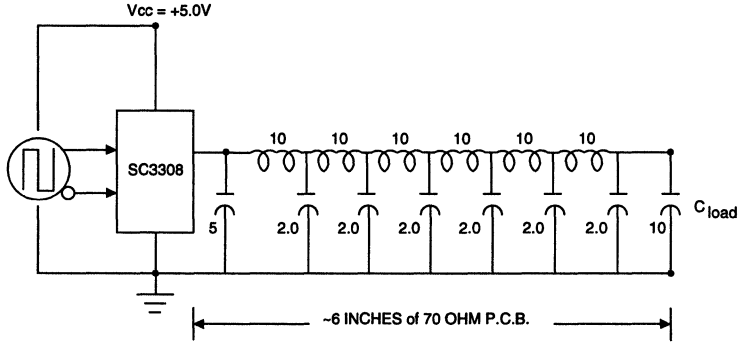
Designing the SC3308 for "Real Loads"

While the AC Test Circuit presented on Page 4-15 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3308 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3308 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in Clock Driver Application Note #1.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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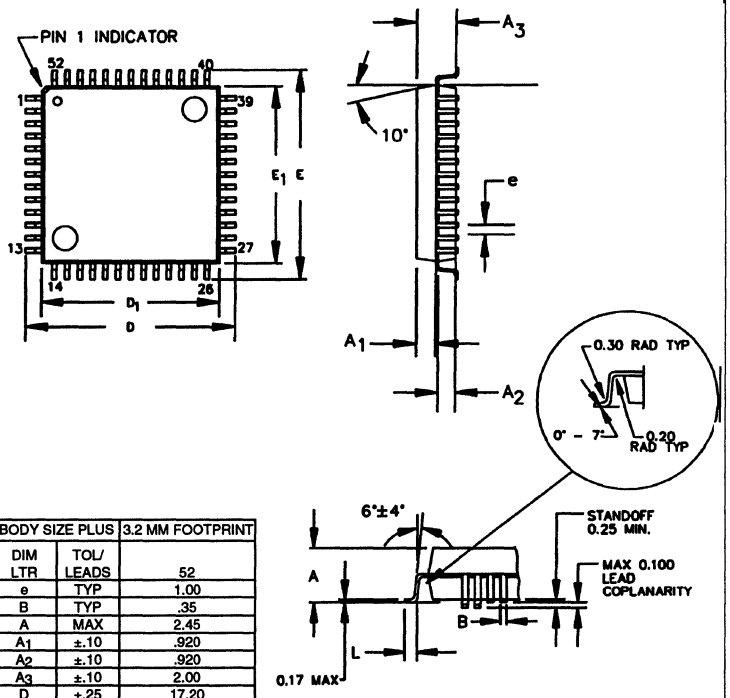
52–Pin PQFP Package

PIN #	SIGNAL	PIN #	SIGNAL
1	$\overline{\text{RESET}}$	27	NC
2	GND	28	NC
3	FA0	29	FC0
4	GND	30	GND
5	FA1	31	FC1
6	VCC	32	VCC
7	FA2	33	FC2
8	GND	34	GND
9	FA3	35	FC3
10	VCC	36	VCC
11	FA4	37	FC4
12	VCC	38	PECL OSCN
13	VCC	39	PECL OSCP
14	VCC	40	TTL OSC
15	GND	41	GND
16	FB0	42	FD0
17	VCC	43	VCC
18	FB1	44	FD1
19	GND	45	GND
20	FB2	46	FD2
21	VCC	47	VCC
22	FB3	48	FD3
23	GND	49	GND
24	FB4	50	FD4
25	VCC	51	VCC
26	NC	52	CLK SEL

All dimensions in mm.



BODY SIZE PLUS	3.2 MM FOOTPRINT	
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

Ordering Codes

Package Type	Max Skew Across All Outputs	Part Number
52 Lead Plastic Quad Flat Pack	0.5 ns	SC3308Q-1
52 Lead Plastic Quad Flat Pack	1.0 ns	SC3308Q

NOTES

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10–OUTPUT LVTTL CLOCK DRIVER SC3318

GENERAL DESCRIPTION

The SC3318 is a minimum skew clock driver with ten outputs. It can employ a clock input from a single ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTL levels.

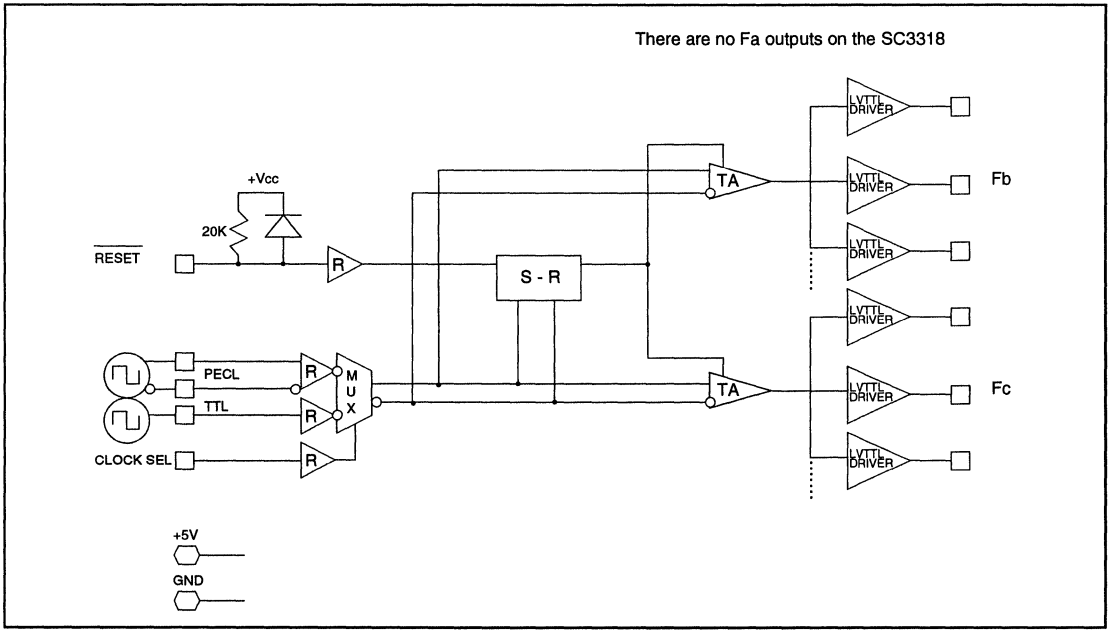
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

FEATURES

- **Ten (10) clock outputs at primary frequency up to 80 MHz**
- **All outputs are leadiing edge synchronized to within ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **Eliminates the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **Compatible with Intel's Pentium™ processor**

4

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

Electrical Characteristics

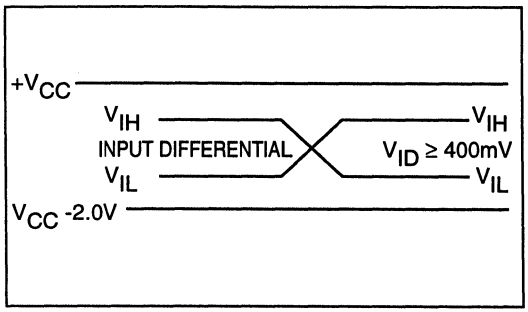
V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference AC Test Circuit, Page 4-23)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC} + .3	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.4	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Power Dissipation	Reference Page 4-23 @ 70°		400	mW

1. Maximum test duration, one second.

The SC3318 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The SC3318 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3318 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

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AC Specifications – Using AC Test Circuit (Page 4-23)

V_{CC} = +5.0V ± 5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

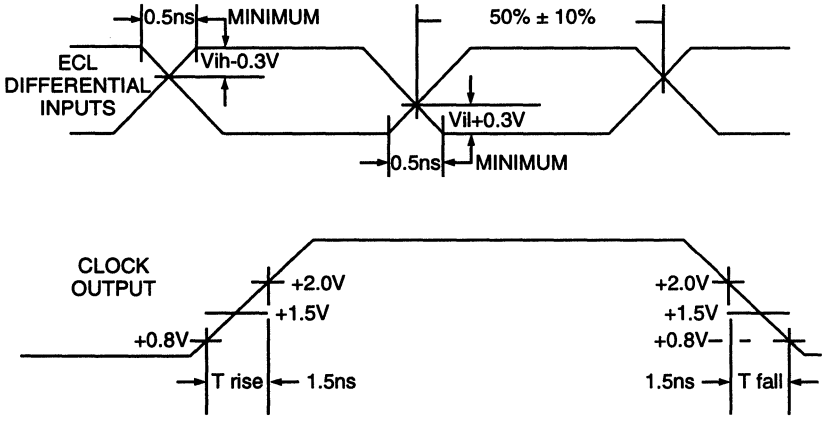
Parameter	SC3318-1	SC3318	Units
Maximum Skew Across All Outputs	0.5	1.0	ns
Maximum Skew Chip to Chip	2.0	—	ns
Maximum Skew Across Fa or Fb Outputs	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum Differential PECL Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip to chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip to chip skew tested at 70°C.
3. The SC3318 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for high loads.

4

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See Application Note #1.

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

AMCC has developed a single chip ten output clock buffer driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all ten outputs.

The clock source input for this device may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V , PECL) or single ended TTL (CMOS) input levels to AMCC's Clock Driver. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagram. The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset" - a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) the outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see Application Note #1 for spice models).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance and capacitance of the package and wire bonding is managed to insure that the SC3318 will exhibit skews less than the specified maximum. A plastic 28 lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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Power Management

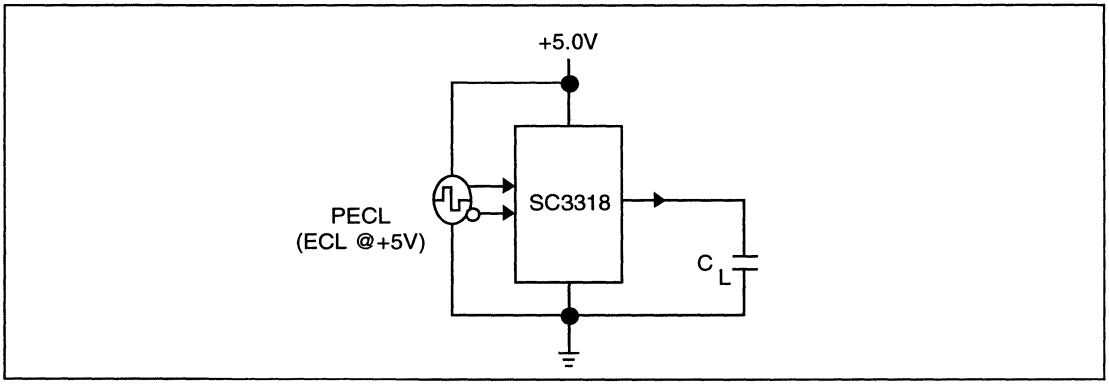
The overall goal of managing the power dissipated by the SC3318 is to limit it's junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3318 is determined by the load that each output drives and the frequency that each output is running. The following table summarizes these dependencies (see Evaluation Circuit on Page 4-24 for complete load definition).

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	92 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	77 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	60 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	49 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	42 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	36 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	31 mW	7 mW

The above output power must then be added to the core power (400 mW) of the SC3318 to determine the total power being dissipated by the SC3318. This total power is then multiplied by the SC3318's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3318. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3318 is as follows:

	STILL AIR
THERMAL RESISTANCE	50°C/WATT

AC Test Circuit



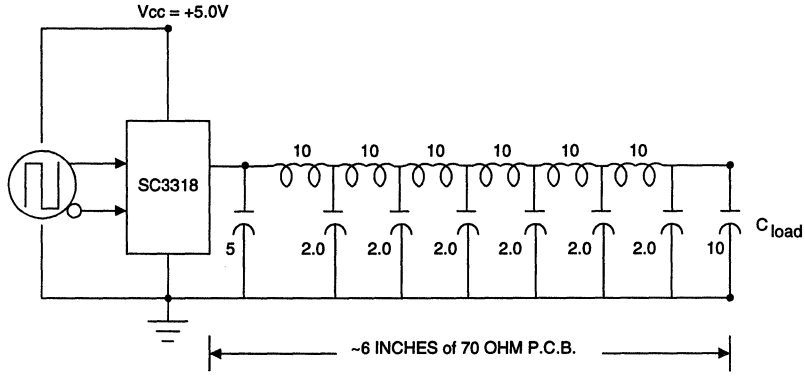
Designing the SC3318 for "Real Loads"

While the AC Test Circuit presented on Page 4-23 can be adequate for initial device evaluation and incoming inspection, it does not represent "real loads" in products.

AMCC has designed the SC3318 to provide clean clock transitions when presented with a realistic reactive load. AMCC's assumptions are that the SC3318 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading will cause overall impedance to drop to under 50 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with input capacitive loads ranging up to 15 pF at frequencies up to 80 MHz. Higher load capacitance can be accommodated by two parallel outputs.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented below. This is a midpoint model and can be modified to reflect a specific end use.

Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point load destination is recommended

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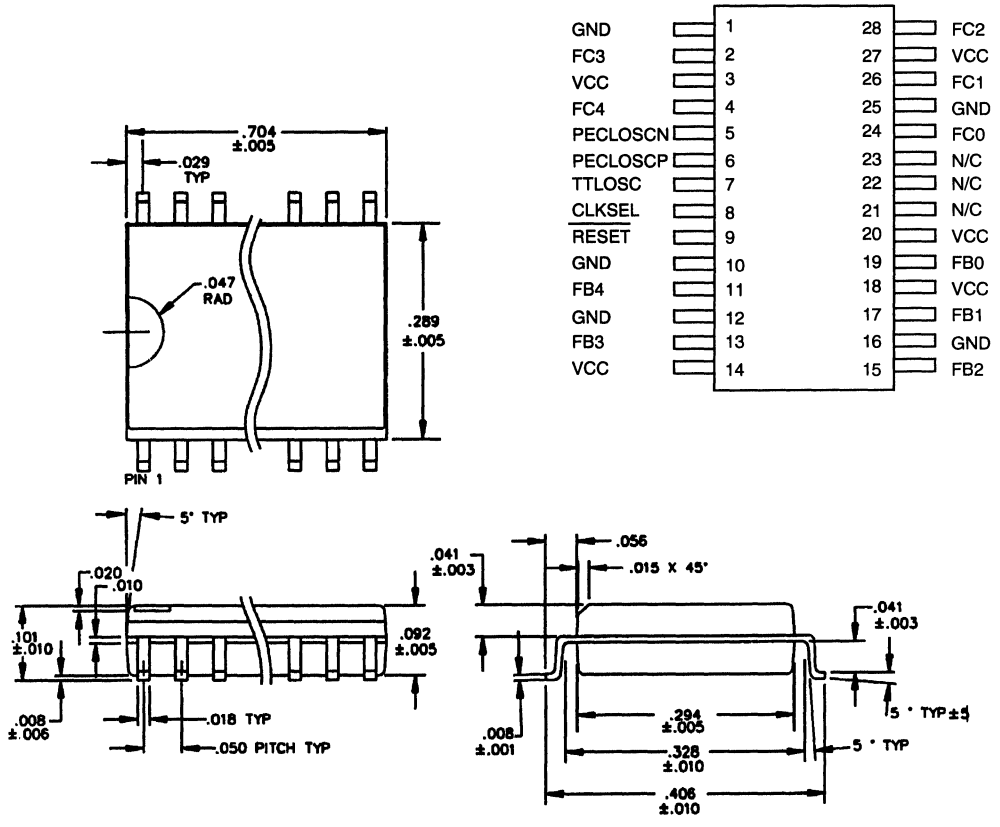
28-Lead Small Outline Integrated Circuit Plastic Package (SOIC)



All dimensions in inches.

Ordering Codes

Package Type All Outputs	Max Skew Across	Part Number
28 Lead Small Integrated Circuit Plastic Package	0.5 ns	SC3318S-1
28 Lead Small Integrated Circuit Plastic Package	1.0 ns	SC3318S

NOTES

Clock Generators and Synthesizers 5

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BiCMOS PLL CLOCK GENERATORS S4402/S4403

FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (the S4403 generates ten outputs and HFOUT generates 10MHz to 40MHz)
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation in board test
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 28/44 PLCC packages

APPLICATIONS

- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

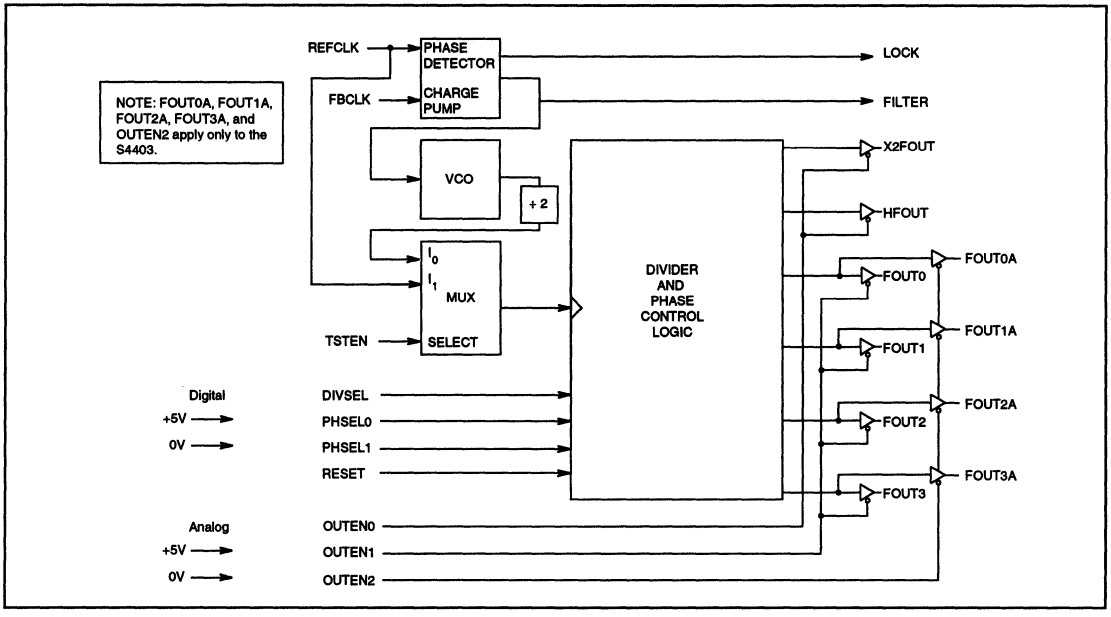
GENERAL DESCRIPTION

The S4402/S4403 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a single off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4402 generates six TTL outputs, while the S4403 provides those six plus four duplicates (FOUT0A–FOUT3A) for a total of ten. Output enables are provided for the various banks, allowing clock control for board and system tests.

5

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

Frequency and Phase Controls

The S4402/S4403 clock generators provide multiple outputs that are synchronized in both frequency and phase to a periodic clock input. Two select pins and an external feedback path allow the user to phase-adjust the six outputs (FOUT0–FOUT3, HFOUT, and X2FOUT) relative to the input clock REFCLK, as well as control their frequency.

The DIVSEL input controls the programmable divider that follows the voltage controlled oscillator (VCO). This doubles the lock range of the PLL by allowing the user to select a VCO frequency divided by four (DIVSEL Low) or by eight (DIVSEL High).

The frequency of the four FOUT0–FOUT3 outputs (and the duplicate set of the four FOUT0A–FOUT3A outputs on the S4403) is determined by the REFCLK clock frequency and the output that is tied back to the FBCLK input. In addition, the X2FOUT TTL output provides a clock signal identical to the FOUT0 output in the divide-by-four mode, and twice the FOUT0 frequency (maximum frequency of 80 MHz) in the divide-by-eight mode. The HFOUT TTL output provides a clock signal that is in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes. Refer to the Output Select Matrix in Table 3 for the specific relationships.

Phase adjustments can be made in increments as small as 3.125 ns. The minimum phase delay between FOUT0–FOUT3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight, controlled by DIVSEL. The minimum phase delay t is equal to the period of the VCO frequency:

$$t = 1 / \text{VCO freq}$$

Since the VCO can operate in the 160 MHz to 320 MHz range, minimum phase delay values can range from 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The PHSEL1 and PHSEL0 inputs allow the user to select several phase relationships among the four FOUT0–FOUT3 TTL clock outputs. These choices can be seen in Table 2, and the Output Select Matrix provided in Table 3 describes the 21 output configurations available to the user. The two "Select Pins" columns specify the signal levels on the pins PHSEL0 and PHSEL1. These are active High signals. The column entitled "Output Fed to FBCLK" indicates which output (FOUT0–FOUT3, HFOUT, or X2FOUT) is externally connected to the feedback input (FBCLK) to produce the resulting waveforms shown in the appropriate row in the table. The last seven columns specify the resulting phase and frequency relationships of each output to the user clock input (REFCLK). A negative value indicates the time by which the output rising edge precedes the input (REFCLK) rising edge. A positive value is the time by which the rising edge of the output follows the rising edge of the input clock.

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	FOUT0–FOUT3 outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	FOUT1 lags FOUT0 by minimum phase, FOUT2 lags FOUT1 by minimum phase, and FOUT3 lags FOUT2 by minimum phase

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to REFCLK, FOUT1 will lead REFCLK by a minimum phase delay, FOUT2 will lag REFCLK by a minimum phase delay, FOUT3 will phase-lag REFCLK by 90°, HFOUT will be phase-aligned with REFCLK but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Several other waveform examples and typical applications are provided on pages 5-8 and 5-9.

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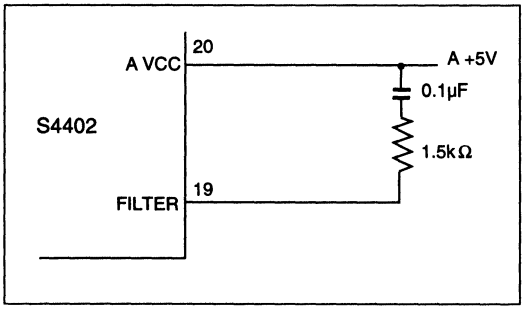
Enabling Outputs

The S4402 has two output-enable inputs that control which outputs toggle. (The S4403 has three output-enable inputs.) When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–FOUT3 outputs. The third input on the S4403, OUTEN2, controls the duplicate set of four outputs FOUT0A–FOUT3A. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the REFCLK input. The filter components should be in surface mounted packages with minimum lead inductance.

Figure 2. External PLL Filter

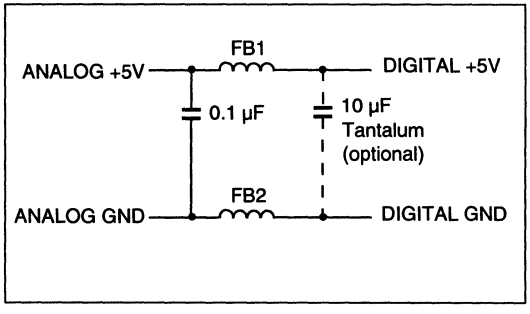


Power Supply Considerations

Power for the analog portion of the S4402/S4403 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 3. External Power Supply Filter



Reset

When the RESET pin is pulled low, all the internal states go to zero one clock cycle (from the VCO or REFCLK in the test mode) before the outputs go low. After the chip is reset, the PLL requires a resynchronization time of ≤5ms before lock is again achieved.

Lock Detect

A lock detect function is provided by the LOCK output. When REFCLK and FBCLK are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Test Capabilities

The TSTEN input puts the S4402/S4403 into a test mode and allows users to bypass the VCO and provide their own clock through the REFCLK input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

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PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

OUTEN2. (S4403 only.) Active Low. Controls the duplicate set of outputs to FOUT0–FOUT3 (FOUT0A, FOUT1A, FOUT2A, AND FOUT3A).

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

LOCK. Goes high when REFCLK and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

FOUT0A. (S4403 only.) Clock output—duplicates FOUT0.

FOUT1A. (S4403 only.) Clock output—duplicates FOUT1.

FOUT2A. (S4403 only.) Clock output—duplicates FOUT2.

FOUT3A. (S4403 only.) Clock output—duplicates FOUT3.

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Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					÷4	÷8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT	X2FOUT	
1	0	0	FOUT0–FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (÷8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	–Q	0	Q	2Q	–Q/2	–Q	2(–Q)
6	0	1	FOUT2	–2Q	–Q	0	Q	–2Q/2	–2Q	2(–2Q)
7	0	1	FOUT3	–3Q	–2Q	–Q	0	–3Q/2	–3Q	2(–3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (÷8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	–t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	t/2	t	2(t)
12	1	0	FOUT2	–t	–2t	0	Q–t	–t/2	–t	2(–t)
13	1	0	FOUT3	–Q	–Q–t	–Q+t	0	–Q/2	–Q	2(–Q)
14	1	0	HFOUT	2(0)	2(–t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (÷8)	0/2	–t/2	t/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	–t	0	t	2t	–t/2	–t	2(–t)
18	1	1	FOUT2	–2t	–t	0	t	–2t/2	–2t	2(–2t)
19	1	1	FOUT3	–3t	–2t	–t	0	–3t/2	–3t	2(–3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (÷8)	0/2	t/2	2t/2	3t/2	0/4		0

Notes:
1. "0" implies the output is aligned with REFCLK.
2. "t" implies the output lags REFCLK by a minimum phase delay.
3. "Q" implies the output lags REFCLK by 90° of phase
4. "–t" implies the output leads REFCLK by a minimum phase delay.
5. "–Q" implies the output leads REFCLK by 90° of phase.
6. "2( )" implies the output is at twice the frequency of REFCLK.

Legend

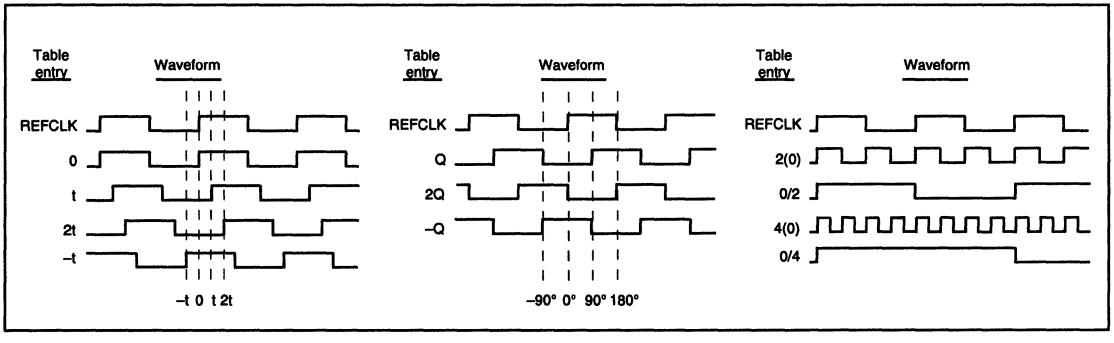
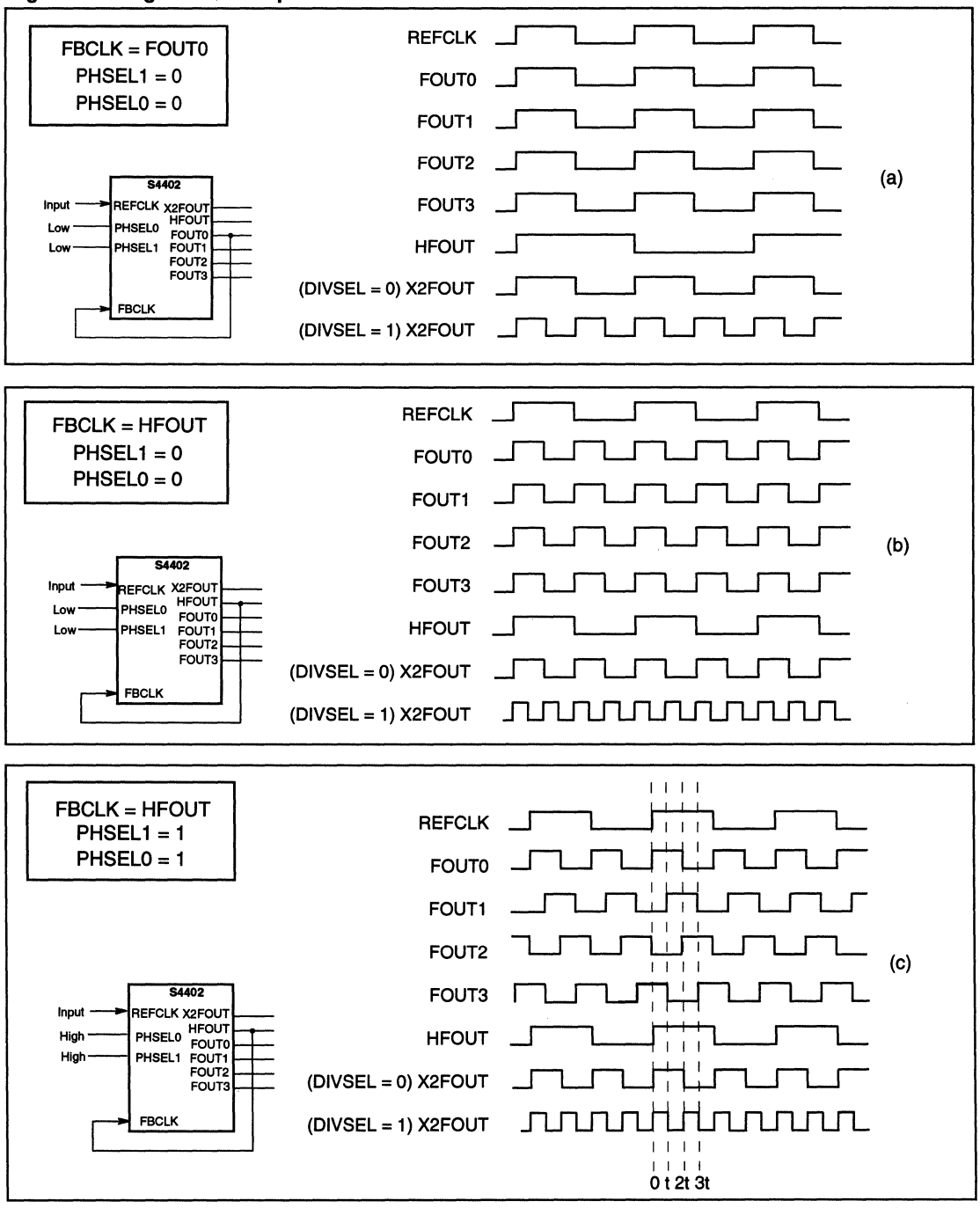


Figure 4. Configuration Examples



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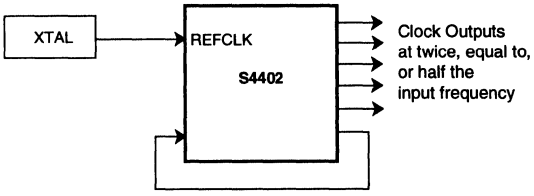
TYPICAL APPLICATIONS

The S4402/S4403 chips are designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

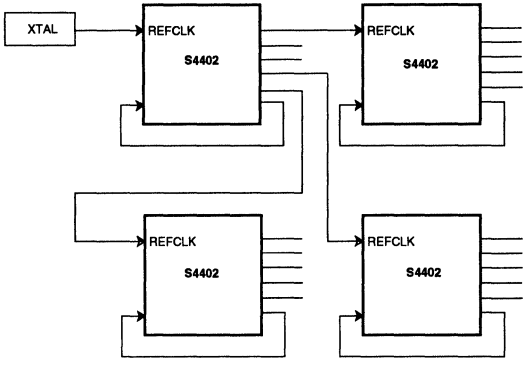
Application 1. High-Frequency, Low-Skew Clock Generation

One of the most basic capabilities of the S4402/S4403 devices is generating multiple phase-aligned low-skew clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards, and synchronization will be maintained.



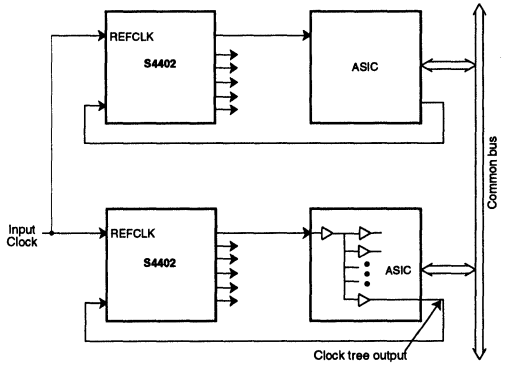
Application 2. Low-Skew Clock Distribution

One common problem in clocking high-speed systems is that of distributing several copies of a system clock while maintaining low skew throughout the system. The S4402/S4403 devices guarantee low skew among all the clocks in the system, as they have effectively zero delay between their input and output signals, with an output skew of less than 400 ps. The user can also adjust the phases of the outputs in increments as small as 3.125 ns, for load and trace length matching.



Application 3. Delay Compensation

Since the relative edges of the S4402/S4403 outputs can be precisely controlled, these chips can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The S4402s ensure that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.



ABSOLUTE MAXIMUM RATINGS

	Commercial
TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Commercial			Units
	Min	Nom	Max	
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18mA			-0.8	-1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} = -12mA[3] (COM)	2.4			V
			I_{OH} = -24mA[3] (COM)	2.0			V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 24mA[3] (COM)			0.5	V
I_{IH}	Input HIGH current	V_{CC} = Min, V_{IN} = 2.4V	OUTEN2			-200	µA
			Other			50	µA
I_I	Input HIGH current at max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW current	V_{CC} = Min, V_{IN} = 0.5V	OUTEN2			-500	µA
			Other			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max	COM			70	mA
I_{CC}	Total I_{CC} (Dynamic and Static)	V_{LOAD} = 25pF at 50 MHz	COM			190	mA

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration is one second.

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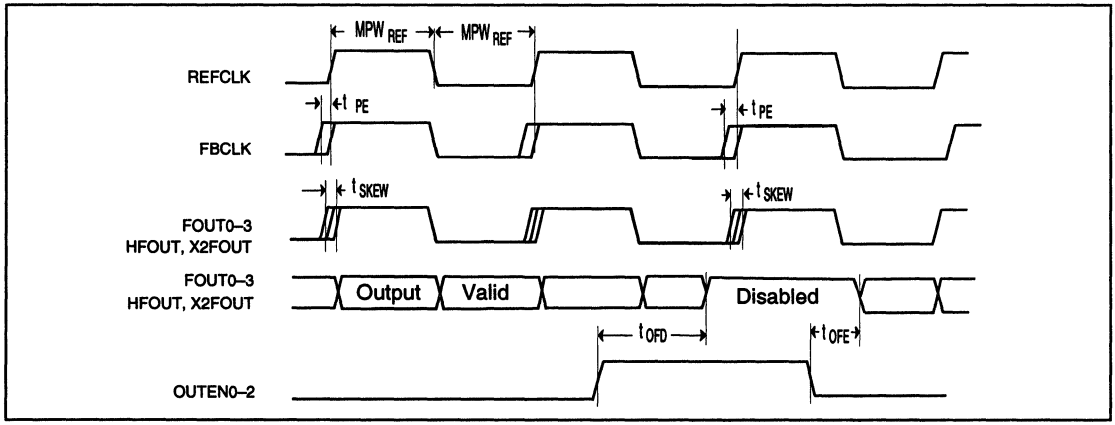
Table 4. AC Specifications

Symbol	Description	S4402/3-66		S4402/3-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	7.0		6.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	0	750	ps
t_{SKEW}	Output Skew[2]	0	400	0	400	ps
t_{DC}	Output Duty Cycle[3]	45	55	45	55	%
f_{FOUT}	FOUT Frequency[4]	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency[4]	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency[4]	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{PSJ}	Phase Shift Variation[5]	-250	+250	-250	+250	ps
t_{OFD}	Tpd OUTEN0–2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0–2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time[6]	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[7]		5		5	ms
t_j	Clock Stability[8]		500		500	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35pF, measured at 1.5V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to FOUT0 at 1.5V.
6. With 35 pF output loading (0.8 V to 2.0 V transition).
7. Depends on loop filter chosen. (Number given is for example filter.)
8. Clock period jitter with all FOUT outputs operating at 66 MHz and loaded with 25pF using loop filter shown. Parameter guaranteed, but not tested.

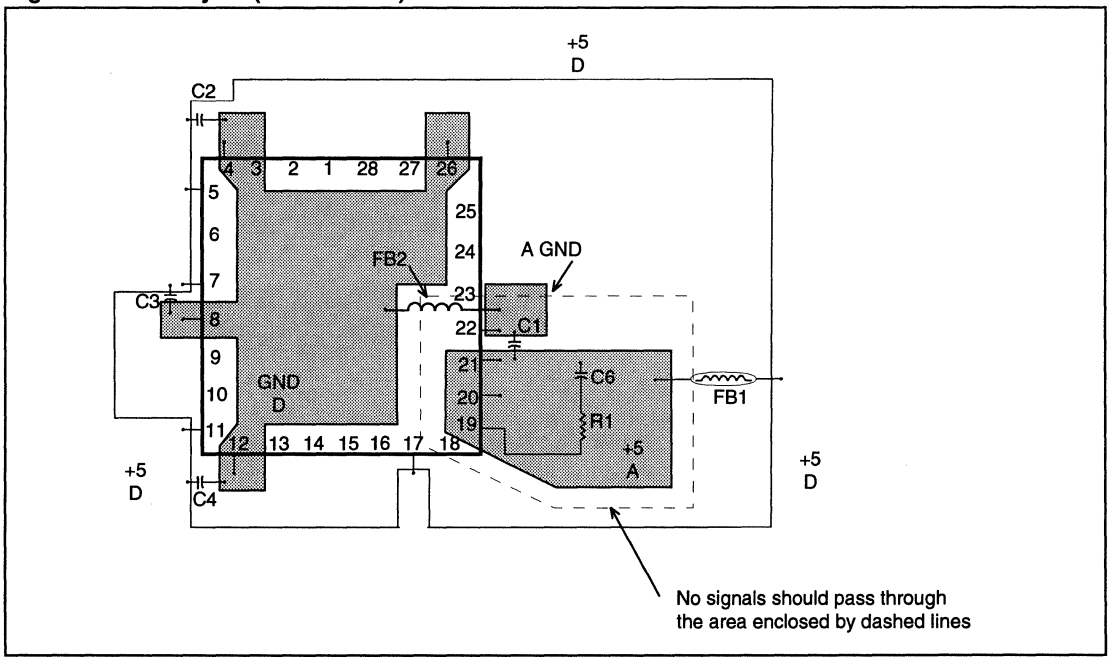
Figure 5. Timing Waveforms



BOARD LAYOUT CONSIDERATIONS

- The S4402/S4403 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4402/S4403 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 6) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 6. Board Layout (S4402 shown)



Component	Description
C1–C4	0.1 µF ceramic capacitor
C6	0.1 µF ceramic capacitor
R1	1.5 K 10% resistor
FB1,FB2	Ferrite bead or inductor

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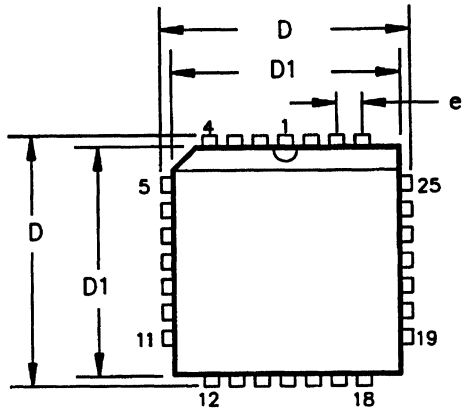
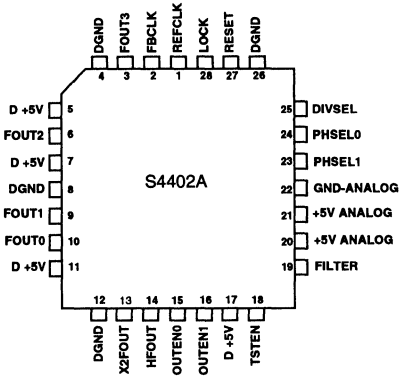
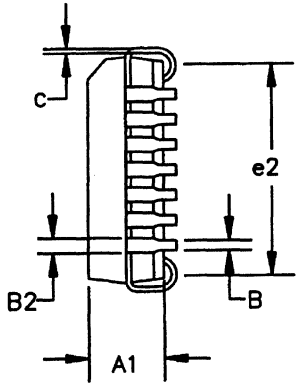
Figure 7. S4402 28 PLCC Package and Pinout







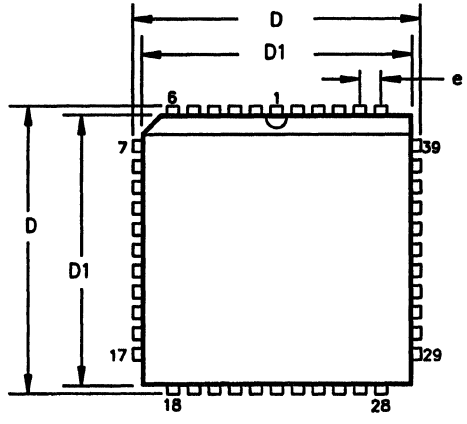
SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.487	.497
D1	.444	.459
e	.048	.052
e2	.410	.430

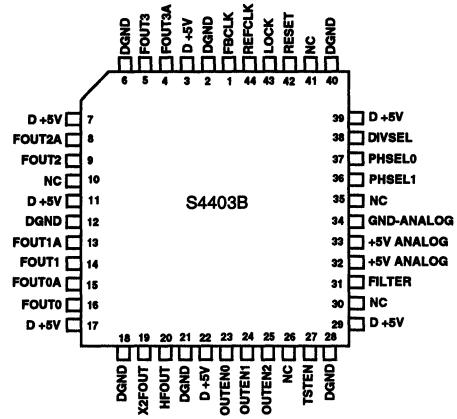
All dimensions nominal in inches.

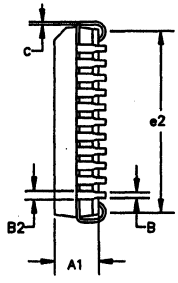
28 PLCC Thermal Resistance

Still Air	100 Linear Ft./Min	200 Linear Ft./Min
60°C/Watt	50°C/Watt	45°C/Watt

Figure 8. S4403 44 PLCC Package and Pinout







SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.687	.697
D1	.644	.659
e	.048	.052
e2	.610	.630

All dimensions nominal in inches.

44 PLCC Thermal Resistance

Still Air	100 Linear Ft./Min	200 Linear Ft./Min
45°C/Watt	40°C/Watt	35°C/Watt

Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE	MAX FREQ
S—commercial	4402	A—28 PLCC	-66 (66 MHz)
S—commercial	4402	A—28 PLCC	-80 (80 MHz)
S—commercial	4403	B—44 PLCC	-66 (66 MHz)
S—commercial	4403	B—44 PLCC	-80 (80 MHz)

X Grade — **XXXX** Part number — **X** Package — **XX** Speed

Example: S4403B-66 — Commercial grade, S4403, 44 PLCC package, 66 MHz

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BiCMOS PECL CLOCK GENERATOR S4405

FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (HFOUT operates from 10 MHz to 40 MHz)
- Allows PECL or TTL reference input
- Provides differential PECL output at up to 160 MHz
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 44 PLCC package

APPLICATIONS

- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

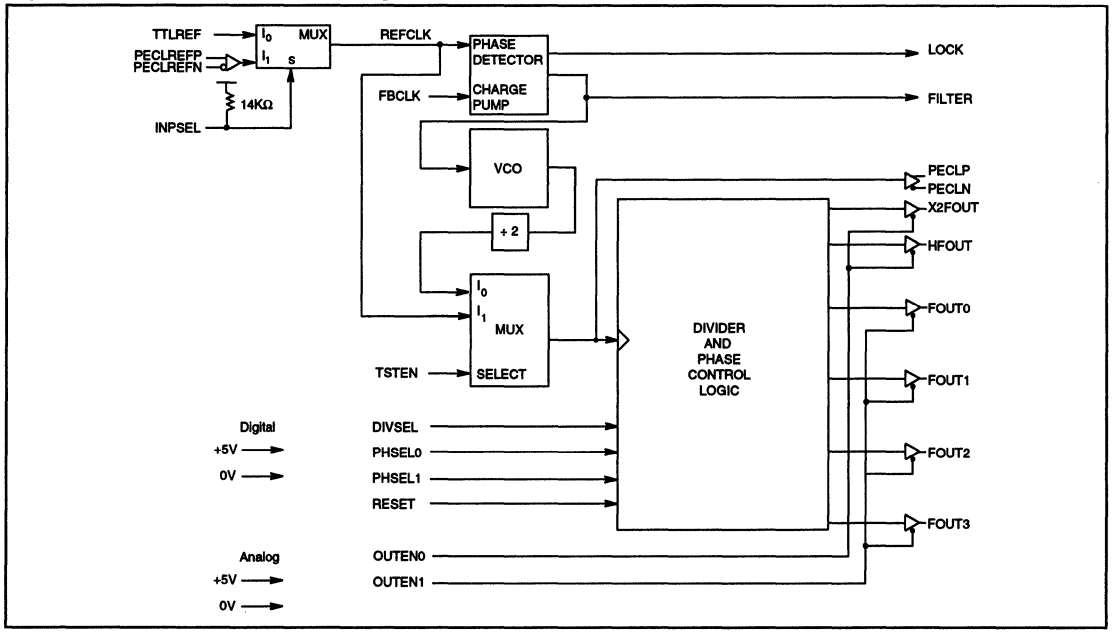
GENERAL DESCRIPTION

The S4405 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a simple off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. The reference is selectable to be either TTL or PECL. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4405 generates six TTL outputs and one differential PECL output. Output enables are provided for the various TTL banks, allowing clock control for board and system tests.

5

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

This BiCMOS clock generator is designed to allow the user to generate TTL clocks, in the 10–80 MHz range, with less than 400 ps of skew. Implemented in AMCC's 1.0µ BiCMOS technology, the internal VCO, phase detector, and programmable divider and phase selector allow the user to tailor the TTL output clocks for his/her system needs. The internal VCO can operate between 160 to 320 MHz, and the programmability allows the user to generate TTL output clocks in the 10–80 MHz range, and a differential +5V referenced ECL output at 80–160 MHz.

The clock generator offers the user the ability to select the appropriate phase relationship among the four FOUT0–3 TTL clock outputs. The phase selection choices are shown in Table 2.

The clock generator also allows the user to choose the divide-by ratio between the VCO frequency and the frequency of the FOUT0–3 signals. The VCO frequency can be divided by 4 when DIVSEL is low, and divided by 8 when DIVSEL is high. The divide ratio between the VCO and the pseudo ECL outputs, PECLP and PECLN, is a fixed divide-by-2.

The clock generator also has two output enable inputs which can be used to control which outputs toggle. OUTEN0 controls the HFOUT and X2FOUT outputs, and OUTEN1 controls the FOUT0–3 outputs. When the output enables are high, the outputs are disabled, and held in a high state.

REFCLK can be driven by either the TTLREF or PECLREF inputs. The reference clock source is selected with the INPSEL input. When INPSEL is low, the TTLREF input is selected as the reference clock.

The FOUT0–3 outputs are the main TTL output clocks that the generator supplies. The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input. FOUT0–3 will be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK. The X2FOUT TTL output provides a clock signal that is identical to the FOUT0 output in the divide-by-4 mode, but twice the FOUT0 frequency (max. freq. of 66 MHz) in the divide-by-8 mode. The HFOUT TTL output provides a clock signal that is also in phase with the FOUT0 output, but at half the FOUT0 frequency.

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single resistor and one capacitor) can be included in the phase-locked loop of the clock generator.

The LOCK output goes high when the reference clock and FBCLK are within 2–4 ns of each other. This output tells the user that the PLL is in lock.

Three pins are included for test purposes. TESTEN allows the chip to use the REFCLK signal instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. The RESET pin initializes the internal counter flip-flops to zeros, but several clock cycles are necessary before the outputs go to a zero state.

The minimum phase delay between FOUT0–3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight. The minimum phase delay is equal to the period of the VCO frequency: M_P = 1/VCO freq. Since the VCO can operate in the 160 MHz to 320 MHz range, the range of minimum phase delay values is 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The charge pump and VCO portion of the chip use a separate analog power supply. This supply is brought onto the chip through a distinct set of power and ground pins. This supply should be free of digital switching noise.

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	Outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	Outputs skewed by minimum phase (determined by the divider selection, and the VCO frequency) from each other.

Note: The PECL output is not affected by the phase select inputs.

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can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to the reference clock, FOUT1 will lead the reference clock by a minimum phase delay, FOUT2 will lag the reference clock by a minimum phase delay, FOUT3 will phase-lag the reference clock by 90°, HFOUT will be phase-aligned with the reference clock but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Enabling Outputs

The S4405 has two output-enable inputs that control which outputs toggle. When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–3 outputs. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the reference clock input.

Reset

When the RESET pin is pulled low, all the internal states go to zero, but the outputs will not go low until one clock cycle later (VCO/2 or period of the reference clock). After the chip is reset, the PLL requires a resynchronization time before lock is again achieved.

Lock Detect

A lock detect function is provided by the LOCK output. When the selected reference clock and FBCLK are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4405 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4405 is sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4405 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 4) to avoid the possibility of noise due to crosstalk.

Figure 2. External PLL Filter

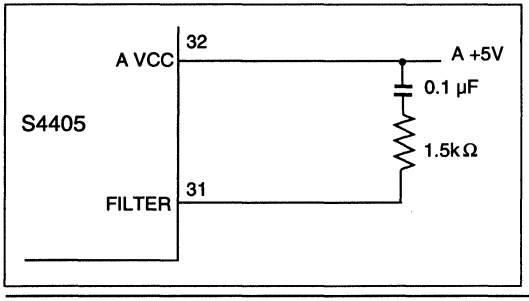
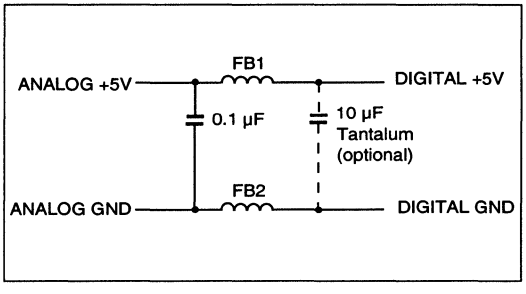


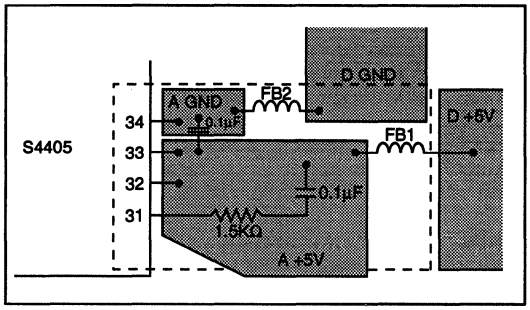
Figure 3. External Power Supply Filter



• The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.

• The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 4. Board Layout



Test Capabilities

The TSTEN input allows users to bypass the VCO and provide their own clock through the selected reference clock input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

TTLREF. TTL. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. INPSEL is used to select between this reference and the PECL reference PECLREFP/N.

PECLREFP/N. Differential PECL. Frequency reference supplied by the user. Selectable by the INPSEL input.

FBCLK. Feedback clock that, along with the reference clock input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK can be divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

INPSEL. Allows user to select between TTLREF and PECLREF reference frequencies. When INPSEL is High, the PECLREF input is selected.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

PECLP/N. Differential PECL output, always one-half the VCO frequency.

LOCK. Goes high when the reference clock and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

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Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships						
									÷4	÷8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT	X2FOUT	
1	0	0	FOUT0–FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (÷8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	–Q	0	Q	2Q	–Q/2	–Q	2(–Q)
6	0	1	FOUT2	–2Q	–Q	0	Q	–2Q/2	–2Q	2(–2Q)
7	0	1	FOUT3	–3Q	–2Q	–Q	0	–3Q/2	–3Q	2(–3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (÷8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	–t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	t/2	t	2(t)
12	1	0	FOUT2	–t	–2t	0	Q–t	–t/2	–t	2(–t)
13	1	0	FOUT3	–Q	–Q–t	–Q+t	0	–Q/2	–Q	2(–Q)
14	1	0	HFOUT	2(0)	2(–t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (÷8)	0/2	–t/2	t/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	–t	0	t	2t	–t/2	–t	2(–t)
18	1	1	FOUT2	–2t	–t	0	t	–2t/2	–2t	2(–2t)
19	1	1	FOUT3	–3t	–2t	–t	0	–3t/2	–3t	2(–3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (÷8)	0/2	t/2	2t/2	3t/2	0/4		0

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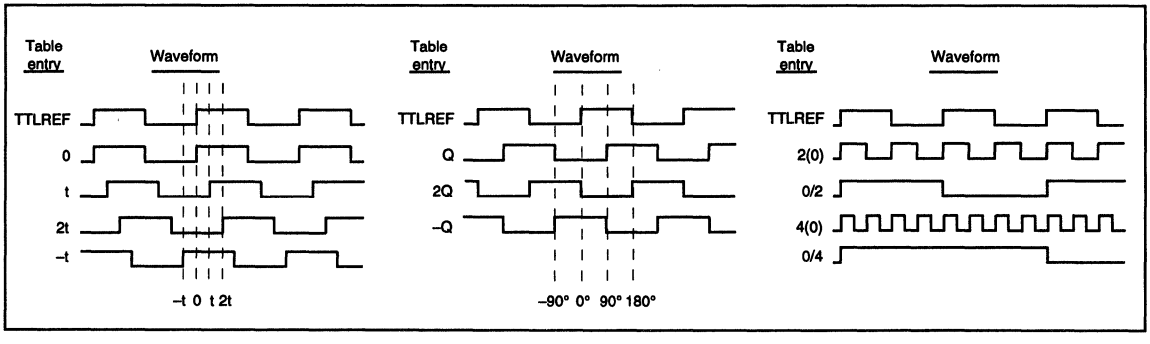
Notes:
1. "0" implies the output is aligned with the reference clock.
2. "t" implies the output lags the reference clock by a minimum phase delay.
3. "Q" implies the output lags the reference clock by 90° of phase.
4. "–t" implies the output leads the reference clock by a minimum phase delay.
5. "–Q" implies the output leads the reference clock by 90° of phase.
6. "2( )" implies the output is at twice the frequency of the reference clock.
7. "/2" implies the output is at half the frequency of the reference clock.
8. The PECLN/P Differential PECL output is not affected by the PHSEL inputs.

Legend



ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (GND = 0)	7.0 V
TTL Input Voltage (GND = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS (TTL I/O)

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage (TTL)	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW Voltage (TTL)	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18mA			-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -12mA[3]	2.4			V
			I_{OH} = -24mA[3]	2.0			V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 24mA[3]			0.5	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.7V				10	µA
I_I	Input HIGH Current at Max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V	INPSEL			-300	µA
			Others			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max				95	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	C_{LOAD} = 25pF at 50 MHz				200	mA

DC CHARACTERISTICS (PECL I/O)

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage (PECL)	Guaranteed input HIGH voltage for all inputs		V_{CC} –1145		V_{CC} –600	V
V_{IL}[2]	Input LOW Voltage (PECL)	Guaranteed input LOW voltage for all inputs		V_{CC} –2000		V_{CC} –1450	V
V_{OH}	Output HIGH voltage	V_{CC} = 5.0 V	Load = 50Ω to V_{CC} –2V	V_{CC} –1075		V_{CC} –650	V
V_{OL}	Output LOW voltage			V_{CC} –1980		V_{CC} –1585	V

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration one second.

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Table 4. AC Specifications

Symbol	Description	S4405B-66		S4405B-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		5.0		ns
t_{PE}	Phase Error between TTLREF and FBCLK	-1	0	-1	0	ns
t_{PEP}	Phase Error between PECLREF and FBCLK	-3	-1	-3	-1	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	0	750	ps
t_{SKEW}	Output Skew[2] (TTL)	0	400	0	400	ps
t_{DC}	Output Duty Cycle	45	55	45	55	%
f_{PECL}	PECLP/N Frequency	80	132	80	160	MHz
f_{FOUT}	FOUT Frequency[3] (TTL)	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency[3]	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency[3]	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{OFD}	Tpd OUTEN0–2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0–2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time[4]	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[5]		5		5	ms

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. C_{LOAD} = 35 pF.
4. With 35 pF output loading (0.8 V to 2.0 V transition).
5. Depends on loop filter chosen. (Number given is for example filter.)

Figure 5. Timing Waveforms

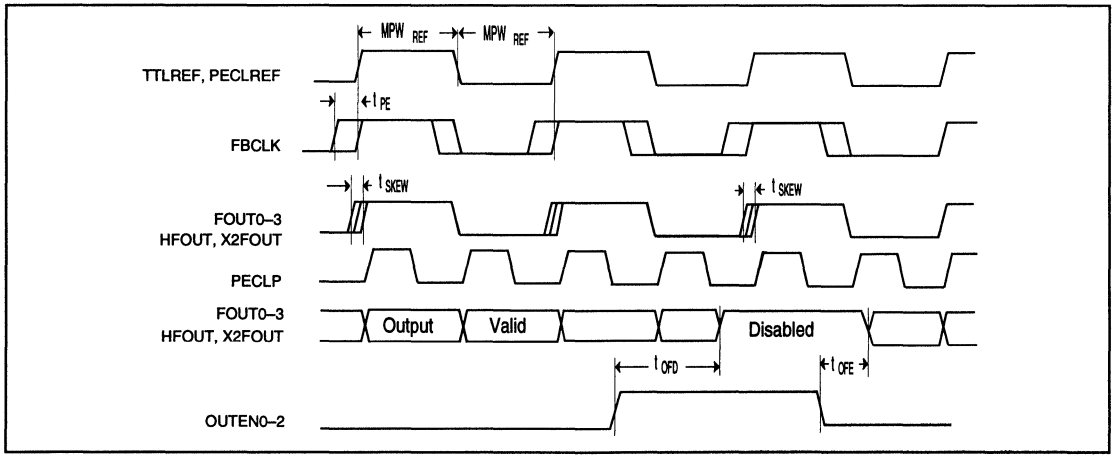
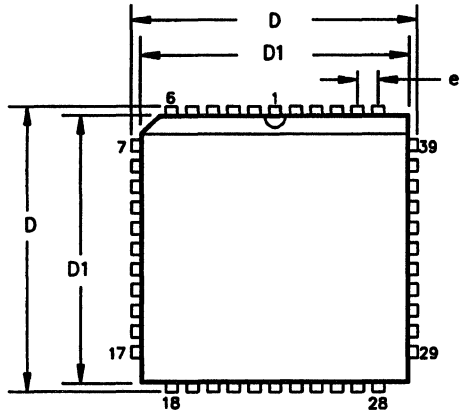
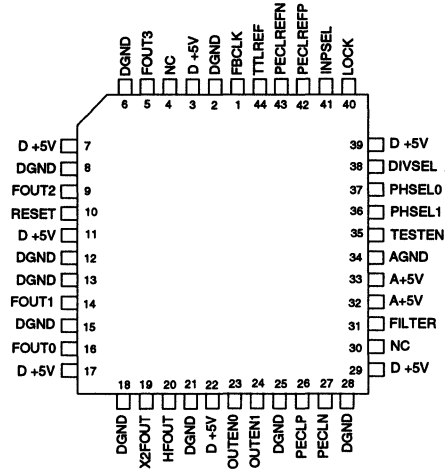
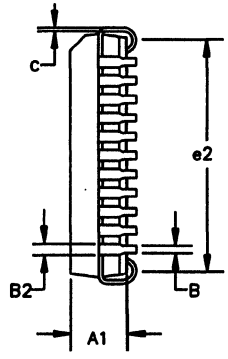


Figure 6. S4405 44 PLCC Package and Pinout







SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.687	.697
D1	.644	.659
e	.048	.052
e2	.610	.630

All dimensions nominal in inches.

Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE	MAX FREQ
S–commercial	4405	B–44 PLCC	-66 (66 MHz) -80 (80 MHz)

X	XXXX	X	XX
Grade	Part number	Package	Speed

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BiCMOS PLL CLOCK GENERATOR S4406

FEATURES

- Generates outputs from 10 MHz to 66 MHz
- Four groups of three outputs (12 outputs total)
- Eight user-selectable output functions for each group
- TTL compatible outputs, with <1.5-ns edge rates
- Performs clock doubling, dividing, invert, lead/lag placement
- Internal VCO running between 160 to 266 MHz
- 1.0µ BiCMOS technology
- Output skew less than 500 ps
- 52 PQFP package

APPLICATIONS

- High-performance microprocessor systems
- CMOS ASIC systems
- Backplane clock deskew and distribution
- Compatible with Intel's Pentium™ processor

GENERAL DESCRIPTION

The S4406 BiCMOS clock generator provides 12 TTL outputs with less than 500 ps of skew. Implemented in AMCC's 1.0µ BiCMOS technology, the internal PLL and divider/delay selector logic allow the user to individually tailor the (4) TTL output groups to the system's needs. The internal VCO can operate between 160 to 266 MHz, and the programmability allows the user to generate output clocks in the 10–66 MHz range.

The S4406 offers the user the ability to select the appropriate phase and frequency relationship for each of the four groups of three TTL clock outputs.

In addition to clock doubling and inversion functions, the S4406 allows any output groups to lead or lag the others by the minimum phase delay of 3.75–6.25 ns.

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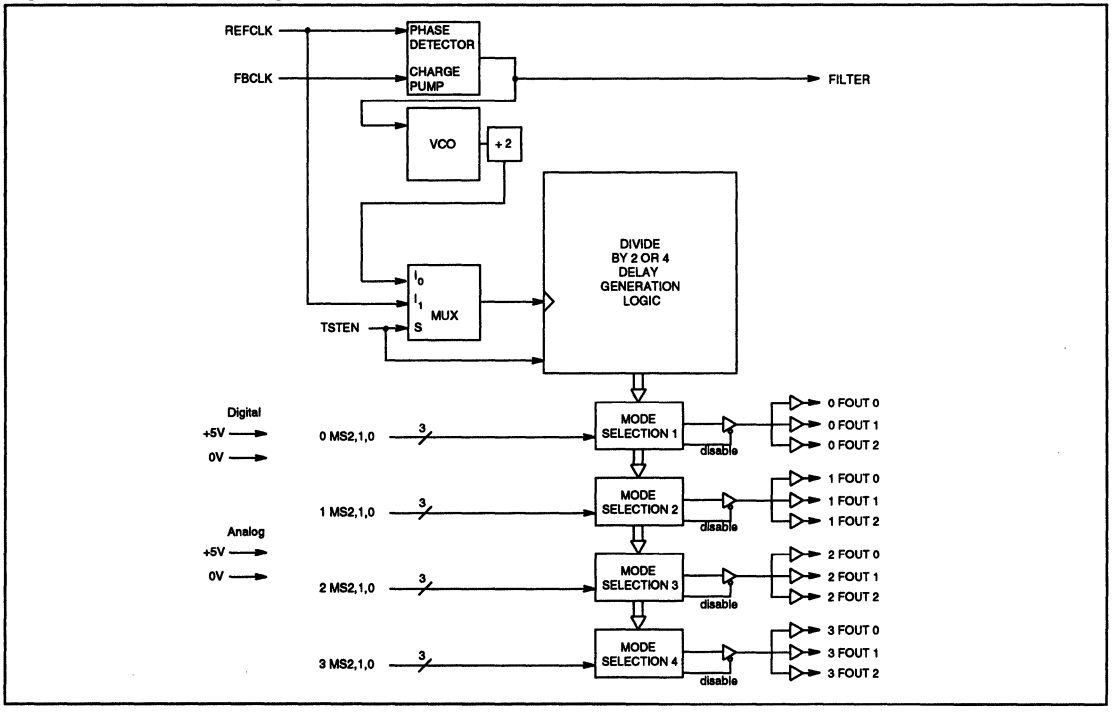
Figure 1. S4406 Block Diagram



FUNCTIONAL DESCRIPTION

The 12 xFOUT0–2 outputs are the main TTL output clocks that the generator supplies. The mode selection choices are shown in Table 1 and waveform definitions are given in Figure 2. The "x" represents the output group number (1–4). The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input (xFOUT0–2 can be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK).

Example:

In order to meet bus timing specifications for a typical system, designers may need three outputs at 66 MHz for the system clock and processor, a 33-MHz output for the cache controller, and a 33-MHz delayed output for a memory management unit. This system requirement can be met using the S4406 by setting the mode select pins for the first group of outputs (0MS2,1,0) to 111, the second group (1MS2,1,0) to 110, and the third group (2MS2,1,0) to 101. In this configuration, one of the 33-MHz outputs should be fed back to the FBCLK input. This example makes use of only three of the four output banks, leaving the fourth available for any other clock signals needed.

Table 1. Mode Selection Options

xMS2,1,0	MODE DESCRIPTION	xFOUT0,1,2
000	Disabled.	Logical Hi
001	All three outputs at the fundamental output frequency, but early by a minimum phase delay.	f – t
010	All three outputs at half the fundamental output frequency and inverted.	I /2
011	All three outputs at the fundamental output frequency and inverted.	I
100	All three outputs at half the fundamental output frequency, but delayed by a minimum phase delay.	f/2 + t
101	All three outputs at the fundamental output frequency, but delayed by a minimum phase delay.	f + t
110	All three outputs at half the fundamental output frequency.	f/2
111	All three outputs at the fundamental output frequency.	f

Note: If f is fed back, the fundamental frequency is equal to REFCLK.
If f/2 is fed back, the fundamental frequency is twice REFCLK.

Filter

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single capacitor and resistor) can be included in the phase locked loop of the clock generator. See Figure 3.

Phase Delay

The minimum phase delay between xFOUT0–2 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the fundamental output frequency by four, or half the fundamental frequency by eight. The minimum phase delay is equal to the period of the VCO frequency: t = 1/(VCO freq). Since the VCO can operate in the 160-MHz to 266-MHz range, the range of minimum phase delay values is 6.25 ns to 3.75 ns (See Table 2).

Figure 2. Waveform Definitions

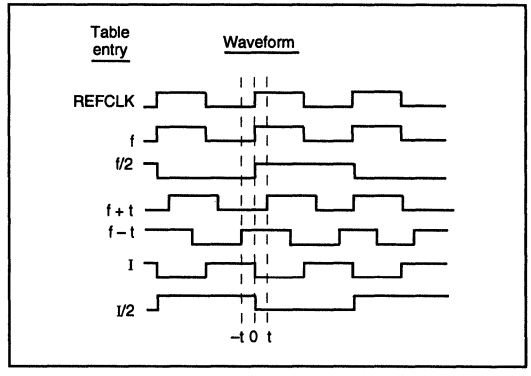
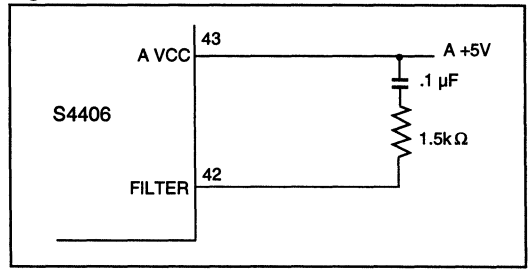


Figure 3. External PLL Filter



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Test Capabilities

TESTEN allows the chip to use the REFCLK input instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. In addition, when TESTEN is brought High, an internal RESET pulse is generated. This initializes the internal counter flip-flops to zeros, and at the end of the next clock cycle, the outputs go to a zero state. TESTEN can also be used for board testing to allow the user to control the output clocks from the S4406 by inputting the board clock to the REFCLK input.

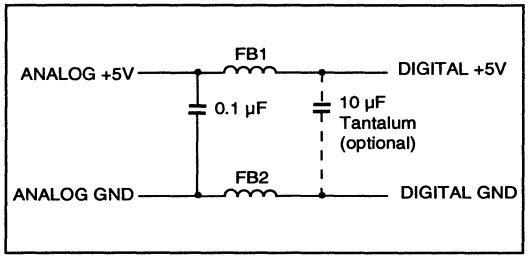
Table 2. VCO Operating Frequencies

xFOUT0–3	VCO FREQ	MIN PHASE DELAY
66.6 MHz	266 MHz	3.750 ns
50 MHz	200 MHz	5.000 ns
40 MHz	160 MHz	6.250 ns
33.3 MHz	266 MHz	3.750 ns
25 MHz	200 MHz	5.000 ns
20 MHz	160 MHz	6.250 ns

Power Supply Considerations

Power for the analog portion of the S4406 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 4). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Figure 4. External Power Supply Filter

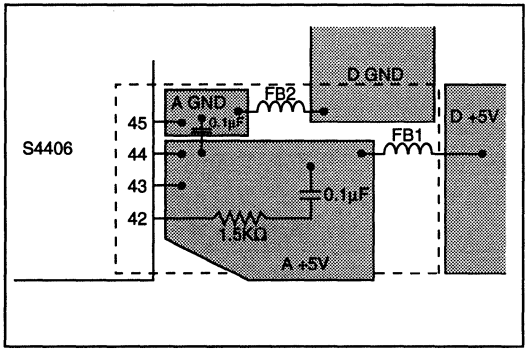


Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4406 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4406 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 6) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 5. Board Layout



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PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Also, when brought High, generates an internal Reset pulse that initializes the internal counter flip-flops to zero.

xMS2,1,0. Mode selection inputs that allow selection of the phase and frequency relationship of each of the four banks of three clock outputs. The "x" represents the output group number (0–3). Refer to Table 1 for mode selection options.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

xFOUT0–2. Clock signal outputs. Refer to Table 1 and Figure 4 for a description of output options.

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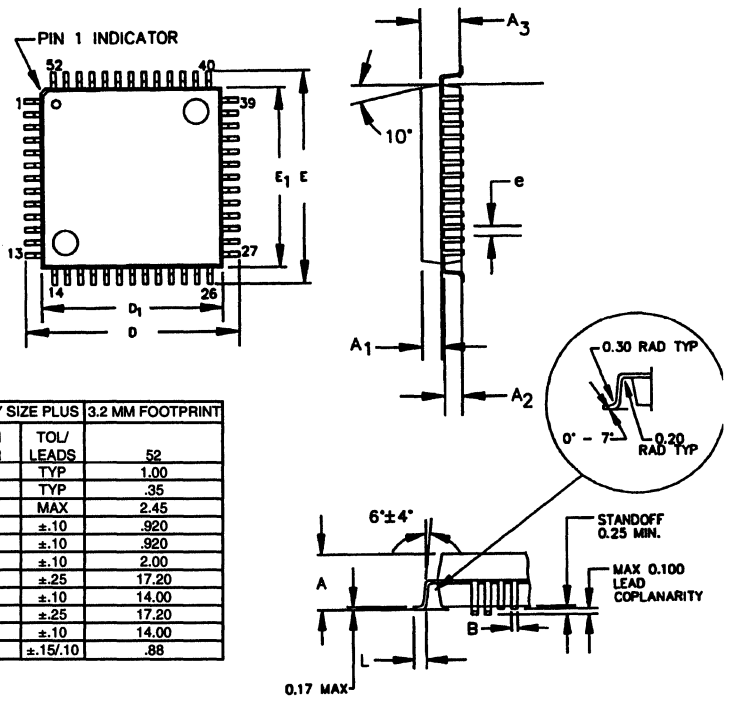
Figure 6. 52–pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

All dimensions in mm.

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18 mA			-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -12 mA[3]	2.4			V
			I_{OH} = -24 mA[3]	2.0			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 24 mA[3]				0.5	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.4V	4MS2,3MS2,1,0			-200	µA
			Other			50	µA
I_I	Input HIGH Current at Max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V	4MS2,3MS2,1,0			-500	µA
			Other			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max				70	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	C_{LOAD} = 25 pF at 50 MHz				200	mA

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher.
4. Maximum test duration one second.

ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

Table 3. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	160	266	MHz
f_{REF}	REFCLK Frequency	10	66	MHz
t_{IRF}	Input Rise/Fall Time	1	3	ns
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	ps
t_{SKEW}	Output Skew[2] across all outputs	0	500	ps
t_{SKEWA}	Output Skew[2] within any bank	0	250	ps
t_{DC}	Output Duty Cycle[3]	45	55	%
f_{FOUT}	FOUT Frequency[4]	10	66	MHz
t_{PS}	Nominal Phase Shift Increment[5]	3.75	6.25	ns
t_j	Clock Stability[6]		500	ps
t_{ORF}	FOUT Rise/Fall Time[7]	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[8]		5	ms
t_{PSV}	Phase Shift Variation[5]	-250	+250	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35 pF, measured at 1.5 V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to 0FOUT0 at 1.5 V.
6. Clock period jitter with all FOUT outputs operating at 66MHz loaded with 25 pF using loop filter shown. Parameter guaranteed, but not tested.
7. With 35 pF output loading (0.8 V to 2.0 V transition).
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 7. Timing Waveforms

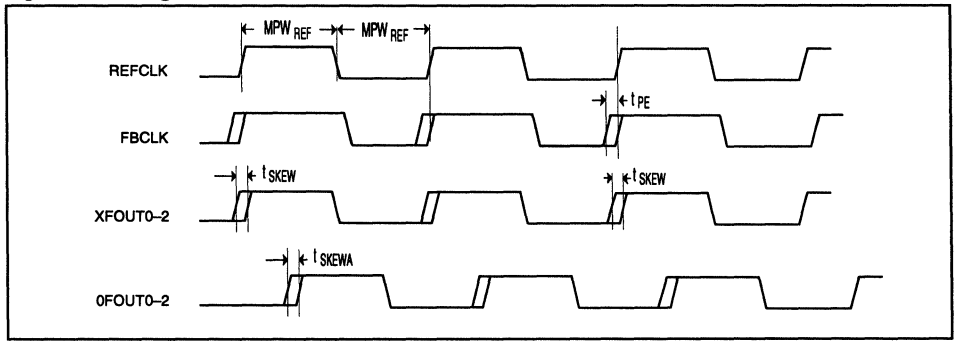


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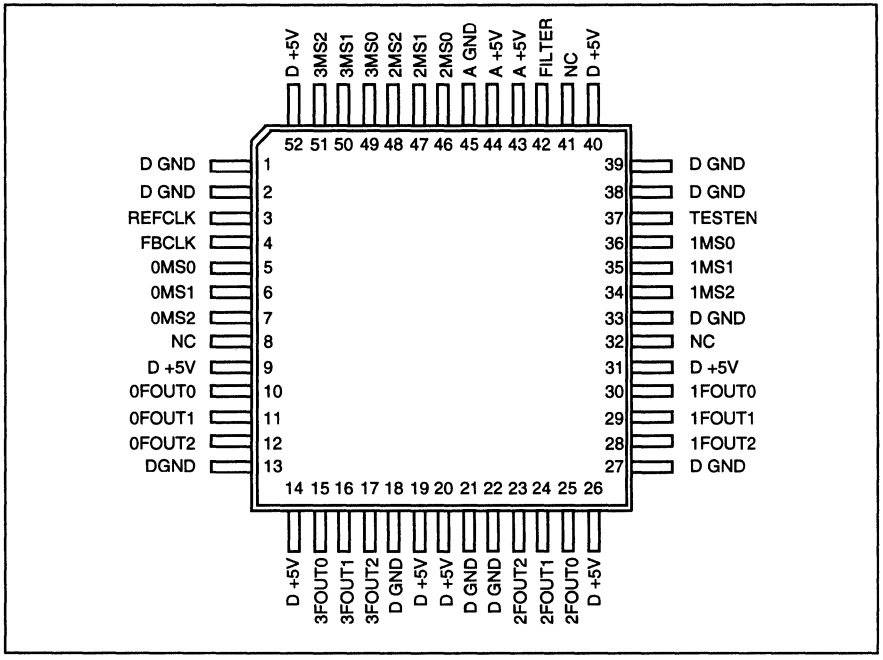
Figure 8. S4406 Pinout



Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE	MAX FREQ
S–Commercial	4406	Q–52 PQFP	-66

X	XXXX	X	XX
Grade	Part number	Package	Speed

5

NOTES

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14-OUTPUT BiCMOS PLL CLOCK GENERATOR S4407

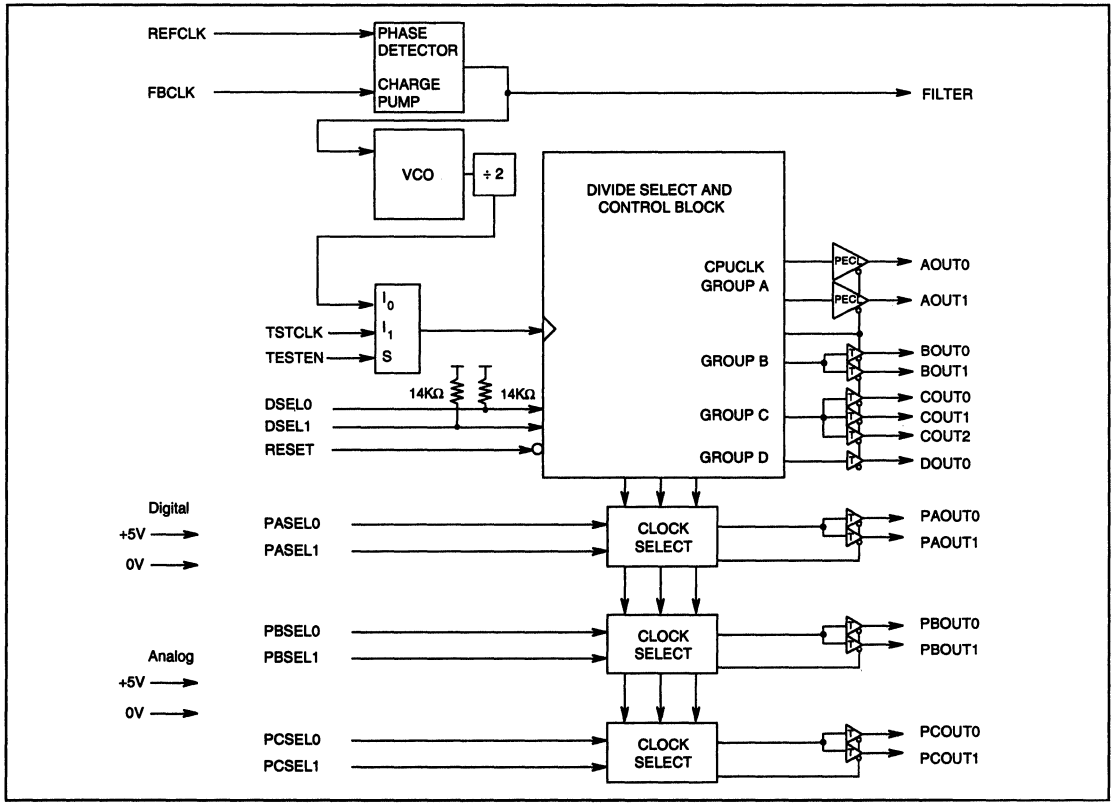
FEATURES

- Compatible with the Hewlett Packard PA-RISC microprocessor
- Dual +5V-referenced ECL (PECL) output clocks at 50 MHz, 75 MHz, or 100 MHz
- 12 programmable TTL system clocks at up to 50 MHz
- Three (3) user-selectable output frequencies for 3 pairs of the TTL outputs
- Internal VCO running between 200 to 320 MHz
- 1.0µ BiCMOS technology
- TTL output skew ≤ 500 ps
- Single +5V supply
- 52 PQFP package

GENERAL DESCRIPTION

The S4407 BiCMOS clock generator provides two +5V-referenced 50-Ω ECL outputs to drive the primary PA-RISC clock inputs, and 12 TTL clock outputs with less than 500 ps of skew for use as system clocks. Implemented in AMCC's 1.0µ BiCMOS technology, the internal VCO, phase detector, and programmable frequency selection allow users to tailor the TTL output clocks to meet system requirements. The internal VCO can operate between 200 to 320 MHz, and the programmable divide-ratios allow the user to generate TTL output clocks in the 12.5–50 MHz range.

Figure 1. S4407 Block Diagram



PA-RISC is a trademark of the Hewlett Packard Company

FUNCTIONAL DESCRIPTION

The S4407 clock generator allows the user to choose the divide ratio between the VCO frequency and the frequency of the outputs by using the DSEL1,0 pins. The selectable divide ratios are shown in Table 1.

The S4407 also gives the user the ability to select the appropriate frequency for each of the three groups of TTL clock outputs. The frequency selection choices are contained in Table 2. Figures 2–4 show the clock division and alignment timing. Mode 0 timing is shown in Figure 2, Mode 1 timing is shown in Figure 3, and Mode 2 timing is shown in Figure 4.

Any of the TTL clock outputs can be used to drive the FBCLK input, and thereby close the loop. The divide ratio selected for this output can be used with the REFCLK input frequency to determine the VCO operating frequency. For example, if COUT2 is used as the FBCLK input, and the divide select is DSEL1,0 = 01, then for a REFCLK input frequency of 25 MHz, the VCO will be operating at 25 MHz x 12=300 MHz.

Test Capabilities

Three pins are included for test purposes. TESTEN allows the chip to use the TSTCLK input instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. For example, when TESTEN = 1 and DSEL1,0 = 11, each of the PECL and TTL outputs will be a divide-by-two version of the TSTCLK input.

For board test purposes, the user should configure the part to operate in one of the test modes, and apply a RESET pulse before supplying clocks to the TSTCLK input. After 14 or 22 rising TSTCLK inputs, all the output will go low and then begin operating with the expected pattern (defined by the DSEL inputs). In TEST Modes 0 and 2, the outputs will go low after 22 clocks, and in TEST modes 1 and 3, the outputs will go low after 14 clock cycles.

Filter

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single capacitor and resistor) can be included in the phase-locked loop (PLL) of the clock generator. See Figure 5.

Figure 2. Mode 0 Timing

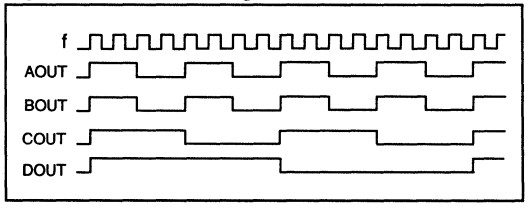


Figure 3. Mode 1 Timing

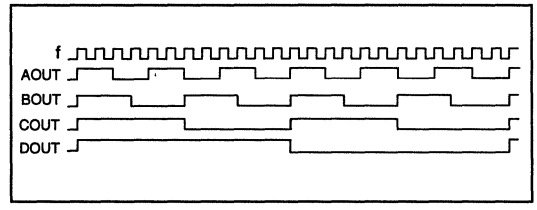


Figure 4. Mode 2 Timing

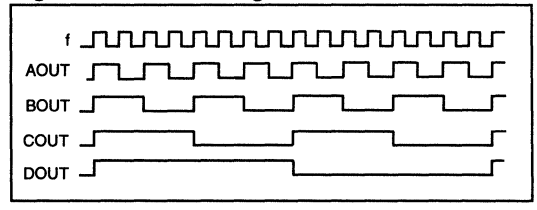


Table 1. Selectable Divide Ratios

DSEL1	DSEL0	RESET	TESTEN	f[1]	AOUT	BOUT	COUT	DOUT	DESCRIPTION
0	0	1	0	200 MHz	f/4	f/4	f/8	f/16	Mode 0 (1/1)[2]
0	1	1	0	300 MHz	f/4	f/6	f/12	f/24	Mode 1 (2/3)[2]
1	0	1	0	200 MHz	f/2	f/4	f/8	f/16	Mode 2 (1/2)[2]
1	1	1	0	X	1	1	1	1	Mode 3
X	X	0	X	X	0	0	0	0	Reset Mode[3]
0	0	1	1	TSTCLK	f/2	f/2	f/4	f/8	TEST Mode 0
0	1	1	1	TSTCLK	f/2	f/3	f/6	f/12	TEST Mode 1
1	0	1	1	TSTCLK	f/1	f/2	f/4	f/8	TEST Mode 2
1	1	1	1	TSTCLK	f/2	f/2	f/2	f/2	TEST Mode 3

1. f is the VCO frequency with COUT as the feedback clock and operating at 25MHz.
2. Processor bus (BOUT) to internal processor (AOUT) clock ratio.
3. Reset Mode initializes all the state machines, to aid in test.

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Power Supply Considerations

Power for the analog portion of the S4407 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 6). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

SINGLE-ENDED TO DIFFERENTIAL CLOCK TRANSLATION

A tight input clock skew budget is a primary design constraint. The single-ended to differential clock translation circuit shown in Figure 7 allows the lowest possible clock skew to the PA-RISC module. In this design, S4407 outputs AOUT0 and AOUT1 are tied together at the output pins. The circuit translates this single-ended signal into four differential inputs that go directly into the PA-RISC with short interconnects. The input clock skew at the PA-RISC inputs is minimized and is due solely to the interconnect lengths and impedance mismatches.

BOARD LAYOUT CONSIDERATIONS

- The S4407 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4407 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 6) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

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Table 2. Frequency Selection Choices

PxSEL1[1]	PxSEL0[1]	Function of CLOCK SELECT Blocks
0	0	Both outputs at the same frequency as Group B
0	1	Both outputs at the same frequency as Group C
1	0	Both outputs at the same frequency as Group D
1	1	Both outputs disabled in the high state[2]

1. "x" = A, B, or C.
2. Outputs disabled when TESTEN = 0. When TESTEN = 1, the programmable outputs will be at half the TSTCLK input frequency.

Figure 5. External PLL Filter

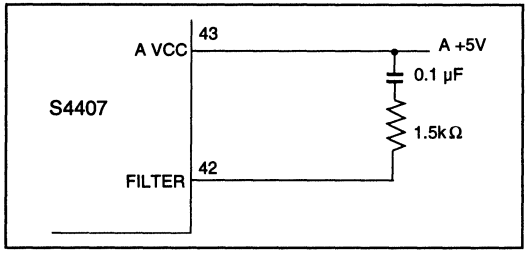
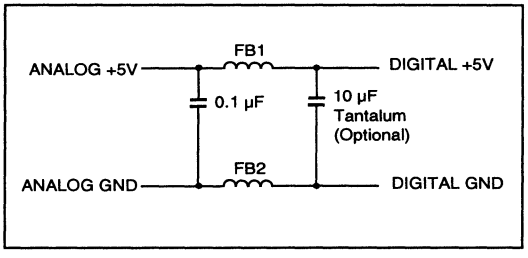


Figure 6. External Power Supply Filter



PIN DESCRIPTIONS

Input Signals

REFCLK. Reference clock supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input. (See Table 1.)

RESET. Active Low. Asynchronously initializes internal counter flip-flops to zero for test purposes. At the end of the next clock cycle, the outputs go to a zero state.

TESTEN. Active High. Test enable input allows the S4407 to use the TSTCLK input instead of the VCO output to clock the chip. Used during chip test to allow the counters and control logic to be tested independently of the VCO. For example, when TESTEN and DSEL1,0 are all high, each of the PECL and TTL outputs are a divide-by-two version of the TSTCLK input.

TSTCLK. Test clock input used by the S4407 to clock the chip when selected by TESTEN. See TESTEN.

DSEL0. This input, along with DSEL1, allows selection of the divide ratio between the VCO frequency and the frequency of the outputs. Refer to Table 1 for the selectable divide ratios. This input incorporates a 14K ohm pull-up resistor and can be left unconnected if the input is intended to be in the high state.

DSEL1. Along with DSEL0, allows selection of the divide ratio between the VCO frequency and the frequency of the outputs. Refer to Table 1 for the selectable divide ratios. This input incorporates a 14K ohm pull-up resistor and can be left unconnected if the input is intended to be in the high state.

PxSEL0. Input that, along with PxSEL1, allows selection of the frequency for each of the three groups of prgrammable TTL outputs. The "x" refers to either Group A, B, or C. Refer to Table 2 for frequency selection options.

PxSEL1. This input, along with PxSEL0, allows selection of the frequency for each of the three groups of programmable TTL outputs. The "x" refers to either Group A, B, or C pairs of programmable outputs. Refer to Table 2 for frequency selection options.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and capacitor) to be included in the PLL.

AOUT0. Single-ended +5V-referenced ECL output clock. See Table 1.

AOUT1. Single-ended +5V-referenced ECL output clock. See Table 1.

BOUT0–1. TTL clock outputs. See Table 1.

COUT0–2. TTL clock outputs. See Table 1.

DOUT0. TTL clock output. See Table 1.

PAOUT0–1. Programmable TTL clock outputs. Refer to Table 2 for output frequency options.

PBOUT0–1. Programmable TTL clock outputs. Refer to Table 2 for output frequency options.

PCOUT0–1. Programmable TTL clock outputs. Refer to Table 2 for output frequency options.

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Figure 7. Single-ended to Differential Clock Translation Circuit

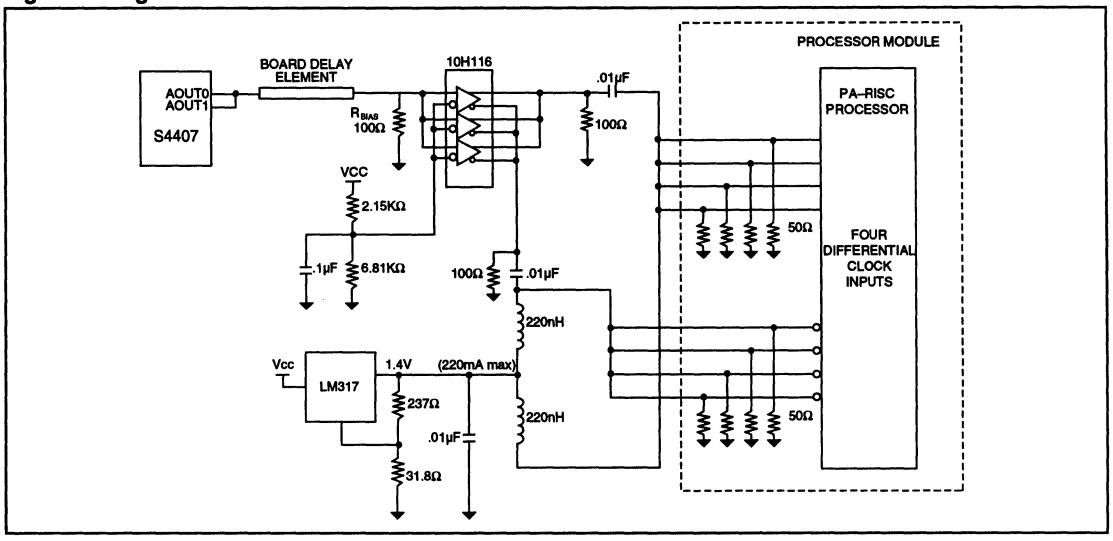
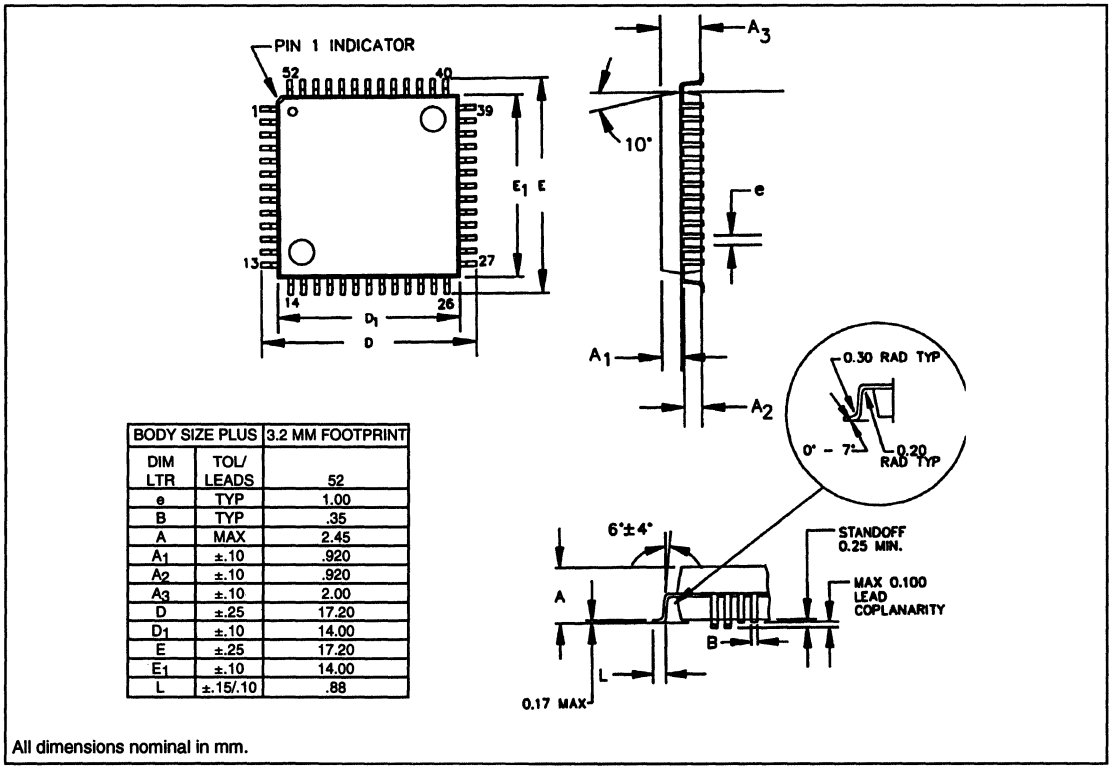


Figure 8. 52–pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

All dimensions nominal in mm.

5

ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS (TTL I/O)

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = –18mA			–0.8	–1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} = –12 mA[3]	2.4			V
			I_{OH} = –24 mA[3]	2.0			V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 24 mA[3]				0.5	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.4V	DSEL0, 1			–200	µA
			Other			50	µA
I_I	Input HIGH Current at Max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V	DSEL0, 1			–500	µA
			Other			–50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		–25		–100	mA
I_{CC}	Static	V_{CC} = Max				100	mA
I_{CCT}	Total Icc (Dynamic and Static)	C_{LOAD} = 25pF at 50MHz				250	mA

DC CHARACTERISTICS (ECL I/O)

Symbol	Parameter	DC Test Conditions	Min	Typ[1]	Max	Units
V_{OH}	Output HIGH voltage	V_{CC} = 5.0V Load 50Ω to V_{CC} – 2V	V_{CC} – 1000		V_{CC} –650	mV
V_{OL}	Output LOW voltage	V_{CC} = 5.0V Load 50Ω to V_{CC} – 2V	V_{CC} – 1960		V_{CC} –1585	mV

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher.
4. Maximum test duration one second.

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Table 3. AC Specifications

Symbol	Description	Min	Typ	Max	Units
f_{VCO}	VCO Frequency	200		320	MHz
f_{REF}	REFCLK Frequency	12.5		50	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	5.0			ns
MPW_{RESET}	RESET Minimum Low Pulse Width	20			ns
t_{IRF}	Input Rise/Fall Time	1		3	ns
t_{PE}	Phase Error Difference[1]	–1000		0	ps
t_{PED}	Phase Error Difference from Part to Part[2]	0		750	ps
t_{SKEWB}	BOUT Skew to other Group B signals		100	250	ps
t_{SKEWC}	COUT Skew to other Group C signals		100	250	ps
t_{SKEWP}	PxOUT Skew to xOUT (x=A,B,C)			500	ps
t_{SKEWT}	Output Skew (across all TTL outputs)			500	ps
t_{DCE}	PECL Output Duty Cycle[3]		50		%
t_{DCT}	TTL Output Duty Cycle[4]	45		55	%
f_{ECL}	AOUT Frequency	50		100	MHz
f_{TTL}	TTL Output Frequency	12.5		50	MHz
t_{AD}	AOUT to DOUT Delay		1.70		ns
t_{ADV}	AOUT to DOUT Delay Variation[5]	0		1	ns
t_{AB}	AOUT to BOUT Delay		1.70		ns
t_{ABV}	AOUT to BOUT Delay Variation[5]	0		1	ns
t_{ER}	ECL Output Rising Edge Delay[6]		1.25		ns
t_{EF}	ECL Output Falling Edge Delay[6]		1.25		ns
t_{TR}	TTL Output Rising Edge Delay[7]	0.5		1.5	ns
t_{TF}	TTL Output Falling Edge Delay[7]	0.5		1.5	ns
t_{LOCK}	Loop Acquisition Time[8]			5	ms

1. A negative T_{PE} indicates the FBCLK leads REFCLK
2. Difference in phase error between two parts at the same voltage, temperature, and frequency.
3. Measured at mid swing with a 35pF load.
4. Measured at 1.5V with a 35pF load.
5. Variation of delay on a given device over voltage and temperature.
6. Measured between 20% and 80% of output swing with 35pF load.
7. Measured between 0.8V and 2.0V with 35pF load.
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 9. Timing Waveforms

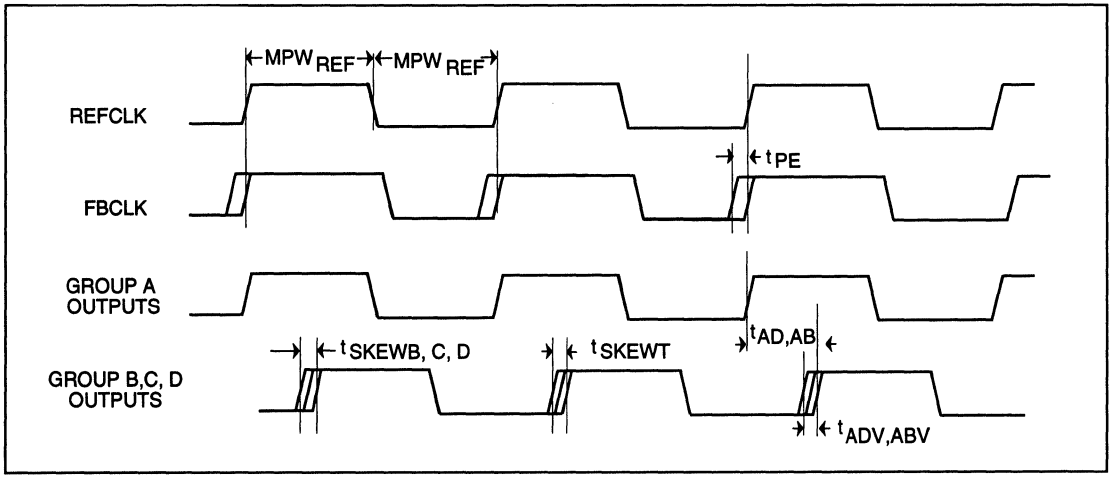
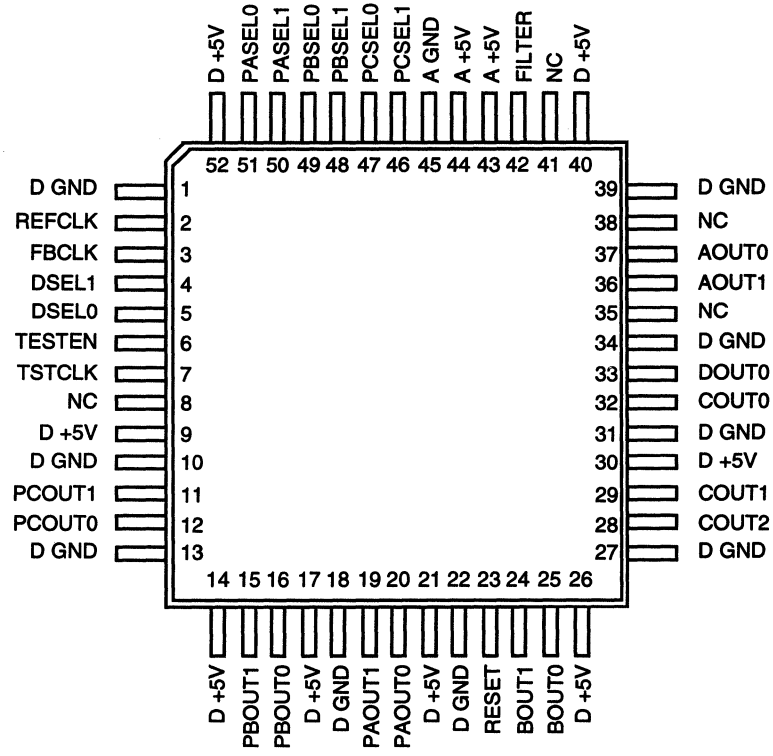


Figure 10. S4407 Pinout.



NC - No Connect. Do not connect to VCC or GND.

Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE
S—commercial	4407	Q—52 PQFP

X — Grade
XXXX — Part number
X — Package

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BiCMOS PLL CLOCK MULTIPLIER S4501

FEATURES

- Performs X2, X4 and X8 Multiplication on Input Clock Frequency
- Eliminates the need for High Speed Crystals
- Simplifies Clock Routing by Reducing High Speed Clock Traces
- Generates 3 TTL Outputs of up to 80 MHz MAX
- Output Skew ± 200 ps MAX
- 160-320 MHz PLL Requires no External Components
- Space Saving 8 pin SIP or SOIC
- Reduces System EMI Generation
- Less than 0.3 W at 80 MHz
- Proven 1-Micron BiCMOS Technology

APPLICATIONS

- "Deskewing" ASIC Devices
- RISC and High Performance Microprocessor Systems
- Clocking synchronous DRAMS and Memory Modules

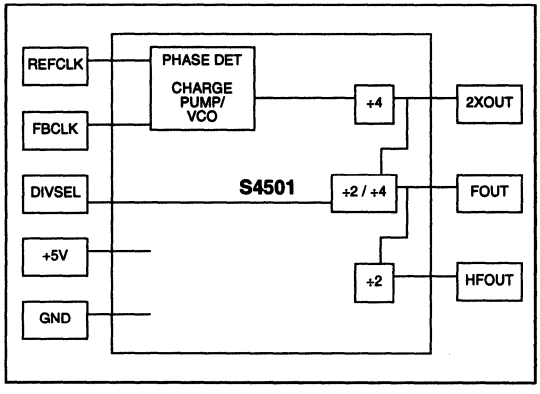


Figure 1. S4501 Block Diagram

GENERAL

The S4501 has two clock inputs, REFCLK and FBCLK and three outputs 2XOUT, FOUT and HFOUT providing signals at 2X, 1X and half the FOUT frequency respectively. The frequency of FOUT depends on DIVSEL, and the choice of outputs (frequencies) fed back to the REFCLK frequency FBCLK input. See Figure 1.

The S4501 Clock Multiplier allows a 1/2, 1/4 or 1/8 speed clock to be routed to the device which in turn produces 2X, 4X or 8X multiples to meet high speed clock requirements.

The S4501 can also be used as a "zero-delay" buffer to provide multiple frequency outputs in sync with the reference clock.

In applications requiring ASIC "deskewing", using an output of the ASIC as FBCLK to the S4501 allows that output (and others related to it) to be synchronized to the REFCLK to within ± 750 ps. The S4501's PLL will then actively align the clock of the ASIC to compensate for its nominal propagation delay as well as any variation due to process or operating conditions.

5

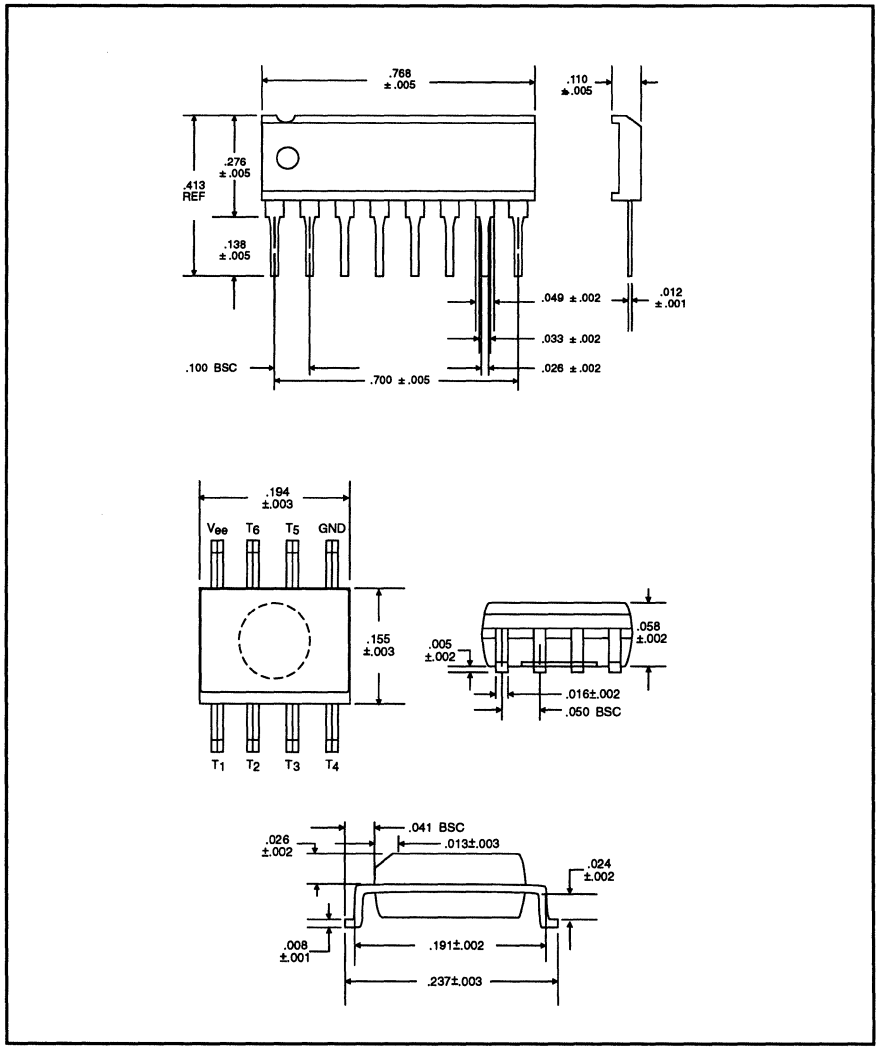
Table 1. AC Performance Summary

Description	Min	Max	Units
Input Frequency	10	80	MHz
Phase Error	—	± 750	ps
Output Skew		± 200	ps
2XOUT Freq.	40	80	MHz

Table 2. DC Performance Summary

Description	Min	Max	Units
Output Current	- 24	+ 24	mA
Voh @ - 16 mA	2.4		V
Vol @ + 24 mA		0.5	V
I_{CC}		55	mA

8 Pin Single In-Line Package



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CLOCK SYNTHESIZER S4503

FEATURES

- Multiplies input reference frequency by integers 2-32
- Digitally programmable output clock frequencies from 10 MHz to 300 MHz
- Two (2) groups of independent clock outputs
  - One group consists of differential PECL outputs
  - One group is a pair of TTL outputs
- Proprietary TTL output drivers with:
  - Complementary 24 mA peak outputs, source and sink
  - Source series termination
  - Edge rates less than 1.5 ns
- Low 250 ps reference clock jitter (PECL outputs)
- 900 mW or less power dissipation, frequency and load dependent
- 150 MHz to 300 MHz phase lock loop VCO frequency range
- Advanced BiCMOS process technology
- Space saving 28 PLCC package

GENERAL DESCRIPTION

The S4503 is a clock synthesizer which utilizes phase-locked loop technology to provide two (2) independently selectable output frequencies in the 10 MHz to 300 MHz range. A reference input may be provided by either a low cost crystal or a TTL frequency source.

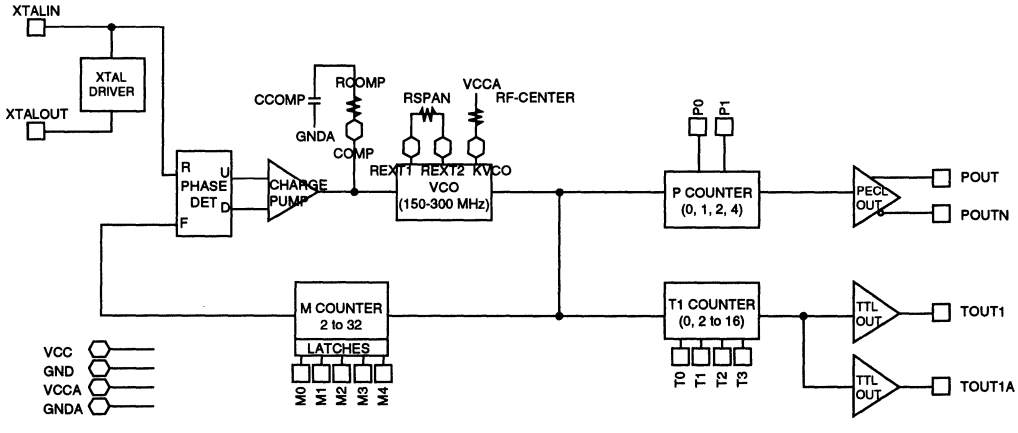
The first of the two (2) output frequency groups consists of a pair of differential PECL (Positive referenced ECL) outputs which will operate up to 300 MHz. The second group (TTL) consist of two outputs with selectable frequency, up to 80 MHz.

The final frequency for each group is digitally selected via three programmable counters. One counter is used to set the internal VCO frequency between 150 MHz to 300 MHz, and the others are used to divide the VCO frequency from 2 thru 16 (TTL) and 1, 2 or 4 (PECL).

All phase lock loop elements are provided on chip with the exception of the passive components needed for the loop filter function and adjustment to the crystal input VCO.

5

Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55°C to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +130°C
Latch-up Current ..... >200 mA
Operating ambient temperature ..... 0°C to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF
PECL Output Pins ..... 5.0 pF

AC Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C

Symbol	Description	Conditions	MIN	MAX	Units
F_{VCO}	VCO Frequency		150	300	MHz
F_{XTL}	XTL Frequency, Fundamental	XTLIN to XTLOUT	5	25	MHz
F_{TTL}	TTL Input Frequency	Standard TTL Levels	5	80	MHz
Pout	PECL Out Frequency		37	300	MHz
T_{OUTn}	TTL Out Frequency		9	80	MHz
$T_{SKEW\ T\text{-}T}$	TTL to TTL Output Skew	TTL Leading Edges at +1.5V		250	ps
$T_{SYM\text{-}T}$	T_{OUT} Symmetry	Measured at 1.5V		± 1.5	ns
$T_{SYM\text{-}P}$	PECL Out Symmetry	Measured at differential crossing points		± 250	ps
T_J	PECL Clock Jitter, pk to pk			250	ps

Notes:
1. Jitter is measured relative to the reference clock input at the XTALIN input.
2. Output symmetry is the deviation from a 50% duty cycle.

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Electrical Characteristics

V_{CC} = +5.0V ±5%, T_a = 0°C to + 70°C

Symbol	Parameter	Conditions	Min	Max	Units
$V_{OH(PECL)}$	Output HIGH Voltage, ECL	50 Ohms to Vcc-2V	V_{OL}+0.6V	Vcc-0.96	V
$V_{OL(PECL)}$	Output LOW Voltage, ECL	50 Ohms to Vcc-2V	Vcc-1.6	V_{OH}-0.6	V
$V_{OH\ (TTL)}$	Output HIGH Voltage	F_{OUT} = 80MHz max, C_L = 10pF	2.4		V
$V_{OL\ (TTL)}$	Output LOW Voltage, TTL	F_{OUT} = 80MHz max, C_L = 10pF		0.6	V
$V_{IH\ (TTL)}$	Input (TTL) HIGH Voltage	All TTL Inputs	2.0	Vcc	V
$V_{IL\ (TTL)}$	Input (TTL) LOW Voltage	All TTL Inputs	-0.5	0.8	V
$I_{OH(PECL)}$	Output HIGH Current	50 Ohms to Vcc-2.0		25	mA
$I_{OL(PECL)}$	Output LOW Current	50 Ohms to Vcc-2.0		8	mA
$I_{IH\ (TTL)}$	Input HIGH Current	Vin=Vcc		200	uA
$I_{IL\ (TTL)}$	Input LOW Current	Vin ≤ 0.8		50	uA
I_{OHS}[1]	Output HIGH Short Current	Output High, V_{OUT} = 0 V, Typical	-55		mA
I_{OLS}[1]	Output LOW Peak Current	Output Low, V_{OUT} = Vcc, Typical	55		mA
I_{cc}	Supply Current	TTL Outputs to 20 pF @ 50 MHz		170	mA
POWER	Power Dissipation	TTL Outputs to 20 pF @ 50 MHz		900	mW

1. Maximum test duration one second.

The S4503 TTL outputs feature source series termination of approximately 40 Ohms to assist in matching 50-75 ohm P.C. boards environments.

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DC Characteristics

The S4503 has been designed specifically for clock distribution. In the development of this product, AMCC has made several modifications to the historic "high drive, totem pole outputs" producing AMCC's dynamically adjusting source series terminated outputs. As a result of this, the S4503 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH}= -8mA	2.4V	
V_{OL}	I_{OL}= 4mA		0.6V

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

The S4503 synthesizer employs a phase locked loop (PLL) which includes a divide down "multiplying" counter to produce a high frequency internal reference oscillator from a low cost, low frequency crystal. This high frequency internal reference is the output of a voltage controlled oscillator or VCO. This single VCO frequency is sub divided down to selectable TTL output frequencies. One positive (+5V) referenced complementary ECL (PECL) output (Pout) pair is also provided.

The M counter is a frequency "multiplying" feedback counter that divides down the VCO frequency, before applying it to the phase detector. Thus the VCO frequency is the product of the input reference (crystal) frequency and the M counter modulus. This divide down counter modulus is externally selected to any integer value from 2 to 32 by a five bit binary coded value, plus 1, entered into input latches via the preset input pins M0 through M4. The M0 to M4 inputs have the binary weight of $M0=2^0$ through $M4=2^4$. The M0-4 inputs are low or 0 if not connected. NOTE: an entry of all binary zeros will not count down and is, therefore, invalid. Designs that will load the M counter inputs from an external register that powers-up with the outputs in a hi-Z state will need to use external resistors to ensure the S4503 M counter inputs are never all zeros.

The output frequency divide down counters "P & T" each have individual select input pins which may be actively driven by CMOS/TTL outputs or strapped to +Vcc (as a 1) or non-connected as appropriate. Non-connected inputs are biased low or 0. When the binary coded value of zero is entered into these counter preselect inputs, their outputs are disabled, thereby saving AC output power. Output symmetry is very close to 50% duty cycle with both odd and even division modulus due to an odd division correction employed at the counter's output. Refer to the counter preset tables for the binary coded preselect input values to division modulus.

The TTL output drivers of the T counter are source series terminated by internal resistors of ~40 Ohms to avoid the need for external termination. This series termination was choosen to match 50 to 75 Ohm transmission line traces into end of line load capacitance of ~20 pF. Refer also to the AMCC Clock Driver Application Note #1. The complementary PECL output emitter followers can source 25 mA from +Vcc and should be externally terminated at the end of the transmission line into an equivalent 50 Ohm resistance to +Vcc - 2V.

The analog VCO circuitry requires some external passive loop filter components mounted very close to the required S4503 package pins. A VCO frequency centering resistor, RFcenter, is connected between KVCO and +VCCA, the analog +5V. A frequency span resistor, Rspan, is connected between pins REXT1 and REXT2. A loop filter series resistor-capacitor pair, RCOMP & CCOMP is connected between pin Comp and analog ground GNDA. Note that the analog ground (GNDA) and +5V (+VCCA) are to be isolated (decoupled) from the noisier digital and output power leads VCC and GND.

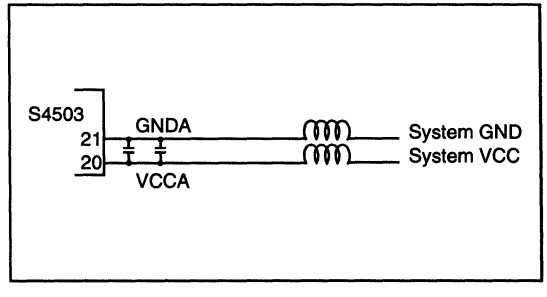
The input to the XTALIN pin will be a series resonant crystal of fundamental frequency from 5 to 25 Mhz. The external addition of series or shunt capacitance to "pull" the frequency is up to the user's discretion. An external series resistor may be required to limit the drive current from the Xtlout pin with low ESR crystals.

When the XTLIN pin is driven by an external TTL clock source, the XTLOUT pin is not connected and the peak TTL amplitude should not exceed 3 volts. TTL output signals should be in the range of 5-80 MHz.

BOARD LAYOUT CONSIDERATIONS

To minimize the impact of board noise on the operation of the S4503, the following guidelines should be followed.

- The analog VCCA and GNDA need to be isolated from the digital supplies. This can be accomplished by creating small analog power and ground planes next to the S4503 under the filter and VCO components. These analog planes can be connected to the digital planes through wire jumpers, small inductors (5-100 uH), or ferrite beads. If the digital supply noise is too large (>100mV), the inductors or ferrite beads will be necessary.



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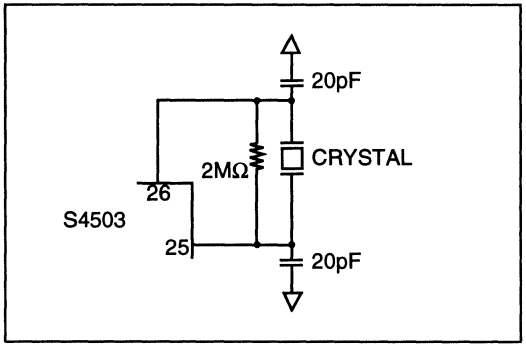
- Decoupling capacitors of 0.1 and 0.01 uF are needed. Three pairs should be placed as close to the S4503 power and ground pins as possible. One pair should be used to decouple the analog VCC and GND, while the others are for the digital supplies. The Vtt supply will also need to be decoupled using 0.1 and 0.01 uF capacitors. These components should be surface mounted chip capacitors, to reduce the parasitic inductance.
- No dynamic signal lines should pass through or beneath the filter circuitry area, to avoid the possibility of noise due to crosstalk.
- The crystal oscillator will need to have a 2 M ohm shunt resistor connected between the terminals of the external crystal, and two 20 pF capacitors connected from each pin of the crystal to VCC (or GND). These components are necessary to ensure the oscillator will operate at the correct frequency.



- The loop filter and VCO components must be surface mounted to reduce the parasitic inductance, and the components are connected to the analog power and ground planes, rather than the digital planes.

FILTER AND VCO COMPONENT SELECTION

The S4503 is designed to operate over a wide range of VCO frequencies. Because of this, it is necessary to modify the values of Rspan and Rfcenter in order to get the best performance at a given frequency.

When operating the S4503 with the VCO in the 150–225 MHz region, the values for the VCO components are:

Rspan = 470 Ohms, Rfcenter = 390 Ohms

When operation the S4503 with the VCO in to 225–300 Mhz, the values for the VCO components are:

Rspan = 390 Ohms, Rfcenter = 820 Ohms

The loop filter components, Rcomp and Ccomp, do not change values at different frequencies. The correct values for these components are:

Rcomp = 2.7K Ohms, Ccomp = 0.1uF

All of the resistor values are 5% and 1/8 watt.

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Power Management

The overall goal of managing the power dissipated by the S4503 is to limit it's junction (die) temperature to 130°C. A major component of the power dissipated internally by the S4503 is determined by the load that each TTL output drives and the frequency that each output is running. The following table summarizes these dependencies.

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	C_{LOAD}=40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	65 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	60 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (700 mW) of the S4503 to determine the total power being dissipated by the S4503. This total power is then multilplied by the S4503's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S4503. For greatest reliability this junction temperature should not exceed 130°C. The thermal resistance for the S4503 is as follows:

	STILL AIR	100 LIN FT/MIN	200 LIN FT/MIN
THERMAL RESISTANCE	60°C/Watt	50°C/Watt	45°C/Watt

Designing the S4503 for "Real Loads"

The S4503 is designed to provide clean clock transitions when presented with a realistic load. The assumptions are that the S4503 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading can cause overall impedance to drop to under 60 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with capacitive loads ranging up to 20 pF at frequencies up to 80 MHz. Higher capacitive loads (greater than 25 pF) at high frequencies (greater than 50 MHz) may require the like output drivers to be strapped in parallel.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented on the following page. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note.

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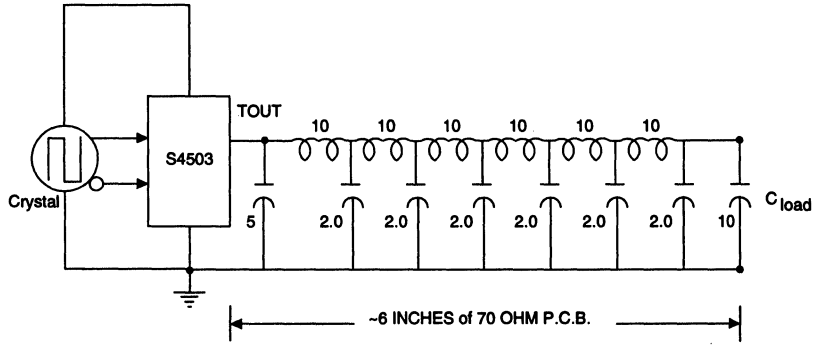
Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point destination is recommended

S4503 M- Counter Division Table

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	0	INVALID
1	0	0	0	0	2
0	1	0	0	0	3
1	1	0	0	0	4
0	0	1	0	0	5
1	0	1	0	0	6
0	1	1	0	0	7
1	1	1	0	0	8
0	0	0	1	0	9
1	0	0	1	0	10
0	1	0	1	0	11
1	1	0	1	0	12
0	0	1	1	0	13
1	0	1	1	0	14
0	1	1	1	0	15
1	1	1	1	0	16

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	1	17
1	0	0	0	1	18
0	1	0	0	1	19
1	1	0	0	1	20
0	0	1	0	1	21
1	0	1	0	1	22
0	1	1	0	1	23
1	1	1	0	1	24
0	0	0	1	1	25
1	0	0	1	1	26
0	1	0	1	1	27
1	1	0	1	1	28
0	0	1	1	1	29
1	0	1	1	1	30
0	1	1	1	1	31
1	1	1	1	1	32

[Where: M(0:4) + 1 = MODULUS and $M0=2^0$, $M1=2^1$, $M2=2^2$, $M3=2^3$, $M4=2^4$]

S4503 Output Counter Division Table

P0	P1	P-MODULUS
0	0	DISABLED
1	0	1
0	1	2
1	1	4

T0	T1	T2	T3	T1-MODULUS
0	0	0	0	DISABLED
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

Where T1 (0:3) + 1 = MODULUS and

$T0 = 2^0$

$T1 = 2^1$

$T2 = 2^2$

$T3 = 2^3$

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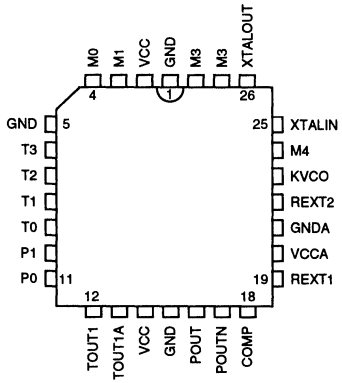
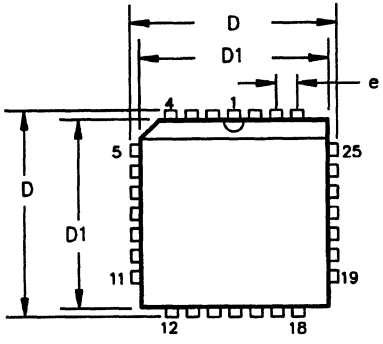
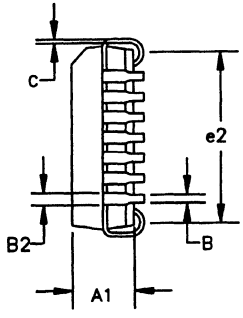
Package 28 PLCC Package and Pinout



SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.687	.697
D1	.644	.659
e	.048	.052
e2	.610	.630





All dimensions nominal in inches.

Ordering Information

Part Number	Package Type
S4503	A-28 PLCC

XXXXX Part Number

X Package

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NOTES

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Bus Products 6

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36-BIT ODD/EVEN PARITY GENERATOR AND CHECKER S4280

Features:

- 10.4ns Propagation Delay (commercial, worst case)
- Generates both Odd and Even Parity
- Checks for both Odd and Even Parity
- Configured as four Independent 9-bit Parity Generators and four 9-bit Parity Checks with Byte Select
- Byte Independent Parity Error Forcing Capability
- Ideal for use in High Performance 32-Bit CPU System Designs
- Surface Mount Technology
- Replaces four '280's and PAL Device

Description:

Packaged in a 68 pin J-leaded chip carrier, the S4280 is a 36-Bit Parity Generator and Checker used to detect errors in high speed data transmission and retrieval systems. Both Odd and Even parity outputs are available for each of the four bytes of data. Four force parity error lines (one for each byte) allow the system to verify the operation of the parity generating and checking circuits by forcing parity errors.

Four select lines are used to select bytes for checking parity. Both even and odd parity error signals are available as outputs. A "read/write" option is also provided, with parity checking enabled during "read" operations.

Signal Names:

DATA (input) [D (0:31)]
32 data input signals.

WRITE (input) [$\overline{WR}$]
This signal is driven by the processor to indicate a read or write operation. A low indicates a write cycle, during which the S4280 will generate parity for each byte, while a high indicates a read cycle and a corresponding check for correct parity on each byte.

FORCE PARITY ERROR (input) [FPE (0:3)]
This active high signal is typically driven by an external control register. When high, it inverts the parity such that "bad" parity is stored at that memory location. Parity circuitry may be tested by writing "bad" parity and then reading it to verify that a parity error occurs. Note: FPE can be disabled by tying this input to ground.

PARITY IN (input) [PI (0:3)]
The four parity input signals (one for each byte) are commonly driven from an external DRAM. PI0 corresponds to D0:7, PI1 corresponds to D8:15, PI2 corresponds to D16:23, and PI3 corresponds to D24:31.

BYTE CONTROL (input) [$\overline{BC}$ (0:3)]
These four active low signals select which byte contains data/parity to be checked. BC0 corresponds to D0:7, BC1 corresponds to D8:15, BC2 corresponds to D16:23, and BC3 corresponds to D24:31.

ODD PARITY OUTPUT (output) [OPO (0:3)]
These parity outputs are active high. OPO0 generates odd parity for D0:7, OPO1 generates odd parity for D8:15, OPO2 generates odd parity for D16:23, and OPO3 generates odd parity for D24:31. These outputs are commonly used only during write cycles and are written to external DRAMS if odd parity is desired.

EVEN PARITY OUTPUT (output) [EPO (0:3)]
These parity outputs are active high. EPO0 generates even parity for D0:7, EPO1 generates even parity for D8:15, EPO2 generates even parity for D16:23, and EPO3 generates even parity for D24:31. These outputs are commonly used only during write cycles, and are the logical inverse of the OPO (0:3) lines.

ODD PARITY ERROR (output) [$\overline{OPE}$]
This active low parity error signal indicates that an odd parity error occurred on one of the four selected data bytes.

EVEN PARITY ERROR (output) [$\overline{EPE}$]
This active low parity error signal indicates that an even parity error occurred on one of the four selected data bytes.

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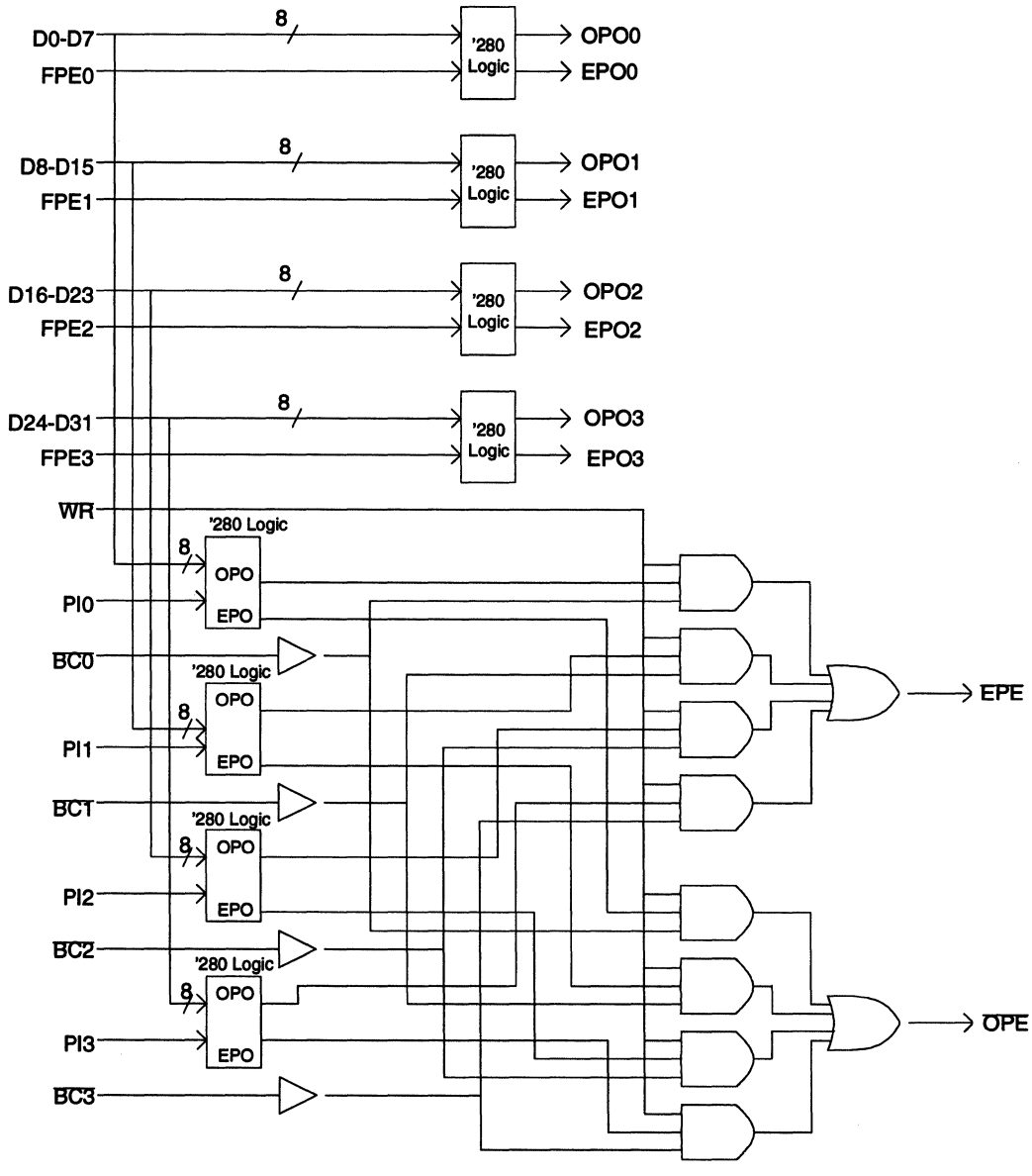

Note: Logical representation only. Circuit level implementation may differ.

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PARITY GENERATION

INPUTS		OUTPUTS	
FPE (0:3)	D0:7, D8:15, D16:23, D24:31 (# of High Data Lines)	OPO (0:3)	EPO (0:3)
L	Even - 0, 2, 4, 6, 8	L	H
L	Odd - 1, 3, 5, 7	H	L
H	Even - 0, 2, 4, 6, 8	H	L

PARITY CHECKING

INPUTS									OUTPUT
$\overline{WR}$	$\overline{BC3}$	$\overline{BC2}$	$\overline{BC1}$	$\overline{BC0}$	D31-D24, PI3	D23-D16, PI2	D15-D8, PI1	D7-D0, PI0	$\overline{EPE}$[1]
L	X	X	X	X	X	X	X	X	H
H	L	L	L	L	Even	Even	Even	Even[2]	H
					X	X	X	Odd[2]	L
					X	X	Odd	X	L
					X	Odd	X	X	L
					Odd	X	X	X	L
H	L	L	L	H	Even	Even	Even	X	H
					X	X	Odd	X	L
					X	Odd	X	X	L
					Odd	X	X	X	L
H	L	L	H	L	Even	Even	X	Even	H
					X	X	X	Odd	L
					X	Odd	X	X	L
					Odd	X	X	X	L
H	L	L	H	H	Even	Even	X	X	H
					X	Odd	X	X	L
					Odd	X	X	X	L
H	L	H	L	L	Even	X	Even	Even	H
					X	X	X	Odd	L
					X	X	Odd	X	L
					Odd	X	X	X	L
H	L	H	L	H	Even	X	Even	X	H
					X	X	Odd	X	L
					Odd	X	X	X	L
H	L	H	H	L	Even	X	X	Even	H
					X	X	X	Odd	L
					Odd	X	X	X	L
H	L	H	H	H	Even	X	X	X	H
					Odd	X	X	X	L
H	H	L	L	L	X	Even	Even	Even	H
					X	X	X	Odd	L
					X	X	Odd	X	L
					X	Odd	X	X	L
H	H	L	L	H	X	Even	Even	X	H
					X	X	Odd	X	L
					X	Odd	X	X	L
H	H	L	H	L	X	Even	X	Even	H
					X	X	X	Odd	L
					X	Odd	X	X	L
H	H	L	H	H	X	Even	X	X	H
					X	Odd	X	X	L
H	H	H	L	L	X	X	Even	Even	H
					X	X	X	Odd	L
					X	X	Odd	X	L
H	H	H	L	H	X	X	Even	X	H
					X	X	Odd	X	L
H	H	H	H	L	X	X	X	Even	H
					X	X	X	Odd	L
H	H	H	H	H	X	X	X	X	H

Note: 1. The truth table for $\overline{OPE}$ is generated by reversing odd and even in the above table and changing the output to $\overline{OPE}$.
2. Even = 0, 2, 4, 6, 8 one's in nine bit input.
Odd = 1, 3, 5, 7, 9 one's in nine bit input.

ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0V
TTL Input Voltage (V_{EE} = 0)	5.5V
Operating Temperature	−55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	−65° to + 150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	COMMERCIAL			MILITARY			UNITS
	MIN	NOM	MAX	MIN	NOM	MAX	
TTL Supply Voltage (V_{CC})	4.25	5.0	5.25	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20			20	mA
Ambient Operating Temperature	0		70	−55		125	°C
Junction Temperature (T_J)			130			150	°C
TTL Supply Current (I_{CC})			201			201	mA

TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} — Min, I_{IN} = −18mA		−.8	−1.2	V
V_{OH}	Output HIGH voltage	V_{CC} — Min, I_{OH} = −1mA	2.7	3.4		V
V_{OL}	Ouput LOW voltage	V_{CC} — Min, I_{OI} = 20mA			0.5	V
I_{IH}	Input HIGH current	V_{CC} — Max, I_{IN} = 2.7V			50	µA
I_I	Input HIGH current at Max.	V_{CC} — Max, I_{IN} = 5.5V			1	mA
I_{IL}	Input LOW current	V_{CC} — Max, I_{IN} = 0.5V			−.4	mA

AC CHARACTERISTICS[3]

PARITY CHECKING

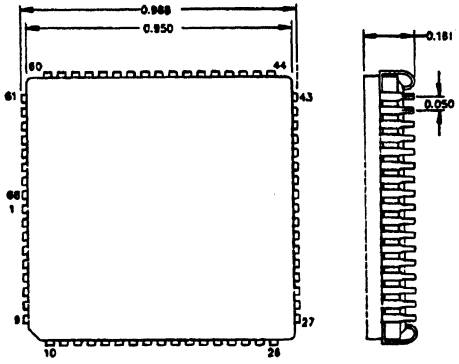
SYMBOL	PARAMETER	COMMERCIAL		MILITARY	
		TYP	MAX	TYP	MAX
t_{LH}	Propagation Delay	8.3	9.1	8.9	9.7
t_{HL}	WR to EPE, OPE	6.6	7.2	7.1	7.8
t_{LH}	Propagation Delay	8.6	9.4	9.2	10.1
t_{HL}	BCn to EPE, OPE	6.2	6.8	6.7	7.3
t_{LH}	Propagation Delay	9.5	10.4	10.2	11.2
t_{HL}	Dn or Pin to EPE, OPE	7.6	8.4	8.2	9.0

PARITY GENERATION

SYMBOL	PARAMETER	COMMERCIAL		MILITARY	
		TYP	MAX	TYP	MAX
t_{LH}	Propagation Delay	9.3	10.2	10.0	10.9
t_{HL}	Dn or FPEn to EPOn	8.3	9.1	8.9	9.8
t_{LH}	Propagation Delay	9.2	10.1	9.9	10.9
t_{HL}	Dn or FPEn to OPOn	8.2	9.0	8.8	9.7

1 Typical limits are at 25°C, V_{CC} = 5.0V.
2 These input levels provide zero noise immunity and should be tested in a static, noise-free environment.
3 Measured with 15pf output load external to device.

68 PIN J-LEADED CHIP CARRIER



Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	23	D15	47	D16
2	OPEN	24	D4	48	D17
3	OP1	25	BC0N	49	D18
4	OP0	27	BC1N	50	D19
5	D0	28	D5	51	GND
6	D1	29	D6	52	VCC
7	PI1	30	D7	53	D20
8	FPE1	32	EP0	54	D21
10	PI0	33	EP1	55	D22
11	FPE0	34	EPEN	56	D23
12	D2	35	VCC	57	D28
13	D3	36	GND	58	FPE2
14	D8	37	OP2	59	FPE3
15	D9	38	OP3	61	PI3
16	D10	39	WRN	62	PI2
17	D11	40	D24	63	D29
18	VCC	41	D25	64	D30
19	GND	42	D26	65	D31
20	D12	44	BC3N	66	EP3
21	D13	45	BC2N	67	EP2
22	D14	46	D27	68	GND

ORDERING INFORMATION

Grade	36 Bit Parity Generator/Checker	Package
S - Commercial M - Military	4280	A - Ceramic B - Plastic

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FEATURES

- Low Cost
- Single–chip PCI–BUS master or PCI–BUS slave for add–on products
- Integrated data path
- Two 32–byte FIFOs (one for each data direction)
- 32–bit width (S5932, S5933), 8– or 16–bit width (S5930, S5931)
- Built–in address decoding (memory space and I/O)
- Data path size matching and lane steering
- Performs PCI Burst transfers
- Dual address counters (one for writes, one for reads) for PCI port
- Throttle control on PCI port
- Two sets of 16 bytes of mailbox register(s) with empty/full status and interrupts
- Interrupt on transfer complete and/or mailbox activity
- Synchronous host interface
- Asynchronous add–on interface
- Supports external x 8 BIOS EPROM S5931, S5933) or serial NVRAM (S5930, S5933)
- Implements PCI Configuration Registers
- Pass–through mode permits PCI Bus access to add–on elements or emulation of other hardware
- 120, 144 and 160 PQFP package

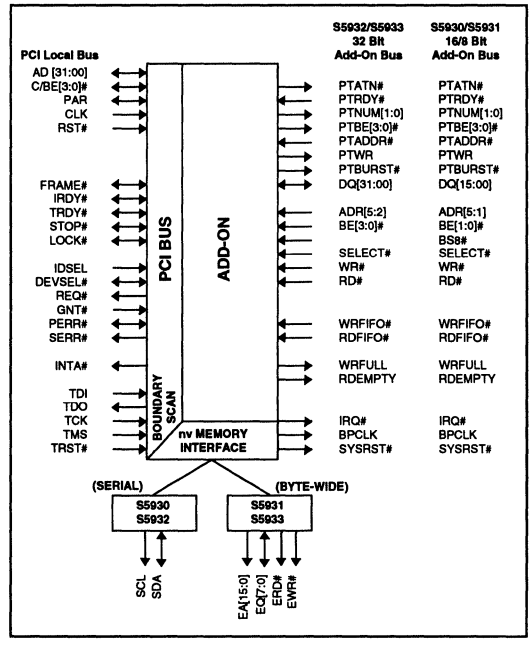
APPLICATIONS

- RAID Systems—File Servers/Work Stations
- Communication Boards—File Servers/Work Stations
- Image Processing—Video Conferencing, Editing, Multimedia, Games, Image Recognition
- Instrumentation, Custom Applications
- Data Acquisition Systems

GENERAL

AMCC's PCI Local Bus Master/Slave Controller Interface provides a high performance single–chip solution between the PCI local Bus Standard and custom add–on boards. Address decoding, address sourcing, burst transfers, and all elements necessary to perform efficient and timely data transfers are provided within the device. Included within is a bidirectional 32–bit wide FIFO which facilitates the system–to–system synchronization and data transfers between the local bus and the add–on product. A custom BIOS EPROM can be used to perform any pre–boot initialization required of the add–on function. The external ROM/EPROM/NVRAM can be either in by eight or serial form and provides a convenient method to customize an add–on board.

Figure 1. PCI Interface Controller Signal Groups



This component is designed to permit the direct connection between the PCI local bus and a variety of general purpose microprocessor style buses. Bus Master transfers can be performed on the PCI Local Bus while accesses occur on the add–on's processor bus. Transfer parameters, such as the PCI address, transfer counts, mailbox registers, and status are provided in the PCI interface controller as I/O mapped locations on the PCI bus.

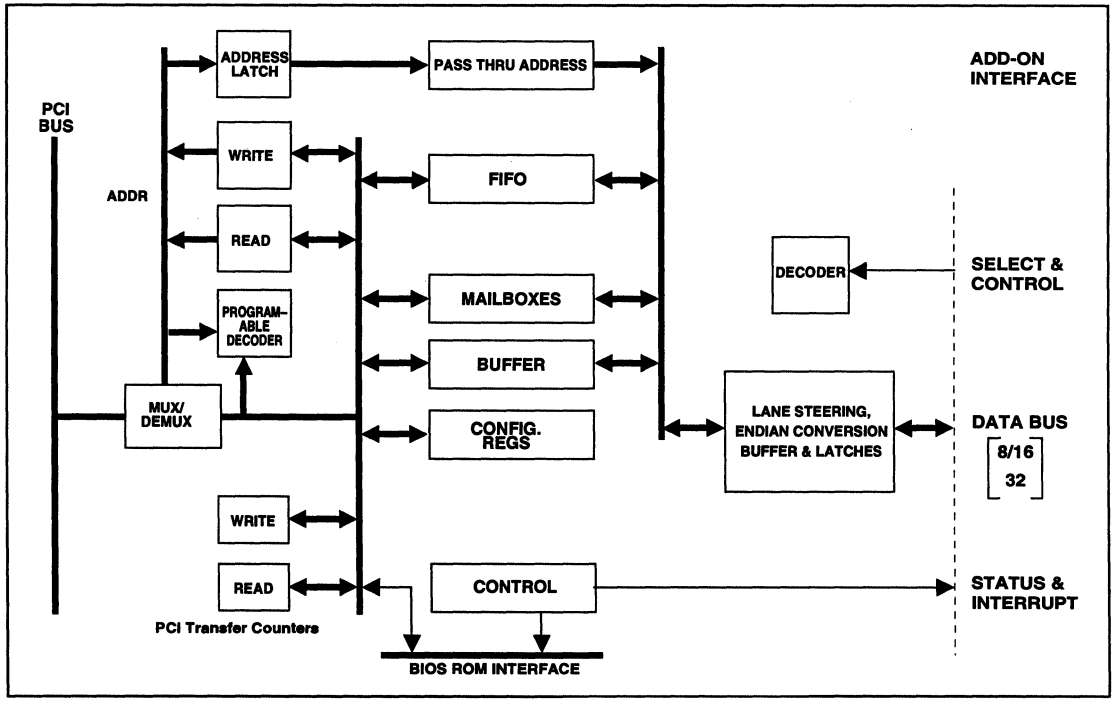
The PCI Local Bus Master/Slave Controller consists of three signal groupings: the Local Bus signals, the EPROM interface, and the add–on general purpose bus signals.

APPLICATIONS

Many of the high–end, complex peripheral functions in today's PCs require (or prefer) their implementation with their own dedicated, embedded microprocessor. Often, the functions desired and the local memory necessary for these add–on products prohibit their integration into a single device. The benefits from the embedded microprocessor approach mostly come from the flexibility, time to market, and function complexity which only software techniques can achieve.

AMCC's PCI controllers provide for a high performance, highly integrated, and easy–to–use method to interface an embedded microprocessor subsystem with the PCI Local Bus.

Figure 2. S5930–S5933 Block Diagram



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Application Notes 7

NOTES

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The SC35XX Family of Clock Drivers have been designed to provide single chip solutions which ease clock distribution for TTL/CMOS I/O compatible microprocessor based systems.

All products have a generous supply (10 or 20) of the various derived frequency outputs to avoid overloading any one output. The outputs may also be used in parallel for driving particularly heavy loads. The availability of numerous clock outputs reduces the need to "daisy chain" or "branch" loads. The end benefit to the user is reduced clock skew with a high quality received wave form. By virtue of this single chip providing clock shape, clock edge alignment and clock fanout, the system designer's task is reduced to providing load balance and careful P.C. board layout.

- This "Appnote" describes and discusses:
- Frequency Sources
- Skew Management
- Clock Waveform Signal Integrity
- Chip Power Estimations
- High Capacitance Loads
- Output Symmetry Compensation
- Reset Control and Timing
- Use of Multiple Clock Chips in a System-Primary and Secondary Distribution

FREQUENCY SOURCE

It is suggested that the basic Frequency Source be a low cost crystal-controlled oscillator (XCO). Frequency tolerance and stability are offered from 0.05% (500PPM) to 0.001% (10PPM), with 0.01% (100PPM) being readily available at competitive prices. These crystal oscillators should be acceptable over most operating temperature ranges. Only with large temperature fluctuations during operation would the higher priced temperature compensated crystal oscillator (TCXO) be suggested. TTL output devices are available up to 100 MHz with ECL output devices spanning the entire range of interest, from 30 to 200 MHz.

An appended list of domestic sources for these oscillators, including phone numbers is provided. While this list is not all inclusive, it will provide an initial reference (See Appendix A).

NOTE: The SC35XX PECL (Positive 5 -Volt ECL) Inputs are designed to interface with an ECL output oscillator operating at ground to +5.0 Volts. The oscillator's complementary emitter follower outputs may be "self-terminated" within the package by 200 to 500 Ohm pull down resistors to ground (- Vee) or they may be terminated discretely via resistors on the P.C. board. The oscillator should be placed close (<4") to the SC35XX driver.

CLOCK SKEW MANAGEMENT

The SC35XX has been designed to reduce the system level Clock Skew Management task to two basic design issues.

1) P.C. Board layout (keeping all clock traces to approximately equal lengths)

2) Matching the end-of-line load capacitance, to within 5 to 10 pF.

These two signal-edge delay (or skew) contributors can be estimated, as follows (Figure 1)

1) "Microstrip", which is the single surface conductor over a distributed ground or power plane, has a nominal propagation delay of approximately 150 pS per inch.

2) "Stripline", which is a buried conductor sandwiched between two ground or power planes, has a nominal propagation delay of approximately 200 pS per inch.

3) Variations in the end-of-line lumped-load capacitance will increase or decrease the clock signal's rise and fall time. These changes will be approximately 0.5 ns per 10 pF over the range of 10 to 40 pF. Be sure to verify the receiving input package capacitance of all clock receptors. Typically, plastic flat packs have the lowest with ceramic pin grid arrays (PGA's) having the highest input pin capacitance values. PGA's also have the disadvantage that their plated thru holes can add significant capacitance (up to 10 pF or more.) This should be checked with a capacitance meter.

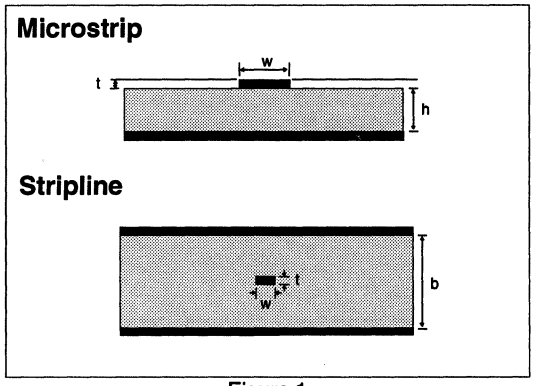

Figure 1

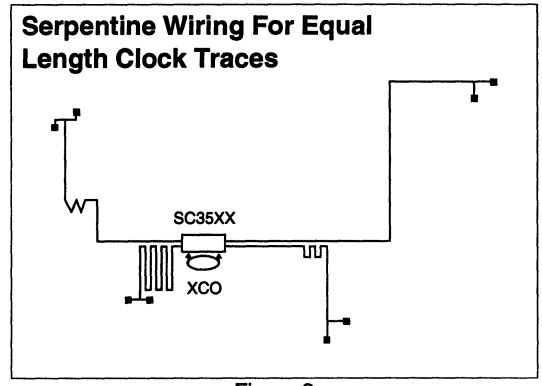

Figure 2

4) To match clock trace lengths, when the receiving devices are differing "Manhattan" distances from the SC35XX driver, the P.C. trace must be lengthened to the closer loads. This can be accomplished by forming a "serpentine" path (Figure 2).

5) Due to the simultaneous switching of up to 20 capacitively loaded output drivers, the $+V_{CC}$ and ground power should be provided by low impedance, well decoupled $+V_{CC}$ and ground planes within the P.C. board (refer to "Summary", pg 8, item 6).

CLOCK WAVEFORM SIGNAL INTEGRITY

Clock waveform signal integrity refers to the control of noise margin and receiver threshold crossing distortions. DC margins for TTL I/O levels are often secondary when operating frequencies exceed 25 MHz. This is due to the overriding effects of "overshoot/undershoot" (i.e., ringing) or poorly terminated transmission lines causing reflections from the end of the line back toward the signal source.

The effect of these reflections can be the presence of half or partial amplitude steps in the clock wave form appearing at intermediate "branched" or "daisy chained" load points. These partial amplitude steps can cause spurious triggering at these intermediate load points.

The TTL/CMOS clock output driver must provide a reasonably square voltage waveform from +0.5 to + 3.5 Volts, as a minimum. Unfortunately, you must distribute this clock over a printed copper trace with variable inductance, capacitance and length, which may exhibit characteristic line impedance (Zo) anywhere from 50 to 200 Ohms. Add to this the variable of receiver(s) load capacitance and notice that the 50% duty cycle square wave that you started with has become distorted with ringing and undershoot. You should be aware that undershoot below about -1.0 Volt can draw substrate bias current at the receivers causing transient errors.

All of this leads to a need for controlled impedance PC wiring with good impedance match termination. This is especially true when you consider device input clock frequencies are approaching > 60 MHz while high and low times of critical minimum widths and voltage levels are specified.

The introduction of line termination is necessitated by the ringing and distortion at the clock receptors caused by the mismatch of the driver source to the line and the load impedance. This added termination, wherever applied, is a compensation to the original mismatch which is sensitive to frequency, inductance and capacitance of the P.C. board.

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Several methods of line termination are available (refer to Transmission Line "Termination", figure 3):

A. DC shunt load termination is generally a Thevenin equivalent resistor pair across the +5 Volts and ground buses with the mid point tied to the end of each clock line. While the signal integrity results are good, the large power consumption, due to the large voltage applied to the low end of line resistance make this scheme a poor choice.

B. AC shunt load termination can be effective to "tune" each load network with a selected series resistor-capacitor pair at the end of each clock line to ground. If the load capacitance or line length varies appreciably, so must the R-C termination pair. As with any of the shunt load termination schemes, you must provide external trace and component mounting locations at the end of every clock line. AC power dissipation is quite high using this method.

C. DC series source termination can be incorporated within the clock output driver on the IC itself thereby eliminating the need for additional board-mounted components. The source termination permits a reasonable compromise to accommodate a variation in line impedance and load capacitance with quite good signal fidelity. Clock loads may only be placed at the end of the line.

NOTE: Use of any of the series or shunt termination methods precludes the use of branch or "Y" wiring within the clock fanouts due to impedance splitting.

The following table compares these three described termination schemes:

	DC SHUNT	AC SHUNT	SOURCE
EXTERNAL MOUNTING	YES	YES	NO
TUNING AT LOADS	NO	POSSIBLE	NO
DAISEY CHAIN	PENALTY	PENALTY	NO
LOAD CLUSTER AT END	DESIRED	DESIRED	REQ'D

The SC35XX helps the designer manage these "reflections" in two ways. First, with a generous number of clock outputs (10 or 20) available, "daisy

Transmission Line "Termination"

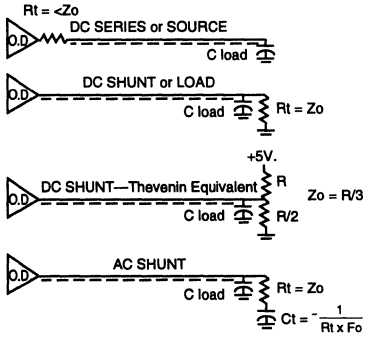

Figure 3

chained" or "branched" connected receivers can be avoided. Secondly, the source termination within the SC35XX output drivers is provided to optimally terminate a lumped-load capacitance at the end of a 50 - 100 Ohm transmission line, without the addition of any discrete termination circuits.

While 100 Ohm traces are preferred, characteristic line impedances of 50 or 75 Ohms, may be necessary at an increase of power in the SC35XX's output drivers. These lower impedance P.C. board traces are generally dictated by manufacturing issues accompanying multiple signal, power, and ground layers in the P.C. board fabrication.

Remember that TTL type signal amplitudes, in the 2.5 to 4.0 Volt peak range, dissipate considerable CV^2F power. This CV^2F power, coupled with the fact that the transmission line capacitance is at least twice as great at Zo=50 Ohms compared to Zo=100 Ohms, strongly suggests that the characteristic trace impedance of high frequency clock lines should be selected at 70 Ohms or above, with 100 Ohms recommended. See Appendix B for equations.

NOTE: For end-of-line lumped capacitance, a cluster or branch of receiver pins within two inches of each other is acceptable. The capacitance of all such pins is additive. See Figure 4.

7

End of Line Load Clustering L1 Or L2 <2"

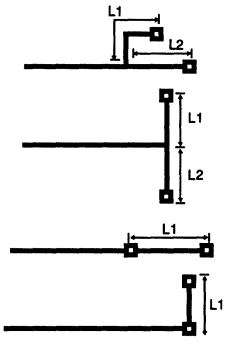

Figure 4

SC35XX POWER DISSIPATION

With output frequencies above 50 MHz, the SC35XX's loading must be "managed" to limit its power dissipation to less than 1 Watt. This can be accomplished by minimizing the loading on each clock output or by connecting fewer of the clock outputs. In this case unused outputs still dissipate a minimum of power, which must be added into the total.

The SC35XX product data sheets detail all necessary power dissipation calculations.

NOTE: The capacitance of 70 Ohm transmission line is approximately 1.5 times that of 100 Ohm line for effective lengths up to one rise time or ~10 inches and, as mentioned above, with Zo=50 Ohms the capacitance is twice that of Zo=100 Ohms. The additional effective output load capacitance is approximately 8pF for 70 Ohms at 10 inches as compared to 100 Ohms. See Appendix B for equations.

CAPACITIVE LOADS

- Capacitive loads consist of the sum of four contributors.
- The "load" package itself, where a plastic flat pack may exhibit 4-8 pF load, while a ceramic pin grid array may represent 8-15 pF load.
- Plug in sockets can add 5-10 pF.
- Plated-through-holes in a dense multiplayer P.C. board may add as much as 5-15 pF.

P.C. board trace impedance (as reviewed above)

The SC35XX products are designed to drive a wide variation in capacitve loads. AMCC strongly recommends that the user "balance" his loads as equally as possible. This will help to minimize skew at the various loads (the larger a load is, the slower the rise time of the clock). Where the user is not able to balance his loads, the skew will typically be derated at 50ps/pF at the 1.5V threshold. (Example - one load is 5 pF heavier than all other loads - that load's clock will cross the 1.5V threshold 250 ps later than the others). A compensatory shortening of the higher capacitance load traces may be considered.

In addition to presenting capacitive loads, some microprocessors and co-processors require minimum peak clock amplitudes of 3.5 Volts or greater along with a minimum dwell time at a specified voltage level.

While each output driver of the SC35XX has been designed to handle a wide frequency-voltage-load range, they have also been designed to allow the parallel application of two (or more) adjacent drivers to a common load. By connecting two adjacent drivers to a common load, such as a microprocessors or co-processor, the user reduces the effective output series termination by half, while doubling the available peak and static output current that can be supplied to that load.

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RESET CONTROL

The Reset control input is shifted into the control of the binary counter to provide both proper sequential count out clearing and rising edge synchronous restart of the clock outputs. Refer to "Reset to Output Timing" Figure, below.

The reset function is delayed by four or five falling input clocks in its effect upon the outputs in deasserting (HIGH). Reset has an assertion (low) window of seven clocks plus a delay of four clocks minimum to provide count down clearing, refer to Reset Timing Figure. The aggregate delay of reset assertion is the 3-clock reset shift register, plus the 0 to 7 clock counter count-out window, plus the single clock at the output resync flip flop. This total is, therefore, 4 to 11, 2F clocks.

The user may choose to implement a gross delayed "power up reset" by withholding clock outputs. This can be obtained by applying an external capacitor between the RESET pin and ground. The input pin provides a ~20K Ohm pull up resistor to +5.0 Volts.

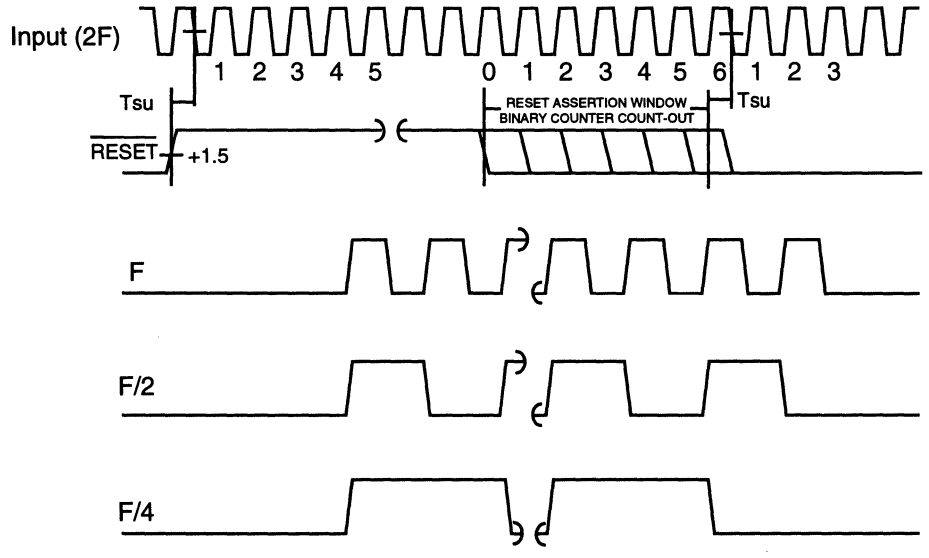
NOTE: The above reset timing control applies to: SC3500, SC3506, SC3507, SC3508, SC3517, SC3518, SC3528 and SC3529. If multiple outputs of SC35XX are to be reset resynchronized by a common RESET input to all, set up and hold times of RESET with respect to input clock of 3 ns must be accommodated.

USE OF MULTIPLE CLOCK CHIPS IN A SYSTEM

Many applications require greater than 20 clock outputs, where the use of multiple SC35XX's would be advantageous. The loads that receive these clocks may all reside on a large PC Board, or they may be distributed across a number of PC Boards interconnected via a backplane.

To effectively distribute these clocks requires the user to give some consideration to the strategy for distributing the SC35XX Primary input clock. The objective is to get a minimal skew, Primary clock distributed to each SC35XX.

Reset To Output Timing



7

Remember that the SC35XX provides the option of two different types of Primary clock inputs. For Primary inputs over short distances and at Primary frequencies of 50 MHz or less the single rail TTL input may be used. For "longer" distances and backplanes or where the Primary frequencies exceed 50 MHz AMCC recommends that the user consider utilizing the "PECL" (Positive referenced 100K ECL input). In either case a single +5V power supply is the only power supply required.

The diagrams below and on the following page summarize these recommendations.

The High Speed PECL distribution scheme utilizes the Motorola MC100E111(Differential, 1:9, 50ps Skew, ECL Driver) fed from the Crystal Oscillator (XCO). This primary fanout driver requires a pair of 240 Ohm pull down resistors to ground at its input pins. All of the output pairs should be source terminated by a 40 Ohm resistor in series and a 240 Ohm pull down (to ground) resistor at both legs of the differential PECL output. The differential primary fan branches should be of equal length when routed to the receiving SC35XX.

Alternatively, the PECL backplane signal pairs can be shunt (load) terminated at each SC35XX input by a thevenin equivalent 50-70 Ohm resistor to +3V. As an example, a 100 Ohm resistor to +5V and a complement 150 Ohm resistor to ground is equivalent to 60 Ohms to +3V.

There are two main advantages to these schemes:

1. Minimal Noise Generation

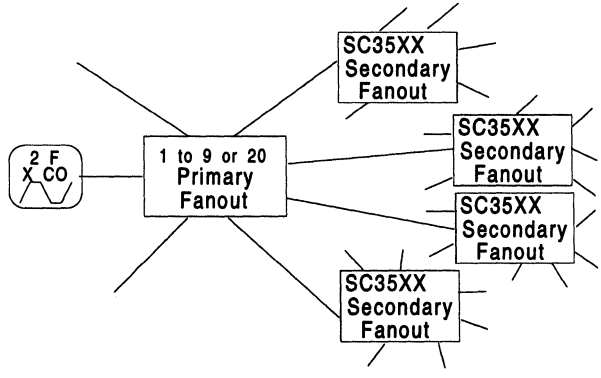
The high speed PECL signals are limited to 0.8V in peak amplitude, limiting the potential effects that they might have on surrounding TTL signals. Furthermore, by running these signals, in pairs with opposing (complementary) signals the crosstalk they might generate into surrounding TTL signals is mostly cancelled.

2. High Noise Immunity

The surrounding TTL swings have somewhat slower rise and fall edge rates than the PECL signals. Since the PECL signals are differentially received at the SC35XX (as well as 40 ohm terminated at the source) the TTL noise will appear in equal phase and equal amplitude on each of the differential signals. The SC35XX will reject this common mode noise at it's receiver, providing excellent noise immunity.

The Low Speed TTL distribution scheme utilizes the SC3508 (TTL 1:20 Driver) fed from the crystal oscillator. As you would guess, good TTL termination techniques should be followed. This includes avoiding "daisy chaining" or "branching" of the Clock Fans (greater than 1" to 2").

Basic Primary to Secondary Clock Fan-Out Tree



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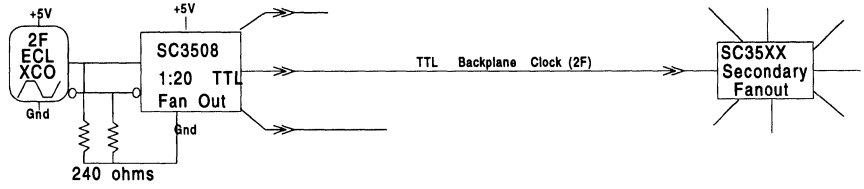
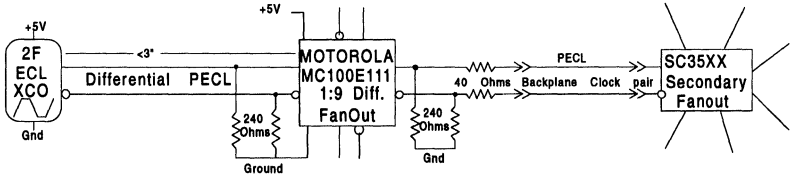
A Low Speed, TTL Primary Clock Fan-Out Path To The SC35XX



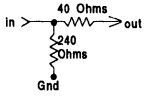
NOTE: A SC3508 primary to SC3508 secondary fanout is not recommended, due to the potential pulse width shrinkage of a 1X single ended output feeding a second 1X driver without reshaping.

A High Speed Series Terminated PECL Primary Clock Fan-Out Path To The SC35XX

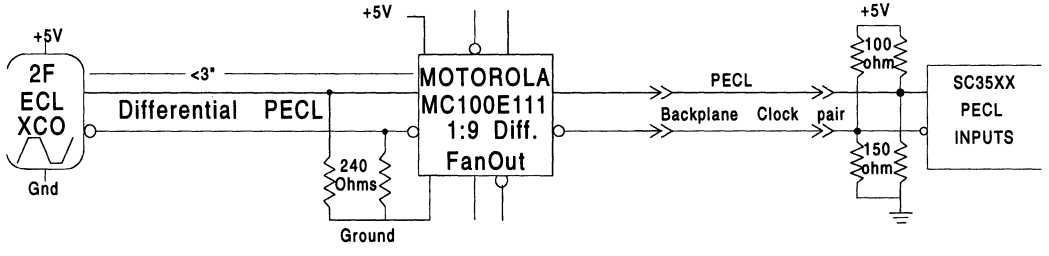


NOTE: Source resistor pairs may be implemented with discrete resistors, resistor packs of 240 Ohms and 40 Ohms each or custom packs of combined 240 and 40 Ohms for each signal through the pack.

Example:



Alternate PECL Primary Fanout Path To SC35XX With Shunt (Load) Termination At Each SC35XX Input Pair



SUMMARY

The SC35XX greatly simplifies the task associated with distributing high performance clocks within today's systems. It accomplishes this by reducing the variables that the designer must contend with to these basic issues:

1) Keep each clock driver's loading light (SC35XX's 10 or 20-clock outputs allows one load per clock output typically);

2) Balance the total load equally among all drivers as closely as possible;

3) Keep clock trace lengths equal (Use serpentine traces to make all clock traces of equal length);

4) Be aware of and manage CV^2F power dissipation in the SC35XX. Where possible make clock traces Zo=70 or 100 Ohms for minimal power dissipation;

5) High capacitive loads at high frequencies can be supported by paralleling two adjacent SC35XX outputs;

6) Be generous with switching noise decoupling capacitors at the two or four sides of the SC35XX drivers, between the +Vcc and ground planes. AMCC recommends a pair of 0.1μF ceramic and 5.0μF tantalum capacitors at each or opposing sides of the SC35XX package.

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APPENDIX - A

Crystal Controlled Oscillator Suppliers

MONITOR PRODUCTS, Oceanside, CA	619-433-4510
CTS, KNIGHTS DIVISION, Sandwich, IL	815-786-8411
ECLIPTEK, Fountain Valley, CA	714-963-4009
SARONIX, Palo Alto, CA	800-227-8974
STANDARD CRYSTAL, El Monte, CA	800-423-4578
CONNOR-WINFIELD, Aurora, IL	708-851-4722
ANDERSON ELECTRIC, Holidaysburg, PA	814-695-4428
CHAMPION TECHNOLOGIES, Franklin Park, IL	708-451-1000

APPENDIX-B

P.C. Board Transmission Line Equations

The characteristic impedance and propagation delay for printed circuit board traces are functions of the board material, physical board layout and board topology. Please refer to Figure 1 for referenced dimensions.

The following calculations assume G-10 glass-epoxy board material with an Er = 4.7:

CHARACTERISTIC IMPEDANCE

$Zo = (Lo/Co)^{1/2}$

PROPAGATION DELAY

$Tpd = (Lo*Co)^{1/2}$ pS/inch, if units are in inches

MICROSTRIP TECHNOLOGY

$Zo = 35.2Ln[(6*h)/(0.8*w+t)]$

STRIPLINE TECHNOLOGY

$Zo = 27.7*Ln[(1.9*b)/(0.8*w+t)]$

7

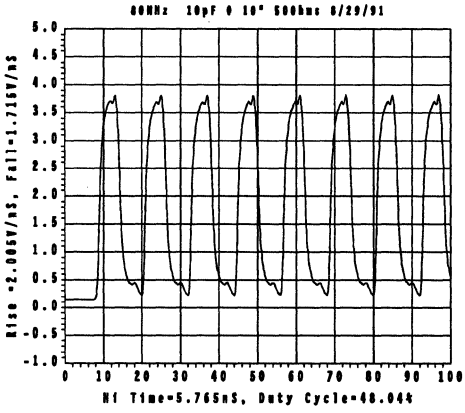
APPENDIX-C

Spice Simulation of Output Waveforms

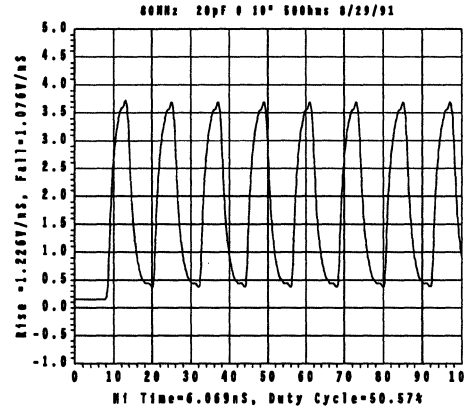
Modeled Frequency - 80MHz

(X-Axis is in ns)

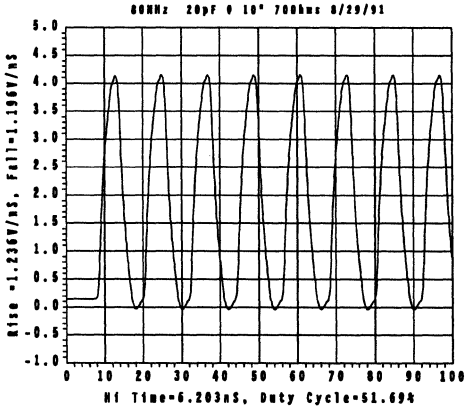
10 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



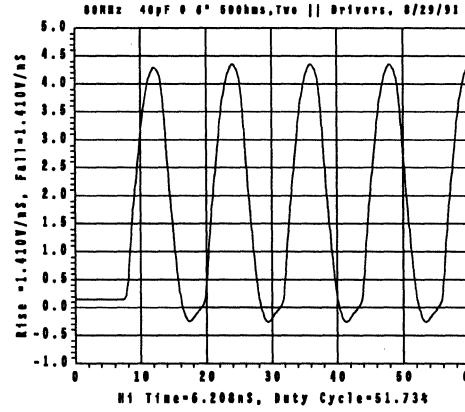
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel



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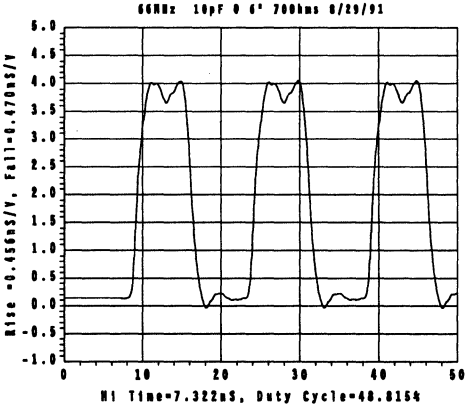
APPENDIX-C

Spice Simulation of Output Waveforms

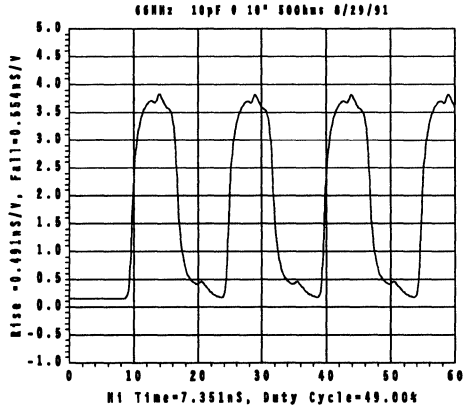
Modeled Frequency - 66MHz

(X-Axis is in ns)

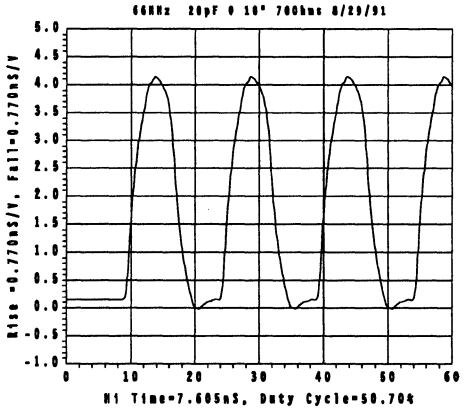
10 pF Load with 6" of Trace (Zo=70Ω)
Single Driver



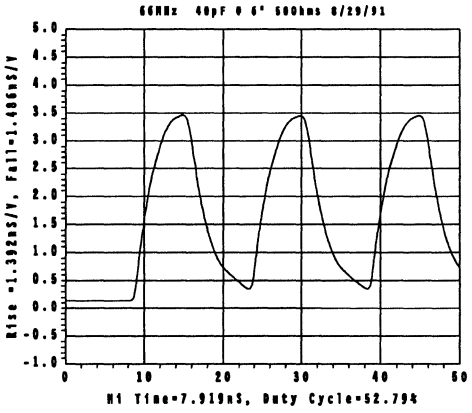
10 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel



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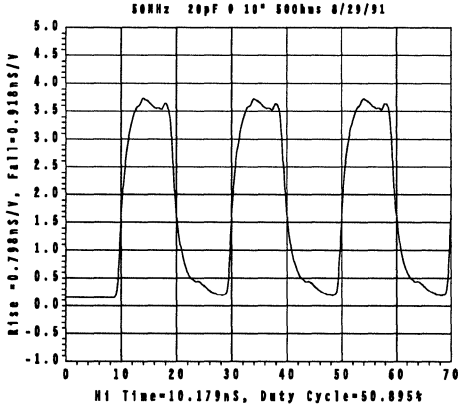
APPENDIX-C

Spice Simulation of Output Waveforms

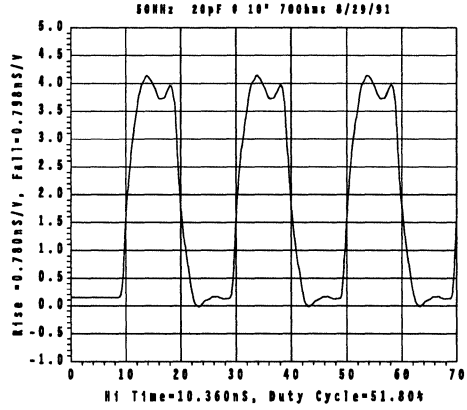
Modeled Frequency - 50MHz

(X-Axis is in ns)

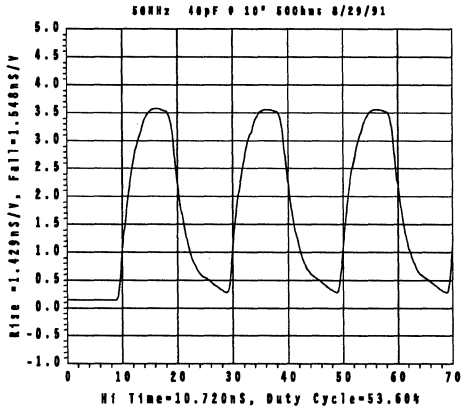
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



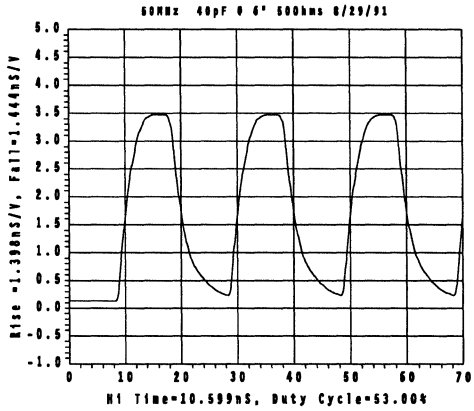
20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel



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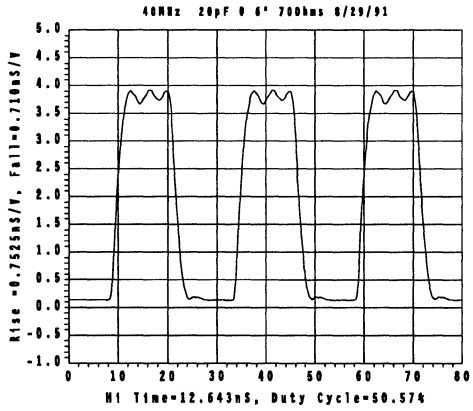
APPENDIX-C

Spice Simulation of Output Waveforms

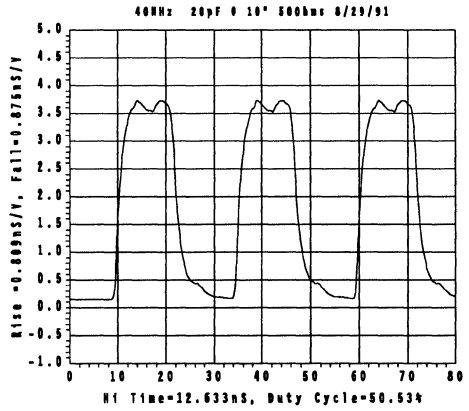
Modeled Frequency - 40MHz

(X-Axis is in ns)

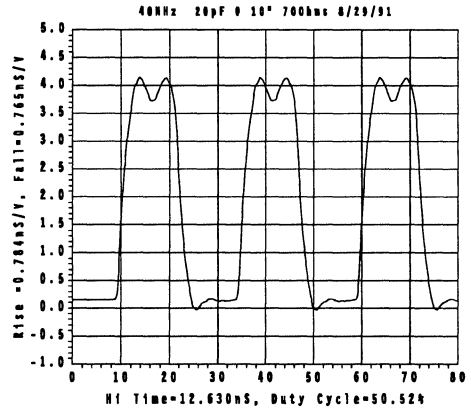
20 pF Load with 6" of Trace (Zo=70Ω)
Single Driver



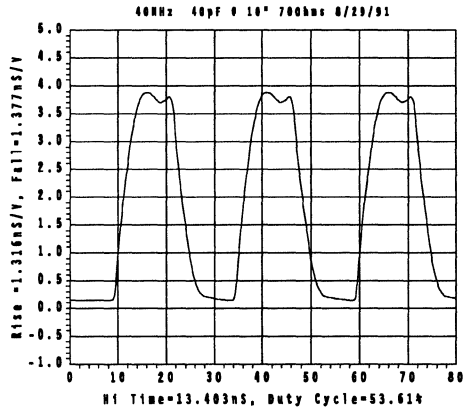
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



7

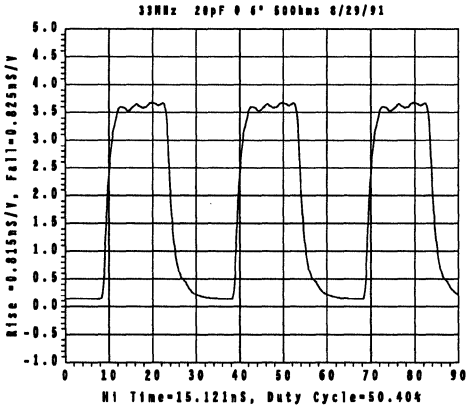
APPENDIX-C

Spice Simulation of Output Waveforms

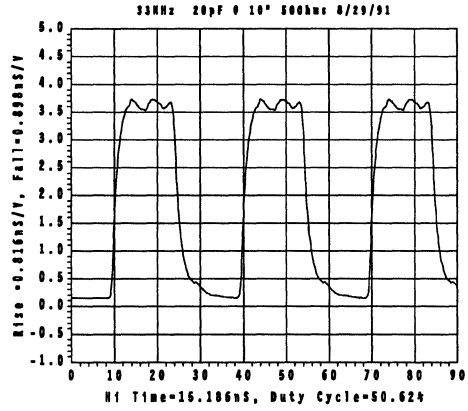
Modeled Frequency - 33MHz

(X-Axis is in ns)

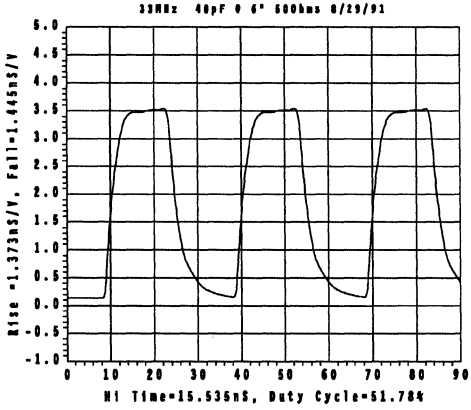
20 pF Load with 6" of Trace (Zo=50Ω)
Single Driver



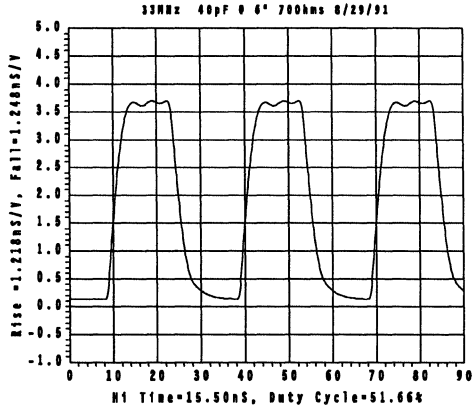
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=70Ω)
Single Driver



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INTRODUCTION

As today's personal computers (PC) and systems push into the 50Mhz realm and beyond, the minimization of system clock skew becomes more important. Clock skew eats into the effective clock period that is available to perform other tasks. Using generic driver chips and careful board layout, current systems can achieve about 4ns of system clock skew. A 4ns clock skew at 25Mhz is 10% of the clock period, while at 66Mhz this same 4ns skew eats up 26% of the system clock period. At 50Mhz and higher, the allowable clock skew is approximately 2ns - 3ns. Clearly this requires a new method of clock generation and distribution.

The key to the reduction of clock skew lies in the development of PLL clock generators, low skew clock drivers, and understanding how to distribute and route the clock signals.

The S4402/S4403 use AMCC's 1.0 micron BiCMOS technology to generate 10 - 80Mhz multiphase TTL clocks with less than +/-200ps of skew. The S4402 offers 6 output drivers, four at the primary output frequency, one at two times the primary frequency, and one at half the primary frequency. The S4403 offers 10 output drivers: four pairs at the primary output frequency, one at twice the primary frequency, and one at half the primary frequency.

The phase relationships between the outputs are programmable. Four different output configurations are available to provide synchronous outputs, quadrature phase delay outputs, minimum phase delay outputs, and a mixture of minimum and quadrature phase delay outputs.

The times-two output and the half frequency output, allow the S4402/03 to multiply and divide the reference clock input for distribution to the system clock loads. This feature is very useful to eliminate the EMI problems of distributing high frequency clocks across the entire system.

PLL CLOCK GENERATOR OVERVIEW

The basic concepts of phase-locked loops are fairly simple. The diagram in Figure 1 shows the fundamental blocks of the S4402/03 PLL. The task of the PLL is to minimize the frequency and phase differences between the reference clock input (REFCLK) and the feedback clock input (FBCLK). In this case, the PLL clock generator can be considered a "zero delay" clock buffer.

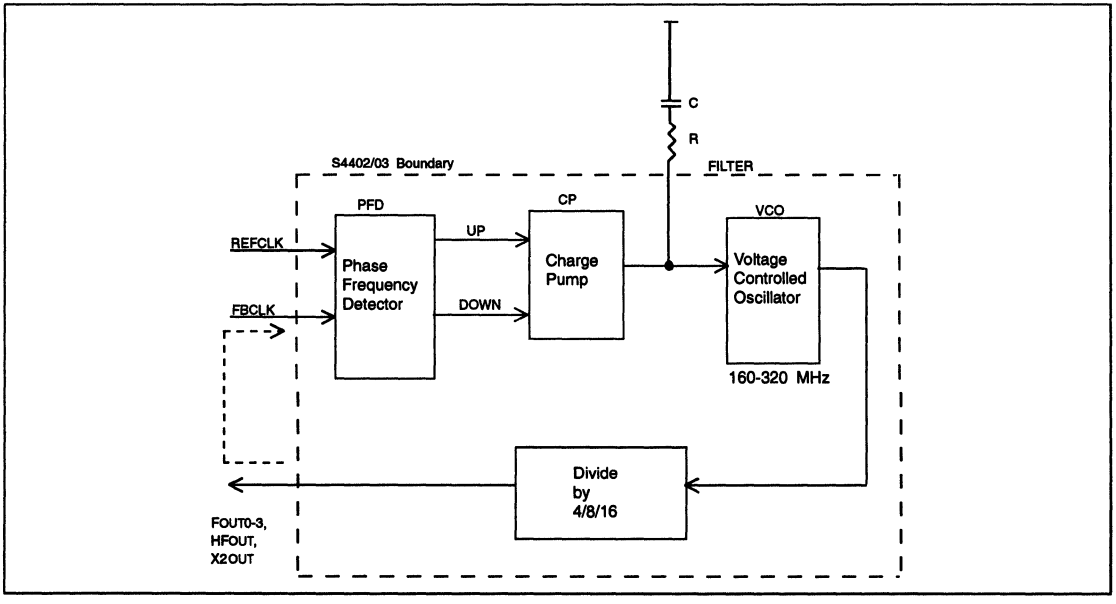

Figure 1 - Phase-Locked Loop of S4402/03

The Phase Frequency Detector (PFD) compares the reference and feedback clocks and provides a signal to the Charge Pump (CP) that tells the charge pump to increase or decrease the voltage into the Voltage Controlled Oscillator (VCO). This in turn increases or decreases the oscillator frequency, thereby changing the frequency or phase of the feedback clock.

The CP converts the digital signals from the PFD into a change in voltage at the external filter pin. This change in voltage is supplied to the VCO input. The CP can provide very small changes in the VCO control voltage that will modify the phase of the VCO output, or it can provide larger changes in the control voltage to change the VCO frequency.

The VCO simply responds to the control voltage at its input and generates an output clock frequency which is proportional to the voltage at its input. This high frequency clock signal goes into the internal logic of the S4402/03 and is divided by four, eight, or sixteen before appearing at the various chip outputs.

By selecting one of the S4402/03 outputs as the feedback clock, the loop is closed, and the internal PLL will try to make the rising edge of the output connected to the feedback input line up with the rising edge of the reference clock input. Due to the closed loop nature of this action, delays between the reference clock output and the subsequent arrival of the feedback clock input can occur without causing the chip to lose lock. Therefore, an external buffer can be introduced into the loop, and an output from the buffer fed back to the feedback input. This provides a simple means of increasing the output drive capability of the S4402. Another option is to introduce an external counter into the loop, and connect an output from the counter into the feedback input. This allows the S4402/03 to accept a lower reference clock frequency.

The two most important specifications for PLL clock generators are phase error and output skew.

Phase error is defined as the delay between the reference input and the feedback input when the chip is locked. When an output is used to drive the feedback input, the phase error can also be specified as a propagation delay. The S4402/03 clock generators have a maximum phase error (across all temperatures, supply voltages, and frequencies) of 1.0ns. On a given chip there will be less than 1.0ns of delay between the REFCLK input and the FBCLK input. Furthermore, at a given frequency, temperature, and supply voltage, the maximum variation in phase error across all parts is less than 750ps. Plus, at a given frequency, the maximum variation in phase error across all parts, is less than 1.25ns, over any temperature and supply voltage difference. These are important specifications in determining total system clock skew.

Output skew is defined as the delay between synchronous outputs. The S4402/03 clock generators have a maximum output skew of +/- 200ps. This means that with equal loading, all the rising outputs will switch within 400ps of each other.

CLOCK DISTRIBUTION ON A BOARD

The first few system clock skew examples are based upon the idea that all the clock loads are located within a single board.

The simplest configurations are that of a single S4402/03 or of multiple S4402/03s in parallel being driven from a single reference source. In Figure 2 the clock generators C1 and C2 are driven from the same crystal oscillator output. The clock skew associated with a single clock generator, such as C1 by itself, is simply the output skew specification of 400ps (+/- 200ps max.).

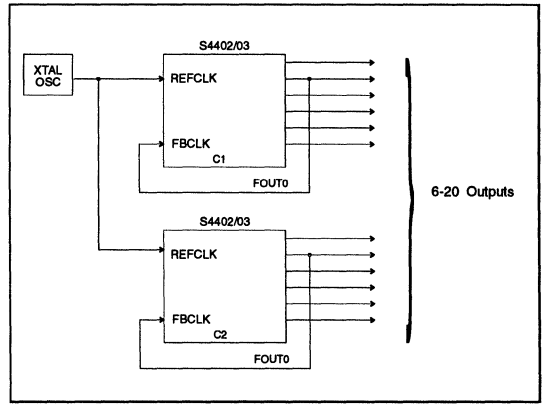

Figure 2 - Clock Distribution on a Board

In the case where the output from the crystal oscillator drives no additional chips on the board, except the clock generators, the total clock skew across all the S4402/03s can be calculated as:

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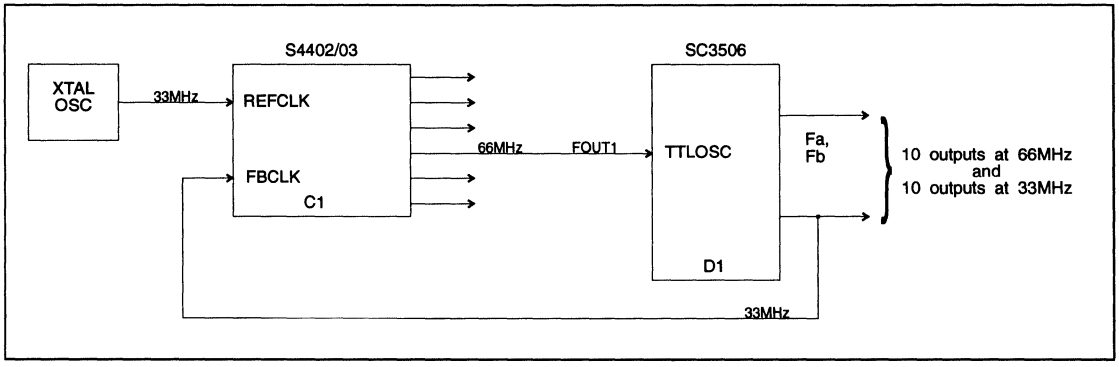

Figure 3 - Clock Distribution on a Board: S4402 with an SC3506

Total skew = Tpev + Tskew
= 750ps + 400ps
Total skew = 1.150ns (max.)

where,

Tpev = the maximum variation in phase error across all parts at a given frequency, temperature, and supply voltage.

Tskew = the maximum output skew on any part.

In this first example, the total clock skew across C1 and C2 depends upon the phase error and the output skew of each chip. Rather than use the total range of phase error for all possible frequencies, temperatures, and supply voltages, this configuration allows the use of the chip to chip variation in phase error. This is possible because the clock generators will be placed close to the crystal oscillator, and therefore experience the same temperature and power supply environment.

The second example, in Figure 3, shows the use of an S4402 clock generator to multiply the 33Mhz crystal oscillator output up to 66Mhz before applying it to the input of the SC3506 clock driver. This is accomplished by feeding back one of the divide-by-two outputs of the SC3506 to the FBCLK input of the S4402/03. This configuration allows the use of a slower crystal oscillator to generate 10 outputs at 66Mhz and 10 outputs at 33Mhz.

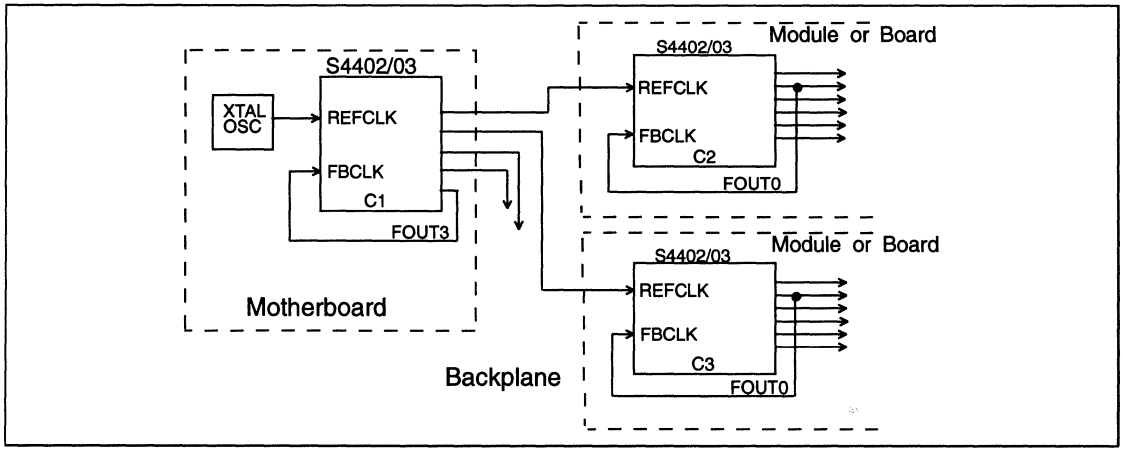

Figure 4 - Clock Distribution Between Boards

Because the output of the SC3506 is fed back to the FBCLK input of the S4402, the delay through the SC3506 is not important in the calculation of the total output clock skew. The total output clock skew is determined solely by the output skew specification of the SC3506, and is therefore, less than 500ps (max.) for the SC3506-1.

CLOCK DISTRIBUTION BETWEEN BOARDS

Most systems do not consist of a single board containing all the computing, memory, I/O, and display functions. A typical system configuration would likely have a central board that ties the system together (the motherboard), and a series of additional modules or expansion boards, that allow the user to update and upgrade the system.

Ideally, the master clock needs to be distributed to the synchronous logic on the motherboard, and each of the expansion boards, with no skew.

Figure 4 shows a configuration using an S4402/03 to distribute the master clock to the motherboard and the expansion boards. On each board or module, the master clock copy is received by another S4402/03, and distributed to the rest of the board.

The maximum clock skew between the motherboard clocks (outputs of C1) and the module clocks (outputs of C2 and C3) can be calculated as:

C1-to-C2 skew = Tskew(C1)
+ Tpemax(C2)
+ Tskew(C2)

= 400ps
+ 1.0ns
+ 400ps

C1-to-C2 skew = 1.80ns (max.),

where,

Tpemax(C2) = the maximum absolute value of phase error for C2.

Tskew(C1 or C2) = the maximum output skew for each chip.

The total system skew will be determined by the maximum skew across all the modules. This total system skew can be calculated, using the results of the C1-to-C2 skew calculation, as:

Total skew = C1-to-C2skew(max.)
- C1-to-C3skew(max.)

= 1.80ns
- C1-to-C3skew(max.)

C1-to-C3skew = Tpevfmin(C3)
+ Tskew(C3)

= [Tpemax(C3)
- Tpevf]
+ Tskew(C3)

= [1.0ns - 1.25ns]
+ -400ps

C1-to-C3skew = -650ps (max.)

Total skew = 1.80ns - [-650ps]

Total skew = 2.45ns (max.)

where,

Tpevf = the maximum chip to chip variation in phase error at a given frequency, across all temperatures and supply voltages.

Tpevfmin(C3) = the most negative phase error of C3 versus C2, based upon a Tpevf variation between C2 and C3.

In this calculation, the objective is to determine the widest variation in output skew between the C2 and C3 clock generators. The calculations make use of the fact that at a given frequency, but with unequal temperatures and supply voltages, the maximum variation in phase error between any two parts is less than 1.25ns. This specification is used to make the maximum skew variation of C3 versus C1 be -650ps, when the maximum skew variation of C2 versus C1 is 1.80ns. With this, the maximum size of the output switching window around C1 is equal to 2.45ns.

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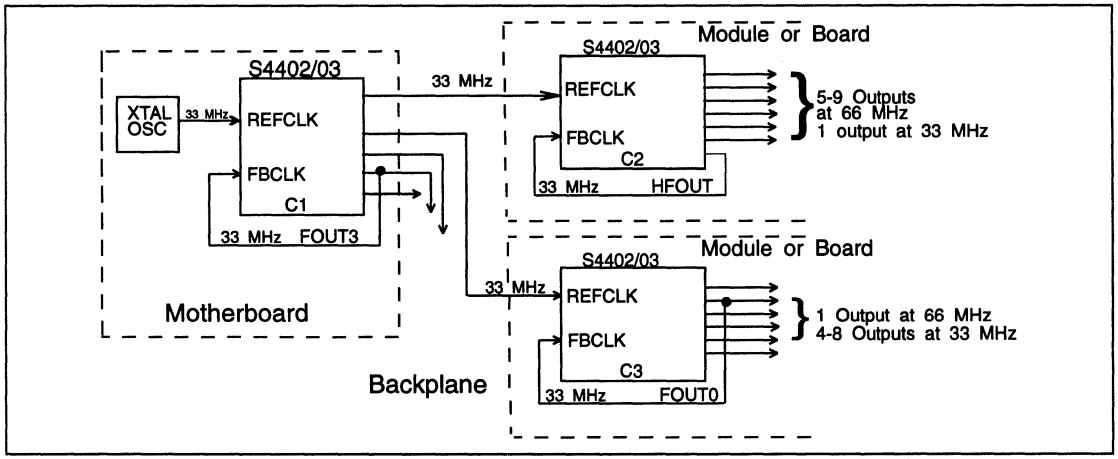

Figure 5 - Clock Dividing and Multiplication for Distribution Between Boards

Figure 5 shows the use of the S4402/03 as a clock multiplier and divider in a board to board clock distribution scheme. In this example, the motherboard clock generator, C1, is used to distribute multiple copies of the crystal oscillator frequency of 33Mhz. These 33Mhz outputs are routed point to point down the backplane to each of the expansion boards or modules. In this manner, it is possible to route slower frequency outputs on the backplane, and reduce the crosstalk, signal noise, and EMI problems.

The S4402/03 chip on each module can be programmed to multiply the 33Mhz backplane clock signal to its previous 66Mhz value, or it can create a set of 33Mhz clock outputs. With this technique, each module or board can be selectively operated at the crystal oscillator frequency, 2X that frequency, or 1/2 the oscillator frequency.

In this application, the total system clock skew is also 2.45ns. The calculation of system clock skew in this example is the same as that for the previous example.

Figure 6 shows a special application of the S4402/03. In this application, data is to be synchronously transferred between boards in the system. The difficulty arises from the fact that in a system, the data delay from one board to the next varies depending upon location. This delay uncertainty, and the total system clock skew, combine to make the job of providing sufficient hold time, at the input register on each board, a difficult task.

For this example, assume the system reference clock on each board is generated by an S4402/03 that is located in a central location, typically the motherboard. From a previous example (Figure 5), this gives a total system clock skew of 2.45ns.

Based upon this 2.45ns clock skew, a scenario can be drawn in which the data that is clocked out from one board reaches its neighbor before the neighboring card has stored the previous data into the input register with sufficient hold time. A solution to this problem is to delay the time at which data is clocked out of all the boards.

In this solution, the data is clocked into each input register, on a clock edge that is synchronous with the system reference clock. A short time later (3-6ns), new data is clocked out onto the backplane data bus. This will provide sufficient hold time at each board, provided that the delay between the two register clocks is at least equal to the system clock skew plus the hold time of the input register.

The example in Figure 6 uses registers with a hold specification between 0.5ns and 1.3ns. Based on these values, the delay between the register clocks on each board must be at least 2.95ns to 3.75ns. In the minimum phase mode of operation, the S4402/03 can be configured to provide 3.75ns delays between output clocks at 33Mhz, and is an ideal solution for this problem. FOUT0 is synchronous to the system reference clock, and is used to clock the input registers R1 and R3. FOUT1 is delayed from FOUT0 by 3.75ns, and is used to clock the output registers R2

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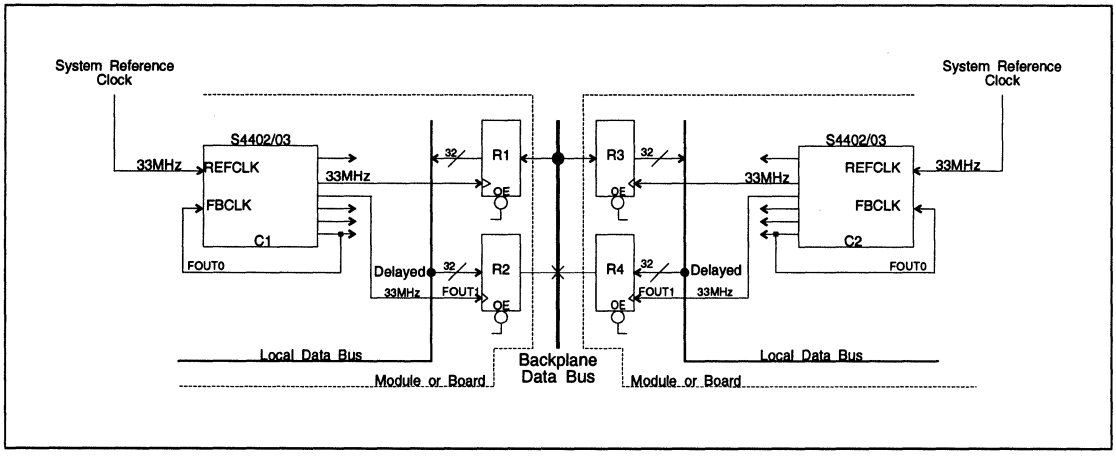

Figure 6 - Data Distribution Between Boards

and R4. If additional delay is necessary, FOUT2 could replace FOUT1, and provide 7.5ns of delay between FOUT0 and FOUT2.

ASIC DESKEWING

In systems where there are multiple ASICs sharing a common synchronous bus, great care must be taken to ensure that data transfers on the bus can happen as rapidly as possible. Each ASIC must be simulated to ensure that it's data setup, hold, and clock to data output times will work with each of the other chips. The designer must assume that each of the ASICs could be operating at any point on its performance curve; therefore, the propagation delays, setup, and hold times are increased to compensate for the variability of each of the ASICs. These increased specifications for each ASIC reduce the maximum attainable performance of the data bus by consuming a portion of the bus cycle time.

Figure 7 demonstrates a couple of ways to reduce the uncertainty of each ASIC's performance. In this figure, an S4402/03 is used to ensure that the output transitions of each ASIC occur synchronously to the system clock. If all the output transitions on the data bus occur at the same point in time, then the setup times for each ASIC can be minimized. With the clock to data output delays effectively reduced to zero, and the setup and hold times minimized, the available bus bandwidth is increased and data traffic can flow at a higher rate.

In the upper half, C1 takes a 25Mhz master clock and generates a 50Mhz clock for the ASIC A1. This 50Mhz clock is buffered through the ASIC's internal clock buffer tree, before clocking a divide by two output flip flop. This 25Mhz output clock is fed back to the S4402/03 chip and the rising edge of this signal is aligned to the rising edge of the 25Mhz master clock.

In the lower half, C2 takes the 25Mhz master clock and generates two 25Mhz outputs that are in quadrature (90 degrees out of phase with each other).

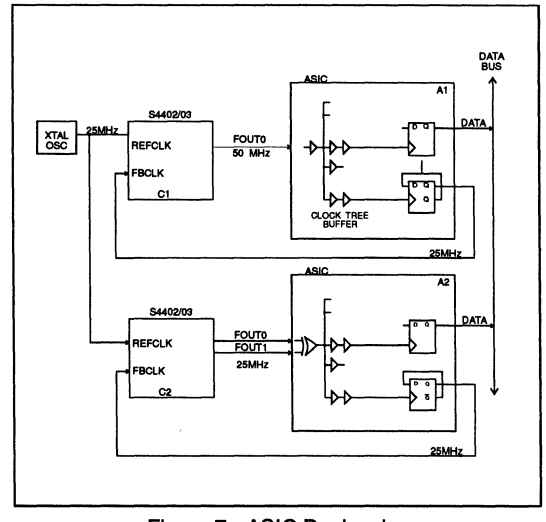

Figure 7 - ASIC Deskewing

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These 25MHz clocks are exclusive OR'ed inside the ASIC to create the 50MHz internal clock for the ASIC. This 50MHz internal clock is again buffered in the same way as the rest of the ASIC clocks, and then divided by two at the same output, and aligned with the 25MHz master clock.

For these two schemes to work correctly, the designer must do three things. The ASIC internal clock buffering must be matched. In other words, the delay from the point at which the buffer tree begins to expand sideways, to the point at which the clocks arrive at the clock input to the output flip flops, must be equal. The output flip flop macros and the delay from the flip flop output to the external pins, must also be equal. And the interconnect length between the ASICs and the S4402/03s must be minimized and equal.

GENERAL GUIDELINES FOR CLOCK DISTRIBUTION

For all of the examples described previously, there are a number of general design guidelines that need to be applied in order to achieve the best performance. These guidelines are:

1. Clock traces need to have equal lengths and impedance.
2. The clock traces must be treated as transmission lines, and therefore use controlled impedance traces.
3. The clock signal termination strategy must be decided early. Series termination will reduce the termination power requirement, but the loads must be clustered at the end of the clock line (<2" stubs).
4. Clock signal capacitive loads must be equal.
5. Do not heavily load the clock output drivers. With heavy loads, two outputs can be paralleled to increase the drive capability.
6. Clocks distributed across backplanes should be point to point connections. This will remove the transit time skew introduced as the signal propagates down the backplane past each board.
7. Be generous with decoupling capacitors. Each power and ground pin of the generators and drivers should be decoupled with 0.1uF ceramic chip capacitors.

SUMMARY

As shown, with careful design of the clocking scheme for a synchronous system, and the correct choice of clock generators and drivers, it is possible to reduce the system clock skew down to 0.4ns to 2.45ns.

The S4402/03 clock generator chips provide the user with the option to tackle the clock distribution problem in many different ways. The controlled output skew of less than 400ps, and the ability to generate clocks at frequencies up to 80Mhz, make the S4402 and S4403 the ideal choice for today's high performance systems.

NOTES

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Clock Design in Intel Pentium™ Processor Systems using the SC3508

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1. INTRODUCTION

The Pentium processor is the latest, high-performance entry in the X86 microprocessor family from Intel. There are 60- and 66-MHz versions. It operates on 64-bit data in two instruction pipelines with instruction prefetching and branch prediction. There is also on-board floating-point processing, as well as sophisticated data and instruction caching. These are all structural elements that, until very recently, were found exclusively in main-frame and supercomputer designs.

At the hardware level, Pentium designs also have a good deal in common with larger computer system designs. For example, the tighter timing margins and the higher clock and edge speeds of Pentium designs dictate the careful application of high-speed digital design methods. This includes employing design methods which preserve the fidelity of the clock pulse and effectively manage the tolerances present in the circuitry which distributes or receives the system clock.

The purpose of this application note is to clearly illustrate an approach to the design of the system clock for the Pentium using the AMCC SC3508. We will methodically work through a simple but representative example. In doing so, we will identify the important design decisions encountered in the design of a correctly timed system, and show methods for resolving them.

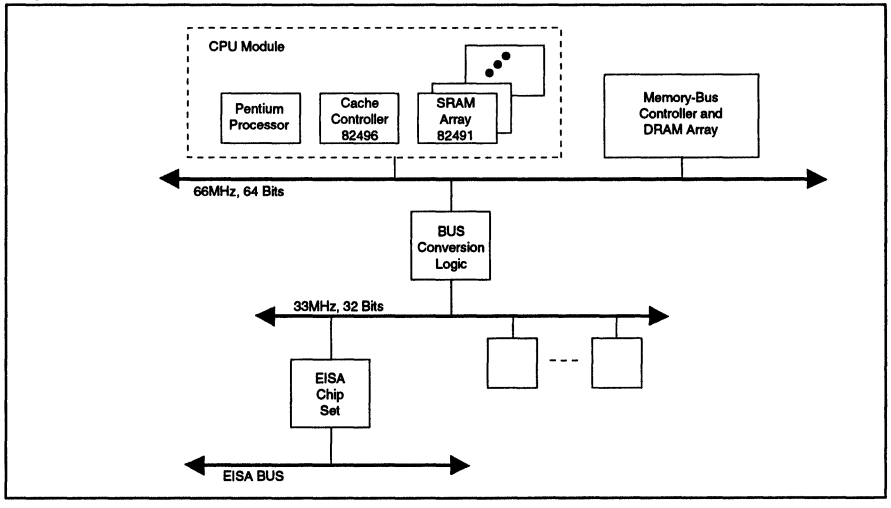
A Word About Specifications

In this document, we make use of a number of Pentium specifications. The reader is cautioned to verify any specifications with Intel prior to applying them, since they are all subject to change. It is also the responsibility of the designer to exercise sound engineering judgment to determine the suitability of how any particular specification or method is to be employed in his design.

2. DETERMINING YOUR DESIGN REQUIREMENTS

The first step in specifying the design of the clock for a Pentium, or any other system, is to clearly define what the design requirements are. Some of these will come from Intel specifications while others will be determined by aspects of the design, such as critical delay paths. In this section, we present some background on the

Figure 1.



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mechanisms we are trying to manage and how to quantify the impact of those mechanisms on the design.

2.1. Timing-Environment Design: Fundamentals

The fundamental goal for any timing environment design is the specification of a *statistically stable* design. That is, it is assumed that the elements from which each system will be assembled will have some statistical distribution on their characteristic parameters (in our case, delay). Since many copies of the design will be fabricated, we must employ design methods which recognize this tolerancing and which ensure that every clock signal in each machine built arrives within the time interval predicted at design-time.

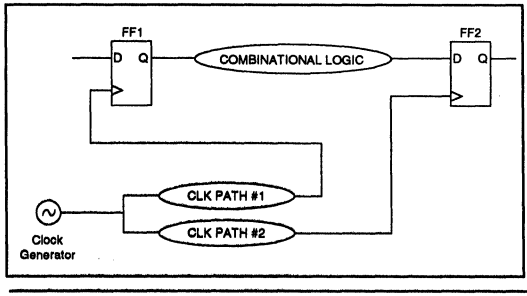
2.1.1. Basic Requirement on Clock-Arrival Time

We will use Figure 2, which shows a critical path, to illustrate the tolerancing effects we are concerned with controlling. Given that the two clock paths are built from components which have some statistical delay distribution, we can describe two pathological situations:

1. Clock-path 1 is slower than anticipated
2. Clock-path 2 is faster than anticipated

For the first case, FF1 is clocked late causing the data to arrive at FF2 after FF2 samples its input. The result is that the data is missed or the flip-flop enters a metastable state. The second case results in an equivalent situation by again clocking FF2 early relative to the arriving data. We can see from this simple example that any mechanism which causes the delay of a clock path to vary by more than the designer anticipated can result in a failure. Notice that it is *delay variation,* rather than the magnitude of the delay that results in timing failures.

Figure 2.



2.1.2. Basic Clock-Tolerancing Mechanisms

As we just saw, we must manage anything which can result in unequal or inconsistent arrival times of the clock at the load. This equates to two important design tasks:

1. Precisely balance the mean delay along every path from the clock generator to the clock loads.
2. Anticipate and manage those mechanisms which tend to alter the delay along these paths.

The merit of balanced mean delays for all clock paths is illustrated by Figure 3. Since the worst-case tolerance is computed from the earliest and latest arrivals, balancing the mean delays moderates the impact of any statistical delay variations.

We will use Figure 4 to illustrate the various tolerancing mechanisms we are attempting to manage. The figure shows a clock-buffer driving a transmission-line which terminates at some clock-input. This circuit is representative of a complete clock path for many Pentium systems (i.e. one-level buffering). Given Pentium speeds (66-MHz clock rates and fast clock edge rates),

Figure 3.

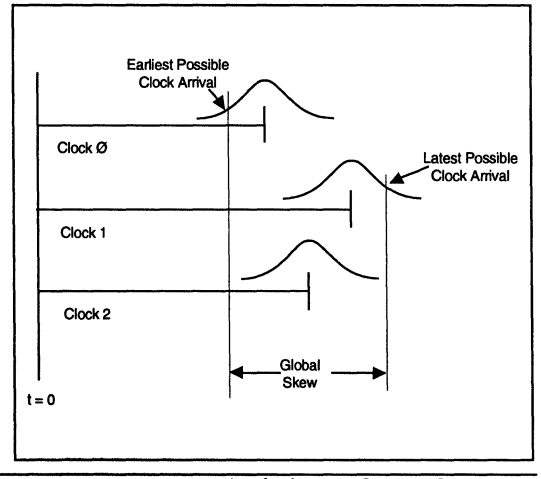


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Figure 4.

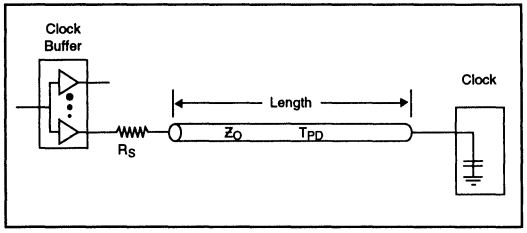
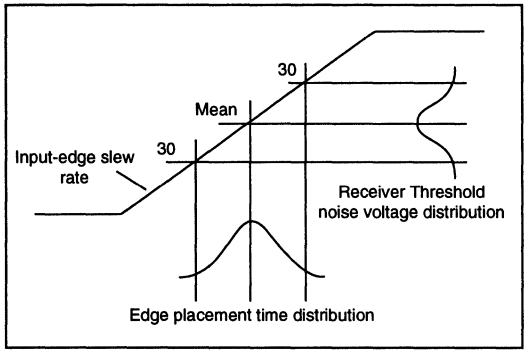


Figure 5.



a controlled-impedance interconnect is required. For this clock net, the expression for the variation in delay along the net is:

Tolerance = Intrinsic skew + Extrinsic skew + Jitter (1)

Where ,

Intrinsic Skew is the delay variation in the clock buffer. This is usually specified separately for part-to-part and pin-to-pin skew. Some clock buffers also specify skew within a group of clock-buffer outputs. Assuming a single-chip solution, we will use pin-to-pin.

Extrinsic Skew is delay variation attributable to effects in the interconnect.

Jitter is the cycle-to-cycle variation in the arrival-time of the clock. It is due primarily to noise in the power environment which, in turn, causes time-varying shifts in the input threshold of a device. The relationship between noise and edge-placement (jitter) is shown in Figure 5. For more information on jitter, see References 1 and 2.

Extrinsic skew is not a single mechanism. It is convenient to break it into three major components:

Extrinsic skew = ΔTOF + ΔDist_Del + MT (2)

Where,

ΔTOF is the **variation in the time of flight** of an undistorted signal. This is due primarily to variation in line lengths, and does not include additional delay variation attributable to edge degradation. This effect is addressed by equalizing all clock net lengths to that of the longest clock net.

ΔDist_Del is the **distortion-delay variation**. As a signal propagates, some of the high-end spectral content is attenuated. One prominent cause of this is the capacitance of the clock load. This results in a slower or degraded edge, and ultimately additional delay in reaching threshold voltage. Any variation in edge degradation (e.g. ΔC_L) results in a variation in delay. This is ΔDist_Del.

MT is the **manufacturing tolerance** on the delay. It ranges from one's of psec/in to mid-10's of psec/in.

The expression can be rewritten as:

Tolerance = Int skew + ΔTOF + ΔDist_Del + MT + Jitter (3)

From transmission-line theory, we know that the propagation rate of a loaded transmission-line is:

$$T_{PD}' = T_{PD}\sqrt{1 + C_L/(L * C_0)} \quad (4)$$

Where,

- T_{PD} is the propagation rate of the unloaded transmission-line.
- C_L is the load capacitance (may be distributed)
- L is the length of the line
- C_0 is the intrinsic capacitance of the line

And the delay (time of flight plus distortion-delay) of a loaded transmission-line is simply:

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$$LT_{PD}' = L*T_{PD}\sqrt{1 + C_L/(L * C_0)} \quad (5)$$

If we know the minimum and maximum values for C_L, we can compute the min and max delays for a given lossless transmission line (exclusive of manufacturing tolerances).

$$\Delta LT_{PD}' = L*T_{PD}(\sqrt{1 + C_{Lmax}/(L * C_0)} - \sqrt{1 + C_{Lmin}/(L * C_0)}) \quad (6)$$

And we can use the difference in these values to replace the second and third terms in expression (3):

$$\text{Tolerance} = \text{Int skew} + \Delta LT_{PD}' + \text{MT} + \text{Jitter} \quad (7)$$

We will use this expression to compute the tolerancing of various "tolerance groups" later in the example. One very important effect to note is that the preceding expression implies that clustering loads which have non-trivial load-capacitance variation on a single clock net will drive the $\Delta LT_{PD}'$ factor up and thus the overall tolerance.

2.1.3. Design Flow/Approach

There are a variety of approaches one can take:

Clocks first - Specify in detail the clock distribution and use resultant tolerances to compute delay margins on critical paths (Tcyc-Ttol = max Tpath).

Critical paths first - Design critical paths and use the resultant maximum delays to compute timing margins (Tcyc-Tpath=Ttol).

Most designers will take an approach that iterates between both styles, ensuring that both the timing and path delays are equally prioritized. In our example design, we are starting with critical-path information to determine timing margins, and then using the margin information to establish constraints on critical-path parameters (e.g. allowable load-capacitance variation on external loads). In detail, our decision-flow is as follows:

1. Determine allowable tolerances in CPU module.
2. Use critical path information to determine allowable clock tolerance (i.e. margin) on external loads.
3. From an inventory of clock loads, determine your slowest clock path in the system.
4. Starting with your tightest tolerance group (Pentium-82496), begin designing clock nets. Make each net approximately as long as that of the slowest path (previous step). As you progress through other tolerance groups, ensure you balance the mean delays.
5. From the unused margin for each group, develop constraints for each of the following:
   - Jitter
   - Manufacturing tolerances on net delays
   - Load-capacitance variation

Three-Level Tolerance Specifications

The Pentium specification dictates tolerances within the CPU module at three voltage levels (0.8, 1.5, and 2.0V). This was most likely done to combine tolerance management and pulse-fidelity into a common specification. However, designing for minimum tolerancing at multiple voltage levels can be very difficult. For clarity, we will design for minimum tolerancing at 1.5V and employ methods which ensure good pulse fidelity. This will ensure that the tolerances are satisfied at all three levels.

2.2. Specific Pentium System Design Requirements

The degree of difficulty for any timing-environment design is derivable from two aspects of the design — the number of board-level clock loads and the fraction of the cycle time allocated to clock tolerancing. Broadly speaking, a design becomes challenging when the number of loads exceeds 10 and the total tolerancing is restricted to 10 to 15% of the cycle time.

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For Pentium systems, the number of board-level clock loads varies according to the complexity of the design. For the most basic designs, the number of loads will be four to eight, primarily the Pentium processor and memory-bus controller. For very sophisticated designs (e.g. large server systems), with a second-level cache, as well as controllers for large interleaved memories and other synchronous devices, the number of board-level clock loads can exceed forty or more.

A typical 66-MHz design with a second-level cache will have 12 clock loads in the CPU module plus more loads for the memory bus controller (MBC) and other logic such as bus conversion. Therefore, depending upon how the MBC, etc. are implemented, a typical 66-MHz design will have 15 to 20 clock consumers.

The small fraction of the period alloted for tolerancing qualifies Pentium designs as quite challenging. At 66-MHz, the cycle time is 15 nsec. Clock tolerances within the CPU module are either 200 or 700 psec, and those external to it vary depending upon critical path delays to/from devices external to the CPU module. Stated another way, the tolerances within the CPU module are 1.3% and 4.7% of the cycle time.

For the rest of this section, we determine the various tolerances in a 66-MHz Pentium system with a second-level cache. The design requirements are configuration-specific and best considered in tolerance groups.

There are very few explicit clock requirements in the basic Pentium specification. Only clock stability (jitter) and pulse fidelity are specified.

Clock Stability (Jitter) - The Pentium clock must have a stability of better than +/- 250 psec. There are many metrics of frequency stability. While it does not explicitly state so, this specification refers to period-jitter. In a footnote to the specification, the distribution of the jitter in the jitter frequency spectrum excludes any peaking between 500kHz and 1/3 of the clock frequency (repetition rate).

Pulse Fidelity - The Pentium clock signal operates at TTL levels. The clock waveform must remain at the high and low levels for a minimum of 4 nsec, and the transition times must be less than 1.5 nsec. The Pentium specification dictates other clock waveform parameters beyond these. The reader is referred to the specification for complete information.

2.2.2. CPU Module

There are four possible configurations for the "CPU module". They are summarized in the following table.

Clock Speed (MHz)	Cache Size	Tolerance (psec)	Number of Loads
60 or 66	None	N/A	1 (CPU only)
66	256K	700	12 CPU, cache control, 10 SRAM
60	512K	800	20 CPU, cache control, 18 SRAM
60	256K	800	12 CPU, cache control, 10 SRAM

Layout Considerations Within CPU Module

There are flight-time specifications for various signal groups within the CPU module. For example:

Pentium - 82496: Only max flight times are specified (1.6 nsec is smallest value).

Pentium - 82491: Min and max flight times are specified (1 - 2.2 nsec range for 66-MHz).

These fight-times are critical, and it is likely that they will drive the placement of devices within the CPU module. That placement, in turn, will interact with clock tolerancing within the CPU module, since the distances from the clock driver to the clock loads determine certain tolerancing components. Specifically, interconnect tolerancing increases with the length of the

7

clock nets. For our example, we will use the configuration for the layout of the CPU module found in the Intel Pentium clock application note (Reference 8). There may be another approach (e.g. locating the clock driver in the center) that results in additional timing margin.

Pentium-82496 Tolerance Group: Two Loads at 200 psec Tolerance

This requirement is very tight and essentially unheard of in microprocessor systems. To meet this specification, both loads must be driven by the same pin of clock buffer. This eliminates the intrinsic skew component of the tolerance. By locating the Pentium and 82496 clock pins close to each other, and moving the branching point to the end of the transmission line (versus stubbing into two lines near the clock buffer), it is possible to minimize the manufacturing tolerance. The 200 psec tolerance thus splits between jitter and arrival time variation due to load capacitance variation.

Are there two different jitter specifications for the Pentium?

There can be some confusion in systems with second-level caches, since there appear to be two conflicting jitter specifications. This, however, is not the case:

> The Pentium clock specification states that the maximum allowable instability (jitter) on the clock to the Pentium processor is +/- 250 psec. Further restrictions as to how this energy can distribute across the jitter spectrum are also specified in a footnote.
>
> When the Intel CPU-Cache chip set is employed, the maximum tolerance between the clock signals driving the Pentium and the 82496 is limited to 200 psec. That is, for systems with second level-caches, the sum of the skew and the jitter between the clock signals driving the cache controller and the Pentium must be less than 200 psec.

Actually, there is no conflict in these specifications once you determine what they represent. The former jitter specification (+/- 250 psec) is established by the timing requirements of segments 100% internal to the Pentium. Any displacements larger than 250 psec run the risk of an internal Pentium timing failure. Furthermore, the requirements on the jitter spectrum are in place to prevent stimulating the resonant frequency of the loop filter in the internal PLL clock receiver. When jitter causes the PLL loop-filter to resonate, the signal out of the PLL (i.e. the internal clock) has more jitter on it than the signal driving into the PLL (i.e. the Pentium clock input), and is possibly larger than acceptable.

The latter specification (200 psec) governs the timing of segments between the Pentium and the 82496. When that specification is violated, timing failure on one of the paths which span both chips is likely.

How do you use this information?

In systems without second-level caching, the latter specification(200 psec) does not apply. Assuming there is sufficient margin on all paths external to the Pentium, system jitter must be less than +/- 250 psec and distributed in the jitter spectrum as specified in the footnote.

In systems with second-level caching, the 200 psec specification sets the upper limit on the jitter amplitude (jitter < 200 psec - Pentium/82496 skew). Furthermore, the jitter must distribute through the jitter spectrum as specified in the Pentium clock specification.

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Pentium-82491 & 82496-82491 Tolerance Groups: 10 SRAM (+2) Loads at 700 psec Tolerance

This group has many more clock loads, which necessitates driving the group by more than one pin of the clock buffer. Much of the margin obtained by increasing the tolerance specification to 700 psec is absorbed by the increased intrinsic skew. There will also be a more significant manufacturing tolerance contribution, since the SRAMs are more widely dispersed on the board and there will be more inches of interconnect in the clock nets that drive them.

Since we are forced to increase the intrinsic skew term of the total tolerance in this group, we want to use a point-to-point scheme (1 load/net). This reduces the range of load-capacitance variation and minimizes the ΔLT_{PD}'.

2.2.3. External Tolerance Groups

There will also be clock consumers external to the CPU module. In more complex Pentium designs, the number of loads in the external tolerance group can be several times the number of loads within the CPU module. The primary external clock loading will be in the memory bus controller (MBC). The tolerance requirements of this group will be dictated by the critical paths in this part of the design. Shortly, we will provide a simple example of computing that tolerance.

The majority of logic external to the CPU module is treated as memory. From a timing perspective, there are three distinct ways in which system memory can be configured:

1. Fully Synchronous
2. Divided Synchronous
3. Asynchronous

This impacts the clock as follows:

Fully synchronous systems: All clock inputs driven at 66-MHz

Divided-synchronous systems: All clock inputs in CPU module driven at 66-MHz, the memory-bus controller driven by both 66- and 33-MHz clocks, and all external devices driven by a 33-MHz clock.

Asynchronous systems: The CPU module and part of the MBC driven by 66-MHz clocks. A second, relatively-asynchronous clock (generated elsewhere in the system) drives part of the MBC and all external devices.

3. DESIGN EXAMPLE

3.1. Configuration

Our example system will be a fully synchronous 66-MHz system with a 256k second-level cache. It will use the Intel 82496 Cache Controller and 82491 Cache SRAMs. This configuration embodies many of the most challenging aspects of a Pentium clock design — the extremely tight tolerancing of the clocks within the CPU module, non-trivial load-capacitance variation, and determination of critical paths external to the CPU module. Furthermore, it will be extended to address other important design decisions — dual-frequency clocking and larger numbers of clock loads.

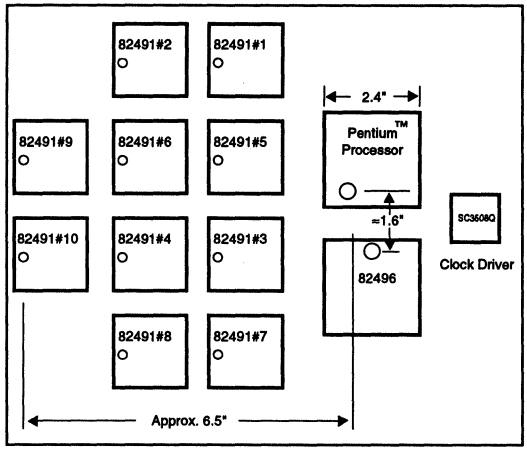
3.2. Preliminary Design Decisions

Before beginning to work through our example design, we will first describe some preliminary design decisions, and the impact they have on the system clock.

Clock-Buffer Selection - We are using an AMCC SC3508Q-1 clock buffer to drive the clock in this example. Our selection criteria for this part is based upon two factors. Specifically, that the SC3508Q-1 has twenty outputs and that the pin-to-pin skew for this part is less than 500 psec. In second-level cache systems, we have to drive 12 loads which have a non-trivial (relative to the tolerance requirement) amount of capacitive load variation. With 20 pins available from the SC3508Q-1, a single-IC point-to-point (i.e. one driver pin for each clock load) clock-distribution solution can be employed. If these loads had to be driven such that two or more SRAM inputs were clustered on a net, the arrival-time variation due to extrinsic skew and C_L effects (c.f. expressions 6 and 7) would exceed the allowed tolerance, even without factoring-in jitter.

Device Placement Within the CPU Module - We will use the placement suggested by Intel in Reference 8. Figure 6 shows that placement.

Figure 6.



Interconnect Environment - For our speeds and spectral content, we obviously need a controlled-impedance interconnect. The reader is referred to References 3 and 10 for detailed background information on this topic.

Microstrip vs stripline - We are routing all clock signals in microstrip, since the propagation rate is higher than that of stripline (146 psec/in for microstrip versus 182 psec/in for stripline). While the twenty or so clock nets may increase the level of radiated noise, the faster rates reduce the impact of interconnect manufacturing tolerances (5% of 146 is less than 5% of 182).

Parameters - Our example assumes a 70-ohm characteristic impedance. Higher values of Z_0 reduce the dynamic current available to charge the load capacitance. This, in turn, results in higher sensitivity to load capacitance variation. However, lower dynamic current also means less noise and therefore less jitter. The other parameters for our assumed interconnection environment follow.

Structure: Microstrip

Dielectric: 4.7 .012" thick

Conductor: .011" W x .0015"T copper

Properties:

C0 2.08 pF/in

L0 10.3 nH/in

Z0 70.4 ohms

Tpd 146.4 psec/in

Definition of External Loading and Tolerance - For any design, it is necessary determine the allowable clock tolerance on external critical paths. To do that, you have to identify the critical paths in the external circuitry. This may be quite difficult, given the large number of bus-transaction types, and that not all segments are 1-cycle long.

To simply illustrate what is required, we will assume we have identified the external critical path as shown in Figures 7 and 8. That is, the critical path runs from the fictitious Pentium output P5_OUT through two PLDs and into the fictitious inputs P5_IN and CC_IN. The delays through the PLDs have been arbitrarily assumed to be 3.5 and 3.2 nsec. For simplicity, we as-

Figure 7.

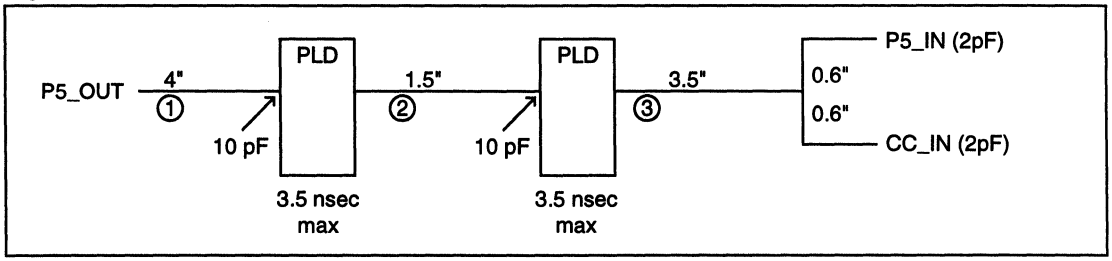


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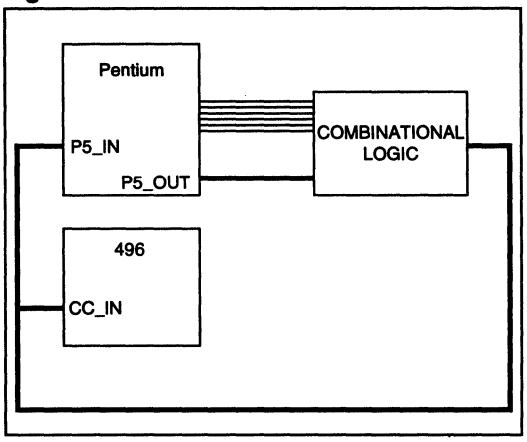
Figure 8.



sume P5_OUT is valid on the rising edge of the clock (add appropriate delay if this not the case for your system). Furthermore, we will assume the setup-time for both inputs is 5 nsec. Computing the path delay:

Segment 1

From our previous discussion, we can compute the delay of a loaded transmission line from expression (5). Using C_L = 10 pF (hopefully a maximum value), L = 4", and our previous values for the remaining variables, we have:

Delay(segment 1) = (4")(146.4ps/in)
$\sqrt{1 + (10pF)/(4" * 2.08pF/in)}$
= 868 psec

Segment 2

Using the same method, we compute:

Delay(segment 2) = 450 psec

Segment 3

For this segment, we analyze the capacitive effects of the two 0.6" segments as a single 1.2" segment with twice the load capacitance:

$LT_{PD}' = (3.5+.6)*(146.4)*$
$\sqrt{1 + (2+2)/((3.5+1.2) * (2.08))}$
Delay(segment 3) = 713 psec

Computing the critical path delay, T_{CPD}:

T_{CPD} = Max gate delays +
Max net delays + MT^+ (8)

where, MT^+ is an estimate of the maximum positive manufacturing tolerance.

T_{CPD} = (3.5 + 3.2) + (.868+.450 + .713) +
9.6"(20 psec/in)
= 8.923 nsec

Computing the available clock tolerance, TOL_{EXT}:

$TOL_{EXT} = T_{CYC} - T_{CPD}$ - Setup-time (9)
= 15 - 8.923 - 5
= 1.077 nsec

We will make use of this figure later in the example.

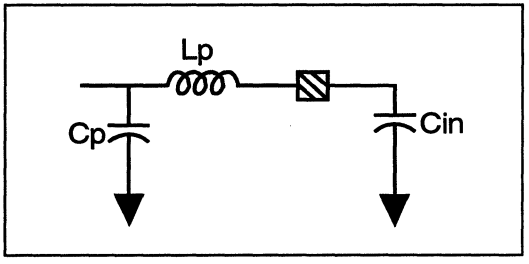
3.4. Inventory of Loading and Placement of Clock Loads

As the expressions illustrated earlier, variation in load-capacitance can be a principal contributor to clock tolerancing. We will see that in Pentium systems with second-level caching, this effect will dominate in the CPU module.

Loading in CPU Module

Intel has characterized the high-frequency behavior of the pins of the devices in the CPU module. Reference 7 provides models for all input pins in the CPU module (it also has output models). The model is shown in Figure 9. The values for the components are shown in Table 1. When analyzing various design approaches with a good simulation tool, these models will contribute to a more accurate answer. They are especially useful since minimum and maximum

Figure 9.



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values are provided instead of typical values. However, since the model is a third-order low-pass filter which is driven by a transmission-line with its own distributed reactive components, we need to simplify it for our manual calculations here. Our transmission-line delay expressions employ a single, lumped load capacitance. So we need to estimate minimum and maximum values for input capacitance from the data in the table.

Table 1 - Component Values for Input Pin Models

Device	Buffer Type	C_P (pF) Min/Max	L_P (nH) Min/Max	C_{IN} (pF) Min/Max
Pentium*	ER3	1.6/2.2	6.2/8.4	1.7/2.3
82496	ER8	1.4/1.9	5.8/7.9	2.4/3.3
82491	ER11	0.5/1.5	6.9/9.3	2.9/3.9

* Ignore 7pF maximum input capacitance rating from DC specification when using these models.

We are concerned about the time at which V_{IN}, the voltage across C_{IN}, charges up to threshold. An edge arriving at the pin on the transmission line can be considered as the sum of several sine-waves - the fundamental (66-MHz) and the harmonics (up to about 250-MHz). The elements of the filter attenuate or resist the high-end spectral components more than the lower ones, degrading the edge and delaying the time V_{IN} charges up to threshold. The fastest time will be when the high-end spectra is attenuated the least, the slowest time when it is attenuated the most. We can assume that the least attenuation will occur when both capacitors and the inductor are at minimum values. If we let the inductance go to zero, the capacitors are in parallel and we can simply add them. This assumption will result in a slightly faster estimate of the arrival time, since the inductor would limit some of the current which charges C_{IN}. The slowest time will occur when both capacitors and the inductor are at their maximum values. In this case, we can simplify, and still account for the effect of the inductor (resisting the passage of the current which charges C_{IN}), by letting the inductance go to zero but scaling C_{IN} up to increase the charging time. Our assumption is that scaling C_{IN} up by 50% will account for the elimination of the inductor. So our maximum value for the pin capacitance will be computed as:

$$\max C_{PIN} = \max C_P + 1.5(\max C_{IN}) \qquad (10)$$

The values we will use are shown in Table 2.

Table 2 - Simplified Pin-Capacitance Values

Device	C_{MIN} (pF)	Typical C_L
Pentium	1.6 + 1.7 = 3.3	2.2 + 1.5(2.3) = 5.7
82496	1.4 + 2.4 = 3.8	1.9 + 1.5(3.3) = 6.9
82491	.5 + 2.9 = 3.4	1.5 + 1.5(3.9) = 7.4

Placement of Loads in CPU Module

Since we are assuming the placement suggested in Reference 8, we can derive the distance to loads from that. The shortest path from the clock driver to either the Pentium or 82496 clock pins is approximately 2 inches. The nearest and farthest 82491s to the clock buffer are approximately 5 and 7.5 inches, respectively.

Loading Outside CPU Module

Assumed placement and loading for the external clock loads is shown in Table 3. It is obvious from the table that either load 1 (largest capacitance value) or load 3 (most remote load) will be our worst case load. Note that we have assumed only typical values for C_L. We would obviously like to have min/max values, but this is usually not available.

Table 3 - External Clock Loads

Load	Estimated Min Distance Clk buffer to load	Typical C_L
1	4"	10pF
2	5"	2pF
3	10"	5pF
4	5.5"	5pF
5	4"	2pF

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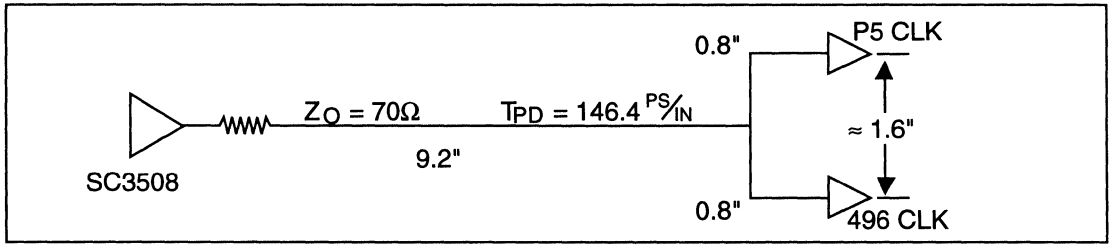
Figure 10.



3.5. Pentium/496 Tolerance Group

Requirement: 200 psec

Structure of Clock Net: This tolerance is sufficiently tight that both loads must be driven off the same pin of the clock buffer to eliminate extrinsic skew (500 psec for the SC3508Q-1). Examining the clock-load inventory from the previous section, we see that the longest clock net will probably be about 10". This will be our starting point for this and all subsequent nets. Nets can be serpentined to use up extra length. The layout of the CPU module tells us the two loads are about 1.6" apart. From this, we will assume the structure for our clock net as shown in Figure 10. The branching point for the stubs has been moved as far out on the transmission line as possible to reduce manufacturing tolerance effects between these two loads.

Analysis: For approximately 1.5 nsec transition times, the 9.2" segment of the line can be treated as a transmission line (i.e. an edge doesn't "know" about a load until it gets there). We can expect the edge to propagate down the 9.2" segment at the unloaded propagation rate, which is 146.4 psec/in. Therefore, we can analyze it and the stubs separately. The stubs are short enough to treat as equipotential nodes. We will treat the two loads as a single capacitive load equal to the sum of the two input capacitance ranges.

Net Delay = Delay of long segment + Stub delay

= 9.2" *Unloaded T_{PD} + Loaded stub delay

$= 1347 \text{ psec} + L*T_{PD}\sqrt{1 + C_L/(L * C_0)}$

where,

L = 0.8" for either stub

T_{PD} = Unloaded propagation rate = 146.4 psec/in

C_0 = 2.08 pF/in (computed earlier)

$3.3 \le C_L \le 5.7$ For Pentium input

$3.8 \le C_L \le 6.9$ For 82496 input

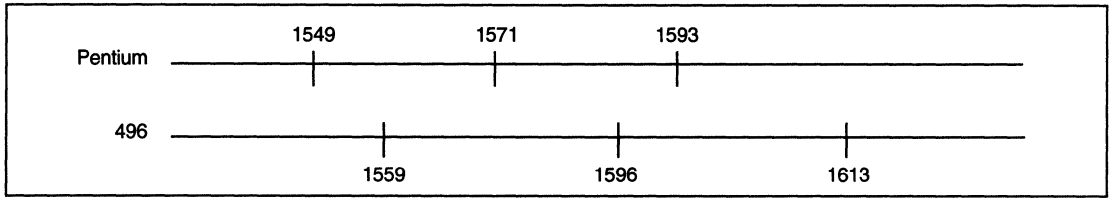
Computing the min and max delays for both paths (SC3508-Pentium and SC3508-82496), we have:

	Min	Max	Mean
Delay SC3508-Pentium	1549 1347+202	1593 1347+246	1571 1347+224
Delay SC3508-82496	1559 1347+212	1613 1347+266	1586 1347+239

Representing this graphically:

The difference between the earliest and latest arrivals is 1613-1549=64 psec. This leaves 200-64=136 psec margin for jitter and manufacturing tolerance on the stubs. We can improve this by aligning the mean delays. In this case, that means increasing the mean delay of the Pentium stub from 224 psec to 239 psec. And

Figure 11.



this is accomplished by lengthening the stub to the Pentium. Solving expression (5) for L, we find that a new Pentium stub length of 882 mils gives us the appropriate alignment.

	Min	Max	Mean
Delay SC3508-Pentium	1563	1609	1586
Delay SC3508-82496	1559	1613	1586

Tolerance: This is determined by the difference in arrival times. There are two cases (early Pentium/late 82496 and late Pentium/early 82496). Since we balanced the mean delays, both cases are identical.

Skew = 1613-1563 = 50 psec.

This should be guard-banded to accommodate manufacturing tolerances on the stubs. These tolerances will probably not be that large due to substantial tracking effects (i.e. these nets are all in the same area of the same layer of the same board). So we'll assume

Guarded skew = **65 psec.**

This leaves 200-65 = **135 psec for jitter** so far. Remember that these figures are just for clocks in this tolerance group.

3.6. Pentium/82491 and 82496/82491 Tolerance Group

Requirement: 700 psec.

Structure of Clock Net: We will assume point-to-point for all SRAM nets to minimize C_L effects. The net will be as shown in Figure 12, with an approximate length of 10".

Analysis: Using

$$3.4 \le C_L \le 7.4 \quad \text{for 491s}$$

and forcing the mean delay to 1586 psec, we solve for a length of 9.621". The full set of delays is:

	Min	Max	Mean
Delay SC3508-82491	1523	1649	1586

Tolerance: If the difference between arrival-times at the 82491s and the 82496 are acceptable, then they will also be acceptable for the difference between the Pentium and the 82491's. This is, of course, because the mean delays are aligned and the arrival time spread is wider at the 82496 than at the Pentium. So we will analyze with respect to the 82496. Using expression (7):

$$\text{Tolerance} = \text{Int skew} + \Delta LT_{PD}' + MT + \text{Jitter} \qquad (7)$$

Substituting our 700 psec limit in for the tolerance

$$700 \text{ psec} \le 500 + \Delta LT_{PD}' + MT + \text{Jitter}$$

$$200 \text{ psec} \le \Delta LT_{PD}' + MT + \text{Jitter}$$

where,

$\Delta LT_{PD}'$ in this case is the worst case arrival time difference (due to C_L effects) between the 82496 and the 82491s. Again, we only have to compute one of the two possible cases due to symmetry.

$$\Delta LT_{PD}' = 1649 - 1559 = 90 \text{ psec}$$

Guard-banding this figure to accommodate manufacturing tolerances, we can assume

Guarded skew = 115 psec

Leaving 200 - 115 = 85 psec for jitter.

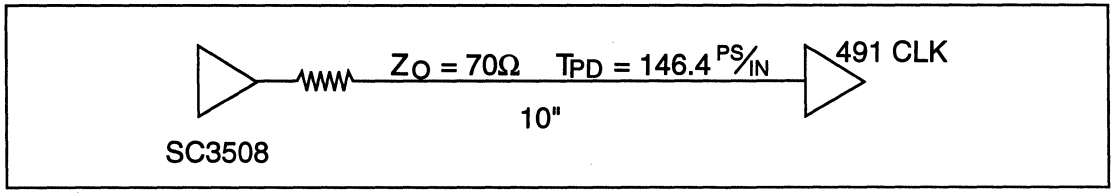
3.7. External Tolerance Group

Requirement: 1.077 nsec (computed earlier)

Structure of Clock Net: We will assume point-to-point for the external loads as well. This net will be identical to that shown in Figure 12.

Analysis: For this group, analysis will not yield the same quality result as it did for the preceding tolerance groups. The reason is that for this

Figure 12.



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group, it is highly likely that you can only get typical values for each load-type. Unfortunately, you require min/max information about load capacitance to compute arrival time variation. There are, however, some approaches that maximize the ability of the design to cope with uncharacterized tolerancing mechanisms. These include:

1. Point-to-point clock nets to minimize the C_L variation on any one net. Given that we have 20 outputs to work with on the clock buffer, this is not a problem for most Pentium designs.
2. Use the lowest possible Z_0 which produces the maximum dynamic current, and thus charges the load capacitance as fast as possible. Reference 2 elaborates on the sensitivity of tolerancing to transmission-line characteristic imedance and variation in load-capacitance.
3. Extending the "charge current" logic applied in the previous point to termination, it is generally advisable to select a termination scheme other than series. The SC3508Q-1 employed in our example design has integral series termination. However, the benefit of point-to-point distribution afforded by the SC3508Q-1's twenty output pins outweighs the impact of series termination.
4. Design each external clock net such that its delay, as computed with typical C_L values, is aligned with the mean delay value of the CPU module.
5. Bypass heavily and use other noise reduction methods to minimize clock jitter at that load, *and* devices it communicates with.

From our earlier computations, we know the maximum allowable tolerance for the external tolerance group is 1.077 nsec. This is the maximum arrival-time difference between either the Pentium and any external load, or the 82496 and any external load. Note that instead of treating all external clock loads identically, we could separately analyze for each load, if necessary.

Computing the mean delay for external load #3 first:

$$LT_{PD}' = L*T_{PD}\sqrt{1 + C_L/(L * C_0)} \qquad (5)$$

Where we will substitute:

$L = 10"$

$C_L = 5pF$ typical

We get a typical delay of 1631 psec. We need to adjust something so that this typical delay aligns with the mean in the CPU module of 1586 psec. We can add delay to all the other nets or possibly reduce the delay of this net. Let us assume we can take the latter approach by slightly repositioning the SC3508 relative to this load. To align the delays, the length of this net must be 9.698" (computed by forcing the loaded delay in (5) to be 1586 psec).

At this point, we may also want to consider reducing Z_0. Repeating the preceding for all the other external loads:

Load	Estimated Min Clock-Net Length	Typical C_L	Actual Length
1	4"	10pF	8.693"
2	5"	2pF	10.363"
3	10"	5pF	9.698"
4	5.5"	5pF	9.698"
5	4"	2pF	10.363"

3.8. Final Design Decisions and Summary

At this point we have "finished" the design of the clock nets. We still have some constraints to compute, which we will do in this section. However, in the event that an unachievable constraint results, it would be necessary to rework the layout of the loads and the lengths of the clock nets.

Jitter, Noise, and External C_L Constraints

The following summarizes the tolerancing for the nets we have just designed:

Tolerance Group	Intrinsic Skew (pin-pin) (psec)	Extrinsic Skew w/ mfg. tol (psec)	Tolerance Constraint (psec)	Jitter Constraint (psec)
Pentium-82496	0	65	200	135 200-65
Pentium-82491	500	< 115*	700	> 85 700-500-<115
82496-82491	500	115	700	85 700-500-115
82496-EX1	500	???	1077	???
82496-EX2	500	???	1077	???
82496-EX3	500	???	1077	???
82496-EX4	500	???	1077	???
82496-EX5	500	???	1077	???
82496-EX6	500	???	1077	???

* - By examination.

System Jitter Constraint - Given the complete information we have about the loads in the first two tolerance groups, we were able to compute jitter constraints. This was done using expression (7). While jitter can be considered to vary from location to location in a system, it is a much more manageable problem to assume it is uniform throughout the system. So, for our example, we will assume a jitter constraint of

System Jitter Constraint = Min(135, <85, 85)
= 85psec

Therefore, we will limit jitter to 85 psec on a system-wide basis. Given the 1077 - 500 = 577 psec of room we have for combined jitter and extrinsic tolerancing in the external tolerance group, it is not likely we will need to control jitter to a lower level. We will now use our jitter constraint to compute the extrinsic skew constraint on the external loads and an approximation on the noise level.

External Extrinsic Skew Constraint- Our limit on tolerancing in the external group due to load-capacitance variation and manufacturing tolerances on the net is:

1077 - 500 - 85 = 492psec

In the following table, we have computed the allowable variation on C_L. The analysis allocates 20 psec/in for manufacturing tolerances on each external net, computes an extrinsic skew constraint from that, and then a constraint on C_L.

Load	C_{TYP} (pF)	Length (in)	Mfg Tol @ 20 psec/in (psec)	Extrinsic Skew Limit (psec)	ΔC_L[2] (pF)
1	10	8.693	174	318	± 5.6
2	2	10.363	207	285	± 4.2
3	5	9.698	194	298	± 4.7
4	5	9.698	194	298	± 4.7
5	2	10.363	207	285	± 4.2

1. 492psec - MT
2. Computed from expression (6) by setting $\Delta LT_{PD}'$ equal to the extrinsinc skew limit, and forcing symmetric variation of the C_L value around the typical value. That is, letting

   $C_{Lmax} = C_{TYP} + C_L/2$ and,

   $C_{Lmin} = C_{TYP} - C_L/2$

The values from the right-most column are a constraint that we place on the clock inputs of the devices that receive the external clocks. In most cases, it is clear we have more than adequate margin on the low side.

System Noise Constraint - From Figure 5, we know that noise in the power environment and clock-signal transition-times interact directly with jitter. Budgeting jitter in a clock-distribution and reception network is complicated and a detailed treatment of that is beyond the scope of this note. In our example, we have a single device performing clock-distribution, and can assume all jitter is added at that point. An approximation of the maximum noise-voltage that the SC3508Q-1 can see at its power pins can be derived from:

$$\text{Max Jitter} \approx \text{Slew}_{max} * V_{noise(p\text{-}p)} \qquad (11)$$

where,

Slew_{max} is the slowest (largest) slew rate in nsec/volt.

$V_{noise(p\text{-}p)}$ is the peak to peak noise voltage.

This was "derived" by examination of Figure 5. Assuming the signal into the SC3508-1 climbs 4V in 5 nsec (typical for many crystal oscillators),

$0.085 \text{ nsec} = (5\text{nsec}/4\text{V}) * V_{noise(p\text{-}p)}$

$V_{noise(p\text{-}p)} = 68\text{mV}$

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This is an aggressive but achievable noise-voltage level at the pin of the SC3508Q-1. To achieve this, noise reduction methods must be used, such as including suitable bypass capacitors. A detailed discussion of noise-voltage reduction is beyond the scope of this note. Notice, however, that employing a crystal oscillator with faster edges increases the allowable noise voltage.

Configuring the SC3508Q-1

The data sheet provides detailed information on configuring the various inputs of the SC3508Q-1. The CLOCK SEL pin must be tied either low for a TTL source or high for an ECL source. Since the clock must toggle during power up (c.f. Section 2.2), the RESET input of the SC3508Q-1 can be tied high (inactive). Finally, source series termination is provided within the SC3508Q-1 to match the output drivers to lines with characteristic impedences in the range of 50 to 75 ohms. The patented output drivers also prevent undershoot and thereby reduce noise at the receiving chip input. The result is that the SC3508 provides 20 outputs with excellent signal integrity.

A Word About Serpentine Delays

Through out this design example we have assumed that the clock net lengths are matched. A typical method of accomplishing this to serpentine clock nets which need additonal length.

The reader is cautioned that serpentining can have an effect on the propagation rate of a net. In Reference 2, this effect is described and illustrated with measurement.

4. EXTENSIONS TO THE DESIGN EXAMPLE

Our example was for a "typical" Pentium system. There are two significant extensions that can be made to this example:

1. Divided synchronous systems
2. Larger systems

4.1. Divided Synchronous Systems

In a divided synchronous system, the CPU module (12 loads) runs at 66-MHz and all of the circuitry external to the CPU module runs at 33-MHz. The memory bus controller will need one or two copies of both clocks to coordinate communication between the two timing environments. If our example design were converted to a divided synchronous system, we would need to select a clock buffer capable of providing an appropriate number of copies both clock frequencies. The AMCC SC3500Q-1 can fill this role. The SC3500's outputs are arranged in three groups (10, 5, & 5 pins), each of which can be operated at various relationships to the input as follows:

Output Group	Relationship to Output
Fa	10 outputs at $F_{input}/2$ (max = 80 MHz)
Fb	5 outputs at $F_{input}/2$ or $F_{input}/4$
Fc	5 outputs at $F_{input}/4$ or $F_{input}/8$

Therefore, we can convert our example to a divided synchronous system using an SC3500 as follows:

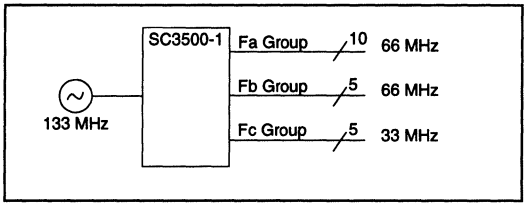
1. Drive the buffer with a 133MHz source.
2. Configure Fa and Fb groups for 66MHz (15 clock signals)

   11 loads in CPU module (as previous)

   4 clock signals available for MBC
3. Configure Fc group for 33-MHz (5 clock signals)

Figure 13 shows this configuration. The analysis of tolerancing for this new arrangement would be similar to what was shown in our original example.

Figure 13.



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4.2. Larger Systems

When the number of loads in a system exceeds the number of pins on the clock buffer employed, it is necessary to move to a tree-structured clock-distribution network to fan out the signals. When this is the case, the tradeoffs and the analysis are more complicated. The most noteable effect is that part-to-part buffer tolerances come into play. In even larger systems, cascaded part-to-part tolerances come into play. A complete discussion of these issues goes beyond the scope of this note. References 1 and 2 cover this subject in more depth. We will, however, provide some guidelines:

1. Exploit locality (i.e. the commonality of clock paths) in signal groups where tolerancing requirements are tight. For example, drive all of the loads in the CPU module from a single SC3508Q-1 to keep the part-to-part tolerances out of tolerances expressions.
2. Align the mean delays of all clock paths.

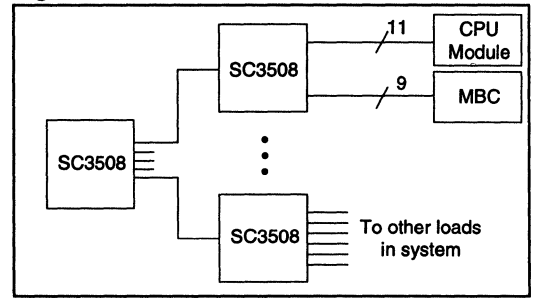
Figure 14 shows a mid-sized Pentium clock distribution network. It takes advantage of the reduced tolerancing among the outputs of the Fa group (250 psec).

5. SUMMARY

This note has presented a detailed example of clock-distribution in a typical Pentium design using AMCC's SC3508Q-1 clock driver. This example discussed the most important design decisions, and extended the example to other common design cases. As we saw, many of the timing-environment design methods previously necessary only in larger and faster computers are now necessary in Pentium systems.

Even with these constraints, this application note shows that the SC3508Q-1 can be used in Pentium systems to create a statistically stable design. With twenty outputs, a low-skew design, and its no-undershoot drivers, the SC3508Q-1 allows the engineer to design a clock distribution scheme that will satisfy the rigorous requirements of the Pentium chips.

Figure 14.



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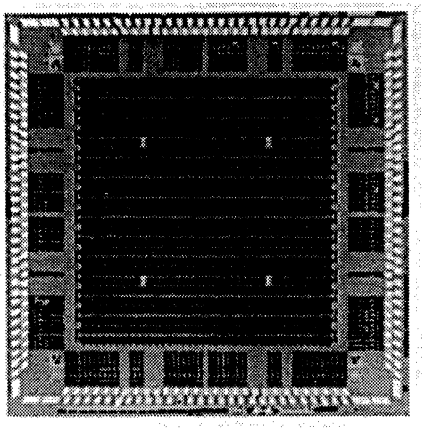
ECL/TTL "TURBO" LOGIC ARRAYS — Q20000

Q20000 FEATURES

- Up to 18,700 gates, channelless architecture
- 100 ps equivalent gate delays
- Ultra low power (.5-1.0 mW/gate)
- 10K, 10KH, 100K ECL and mixed ECL/TTL capability
- Structured arrays with 1.25 GHz PLLs*
- High precision programmable delay line macro
- Speed/power programmability
- Single cell 25 & 50 ohm parallel termination drive
- Symmetrical rise and fall times
- Operation over commercial and military ranges
- Up to 100% utilization



Q20080 DIE

DESCRIPTION

The AMCC Q20000 Series of logic arrays is comprised of eight products ranging in density from 1400 to 18,700 equivalent gates (full adder counting method) including structured arrays with 1.25 GHz PLLs.* The **Turbo** series is optimized to provide high performance and proven reliability to today's advanced hi-rel commercial and military semicustom applications.

Q20000 arrays are designed to operate at frequencies as high as 1.25 GHz. These Turbo arrays achieve this very high performance by combining an advanced one micron process with innovative A.C.-coupled active drive circuitry. The combination of this advanced process and patented circuit design technique has achieved operating performance efficiencies as much as eight times over previous bipolar families.

An extensive library of SSI, MSI and LSI logic macros, including a high resolution programmable delay line, is currently available in conjunction with AMCC's MacroMatrix® design kit. The library features speed/power options that allow the designer to maximize critical path speed while minimizing overall chip power. MacroMatrix is available on most popular engineering workstations (EWS) and simulators.

PERFORMANCE SUMMARY	
PARAMETER	**VALUE**
Typical gate delay(1)	100-250 ps
Maximum toggle frequency	1.25 GHz
Maximum TTL input frequency	100 MHz
Maximum TTL output frequency	60 MHz
Maximum ECL input frequency (DIFF)	1.25 GHz
Maximum ECL output frequency	
single ended	350 MHz
differential	1.25 GHz
Darlington (single ended, mixed mode only)	600 MHz
ECL I/O pair delay (min/max)	330/560 ps

(1)Based upon the use of complex macros and availability of speed/power options.

Table 1

PRODUCT SUMMARY							
PARAMETER	**Q20004**	**Q20010**	**Q20025**	**Q20045**	**Q20080**	**Q20P010***	**Q20P025***
Equivalent Gates - Flip Flop (1)	450	979	2687	4520	7494	649	2178
- Full Adder(2)	671	1469	4032	6782	11242	973	3272
Core Cells	123	267	733	1233	2044	177	595
I/O Cell Count(3)	28	66	100	128	162	34	51
Structured Array Blocks						PLL	PLL
Power (W)(4)	<1W	1-2	1.25-2.5	2-4	4-8	1.5-2.5	2-4

[1] Computed using 11 gate equivalent, 3 cell 3:1 MUXed D Flip-Flop - FF48 Macro.
[2] Computed using 11 gate equivalent, 2 cell, One bit Full Adder, AD05 Macro.
[3] Available I/O signals depends upon package and macro selection. Some I/O macros utilize more than 1 I/O cell.
[4] Assumes 50% Inputs, 50% Outputs, Mixed mode supply. Utilization determines actual array power dissipation.
*Refer to the Q20P025/P010 datasheet for further information.

Table 2

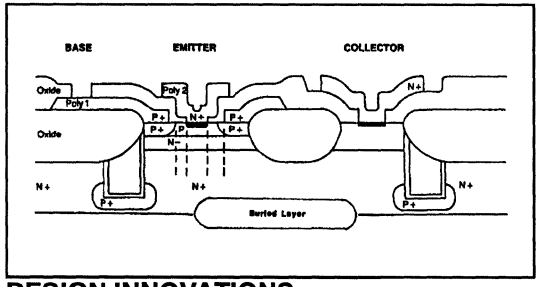
8

TECHNOLOGY

The Q20000 Series of ultra high performance ECL/TTL logic arrays are fabricated using a one micron bipolar process incorporating polysilicon emitter contacts, trench oxide isolation and an advanced base emitter structure (fig. 1). The 1μm wide trench reduces the collector substrate capacitance to less than half and doubles packing density when compared to conventional oxide isolated devices.

The minimum emitter feature size of 1μm x 2μm (.6 x 1.6 effective) combined with the low capacitance of the double poly, trench isolated process, achieves a cut-off frequency (Fτ) of 14 GHz. The three level metal interconnect system employs fine pitch geometries of 4μm first, 5μm second and 7μm for the third level.

Figure 1. Process Cross Section



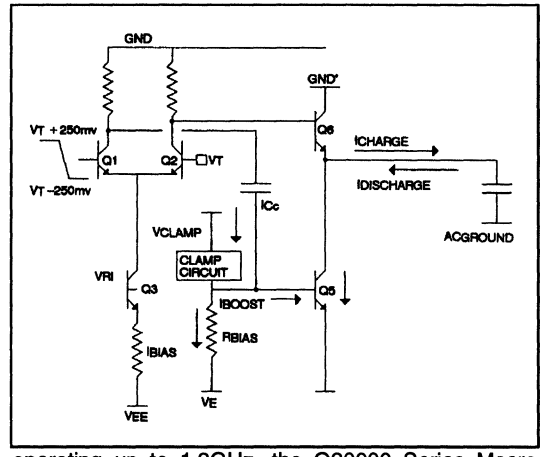
DESIGN INNOVATIONS

Conventional ECL structures use an output emitter follower biased with a static current source. When replicated and used hundreds or thousands of times per array these static current sources consume large amounts of current. As gate densities increase, this static current becomes a large power burden.

To overcome this power burden, AMCC developed a patented dynamic discharge circuit (fig. 2) in place of the static current source for the emitter follower. This dynamic discharge circuit is comprised of a capacitively coupled active pull down arrangement. The static power requirements of this innovative technique are reduced substantially. Output skews between rising and falling edge delays are virtually eliminated and are significantly less affected by interconnect loading. This circuit technique in effect "**Turbo** Charges" the output.

The Turbo circuit is beneficial for circuits operating as high as 600 MHz and is used for the majority of macro functions in Q20000 series designs. For circuit paths

Figure 2. Q20000 Internal Cell Turbo Driver



operating up to 1.2GHz, the Q20000 Series Macro Library includes functions with the traditional ECL output emitter follower structure. Refer to the "High Frequency Design Rules" section of the Q20000 Series Design Manual for further details on appropriate macro choices.

The I/O cell also benefits from the innovative **Turbo** design. Off chip skews for ECL outputs (10KH or 100K) as well as loading effects over conventional emitter follower structures are greatly improved. If a dual supply is available, the I/O cell can be configured with a Darlington output stage plus **Turbo**. This option allows a single I/O cell the ability to drive a 25 ohm parallel terminated line at reduced switch current, therefore reducing power requirements. Table 1 gives a brief summary of the I/O performance figures for the Q20000 family.

ARRAY ARCHITECTURE

The Q20000 Series is the industry's first ECL logic array family to utilize a channelless architecture called **Sea-of-Cells®**. The Sea-of-Cells organization eliminates the dedicated routing channels between cells used in channeled array architectures, thereby doubling the core density. Utilization is maintained at above 95% because of three levels of metal interconnect and AMCC's state-of-the-art place and route software. First level metal is used primarily for macro definition while second and third level metal handle inter-macro routing. The reduced static power of the **Turbo** cell allows power and ground distribution to be interspersed on the second and third level of metal, eliminating the need for a dedicated power plane.

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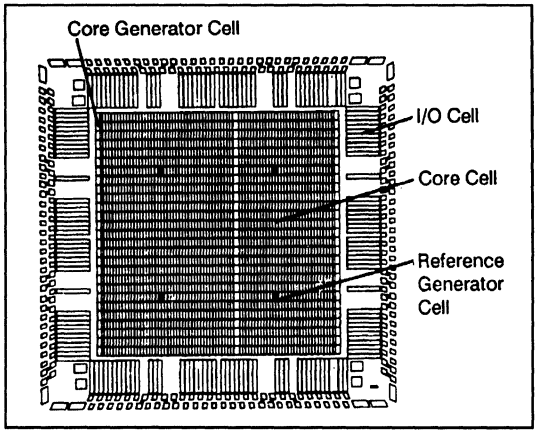
Figure 3. Q20080 Die Organization



Like previous ECL logic array families from AMCC, the internal core cell of the Q20000 Series uses logic efficient three level series gated structures. The three level structure can operate over the full military temperature (–55°C ambient to +125°C case) and voltage range of 10KH or 100K logic because of AMCC's unique design. Table 3 lists representative macro functions and the number of cells required for implementation. A latch can be implemented in only one cell.

The I/O cells are designed to interface with either 10KH, 100K or TTL thresholds. For over 1 GHz operation, a differential CML output structure is also available for use with selected I/O cells and package pins.

Each I/O cell in the array family can be either an input or an output. Bi-directional operation is achieved by paralleling any two adjacent I/O cells. The flexible I/O structure of the Q20000 family allows operation in either 100% ECL I/O, 100% TTL I/O and mixed ECL/TTL I/O in either dual supply or single supply modes.

FUNCTIONAL DENSITY TABLE		
MACRO FUNCTION	**CELL USAGE**	**MACRO NAME**
Flip-Flop with AR; Q/QN outputs	2	FF12
Flip-Flop with EXORed Data; Q output	2	FF22
Flip-Flop with 3:1 MUXed Data, Q output	3	FF48
D Latch	1	LA11
4:1 Mux	2	MX21
2 Input Exclusive-OR, Y output	1	EX30
4 Bit Carry Look Ahead Adder	24	ADD00
4 Bit Counter with AR,AS;	26	CTR02
8 Bit Comparator	40	CMP00

Table 3

STRUCTURED ARRAYS

Two members of the Q20000 family feature embedded high performance Phase Locked Loops. The Q20P025 and Q20P010 arrays include a 1.25GHz PLL with 1000 and 2500 usable gates. Refer to the Q20P010/025 data sheet for further details.

PACKAGING

The Q20000 Series logic arrays are available in a range of standard packages including surface-mountable chip carriers and pin grid arrays. In addition to high pin count packages, special low inductance packages for high speed operation are also available. For complete details consult the AMCC Packaging Guide.

HIGH SPEED/LOW POWER MACROS

The Q20000 Series macro library offers maximum flexibility in the optimization of circuit performance and power consumption. A full complement of macros is offered with low power, standard and high speed options. The high speed options require somewhat more power than standard, but provide a significant improvement in propagation delay and/or maximum operating frequency. The low power versions of macros can be used to reduce power consumption in non-critical paths.

Q20000 SERIES PACKAGING MATRIX Θ_{jc} in °C/W						
Package	**Q20010**	**Q20P010**	**Q20025**	**Q20P025**	**Q20045**	**Q20080**
68 LDCC		2.5				
100 LDCC	2.7	2.7		2.7		
132 LDCC			2.5	2.5		
196 LDCC					2.3	2.0
100 PGA	2.2					
149 PGA			2.0			
208 PGA					1.8	
251 PGA						1.4
301 PGA						
Various						

Table 4

8

Table 5 illustrates the effects of speed/power selections on equivalent gate delay and power consumption. As the table indicates the overall macro performance versus power consumption can be varied significantly depending upon the option selected.

MACRO SPEED POWER OPTIONS: EXAMPLE			
GT65 - 8-INPUT OR	High Speed	Standard	Low Power
TPD min/max (ps) (1)	87/160	103/189	167/298
IEE (mA)	1.12	0.776	0.455
Max Operating Frequency (MHz)	1200	800	600

(1) Tpd = [$TPD_{(++)}$ + $TPD_{(-)}$]/2. Path shown is any input to Y output

Table 5

The circuit designer can make the selection of speed/power options at the time of schematic capture on a supported engineering workstation. Through simulation, the designer can fine-tune the circuit to provide the required mix of performance and power savings.

The macro section in the final portion of this data sheet provides additional information on speed/ power trade-offs.

SIGNAL INTERFACE OPTIONS		
INPUT	BIDIRECTIONAL	OUTPUT
TTL	TTL Transceivers	TTL Totem Pole TTL Tri-State TTL Open Collector
ECL 10K and 10KH	ECL 10K and 10KH Transceivers	ECL 10K and 10KH
ECL 100K	ECL 100K Transceiver	ECL 100K
CML		CML Open Collector

Table 6

PROGRAMMABLE DELAY LINE MACRO (PD00S)

The PD00S is a programmable delay macro in the Q20000 gate array library that provides a timing generation or deskew function for precision timing applications, such as ATE, instrumentation, clock distribution, and high speed buses.

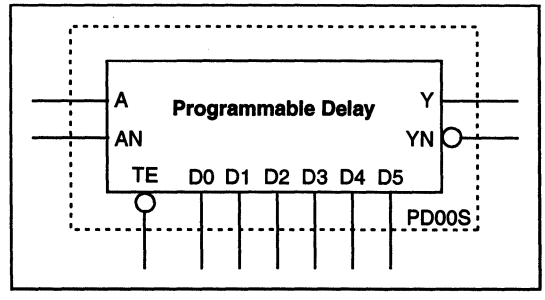
Key features of the PD005 include:

- Up to 30 delay lines per array possible
- Local macro voltage regulation for superior crosstalk performance
- Cascadable for greater delay range
- 46 core cells in size
- Ring oscillator mode for testability
- 6 decode bits for 63 selectable delay steps

PERFORMANCE SUMMARY	
Accuracy	≤ 80 ps
Resolution (typ)	40 ps
Minimum delay range	2.1 ns
IEE (typ)	22 mA
Max frequency	250 MHz
Minimum pulse width	2 ns
Minimum propagation delay	1.30 ns
Linearity to D1	—
No missing codes in 80 ps steps	—

A differential signal is applied to input pin A/AN, is modified with the addition of a delay specified by the binary input address pins D(0:5), and emerges at output pins Y/YN. The test enable input (TE) is held high for normal operation. When the TE input is put low in the test mode, the Y/YN output is internally inverted and fed back to the A/AN input thus allowing the PD00S to function as a ring oscillator and enable operation verification. Changing the binary code of address pins D(0:5), changes the frequency of Oscillations of the PD00S macro that allows for convenient testing of accuracy through delta frequency measurements.

Functional Block Diagram



1. (Y,YN) = (A,AN)
2. NOMINAL DELAY = (40*D0 + 80*D1 + 160*D2 + 320*D3 + 640*D4 + 1280*D5 +1300) ps
3. TE = LOW, Puts PD00S in Ring Oscillator Mode
4. TE = High, Normal Mode

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CUSTOM MACROS

To further enhance the functionality of the Q20000 Series macro library, AMCC has developed a macro development system. It uses a correct-by-construction approach to develop macros that meet all the pertinent design rules. As individual circuit applications warrant, macros with unique characteristics can be developed rapidly and used to optimize the array design.

FLEXIBLE I/O STRUCTURE

The Q20000 Series I/O cells are configurable to provide a universal range of interface options for both single and dual supply modes. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. (Refer to Table 6.)

DESIGN INTERFACE

AMCC has structured its circuit design interface to provide maximum flexibility while ensuring design correctness. For implementations using an engineering workstation, AMCC provides MacroMatrix software. MacroMatrix works in conjunction with the popular, commercial EDA tools to provide the following capabilities:

- Schematic Capture
- Logic Simulation
- Pre-Layout Delay Estimation (Front Annotation)
- Array and Technology-Specific Rules Checks (ERC's)
- Estimated Power Computation
- Layout Netlist Generation
- Post-Layout Timing Verification (Back Annotation)

RaceCheck™, a powerful dynamic timing and test vector analysis tool, is an available option to MacroMatrix. AMCC recommends its use with all design submissions.

Upon submission of the design database to AMCC, a comprehensive review of the circuit is performed making use of the very same EWS and MacroMatrix tools used by the designer. No "golden simulator" is employed to verify the timing of the design. No translation of the logic data is required so the chance of non-design-related errors is virtually eliminated. A complete description of the AMCC Logic Array design interface is available in the Design Interface Brochure.

AMCC DESIGN SERVICES

In addition to supporting design work at the designer's location, AMCC also offers customers the option of working at the San Diego Design Center. At the Design Center, engineers have access to the same sophisticated CAD/CAE tools supported for customer-site designs plus direct contact with a dedicated applications engineer to assist with the array implementation.

AMCC also provides a number of additional support services including:

- Local and Factory Applications Engineering Support
- Comprehensive Training Courses
- Complete Design Documentation
- Full Design Implementation Service (consult AMCC)

ECL INTERFACE

The Q20000 Series arrays can interface to standard and positive reference (+5V) ECL 10K, 10KH and 100K levels. ECL inputs can enter the array from any I/O cell and, in some cases, may be connected directly to core cells without additional buffering. Path delays from different inputs are considerably reduced as indicated by the propagation delays summarized in Table 7. Additionally, signals can be input differentially to remove common mode noise.

ECL outputs can leave the arrays from any I/O cell. Different configurations of the I/O cells provide for a 50 ohm or 25 ohm output drive. Differential CML outputs are available for high frequency paths.

The Q20000 Series allows for a special type of ECL output macro which incorporates a Darlington output configuration. These macros maintain standard ECL 10K, 10KH and 100K output levels, while netting an improvement in drive capability and toggle frequency over standard ECL outputs. While requiring dual power supplies, the Darlington output macros will accommodate 25 or 50 ohm loads in a single I/O location while maintaining ECL standard levels.

Bidirectional ECL operation is available using two adjacent I/O cells.

REPRESENTATIVE ECL INTERFACE MACROS

DESCRIPTION	CELLS	FMAX (MHz)	MAX. FAN OUT (Loads)	DELAY[1] (COM5, Max) (ps)	POWER[2] (Typical, mW)
INPUTS					
Non-Inverting Super Driver (IE23D)	1	1200	32	314	8.0
Differential CML (IE31)	2	800	18	285	11.4
Differential Super Driver (IE32D)	2	1200	32	219	8.9
Differential Super Driver (IE33D)	3	1250	32	139	10.1
Diff, Complementary Outputs (IE34)	2	800	18	274	8.9
Complementary Outputs (IE93)	1	600	18	409	5.8
Std. Non-Inverting (IE94)	1	600	18	263	5.2
Std., Inverting (IE96)	1	600	18	193	5.2
OUTPUTS			**Termination**		
3-Input OR-NOR, Differential (OE15)	3	500	50Ω	439	30.6
CML, Diff'l, Open Collector (OE60)	2	1200	50Ω	121	80.8
3-Input NOR, Differential (OE14)	2	500	50Ω	426	30.6
2-Input NOR, Darlington (OK20)	1	600	25Ω	372	45.5
2-Input OR (OE11)	1	350	50Ω	434	30.6
BIDIRECTIONALS					
3-Input NOR (UE54)	2	600/350	50Ω	532/461	43.2

NOTES:

1 Maximum Worst-Case Prop Delays (unloaded) are for the slowest path. V_{EE} = -4.75, T_J = 130°C (Commercial)
2 At V_{EE} = -5.2V, V_{cc} =+5V for Darlington outputs. Does not include I_{OEF}.

Table 7

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TTL INTERFACE

TTL signals can enter from any I/O cell. Once on-chip, TTL signals are automatically converted to internal voltage levels for internal logic operations.

Signals leaving the array are translated from an internal voltage level to TTL level in the I/O cell. Following this translation, TTL outputs are available in totem pole, 3-state or open collector configurations. TTL outputs, like inputs, can be configured with any I/O cell.

Bidirectional TTL operation is available in single cell and dual I/O cell implementations.

POWER SUPPLY CONFIGURATIONS

On the Q20000 Series arrays there are four basic interface configurations: single-supply ECL, single-supply TTL, and dual-supply and single-supply mixed TTL/ECL. Power supply requirements for each mode of operation are shown in Table 8. Representative TTL I/O configurations are summarized in Table 9.

I/O POWER SUPPLY CONFIGURATION		
I/O Mode	**V_{EE}**	**V_{CC}**
ECL 100K	–4.2 to –4.8V*	–
ECL 10K, 10KH	–4.7 to –5.7V	–
ECL 100K	–4.2 to –4.8V*	4.5 to 5.5V
ECL 10K, 10KH	–4.7 to –5.7V	4.5 to 5.5V
ECL 100K/TTL	–4.2 to –4.8V*	4.5 to 5.5V
ECL 10K, 10KH/TTL	–4.7 to –5.7V	4.5 to 5.5V

* May be configured with a –5.7 supply. Consult AMCC for DC parametrics.

Table 8

REPRESENTATIVE TTL INTERFACE MACROS [3]					+
DESCRIPTION	**CELLS**	**FMAX (MHz)**	**MAX. FAN OUT (Loads)**	**DELAY[1] (COM5, Max) (ns)**	**POWER[2] (Typical, mW)**
INPUTS					
Non-Inverting, Buffered (IT12)	1	100	18	0.76	6.4
OUTPUTS			**DRIVE**		
2-Input NOR (OT22)	1	45	8 mA	5.1	18.8
Tri-State, 2-Input NOR (OT36)	2	45	8 mA	5.8	21.0
BIDIRECTIONALS		**(In/Out)**		**(In/Out)**	
2-Input NOR (UT31)	2	100/45	8 mA	0.63 / 5.9	28.9
Inverting, Controlled Edge Rate (UT70)	1	100/60	8 mA	.76 / 9.27	35.0

Notes:
1 Maximum Worst-Case Prop Delays (unloaded) are for the slowest path. V_{CC} = 5.0V, T_J = 130°C(COMMERCIAL)
2 Computed at V_{CC} = +5.0V, Tri-State enabled. Macro I_{CC} average.
3 All specifications reflect release version (210).

Table 9

8

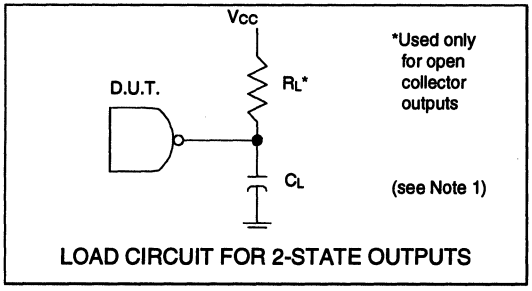

Figure 4

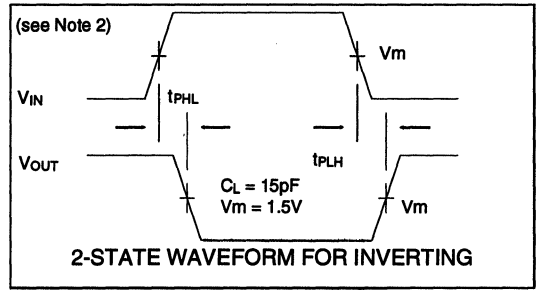

Figure 5

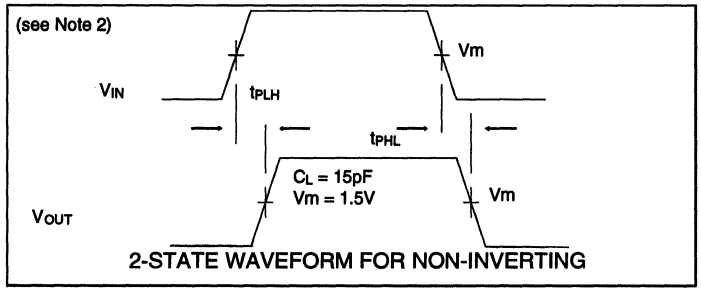

Figure 6

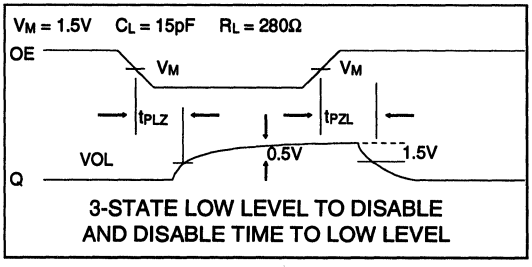

Figure 7

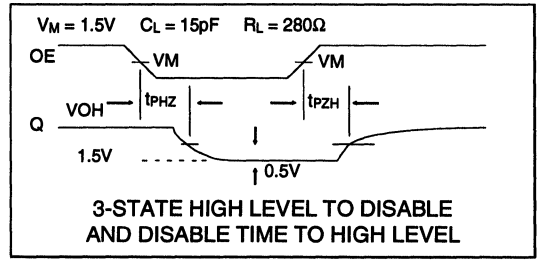

Figure 8

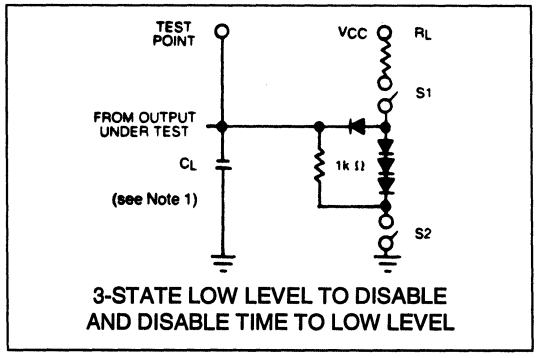

Figure 9

3-STATE TEST CIRCUIT SWITCH TABLE		
TEST FUNCTIONS	**S1**	**S2**
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

NOTES:
1. Standard TTL load circuit used for macro specification. C_L includes probe, jig and package.
2. V_{IN} = 0 to 3.0 volts.

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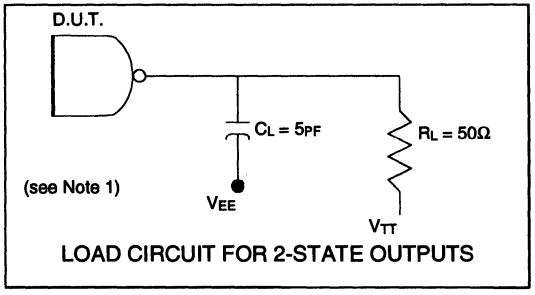

Figure 10

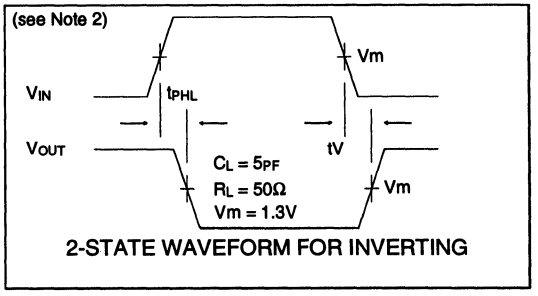

Figure 11

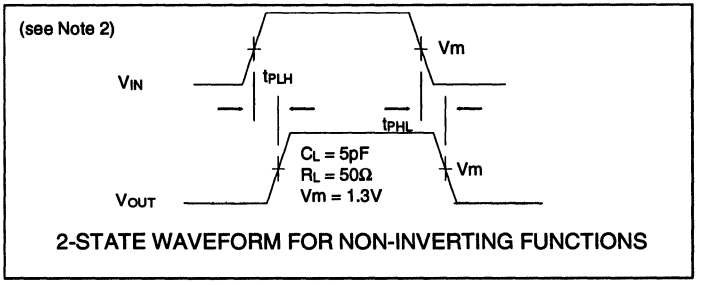

Figure 12

NOTES:
1. Standard ECL load circuit used for macro specification see Figure 10.
2. $V_{IN} = V_{IHMAX}$ to V_{ILMIN}.

8

INTERNAL LOGIC CELL CAPABILITIES

The Q20000 Series internal logic cells are all identical in structure and are uniformly positioned in a Sea-Of-Cells matrix across the internal core area of the array. Each cell contains 17 uncommitted transistors and 13 resistors. The cells are individually configurable to provide a variety of logic functions through the use of the Q20000 Series macro library. The macro library provides SSI, MSI and some basic LSI functions. The higher functionality macros provide the advantages of higher speed, lower power and increased circuit density over a logically equivalent SSI macro implementation.

Table 10 lists parameters for a number of representative Q20000 Series internal macros. The typical power for each macro option can be estimated using the value given in Table 10.

TABLE 10. REPRESENTATIVE INTERNAL MACROS[3]

FUNCTION	CELLS	COM5 DELAY (ps)[1]			TYPICAL POWER (mW)[2]		
		LOW POWER OPTIONS (MIN/MAX)	STD (MIN/MAX)	HIGH POWER (MIN/MAX)	LOW POWER (MIN/MAX)	STD. (MIN/MAX)	HIGH POWER (MIN/MAX)
4 Bit Adder (ADD00)	24/28	369/1009	253/642	165/684	52.5	72.4	81.8
8 Bit Comparator (CMP00)	40		271/871			104	
1:2 Decoder (DE04)	2	104/254	78/162		3.3	4.9	
2 Input EXOR/EXNOR (EX31)	2	207/796	138/435		2.3	3.1	
Flip/Flop w/ AR;Q, QN (FF10)	3	290/773	187/409		3.8	4.6	
D Flip Flop; Q output	2/2/3	193/403	143/254	136/255	3.3	4.1	7.1
4 Input OR/NOR (GT00)	2	193/867	122/411	81/274	1.9	2.6	3.6
8 Input OR/NOR (GT60)	3	170/827	105/338	86/271	2.6	4.5	6.2
2-4 AND-OR Tree (GAT00)	6			148/374			19.3
D Latch (LA11)	1	217/410	148/247		2.4	3.2	
2:1 Mux (MX13)	1	114/294	79/171		1.8	2.6	

NOTES:
1 Minimum/maximum delays are for the fastest and slowest edges: data paths for gates, muxes, decoders, and comparators, Clock to Q for F/F's and latches.
2 Power calculated with V_{EE} = -5.2V , T_J = 130°C (COMM).
3 All specifications reflect release version (210).

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RECOMMENDED OPERATING CONDITIONS - COMMERCIAL

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC} = 0				
10K, 10KH Mode	–4.94	–5.2	–5.46	V
100K Mode	–4.2	–4.5	–4.8*	V
ECL Input Signal Rise/Fall Time	-	1.0	3.0	ns
ECL Input Voltage	–2.0			V
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low(I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

RECOMMENDED OPERATING CONDITIONS - MILITARY

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC} = 0				
10K, 10KH Mode	–4.7	–5.2	–5.7	V
100K Mode	–4.5	–4.5	–4.8*	V
ECL Input Signal Rise/Fall Time	-	1.0	3.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low(I_{OL})			20	mA
Operating Temperature	–55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* –5.7V is possible. Consult AMCC for ECL 100K DC parametric operating at this voltage.

ABSOLUTE MAXIMUM RATINGS*

ECL Supply Voltage V_{EE} (V_{CC} = 0)	–8.0VDC
ECL Input voltage (V_{CC} = 0)	GND to –2.0V
ECL Output Source Current (continuous)	–50mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0V
TTL Input Voltage (V_{EE} = 0)	5.5V
Operating Temperature	–55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	–65°C to +150°C

* Long term exposure at these limits may result in permanent change or damage to the circuits. Actual circuit operation at these conditions is not recommended nor implied.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COM 0°/+70°C		MIL -55°/+125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{IPD}-ECL	ECL Input Propagation Delay Including Buffer IE94S		59	263	57	281	ps
t_{IPD}-TTL	TTL Input Propagation Delay Including Buffer IT50H		93	535	65	602	ps
t_{OPD}-ECL	ECL Output Propagation Delay - Darlington OK40S	No Load	185	340	157	356	ps
t_{OPD}-TTL	TTL Output Propagation Delay Standard OT67S	No Load	2213	4292	2056	4375	ps
t_{FPD}	Internal Equivalent Gate Delay Low Power		120	250	120	250	ps
	Internal Equivalent Gate Delay Standard		105	175	105	175	ps
F_{maxt}	Internal Flip/Flop Toggle Freq. High Speed			1.25		1.25	GHz
F_{in}-ECL	ECL Input Frequency at Package Pin[1] Single-Ended			600		600	MHz
	ECL Input Frequency at Package Pin[1] Differential High Speed			800		800	MHz
	ECL Input Frequency at Package Pin[1] Driver			1.25		1.25	GHz
F_{out}-ECL	ECL Output Frequency at Package Pin[1] Single-Ended			350		350	MHz
	ECL Output Frequency at Package Pin[1] Differential			1.25		1.25	GHz
	ECL Output Frequency at Package Pin[1] Darlington			600		600	MHz
	ECL Output Frequency at Package Pin[1] CML			1.25		1.25	GHz
F_{in}-TTL	TTL Input Frequency at Package Pin[1] Standard			60		60	MHz
	TTL Input Frequency at Package Pin[1] High Speed			100		100	MHz
F_{out}-TTL	TTL Output Frequency at Package Pin Low Power			20		20	MHz
	TTL Output Frequency at Package Pin Standard			45		45	MHz

1 Based on package selection.

8

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS V_{EE} = -5.2V[1,8]

	$T_{ambient}$				T_{case}	UNIT
	-55°C	0°C	25°C	75°C	125°C	
V_{OHmax}[3]	V_{CC}–850	V_{CC}–770	V_{CC}–730	V_{CC}–650	V_{CC}–575	mV
V_{IHmax}[5]	V_{CC}–800	V_{CC}–720	V_{CC}–680	V_{CC}–600	V_{CC}–525	mV
V_{OHmin}[3]	V_{CC}–1080	V_{CC}–1000	V_{CC}–980	V_{CC}–920	V_{CC}–850	mV
V_{IHmin}[5]	V_{CC}–1255	V_{CC}–1145	V_{CC}–1105	V_{CC}–1045	V_{CC}–1000	mV
V_{ILmax}[5]	V_{CC}–1510	V_{CC}–1490	V_{CC}–1475	V_{CC}–1450	V_{CC}–1400	mV
V_{OLmax}	V_{CC}–1655	V_{CC}–1625	V_{CC}–1620	V_{CC}–1585	V_{CC}–1545	mV
V_{OLmin}	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	V_{CC}–1980	mV
V_{ILmin}[5]	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	V_{CC}–2000	mV
I_{IH}[2]MAX	30	30	30	30	30	µA
I_{IL}[2]MAX	–.5	–.5	–.5	–.5	–.5	µA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS V_{EE} = -4.5V[3,8]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C			MIL -55°/+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to -2V	V_{CC}–1035		V_{CC}–850	V_{CC}–1080		V_{CC}–835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to -2V	V_{CC}–1830		V_{CC}–1605	V_{CC}–1880		V_{CC}–1595	mV
V_{IHmin}[5]	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}–1145		V_{CC}–800	V_{CC}–1145		V_{CC}–800	mV
V_{ILmax}[5]	Input Voltage LOW	Maximum input voltage LOW	V_{CC}–1950		V_{CC}–1475	V_{CC}–1950		V_{CC}–1475	mV
I_{IL}[2]	Input LOW Current	V_{IN} = V_{ILmin}			–0.5			–0.5	µA
I_{IH}[2]	Input HIGH Current	V_{IN} = V_{IHmax}			30			30	µA

TTL INPUT/OUTPUT DC CHARACTERISTICS[7]

SYMBOL	PARAMETER	TEST DC CONDITIONS		COMM 0°/+70°C			MIL -55°/+125°C			UNIT
				MIN	TYP[4]	MAX	MIN	TYP[4]	MAX	
V_{IH}[5]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IL}[5]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = –13mA			–.8	–1.2		–.8	–1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} =–1mA		2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 4mA			0.4			0.4	V
			I_{OL} = 20mA			0.5			0.5	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V		–50		50	–50		50	µA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V		–50		50	–50		50	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V				50			50	µA
I_I	Input HIGH current at Max	V_{CC} = Max, V_{IN} = 5.5V				1.0			1.0	mA
I_{IL}[6]	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V				–0.4			–0.4	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} =0.5V		–25		–100	–25		–100	mA

1 Data measured with V_{EE} = –5.2± .1V (or V_{CC} = 5.0 ±.1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_a) and junction temperature (T_J) for -55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_J for packages and operating conditions.
2 Per fan-in.
3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.
4 Typical limits are at 25°C, V_{CC} = 5.0V.
5 These input levels provide zero noise immunity and should only be tested in a static, noise-free environment. Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.
6 For standard speed options only.
7 See figures 4-9.
8 See figures 10-12.

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ECL/TTL "TURBO" LOGIC ARRAYS WITH PHASE-LOCKED LOOP Q20P010/Q20P025

FEATURES

- On-chip high frequency phase-locked loop
- Up to 1.25 GHz capability
- Edge jitter as low as 50 ps (pk-pk)
- 900 and 3000 gates of customizable digital logic
- Utilizes proven Q20000* Series macro library
- 100ps equivalent gate delays
- Ultra low power (.5-1.0mW/gate)
- 10K, 10KH, 100K ECL, PECL and mixed ECL/TTL capability
- Speed/power programmable logic and I/O
- Operation over commercial and military ranges
- Up to 95% utilization of digital logic
- Full logic simulation modeling support of PLL functions

PERFORMANCE SUMMARY	
PARAMETER	VALUE
Phase-Locked Loop	
Operating Frequency	125 MHz - 1.25 GHz
Edge Jitter (pk - pk)	50 - 100 ps
Residual BER	10E - 12
Acquisition Time (typical)	1.0 µs
Digital	
Typical Gate Delay	100 - 250 ps
Maximum Toggle Frequency	1.25 GHz
Maximum TTL Input Frequency	100 Mhz
Maximum TTL Output Frequency	60 MHz
Maximum ECL Input Frequency	1.25 GHz
Maximum ECL Output Frequency	1.25 GHz

TABLE 1

PRODUCT SUMMARY				
	Q20P010		Q20P025	
Equivalent Gates				
Full Adder Method	928		3120	
Flip-flop Method	637		2142	
Internal Logic Cells	177		595	
I/O Pins				
Package	68 LDCC	100 LDCC	100 LDCC	132 LDCC
PLL Related				
Loop Filter	0	0	0	1
Signals	12	12	12	12
Powers & Grounds	8	8	8	8
Digital				
Signals	23	34	45	51
Powers & Grounds	20	20	22	22
AC Monitor & Thermal Diode	4	4	4	4
Maximum Total Power (W)	1.5 - 3		2 - 5	
Availability	Now		Now	

TABLE 2

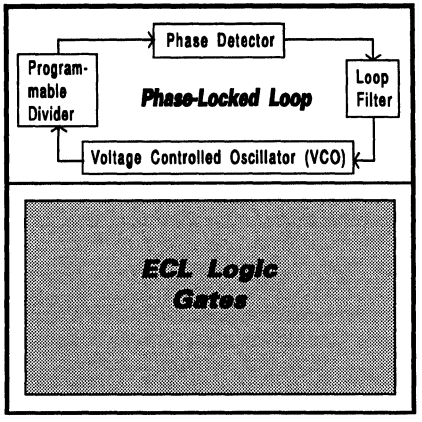

FIGURE 1

APPLICATIONS

- High speed datacom
- High performance telecom
- Timing generation circuits
- Video shift registers
- Frequency synthesis
- Self-timed systems

DESCRIPTION

The AMCC Q20P010 and Q20P025 PLL logic arrays offer gate densities of 900 and 3000 equivalent gates with a high frequency phase-locked loop on-chip. Combining a PLL with user-definable Q20000 series arrays, the Q20P010 and Q20P025 are tailored for high speed serial communication, video, and clock generation applications.

Clock synthesis and clock recovery macros are available for the on-chip phase-locked loop. Speed options ranging from 125 MHz to 1.25 GHz are available. Complete simulation models, implementing all CSU/CRU functions, are available for digital logic simulation on Mentor and Valid workstations as well as the LASAR simulator. Lock detect, local and link loopback features are also selectable options.

For the digital logic portion of the array, an extensive library of SSI and MSI macros is available as part of AMCC's MacroMatrix™ design kit. Latches, parallel-to-serial converters, encode/decode functions, high speed shift registers, bit error rate computation and divide-down counters can easily be assembled to operate in conjunction with the phase-locked loop to meet specific application needs.

*This device specification is an addendum to the Q20000 Series device specification.

8

DIGITAL LOGIC

The Q20000 Series is the industry's first ECL logic array family to utilize a channelless architecture called **Sea-of-Cells™**. The Sea-of-Cells organization eliminates the dedicated routing channels between cells thereby doubling the core density. Utilization is maintained at greater than 95% due to three layer metal interconnect and AMCC's state-of-the-art place and route system. A full complement of SSI and MSI macros is offered with low power, standard and high speed options.

To minimize noise injection from the core logic into the PLL section of the device, all core logic must be operated synchronously with the PLL.

PHASE-LOCKED LOOP MACROS

A selection of clock synthesis and clock recovery macros are available for the on-chip phase-locked loop. PLL center frequencies of 1000, 1062, and 1244 MHz are available with user selectable divide ratios of 1, 2, 4, and 8. This results in speed options of 125, 133, 155, 250, 266, 311, 500, 531, 622, 1000, 1062, and 1244 MHz that are available to operate synchronously with the logic in the digital portion of the array. Additional frequency options can be created to meet specific design requirements. AMCC defined loop filter components for each frequency option have been established for applications with divide ratios up to 64, transition densities of 30% - 70%, and run lengths up to 64 bit times. Lock detect, local and link loopback features are also available options.

Representative Transmitter Block Diagram

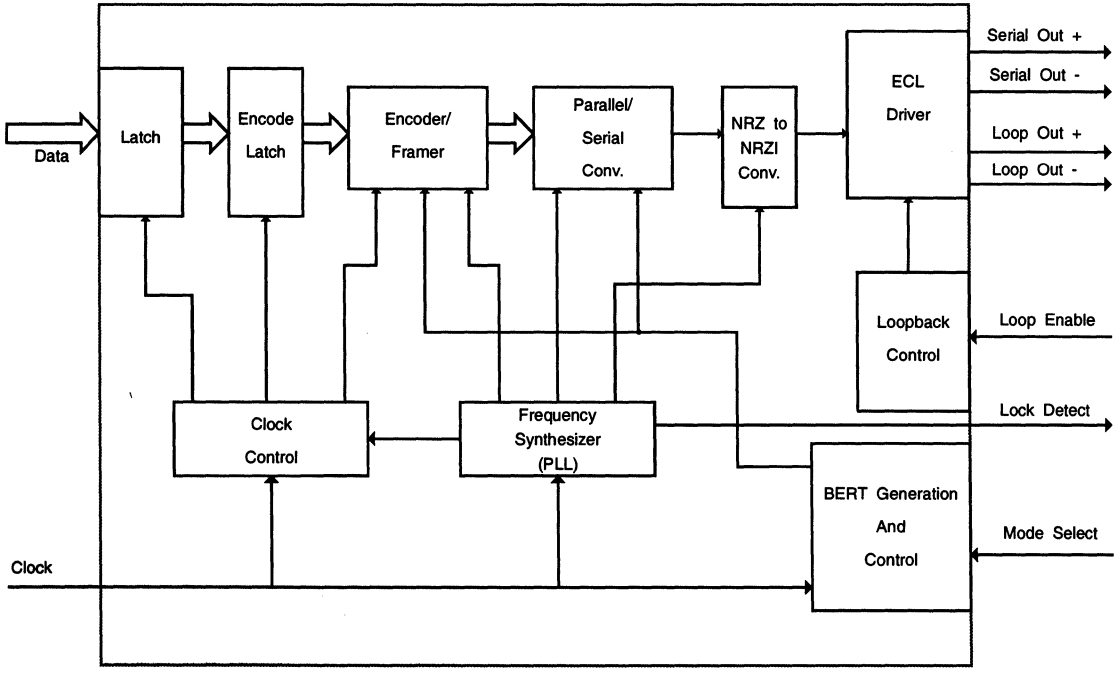

FIGURE 2

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ENCODING/DECODING

High speed datacom and telecom applications frequently require a standard encoding scheme to ensure favorable bit stream characteristics and inter-operability. AMCC initially offers an encoder/decoder scheme implemented using standard macro library components. Popular in datacom applications, IBM's 8B/10B encoding scheme offers DC-balance and short run lengths in an efficiently architected implementation. The 8B/10B macros are available under a licensing and non-disclosure agreement. Other preferred encoding and decoding schemes can easily be designed using the digital portion of the Q20P010 and Q20P025.

FLEXIBLE I/O STRUCTURE

The Q20P010 and Q20P025 array I/O cells are configurable to provide a flexible range of interface options. The I/O cells are designed to interface with standard (-5.2V or 4.5V) and positive reference (+5V) ECL 10KH and ECL 100K or TTL thresholds. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. For dual power supply devices, the I/O is also capable of a Darlington-type ECL output which provides significant improvement in drive capability, toggle frequency, and power dissipation over standard ECL outputs. For TTL signals, a special low-noise, low-power controlled edge rate, single cell bidirectional I/O macro is available for use in Q20P010 and Q20P025 circuits.

Representative Receiver Block Diagram

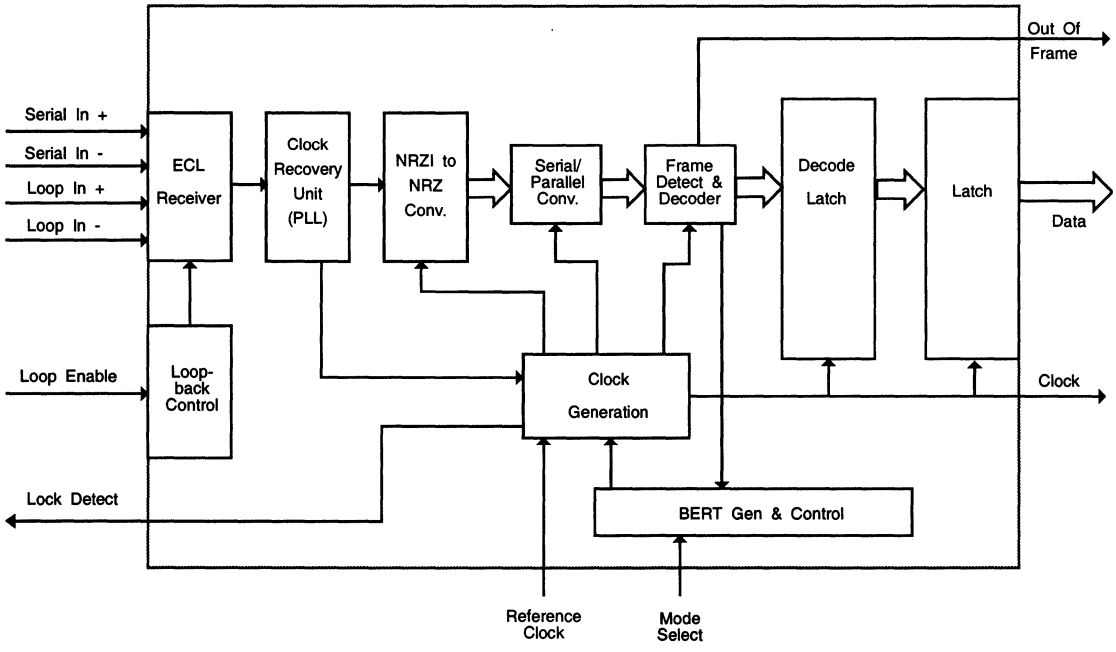

FIGURE 3

8

HIGH SPEED I/O CONNECTIONS

The high speed ECL compatible differential inputs in both the CRU and CSU macros have a built in 100Ω termination resistor across the differential pair, eliminating terminating components in loopback and data paths and ensuring low jitter interfaces. Figure 4 shows some examples of high speed CSU/CRU input and output connections.

High Speed Input and Output Applications

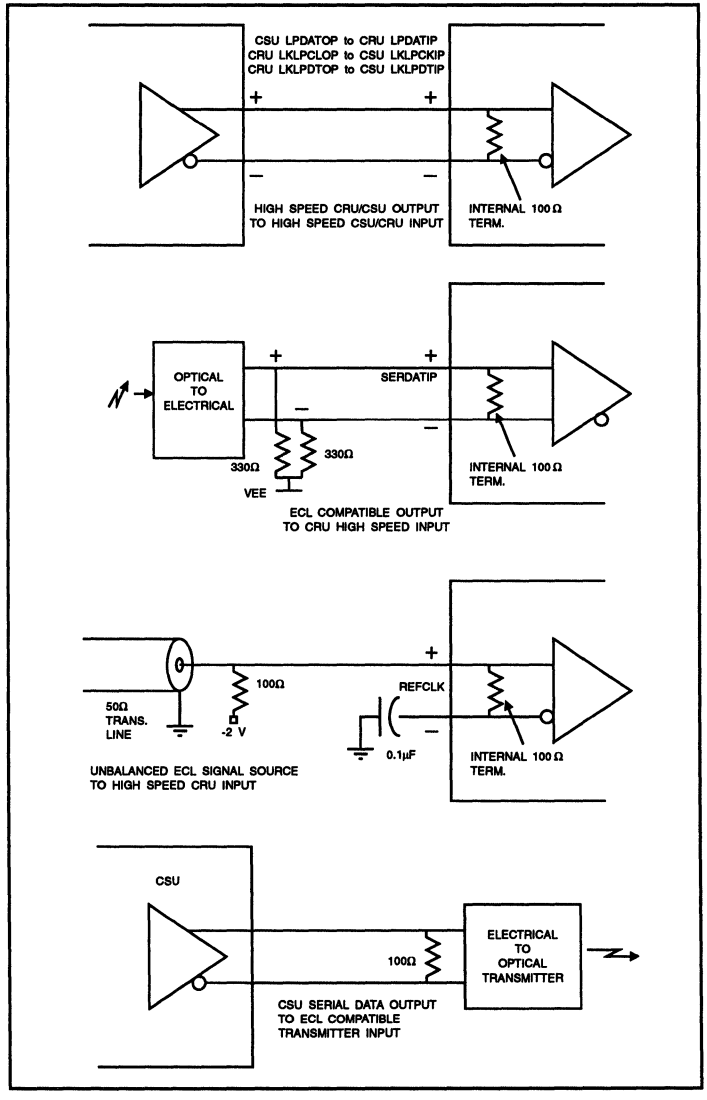

FIGURE 4

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PHASE-LOCKED LOOP

The basic phase-locked loop components are shown in the PLL block diagram (Figure 5). The loop consists of a phase detector, which compares the phase difference between the VCO and the reference input, a loop filter, which converts the phase detector output into a smooth DC voltage, and the VCO, which generates a frequency based on its input voltage.

Metal pattern implementations on AMCC-provided PLL building blocks differ for clock synthesis and clock recovery. This is due to the differences in reference inputs to the phase detector. In the case of the clock synthesis PLL, the reference input is a very stable crystal-based source. For clock recovery from a serial data stream the reference input has varying transition density; i.e., different run lengths of 1's and 0's with short term frequency variations.

The loop filter generates a control voltage for the VCO input based on the output of the phase detector. Different sets of loop filter components must be specified for both the clock synthesis and clock recovery applications. Appropriate filter components will be required for different encoding schemes, acquisition time requirements and system noise environments. AMCC provides on-chip selected sets of resistors and capacitors appropriate for specific system conditions.

SPECIAL FEATURES

LOCK DETECT

For CRU macros, lock detect indicates the phase state of the PLL relative to the incoming data stream. Control pins from the core logic area permit lock detect to be indicated after 512, 1024, 2048, or 4096 bit times depending upon loop filter parameters. On CRU macros, if the serial data inputs have an instantaneous phase jump, the CRU will not indicate out-of-lock state, but will recover correct phase alignment within the pre-loaded bit times.

For the CSU macro, lock detect indicates the phase state of the PLL relative to the incoming reference clock.

Phase-Locked Loop Block Diagram

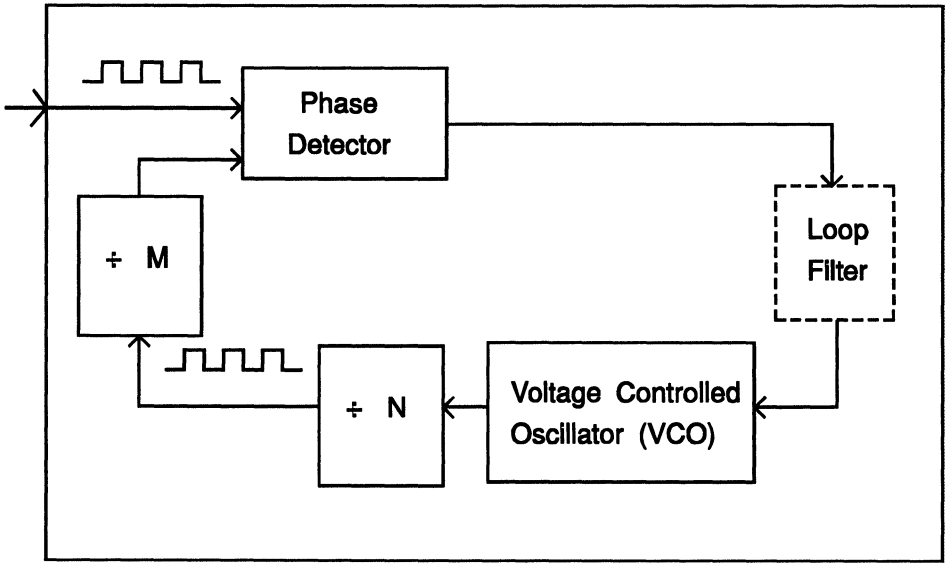

FIGURE 5

8

LOOPBACK MODE

Local Loopback

For datacom or telecom applications, local and link loopback is supported. Local loopback requires both a transmit chip and a receive chip. When enabled, serial encoded data from the transmit chip is sent to the receive chip where the clock is extracted and the data decoded. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium, and allows system diagnostics.

Link Loopback

Link loopback provides a means for link testing. When link loopback mode is enabled, the transmitter accepts serial clock and data from the receiver chip. The serial data is reclocked using the link loopback clock to minimize the data distortion and then transmitted via the serial data output pins. Link loopback can also be used to implement a repeater function, with clock jitter and data distortion determining the number of repeaters allowed.

TEST/BYPASS MODE

Clock recovery and clock synthesis macros have testability input pins to aid in functional testing or PLL clock bypass tests. "Test Clock Enable" places the macros into test mode. An externally generated clock can then be input via the reference clock inputs. The PLL clock bypass path is capable of operating at 1.25 GHz to allow at speed testing of the chip functions or for applications in which a user selectable external clock signal needs to be supported.

Loopback Diagram

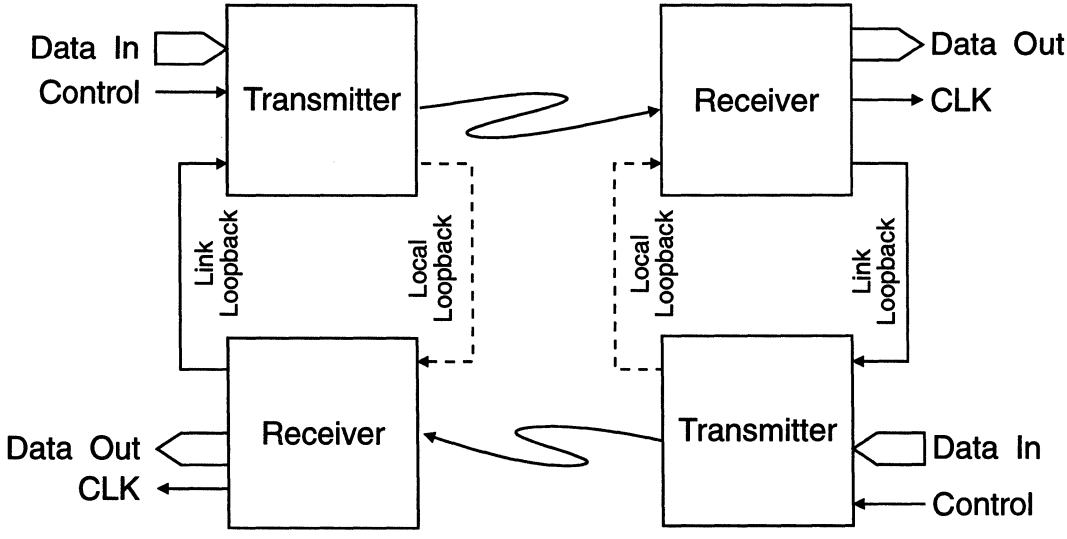

FIGURE 6

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Clock Synthesis Macros

The clock synthesis PLL will generate a high frequency clock in phase with the input reference. A typical frequency multiplication factor is 20, with extension as high as 64. Critical parameters for the clock synthesis PLL are jitter and accuracy. AMCC loop filter components are set to optimize the loop for minimum phase jitter and maximum accuracy, with less emphasis on acquisition time. Loop filter parameters can be varied by AMCC on a custom basis.

Specifications

Input Reference Frequency - The input reference frequency can be a selected divide ratio of the synthesized clock frequency. The maximum divide ratio is 64.

Reference Clock Jitter - The reference clock needs to be generated from a stable source such as a crystal oscillator. The allowable rms jitter cannot exceed .04 % of the reference clock pulse width.

Input Reference Stability - The reference clock stability should be less than 100 ppm.

Acquisition Time - The loop acquisition time will depend on the loop filter parameters. (1.0 µs to 250 µs values are typical)

Edge jitter - The output edge jitter will depend on the loop filter parameters. (50 to 100 ps pk-pk values are typical)

Supply Voltage Sensitivity - Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

Clock Synthesis Macro Diagram

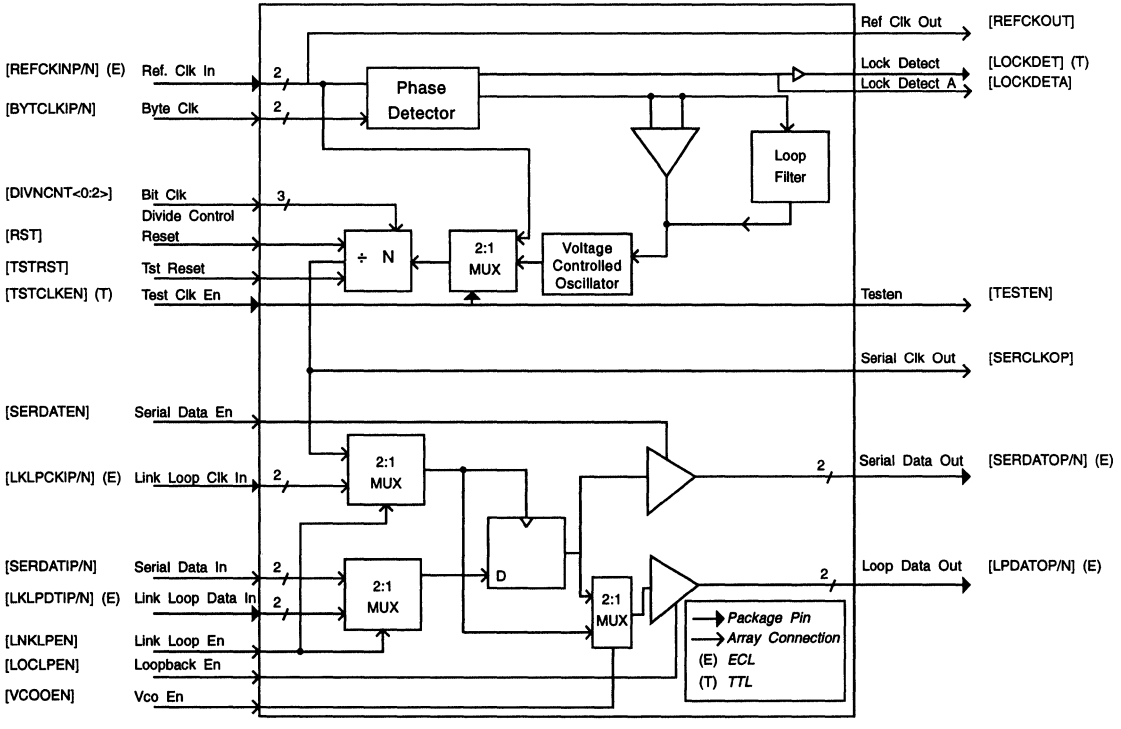

FIGURE 7

Clock Recovery Macros

The clock recovery PLL will generate a clock which is at the same frequency and 180 degrees out of phase with the serial data input. This generates clock and data outputs from the incoming serial bit steam which feeds the subsequent parallel conversion. An external clock reference is used to reduce initial acquisition time and to provide stability in the absence of serial data. The filter parameters are set to optimize the loop for the anticipated serial data input characteristics. These include: maximum run length and transition density of 1's or 0's, and the jitter associated with the fiber optic link. Loop filter parameters can be varied on a custom basis by AMCC.

Specifications

Input Reference Frequency - The input reference frequency can be a selected divide ratio of the VCO clock frequency. The maximum divide ratio is 64.

Reference Clock Jitter - The reference clock needs to be generated from a stable clock source such as a crystal oscillator. For maximum performance rms jitter should not exceed .04 % of the reference clock pulse width.

Input Reference Stability - The reference clock stability should be less than 100 ppm.

Acquisition Time - The loop acquisition time will depend on the loop filter parameters. (1.0 µs to 250 µs values are typical)

Edge jitter - The edge jitter will depend on the loop filter parameters and the serial data input specifications. (50 ps to 100 ps pk-pk values are typical)

Supply Voltage Sensitivity - Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

Data Rate - The possible serial data rates from which a clock can be recovered will be grouped around the VCO center frequency and integer divide ratios of 1, 2, 4, and 8.

Allowed Data Jitter - The allowed input data jitter will be a function of the acquisition time, the loop filter parameters, the data rate and the allowed bit error rate. The jitter specification includes duty cycle distortion, random jitter and data dependent jitter.

Pull In Range - The pull in range of the VCO is ± 6%.

Bit Error Rate - Bit error rates of 10^{-12} or lower are achievable.

Clock Recovery Macro Diagram

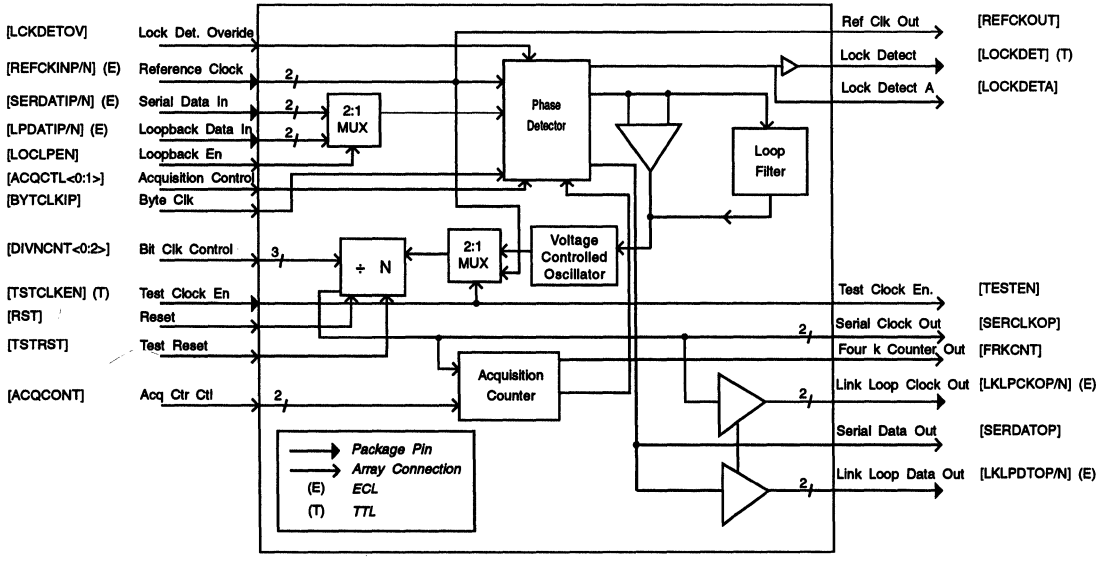

FIGURE 8

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TTL Controlled Edge Rate BiDirectional I/O Macro
AC Electrical Characteristics
(Dual Supply +5V/–5.2V or –4.5V)

SYMBOL	PARAMETER	Test Conditions	COM 0°C to 70°C		MIL –55° to +125°C		UNIT
			MIN	MAX	MIN	MAX	
TOPD+–	TTL Output Propagation Delay, Falling Edge	No Load	2.741	4.278	2.598	4.469	ns
		15pF	3.596	6.138	3.033	6.689	
TOPD–+	TTL Output Propagation Delay, Rising Edge	No Load	4.174	6.942	3.652	7.226	ns
		15 pF	4.489	7.647	3.922	8.066	
TIPD++	TTL Input Propagation Delay, Rising Edge	No Load	247	755	177	1085	ps
TIPD–+	TLL Input Propagation Delay, Falling Edge	No Load	40	260	8	323	ps
TPLZ	Output Disable Time from Low Level	refer to the Q20000 Data Sheet	2.164	3.685	1.718	3.910	ns
TPHZ	Output Disable Time from High Level	refer to the Q20000 Data Sheet	2.741	4.032	2.655	4.091	ns
TPZH	Output Enable Time to High Level	refer to the Q20000 Data Sheet	2.265	5.235	1.818	5.979	ns
TPZL	Output Enable Time to Low Level	refer to the Q20000 Data Sheet	5.166	8.745	4.805	11.284	ns

TABLE 3

High Speed ECL Output
AC Electrical Characteristics

SYMBOL	PARAMETER	Test Conditions	COM 0°C to 70°C		MIL –55° to +125°C		UNIT
			MIN	MAX	MIN	MAX	
TPD+–	ECL Output Delay, Falling Edge	No Load	203	382	176	399	ps
		15pF	443	922	386	1059	
TPD–+	ECL Output Delay, Rising Edge	No Load	256	439	228	466	ps
		15pF	556	1009	483	1261	
Fout	ECL Output Frequency			1.25		1.25	GHz

TABLE 4

Minimum and maximum specifications account for temperature, voltage, and process variations over the given operating range. For complete specifications, refer to the Q20000 Device Specification and Q20000 Array Series Design Manual.

PACKAGING

The Q20P010 and Q20P025 PLL arrays are available in surface mount technology offering loop filter elements mounted on the package. All packages have been custom designed by AMCC to offer controlled impedance on high speed signals and minimal digital noise injection to the PLL area. For complete details consult the AMCC Packaging Guide.

PACKAGE AVAILABILITY & THERMAL CHARACTERISTICS Θjc in °C/W		
PACKAGE TYPE	Q20P010	Q20P025
68 LDCC	6.0	–
100 LDCC	6.5	5.0
132 LDCC	–	5.0

68 Lead Hermetic Ceramic Flatpack

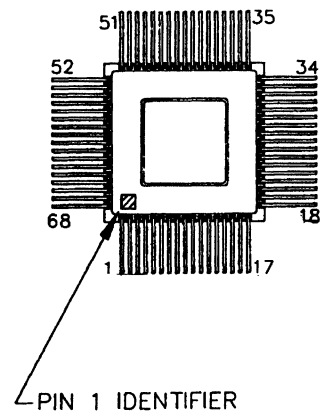

FIGURE 9

100 Lead Hermetic Ceramic Leaded Chip Carrier

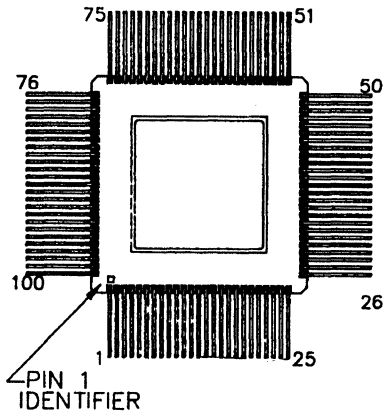

FIGURE 10

132 Lead Hermetic Ceramic Leaded Chip Carrier

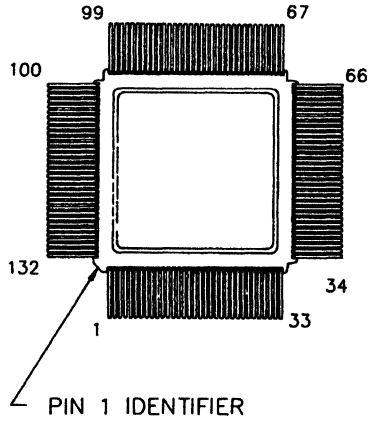

FIGURE 11

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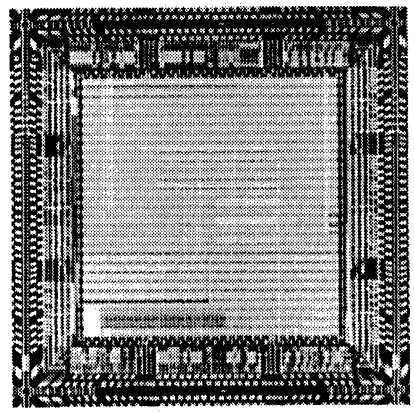
DESCRIPTION

The AMCC Q24000 Series of BiCMOS logic arrays is comprised of six products with densities ranging from 720 to 13440 equivalent gates including a structured array with a high performance Phase-Locked Loop*. The series is optimized to provide CMOS densities with bipolar performance for today's sophisticated semicustom applications.

The Q24000 Series combines 1.0-micron CMOS features with an advanced 1.5-micron oxide-isolated bipolar process on a single silicon chip. AMCC's BiCMOS is especially optimized for high speed utilizing a BiCMOS core with primarily bipolar devices in the I/O. The BiCMOS process uses an N-type epitaxial layer as the foundation for both the NPN bipolar and CMOS devices. The CMOS transistors are used for logic implementation only while bipolar devices are utilized for drive capability necessary for large intermacro connections. For high performance systems, such capability is necessary to drive high fanout and large metal interconnect.

In addition, the Q24000 Series is highly flexible providing interface to ECL 10K, ECL 100K, TTL, CMOS or mixed CMOS/ECL/TTL systems.



Q24140 Die

An extensive library of SSI and MSI logic macros is available in conjunction with AMCC's MacroMatrix® design kit. MacroMatrix is available for use with Dazix, Mentor, Valid and Synopsys as well as Lasar 6.

FEATURES

- Mixed 1.0 Micron CMOS/1.5 Micron Bipolar Technology
- Equivalent Speeds of Second-generation ECL - .4nS Gate Delays
- Extremely Low Power
- High Density - Up to 13,440 Usable Gates
- Low Interconnect Delay Penalty - 25 pS/fanout
- Speed/Power Programmable I/O Macros
- 10K ECL, 100K ECL, CMOS, TTL or Mixed CMOS/ECL/TTL
- Operation from -55°C Ambient to +125°C Case
- Performance Specified to T_J = 130°C Commercial, 150°C Military
- High Output Drive Capability

8

Table 1. Performance Summary

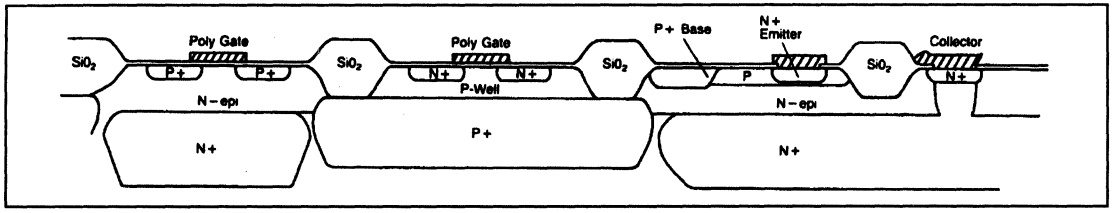
Parameter	Value
Typical internal gate delay	
1 load, no metal	.31 ns
2 load, 2 mm of metal	.40 ns
Typ. internal F/F toggle frequency	280 MHz
Typ. input delay	
ECL–	1.3 ns
TTL–	3.0 ns
Typ. output delay	
ECL–	.6 ns
TTL–	2.2 ns
ECL compatible output drive	25Ω, 50Ω
TTL compatible output drive	8, 20, 48 ma
Cell utilization	up to 100%

Table 2. Product Summary

Description	Q24008	Q24021	Q24060	Q24091	Q24140	Q24P008*
Equivalent gates	760	2160	5760	9072	13440	720
Internal logic cells	190	540	1440	2268	3360	180
I/O pads	44	80	132	160	226	36
Fixed power/ground pads	6	28	50	56	56	6
Total pads	50	108	182	216	282	50
Typical power[1]	.4–.8W	1–2W	1–2.8W	2–4W	1.4–4.4W	.4–.8W

1 4.5 Volts supply @ 25°C, 50% inputs/50% outputs; 40 MHz with 20% of internal gate switching.
* Refer to the Q24P008 device specification for more information.

Figure 1. Process Cross Section



ARRAY ARCHITECTURE

The Q24000 Series logic arrays are comprised of both channelled and channelless architectures. While the Q24021 and Q24091 are channelled arrays, the Q24008, Q24P008, Q24060, Q24140 and utilize AMCC's innovative Sea-of-Cells channelless architecture. The Sea-of-Cells organization eliminates the dedicated routing channels between cells, used in channelled array architectures, thereby increasing the core density. 100% routing capability is maintained up to 100% utilization with three levels of metal interconnect. First level metal is used primarily for macro definition while second and third level metal handle inter-macro routing.

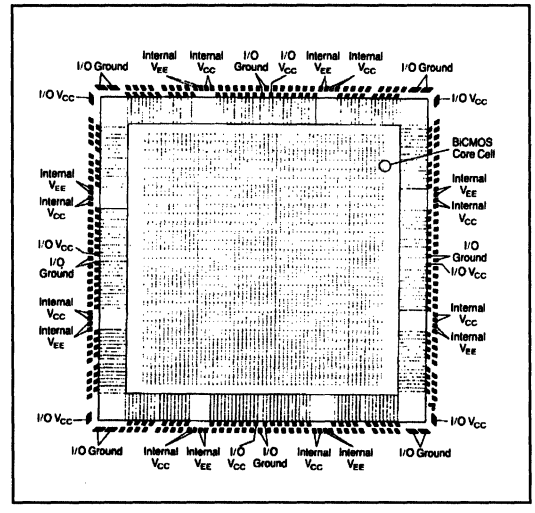
The Q24000 Series is a true BiCMOS array. Each core cell has BiCMOS components, while the I/O is comprised primarily of bipolar construction. BiCMOS performance is not limited by I/O switching speeds. Core macros employ a bipolar totem pole configuration used to drive the next function for all macros. The I/O cells are highly flexible and can be configured as an input or an output.

Both channelled and channelless arrays utilize the same logic cell. The internal logic library is common to both array architectures. However, the I/O cells between the channelled and the channelless arrays are constructed differently.

The channelled arrays have two types of I/O cells. On three sides of the array, the I/O cells can be used to implement unidirectional input or output. The remaining side of the array can implement single-cell bidirectional or unidirectional I/O functions. However, this does not restrict the number of bidirectional I/Os in the channelled arrays. Bidirectional functions can also be implemented by tying two unidirectional I/Os together. In addition, all I/O cells can implement ECL 10K, ECL 100K, TTL, CMOS or a mixture of all these technology interfaces on one chip.

The channelless arrays have only one type of I/O cell. All I/O cells implement unidirectional input or output. Bidirectional I/Os are created by tying two unidirectional I/Os together. In addition, all I/O cells can implement ECL 10K, ECL 100K, CMOS, TTL or a mixture of these technology interfaces on one chip.

Figure 2. Q24140 Array Layout Sea-of-Cells Architecture



LOW INTERCONNECT DELAY

When considering the performance of a design, the interconnect can contribute a significant proportion of the overall delay. The performance of an internal macro is directly related to the drive, or k-factor, associated with the macro. Typical CMOS drive factors can range from 150 to 250 ps per fanout. However, each internal macro of AMCC's BiCMOS typically has loading delay penalties of 25 ps per fanout, a 6X to 10X improvement. Since the bipolar transistors used in the Q24000 Series basic cell yield drive factors

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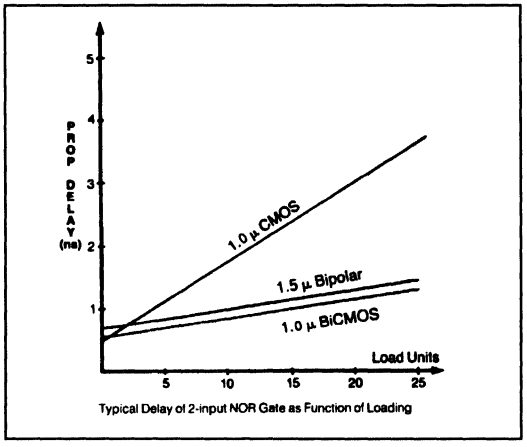
Figure 3. Fanout Degradation Comparison



Typical Delay of 2-input NOR Gate as Function of Loading

6 to 10 times lower than those of comparable CMOS transistors, BiCMOS macros experience little performance degradation as fanout loads are increased.

Another benefit to AMCC's BiCMOS is the symmetric k-factors. Loading delays of 25 ps per fan-out apply to both rise and fall delay penalties. Typically for CMOS devices, p-channel and n-channel devices have inherently different drive factors. This contributes to uneven k-factors for rising and falling edges, further pronouncing signal skews. Uneven skews contribute to pulse width degradation of system clocks, limiting maximum system performance. BiCMOS designs can improve high performance system speeds due to the minimal loading skews.

HIGH DRIVE CAPABILITY

TTL output drive strengths of 8 or 20 mA from a single I/O cell are available to optimize power versus drive strength. Thus, users will no longer sacrifice I/O cells for increased drive capability. In addition, two output buffers can be used in parallel to achieve 48 mA sink current capability. Such high drive strength will allow direct interface to common bus specifications.

210 MHZ PERFORMANCE

Even though shrinking geometries have dramatically increased CMOS internal switching frequencies, the I/O has not reaped the same benefit. CMOS I/O frequencies continue to be less than 100 MHz due to limitations of the I/O switching. With AMCC's BiCMOS the maximum switching frequency is not limited by the I/O since the I/O is primarily bipolar. Instead BiCMOS benefits from the high nominal internal switching frequency, yielding a frequency of 210 MHz under worst case commercial conditions.

With this performance, applications such as high resolution graphics, telecommunications, high end personal computers, workstations, and military can capitalize on ECL type speeds with extremely low power.

BICMOS INTERNAL LOGIC CELL STRUCTURE

The Q24000 Series internal logic cell utilizes both CMOS and bipolar devices. Each cell has 4 resistors, 8 CMOS transistor pairs with four bipolar transistors in a totem pole configuration. The CMOS devices are used for logic implementation while the bipolar device pairs provide necessary drive capability. (See figure 4.) With this type of core cell design, each macro benefits from the additional drive of bipolar transistors. There is very little real estate penalty from the bipolar drivers since they occupy only 10% of the entire chip area. There is only one logic cell type, simplifying the gate array design process. With such a large cell, macro functions such as D latches, 6-input ORs or Exclusive ORs can be implemented in a single cell with minimum intramacro metal delay penalty.

POWER CONSIDERATIONS

AMCC's Q24000 Series arrays have been designed for high performance while maintaining low power dissipation. The power consumption of the internal core of a BiCMOS array is directly proportional to the number of gates switching simultaneously during a clock cycle and the operating frequency. Internal power consumption for Q24000 Series BiCMOS arrays is approximately 20μW/gate-MHz for active gates switching during the clock cycle. The core area consumes no DC power. Figure 5 plots internal power versus the percentage of simultaneously switching gates.

I/O cell power is determined by the interface mode selected and the particular macro selected. Power consumption for representative I/O macros is defined in the CMOS, ECL and TTL Interface sections of this data sheet.

8

Figure 4. 2–Input NAND Schematic

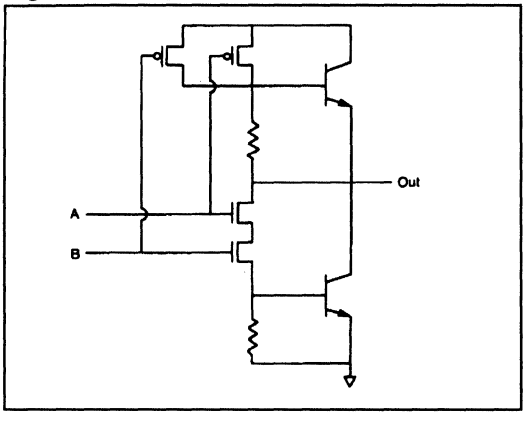
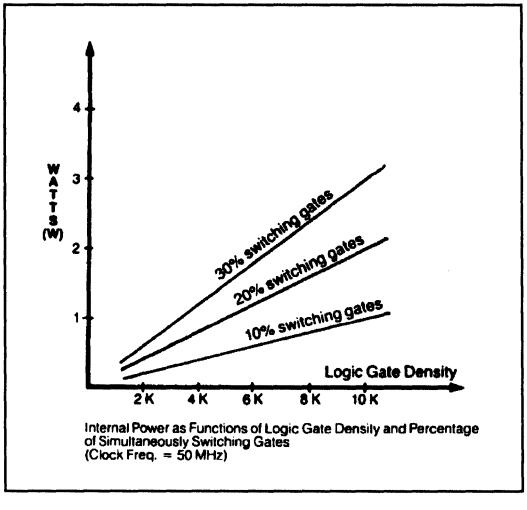


Figure 5. Typical Core Power Dissipation



Internal Power as Functions of Logic Gate Density and Percentage of Simultaneously Switching Gates (Clock Freq. = 50 MHz)

HIGH SPEED/LOW POWER MACROS

The Q24000 Series macro library offers maximum flexibility in the optimization of circuit performance and power consumption. I/O macros are offered with low power, standard and high-speed options. The high speed options require somewhat more power than standard and low power but provide a significant improvement in performance.

Table 3 illustrates the effects of speed/power selections on maximum frequency versus power. As the table indicates the overall macro performance versus power consumption can be varied significantly depending upon the option selected.

Table 3. I/O Speed/Power Options

	I/O Type	Parameter	Speed/Power Options[1] Low Power	Standard	High Speed
ECL[2]	Input	Max Freq (MHz)		160	210
		Power (mw)		10	13
	Output	Max Freq (MHz)		210	
		Power (mw)		22	
TTL[3]	Input	Max Freq (MHz)	35		65
		Power (mw)	5		14
	Output (8mA)	Max Freq (MHz)	25		
		Power (mw)	5		
	Output (20mA)	Max Freq (MHz)	50	65	
		Power (mw)	8	12	

1 Maximum rating frequency under commercial conditions.
2 ECL power determined at VEE = -4.5V.
3 TTL outputs illustrated are used for mixed mode. 100% TTL mode macros will experience considerably lower power.

The circuit designer can make the selection of speed/power options at the time of schematic capture on a supported engineering workstation. Through simulation, the designer can fine-tune the circuit to provide the required mix of performance and power savings.

The interface macro sections of the data sheet provide additional information on speed/power trade-offs.

FLEXIBLE I/O STRUCTURE

The Q24000 Series I/O cells are configurable to provide a wide range of interface options.

The Q24000 Series arrays also offer the following special options to support various interface requirements such as high speed and +5V, single-supply ECL and TTL I/O (see Table 4). The mixed ECL/TTL capabilities allow the interface to both technologies on a single chip without the use of external translators.

Table 4. Flexible I/O Structure

Input	Bi-Directional	Output
TTL ECL 10K ECL 100K CMOS	TTL Transceiver ECL 10K Transceiver ECL 100K Transceiver CMOS	TTL Totem Pole TTL 3-State TTL Open Collector ECL 10K ECL 100K CMOS

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PSEUDO ECL

+5V referenced ECL (PSEUDO ECL) has a number of advantages that can improve system cost and performance. First, +5V referenced ECL mixed with TTL allows a single power supply to be utilized in the system. Second, the ECL I/O can provide fast on and off chip delays. Paired ECL I/O delay can be as a fast as 2.0 nS, a 60% improvement over TTL I/O delays. Pseudo ECL is also ideal for clock lines, providing minimal skew for clock distribution trees or the capability for differentially driven inputs or differential outputs. Differential signals provide higher noise immunity. Last of all, mixed +5V ECL/TTL, systems can break the 100 MHz frequency barrier, and still maintain TTL system compatibility.

ECL INTERFACE

The Q24000 Series BiCMOS arrays can interface to standard ECL 10K and ECL 100K levels. In fact, 10K and 100K output cells can be combined in one array.

ECL outputs can leave the arrays from any I/O cell and provide 50 ohm or 25 ohm output drive. Some 50 ohm output macros incorporate simple logic functions within the I/O cell effectively providing added density.

On the channeled arrays, single cell bidirectional ECL operation is available using one-quarter of the available I/O cells. 20 and 40 ECL transceiver macros are located along one side of the Q24021 and Q24091 arrays, respectively. For the channelless arrays, bidirectional ECL is achieved by tying two I/O cells together.

Table 5. I/O Power Supply Configuration

I/O	V_{EE}	V_{TTL}
ECL 100K	-4.2 to -4.8V	—
ECL 10K	-4.7 to -5.7V	—
ECL 100K/TTL	-4.2 to -4.8V	4.5 to 5.5V
ECL 10K/TTL	-4.7 to -5.7V	4.5 to 5.5V
TTL	—	4.5 to 5.5V
ECL/TTL Single Supply	4.5 to 5.5V	4.5 to 5.5V

Table 6. Representative CMOS Interface Macros

	Cells	Maximum Delay (ns)[3]	Maximum Power (mW)[4]
INPUT Non-Inverting	1	1.6	3.1
OUTPUT 2-Input OR	1	3.2	7.7

Table 7. Representative ECL Interface Macros

Description	Cells	Maximum Delay (ns)[1]		Maximum Power (mW)[2]	
ECL 10K/100K		**Standard**	**High Speed**	**Standard**	**High Speed**
INPUTS Non-Invert[3]	1	1.8	1.5	14.8	18.8
OUTPUTS 2-Input OR	1	.8	—	32.6	—
25Ω Driver	2	.8	—	84.8	—
Bidirectional	1	4.9/.8	1.8/.5	48.1	51.7

* Under Development

8

TTL INTERFACE

TTL signals can enter the Q24000 Series arrays from any I/O cell. Once on-chip, TTL signals are automatically converted to internal operating levels for logic operations. TTL outputs are available in bi-state or 3-state configurations.

TTL and ECL I/O can be mixed on each array yielding three basic configurations: TTL-only, mixed ECL/TTL (dual supply) and mixed ECL/TTL (single supply). Power supply requirements for each mode of operation are shown in Table 5. Representative TTL and TTLMIX I/O configurations are summarized in Table 8.

One quarter of the I/O cells on each channelled array can be configured to allow single cell bidirectional TTL operation. All single-cell bidirectional I/O cells are located along a single side of each array. For the channelless arrays, bidirectional TTL is achieved by tying two I/O cells together.

CMOS INTERFACE

CMOS signals can enter the Q24000 Series from any I/O cell. For driving CMOS logic devices, AMCC has designed special macros which can maintain the high noise margins of CMOS but with improved drive capability of bipolar. With AMCC's BiCMOS, complete flexibility to mix CMOS, ECL and TTL can be integrated on a single chip. Translators are no longer necessary, reducing board space requirements.

Table 8. Representative TTL Interface Macros

	Description	Cells	Maximum Delay (ns)[3]			Maximum Power (mW)[4]		
			Low Power	Standard	High Speed	Low Power	Standard	High Speed
SINGLE SUPPLY	INPUTS Noninverting	1	1.6	—	—	3.1	—	—
	OUTPUTS 2-Input	1		2.7	—	—	7.4	—
DUAL SUPPLY	INPUTS Noninverting	1	4.7	—	1.8	8.1	—	20.1
	OUTPUTS 2-Input OR	1		5.3	4.1	—	12.1	18.2
	3-state	1		5.5	4.3	—	21.3	27.3
	Bi-directional	1		5.9	—	—	44.0	—
	2-Input OR (8mA)	1		8.9	—	—	6.8	—
	3-state (8mA)	1		9.9	—	—	11.3	—

Notes:
1 Prop Delays are commercial max averaged, V_{EE} = -4.2V, T_J = 130°C under no load conditions.
2 At V_{EE} = -4.8V. Does not include I_{OEF}.
3 Prop Delays are commercial max averaged. V_{CC} = 4.75V, T_J = 130°C.
4 At V_{CC} = 5.25V.

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Figure 6. Load Circuit for 2-State Outputs

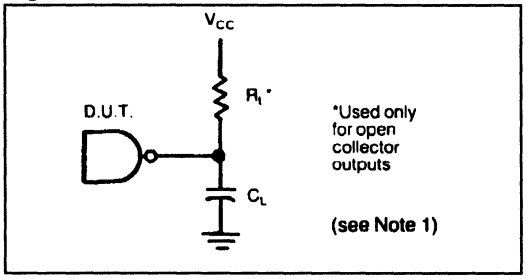


Figure 7. 2-State Waveform for Inverting Functions

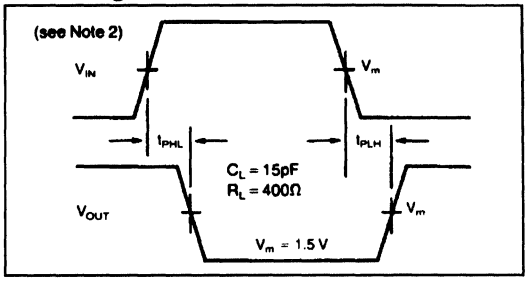


Figure 8. 2-State Waveform for Non-Inverting Functions

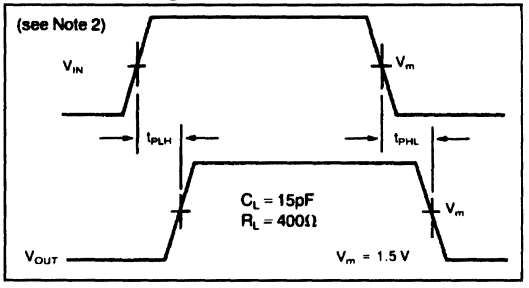


Figure 9. 3-State Low Level to High Level and Disable Time to Low Level

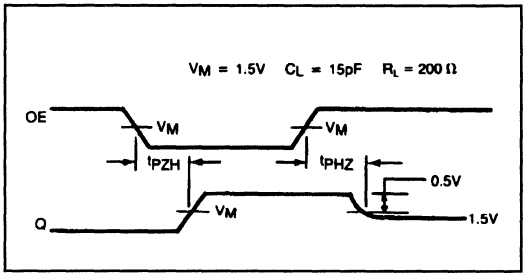


Figure 10. 3-State High Level to Disable and Disable Time to High Level

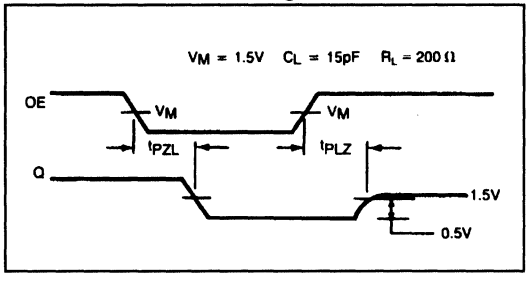


Figure 11. Load Circuit for 3-State Outputs

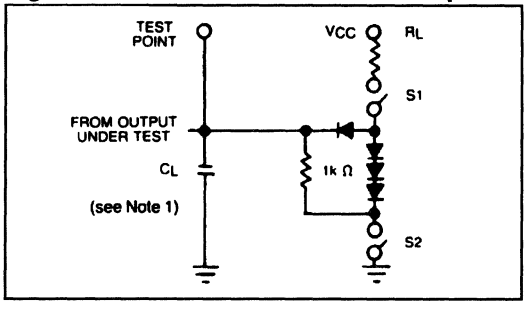


Table 9. 3-State Test Circuit Switch

Test Functions	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

Notes: 1 Standard TTL load circuit used for macro specification, see Figures 6 and 7. CL includes probe, jig and package.
2 V_{IN} = 0 to 3.0 volts.

8

INTERNAL LOGIC CELL CAPABILITIES

The Q24000 Series internal logic cells are all identical in structure and are positioned in uniform columns across the arrays. Each cell contains 16 CMOS and 4 bipolar uncommitted transistors along with 4 resistors. The cells are individually configurable to provide a variety of logic functions through the use of the Q24000 Series macro library. The macro library provides SSI, MSI and some basic LSI functions. The higher level macros provide the advantages of higher speed, lower power and increased circuit density over a logically equivalent SSI macro implementation.

Table 10 lists parameters for a number of representative Q24000 Series internal macros.

Table 10. Representative Internal Macros

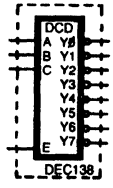
Description	Number of Cells	Maximum Delay (ns)[1]		Loaded Delay (ns)[2]	
		tpLH	tpHL	tpLH	tpHL
2-input NAND (DUAL)	1	.53	.45	.90	.82
3-input NAND	1	.79	.99	1.16	1.36
4-input NAND	1	.78	.84	1.15	1.21
2-input NOR (DUAL)	1	.81	.37	1.18	.74
3-input NOR	1	2.20	1.46	2.57	1.83
4-input NOR	1	1.88	1.72	2.25	2.09
Exclusive OR	1	1.01	0.75	1.38	1.12
Exclusive NOR	1	0.99	0.90	1.36	1.27
Latch with Reset					
$D \rightarrow Q$	1	1.68	1.47	2.05	1.84
$D \rightarrow \overline{Q}$		1.08	1.10	1.45	1.47
$C \rightarrow Q$		3.03	2.60	3.40	2.97
$C \rightarrow \overline{Q}$		2.24	2.41	2.61	2.78
D F/F with Reset					
$C \rightarrow Q$	2	1.80	2.04	2.17	2.41
$C \rightarrow \overline{Q}$		2.60	2.15	2.97	2.52
4:1 Mux					
Data → Y	2	2.01	1.70	2.38	2.07
Select → Y		2.27	2.29	2.64	2.66

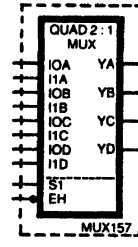
Notes: 1 Driving no loads, commercial max, V_{EE} = -4.8V, T_J = 130°C.
2 Driving 4 loads plus 4mm of metal, commercial max, V_{EE} = -4.8V, T_J = 130°C.

HARD MSI MACROS

In addition to basic macros, the Q24000 Series incorporates hard MSI macros for faster, more efficient designs. MSI macros can decrease design time by using large building-blocks rather than one-cell macros. Hard MSI macros are customized transistor level implementation of complex functions as opposed to "soft macros", which are gate-level implementation through logic equivalence. AMCC's hard macros have a distinct advantage over "soft macros" by 1) improving density in utilizing more transistors per cell 2) performance improvement due to optimized metal interconnect and 3) predictable delay characteristics from pre-determined layout constraints.

Typical MSI Macros





3:8 Decoder with Enable (6 Cells)

Delay Path	Maximum Delay (ns)[1]		Loaded Delay (ns)[2]	
	tpLH	tpHL	tpLH	tpHL
A,B,C → Y	2.11	2.31	2.48	2.68
Enable → Y	2.08	2.16	2.45	2.53

Quad 2:1 MUX (4 Cells)

Delay Path	Maximum Delay (ns)[1]		Loaded Delay (ns)[2]	
	tpLH	tpHL	tpLH	tpHL
I0, I1 → Y	1.83	1.56	2.20	1.93
S1 → Y	2.87	2.90	3.24	3.27

Notes: 1 Driving no loads, commercial max, V_{EE} = -4.8V, T_J = 130°C.
2 Driving 4 loads plus 4mm of metal, commercial max, V_{EE} = -4.8V, T_J = 130°C.

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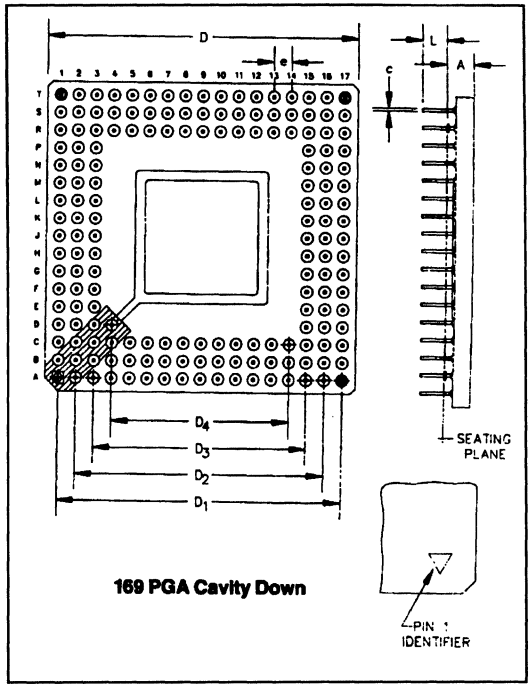
PACKAGING

The Q24000 Series logic arrays are available in a broad range of standard packages including surface mount chip carriers and pin grid arrays. Each package is custom designed by matching the bond finger layout to the power and ground locations of each AMCC BiCMOS array. Special attention has been paid to minimizing resistances and inductance on power and ground pins by using multi-layer construction for package power and ground planes. In addition, capacitance on signal pins has been minimized while consideration for low thermal resistance is designed into each BiCMOS package. For more details consult the AMCC Packaging Guide.



169 PGA Cavity Down

Table 11. Q24000 Series Standard Packaging

		Matrix/Maximum Signal I/O Count[1]				
Package	**Remarks**	**Q24008**	**Q24021**	**Q24060**	**Q24091**	**Q24140**
Leaded Quads						
44 J-lead	0.050 ctr	34[2]				
68 J-lead	0.050 ctr	42[2]				
84 leaded flatpack	0.050 ctr		62			
100 LDCC	0.050 ctr					
132 LDCC	0.025 ctr		78	90	90	90
196 LDCC	0.025 ctr				158	158
Pin Grid Arrays[3]						
68 PGA cavity down	0.100 center		46			
84 PGA	0.100 ctr		62			
100 PGA	0.100 ctr		78	66		
169 PGA	0.100 ctr			130	130	130
225 PGA	0.100 ctr				158	158
301 PGA	0.100 ctr				224	224

1 Signal I/O remaining after thermal diode (2-pins) is used. Adding power or ground pins may lower max signal I/O.
2 Approximate value, depends upon I/O mode and SSO requirements. Consult design manual.
3 All odd number PGAs include an additional pin for orientation.

Table 12.

Sym.	Inches (mm)	
	Max.	**Min.**
A	.165 (4.19)	.135 (3.43)
c	.020 (0.51)	.016 (0.41)
D	1.768 (44.91) sq.	1.732 (43.99) sq.
D1	1.605 (40.77) sq.	1.595 (40.51) sq.
D2	1.405 (35.69) sq.	1.395 (35.43) sq.
D3	1.205 (30.61) sq.	1.195 (30.35) sq.
D4	1.005 (25.53) sq.	.995 (25.27) sq.
e	.105 (2.67)	.095 (2.41)
L	.145 (3.68)	.115 (2.92)
S	.088 (2.224) sq.	.062 (1.58) sq.

Table 13. Pad to Pin Interconnection List

PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN	PAD	PIN
1	B1	26	L3	51	S7	76	S14	101	J18	126	B15	151	A5		D9		D6		D4
2	D3	27	M2	52	T6	77	U16	102	J17	127	A15	152	B5		D10		D7		D5
3	C2	28	N1	53	U6	78	T16	103	H18	128	C13	153	C6		J4		D8		D14
4	C1	29	N2	54	T7	79	S15	104	H17	129	B14	154	A4		J15		D11		D15
5	E3	30	M3	55	S8	80	U17	105	G18	130	A14	155	B4	VSS	K4		D12		E4
6	D2	31	P1	56	U7	81	T18	106	H16	131	C12	156	C5		K15		D13	VCC	E15
7	D1	32	P2	57	T8	82	R16	107	G17	132	B13	157	A3		R9		F4		P4
8	F3	33	N3	58	U8	83	S17	108	F18	133	A13	158	B3		R10		F15		P15
9	E2	34	R1	59	T9	84	S18	109	F17	134	B12	159	C4		C9		G4		R4
10	E1	35	R2	60	U9	85	P16	110	G16	135	C11	160	A2		C10		G15		R5
11	G3	36	P3	61	U10	86	R17	111	E18	136	A12				J3		H4		R14
12	F2	37	S1	62	T10	87	R18	112	E17	137	B11			VEE	J16	VDD	H15		R15
13	F1	38	S2	63	U11	88	N16	113	F16	138	A11				K3		L4		A1
14	G2	39	R3	64	T11	89	P17	114	D18	139	B10				K16		L15		A18
15	H3	40	T1	65	U12	90	P18	115	D17	140	A10				S9		M4		B2
16	G1	41	U2	66	S11	91	M16	116	E16	141	A9				S10		M15		B17
17	H2	42	S4	67	T12	92	N17	117	C18	142	B9						N4		C3
18	H1	43	T3	68	U13	93	N18	118	C17	143	A8						N15		C16
19	J2	44	U3	69	T13	94	M17	119	D16	144	B8						R6		E5
20	J1	45	S5	70	S12	95	L16	120	B18	145	A7						R7	None	S3
21	K1	46	T4	71	U14	96	M18	121	A17	146	C8						R8		S16
22	K2	47	U4	72	T14	97	L17	122	C15	147	B7						R11		T2
23	L1	48	S6	73	S13	98	L18	123	B16	148	A6						R12		T17
24	L2	49	T5	74	U15	99	K17	124	A16	149	B6						R13		U1

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DESIGN INTERFACE

AMCC has structured its circuit design interface to provide maximum flexibility without compromising design correctness. For implementations using an engineering workstation, AMCC provides MacroMatrix software. MacroMatrix works in conjunction with the most popular workstations to provide the following capabilities:

- Schematic Capture & Logic Synthesis
- Logic Simulation
- Pre-Layout Delay Estimation
- Array and Technology-Specific Rules Checks
- Estimated Power Computation
- Preliminary Package Pinouts

Upon submission of the design database to AMCC, a comprehensive review of the circuit is performed making use of the same EWS and MacroMatrix tools used by the designer. No translation of the logic data is required so the chance of non design-related errors is virtually eliminated.

CUSTOM MACROS

To further enhance the functionality of the Q24000 Series macro library, AMCC has developed MDS. Macro Development System (MDS) uses a "correct by construction" approach to develop macros that meet all the pertinent design rules. As individual circuit applications warrant, macros with unique characteristics can be developed rapidly and used to optimize the array design.

BICMOS EVALUATION KIT

AMCC has developed the BiCMOS Evaluation Kit to facilitate reliable assessment of the Q24000 Series BiCMOS Logic Arrays. The Evaluation Kit consists of a Q24021 Design Verification Chip, multi-layer high performance board, miniature coax cables and 50 ohm input terminators. The user need not develop a test board or special hardware to use the Evaluation Kit. Evaluation features include:

- ECL I/O Pair Delay
- TTL I/O Pair Delay
- D Flip-Flop Toggle Frequency
- D Flip-Flop Set-Up and Hold Time
- Ring Oscillators for Internal Macro Delays
- Fanout Delay Loading Penalty
- Metal Delay Loading Penalty
- Simultaneous Switching Outputs

Evaluation Kits are available through AMCC's Regional Sales Manager

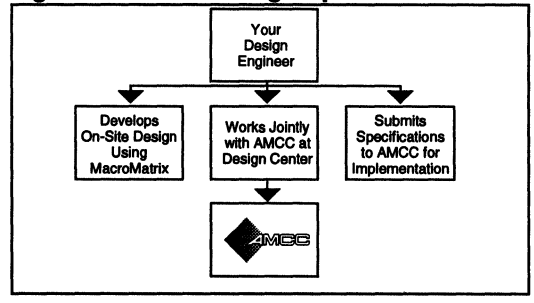
AMCC DESIGN SERVICES

In addition to supporting design work at the designer's location, AMCC also offers customers the option of working at the San Diego Design Center. At the Design Center, engineers have access to the same sophisticated CAE/CAD tools supported for customer site designs plus direct contact with a dedicated applications engineer to assist with the array implementation.

AMCC also provides a number of additional support services including:

- Full Design Implementation Service
- Local and Factory Applications Engineering Support
- Comprehensive Training Courses
- Complete Design Documentation

Figure 12. AMCC Design Options



RELIABILITY

Reliability is created through stringent design reviews followed by vigorous characterization and qualification testing of new products and processes. Prior to building first customer designs, AMCC institutes high temperature operating life testing to achieve a high equivalent number of device hours. During production, life testing and thermal stress testing are run on production released designs to ensure that reliability of the proven design is maintained. The ongoing Rel Program monitors the quality and reliability of production released products manufactured by AMCC. Samples are chosen from normal military and commercial hi-rel production device runs. From the accumulated data, device family reliability data can be estimated by using the Arrhenius equation model. Specific information about test conditions and activation energy assumptions are available from AMCC's reliability brochure.

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Recommended Operating Conditions – Commercial

Parameter	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC}=0				
10K, 10KH Mode	-4.94	-5.2	-5.46	V
100K Mode	-4.2	-4.5	-4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

Recommended Operating Conditions – Military

Parameter	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC}=0				
10K, 10KH Mode	-4.7	-5.2	-5.7	V
100K Mode	-4.2	-4.5	-4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	-55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* -5.7V is possible. Consult AMCC for ECL 100K DC parametrics operating at this voltage.

Absolute Maximum Ratings[1]

ECL Supply Voltage V_{EE} (V_{CC} = 0)	-8.0 VDC
ECL Input Voltage (V_{CC} = 0)	GND to V_{EE}
ECL Output Source Current (continuous)	-50mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0V
TTL Input Voltage (V_{EE} = 0)	5.5V
Operating Temperature	-55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	-65°C to + 150°C

1 Long term exposure at these limits may result in permanent damage to the circuits. Actual circuit operation at these conditions is not recommended nor implied.

AC Electrical Characteristics

Symbol	Parameter		Test Conditions	COM 0°/+70°C		MIL -55°/+125°C		Unit
				MIN	MAX	MIN	MAX	
t_{IPD}-ECL	ECL Input Propagation Delay Including Buffer	Standard	3 loads		4.3		4.6	ns
		High Speed	3 loads		1.6		1.7	ns
t_{IPD}-TTL	TTL Input Propagation Delay Including Buffer (Std.)	Low Power	3 loads		4.7		5.1	ns
		High Speed	3 loads		1.8		1.9	ns
t_{OPD}-ECL	ECL Output Propagation Delay				0.8		0.9	ns
t_{OPD}-TTL	TTL Output Propagation Delay	Standard	15 pf		6.3		6.8	ns
		High Speed	15 pf		5.2		5.5	ns
t_{FPD}	Internal Gate Delay		2 loads +2mm of metal		0.62		0.75	ns
F_{maxt}	Maximum Internal Flip/Flop Toggle Frequency				210		180	MHz
F_{in}-ECL	ECL Input Frequency at Package Pin	Standard	3 loads		160		135	MHz
		High Speed	3 loads		210		180	MHz
F_{out}-ECL	ECL Output Frequency at Package Pin		50Ω		210		180	MHz
F_{in}-TTL	TTL Input Frequency at Package Pin	Low Power	3 loads		35		30	MHz
		Standard	3 loads		65		60	MHz
F_{out}-TTL	TTL Output Frequency at Package Pin	Low Power	15 pf		50		45	MHz
		Standard	15 pf		65		60	MHz
t_{PZH}	Enable time to high level		Fig. 9		12.3		13.0	ns
t_{PZL}	Enable time to low level		Fig. 10		12.3		13.0	ns
t_{PHZ}	Disable time from high level		Fig. 9		12.3		13.0	ns
t_{PLZ}	Disable time from low level		Fig. 10		12.3		13.0	ns

ECL 10K Input/Output DC Characteristics V_{EE} = -5.2V[1]

	$T_{ambient}$				T_{case}	
	-55°C	0°C	25°C	75°C	125°C	Unit
V_{OHmax}	V_{CC}-850	V_{CC}-770	V_{CC}-730	V_{CC}-650	V_{CC}-575	mV
V_{IHmax}[5]	V_{CC}-800	V_{CC}-720	V_{CC}-680	V_{CC}-600	V_{CC}-525	mV
V_{OHmin}	V_{CC}-1080	V_{CC}-1000	V_{CC}-980	V_{CC}-920	V_{CC}-850	mV
V_{IHmin}[5]	V_{CC}-1255	V_{CC}-1145	V_{CC}-1105	V_{CC}-1045	V_{CC}-1000	mV
V_{ILmax}[5]	V_{CC}-1510	V_{CC}-1490	V_{CC}-1475	V_{CC}-1450	V_{CC}-1400	mV
V_{OLmax}	V_{CC}-1655	V_{CC}-1625	V_{CC}-1620	V_{CC}-1585	V_{CC}-1545	mV
V_{OLmin}	V_{CC}-1980	V_{CC}-1980	V_{CC}-1980	V_{CC}-1980	V_{CC}-1980	mV
V_{ILmin}[5]	V_{CC}-2000	V_{CC}-2000	V_{CC}-2000	V_{CC}-2000	V_{CC}-2000	mV
I_{IH}[2]MAX	30	30	30	30	30	µA
V_{IL}[2]MAX	-.5	-.5	-.5	-.5	-.5	µA

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ECL 100K Input/Output DC Characteristics V_{EE} = -4.5V[3]

Symbol	Parameter	Test DC Conditions	Comm 0°/+70°C			MIL -55°/+125°C			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to -2V	V_{CC}–1035		V_{CC}–850	V_{CC}–1080		V_{CC}–835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to -2V	V_{CC}–1900		V_{CC}–1605	V_{CC}–2000		V_{CC}–1595	mV
V_{IH}	Input Voltage HIGH	Maximum Input Voltage HIGH	V_{CC}–1145		V_{CC}–800	V_{CC}–1145		V_{CC}–800	mV
V_{IL}	Input Voltage LOW	Maximum Input Voltage LOW	V_{CC}–1950		V_{CC}–1475	V_{CC}–2000		V_{CC}–1475	mV
I_{INL}[2]	Input Current LOW	$V_{IN} = V_{IL}$ min			-0.5			-0.5	µA
I_{IH}[2]	Input Current HIGH	$V_{IN} = V_{IH}$ max			30			30	µA

TTL Input/Output DC Characteristics

Symbol	Parameter	Test DC Conditions		Comm 0°/+70°C			Mil -55°/+125°C			Unit
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}[5]	Input Voltage HIGH	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IL}[5]	Input Voltage LOW	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18MA			-.8	-1.2		-.8	-1.2	V
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = -1MA		2.7	3.4		2.4	3.4		V
V_{OL}	Output Voltage LOW	V_{CC} = Min,	I_{OL} = 8MA			0.5			0.5	V
			I_{OL} = 20MA			0.5			0.5	V
			I_{OL} = 48MA			0.6			0.6	V
I_{OZH}	Output "off" Current HIGH (3–state)	V_{CC} = Max, V_{OUT} = 2.4V		-50		50	-50		50	µA
I_{OZL}	Output "off" Current LOW (3–state)	V_{CC} = Max, V_{OUT} = 0.4V		-50		50	-50		50	µA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_{IN} = 2.7V				50			50	µA
I_I	Input Current HIGH at Max	V_{CC} = Max, V_{IN} = 5.5V				1.0			1.0	mA
I_{IL}[6]	Input Current LOW	V_{CC} = Max, V_{IN} = 0.5V				50			50	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-25		-100	-25		-100	mA

1 Data measured with V_{EE} = -5.2 ± .1V (or V_{CC} = 5.0 ± .1V for +5V ref. ECL 10K assuming a +50°C rise between ambient (T_a) and junction temperature (T_J) for -55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with TJ for packages and operating conditions.

2 Per fan-in.

3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.

4 Typical limits are at 25°C, V_{CC} = 5.0V.

5a These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

5b Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

6 For standard speed options only.

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BiCMOS LOGIC ARRAY WITH PHASE-LOCKED LOOP Q24P008

FEATURES

- On-chip phase-locked loop with VCO operating at 160 to 320 MHz
- 720 gates of customizable digital logic
- Support for up to 10 TTL outputs at up to 80 MHz
- Support for PECL and ECL outputs up to 210 MHz
- TTL outputs have less than 400 ps maximum skew (with balanced routing and loading)
- Utilizes proven Q24000 Series macro library
- TTL, CMOS and +5V ECL capability
- Speed/power programmable I/O macros
- Maximum 1 ns of phase error
- Up to 100% gate utilization of digital logic
- Typical power less than 1 Watt
- 28/44/68 PLCC, 44 LDCC, 44/68 Ceramic J-Lead Cerquad, 52 PQFP packages

APPLICATIONS

- Clock generation and distribution
- Frequency synthesis
- CMOS ASIC system clock deskewing
- High-speed microprocessor systems
- Backplane clock deskew and distribution

GENERAL DESCRIPTION

The AMCC Q24P008 logic array combines proven AMCC 1.0 micron BiCMOS logic array technology with an internal phase-locked loop to provide a high performance, low power solution for synchronous clock generation, distribution, and deskewing applications.

Use of a simple off-chip filter allows an entire 160 to 320 MHz phase-locked loop (PLL) to be implemented on-chip. Utilizing the PLL, the Q24P008 supplies sufficient resources to support the generation of up to 10 TTL outputs operating at frequencies of up to 80 MHz. ECL or PECL output levels can be used for frequencies up to 210 MHz. Custom I/O levels can also be implemented in a custom output macro for non-standard or low-swing I/O interfaces. TTL outputs with less than ± 200 ps of maximum skew (implementation dependent, based on equal loading) are available, and a test enable input allows users to bypass the VCO and provide their own external clock.

An extensive library of SSI and MSI logic macros is available for use on the digital portion of the array, in conjunction with the rest of AMCC's MacroMatrix® design kit. Using the library elements, functions can easily be assembled to operate with the phase-locked loop to meet specific application needs. MacroMatrix is available for use with today's leading EWS and CAE tools.

PERFORMANCE SUMMARY	
Parameter	**Value**
Phase-Locked Loop	
VCO Operating Frequency	160–320 MHz
Maximum Phase Error	1 ns
Loop Acquisition Time (typ)	500 µs
Input Reference Freq. Range	10–80 MHz
Digital	
Typical Gate Delay	310–400 ps
Max. Int. Toggle Frequency	280 MHz
Typical TTL Input Delay	3.0 ns
Typical ECL Input Delay	1.3 ns
Typical TTL Output Delay	2.2 ns
Typical ECL Output Delay	0.6 ns
ECL Compatible Output Drive	25 Ohm 50 Ohm
TTL Compatible Output Drive	8, 20, 24 mA

PRODUCT SUMMARY	
Equivalent Gates – Flip Flop Method	720
Internal Logic Cells	180
I/O Pads	34
PLL-Related Pads	9
Fixed Power/Ground Pads (Digital)	6
Total Pads	49
Typical Power Dissipation	< 1W

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THIS DEVICE SPECIFICATION IS AN ADDENDUM TO THE Q24000 SERIES DATA SHEET. REFER TO THAT DOCUMENT FOR ADDITIONAL INFORMATION.

NOTES

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FAX: 919/848-1787

NORTH AMERICAN SALES REPRESENTATIVES

NORTH DAKOTA

Customer 1st
8841 East Research Center Road
New Hope, MN 55428
Tel: 612/533-5604
FAX: 612/533-5632, Ext. 0364

OHIO

Norm Case Associates
21010 Center Ridge Road
Rocky River, OH 44116
Tel: 216/333-0400
FAX: 216/333-0403

OKLAHOMA

Logic 1 Sales, Inc.
200 East Spring Valley
Suite A
Richardson, TX 75081
Tel: 214/234-0765
FAX: 214/669-3042

OREGON

Components West
16300 SW Hart Road
Suite G
Beaverton, OR 97007
Tel: 503/642-9110
FAX: 503/642-9592

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(Pittsburgh Area)
Norm Case Associates
21010 Center Ridge Road
Rocky River, OH 44116
Tel: 216/333-0400
FAX: 216/333-0403

Delta Technical Sales, Inc.
122 N. York Road
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Hatboro, PA 19040
Tel: 215/957-0600
FAX: 215/957-0920

RHODE ISLAND

CompRep Associates
100 Everett Street
Westwood, MA 02090
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9111 Jollyville Road
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Tel: 512/345-2952
FAX: 512/346-5309

Logic 1 Sales, Inc.
4606 FM 1960 West
Suite 320
Houston, TX 77069
Tel: 713/444-7594
FAX: 713/444-8236

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First Source
2688 Willow Bend Drive
Sandy, UT 84093
Tel: 801/943-6894
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100 Everett Street
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541 Dunkirk Road
Baltimore, MD 21212
Tel: 410/377-4788
FAX: 410/377-4789

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Components West
4020 148th Avenue, N.E.
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Tel: 206/885-5880
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WISCONSIN

Phase II Marketing
11040 West Bluemond Road
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Customer 1st
2950 Metro Drive
Suite 110
Bloomington, MN 55425
Tel: 612/851-7909
FAX: 612/851-7907

AMCC EUROPE & ISRAEL

AM&T, Ltd.
Saville Court, Saville Place
Clifton, Bristol BS8 4EJ
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Tel: 44/272-237-594
FAX: 44/272-237-598

UNITED KINGDOM

AMEGA Electronics, LTD.
Loddon Business Centre
Roentgen Road
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Tel: 44/256-843-166
FAX: 44/256-842-956

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Nagano 386, Japan
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SEBO Trading Company
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408-14, Seokyo-Dong,
Mapo-Ku
Seoul, Korea
Tel: 82/2-326-0854
FAX: 82/2-326-0856

MALASIA

Gates Engineering, PTE, Ltd.
1 Syed Alwi Road. #0402
Song Lin Building
Singapore, 0820
Tel: 65/299-9937
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Johnson Trading & Engineering Co.
10F-3, 293, Sec. 2
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Tel: 88/62-7331211
FAX: 88/62-7336889

NOTES

Applied Micro Circuits Corporation
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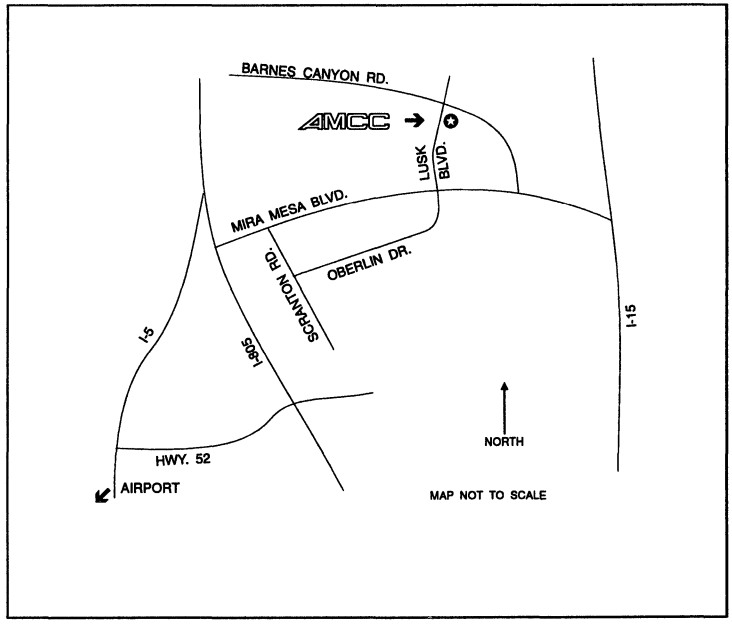

From the airport take I-5 north to Hwy. 52 east to I-805 north.
Exit at Mira Mesa Blvd. to Lusk Blvd.

Corporate Headquarters Address:

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