Advanced Micro Devices, Inc.

The 8080A/9080A MOS Microprocessor Handbook

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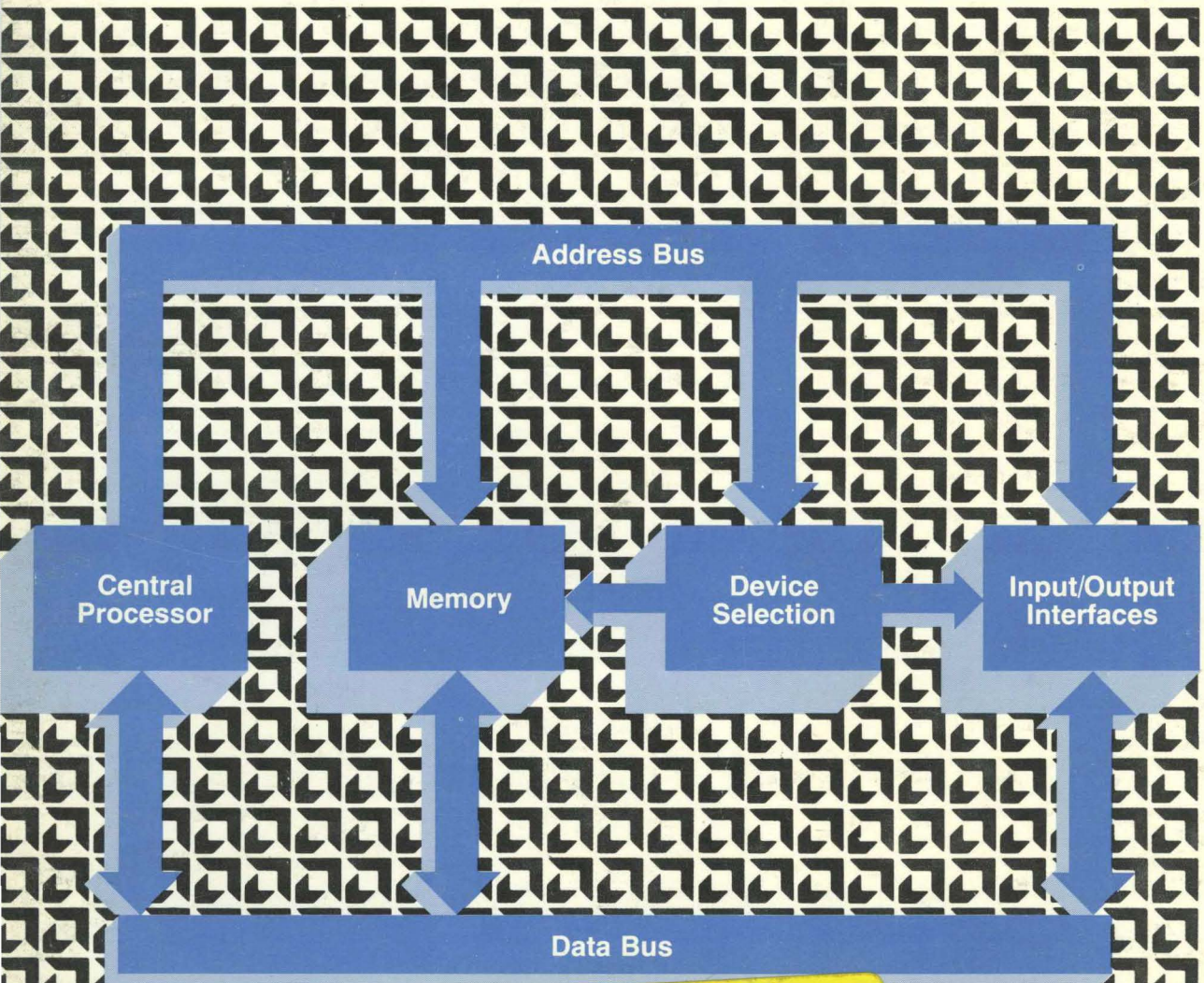

Advanced Micro Devices

The 8080A/9080A MOS MICROPROCESSOR HANDBOOK

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Chapter 1
INTRODUCTION

Of all the results of the development of large-scale integrated (LSI) circuit technology, none is having as much impact as the microprocessor. Since the introduction of the first 8-bit monolithic microprocessor in 1972, the influence of these devices has become increasingly pervasive. The trends clearly indicate that we can look forward to the appearance of microprocessors in more and more applications.

Advances in both bipolar and metal-oxide-semiconductor (MOS) processing and technology have resulted in the evolution of two distinct types of microprocessor circuit elements. The monolithic MOS devices, such as the 8080A/9080A, provide moderate performance, high density and low power — usually in the form of a fixed instruction architecture. Bipolar devices, like the Am2901, on the other hand, make use of the very high performance available to implement microprogrammed architectures, with their concomitant flexibility. Density and power constraints have led to the development of "bit-slice" bipolar devices which use multiple chips to obtain the data word length required by a specific application.

Advanced Micro Devices occupies a unique position in the industry in that both mainstream microprocessor chip sets are supported by the company. The 8080A/9080A, industry standard, 8-bit MOS microprocessor family of devices is described in this handbook. Other publications available from AMD describe the widely used Am2900 bipolar family.

Despite the wide publicity being given to the microprocessor, and despite the tremendous amount of material being published, there is a surprising lack of detailed technical information available to the system designer. Unfortunately, many designers have found that the sort of information which they need is not readily available. That is the area which this handbook addresses. It is not another introduction to microprocessors, for which the reader is referred to the many publications addressing that general requirement. Rather, it is an attempt to introduce the microcomputer system designer to the 8080A/9080A family of devices and offer some detailed design information to the designer already familiar with these circuits.

Soon after the microprocessor was introduced, it became clear that one key to their application lay in support circuits. Early microcomputer designs required so many additional devices to make them useful that a substantial portion of the potential benefit was lost. Since that time, much work has been done in developing support circuits which greatly reduce the package count in microcomputer systems. It is this development, which is continuing at a rapid pace, as much as the dramatic decrease in the price of microprocessors, which has fueled the explosive growth in their utilization.

In addition to the standard 8080A/9080A family support circuits shown at the end of this chapter, Advanced Micro Devices is a leading manufacturer of standard Low-power Schottky MSI circuits. These products seem likely to have as profound an impact on microprocessor system design as they have had in TTL logic design. They offer further reduction in package count and power dissipation with no sacrifice in performance. Several of these devices which are particularly well suited to microcomputer design are included in the table and described in more detail later in the handbook. Another product area of critical importance to the microcomputer system designer is memories. Several configurations of 1K and 4K static read/write memories (RAMs) are available in addition to dynamic types. Also described are various read only memories, both mask programmed and erasable.

Presented in the following chapters of this handbook are detailed descriptions of the Am9080A central processing unit and the associated clock generator and system controllers. Three important input/output interfaces are then presented followed by two groups of support circuits. Following these will be found a chapter on memory devices and a selection of application notes.

Additional technical information regarding all AMD products may be obtained from local Field Applications Engineers or from factory Applications Groups.

MICROPROCESSOR & SUPPORT CIRCUITS

AMD Part Number	Description	Availability
	CPU	
Am9080A/−2/−1/−4	0 to + 70°C	Now
Am9080A/−2/−1	−25 to +85°C	Now
Am9080A/−2	−55 to +125°C	Now
	STATIC READ/WRITE RANDOM ACCESS MEMORIES	
Am91L01A/B/C/D	256 x 4, 22 Pin	Now
Am91L01A/B/C	256 x 4, 22 Pin	Now
Am9102A/B/C/D	1K x 1, 16 Pin	Now
Am91L02A/B/C	1K x 1, 16 Pin	Now
Am9111A/B/C/D	256 x 4, 18 Pin	Now
Am91L11A/B/C	256 x 4, 18 Pin	Now
Am9112A/B/C/D	256 x 4, 16 Pin	Now
Am91L12A/B/C	256 x 4, 16 Pin	Now
Am9131A/B/C/D/E	1K x 4, 22 Pin	Now
Am91L31A/B/C/D	1K x 4, 22 Pin	Now
Am9141A/B/C/D/E	4K x 1, 22 Pin	Now
Am91L41A/B/C/D	4K x 1, 22 Pin	Now
	DYNAMIC READ/WRITE RANDOM ACCESS MEMORIES	
Am9050C/D/E	4K x 1, 18 Pin	Now
Am9060C/D/E	4K x 1, 22 Pin	Now
	MASK PROGRAMMABLE READ-ONLY MEMORIES	
Am9208B/C/D	1K x 8, 250 nsec max	Now
Am9216B/C	2K x 8, 300 nsec max	Now
Am8316A	2K x 8, 850 nsec max	Now
Am8316E	2K x 8, 550 nsec max	Now
	ERASABLE READ-ONLY MEMORIES	
Am1702A	256 x 8, 1.0 μsec	Now
Am2708	1K x 8, 450 nsec	1st Q 1977

CPU: 9080A = 480 nsec 2 = 380 nsec -1 = 320 nsec −4 = 250 nsec
MEM: A = 500 nsec. B = 400 nsec C = 300 nsec D = 250 nsec E = 200 nsec

AMD Part Number	Description	Availability
	SECOND SOURCE SUPPORT	
Am8212	8-bit I/O Port	Now
Am8216	Non-Inverting Bus Transceiver	Now
Am8224	Clock Generator	Now
Am8226	Inverting Bus Transceiver	Now
Am8228	System Controller	Now
Am8238	Extended Write System Controller	Now
Am8251	Prog. Communications Interface	Now
Am8255	Prog. Peripheral Interface	Now
Am8257	Direct Memory Access Controller	3rd Q 1977

	IMPROVED SUPPORT		
		REPLACES	
Am8224-4	High-Speed Generator	N/A	Now
Am8238-4	High-Speed System Controller	N/A	Now
Am9511	Arithmetic Processing Unit	N/A	3rd Q 1977
Am9517	Multi-mode DMA Controller	8257	3rd Q 1977
Am9519	Universal Interrupt Controller	8259	3rd Q 1977
Am9551/−4	Prog. Communications Interface	8251	Now
Am9555/−4	Prog. Peripheral Interface	8255	Now
Am25LS138	1-of-8 Decoder	8205	Now
Am25LS139	Dual 1-of-4 Decoder	8205	Now
***Am25LS273**	8-bit Common Clear Register	N/A	2nd Q 1977
***Am25LS373**	8-bit Transparent Latch	8212	4th Q 1977
***Am25LS374**	8-bit 3-State Register	8212	Now
***Am25LS377**	8-bit Common Enable Register	8212	2nd Q 1977
***Am25LS2513**	Priority Encoder	8214 & 8212	Now
***Am25LS2537**	1-of-10 3-State Decoder	8205 (2)	Now
***Am25LS2538**	1-of-8 3-State Decoder	N/A	Now
***Am25LS2539**	Dual 1-of-4 3-State Decoder	N/A	Now

*All combine high performance and low power in space saving 20-pin package

Chapter 2
8080A/9080A FUNCTIONAL DESCRIPTION

The Am9080A family of devices are complete, general-purpose, monolithic digital processors with a fixed instruction set and 8-bit parallel arithmetic logic and registers. The entire Arithmetic and Logic Unit, internal registers and instruction decoding and execution logic are contained within the microprocessor, which is pin and function compatible with the 8080A. The Am9080A versions feature improvements resulting from the use of the latest in N-channel, silicon gate, Ion-implanted Metal-Oxide Semiconductor technology.

Four versions of the Am9080A are currently offered, providing instruction cycle times of 2, 1.5, 1.3 and 1.0 μsec. In addition to providing the highest speed 8080A compatible device available, the improved processing technology provides significantly smaller products that dissipate much less power than the original 8080A. Features of the Am9080A microprocessors include:

- Full functional replacement for 8080A, 8080A-1, 8080A-2.
- Maximum power dissipation of 829 milliwatts.
- Instruction cycle times to 1 μsec.
- Military versions for full temperature range with a 2.0 and a 1.5 μsec instruction cycle time.
- 3.2 mA of sink current capability on output connections.
- 100% reliability assurance testing to MIL-STD-883 standard on all products, commercial or military.

FUNCTIONAL ORGANIZATION OF THE Am9080A CPU

Three groups of signals are provided by the Am9080A to transmit data and controls between the Central Processing Unit, memory and input/output logic. The first is an 8-bit parallel Data Bus; its function is to transmit both instructions and data to and from the CPU. A 16-bit Address Bus identifies any one of 65,536 (64K) memory locations during a memory access operation. The Address Bus may also be used to address peripheral devices during the execution of input/output

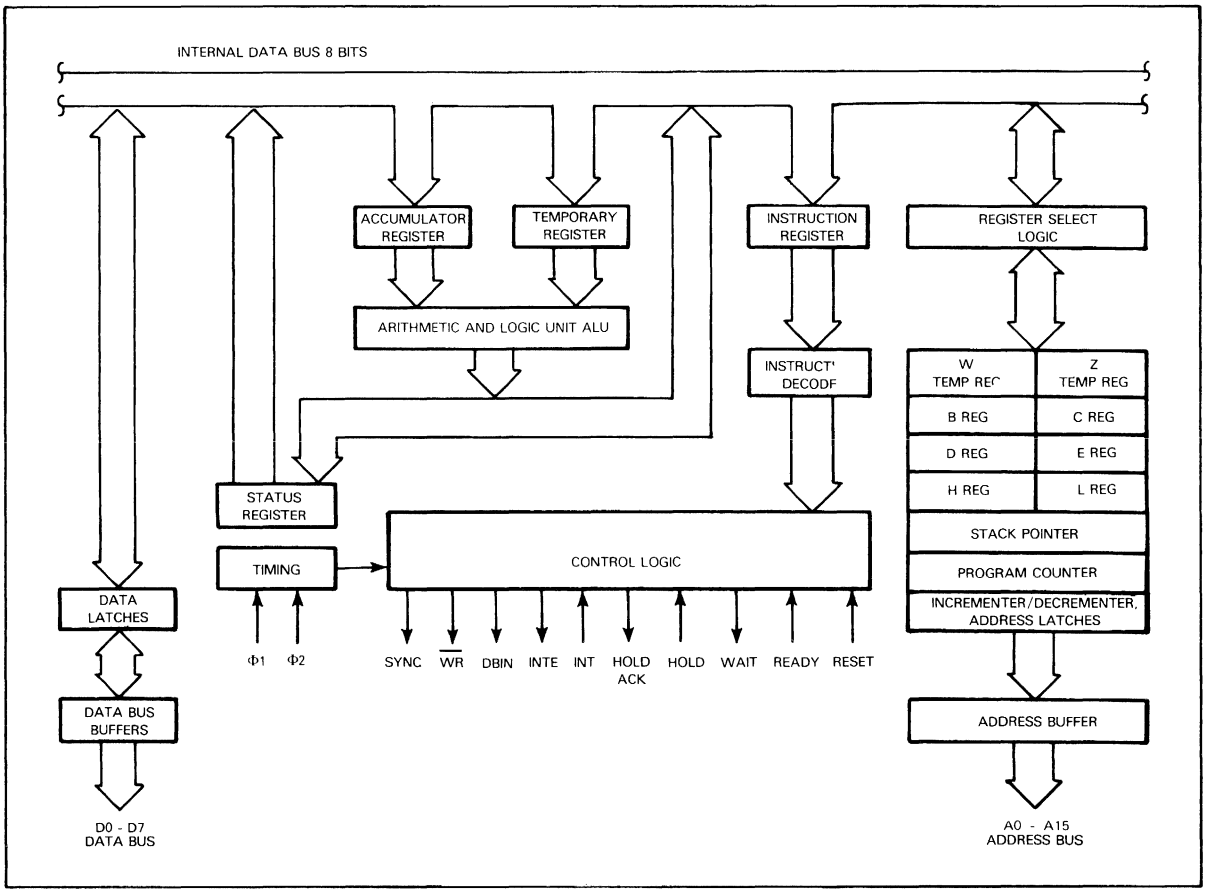


FIGURE 2-1 Am9080A FUNCTIONAL BLOCK DIAGRAM

instructions. The third group of signals includes ten control lines to synchronize the operation of the CPU with memory and input/output logic.

As illustrated in Figure 2-1, the 9080A microprocessor contains control and data processing logic.

Control Logic

Control logic coordinates the sequences of operations that are performed on a step-by-step basis as clock pulses are applied to the microprocessor. The data processing functions operate on the data in accordance with whatever instruction is being executed by the microprocessor.

The Instruction Register, Instruction Decoder, Timing, and Control Unit comprise the control logic of the microprocessor.

The Instruction Register receives those contents of the Data Bus which are obtained from memory during the first machine cycle of every new instruction. This 8-bit value is interpreted as the operation code (opcode) of an instruction. The Instruction Decoder monitors the outputs of the Instruction Register and establishes the sequence of events that follow. This sequence of events constitutes execution of the remainder of the instruction. For example, if the byte loaded into the Instruction Register during the first machine cycle is interpreted as the first byte of a 2-byte instruction, then the necessary control sequences will be established to cause a second memory access during the next machine cycle, to obtain the second byte of the instruction. The Instruction Decoder will then cause the contents of the data byte obtained during the second machine cycle to be routed to the appropriate internal logic so as to cause the desired function to be executed. The Timing and Control Logic generates the internal and external timing sequences necessary for controlling operations of the CPU.

Registers

The register section of the processor consists of:

- An 8-bit Accumulator
- A Status Register
- Two Temporary Registers, W and Z
- Three register pairs consisting of Registers B and C, D and E, H and L
- A Stack Pointer
- A Program Counter

The Accumulator is the primary source and destination for data being operated on by the Arithmetic and Logic Unit (ALU). ALU operations also modify Status Register bits; Status Register bits can be tested by the program being executed in order to define subsequent conditional logic.

The Temporary Registers hold values used during the execution of certain instructions. They are transparent to the programmer in that no instructions specifically address these registers as a source or destination.

Some instructions access the general register pairs independently as 8-bit registers; other instructions link them together as 16-bit register pairs (B and C, D and E, H and L).

The 16-bit Stack Pointer allows the programmer to reserve any area within the 64K bytes of Memory Space for use as a Last In/First Out (LIFO) stack memory. This permits efficient handling of program subroutines and intermediate storage of data.

The Stack Pointer maintains the address of the next available stack location in memory. Whenever information is pushed onto the stack, the Stack Pointer is incremented, and when information is removed from the stack, the Stack Pointer is decremented. This organization of the Stack in general purpose memory allows the programmer to construct system software with an indefinite number and depth of stacks. The Stack program memory and data memory usually share a memory space; however, it is possible to create a separate addressable memory space solely for the use of the stack.

The Program Counter provides a 16-bit address that always points to a memory location from which the next instruction object code byte will be obtained. The Program Counter is automatically incremented after each instruction byte is fetched, thereby pointing to the next sequential memory location. Some instructions modify the Program Counter contents by inserting a new 16-bit address, thereby causing the next instruction byte to be obtained from a non-sequential location.

Arithmetic and Logic Unit (ALU)

The Arithmetic and Logic Unit contains all logic which performs operations on data. Registers whose data contents are operated on are included within the Arithmetic and Logic Unit; these include the Accumulator, the Status Register, an Accumulator latch and a Temporary Register.

The Accumulator is a programmable register which has been described; it is the primary source and destination for data operated on by the ALU; however, actual data operations are performed on the contents of Accumulator latches. The Temporary Register holds operands that are not stored in an addressable register.

INTERFACE SIGNALS

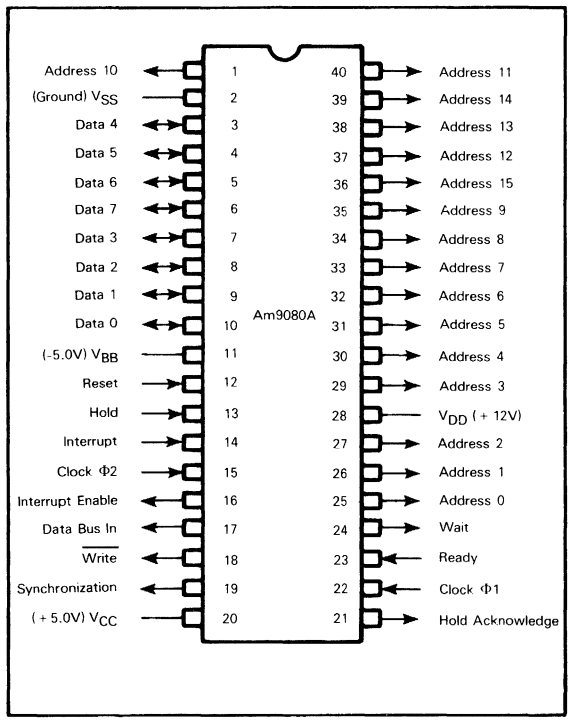


FIGURE 2-2 8080A/9080A CONNECTION DIAGRAM

The interface signals and connections to the Am9080A are shown in Figure 2-2.

Power

Four connections are provided for applying power to the Am9080A CPU:

V_{SS}	Pin 2	0 Volts
V_{BB}	Pin 11	-5 Volts
V_{CC}	Pin 20	+ 5 Volts
V_{DD}	Pin 28	+ 12 Volts

Inputs

Clocks (Φ1, Φ2; Input)

A two-phase nonoverlapping clock system is used to provide the basic timing for the Am9080A CPU. These are the only high level signals required by the processor and are conveniently provided by the Am8224 Clock Generator.

Reset (RESET, Input)

The Reset signal is used to initialize the microprocessor by performing the following seven functions:

1) Suspends all normal internal operations.
2) Clears the Program Counter.
3) Clears the Instruction Register.
4) Clears the INTE flip-flop.
5) Clears the HLDA flip-flop, thereby removing the microprocessor from a Hold state.
6) Clears the Halt state.
7) Forces the timing generator to assume the M1, T1 state when Reset is removed.

General registers within the CPU are not cleared when Reset is activated. The Reset line must be activated for a minimum of three full clock periods.

Hold (HOLD, Input)

The HOLD signal causes the CPU to enter the Hold state. The Hold state places Data and Address Busses in the high impedance state. This allows external circuits such as Direct Memory Access controllers to utilize the Data and Address Busses for purposes of transferring information to or from memory or I/O circuits, without CPU intervention.

Interrupt (INT, Input)

INT is the interrupt request signal. This signal can be used by external devices to notify the CPU that they require service.

Ready (READY, Input)

The READY input provides a means for the Central Processing Unit to enter a Wait state and allow extra time for external circuits to respond to requests by the processor. The signals applied by the CPU to the Address and Data Busses are maintained during the Wait state. The Ready signal may be held at the low level indefinitely, the processor remaining in the Wait state until the end of the Φ1 clock cycle after Ready becomes active.

Data 0 - Data 7 (D0 - D7, Bidirectional)

The eight data lines, D0 through D7, are multiplexed bidirectional data lines over which both data and controls are transferred between the CPU and external circuits. The Data Bus drivers within the CPU are placed in the high impedance state before data are transmitted from external devices to the CPU.

Outputs

Address 0 - Address 15 (A0 - A15, Output)

The 16 address lines A0 through A15, provide for accessing up to 65,536 (64K) possible memory locations. The low order eight bits, A0 through A7, and the high order eight bits, A8 through A15, are used also for addressing one of 256 input or output ports. When the Input or Output instructions are executed, an 8-bit I/O port address appears at both the low and high order eight bits.

Interrupt Enable (INTE, Output)

The INTE signal indicates the state of the interrupt enable flip-flop contained in the CPU logic. It indicates whether the CPU will recognize interrupts or not. A high output indicates that the internal interrupt mechanism is enabled.

Data Bus In (DBIN, Output)

DBIN is an active high signal; it indicates that the Data Bus is conditioned to read from the external circuits into the CPU. DBIN is used by external logic to gate data from an external source onto the Data Bus.

Write ($\overline{WR}$, Output)

The $\overline{WR}$ signal indicates to external memory and I/O circuits that the CPU has placed eight bits of data on the Data Bus during the current cycle. This signal is an active low logic level.

Synchronization (SYNC, Output)

The positive-going SYNC pulse appears during the first clock period of each new instruction cycle executed by the CPU. It indicates that the processor status is available on the Data Bus.

Hold Acknowledge (HLDA, Output)

HLDA appears in response to the Hold input request signal and indicates that the Data and Address Busses have been placed in their high impedance states.

Wait (WAIT, Output)

The WAIT line is activated by the CPU to indicate to external circuits that the CPU has entered the Wait state.

CLOCKING

The Am9080A uses a two-phase clock, Φ1, Φ2, to control the CPU functions. The clock signals Φ1 and Φ2 are generated externally and applied to the CPU circuit. All other timing functions for the microprocessor are generated within the CPU.

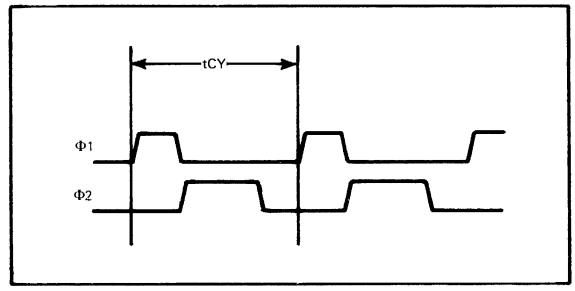


FIGURE 2-3 Φ1 AND Φ2

The clock period is measured as the interval of time between the leading edges of successive Φ1 pulses. The Φ2 pulse is generated between Φ1 pulses such that Φ1 and Φ2 are not high concurrently (see Figure 2-3). There is a delay from the end of Φ2 to the start of the next Φ1.

MACHINE CYCLES

Functions performed by the Am9080A CPU while executing instructions take place in intervals consisting of three, four or five clock periods referred to as a machine cycle. Instructions require at least one, and as many as five machine cycles to complete execution.

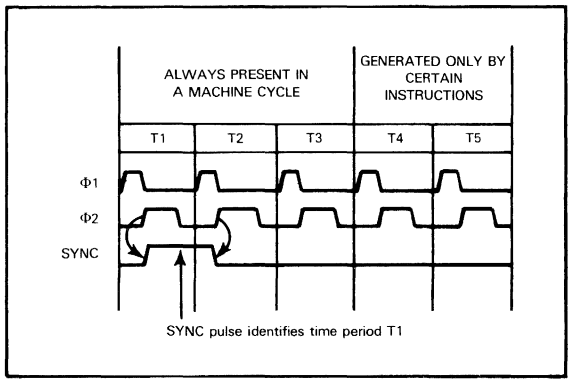


FIGURE 2-4 MACHINE CYCLE TIMING

Figure 2-4 shows consecutive clock periods, T1 through T5, in a machine cycle. The SYNC pulse is generated by the processor from the basic timing inputs. It begins with the leading edge of Φ2 during clock period T1 and ends with the leading edge of Φ2 in clock period T2.

Clock periods T1, T2 and T3 of the machine cycle are used to execute memory reference operations.

Data is read from, or written to memory during this period. The operation code for the instruction to be executed is always fetched during T1, T2 and T3 in the first machine cycle (M1). In subsequent machine cycles T1, T2 and T3 will be used to read additional bytes of the instruction object code, to read data operands, or to write information to memory. When present, clock periods T4 and T5 are used for internal CPU operations.

STATUS

The CPU specifies the operations that are to be performed during a machine cycle by placing status information on the Data Bus during the T1 clock period of each machine cycle. The status information functions as control signals to the rest of the microcomputer system, specifying events that are to occur during the machine cycle.

Data Bus status must be stored in external latches and decoded for use by the rest of the system circuits. The strobe signal for reading status is usually generated as the "AND" of SYNC and Φ1. Figure 2-5 shows the timing relationship of the status appearing on the Data Bus, slightly delayed from the leading edge of Φ2 in time period T1. Status remains static on the bus until the leading edge of the next Φ2, which occurs during the T2 clock period.

Table 2-1 shows the status signals which are generated to indicate various types of machine cycle.

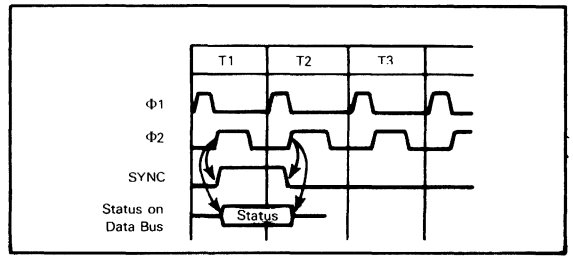


FIGURE 2-5 STATUS OUTPUT DURING T1 OF EVERY MACHINE CYCLE

Only those status signals that are used to define the operation to be performed are active during a machine cycle. For example, the $\overline{WO}$ signal (write pulse) is only active ($\overline{WO}$=0) in a machine cycle that requires information to be stored in an external memory location or output port.

MACHINE CYCLE OPERATION AND TIMING

The Am9080A executes eleven different types of machine cycles. One to five of the machine cycles may be executed sequentially to perform operations required by the instruction being executed. Nine of the machine cycles are described in the following paragraphs. Timing diagrams are included with the descriptions and a schematic notation is included in each timing diagram to explain the function performed during each clock period.

TABLE 2-1 Am9080A STATUS

DATA BUS BIT	D0	D1	D2	D3	D4	D5	D6	D7
STATUS SIGNAL	INTA	$\overline{WO}$	STACK	HLTA	OUT	M1	INP	MEMR
Instruction Fetch	0	1	0	0	0	1	0	1
Memory Read	0	1	0	0	0	0	0	1
Memory Write	0	0	0	0	0	0	0	0
Stack Read	0	1	1	0	0	0	0	1
Stack Write	0	0	1	0	0	0	0	0
Input Read	0	1	0	0	0	0	1	0
Output Write	0	0	0	0	1	0	0	0
Interrupt Acknowledge	1	1	0	0	0	1	0	0
Halt Acknowledge	0	1	0	1	0	0	0	1
Interrupt Acknowledge While Halted	1	1	0	1	0	1	0	0
Null	0	1	0	0	0	0	0	0

The following definitions are used in the description of instruction timing:

A	Accumulator
AB	Address Bus
AC	Auxiliary Carry = Carry propagation between 2^3 and 2^4 stages.
ACT	Accumulator Temporary Register
CY	Carry Status
d	Destination location (e.g., rd = Destination register).
DB	Data Bus
ddd	Destination location address
(H,L)	Contents of H and L registers, or memory location addressed by H and L registers.
((H,L))	Designates the contents of a memory location addressed by the 16-bit contents of the H and L registers.
INST	Any instruction code byte
INTE	Interrupt Enable flip-flop
IR	Instruction Register
Opcode	Instruction operation code byte
Operand	Operand of the instruction
P	Parity = Odd number of 1s in ALU result.
PCH	Eight most significant bits of the Program Counter.
PCL	Eight least significant bits of the Program Counter.
port	I/O device address
r	CPU register
rd	Destination register
rs	Source register
rp	Register pair
rpd	Destination register pair
rps	Source register pair
rpsh	Most significant register of source register pair
rpsl	Least significant register of source register pair
s	Source location (e.g., rs = Source register).
S	Sign of Result = ALU7
SR	Status Register
sss	Source location binary address
STATUS	Status Conditions appearing on Data Bus at T2 Φ1 time.
STATUS FLAGS	Condition representing results of an ALU operation.
TEMP	Temporary operand register
VVV	3-bit binary value, 000 to 111 inclusive.
VVVV	4-bit binary value, 0000 to 1111 inclusive.
W,Z	Temporary address registers
Z	Zero Result = $\overline{ALU7 \cdot ALU6 \cdot ALU5 \cdot ALU4 \cdot ALU3 \cdot ALU2 \cdot ALU1 \cdot ALU0}$
( )	The contents of
$\overline{( )}$	Complement of the contents of
(( ))	The contents of the contents of. The contents of the designated location in the inner brackets are interpreted as an address to a second location which supplies the 8-bit operand used by the instruction.
←	Receives. The notation ( ) ← means the location designation contained in the inner brackets is used as an address to which the operand will be stored.
→	Goes to
←→	Is exchanged with
+	Arithmetic Addition
-	Arithmetic Subtraction
x	Arithmetic Multiplication
Λ	Logical AND
V	Logical OR
⊻	Logical Exclusive-OR

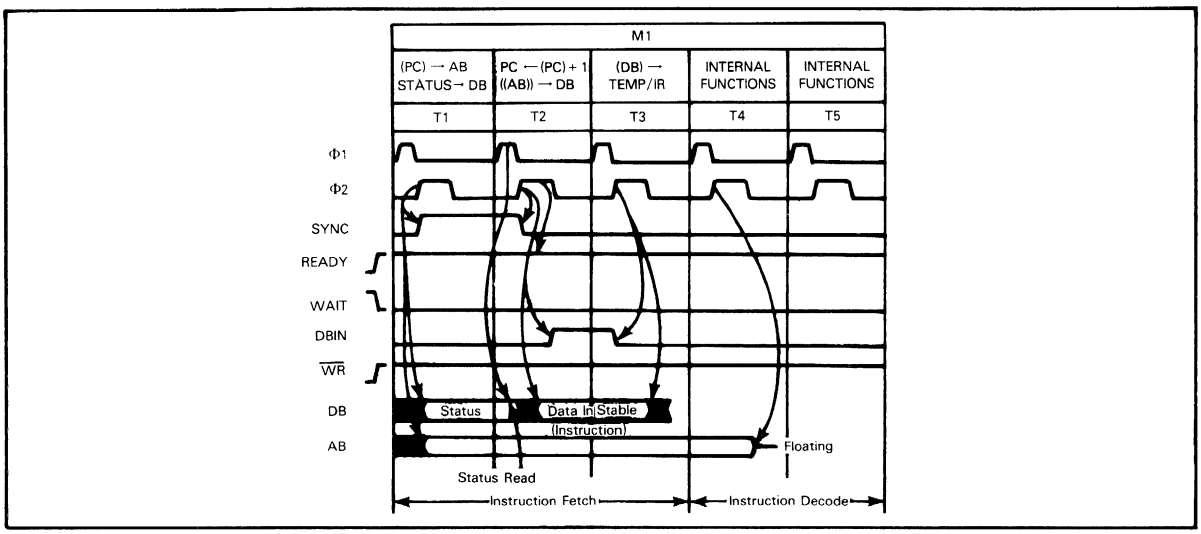


FIGURE 2-6 INSTRUCTION FETCH MACHINE CYCLE

Instruction Fetch

The first machine cycle during the execution of any instruction is the Instruction Fetch (M1) cycle. Figure 2-6 shows the timing and events that occur for each clock period in the Instruction Fetch machine cycle.

M1 begins with the leading edge of Φ1 in clock period T1. SYNC is generated with the leading edge of the first Φ2 in clock period T1. Shortly after this time the status information is placed on the Data Bus from the CPU. In order to generate control functions for the external system components, the status information must be latched in external circuits while SYNC is present.

This is conveniently achieved by means of the Status Strobe ($\overline{STSTB}$) signal generated by the Am8224. An alternative would be to use Φ1 and SYNC to latch the status data.

Since M1 is the Instruction Fetch cycle, the only two status lines active are the M1 status (D5), indicating that this is a first byte instruction fetch, and the MEMR status (D7), indicating that a byte is to be supplied by external memory.

The Address Bus receives the contents of the Program Counter slightly after the leading edge of the Φ2 in T1. The address signals remain active at the output of the Address Bus until after T3, when information received from the memory has been strobed into the Instruction Register.

The status signals on the Data Bus are deactivated with the leading edge of Φ2 during clock period T2 to allow the instruction byte from memory to be transmitted to the CPU via the Data Bus. Internal decoding of the instruction takes place during clock periods T4 and T5.

Note that in Figure 2-6 the Ready signal is continuously high (active). In the event that slow memory components are used in conjunction with the CPU, the Ready signal can be used to introduce an extra delay between T2 and T3 to allow time for the memories to respond. A more complete discussion of the effect of the Ready signal is contained in the Wait state description.

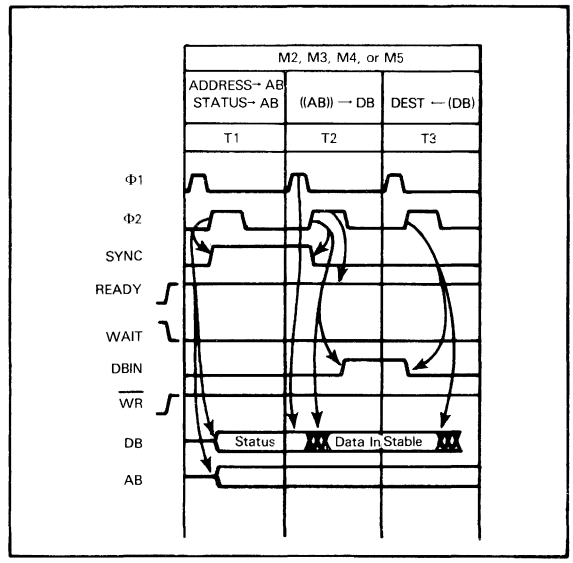


FIGURE 2-7 MEMORY READ MACHINE CYCLE

Memory Read

Figure 2-7 shows the timing for the Memory Read machine cycle.

The Memory Read machine cycle is identical to the Instruction Fetch cycle above except that the M1 status signal is not activated. Memory Read only occurs in the M2, M3, M4 or M5 machine cycles. The only active status signal on the Data Bus is the MEMR signal. Table 2-1 shows $\overline{WO}$ as a binary 1, but that is the inactive state for this signal.

Memory Write

The Memory Write machine cycle differs from the Memory Read machine cycle in that information generated within the CPU is written into the designated memory location. The timing for the Memory Write machine cycle is shown in Figure 2-8.

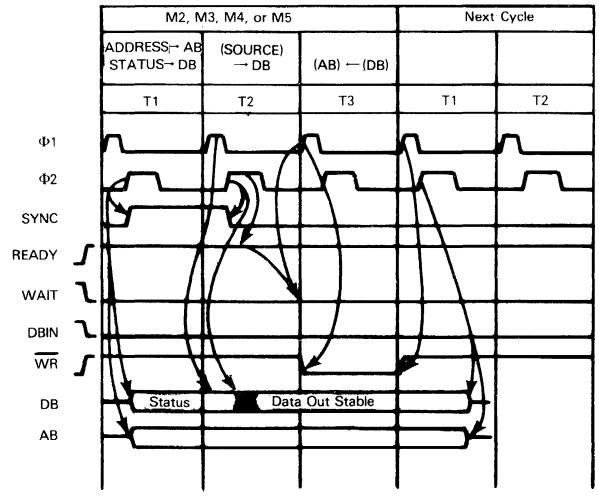


Figure 2-8 MEMORY WRITE MACHINE CYCLE

Notice that the machine cycle designated in Figure 2-8 can be any machine cycle in which a write operation takes place. The timing waveforms are similar to those for the Instruction Fetch or Memory Read machine cycles except for the operation of the Data Bus. Status appears on the outputs of the Data Bus during clock period T1 and is removed slightly after the leading edge of Φ2 in clock period T2. In the Memory Read cycle or Instruction Fetch cycle, the CPU causes the Data Bus drivers to go to the high impedance state. In the Memory Write cycle the data to be written to memory is immediately placed on the Data Bus, remaining present during the entire T3 period.

The Data Bus is returned to the high impedance state with the leading edge of Φ2 in clock period T1 of the next machine cycle.

Stack Read And Write

The timing for both the Stack Read and Stack Write machine cycles is identical to the Memory Read and Memory Write cycles. However, they are differentiated from standard Memory Read and Memory Write cycles by the presence of the Stack status signal (D2) during the T1 clock period.

The Stack status signal can be used to create a separate addressable memory space. One problem that is sometimes encountered when debugging programs incorporating a stack in main memory is that the stack increases without bound if the program is not functioning as intended. The results are usually rather dramatic and make it difficult to debug the program.

One way to prevent this is to differentiate between the areas of memory allocated to program data storage and stack storage. This can be accomplished by incorporating the Stack status signal into the memory chip select generation circuitry. The Stack status can be used to inhibit chip selects to non-stack areas of memory when a Stack Read or Stack Write machine cycle is being executed.

Input Read And Output Write

The waveforms of Figures 2-7 and 2-8 are also applicable to the timing for either an Input Read or Output Write machine cycle. These states are differentiated during the T1 machine period by the presence of the Input status signal (D6) in the case of an I/O read cycle, or the presence of the Out status signal (D4) in the event of the I/O write cycle.

Halt Acknowledge

The Halt Acknowledge machine cycle is characterized by the presence of the MEMR (D7) and Halt (D3) status signals. All other status signals are inactive.

Figure 2-9 shows the timing for the Halt Acknowledge.

The Halt Acknowledge machine cycle can be entered only in response to execution of a Halt instruction.

There are three functions which can terminate the Halt Acknowledge machine cycle:

- Activating Reset causes the Am9080A to enter a new Instruction Fetch machine cycle with the Program Counter pointing to location 0.
- Activating the Hold input causes the CPU to enter the Hold state. When Hold is released the CPU will return to the Wait state, and the Halt Acknowledge machine cycle will continue.
- Activating the Interrupt signal when INTE is enabled. This causes the Interrupt Acknowledge machine cycle to be executed. Normal program processing will continue.

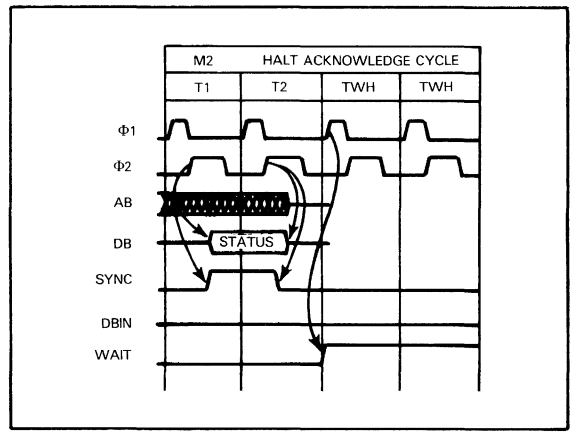


FIGURE 2-9 HALT ACKNOWLEDGE MACHINE CYCLE

Notice that the Interrupt Enable flip-flop (INTE) must be active in order to recognize the interrupt request that terminates the Halt Acknowledge state. The only way to terminate Halt if the Interrupt Enable flip-flop is reset when the Halt instruction is executed is to Reset.

Null

The Null machine cycle is entered only when an interrupt request has been acknowledged by the CPU. The CPU first enters the Interrupt Acknowledge machine cycle, and the external circuits respond by placing an instruction operation code on the Data Bus. If the CPU interprets the opcode as a 2- or 3-byte instruction, one or two Null machine cycles respectively are generated. The Null machine cycles allow the interrupting circuit to supply the second and third bytes to the CPU. The instructions which may be used in response to the Interrupt Acknowledge machine cycle are discussed in the paragraphs on interrupt processing.

The operation and timing of the Null machine cycle is identical to the Memory Read machine cycle of Figure 2-7 except for the following:

- The Program Counter is not incremented in T2 of the Null cycle.
- MEMR is not generated; therefore the memory system does not respond.

Figure 2-10 shows the timing diagram for the Null machine cycle. All status bits are inactive.

Am9080A MACHINE STATES

The Am9080A, like all microprocessors, is a sequential state machine. The operation being performed by any particular clock pulse at any instant in time is determined by the internal control logic and the condition of the input signals applied to the microprocessor. The instantaneous condition of all internal control flip-flops is known as the current machine state. The execution of instructions proceeds as a sequence of machine states that are executed in synchronism with the microprocessor timing to complete the desired operation.

Note that machine states are not the same as machine cycles. States denote the internal conditions of the control flip-flops and may be present only for the duration of a single clock pulse. A machine cycle, on the other hand, is composed of several internal machine states. There are three machine states

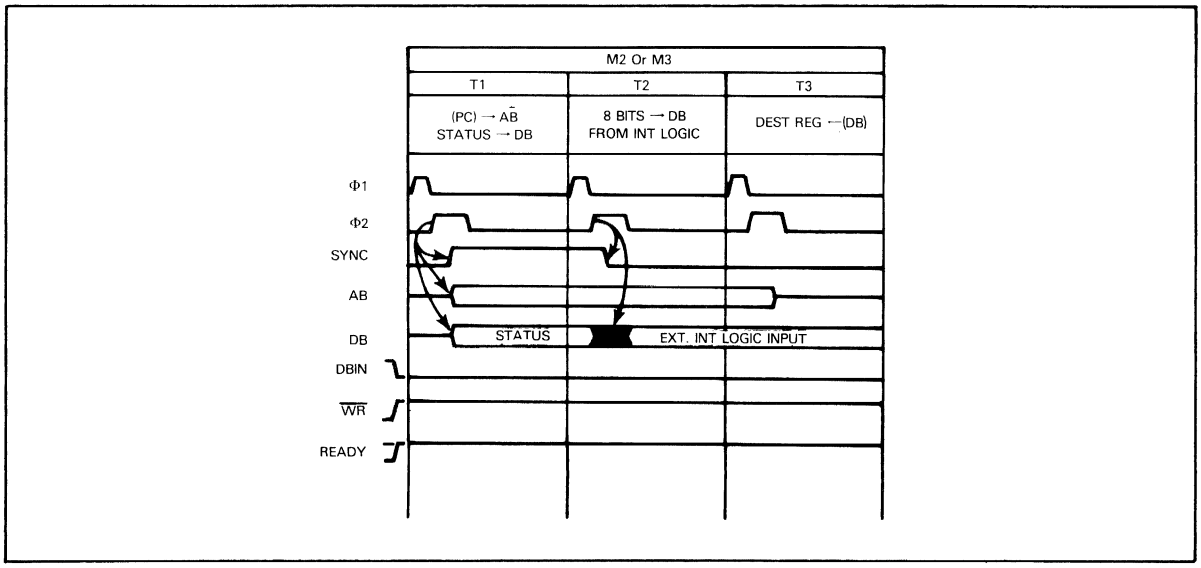


FIGURE 2-10 NULL MACHINE CYCLE TIMING

which are important since they affect the operation of memories and other external components used in an Am9080A microcomputer system. These are the Wait, Hold and the Halt machine states.

The principle function of the Wait state is to insert a delay between T2 and T3 clock periods to allow time for slow external devices to respond to a read or write operation. The Hold state is utilized to disconnect the Am9080A CPU circuit from the microcomputer memory and I/O. This permits externally controlled operations such as DMA to gain control of the Address and Data Busses independently of the CPU. The Halt state causes instruction processing to cease.

Wait State

Dynamic logic is used in the design of the Am9080A. This requires the application of continuous clock pulses with certain frequency and pulse width constraints. The Φ1 and Φ2 clocks cannot be delayed to accommodate external circuits. Instead, a Wait state is utilized to introduce delays during the execution of instructions.

Two possible uses of the Wait state are:

- Insert a delay to accommodate the response time of slow memory or I/O circuits.
- Stop processing during machine cycles within an instruction to permit the functions about to be performed to be examined.

A Wait state will always consist of an integral number of clock periods. Figure 2-11 shows the timing for a Wait state inserted between T2 and T3.

Use Of Ready

During a Memory Read cycle, the CPU can be forced to enter a Wait state if memory is too slow to provide the data within the required set-up time. The CPU samples the Ready input during a set-up time, tRS, which occurs within the T2 state just prior to the falling edge of Φ2. Therefore, indication of a Wait state requirement must be given via the RDY input, prior to the tRS time. This timing relationship is shown in Figure 2-12 along with associated parameters.

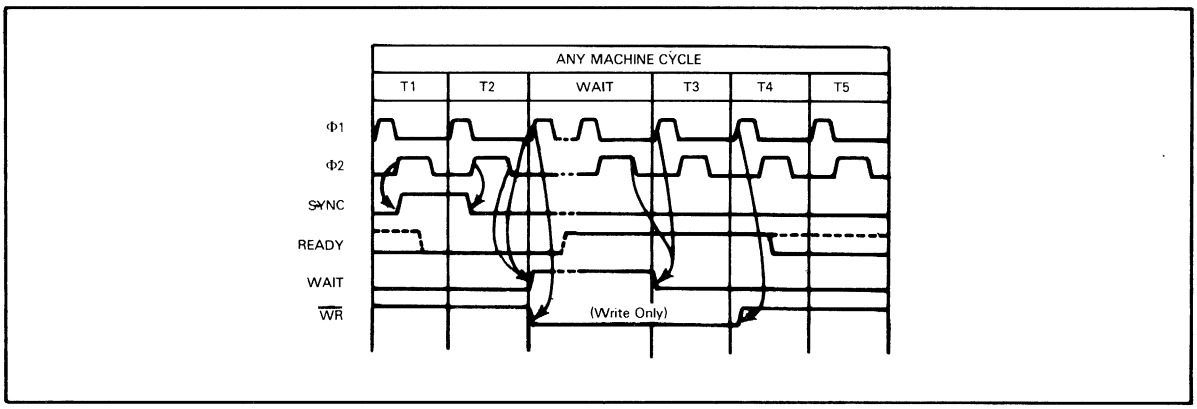


FIGURE 2-11 WAIT STATE TIMING

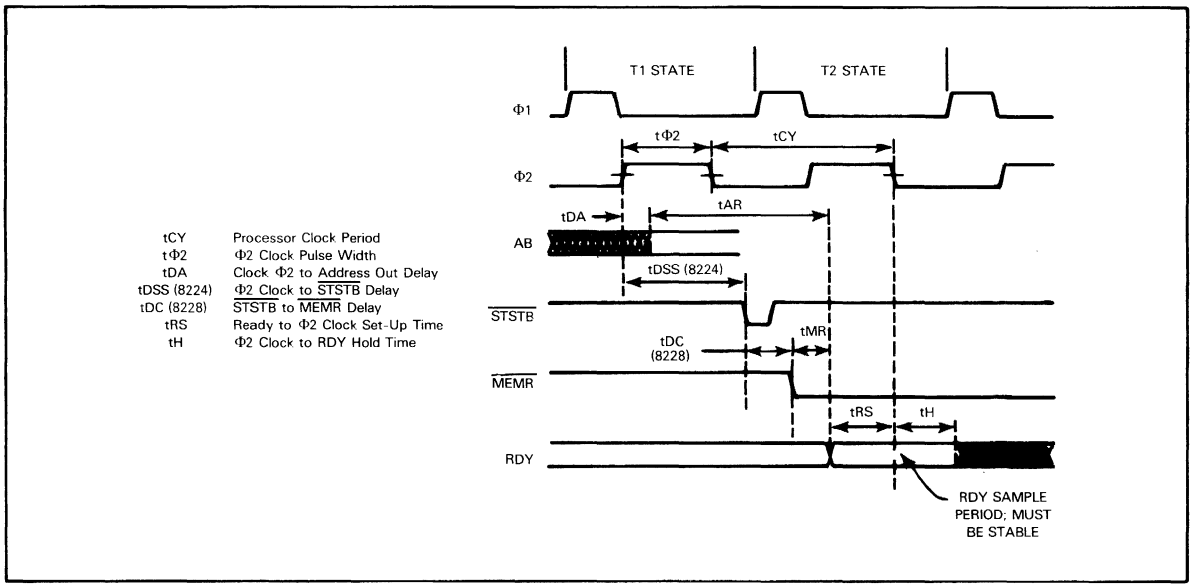


FIGURE 2-12 READY DECISION TIME

Normally, the earliest indication to the system that a Memory Read cycle is to be performed is when the MEMR signal is activated. With this in mind, then the time period available for a decision to request a Wait state is:

$$tMR = tCY + t\Phi2\text{-}tDSS\text{-}tDC\text{-}tRS = \frac{tCY}{3} + t\Phi2\text{-}tDC\text{-}tRS$$

The time from the address being valid and stable to the RDY sample time is given by:

$$tAR = tCY + t\Phi2\text{-}tDA\text{-}tRS$$

In system designs which do not make use of Ready, memory speed must be such that data is valid at the CPU when required. A detailed discussion of memory timing, including derivation of maximum access times can be found in the application section of this handbook.

Table 2-2 indicates the values of tMR and tAR for the various versions of the Am9080A at different operating speeds.

Hold State

The Hold state causes the CPU to suspend the function it is executing and places the Address and Data Busses in the high impedance state. This allows DMA or other external functions to gain access to the system busses. The Hold state is activated by means of the Hold input signal to the CPU. The following events occur in response to a Hold request:

1) The processor completes execution of the current machine cycle.
2) The processor enters the Hold state and acknowledges this condition by activating the HLDA control signal from the CPU. This occurs with the leading edge of Φ1 in period T3 if the machine cycle currently executing is not a Stack Write, Memory Write or Output Write cycle. If so, the Hold state is entered with the leading edge of the Φ1 in the next clock period following T3.
3) The processor places the Address Bus and the Data Bus in the high impedance state.
4) The processor enters the Wait state within the Hold state until the Hold request input returns to a low input level.

TABLE 2-2 WAIT STATE TIMING (IN NS)

PROCESSOR VERSION	tCY	tCY/3	tΦ2 (5/9 tCY)	tDA	tDC	tRS	tMR	tAR
Am9080A	480 500	160 167	266 277	200 200	60 60	120 120	246 264	426 457
Am9080A-2	380 480	127 160	211 266	175 175	60 60	90 90	188 276	326 481
Am9080A-1	320 380	106 127	177 211	150 150	60 60	90 90	133 188	257 351

Note the difference between this and a normal Wait state; the Address and Data Busses are in a high impedance state.

Figure 2-13A shows the timing when the current machine cycle is performing a read function. Notice the following events as indicated by numbers in the diagram:

1) The Am9080A specification requires that the Hold signal be active for at least 140 nsec preceding the leading edge of Φ2. This requirement may be met by synchronizing the Hold signal with the trailing edge of Φ2.
2) The Hold state is entered with the leading edge of Φ1 in clock period T3. HLDA is activated.
3) The Data Bus is placed in the high impedance state by the leading edge of Φ2 in T3.
4) The Address Bus is released by the leading edge of Φ2 in T4.
5) Internal functions are completed in T4 and T5 of the machine cycle, and the Wait state is entered and held until the Hold input is returned low.
6) Hold is deactivated. The release of the Hold signal may be synchronized with the trailing edge of Φ2.
7) The Hold state is terminated and the next machine cycle begins with a T1 period. This machine cycle is not necessarily an Instruction Fetch but could be the next machine cycle in an imcomplete instruction.

Figure 2-13B shows the Hold timing conditions when a write function is being performed. The two differences occur in events 8 and 9.

8) The Hold state is not entered until the leading edge of Φ1 in T4.
9) Data supplied to the Data Bus remains active through T3. The Data Bus is placed in the high impedance state by Φ2 in T4.

The Hold state for machine cycles requiring three clock periods is shown in Figure 2-14. All timing functions for both machine cycles performing a Read function and those performing a Write function are the same as the timing of Figure 2-13 except that the Wait state will be the next clock period after T3.

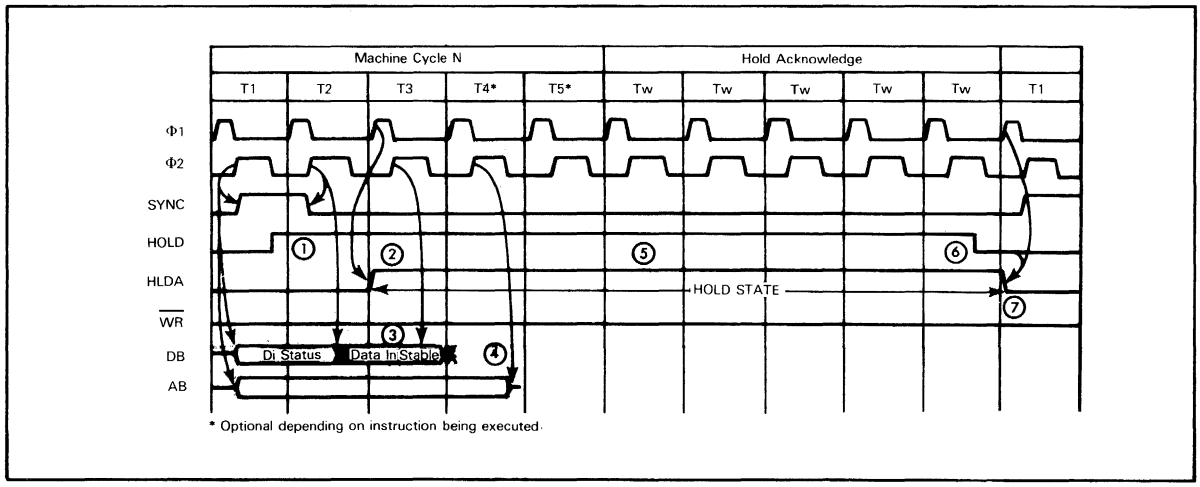


FIGURE 2-13A HOLD TIMING DURING FIVE TIME PERIOD READ OPERATIONS

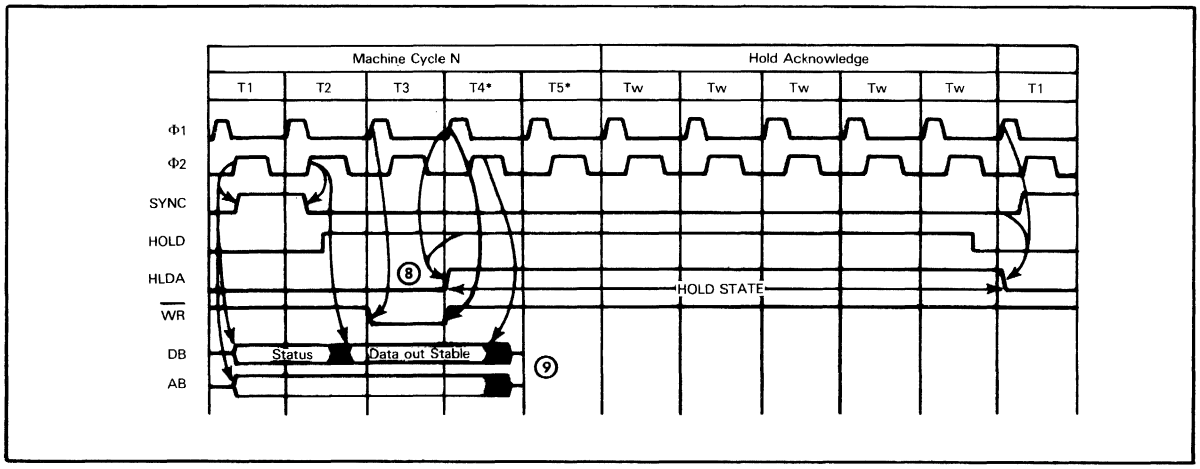


FIGURE 2-13B HOLD TIME PERIOD DURING FIVE TIME PERIOD WRITE OPERATIONS

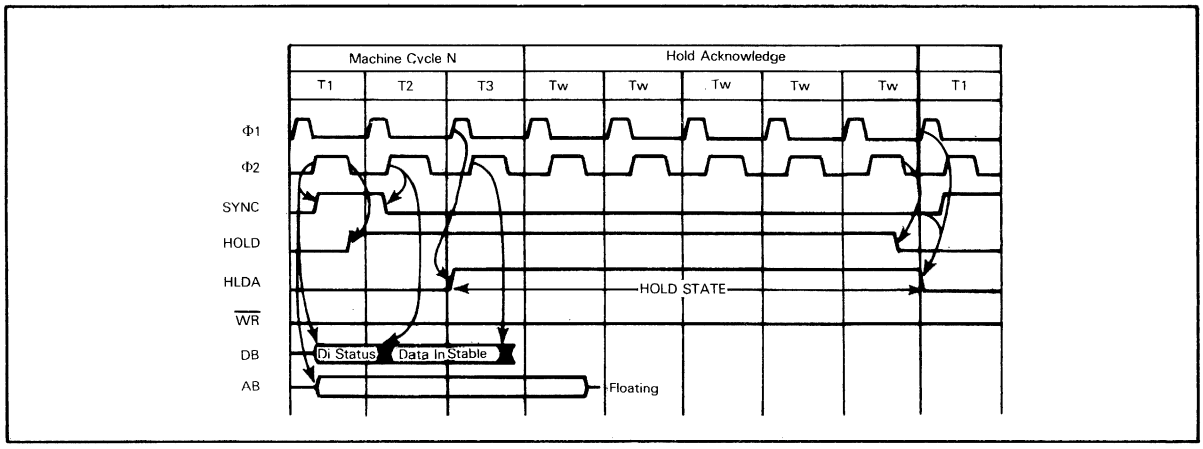


FIGURE 2-14A HOLD TIMING FOR READ IN A THREE TIME PERIOD READ MACHINE CYCLE

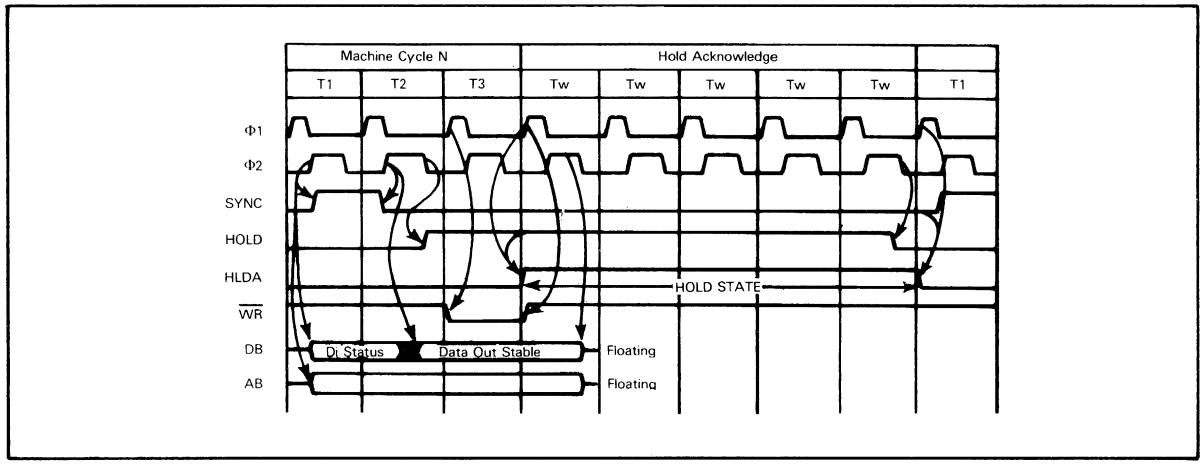


FIGURE 2-14B HOLD TIMING FOR ANY NON-READ OPERATION COMPLETED PRIOR TO ONSET OF HOLD STATE

Halt State

The Halt state introduces a delay in instruction processing by inserting Wait states in the Halt Acknowledge machine cycle, after the T2 clock period. The Halt state is differentiated from the Wait state in the following ways:

- The Halt state is initiated by executing the Halt instruction, whereas the Wait state is initiated by setting the Ready input low.
- Wait will occur in any machine cycle between T2 and T3. The Halt state occurs only in a Halt Acknowledge machine cycle. The Halt Acknowledge machine cycle is the M2 machine cycle when the instruction fetched in the M1 cycle is decoded as the Halt instruction.
- The Halt state can be terminated and program processing allowed to continue only if an interrupt is received or a Reset is applied to the processor.

During the Halt state the system bus is not floated; this contrasts with the Hold state during which the system bus is floated. Thus the Hold state can be used by external logic to gain control of the system bus, for example to perform Direct Memory Access operations. The Halt state stops all activity within the microcomputer system.
Figure 2-15 shows the timing for the Halt state.

INTERRUPT PROCESSING

Interrupt capability is included in most microprocessors to increase performance (throughput). If interrupts were not available, the microcomputer program would have to periodically stop the task that it was performing and test each I/O device to determine if service is required. In microcomputers where I/O response time must be short, the rate at which the devices are tested must be much greater than the actual rate at which the I/O devices require service. As a consequence, the application processing capability of the microcomputer would be reduced considerably, especially as the number of devices grows.

In the Am9080A, an interrupt causes a new instruction to be inserted into the program sequence being executed. This capability is usually used to terminate processing at the location to which the Program Counter was pointing when the interrupt occurred and resume executing instructions at a new location. The program which begins at the new location is called the "Interrupt Service Routine". When the interrupt service routine is completed, control is returned to the main program, and processing continues with the instruction in the interrupted program which would have been executed, had the interrupt not occurred. Figure 2-16 illustrates the interrupt scheme.

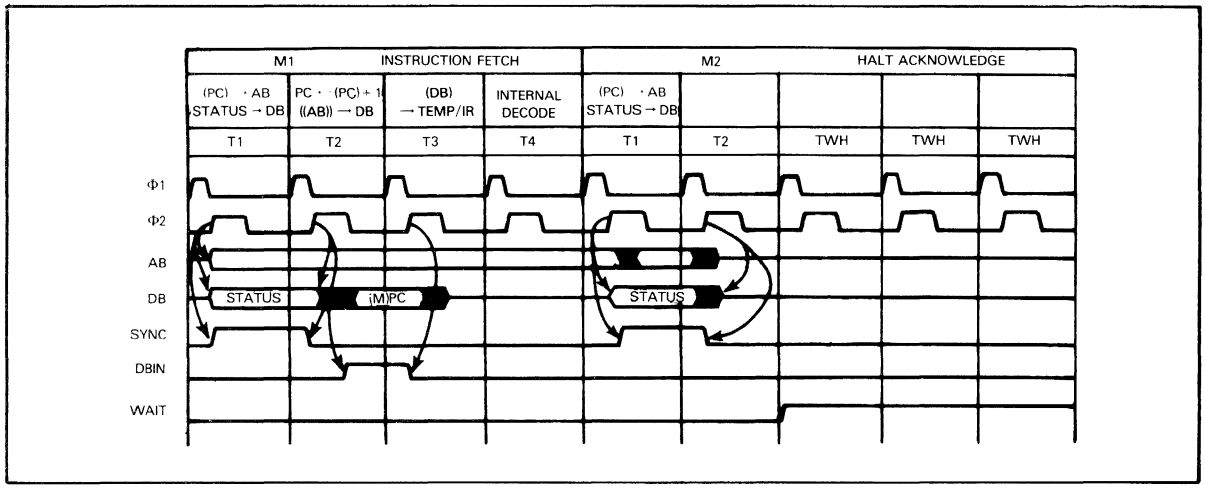


FIGURE 2-15 HALT TIMING

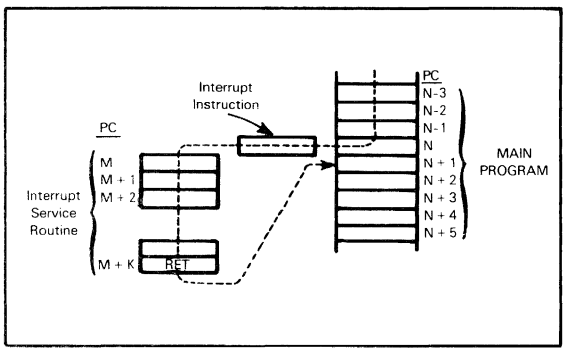


FIGURE 2-16 INTERRUPT PROGRAM FLOW

Notice that the Program Counter is used to address instructions both in the main program and in the interrupt service routine. These are the events that occur to transfer control to the interrupt service routine:

1) INTE is high, and an active INT input is sensed by the processor during execution of instruction N.
2) Execution of instruction N is completed, including incrementing of the Program Counter to point to location N + 1.
3) The Interrupt Acknowledge output is generated to signal the interrupting device that the processor has recognized the Interrupt input and is ready to process it.
4) INTE is reset.
5) The interrupting device supplies a Call or Restart instruction from which the address of the service routine (M) is determined.
6) The Program Counter contents (N + 1) are stored on the stack as a consequence of executing the interrupt instruction.
7) Address M supplies the first instruction of the service routine and this is loaded into the Program Counter.

When the Interrupt Acknowledge machine cycle is generated, the interrupting external device supplies the instruction to be executed next. Notice that this instruction is not coded in either the application program or the interrupt service routine. It is an extra instruction inserted by external logic which requests the interrupt. Typical microcomputers designed with the Am9080A insert the Restart or one of the Call instructions onto the Data Bus in response to the Interrupt Acknowledge machine cycle; however, any instruction except XTHL can be used.

When the interrupt service routine is complete, control is transferred back to the main program by the following sequence of events:

- A Return instruction is executed at instruction M + K.
- The address of the next main program instruction (N + 1) is pulled from the stack and used to fetch an instruction.
- The instruction address is incremented and the result placed in the Program Counter.

Interrupt Control

Three interrupt control signals are provided by the Am9080A. These are:

- INT — an input signal used by external devices to request an interrupt.
- INTE — an output signal which indicates when the processor is, or is not accepting interrupts.
- INTA — Interrupt acknowledge signal output in response to INT.

After INT is detected high, the processor will finish executing the current instruction and enter the Interrupt Acknowledge machine cycle. INTE is reset low.

INT may be reset low any time after the Interrupt Acknowledge machine cycle is started, but must be low before interrupts are enabled again. If the INT signal is not reset low before interrupts are re-enabled, it will be interpreted as a new interrupt and the interrupt acknowledge process will be repeated. The INTA signal appears on D0 during the Interrupt Acknowledge machine cycle; it may be used to reset the interrupt request.

Any of the following three conditions will clear INTE, disabling interrupts:

- RESET input being activated.
- The rising edge of Φ2 during T1 in the Interrupt Acknowledge machine cycle.

- Executing the Disable Interrupt instruction.

Interrupt Acknowledge

The interrupt acknowledge sequence, which was just described, occurs during an Interrupt Acknowledge machine cycle.

The Interrupt Acknowledge machine cycle is characterized by active INTA (D0) and M1 (D5) status signals during T1. Figure 2-17 shows the timing for the Interrupt Acknowledge machine cycle.

The interrupt service sequence is initiated by an external Interrupt Request (INT) becoming active prior to the end of Φ2 in the last machine clock period of an instruction being completed. The next clock period will initiate the Interrupt Acknowledge machine cycle which requests one byte from the interrupting circuit. The byte that is returned to the CPU is loaded into the Instruction Register and interpreted as an instruction opcode. The following events occur during the Interrupt Acknowledge machine cycle:

1) The INTE signal is disabled in the T1 clock period, preventing future interrupts from being serviced.
2) Although the Program Counter contents are supplied to the Address Bus, the Program Counter is not incremented.
3) The MEMR status signal is not activated.
4) External logic supplies the interrupt instruction to the Data Bus to be received by the Instruction Register during T3.

Restart Instruction

Restart is a one-byte subroutine Call instruction; it saves the Program Counter contents on the stack and provides a subroutine entry address. A 3-bit vector is issued to select one of eight fixed memory locations to which program execution may transfer.

The binary format for the Restart instruction is:

7	6	5	4	3	2	1	0
1	1	N	N	N	1	1	1

where NNN is the interrupt vector. Table 2-3 lists the eight Restart vectors and the corresponding addresses.

TABLE 2-3 RESTART INSTRUCTION INTERRUPT VECTOR ADDRESS

INSTRUCTION	INTERRUPT VECTOR NNN	MEMORY ADDRESS	
		HEXADECIMAL	OCTAL
RST 0	000	0000	000000
RST 1	001	0008	000010
RST 2	010	0010	000020
RST 3	011	0018	00030
RST 4	100	0020	000040
RST 5	101	0028	000050
RST 6	110	0030	000060
RST 7	111	0038	000070

Figure 2-17 shows the complete timing diagram for processing the Restart instruction. M1 is the Interrupt Acknowledge machine cycle. It causes the interrupting circuit to respond by transmitting the Restart instruction back to the CPU. The Restart instruction is decoded in T4 and the Stack Pointer is decremented. Two Stack Write machine cycles are performed in M2 and M3 to store the current Program Counter contents onto the stack and to form a new memory address from the decoded information in the Restart instruction. The new memory address represents the address of the first instruction to be executed in the interrupt subroutine.

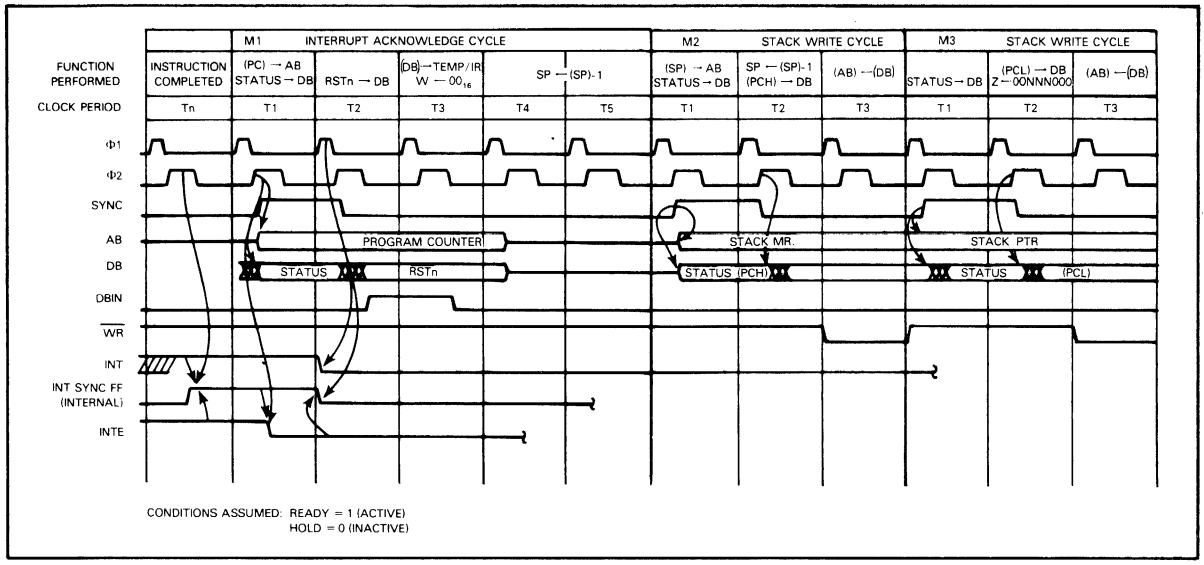


FIGURE 2-17 INTERRUPT TIMING, RESTART INSTRUCTION

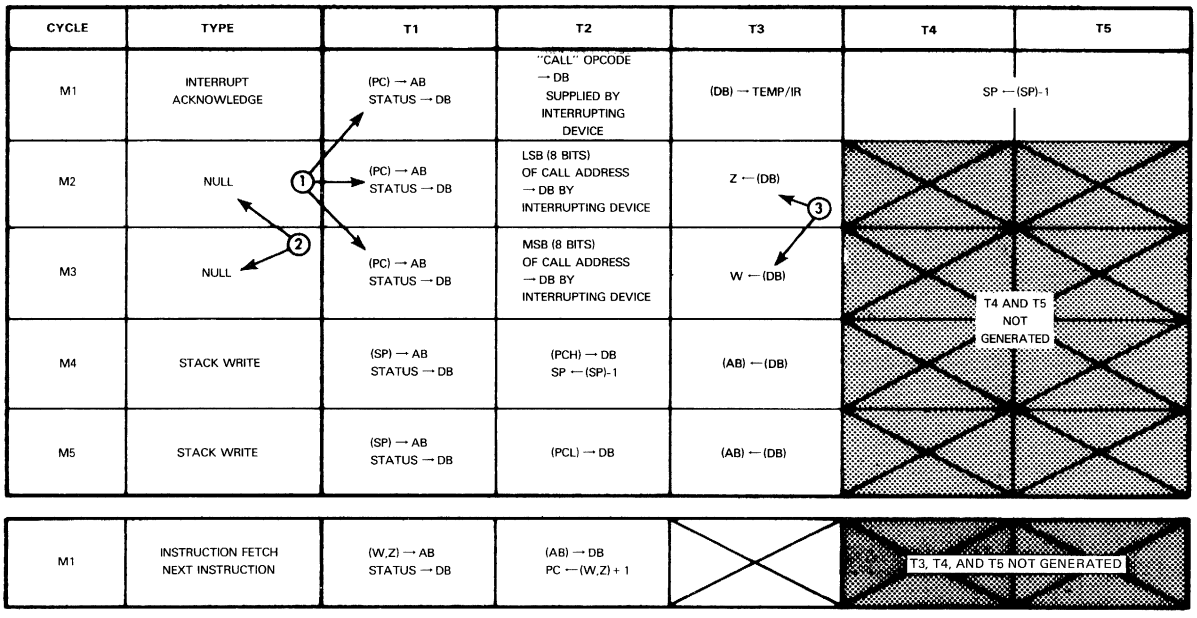


FIGURE 2-18 EXECUTION OF CALL INSTRUCTION DURING INTERRUPT ACKNOWLEDGE

Call Instruction

The Call instruction saves the Program Counter contents on the stack and provides a subroutine address. The Call instruction is particularly useful as a response to the Interrupt Acknowledge machine cycle. It supplies a full 16-bit subroutine address, allowing direct entry to interrupt service routines located anywhere in memory without first branching to the restart locations. Any number of interrupt locations may be directly addressed by the peripherals rather than only one of the eight restart locations.

The execution of the Call instruction in response to the Interrupt Acknowledge machine cycle is shown in Figure 2-18.

Notice that a Call instruction inserted into the CPU in response to the Interrupt Acknowledge machine cycle (M1 in Figure 2-18) executes as if it were a normal Call instruction except for the following, numbered as in Figure 2-18:

1) The Program Counter is not incremented in T2 of any machine cycle.
2) Null machine cycles are substituted for the usual Memory Read machine cycle. The Null cycle does not activate the MEMR status bit and thus inhibits the memory system.
3) The least significant eight bits of the interrupt subroutine address generated by the external interrupt logic are loaded into the Z Register, and the most significant eight bits are loaded into the W Register.

The conditional Call instructions could be used also; however, since the interrupt may occur after any instruction, the condition codes which determine the branch to the subroutine may be unpredictable.

OTHER INTERRUPT INSTRUCTIONS

Any Am9080A instruction except XTHL may be used as a response to the Interrupt Acknowledge machine cycle. However, instructions other than the Restart or Call do not cause the Program Counter contents to be saved and do not supply an interrupt service routine address. Therefore, interrupt servicing cannot be distinguished clearly as a separate subroutine.

Also, INTE is disabled when the interrupt is serviced. If an interrupt is not serviced via a separate subroutine, there exists no definite position in the program where the EI instruction should be executed. The Enable Interrupt instruction may have to be inserted periodically throughout the program to ensure that interrupts are re-enabled.

Nevertheless, some applications use special instructions in response to the Interrupt Acknowledge machine cycle. For example, an instruction which increments a register or memory location may record an external event such as a clock pulse or limit switch closure and allow the main program to finish executing its task before attention is directed to the event.

The execution of the INR d inserted in response to an Interrupt Acknowledge machine cycle is shown in Figure 2-19.

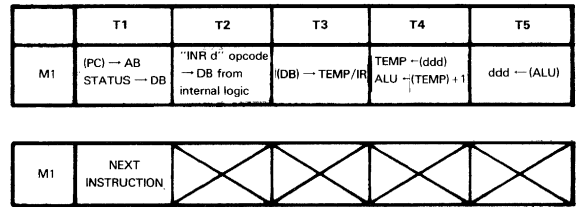


FIGURE 2-19 INR d RESPONSE TO INTERRUPT ACKNOWLEDGE

Notice that PC is not incremented in T2 as it is when INR d is executed in response to the usual Instruction Fetch machine cycle.

Wait And Hold Conditions During An Interrupt

Interrupts cannot be acknowledged during a Wait or Hold condition. However, it is possible to enter the Wait or Hold state after the Interrupt Acknowledge machine cycle has been generated. This may be useful in logic systems where there is

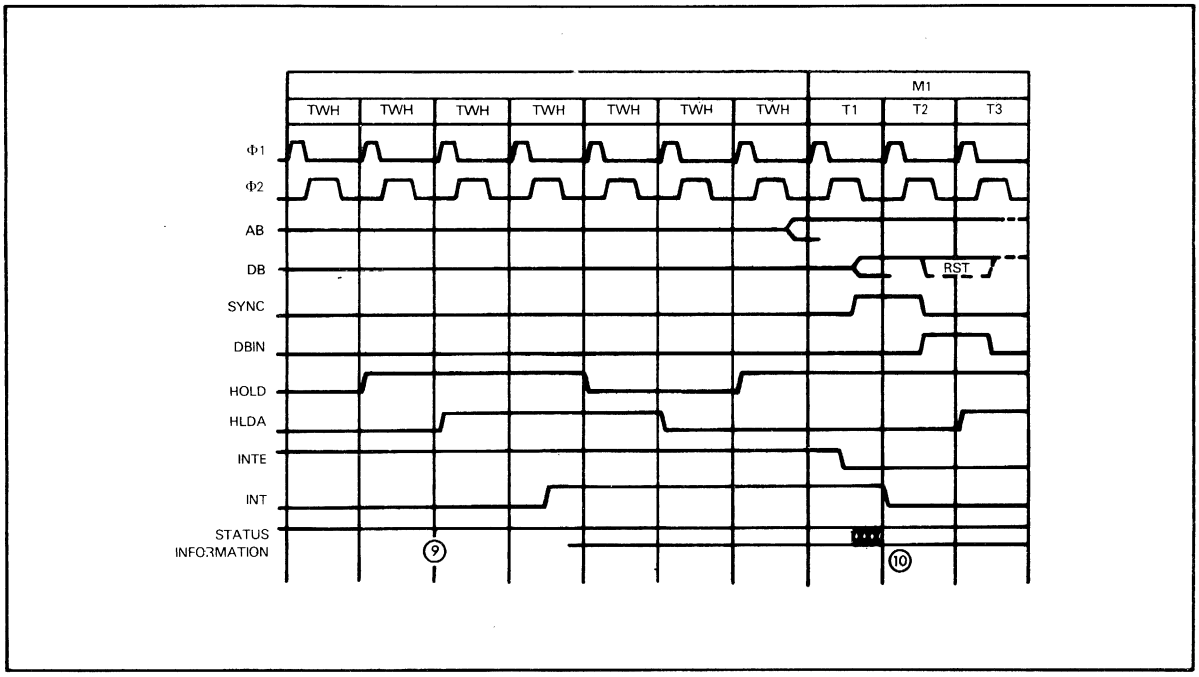


FIGURE 2-20 RELATION BETWEEN HOLD AND INT IN THE HALT STATE

insufficient time in the normal machine cycle to generate an interrupt instruction and place it on the Data Bus for execution by the CPU. The Ready signal can be deactivated to cause the machine to insert the Wait state for one or more clock periods as required until the appropriate duration has elapsed.

When the Am9080A is in the Halt state, an interrupt will cause program processing to continue. However, a Hold state can be superimposed on the Halt state to cause the Data and Address Busses to be released for external control of these busses. While the Hold condition is active, the interrupt will be inhibited. Figure 2-20 shows the relationship between the Hold and INT inputs during the Halt state.

Interrupt Acknowledge During A Halt

This machine cycle occurs in response to an interrupt request (INT) when the processor is in the Halt state (HLTA is active). The timing diagram for this state is shown in Figure 2-20. The Interrupt Acknowledge While Halt machine cycle is similar to the Interrupt Acknowledge machine cycle in that the Program Counter is not incremented when this instruction opcode is supplied to the Data Bus.

INPUT/OUTPUT PROCESSING

This section discusses some general considerations for Input/Output processing. The concept of address space is introduced and methods of I/O addressing are discussed.

Maximum Address Space

A microprocessor is capable of accessing any one of a number of external devices or locations with a single instruction. The unique identification of the device which is accessed is contained in the address transmitted by the CPU during the access. The maximum number of addresses which may be generated is the Maximum Address Space of the microprocessor.

The Am9080A provides two independent address spaces. The first provides 64K bytes of addressable space for memory. The second is a totally independent addressable space which is used only by the Input/Output instructions of the machine.

The status signals supplied to the Data Bus by the CPU at the beginning of every machine cycle determine whether the external device access will be to a location in the addressable memory space or to one of the I/O circuits. Table 2-4 shows the type of access that occurs as a result of these status signals. When used in a system with an 8228 or 8238 System Controller, the control lines are latched and decoded even more explicitly as MEMR, MEMW, IOR, IOW.

TABLE 2-4 ADDRESS SPACE ACCESSES AS A FUNCTION OF MACHINE CYCLE STATUS BITS

STATUS	DATA BUS BIT	ADDRESS SPACE ACCESSED	FUNCTION PERFORMED
MEMR	D7	MEMORY	READ FROM MEMORY LOCATION ADDRESSED
$\overline{WO}$	D1	MEMORY	WRITE TO MEMORY LOCATION ADDRESSED
INP	D6	I/O	READ FROM INPUT DEVICE ADDRESSED
OUT	D4	I/O	WRITE TO OUTPUT DEVICE ADDRESSED

I/O Addressing

Peripheral devices may be configured in the Am9080A system to function in either the I/O address space or in the memory address space. However, the performance of the CPU in handling I/O transfers through the two addressable memory spaces is different. Each of these is discussed in the following sections.

Addressing Peripheral Devices With The I/O Instruction

The Input and Output instructions cause the transfer of an 8-

bit value between the Accumulator and an external device. They are two bytes long. The first byte always contains the operation code that defines the instruction as either an Input or Output function. The second byte is always an 8-bit address that defines the location of the external unit which is addressed.

The executions of the Input and Output instructions are defined by the corresponding Input Read and Output Write machine cycles. The status generated during the T1 clock period of these machine cycles causes either the INP or the OUT status signal to be generated. Notice that the corresponding MEMR and $\overline{WO}$ signals are not active when these machine cycles are generated as shown in Table 2-1. M2 machine cycle accesses byte 2 of the Input or Output instruction for the address of the peripheral device. This address is placed in both the Z and W Temporary registers and made available via the Address Bus. The address appears on address lines A0 through A7 and again on address lines A8 through A15.

Input/Output Devices As A Function Of Addressable Memory Space

An alternate method of organizing the I/O system in an Am9080A microcomputer is to assign specific memory addresses to the input and output functions. The advantage of using memory space for Input/Output ports is that the full flexibility of all the memory reference instructions can be used for servicing input/output devices. It also greatly expands the number of locations available for I/O.

For example, the exclusive "OR" instruction (XRA M) with an address pointing to a location assigned to an I/O device would cause a byte to be read from the peripheral device and exclusive "OR"ed with the contents of the Accumulator. This would require the execution of at least two instructions using the standard Input instruction. The first instruction reads the contents of the peripheral device and loads it to the Accumulator. The second instruction performs the exclusive "OR" with the contents of a CPU register or a memory location.

The external system distinguishes memory from I/O operations by examining the location being addressed.

In conclusion, addressing I/O devices within a separate I/O space reduces device select logic by limiting select logic input to 8 of the 16 Address Bus lines; however, just two instructions are available to input or output data from or to the I/O devices. If I/O devices are addressed within the memory space of the microprocessor system, then all 16 address lines must be decoded by the device select logic. However, any memory reference instruction can now access the I/O device.

Chapter 3
8080A/9080A INSTRUCTION SET

The functions performed by a microcomputer are determined by a sequence of instructions, which, taken together, constitute a program.

This section provides a detailed description of every Am9080A instruction.

All instructions are one, two or three bytes in length, the first byte always containing the opcode for the instruction. The instruction formats are shown below.

Single Byte Instructions

Type 1 Control, Subroutine Return and other Data Manipulation instructions, where the source and destination are implied, use a single, 8-bit opcode, as illustrated in Figure 3-1.

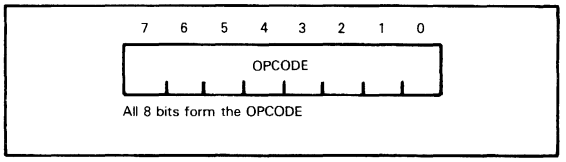
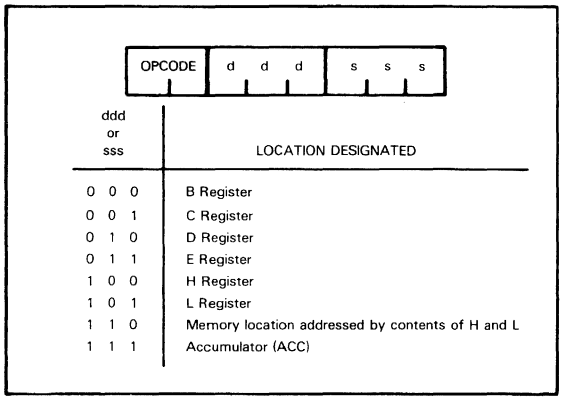


FIGURE 3-1 A TYPE 1, SINGLE BYTE INSTRUCTION OPCODE

Type 2 instructions utilize a 2-bit opcode and specify the source and destination addresses for operands, as illustrated in Figure 3-2.



ddd or sss	LOCATION DESIGNATED
0 0 0	B Register
0 0 1	C Register
0 1 0	D Register
0 1 1	E Register
1 0 0	H Register
1 0 1	L Register
1 1 0	Memory location addressed by contents of H and L
1 1 1	Accumulator (ACC)

FIGURE 3-2 A TYPE 2, SINGLE BYTE INSTRUCTION

When sss or ddd have the value 110, a memory location is addressed. The contents of the H and L registers form a 16-bit binary address which is used to access the desired location.

The general format for Type 2, single byte instructions allows either or both the source and destination locations to be specified. Both source and destination are present only in the MOVE instruction.

Type 3, single byte instructions of the Arithmetic group, as well as some of the instructions from the logical group, specify only the source address, sss. The remaining five bits of the 1-byte, Type 2 instructions form the opcode, as illustrated in Figure 3-3.

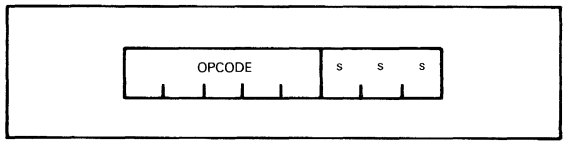
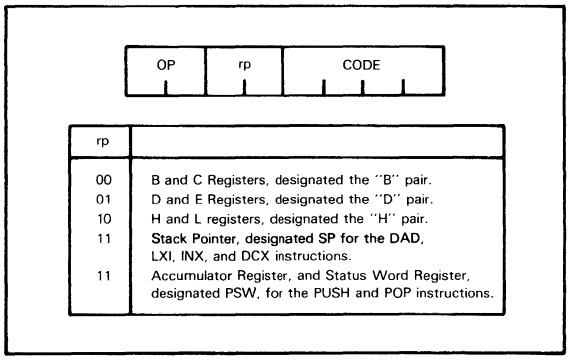


FIGURE 3-3 TYPE 3 SINGLE BYTE INSTRUCTIONS

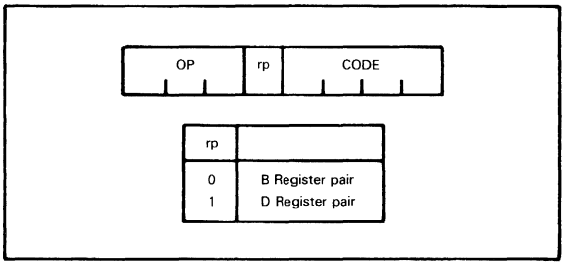
Type 4 instructions treat the contents of pairs of registers as a 16-bit binary value. These instructions include DAD, LXI, INX, DCX, PUSH and POP, as illustrated in Figure 3-4.



rp	
00	B and C Registers, designated the "B" pair.
01	D and E Registers, designated the "D" pair.
10	H and L registers, designated the "H" pair.
11	Stack Pointer, designated SP for the DAD, LXI, INX, and DCX instructions.
11	Accumulator Register, and Status Word Register, designated PSW, for the PUSH and POP instructions.

FIGURE 3-4 TYPE 4 SINGLE BYTE INSTRUCTIONS

The LDAX rp instruction is a special case in which the designated register pair (rp) is only one bit, as illustrated in Figure 3-5.



rp	
0	B Register pair
1	D Register pair

FIGURE 3-5 LDAX rp INSTRUCTION

Two Byte Instructions

Type 1 has both the immediate operand and the destination address contained within the instruction. The only instruction using this format is MOVE IMMEDIATE (MVI).

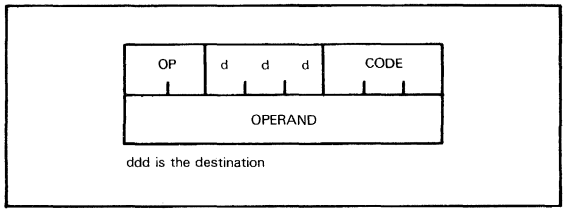


FIGURE 3-6 TYPE 1, TWO BYTE INSTRUCTIONS

Type 2 has an 8-bit opcode and an 8-bit operand. All instructions with immediate operands, with the exception of the MVI instruction, use this format.

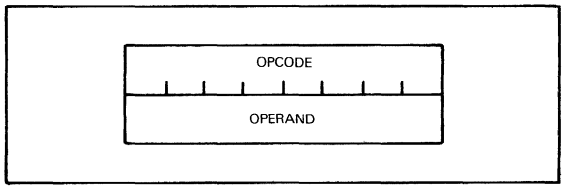


FIGURE 3-7 TYPE 2, TWO BYTE INSTRUCTIONS

Type 3 has an 8-bit opcode and an 8-bit I/O device address. Input and Output instructions use this format.

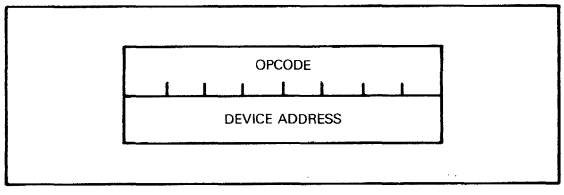


FIGURE 3-8 TYPE 3, TWO BYTE INSTRUCTIONS

Three Byte Instructions

These have an 8-bit opcode and a 16-bit address. All Direct Address, Jump and Call instructions use this format.

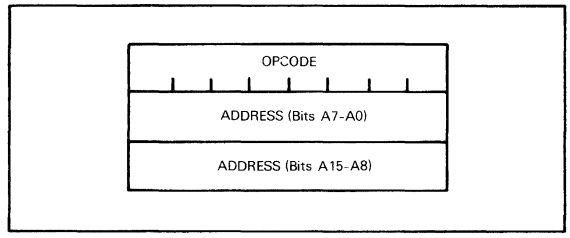


FIGURE 3-9 THREE BYTE INSTRUCTIONS

Unused Opcodes

There are 12 unused opcodes which are not decoded by the CPU. The hexadecimal opcodes for these instructions are:

08	20	38	DD
10	28	CB	ED
18	30	D9	FD

The response of the Am9080A is unpredictable when one of these codes is loaded into the Instruction Register during the Instruction Fetch or Interrupt Acknowledge machine cycle.

INSTRUCTION EXECUTION

All Am9080A instructions are executed as a sequence of machine cycles which are subdivided into clock periods. An instruction may execute in one, two, three, four or five machine cycles, each of which may have three, four or five clock periods. The first machine cycle may have four or five clock periods. Figure 3-10 illustrates instruction machine cycle and clock period options.

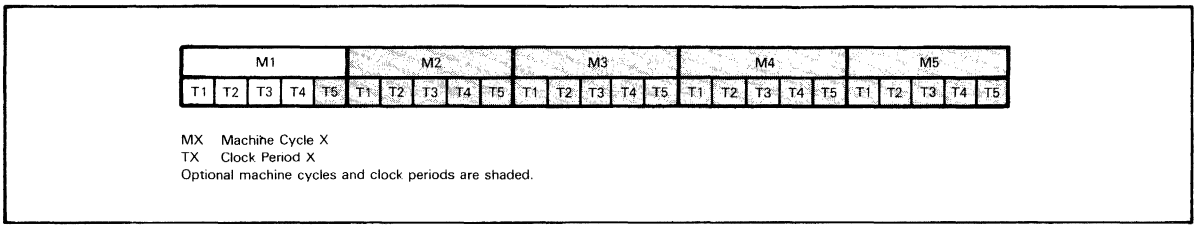


FIGURE 3-10 Am9080A MACHINE CYCLES AND CLOCK PERIODS

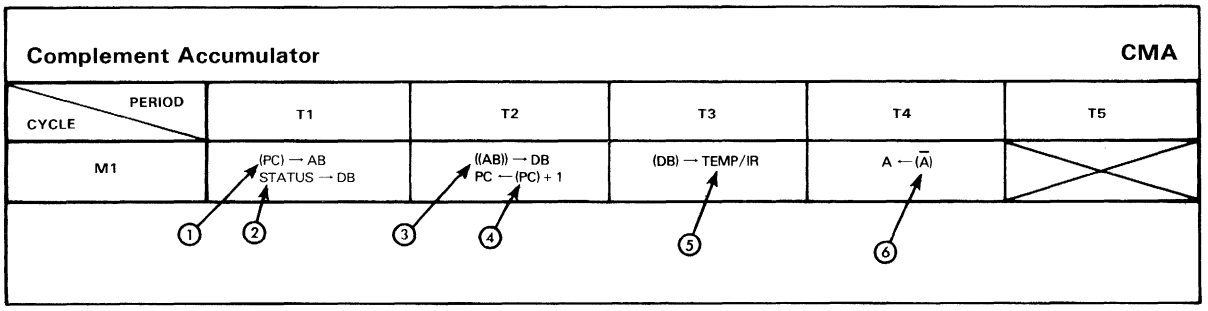


FIGURE 3-11 INSTRUCTION EVENT SCHEMATIC FOR THE CMA INSTRUCTION

Format

Throughout this chapter, a standard format is used to identify the operations which occur during each clock period of every machine cycle. Figure 3-11 and Table 3-1 are taken from the Complement Accumulator instruction (CMA) in order to illustrate the standard format used.

CMA

Complement Accumulator

The first machine cycle (M1) of each instruction is always used to fetch the instruction. If the instruction does not require data to be accessed at a memory location or I/O port, the instruction can be executed completely within the M1 machine cycle. Thus the CMA instruction consists of a single machine cycle, M1, containing four clock periods, T1 through T4.

TABLE 3-1 EXECUTION SEQUENCE FOR THE CMA INSTRUCTION

MACHINE CYCLE	EVENT #	CLOCK PERIOD	DESCRIPTION
M1	① ②	T1	The contents of the Program Counter (PC) are gated to the Address Bus (AB). The machine Status is gated to the Data Bus (DB).
	③	T2	The contents of the memory location addressed by the contents of the Address Bus are gated to the Data Bus from the Memory System.
	④		The contents of the Program Counter are incremented and returned to the Program Counter.
	⑤	T3	The contents of the Data Bus, which constitute the opcode for the instruction, are clocked into the Temporary Register and the Instruction Register.
	⑥	T4	The contents of the Accumulator (A) are complemented and returned to the Accumulator.

The sequence of events that occur for the CMA instruction are summarized in Table 3-1. The numbers in the circles of Figure 3-11 correspond to the numbers next to each event shown in the table and do not imply that the events are necessarily executed in that order.

The Move instruction (MOV) is an example of an instruction which requires more than one machine cycle. The instruction event schematic for the MOV rd,M instruction is shown in Figure 3-12. Table 3-2 lists the events that occur in each clock period for the two machine cycles.

TABLE 3-2 EXECUTION SEQUENCE FOR THE MOV rd,M INSTRUCTION

MACHINE CYCLE	EVENT #	CLOCK PERIOD	DESCRIPTION
M1	①	T1	The contents of the Program Counter (PC) are gated to the Address Bus (AB).
	②		Machine status is gated to the Data Bus, DB.
	③	T2	The contents of the memory location addressed by the contents of the Address Bus are gated to the Data Bus.
	④		The contents of the Program Counter are incremented and returned to the Program Counter.
	⑤	T3	The contents of the Data bus are clocked into the Temporary Register and the Instruction Register.
	⑥	T4	Delay introduced to complete internal functions.
M2	⑦	T1	The 16-bit contents of the H and L Registers are gated to the Address Bus.
	⑧		Machine status is gated to the Data Bus.
	⑨	T2	The contents of the memory location addressed by the contents of the Address Bus are gated to the Data bus.
	⑩	T3	The contents of the Data Bus are gated to the Destination Register, rd, within the CPU.

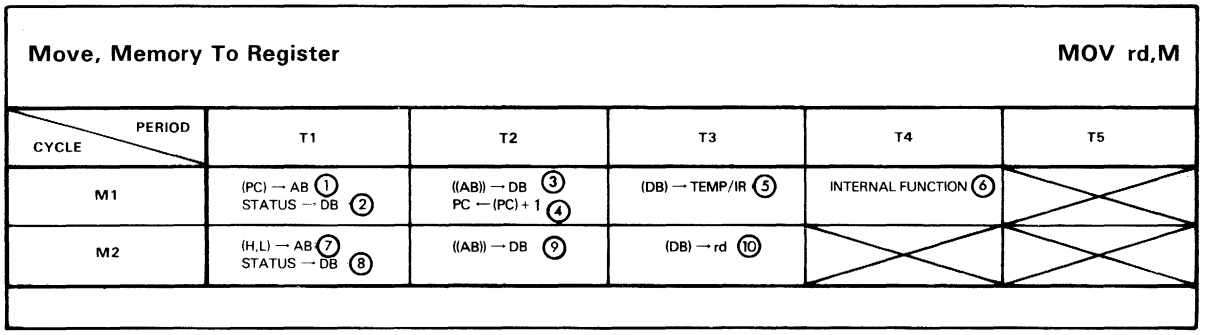


FIGURE 3-12 EVENT SCHEMATIC FOR MOVE MEMORY TO REGISTER INSTRUCTION

ADDRESSING MODES

The Am9080A provides five modes of memory addressing; these are:

Direct

3-byte instructions in which bytes 2 and 3 provide a 16-bit address, identifying one of 65,536 memory bytes, the maximum addressable memory space of the Am9080A microprocessor.

Register Indirect

A single byte opcode specifies internal registers that contain the required memory address. The register pair H and L most frequently provides the 16-bit, register indirect address. The B and C register pair or the D and E register pair provide the register indirect address for some memory reference instructions.

Register, single byte

The contents of a source register are transferred directly to a destination register.

Immediate, 2 or 3 byte

The operand is stored in the second, or in the second and third instruction bytes.

Implied Addressing

Although not an addressing mode in the strictest sense, instructions which perform operations on data stored in the Accumulator, and leave the result in the Accumulator, are said to be addressed in an implied mode. The instruction actually interprets the operand location as the Accumulator and no address is needed to obtain the operand.

STATUS FLAGS

During the execution of instructions, the results of arithmetic and logical operations performed on the operands by the ALU are stored in a Status Register. The individual bits are referred to as flags. The five flags which make up the Status Register of the Am9080A microprocessor are:

Zero	Result of an arithmetic or logic function.
Carry	Propagated out of the most significant bit of the Arithmetic and Logic Unit.
Parity	Odd or even number of binary 1s in the 8-bit result emanating from the Am9080A Arithmetic and Logic Unit.
Sign	The most significant bit of the ALU output for use when the result represents a signed binary number.
Intermediate Carry	Saves the result of a carry propagation between the 2^3 and 2^4 stages.

DEFINITIONS

The following definitions are used in the description of the Am9080A instruction set:

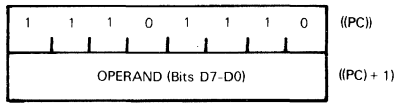
AB	Address Bus
AC	Auxiliary Carry = Carry propagation between 2^3 and 2^4 stages.
ACT	Accumulator Temporary Register
CY	Carry Status
d	Destination location (e.g., rd = Destination register).
DB	Data Bus
ddd	Destination location address
(H,L)	Contents of H and L registers, or memory location addressed by H and L registers.
((H,L))	Designates the contents of a memory location addressed by the 16-bit contents of the H and L registers.
INST	Any instruction code byte
INTE	Interrupt Enable flip-flop
IR	Instruction Register
Opcode	Instruction operation code byte
Operand	Operand of the instruction
P	Parity = Odd number of 1s in ALU result.
PCH	Eight most significant bits of the Program Counter.
PCL	Eight least significant bits of the Program Counter.
port	I/O device address
r	CPU register
rd	Destination register
rs	Source register
rp	Register pair
rpd	Destination register pair
rps	Source register pair
rpsh	Most significant register of source register pair
rpsl	Least significant register of source register pair
s	Source location (e.g., rs = Source register).
S	Sign of Result = ALU7
SR	Status Register
sss	Source location binary address
STATUS	Status Conditions appearing on Data Bus at T2 Φ1 time.
STATUS FLAGS	Condition representing results of an ALU operation.
TEMP	Temporary operand register
VVV	3-bit binary value, 000 to 111 inclusive.
VVVV	4-bit binary value, 0000 to 1111 inclusive.
W,Z	Temporary address registers
Z	Zero Result = $\overline{ALU7} \cdot \overline{ALU6} \cdot \overline{ALU5} \cdot \overline{ALU4} \cdot \overline{ALU3} \cdot \overline{ALU2} \cdot \overline{ALU1} \cdot \overline{ALU0}$
( )	The contents of
$\overline{(\ )}$	Complement of the contents of
(( ))	The contents of the contents of. The contents of the designated location in the inner brackets are interpreted as an address to a second location which supplies the 8-bit operand used by the instruction.
←	Receives. The notation ( ) ← means the location designation contained in the inner brackets is used as an address to which the operand will be stored.
→	Goes to
←→	Is exchanged with
+	Arithmetic Addition
-	Arithmetic Subtraction
x	Arithmetic Multiplication
$\wedge$	Logical AND
V	Logical OR
$\forall$	Logical Exclusive-OR

A complete list of all instructions can be found in the data sheet at the end of Chapter 4.

Add Immediate To Accumulator With Carry

ACI

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A) + ((PC) + 1) + (CY)

Description: The contents of the Accumulator, the contents of Byte 2 of the instruction ((PC) + 1), and the Carry status flag (CY) are added together. The result is placed in the Accumulator. The source operand ((PC) + 1) is not modified.

The addition is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: EE

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the addition.

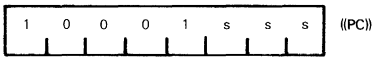
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) + (TEMP) + (CY) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

Add Register To Accumulator With Carry — ADC

Binary Format



Bytes

1

Clock Periods

4 if sss ≠ 110
7 if sss = 110

Operation:

A ← (A) + (rs) + CY; sss ≠ 110
A ← (A) + ((H,L)) + CY; sss = 110

Description: The contents of the Accumulator, the contents of the source location (sss), and the current state of the Carry status flag are added together. The result is returned to the Accumulator. The source location contents are not modified. When the source location is specified as a memory location (sss = 110), the H and L registers supply the 16-bit address to memory. The addition is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

s s s	REGISTER	HEX FORMAT
0 0 0	B	88
0 0 1	C	89
0 1 0	D	8A
0 1 1	E	8B
1 0 0	H	8C
1 0 1	L	8D
1 1 0	M	8E
1 1 1	A	8F

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the addition.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	(sss) → TEMP ACT ← (A)	

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) + (TEMP) + (CY) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

SOURCE IS MEMORY (sss = 110)

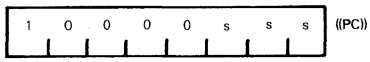
	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	TEMP ← (DB)		

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) + TEMP + (CY) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

Add Register To Accumulator

ADD s

Binary Format



Bytes

1

Clock Periods

4 if sss ≠ 110
7 if sss = 110

Operation: A ← (A) + (s); sss ≠ 110
A ← (A) + ((H,L)); sss = 110

Description: The contents of the Accumulator are added to the contents of the source register and the result returned to the Accumulator. The source register contents are not modified. If the source register is a memory location, the contents of the H and L register supply the 16-bit address to memory.

The addition is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

s s s	REGISTER	HEX FORMAT
0 0 0	B	80
0 0 1	C	81
0 1 0	D	82
0 1 1	E	83
1 0 0	H	84
1 0 1	L	85
1 1 0	M	86
1 1 1	A	87

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the addition.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (sss) ACT ← (A)	
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

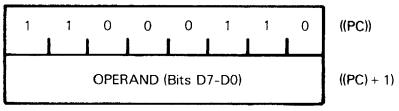
SOURCE IS MEMORY (sss = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	((AB)) · DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Add Immediate To Accumulator

ADI

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A) + ((PC) + 1)

Description: The contents of the Accumulator are added to the second byte of the instruction ((PC) + 1). The result is placed in the Accumulator. The source operand ((PC) + 1) is not modified.

The addition is not completed until T2 of M1 in the following instruction.

Hexadecimal Format: C6

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the addition.

Execution States:

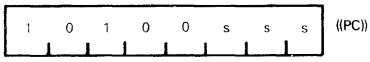
	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR TEMP ← (DB)	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (A) + TEMP ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

AND Source With Accumulator

ANA s

Binary Format



Bytes

1

Clock Periods

4 if sss ≠ 110
7 if sss = 110

Operations: A ← (A) + (rs)

Description: The contents of the Accumulator are logically "AND"ed with the contents of the designated source location. The results are placed in the Accumulator. When the source location designated is a memory location, the H and L registers supply the 16-bit address to memory. The AND is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

REGISTER	s s s	HEX FORMAT
B	0 0 0	A0
C	0 0 1	A1
D	0 1 0	A2
E	0 1 1	A3
H	1 0 0	A4
L	1 0 1	A5
M	1 1 0	A6
A	1 1 1	A7

Status Flags: Z, S, P are modified to reflect the results of the operation. CY and AC are reset.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (sss) ACT ← (A)	
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) ∧ (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

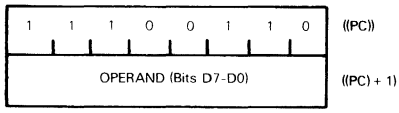
SOURCE IS MEMORY (sss = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(H,L) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) ∧ (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

AND With Accumulator Immediate

ANI operand

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A) Λ ((PC) + 1)

Description: The contents of the Accumulator are logically "AND"ed with the contents of the second byte of the instruction, (PC) + 1. The result is placed in the Accumulator.

The "AND" function is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: E6

Status Flags: Z, S, P are modified to reflect the result of the operation. CY and AC are reset.

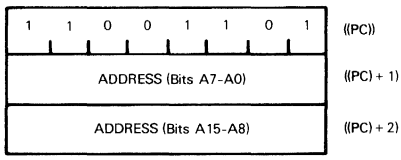
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) Λ (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Unconditional Subroutine Call

CALL address

Binary Format



Bytes

3

Clock Periods

17

Operation:

(SP) - 1 ← (PCH)
(SP) - 2 ← (PCL)
SP ← (SP) - 2
PC ← (PC + 2, PC + 1)

Description: The current Program Counter contents are pushed onto the Stack and Bytes 2 and 3 of the instruction are loaded to the Program Counter.

The functional sequence of execution is:

1) Stack Pointer is decremented.
2) Most significant eight bits of the Program Counter are stored at the memory location addressed by the Stack Pointer.
3) Stack Pointer is decremented.
4) Least significant eight bits of the Program Counter are stored to the memory location addressed by the Stack Pointer.
5) Bytes 2 and 3, which are contained in the W and Z registers, are copied into the Program Counter.

Hexadecimal Format: CD

Status Flags: No status flags are modified.

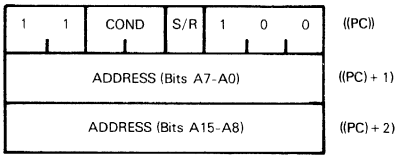
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	SP ← (SP)-1	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB)		
M4	(SP) → AB STATUS → DB	SP ← (SP)-1 (PCH) → DB	(AB) ← (DB)		
M5	(SP) → AB STATUS → DB	(PCL) → DB	(AB) ← (DB)		
M1 NEXT INSTRUCTION	(W,Z) → AB STATUS → DB	((AB)) → DB PC ← (W,Z) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Call To Subroutine Conditionally

CC CNC
CP CM
CPE CPO
CZ CNZ

Binary Format



Bytes

3

Clock Periods

17 if condition is true
11 if condition is false

Operation:

(SP) - 1 ← (PCH)
(SP) - 2 ← (PCL)
SP ← (SP) - 2
PC ← ((PC) + 2, (PC) + 1)

} If condition test is met

PC ← (PC) + 3; if condition test is not met

Description:

The status flag specified in the instruction opcode is tested for the specified binary state (S/R). If the condition matches the test specified, the Program Counter contents are written to the Stack and the Program Counter is loaded with the contents of Bytes 2 and 3 of the instruction. The eight most significant bits of PC (PCH) are written to the memory location addressed by the Stack Pointer contents after decrement, (SP-1). The eight least significant bits of the Program Counter (PCL) are written to the next location (SP-2). The most significant eight bits of the Program Counter are loaded from Byte 3 and the least significant eight bits of the Program Counter are loaded from Byte 2 of the instruction.

If the condition tested is met; the M4 and M5 Stack Write machine cycles are executed. The next M1 Instruction Fetch cycle is then modified to provide the W and Z register contents to the Address Bus. If the condition is not met, the next Instruction Fetch is entered at the end of machine cycle M3.

Hexadecimal Formats:

The Call conditions are:

MNEMONIC	COND	S/R	CALL CONDITION	HEX FORMAT
CC	01	1	CY=1; NO CARRY	DC
CNC	01	0	CY=0; CARRY SET	D4
CP	11	0	S=0; POSITIVE	F4
CM	11	1	S=1; NEGATIVE	FC
CPE	10	1	P=1; PARITY EVEN	EC
CPO	10	0	P=0; PARITY ODD	E4
CZ	00	1	Z=1; NOT ZERO	CC
CNZ	00	0	Z=0; ZERO	C4

Execution States:

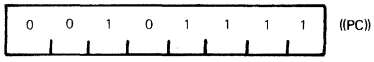
Status Flags: No status flags are modified.

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEST CONDITION	SP ← (SP)-1 IF CONDITION TESTS VALID
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB) IF CONDITION INVALID CONTINUE WITH NEXT M1		
M4	(SP) → AB STATUS → DB	SP ← (SP)-1 (PCH) → DB	(AB) ← (DB)		
M5	(SP) → AB STATUS → DB	(PCL) → DB	(AB) ← (DB)		
M1, NEXT INSTRUCTION IF CONDITION VALID	(W,Z) → AB STATUS → DB	((AB)) → DB PC ← (W,Z) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Complement Accumulator

CMA

Binary Format



Bytes

1

Clock Periods

4

Operation: $A \leftarrow (\overline{A})$

Description: The contents of the Accumulator are complemented.

Hexadecimal Format: 2F

Status Flags: No status flags are modified.

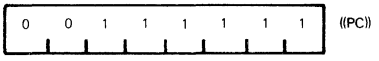
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	$A \leftarrow (\overline{A})$	

Complement Carry Status

CMC

Binary Format



Bytes

1

Clock Periods

4

Operation: CY ← $(\overline{CY})$

Description: The Carry bit is complemented.

Hexadecimal Format: 3F

Status Flags: Only the Carry flag is affected.

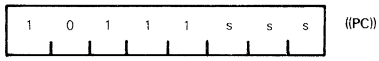
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	CY ← $(\overline{CY})$	

Compare Source With Accumulator

CMP s

Binary Format



Bytes

1

Clock Periods

4 if sss ≠ 110
7 if sss = 110

Operations: CY,Z ← (A) - (rs)

Description: The contents of the designated source are subtracted from the contents of the Accumulator. The Accumulator and the contents of the designated source location are not altered. When the designated source location is a memory location, the H and L registers supply a 16-bit address to memory.

The subtract is performed for comparison of the operands only.

The function is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

REGISTER	s s s	HEX FORMAT
B	0 0 0	B8
C	0 0 1	B9
D	0 1 0	BA
E	0 1 1	BB
H	1 0 0	BC
L	1 0 1	BD
M	1 1 0	BE
A	1 1 1	BF

Status Flags: CY is set to 1 if (A) < (sss). Z is set to 1 if (A) = (sss).

S, P, AC are modified to reflect the result of the comparison.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A) TEMP ← (sss)	
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	CY,Z ← (ACT)-(TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

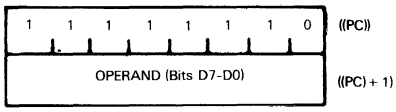
SOURCE IS MEMORY (sss = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	CY,Z ← (ACT) - (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Compare With Accumulator Immediate

CPI

Binary Format



Bytes

2

Clock Periods

7

Operation: CY,Z ← (A)-((PC) + 1)

Description: The contents of the second byte of the instruction are subtracted from the Accumulator contents. The result is indicated in the CY and Z status flags. The Accumulator contents and the contents of Byte 2 of the instruction are not altered.

The function is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: FE

Status Flags: CY is set to 1 if (A) < ((PC) + 1). Z is set to 1 if (A) = ((PC) + 1). S, P, AC are modified to reflect the results of the operation.

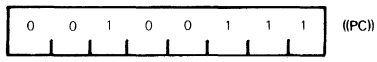
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	CY,Z ← (ACT)-(TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Decimal Adjust Accumulator

DAA

Binary Format



Bytes

1

Clock Periods

4

Operation:

STATUS		OPERATION
CY or 4 msb's > 9	AC or 4 lsb's > 9	
0	0	A ← (A)
0	1	A ← (A) + 06_{16}
1	0	A ← (A) + 60_{16}
1	1	A ← (A) + 66_{16}

Description: The contents of the Accumulator are altered from a binary value to two 4-bit binary coded decimal digits. If the four least significant bits of the Accumulator are greater than nine or if the Auxiliary Carry (AC) is set, 6 (0110) is added to the four least significant bits. If the four most significant bits of the Accumulator are greater than 9 or if the Carry status (CY) is set, 6 is added to the four most significant bits.

Hexadecimal Format: 27

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the decimal adjust.

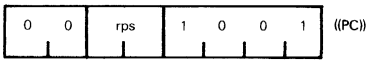
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB	(DB) → TEMP/IR	A ← (A) + CORRECTION STATUS ← (A) + CORRECTION	

Add Register Pair To H And L Registers

DAD rps

Binary Format



Bytes

1

Clock Periods

10

Operation: H,L ← (H,L) + (rps)

Description: The 16-bit contents of the designated source register pair are added to the H and L registers. The result is placed in the H,L registers.

The source operand is not altered.

Hexadecimal Formats:

OPCODE	rps	HEX FORMAT
DAD B	00	09
DAD D	01	19
DAD H	10	29
DAD SP	11	39

Status Flags: CY status is modified to reflect the result of the addition. No other status flags are altered.

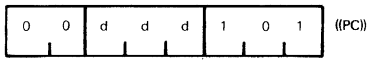
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	ACT ← (rpsl)	TEMP ← (L) ALU ← (TEMP) + (ACT)	L ← (ALU) CY ← (ALU)		
M3	ACT ← (rpsh)	TEMP ← (H) ALU ← (TEMP) + (ACT)	H ← (ALU) CY ← (ALU)		

Decrement Destination Location

DCR d

Binary Format



Bytes

1

Clock Periods

5 if ddd ≠ 110
10 if ddd = 110

Operations: rd ← (rd) - 1

Description: The contents of the designated location are decremented and the result restored to the designated location. If a memory location is designated, the H and L registers supply the 16-bit address to memory.

Hexadecimal Formats:

OPCODE	d d d	HEX FORMAT
DCR B	0 0 0	05
DCR C	0 0 1	0D
DCR D	0 1 0	15
DCR E	0 1 1	1D
DCR H	1 0 0	25
DCR L	1 0 1	2D
DCR M	1 1 0	35
DCR A	1 1 1	3D

Status Flags: Z, S, P, AC are modified to reflect the result of the decrement. CY is not modified.

Execution States:

REGISTER IS DESTINATION (ddd ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (ddd) ALU ← (TEMP)-1	ddd ← (ALU)

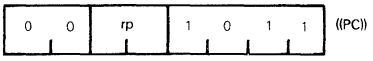
MEMORY IS DESTINATION (ddd = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	TEMP ← (DB) ALU ← (TEMP) - 1		
M3	(H,L) → AB STATUS → DB	(ALU) → DB	(AB) ← (DB)		

Decrement Register Pair

DCX rp

Binary Format



Bytes

1

Clock Periods

5

Operations: rp ← (rp) - 1

Description: The designated register pair (rp) is decremented (16-bit binary subtraction) and the result is restored to the designated register pair.

Hexadecimal Formats:

OPCODE	rp	HEX FORMAT
DCX B	00	0B
DCX D	01	1B
DCX H	10	2B
DCX SP	11	3B

Status Flags: No status flags are modified.

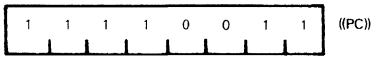
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	rp ← (rp)-1	

Disable Interrupts

DI

Binary Format



Bytes

1

Clock Periods

4

Operation: INTE ← 0

Description: The Interrupt Enable flip-flop is reset.

Hexadecimal Format: F3

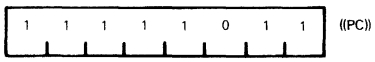
Status Flags: No status flags are modified.

Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTE ← 0	

Enable Interrupt **EI**

Binary Format



Bytes
1

Clock Periods
4

Operation: INTE ← 1

Description: The Interrupt Enable flip-flop is set.

Hexadecimal Format: FB

Status Flags: No status flags are modified.

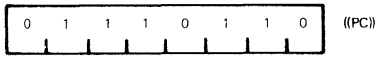
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTE ← 1	

Halt And Enter Wait State

HLT

Binary Format



Bytes

1

Clock Periods

7 or more

Operation: $\overline{\text{HALT}}$

Description: The CPU finishes execution of the current instruction and then enters the Halt Acknowledge machine cycle. The Address Bus and the Data Bus are put in the high impedance state. Wait states are induced in every clock period while machine is in Halt Acknowledge Machine Cycle.

An interrupt or reset must be processed to exit from the Halt condition.

Hexadecimal Format: 76

Status Flags: No status flags are modified.

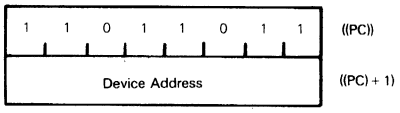
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	Hi Z → AB Hi Z → DB			

Input To Accumulator

IN port

Binary Format



Bytes

2

Clock Periods

10

Operation: A ← (port)

Description: The Accumulator is loaded with the contents of the Data Bus supplied by the I/O port accessed by the Device Address.

Hexadecimal Format: DB

Status Flags: No status flags are modified.

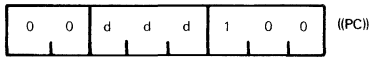
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB) W ← (DB)		
M3	(W,Z) → AB STATUS → DB	DB ← (port)	A ← (DB)		

Increment Destination Location

INR d

Binary Format



Bytes

1

Clock Periods

5 if ddd ≠ 110
10 if ddd = 110

Operations: rd ← (rd) + 1

Description: The contents of the designated location are incremented and returned to the designated location. If a memory location is designated, the H and L registers supply the 16-bit address to memory.

Hexadecimal Formats:

OPCODE	d d d	HEX FORMAT
INR B	0 0 0	04
INR C	0 0 1	0C
INR D	0 1 0	14
INR E	0 1 1	1C
INR H	1 0 0	24
INR L	1 0 1	2C
INR M	1 1 0	34
INR A	1 1 1	3C

Status Flags: Z, S, P, AC are modified to reflect the result of the increment. CY is not modified.

Execution States:

REGISTER IS DESTINATION (ddd ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (ddd) ALU ← (TEMP) + 1	ddd ← (ALU)

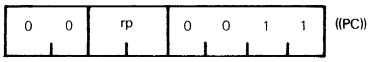
MEMORY IS DESTINATION (ddd = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	TEMP ← (DB) ALU ← (TEMP) + 1		
M3	(H,L) → AB STATUS → DB	(ALU) → DB	(AB) ← (DB)		

Increment Register Pair

INX rp

Binary Format



Bytes

1

Clock Periods

5

Operation: rp ← (rp) + 1

Description: The designated register pair (rp) is incremented (16-bit binary addition) and the result is restored to the designated register pair.

Hexadecimal Formats:

OPCODE	rp	HEX FORMAT
INX B	00	03
INX D	01	13
INX H	10	23
INX SP	11	33

Status Flags: No status flags are modified.

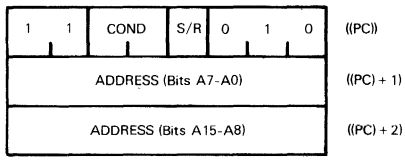
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	rp ← (rp) + 1	

Jump Conditionally

JC JNC
JP JM
JPE JPO
JZ JNZ

Binary Format



Bytes
3

Clock Periods
10

Operation: PC ← ((PC) + 2, (PC) + 1); if Flag = S/R
PC ← ((PC) + 3); if Flag = S/R

Description: One of four status flags is tested to meet the S/R (set or reset) condition. If the condition of the status flag meets the condition specified in the (S/R) bit, the Program Counter is effectively replaced with the contents of Bytes 2 and 3 of the instruction. Otherwise the Program Counter is incremented.

Hexadecimal Formats:

MNEMONIC	COND	S/R	JUMP CONDITION	HEX FORMAT
JC	01	1	CY=1; CARRY SET	DA
JNC	01	0	CY=0; NO CARRY	D2
JP	11	0	S=0; POSITIVE	F2
JM	11	1	S=1; NEGATIVE	FA
JPE	10	1	P=1; PARITY EVEN	EA
JPO	10	0	P=0; PARITY ODD	E2
JZ	00	1	Z=1; ZERO SET	CA
JNZ	00	0	Z=0; NOT ZERO	C2

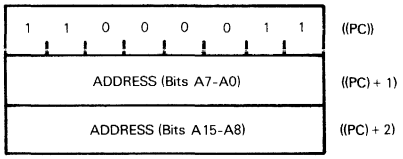
Status Flags: No status flags are modified.

Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEST CONDITION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB)		
M1, NEXT INSTRUCTION TEST VALID	(W,Z) → AB STATUS → DB	((AB)) → DB PC ← (W,Z) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		
M1, NEXT INSTRUCTION TEST INVALID	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Jump Unconditionally **JMP address**

Binary Format



Bytes
3

Clock Periods
10

Operation: PC ← ((PC) + 1, (PC) + 2)

Description: The Program Counter is loaded with the 16 bits contained in Byte 2 and Byte 3 of the instruction. Byte 2 contains the eight least significant bits and Byte 3 contains the eight most significant bits.

The next instruction to be fetched will be at location ((PC) + 1,(PC) + 2).

The next Instruction Fetch cycle is modified to provide the contents of the W and Z registers to the Address Bus.

Hexadecimal Format: C3

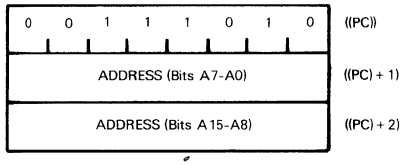
Status Flags: No status flags are modified.

Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB)		
M1 NEXT INSTRUCTION	(W,Z) → AB STATUS → DB	((AB)) → DB PC ← (W,Z) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Load Accumulator Direct — LDA

Binary Format



Bytes
3

Clock Periods
13

Operation: A ← ((PC) + 2, (PC) + 1)

Description: The eight bits stored in a memory location pointed to by Bytes 2 and 3 of the instruction are copied to the Accumulator. The contents of the memory location accessed are not altered. Bytes 2 and 3 form the full 16-bit address of the desired operand location. The address is first loaded from Bytes 2 and 3 to the Z and W temporary registers, then supplied to the Address Bus to access the desired location in memory.

Hexadecimal Format: 3A

Status Flags: No status flags are modified.

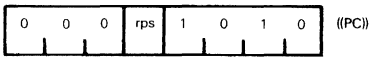
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → Z		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → W		
M4	(W,Z) → AB STATUS → DB	((AB)) → DB	A ← (DB)		

Load Accumulator Indirect

LDAX rps

Binary Format



Bytes

1

Clock Periods

7

Operation: A ← ((rps))

Description: The contents of the memory location pointed to by the designated register pair (rps) are copied to the Accumulator. The contents of the memory location accessed are not altered. The designated register pair supplies a 16-bit address to the Address Bus for accessing the desired location. The register pair specified by rps can only be Registers B and C (rps = B) or Registers D and E (rps = D). The contents of the register pair (rps) are not altered.

Hexadecimal Formats:

rps	HEX FORMAT
B	0A
D	1A

Status Flags: No status flags are modified.

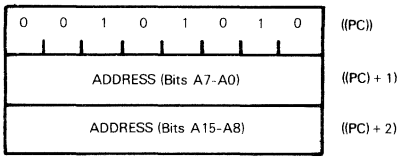
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(rp) → AB STATUS → DB	((AB)) → DB	A ← (DB)		

Load H And L Registers Direct

LHLD

Binary Format



Bytes

3

Clock Periods

16

Operation: L ← ((PC) + 2, (PC) + 1)
H ← ((PC) + 2, (PC) + 1) + 1)

Description: Two consecutive locations in memory addressed by the contents of Bytes 2 and 3 of the instruction [(PC) + 1, (PC) + 2]are copied to the H and L registers. The Program Counter is incremented to access Bytes 2 and 3 and copy these bytes into the Temporary Registers Z and W to form the address of the first of the two memory locations to be loaded to H and L. Data accessed from this location is copied to Register L. The 16-bit address held in Temporary Registers Z and W is incremented to address the next byte which is copied to the H register. None of the memory locations that are copied are altered.

Hexadecimal Format: 2A

Status Flags: No status flags are modified.

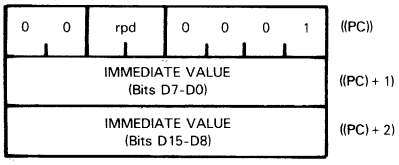
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB)		
M4	(W,Z) → AB STATUS → DB	((AB)) → DB W,Z ← (W,Z) + 1	L ← (DB)		
M5	(W,Z) → AB STATUS → DB	((AB)) → DB	H ← (DB)		

Load Register Pair Immediate

LXI rpd

Binary Format



Bytes

3

Clock Periods

10

Operation:

rd ← ((PC) + 2)
rd + 1 ← ((PC) + 1)

Description: The eight bits stored in Byte 3 of the instruction are copied to Register rd where rd is designated as the B(00), D(01), H(10) register or the most significant eight bits of the Stack Pointer (11) register. The eight bits in Byte 2 of the instruction are copied to Register rd + 1 where rd + 1 is the C, E, L register respectively or least significant eight bits of the Stack Pointer register. The immediate values stored in Bytes 2 and 3 of the instruction are not altered.

Hexadecimal Formats:

rpd	HEX FORMAT
B	01
D	11
H	21
SP	31

Status Flags: No status flags are modified.

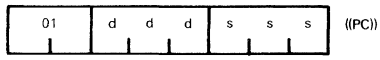
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	rd ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	rd + 1 ← (DB)		

Move

MOV d,s

Binary Format



Bytes

1

Clock Periods

5,7

Operation:

rd ← (rs); if ddd,sss ≠ 110
rd ← ((H,L)); if ss = 110
(H,L) ← (rs); if ddd = 110

Description:

The contents of the source location (s) are copied to the destination location (d). The source and destination addresses are contained as 3-bit addresses within the instruction format. However, when either the source or destination address is 110, then the contents of the H and L registers are used as the 16-bit address of a memory location where the source or destination operand will be located.

The contents of the source location are not modified.

Hexadecimal Formats:

Status Flags: No status flags are modified.

DESTINATION LOCATION \ SOURCE LOCATION	B	C	D	E	H	L	M	A
B	40	41	42	43	44	45	46	47
C	48	49	4A	4B	4C	4D	4E	4F
D	50	51	52	53	54	55	56	57
E	58	59	5A	5B	5C	5D	5E	5F
H	60	61	62	63	64	65	66	67
L	68	69	6A	6B	6C	6D	6E	6F
M	70	71	72	73	74	75		77
A	78	79	7A	7B	7C	7D	7E	7F

LOCATION	BINARY ADDRESS
B	000
C	001
D	010
E	011
H	100
L	101
M	110
A	111

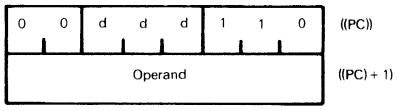
Execution States:

	T1	T2	T3	T4	T5
FUNCTION rd ← (rs) **M1**	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	(rs) → TEMP	(TEMP) → rd
FUNCTION rd ← ((H,L)) **M1**	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	(DB) → rd		
FUNCTION (H,L) ← rs **M1**	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	(rs) → TEMP	
M2	(H,L) → AB STATUS → DB	(TEMP) → DB	(DB) → (AB)		

Move Immediate

MVI d

Binary Format



Bytes

2

Clock Periods

7 if ddd ≠ 110
10 if ddd = 110

Operation: rd ← ((PC) + 1), if ddd ≠ 110
(H,L) ← ((PC) + 1), if ddd = 110

Description: The contents of Byte 2 of the instruction are stored to the destination location. When the destination (ddd) is 110, the destination location is the memory location at the address pointed to by the 16-bit contents of Registers H and L. The contents of the source operand at Byte 2 ((PC) + 1) of the instruction are not modified.

Hexadecimal Formats:

DESTINATION LOCATION

B	C	D	E	H	L	M	A
06	0E	16	1E	26	2E	36	3E

Status Flags: No flags are modified.

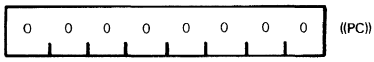
Execution States:

	T1	T2	T3	T4	T5
FOR ddd ≠ 110 M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → rd		

FOR ddd = 110 M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP		
M3	(H,L) → AB STATUS → DB	(TEMP) → DB	(DB) → (AB)		

No Operation **NOP**

Binary Format



Bytes
1

Clock Periods
4

Operation: None

Description: No operation is performed.

Hexadecimal Format: 00

Status Flags: No status flags are modified.

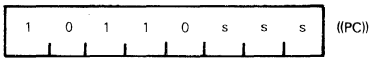
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	

OR Inclusive Source With Accumulator

ORA s

Binary Format



Bytes

1

Clock Periods

4 if sss ≠ 110
7 if sss = 110

Operations: A ← (A) V (rs)

Description: The contents of the Accumulator are logically "OR"ed with the contents of the designated source location. The result is placed in the Accumulator. When the designated source location is a memory location, the contents of the H,L registers supply the 16-bit address to memory. The "OR" function is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats: See Table

Status Flags: Z, S, P are modified to reflect the result of the operation. CY and AC are reset.

REGISTER	s s s	HEX FORMAT
B	0 0 0	B0
C	0 0 1	B1
D	0 1 0	B2
E	0 1 1	B3
H	1 0 0	B4
L	1 0 1	B5
M	1 1 0	B6
A	1 1 1	B7

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A) TEMP ← (sss)	
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) V (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

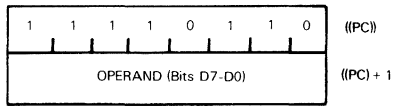
SOURCE IS MEMORY (sss = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) V (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

OR Inclusive With Accumulator Immediate

ORI

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A) V ((PC) + 1)

Description: The contents of the Accumulator are logically "OR"ed with the contents of Byte 2 of the instruction ((PC) + 1). The result is placed in the Accumulator.

The "OR" function is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: F6

Status Flags: Z, S, P are modified to reflect the result of the operation. CY and AC are reset.

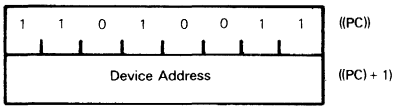
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) V (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Output From Accumulator

OUT port

Binary Format



Bytes

2

Clock Periods

10

Operation: port ← (A)

Description: The contents of the Accumulator are copied to the I/O port addressed by the second byte of the instruction. The contents of the Accumulator are not modified.

Hexadecimal Format: D3

Status Flags: No status flags are modified.

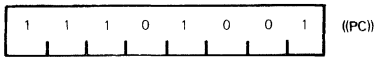
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) ! TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB) W ← (DB)		
M3	(W,Z) → AB STATUS → DB	(A) → DB	port ← (DB)		

Load Program Counter

PCHL

Binary Format



Bytes

1

Clock Periods

5

Operation: PCH ← (H)
PCL ← (L)

Description: The contents of the H and L registers are copied to the Program Counter. The most significant eight bits of the Program Counter are copied from the H register and the least significant eight bits are copied from the L register.

Hexadecimal Format: E9

Status Flags: No status flags are modified.

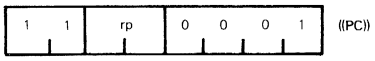
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	PC ← (H,L)	

Pop Off Stack To Register Pair

POP rp

Binary Format



Bytes

1

Clock Periods

10

Operations: rp ← ((SP), (SP) + 1)

Description: The contents of the memory location addressed by the Stack Pointer (SP) are copied to the eight least significant bits (rpl) of the designated register pair (Register C,E,L, or SR). The Stack Pointer is incremented and the contents of the next memory location (SP + 1) are copied to the most significant eight bits (rph) of the designated register pair (Register B,D,H, or A).

Hexadecimal Formats:

rp	REGISTER PAIR	HEX FORMAT
00	B	C1
01	D	D1
10	H	E1
11	PSW	F1

Status Flags: No status flags are modified when the designated register pair is B,D, or H. When the PSW register pair is designated, the status flats are copied from the memory location addressed by the contents of the Stack Pointer.

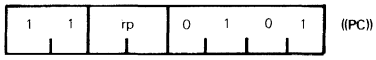
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(SP) → AB STATUS → DB	((AB)) → DB SP → (SP) + 1	rpl ← (DB)		
M3	(SP) → AB STATUS → DB	((AB)) → DB SP ← (SP) + 1	rph ← (DB)		

Push Register Pair Onto Stack

PUSH rp

Binary Format



Bytes

1

Clock Periods

11

Operation: (SP) - 1, (SP) - 2 ← (rp)

Description: The Stack Pointer is decremented. Next the most significant eight bits (rph) of the designated register pair (the contents of B, D, H, or A) are copied to the memory location addressed by the Stack Pointer. The Stack Pointer is again decremented and the least significant eight bits (rpl) of the designated register pair (the contents of C, E, L, or SR) are copied to the memory location addressed by the Stack Pointer.

Hexadecimal Formats:

OPCODE	rp	HEX FORMAT
B	00	C5
D	01	D5
H	10	E5
PSW	11	F5

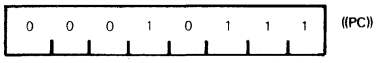
Status Flags: No status flags are modified.

Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	SP ← (SP)-1	
M2	(SP) → (AB) STATUS → DB	SP ← (SP)-1 (rph) → DB	(AB) ← (DB)		
M3	(SP) → AB STATUS → DB	(rpl) → DB	(AB) ← (DB)		

Rotate Accumulator Left Through Carry — RAL

Binary Format



Bytes

1

Clock Periods

4

Operation: An + 1 ← (An); CY ← (A7); A0 ← (CY)

Description: The contents of the Accumulator are rotated left one position through the Carry status flag. The Carry flag is shifted to the least significant bit of the Accumulator, A0.

Hexadecimal Format: 17

Status Flags: CY receives the value of A7 before the shift. Z, S, P, AC are not modified.

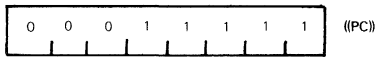
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	An ← (An + 1) CY ← (A0) A7 ← (CY)	

Rotate Accumulator Right Through Carry

RAR

Binary Format



Bytes

1

Clock Periods

4

Operation: An ← (An + 1); CY ← (A0); A7 ← (CY)

Description: The contents of the Accumulator are rotated right one position through the Carry status flag. The Carry flag is shifted to the most significant bit of the Accumulator, A7.

Hexadecimal Format: 1F

Status Flags: CY receives the value of A0 before the shift. Z, S, P, AC are not modified.

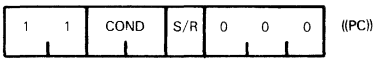
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	An ← (An + 1) CY ← (A0) A7 ← (CY)	

Return Conditionally

RC RNC
RP RM
RPE RPO
RZ RNZ

Binary Format



Bytes

1

Clock Periods

11 if condition is true
5 if condition is false

Operation:

PCL ← ((SP))
PCH ← ((SP) + 1)
SP ← (SP) + 2
} If Condition test is met

PC ← (PC) + 1 If Condition is not met

Description:

A test of the Status Flags is made to the conditions specified in the opcode. If the Status Register meets the test condition, the Program Counter is loaded with two bytes from the top of the Stack and the Stack Pointer is incremented by two. Otherwise, the Program Counter is incremented.

If the test condition is met, machine cycles M2 and M3 are executed and the next M1 Instruction Fetch is modified to place the contents of W and Z registers on the Address Bus. Otherwise, a normal Instruction Fetch cycle is initiated after the M1 Instruction Fetch cycle of the conditional Return instruction.

Hexadecimal Formats:

MNEMONIC	COND	S/R	RETURN CONDITION	HEX FORMAT
RC	0i	1	CY=1; CARRY SET	D8
RNC	01	0	CY=0; NO CARRY	D0
RP	11	0	S=0; POSITIVE	F0
RM	11	1	S=1; NEGATIVE	F8
RPE	10	1	P=1; PARITY IS EVEN	E8
RPO	10	0	P=0; PARITY IS ODD	E0
RZ	00	1	Z=1; RETURN IF ZERO	C8
RNZ	00	0	Z=0; RETURN NOT ZERO	C0

Execution States:

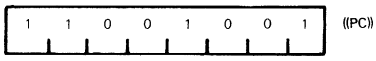
Status Flags: No status flags are modified.

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEST STATUS FLAGS FOR CONDITION	
M1 IF CONDITION NOT MET	(PC) → AB STATUS → DB	NORMAL INSTRUCTION SEQUENCE RESUMES			
M2 IF CONDITION NOT MET	(SP) → AB STATUS → DB	((AB)) → DB SP ← (SP) + 1	Z ← (DB)		
M3	(SP) → AB STATUS → DB	((AB)) → DB	W ← (DB)		
M1 NEXT INSTRUCTION	(W,Z) → AB STATUS → DB	(AB) → DB PC ← (W,Z) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Return Unconditionally

RET

Binary Format



Bytes

1

Clock Periods

10

Operation:

PCL ← ((SP))
PCH ← ((SP) + 1)
SP ← (SP) + 2

Description:

Two bytes are pulled from the Stack and copied to the Program Counter. The Stack Pointer is incremented twice to point to the next position on the Stack.

The next Instruction Fetch cycle is modified to provide the contents of the W and Z registers to the Address Bus.

Hexadecimal Format: C9

Status Flags: No status flags are modified.

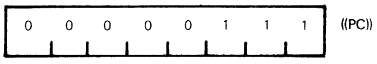
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(SP) → AB STATUS → DB	((AB)) → DB SP ← (SP) + 1	Z ← (DB)		
M3	(SP) → AB STATUS → DB	((AB)) → DB SP ← (SP) + 1	W ← (DB)		
M1 NEXT INSTRUCTION	(W,Z) → AB STATUS → DB	((AB)) → DB PC ← (W,Z) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Rotate Accumulator Left

RLC

Binary Format



Bytes

1

Clock Periods

4

Operation: An + 1 ← (An); A0 ← (A7); CY ← (A7)

Description: The contents of the Accumulator are rotated left one position. The most significant bit of the Accumulator, A7, is placed in A0 and CY.

Hexadecimal Format: 07

Status Flags: CY ← (A7), Z, S, P, AC are not modified.

CY receives the value of A7 before bits are rotated.

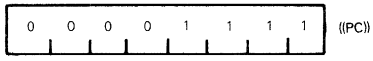
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	An + 1 ← (An) A0 ← (A7) CY ← (A7)	

Rotate Accumulator Right

RRC

Binary Format



Bytes

1

Clock Periods

4

Operation: An ← (An + 1); A7 ← (A0); CY ← (A0)

Description: The contents of the Accumulator are rotated right one position. The least significant bit of the Accumulator is placed in A7 and CY.

Hexadecimal Format: 0F

Status Flags: CY receives the value of A0 prior to the rotate. Z, S, P, AC are not modified.

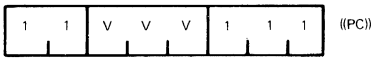
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	An ← (An + 1) A7 ← (A0) CY ← (A0)	

Restart

RST n

Binary Format



Bytes

1

Clock Periods

11

Operation:

(SP) - 1 ← (PCH)
(SP) - 2 ← (PCL)
SP ← (SP) - 2
PCL ← 00VVV000
PCH ← 00000000

Description:

The Program Counter is copied to the next two available locations on the Stack. Next, the Program Counter is loaded with a 16-bit value containing the address bits VVV of the instruction opcode in bits 5, 4, 3 of the Program Counter. All other bits are reset in the Program Counter.

A memory address is formed in the temporary registers (W,Z) such that W ← 00000000 and Z ← 00VVV000. This address is used in the next instruction fetch instead of PC; then it is incremented and loaded to PC to complete the jump to the restart location.

Hexadecimal Formats:

OPCODE	V V V	HEX FORMAT
RST 0	0 0 0	C7
RST 1	0 0 1	CF
RST 2	0 1 0	D7
RST 3	0 1 1	DF
RST 4	1 0 0	E7
RST 5	1 0 1	EF
RST 6	1 1 0	F7
RST 7	1 1 1	FF

Status Flags:

No status flags are modified.

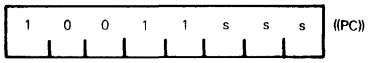
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR W ← 00000000	SP ← (SP)-1	
M2	(SP) → AB STATUS → DB	SP ← (SP)-1 (PCH) → DB	(AB) ← (DB)		
M3	(SP) → AB STATUS → DB	(PCL) → DB Z ← 00VVV000	(AB) ← (DB)		
M1 NEXT INSTRUCTION	(W,Z) → AB STATUS → DB	((AB)) → DB PC ← (W,Z) + 1			

Subtract Source And Borrow From Accumulator

SBB s

Binary Format



Bytes

1

Clock Periods

4/7
4 if sss ≠ 110
7 if sss = 110

Operation:

A←(A)−(rs)−CY; sss≠110
A←(A)−(H,L)−B; sss=110

Description:

The contents of the source location are subtracted from the Accumulator. The Carry status (CY) is subtracted from this result. The result is placed in the Accumulator. The designated source location is not altered.

When a memory location is designated as the source (sss = 110), the H and L registers supply the 16-bit address to memory.

The subtraction is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

REGISTER	s s s	HEX FORMAT
B	0 0 0	98
C	0 0 1	99
D	0 1 0	9A
E	0 1 1	9B
H	1 0 0	9C
L	1 0 1	9D
M	1 1 0	9E
A	1 1 1	9F

Status Flags:

Z, S, P, CY, AC are modified to reflect the results of the subtraction.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

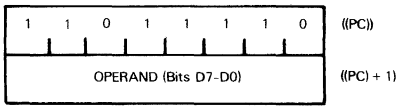
	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (sss) ACT ← (A)	
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT)-(TEMP) -(CY) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

SOURCE IS MEMORY (sss = 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	TEMP ← (DB)		
M1 NEXT INSTRUCTION'	(PC) → AB STATUS → DB	A ← (ACT)-(TEMP) -(CY) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Subtract With Borrow From Accumulator Immediate — SBI

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A)-((PC) + 1)-(CY)

Description: The contents of the second byte of the instruction ((PC) + 1) are subtracted from the Accumulator. The Carry status (CY) is subtracted from this result. The result is placed in the Accumulator. The contents of the source operand ((PC) + 1) are not altered.

The subtraction is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: DE

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the subtraction.

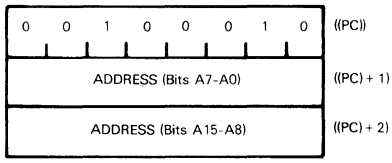
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR		
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT)-(TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Store H and L Registers Direct

SHLD

Binary Format



Bytes

3

Clock Periods

16

Operation: ((PC) + 2, (PC) + 1) ← (L)
([(PC) + 2, (PC) + 1] + 1) ← (H)

Description: The H and L registers are transferred to two consecutive locations in memory determined by the 16-bit address formed in Bytes 2 and 3 of the instruction. Bytes 2 and 3 form the 16-bit address of a memory location into which the L Register is copied. The address is then incremented to access the next sequential location in memory into which the H Register is copied. The contents of the H and L registers are not altered.

Hexadecimal Format: 22

Status Flags: No status flags are modified.

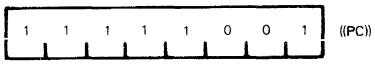
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB)		
M4	(W,Z) → AB STATUS → DB	(L) → DB W,Z ← (W,Z) + 1	(AB) ← (DB)		
M5	(W,Z) → AB STATUS → DB	(H) → DB	(AB) → (DB)		

Copy H and L Registers To The Stack Pointer

SPHL

Binary Format



Bytes

1

Clock Periods

5

Operation: SP ← (H,L)

Description: The 16-bit contents of the H and L registers are copied to the Stack Pointer. The H register will supply the most significant eight bits and the L register will supply the least significant eight bits. The contents of the H and L registers are not altered.

Hexadecimal Format: F9

Status Flags: No status flags are modified.

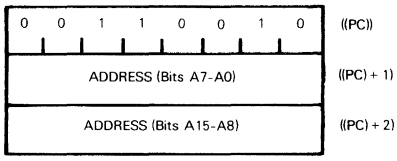
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	SP ← (H,L)	

Store Accumulator Direct

STA

Binary Format



Bytes

3

Clock Periods

13

Operation: ((PC) + 2, (PC) + 1) ← (A)

Description: The contents of the Accumulator are copied to a location in memory which is addressed by the 16-bit contents of Bytes 2 and 3 of the instruction.

Hexadecimal Format: 32

Status Flags: No status flags are modified.

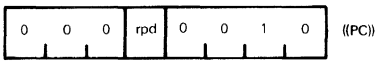
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	Z ← (DB)		
M3	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	W ← (DB)		
M4	(W,Z) → AB STATUS → DB	(A) → DB	(AB) ← (DB)		

Store Accumulator Indirect

STAX rpd

Binary Format



Bytes

1

Clock Periods

7

Operation: (rpd) ← (A)

Description: The contents of the Accumulator are copied into the location in memory addressed by the contents of the register pair designated rpd. When rpd specifies "B", the B and C registers will be used to supply the memory address. When rpd specifies "D", the D and E registers specify the memory address.

The contents of the Accumulator are not modified.

Hexadecimal Formats:

rpd	HEX FORMAT
B	02
D	12

Status Flags: No status flags are altered.

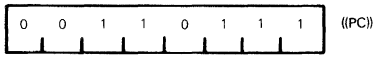
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(rpd) → AB STATUS → DB	(A) → DB	(AB) ← (DB)		

Set Carry Status

STC

Binary Format



Bytes

1

Clock Periods

4

Operation: CY ← 1

Description: The Carry bit is set to binary 1.

Hexadecimal Format: 37

Status Flags: Only the Carry flag is affected.

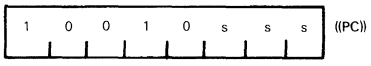
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	CY ← 1	

Subtract Source From Accumulator

SUB s

Binary Format



Bytes

1

Clock Periods

4/7
4 if sss ≠ 110
7 if sss = 110

Operation: A ← (A) + (rs)

Description: The contents of the source location are subtracted from the Accumulator. The result is placed in the Accumulator. The contents of the designated source location are not altered. When the memory is designated as the source location, the H and L registers supply the 16-bit address to memory.

The subtraction is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

REGISTER	s s s	HEX FORMAT
B	0 0 0	90
C	0 0 1	91
D	0 1 0	92
E	0 1 1	93
H	1 0 0	94
L	1 0 1	95
M	1 1 0	96
A	1 1 1	97

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the subtraction.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (sss) ACT ← (A)	

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT)-(TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

SOURCE IS MEMORY (sss = 110)

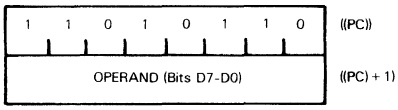
	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(H,L) → AB STATUS → DB	((AB)) → DB	TEMP ← (DB)		

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT)-(TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

Subtract From Accumulator Immediate

SUI

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A)-((PC) + 1)

Description: The contents of the second byte of the instruction ((PC) + 1) are subtracted from the contents of the Accumulator. The result is placed into the Accumulator. The contents of the source operand ((PC) + 1) are not altered.

The subtraction is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: D6

Status Flags: Z, S, P, CY, AC are modified to reflect the results of the subtraction.

Execution States:

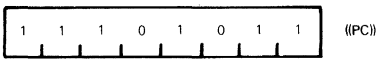
	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		

M1 **NEXT** **INSTRUCTION**	(PC) → AB STATUS → DB	A ← (ACT)-(TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

Exchange H, L With D,E

XCHG

Binary Format



Bytes

1

Clock Periods

4

Operation: (H) ⟷ (D)
(L) ⟷ (E)

Description: The contents of register H are exchanged with the contents of register D, and the contents of register L are exchanged with the contents of register E.

Hexadecimal Format: EB

Status Flags: No status flags are modified.

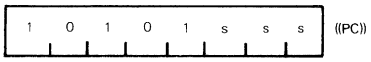
Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	(H) ⟷ (D) (L) ⟷ (E)	

Exclusive OR Source With Accumulator

XRA s

Binary Format



Bytes

1

Clock Periods

4/7

4 if sss ≠ 110
7 if sss = 110

Operations: A ← (A) ⊻ (rs)

Description: The contents of the Accumulator are logically "Exclusive OR"ed with the contents of the designated source location. The result is placed in the Accumulator. When the designated source location is a memory location, the contents of the H and L registers supply the 16-bit address to memory.

The "Exclusive OR" function is not completed until T2 of M1 in the next instruction.

Hexadecimal Formats:

REGISTER	s s s	HEX FORMAT
B	0 0 0	A8
C	0 0 1	A9
D	0 1 0	AA
E	0 1 1	AB
H	1 0 0	AC
L	1 0 1	AD
M	1 1 0	AE
A	1 1 1	AF

Status Flags: Z, S, P are modified to reflect the result of the operation. CY and AC are reset.

Execution States:

SOURCE IS REGISTER (sss ≠ 110)

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	TEMP ← (sss) ACT ← (A)	

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) ⊻ (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

SOURCE IS MEMORY (sss = 110)

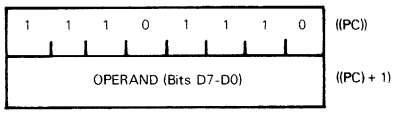
	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		

M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) ⊻ (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES

Exclusive OR With Accumulator Immediate

XRI

Binary Format



Bytes

2

Clock Periods

7

Operation: A ← (A) ⊻ ((PC) + 1)

Description: The contents of the Accumulator are logically "Exclusive OR"ed with the contents of Byte 2 of the instruction ((PC) + 1). The result is placed in the Accumulator.

The Exclusive OR function is not completed until T2 of M1 in the next instruction.

Hexadecimal Format: EE

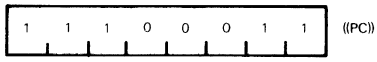
Status Flags: Z, S, P are modified to reflect the result of the operation. CY and AC are reset.

Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	ACT ← (A)	
M2	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	TEMP ← (DB)		
M1 NEXT INSTRUCTION	(PC) → AB STATUS → DB	A ← (ACT) ⊻ (TEMP) ((AB)) → DB PC ← (PC) + 1	NORMAL INSTRUCTION SEQUENCE RESUMES		

Exchange Top Of Stack With H and L — XTHL

Binary Format



Bytes

1

Clock Periods

18

Operation: (L) ⟷ ((SP))
(H) ⟷ ((SP) + 1)

Description: The contents of the L register are exchanged with the contents of the memory location pointed to by the contents of the Stack Pointer. The contents of the H register are exchanged with the contents of the memory location pointed to by the contents of the Stack Pointer incremented by one.

Hexadecimal Format: E3

Status Flags: No status flags are modified.

Execution States:

	T1	T2	T3	T4	T5
M1	(PC) → AB STATUS → DB	((AB)) → DB PC ← (PC) + 1	(DB) → TEMP/IR	INTERNAL FUNCTION	
M2	(SP) → AB STATUS → DB	((AB)) → DB SP ← (SP) + 1	Z ← (DB)		
M3	(SP) → AB STATUS → DB	((AB)) → DB	W ← (DB)		
M4	(SP) → AB STATUS → DB	SP ← (SP)-1 (H) → DB	(AB) ← (DB)		
M5	(SP) → AB STATUS → DB	(L) → DB	(AB) ← (DB)	H,L ← (W,Z)	

Chapter 4
8080A/9080A INSTRUCTION TIMING

This chapter contains functional timing for each instruction, plus full data sheets for Am9080A devices.

The timing diagrams for the instructions show when events occur and are referenced to the clock pulse or other preceeding event that cause them to occur. Minimum and maximum specifications for all timing parameters can be derived from the switching waveform summary and the table of switching characteristics.

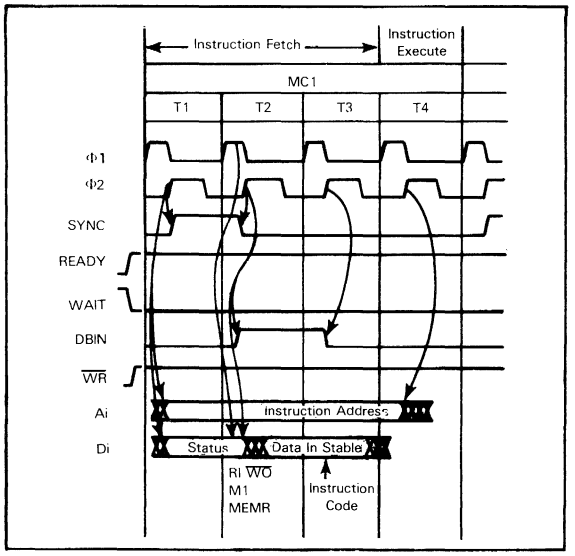


FIGURE 4-1
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: STC, CMC, CMA, NOP, RLC, RRC, RAL, RAR, XCHG, EI, DI, DAA, ADD R, ADC R, SUB R, SBB R, ANA R, XRA R, ORA R, CMP R

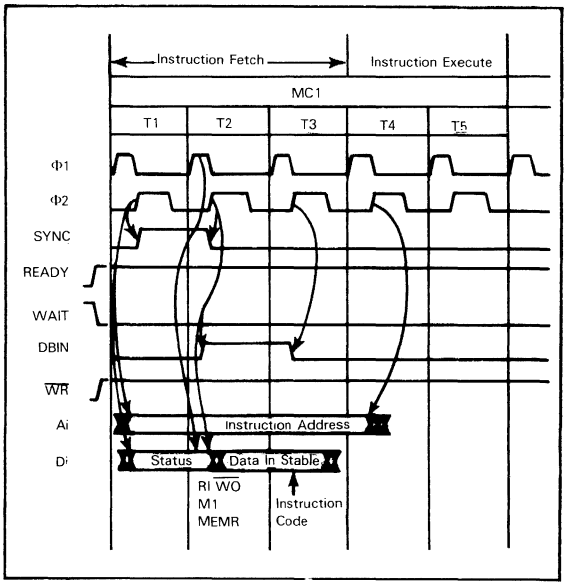


FIGURE 4-2
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: INR, DCR, MOV REG REG, SPHL, PCH, DCX, INX

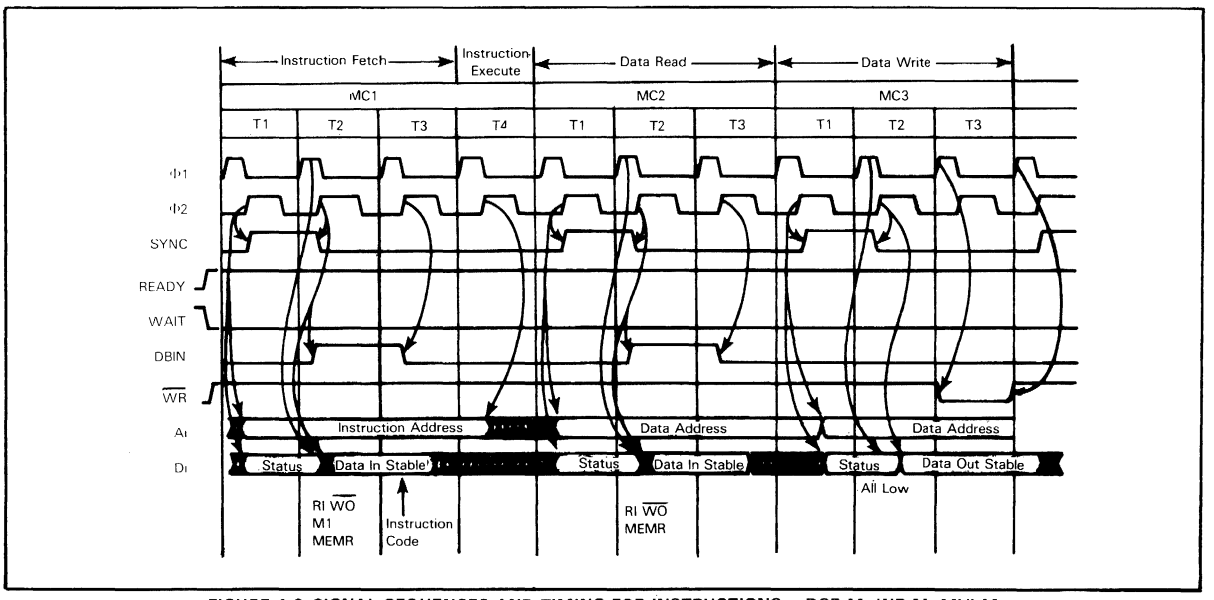


FIGURE 4-3 SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: DCR M, INR M, MVI M

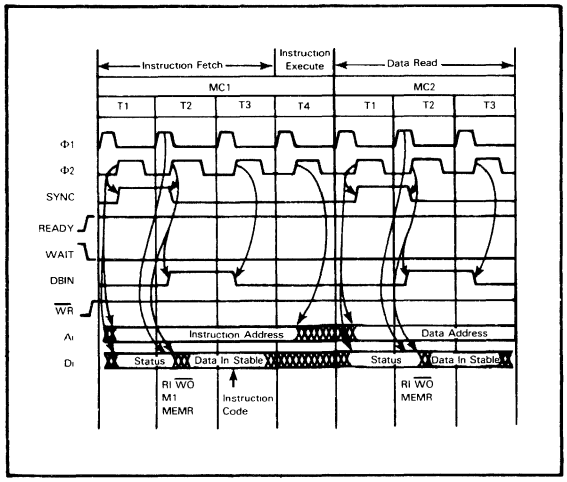


FIGURE 4-4
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: LDAX, MOV REG M, ADI, ACI, SUI, SI, ANI, XRI, ORI, CPI, MVI R, ADD M, ADC M, SUB M, SBB M, ANA M, XRA M, ORA M, CMP M

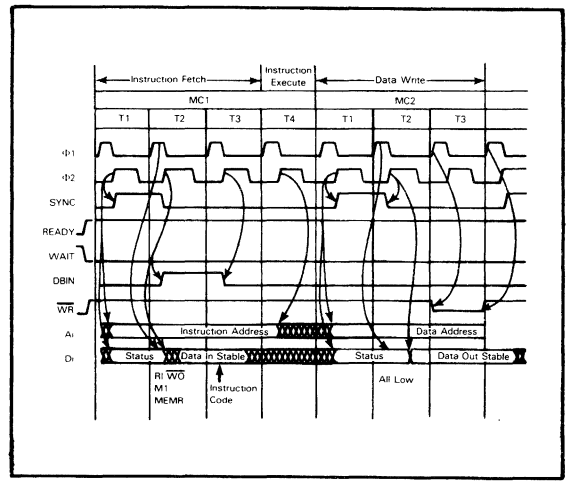


FIGURE 4-5
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: STAX, MOV M REG

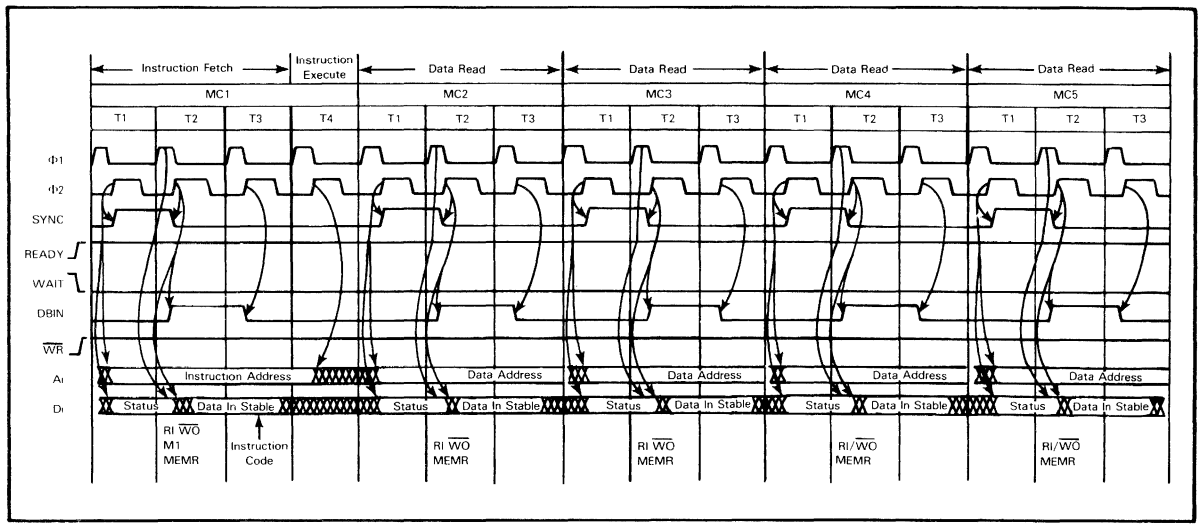


FIGURE 4-6
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: LHLD

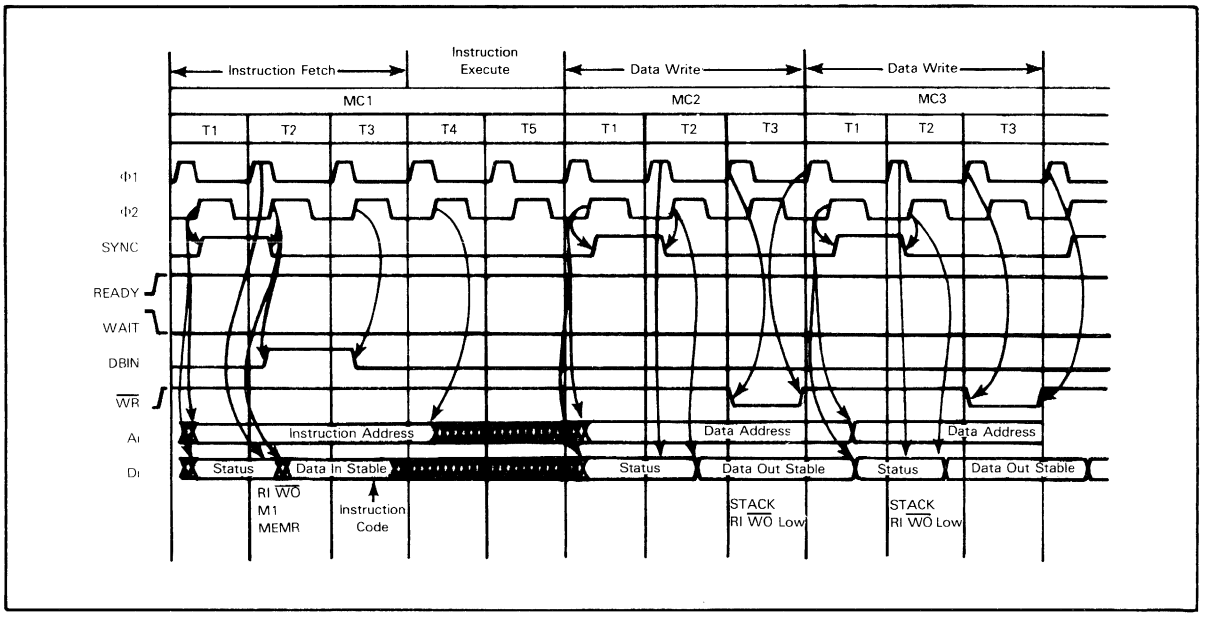


FIGURE 4-7
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
PUSH, RST

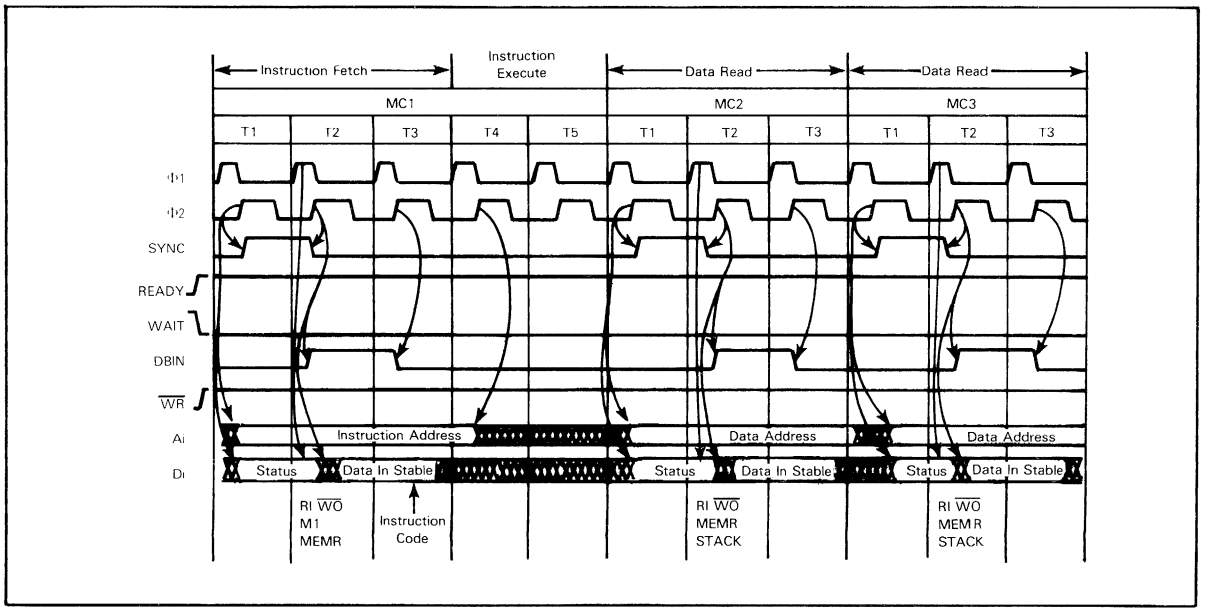


FIGURE 4-8
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
POP, RET

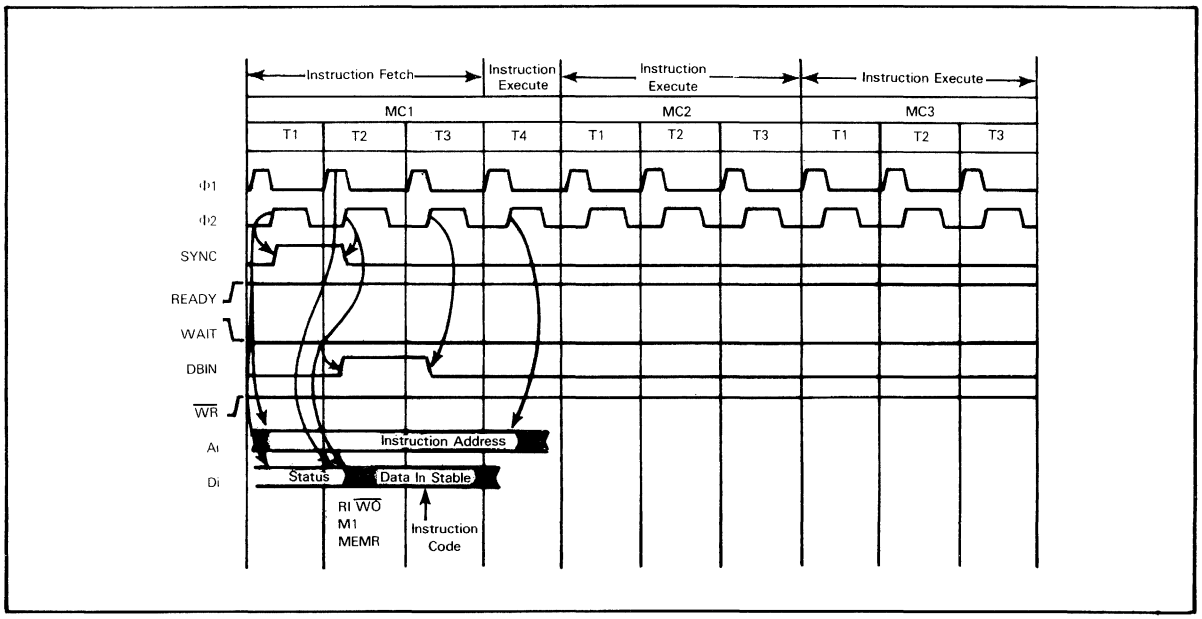


FIGURE 4-9
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
DAD

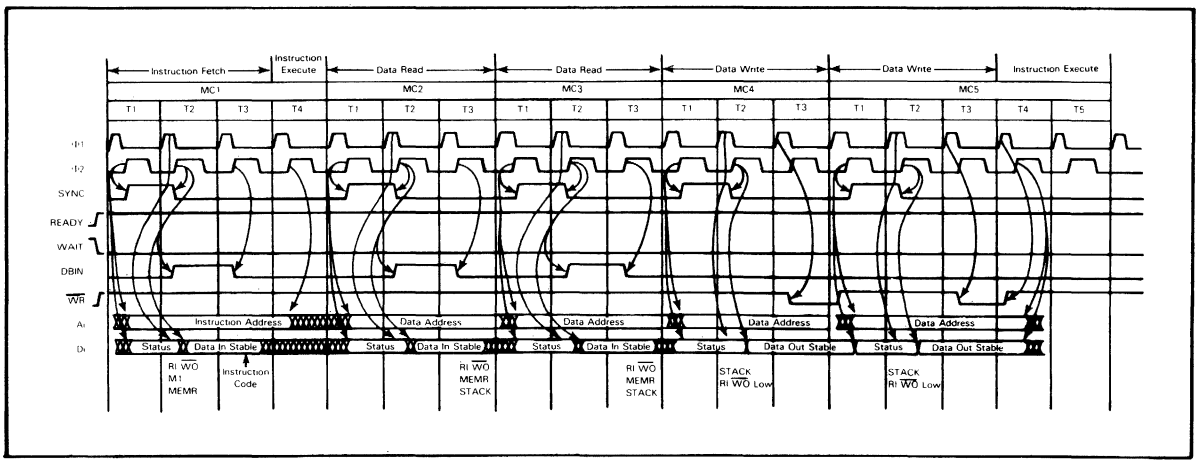


FIGURE 4-10
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
XTHL

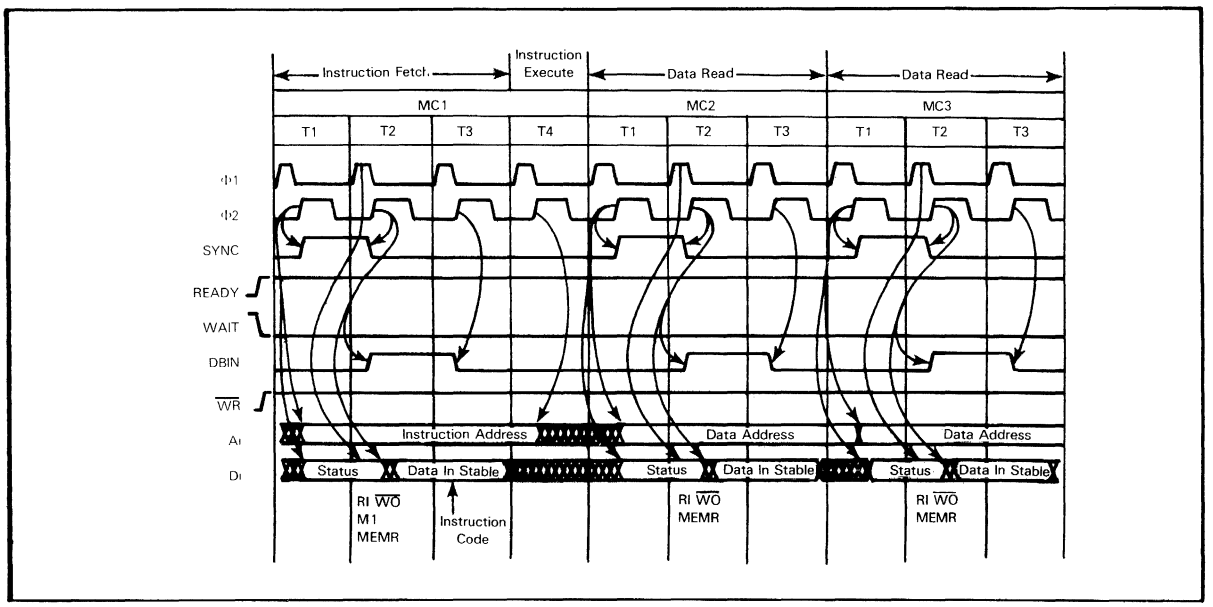


FIGURE 4-11
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
LXI, JMP, JNZ, JZ, JNC, JC, CPO, JPE, JP, JM

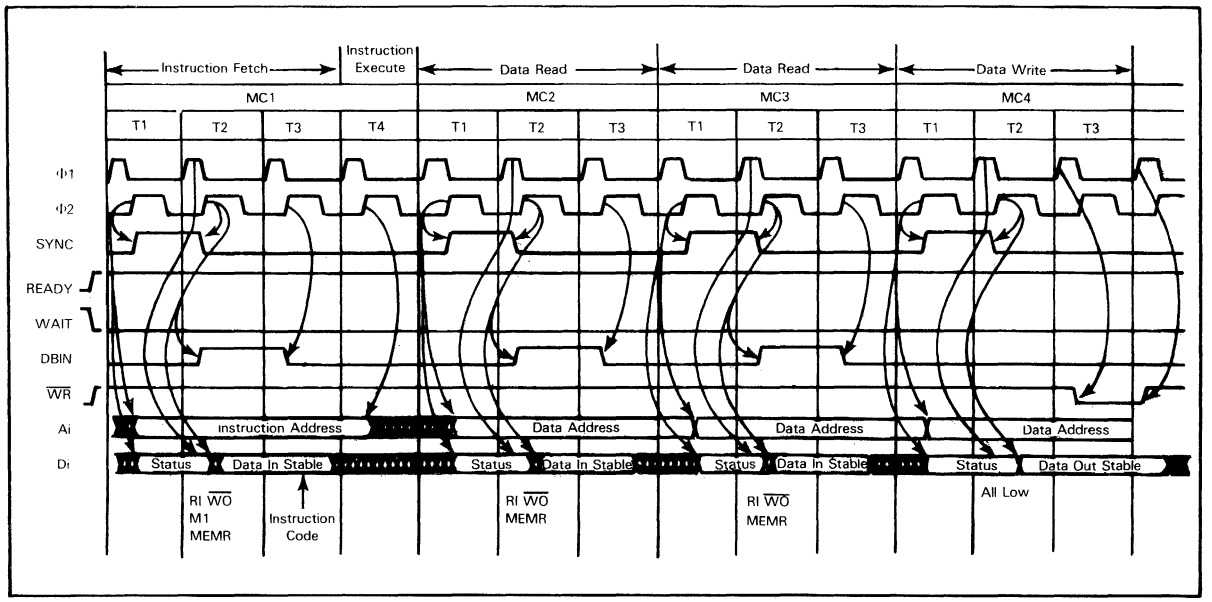


FIGURE 4-12
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
STA

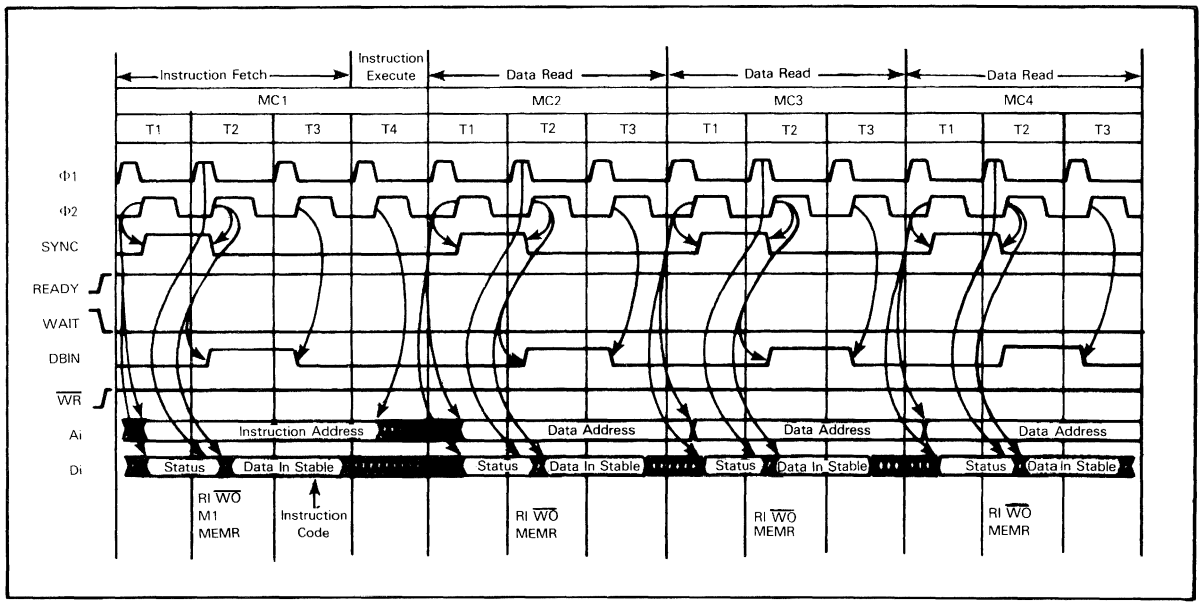


FIGURE 4-13
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: LDA

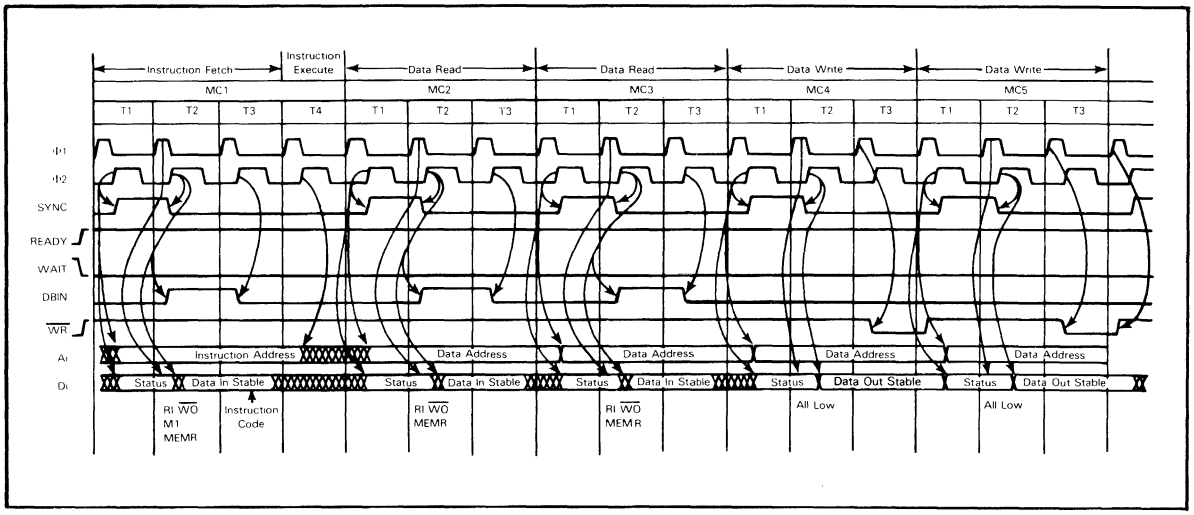


FIGURE 4-14
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: SHLD

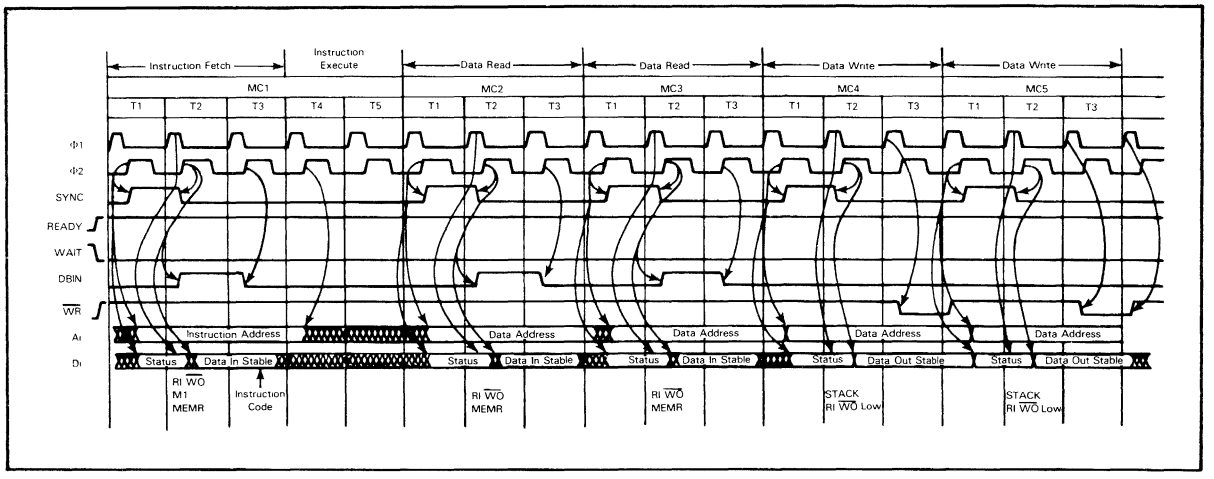


FIGURE 4-15
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
CALL, CNZ, CA, CNC, CC, CPO, CPE, CP, CM

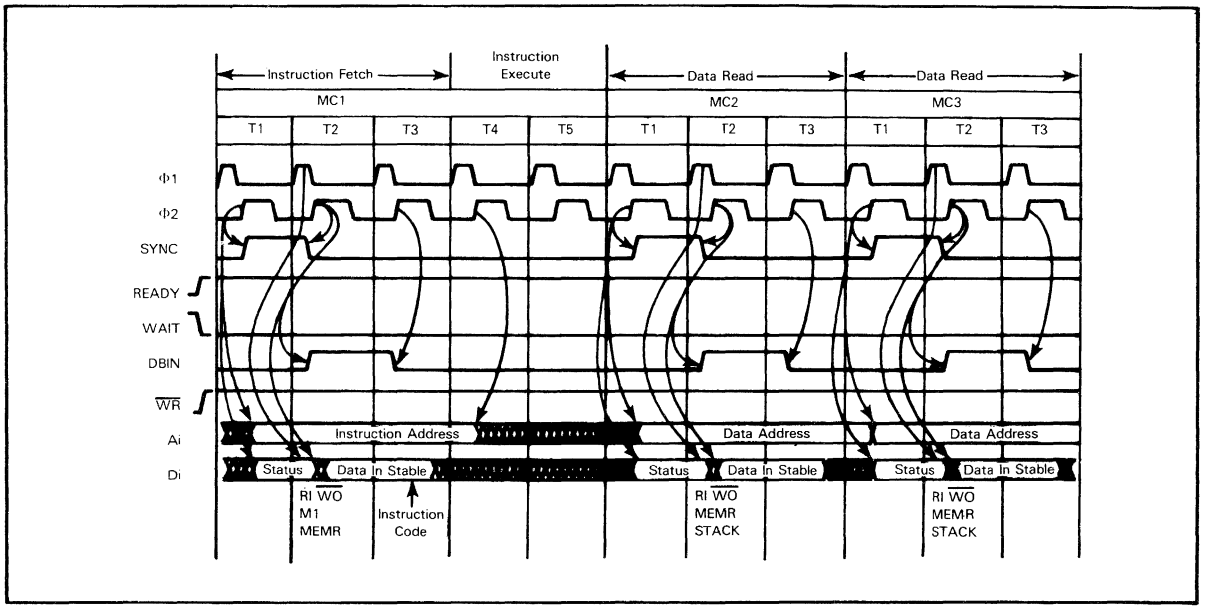


FIGURE 4-16
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
RNZ, RZ, RNC, RPO, RPE, RP, RM

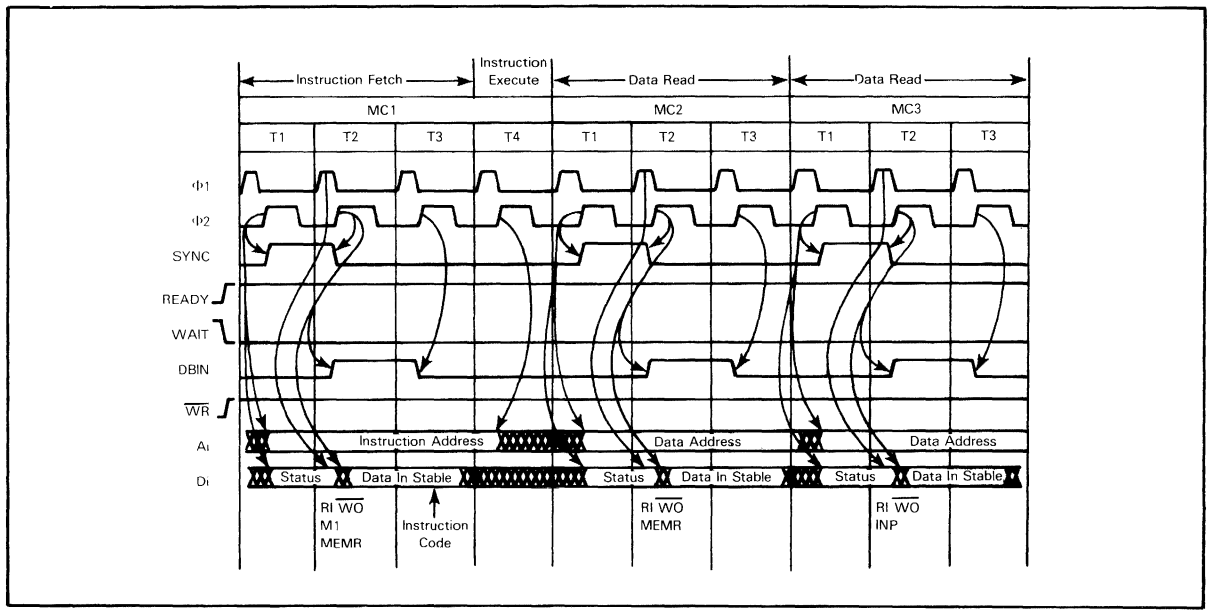


FIGURE 4-17
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
IN

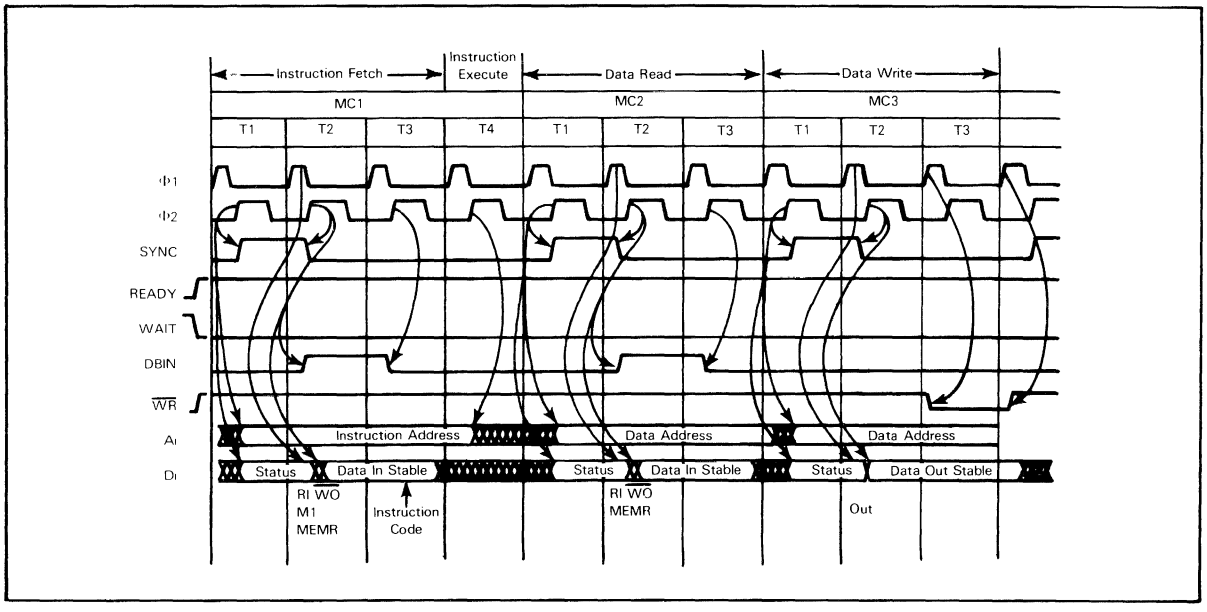


FIGURE 4-18
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS:
OUT

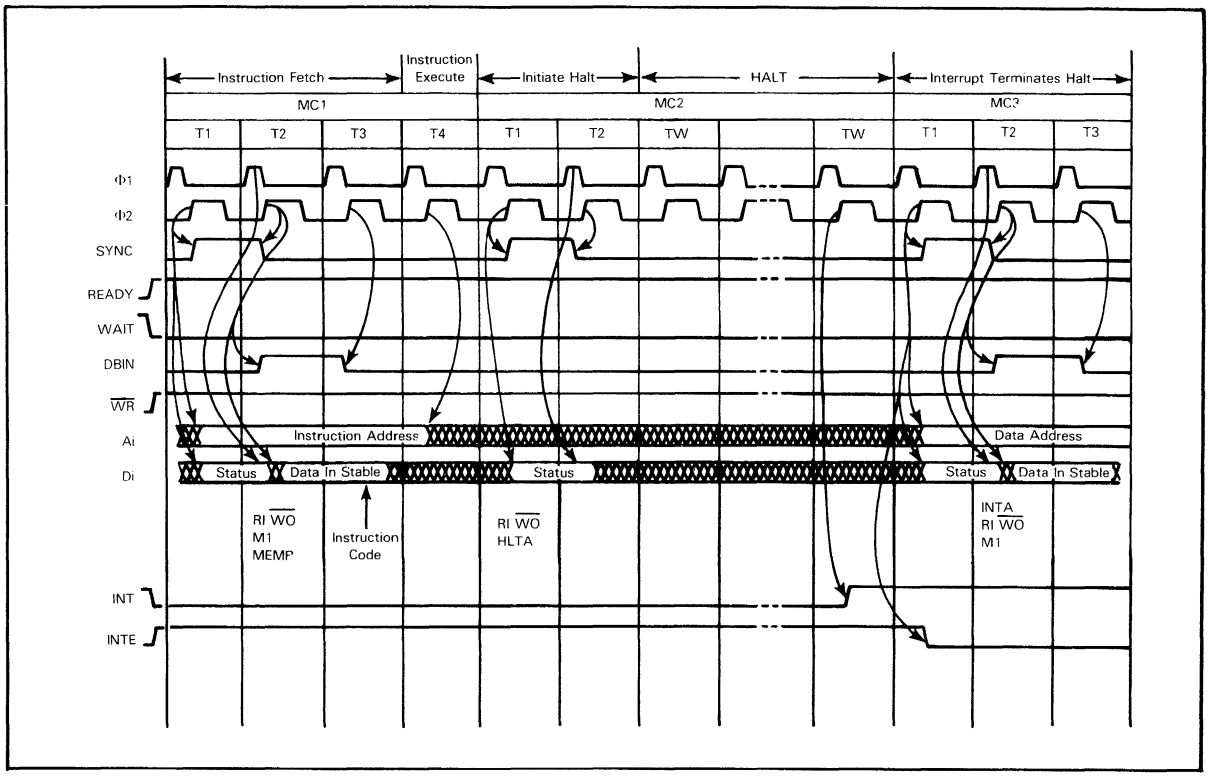


FIGURE 4-19
SIGNAL SEQUENCES AND TIMING FOR INSTRUCTIONS: HLT

Am9080A
8-Bit Microprocessor

Distinctive Characteristics

- Plug-in replacements for 8080A, 8080A-1, 8080A-2
- High-speed version with 1μsec instruction cycle
- Military temperature range operation to 1.5μsec
- Ion-implanted, n-channel, silicon-gate MOS technology
- 3.2mA of output drive at 0.4V (two full TTL loads)
- 700mV of high, 400mV of low level noise immunity
- 820mW maximum power dissipation at ±5% power
- 100% reliability assurance testing to MIL-STD-883

GENERAL DESCRIPTION

The Am9080A products are complete, general-purpose, single-chip digital processors. They are fixed instruction set, parallel, 8-bit units fabricated with Advanced N-Channel Silicon Gate MOS technology. When combined with external memory and peripheral devices, powerful microcomputer systems are formed. The Am9080A may be used to perform a wide variety of operations, ranging from complex arithmetic calculations to character handling to bit control. Several versions are available offering a range of performance options.

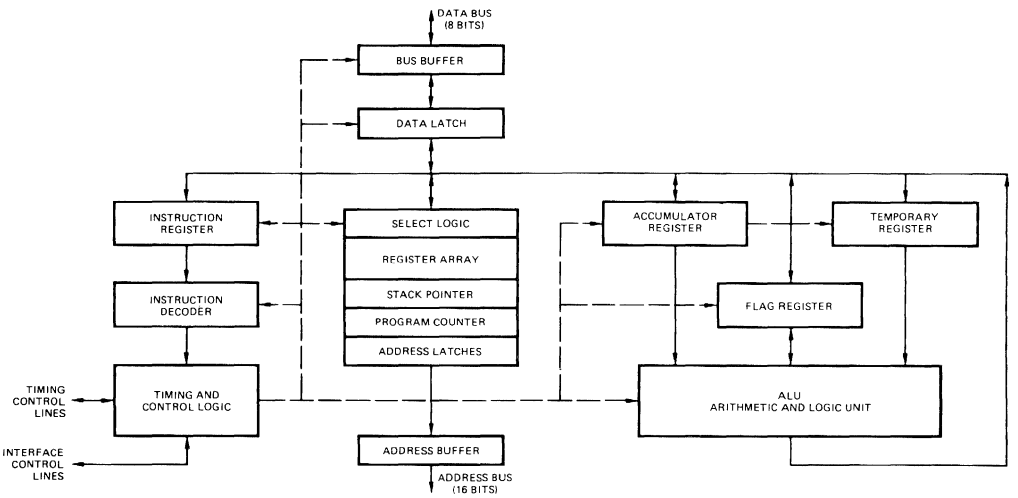
The processor has a 16-bit address bus that may be used to directly address up to 64K bytes of memory. The memory may be any combination of read/write and read-only. Data are transferred into or out of the processor on a bi-directional 8-bit data bus that is separate from the address lines. The data bus transfers instructions, data and status information between system devices. All transfers are handled using asynchronous handshaking controls so that any speed memory or I/O device are easily accommodated.

An accumulator plus six general purpose registers are available to the programmer. The six registers are each 8 bits long and may be used singly or in pairs for both 8 and 16-bit operations. The accumulator forms the primary working register and is the destination for many of the arithmetic and logic operations.

A general purpose push-down stack is an important part of the processor architecture. The contents of the stack reside in R/W memory and the control logic, including a 16-bit stack pointer, is located on the processor chip. Subroutine call and return instructions automatically use the stack to store and retrieve the contents of the program counter. Push and Pop instructions allow direct use of the stack for storing operands, passing parameters and saving the machine state.

An asynchronous vectored interrupt capability is included to allow external signals to modify the instruction stream. The interrupting device may specify an interrupt instruction to be executed and may thus vector the program to a particular service location, or perform some other direct function. Direct memory access (DMA) capability is also included.

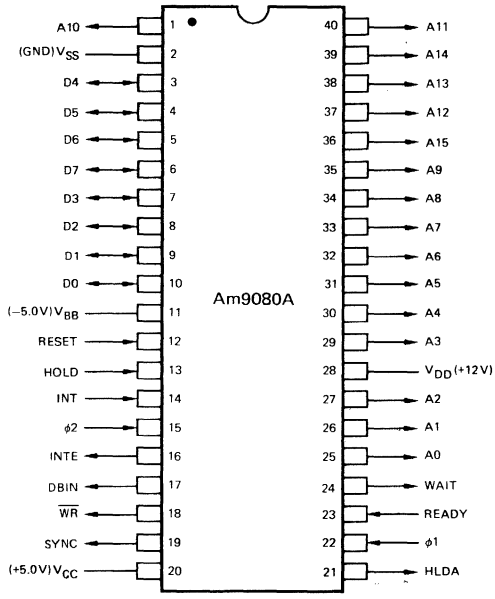
BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Clock Period			
		250 ns	320 ns	380 ns	480 ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	AM9080A-4DC	AM9080A-1DC C8080A-1	AM9080A-2DC C8080A-2	AM9080ADC C8080A
	$-55°C \leq T_A \leq +125°C$			AM9080A-2DM	AM9080ADM
Molded DIP	$0°C \leq T_A \leq +70°C$		AM9080A-1PC	AM9080A-2PC	AM9080APC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

INTERFACE SIGNAL SUMMARY

TYPE	PINS	ABBREVIATION	SIGNAL
INPUT	1	V_{SS}	Ground
INPUT	3	V_{DD}, V_{CC}, V_{BB}	+12V, +5V, −5V Supplies
INPUT	2	$\phi 1$, $\phi 2$	Clocks
INPUT	1	RESET	Reset
INPUT	1	HOLD	Hold
INPUT	1	INT	Interrupt
INPUT	1	READY	Ready
IN/OUT	8	D_0–D_7	Data Bus
OUTPUT	16	A_0–A_{15}	Address
OUTPUT	1	INTE	Interrupt Enable
OUTPUT	1	DBIN	Data Bus In Control
OUTPUT	1	$\overline{WR}$	Write Not
OUTPUT	1	SYNC	Cycle Synchronization
OUTPUT	1	HLDA	Hold Acknowledge
OUTPUT	1	WAIT	Wait

INTERFACE SIGNAL DESCRIPTION

$\phi 1$, $\phi 2$ The Clock inputs provide basic timing generation for all internal operations. They are non-overlapping two phase, high level signals. All other inputs to the processor are TTL compatible.

RESET The Reset input initializes the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop and the hold acknowledge flip-flop. The Reset signal should be active for at least three clock periods. The general registers are not cleared.

HOLD The Hold input allows an external signal to cause the processor to relinquish control over the address lines and the data bus. When Hold goes active, the processor completes its current operation, activates the Hlda output, and puts the 3-state address and data lines into their high-impedance state. The Holding device can then utilize the address and data busses without interference.

READY The Ready input synchronizes the processor with external units. When Ready is absent, indicating the external operation is not complete, the processor will enter the Wait state. It will remain in the Wait state until the clock cycle following the appearance of Ready.

INT The Interrupt input signal provides a mechanism for external devices to modify the instruction flow of the program in progress. Interrupt requests are handled efficiently with the vectored interrupt procedure and the general purpose stack. Interrupt processing is described in more detail on the next page.

D_0-D_7 The Data Bus is comprised of 8 bidirectional signal lines for transferring data, instructions and status information between the processor and all external units.

A_0-A_{15} The Address Bus is comprised of 16 output signal lines used to address memory and peripheral devices.

SYNC The Sync output indicates the start of each processor cycle and the presence of processor status information on the data bus.

DBIN The Data Bus In output signal indicates that the bidirectional data bus is in the input mode and incoming data may be gated onto the Data Bus.

WAIT The Wait output indicates that the processor has entered the Wait state and is prepared to accept a Ready from the current external operation.

$\overline{WR}$ The Write output indicates the validity of output on the data bus during a write operation.

HLDA The Hold Acknowledge output signal is a response to a Hold input. It indicates that processor activity has been suspended and the Address and Data Bus signals will enter their high impedance state.

INTE The Interrupt Enable output signal shows the status of the interrupt enable flip-flop, indicating whether or not the processor will accept interrupts.

INSTRUCTION SET INTRODUCTION

The instructions executed by the Am9080A are variable length and may be one, two or three bytes long. The length is determined by the nature of the operation being performed and the addressing mode being used.

The instruction summary shows the number of successive memory bytes occupied by each instruction, the number of clock cycles required for the execution of the instruction, the binary coding of the first byte of each instruction, the mnemonic coding used by assemblers and a brief description of each operation. Some branch-type instructions have two execution times depending on whether the conditional branch is taken or not. Some fields in the binary code are labeled with alphabetic abbreviations. That shown as **vvv** is the address pointer used in the one-byte Call instruction (RST). Those shown as **ddd** or **sss** designate destination and source register fields that may be filled as follows:

111 A register
000 B register
001 C register
010 D register
011 E register
100 H register
101 L register
110 Memory

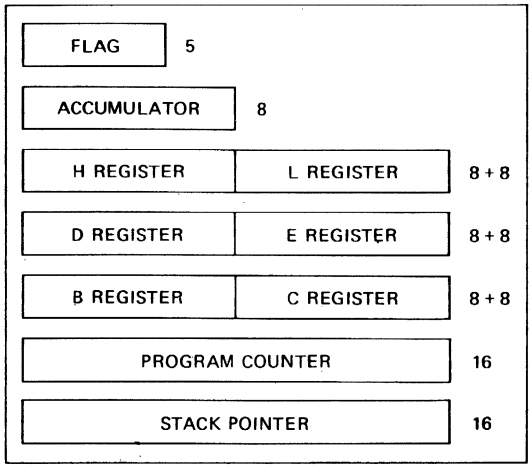
The register diagram shows the internal registers that are directly available to the programmer. The accumulator is the primary working register for the processor and is a specified or implied operand in many instructions. All I/O operations take place via the accumulator. Registers H, L, D, E, B and C may be used singly or in the indicated pairs. The H and L pair is the implied address pointer for many instructions.

The Flag register stores the program status bits used by the conditional branch instructions: carry, zero, sign and parity. The fifth flag bit is the intermediate carry bit. The flags and the accumulator can be stored on or retrieved from the stack with a single instruction. Bit positions in the flag register when pushed onto the stack (PUSH PSW) are:

7	6	5	4	3	2	1	0
S	Z	0	CY1	0	P	1	CY2

where S = sign, Z = zero, CY1 = intermediate carry, P = parity, CY2 = carry.

REGISTER DIAGRAM



During Sync time at the beginning of each instruction cycle the data bus contains operation status information that describes the machine cycle being executed. Positions for the status bits are:

7	6	5	4	3	2	1	0
MEMR	INP	M1	OUT	HLTA	STK	$\overline{WO}$	INTA

STATUS DEFINITION:

INTA Interrupt Acknowledge. Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus when DBIN goes true.

$\overline{WO}$ Write or Output indicated when signal is low. When high, a Read or Input will occur.

STK Stack indicates that the content of the stack pointer is on the address bus.

HLTA Halt Acknowledge.

OUT Output instruction is being executed.

M1 First instruction byte is being fetched.

INP Input instruction is being executed.

MEMR Memory Read operation.

INTERRUPT PROCESSING

When the processor interrupt mechanism is enabled (INTE=1), interrupt signals from external devices will be recognized unless the processor is in the Hold State. In handling an interrupt, the processor will complete the execution of the current instruction, disable further interrupts and respond with INTA status instead of executing the next sequential instruction in the interrupted program.

The interrupting device should supply an instruction opcode to the processor during the next DBIN time after INTA status appears.

Any opcode may be used except XTHL. If the instruction supplied is a single byte instruction, it will be executed. (The usual single byte instruction utilized is RST.) If the interrupt instruction is two or three bytes long, the next one or two processor cycles, as indicated by the DBIN signal, should be used by the external device to supply the succeeding byte(s) of the interrupt instruction. Note that INTA status from the processor is not present during these operations.

If the interrupt instruction is not some form of CALL, it is executed normally by the processor except that the Program Counter is not incremented. The next instruction in the interrupted program is then fetched and executed. Notice that the interrupt mechanism must be re-enabled by the processor before another interrupt can occur.

If the interrupt instruction is some form of CALL, it is executed normally. The Program Counter is stored and control transferred to the interrupt service subroutine. This routine has responsibility for saving and restoring the machine state and for re-enabling interrupts if desired. When the interrupt service is complete, a RETURN instruction will transfer control back to the interrupted program.

INSTRUCTION SET SUMMARY

DATA TRANSFER

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
01dddsss	1	5	MOVr, r	Move register to register
01110sss	1	7	MOVm, r	Move register to memory
01ddd110	1	7	MOVr, m	Move memory to register
00ddd110	2	7	MVI, r	Move to register, immediate
00110110	2	10	MVI, m	Move to memory, immediate
00111010	3	13	LDA	Load Acc, direct
00001010	1	7	LDAX B	Load Acc, indirect via B & C
00011010	1	7	LDAX D	Load Acc, indirect via D & E
00101010	3	16	LHLD	Load H & L, direct
00100001	3	10	LXI H	Load H & L, immediate
00010001	3	10	LXI D	Load D & E, immediate
00000001	3	10	LXI B	Load B & C, immediate
00110001	3	10	LXI SP	Load stack pointer, immediate
00100010	3	16	SHLD	Store H & L, direct
00110010	3	13	STA	Store Acc, direct
00000010	1	7	STAX B	Store Acc, indirect via B & C
00010010	1	7	STAX D	Store Acc, indirect via D & E
11111001	1	5	SPHL	Transfer H & L to stack pointer
11101011	1	4	XCHG	Exchange D & E with H & L
11100011	1	18	XTHL	Exchange top of stack with H & L
11011011	2	10	IN	Input to Acc
11010011	2	10	OUT	Output from Acc

CONTROL

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
01110110	1	7	HLT	Halt and enter wait state
00110111	1	4	STC	Set carry flag
00111111	1	4	CMC	Compliment carry flag
11111011	1	4	EI	Enable interrupts
11110011	1	4	DI	Disable interrupts
00000000	1	4	NOP	No operation

BRANCHING

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
11000011	3	10	JMP	Jump unconditionally
11011010	3	10	JC	Jump on carry
11010010	3	10	JNC	Jump on no carry
11001010	3	10	JZ	Jump on zero
11000010	3	10	JNZ	Jump on not zero
11110010	3	10	JP	Jump on positive
11111010	3	10	JM	Jump on minus
11101010	3	10	JPE	Jump on parity even
11100010	3	10	JPO	Jump on parity odd
11001101	3	17	Call	Call unconditionally
11011100	3	17-11	CC	Call on carry
11010100	3	17-11	CNC	Call on no carry
11001100	3	17-11	CZ	Call on zero
11000100	3	17-11	CNZ	Call on not zero
11110100	3	17-11	CP	Call on positive
11111100	3	17-11	CM	Call on minus
11101100	3	17-11	CPE	Call on parity even
11100100	3	17-11	CPO	Call on parity odd
11001001	1	10	RET	Return unconditionally
11011000	1	11-5	RC	Return on carry
11010000	1	11-5	RNC	Return on no carry
11001000	1	11-5	RZ	Return on zero
11000000	1	11-5	RNZ	Return on not zero
11110000	1	11-5	RP	Return on positive
11111000	1	11-5	RM	Return on minus
11101000	1	11-5	RPE	Return on parity even
11100000	1	11-5	RPO	Return on parity odd
11101001	1	5	PCHL	Jump unconditionally, indirect via H & L
11VVV111	1	11	RST	Restart

ARITHMETIC

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
10000sss	1	4	ADDr	Add register to Acc
10001sss	1	4	ADCr	Add with carry register to Acc
10000110	1	7	ADDm	Add memory to Acc
10001110	1	7	ADCm	Add with carry memory to Acc
11000110	2	7	ADI	Add to Acc, immediate
11001110	2	7	ACI	Add with carry to Acc, immediate
00001001	1	10	DAD B	Double add B & C to H & L
00011001	1	10	DAD D	Double add D & E to H & L
00101001	1	10	DAD H	Double add H & L to H & L
00111001	1	10	DAD SP	Double add stack pointer to H & L
10010sss	1	4	SUBr	Subtract register from Acc
10011sss	1	4	SBBr	Subtract with borrow register from Acc
10010110	1	7	SUBm	Subtract memory from Acc
10011110	1	7	SBBm	Subtract with borrow memory from Acc
11010110	2	7	SUI	Subtract from Acc, immediate
11011110	2	7	SBI	Subtract with borrow from Acc, immediate
00100111	1	4	DAA	Decimal adjust Acc

STACK OPERATIONS

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
11000101	1	11	PUSH B	Push registers B & C on stack
11010101	1	11	PUSH D	Push registers D & E on stack
11100101	1	11	PUSH H	Push registers H & L on stack
11110101	1	11	PUSH PSW	Push Acc and flags on stack
11000001	1	10	POP B	Pop registers B & C off stack
11010001	1	10	POP D	Pop registers D & E off stack
11100001	1	10	POP H	Pop registers H & L off stack
11110001	1	10	POP PSW	Pop Acc and flags off stack

LOGICAL

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
10100sss	1	4	ANA r	And register with Acc
10100110	1	7	ANA m	And memory with Acc
11100110	2	7	ANI	And with Acc, immediate
10101sss	1	4	XRA r	Exclusive or register with Acc
10101110	1	7	XRA m	Exclusive Or memory with Acc
11101110	2	7	XRI	Exclusive Or with Acc, immediate
10110sss	1	4	ORA r	Inclusive Or register with Acc
10110110	1	7	ORA m	Inclusive Or memory with Acc
11110110	2	7	ORI	Inclusive Or with Acc, immediate
10111sss	1	4	CMP r	Compare register with Acc
10111110	1	7	CMP m	Compare memory with Acc
11111110	2	7	CPI	Compare with Acc, immediate
00101111	1	4	CMA	Compliment Acc
00000111	1	4	RLC	Rotate Acc left
00001111	1	4	RRC	Rotate Acc right
00010111	1	4	RAL	Rotate Acc left through carry
00011111	1	4	RAR	Rotate Acc right through carry

INCREMENT/DECREMENT

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
00ddd100	1	5	INR r	Increment register
00110100	1	10	INR m	Increment memory
00000011	1	5	INX B	Increment extended B & C
00010011	1	5	INX D	Increment extended D & E
00100011	1	5	INX H	Increment extended H & L
00110011	1	5	INX SP	Increment stack pointer
00ddd101	1	5	DCR r	Decrement register
00110101	1	10	DCR m	Decrement memory
00001011	1	5	DCX B	Decrement extended B & C
00011011	1	5	DCX D	Decrement extended D & E
00101011	1	5	DCX H	Decrement extended H & L
00111011	1	5	DCX SP	Decrement stack pointer

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
All Signal Voltages With Respect to V_{BB}	−0.3V to +20V
All Supply Voltages With Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	V_{DD}	V_{CC}	V_{BB}	V_{SS}
Am9080A-XDC C8080A-X	0°C to +70°C	+12V ±5%	+5.0V ±5%	−5.0V ±5%	0V
Am9080A-XDM	−55°C to +125°C	+12V ±10%	+5.0V ±10%	−5.0V ±10%	0V

No signal or supply voltage should ever be greater than 0.3V more negative than V_{BB}.

ELECTRICAL CHARACTERISTICS over operating range (note 1)

Parameters	Description	Test Conditions			C8080A-X Min.	C8080A-X Typ.	C8080A-X Max.	Am9080A-XDC Min.	Am9080A-XDC Typ.	Am9080A-XDC Max.	Am9080A-XDM Min.	Am9080A-XDM Typ.	Am9080A-XDM Max.	Units
V_{IL}	Input LOW Voltage				−1.0		0.8	−1.0		0.8	−1.0		0.8	Volts
V_{IH}	Input HIGH Voltage				**3.3**		V_{CC}+1	**3.0**		V_{CC}+1	**3.0**		V_{CC}+1	Volts
V_{ILC}	Input LOW Voltage, Clock				−1.0		0.8	−1.0		0.8	−1.0		0.8	Volts
V_{IHC}	Input HIGH Voltage, Clock				9.0		V_{DD}+1	9.0		V_{DD}+1	V_{DD}−2		V_{DD}+1	Volts
			Am9080A-4					V_{DD}−2		V_{DD}+1				
V_{OL}	Output LOW Voltage	I_{OL} = **3.2mA**								**0.40**			**0.40**	Volts
		I_{OL} = **1.9mA**					**0.45**							Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA						3.7			3.7			Volts
		I_{OH} = −100μA			3.7									
I_{DD}(AV)	V_{DD} Supply Current, Average	Operating, Minimum Clock Period	Am9080A Am9080A-2 Am9080A-1	T_A = +25°C		40			30	45		30	50	mA
				T_A = 0°C			**70**		35	**50**		35	**55**	
				T_A = −55°C								45	70	
			Am9080A-4	T_A = +25°C					45	60				
				T_A = 0°C					55	70				
I_{CC}(AV)	V_{CC} Supply Current, Average	Operating, Minimum Clock Period	Am9080A Am9080A-2 Am9080A-1	T_A = +25°C		60			25	30		15	35	mA
				T_A = 0°C			**80**		20	**35**		20	**40**	
				T_A = −55°C								25	50	
			Am9080A-4	T_A = +25°C					35	50				
				T_A = 0°C					40	60				
I_{BB}(AV)	V_{BB} Supply Current, Average	Operating, Minimum Clock Period					1.0			1.0			1.0	mA
I_{IL}	Input Leakage Current	(Note 4)					±10			±10			±10	μA
I_{CL}	Clock Leakage Current	$V_{SS} \leq V_\phi \leq V_{DD}$					±10			±10			±10	μA
I_{DL}	Data Bus Current, Input Mode (Note 2)	$V_{IN} \leq V_{SS}$ + 0.8V					−100			−100			−100	μA
		$V_{IN} \geq V_{SS}$ + 0.8V					−2.0			−2.0			−2.0	mA
I_{FL}	Address and Data Bus Leakage in OFF State	$V_{A/D} = V_{CC}$					10			10			10	μA
		$V_{A/D} = V_{SS}$					−100			−100			−100	μA

CAPACITANCE

f = 1.0MHz, Inputs = 0V, T_A = 25°C

$V_{DD} = V_{CC} = V_{SS}$ = 0V, V_{BB} = −5.0V

Parameters	Description	Typ.	Max.	Units
C_ϕ	Clock Input Capacitance	12	20	pF
C_I	Input Capacitance	4.0	8.0	pF
C_O	Output Capacitance	8.0	15	pF
$C_{I/O}$	I/O Capacitance	10	18	pF

SWITCHING CHARACTERISTICS over operating range

Boldface numbers are 8080A specs which are exceeded.

Parameters	Description	Test Conditions	Am9080A-4 Min.	Am9080A-4 Max.	Am9080A-1 / C8080A-1 Min.	Am9080A-1 / C8080A-1 Max.	Am9080A-2 / C8080A-2 Min.	Am9080A-2 / C8080A-2 Max.	Am9080A / C8080A Min.	Am9080A / C8080A Max.	Unit
t_{DA}	Clock $\phi 2$ to Address Out Delay	Load Capacitance = 100pF		**125**		150		175		200	ns
t_{DD}	Clock $\phi 2$ to Data Out Delay			**140**		180		200		220	ns
t_{DI}	Clock $\phi 2$ to Data Bus Input Mode Delay	(Note 5)		**t_{DF}**		t_{DF}		t_{DF}		t_{DF}	ns
t_{DS1}	Data In to Clock $\phi 1$ Set-up Time	Both t_{DS1} and t_{DS2} must be satisfied	**10**		10		20		30		ns
t_{DS2}	Data In to Clock $\phi 2$ Set-up Time		**110**		120		130		150		ns
t_{DC}	Clock to Control Output Delay	Load Capacitance = 50pF		**100**		110		120		120	ns
t_{RS}	Ready to Clock $\phi 2$ Set-up Time		**80**		90		90		120		ns
t_H	Clock $\phi 2$ to Control Signal Hold Time		**0**		0		0		0		ns
t_{IS}	Interrupt to Clock $\phi 2$ Set-up Time		**90**		100		100		120		ns
t_{HS}	Hold to Clock $\phi 2$ Set-up Time		**100**		120		120		140		ns
t_{IE}	Clock $\phi 2$ to INTE Delay	Load Capacitance = 50pF		**100**		200		200		200	ns
t_{FD}	Clock $\phi 2$ to Address/Data OFF Delay		**100**			120		120		120	ns
t_{DF}	Clock $\phi 2$ to DBIN Delay	Load Capacitance = 50pF	**25**	**110**	25	130	25	140	25	140	ns
t_{DH}	Clock $\phi 2$ to Data In Hold Time	(Note 5)	–	–	–	–	–	–	–	–	ns
t_{AW}	Address Valid to Write Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{DW}	Output Data Valid to Wtite Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{KA}	Address Valid to Write Increment	(Note 8)		**90**		110		130		140	ns
t_{KD}	Output Data Valid to Write Increment	(Note 8)		**130**		150		170		170	ns
t_{WA}	Write to Address Invalid Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{WD}	Write to Output Data Invalid Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{HF}	HLDA to Address/Data OFF Delay	(Note 9)	–	–	–	–	–	–	–	–	ns
t_{WF}	Write to Address/Data OFF Delay	(Note 9)	–	–	–	–	–	–	–	–	ns
t_{KH}	HLDA to Address/Data OFF Increment	(Note 9)		**40**		50		50		50	ns
t_{AH}	DBIN to Address Hold Time		**0**		–20		–20		–20		ns

Notes: 1. Typical values are at $T_A = 25^\circ C$, nominal supply voltages and nominal processing parameters.

2. Pull-up devices are connected to the Data Bus lines when the input signal is high during DBIN time. When switching the input from HIGH-to-LO a transient current must be absorbed by the driving device until the input reaches a LOW level.

3. Timing reference levels –
   Clocks: HIGH = 8.0V, LOW = 1.0V
   Inputs: HIGH = 3.3V, LOW = 0.8V
   Outputs: HIGH = 2.0V, LOW = 0.8V

4. Control inputs impress currents on the driving signal during HIGH-to-LOW transitions. Values shown are for logic high or logic low levels. Pea current during transition is as much as 1.0mA.

5. Bus contention cannot occur and data hold times are adequate when DBIN is used to enable Data In. t_{DH} is the smaller of 50ns or t_{DF}.

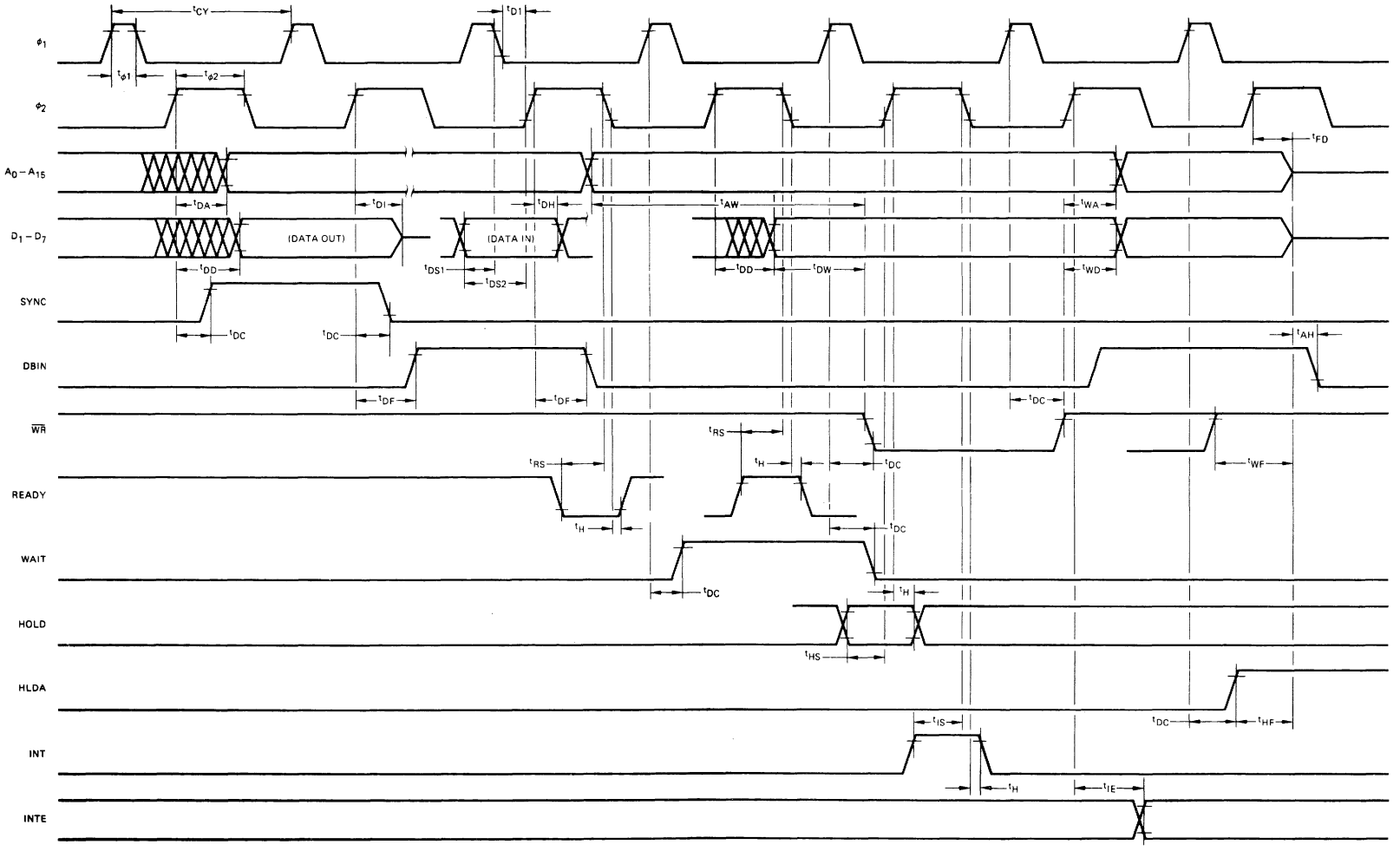
6. RESET should remain active for at least three clock periods.

7. With interrupts enabled, the interrupted instruction will be one with an interrupt input stable during the indicated interval of the last clock peric of the preceeding instruction. Additional synchronization not necessary.

8. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi 2} - t_{KA}$
   $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - t_{KD}$
   For HLDA Off: $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10ns$
   For HLDA On: $t_{WD} = t_{WA} = t_{WF}$

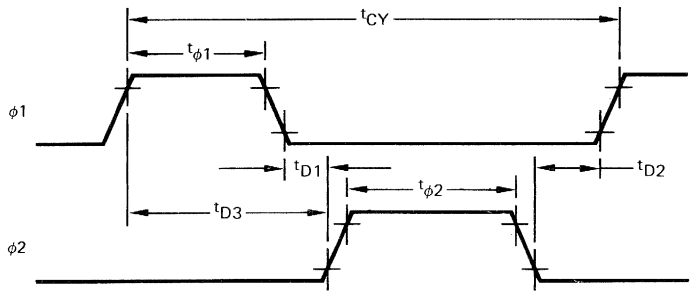
9. $t_{HF} = t_{D3} + t_{r\phi 2} - t_{KH}$
   $t_{WF} = t_{D3} + t_{r\phi 2} - 10ns$

SWITCHING WAVEFORMS SUMMARY



This chart presents relative timing waveform relationships and does not show actual processor operating cycles.

CLOCK WAVEFORM DETAIL

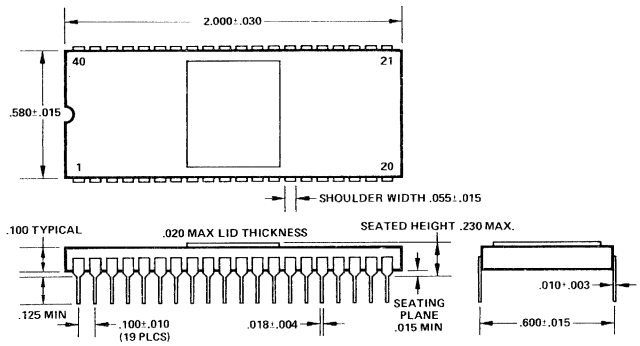


$$t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1}$$

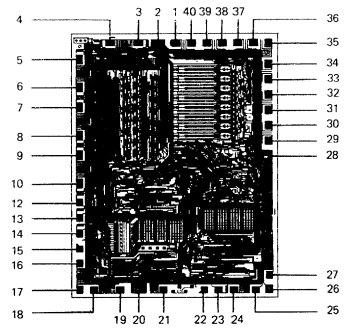
CLOCK SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Am9080A-4 Min.	Am9080A-4 Max.	Am9080A-1 C8080A-1 Min.	Am9080A-1 C8080A-1 Max.	Am9080A-2 C8080A-2 Min.	Am9080A-2 C8080A-2 Max.	Am9080A C8080A Min.	Am9080A C8080A Max.	Units
t_{CY}	Clock Period	**250**	**2000**	320	2000	380	2000	480	2000	ns
t_r, t_f	Clock Transition Times	**0**	**15**	0	25	0	50	0	50	ns
$t_{\phi 1}$	Clock $\phi 1$ Pulse Width	**50**		50		60		60		ns
$t_{\phi 2}$	Clock $\phi 2$ Pulse Width	**120**		145		175		220		ns
t_{D1}	$\phi 1$ to $\phi 2$ Offset	**0**		0		0		0		ns
t_{D2}	$\phi 2$ to $\phi 1$ Offset	**50**		60		70		70		ns
t_{D3}	$\phi 1$ to $\phi 2$ Delay	**50**		60		70		80		ns

PHYSICAL DIMENSIONS
40-Pin Hermetic DIP



Metallization and Pad Layout



Pin 11 connection is substrate

DIE SIZE 0.131" X 0.169"

Chapter 5
Am8224 and Am8228/8238

Am8224 CLOCK GENERATOR

The Am8224 is a single integrated circuit designed to provide the clock signals required to operate 8080A/9080A microprocessor systems. Additional circuits are included in the Am8224 to synchronize externally generated Reset and Ready signals with the timing of the CPU.

The block diagram for the Am8224 is shown in Figure 5-1.

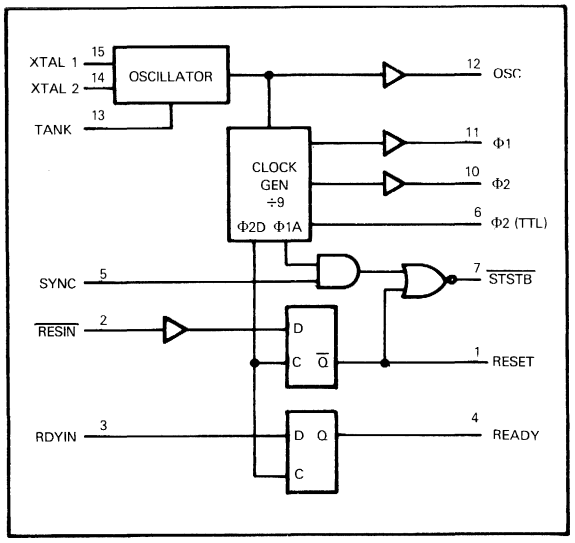


FIGURE 5-1 Am8224 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The oscillator provides a basic operating frequency which is nine times greater than the operating frequency of the microprocessor. The clock generator consists of a divide-by-nine counter that operates from the oscillator output and generates the Φ1 and Φ2 clock pulses required by the microprocessor. Additional circuits generate the synchronized Reset and Ready control inputs required by the 8080A/9080A and a signal, STSTB, which can be used to latch the machine status.

Am8224 INTERFACE SIGNALS

Figure 5-2 shows the connection diagram for the Am8224.

Power

+5V, +12V, Ground

These input connections supply power to the circuit.

Inputs

Reset Input (RESIN, Input)
RESIN is the microprocessor reset input signal. RESIN may be developed from any source circuit that supplies the required input signal levels. There is no constraint on the input signal rise or fall time since a Schmitt trigger internal to the Am8224 reshapes the RESIN signal and synchronizes the signal with Φ2; this ensures that the system reset will occur within the timing requirements of the 8080A/9080A.

Ready Input (RDYIN, Input)
RDYIN is connected to the source of the microcomputer Ready signal. It is synchronized with Φ2 in the Am8224 to meet the Ready signal timing requirements of the 8080A/9080A.

Synchronization (SYNC, Input)
SYNC is an input connected to the SYNC output from the microprocessor. It is gated with Φ1 to generate a strobe pulse (STSTB) for reading the machine cycle status bits from the Data Bus during T1 in every machine cycle.

XTAL 1 And XTAL 2 (Inputs)
These signals are input connections used for connecting the crystal which sets the Am8224 oscillator frequency.

Tank (Input)
Tank is connected to a parallel resonant circuit tuned to the desired operating frequency of the oscillator when operating in overtone mode.

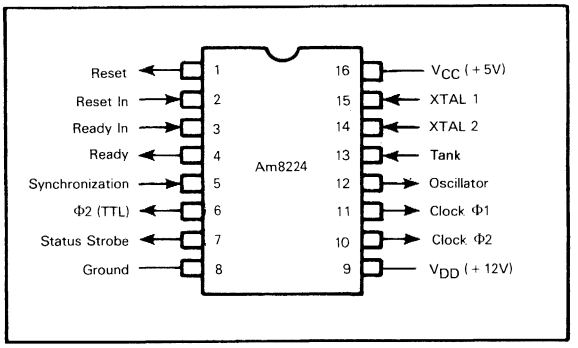


FIGURE 5-2 Am8224 CONNECTION DIAGRAM

Outputs

Reset Output (RESET, Output)
Reset is the system reset pulse supplied to the 8080A/9080A microprocessor and other circuits in the microcomputer that require a reset signal. Reset conforms to all timing and amplitude requirements of the 8080A/9080A.

Ready Output (READY, Output)
Ready is connected to the microprocessor Ready input connection. When high, Ready allows the 8080A/9080A to execute machine cycles normally. When low, it causes Wait states to be inserted between T2 and T3 in the CPU machine cycle.

Status Strobe ($\overline{STSTB}$, Output)
$\overline{STSTB}$ is the status strobe signal used to read the CPU machine cycle status from the Data Bus during T2. It is the "AND" of Φ1 and SYNC.

Clock Φ1 and Clock Φ2 (Outputs)
These are the two clock signals required by the CPU. Output buffers provide the high level signals required by the 8080A/9080A.

Oscillator (OSC, Output)
OSC is the oscillator output reference signal.

Clock Φ2 TTL (Output)
This signal is a TTL compatible Φ2 clock pulse used for timing by circuits other than the microcomputer.

OPERATION OF THE OSCILLATOR

The oscillator generates a basic operating frequency from which the microprocessor clocks are generated. A crystal connected between XTAL 1 and XTAL 2 sets an accurate operating frequency for the oscillator. A capacitor in the range of 20 pf to 25 pf connected in series with the crystal may be required to maintain proper operation. This is larger than the 3 pf to 10 pf recommended for other manufacturers' versions of the 8224 due to the higher maximum operating frequency of the Am8224.

SELECTING THE CLOCK FREQUENCY AND THE CRYSTAL

There are three decisions to be made in incorporating the Am8224 in an 8080A/9080A system. These are:

- Select the clock period
- Select the crystal
- Select the values of the inductive and capacitive components for the parallel resonant circuit if required

The clock period for the CPU is limited by the minimum and maximum specification for the clock period, tCY; and is dependent on which of the CPU circuits is to be used. The 8080A is limited to clock periods longer than 480 nsec but less than 2000 nsec, while the Am9080A-4 can operate with a clock period of 250 nsec. The frequency of Φ1 is determined from the clock period as:

$$\frac{1}{tCY\ max} \leqslant F\,\Phi1 \leqslant \frac{1}{tCY\ min}$$

The Am8224 is designed to operate with series resonant crystals. The frequency may be specified as the fundamental frequency of the crystal or as an overtone (harmonic).

When selecting a frequency less than 25 MHz, the crystal may be specified to operate at the fundamental mode of oscillation. However, at frequencies above 25 MHz, it is necessary to use a crystal which is manufactured with a fundamental frequency which is less than that desired. The crystal is then operated at an overtone of the fundamental. The crystal must be specified for operation at the overtone at the time of manufacture to ensure that it will provide maximum energy of oscillation at the desired overtone. The most popular overtone is the third harmonic of the fundamental frequency. A parallel resonant (Tank) circuit is employed to increase the oscillator circuit gain at the desired frequency. This circuit is connected to the Tank input of the Am8224.

EXAMPLE: Assume that an Am9080A-4 system is to operate with a clock period of 250 nsec.

Then: $$F\Phi1 = \frac{1}{tCY} = \frac{1}{250 \times 10^{-9}\ sec} = 4\ MHz$$

Since the Am8224 oscillator operates at 9x the desired frequency, 36 MHz is required.

A 12 MHz crystal may be selected and operated at the third overtone. A parallel resonant circuit is required with a center frequency of 36 MHz for connection to the Tank input.

The parallel resonant circuit is shown in Figure 5-3.

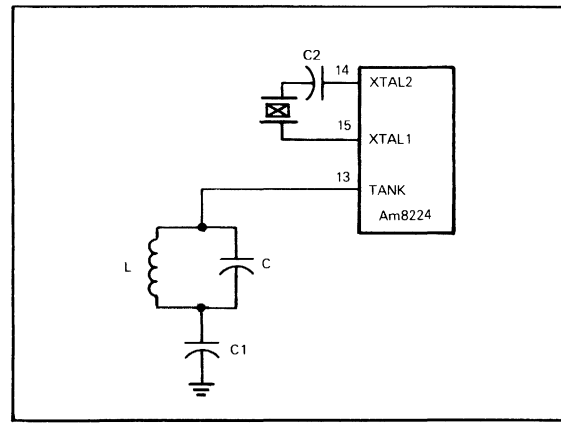


FIGURE 5-3 SCHEMATIC OF PARALLEL RESONANT CIRCUIT

L and C form the resonant circuit. Capacitor C1 is a decoupling capacitor that blocks DC current from flowing through the Tank input. A 1 μf capacitor is adequate for decoupling at the frequencies at which all of the Am9080A microprocessors operate.

The frequency of the parallel resonant circuit at resonance is:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

After the Φ1 clock period has been selected, the values of L and C can be calculated from the above relationship as follows:

$$\frac{tCY}{9} = \frac{1}{f} = 2\pi\sqrt{LC}$$

Therefore:

$$LC = \left(\frac{tCY}{2\pi X\,9}\right)^2$$

Using the previous example, tCY was selected at 250 nsec.

Then:

$$LC = \left(\frac{250}{18\pi} \times 10^{-9}\right)^2 \simeq 1.9 \times 10^{-17}$$

if L is selected as 3.9 μH, then C $\simeq$ 5 pf.

Figure 5-4 shows parallel resonant circuits that may be used with the Am8224 for Am9080A-1 and Am9080A-4 microprocessors operating at their minimum tCY.

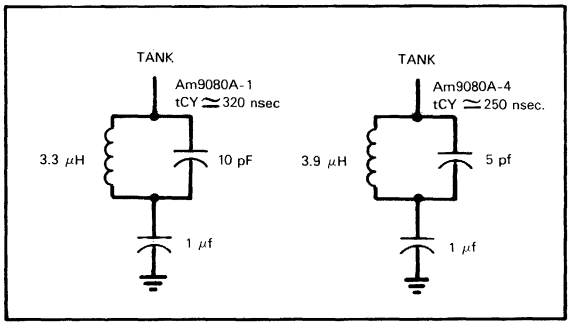


FIGURE 5-4 PARALLEL RESONANT CIRCUITS FOR USE IN Am9080A-1 AND Am9080A-4 MICROCOMPUTERS

The maximum oscillator and crystal frequencies for each of the Am9080A microprocessors is shown in Table 5-1.

TABLE 5-1 MICROPROCESSOR OSCILLATORY AND CRYSTAL FREQUENCIES

UNIT	MIN tCY NSEC	MAX Am8224 OSC FREQ	CRYSTAL FREQUENCY
Am9080A	480	18.75 MHz	18.75 MHz
Am9080A-2	380	23.684 MHz	23.684 MHz
Am9080A-1	320	28.125 MHz	9.372 MHz
Am9080A-4	250	36 MHz *	12 MHz

*Am8224-4

CLOCK GENERATOR

The clock waveform generator receives the oscillator output and produces the two basic microprocessor clock signals Φ1 and Φ2. The clock generator consists of a divide-by-nine counter operating at the oscillator frequency to produce two non-overlapping clock pulses at 1/9th of the oscillation frequency. Figure 5-5 shows how the Φ1 and Φ2 clock pulses are generated.

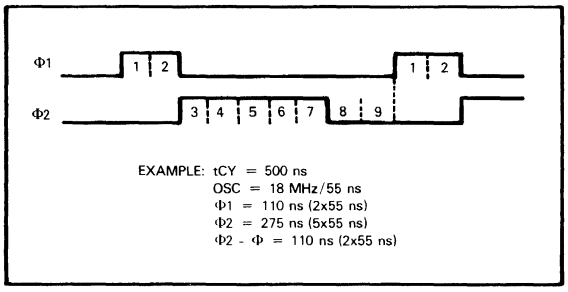


FIGURE 5-5 GENERATION OF Φ1 AND Φ2

The clock waveforms are buffered to provide the high level clock signals required by the 8080A/9080A CPU. A separate TTL compatible Φ2 is provided to be used by other microcomputer components.

READY, RESET AND $\overline{\text{STSTB}}$ LOGIC

Logic is included in the Am8224 to synchronize a system reset and ready line with Φ2 to meet the requirements of the 8080A/9080A.

The Am8224 generates a strobe pulse ($\overline{\text{STSTB}}$) to sample machine cycle status codes. $\overline{\text{STSTB}}$ is the "AND" function of SYNC generated by the CPU and Φ1. Reset is "OR"ed with the output of the "AND" gate to cause $\overline{\text{STSTB}}$ to remain low when Reset is active.

Am8228/8238 SYSTEM CONTROLLER

The Am8228 and Am8238 System Controllers are single integrated circuits that demultiplex control signals, and buffer the Data Bus. Control signals generated operate memory and peripheral circuits.

The Am8228 generates the $\overline{\text{I/OW}}$ and $\overline{\text{MEMW}}$ control signals from the $\overline{\text{WR}}$ signal generated by the CPU. The Am8238 generates these control signals immediately after the status bits are latched in the Am8238. Thus, the appropriate control signals to initiate a write function in external circuits are generated earlier by the Am8238; this allows sufficient time to execute a write in large memory systems, or for high speed systems such as those using the Am9080A-4 microprocessor.

In summary, the two principal functions of the Am8228/8238 are:

- Provide control signals with correct timing to read from or write to memory, to sample I/O ports, and to acknowledge the receipt of an interrupt request.
- Buffer the bidirectional Data Bus to the memory and I/O circuits.

The functional block diagram is shown in Figure 5-6.

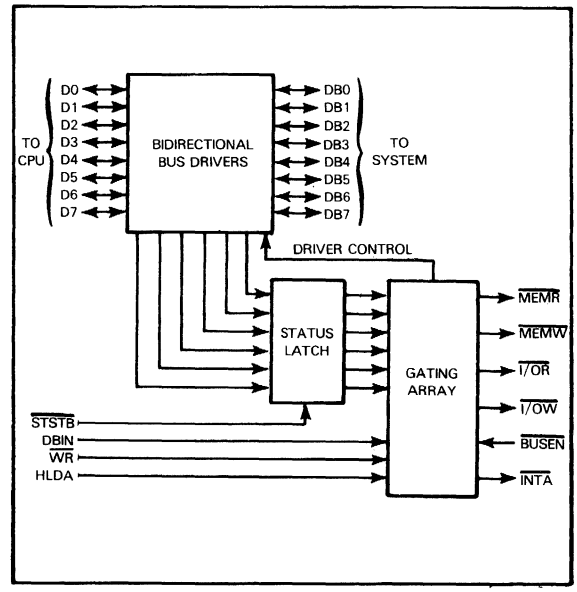


FIGURE 5-6 Am8228/8238 BLOCK DIAGRAM

SELECTING THE CORRECT SYSTEM CONTROLLER

The Am9080A-1 and the Am9080A-4 microprocessors are high speed devices which, in the worst case, should not be connected to normal System Controller devices; the Am8238-4 high speed System Controller should be used with these two high speed microprocessors.

There are no other restrictions placed on microprocessor-System Controller combinations.

FUNCTIONAL DESCRIPTION

Refer to Figure 5-6.

The bidirectional bus drivers isolate the system Data Bus from the microprocessor and provide internal control to ensure that the data path is enabled in the direction appropriate to the function being performed. For example, when DBIN is high, a memory read function is being performed and the bidirectional bus drivers will transmit from the System Data Bus to the CPU Data Bus.

The Status Latches sample the status bits appearing on the Am9080A Data Bus during the T1 clock period of each machine cycle. All status bits remain latched for the duration of the machine cycle; status bits are used by the Gating Array, which generates control signals required by the rest of the microcomputer system. The $\overline{STSTB}$ signal generated by the Am8224 can be used to latch status information.

Am8228/8238 INTERFACE SIGNALS

Figure 5-7 shows the Am8228/8238 connection diagram.

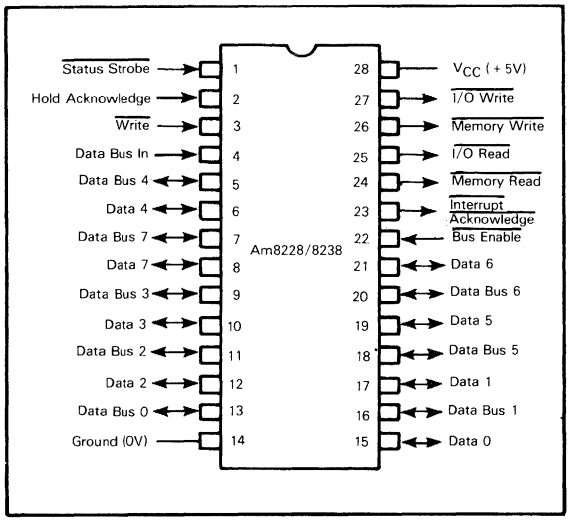


FIGURE 5-7 Am8228/8238 CONNECTION DIAGRAM

Power

V_{CC}, Ground

V_{CC} and GND are the +5V and 0V power inputs respectively.

Inputs

Data Bus In (DBIN, Input)

DBIN is a control signal from the CPU used to activate the output drivers of the Am8228/8238 to the CPU Data Bus when a read function is performed from memory or I/O.

Hold Acknowledge (HLDA, Input)

HLDA acknowledges that the CPU has entered the Hold state. it causes the System Data Bus and control outputs to switch to the high impedance state.

Control Bus signals $\overline{I/OR}$, $\overline{INTA}$, and $\overline{MEMR}$ will be forced high for the duration in which HLDA is high.

Write ($\overline{WR}$, Input)

$\overline{WR}$ is the write pulse from the CPU. When $\overline{WR}$ is low, the bidirectional bus drivers in the Am8228/8238 are conditioned to transmit data from the CPU Data Bus to the System Data Bus. The Data Bus drivers to the CPU are placed in the high impedance state.

Bus Enable ($\overline{BUSEN}$, Input)

$\overline{BUSEN}$ is supplied to the Am8228/8238 by external circuits to allow the CPU Data Bus to be disconnected from the memory and I/O circuits for external control of these circuits. The System Data Bus, DB0 through DB7 function normally when $\overline{BUSEN}$ is low. When $\overline{BUSEN}$ is high the output drivers for the System Data Bus, DB0 through DB7, are switched to the high impedance state.

Status Strobe ($\overline{STSTB}$, Input)

$\overline{STSTB}$ is a sample pulse used to strobe machine cycle status into the Status Latches. $\overline{STSTB}$ developed from the coincidence of $\Phi 1$ and SYNC of the Am8224.

Bidirectional

Data Bus 9080A Side (D0 - D7, Bidirectional)

D0 through D7 forms the CPU bidirectional Data Bus. The direction of information transfer is controlled by $\overline{WR}$ and $\overline{DBIN}$.

Data Bus System Side (DB0 - DB7, Bidirectional)

DB0 through DB7 forms the System bidirectional Data Bus. This connects to all microcomputer devices except the CPU requiring a Data Bus connection. Information transfer on the System Data Bus is controlled by $\overline{WR}$, $\overline{DBIN}$, HLDA and $\overline{BUSEN}$.

Outputs

I/O Read ($\overline{I/OR}$, Output)

$\overline{I/OR}$ is the Input read control signal. It is generated in response to the execution of an INP instruction by the CPU. $\overline{I/OR}$ is generated when the INP status bit is latched in the Am8228/8238. This signal provides the correct timing to read information from a selected I/O Port.

I/O Write ($\overline{I/OW}$, Output)

$\overline{I/OW}$ is a write control signal which is used to gate information supplied by the CPU to the appropriately addressed I/O peripheral device. It is generated in the Am8228 when $\overline{WR}$ is low and the OUT status bit is latched. In the Am8238, $\overline{I/OW}$ appears as soon as the OUT status bit is latched.

Memory Read ($\overline{MEMR}$, Output)

$\overline{MEMR}$ is the memory read signal; it is used by the memory system to control the time at which a byte of data is placed on the Data Bus to be read by the CPU. The $\overline{MEMR}$ signal appears at the output of the Am8228/8238 when the $\overline{MEMR}$ status bit is latched in the status latches.

Memory Write ($\overline{MEMW}$, Output)

$\overline{MEMW}$ causes the memory system to store the contents of the Data Bus in a selected memory byte. The latched $\overline{WO}$ status bit is gated with $\overline{WR}$ in the Am8228 to produce $\overline{MEMW}$. In the Am8238, $\overline{MEMW}$ appears at the output after

the $\overline{WO}$ status bit is latched.

Interrupt Acknowledge (INTA, Output)
The Interrupt acknowledge control signal requests the interrupting device to place one instruction byte on the Data Bus.

Circuits are included in the Am8228/8238 to place the instruction RST7 onto the Data Bus automatically during the Interrupt Acknowledge machine cycle if INTA is connected to + 12V through a limiting resistor.

THE SYSTEM CONTROL BUS

Five Control Bus signals are generated within the Am8228/8238 for use by other microcomputer components. These are:

- $\overline{I/OR}$ causes a byte to be read from an I/O device.
- $\overline{I/OW}$ causes a byte to be written to an I/O device.
- $\overline{MEMR}$ causes a byte to be read from memory.
- $\overline{MEMW}$ causes a byte to be written to memory.
- $\overline{INTA}$ calls for an interrupt instruction byte from an external device.

Table 5-2 shows the control signals generated for different machine cycles.

TABLE 5-2 Am8228/8238 CONTROL SIGNALS

TYPE OF MACHINE CYCLE	STATUS BIT AND DATA BUS LOCATION								ACTIVE CONTROL SIGNAL GENERATED
	D7 MEMR	D6 INP	D5 M1	D4 OUT	D3 HLTA	D2 STACK	D1 $\overline{WO}$	D0 INTA	
Instruction Fetch	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	1	0	0	0	1	0	1	0	NONE
Interrupt Acknowledge While Halted	0	0	1	0	1	0	1	1	$\overline{INTA}$
Null	0	0	0	0	0	0	1	0	$\overline{INTA}$

TABLE 5-3 Am8228/8238 CONTROL BUS RESPONSES FOR CALL INTERRUPT INSTRUCTION

INSTRUCTION TYPE	INPUTS TO STATUS LATCHES								MACHINE CYCLE		CONTROL BUS OUTPUTS				
	D7 MEMR	D6 INP	D5 M1	D4 OUT	D3 HLTA	D2 STACK	D1 $\overline{WO}$	D0 INTA	#	TYPE	$\overline{MEMR}$	$\overline{MEMW}$	$\overline{I/OR}$	$\overline{I/OW}$	$\overline{INTA}$
CALL	0	0	1	0	0	0	1	1	M1	INTERRUPT ACKNOWLEDGE	1	1	1	1	0
	0	0	0	0	0	0	1	0	M2	NULL	1	1	1	1	0
	0	0	0	0	0	0	1	0	M3	NULL	1	1	1	1	0
	0	0	0	0	0	1	0	0	M4	STACK WRITE	1	0	1	1	0
	0	0	0	0	0	1	0	0	M5	STACK WRITE	1	0	1	1	0
NEXT INSTRUCTION	1	0	1	0	0	0	1	0	M1	INSTRUCTION FETCH	0	1	1	1	1

1 = HIGH LOGIC LEVEL
0 = LOW LOGIC LEVEL

Am8224

Clock Generator and Driver

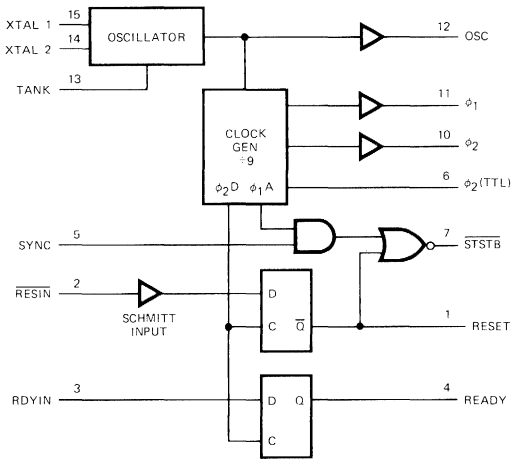
Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- Oscillator output for external system timing
- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and ϕ_2 outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications.

LOGIC DIAGRAM

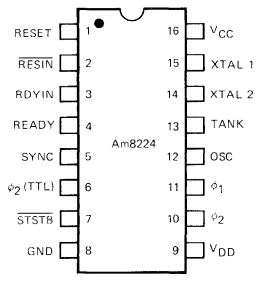


PIN DEFINITION

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2(TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5.0V
V_{DD}	+12V
GND	0V
$\overline{\text{RESIN}}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{\text{STSTB}}$	STATUS STB (ACTIVE LOW)
ϕ_1	Am9080A/8080A CLOCKS
ϕ_2	

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM8224DM
Hermetic DIP	0°C to +70°C	AM8224DC
Molded DIP	0°C to +70°C	AM8224PC
Dice	0°C to +70°C	AM8224XC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	7.5V
V_{DD}	15V
Maximum Output Current ϕ_1 and ϕ_2 (Note 1)	100mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ $V_{DD} = 12V \pm 5\%$
Am8224XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ $V_{DD} = 12V \pm 10\%$

Parameters	Description	Test Conditions		Min.	Typ. (Note 2)	Max.	Units
I_F	Input Current Loading	$V_F = 0.45V$				−0.25	mA
I_R	Input Leakage Current	$V_R = 5.25V$				10	μA
V_C	Input Forward Clamp Voltage	$I_C = -5.0mA$	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage	$V_{CC} = 5.0V$				0.8	Volts
V_{IH}	Input HIGH Voltage	Reset input	COM'L	2.6	2.2		Volts
			MIL	2.8	2.2		
		All other inputs		2.0			
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	$V_{CC} = 5.0V$		0.25	0.5		Volts
V_{OL}	Output LOW Voltage	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ $I_{OL} = 2.5mA$				0.45	Volts
		All other inputs $I_{OL} = 15mA$				0.45	
V_{OH}	Output HIGH Voltage	ϕ_1, ϕ_2; $I_{OH} = -100\mu A$	COM'L	9.4	11		Volts
			MIL	$V_{DD}-1.6V$	$V_{DD}-1.0V$		
		READY, RESET; $I_{OH} = -100\mu A$	COM'L	3.6	4.0		
			MIL	3.35	4.0		
		All other outputs; $I_{OH} = -1.0mA$		2.4	3.0		
I_{SC}	Output Short Circuit Current (All Low Voltage Outputs Only)	$V_O = 0V$ $V_{CC} = 5.0V$		−10		−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 3)			70	115	mA
I_{DD}	Power Supply Current	V_{DD} = MAX.			5.0	12	mA

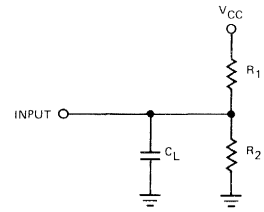
Notes: 1. Caution: ϕ_1 and ϕ_2 outputs do not have short circuit protection.
2. Typical limits are at $V_{CC} = 5.0V$, $V_{DD} = 12V$, 25°C ambient and maximum loading.
3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C - 70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

TEST CIRCUIT



AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am8224XM Min.	Am8224XM Typ.	Am8224XM Max.	Am8224XC Min.	Am8224XC Typ.	Am8224XC Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	C_L = 20pF to 50pF	$\frac{2t_{CY}}{9}$ - 23ns			$\frac{2t_{CY}}{9}$ - 20ns			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		$\frac{5t_{CY}}{9}$ - 35ns			$\frac{5t_{CY}}{9}$ - 35ns			
t_{D1}	ϕ_1 to ϕ_2 Delay		0			0			
t_{D2}	ϕ_2 to ϕ_1 Delay		$\frac{2t_{CY}}{9}$ - 17ns			$\frac{2t_{CY}}{9}$ - 14ns			
t_{D3}	ϕ_1 to ϕ_2 Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ + 22ns	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ + 20ns	
t_r	ϕ_1 and ϕ_2 Rise Time				20			20	
t_f	ϕ_1 and ϕ_2 Fall Time				20			20	
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay	ϕ_2(TTL), C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω	−5.0		15	−5.0		15	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{6t_{CY}}{9}$ - 33ns		$\frac{6t_{CY}}{9}$	$\frac{6t_{CY}}{9}$ - 30ns		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9}$ - 18ns			$\frac{t_{CY}}{9}$ - 15ns			
t_{DRS}	RDYIN Set-up Time to Status Strobe		50ns - $\frac{4t_{CY}}{9}$			50ns - $\frac{4t_{CY}}{9}$			
t_{DRH}	RDYIN Hold Time After STSTB		$\frac{4t_{CY}}{9}$			$\frac{4t_{CY}}{9}$			
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	Ready and Reset C_L = 10pF, R_1 = 2.0kΩ, R_2 = 4.0kΩ	$\frac{4t_{CY}}{9}$ - 25ns			$\frac{4t_{CY}}{9}$ - 25ns			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$			$\frac{t_{CY}}{9}$		
f_{max}	Maximum Oscillating Frequency		27			28.12			MHz
C_{in}	Input Capacitance	V_{CC} = 5.0V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1.0MHz			8.0			8.0	pF

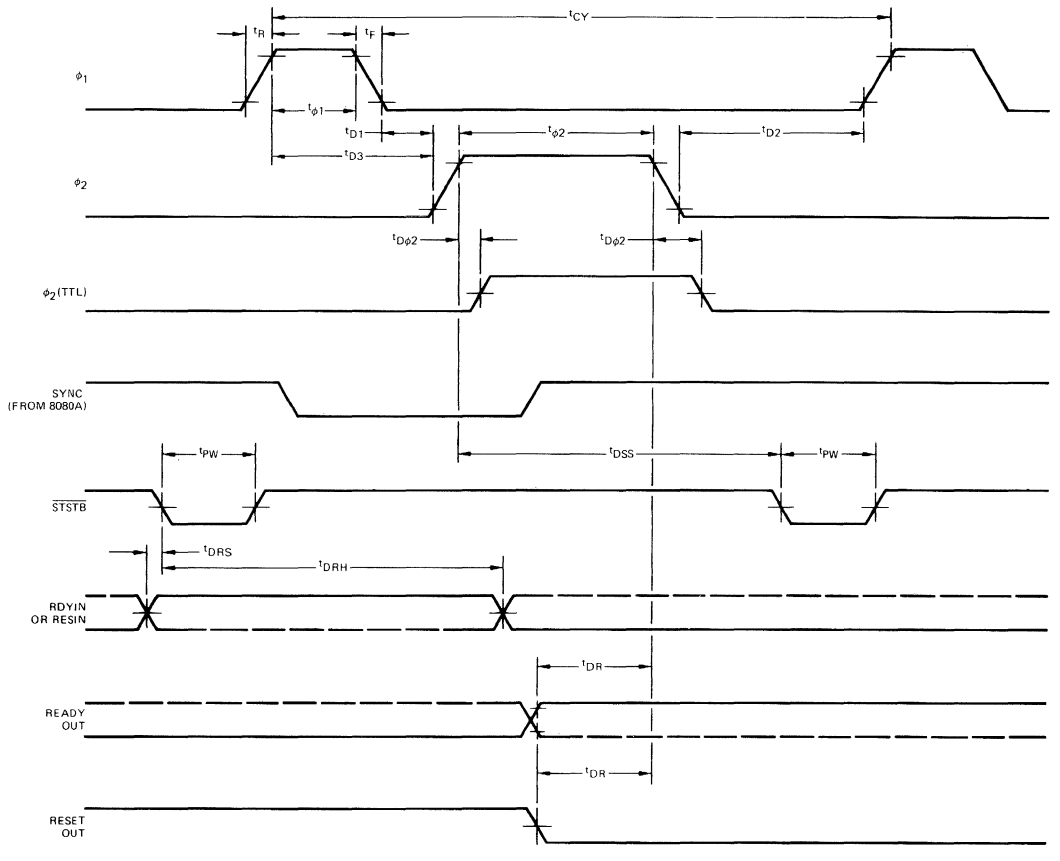
AC CHARACTERISTICS (For t_{CY} = 488.28ns)

T_A = 0°C to +70°C V_{CC} = +5.0V ±5% V_{DD} = +12V ±5%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	ϕ_1 and ϕ_2 Loaded to C_L = 20 to 50pF	89			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		236			ns
t_{D1}	Delay ϕ_1 to ϕ_2		0			ns
t_{D2}	Delay ϕ_2 to ϕ_1		95			ns
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay		−5.0		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-up Time to $\overline{STSTB}$	Ready and Reset Loaded to 2.0mA/10pF	−167			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		217			ns
t_{DR}	Ready or Reset to ϕ_2 Delay		192			ns
FREQ	Oscillator Frequency				18.432	MHz

Note: 1. All measurements referenced to 1.5V unless specified otherwise.

SWITCHING WAVEFORMS



Voltage measurement points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to guide the crystal selection is:

$$\text{Crystal Frequency} = \frac{1}{t_{CY}} \text{ times } 9$$

When using crystals above 10MHz a small amount of frequency "trimming" may be necessary to produce the desired frequency. The addition of a small selected capacitance (3pF – 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has much lower "gain" than the fundamental type so an external LC network is necessary to provide the additional "gain" for proper oscillator operation. The external LC network is connected to the TANK input and is AC coupled to ground. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; phase 1 and phase 2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator fre-

quency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{\text{STSTB}}$) is achieved.

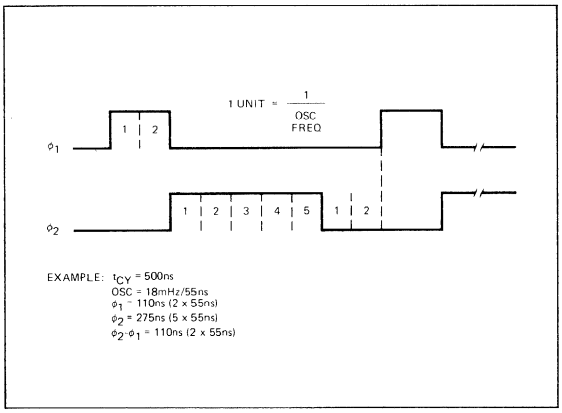


Figure 1. Clock Generator Waveforms.

$\overline{\text{STSTB}}$ (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ1A), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{\text{STSTB}}$ signal connects directly to the Am8228 System Controller.

The power-on Reset also generates $\overline{\text{STSTB}}$, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the $\overline{\text{RESIN}}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ2D (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ2D, a synchronized READY signal at the correct input level, can be connected directly to the CPU.

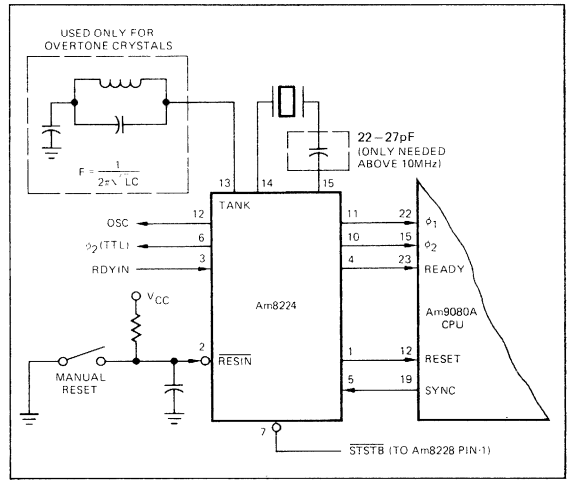
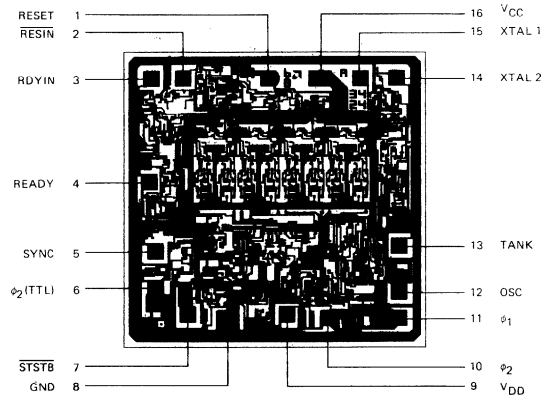


Figure 2. Typical Application with Am8224 and Am9080A.

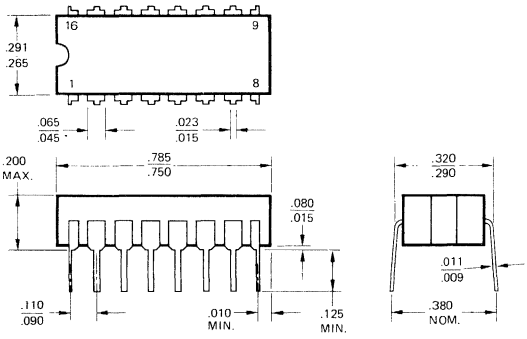
Metallization and Pad Layout



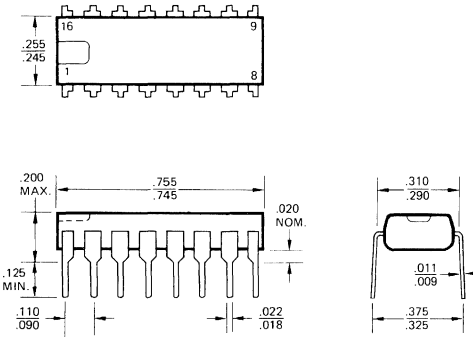
DIE SIZE
0.085" X 0.084"

PHYSICAL DIMENSIONS
Dual-In-Line

Hermetic



Molded



Am8228 • Am8238

System Controller and Bus Driver

Distinctive Characteristics

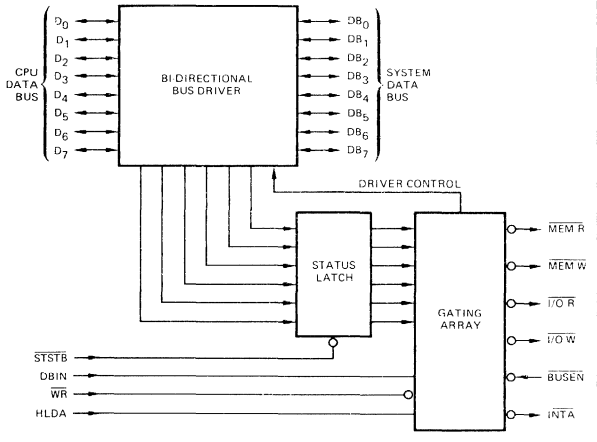
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080A/8080A systems
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}$/$\overline{MEMW}$ pulse width

FUNCTIONAL DESCRIPTION

The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A single byte and multiple byte interrupt operation.

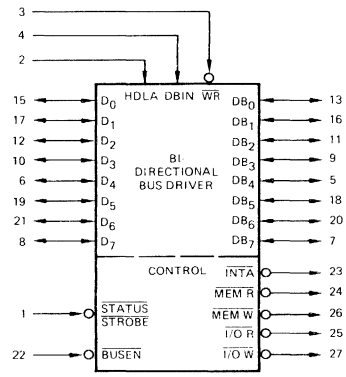
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am8228 Order Number	Am8238 Order Number
Molded DIP	0°C to +70°C	AM8228PC	AM8238PC
Hermetic DIP	0°C to +70°C	D8228	D8238
Hermetic DIP	−55°C to +125°C	AM8228DM	AM8238DM
Dice	0°C to +70°C	AM8228XC	AM8238XC

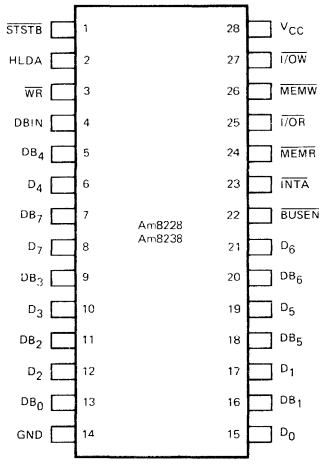
LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−1.5V to +7.0V
DC Output Current, Into Outputs	50mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

Am8228DM, Am8238DM T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

Am8228PC, Am8228XC, D8228, Am8238PC, Am8238XC, D8238 T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −10μA	D_0-D_7	MIL	3.35	3.8		Volts
					COM'L	3.6	3.8		
			I_{OH} = −1.0mA	All other outputs		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 2.0mA	D_0-D_7				0.45	Volts
			I_{OL} = 10mA	All other outputs				0.45	
V_C	Input Clamp Voltage (All Inputs)	V_{CC} = MIN., I_C = −5.0mA					−0.75	−1.0	Volts
V_{TH}	Input Threshold Voltage (All Inputs)	V_{CC} = 5.0V				0.8		2.0	Volts
I_F	Input Load Current	V_{CC} = MAX., V_F = 0.45V		$\overline{STSTB}$				500	μA
				D_2 and D_6				750	
				All other inputs				250	
I_R	Input Leakage Current	V_{CC} = MAX., V_R = 5.25V		DB_0 – DB_7				20	μA
				All other inputs				100	
I_{INT}	INTA Current	See INTA test circuit						5.0	mA
$I_{O(OFF)}$	Off State Output Current (All Control Outputs)	V_{CC} = MAX., V_O = 5.25V						100	μA
		V_O = 0.45V						−100	
I_{OS}	Short Circuit Current (All Ouputs)	V_{CC} = 5.0V				15		90	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					140	190	mA

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am8228XM/Am8238XM Min.	Typ. (Note 1)	Max.	Am8228XC/Am8238XC Min.	Typ. (Note 1)	Max.	Units
t_{PW}	Width of Status Strobe		22			22			ns
t_{SS}	Set-up Time, Status Inputs D_0-D_7		12			8.0			ns
t_{SH}	Hold Time, Status Inputs D_0-D_7		5.0			5.0			ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	C_L = 100pF	20	30	60	20	30	60	ns
t_{RR}	Delay from DBIN to Control Outputs			15	35		15	30	ns
t_{RE}	Delay from DBIN to Enable/Disable 8080A Bus	C_L = 25pF		25	45		25	45	ns
t_{RD}	Delay from System Bus to 8080A Bus During Read			15	30		15	30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	C_L = 100pF	5.0	20	45	5.0	20	45	ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 After $\overline{STSTB}$			25	36		25	30	ns
t_{WD}	Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 During Write		5.0	20	40	5.0	20	40	ns
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7			25	35		25	30	ns
t_{HD}	HLDA to Read Status Outputs			15	28		15	25	ns
t_{DS}	Set-up Time, System Bus Inputs to HLDA		10			10			ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20			20			ns

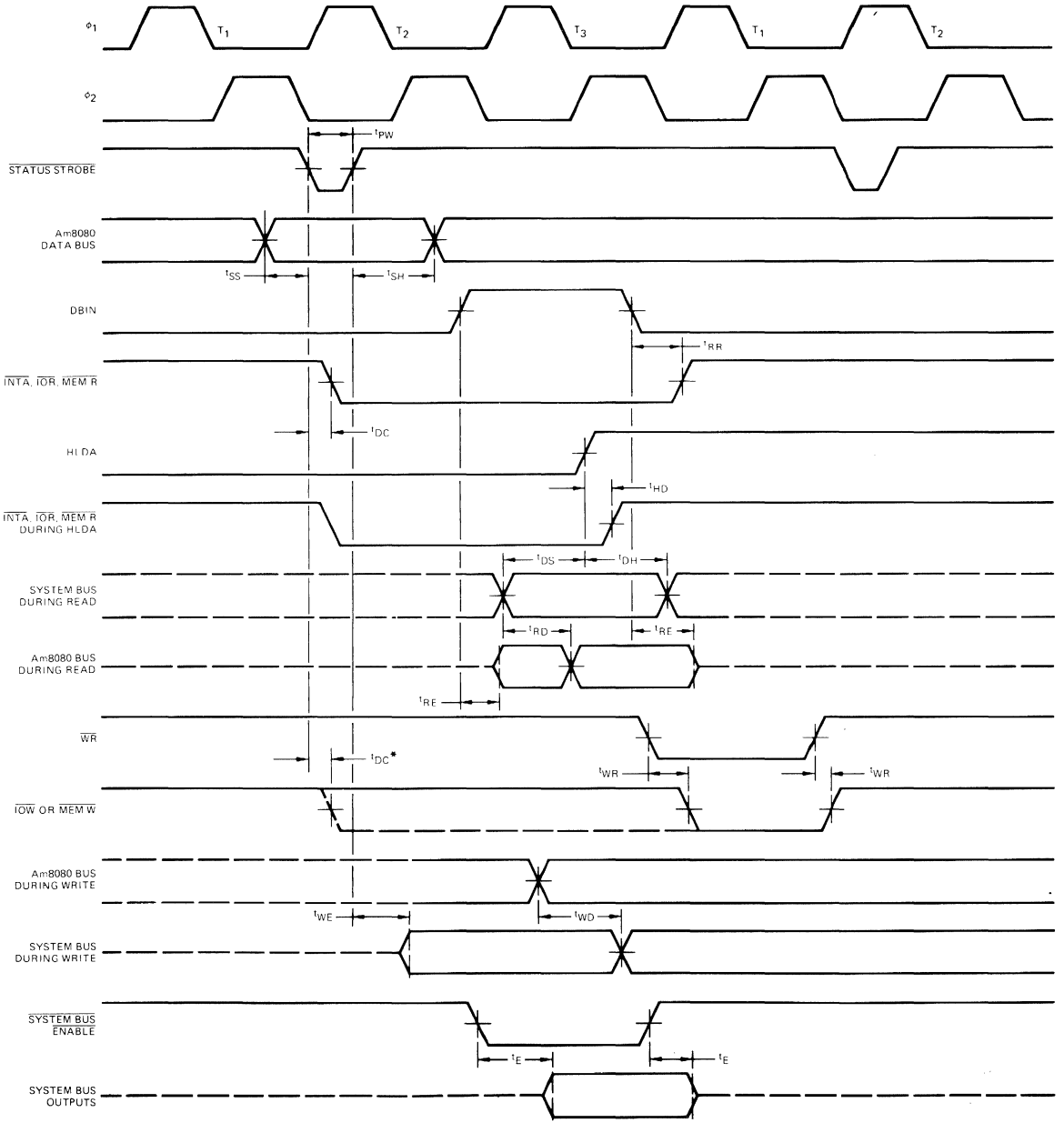
Notes: 1. Typical values are for T_A = 25°C and nominal supply voltages.

2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

CAPACITANCE (This parameter is periodically sampled and not 100% tested.)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5 V, V_{CC} = 5.0 V T_A = 25°C, f = 1.0 MHz		8.0	12	pF
C_{OUT}	Output Capacitance Control Signals			7.0	15	pF
I/O	I/O Capacitance (D or DB)			8.0	15	pF

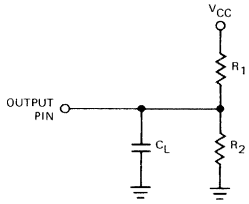
SWITCHING WAVEFORMS

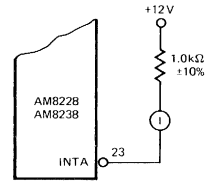


Voltage measurements points: $D_0 - D_7$ (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Extended $\overline{IOW}/\overline{MEMW}$ for Am8238 only.

TEST CIRCUITS





Note 1. For $D_0 - D_7$: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.

INTA (for RST 7)

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver: An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

Status Latch: The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{STSTB}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array: The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch Am9080A signals; i.e., DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

DEFINITION OF FUNCTIONAL TERMS

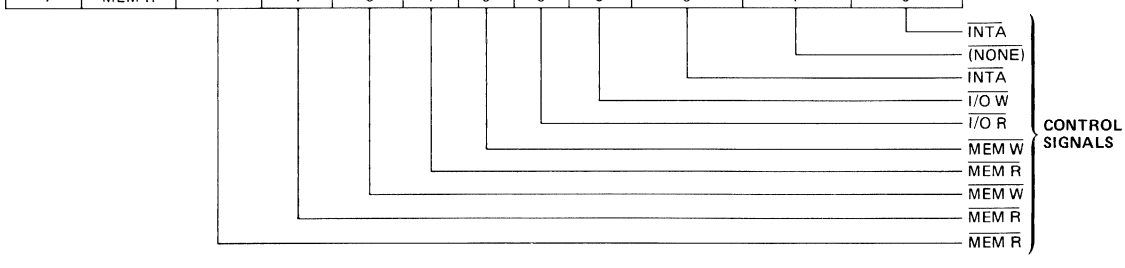
D_7-D_0	Data bus to-from Am9080A/8080A
DB_7-DB_0	Data bus to-from user system
$\overline{I/OR}$	Input/output read strobe output active LOW
$\overline{I/OW}$	Input/output write strobe output active LOW
$\overline{MEM\ R}$	Memory read strobe, output, active LOW
$\overline{MEM\ W}$	Memory write strobe, output, active LOW
DBIN	Data bus input strobe, input active HIGH
$\overline{INTA}$	Interrupt acknowledge strobe, input, active LOW
HLDA	Hold input from Am9080A/8080A active HIGH
$\overline{WR}$	Write input strobe, active HIGH
$\overline{BUSEN}$	BUSS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out
$\overline{STSTB}$	Status Strobe, input, strobes status on data bus into status latch, active LOW

LOADING RULES

Signal	Pin No.	Input Load	Output Sink	Output Source
D_0	15	250μA	2mA	−10μA
D_1	17	250μA	2mA	−10μA
D_2	12	750μA	2mA	−10μA
D_3	10	250μA	2mA	−10μA
D_4	6	250μA	2mA	−10μA
D_5	19	250μA	2mA	−10μA
D_6	21	750μA	2mA	−10μA
D_7	8	250μA	2mA	−10μA
DB_0	13	250μA	10mA	−1mA
DB_1	16	250μA	10mA	−1mA
DB_2	11	250μA	10mA	−1mA
DB_3	9	250μA	10mA	−1mA
DB_4	5	250μA	10mA	−1mA
DB_5	18	250μA	10mA	−1mA
DB_6	20	250μA	10mA	−1mA
DB_7	7	250μA	10mA	−1mA
$\overline{STSTB}$	1	500μA	–	–
DBIN	4	250μA	–	–
$\overline{WR}$	3	250μA	–	–
HLDA	2	250μA	–	–
$\overline{MEM\ R}$	24	–	10mA	−1mA
$\overline{MEM\ W}$	26	–	10mA	−1mA
$\overline{I/OR}$	25	–	10mA	−1mA
$\overline{IOW}$	27	–	10mA	−1mA
$\overline{BUSEN}$	22	250μA	–	–
$\overline{INTA}$	23	–	10mA	−1mA
GND	14			
V_{CC}	28			

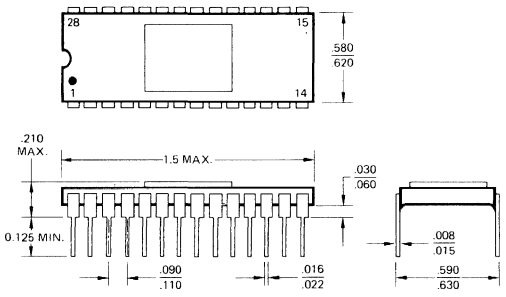
STATUS WORD CHART

		TYPE OF MACHINE CYCLE										
Data Bus Bit	Status Information	Instruction Fetch	Memory Read	Memory Write	Stack Read	Stack Write	Input Read	Output Write	Interrupt Acknowledge	Halt Acknowledge	Interrupt Acknowledge While Halt	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEM R	1	1	0	1	0	0	0	0	1	0	

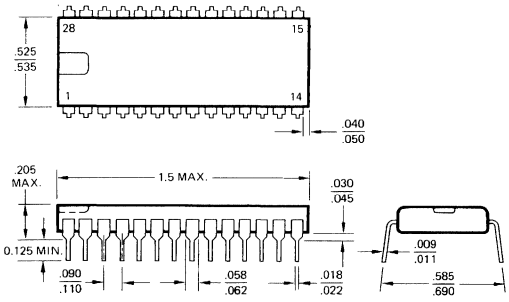


PHYSICAL DIMENSIONS
Dual-In-Line

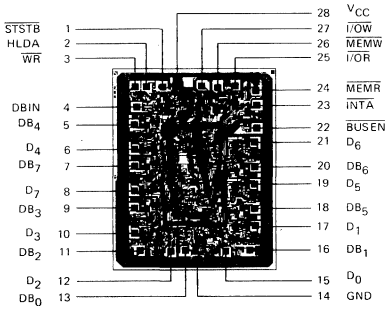
28-Pin Side Brazed



28-Pin Molded



Metallization and Pad Layout



DIE SIZE
0.110" X 0.136"

Chapter 6
Am8212 INPUT/OUTPUT PORT

The Am8212 is a general purpose device that provides TTL compatible, parallel 8-bit interface logic with high fan-out for a wide variety of applications in typical microprocessor systems. It may be used as a bus driver, an input port, an output port, or in other applications such as gating interrupt vectors to the Data Bus.

This device has an output high signal level of 3.65 volts or greater, insuring compatibility with virtually every microprocessor available. An input low current load on the data lines of 0.25 mA and a high output sink current drive on the data lines of 15 mA makes the part very flexible as an interface element to microprocessor Data Busses.

FUNCTIONAL DESCRIPTION

The logic diagram for the Am8212 is shown in Figure 6-1. It shows 8-bit parallel latch and driver circuits, plus interrupt request and enable control logic.

The 8-bit parallel data logic consists of eight D-type flip-flops each of which has a noninverting 3-state buffer on the Q outputs. This combination allows data to be transferred from external logic into the microcomputer system or from the microcomputer system to external logic.

In order to transfer data from external logic to the microcomputer system, information can be input to the D-type flip-flops at any time, whether or not the Am8212 device has been selected by the microprocessor. When the microprocessor selects the device, internal logic causes the contents of the flip-flops to be output by enabling the eight 3-state buffers on the flip-flop output lines.

The interrupt logic is designed to create an interrupt request during the time interval between external logic strobing data into the latches and the microprocessor reading this data.

When the Am8212 device is being used to transfer data from a microcomputer system to external logic, the microprocessor provides the data input and device select logic causes input data to be strobed into the flip-flops. Simultaneously the 3-state buffers on the flip-flop outputs are enabled so that external logic is able to read data off the output lines.

Am8212 INTERFACE SIGNALS

Figure 6-2 shows the Connection Diagram for the Am8212.

Input

Data Input (DI0 - DI7, Input)
These are the eight Data Input signals to the D-type flip-flops.

Clear ($\overline{CLR}$, Input)
$\overline{CLR}$ resets all of the data flip-flops when input low, and sets the interrupt request signal $\overline{INT}$ high.

Device Select ($\overline{DS1}$ and DS2, Input)
These signals are used to select the Am8212 for an active operation. $\overline{DS1}$ must be low and DS2 must be high for selection. The consequences of selecting the Am8212 are a function of the mode in which the device is operating.

Mode Select (MD, Input)
The MD input determines whether the unit will be operated in Input or Output mode.

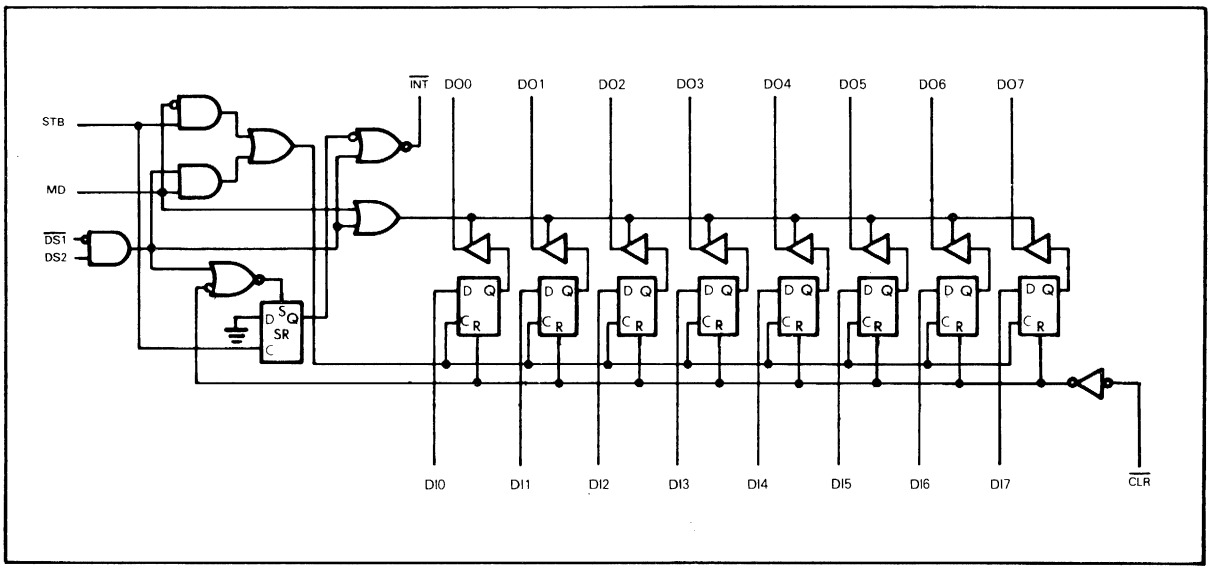


FIGURE 6-1 Am8212 LOGIC DIAGRAM

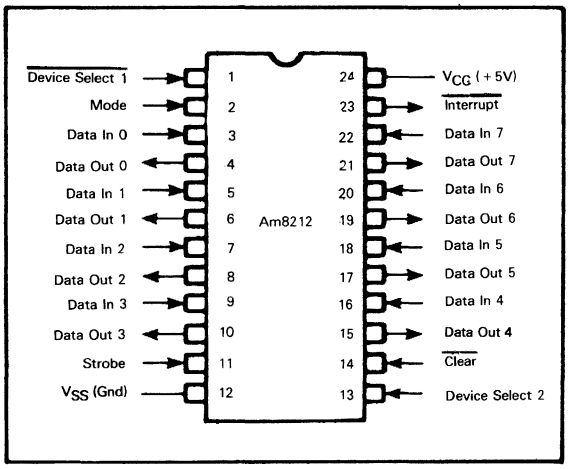


FIGURE 6-2 Am8212 CONNECTION DIAGRAM

When MD is low, the Am8212 is operating in Input mode. In this mode device select logic enables output on the DO0-DO7 pins while separate logic strobes data into the Am8212, irrespective of whether the device has been selected.

When MD is high, the Am8212 is operating in Output Mode. Now device select logic simultaneously strobes data into the flip-flops and enables data out.

Strobe (STB, Input)

Strobe is an input control signal which is active in Input Mode only. External logic uses this signal in order to strobe data into the flip-flops. This signal also contributes to the logic which determines the level of the interrupt request signal INT.

Output

Data Output (DO0 - DO7, Output)

DO0 through DO7 are the eight data output signals from the 3-state buffers.

Interrupt Request ($\overline{INT}$, Output)

This is the output signal used to request interrupt service from the microprocessor.

OPERATING MODES

The simplest way of understanding Am8212 logic is to initially ignore the interrupt section and examine the 8-bit parallel data path when the device is operating in Input or Output mode.

There are two important signals created within the Am8212: the D-type flip-flop clock input and the output buffer enable. Logic equations for these two signals are as follows:

$C = (\overline{MD} \cdot STB) + (MD \cdot (\overline{DS1} \cdot DS2))$ Clock equation

$EN = MD + \overline{DS1} \cdot DS2$ Output buffer enable equation

Output Mode

Output Mode operation is selected by the MD control being input high. MD high forces the first term of the clock equation to remain permanently low thereby negating the STB signal. The D-type flip-flop clock input will now follow the device select. Simultaneously, MD high permanently enables EN, the output buffer enable control. Thus, flip-flops will be enabled. The flip-flop inputs will be sampled when the clock signal is high, which occurs when the device is selected.

Output Mode acquires its name from the fact that this use of the Am8212 will normally occur when the DI pins are connected to the microcomputer system Data Bus while the DO pins are connected to external logic. Thus an output or write instruction that selects the Am8212 will cause select logic to go true. This permits the data to flow through the flip-flops and out to external logic.

If external logic is connected to the DI pins in Output Mode, while the microcomputer system Data Bus is connected to the DO pins, then a memory read or input instruction that selects the Am8212 will cause the microcomputer system to read whatever data happens to be instantaneously present at the DI pins when the Am8212 is selected.

Input Mode

Input Mode operation is characterized by the MD control signal being input low. Referring to the flip-flop clock signal equation, a low MD input will force the second term of the clock signal equation to be inactive. Now the clock signal will follow the strobe input (STB). Irrespective of whether the Am8212 is selected or not, external logic may load data into the flip-flops by pulsing STB high while data is stable on the DI pins. The output buffer enable signal, on the other hand, must rely on device select logic for a high input, since in the first term of the buffer enable equation MD will always be low. Thus, the outputs of the flip-flops will not be available at the DO pins until the Am8212 has been selected by an input or read instruction.

Input Mode gets its name from the fact that in this mode external logic is normally connected to the DI pins while the DO pins connect to the system Data Bus. Clocking data into the flip-flops via the STB signal and enabling the outputs onto the Data Bus via the device select logic are asynchronous events. External logic can input data to the D-type flip-flops at any time and the microprocessor can subsequently read the data.

Note that nothing in the logic of the device prevents the microprocessor from connecting to the DI inputs in Input Mode, while external logic connects to the DO outputs. In this case, device select logic must now create the STB signal, while external logic must input the device select signals, $\overline{DS1}$ and DS2. In this configuration, the Am8212 is operating as a buffered and strobed output port.

INTERRUPT LOGIC

Interrupt logic associated with the Am8212 is aimed at providing Input Mode handshaking controls. Timing is illustrated in Figure 6-3.

With its D input tied to ground, the STB pulse will force the $\overline{INT}$ output low as long as the SR flip-flop is not being

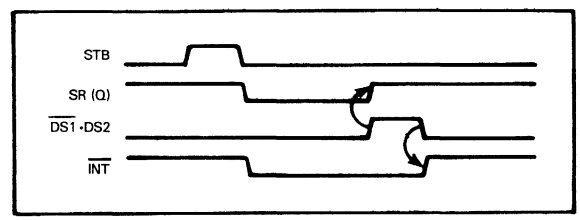


FIGURE 6-3 INTERRUPT LOGIC

clamped by the CLR input. $\overline{INT}$ will remain low until device select logic has completed a select high pulse. Thus, the $\overline{INT}$ signal remains low for the time interval between external logic strobing data into the D-type flip-flops and the microprocessor reading this data. Table 6-1 summarizes the condition of the INT output as a function of the possible inputs. SR is the internal Service Request Latch.

In the simplest case the $\overline{INT}$ output of the Am8212 device will be connected to the microprocessor's interrupt request logic. As soon as external logic strobes data into the D-type flip-flops, an interrupt request will occur. The microprocessor can enter an interrupt service routine which reads the contents of the flip-flops.

Alternatively, the $\overline{INT}$ output may be used as a handshaking signal to external logic. When external logic strobes data into the D-type flip-flops, $\overline{INT}$ is immediately output low. External logic may use the subsequent low-to-high transition of $\overline{INT}$ as an acknowledge that the microprocessor has read the contents of the Am8212 device, indicating that the external logic is free to transmit new data to the DI pins.

TABLE 6-1 $\overline{INT}$ SIGNAL LOGIC

CLR	$\overline{(DS1 \cdot DS2)}$	STB	SR	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

APPLICATIONS

Shown here are several examples of the use of the Am8212 8-bit I/O Port. These are largely illustrative in that many of its functions can now be implemented in Low-power Schottky.

Unidirectional Bus Buffer

Figure 6-4 illustrates the Am8212 device being used as a simple bus buffer.

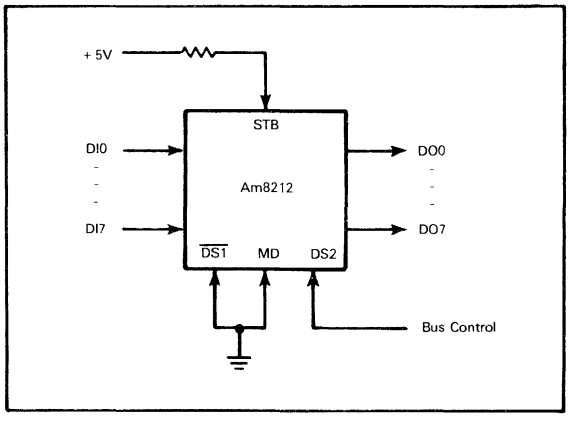


FIGURE 6-4 AN Am8212 CONFIGURED AS A BUS BUFFER

In this case, the device is operated in Input Mode, since device select logic enables or disables the buffers on the outputs. Since latching in the Input Mode is not required, the STB signal is tied high. Thus, data entering the DI pins will appear at the output. MD is shown tied to ground, which is required for Input Mode. $\overline{DS1}$ is also tied to ground. Select logic is now based on DS2. Whenever a high input occurs at DS2, data entering via the DI pins will flow through to the DO pins. Any signal will do — a data line, an address line or a control signal. As soon as DS2 receives a low input, the DO pins will enter their high impedance state. Newer microcomputer system designs would make use of the Am74LS241 for the application. This results in lower cost and lower power and replaces a 24-pin with a 20-pin device.

Bidirectional Buffer/Bus Driver

The Am8212 is easily configured as a bidirectional bus driver. In the high impedance state, the bidirectional bus driver configuration provides very low loading on one side of the bus, while maintaining high fan-out capability on the other side.

Figure 6-5 shows two Am8212 circuits connected in parallel as a bidirectional buffer/bus driver. The $\overline{STB}$, MD and DS control signal connections are similar to the unidirectional bus driver; however the $\overline{DS1}$ and DS2 control signals are selected so that the output of one is in the high impedance state when the other is in the active data transfer mode.

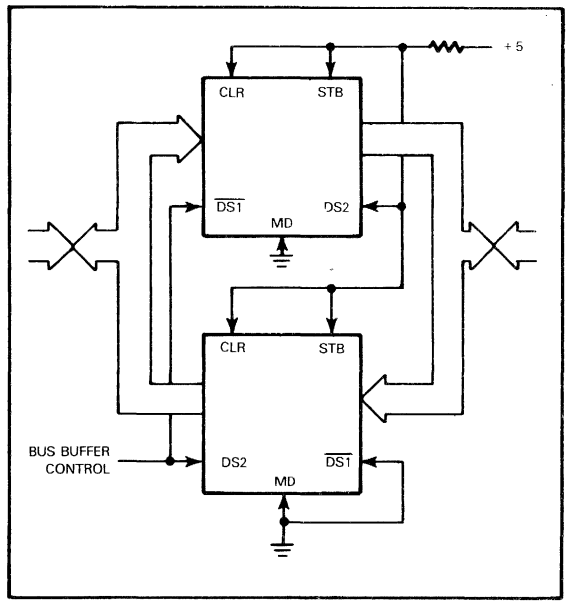


FIGURE 6-5 BIDIRECTIONAL BUS BUFFER

Again, the Low-power Schottky Am74LS241 would be a better choice for new designs in many applications.

Input Port

Two configurations for the Am8212 used as an input port, are shown in Figures 6-6 and 6-7.

In Figure 6-6 the Am8212 is connected as a port without latched inputs. The Interrupt signal is not used with this configuration because STB is permanently high.

Since MD is held low, the Am8212 is being operated in Input

Mode. However, STB is held high; therefore data arriving on the DI inputs from external logic will flow continuously into the flip-flops.

The device select signals, $\overline{DS1}$ and DS2, are used in an interesting way. Device address logic creates a single high signal in order to select the Am8212; this high signal is input at DS2. Simultaneously, the read pulse which will accompany an input or memory read instruction's execution is connected to $\overline{DS1}$. Thus the low read pulse accompanying device select will satisfy the device select logic to enable the output buffers.

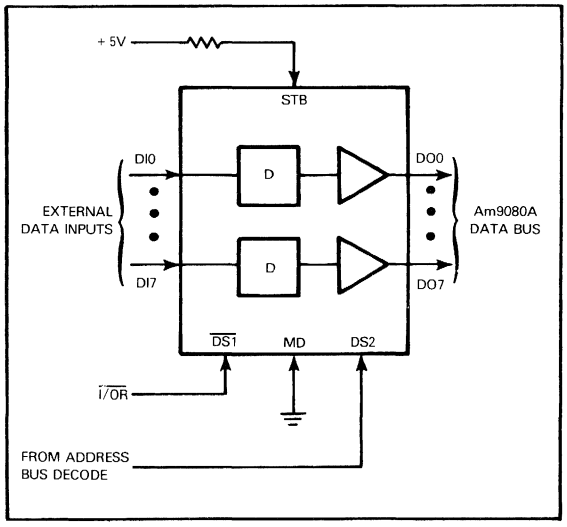


FIGURE 6-6 UNLATCHED INPUT PORT

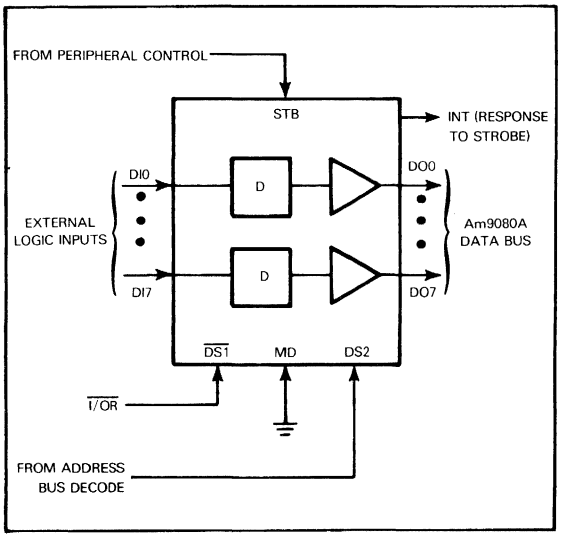


FIGURE 6-7 LATCHED INPUT PORT

The Figure 6-7 configuration shows the strobe signal STB connected to peripheral control logic which latches the input data and creates an interrupt request. Notice that STB determines the instant at which the latches accept data at the DI inputs. The DS signals determine when the latch outputs are connected to the Data Bus, and when they are in the high impedance state.

Output Port

Figure 6-8 shows the use of the Am8212 as an output port. Notice that MD is connected to +5V, creating Output Mode. $\overline{DS1}$ is connected to the microprocessor system $\overline{I/OW}$ signal, and STB can be used by the external peripheral circuit to acknowledge that information has been read by the peripheral device. In Output Mode the operation of STB does not affect the transfer of information from the input Data Bus to the latches or the data output of the Am8212; STB does activate the interrupt request to signal the CPU that the data transfer has been completed. The operation of $\overline{DS1}$ and DS2 will determine when information is read from the Data Bus into the Am8212. $\overline{DS1}$ is connected to the $\overline{I/OW}$ signal from the Am8228/8238 and DS2 is generated from the chip select logic connected to the Address Bus.

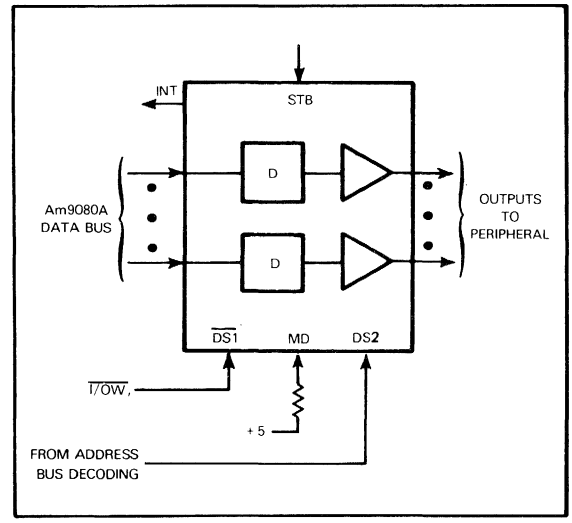


FIGURE 6-8 OUTPUT PORT

Status Latch

An Am8212 may be used as a latch to store the status signals that occur on the Am9080A Data Bus during the T1 clock period of each M1 machine cycle. When using the Am8212, rather than the Am8228/8238 System Controller, the status signal Stack will be present at the output of status latches for those applications that require it. Figure 6-9 shows a logical connection of the Am8212 as a status latch.

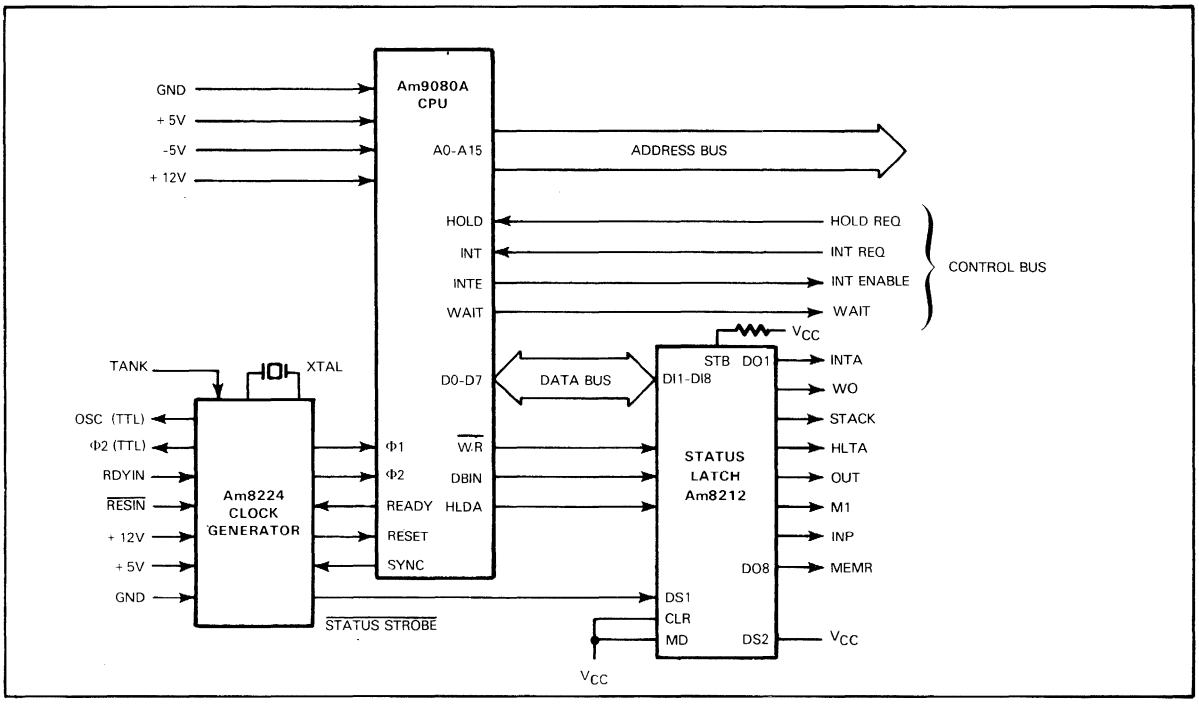


FIGURE 6-9 THE Am8212 USED AS A STATUS LATCH

Am3212·Am8212

Eight-Bit Input/Output Port

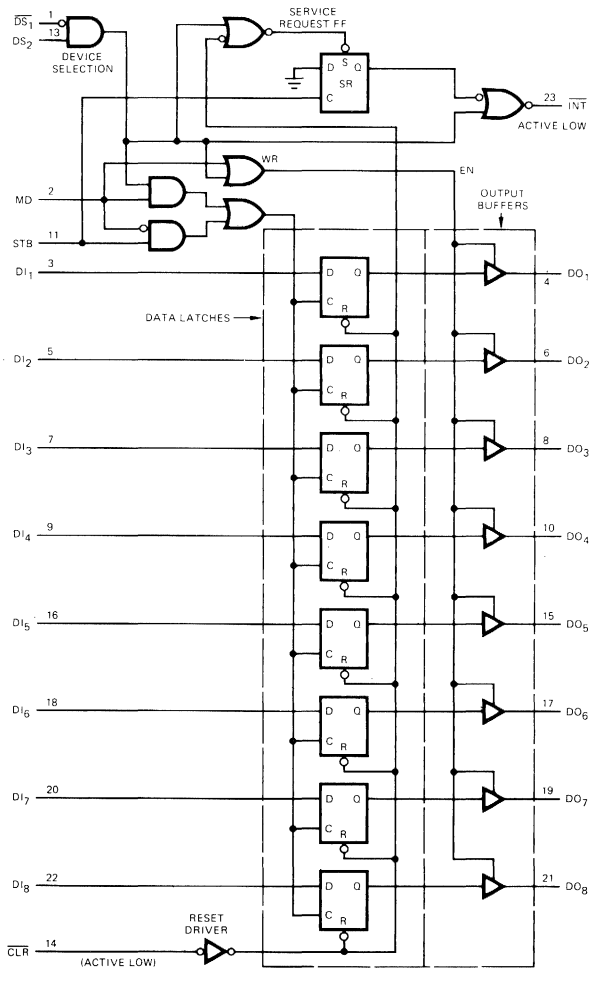
Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

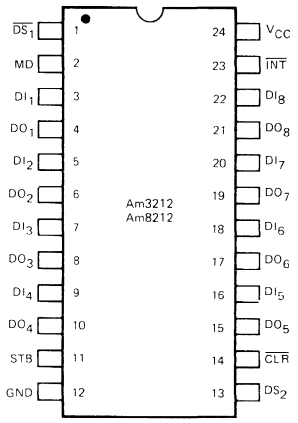
FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am3212 • Am8212. The Am3212 • Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

LOGIC DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	D8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC
Hermetic DIP	0°C to +70°C	D3212
Hermetic DIP	−55°C to +125°C	MD3212
Molded DIP	0°C to +70°C	P3212

FUNCTIONAL DESCRIPTION (Cont'd)

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am3212 • Am8212 to be connected directly onto the microprocessor bi-directional data bus.

Control Logic

The Am3212 • Am8212 has control inputs $\overline{DS_1}$, DS_2, MD And STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS_1}$, DS_2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS_1}$ is low and DS_2 is high ($\overline{DS_1} \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS_1} \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS_1} \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS_1} \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

TRUTH TABLE

STB	MD	$\overline{DS_1} - DS_2$	Data Out Equals
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$\overline{DS_1} - DS_2$	STB	SR*	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

$\overline{CLR}$ – Resets Data Latch
– Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage	−0.5V to +7.0V
Output Voltage	−0.5V to +7.0V
Input Voltages	−1.0V to +5.5V
Output Current (Each Output)	125mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212, P3212, D3212 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$
Am8212DM, MD3212 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_F	Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current DS_1 Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	$V_R = 5.25V$				10	μA
I_R	Input Leakage Current MO Input	$V_R = 5.25V$				30	μA
I_R	Input Leakage Current DS_1 Input	$V_R = 5.25V$				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5.0mA$	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage		COM'L			0.85	Volts
			MIL			0.80	
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 15mA$				0.45	Volts
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0mA$	COM'L	3.65	4.0		Volts
			MIL	3.3	4.0		
		$I_{OH} = -0.5mA$	MIL	3.5	4.0		
I_{SC}	Short Circuit Output Current	$V_O = 0V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current High Impedance	$V_O = 0.45V/5.25V$				20	μA
I_{CC}	Power Supply Current	Note 2			90	130	mA

AC CHARACTERISTICS (Note 3)

Parameters	Description	Min.	Typ. (Note 1)	Max.	Units
t_{pw}	Pulse Width	30	8		ns
t_{pd}	Data to Output Delay		12	30	ns
t_{we}	Write Enable to Output Delay		18	40	ns
t_{set}	Data Set-up Time	15			ns
t_h	Data Hold Time	20			ns
t_r	Reset to Output Delay		18	40	ns
t_s	Set to Output Delay		15	30	ns
t_e	Output Enable/Disable Time		14	45	ns
t_c	Clear to Output Delay		25	55	ns

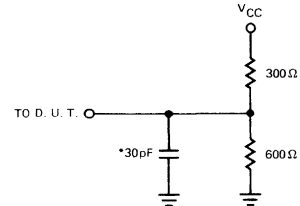
CAPACITANCE (Note 4)

F = 1.0MHz, $V_{BIAS} = 2.5V$, $V_{CC} = +5.0V$, $T_A = 25°C$

Parameters	Description	Typ.	Max.	Units
C_{IN}	DS_1 MD Input Capacitance	9.0	12	pF
C_{IN}	DS_2, CK, ACK, $DI_1 - DI_8$ Input Capacitance	5.0	9.0	pF
C_{OUT}	$DO_1 - DO_8$ Output Capacitance	8.0	12	pF

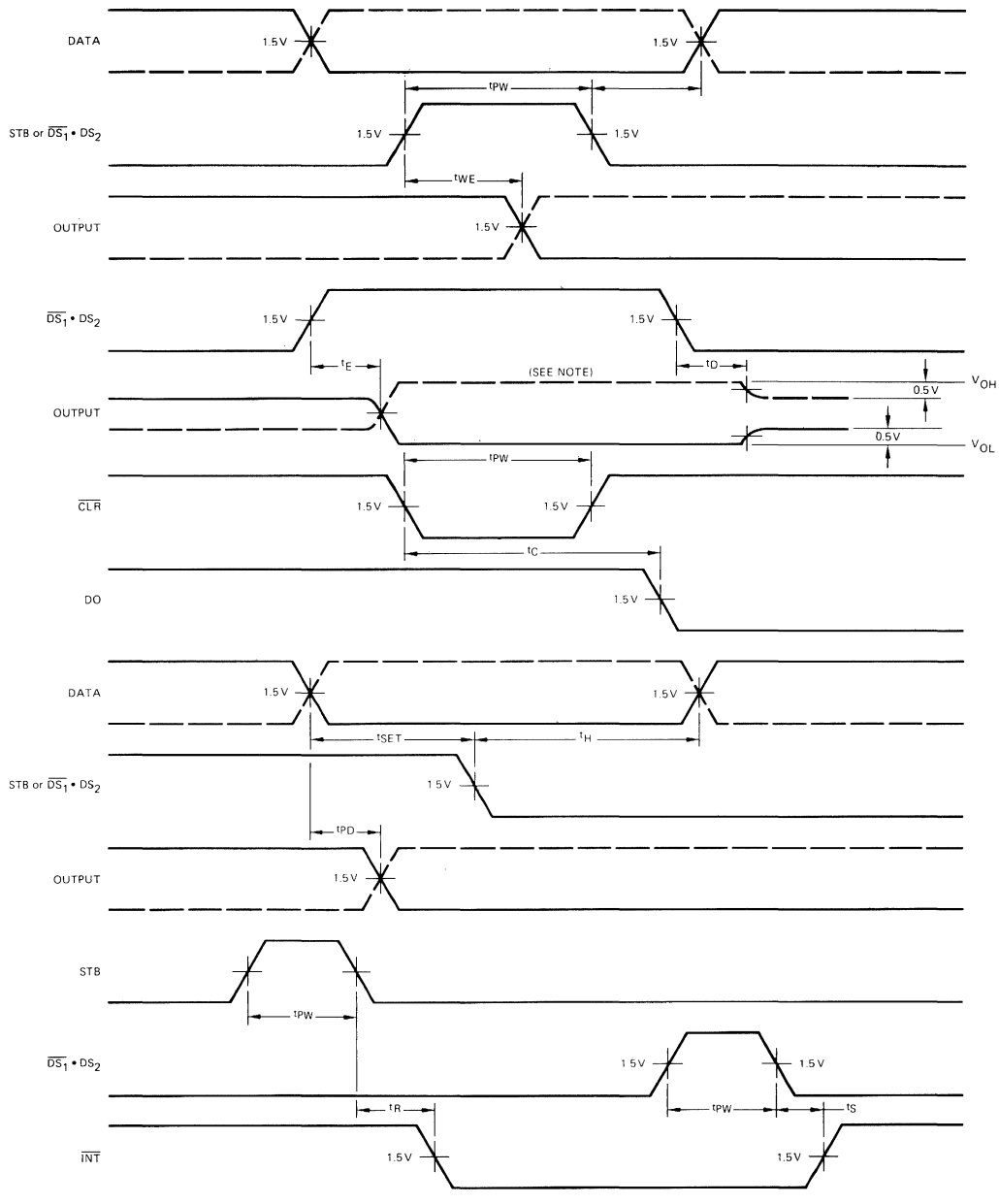
Notes: 1. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; $DS_1 = DS_2$ = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

TEST LOAD (15mA and 30pF)

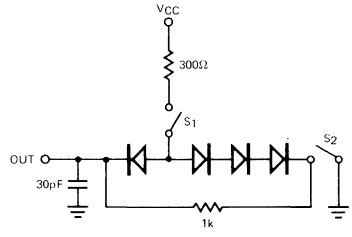


*Including Jig and Probe Capacitance.

TIMING DIAGRAM

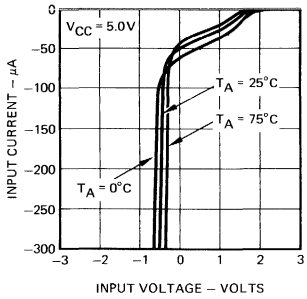


Note: Alternative Test Load.

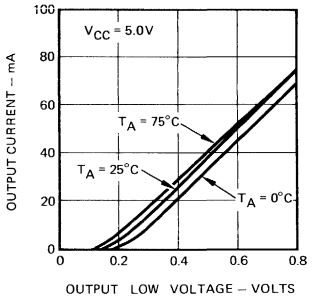


TYPICAL CHARACTERISTICS

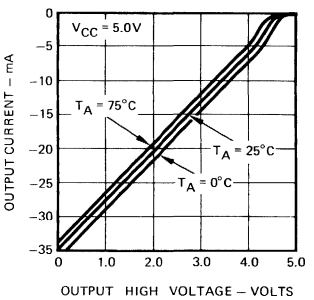
Input Current Versus Input Voltage



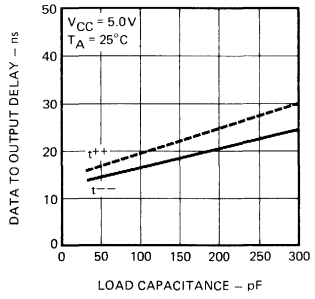
Output Current Versus Output LOW Voltage



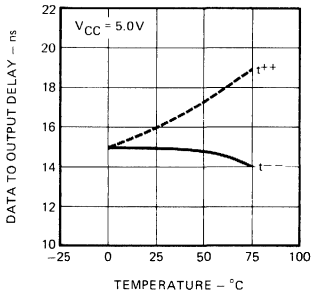
Output Current Versus Output HIGH Voltage



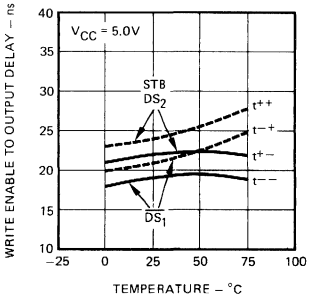
Data to Output Delay Versus Load Capacitance



Data to Output Delay Versus Temperature

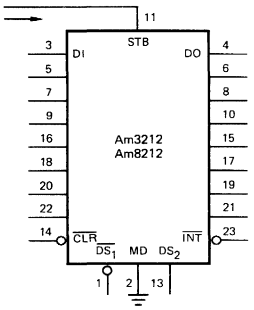


Write Enable to Output Delay Versus Temperature



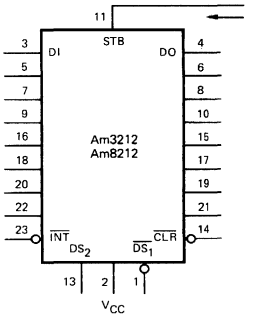
LOGIC SYMBOLS

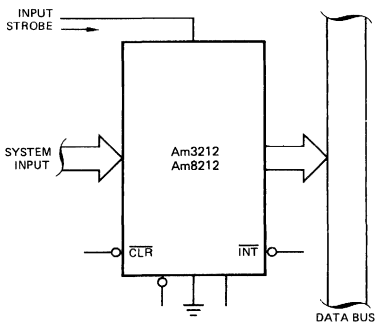
INPUT DEVICE



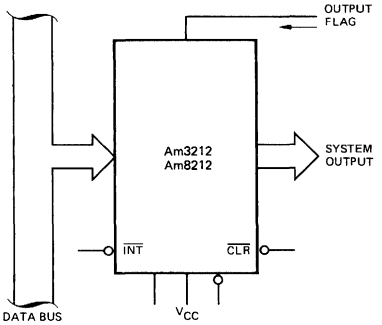
Detailed

OUTPUT DEVICE





Symbolic



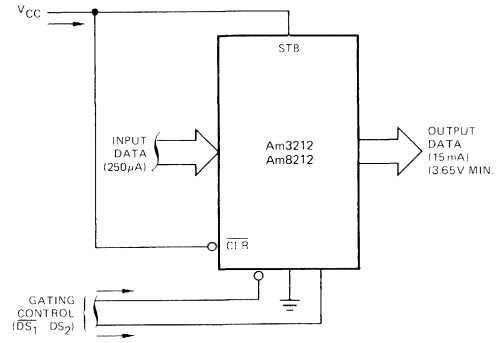
TYPICAL APPLICATIONS OF THE Am8212

GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and DS_2.

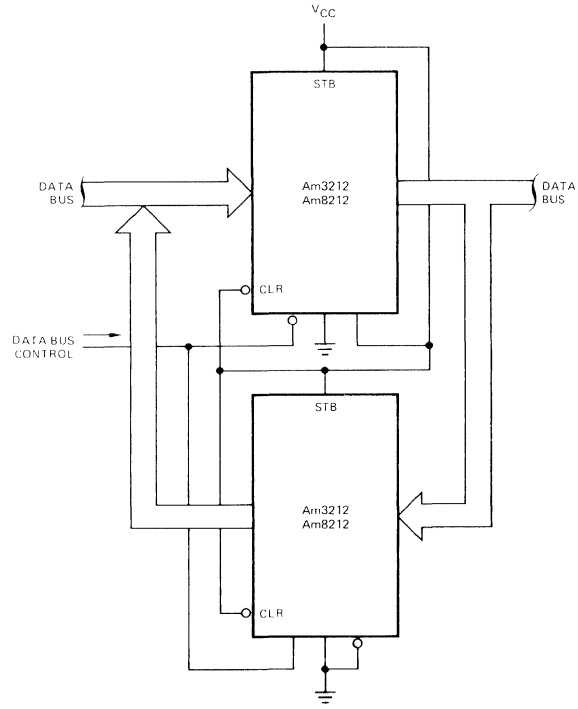
When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output.



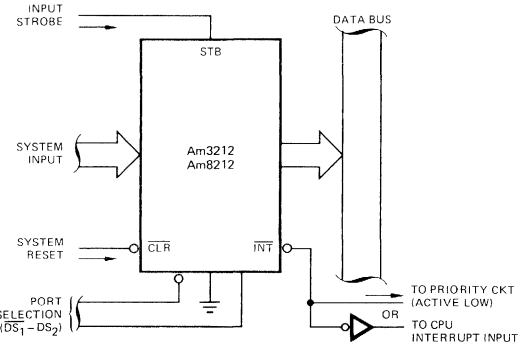
Bi-Directional Bus Driver

Two Am3212 • Am8212's wired back-to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am3212 • Am8212 and to DS_2 on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.



Interrupting Input Port

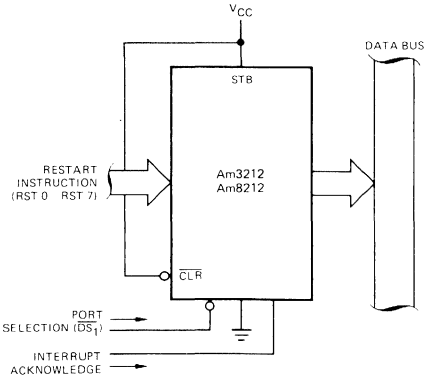
The Am3212 • Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.



TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

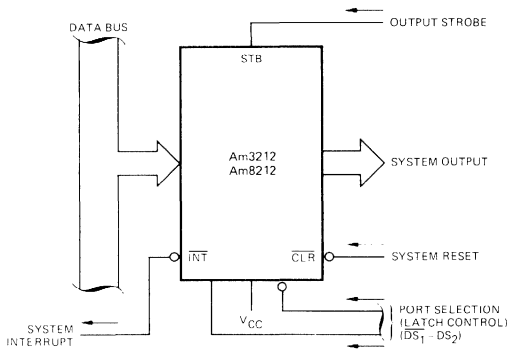
Interrupt Instruction Port

The Am3212 • Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).



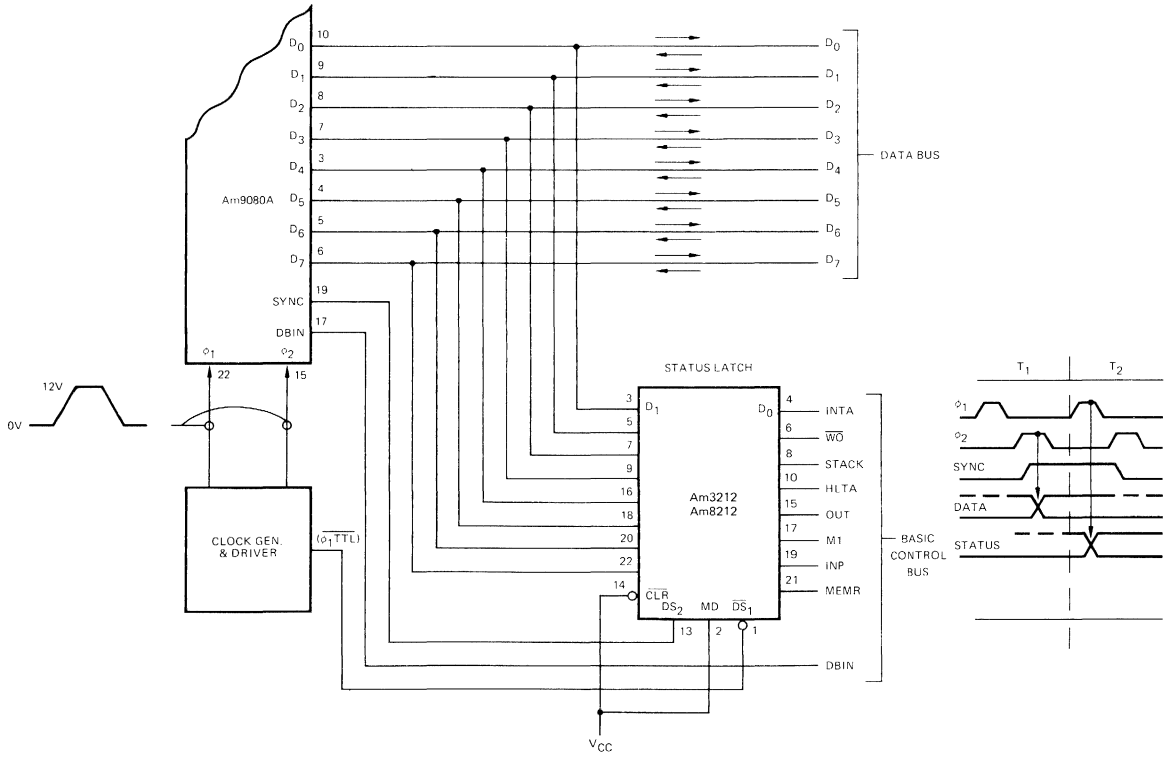
Output Port (With Hand-Shaking)

The Am3212 • Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of date. The selection of the port comes from the device selection logic. ($\overline{DS_1} \cdot DS_2$).



Am9080A Status Latch

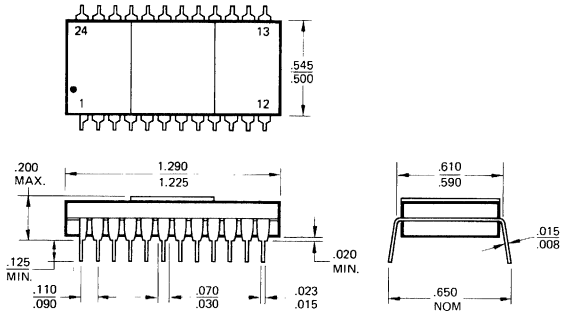
The input to the Am3212 • Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am3212 • Am8212. The mode signal is tied high so that the output on the latch is active and evabled all the time.



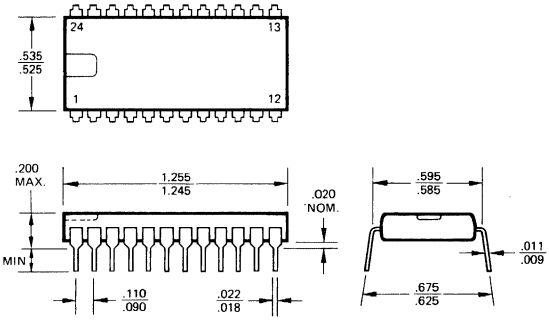
PHYSICAL DIMENSIONS

Dual-In-Line

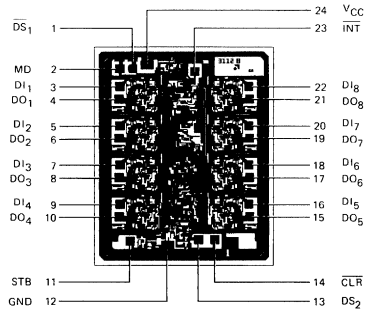
Hermetic



Molded



Metallization and Pad Layout



DIE SIZE
0.091" X 0.112"

Chapter 7
Am8255/9555 PERIPHERAL INTERFACE

Early 8080A/9080A microcomputer systems used the 8212 Data Buffer in order to generate 8-bit parallel I/O. As compared to logic available at the time, the 8212 was an effective device; by today's standards, however, it is often difficult to use. The 8255 Programmable Peripheral Interface (PPI) device has become a standard part for generating parallel data input and output. With the advent of the Am9080A enhancement of the 8080A, the Am9555 PPI is now available and may be used wherever appropriate when generating parallel data input and output.

Just as the Am9080A microprocessors are pin compatible with the 8080A, yet have significant enhancements, so the Am9555 PPI can be used wherever an 8255 currently exists. The Am9555 PPI has additional features which the 8255 PPI does not have, but these additional features represent strict enhancements, which in no way interfere with the Am9555 acting as an exact replacement for the 8255.

The Am9555 Programmable Peripheral Interface circuit provides flexible, parallel I/O capability for the Am9080A, and most other 8-bit microprocessors.

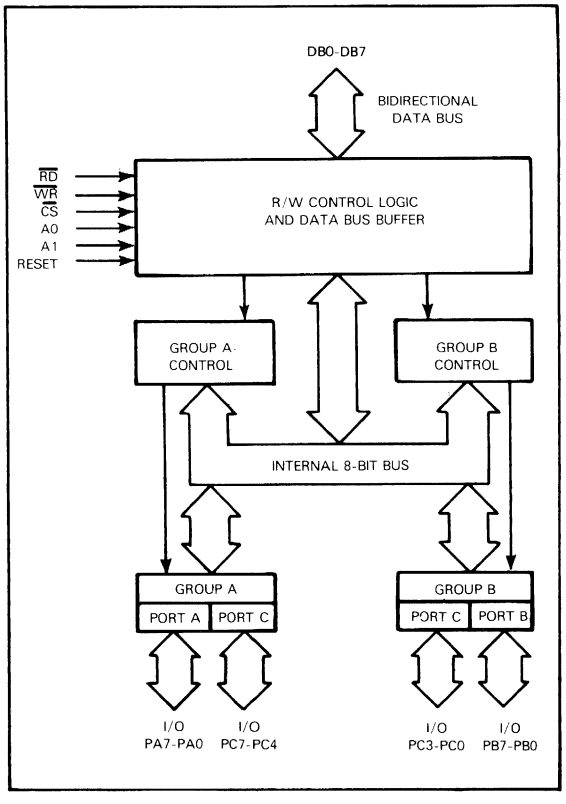


FIGURE 7-1 Am9555 BLOCK DIAGRAM

Significant features of the Am9555 are:

- 24 bits of Input/Output, divided into three 8-bit ports.
- Uni- or bidirectional I/O, with or without handshaking control signals.
- Output drivers for any eight of the I/O signals provide 2 mA of source current.

Am9555 FUNCTIONAL DESCRIPTION

A block diagram for the Am9555 is shown in Figure 7-1. The bidirectional Data Bus interfaces the Am9555 with an Am9080A microprocessor, and handles all information transfers between the two.

There are four destinations for information written to the Am9555. These are I/O ports A, B, and C, and a Control Register. The Control Register is contained in the Read/Write Control Logic. The Am9080A microprocessor may read from, or write to I/O Port A, B, or C. The Control Register is a write only location and cannot be read.

Am9555 INTERFACE SIGNALS

The Connection Diagram and the assignments of I/O connections to the Am9555 are shown in Figure 7-2. Descriptions of the I/O connections and their functions follow.

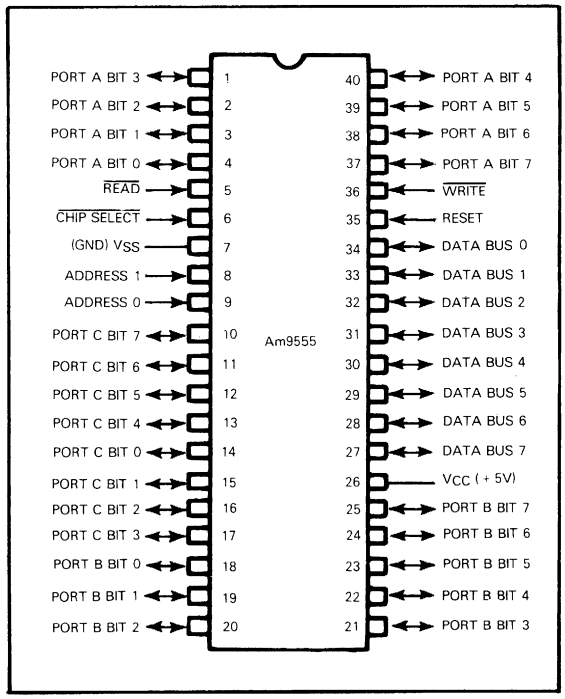


FIGURE 7-2 Am9555 CONNECTION DIAGRAM

Input/Output

Data Bus (DB0 - DB7, Bidirectional)

The Data Bus connections, DB0 through DB7, form the bidirectional Data Bus connecting the Am9555 with the microprocessor system. Information is transferred between the Am9555 and the Am9080A microprocessor via the Data Bus.

I/O Port A (PA0 - PA7, Bidirectional)

These eight pins constitute I/O Port A. They may be configured to serve as an input, an output, or a bidirectional parallel data port. Input-only and output-only pins cannot coexist within I/O Port A.

I/O Port B (PB0 - PB7, Bidirectional)

I/O Port B may be configured as an input or an output port; it is designed to support bidirectional parallel data. Also, input-only and output-only pins cannot coexist within I/O Port B.

I/O Port C (PC0 - PC7, Bidirectional)

I/O Port C may be accessed as a single 8-bit parallel unit, or as two separate 4-bit parallel units. When either I/O Port A or I/O Port B is configured as an I/O port with handshaking, then selected I/O Port C pins provide the handshaking signals.

Input

Chip Select and Address ($\overline{CS}$, A0, A1, Input)

There are four addressable locations within the Am9555 PPI: I/O Ports A, B and C plus a Control Register. $\overline{CS}$ must be low in order to select the PPI. Once selected, A0 and A1 identify the addressable location which will be accessed, as defined in Table 7-1.

TABLE 7-1 Am9555 CONTROL LINE OPERATION

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	Transfer Port A to Data Bus
0	1	0	1	0	Transfer Port B to Data Bus
1	0	0	1	0	Transfer Port C to Data Bus
1	1	0	1	0	Non-functional Condition
0	0	1	0	0	Transfer Data Bus to Port A
0	1	1	0	0	Transfer Data Bus To Port B
1	0	1	0	0	Transfer Data Bus to Port C
1	1	1	0	0	Data Bus→Control
X	X	X	X	1	Data Bus Output Off

$\overline{CS}$, A0 and A1 will usually be derived from the low order eight Address Bus lines from the microprocessor, if the Am9555 is accessed using I/O instructions. $\overline{CS}$, A0 and A1 will usually be derived from the full Address Bus if the Am9555 is accessed using memory reference instructions. $\overline{RD}$ and $\overline{WR}$ signals determine whether the Am9555 will be accessed by I/O instructions as four I/O locations, or by memory reference instructions as four memory locations.

Read and Write (RD, $\overline{WR}$, Input)

These two control signals determine whether data will be read from, or written into an addressed location within a selected Am9555 PPI. When $\overline{WR}$ is pulsed low, data entering via the bidirectional Data Bus will be written into a selected location. When $\overline{RD}$ is pulsed low, the contents of the selected location will be output to the bidirectional Data Bus. Note that the Control Register is a write-only location. Thus, accessing the Control Register while $\overline{RD}$ is low is an invalid operation.

$\overline{RD}$ and $\overline{WR}$ will usually be connected to control signals output by the Am8228 System Controller. If the Am9555 is being accessed as four I/O ports via I/O instructions, then $\overline{RD}$ will be connected to $\overline{I/OR}$ and $\overline{WR}$ will be connected to $\overline{I/OW}$. If the Am9555 is being accessed via memory reference instructions, as four memory locations, then $\overline{RD}$ will be connected to $\overline{MEMR}$ and $\overline{WR}$ will be connected to $\overline{MEMW}$.

Reset (Reset, Input)

The Reset connection provides a system reset to the Am9555 PPI. When the Reset line is activated with a high level signal, all internal registers are cleared and all three I/O ports (A, B, and C) are configured to function in their input mode only. Thus, peripheral circuits may read information into the Am9555, but no information may be written from the Am9555 to peripheral circuits without writing appropriate control codes to modify the configuration of I/O ports.

SELECT LOGIC

Figure 7-3 shows how an Am9080A system can access six or less Am9555 PPIs without incorporating additional Address Bus decoding logic using I/O instructions. Since each Am9555 has three I/O ports, the configuration in Figure 7-3 provides a maximum of 18 I/O ports. Table 7-2 gives the unique hexadecimal addresses for each of the possible 18 I/O ports. Notice in Figure 7-3 that each of the Am9555 chip selects ($\overline{CS}$) is attached to a separate Address Bus line. The two low order Address Bus lines are attached to the A0 and A1 inputs of each PPI. When any address other than those shown in Table 7-2 is used in an IN or OUT instruction, care must be exercised as more than one chip select will be generated.

When more than 18 I/O ports are needed in an Am9080A system, chip select decode logic must be added. A maximum of 64 PPI chips can be connected to the system if they are accessed using I/O instructions. Note that 64 Am9555 devices provide 192 I/O ports. Figure 7-4 shows chip select decoding accomplished using the Am25LS138 one-of-eight decoder.

TABLE 7-2 HEX PORT ADDRESSES FOR THE SYSTEM OF FIGURE 7-3

Am9555 UNIT 1	I/O PORT A	I/O PORT B	I/O PORT C	CONTROL REGISTER
1	F8	F9	FA	FB
2	F4	F5	F6	F7
3	EC	ED	EE	EF
4	DC	DD	DE	DF
5	BC	BD	BE	BF
6	7C	7D	7E	7F

OPERATING MODES

Parallel data may be transferred via I/O ports of the Am9555 PPI using one of three modes. These three modes are described next in conjunction with Table 7-3 and Figure 7-5.

Mode 0 — Simple Input Or Output

In the simplest case, parallel data is either input or output,

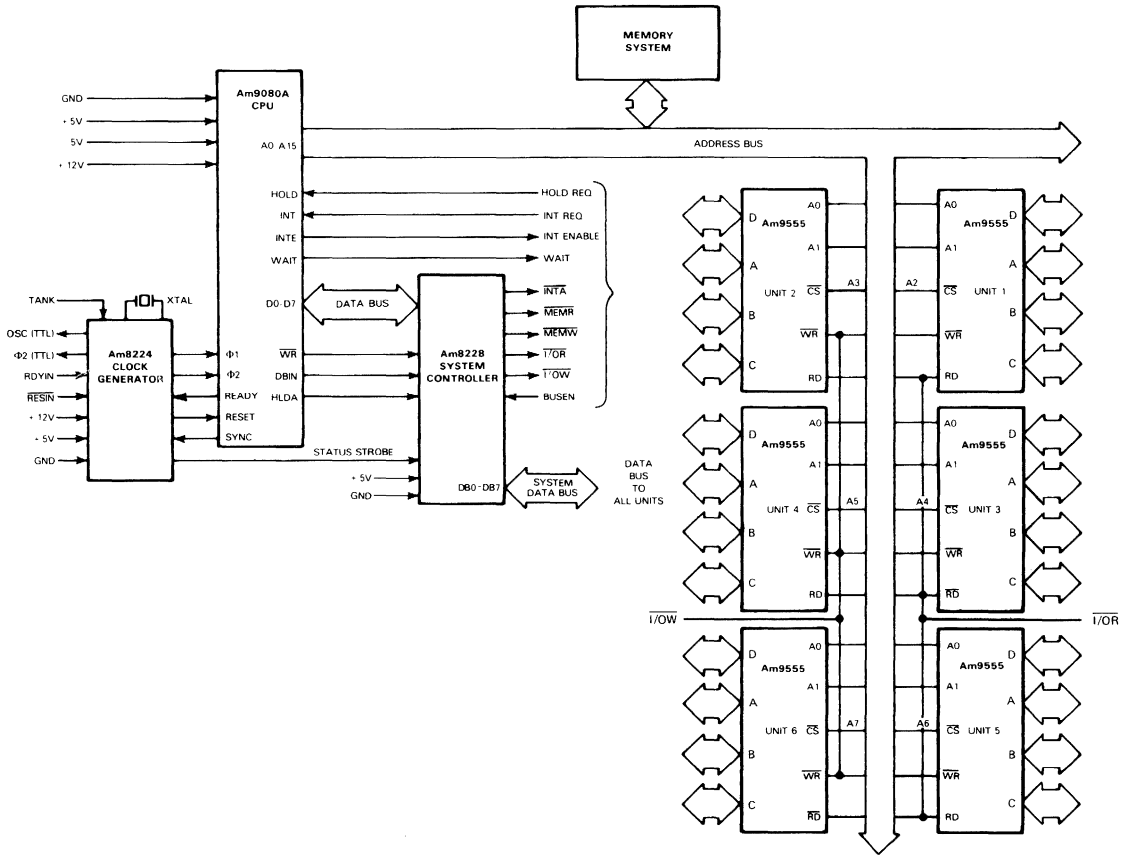
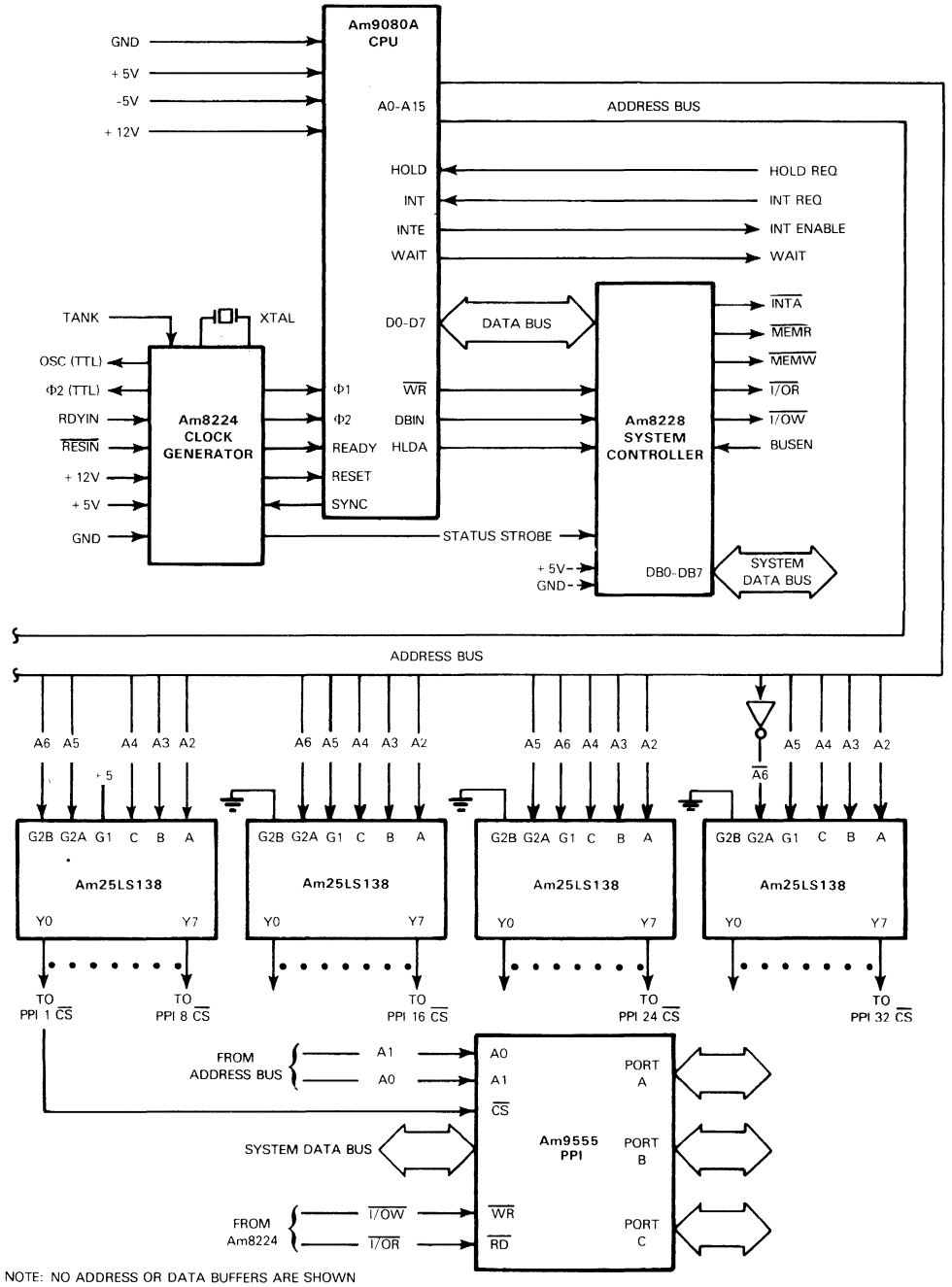


FIGURE 7-3 MAXIMUM Am9555 CONNECTIONS WITHOUT RESORTING TO DEVICE SELECT LOGIC



NOTE: NO ADDRESS OR DATA BUFFERS ARE SHOWN

FIGURE 7-4 Am9080A MICROCOMPUTER I/O SYSTEM WITH ADDRESS DECODING FOR 32 I/O PORTS

TABLE 7-3 ALLOWED Am9555 I/O PORT ASSIGNMENTS AND PIN FUNCTIONAL ASSIGNMENTS

PORT A		PORT B		PORT C							
Mode	Assignment	Mode	Assignment	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0	I or O	0	I or O	I or O	I or O	I or O	I or O	I or O	I or O	I or O	I or O
0	I or O	1	I	I or O	I or O	I or O	I or O	I or O	$\overline{STB}$ (B)	IBF (B)	INTR (B)
0	I or O	1	O	I or O	I or O	I or O	I or O	I or O	$\overline{ACK}$ (B)	$\overline{OBF}$ (B)	INTR (B)
1	I	0	I or O	I or O	I or O	IBF (A)	$\overline{STB}$ (A)	INTR (A)	I or O	I or O	I or O
1	O	0	I or O	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	I or O	I or O	INTR (A)	I or O	I or O	I or O
1	I	1	I	I or O	I or O	IBF (A)	$\overline{STB}$ (A)	INTR (A)	$\overline{STB}$ (B)	IBF (B)	INTR (B)
1	I	1	O	I or O	I or O	IBF (A)	$\overline{STB}$ (A)	INTR (A)	$\overline{ACK}$ (B)	$\overline{OBF}$ (B)	INTR (B)
1	O	1	I	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	I or O	I or O	INTR (A)	$\overline{STB}$ (B)	IBF (B)	INTR (B)
1	O	1	O	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	I or O	I or O	INTR (A)	$\overline{ACK}$ (B)	$\overline{OBF}$ (B)	INTR (B)
2	I/O	0	I	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	IBF (A)	$\overline{STB}$ (A)	INTR (A)	I or O	I or O	I or O
2	I/O	0	O	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	IBF (A)	$\overline{STB}$ (A)	INTR (A)	I or O	I or O	I or O
2	I/O	1	I	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	IBF (A)	$\overline{STB}$ (A)	INTR (A)	$\overline{STB}$ (B)	IBF (B)	INTR (B)
2	I/O	1	O	$\overline{OBF}$ (A)	$\overline{ACK}$ (A)	IBF (A)	$\overline{STB}$ (A)	INTR (A)	$\overline{ACK}$ (B)	$\overline{OBF}$ (B)	INTR (B)

I means input only.
O means output only
I or O means input or output, but not both
I/O means bidirectional

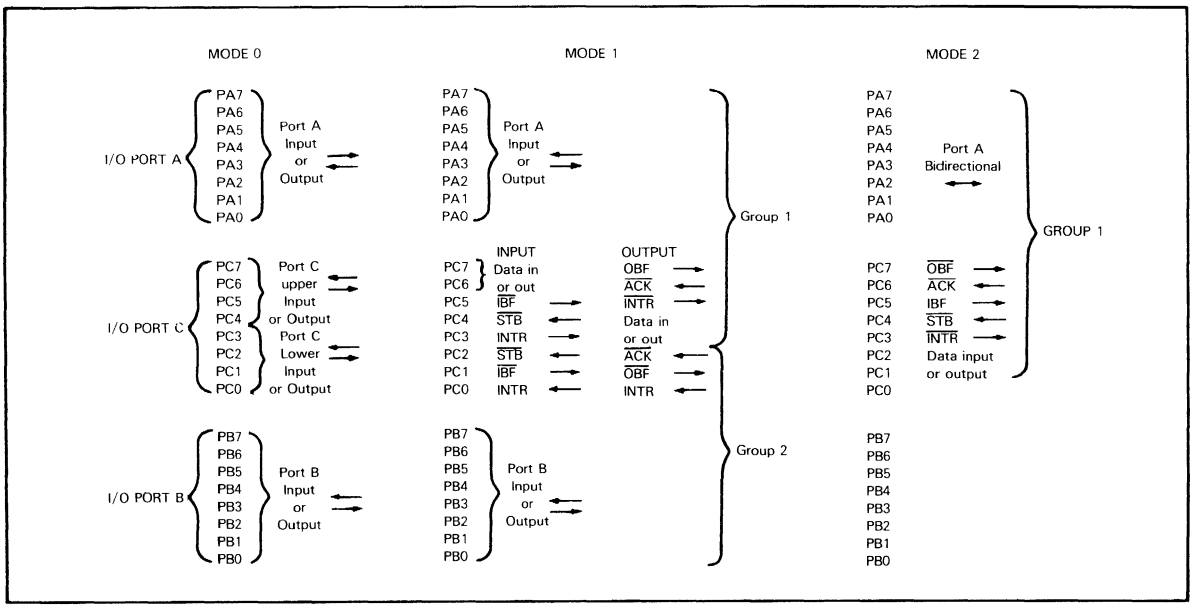


FIGURE 7-5 PIN ASSIGNMENTS FOR Am9555 I/O PORTS OPERATING IN MODES 0, 1 AND 2

without accompanying control signals. This type of operation is available in the Am9555 in Mode 0.

In Mode 0, I/O Ports A and B are treated as separate 8-bit parallel entities; I/O Port C is treated as two separate 4-bit entities. Ports A and B can be defined either as input or output ports. Each half of I/O Port C can be separately specified as an input or an output 4-bit port.

As defined in Table 7-3 ports may be specified as inputs and outputs in any combination; however, in Mode 0 no bidirectional I/O ports are allowed. Input and output signals cannot be mixed within a single I/O port, with the exception of I/O Port C, whose upper and lower halves may be separately assigned to input and output.

Figure 7-6 illustrates Mode 0 input and output timing.

Mode 1 — Input Or Output With Handshaking Control

The first enhancement over simple parallel data transfer is provided by Mode 1, which uses selected pins of I/O Port C to generate control signals accompanying the parallel data transfers. These control signals are referred to as handshaking controls.

Figure 7-7 illustrates the flow of handshaking signals that accompany parallel data input. External logic must be able to indicate that new data has been placed at an input port. An input strobe signal ($\overline{STB}$) is provided for this purpose.

In order to avoid prematurely inputting new data and overwriting prior data which the microprocessor has not yet had time to access, external logic must be told when the data it has

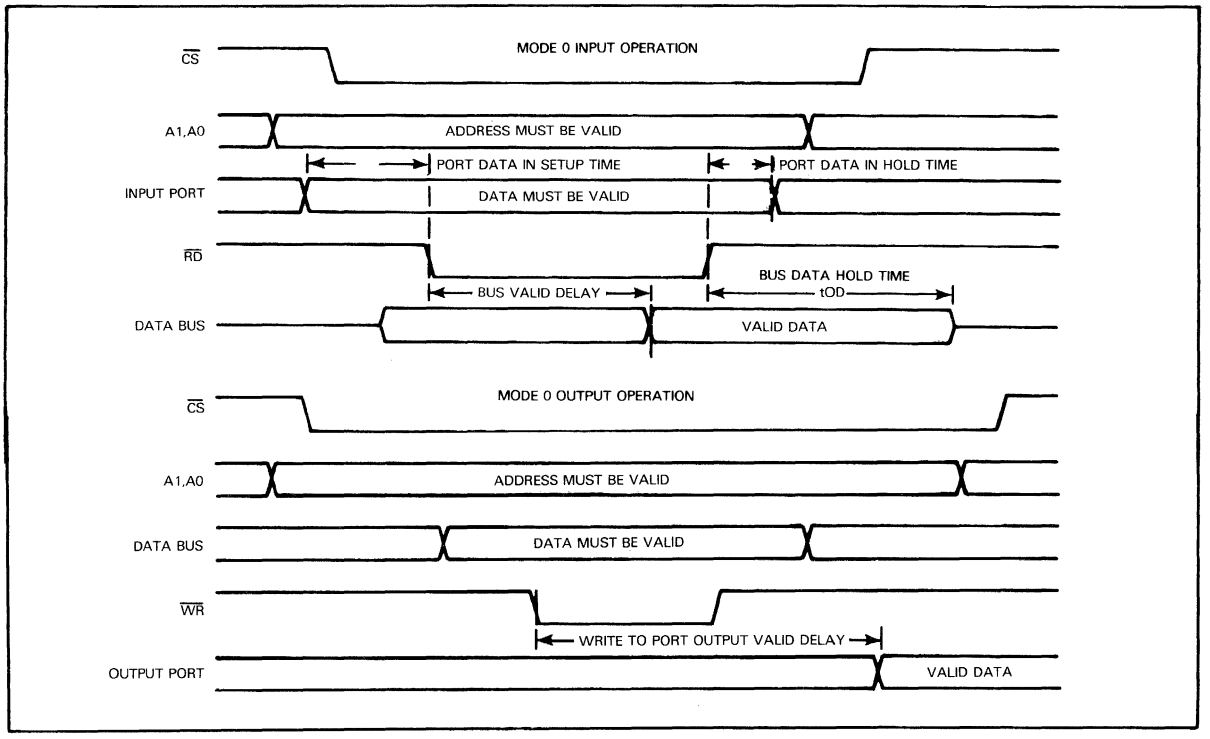


FIGURE 7-6 MODE 0 INPUT AND OUTPUT TIMING

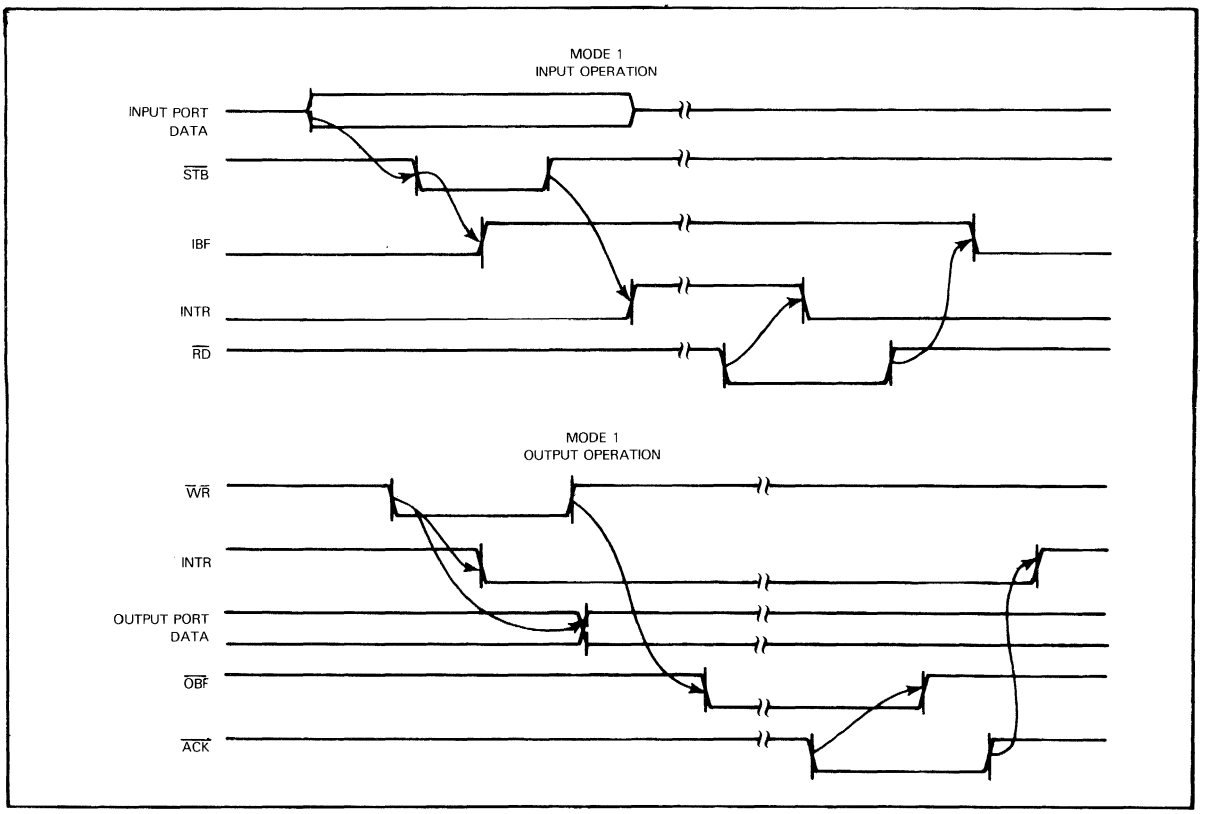


FIGURE 7-7 MODE 1 HANDSHAKING

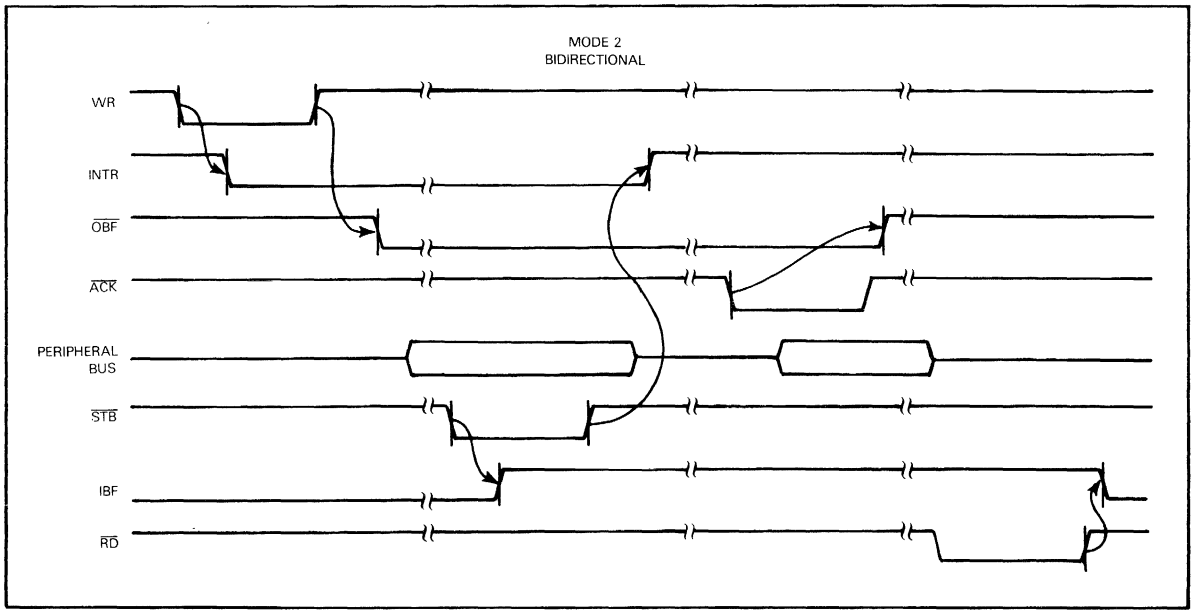


FIGURE 7-8 MODE 2 HANDSHAKING

presented to an I/O port has been read. Output control signal IBF serves this purpose. As soon as $\overline{STB}$ pulses low, IBF is output high. IBF remains high until the trailing edge of the $\overline{RD}$ pulse, which is the control strobe output by the microprocessor when reading data from the I/O port.

Parallel I/O is frequently handled by interrupt driven programs. Interrupt request signal INTR is output high during the time interval between external logic transmitting data to an I/O port and the CPU reading this data. Thus, while there is data at the I/O port waiting to be read, an interrupt request will be active.

Three similar control signals accompany data being output with handshaking. Timing is illustrated in Figure 7-7. As soon as the CPU writes data to an I/O port in Mode 1, $\overline{OBF}$ is output low, telling external logic that data at the output port is ready to be read. When external logic reads the data, it pulses $\overline{ACK}$ low as an acknowledge input and this causes $\overline{OBF}$ to return high. Thus external logic has acknowledged the presence of output data.

In the event that the program which controls parallel I/O operations is interrupt driven, an interrupt will be requested via INTR as soon as external logic completes acknowledgement of data output; the interrupt request will remain active until the CPU outputs the next data byte.

Mode 2 — Bidirectional Data Transfer

The PPI also allows bidirectional parallel data transfer via I/O Port A. This is referred to as Mode 2. Timing for Mode 2 data transfer is illustrated in Figure 7-8. Handshaking signals are a simple combination of Mode 1 input and output handshaking signals which have already been described.

Mode And Port Combinations

Within the limits of signal conflicts, I/O ports can be operated in any combination of modes. Table 7-3 identifies the combinations which are physically feasible. Any combination identified in Table 7-3 is allowed.

Note that in Modes 1 and 2, certain I/O Port C pins are not used as input or output controls. These pins may be used for simple data input or output.

PROGRAMMING

The three I/O ports are each accessed as a single data entity. I/O Port C, which may have its two halves assigned separately to input and/or output, or may have individual pins assigned to support handshaking control signals, is also accessed as a single, 8-bit entity when reading or writing data; in addition, control codes allow single bits of I/O Port C to be set or reset.

The various I/O port modes are specified by writing appropriate control words to the Control Register. There are two types of control word:

- Mode control words, identified by 1 in the high order bit.
- Selective control of I/O Port C bits, identified by 0 in the high order bit.

The mode control word is used to define individual I/O port modes. The control word format is given in Figure 7-9. Observe that the control word defines whether I/O Port A, B, C

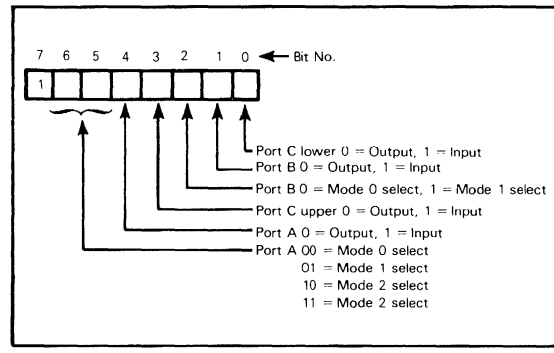


FIGURE 7-9 Am9555 CONTROL WORD FORMAT

upper and C lower will act as an input or an output port. Port B may be defined as operating in Mode 0 or Mode 1, while Port A may be defined as operating in Mode 0, Mode 1 or Mode 2.

There are some potentials for conflict in the control word as illustrated. Conflicts are resolved as follows:

1) If I/O Port A is specified as operating in Mode 2, then bidirectional operation is assumed. It does not matter whether I/O Port A has been defined as an input or an output via control word bit 4.
2) If either Port A or Port B is operating in a mode other than 0, then selected Port C pins must serve as control signals. Those Port C pins which are not serving as control signals will support independent input or output, as specified by control word bits 3 and 0.

When the high order bit of the control word is 0, the remaining bits are used to selectively set or reset single Port C pins. Figure 7-10 illustrates the control word when being used in this fashion. Any Port C pin that is serving as an output signal may be set or reset using a control word as illustrated in Figure 7-10.

ELECTRICAL SPECIFICATIONS

In the 9555, any 8 of the 24 output pins (8 of 16 for the 8255) from I/O Ports A, B or C may be used to provide a source current drive capability of 2 milliamps (1 for the 8255) at 1.5 volts. This feature provides easier interface to relay drivers, LED multiplex displays and other types of circuits requiring a higher source current capability from the I/O port. These and other differences between the 8255 and 9555 specifications are shown in the data sheet which follows.

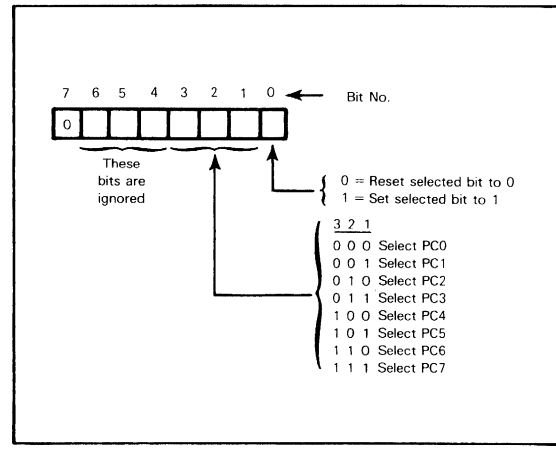


FIGURE 7-10 Am9555 PORT C CONTROL WORD FORMAT

Am9555

Programmable Peripheral Interface

DISTINCTIVE CHARACTERISTICS

- Direct replacement for Intel C8255
- High speed version available
- Minimum output source current 2mA at 1.5V
- Minimum output sink current 3.2mA at 0.4V
- 24 programmable I/O pins
- Programmable modes of operation
- Bit set/reset capability
- Commercial and military temperature range operation
- Ion-implanted N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

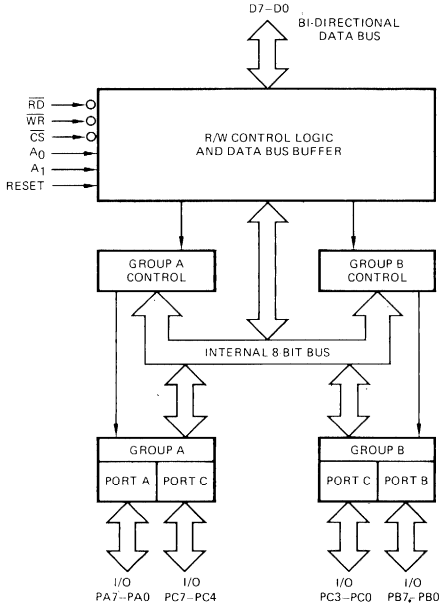
GENERAL DESCRIPTION

The Am9555 is a high-speed programmable peripheral interface device. It can be programmed for several modes of operation allowing simplified interfacing between microprocessor and peripherals.

The 24 I/O pins are programmable to be either inputs or outputs. Outputs provide high source current on any eight of the twenty-four pins and high sink current on all pins. All signal levels are identical to TTL specifications.

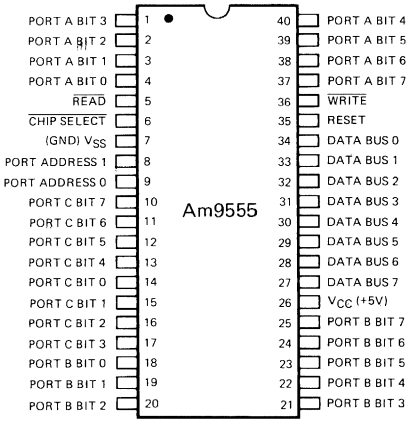
Chip Select ($\overline{CS}$) input used in conjunction with the port address A0 and A1 allows communication between processor and Am9555 ports. Data is written or read from a specific port by using the Write input, $\overline{WR}$, or Read input, $\overline{RD}$.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	FOR USE WITH			
		Am9080A C8080A	Am9080A-2 C8080A-2	Am9080A-1 C8080A-1	Am9080A-4
Hermetic DIP	$0°C \leq T_A \leq +70°C$	Am9555DC C8255	Am9555DC	Am9555-4DC	Am9555-4DC
	$-55°C \leq T_A \leq +125°C$	Am9555DM	Am9555DM		

INTERFACE SIGNAL DESCRIPTION

The Am9555 uses an 8-bit bi-directional data bus to exchange data with an associated processor. Internally, information can be transferred between the data bus and the control register or the two output port groups, A and B. Group A consists of the 8-bit port A and the 4 high order bits of Port C. Group B consists of the 8-bit Port B and the 4 lower order bits of Port C.

Port A — Provides an output latch, an input latch, an input buffer or a bi-directional bus for eight data bits.

Port B — Provides an output latch, an input latch or an input buffer for eight data bits.

Port C — Operates as an output latch for eight bits, an input buffer for eight bits or as two separate four bit control ports used in conjunction with Ports A and B.

The specific function of each port is determined under program control.

Port Address 0
Port Address 1
(A0, A1) — These two inputs allow selection, by the processor, of a specific port or the control word register when used with the Read Input, Write Input and the Chip Select.

Port A Selection: A1 = 0, A0 = 0
Port B Selection: A1 = 0, A0 = 1
Port C Selection: A1 = 1, A0 = 0
Control Register Selection: A1 = 1, A0 = 1
(Reading the Control Register is prohibited.)

Read ($\overline{RD}$) — The active low Read input provides control to read data from the Am9555 onto the Data Bus.

Write ($\overline{WR}$) — The active low Write input provides control to write data into the Am9555 from the Data Bus.

Chip Select ($\overline{CS}$) — The active low Chip Select input allows the Am9555 to be individually addressed. When Chip Select is at a high level, the Data Bus drivers go to a high impedance state and data bus transfers are inhibited.

Reset — All internal registers are cleared and the ports are set to the high impedance input mode when a high level is presented to the Reset input and during mode selection. Initialization must include setting the status flip-flops to their required logic level.

Data Bus — The eight-bit Data Bus is used for transferring data or programming information between the associated processor and the Am9555.

PROGRAMMING THE Am9555

In order to program the Am9555, the programmable internal control functions are selected by the processor. This is accomplished by performing a write operation in the programming mode (A1 = A0 = $\overline{RD}$ = 1 and $\overline{CS}$ = $\overline{WR}$ = 0). Under these conditions, the data bus information is written into one of two areas of control. A programmable register is provided for the control of the operation mode of each group and Input/Output selection of ports. Other logic controls the Bit Set/Reset capability in Port C. Bit 7 of the Data Bus selects which control is being programmed.

If Bit 7 = 1, the Operation Control Register is selected.
If Bit 7 = 0, the Bit Set/Reset Function is selected.

The definition of bits 0 through 6 depends on the particular control mode selected.

Operation Control

1	Group A Control				Group B Control		
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Group A Control: (Bit 6, 5, 4, 3)
Bits 6 & 5 determine the mode of operation:

For Mode 0, Bit 6 = 0, Bit 5 = 0
For Mode 1, Bit 6 = 0, Bit 5 = 1
For Mode 2, Bit 6 = 1, Bit 5 = X

A detailed description of the modes of operation can be found on the next page.

Bit 4 determines whether Port A will be inputs (1) or outputs (0).
Bit 3 determines whether the 4 high-order bits of Port C will be inputs (1) or outputs (0).

Group B Control: (Bits 2, 1, 0)
Bit 2 determines the mode of operation:

For Mode 0, Bit 2 = 0
For Mode 1, Bit 2 = 1

Bit 1 determines whether Port B will be inputs (1) or outputs (0).
Bit 0 determines whether the 4 low-order bits of Port C will be inputs (1) or outputs (0).

Bit Set/Reset

0	X	X	X	Bit Selection			Set/ Reset
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Bit Selection:
Bits 3, 2 & 1 specify the bit in Port C that will be set or reset.

Port C Bit Selected	Control Bit		
	3	2	1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Set/Reset:
Bit 0 determines whether the selected bit in Port C is set (1) or reset (0).

Bits 6, 5 & 4 are not assigned a function and can be either a '1' or '0'.

MODES OF OPERATION

The Am9555 can be programmed in a variety of ways to meet the requirements of interfacing to a multitude of peripherals. To accomplish this, three basic modes of operation are provided.

MODE 0 is a basic interface allowing the 24 I/O pins of the three ports to be programmed, in four sets, as inputs or outputs. The four sets are the 8-bit Port A, 8-bit Port B, high-order 4 bits of Port C and the low-order 4 bits of Port C. Data is latched on an output port but is not latched on an input port. During inputs the data bus will effectively follow the input data while $\overline{RD} = 0$. With four sets there are sixteen combinations of input and output arrangements. These combinations are selected via the programmable Operation Mode Register in the Am9555, using Bits 0, 1, 3 and 4 of the data bus byte.

Programming for Mode 0

$\overline{CS} = \overline{WR} = 0$ A1 = A0 = $\overline{RD}$ = 1 Data Bus Bit 7 = 1
Data Bus Bit 6 = Bit 5 = Bit 2 = 0

Data Bus Bit				Port A	Port C (PC7–PC4)	Port B	Port C (PC3–PC0)
4	3	1	0				
0	0	0	0	Out	Out	Out	Out
0	0	0	1	Out	Out	Out	In
0	0	1	0	Out	Out	In	Out
0	0	1	1	Out	Out	In	In
0	1	0	0	Out	In	Out	Out
0	1	0	1	Out	In	Out	In
0	1	1	0	Out	In	In	Out
0	1	1	1	Out	In	In	In
1	0	0	0	In	Out	Out	Out
1	0	0	1	In	Out	Out	In
1	0	1	0	In	Out	In	Out
1	0	1	1	In	Out	In	In
1	1	0	0	In	In	Out	Out
1	1	0	1	In	In	Out	In
1	1	1	0	In	In	In	Out
1	1	1	1	In	In	In	In

MODE 1 is a strobed input/output interface utilizing Port A with the high-order five bits of Port C and Port B with the low-order three bits of Port C. The two sections of Port C are available for communication between the associated port and attached peripheral. Ports A and B can be programmed independently to be either outputs or inputs and either function allows the data to be latched in the Am9555.

Interrupt Enable/Disable flip-flops (INTE) are available on Port C. The access to INTE for Port A and Port B, respectively, is via Bit 4 and Bit 2 during an input function and Bit 6 and Bit 2 during an output function. These bits are programmed via the Bit Set/Reset Logic, set/reset = 1, enables the interrupt and set/reset = 0, disables the interrupt.

Communication between port and peripheral is accomplished with three control signals for an input operation and three control signals for an output operation. Specific bits in Port C are assigned the functions as shown in the following table.

Control Function		Associated Port A	Associated Port B
INPUT	$\overline{STB}$	PC4	PC2
	IBF	PC5	PC1
	INTR	PC3	PC0
OUTPUT	$\overline{OBF}$	PC7	PC1
	$\overline{ACK}$	PC6	PC2
	INTR	PC3	PC0

For an input operation:

Strobe Input ($\overline{STB}$): loads data into input latch during $\overline{STB} = 0$.

Input Buffer Full (IBF): acknowledges that the data has been loaded. IBF is set when $\overline{STB}$ goes low and reset by $\overline{RD} = 0$.

Interrupt Request (INTR): if the INTE flag has been enabled and the IBF = 1, the INTR signal will go to a high level when STB returns to a high.

The INTR signal can be connected directly to the INT input on the processor, allowing an interrupt to be generated when data is loaded into the port. INTR is reset when the port receives the $\overline{RD}$ signal from the processor.

For an output operation:

Output Buffer Full ($\overline{OBF}$): a flag that indicates that the processor has loaded data into a particular port ($\overline{OBF} = 0$). $\overline{OBF}$ will be activated by the trailing edge of $\overline{WR}$ and deactivated by the leading edge of the $\overline{ACK}$ signal from the peripheral device.

Acknowledge ($\overline{ACK}$): having read the data from the port, the peripheral device will respond to the Am9555 with an Acknowledge signal, $\overline{ACK}$. This signal will be active when $\overline{ACK} = 0$.

Interrupt Request (INTR): this output can be used to interrupt the processor indicating that the peripheral device has received the data. If the INTE flag has been enabled and the OBF = 1, the INTR signal will be set by $\overline{ACK}$ going high and reset by $\overline{WR}$ going to a low level.

MODE 2 allows port A to be used as an eight-bit bi-directional bus. Port A inputs and outputs are latched. 5 bits of Port C are used for control between the peripheral device and the Am9555.

An Interrupt Enable/Disable flip-flop (INTE) is available for programming via Bit 6 for output operations and Bit 4 for input operations.

Communication between port and peripheral is performed via the same pins of Port C as those associated with Port A operation in Mode 1.

$\overline{STB}$, IBF, $\overline{OBF}$, and INTR functions are identical to those described for Mode 1.

$\overline{ACK}$ being activated enables the three-state output buffer on Port A allowing data to be transferred to the peripheral device. At all other times, the output buffer will be in the high impedance condition.

In Modes 1 and 2 the Port C status and control bits can be tested by a read operation accessing Port C. Not all the bits of Port C are assigned to control or status functions. The unassigned bits can be programmed as Inputs or Outputs as follows:

If programmed as inputs, the pins can be read by a read operation addressing Port C.

If programmed as outputs, the bits in Group A (PC7-PC4) must be individually accessed using the Bit Set/Reset function. Group B bits (PC3-PC0) can be accessed either by writing to Port C or by use of the Bit Set/Reset capability.

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9555DC C8255 Am9555-4DC	$0°C \leq T_A \leq +70°C$	+5.0V ± 5%	0V
Am9555DM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions	C8255 Min.	C8255 Typ.	C8255 Max.	Am9555 Min.	Am9555 Typ.	Am9555 Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$				**2.4**			Volts
		$I_{OH} = -100\mu A$ (DB) $I_{OH} = -50\mu A$	2.4						
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$						**0.4**	Volts
		$I_{OL} = 1.6mA$			0.4				
V_{IH}	Input HIGH Voltage		2.0			2.0			Volts
V_{IL}	Input LOW Voltage				0.8			0.8	Volts
I_{LI}	Input Load Current							10	μA
I_{OH} (Note 3)	Darlington Drive Current	$V_{OH} = 1.5V$, $R_{EXT} = 390\Omega$		2.0		**2.0**			mA
I_{LO}	Output Leakage Current							100	μA
I_{CC}	V_{CC} Supply Current	$T_A = +25°C$		40				**40**	mA
		$T_A = 0°C$						50	
		$T_A = -55°C$						65	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 2)

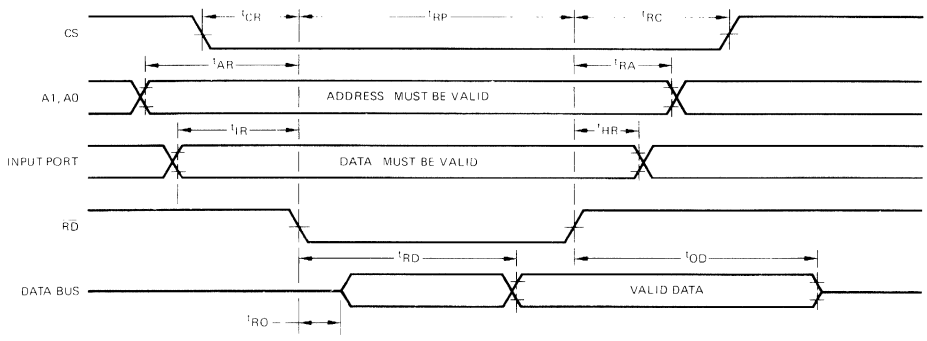
Parameter	Description	C8255 Min.	C8255 Max.	Am9555DC Am9555DM Min.	Am9555DC Am9555DM Max.	Am9555-4DC Min.	Am9555-4DC Max.	Units
t_{AD}	$\overline{ACK}$ low to output ON delay (mode 2)		500		500		400	ns
t_{AK}	$\overline{ACK}$ pulse width	500		500		250		ns
t_{AN}	$\overline{ACK}$ high to INTR high delay		500		500		400	ns
t_{AO}	$\overline{ACK}$ low to $\overline{OBF}$ low delay		500		500		400	ns
t_{AR}	Port address to $\overline{RD}$ set-up time	50		50		50		ns
t_{AW}	Port address to $\overline{WR}$ set-up time	20		**0**		0		ns
t_{CR}	$\overline{CS}$ low to $\overline{RD}$ set-up time	50		50		50		ns
t_{CW}	$\overline{CS}$ low to $\overline{WR}$ set-up time	20		**0**		0		ns
t_{DW}	Data bus stable to $\overline{WR}$ set-up time	10		**0**		0		ns
t_{HR}	$\overline{RD}$ to Port input stable hold time	50		**0**		0		ns
t_{IR}	Port input to $\overline{RD}$ low set-up time	50		**0**		0		ns
t_{KD}	$\overline{ACK}$ high to output off delay (mode 2)		300		300		300	ns
t_{OD}	$\overline{RD}$ high to data bus OFF delay	25	150	25	150	25	100	ns
t_{PH}	Peripheral input from $\overline{STB}$ hold time	150		150		150		ns
t_{PS}	Peripheral input to $\overline{STB}$ set-up time	150		150		100		ns
t_{RA}	$\overline{RD}$ high to Address stable hold time	379		**0**		0		ns
t_{RC}	$\overline{RD}$ high to $\overline{CS}$ high hold time	5.0		**0**		0		ns
t_{RD}	$\overline{RD}$ to data bus valid delay		350		**300**		175	ns
t_{RI}	$\overline{RD}$ high to IBF low delay		300		300		200	ns
t_{RN}	$\overline{RD}$ low to INTR low delay		400		400		400	ns
t_{RO}	$\overline{RD}$ low to data bus ON delay			25		25		ns
t_{RP}	$\overline{RD}$ pulse width	430		380		250		ns
t_{SI}	$\overline{STB}$ low to IBF high delay		600		600		400	ns
t_{SN}	$\overline{STB}$ high to INTR high delay		500		500		500	ns
t_{ST}	$\overline{STB}$ pulse width	350		350		250		ns
t_{WA}	$\overline{WR}$ high to Address stable hold time	35		35		35		ns
t_{WB}	$\overline{WR}$ to output valid delay		500		500		450	ns
t_{WC}	$\overline{WR}$ high to $\overline{CS}$ high hold time	35		35		35		ns
t_{WD}	$\overline{WR}$ high to data bus stable hold time	65		65		65		ns
t_{WN}	$\overline{WR}$ low to INTR low delay		600		600		500	ns
t_{WO}	$\overline{WR}$ high to $\overline{OBF}$ low delay		300		300		250	ns
t_{WP}	$\overline{WR}$ pulse width	430		**380**		250		ns

NOTES:

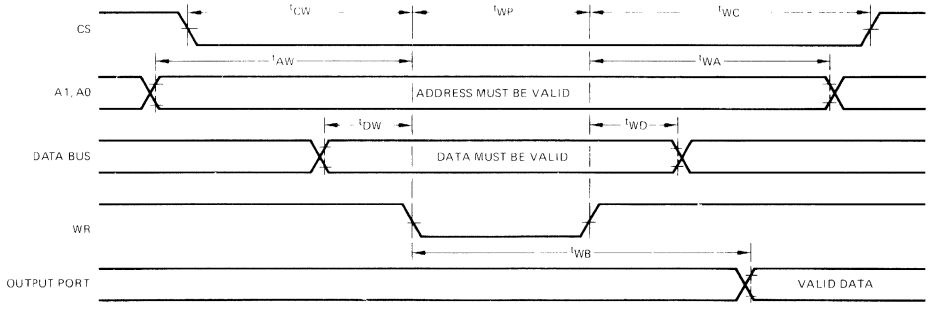
1. Typical values are for $T_A = 25^\circ C$, nominal supply voltage and nominal processing parameters.
2. Test conditions include: transition times $\leq$ 20ns, output loading of 1 TTL gate plus 50pF, input and output timing reference levels 0.8V and 2.0V.
3. Available on any 8 of the 24 I/O pins.
4. Switching parameters are listed in alphabetical order.

SWITCHING WAVEFORMS

MODE 0
INPUT OPERATION

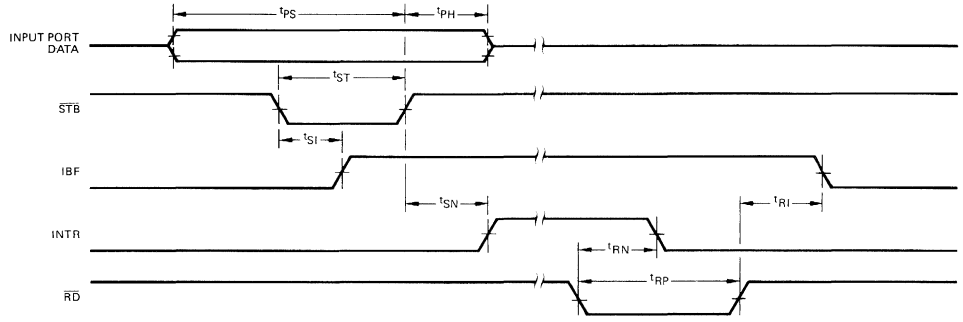


MODE 0
OUTPUT OPERATION

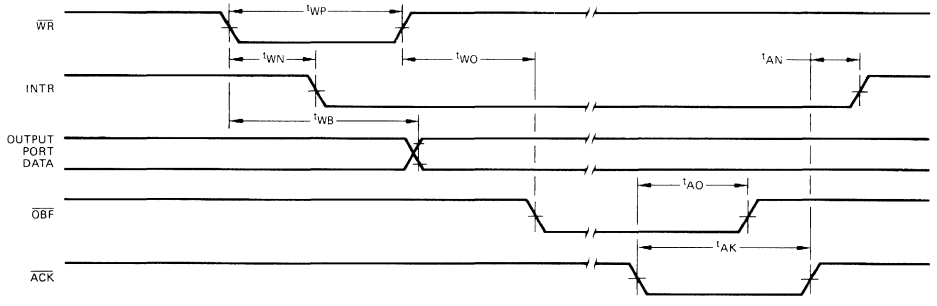


SWITCHING WAVEFORMS (Cont.)

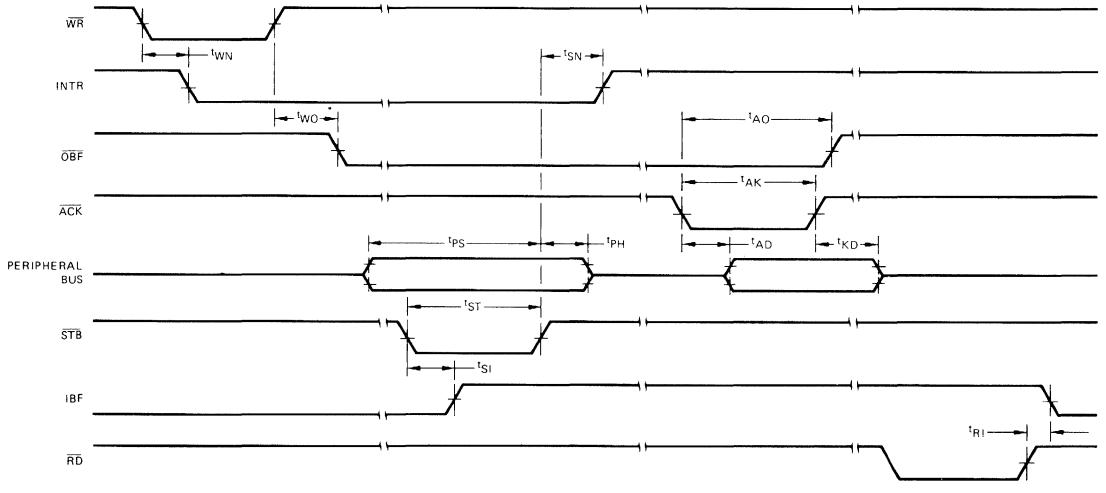
MODE 1
INPUT OPERATION



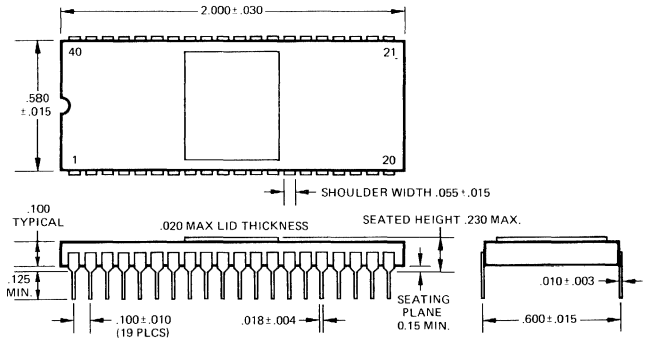
MODE 1
OUTPUT OPERATION



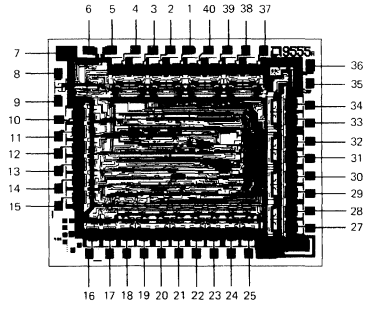
MODE 2
BI DIRECTIONAL



PHYSICAL DIMENSIONS
40-Pin Hermetic DIP



Metallization and Pad Layout



DIE SIZE
0.111" X 0.134"

Chapter 8
Am8251/9551
COMMUNICATION INTERFACE

The Am8251/9551 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed to provide serial communications capability in microprocessor systems. It offers the following features:

- Synchronous or asynchronous serial data transfer
- Half or full duplex signaling
- Data transmitted in character format with five, six, seven or eight bits per character
- Odd, even or no parity bit
- Microprocessor control of modem control signals
- A programmable synchronizing pattern, loaded into the device for transmission when no data is present or for automatic sync detection during receiver operations
- Separate registers for control codes and for data written to transmitter logic (Am9551 only)

FUNCTIONAL DESCRIPTION

The block diagram of the Communication Interface circuit is shown in Figure 8-1.

The circuit consists of the Control Register, Transmitter, Receiver, Modem Control, and Read/Write Control sections.

The Control Register section receives eight-bit control words from the microprocessor; control words are used to establish or change operating modes and control signal levels, for both the Transmitter and the Receiver sections.

The Transmitter section receives eight-bit data bytes from the microprocessor Data Bus, adds formatting bits appropriate to the operating mode selected and transmits the information serially. Appropriate control signals indicate when the Transmit Registers are empty so that the microprocessor may transmit another parallel data byte.

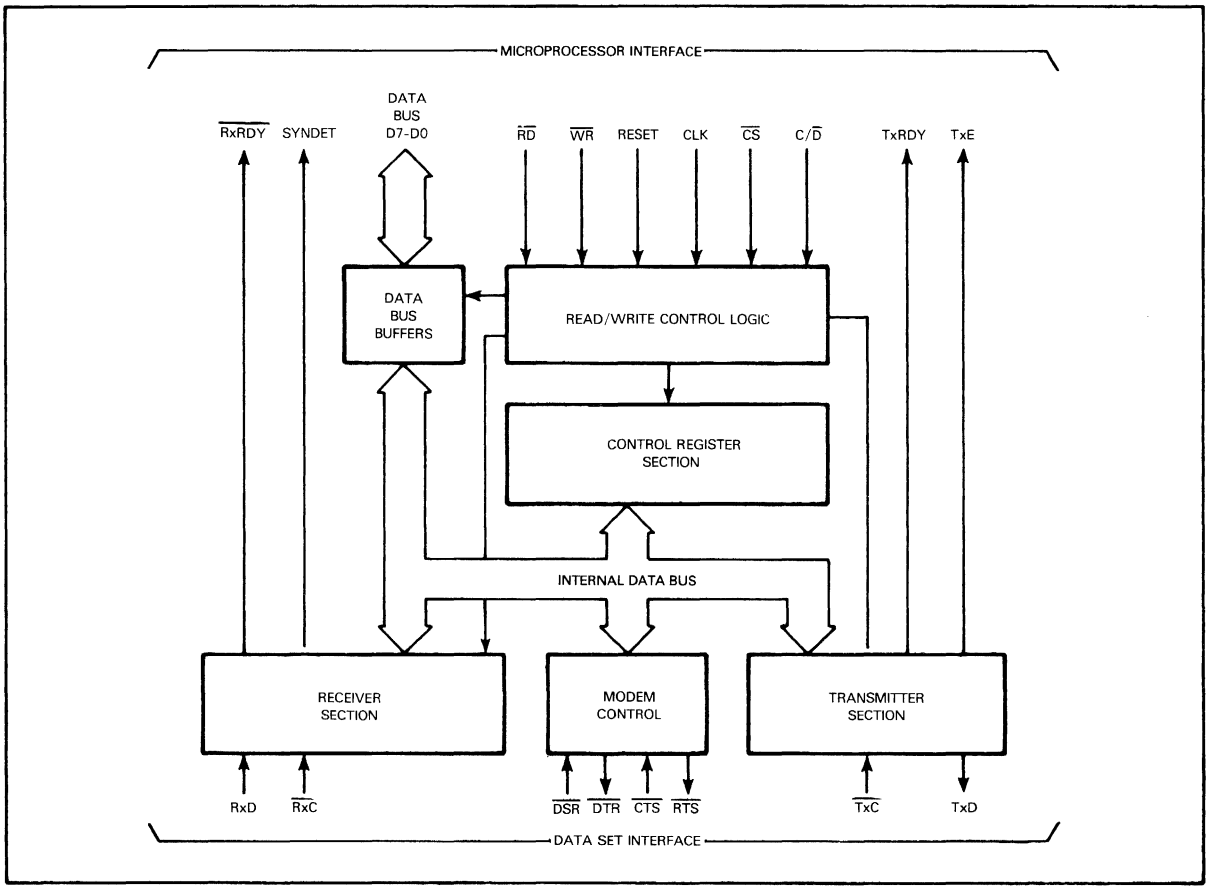


FIGURE 8-1 BLOCK DIAGRAM

Data being transmitted is double buffered; the Transmitter section contains a Transmitter Output Register and a Transmitter Buffer Register. Data is output serially from the Transmitter Output Register. Data is written by the microprocessor into the Transmitter Buffer Register. As soon as the contents of the Transmitter Output Register have been exhausted, Transmitter section logic automatically moves the contents of the Transmitter Buffer Register to the Transmitter Output Register. Thus, while one character is being output serially from the Transmitter Output Register, the microprocessor can be loading the next data byte into the Transmitter Buffer Register.

The Receiver section accepts serial data input, frames groups of bits into characters as required by the selected operating mode, and outputs characters to the Data Bus when requested by the microprocessor. The Receiver section develops the necessary control and status signals to notify the microprocessor that a complete character has been framed.

Like the Transmitter section, the Receiver section contains double buffer registers. Serial data input is framed in the Receiver Input Register. Once a complete character has been framed, Receiver section logic automatically transfers the character into the Receiver Buffer Register. The microprocessor can read the contents of the Receiver Buffer Register while the next character is being framed in the Receiver Input Register.

The Modem Control function contains standard control signals necessary to coordinate the operation of the communication interface and a data set.

Read/Write Control logic provides the interface to microprocessor Control and Address Busses. This logic also creates microprocessor control signals.

SERIAL I/O CONCEPTS

While a detailed discussion of serial I/O philosophy is beyond the scope of this book, a summary of elementary serial I/O protocol is provided since it defines terms used in the following discussion.

Serial data characters are transmitted in data units that may be five, six, seven or eight bits in length. These different data lengths result from historical practice. For example, the early model 28 Teletype® terminals used a five-bit BAUDOT code, while the more recent model 33 and 35 Teletypes® use an eight-bit ASCII code. A number of small data processing computers use six-bit bytes, while a seven-bit data unit is useful when handling ASCII codes without parity.

There are two significant problems which must be solved when transmitting or receiving serial data. First of all, since the data is, in effect, a signal which asynchronously changes state, some method must be devised for sampling the signal at time intervals which correspond to individual data bits. Secondly, serial bits must be framed accurately into parallel data units. When examining a serial data stream, there is no direct way of telling whether two data bits are contiguous members of a single character, or whether a character boundary occurs between them.

The problem of determining when to sample a serial data signal in order to read bit levels is solved by using a clock signal to time the sampling points on the serial data stream. The Am9551 has two separate clock signals: RxC identifies sampling points on the serial received data stream; TxC identifies sampling points on the transmitted data stream. The high-to-low transitions of TxC and RxC identify the sampling point on the accompanying signals. These two signals may or may not have the same frequency and be derived from the microcomputer system clock.

The data set or other logic which is communicating with the Am9551 must also have clock signals to time the serial data stream being transmitted or received. These remote clock signals will be generated by separate and distinct logic from that which generates clock signals for the Am9551. This being the case, it is important to ensure that some method of synchronization is guaranteed between the two ends of the serial data transfer. This synchronization is established by one of two schemes, which result in "synchronous" or "asynchronous" serial data transfer.

SYNCHRONOUS SERIAL DATA TRANSFER

Synchronous serial data transfer requires a valid data bit to be transferred on every active transition of the accompanying clock signal. So long as the frequencies of the clock signals at the two ends of the serial data transfer are the same, within some reasonable margin of error, transmitted data will be accurately interpreted at the receiving station.

In a synchronous data stream, character boundaries are established by preceding each block of serial data with a known bit pattern. This is referred to as the SYNC character. A SYNC character typically has the binary value 01101001. Commonly there will be either one or two SYNC characters preceding any data block. Thus, receiving logic can hunt for SYNC characters, and upon detecting one or two SYNC character patterns in a data stream, will be able to establish character boundaries. The first data bit following the SYNC pattern is the first data bit of a new character, and each character has a known number of data bits. In order to provide complete flexibility, the Am9551 allows one or two SYNC characters to be specified, and allows any character to be used as a SYNC character.

The characters of the synchronous data stream will each have five, six, seven or eight data bits, with an optional parity bit. The parity bit can provide either odd or even parity, under program control.

When transmitting synchronous serial data, transmitting logic is obliged to transmit a valid data bit on every active transition of the TxC clock. If no valid data is ready to be transmitted, then a SYNC character is inserted. When the Am9551 is receiving serial data it recognizes and discards SYNC characters in order to start assembling data characters; however, within the data stream, any SYNC characters that may occur are assembled and transmitted as valid data.

ASYNCHRONOUS SERIAL DATA

Asynchronous serial data is the second method used to transmit and receive serial data. In an asynchronous data stream, valid data characters are transmitted only as available. In between transmission of valid data characters, the serial data signal is held high, referred to as "marking". Each asynchronous data character is "framed" by a single start bit, and either 1, 1-1/2 or 2 stop bits. A start bit is a low level, or 0 bit. A stop bit is a high level, or 1 bit. A 1/2 stop bit is a high level signal maintained for half of the time assigned to a normal serial data bit. Between the start and stop bits, there will be five, six, seven or eight data bits, together with an optional parity bit.

At the beginning of every asynchronous character, logic must identify the start bit in order to assemble the data character which follows. This being the case, there is a chance of errors resulting from the transmit and receive logic clocks not being

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exactly in phase. In order to resolve this problem, asynchronous serial data is usually sampled by a clock running at 16 or 64 times the serial data frequency. Thus, receive logic will sample the serial data stream on the 8th or 32nd clock pulse after detecting the leading edge of the start pulse, in which case, an error of 7 or 31 clock pulses can be tolerated. Thereafter, data bits are sampled every 16 or 64 clocks so that the sample continues to occur in the middle of the assigned bit slots.
Synchronous and asynchronous character streams are illustrated in Figure 8-6.

INTERFACE SIGNALS

Figure 8-2 shows the Connection Diagram for the Am9551.

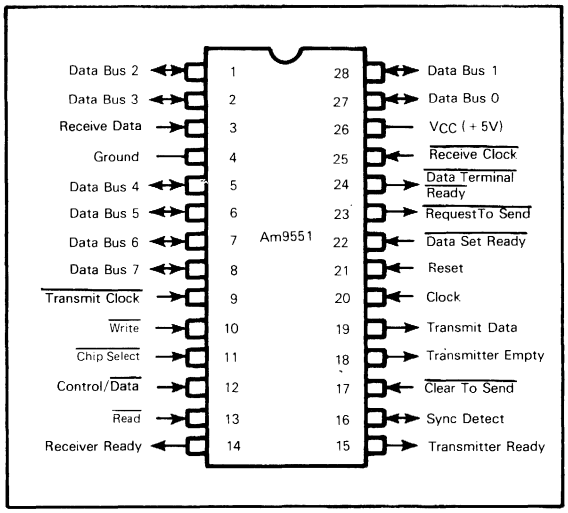


FIGURE 8-2 Am9551 CONNECTION DIAGRAM

Input

Chip Select ($\overline{CS}$, Input)
This signal must be input low for the device to be selected.

Control Or Data (C/$\overline{D}$, Input)
Within a selected device C/$\overline{D}$ is used as an address input. When C/$\overline{D}$ is low, data locations are addressed. When C/$\overline{D}$ is high, control/status locations are addressed.

Read ($\overline{RD}$, Input)
Within a selected device, $\overline{RD}$ low causes the unit to place the contents of its addressed location on the Data Bus.

Write ($\overline{WR}$, Input)
Within a selected device, $\overline{WR}$ low causes the unit to store Data Bus contents in the addressed device location.

Data Set Ready ($\overline{DSR}$, Input)
This signal is input low by a data set (modem) which is ready to transmit or receive data.

Clear To Send ($\overline{CTS}$, Input)
This signal is input low by a data set (modem) in response to RTS.

Transmitter Clock ($\overline{TxC}$, Input)
This clock signal is input to control the serial data output transfer rate.

Receiver Clock ($\overline{RxC}$, Input)
This clock signal is input to control the serial data input transfer rate.

Receive Data ($\overline{RxD}$, Input)
Serial Data is input via this signal.

Reset (RESET, Input)
This control input forces the Am8251/9551 into idle mode.

Clock (CLK, Input)
This is the master synchronization timing signal input to the Am8251/9551 from the microprocessor.

Output

Data Terminal Ready ($\overline{DTR}$, Output)
This is a control signal which may be output low when the device is ready to transmit data to a data set.

Request To Send ($\overline{RTS}$, Output)
This is a control output which precedes individual transmissions from the Am8251/9551 to a data set.

Transmitter Ready (TxRDY, Output)
This control signal is output high when data is transferred from the Transmitter Buffer Register to the Transmitter Output Register.

Transmitter Empty (TxE, Output)
This control signal is output high when the contents of the Transmitter Output Register has been output.

Transmit Data ($\overline{TxD}$, Output)
Serial data is output from the Am8251/9551 via this signal.

Receiver Ready ($\overline{RxRDY}$, Output)
This control signal is output low when a completely framed character is in the Receiver Buffer Register.

Bidirectional

Data Bus 0 - 7 (D0 - D7, Bidirectional)
Data Bus via which 8-bit parallel data is transferred between the microprocessor and the device.

Sync Detect (SYNDET, Input)
A low-to-high input at SYNDET synchronizes a synchronous serial data input stream in external sync mode.

Sync Detect (SYNDET, Output)
A high SYNDET output occurs whenever the Am8251/9551 finds sync when receiving synchronous input data in internal sync mode.

DEVICE OPERATIONS

Many aspects of Am8251/9551 operations are not immediately obvious; therefore the following discussion explains the functions performed by device signals in greater detail.

POWER

Input/Output Control

Data Bus Buffers

The Data Bus buffers connect to the microcomputer Data Bus for bidirectional transfer of information between the microprocessor and the Am9551. The output buffers use 3-state drivers controlled by Chip Select ($\overline{CS}$). Unselected devices have their outputs in the high impedance condition.

Addressing

There are four addressable locations within the Am9551:

- The Receiver Buffer Register
- The Transmitter Buffer Register
- The Status Register
- The Control Register

The Receiver Buffer Register is a read-only location while the Transmitter Buffer Register is a write-only location. These two locations are therefore accessed via a single address, and selected by the Read or Write signals. The Status Register is a read-only location, while the Control register is a write-only location. Thus, these two are accessed using another single address and differentiated in the same way.

Note that a Control code written to control logic has its own Control Register. The 8251 Communication Interface which the Am9551 replaces, requires Control codes to be written into the Transmitter Buffer Register. Special programming techniques are required to account for this anomaly in 8251 design. The fact that the Am9551 has a separate Control Register is transparent to the user; programs written to control the 8251 will also operate with the Am9551. New programs being generated for the Am9551 need not include the precautions that surround transmitting Control codes to the 8251.

In summary, each Am9551 must have two assigned addresses. These may be memory or I/O addresses. They are selected by the logic which creates $\overline{CS}$ and C/$\overline{D}$. For an Am9551 to be selected, $\overline{CS}$ must be input low. If C/$\overline{D}$ is high, then the Control Register or the Status Register will be accessed. If C/$\overline{D}$ is low, then the Receiver or Transmitter Buffer Register will be accessed.

If the Am9551 is being accessed using input/output instructions, then $\overline{CS}$ and C/$\overline{D}$ will be decoded from Address Bus lines A0 - A7. If the Am9551 is being accessed via memory reference instructions, then $\overline{CS}$ and C/$\overline{D}$ will be decoded from the entire Address Bus.

Table 8-1 summarizes Am9551 access logic.

TABLE 8-1 Am9551 FUNCTIONAL OPERATION DURING READ AND WRITE

$\overline{RD}$	$\overline{WR}$	C/$\overline{D}$	$\overline{CS}$	FUNCTION
0	1	0	0	Receiver Register → Data Bus
1	0	0	0	Data Bus → Transmitter Register
0	1	1	0	Status Register → Data Bus
1	0	1	0	Data Bus → Control Register
X	X	X	1	Data Bus → High impedance

Read And Write

These are two control signals which determine whether data will be read from, or written into an addressed location within a selected Am9551. When $\overline{WR}$ is pulsed low, data entering via the bidirectional Data Bus will be written into a selected location. When $\overline{RD}$ is pulsed low, the contents of the selected location will be output to the bidirectional Data Bus.

$\overline{RD}$ and $\overline{WR}$ will usually be connected to control signals output by the Am8228/38 System Controller. If the Am9551 is being accessed via I/O instructions, as two I/O ports, then $\overline{RD}$ will be connected to $\overline{IOR}$ and $\overline{WR}$ will be connected to $\overline{IOW}$. If the Am9551 is being accessed via memory reference instructions, as two memory locations, then $\overline{RD}$ may be connected to $\overline{MEMR}$ and $\overline{WR}$ may be connected to $\overline{MEMW}$.

Data Set Ready, Data Terminal Ready

Data Set Ready is input low from a data set (modem) which is ready to transmit or receive data. $\overline{DSR}$ controls one of the eight bits of an internal status word which can be monitored by the CPU and has no other internal effect.

Data Terminal Ready is a control signal output from the Am9551 to a data set. It acknowledges that the microcomputer system is ready to transfer data to or from the data set.

$\overline{DTR}$ is set and reset by control commands sent by the microcomputer to the Am9551.

Request To Send and Clear To Send

When $\overline{DSR}$ and $\overline{DTR}$ are both low, the Am9551 can communicate with external logic. Individual messages, however, are initiated by the Am9551 outputting $\overline{RTS}$ low. This indicates that the Am9551 is ready to transmit.

$\overline{CTS}$ is the Clear To Send signal with which external logic acknowledges RTS. In a full duplex data link, $\overline{RTS}$ from the transmitter becomes $\overline{CTS}$ at the receiver. In a half duplex data link, the modem receiving $\overline{RTS}$ sends back $\overline{CTS}$ two milliseconds later.

Transmitter Ready

Transmitter logic contains two registers in order to buffer data output. The actual data byte being serially output is stored in the Transmitter Output Register. When the microprocessor transmits data to the Transmitter section, the data is stored in a Transmitter Buffer Register.

As soon as the serial output of data in the Transmitter Output Register is complete, Transmitter Buffer Register contents are transferred to the Transmitter Output Register and TxRDY is output high. TxRDY remains high until the microprocessor outputs another data byte to the Transmitter Buffer Register. TxRDY also forms one bit in the status word.

The microprocessor can use TxRDY in one of two ways. If the program controlling the Am9551 is interrupt-driven, then the TxRDY high pulse can be used to create an interrupt request. Upon acknowledging this interrupt request, the microprocessor simply writes another data byte to the Transmitter Buffer Register. If the program monitoring the Am9551 is not interrupt-driven, then the microprocessor can read the status word and test the TxRDY bit to see if the Am9551 is ready to receive another byte of data.

Transmitter Empty

TxE is output high as soon as data in the Transmitter Output Register has been output. TxE remains high until data has been loaded by Transmitter section logic from the Transmitter Buffer Register into the Transmitter Output Register.

If valid data is not present in the Transmitter Buffer Register, then TxE will remain high while a Break signal is output during asynchronous serial output. During synchronous serial transmission, however, a SYNC character will be shifted into the Transmitter Buffer Register. TxE will be pulsed high for the short time interval during which data is transferred from the Transmitter Buffer Register to the Transmitter Output Register, irrespective of whether valid data or a SYNC character is being transmitted.

Transmitter Clock

$\overline{TxC}$ provides the signal which clocks data being shifted out from the Transmitter Output Register. When the Am9551 is used in a synchronous communication system, the transmitter clock is set to the actual frequency of data transmission. In an asynchronous communication system, the transmitter clock may be selected to be 1x, 16x or 64x the data transmission frequency. Information is shifted on the high-to-low transition of the clock pulse. 1x asynchronous transmission is sometimes referred to as isosynchronous transmission.

Receiver Ready

$\overline{RxRDY}$ is a status signal output by the Am9551 when a completely framed character is in the Receiver Buffer Register, waiting for transfer to the CPU. $\overline{RxRDY}$ also forms one bit of the status word. $\overline{RxRDY}$ may be used to generate an interrupt request or the $\overline{RxRDY}$ Status bit may be polled by reading the Status Register. This signal is reset when the Receiver Buffer Register is read by the CPU.

Receiver Clock

$\overline{RxC}$ provides the clock signal which times data being shifted into the Receiver Register of the Am9551. When the Am9551 is used in the synchronous mode, $\overline{RxC}$ is set to the actual frequency at which data is received. In the asynchronous mode, $\overline{RxC}$ may be selected to be 1x, 16x or 64x the actual rate at which data is received. Data is shifted into the Receiver Register during the low-to-high transition of $\overline{RxC}$.

Sync Detect

When the Am9551 is operating in synchronous mode SYNDET is output high after the binary pattern defined by the microprocessor as the synchronizing pattern has been detected at the beginning of serial data stream. Subsequently, when the Am9551 is operating in the synchronous mode with internal sync detection, SYNDET is output high whenever the SYNC pattern is detected within the receive data input.

The Am9551 can also be programmed to operate in the synchronous mode with external SYNC detect. SYNDET then becomes an input signal. A low-to-high transition on the SYNDET input will cause the Receiver Register to start framing a new character, after the next low-to-high transition of the $\overline{RxC}$ signal. SYNDET must remain high until $\overline{RxC}$ has made its low-to-high transition.

Reset

When Reset is activated with a high input, it forces the Am9551 into an idle mode in which data is neither transmitted nor received. Following Reset, a new set of Control words must be output by the microprocessor to the Am9551 before operations can resume. The Am9551 should be reset after power is first applied to the device.

Clock

The Clock signal provides timing for Am9551 internal operations. Clock may be connected to any system timing signal that meets the requirements for minimum and maximum frequency. CLK does not determine serial data transmit or receive frequencies. CLK must be more than 30 times the frequency of the Receiver Clock input ($\overline{RxC}$) or the Transmitter Clock input ($\overline{TxC}$) when the Am9551 is operated in the synchronous mode. When the Am9551 is operated in the asynchronous mode, CLK must be greater than 4.5 times the frequency of either the Receiver or the Transmitter Clock. In addition, there are minimum and maximum frequencies specified in the data sheet for individual devices.

DEVICE PROGRAMMING

A USART is operated within a microcomputer system under program control. The microcomputer program controlling the Am9551 must perform these tasks:

- Output Control codes
- Input status
- Output data to be transmitted
- Input data which has been received

Control codes determine the mode in which the Am9551 will operate and are used to set or reset control signals output by the Am9551.

The Status Register contents will be read by the program monitoring the device's operation in order to determine error conditions, when and how to read data, write data or output Control codes. Program logic may be based on reading status bit levels, or Am9551 control signals may be used to request interrupts.

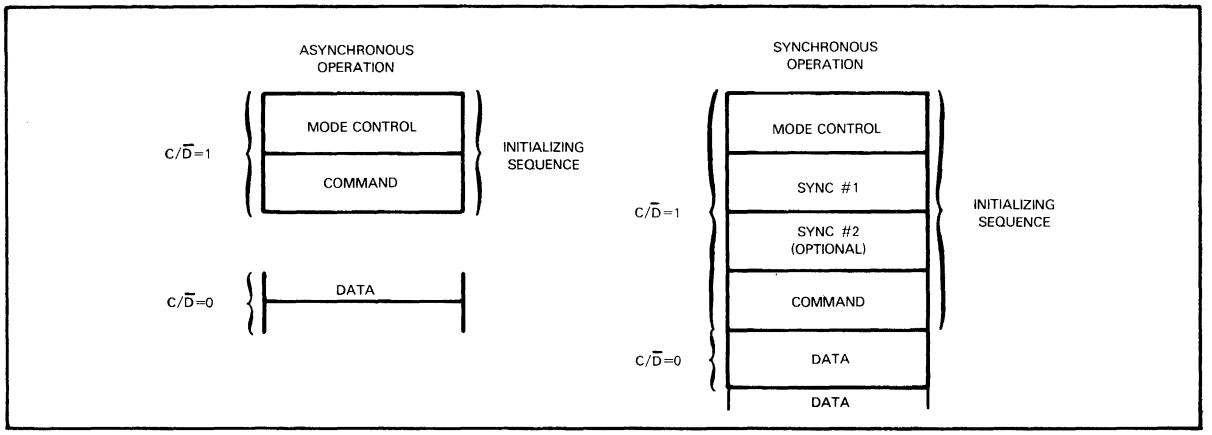


FIGURE 8-3 INITIALIZATION CONTROL WORD SEQUENCE

INITIALIZATION

The Am9551 must be initialized following a system reset, or prior to starting a new serial I/O operation sequence. It is reset following power up and subsequently may be reset at any time following completion of one set of operations and preceding a new set. Following a reset, the idle state in which data can be neither transmitted nor received is entered.

The Am9551 is initialized by outputting two, three or four control words, as shown in Figure 8-3. Note that in asynchronous operation a mode control word must be output to the Am9551 device followed by a command word. For synchronous operation, the mode control word is followed by one or two SYNC characters, and then a command word.

A single address is set aside internally for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the Am9551 directs control information to its proper destination based on the sequence in which it is transmitted. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes output as control codes will be interpreted as SYNC characters; the preceding mode determines whether one or two SYNC characters must follow. For either asynchronous or synchronous operation, the next byte output as a Control code is interpreted as a command. All subsequent bytes output as Control codes are interpreted as commands.

There are two ways in which control logic may return to the state of anticipating a mode control input:

- There is a specific command which forces a return to mode control.
- Following a reset, control logic will revert to interpreting the next control code as a mode control.

MODE CONTROL CODES

The Am9551 will interpret mode control codes as illustrated in Figures 8-4 and 8-5. Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

A non-zero value in bits 0 and 1 specifies asynchronous mode and defines the relationship between data transfer baud rate and receive or transmit clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse.

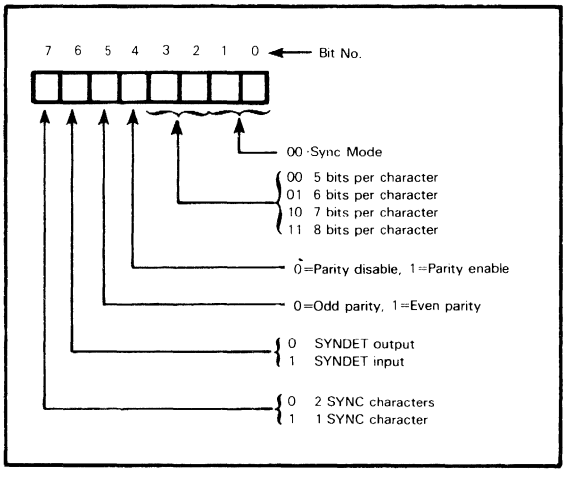


FIGURE 8-4 SYNCHRONOUS MODE CONTROL CODE

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character. Similarly, bits 4 and 5 determine whether there will be a parity bit in each data unit, and if so, whether odd or even parity will be adopted.

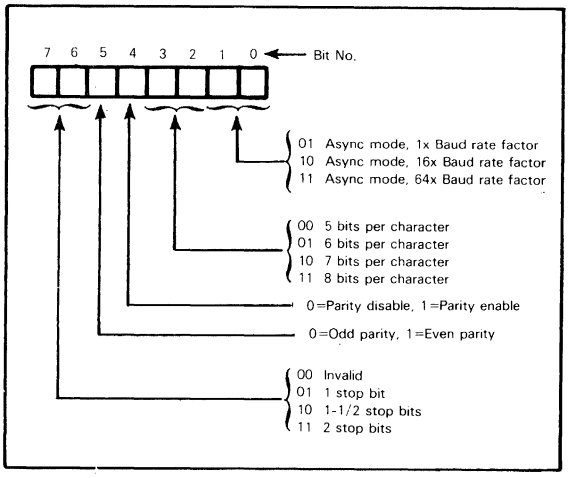


FIGURE 8-5 ASYNCHRONOUS MODE CONTROL CODE

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will terminate each character. 1-1/2 stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization. When SYNDET is an input, external logic forces synchronization by inputting SYNDET high.

Figure 8-6 illustrates synchronous and asynchronous serial data stream options.

SYNC WORD

The SYNC WORD, although classified as a control word in the context of initializing the Am9551, does not actually control operation of the circuit. The first control word in the initializing sequence for the Am9551 is interpreted as the Mode Control word. If the Mode Control word specifies operation in the synchronous mode, the next one or two control words transmitted will be treated as sync character(s) and will be loaded to the SYNC Word Register for use by the transmitter and the receiver circuits.

COMMAND WORDS

Command words are used to initiate specific functions within the Am9551 such as, "reset all error flags" or "start searching for sync". Command Words may be issued by the microprocessor to the Am9551 at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

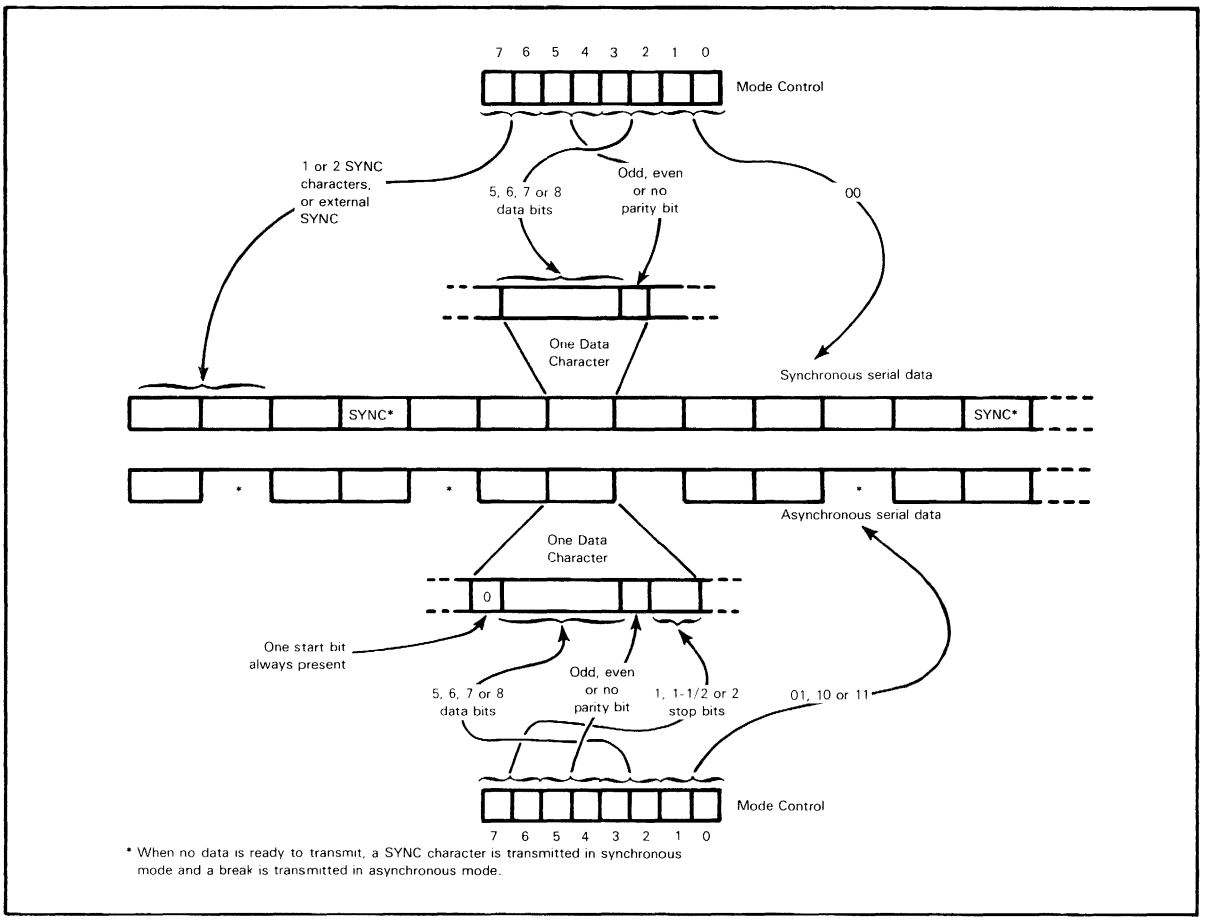


FIGURE 8-6 SYNCHRONOUS AND ASYNCHRONOUS DATA CHARACTERS AS A FUNCTION OF MODE CONTROL

During initialization, the last Control Word issued must be a Command Word to initiate operation of the Am9551. The initializing sequence consists of programming the mode of operation, then coding the Sync characters (if appropriate) and sending the Command Word.

Figure 8-7 shows the Command Word format.

COMMAND WORD FUNCTIONS

Bit D0 is the Transmit Enable control (TxEN). Data transmission from the Am9551 cannot take place unless TxEN is set in the Command Register. Table 8-2 defines the way in which TxEN, TxE and TxRDY combine to control transmitter section operations.

Bit D1 is the Data Terminal Ready ($\overline{DTR}$) bit. When the DTR command bit is set, the $\overline{DTR}$ output connection is active (low). $\overline{DTR}$ is used to advise the data set that the data terminal is prepared to accept or transmit data. The $\overline{DTR}$ signal is used in systems where data communications are operated by remote control.

Bit D2 is the Receiver Enable command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the CPU that a complete character is framed in the Receive Character Buffer. It does

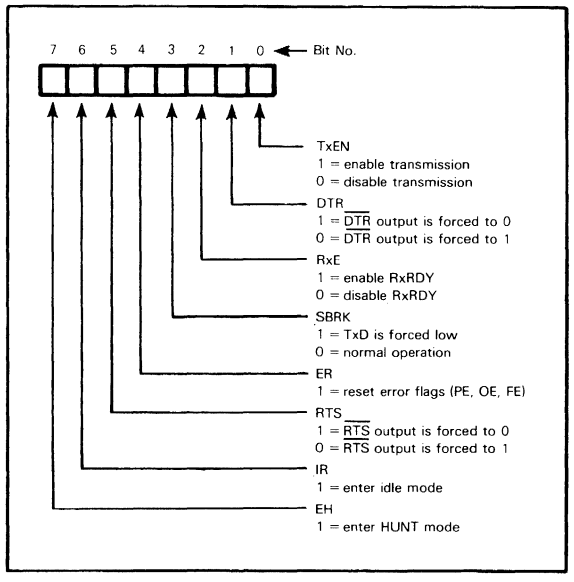


FIGURE 8-7 COMMAND WORD FORMAT

TABLE 8-2 OPERATION OF THE TRANSMITTER SECTION AS A FUNCTION OF TxE, TxRDY, AND TxEN

TxEN	TxE	TxRDY	OPERATION
1	1	1	Transmit Register and Transmit Character Buffer empty. TxD continues to mark if Am9551 is in the asynchronous mode. TxD will send Sync pattern if Am9551 is in the Synchronous Mode.
1	0	1	Transmit Register is shifting a character to TxD. Transmit Character Buffer is available to receive a new byte from the CPU.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	X	X	Transmitter not enabled.

not, however, inhibit the assembly of data characters at the input. Consequently, if communication circuits are active, characters will be assembled by the reciever and transferred to the Receiver Character Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to ensure proper operation of the Am9551, the Overrun Error should be reset with the same command that enables RxE.

Bit D3 is the Send Break command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "1" level (mark) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the Am9551 to reset SBRK.

Bit D4 is the Error Reset bit (ER). When a Command Word is transmitted with the ER bit set, all three error flags in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the Am9551. No latch is provided in the Command Register to save the ER command bit.

Bit D5, the Request To Send command bit (RTS), sets a latch to reflect the $\overline{RTS}$ signal level. The output of this latch is independent of other signals in the Am9551. As a result, data transfers may be made by the microprocessor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of $\overline{RTS}$.

Bit D6, the Internal Reset bit (IR), causes the Am9551 to return to the Idle mode. All operations cease and no new operation can be resumed until the circuit is reinitialized.

If the operating mode is to be altered during the execution of a microprocessor program, the Am9551 must first be reset. Either the external reset connection can be activated, or the Internal Reset command can be sent to the Am9551. Internal Reset is a momentary function performed only when the command is issued.

Bit D7 is the Enter Hunt mode command bit (EH). This command is only effective for the Am9551 when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue until SYNC is found or until EH is reset by a subsequent command, or the IR command is sent to the Am9551.

THE STATUS REGISTER

The Status Register maintains information about the current operational status of the Am9551. Figure 8-8 shows the format of the Status Register.

TxRDY signals the CPU that the Transmit Character Buffer is empty and that the Am9551 can accept a new character for transmission.

RxRDY signals the CPU that a completed character is holding in the Receive Buffer Register for transfer to the CPU.

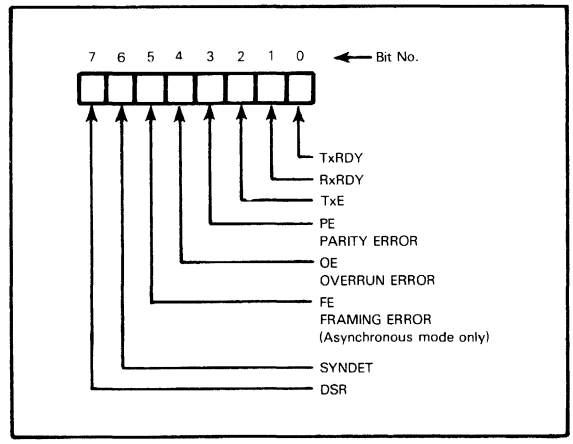


FIGURE 8-8 STATUS REGISTER

TxE signals the CPU that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before it could be transferred to the CPU.

FE is the character Framing Error which indicates that the byte stored in the Receiver Character Buffer was received with incorrect character bit format, as specified by the current mode.

SYNDET is the synchronous mode status bit associated with internal sync detection.

DSR is the status bit set by the external Data Set Ready signal to indicate that the communication Data Set is operational.

All status bits are set by the functions described for them. All status bits, once set, remain set until the CPU reads the Status Register, at which time all status bits are reset. The three error status bits may also be reset with the ER command.

Am8251 • Am9551

Programmable Communications Interface

DISTINCTIVE CHARACTERISTICS

- Direct replacement for Intel C8251
- Separate control and transmit register input buffers
- 8080A/9080A compatible
- Synchronous or asynchronous serial data transfer
- Parity, overrun and framing errors detected
- Half or full duplex signalling
- Character length of 5, 6, 7 or 8 bits
- Internal or external synchronization
- Odd parity, even parity or no parity bit
- Modem interface controlled by processor
- Programmable Sync pattern
- Fully TTL compatible logic levels
- +5 only power supply
- Commercial and military temperature range operation
- Ion-implanted N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

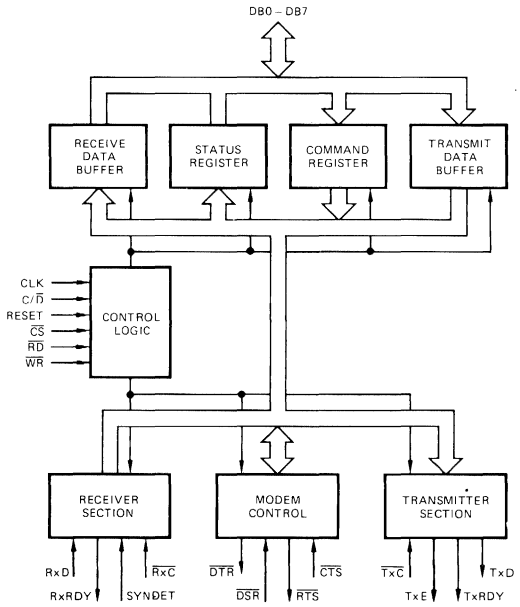
GENERAL DESCRIPTION

The Am8251/9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor, and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream. Simultaneously, serial data can be received, converted into parallel form, de-formated, and then presented to the CPU. The USART can operate in an independent full duplex mode.

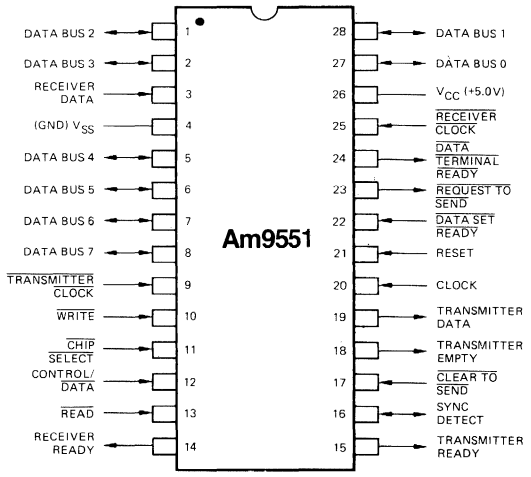
Data, Control, operation and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the Am8251/9551 to service a wide range of communication disciplines and applications.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	FOR USE WITH			
		Am9080A C8080A	Am9080A-2 C8080A-2	Am9080A-1 C8080A-1	Am9080A-4
Hermetic DIP	$0°C \leq T_A \leq +70°C$	Am9551DC C8251	Am9551DC	Am9551-4DC	Am9551-4DC
	$-55°C \leq T_A \leq +125°C$	Am9551DM	Am9551DM		

INTERFACE SIGNAL DESCRIPTION

Data Bus

The Am9551 uses an 8 bit bi-directional data bus to exchange information with an associated processor. Internally, data is routed between the data bus buffers and the transmitter section or receiver section as selected by the Read ($\overline{RD}$) or Write ($\overline{WR}$) control inputs.

Chip Select ($\overline{CS}$)

The active low Chip Select input allows the Am9551 to be individually selected from other devices within its address range. When Chip Select is high, reading or writing is inhibited, and the data bus output is in it's high impedance state.

Reset

The Am9551 will assume an idle state when a high level is applied to the Reset input. When the Reset is returned Low, the Am9551 will remain in the idle state until it receives a new mode control instruction.

Read ($\overline{RD}$)

The active low Read input enables data to be transferred from the Am9551 to the processor.

Write ($\overline{WR}$)

The active low Write input enables data to be transferred from the processor to the Am9551.

Control/Data (C/$\overline{D}$)

During a Read operation, if this input is at a high level the status byte will be read, and if it is at a low level the receive data will be read by the processor. When a Write operation is being performed, this input will indicate to the Am9551 that the bus information being written is a command if C/$\overline{D}$ is high and data if C/$\overline{D}$ is low.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Am9551 DATA → DATA BUS
0	1	0	0	DATA BUS → Am9551 DATA
1	0	1	0	Am9551 STATUS → DATA BUS
1	1	0	0	DATA BUS → Am9551 COMMAND
X	X	X	1	DATA BUS → 3-STATE

Clock (CLK)

This input is used for internal timing within the Am9551. It does not control the transmit or receive rate. However, it should be at least 30 times the receive or transmit rate in the synchronous mode and 4.5 times the receive or transmit rate in the asynchronous mode. The CLK frequency is also restricted by both an upper and a lower bound. This input is often connected to a clock from the associated processor.

Receiver Data (RxD)

Serial data is received from the communication line on this input.

Receiver Clock ($\overline{RxC}$)

The serial data on input RxD is clocked into the Am9551 by the $\overline{RxC}$ clock signal. In the synchronous mode, $\overline{RxC}$ is determined by the baud rate and supplied by the modem. In the asynchronous mode, $\overline{RxC}$ is 1, 16, or 64 times the baud rate as selected in the mode control instruction. Data is sampled by the Am9551 on the rising edge of $\overline{RxC}$.

Receiver Ready (RxRDY)

The RxRDY output signal indicates to the processor that data has been shifted into the receiver buffer from the receiver section and may be read. The signal is active high and will be reset when the buffer is read by the processor. RxRDY can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver may be running. If the processor does not read the receiver buffer before the next character is shifted from the receiver section then an overrun error will be indicated in the status buffer.

Sync Detect (SYNDET)

This signal is used only in the synchronous mode. It can be either an output or input depending on whether the program is set for internal or external synchronization. As an output, a high level indicates when the sync character has been detected in the received data stream after the Internal Synchronization mode has been programmed. If the Am9551 is programmed to utilize two sync characters, then SYNDET will go to a high level when the last bit of the second sync character is received. SYNDET is reset when the status buffer is read or when a Reset signal is activated. SYNDET will perform as an input when the External Synchronization mode is programmed. External logic can supply a positive-going signal to indicate to the Am9551 that synchronization has been attained. This will cause it to initialize the assembly of characters on the next falling edge of $\overline{RxC}$. To successfully achieve synchronization the SYNDET signal should be maintained in a high condition for at least one full period of $\overline{RxC}$.

Transmit Data (TxD)

Serial data is transmitted to the communication line on this output.

Transmitter Clock ($\overline{TxC}$)

The serial data on TxD is clocked out with the $\overline{TxC}$ signal. The relationship between clock rate and baud rate is similar to that for $\overline{RxC}$. Data is shifted out of the Am9551 on the falling edge of $\overline{TxC}$.

Transmitter Ready (TxRDY)

The TxRDY output signal goes high when data in the Transmit Data Buffer has been shifted into the transmitter section allowing the Transmit Data Buffer to accept the next byte from the processor. TxRDY will be reset when information is written into the Transmit Data Buffer. Loading command register also resets TxRDY. TxRDY will be available on this output pin only when the Am9551 is enable to transmit (CTS = 0, TxEN = 1). However, the TxRDY bit in the status Buffer will always be set when the Transmit Data Buffer is empty regardless of the state of TxEN and $\overline{CTS}$.

Transmitter Empty (TxE)

The TxE output signal goes high when the Transmitter section has transmitted its data and is empty. The signal will remain high until a new data byte is shifted from the Transmit Data Buffer to the Transmitter section. In the synchronous mode if the processor does not load a new byte into the buffer in time, TxE will, independent of the status of the TxEN bit in the command register, momentarily go to a high level as SYNC characters are loaded into the Transmitter Section.

Data Terminal Ready ($\overline{DTR}$)

This signal is a general purpose output which reflects the state of bit 1 in the Command instruction. It is commonly connected to an associated modem to indicate that the Am9551 is ready.

Data Set Ready ($\overline{DSR}$)

This is a general purpose input signal and forms part of the status byte that may be read by the processor. $\overline{DSR}$ is generally used as a response to $\overline{DTR}$, by the Modem, to indicate that it is ready. The signal acts only as a flag and does not control any internal logic.

INTERFACE SIGNAL DESCRIPTION (Cont.)

Request to Send ($\overline{RTS}$)

This is a general purpose output, similar to $\overline{DTR}$, and reflects the state of bit 5 in Command Instruction. It is normally used to initiate a data transmission by requesting the modem to prepare to send.

Clear to Send ($\overline{CTS}$)

This is a general purpose input signal used to enable the 8251/9551 to transmit data if the TxEN bit in the Command byte is a one. $\overline{CTS}$ is generally used as a response to $\overline{RTS}$ by a modem to indicate that transmission may begin. Designers not using $\overline{CTS}$ in their systems should remember to tie it low so that 8251/9551 data transmission will not be disabled.

OPERATION AND PROGRAMMING

The microcomputer program controlling the Am9551 performs these tasks:

- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which have been received

Control codes determine the mode in which the Am9551 will operate and are used to set or reset control signals output by the Am9551.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

INITIALIZING THE Am9551

The Am9551 may be initialized following a system reset or prior to starting a new serial I/O sequence. The USART must be reset following power up and subsequently may be reset at any time following completion of one activity and preceeding a new set of operations. Following a reset, the Am9551 enters an idle state in which it can neither transmit nor receive data.

The Am9551 is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the Am9551, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

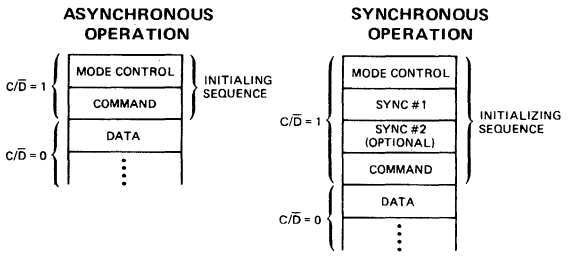


Figure 1. Control Word Sequence for Initialization.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following an external Reset signal or following an internal Reset command.

MODE CONTROL CODES

The Am9551 interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or

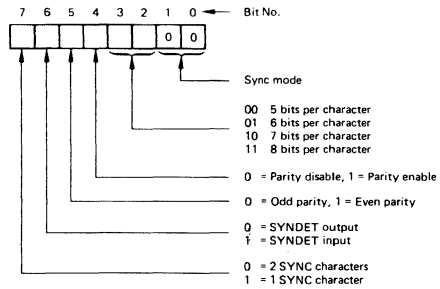


Figure 2. Synchronous Mode Control Code.

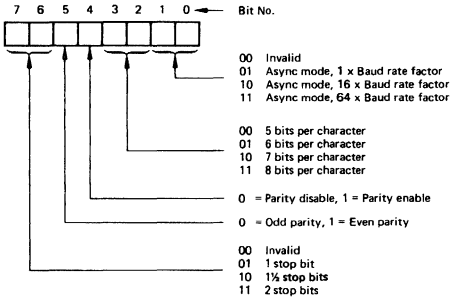


Figure 3. Asynchronous Mode Control Code.

OPERATION AND PROGRAMMING (Cont.)

eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½, or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

COMMAND WORDS

Command words are used to initiate specific functions within the Am9551 such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the microprocessor to the Am9551 at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

Figure 4 shows the format for the Command Word.

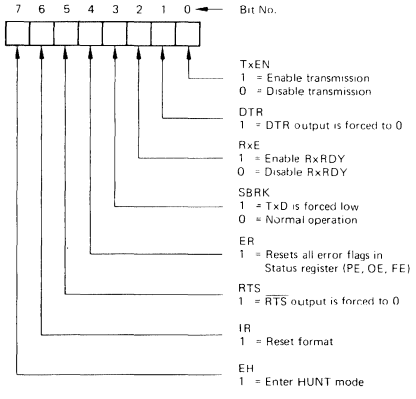


Figure 4. Am9551 Control Command.

Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission from the Am9551 cannot take place unless TxEN is set in the command register. Figure 5 defines the way in which TxEN, TxE and TxRDY combine to control transmitter operations.

Bit 1 is the Data Terminal Ready (DTR) bit. When the DTR command bit is set, the $\overline{DTR}$ output connection is active (low). DTR is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Character Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

TxEN	TxE	TxRDY	
1	1	1	Transmit Output Regsiter and Transmit Character Buffer empty. TxD continues to mark if Am9551 is in the asynchronous mode. TxD will send Sync pattern if Am9551 is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Figure 5. Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the Am9551 to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transmitted with the ER bit set, all three error flags in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the Am9551. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit (RTS), sets a latch to reflect the RTS signal level. The output of this latch is created independently of other signals in the Am9551. As a result, data transfers may be made by the microprocessor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of RTS.

Bit 6, the Internal Reset (IR), causes the Am9551 to return to the Idle mode. All functions within the Am9551 cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a microprocessor program, the Am9551 must first be reset. Either the external reset connection can be activated, or the Internal Reset Command can be sent to the Am9551. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the Am9551 when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will

OPERATION AND PROGRAMMING (Cont.)

continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the Am9551, or when SYNC characters are recognized.

STATUS REGISTER

The Status Register maintains information about the current operational status of the Am9551. Figure 6 shows the format of the Status Register.

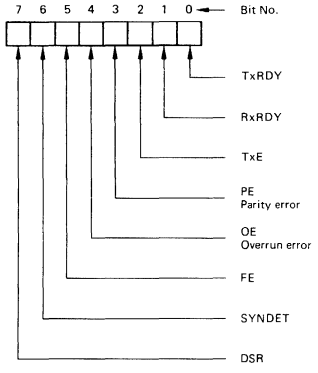


Figure 6. The Am9551 Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the Am9551 can accept a new character for transmission.

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor.

FE is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect character bit format, as specified by the current mode.
SYNDET is the synchronous mode status bit associated with internal sync detection.

DSR is the status bit set by the external Data Set Ready signal to indicate that the communication Data Set is operational. All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset only by command.

MAXIMUM RATINGS Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9551DC C8251 Am9551-4DC	$0°C \leq T_A \leq +70°C$	+5.0V ± 5%	0V
Am9551DM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

Parameters	Description	Test Conditions	C8251 Min.	C8251 Typ.	C8251 Max.	Am9551 Min.	Am9551 Typ.	Am9551 Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$				2.4			Volts
		$I_{OH} = -100\mu A$	2.4						
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$						0.4	Volts
		$I_{OL} = 1.6mA$			0.45				
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage		−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			10			10	μA
I_{DL}	Data Bus Leakage	$V_{OUT} = 0.45V$			−50			−50	μA
		$V_{OUT} = V_{CC}$			10			10	
I_{CC}	V_{CC} Supply Current	$T_A = +25°C$		45			45		mA
		$T_A = 0°C$			80			80	
		$T_A = -55°C$						120	
C_O	Output Capacitance	fc = 1.0MHz, Inputs = 0V						15	pF
C_I	Input Capacitance				10			10	pF
$C_{I/O}$	I/O Capacitance				20			20	pF

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 2)

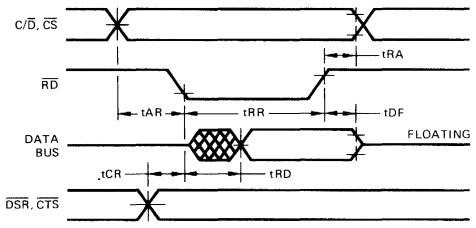
Parameters	Description		C8251 Min.	C8251 Max.	Am9551DM Am9551DC Min.	Am9551DM Am9551DC Max.	Am9551-4DC Min.	Am9551-4DC Max.	Units
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{READ}$ Low Set-up Time		50		50		50		ns
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{WRITE}$ Low Set-up Time		20		20		20		ns
t_{CR}	$\overline{DSR}$, $\overline{CTS}$ to $\overline{READ}$ Low Set-up Time			16		16		16	tCY
t_{CY}	Clock Period		.420	1.35	.380	1.35	.380	1.35	μs
t_{DF}	$\overline{READ}$ High to Data Bus Off Delay		25	200	25	200	25	200	ns
t_{DTx}	TxC Low to TxD Delay			1.0		1.0		1.0	μs
t_{DW}	Data to $\overline{WRITE}$ High Set-up Time		200		150		100		ns
t_{ES}	External SYNDET to RxC Low Set-up Time			16		16		16	tCY
t_{HRx}	Sampling Pulse to Rx Data Hold Time		2.0		2.0		2.0		μs
t_{IS}	Data Bit (Center) to Internal SYNDET Delay			25		25		25	tCY
$t_{\phi W}$	Clock Pulse Width		220	0.7tCY	175	0.7tCY	175	0.7tCY	ns
t_R, t_F	Clock Rise & Fall Time		0	50	0	50	0	50	ns
t_{RA}	$\overline{READ}$ High to $\overline{CS}$, C/D Hold Time		5.0		5.0		5.0		ns
t_{RD}	$\overline{READ}$ Low to Data Bus On Delay			350		250		180	ns
t_{RPD}	Receiver Clock High Time	1x Baud Rate	15		15		15		tCY
		16x & 64x Baud Rate	3.0		3.0		3.0		
t_{RPW}	Receiver Clock Low Time	1x Baud Rate	12		12		12		tCY
		16x & 64x Baud Rate	1.0		1.0		1.0		
t_{RR}	$\overline{READ}$ Pulse Width		430		380		250		ns
t_{RV}	Time Between $\overline{WRITE}$ Pulses During Initialization (Note 3)		6.0		6.0		6.0		tCY
t_{Rx}	Data Bit (Center) to RxRDY Delay			20		20		20	tCY
t_{SRx}	Rx Data to Sampling Pulse Set-up Time		2.0		2.0		2.0		μs
t_{TPD}	Transmitter Clock High Time	1x Baud Rate	15		15		15		tCY
		16x & 64x Baud Rate	3.0		3.0		3.0		
t_{TPW}	Transmitter Clock Low Time	1x Baud Rate	12		12		12		tCY
		16x & 64x Baud Rate	1.0		1.0		1.0		
t_{Tx}	Data Bit (Center) to TxRDY Delay			16		16		16	tCY
t_{TxE}	Data Bit (Center) to Tx EMPTY Delay			16		16		16	tCY
t_{WA}	$\overline{WRITE}$ High to $\overline{CS}$, C/D Hold Time		20		20		20		ns
t_{WC}	$\overline{WRITE}$ High to TxE, $\overline{DTR}$, $\overline{RTS}$ Delay			16		16		16	tCY
t_{WD}	$\overline{WRITE}$ High to Data Hold Time		65		65		65		ns
t_{WW}	$\overline{WRITE}$ Pulse Width		400		380		250		ns
f_{Rx}	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	DC	520	
f_{Tx}	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	DC	520	

NOTES:

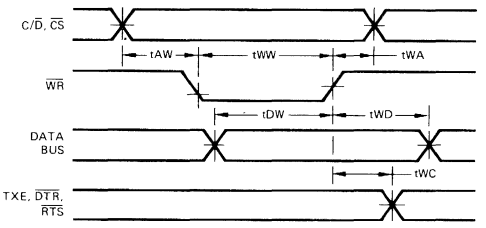
1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. Test conditions include: transition times $\leq$ 20nS, output loading of 1TTL gate plus 100pF, input and output timing reference levels of 0.8V and 2.0V.
3. This time period between write pulses is specified for initialization purposes only; when MODE, SYNC 1, SYNC 2, COMMAND and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
4. Reset Pulse Width = 6tCY min.
5. Switching Characteristic parameters are listed in alphabetical order.

SWITCHING WAVEFORMS

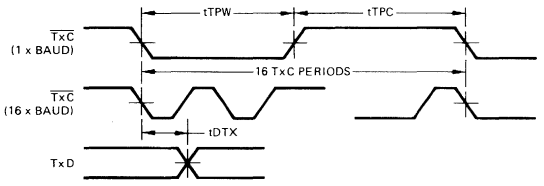
READ OPERATION



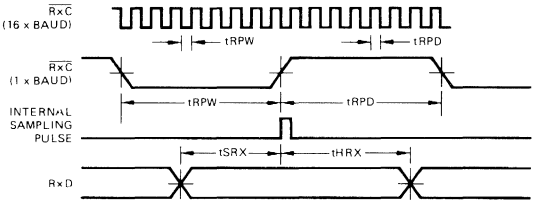
WRITE OPERATION



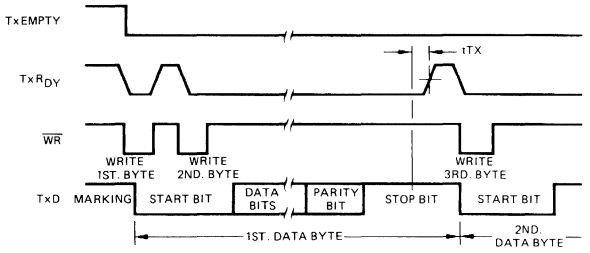
TRANSMITTER CLOCK AND DATA



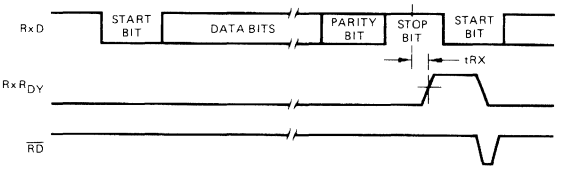
RECEIVER CLOCK AND DATA



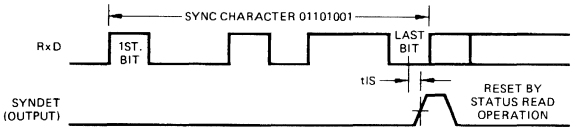
TxRDY TIMING (ASYNC MODE)



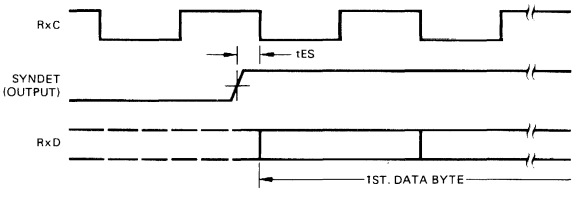
RxRDY TIMING (ASYNC MODE)



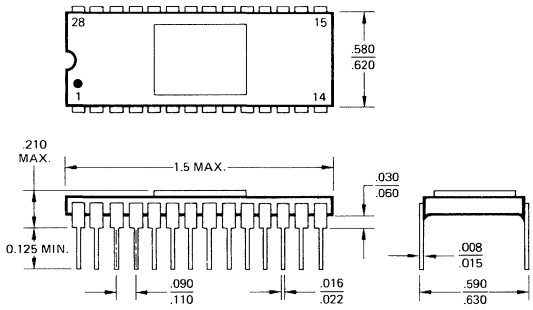
INTERNAL SYNC DETECT (SYNC MODE ONLY)



EXTERNAL SYNC DETECT (SYNC MODE ONLY)



PHYSICAL DIMENSIONS
28-Pin Hermetic DIP



Chapter 9
REGISTERS AND BUFFERS

Am8216/8226	BIDIRECTIONAL BUFFERS
Am25LS240/241	EIGHT-BIT BUFFERS
Am25LS273	EIGHT-BIT REGISTERS with common clear
Am25LS373	EIGHT-BIT LATCH with 3-state output
Am25LS374	EIGHT-BIT REGISTER with 3-state output
Am25LS377	EIGHT-BIT REGISTER with common enable

The design of microprocessor systems frequently calls for the use of buffers and registers in addition to the more specialized circuits described in the preceding chapters. Early 8080A system designs made extensive use of the 8212 discussed previously and the 8216/8226 Bidirectional Buffers described in this chapter. The impact of Low-power Schottky Technology is beginning to be felt however, and several devices are now available which offer considerable benefit to the system designer. In particular, the space-saving 20-pin Low-power Schottky devices presented here can be used to implement many of its functions for which the older parts were designed, and often offer added capability as well. Since the operation and application of buffers and registers are generally well understood, discussion in these chapters is limited to a brief description of all the parts. This is followed by a section containing data sheets for each of the parts.

Am8216/8226

The Am8216/8226 Bidirectional Buffers provide 4-bit parallel driver/receiver capability. They are used in microcomputer systems to isolate loads presented by memory and I/O circuits from the system busses. Inversion of the inputs is provided by the Am8226, while the Am8216 propagates inputs uninverted.

These Schottky Bipolar devices feature high level outputs for direct interfacing to MOS devices, and 3-state control.

Am25LS240/241

These devices are 8-bit parallel buffers providing 40mA of sink and 10mA of source current capability. Schmitt trigger inputs with a minimum of 200mV of hysteresis are provided on all inputs. The Am25LS240 and Am25LS241, which are respectively inverting and non-inverting buffers, have two enable pins, each of which controls four of the eight buffer outputs.

Am25LS273
Am25LS373
Am25LS374
Am25LS377

These circuits consist of four different implementations of a 20-pin, 8-bit parallel register. Each device contains eight high speed D-type flip-flops with a maximum clock frequency of 40 MHz. All have 8mA of sink and 440μA of source current capability. In addition, two buffered control signals common to all eight stages are provided. In the Am25LS273, the combined signals are Clock (CP) and an active low Clear ($\overline{CL}$). The Am25LS373 is implemented as an 8-bit latch with Latch Enable (G) and 3-state Output Enable ($\overline{OE}$). For the Am25LS374, Clock (CP) and Output Enable ($\overline{OE}$), provide an 8-bit register with 3-state control while the Am25LS377 offers clock enable capability by means of the Enable ($\overline{E}$) signal.

Am8216 • Am8226

Four-Bit Parallel Bidirectional Bus Driver

Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current – 0.25mA maximum
- High output drive capability for driving system data bus – 50mA at 0.5V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am3216 and Am8216 have non-inverting outputs
- Output high voltage compatible with direct interface to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperature range
- Am3226 and Am8226 have inverting outputs

FUNCTIONAL DESCRIPTION

The Am3216, Am3226, Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am3216 and Am8216, and inverting Am3226 and Am8226 drivers are provided for flexibility in system design.

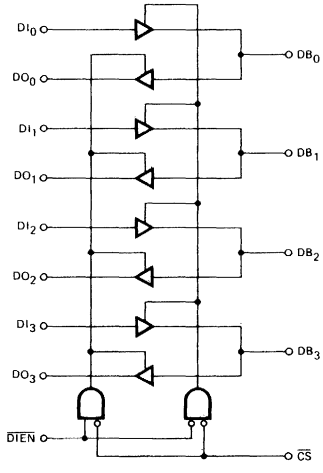
Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

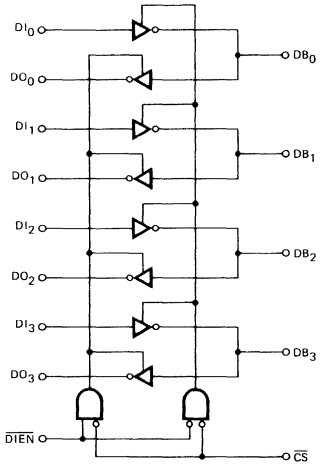
The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

LOGIC DIAGRAMS

Am3216 • Am8216



Am3226 • Am8226

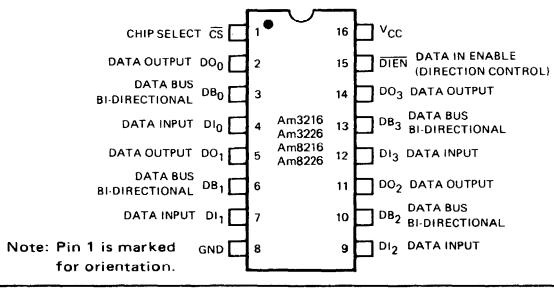


ORDERING INFORMATION

Package Type	Temperature Range	Am3216 Am8216 Order Number	Am3226 Am8226 Order Number
Hermetic DIP	–55°C to +125°C	MD3216	MD3226
Hermetic DIP	0°C to +70°C	D3216	D3226
Molded DIP	0°C to +70°C	P3216	P3226
Hermetic DIP	–55°C to +125°C	MD8216	MD8226
Hermetic DIP	0°C to +70°C	D8216	D8226
Molded DIP	0°C to +70°C	P8216	P8226
Dice	0°C to +70°C	AM8216XC	AM8226XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Temperature (Ambient) Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5V to +7.0V
All Input Voltages	−1.0V to +5.5V
Output Currents	125mA

Am3216, Am3226, Am8216 AND Am8226 MILITARY ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (−55°C to +125°C)

The following conditions apply unless otherwise specified:

MD3216, MD8216, MD3226, MD8226 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$			−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$			−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.5V$				80	μA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.5V$				40	μA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$				−1.2	Volts
V_{IL}	Input LOW Voltage	Am3216, Am8216					0.95	Volts
		Am3226, Am8226					0.9	
V_{IH}	Input HIGH Voltage				2.0			Volts
I_O	Output Leakage Current (Three-State)	DO	$V_O = 0.45V/5.5V$				20	μA
		DB					100	
I_{CC}	Power Supply Current	Am3216, Am8216				95	130	mA
		Am3226, Am8226				85	120	
V_{OL1}	Output LOW Voltage		DO Outputs $I_{OL} = 15mA$ DB Outputs $I_{OL} = 25mA$			0.3	0.45	Volts
V_{OL2}	Output LOW Voltage		DB Outputs $I_{OL} = 45mA$			0.5	0.6	Volts
V_{OH1}	Output HIGH Voltage		DO Outputs	$I_{OH} = -0.5mA$	3.4	4.0		Volts
				$I_{OH} = -2.0mA$	2.4			
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -5.0mA$		2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V, $V_{CC} = 5.0V$		−15	−35	−65	mA
			DB Outputs = 0V, $V_{CC} = 5.0V$		−30	−75	−120	

AC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am3216, Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	33	ns
		Am3226, Am8226			16	25	
t_E	Output Enable Time	Am3216	Note 3		45	75	ns
		Am8216	Note 2		45	75	
		Am3226, Am8226	Note 3		35	62	
t_D	Output Disable Time	Am3216, Am8216	Note 4		20	40	ns
		Am3226, Am8226			16	38	

Am3216, Am3226, Am8216 AND Am8226 COMMERCIAL ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

The following conditions apply unless otherwise specified:

D3216, D8216, D3226, D8226, P3216, P8216, P3226, P8226 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$		−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$		−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.25V$			20	µA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.25V$			10	µA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$			−1.0	Volts
V_{IL}	Input LOW Voltage					0.95	Volts
V_{IH}	Input HIGH Voltage			2.0			Volts
$\|I_{OL}\|$	Output Leakge Current (Three-State)	DO	$V_O = 0.45V/5.5V$			20	µA
		DB				100	
I_{CC}	Power Supply Current	Am3216, Am8216			95	130	mA
		Am3226, Am8226			85	120	
V_{OL1}	Output LOW Voltage		DB Outputs $I_{OL} = 15mA$ DB Outputs $I_{OL} = 25mA$		0.3	0.45	Volts
V_{OL2}	Output LOW Voltage	Am3216, Am8216	DB Outputs $I_{OL} = 55mA$		0.5	0.6	Volts
		Am3226, Am8226	DB Outputs $I_{OL} = 50mA$		0.5	0.6	
V_{OH1}	Output HIGH Voltage		DO Outputs $I_{OH} = -1.0mA$ COM'L	3.65	4.0		Volts
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -10mA$	2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V	−15	−35	−65	mA
			DB Outputs $V_{CC} = 5.0V$	−30	−75	−120	

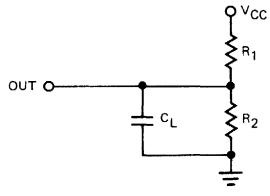
AC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am3216, Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	30	ns
		Am3226, Am8226			16	25	
t_E	Output Enable Time	Am3216	Note 3		45	65	ns
		Am8216	Note 2		45	65	
		Am3226, Am8226	Note 3		35	54	
t_D	Output Disable Time		Note 4		20	35	ns

TEST CONDITIONS

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0 and 2.0 volts.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

TEST LOAD CIRCUIT

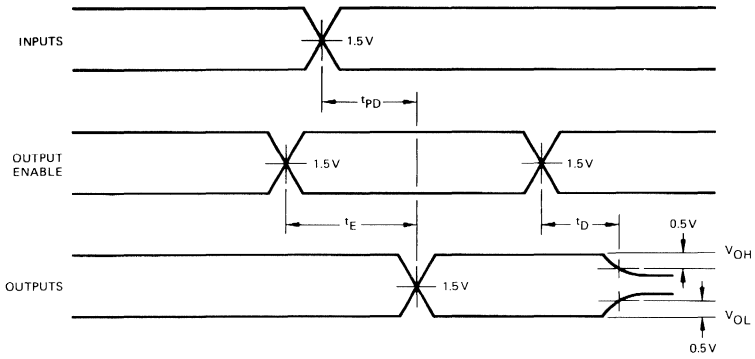


CAPACITANCE (Note 5)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		4.0	8.0	pF
C_{OUT1}	Output Capacitance			6.0	10	pF
C_{OUT2}	Output Capacitance			13	18	pF

Notes: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO outputs, C_L = 30pF, R_1 = 300/10kΩ, R_2 = 180/1.0kΩ; DB outputs, C_L = 300pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
3. DO outputs, C_L = 30pF, R_1 = 300/10kΩ, R_2 = 600/1.0kΩ; DB outputs, C_L = 300pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
4. DO outputs, C_L = 5.0pF, R_1 = 300/10kΩ, R_2 = 600/1.0kΩ; DB outputs, C_L = 5.0pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
5. This parameter is periodically sampled and not 100% tested.

SWITCHING WAVEFORMS

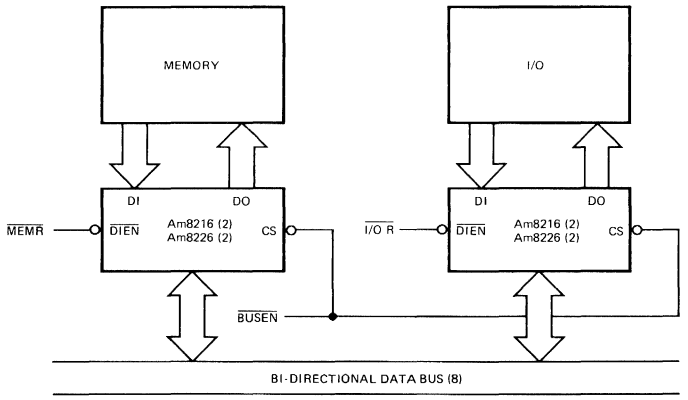


FUNCTION TABLE

$\overline{DIEN}$	$\overline{CS}$		8216 DB	8216 DO	8226 DB	8226 DO
L	L	DI ⇒ DB	DI	Z	$\overline{DI}$	Z
H	L	DB ⇒ DO	Z	DB	Z	$\overline{DB}$
L	H		Z	Z	Z	Z
H	H		Z	Z	Z	Z

H = HIGH
L = LOW

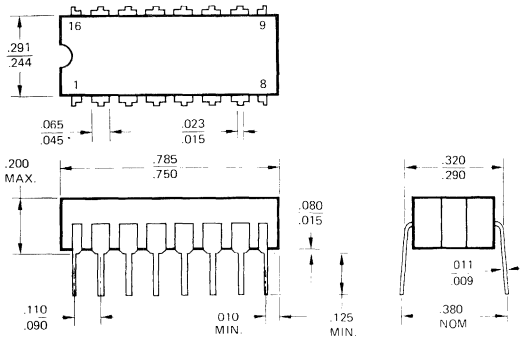
TYPICAL APPLICATION



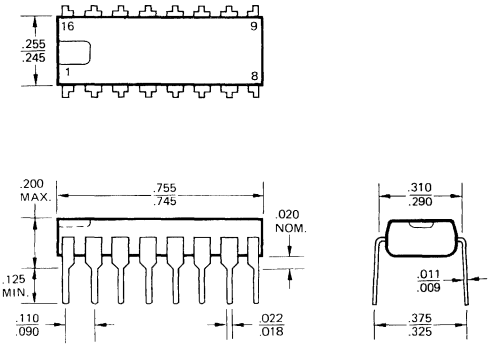
MEMORY AND I/O INTERFACE TO A BI-DIRECTIONAL BUS

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Hermetic DIP

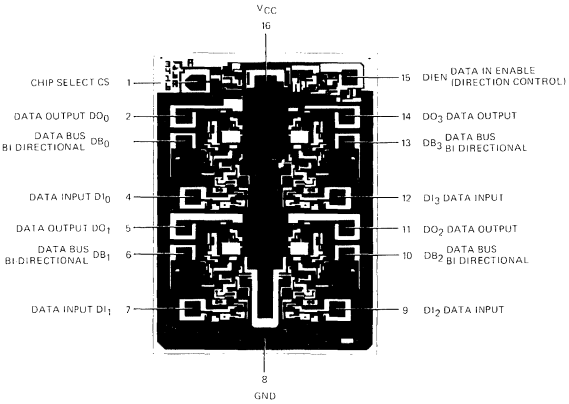


16-Pin Molded DIP



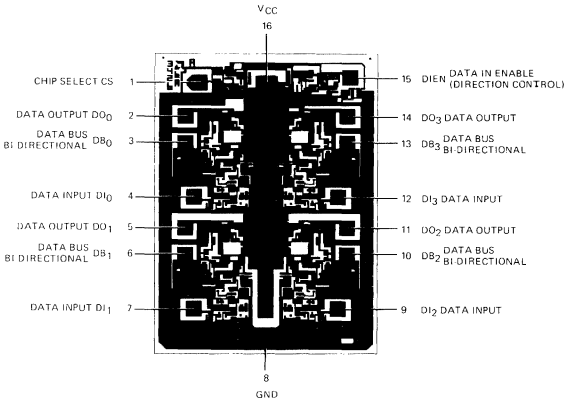
Metallization and Pad Layout

Am3216
Am8216



. DIE SIZE 0.066" X 0.090"

Am3226
Am8226



DIE SIZE 0.066" X 0.090"

Am25LS240 · Am25LS241

Octal Buffers/Line Drivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines or buffer memory address registers
- Hysteresis at inputs improve noise margins
- Drive output can sink 40mA at 0.5V max.
- 10mA source current
- 200mV minimum hysteresis
- Typical data-to-output propagation delay times:
  - Inverting – 14ns
  - Non-inverting – 18ns
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20-pin hermetic and molded DIP packages

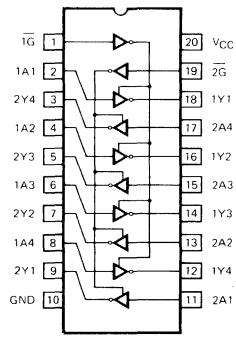
FUNCTIONAL DESCRIPTION

These octal buffers/line drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers provide improved PC board density. The outputs have 40mA sink and 10mA source capability which allow operation with 130Ω bus termination to V_{CC}. Schmitt trigger inputs are on all bus drivers (0.2V minimum guaranteed noise margin). All data inputs offer one LPS unit load.

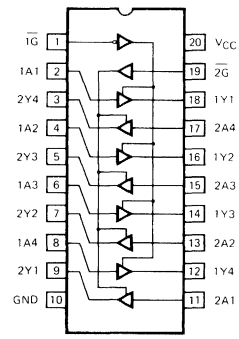
The Am25LS240 and Am25LS241 have four buffers which are enabled from one common line, and the other four buffers are enabled from another common line. The Am25LS240 is inverting, while the Am25LS241 presents true data at the outputs.

LOGIC DIAGRAMS

Am25LS240



Am25LS241



ORDERING INFORMATION

Package Type	Temperature Range	Am25LS240 Order Number	Am25LS241 Order Number
Hermetic DIP	−55°C to +125°C	AM25LS240DM	AM25LS241DM
Dice	−55°C to +125°C	AM25LS240XM	AM25LS241XM
Hermetic DIP	0°C to +70°C	AM25LS240DC	AM25LS241DC
Molded DIP	0°C to +70°C	AM25LS240PC	AM25LS241PC
Dice	0°C to +70°C	AM25LS240XC	AM25LS241XC

Am25LS273

8-Bit Register With Clear

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Buffered outputs to eliminate output commutation
- Positive edge-triggered D-type flip-flops
- Common clock and common clear
- Am25LS273 features 8mA sink current over the military temperature range
- Am25LS273 has 50mV improved V_{OL} compared to Am54LS/74LS273
- Am25LS273 features 40MHz clock frequency
- Am25LS273 has 440μA source current at HIGH output
- 100% reliability assurance testing in compliance with MIL-STD-883

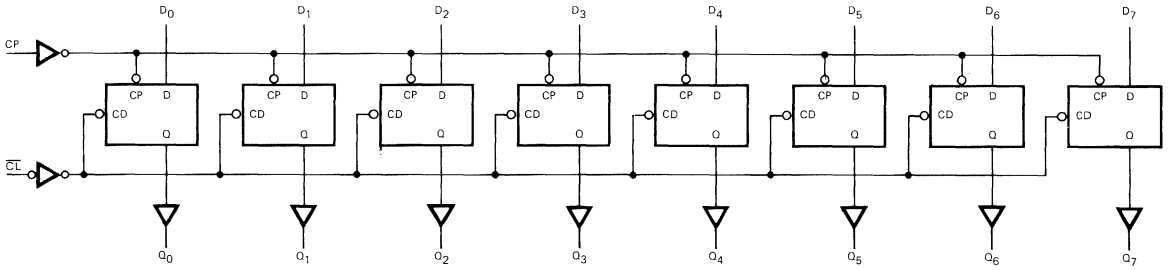
FUNCTIONAL DESCRIPTION

The Am25LS273 and the Am54LS/74LS273 are eight-bit registers built using Advanced Low-Power Schottky Technology. These registers consist of D-type flip-flops with a buffer common clock and an asynchronous active LOW buffered common clear.

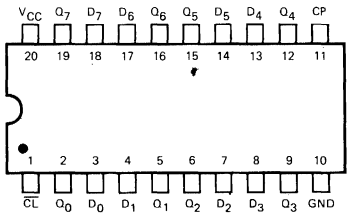
When the clear input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input. These devices are supplied in the 20-pin space saving package featuring 0.3-inch centers between rows of leads.

The Am25LS273 is a high performance version of the Am54LS/74LS273. Improvements include faster A.C. specifications, higher noise margin and twice the fan-out over the military temperature range.

LOGIC DIAGRAM

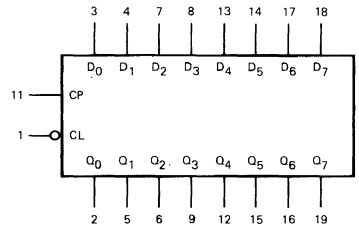


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS373

Octal Latches With Three-State Output

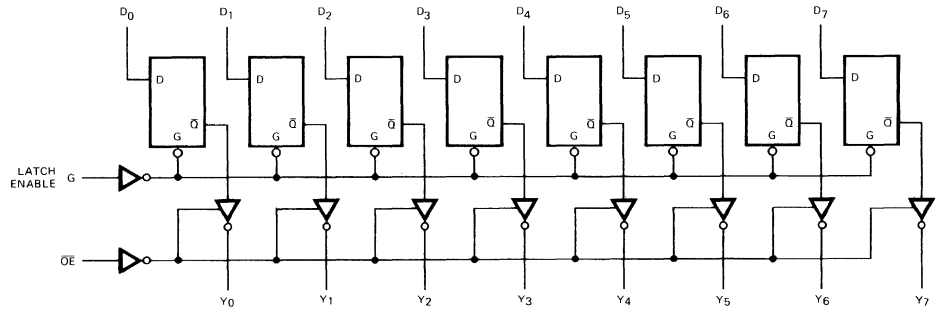
DISTINCTIVE CHARACTERISTICS

- 8 latches in a single package
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- Am25LS features improved noise margin, higher drive and more speed
- 100% reliability assurance testing in compliance with MIL-STD-883

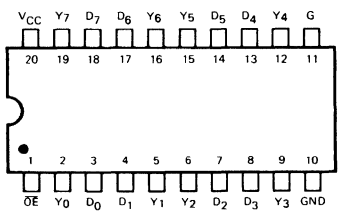
FUNCTIONAL DESCRIPTION

The Am25LS373 and Am54LS/74LS373 are octal latches with three-state outputs for bus organized system applications. The latching flip-flops appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

LOGIC DIAGRAM

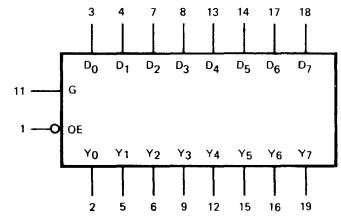


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS374

8-Bit Register With Three-State Outputs

DISTINCTIVE CHARACTERISTICS

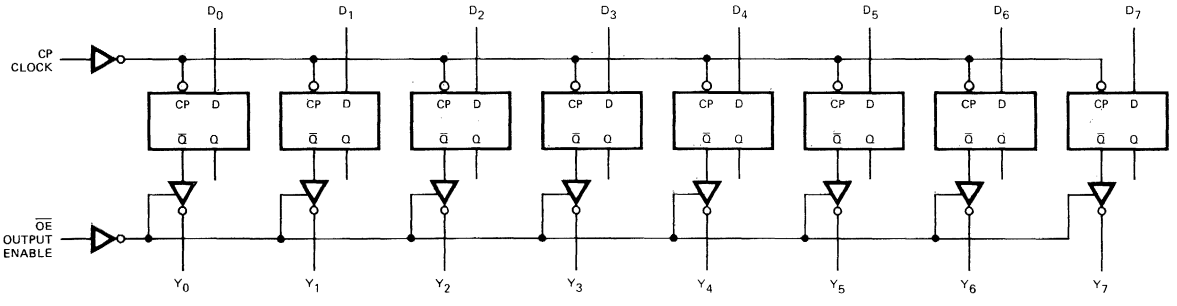
- Eight-bit, high speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Am25LS374 features 8mA sink current over the military temperature range
- Am25LS374 has 50mV improved V_{OL} compared to Am54/74LS374
- Am25LS374 has 440μA HIGH output current
- 100% reliability testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

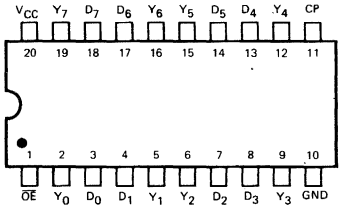
The Am25LS374 and Am54LS/74LS374 are eight-bit registers built using advanced Low-Power Schottky technology. These registers consist of eight D-type flip-flops with a buffered common clock and a buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input. The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. The Am25LS374 is a high-performance version of the Am54LS/74LS374. Improvements include faster AC specifications, higher noise margin and twice the fan-out over the military temperature range.

LOGIC DIAGRAM

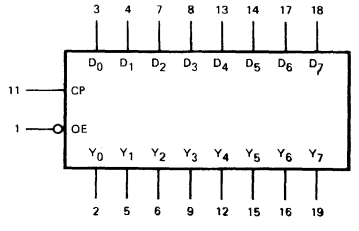


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS377

8-Bit Register With Register Enable

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common clock enable
- Am25LS377 features 8mA sink current over the military temperature range
- Am25LS377 has 50mV improved V_{OL} compared to Am74LS
- Am25LS377 features 40MHz clock frequency
- Am25LS377 has 440μA source current at HIGH output
- 100% reliability assurance testing in compliance with MIL-STD-883

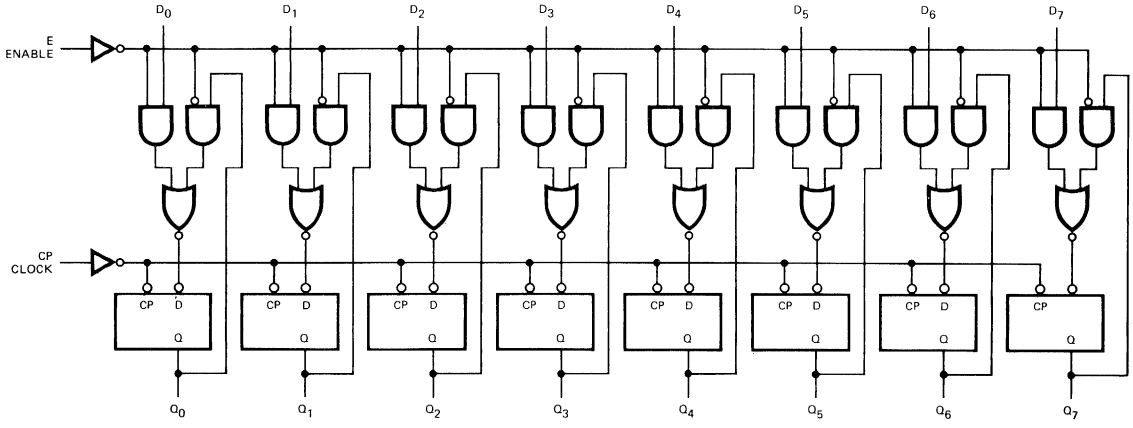
FUNCTIONAL DESCRIPTION

The Am25LS377 and the Am54LS/74LS377 are eight-bit registers built using advanced Low-Power Schottky technology. These registers consist of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

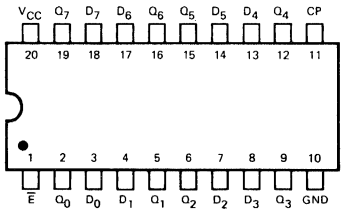
When the clock enable ($\overline{E}$) input is LOW, new data is entered into the flip-flop register on the LOW-to-HIGH transition of the clock input. When the ($\overline{E}$)input is HIGH, the register will retain the present data independent of the clock inputs.

The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. The Am25LS377 is a high-performance version of the Am54LS/74LS377. Improvements include faster switching specifications, higher noise margin, and twice the fan-out over the military temperature range.

LOGIC DIAGRAM

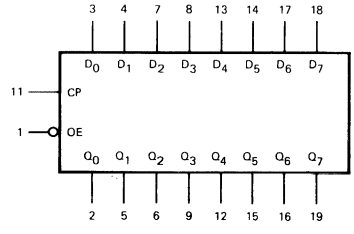


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Chapter 10
ENCODERS AND DECODERS

Am25LS2513 Priority Encoder

The Am25LS2513 is an 8-to-3 priority encoding circuit with 3-state output buffers. It is packaged in a space-saving 20 pin, 300 mil wide package and dissipates only 120mW; the device utilizes Advanced Low-power Schottky processing technology. Because of the combination of encoding and 3-state circuitry, this product can be used directly as an interface between a multiple interrupt I/O system and the 8080A/9080A Data Bus. No other chips are required, since the Am25LS2513 handles the following functions directly:

- Arbitrates priority among contending service requests
- Encodes the highest priority request into a 3-bit binary vector appropriate for the RST instruction
- Generates the interrupt request (INT) input to the processor
- Presents a vector to the Data Bus in response to interrupt acknowledge (INTA) from the processor

Am25LS138 1-Of-8 Decoder
Am25LS139 Dual 1-Of-4 Decoder
Am25LS2537 3-State 1-Of-10 Decoder
Am25LS2538 3-State 1-Of-8 Decoder
Am25LS2539 3-State Dual 1-Of-4 Decoder

These devices are used in microprocessor systems to decode memory and I/O circuit device selects from the Address Bus. They are available in a variety of forms which are easily adapted to many applications.

The Am25LS138 is a conventional 3-to-8 line decoder that is easily expanded. It has active-low 2-state outputs.

The Am25LS139 is a dual 2-to-4 line decoder, also expandable, with active-low 2-state outputs. The two can be used together to provide a wide variety of address selection capabilities.

The Am25LS2538 and Am25LS2539 provide the same type of decoding as their Am25LS138 and Am25LS139 counterparts, but also provide polarity control and 3-state outputs, all in space-saving 20 pin "skinny-dips".

The polarity control allows the output to be specified as either active-low or active-high. This simplifies interfacing with device select inputs of either polarity, and allows an all-low multiple select mode to be achieved.

The Am25LS2537 operates in the same manner as the Am25LS2538, but has two more outputs, thus providing a decade decode function instead of octal.

Data sheets for all five parts are included at the end of this chapter.

USING DECODERS IN DEVICE SELECT LOGIC

The address space of the computer system may be defined by the number of address lines on the microcomputer Address Bus. Thus 8080A/9080A microcomputer systems, having 16 address lines, allow an address space of 65,536 memory bytes ($65,536 = 2^{16}$).

Actual memory blocks may be implemented in units ranging from 256 to 16,384 byte blocks. Thus memory may be visualized as consisting of a number of blocks, each of which is implemented by one, or a group of packages. Each block of memory is a unique memory device. The number of memory devices present in a total memory system will depend on the memory space occupied by individual memory devices and the total memory space required by the entire system. Figure 10-1 illustrates this concept.

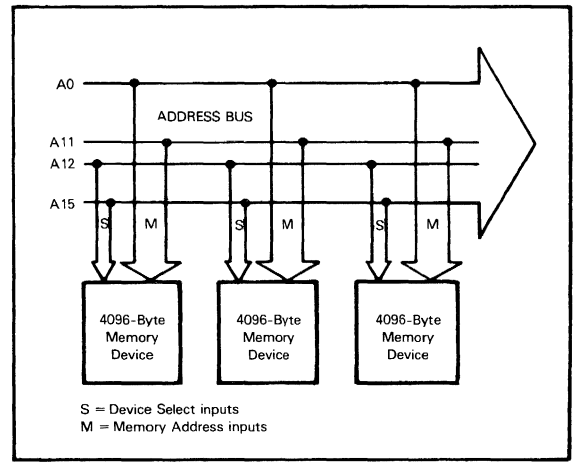


FIGURE 10-1 THE CONCEPT OF MEMORY DEVICES AND ADDRESS SPACES

For any memory, the 16 address lines of the Address Bus may be separated into device select lines and memory address lines. Device select lines are used to decode a master enable for each device block while memory select lines are used to generate memory addresses within a selected memory device.

Figure 10-1 shows blocks of memory each containing 4096 addressable locations. Twelve address lines are required to specify 4096 address locations. There are a total of 16 address

lines on the 8080A/9080A Address Bus, therefore, four address lines remain from which 16 device selects can be generated. This is illustrated in Figure 10-2.

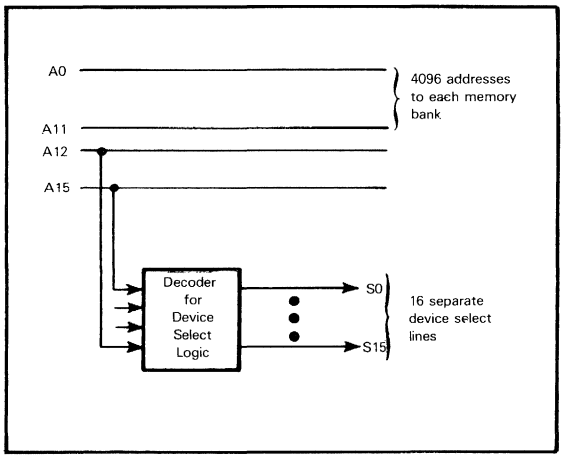


FIGURE 10-2 ADDRESS BUS LINES AND DEVICE SELECT LOGIC

Decoder logic must be used to create device select signals such that one line will be high while the remaining 15 are low. Inputs to the decoder logic then will consist of the four high order address lines which generate 16 different combinations of high and low levels.

Figure 10-3 shows how Am25LS139 1-of-4 decoders may be used in device select logic to create select lines for blocks of memory. The size of a memory block will depend on the level to which devices have been cascaded. Since each Am25LS139 is a 1-of-4 decoder, only two input lines can be selected from the Address Bus. Assuming that the Address Bus has 16 lines, the first level of decode logic can break the total memory space (64K bytes) into quarters or 16K blocks. This can be used with the new 16K x 1 RAM chips. Each of the four select lines created by the first level of decode logic may be used as a simple device select, or it may be input as an enable to the second level of decode logic which, in Figure 10-3, is shown receiving A12 and A13 as address inputs. Thus, the first level decoder may drive up to four second level decoders. Each output from a second level decoder selects a 4K block of memory for 4K x 1 RAMs — static or dynamic — and two 2K x 8 ROMs.

Third level decoders may be driven from the outputs of the second level decoders. Each third level decoder will address one quarter of the second level decoder's address space, which is 1024 addressable locations. This is useful when using 1024 (1K) byte memory devices, implemented as 1K x 8 ROMs, 1K x 1 RAMs, 1K x 4 RAMs, etc.

In many microcomputer systems, memory will be implemented in blocks of different sizes. For example, read only memory may be present in 8K, 4K, 2K, or 1K byte blocks, while read/write memory may be present in 16K, 4K, 1K or 256-byte blocks.

Figure 10-4 shows how 1-of-4 and 1-of-8 decoders may be mixed in order to create device select lines for various sizes of memory blocks. The only significant difference between logic illustrated in Figures 10-4 and 10-5, is the mix of memory block sizes. Notice that G1, the enable input to the 1-of-8 decoders, is used in Figure 10-5 as a means of switching devices on and off based on the status of the high order address line.

The device select network in Figure 10-6 illustrates how a 1-of-4 decoder can be used at the first level of decode logic with 1-of-8 decoders at the second level of decode logic.

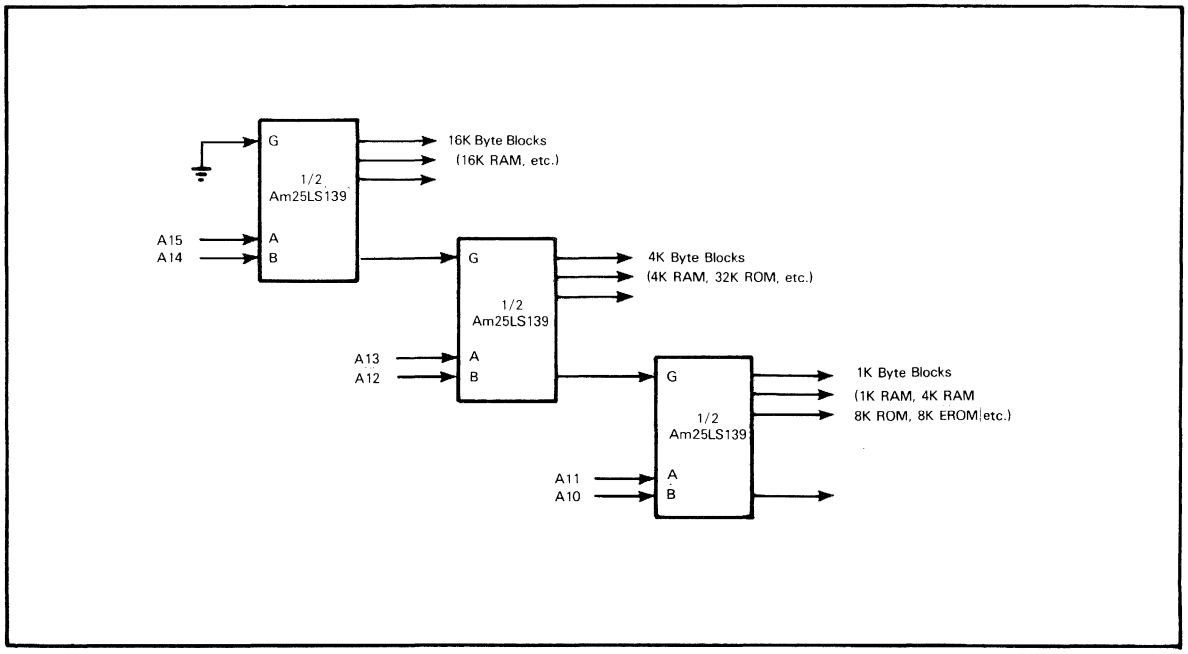


FIGURE 10-3 Am25LS139 DEVICE SELECT NETWORK

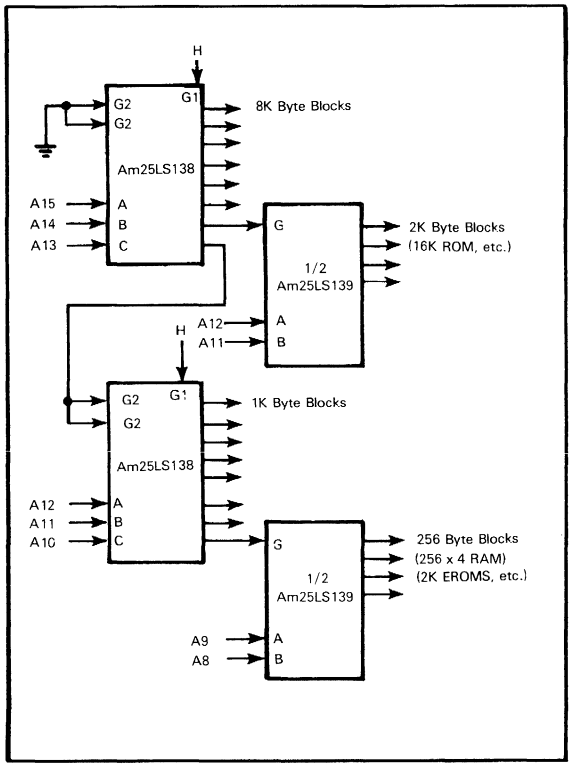


FIGURE 10-4 1-OF-8 AND 1-OF-4 DECODERS IN A DEVICE SELECT NETWORK

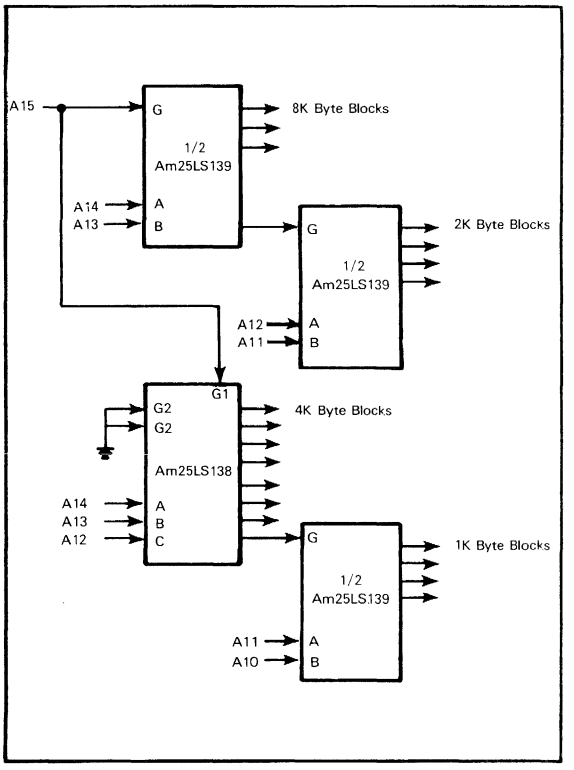


FIGURE 10-5 ANOTHER MIXED 1-OF-8 AND 1-OF-4 DECODER NETWORK FOR DEVICE SELECT LOGIC

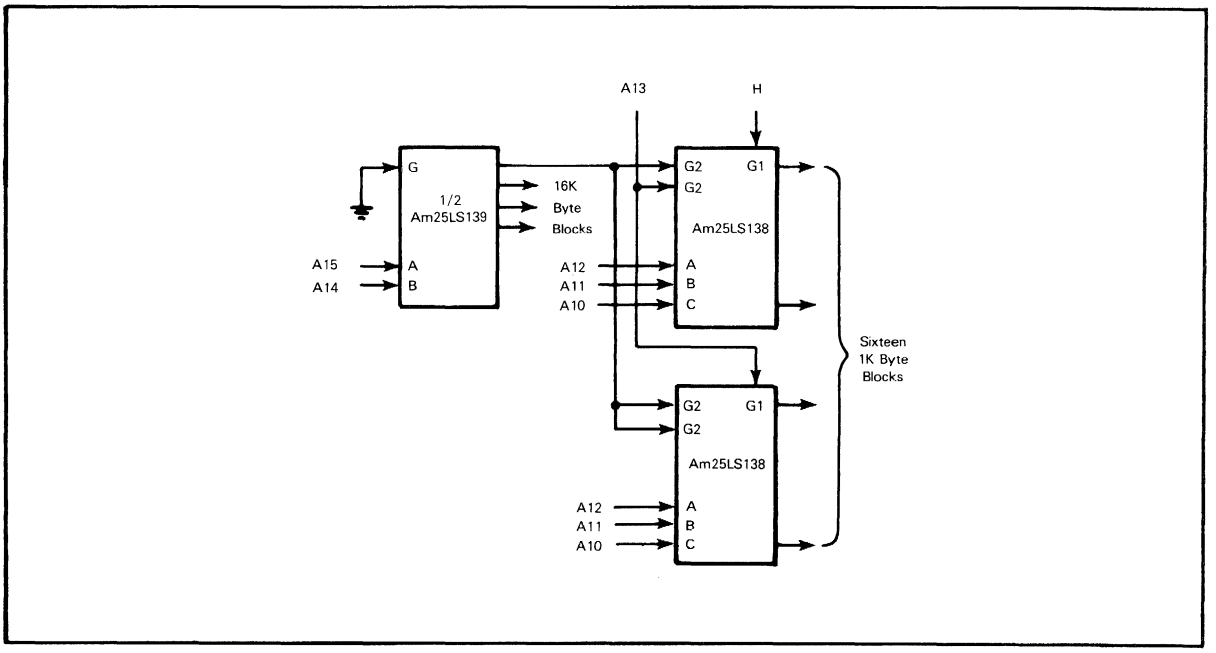


FIGURE 10-6 1-OF-8 DECODERS DRIVEN BY A 1-OF-4 DECODER IN A DEVICE SELECT NETWORK

Am25LS2513

Three-State Priority Encoder

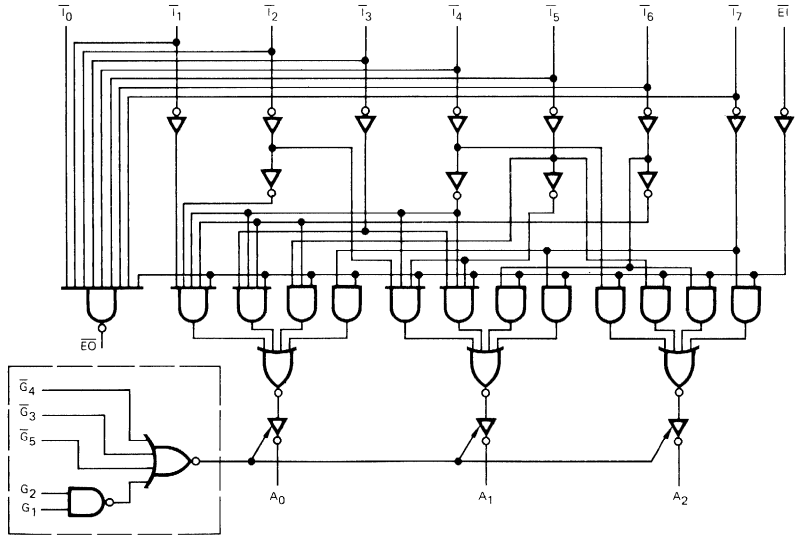
DISTINCTIVE CHARACTERISTICS

- Encodes eight lines to three-line binary
- Expandable
- Cascadable
- Three State version of Am54LS/74LS/25LS148
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

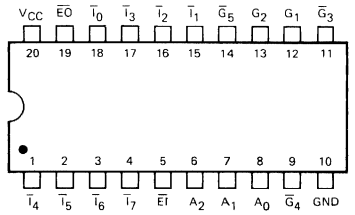
FUNCTIONAL DESCRIPTION

The Am25LS2513 Low-Power Schottky Priority Encoder performs priority encoding of 8 inputs to provide a binary-weighted code of the priority order of the 3 tri-state active HIGH outputs A_0, A_1, A_2. Three active LOW and two active HIGH inputs in AND-OR configuration allow control of the tri-state outputs. The use of the input enable ($\overline{EI}$) combined with the enable output ($\overline{EO}$) permits cascading without additional circuitry. Enable input ($\overline{EI}$) HIGH will force all outputs LOW subject to the tri-state control. The enable output is LOW when all inputs $\overline{I}_0$ through $\overline{I}_7$ are HIGH and the enable input is LOW.

LOGIC DIAGRAM

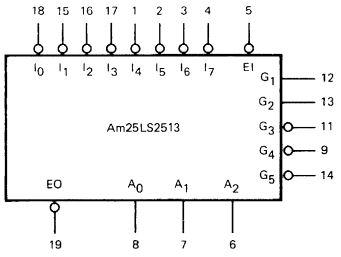


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



Am25LS138

3-Line To 8-Line Decoder/Demultiplexer

Distinctive Characteristics

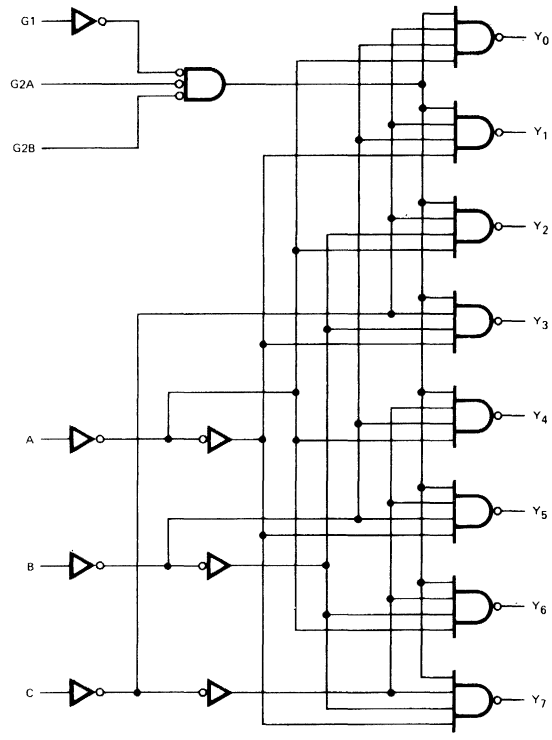
- Higher Speed compared to Am54LS/74LS
- Inverting and non-inverting enable inputs
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to Am74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am25LS138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

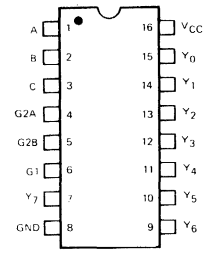
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS138PC
Dice	0°C to +70°C	AM25LS138XC
Hermetic DIP	−55°C to +125°C	AM25LS138DM
Hermetic Flat Pak	−55°C to +125°C	AM25LS138FM
Dice	−55°C to +125°C	AM25LS138XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25LS139

Dual 2-Line To 4-Line Decoder/Demultiplexer

Distinctive Characteristics

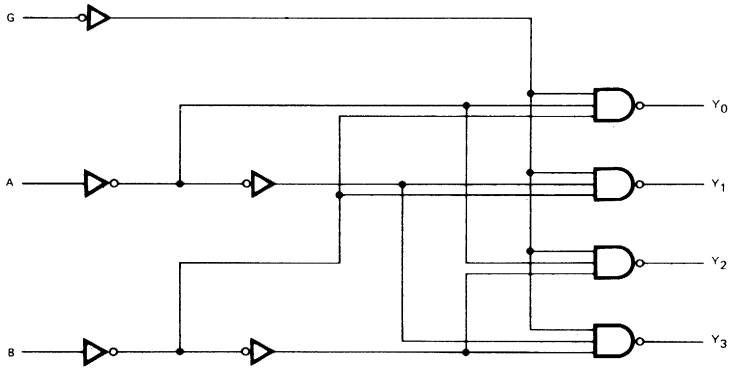
- Higher speed compared to Am54LS/74LS
- Two independent decoders/demultiplexers
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to Am74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am25LS139 is a dual 2-line to 4-line decoder/demultiplexer unit fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs A and B which are decoded to one of four Y outputs.

An active LOW enable can be used for gating or can be used as a data input for demultiplexing applications. When the enable is HIGH, all four Y outputs are HIGH, regardless of the A and B inputs.

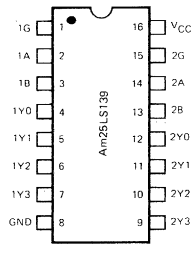
LOGIC DIAGRAM
(One Decoder Shown)



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS139PC
Hermetic DIP	0°C to +70°C	AM25LS139DC
Dice	0°C to +70°C	AM25LS139XC
Hermetic DIP	–55°C to +125°C	AM25LS139DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS139FM
Dice	–55°C to +125°C	AM25LS139XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

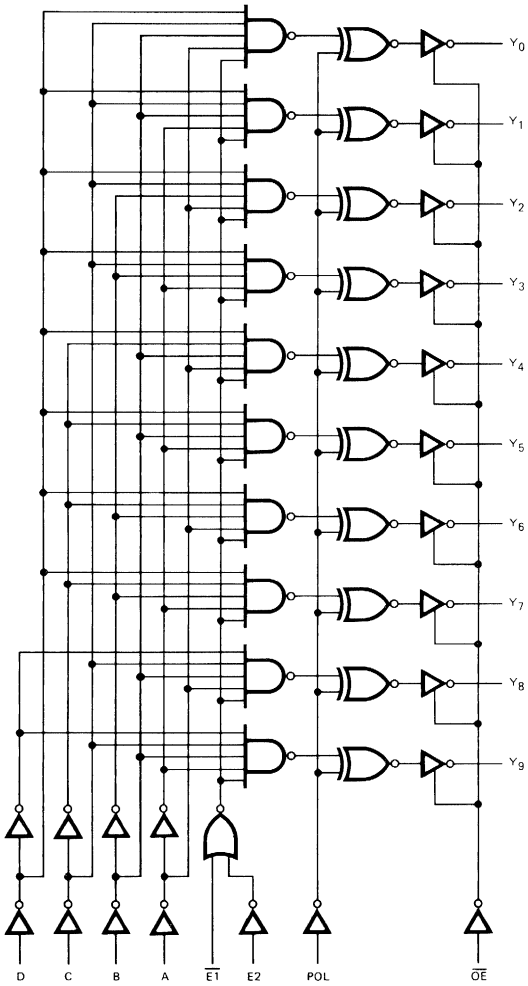
Am25LS2537

One-Of-Ten Decoder With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state outputs
- Separate output polarity control
- Inverting and non-inverting enable inputs
- Does not respond to codes above nine
- Am25LS family has improved sink current, source current, and higher noise margin
- 100% reliability assurance testing in compliance with MIL-STD-883

LOGIC DIAGRAM



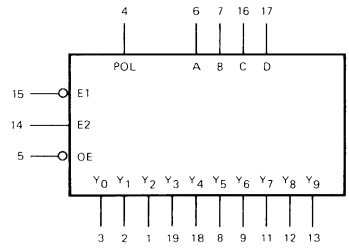
FUNCTIONAL DESCRIPTION

The Am25LS2537 is a demultiplexer/one-of-ten decoder that accepts four active high BCD inputs and selects one-of-ten mutually exclusive outputs. The device features three-state outputs as well as a buffered common polarity control such that the outputs are mutually exclusive active-low or mutually exclusive active-high. The logic design of the Am25LS2537 ensures that all outputs are unselected when the binary codes greater than nine are applied to the inputs. The inputs A, B, C, and D of the Am25LS2537 correspond to the respective binary weight of 1, 2, 4, and 8.

The output enable ($\overline{OE}$) input controls the three-state outputs. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the outputs are enabled. The polarity (POL) input is used to drive the Y outputs to either the active-HIGH state or the active-LOW state. When the POL input is LOW, the outputs are active-HIGH. When the POL input is HIGH, the Y outputs are active-LOW. The device features one active-HIGH and one active-LOW enable input which can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

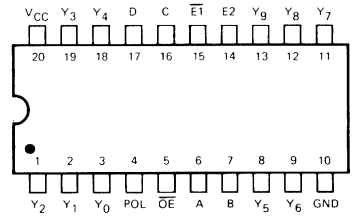
The Am25LS2537 is packaged in a space saving (0.3-inch row spacing) 20-pin package. The device also features Am25LS family faster switching specifications, higher noise margin, and twice the fan-out over the military temperature range.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am25LS2538

One-of-Eight Decoder With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- Am25LS family has improved sink current, source current, and noise margin characteristics
- 100% reliability assurance testing in compliance with MIL-STD-883

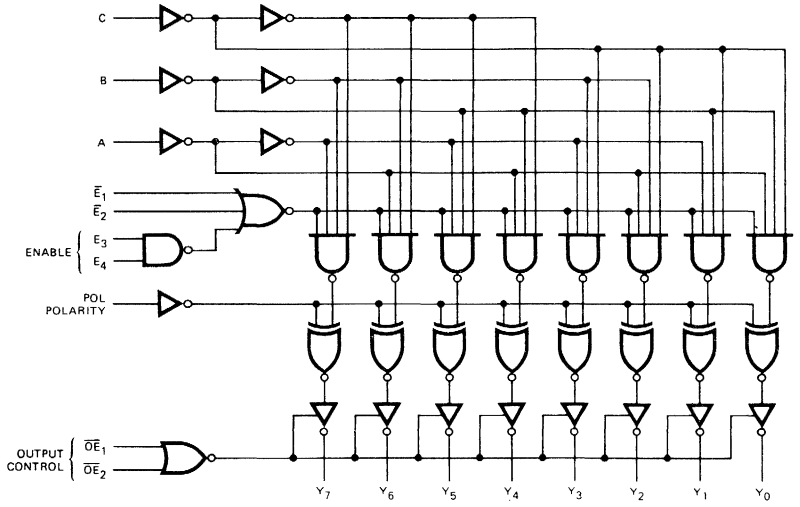
FUNCTIONAL DESCRIPTION

The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs—A, B, and C—that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

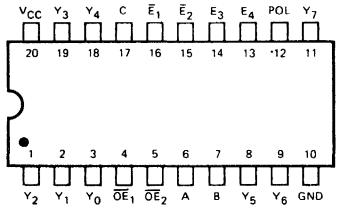
A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features Am25LS family improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range.

LOGIC DIAGRAM
One-of-Eight Decoder

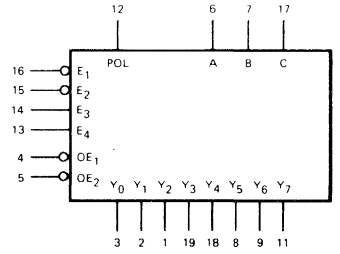


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS2539

Dual One-Of-Four Decoder With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

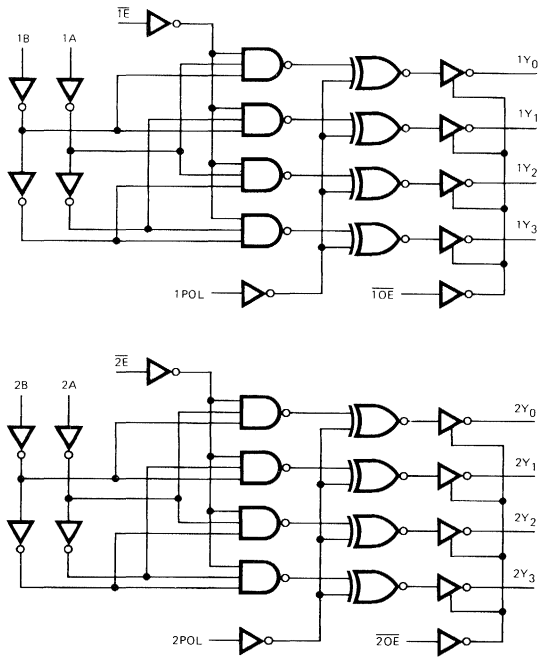
- Two independent decoders/demultiplexers
- Three-state outputs
- Buffered common polarity control
- Am25LS family has improved sink current, source currents, and noise margin characteristics
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

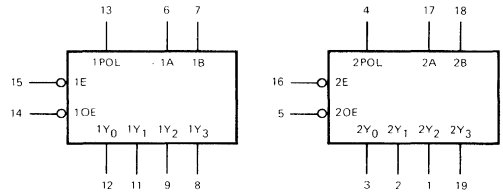
The Am25LS2539 is a dual two-line to four-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs—A and B which are decoded to one-of-four Y outputs. An enable input ($\overline{E}$) is used for gating or can be used as a data input for demultiplexing applications. When the enable input goes HIGH, all four decoder functions are inhibited.

An output enable ($\overline{OE}$) input is used to control the three-state outputs of the device. When the $\overline{OE}$ input is LOW, the outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance (off) state. The device also has separate buffered polarity (POL) inputs to force the outputs to either an active-HIGH state or an active-LOW state. When the POL input is LOW, the outputs are active-HIGH and when the POL input is HIGH, the outputs are active-LOW. The device is packaged in a space saving (0.3 inch row spacing) 20-pin package. The device features Am25LS family improved switching specification, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

LOGIC DIAGRAM

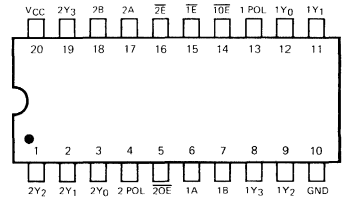


LOGIC SYMBOLS



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Chapter 11
MEMORIES

The principles of memory system design are covered elsewhere in this handbook. Presented in this chapter are data sheets for the following memories:

Read/Write Memory

Static

Am9101, 91L01	256x4	22-pin
Am9102, 91L02	1Kx1	16-pin
Am9111, 91L11	256x4	18-pin
Am9112, 91L12	256x4	16-pin
Am9130, 91L30	1Kx4	22-pin
Am9131, 91L31	1Kx4	22-pin
Am9140, 91L40	4Kx1	22-pin
Am9141, 91L41	4Kx1	22-pin
Am9135	1Kx4	18-pin
Am9145	4Kx1	18-pin

Dynamic

Am9050	4Kx1	18-pin
Am9060	4Kx1	22-pin

Read Only Memory

Mask Programmed

Am9208	1Kx8	24-pin
Am9216	2Kx8	24-pin
Am9217/8316A	2Kx8	24-pin
Am9218/8316E	2Kx8	24-pin

Erasable

Am1702A	256x8	24-pin
Am2708	1Kx8	24-pin

Am9101/Am91L01/Am2101 FAMILY

256x4 Static R/W Random Access Memories

PART NUMBER	Am2101	Am2101-2	Am9101A Am91L01A Am2101-1	Am9101B Am91L01B	Am9101C Am91L01C	Am9101D	Am9101E
ACCESS TIME	1000ns	650ns	500ns	400ns	300ns	250ns	200ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- Low operating power
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply —
  tolerances: ±5% commercial, +10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Two chip enable inputs
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

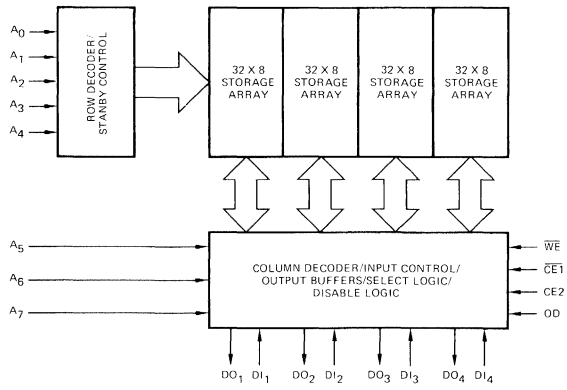
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84 percent of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the stand-by mode.

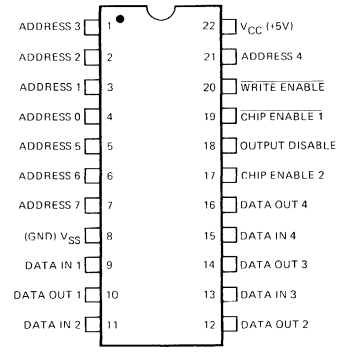
The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9101 BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Flat Pack version available in 24-pin package.

ORDERING INFORMATION

AMBIENT TEMPERATURE SPECIFICATION	PACKAGE TYPE	POWER TYPE	ACCESS TIMES						
			1000ns	650ns	500ns	400ns	300ns	250ns	200ns
0°C to +70°C	Molded DIP	Standard	P2101	P2101-2	P2101-1 AM9101APC	AM9101BPC	AM9101CPC	AM9101DPC	AM9101EPC
		Low			AM91L01APC	AM91L01BCP	AM91L01CPC		
	Hermetic DIP	Standard	C2101	C2101-2	C2101-1 AM9101ADC	AM9101BDC	AM9101CDC	AM9101DDC	AM9101EDC
		Low			AM91L01ADC	AM91L01BDC	AM91L01CDC		
−55°C to +125°C	Hermetic DIP	Standard			AM9101ADM	AM9101BDM	AM9101CDM		
		Low			AM91L01ADM	AM91L01BDM	AM91L01CDM		
	Hermetic Flat Pack	Standard			AM9101AFM	AM9101BFM			
		Low			AM91L01AFM	AM91L01BFM			

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9101PC, Am9101DC, Am91L01PC, Am91L01DC, Am2101 — T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%

Parameters	Description	Test Conditions			Am9101/Am91L01 Family Min.	Am9101/Am91L01 Family Max.	Am2101 Family Min.	Am2101 Family Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.		I_{OH} = −200μA	2.4				Volts
				I_{OH} = −150μA			2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN.		I_{OL} = 3.2mA		0.4			Volts
				I_{OL} = 2.0mA				0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.2	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.25V				10		10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		5.0		15	μA
				V_{OUT} = 0.4V		−10		−50	
I_{CC1}	Power Supply Current	Data out open, V_{CC} = Max., $V_{IN} = V_{CC}$	T_A = 25°C	Am9101A/B		50		60	mA
				Am9101C/D/E		55			
				Am91L01A/B		31			
				Am91L01C		34			
I_{CC2}			T_A = 0°C	Am9101A/B		55		70	
				Am9101C/D/E		60			
				Am91L01A/B		33			
				Am91L01C		36			

ELECTRICAL CHARACTERISTICS

Am9101DM, Am9101FM, Am91L01DM, Am91L01FM — T_A = −55°C to +125°C, V_{CC} = +5.0V ±10%

Parameters	Description	Test Conditions			Am9101/Am91L01 Family Min.	Am9101/Am91L01 Family Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA		V_{CC} = 4.75V	2.4		Volts
				V_{CC} = 4.5V	2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.5V				10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		10	μA
				V_{OUT} = 0.4V		−10	
I_{CC1}	Power Supply Current	Data out open, V_{CC} = Max., $V_{IN} = V_{CC}$	T_A = 25°C	Am9101A/B		50	mA
				Am9101C		55	
				Am91L01A/B		31	
				Am91L01C		34	
I_{CC3}			T_A = −55°C	Am9101A/B		60	
				Am9101C		65	
				Am91L01A/B		37	
				Am91L01C		40	

CAPACITANCE

Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	T_A = 25°C, f = 1 mHz	Am2101	4.0	8.0	pF
			Am9101/Am91L01	3.0	6.0	
C_{OUT}	Output Capacitance, V_{OUT} = 0V		Am2101	8.0	12	pF
			Am9101/Am91L01	6.0	9.0	

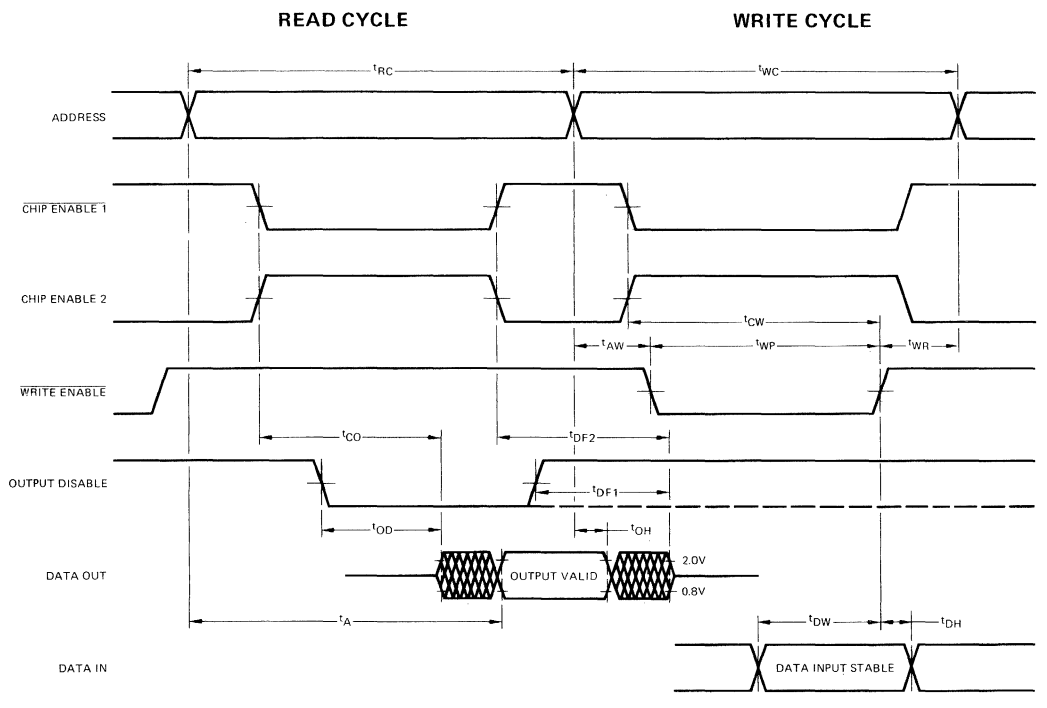
SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate +100pF — $T_A = 0°C$ to $+70°C$ — $V_{CC} = +5V \pm 5\%$
Transition Times = 10ns — $T_A = -55°C$ to $+125°C$ — $V_{CC} = +5V \pm 10\%$
Input Levels, Output References = 0.8V and 2.0V

Parameters	Description	2101		2101-2		2101-1		9101A 91L01A		9101B 91L01B		9101C 91L01C		9101D		9101E		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	1000		650		500		500		400		300		250		200		ns
t_A	Access Time		1000		650		500		500		400		300		250		200	ns
t_{CO}	Chip Enable to Output ON Delay (Note 1)		800		400		350		200		175		150		125		100	ns
t_{OD}	Output Disable to Output ON Delay		700		350		300		175		150		125		100		85	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		40		40		40		30		30		ns
t_{DF1}	Output Disable to Output OFF Delay	0	200	0	150	0	150	5.0	125	5.0	100	5.0	100	5.0	75	5.0	60	ns
t_{DF2}	Chip Enable to Output OFF Delay	0	200	0	150	0	150	10	125	10	125	10	100	10	100	10	80	ns
t_{WC}	Write Cycle Time	1000		650		500		500		400		300		250		200		ns
t_{AW}	Address Set-up Time	150		150		100		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	750		400		300		175		150		125		100		85		ns
t_{CW}	Chip Enable Set-up Time (Note 1)	900		550		400		175		150		125		100		85		ns
t_{WR}	Address Hold Time	50		50		50		0		0		0		0		0		ns
t_{DW}	Input Data Set-up Time	700		400		280		150		125		100		85		65		ns
t_{DH}	Input Data Hold Time	100		100		100		0		0		0		0		0		ns

Notes: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

SWITCHING WAVEFORMS



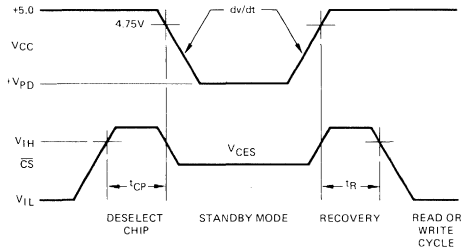
POWER DOWN STANDBY OPERATION

The Am9101/Am91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

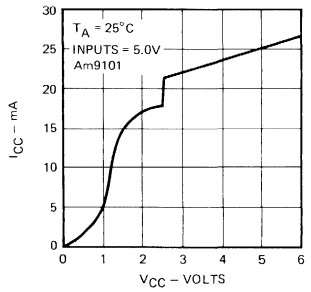
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

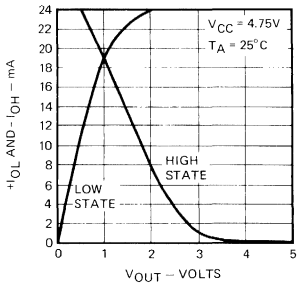
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L01		11	25	mA
				Am9101		13	31	
			$V_{PD} = 2.0V$	Am91L01		13	31	
				Am9101		17	41	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L01		11	28	mA
				Am9101		13	34	
			$V_{PD} = 2.0V$	Am91L01		13	34	
				Am9101		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



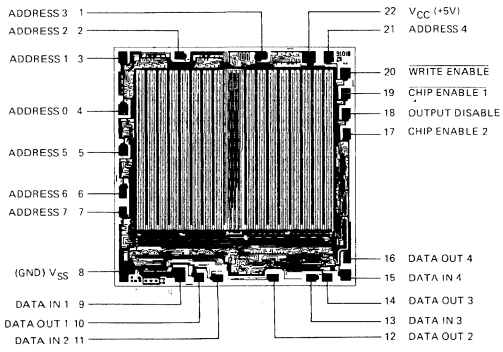
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage



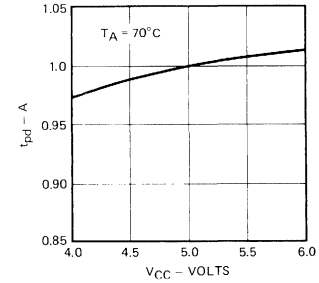
Metallization and Pad Layout



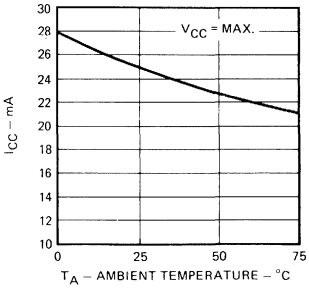
DIE SIZE 0.132" X 0.131"

(Pin numbers are for DIP configurations only)

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE1}$, CE2 Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ is low and CE2 is high.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{OD} Output enable time. Delay time from falling edge of OD to output on.

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH} Minimum time which will elapse between change of address and any change of the data output.

t_{DF1} Time delay between output disable HIGH and output data float.

t_{DF2} Time delay between chip enable OFF and output data float.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

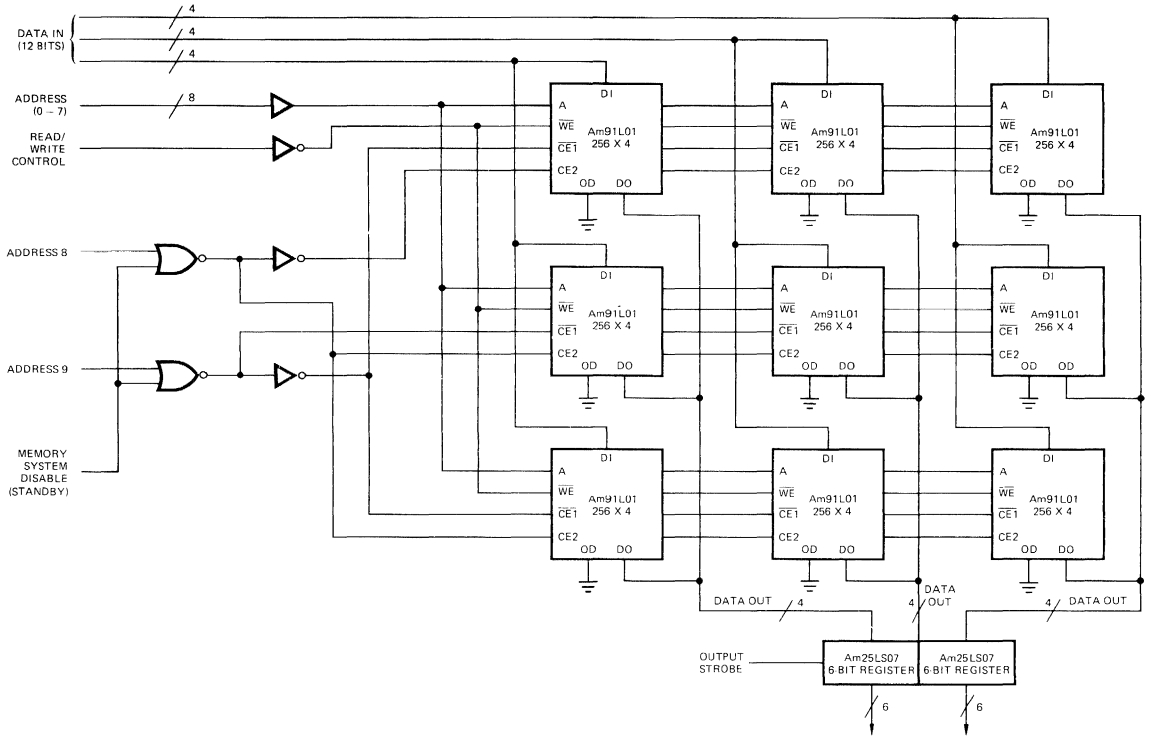
t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

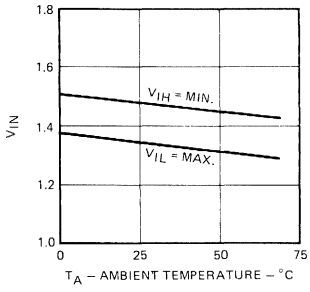
t_{CW} Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

APPLICATIONS

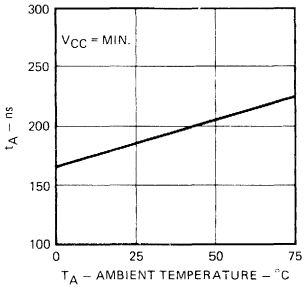


MEMORY SYSTEM
768 WORDS BY 12 BITS PER WORD

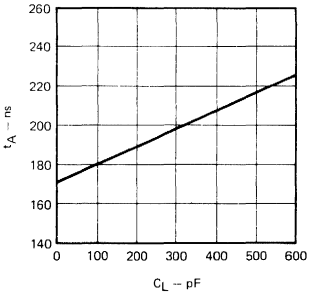
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature

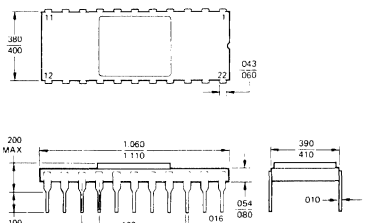


Typical t_A Versus C_L

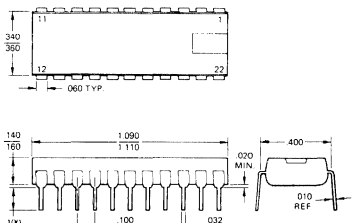


PHYSICAL DIMENSIONS
Dual-In-Line

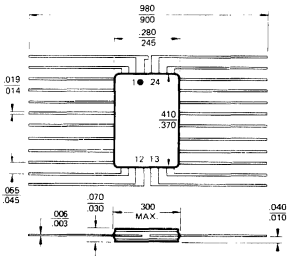
22-Pin Side-Brazed



22-Pin Molded



24-Pin Flat Package



Am9102/Am91L02 FAMILY

1024x1 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Low-Power Dissipation
  100 mW typical; 260 mW maximum
- Standby operating mode reduces power 84%
  18 mW typical; 42 mW maximum
- Input and output voltage levels identical to TTL
- High-Output Drive – Two full TTL loads guaranteed
- High Noise Immunity – 400 mV guaranteed
- Uniform Access Times
  Switching characteristics are insensitive to data patterns, addressing patterns, and power supply variations
- Single 5-Volt Power Supply
  10% tolerance for full temperature range devices
  5% tolerance for commercial range devices
- High-Performance Plug-In Replacement for: Intel 2102, Signetics 2602, Intersil IM7552, Mostek 4102, TI4033/4/5
- Available for operation over both commercial and military ranges
- 100% reliability assurance testing in accordance with MIL-STD-883
- Zero data hold and address hold times simplify timing requirements

FUNCTIONAL DESCRIPTION

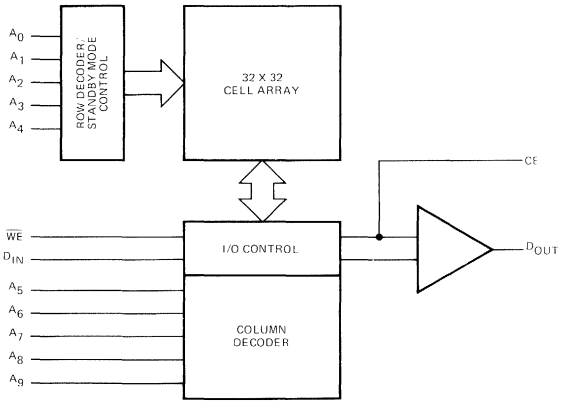
The Am9102 Family of 1024-bit static N-channel RAMs contains members with cycle times ranging from 650ns to 200ns All the devices are organized as 1024 x 1, and all have a power-saving standby operating mode.

Each device has a chip enable input (CE) that controls a three-state output to make construction of large memory systems simple. Reading and writing are performed by enabling the chip and applying a LOW to write or a HIGH to read on the write enable input ($\overline{WE}$). All inputs are directly TTL compatible with no external components required, and the output will drive two full TTL loads in both the HIGH and LOW states.

The devices operate from a single +5 volt power supply. The power dissipation of the devices can be reduced to about 16% of the normal operating power by lowering the voltage on the power supply pin. Data is guaranteed to be retained in the power-down condition.

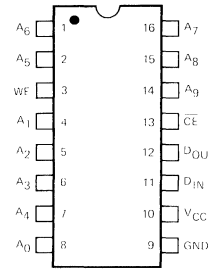
All unit members in the family are available in plastic or hermetic DIPs for operation over the commercial temperature range and, except for the Am9102D/E, may all also be purchased for operation over the military temperature range. All AC and DC parameters are guaranteed over the operating range.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

AMBIENT TEMPERATURE	PACKAGE TYPE	POWER TYPE	ACCESS TIMES					
			650ns	500ns	400ns	300ns	250ns	200ns
0°C ≤ T_A ≤ +70°C	Molded DIP	Standard	AM9102PC	AM9102APC	AM9102BPC	AM9102CPC	AM9102DPC	Am9102EPC
		Low	AM91L02PC	AM91L02APC	AM91L02BPC	AM91L02CPC		
	Hermetic DIP	Standard	AM9102DC	AM9102ADC	AM9102BDC	AM9102CDC	AM9102DDC	Am9102EDC
		Low	AM91L02DC	AM91L02ADC	AM91L02BDC	AM91L02CDC	AM91L01CDC	
−55°C to +125°C	Hermetic DIP	Standard	AM9102DM	AM9102ADM	AM9102BDM	AM9102CDM	AM9101CDM	
		Low	AM91L02DM	AM91L02ADM	AM91L02BDM	AM91L02CDM	AM91L01CDM	
	Hermetic Flat Pack	Standard	AM9102FM	AM9102AFM	AM9102BFM			
		Low	AM91L02FM	AM91L02AFM	AM91L02BFM			

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7V
DC Voltage Applied to Outputs	−0.5V to +7V
DC Input Voltage	−0.5V to +7V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS over operating range

Am91L02PC, Am91L02DC
Am9102PC, Am9102DC
T_A = 0°C to +70°C V_{CC} = +5.0V ±5%

Parameters	Description	Test Conditions			Am9102/A/B Am91L02/A/B Min.	Am9102/A/B Am91L02/A/B Max.	Am9102C Am9102D Am9102E Min.	Am9102C Am9102D Am9102E Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −200μA			2.4		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4		0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0	V_{CC}	2.0	V_{CC}	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			−0.5	0.8	−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., V_{IN} = 0V to 5.25V				10		10	μA
I_{CC1}	Power Supply Current	All inputs = V_{CC} Data out open V_{CC} = MAX.	T_A = 25°C	Am91L02		28		31	mA
				Am9102		45		50	
I_{CC2}			T_A = 0°C	Am91L02		30		33	
				Am9102		50		55	
I_{LO}	Output Leakage Current	$V_{\overline{CS}} = V_{IH}$	$V_{OUT} = V_{CC}$			5.0		5.0	μA
			V_{OUT} = 0.4V			−10		−10	

Am91L02DM, FM
Am9102DM, FM
T_A = −55°C to +125°C V_{CC} = +5.0V ±10%

Parameters	Description	Test Conditions			Am9102/A/B Am91L02/A/B Min.	Am9102/A/B Am91L02/A/B Max.	Am9102C Am91L02C Min.	Am9102C Am91L02C Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA	V_{CC} = 4.75V		2.4		2.4		Volts
			V_{CC} = 4.50V		2.2		2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4		0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0	V_{CC}	2.0	V_{CC}	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			−0.5	0.8	−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., V_{IN} = 0V to 5.5V				10		10	μA
I_{CC1}	Power Supply Current	All inputs = V_{CC} Data out open V_{CC} = MAX.	T_A = 25°C	Am91L02		28		31	mA
				Am9102		45		50	
I_{CC3}			T_A = −55°C	Am91L02		35		37	
				Am9102		55		60	
I_{LO}	Output Leakage Current	$V_{\overline{CS}} = V_{IH}$	$V_{OUT} = V_{CC}$			10		10	μA
			V_{OUT} = 0.4V			−10		−10	

CAPACITANCE (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance, Any Input	V_{IN} = 0V, f = 1MHz		3.0	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1MHz		4.0	6.0	pF

Am9102 FAMILY SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS

over operating temperature and voltage range

Load = 1 TTL gate and 100pF, V_{IL} = 0.8V, V_{IH} = 2.0V, $t_r = t_f$ = 10ns. Output reference level 0.8V, 2.0V

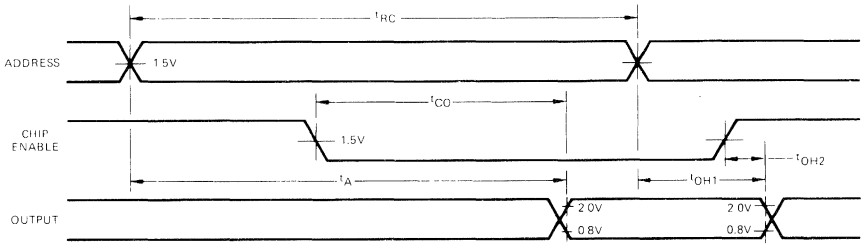
Read Cycle Characteristics		Am9102 Am91L02		Am9102A Am91L02A		Am9102B Am91L02B		Am9102C Am91L02C		Am9102D		Am9102E		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	650		500		400		300		250		200		ns
t_A	Access Time		650		500		400		300		250		200	ns
t_{CO}	$\overline{CE}$ LOW to Output HIGH or LOW		200		175		150		125		100		80	ns
t_{OH1}	Previous Read Data Valid with Respect to Chip Select	50		50		50		50		40		30		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select	0		0		0		0		0		0		ns

Write Cycle Requirements

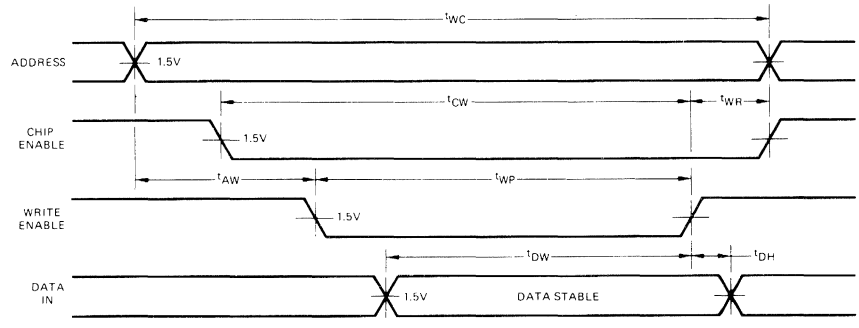
t_{WC}	Write Cycle Time	650		500		400		300		250		200		ns
t_{AW}	Address Set-Up Time	20		20		20		20		20		20		ns
t_{WP}	Write Pulse Width	200		175		150		125		100		80		ns
t_{WR}	Write Recovery Time (Address Hold Time)	0		0		0		0		0		0		ns
t_{DW}	Data Set-Up Time	175		150		125		100		75		60		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{CW}	Chip Enable Set-Up Time	200		175		150		125		100		85		ns

SWITCHING WAVEFORMS

READ CYCLE



WRITE CYCLE



POWER DOWN STANDBY OPERATION

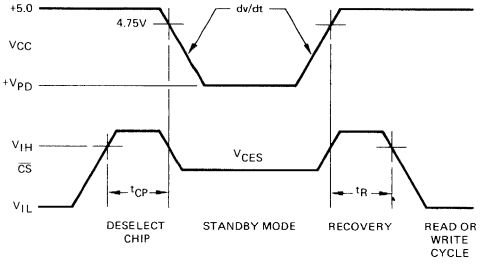
The Am9102 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated back-up power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power.

A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

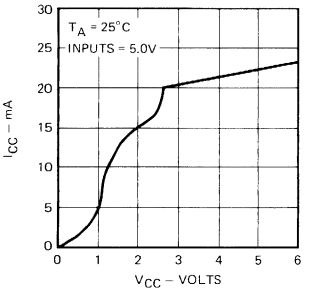
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be raised for the chip disable time (t_{CP}) prior to entering the standby mode, and should be held at V_{PD} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

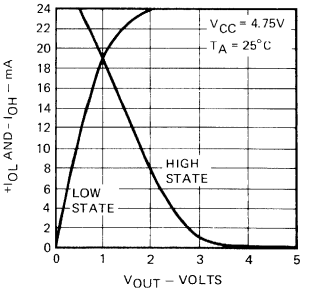
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L02		10	23	mA
				Am9102		12	28	
			$V_{PD} = 2.0V$	Am91L02		12	28	
				Am9102		15	38	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L02		10	26	mA
				Am9102		12	31	
			$V_{PD} = 2.0V$	Am91L02		12	31	
				Am9102		15	42	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				T_{RC}			ns
T_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



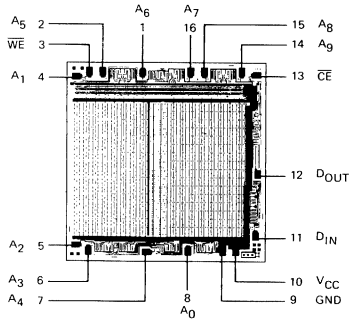
Power Supply Current Versus Voltage



Typical Output Current Versus Voltage

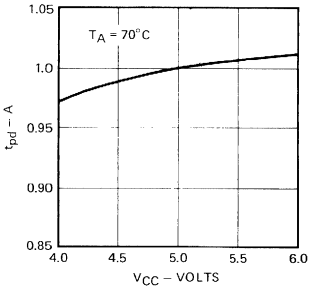


Metallization and Pad Layout

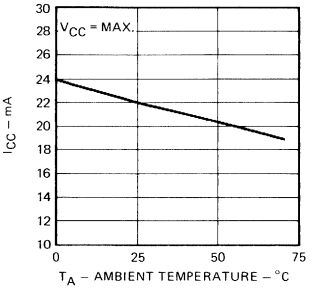


DIE SIZE 0.128" X 0.128"

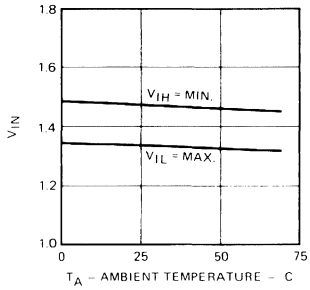
Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



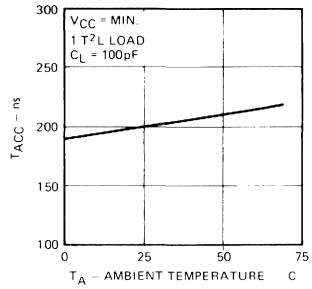
Typical Power Supply Current Versus Ambient Temperature



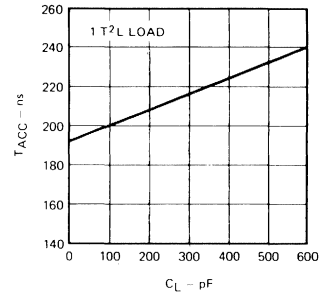
Typical V_{IN} Limits Versus Ambient Temperature



Typical T_{ACC} Versus Ambient Temperature



Typical T_{ACC} Versus C_L



DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE}$ Active LOW chip enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW write enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drains are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH1} Minimum Access Time. Minimum time which will elapse between change of address and any change on the data output.

t_{OH2} Minimum time which will elapse between a change on the chip enable and any change on the data output.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-Up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

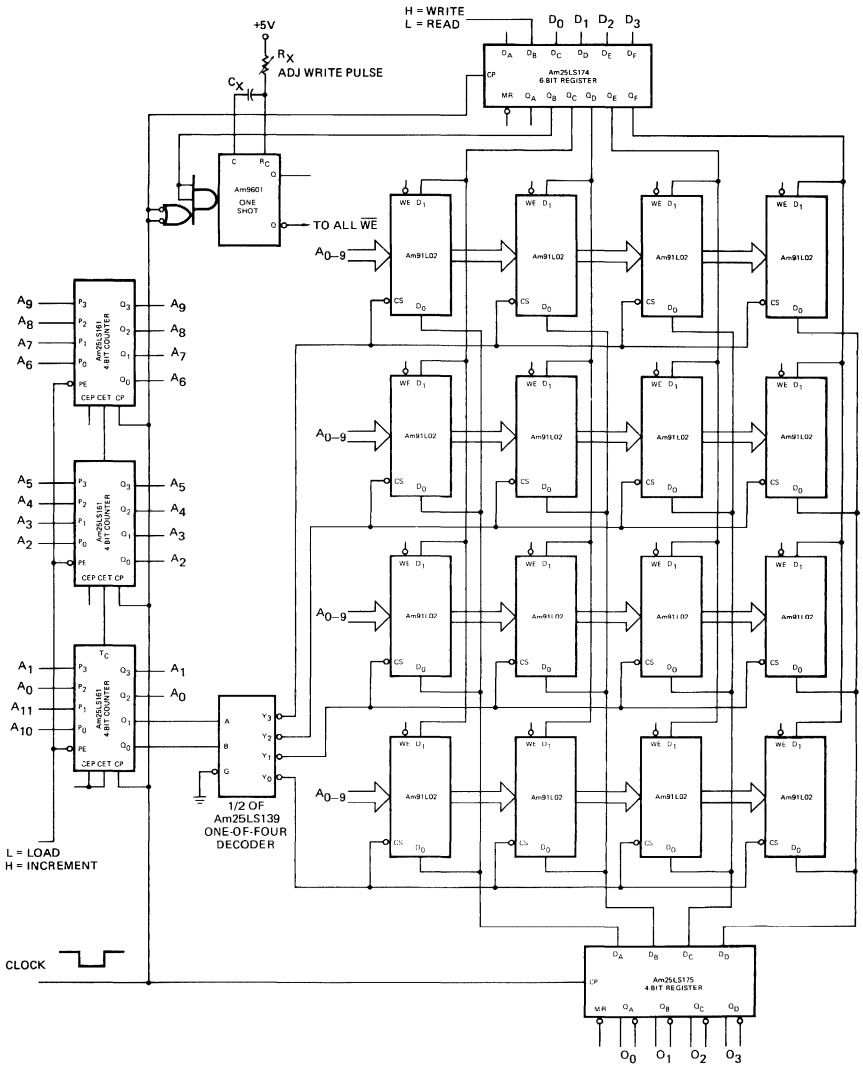
t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-Up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

APPLICATIONS

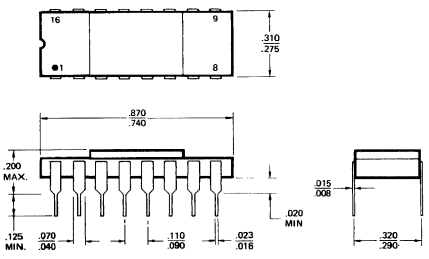


4K WORD BY 4-BIT MEMORY SYSTEM

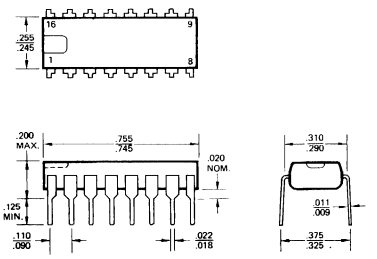
The clock signal HIGH-to-LOW transition fires the one-shot and initiates the write pulse. The write pulse should end 100ns prior to the next clock LOW-to-HIGH transition. On each clock pulse, the data input register is loaded with four bits of data and a read/write bit and the address register is either loaded or incremented. Output data is loaded on the next clock pulse.

PHYSICAL DIMENSIONS
Dual-In-Line

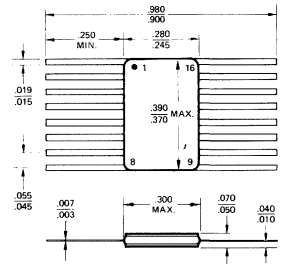
Side-Brazed



Molded



Flat Package



Am9111/Am91L11/Am2111 FAMILY

256x4 Static R/W Random Access Memories

PART NUMBER	Am2111	Am2111-2	Am9111A Am91L11A Am2111-1	Am9111B Am91L11B	Am9111C Am91L11C	Am9111D	AM9111E
ACCESS TIME	1000ns	650ns	500ns	400ns	300ns	250ns	200ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization for small memory systems
- Low operating power dissipation
  125mW Typ; 290mW maximum — standard power
  100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply —
  tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Bussed input and output data on common pins.
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

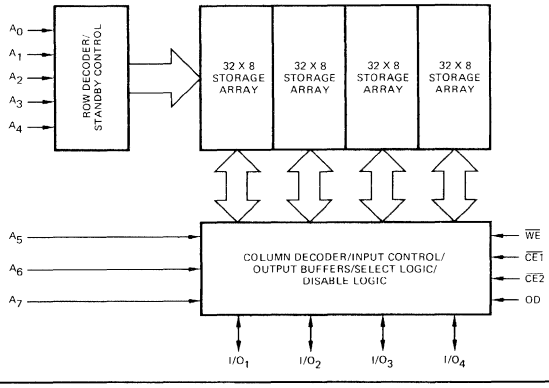
The Am9111/Am91L11 series of devices are high performance, low power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but helps eliminate external logic in bus-oriented memory systems.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

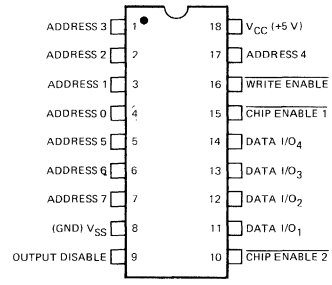
The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9111 BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Flat Pack version available in 24-pin package.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times						
			1000ns	650ns	500ns	400ns	300ns	250ns	200ns
0°C to +70°C	Molded DIP	Standard	P2111	P2111-2	P2111-1 AM9111APC	AM9111BPC	AM9111CPC	AM9111DPC	AM9111EPC
		Low			AM91L11APC	AM91L11BPC	AM91L11CPC		
	Hermetic DIP	Standard	C2111	C2111-2	C2111-1 AM9111ADC	AM9111BDC	AM9111CDC	AM9111DDC	AM9111EDC
		Low			AM91L11ADC	AM91L11BDC	AM91L11CDC		
−55°C to +125°C	Hermetic DIP	Standard			AM9111ADM	AM9111BDM	AM9111CDM		
		Low			AM91L11ADM	AM91L11BDM	AM91L11CDM		
	Hermetic Flat Pack	Standard			AM9111AFM	AM9111BFM			
		Low			AM91L11AFM	AM91L11BFM			

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9111PC, Am9111DC, Am91L11PC, Am91L11DC, Am2111
$T_A = 0°C$ to $+70°C$
$V_{CC} = +5.0V \pm 5\%$

Parameters	Description	Test Conditions			Am9111/ Am91L11 Family Min.	Am9111/ Am91L11 Family Max.	Am2111 Family Min.	Am2111 Family Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.		$I_{OH} = -200\mu A$	2.4				Volts
				$I_{OH} = -150\mu A$			2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN.		$I_{OL} = 3.2mA$		0.4			Volts
				$I_{OL} = 2.0mA$				0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.2	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.25V$				10		10	μA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		5.0		15	μA
				$V_{OUT} = 0.4V$		−10		−50	
I_{CC1}	Power Supply Current	Data out open V_{CC} = Max. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9111A/B		50		60	mA
				Am9111C/D/E		55			
				Am91L11A/B		31			
				Am91L11C		34			
I_{CC2}			$T_A = 0°C$	Am9111A/B		55		70	
				Am9111C/D/E		60			
				Am91L11A/B		33			
				Am91L11C		36			

ELECTRICAL CHARACTERISTICS

Am9111DM, Am9111FM, Am91L11DM, Am91L11FM
$T_A = -55°C$ to $+125°C$
$V_{CC} = +5.0V \pm 10\%$

Parameters	Description	Test Conditions			Am9111/ Am91L11 Family Min.	Am9111/ Am91L11 Family Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$		$V_{CC} = 4.75V$	2.4		Volts
				$V_{CC} = 4.5V$	2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 3.2mA$				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.5V$				10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		10	μA
				$V_{OUT} = 0.4V$		−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = Max. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9111A/Am9111B		50	mA
				Am9111C		55	
				Am91L11A/Am91L11B		31	
				Am91L11C		34	
I_{CC3}			$T_A = -55°C$	Am9111A/Am9111B		60	
				Am9111C		65	
				Am91L11A/Am91L11B		37	
				Am91L11C		40	

CAPACITANCE

Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, $V_{IN} = 0V$	$T_A = 25°C$, f = 1 mHz	Am2111	4.0	8.0	pF
			Am9111/Am91L11	3.0	6.0	
C_{OUT}	Output Capacitance, $V_{OUT} = 0V$		Am2111	10	15	pF
			Am9111/Am91L11	8.0	11	

SWITCHING CHARACTERISTICS over operating and voltage range

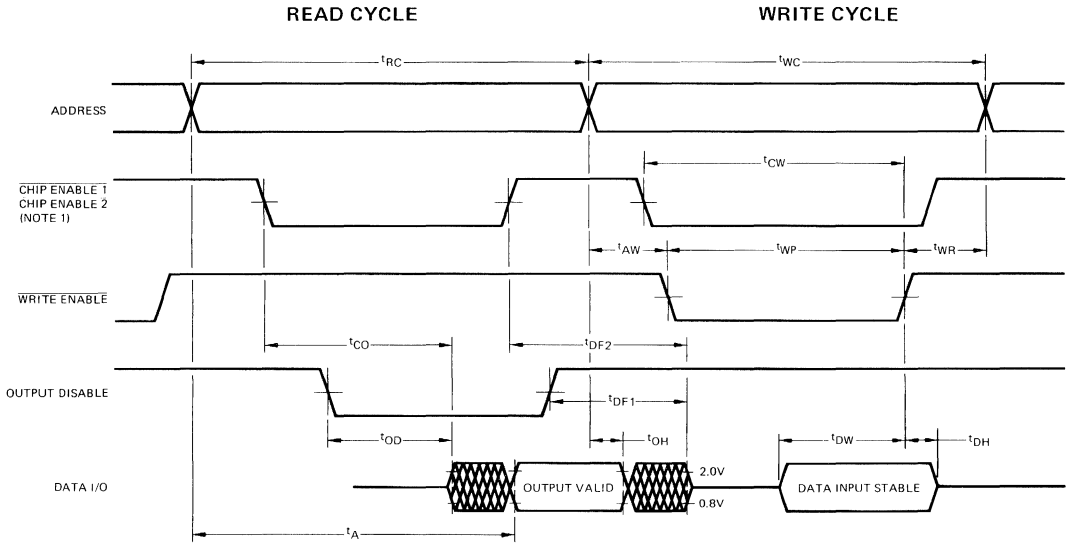
Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

$T_A = 0°C$ to $+70°C$ $V_{CC} = +5V \pm 5\%$
$T_A = -55°C$ to $+125°C$ $V_{CC} = +5V \pm 10\%$

Parameters	Description	2111 Min.	2111 Max.	2111-2 Min.	2111-2 Max.	2111-1 Min.	2111-1 Max.	9111A 91L11A Min.	9111A 91L11A Max.	9111B 91L11B Min.	9111B 91L11B Max.	9111C 91L11C Min.	9111C 91L11C Max.	9111D Min.	9111D Max.	9111E Min.	9111E Max.	Units
t_{RC}	Read Cycle Time	1000		650		500		500		400		300		250		200		ns
t_A	Access Time		1000		650		500		500		400		300		250		200	ns
t_{CO}	Chip Enable to Output ON Delay (Note 1)		800		400		350		200		175		150		125		100	ns
t_{OD}	Output Disable to Output ON Delay		700		350		300		175		150		125		100		85	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		40		40		40		30		30		ns
t_{DF1}	Output Disable to Output OFF Delay	0	200	0	150	0	150	5.0	125	5.0	100	5.0	100	5.0	75	5.0	60	ns
t_{DF2}	Chip Enable to Output OFF Delay	0	200	0	150	0	150	10	150	10	125	10	125	10	100	10	80	ns
t_{WC}	Write Cycle Time	1000		650		500		500		400		300		250		200		ns
t_{AW}	Address Set-up Time	150		150		100		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	750		400		300		175		150		125		100		85		ns
t_{CW}	Chip Enable Set-up Time (Note 1)	900		550		400		175		150		125		100		85		ns
t_{WR}	Address Hold Time	50		50		50		0		0		0		0		0		ns
t_{DW}	Input Data Set-up Time	700		400		280		150		125		100		85		65		ns
t_{DH}	Input Data Hold Time	100		100		100		0		0		0		0		0		ns

Notes: 1. Both $\overline{CE1}$ and $\overline{CE2}$ must be LOW to enable the chip.

SWITCHING WAVEFORMS



DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE1}$, $\overline{CE2}$ Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ and $\overline{CE2}$ are LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if WE is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{OD} Output enable time. Delay time from falling edge of OD to output on.

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH} Minimum time which will elapse between change of address and any change of the data output.

t_{DF1} Time delay between output disable HIGH and output data float.

t_{DF2} Time delay between chip enable OFF and output data float.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

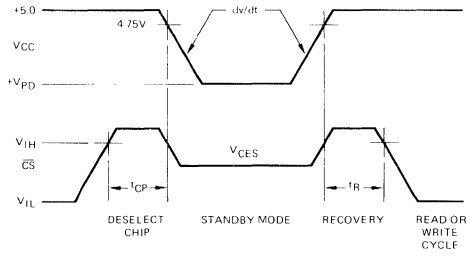
POWER DOWN STANDBY OPERATION

The Am9111/Am91L11 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

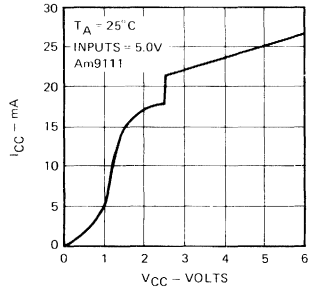
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

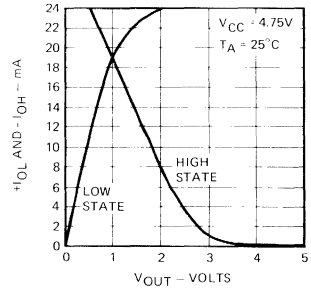
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L11		11	25	mA
				Am9111		13	31	
			$V_{PD} = 2.0V$	Am91L11		13	31	
				Am9111		17	41	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L11		11	28	mA
				Am9111		13	34	
			$V_{PD} = 2.0V$	Am91L11		13	34	
				Am9111		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



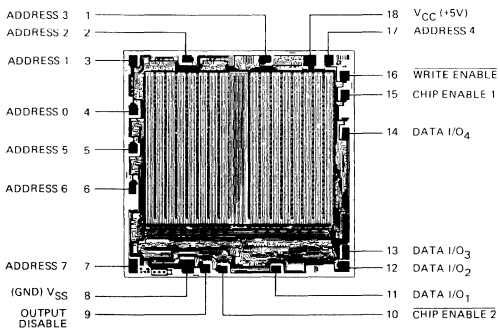
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage



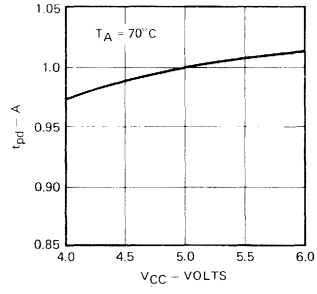
Metallization and Pad Layout



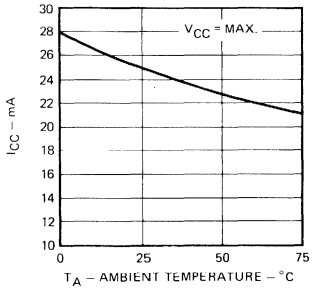
DIE SIZE: 0.132" X 0.131"

(Pin numbers shown are for DIP versions only)

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



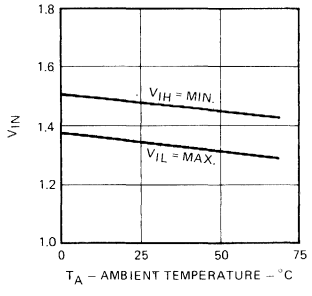
Am9111 FAMILY — APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9111 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

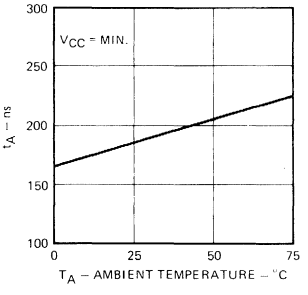
This bussed I/O approach cuts down the package pin count allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9111 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

The Output Disable control signal is provided to prevent signal contention for the bus lines, and to simplify tri-state bus control in the external circuitry. If the chip is enabled and the output is enabled and the memory is in the Read state, then the output buffers will be impressing data on the bus lines. At that point, if the external system tries to drive the bus with data, in preparation for a write operation, there will be conflict for domination of the bus lines. The Output Disable signal allows the user direct control over the output buffers, independent of the state of the memory. Although there are alternative ways to resolve the conflict, normally Output Disable will be held high during a write operation.

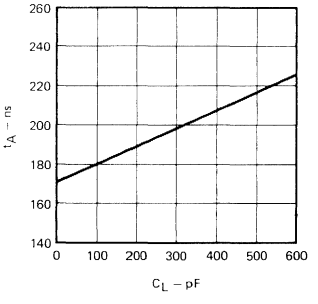
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature

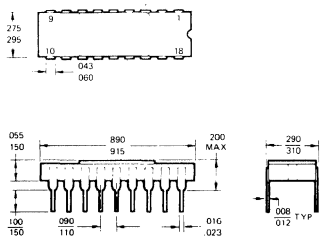


Typical t_A Versus C_L

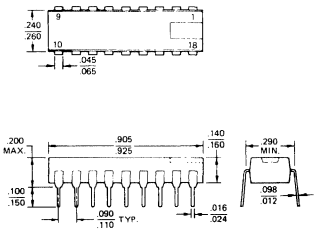


PHYSICAL DIMENSIONS
Dual-In-Line

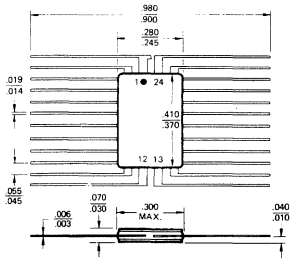
18-Pin Side Brazed



18-Pin Molded



24-Pin Flat Package



Am9112/Am91L12 FAMILY

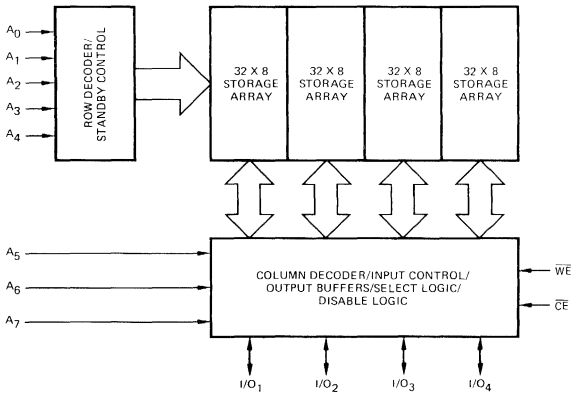
256x4 Static R/W Random Access Memories

Part Number	Am2112	Am2112-2	Am9112A Am91L12A	Am9112B Am91L12B	Am9112C Am91L12C	Am9112D	AM9112E
Access Time	1000ns	650ns	500ns	400ns	300ns	250ns	200ns

Distinctive Characteristics

- 256 x 4 organization
- 16-pin standard DIP
- Low operating power dissipation
  125mW Typ; 290mW maximum – standard power
  100mW Typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
  20mW Typ; 47mW maximum
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads guaranteed
- High noise immunity – full 400mV
- Uniform switching characteristics – access times insensitive to supply variations, address patterns and data patterns.
- Single +5 V power supply – tolerances ±5% commercial, ±10% military
- Bus oriented I/O data
- Zero address, set-up, and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices
- 100% MIL-STD-883 reliability assurance testing

Am9112 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

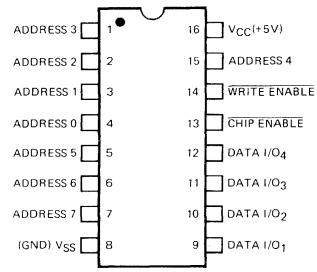
Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Time						
			1000ns	650ns	500ns	400ns	300ns	250ns	200ns
0°C to +70°C	Molded DIP	Standard	P2112	P2112-2	AM9112APC	AM9112BPC	AM9112CPC	AM9112DPC	AM9112EPC
		Low			AM91L12APC	AM91L12BPC	AM91L12CPC		
	Hermetic DIP	Standard	C2112	C2112-2	AM9112ADC	AM9112BDC	AM9112CDC	AM9112DDC	AM9112EDC
		Low			AM91L12ADC	AM91L12BDC	AM91L12CDC		
−55°C to +125°C	Hermetic DIP	Standard			AM9112ADM	AM9112BDM	AM9112CDM		
		Low			AM91L12ADM	AM91L12BDM	AM91L12CDM		
	Hermetic Flat Pack	Standard			AM9112AFM	AM9112BFM			
		Low			AM91L12AFM	AM91L12BFM			

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9112PC, Am9112DC $T_A = 0°C$ to $+70°C$
Am91L12PC, Am91L12DC $V_{CC} = +5V \pm 5\%$

Parameters	Description	Test Conditions			Am9112/ Am91L12 Family Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -200\mu A$			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.25V$				10	µA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_{OUT} = V_{CC}$			5.0	µA
			$V_{OUT} = 0.4V$			−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = MAX. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9112A/B		50	mA
				Am9112C/D/E		55	
				Am91L12A/B		31	
				Am91L12C		34	
I_{CC2}			$T_A = 0°C$	Am9112A/B		55	
				Am9112C/D/E		60	
				Am91L12A/B		33	
				Am91L12C		36	

ELECTRICAL CHARACTERISTICS

Am9112DM, Am9112FM $T_A = -55°C$ to $+125°C$
Am91L12DM, Am91L12FM $V_{CC} = +5.0V \pm 10\%$

Parameters	Description	Test Conditions			Am9112/ Am91L12 Family Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$		2.4		Volts
			$V_{CC} = 4.50V$		2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.5V$				10	µA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_{OUT} = V_{CC}$			10	µA
			$V_{OUT} = 0.4V$			−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = MAX. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9112A/B		50	mA
				Am9112C		55	
				Am91L12A/B		31	
				Am91L12C		34	
I_{CC3}			$T_A = -55°C$	Am9112A/B		60	
				Am9112C		65	
				Am91L12A/B		37	
				Am91L12C		40	

CAPACITANCE

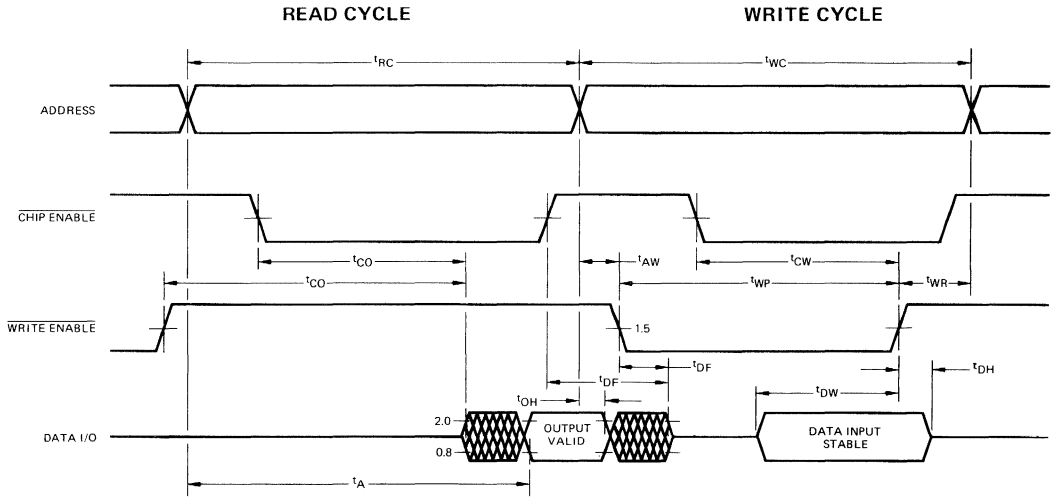
Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	$T_A = 25°C$, f = 1 mHz	Am2112	4.0	8.0	pF
			Am9112/Am91L12	3.0	6.0	
C_{OUT}	Output Capacitance, V_{OUT} = 0V		Am2112	10	18	pF
			Am9112/Am91L12	8.0	11	

SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

Parameters	Description	Am9112A Am91L12A Min.	Am9112A Am91L12A Max.	Am9112B Am91L12B Min.	Am9112B Am91L12B Max.	Am9112C Am91L12C Min.	Am9112C Am91L12C Max.	Am9112D Min.	Am9112D Max.	Am9112E Min.	Am9112E Max.	Units
t_{RC}	Read Cycle Time	500		400		300		250		200		ns
t_A	Access Time		500		400		300		250		200	ns
t_{CO}	Output Enabled to Output ON Delay (Note 1)	5.0	175	5.0	150	5.0	125	5.0	100	5.0	85	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		30		ns
t_{DF}	Output Disabled to Output OFF Delay (Note 2)	5.0	125	5.0	100	5.0	100	5.0	75	5.0	60	ns
t_{WC}	Write Cycle Time	500		400		300		250		200		ns
t_{AW}	Address Set-up Time	0		0		0		0		0		ns
t_{WR}	Address Hold Time	0		0		0		0		0		ns
t_{WP}	Write Pulse Width (Note 3)	175		150		125		100		85		ns
t_{CW}	Chip Enable Set-up Time	175		150		125		100		85		ns
t_{DW}	Input Data Set-up Time	150		125		100		85		65		ns
t_{DH}	Input Data Hold Time (Note 4)	0		0		0		0		0		ns

SWITCHING WAVEFORMS (Note 5)



Notes:
1. Output is enabled and t_{CO} commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and t_{DF} defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum t_{WP} is valid when $\overline{CE}$ has been HIGH at least t_{DF} before $\overline{WE}$ goes LOW. Otherwise $t_{WP(min.)} = t_{DW(min.)} + t_{DF(max.)}$.
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
5. See "Application Information" section of this specification.

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE}$ Active LOW Chip Enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Output Enable Time. The time during which $\overline{CE}$ must be LOW and $\overline{WE}$ must be HIGH prior to data on the output.

t_{OH} Minimum time which will elapse between change of address and any change on the data output.

t_{DF} Time which will elapse between a change on the chip enable or the right enable and on data outputs being driven to a floating status.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

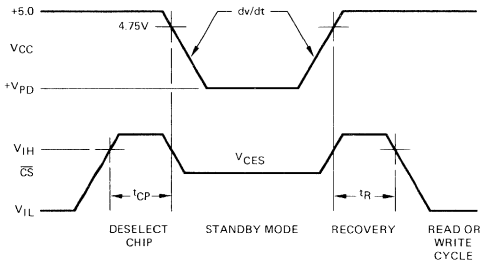
POWER DOWN STANDBY OPERATION

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

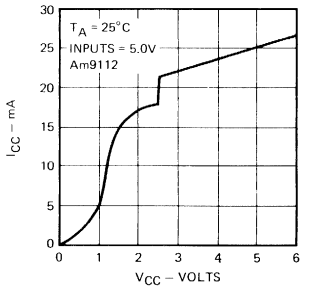
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

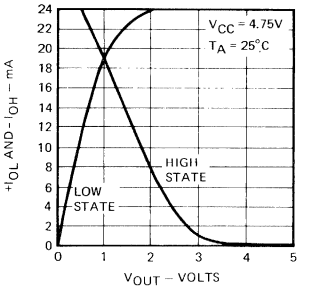
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L12		11	25	mA
				Am9112		13	31	
			$V_{PD} = 2.0V$	Am91L12		13	31	
				Am9112		17	41	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L12		11	28	mA
				Am9112		13	34	
			$V_{PD} = 2.0V$	Am91L12		13	34	
				Am9112		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



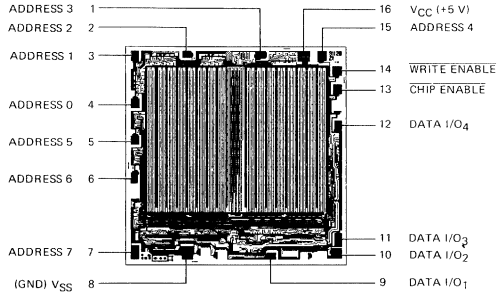
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage

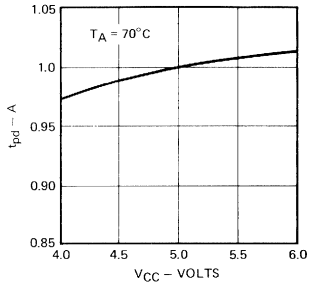


Metallization and Pad Layout

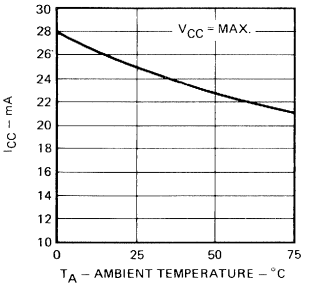


DIE SIZE 0.132" X 0.131"

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

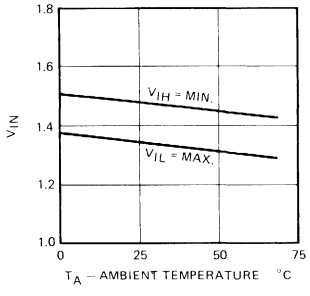
This bussed I/O approach keeps the package pin count low allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ low) and the memory is in the Read state ($\overline{WE}$ high), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

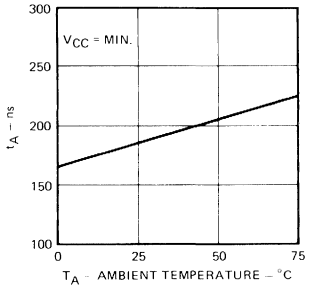
These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always low or is derived directly from addresses and so is low for the whole cycle, make sure t_{WP} is at least $t_{DW} + t_{DF}$ and delay the input data until t_{DF} following the falling edge of $\overline{WE}$. With zero address set-up and hold times it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.
2. For systems where $\overline{CE}$ is high for at least t_{DF} preceeding the falling edge of $\overline{WE}$, t_{WP} may assume the minimum specified value. When $\overline{CE}$ is high for t_{DF} before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.
3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be low to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25 ns.

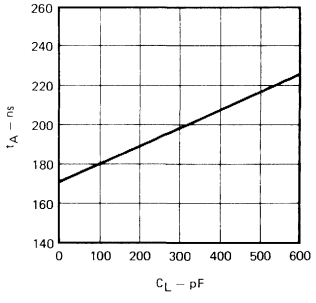
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature

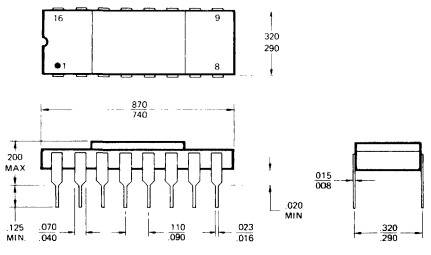


Typical t_A Versus C_L

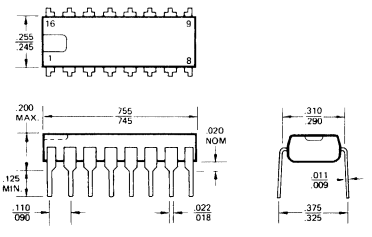


PHYSICAL DIMENSIONS
Dual-In-Line

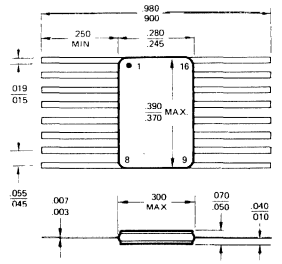
16-Pin Side Brazed



16-Pin Molded



16-Pin Flat Package



Am9130 • Am91L30

1024 x 4 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- 1k X 4 organization
- Fully static data storage – no refreshing
- Single +5V power supply
- High-speed – access times down to 200ns max.
- Low operating power
  - 578mW max., 9130
  - 368mW max., 91L30
- Interface logic levels identical to TTL
- High noise immunity – 400mV worst-case
- High output drive – two standard TTL loads
- DC power-down mode – reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain – no large surges
- Unique Memory Status signal
  - improves performance
  - self clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

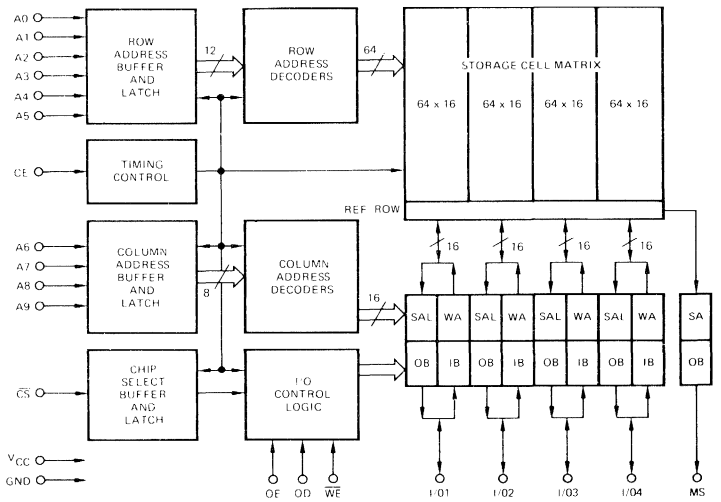
The Am9130 and Am91L30 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

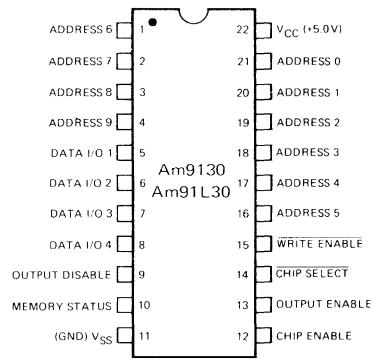
Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature	Power Type	Access Time				
			500ns	400ns	300ns	250ns	200ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	Am9130ADC	Am9130BDC	Am9130CDC	Am9130DDC	Am9130EDC
		LOW	Am91L30ADC	Am91L30BDC	Am91L30CDC	Am91L30DDC	
	$-55°C \leq T_A \leq +125°C$	STD	Am9130ADM	Am9130BDM	Am9130CDM		
		LOW	Am91L30ADM	Am91L30BDM	Am91L30CDM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE		POWER-DOWN RANGE			
V_{CC}	V_{SS}	V_{CC}	V_{SS}	Ambient Temperature	Part Number
$4.75V \leq V_{CC} \leq 5.25V$	0V	$1.5V \leq V_{CC} \leq 5.25V$	0V	$0°C \leq T_A \leq +70°C$	AM91X30XDC
$4.50V \leq V_{CC} \leq 5.50V$	0V	$1.5V \leq V_{CC} \leq 5.50V$	0V	$-55°C \leq T_A \leq +125°C$	AM91X30XDM

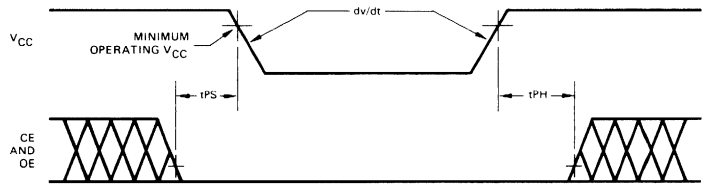
ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Am9130 Min.	Am9130 Typ.	Am9130 Max.	Am91L30 Min.	Am91L30 Typ.	Am91L30 Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$	2.2			2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	μA
I_{CC}	V_{CC} Supply Current	Max. V_{CC}, Output disabled	$T_A = 25°C$		50	100		40	65	mA
			$T_A = 0°C$			110			70	
			$T_A = -55°C$			125			80	
C_{IA}	Input Capacitance (Address)	Test frequency = 1MHz, $T_A = 25°C$, All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF
$C_{I/O}$	I/O Capacitance				6.0	9.0		6.0	9.0	pF

POWER DOWN CHARACTERISTICS

Parameter	Description	Test Conditions		Am9130 Min.	Am9130 Typ.	Am9130 Max.	Am91L30 Min.	Am91L30 Typ.	Am91L30 Max.	Unit
dv/dt	V_{CC} Rate of Change					3.0			3.0	V/μs
tPS	Power Down Set-Up Time			tEL			tEL			ns
tPH	Power Up Hold Time			tEL			tEL			ns
I_{PD}	I_{CC} in Standby (Note 2)	$V_{CC} = 2.0V$	$T_A = 25°C$		36	72		28	55	mA
			$T_A = 0°C$			78			60	mA
			$T_A = -55°$			89			68	mA
		$V_{CC} = 1.5V$	$T_A = 25°C$		20	52		16	45	mA
			$T_A = 0°C$			56			48	mA
			$T_A = -55°C$			64			55	mA

POWER DOWN WAVEFORM



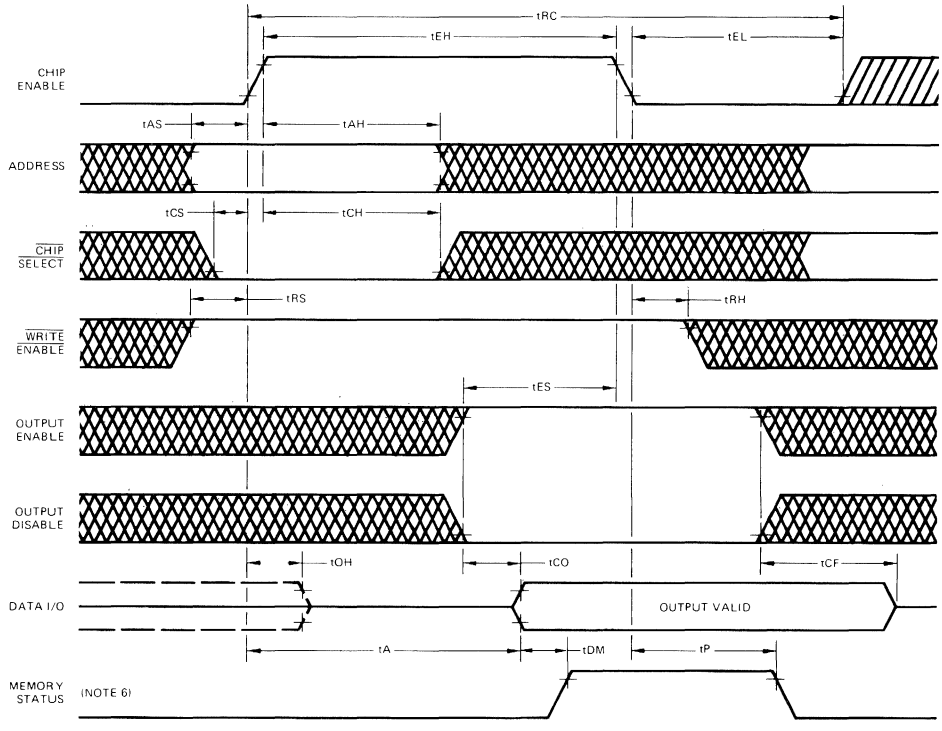
SWITCHING CHARACTERISTICS over operating range

READ CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A Am91L30A Min.	Am9130A Am91L30A Max.	Am9130B Am91L30B Min.	Am9130B Am91L30B Max.	Am9130C Am91L30C Min.	Am9130C Am91L30C Max.	Am9130D Am91L30D Min.	Am9130D Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tRC	Read Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (Note 3) (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Note 14)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Note 14)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRH	Chip Enable to Read Hold Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay (Note 3)	0		0		0		0		0		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tES	Output Enable to CE LOW Set-Up Time (Note 12)	90		75		60		55		50		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval (Note 14)		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

READ CYCLE



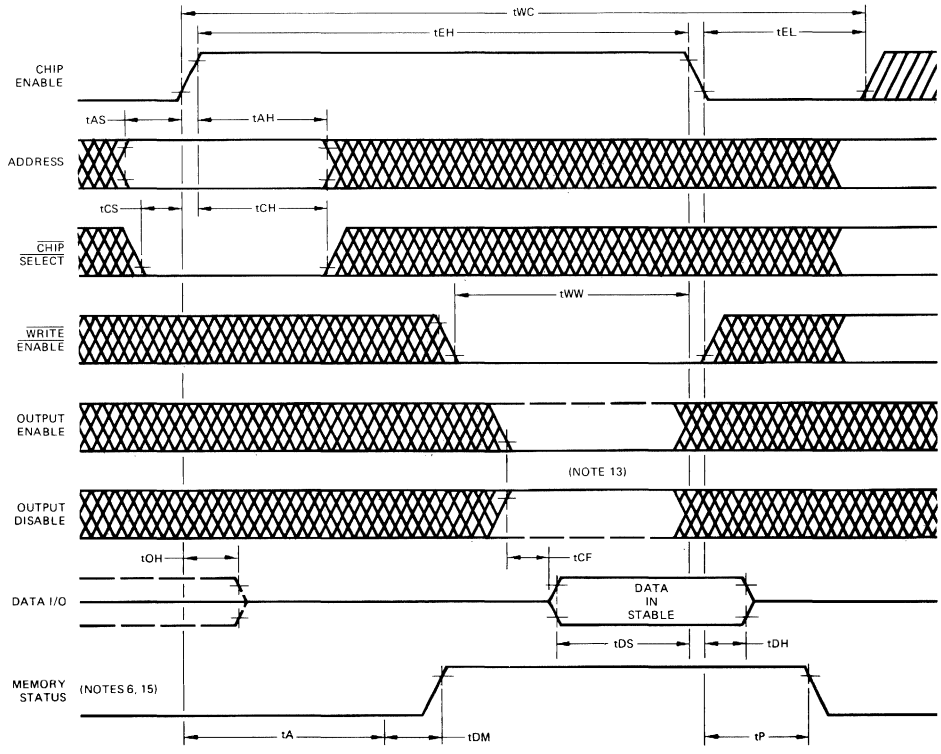
SWITCHING CHARACTERISTICS over operating range

WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A Am91L30A Min.	Am9130A Am91L30A Max.	Am9130B Am91L30B Min.	Am9130B Am91L30B Max.	Am9130C Am91L30C Min.	Am9130C Am91L30C Max.	Am9130D Am91L30D Min.	Am9130D Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tWC	Write Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (CE to Output ON Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	−5		−5		−5		−5		−5		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

WRITE CYCLE

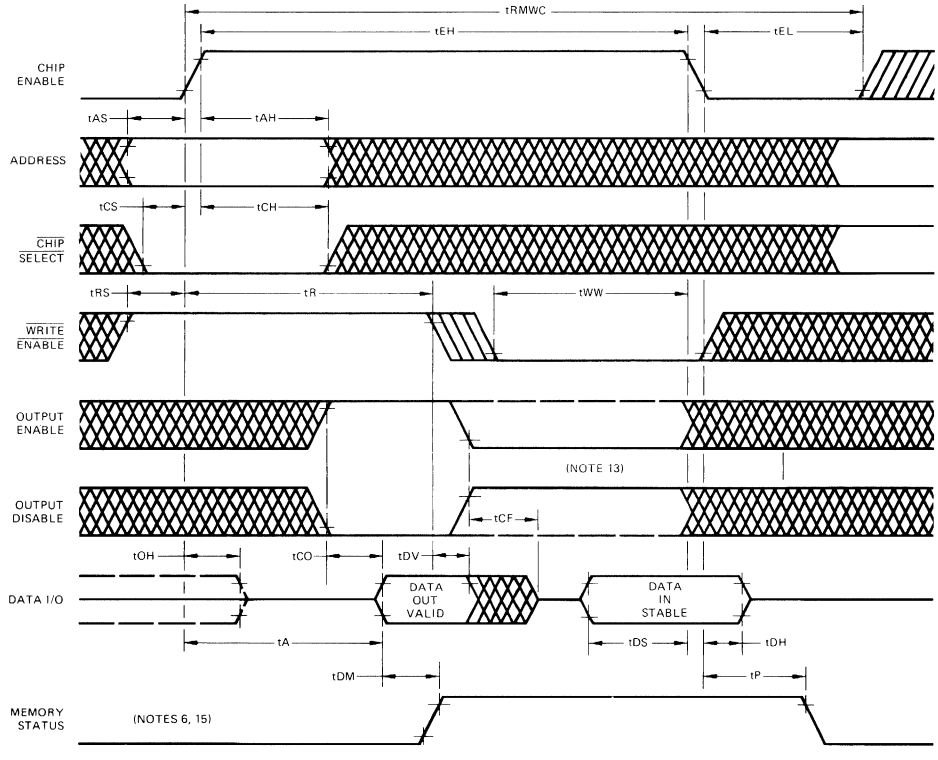


SWITCHING CHARACTERISTICS over operating range

READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

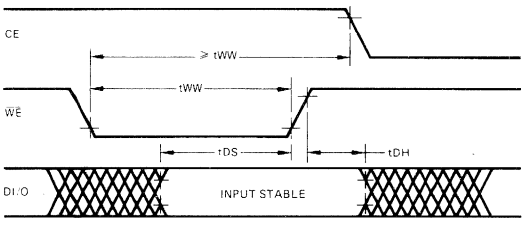
Parameter	Description	Am9130A Am91L30A Min.	Am9130A Am91L30A Max.	Am9130B Am91L30B Min.	Am9130B Am91L30B Max.	Am9130C Am91L30C Min.	Am9130C Am91L30C Max.	Am9130D Am91L30D Min.	Am9130D Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tRMWC	R/M/W Cycle Time (Notes 5, 16)	1170		950		740		625		520		ns
tA	Access Time (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	900		730		570		480		400		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	−5		−5		−5		−5		−5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay	0		0		0		0		0		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tDV	Data Valid after Write Delay	10		10		10		10		10		ns
tR	Read Mode Hold Time	tA		tA		tA		tA		tA		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING CHARACTERISTICS
READ/MODIFY/WRITE CYCLE

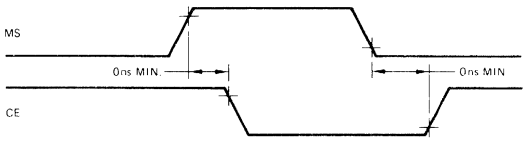


NOTES:

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.
2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.
3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).
4. The negative value shown indicates that the Chip Select input may become valid as late as 5ns following the start of the Chip Enable rising edge.
5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.
7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.
8. Timing reference levels for both input and output signals are 0.8V and 2.0V.
9. CE and $\overline{WE}$ transition times are assumed to be $\leqslant$10ns.
10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:



11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.
12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.
13. Input and output data are the same polarity.
14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH $\geqslant$ tA and tEL $\geqslant$ tP:



15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.
16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) +tCF (max.) + tDS (min.). This provides a conservative design with no I/O overlap and assumes that tCF begins at the end of the tR time. Other designs with somewhat shorter R/M/W cycles are possible.

FUNCTION DESCRIPTION

Block Diagram

The block diagram for the Am9130 shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing 4 bits. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) are decoded and used to select 4 of 64 columns for the sense amplifiers. Thus a single cell is connected to each output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column

bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

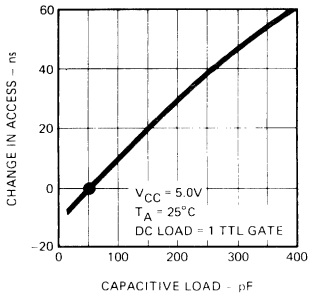
Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

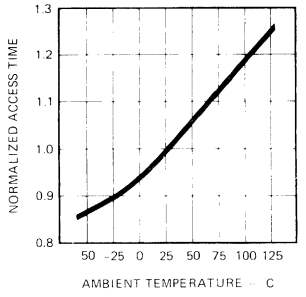
The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

CHARACTERISTICS

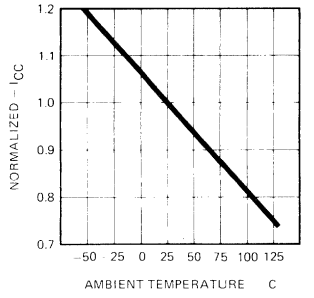
Access Change Versus Capacitive Load



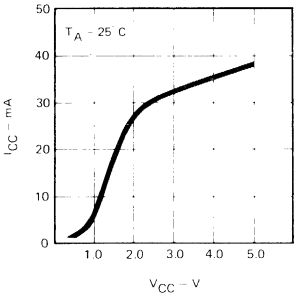
Access Time Versus Ambient Temperature



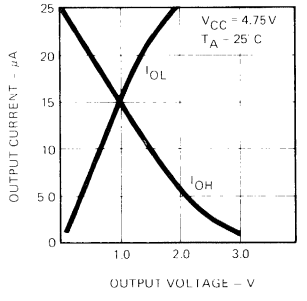
Supply Current Versus Ambient Temperature



Typical I_{CC} Versus V_{CC}

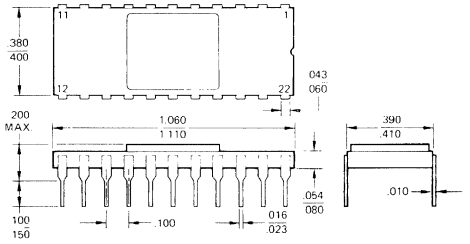


Typical Output Currents Versus Output Voltage

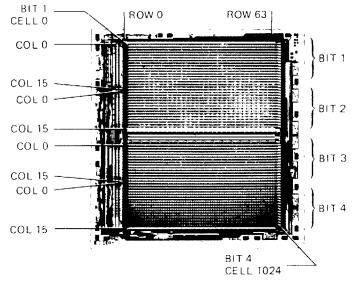


PHYSICAL DIMENSIONS
Dual-In-Line

22-Pin Molded

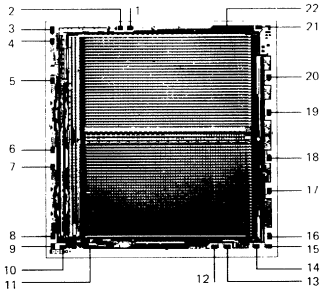


Bit Map



For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A9

Metallization and Pad Layout



DIE SIZE
0.192" X 0.197

Am9131 • Am91L31

1024 x 4 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- 1k X 4 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9131
  - 368mW max., 91L31
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

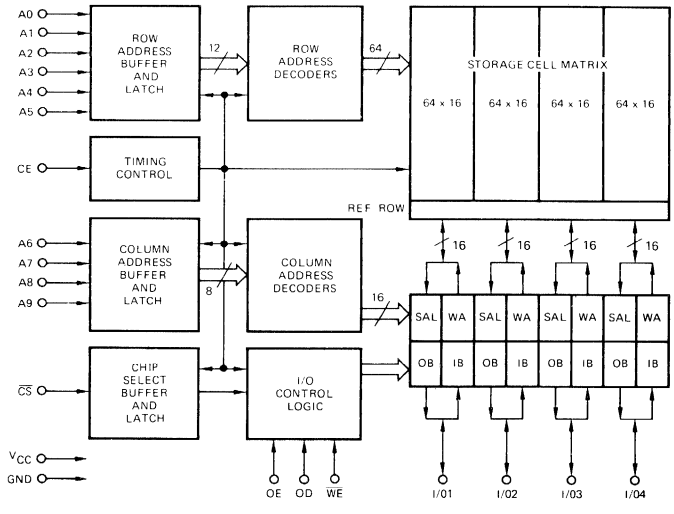
GENERAL DESCRIPTION

The Am9131 and Am91L31 products are high performance, low-power, 4k-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

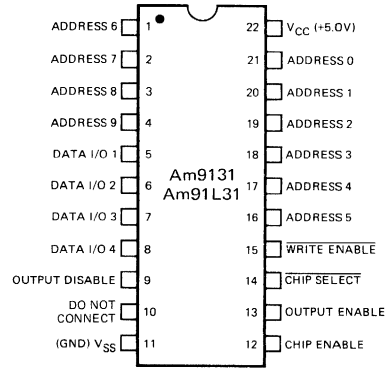
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

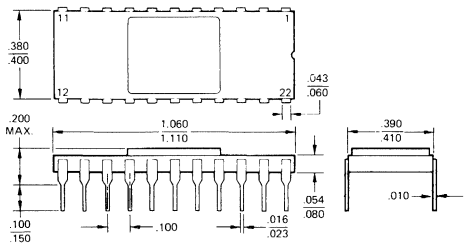
Pin 1 is marked for orientation.

ORDERING INFORMATION

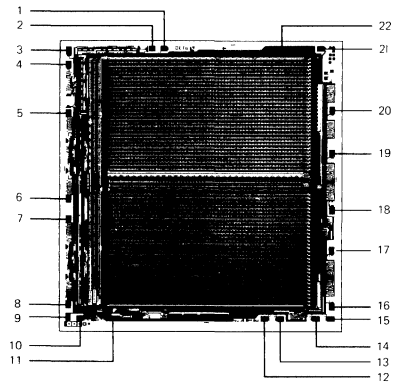
Package Type	Ambient Temperature	Power Type	Access Time				
			500ns	400ns	300ns	250ns	200ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	Am9131ADC	Am9131BDC	Am9131CDC	Am9131DDC	Am9131EDC
		LOW	Am91L31ADC	Am91L31BDC	Am91L31CDC	Am91L31DDC	
	$-55°C \leq T_A \leq +125°C$	STD	Am9131ADM	Am9131BDM	Am9131CDM		
		LOW	Am91L31ADM	Am91L31BDM	Am91L31CDM		

The Am9131 and Am91L31 memories are identical in every respect to their counterparts in the Am9130 and Am91L30 family, with the single exception that the Memory Status output is not functional. Pin 10 on the Am9131/L31 products should not be used and should not be connected to any external circuit. Please refer to the Am9130/L30 data sheet for the electrical and switching characteristics of the Am9131/L31.

PHYSICAL DIMENSIONS
Dual-In-Line
22-Pin Hermetic



Metallization and Pad Layout



DIE SIZE 0.192" x 0.197"

Am9140 • Am91L40

4096 x 1 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- 4k X 1 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9140
  - 368mW max., 91L40
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Unique Memory Status signal
  - improves performance
  - self-clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

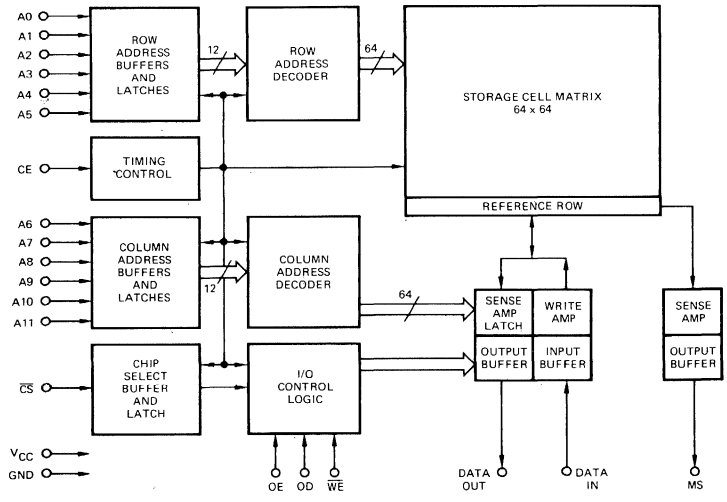
The Am9140 and Am91L40 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bit per word. Only a single +5V power supply is required for normal operation. A DC power down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

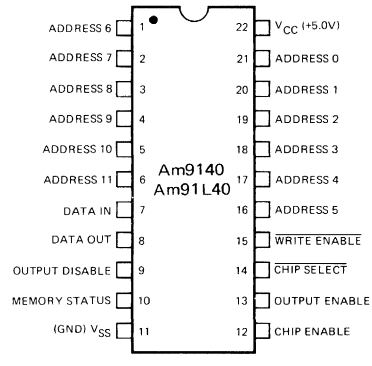
Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write.

Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature	Power Type	Access Time				
			500ns	400ns	300ns	250ns	200ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	Am9140ADC	Am9140BDC	Am9140CDC	Am9140DDC	Am9140EDC
		LOW	Am91L40ADC	Am91L40BDC	Am91L40CDC	Am91L40DDC	
	$-55°C \leq T_A \leq +125°C$	STD	Am9140ADM	Am9140BDM	Am9140CDM		
		LOW	Am91L40ADM	Am91L40BDM	Am91L40CDM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE		POWER DOWN RANGE			
V_{CC}	V_{SS}	V_{CC}	V_{SS}	Ambient Temperature	Part Number
$4.75V \leq V_{CC} \leq 5.25V$	0V	$1.5V \leq V_{CC} \leq 5.25V$	0V	$0°C \leq T_A \leq +70°C$	AM91X40XDC
$4.50V \leq V_{CC} \leq 5.50V$	0V	$1.5V \leq V_{CC} \leq 5.50V$	0V	$-55°C \leq T_A \leq +125°C$	AM91X40XDM

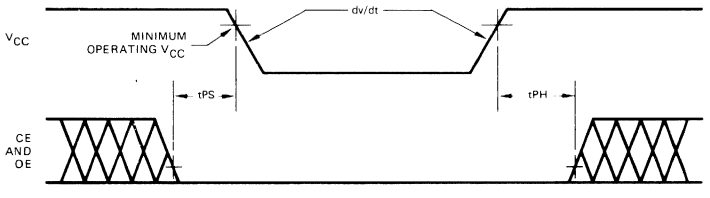
ELECTRICAL CHARACTERISTICS over operating range (Note 1)

				Am9140			Am91L40			
Parameters	Description	Test Conditions		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$	2.2			2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	µA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	µA
I_{CC}	V_{CC} Supply Current	Max. V_{CC} Output disabled	$T_A = 25°C$		50	100		40	65	mA
			$T_A = 0°C$			110			70	
			$T_A = -55°C$			125			80	
C_{IA}	Input Capacitance (Address)	Test frequency = 1MHz $T_A = 25°C$ All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF

POWER DOWN CHARACTERISTICS

				Am9140			Am91L40			
Parameter	Description	Test Conditions		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
dv/dt	V_{CC} Rate of Change					3.0			3.0	V/µs
tPS	Power Down Set-Up Time			tEL			tEL			ns
tPH	Power Up Hold Time			tEL			tEL			ns
I_{PD}	I_{CC} in Standby (Note 2)	$V_{CC} = 2.0V$	$T_A = 25°C$		36	72		28	55	mA
			$T_A = 0°C$			78			60	mA
			$T_A = -55°$			89			68	mA
		$V_{CC} = 1.5V$	$T_A = 25°C$		20	52		16	45	mA
			$T_A = 0°C$			56			48	mA
			$T_A = -55°C$			64			55	mA

POWER DOWN WAVEFORM



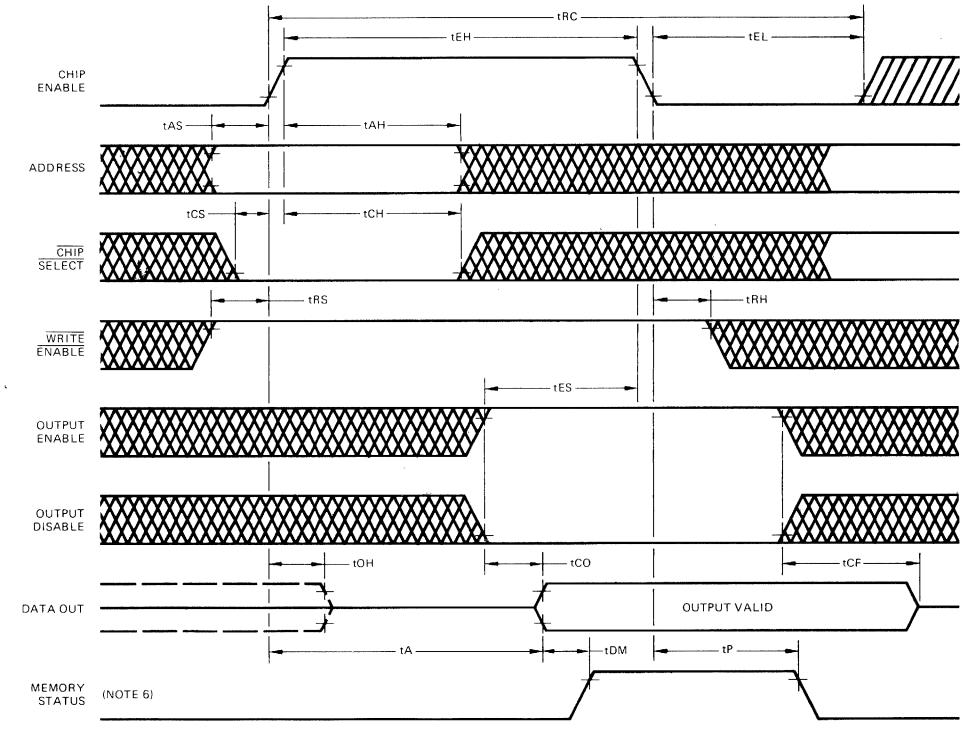
SWITCHING CHARACTERISTICS over operating range

READ CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9140A Am91L40A Min.	Max.	Am9140B Am91L40B Min.	Max.	Am9140C Am91L40C Min.	Max.	Am9140D Am91L40D Min.	Max.	Am9140E Min.	Max.	Unit
tRC	Read Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (Note 3) (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Note 14)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Note 14)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	−5		−5		−5		−5		−5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRH	Chip Enable to Read Hold Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay (Note 3)	0		0		0		0		0		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tES	Output Enable to CE LOW Set-Up Time (Note 12)	90		75		60		55		50		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval (Note 14)		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

READ CYCLE



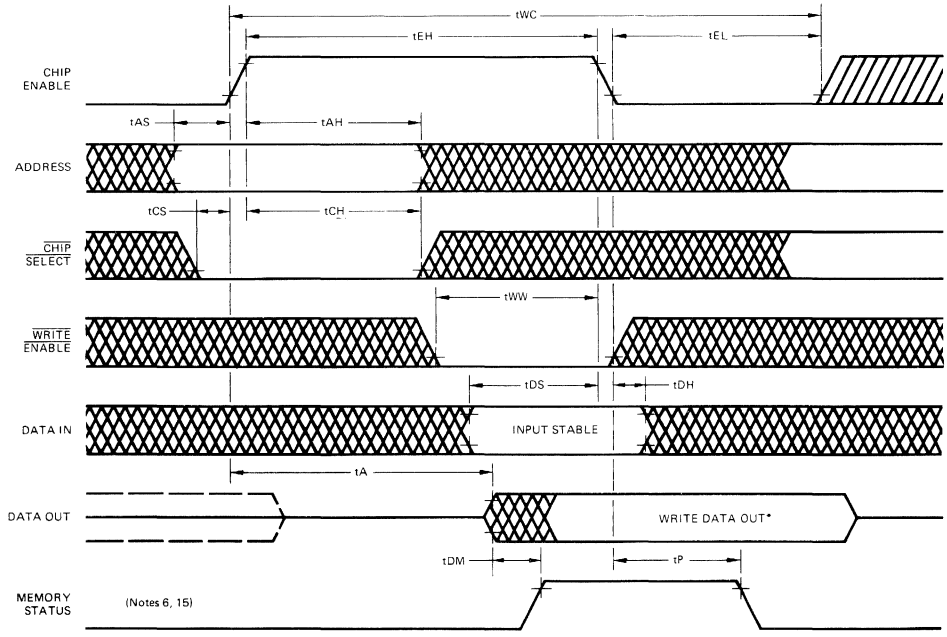
SWITCHING CHARACTERISTICS over operating range

WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9140A Am91L40A Min.	Am9140A Am91L40A Max.	Am9140B Am91L40B Min.	Am9140B Am91L40B Max.	Am9140C Am91L40C Min.	Am9140C Am91L40C Max.	Am9140D Am91L40D Min.	Am9140D Am91L40D Max.	Am9140E Min.	Am9140E Max.	Unit
tWC	Write Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (CE to Output ON Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		– 5		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

WRITE CYCLE



*Assumes output is enabled.

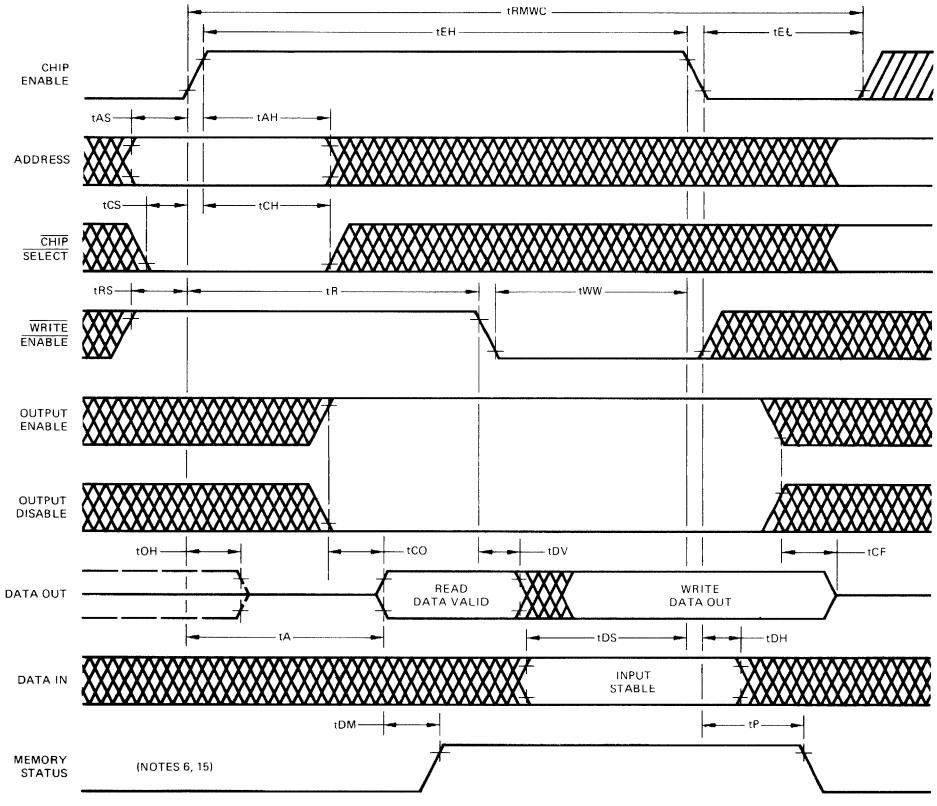
SWITCHING CHARACTERISTICS over operating range

READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9140A Am91L40A Min.	Am9140A Am91L40A Max.	Am9140B Am91L40B Min.	Am9140B Am91L40B Max.	Am9140C Am91L40C Min.	Am9140C Am91L40C Max.	Am9140D Am91L40D Min.	Am9140D Am91L40D Max.	Am9140E Min.	Am9140E Max.	Unit
tRMWC	R/M/W Cycle Time (Notes 5, 16)	970		785		605		510		420		ns
tA	Access Time (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	700		565		435		365		300		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	−5		−5		−5		−5		−5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay	0		0		0		0		0		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tDV	Data Valid after Write Delay	10		10		10		10		10		ns
tR	Read Mode Hold Time	tA		tA		tA		tA		tA		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

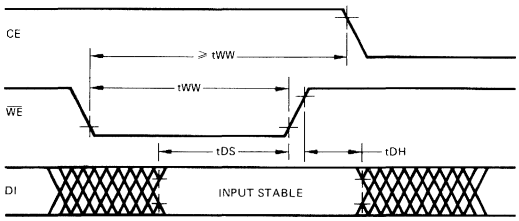
SWITCHING WAVEFORMS

READ/MODIFY/WRITE CYCLE

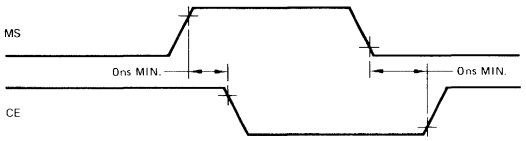


NOTES:

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.
2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.
3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).
4. The negative value shown indicates that the Chip Select input may become valid as late as 5.0ns following the start of the Chip Enable rising edge.
5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.
7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.
8. Timing reference levels for both input and output signals are 0.8V and 2.0V.
9. CE and $\overline{WE}$ transition times are assumed to be $\leqslant$10ns.
10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:



11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.
12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.
13. Input and output data are the same polarity.
14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH $\geqslant$ tA and tEL $\geqslant$ tP:



15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.
16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) + tWW. Note 5 defines tRMWC but it may also be viewed as tRC + tWW. Modify times are assumed to be zero. For systems with Data In and Data Out tied together R/M/W timing should make allowance for tCF time so that no bus conflict occurs (see Am9130 data sheet for timing approach).

FUNCTIONAL DESCRIPTION

Block Diagram

The block diagram for the Am9140 shows the interface connections along with the general signal flow. There are twelve address lines (A0 through A11) that are used to specify one of 4096 locations, with each location containing one bit. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A11) are decoded and used to select one of 64 columns for the sense amplifier. Thus a single cell is connected into the output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column

bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

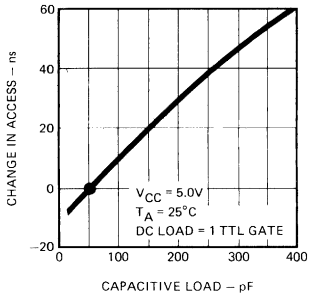
Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

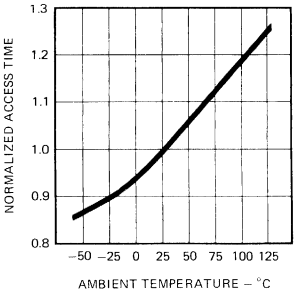
The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

CHARACTERISTICS

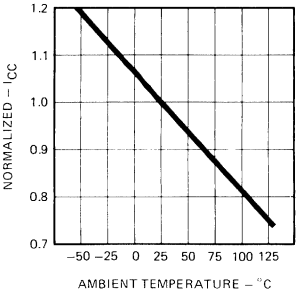
Access Change Versus Capacitive Load



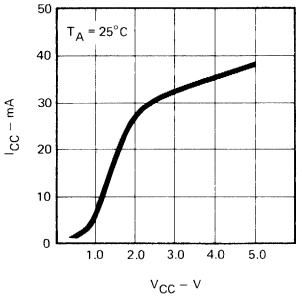
Access Time Versus Ambient Temperature



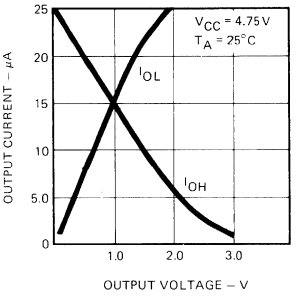
Supply Current Versus Ambient Temperature



Typical I_{CC} Versus V_{CC}

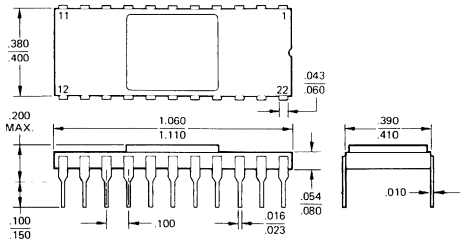


Typical Output Currents Versus Output Voltage

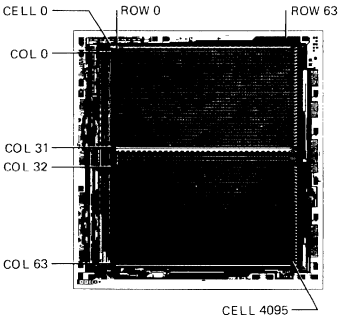


PHYSICAL DIMENSIONS
Dual-In-Line

22-Pin Hermetic

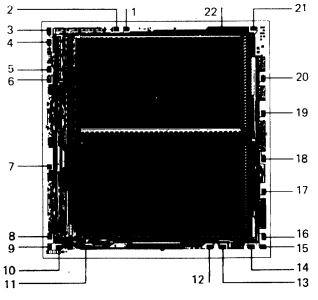


Bit Map



For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A11

Metallization and Pad Layout



DIE SIZE
0.192" X 0.197"

Am9141 • Am91L41

4096 x 1 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- 4k X 1 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9141
  - 368mW max., 91L41
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Full MIL temperature range available
- 100% reliability assurance testing in compliance with MIL-STD-883

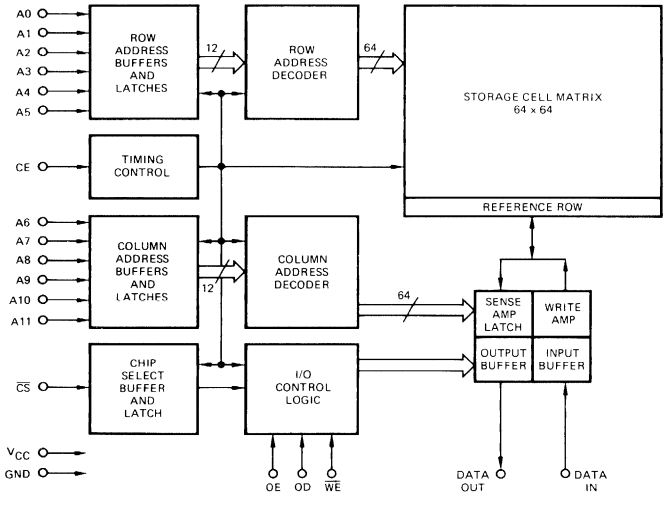
GENERAL DESCRIPTION

The Am9141 and Am91L41 products are high performance, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bit per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

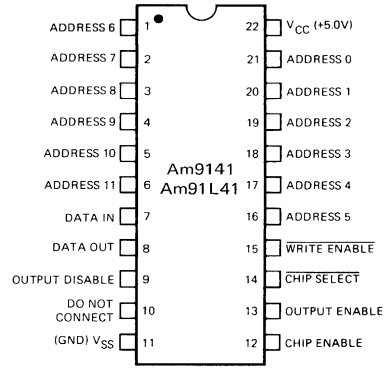
All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

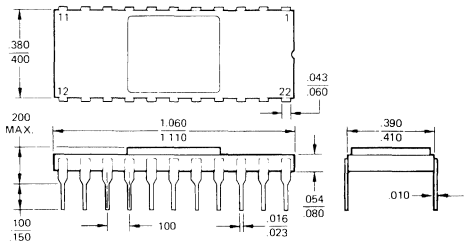
Pin 1 is marked for orientation.

ORDERING INFORMATION

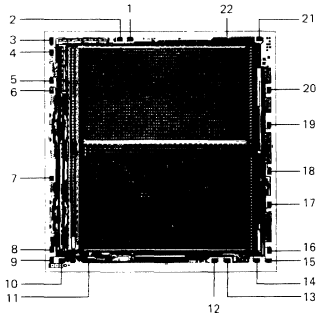
Package Type	Ambient Temperature	Power Type	Access Time				
			500ns	400ns	300ns	250ns	200ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	Am9141ADC	Am9141BDC	Am9141CDC	Am9141DDC	Am9141EDC
		LOW	Am91L41ADC	Am91L41BDC	Am91L41CDC	Am91L41DDC	
	$-55°C \leq T_A \leq +125°C$	STD	Am9141ADM	Am9141BDM	Am9141CDM		
		LOW	Am91L41ADM	Am91L41BDM	Am91L41CDM		

The Am9141 and Am91L41 memories are identical in every respect to their counterparts in the Am9140 and Am91L40 family, with the single exception that the Memory Status output is not functional. Pin 10 on the Am9141/L41 products should not be used and should not be connected to any external circuit. Please refer to the Am9140/L40 data sheet for the electrical and switching characteristics of the Am9141/L41.

PHYSICAL DIMENSIONS
Dual-In-Line
22-Pin Hermetic



Metallization and Pad Layout



DIE SIZE 0.192 x 0.197"

Am9135

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High-speed – access times down to 80ns max.
- Standard 18-pin dual in-line package
- 1k x 4 organization
- Fully static data storage
- Clocked static access circuitry
- No dynamic nodes
- No refreshing
- Single +5V power supply
- Interface logic levels fully TTL compatible
- High output drive – 4.0mA @ 0.4V
- Bidirectional Data Bus
- Constant power drain – no large surges
- Military temperature range available
- Advanced N-channel Silicon Gate Technology
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

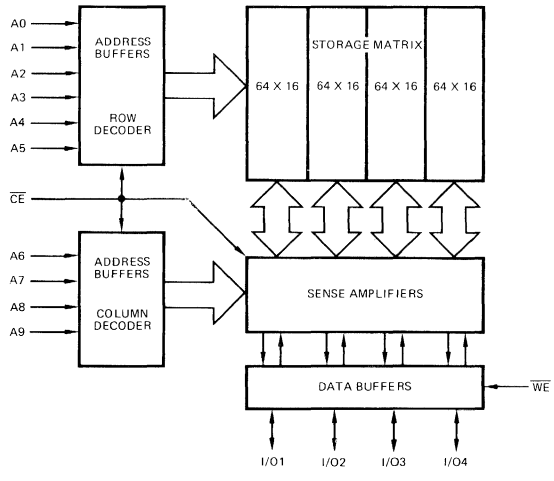
The Am9135 products are high performance, 4096-bit, static, read/write random access memories, designed for applications requiring high speed. They are implemented as 1024 words by 4 bits per word. The data input and output signals are bussed together and share common I/O pins. Input and output data are the same polarity. A single +5 volt power supply is required.

All interface signal levels are fully compatible with TTL specifications, providing good noise immunity and simplified system design. The outputs will drive two full Schottky loads or eleven LS loads for increased fan-out, better capacitive drive and improved bus interface capability.

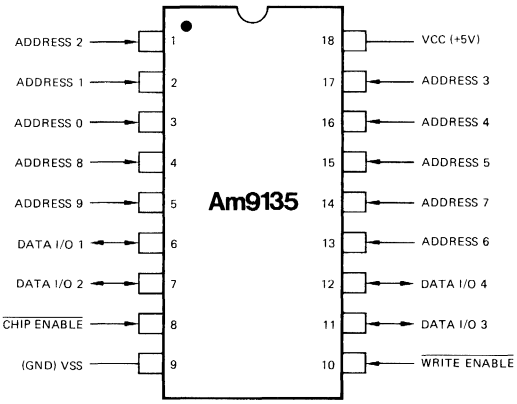
The memory matrix uses a conventional fully static, six-device storage cell. The addressing and sensing functions use clocked static circuitry for improved speed and lower power. The Chip Enable clock may be stopped indefinitely in either state.

Operational cycles are initiated when the Chip Enable signal goes low. When the read or write is complete, Chip Enable goes high to preset the memory for the next cycle. The WE signal is high for read operations and low during the Chip Enable low time to perform a write.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time			
		150ns	120ns	100ns	80ns
Hermetic DIP	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	Am9135FDC	Am9135GDC	Am9135HDC	Am9135JDC
	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	Am9135FDM	Am9135GDM	Am9135HDM	

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VCC	VSS
Am9135DC	$0°C \leq T_A \leq +70°C$	+5.0V ± 5%	0V
Am9135DM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Am9135DC Min.	Am9135DC Typ.	Am9135DC Max.	Am9135DM Min.	Am9135DM Typ.	Am9135DM Max.	Units
VOH	Output HIGH Voltage	IOH = −400μA, VCC = 4.75V		2.4			2.4			Volts
		IOH = −200μA, VCC = 4.5V					2.2			
VOL	Output LOW Voltage	IOL = 4.0mA				0.4			0.4	Volts
VIH	Input HIGH Voltage			2.4		VCC	2.4		VCC	Volts
VIL	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VIN ≤ VCC				10			10	μA
IOZ	Output Leakage Current	VSS ≤ VOUT ≤ VCC, Output disabled				10			50	μA
ICC	VCC Supply Current	Max. VCC, Output disabled	$T_A = 25°C$		90	120		90	120	mA
			$T_A = 0°C$			135			135	
			$T_A = -55°C$						150	
CIA	Input Capacitance (Address)	Test Frequency = 1.0MHz, $T_A = 25°C$, All pins at 0V			3.0	6.0		3.0	6.0	pF
CI/O	I/O Capacitance				6.0	9.0		6.0	9.0	pF
CIC	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF

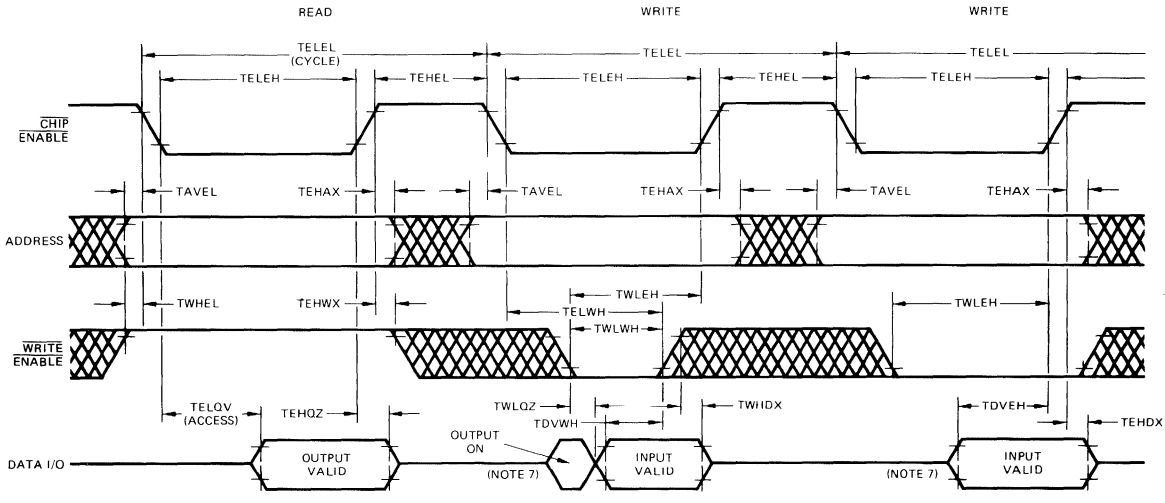
NOTES

1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. Timing reference levels for both input and output signals are 0.8V low and 2.0V high.
3. Output loading is one standard Schottky TTL load plus 100pF capacitance.
4. Cycle times (TELEL) are the sum of CE fall time, CE low time (TELEH), CE rise time and CE high time (TEHEL). The values shown for cycle times include worst-case CE low and CE high requirements and assume transition times of 5ns.
5. The output buffers turn off when CE goes high. They remain off until the access time following the next falling edge of CE.
6. The internal write time is defined by the overlap of CE low and WE low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. When the WE line goes low the output buffers are turned off following the turn-off delay (TWLQZ). When the falling edge of WE occurs early in the write cycle or preceeds the falling edge of CE, the output buffers will not turn on and the Data I/O lines will be available for input information. When the falling edge of WE occurs late in the write cycle, output data may occupy the I/O bus and input data should not be asserted until after the TWLQZ delay.

SWITCHING CHARACTERISTICS over operating range (Notes 2 and 3)

		Am9135F		Am9135G		Am9135H		Am9135J		
Parameters	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TELEL	CE Low to CE Low Time (Note 4) (Cycle Time)	235		190		160		130		ns
TELQV	CE Low to Output Valid Delay (Access Time)		150		120		100		80	ns
TELEH	CE Low Time	150		120		100		80		ns
TEHEL	CE High Time	75		60		50		40		ns
TAVEL	Address Valid to CE Low (Address Set-up Time)	0		0		0		0		ns
TEHAX	CE High to Address Don't Care (Address Hold Time)	0		0		0		0		ns
TWHEL	WE High to CE Low (Read Set-up Time)	0		0		0		0		ns
TEHWX	CE High to WE Don't Care (Read Hold Time)	0		0		0		0		ns
TEHQZ	CE High to Output Off (Note 5)		60		55		45		35	ns
TWLQZ	WE Low to Output OFF (Note 7)		40		35		30		25	ns
TELWH	CE Low to WE High	120		100		80		55		ns
TWLWH	WE Low to WE High (Write Pulse Duration)	90		80		65		50		ns
TWLEH	WE Low to CE High	90		80		65		50		ns
TDVWH TDVEH	Data In Valid to WE or CE High (Data In Set-up Time) (Note 6)	90		80		65		50		ns
TWHDX TEHDX	WE or CE High to Data In Don't Care (Data In Hold Time) (Note 6)	0		0		0		0		ns

TIMING DIAGRAM



SYMBOLS AND ABBREVIATIONS

This data sheet uses a new type of specification nomenclature that is derived from background work of several users and manufacturers of semiconductor memories. It should help to clarify signal and parameter symbols and definitions and make data sheet information more consistent.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

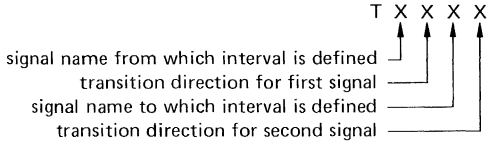
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurement. Examples:

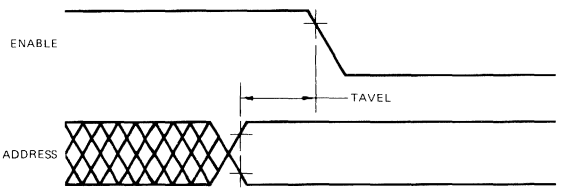
VOH = Output high voltage
IIL = Input low current
IOZ = Output off current (leakage)

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a 'from-to' sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



Example:



The drawing shows the address setup time defined as TAVEL, Address Valid to Enable Low time.

The signal definitions used in this data sheet are:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable

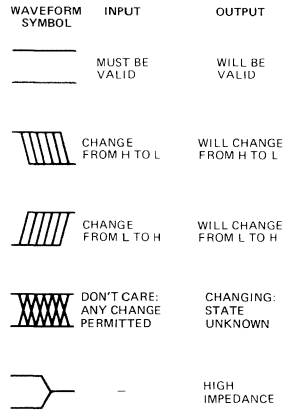
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

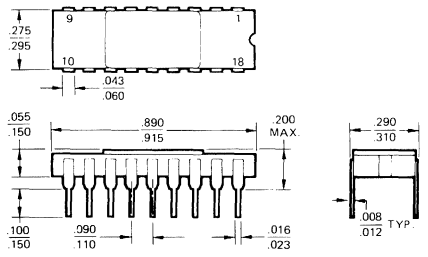
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS



PHYSICAL DIMENSIONS

Dual-In-Line
18-Pin Hermetic



Am9145

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High-speed — access times down to 80ns max.
- Standard 18-pin dual in-line package
- 4k x 1 organization
- Fully static data storage
- Clocked static access circuitry
- No dynamic nodes
- No refreshing
- Single +5V power supply
- Interface logic levels fully TTL compatible
- High output drive — 4.0mA @ 0.4V
- Separate Data In and Data Out
- Constant power drain — no large surges
- Military temperature range available
- Advanced N-channel Silicon Gate Technology
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

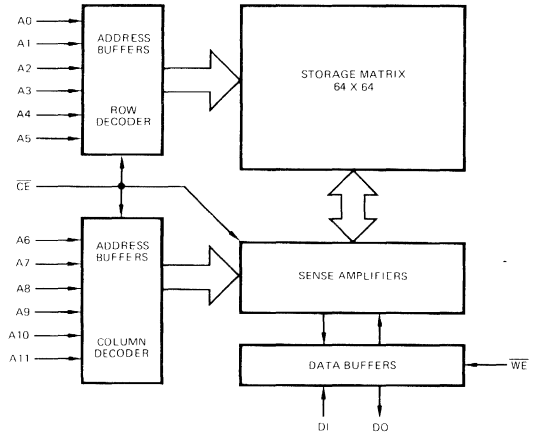
The Am9145 products are high performance, 4096-bit, static, read/write random access memories, designed for applications requiring high speed. They are implemented as 4096 words by 1 bit per word. The data input and output signals use separate interface pins. Input and output data are the same polarity. A single +5 volt power supply is required.

All interface signal levels are fully compatible with TTL specifications, providing good noise immunity and simplified system design. The outputs will drive two full Schottky loads or eleven LS loads for increased fan-out, better capacitive drive and improved bus interface capability.

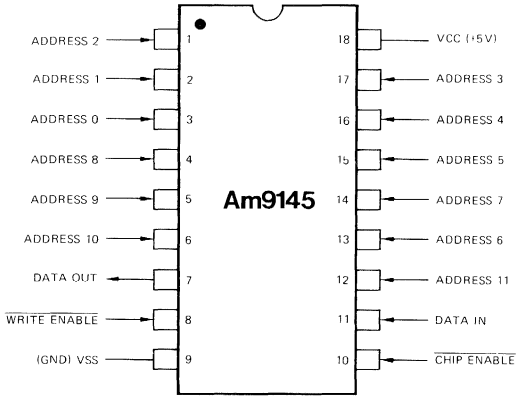
The memory matrix uses a conventional fully static, six-device storage cell. The addressing and sensing functions use clocked static circuitry for improved speed and lower power. The Chip Enable clock may be stopped indefinitely in either state.

Operational cycles are initiated when the Chip Enable signal goes low. When the read or write is complete, Chip Enable goes high to preset the memory for the next cycle. The WE signal is high for read operations and low during the Chip Enable low time to perform a write.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time			
		150ns	120ns	100ns	80ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	Am9145FDC	Am9145GDC	Am9145HDC	Am9145JDC
	$-55°C \leq T_A \leq +125°C$	Am9145FDM	Am9145GDM	Am9145HDM	

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VCC	VSS
Am9145DC	$0°C \leq T_A \leq +70°C$	+5.0V ± 5%	0V
Am9145DM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Am9145DC Min.	Am9145DC Typ.	Am9145DC Max.	Am9145DM Min.	Am9145DM Typ.	Am9145DM Max.	Units
VOH	Output HIGH Voltage	IOH = −400μA, VCC − 4.75V		2.4			2.4			Volts
		IOH = −200μA, VCC = 4.5V					2.2			
VOL	Output LOW Voltage	IOL = 4.0mA				0.4			0.4	Volts
VIH	Input HIGH Voltage			2.4		VCC	2.4		VCC	Volts
VIL	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VIN ≤ VCC				10			10	μA
IOZ	Output Leakage Current	VSS ≤ VOUT ≤ VCC, Output disabled				10			50	μA
ICC	VCC Supply Current	Max. VCC, Output disabled	$T_A = 25°C$		90	120		90	120	mA
			$T_A = 0°C$			135			135	
			$T_A = -55°C$						150	
CIA	Input Capacitance (Address)	Test Frequency = 1.0MHz, $T_A = 25°C$, All pins at 0V			3.0	6.0		3.0	6.0	pF
COUT	Output Capacitance				4.0	7.0		4.0	7.0	pF
CIC	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF

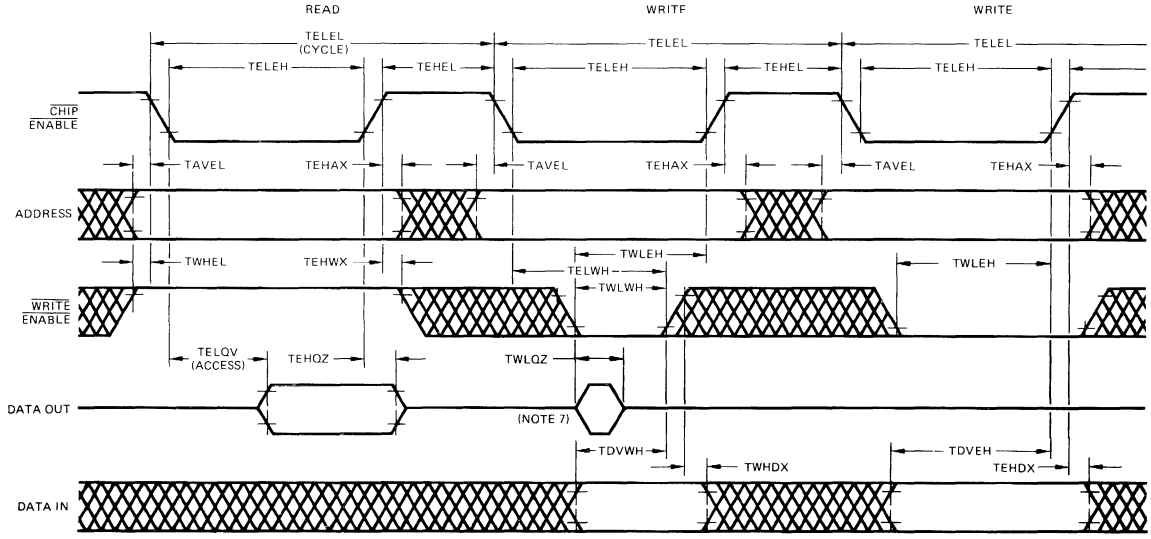
NOTES

1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. Timing reference levels for both input and output signals are 0.8V low and 2.0V high.
3. Output loading is one standard Schottky TTL load plus 100pF capacitance.
4. Cycle times (TELEL) are the sum of CE fall time, CE low time (TELEH), CE rise time and CE high time (TEHEL). The values shown for cycle times include worst-case CE low and CE high requirements and assume transition times of 5ns.
5. The output buffer turns off when CE goes high. It remains off until the access time following the next falling edge of CE.
6. The internal write time is defined by the overlap of CE low and WE low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The input data setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. When the WE line goes low the output buffer is turned off following the TWLQZ delay. This permits the Data In and Data Out lines to be tied together and used as a bidirectional Data I/O bus. Timing will then be as shown on the Am9135 data sheet.

SWITCHING CHARACTERISTICS over operating range (Notes 2 and 3)

		Am9145F		Am9145G		Am9145H		Am9145J		
Parameters	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
TELEL	CE Low to CE Low Time (Note 4) (Cycle Time)	235		190		160		130		ns
TELQV	CE Low to Output Valid Delay (Access Time)		150		120		100		80	ns
TELEH	CE Low Time	150		120		100		80		ns
TEHEL	CE High Time	75		60		50		40		ns
TAVEL	Address Valid to CE Low (Address Set-up Time)	0		0		0		0		ns
TEHAX	CE High to Address Don't Care (Address Hold Time)	0		0		0		0		ns
TWHEL	WE High to CE Low (Read Set-up Time)	0		0		0		0		ns
TEHWX	CE High to WE Don't Care (Read Hold Time)	0		0		0		0		ns
TEHQZ	CE High to Output Off (Note 5)		60		55		45		35	ns
TWLQZ	WE Low to Output OFF (Note 7)		40		35		30		25	ns
TELWH	CE Low to WE High	120		100		80		55		ns
TWLWH	WE Low to WE High (Write Pulse Duration)	90		80		65		50		ns
TWLEH	WE Low to CE High	90		80		65		50		ns
TDVWH TDVEH	Data In Valid to WE or CE High (Data In Set-up Time) (Note 6)	90		80		65		50		ns
TWHDX TEHDX	WE or CE High to Data In Don't Care (Data In Hold Time) (Note 6)	0		0		0		0		ns

TIMING DIAGRAM



SYMBOLS AND ABBREVIATIONS

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All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

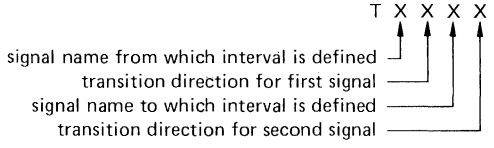
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurement. Examples:

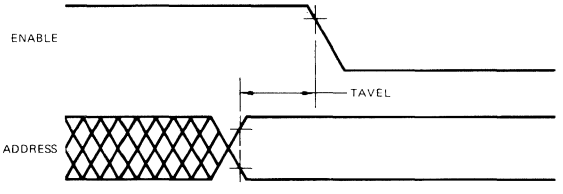
VOH = Output high voltage
IIL = Input low current
IOZ = Output off current (leakage)

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a 'from-to' sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



Example:



The drawing shows the address setup time defined as TAVEL, Address Valid to Enable Low time.

The signal definitions used in this data sheet are:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable

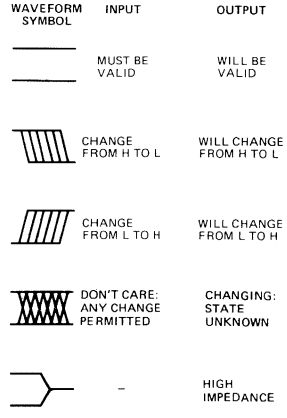
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

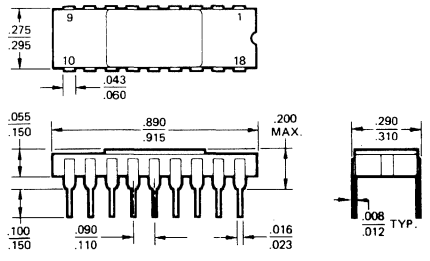
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS



PHYSICAL DIMENSIONS

Dual-In-Line
18-Pin Hermetic



Am9050

4096-Bit Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 4096 x 1 organization
- Standard 18-pin dual-in-line package
- High output drive
- TTL compatible interface (except CE)
- Low power dissipation—
  - 400mW typ., 750mW max. operating
  - 5.0mW typ., 13mW max. refresh only
  - 0.1mW typ., 3.0mW max. standby
- Low I_{DD} current surges—easier decoupling
- Simplified timing requirements—
  - Zero data hold with respect to CE
  - Optional data hold with respect to R/W
  - Optional data set-up with respect to R/W
- Low clock capacitance –20pF max.
- Unique fully capacitive input circuits—eliminate extraneous current surges
- Direct plug-in replacement for TMS 4050
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

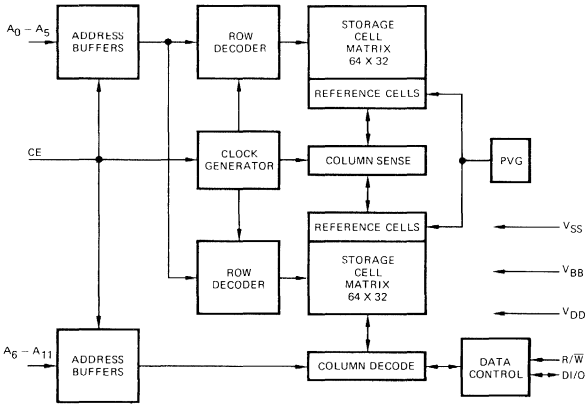
FUNCTIONAL DESCRIPTION

The Am9050 devices are high performance, 4k-bit, dynamic, read/write, random access memories. They are organized as 4096 words by 1-bit per word. The basic memory element is a one-transistor cell that stores charge on a small internal capacitor. The memory mechanism is dynamic and the chip should be periodically refreshed in order to maintain stored data integrity.

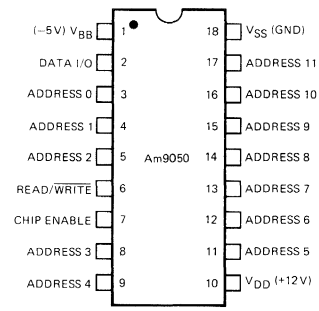
All input signals are fully TTL compatible except the single high-level clock signal called Chip Enable. When CE goes low the memory is internally precharged and then assumes its low power standby mode. All operating cycles are initiated when CE goes high. Read-out is nondestructive so that re-writing is not necessary. Successive read and write operations at the same location can improve performance since readdressing is not required. This combination is specified as a Read/Modify/Write cycle.

Data In and Data Out signals are bussed together as a common I/O signal line. An external pull-up resistor is used for TTL compatibility. Input and output data are the same polarity.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Access Time		
		300ns	250ns	200ns
$0°C \leq T_A \leq +70°C$	Molded DIP	AM9050CPC	AM9050DPC	AM9050EPC
	Hermetic DIP	AM9050CDC	AM9050DDC	AM9050EDC

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
All Supply Voltages with Respect to V_{BB}	−0.3 V to +20 V
All Input Signal Voltages with Respect to V_{BB}	−0.3 V to +20 V
Output Voltage with Respect to V_{SS}, Operating	−2.0 V to +7.0 V
Power Dissipation	1.0 W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	V_{DD}	V_{SS}	V_{BB}
0°C to +70°C	+12 V ± 5%	0	−5.0 V ± 10%

No signal or supply voltage should ever be more than 0.3 V more negative than V_{BB}.

ELECTRICAL CHARACTERISTICS over operating range (note 1)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5 mA 2.2 kΩ to 5.5 V		2.4		V_{CC}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 5 mA		V_{SS}		0.4	Volts
V_{IH}	Input HIGH Voltage (Except CE)			2.4		V_{CC}	Volts
V_{IL}	Input LOW Voltage (Except CE)			−0.6		0.8	Volts
$V_{IH(CE)}$	Chip Enable Input HIGH Voltage			V_{DD} −0.6		V_{DD} +1.0	Volts
$V_{IL(CE)}$	Chip Enable Input LOW Voltage			−1.0		0.8	Volts
I_I	Input Load Current (Except CE)	0.6 V ≤ V_I ≤ 5.5 V				10	μA
$I_{I(CE)}$	Input Load Current, CE	−1.0 ≤ $V_{I(CE)}$ ≤ 13.2 V				10	μA
I_{DD}	V_{DD} Supply Current	$V_{IH(CE)}$ = 13.2 V			35	60	mA
		$V_{IL(CE)}$ = 0.6 V			10	200	μA
$I_{DD(AV)}$	Average V_{DD} Supply Current	Read or Write cycle minimum cycle time	Am9050C		32	60	mA
			Am9050D		34	60	
			Am9050E		35	60	
		Read/Modify/Write cycle minimum cycle time	Am9050C		32	60	
			Am9050D		34	60	
			Am9050E		35	60	
I_{BB}	V_{BB} Supply Current	V_{BB} = −5.5 V, V_{DD} = 12.6 V V_{SS} = 0 V			−5.0	−100	μA

CAPACITANCE

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
C_i	Input Capacitance (Except CE)	V_{DD} = 12 V, V_{SS} = 0 V V_{BB} = −5.0 V All inputs = 0 V f = 1 MHz			5.0	7.0	pF
$C_{i(CE)}$	Input Capacitance (Chip Enable)		$V_{I(CE)}$ = 0, 12 V		15	20	pF
$C_{I/O}$	I/O Capacitance				6.0	8.0	pF

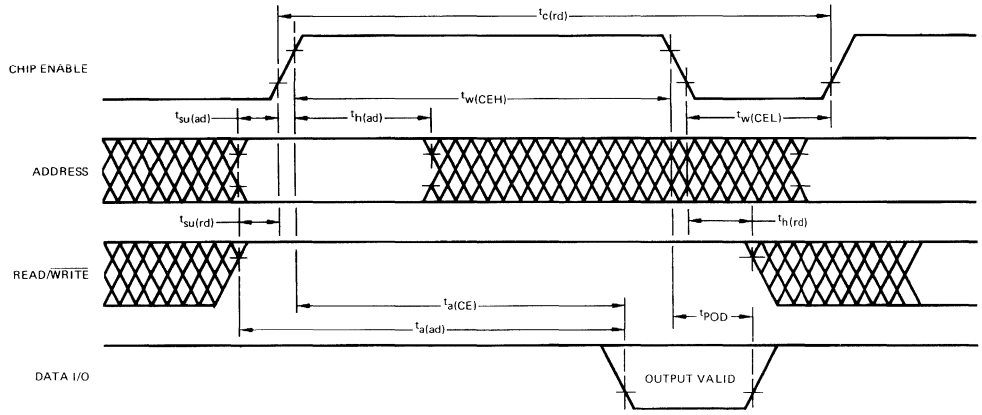
SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Test Conditions		Am9050C Min.	Am9050C Max.	Am9050D Min.	Am9050D Max.	Am9050E Min.	Am9050E Max.	Units
t_R	Column Refresh Interval				2.0		2.0		2.0	ms
Read Cycle										
$t_{c(rd)}$	Read Cycle Time	CE transition times ≤ 20ns		470		430		400		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width	Chip Enable transition times ≤ 40ns		300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width			130		130		130		ns
$t_{su(ad)}$	Address Set-up Time			0		0		0		ns
$t_{su(rd)}$	Read Set-up Time			0		0		0		ns
$t_{h(ad)}$	Address Hold Time			125		100		100		ns
$t_{h(rd)}$	Read Hold Time			0		0		0		ns
t_{POD}	CE to Output Disable Delay	Output load: TTL gate, 50pF 2.2kΩ to 5.5V		40		40		40		ns
$t_{a(CE)}$	Chip Enable Access Time (Note 6)		Chip Enable rise time ≤20ns		280		230		180	ns
$t_{a(ad)}$	Address Access Time (Note 6)				300		250		200	ns
Write Cycle										
$t_{c(wr)}$	Write Cycle Time	CE transition times ≤ 20ns		470		430		400		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width	Chip Enable transition times ≤ 40ns		300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width			130		130		130		ns
$t_{w(wr)}$	Write Pulse Width			200		190		180		ns
$t_{su(ad)}$	Address Set-up Time			0		0		0		ns
$t_{su(da)}$	Data In Set-up Time			180		170		160		ns
$t_{su(wr)}$	Write Pulse Set-up Time			240		220		210		ns
$t_{h(ad)}$	Address Hold Time			125		100		100		ns
$t_{h(da)}$	Data In Hold Time (Note 2)			0(30)		0(20)		0(10)		ns
$t_{d(wr)}$	Write Delay				40		40		40	ns
t_{POI}	Write to Output OFF Delay				40		40		40	ns
Read/Modify/Write Cycle										
$t_{c(RMW)}$	Read/Modify/Write Cycle Time	CE transition and Read/Write fall time ≤ 20ns		730		660		600		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width			560	4000	490	4000	430	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width	Chip Enable transition times ≤ 40ns		130		130		130		ns
$t_{w(wr)}$	Write Pulse Width			200		190		180		ns
$t_{su(ad)}$	Address Set-up Time			0		0		0		ns
$t_{su(da)}$	Data In Set-up Time			180		170		160		ns
$t_{su(rd)}$	Read Set-up Time			0		0		0		ns
$t_{su(wr)}$	Write Pulse Set-up Time			240		220		210		ns
$t_{h(ad)}$	Address Hold Time			125		100		100		ns
$t_{h(rd)}$	Read Hold Time			300		250		200		ns
$t_{h(da)}$	Data In Hold Time (Note 2)			0(30)		0(20)		0(10)		ns
t_{POI}	Write to Output OFF Delay	Output load: TTL gate, 50pF 2.2kΩ to 5.5V			40		40		40	ns
$t_{a(CE)}$	Chip Enable Access Time (Note 6)		Chip Enable rise time ≤ 20ns		280		230		180	ns
$t_{a(ad)}$	Address Access Time (Note 6)				300		250		200	ns

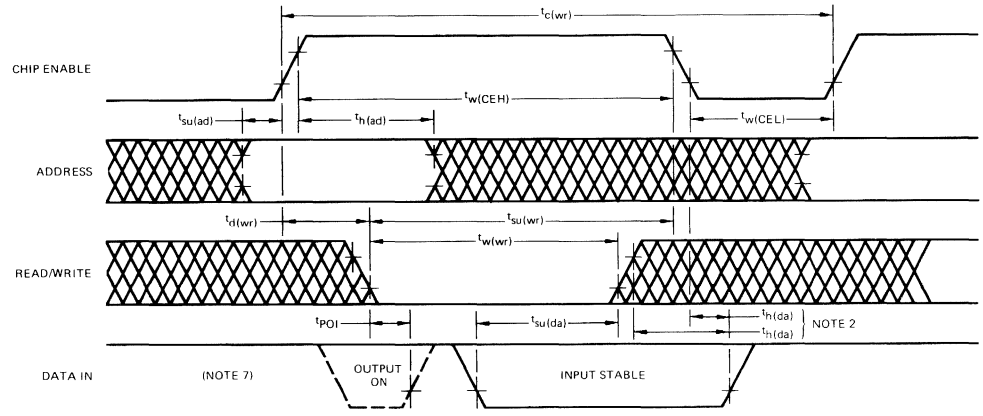
Notes:
1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Data Hold Time ($t_{h(da)}$) may be optionally specified with respect to either the rising edge of Read/Write or the falling edge of Chip Enable. The zero data hold time shown in the characteristics table is with respect to Chip Enable. Data hold time with respect to Read/Write is shown in parenthesis.
3. Input signal (except Chip Enable) timing references are 0.6V and 2.2V.
4. Chip Enable timing references are at 10% and 90% of $V_{IH}(CE)$.
5. Output timing references are 0.4V and 2.4V.
6. Slope of access time versus load capacitance is approximately 0.1ns/pF.
7. In a write cycle, when $t_{d(wr)}$, the delay between the rising edge of CE and the falling edge of R/W, exceeds 40ns then the output buffer may turn on. To avoid bus conflict with input data in such a case it is recommended that $t_{w(wr)} > t_{POI}(max.) + t_{su}(da)$ be observed. When $t_{d(wr)}$ is less than 40ns the output buffer will not turn on and t_{POI} will not apply. No bus conflict will occur in such a case and $t_{su(da)}$ (max.) will not be limited by the potential presence of output data.

SWITCHING WAVEFORMS

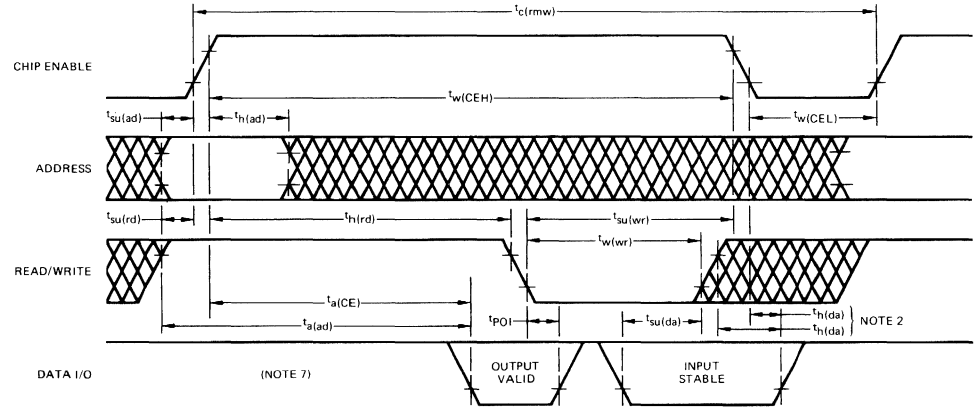
READ CYCLE



WRITE CYCLE



READ/MODIFY/WRITE CYCLE



APPLICATION INFORMATION

INTERFACE SIGNALS

The 12 Address inputs are used to specify one of 2^{12} locations within the memory ($2^{12} = 4096$). Chip Enable signals can be decoded externally for high order addressing so that several memory chips may be operated together for capacities greater than 4 K words. Registers are included on chip for the Address signals in order to simplify system timing requirements.

The Data In signal timing is specified relative to the rising edge of R/W. The Data In and Read/Write circuitry are static and the input data set-up requirement is independent of the write pulse width. The hold time for input data may be timed relative to either R/W or to CE, for extra flexibility in system design.

The Read/Write line controls the effective state of the I/O data line as well as the type of operation being performed. It may be thought of as a normally high signal that is pulsed low when writing is desired. The normally high state prevents unintentional modification of data. R/$\overline{W}$ should also be high during all refresh operations.

The Chip Enable input is a high level clock signal that controls the basic timing of all internal operations. When CE is low the memory enters the standby mode and dissipates very little power. Active operations begin when CE goes high. In a memory system with an array of storage chips, it is usually the case that only a few devices will be active at any one time, thus keeping the average power dissipation at very low levels.

The input and output data signals share a common I/O line. The output buffer is an open drain configuration permitting wired-OR connection of several chips for increased memory depth. Unclocked devices will have their outputs off, allowing other external data signals to dominate the I/O bus.

All input circuitry in the Am9050 memories is purely capacitive and does not cause clock related current surges to flow in the input lines. This feature improves noise immunity margins and helps simplify input driving requirements.

Current surges occur in the V_{DD} and V_{BB} supplies in conjunction with both the rising and falling transitions of Chip Enable. Both voltages must be decoupled to V_{SS} to prevent the current spikes from generating excessive noise.

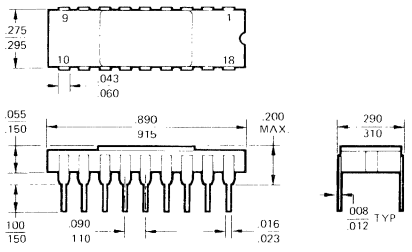
REFRESH

Information is stored as the presence or absence of charge within each internal cell. Leakage currents eventually drain away any charge present in a cell and information is lost. To prevent data loss, a cell can have its charge level restored before too much charge has leaked off. Each cell must be refreshed at least once every 2 ms, worst case.

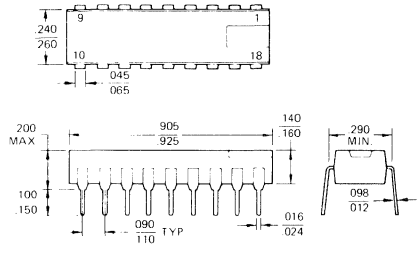
The 4096 cells in the memory matrix are organized as an array of 64 rows and 64 columns. When any cell within a row is actively cycled, all 64 locations in the row are refreshed. Thus the refresh requirement is met if all 64 rows are accessed every 2ms. Address lines A_0 through A_5 specify the rows.

PHYSICAL DIMENSIONS

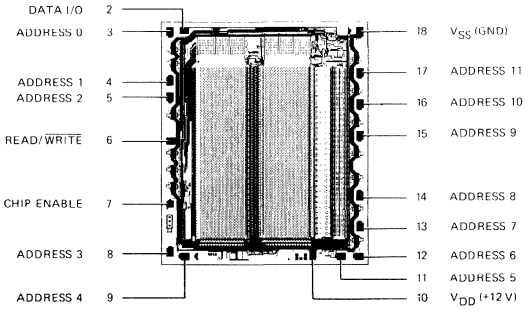
18- Pin Side Brazed



18-Pin Molded



Metallization and Pad Layout



1 – Connected to Substrate (–5 V V_{BB})

DIE SIZE 136" X 161"

Am9060

4096-Bit Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 4096 x 1 organization
- High output drive – two full TTL loads
- TTL compatible interface (except CE)
- Low power dissipation –
  400mW typ., 750mW max. operating
  5.0mW typ., 13mW max. refresh only
  0.1mW typ., 3.0mW max. standby
- Low I_{DD} current surges – easier decoupling
- Low V_{CC} current drain – 10μA
- Simplified timing requirements –
  Zero data hold with respect to CE
  Optional data hold with respect to R/W
  Optional data set-up with respect to R/W
- Low clock capacitance –20pF max.
- Unique fully capacitive input circuits –
  eliminate extraneous current surges
- Direct plug-in replacement for TMS4060
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

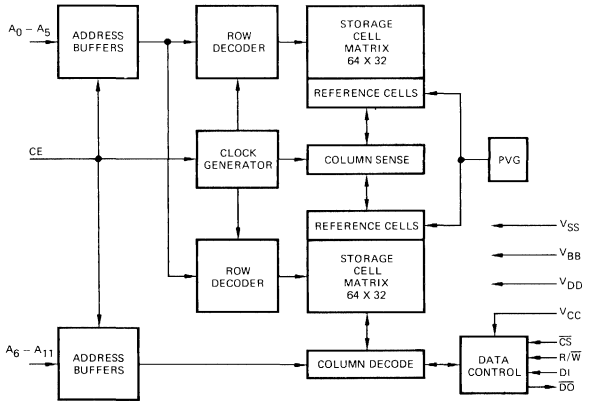
FUNCTIONAL DESCRIPTION

The Am9060 devices are high performance, 4k-bit, dynamic, read/write, random access memories. They are organized as 4096 words by 1-bit per word. The basic memory element is a one-transistor cell that stores charge on a small internal capacitor. The memory mechanism is dynamic and the chip should be periodically refreshed in order to maintain stored data integrity.

All input signals are fully TTL compatible, except the single high-level clock signal called Chip Enable. When CE goes low the memory is internally precharged and then assumes its low power standby mode. All operating cycles are initiated when CE goes high. Read-out is nondestructive so simple read or write operations are normally performed. Successive operations at the same location can be designed to improve performance since readdressing is not required. The most useful double operation combination is specified as a Read/Modify/Write cycle.

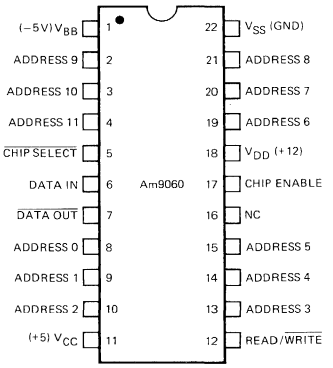
The output buffer will drive two standard TTL loads. The buffer is a three-state totem-pole configuration and exhibits a high output impedance when CE is low or when the chip is unselected. Output data polarity is inverted relative to the input data.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Access Time		
		300ns	250ns	200ns
$0°C \leq T_A \leq +70°C$	Molded DIP	AM9060CPC	AM9060DPC	AM9060EPC
	Hermetic DIP	AM9060CDC	AM9060DDC	AM9060EDC

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
All Supply Voltages with Respect to V_{BB}	−0.3 V to +20 V
All Input Signal Voltages with Respect to V_{BB}	−0.3 V to +20 V
Output Voltage with Respect to V_{SS}, Operating	−2.0 V to +7.0 V
Power Dissipation	1.0 W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	V_{DD}	V_{CC}	V_{SS}	V_{BB}
0°C to +70°C	+12 V ± 5%	+5.0 V ± 5%	0	−5.0 V ± 10%

No signal or supply voltage should ever be more than 0.3 V more negative than V_{BB}.

ELECTRICAL CHARACTERISTICS over operating range (note 1)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA		2.4		V_{CC}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA		V_{SS}		0.4	Volts
V_{IH}	Input HIGH Voltage (Except CE)			2.4		V_{CC}	Volts
V_{IL}	Input LOW Voltage (Except CE)			−0.6		0.8	Volts
$V_{IH(CE)}$	Chip Enable Input HIGH Voltage			V_{DD} −0.6		V_{DD} +1.0	Volts
$V_{IL(CE)}$	Chip Enable Input LOW Voltage			−1.0		0.8	Volts
I_I	Input Load Current (Except CE)	$V_{SS} \leq V_I \leq V_{CC}$				10	µA
$I_{I(CE)}$	Input Load Current, CE	$-1.0\,V \leq V_{I(CE)} \leq 13.2\,V$				2.0	µA
I_{OZ}	Output Leakage Current	$-0.6V \leq V_O \leq V_{CC}$ $CE = V_{IL(CE)}$ or $\overline{CS} = V_{IH}$				10	µA
I_{CC}	V_{CC} Supply Current (Note 7)	$CE = V_{IL(CE)}$ or $\overline{CS} = V_{IH}$				10	µA
I_{DD}	V_{DD} Supply Current	$V_{IH(CE)}$ = 12.6 V			32	60	mA
		$V_{IL(CE)}$ = 0.6 V			10	200	µA
$I_{DD(AV)}$	Average V_{DD} Supply Current	Read or Write cycle minimum cycle time	Am9060C		29	60	mA
			Am9060D		31	60	
			Am9060E		32	60	
		Read/Modify/Write cycle minimum cycle time	Am9060C		29	60	
			Am9060D		31	60	
			Am9060E		32	60	
I_{BB}	V_{BB} Supply Current	V_{BB} = −5.5 V, V_{DD} = 12.6 V V_{CC} = 5.25 V, V_{SS} = 0 V			−5.0	−100	µA

CAPACITANCE

Parameters	Description	Test Conditions		Typ. (Note 1)	Max.	Units
$C_{i(AW)}$	Input Capacitance (Address and Write)	V_{DD} = 12 V, V_{SS} = 0 V V_{BB} = −5.0 V, V_{CC} = 5.0 V All inputs = 0 V f = 1 MHz		5.0	7.0	pF
$C_{i(CD)}$	Input Capacitance (Chip Select and Data)			3.0	5.0	pF
$C_{i(CE)}$	Input Capacitance (Chip Enable)		$V_{I(CE)}$ = −1.0, 10.8	15	20	pF
C_O	Output Capacitance			3.0	5.0	pF

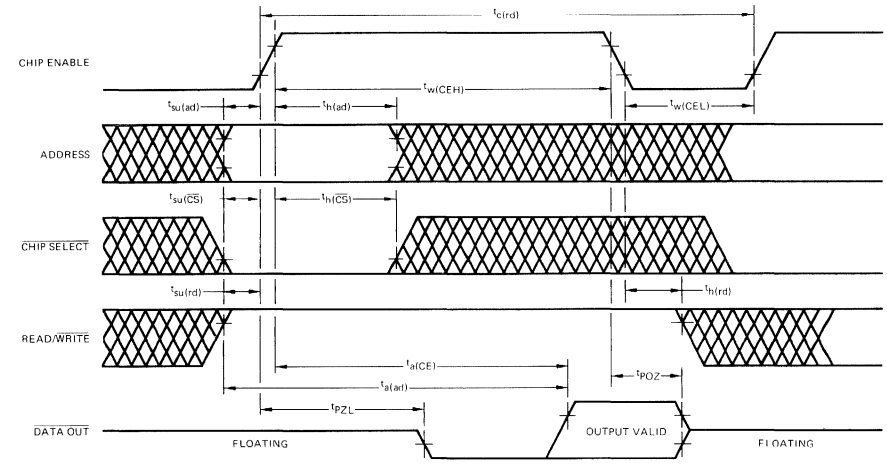
SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	Am9060C Min.	Am9060C Max.	Am9060D Min.	Am9060D Max.	Am9060E Min.	Am9060E Max.	Units
t_R	Column Refresh Interval			2.0		2.0		2.0	ms
Read Cycle									
$t_{c(rd)}$	Read Cycle Time	CE transition time ⩽ 20ns	470		430		400		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width	Chip Enable transition times ⩽40ns	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width		130		130		130		ns
$t_{su(ad)}$	Address Set-up Time		0		0		0		ns
$t_{su(CS)}$	Chip Select Set-up Time		0		0		0		ns
$t_{su(rd)}$	Read Set-up Time		0		0		0		ns
$t_{h(ad)}$	Address Hold Time		125		100		100		ns
$t_{h(CS)}$	Chip Select Hold Time		125		100		100		ns
$t_{h(rd)}$	Read Hold Time		0		0		0		ns
t_{PZL}	Chip Enable to Output ON Delay	Output load: one standard TTL gate plus 50pF		175		150		125	ns
t_{POZ}	Chip Enable to Output OFF Delay		30		30		30		ns
$t_{a(CE)}$	Chip Enable Access Time (Note 6)	Chip enable rise time ⩽20ns		280		230		180	ns
$t_{a(ad)}$	Address Access Time (Note 6)			300		250		200	ns
Write Cycle									
$t_{c(wr)}$	Write Cycle Time	CE transition time ⩽ 20ns	470		430		400		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width	Chip Enable transition times ⩽40ns	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width		130		130		130		ns
$t_{w(wr)}$	Write Pulse Width		200		190		180		ns
$t_{su(ad)}$	Address Set-up Time		0		0		0		ns
$t_{su(CS)}$	Chip Select Set-up Time		0		0		0		ns
$t_{su(da)}$	Data In Set-up Time		180		170		160		ns
$t_{su(wr)}$	Write Pulse Set-up Time		240		220		210		ns
$t_{h(ad)}$	Address Hold Time		125		100		100		ns
$t_{h(CS)}$	Chip Select Hold Time		125		100		100		ns
$t_{h(da)}$	Data In Hold Time (Note 2)		0 (30)		0 (20)		0 (10)		ns
Read/Modify/Write Cycle									
$t_{c(RMW)}$	Read/Modify/Write Cycle Time	CE transition time and Read/Write fall time ⩽ 20ns	710		640		580		ns
$t_{w(CEH)}$	Chip Enable HIGH Pulse Width		540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Chip Enable LOW Pulse Width	Chip Enable transition times ⩽40ns	130		130		130		ns
$t_{w(wr)}$	Write Pulse Width		200		190		180		ns
$t_{su(ad)}$	Address Set-up Time		0		0		0		ns
$t_{su(CS)}$	Chip Select Set-up Time		0		0		0		ns
$t_{su(da)}$	Data In Set-up Time		180		170		160		ns
$t_{su(rd)}$	Read Set-up Time		0		0		0		ns
$t_{su(wr)}$	Write Pulse Set-up Time		240		220		210		ns
$t_{h(ad)}$	Address Hold Time		125		100		100		ns
$t_{h(CS)}$	Chip Select Hold Time		125		100		100		ns
$t_{h(rd)}$	Read Hold Time		280		230		180		ns
$t_{h(da)}$	Data In Hold Time (Note 2)		0 (30)		0 (20)		0 (10)		ns
t_{PZL}	Chip Enable to Output ON Delay	Output load: one standard TTL gate plus 50pF		175		150		125	ns
t_{POI}	Write to Output Invalid Delay		30		30		30		ns
t_{POZ}	Chip Enable to Output OFF Delay		30		30		30		ns
$t_{a(CE)}$	Chip Enable Access Time	Chip Enable rise time ⩽20ns		280		230		180	ns
$t_{a(ad)}$	Address Access Time (Note 6)			300		250		200	ns

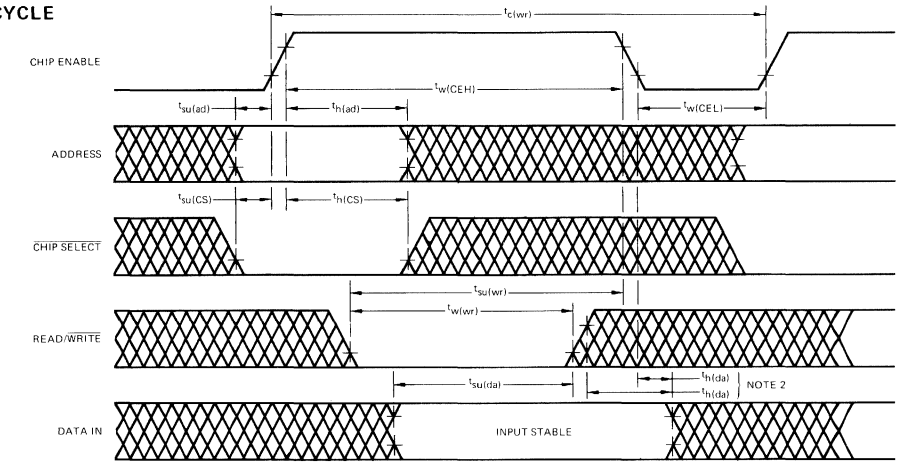
Notes:
1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Data Hold time ($t_{h(da)}$) may be optionally specified with respect to either the rising edge of Read/Write or the falling edge of Chip Enable. The zero value shown in the Characteristics table is with respect to Chip Enable. Data hold time with respect to Read/Write is shown in parenthesis.
3. Input signal (except Chip Enable) timing references are 0.6V and 2.2V.
4. Chip Enable timing references are at 10% and 90% of $V_{IH}(CE)$.
5. Output timing references are 0.4V and 2.4V.
6. Slope of access time versus load capacitance is approximately 0.1ns/pF.
7. V_{CC} supplies the final output transistor only. Except for leakage, V_{CC} supply current during CE on is dependent on output loading only.

SWITCHING WAVEFORMS

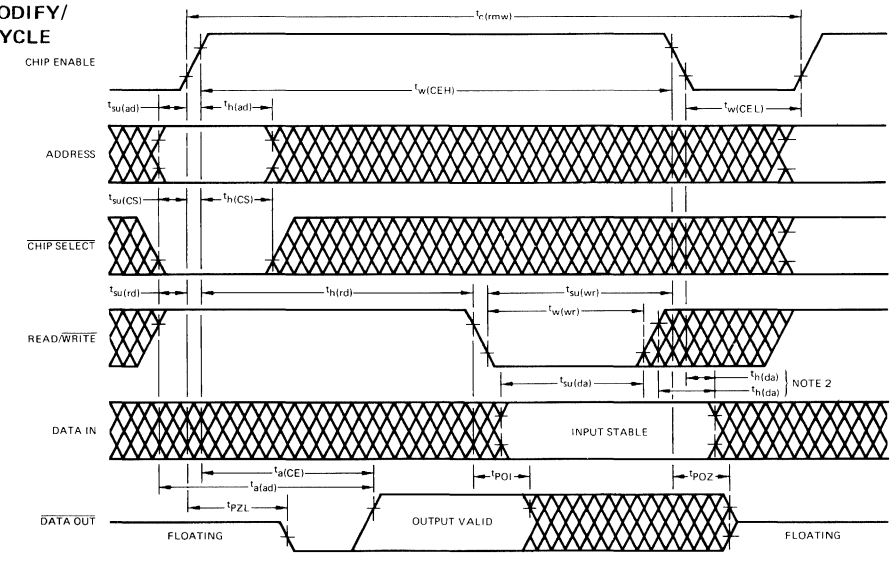
READ CYCLE



WRITE CYCLE



READ/MODIFY/ WRITE CYCLE



APPLICATION INFORMATION

INTERFACE SIGNALS

The 12 Address inputs are used to specify one of 2^{12} locations within the memory (2^{12} = 4096). The Chip Select signal acts as a high order address so that several memory chips may be operated together for capacities greater than 4k words. Registers are included on chip for the Chip Select and Address signals in order to simplify system timing requirements. After the Chip Select input has been latched by the rising edge of CE, the select status of the chip cannot be altered by changing the state of Chip Select line. Chip Select only affects the data control circuitry.

The Data In signal timing is specified relative to the rising edge of R/$\overline{W}$. The Data In and Read/Write circuitry are static and the input data set-up requirement is independent of the write pulse width. The hold time for input data may be timed relative to either R/$\overline{W}$ or to CE, for extra flexibility in system design.

The Read/Write line controls the type of operation being performed. It may be thought of as a normally high signal that is pulsed low when writing is desired. The normally high state prevents unintentional modification of data. R/$\overline{W}$ should also be high during all refresh operations, unless Chip Select is high.

The Chip Enable input is a high level clock signal that controls the basic timing of all internal operations. When CE is low the memory enters the standby mode and dissipates very little power. Active operations begin when CE goes high. In a memory system with an array of storage chips, it is usually the case that only a few devices will be active at any one time, thus keeping the average power dissipation at very low levels.

The Data Out circuitry is three-state and designed to permit wired-OR connection of several chips for greater memory depth than 4k. Unclocked or unselected devices will have high impedance outputs, allowing a selected and clocked device to dominate the output data bus. The output data is inverted relative to the input data; that is, information written in as a logic one will be read out as a logic zero. Valid output is always preceeded by a period of low output data.

All input circuitry in the Am9060 memories is purely capacitive and does not cause clock related current surges to flow in the input lines. This feature improves noise immunity margins and helps simplify input driving requirements.

Current surges occur in the V_{DD} and V_{BB} supplies in conjunction with both the rising and falling transitions of Chip Enable. Both voltages must be carefully decoupled to V_{SS} to prevent the current spikes from generating excessive noise.

REFRESH

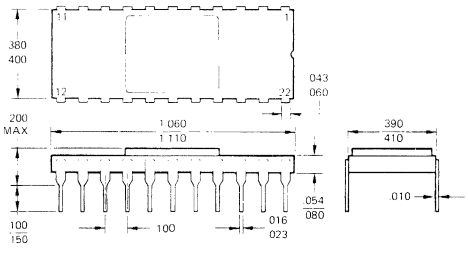
Information is stored as the presence or absence of charge within each internal cell. Leakage currents eventually drain away any charge present in a cell and information is lost. To prevent data loss, a cell can have its charge level restored before too much charge has leaked off. Each cell must be refreshed at least once every 2 ms, worst case.

The 4096 cells in the memory matrix are organized as an array of 64 rows and 64 columns. When any cell within a row is actively cycled, all 64 locations in the row are refreshed. Thus the refresh requirement is met if all 64 rows are accessed every 2 ms. Address lines A_0 through A_5 specify the rows.

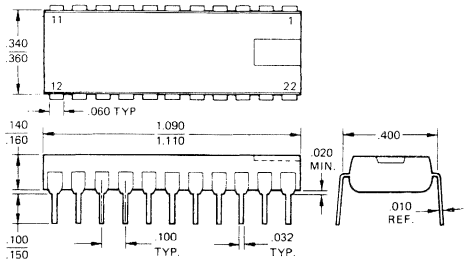
The Chip Select input only controls the Data Out and Read/Write circuitry so that a chip need not be selected in order to be refreshed. This allows parallel refreshing of many devices without causing contention on output busses.

PHYSICAL DIMENSIONS

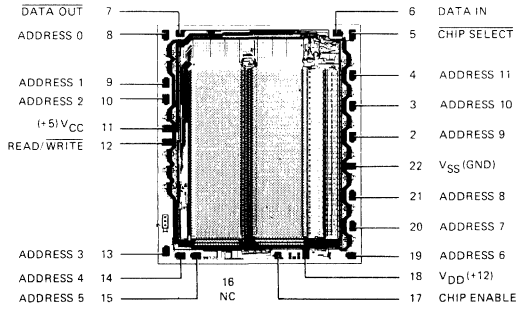
22-Pin Side Brazed



22-Pin Molded



Metallization and Pad Layout



1 – Connected to Substrate (–5V) V_{BB}

DIE SIZE 136" X 161"

Am9208
1024 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 1024 x 8 organization
- High speed – 250ns access time
- Fully capacitive inputs – simplified driving
- 2 fully programmable chip selects – increased flexibility
- Logic voltage levels compatible to TTL
- Three-state output buffers – simplified expansion
- Standard supply voltages – +12V, +5.0V
- No V_{BB} supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Direct plug-in replacement for Intel 8308/2308 and T.I. 4700

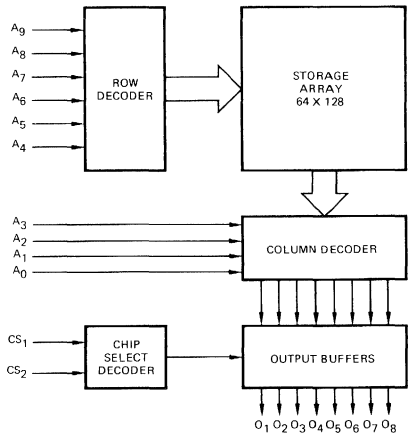
FUNCTIONAL DESCRIPTION

The Am9208 devices are high performance, 8192 bit, static, mask programmed, read only memories. Each memory is implemented as 1024 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 1024 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

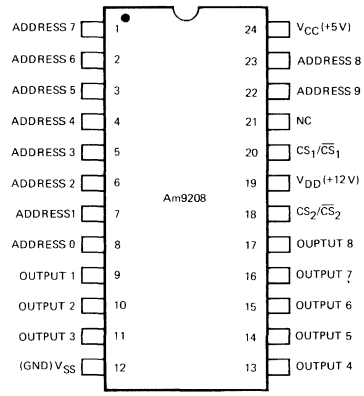
Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9208 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9208 is pin compatible with the Am9216 which is a 16k-bit mask programmed ROM. Input and output voltage levels are compatible to TTL specifications, providing simplified interfacing.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time		
		400ns	300ns	250ns
Hermetic DIP	$0°C \leq T_A \leq 70°C$	Am9208BDC	Am9208CDC	Am9208DDC
	$-55°C \leq T_A \leq 125°C$	Am9208BDM	Am9208CDM	

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{DD} with Respect to V_{SS}	15V
V_{CC} with Respect to V_{SS}	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{DD}	V_{CC}	V_{SS}
Am9208DC	$0°C \leq T_A \leq +70°C$	+12V ± 5%	+5.0V ± 5%	0V
Am9208DM	$-55°C \leq T_A \leq +125°C$	+12V ± 10%	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

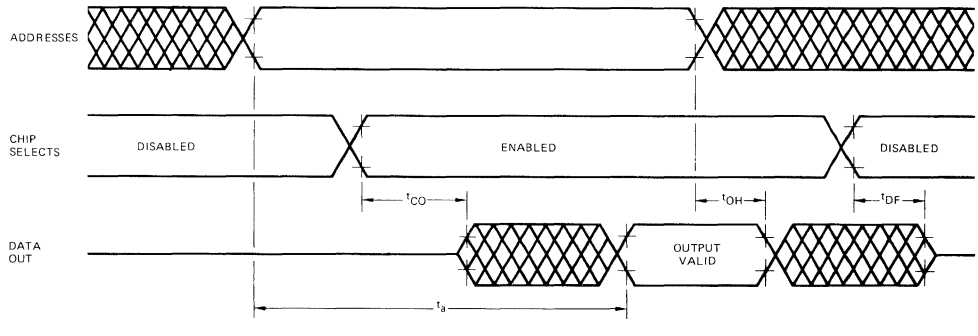
Parameters	Description	Test Conditions		Am9208DC Min.	Am9208DC Max.	Am9208DM Min.	Am9208DM Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0mA$		3.7		3.7		Volts
		$I_{OH} = -4.0mA$		2.4		2.4		
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$			0.4		0.4	Volts
V_{IH}	Input HIGH Voltage			2.4	$V_{CC}+1.0$	2.6	$V_{CC}+1.0$	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
I_{LO}	Output Leakage Current	Chip disable		10		10		μA
I_{LI}	Input Leakage Current			10		10		μA
I_{DD}	V_{DD} Supply Current	Selected	Am9208B/C	35		43		mA
			Am9208D	44		50		
		Deselected	Am9208B/C	48		53		
			Am9208D	55		61		
I_{CC}	V_{CC} Supply Current		Am9208B/C	13		15		mA
			Am9208D	15		17		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Am9208BDC Am9208BDM Min.	Am9208BDC Am9208BDM Max.	Am9208CDC Am9208CDM Min.	Am9208CDC Am9208CDM Max.	Am9208DDC Min.	Am9208DDC Max.	Units
t_a	Address to Output Access Time	$t_r = t_f = 20ns$		400		300		250	ns
t_{CO}	Chip Select to Output ON Delay	Output load: one standard TTL gate plus 100pF (Note 1)		160		140		125	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change		20		20		20		ns
t_{DF}	Chip Select to Output OFF Delay			120		100		90	ns
C_I	Input Capacitance	$T_A = 25°C$, f = 1MHz		6.0		6.0		6.0	pF
C_O	Output Capacitance	All pins at 0V		6.0		6.0		6.0	pF

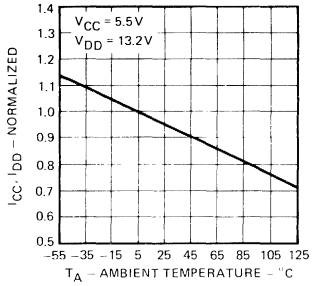
Notes: 1. Timing reference levels — Inputs: High = 2.0V, Low = 1.0V. Outputs: High = 2.4V, Low = 0.8V.

SWITCHING WAVEFORMS

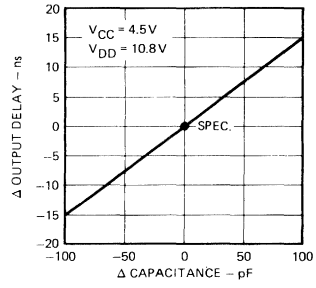


TYPICAL CHARACTERISTICS

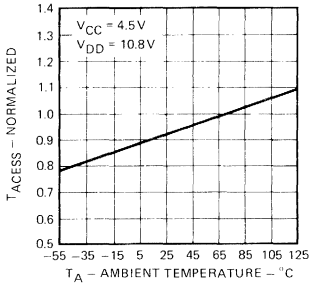
I_{DD}, I_{CC} Versus Temperature (Normalized)



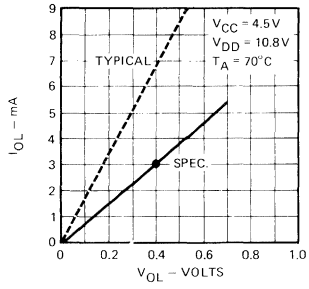
Δ Output Capacitance Versus Δ Output Delay



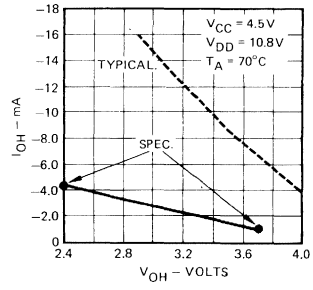
T_{Access} Versus Temperature (Normalized)



I_{OL} Versus V_{OL}



I_{OH} Versus V_{OH}



PROGRAMMING INSTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9208 is programmed from punched cards, card coding forms or from paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	9208B or 9208C
65 thru 72	Data

SECOND CARD

Column Number	Description
31	CS_2 input required to select chip (0 or 1)
33	CS_1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

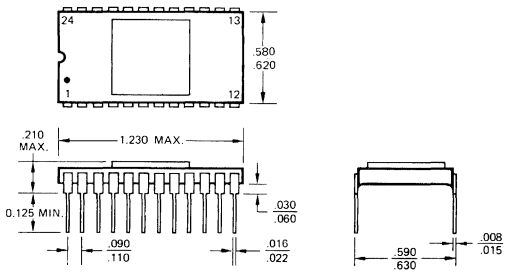
OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 1024 data cards are required.

Column Number	
10, 12, 14, 16, 18 20, 22, 24, 26, 28	Address input pattern with the most significant bit (A_9) in column 10 and the least significant bit (A_0) in column 28.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O_8) in column 40 and the least significant bit (O_1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 64 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 3F: 64 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

ADDR	OUTPUT VALUES FOR ADDR +															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
21 22 23	30 31	32 33 34	35 36 37	38 39 40	41 42 43 44	45 46 47	48 49 50	51 52	53 54 55	56 57 58	59 60 61	62 63 64	65 66 67	68 69 70	71 72 73 74	75 76
0 0 0																
0 1 0																
0 2 0																
• • •																
1 F 0																
2 0 0																
• • •																
3 F 0																

PHYSICAL DIMENSIONS
Dual-In-Line
24-Pin Side Brazed



Am9216
2048 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- High speed – 300ns access time
- Fully capacitive inputs – simplified driving
- 2 fully programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers – simplified expansion
- Standard supply voltages – +12V, +5.0V
- No V_{BB} supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

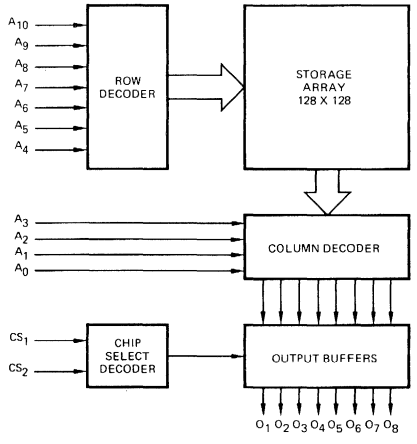
FUNCTIONAL DESCRIPTION

The Am9216 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

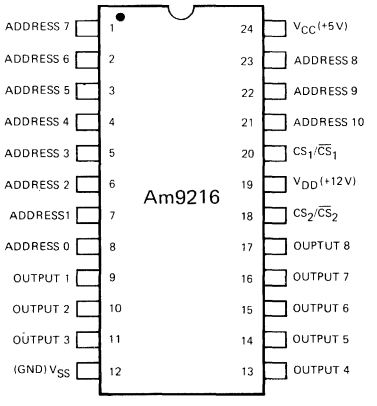
Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9216 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9216 is pin compatible with the Am9208 which is an 8k-bit mask programmed ROM. Input and output voltage levels are compatible with TTL specifications.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		400ns	300ns
Hermetic DIP	$0°C \leq T_A \leq 70°C$	AM9216BDC	AM9216CDC
	$-55°C \leq T_A \leq 125°C$	AM9216BDM	

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{DD} with Respect to V_{SS}	15V
V_{CC} with Respect to V_{SS}	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{DD}	V_{CC}	V_{SS}
Am9216DC	$0°C \leq T_A \leq +70°C$	+12V ± 5%	+5.0V ± 5%	0V
Am9216DM	$-55°C \leq T_A \leq +125°C$	+12V ± 10%	+5.0V ± 10%	0V

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions		Am9216DC Min.	Am9216DC Max.	Am9216DM Min.	Am9216DM Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0mA$		3.7		3.7		Volts
		$I_{OH} = -4.0mA$		2.4		2.4		
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$			0.4		0.4	Volts
V_{IH}	Input HIGH Voltage			2.4	$V_{CC}+1.0$	2.6	$V_{CC}+1.0$	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
I_{LO}	Output Leakage Current	Chip disabled			10		10	μA
I_{LI}	Input Leakage Current				10		10	μA
I_{DD}	V_{DD} Supply Current	Selected	Am9216B		42		47	mA
			Am9216C		49			
		Deselected	Am9216B		52		57	
			Am9216C		60			
I_{CC}	V_{CC} Supply Current		Am9216B		13		15	mA
			Am9216C		15			

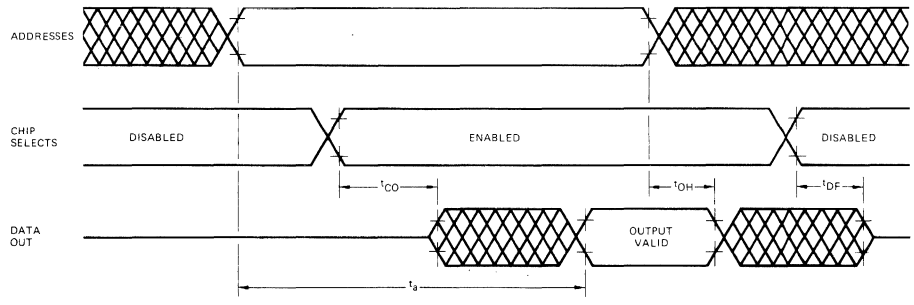
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Am9216BDC, Am9216BDM, Am9216CDC

Parameters	Description	Test Conditions	Am9216DC/DM Min.	Am9216DC/DM Max.	Am9216CDC Min.	Am9216CDC Max.	Units
t_a	Address to Output Access Time	$t_r = t_f = 20ns$ Output load: one standard TTL gate plus 100pF (Note 1)		400		300	ns
t_{CO}	Chip Select to Output ON Delay			160		140	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change		20		20		ns
t_{DF}	Chip Select to Output OFF Delay			120		100	ns
C_I	Input Capacitance	$T_A = 25°C$, f = 1.0MHz All pins at 0V		6.0		6.0	pF
C_O	Output Capacitance			6.0		6.0	pF

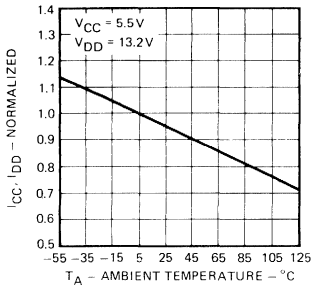
Notes: 1. Timing reference levels — Inputs: High = 2.0V, Low = 1.0V.
Outputs: High = 2.4V, Low = 0.8V.

SWITCHING WAVEFORMS

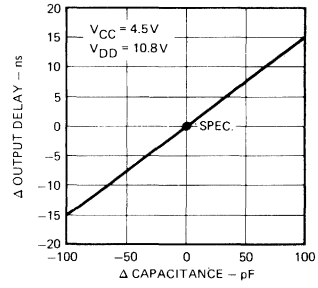


TYPICAL CHARACTERISTICS

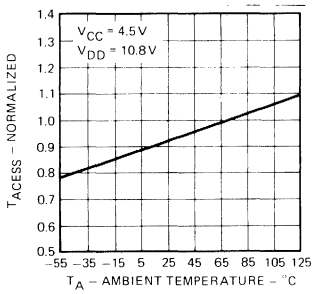
I_{DD}, I_{CC} Versus Temperature (Normalized)



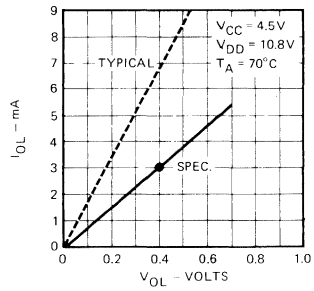
Δ Output Capacitance Versus Δ Output Delay



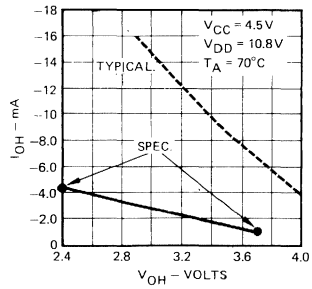
T_{Access} Versus Temperature (Normalized)



I_{OL} Versus V_{OL}



I_{OH} Versus V_{OH}



PROGRAMMING INSTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9216 is programmed from punched cards, card coding forms or from paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	9216B or 9216C
65 thru 72	Data

SECOND CARD

Column Number	Description
31	CS_2 input required to select chip (0 or 1)
33	CS_1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

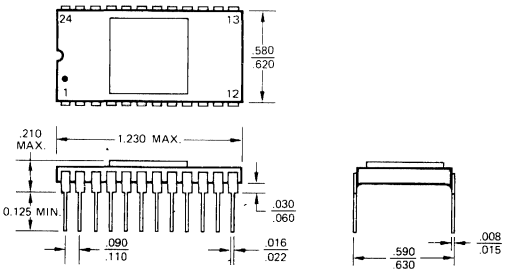
OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

Column Number	
10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A_{10}) in column 10 and the least significant bit (A_0) in column 30.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O_8) in column 40 and the least significant bit (O_1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data in entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

ADDR	OUTPUT VALUES FOR ADDR +															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
21 22 23	30 31	32 33	34 35	36 37	38 39	40 41	42 43	44 45	46 47	48 49	50 51	52 53	54 55	56 57	58 59	60 61	62 63	64 65	66 67	68 69	70 71	72 73	74 75	76
0 0 0																
0 1 0																
0 2 0																
• • •																
1 F 0																
2 0 0																
• • •																
3 F 0																
• • •																
7 F 0																

PHYSICAL DIMENSIONS
Dual-In-Line
24-Pin Side Brazed



Am9217/8316A

2048 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316A
- Access times as fast as 450 ns
- Fully capacitive inputs — simplified driving
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Drives two full TTL loads
- Single supply voltage — +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

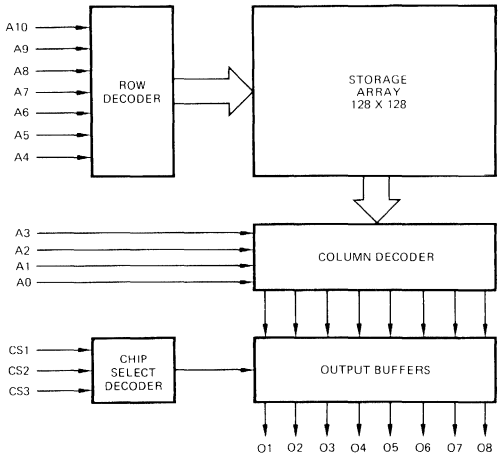
FUNCTIONAL DESCRIPTION

The Am9217 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

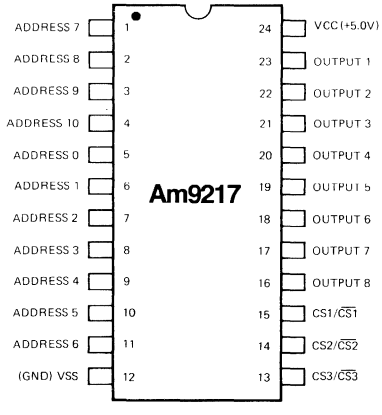
Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9217 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		550 ns	450ns
Hermetic DIP	$0°C \leq T_A \leq 70°C$	Am9217ADC C8316A	Am9217BDC
	$-55°C \leq T_A \leq 125°C$	Am9217ADM	Am9217BDM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS

Am9217ADC, Am9217BDC, C8316A: T_A = 0°C to +70°C, VCC = 5.0V ± 5%

Parameters	Description	Test Conditions		Am9217XDC Min.	Am9217XDC Max.	C8316A Min.	C8316A Max.	Units
VOH	Output HIGH Voltage	9217	IOH = −200µA	2.4				Volts
		8316A	IOH = −100µA			2.2		
VOL	Output LOW Voltage	9217	IOH = 3.2mA		0.4			Volts
		8316A	IOL = 2.0mA				0.45	
VIH	Input HIGH Voltage			2.0	VCC + 1.0	2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled			10		10	µA
ILI	Input Leakage Current				10		10	µA
ICC	VCC Supply Current				70		98	mA

ELECTRICAL CHARACTERISTICS

Am9217ADM, Am9217BDM: T_A = −55°C to +125°C, VCC = 5.0V ± 10%

Parameters	Description	Test Conditions		Am9217XDM Min.	Am9217XDM Max.	Min.	Max.	Units
VOH	Output HIGH Voltage	9217	IOH = −200µA	2.2				Volts
VOL	Output LOW Voltage	9217	IOL = 3.2mA		0.45			Volts
VIH	Input HIGH Voltage			2.0	VCC + 1.0			Volts
VIL	Input LOW Voltage			−0.5	0.8			Volts
ILO	Output Leakage Current	Chip Disabled			10			µA
ILI	Input Leakage Current				10			µA
ICC	VCC Supply Current				80			mA

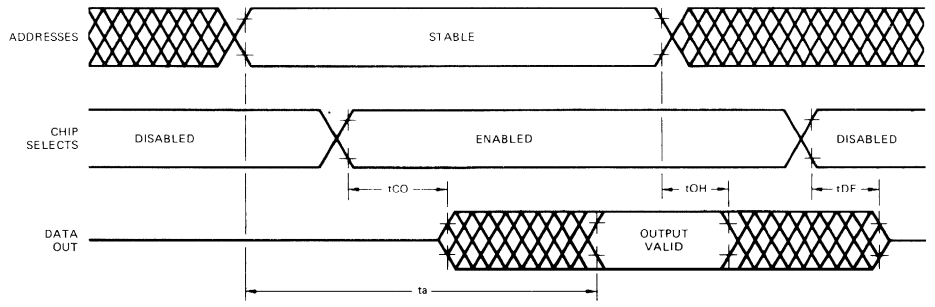
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Am9217XDC/C8316A: T_A = 0°C to +70°C, VCC = 5.0V ± 5%
Am9217XDM: T_A = −55°C to +125°C, VCC = 5.0V ± 10%

Parameters	Description	Test Conditions	Am9217A Min.	Am9217A Max.	Am9217B Min.	Am9217B Max.	8316A Min.	8316A Max.	Units
ta	Address to Output Access Time	tr = tf = 20ns Output load: one standard TTL gate plus 100pF (Note 1)		550		450		850	ns
tCO	Chip Select to Output ON Delay			180		150		300	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		–		ns
tDF	Chip Select to Output Off Delay			180		150		300	ns
CI	Input Capacitance	T_A = 25°C, f = 1.0MHz All pins at 0V		7.0		7.0		10	pF
CO	Output Capacitance			7.0		7.0		15	pF

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

SWITCHING WAVEFORMS



PROGRAMMING INSTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9217 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0 V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	8316A or 9217
65 thru 72	Optional information

SECOND CARD

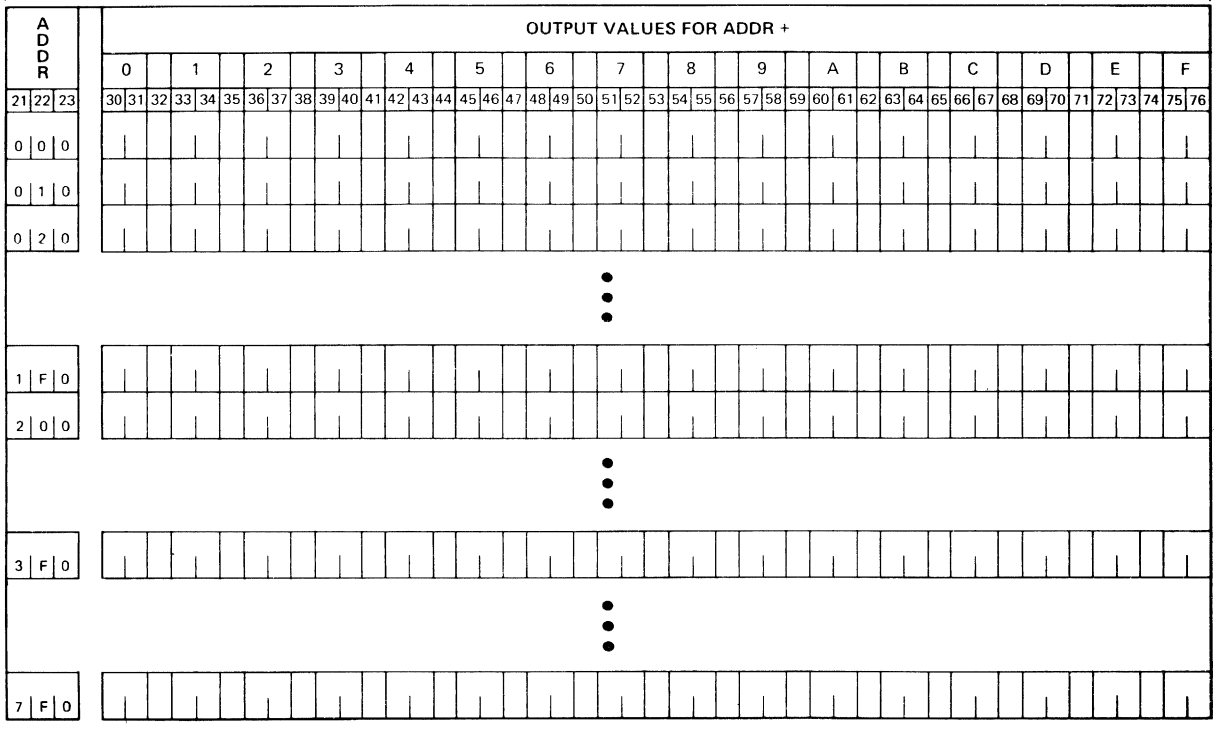
Column Number	Description
29	CS3 input required to select chip (0 or 1)
31	CS2 input required to select chip (0 or 1)
33	CS1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

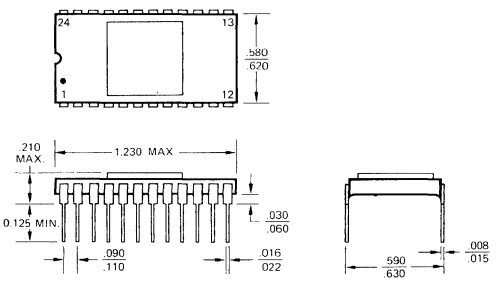
OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

Column Number	
10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data in entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



PHYSICAL DIMENSIONS
Dual-In-Line
24-Pin Side Brazed



Am9218/8316E

2048 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316E
- Access times as fast as 350 ns
- Fully capacitive inputs — simplified driving
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Drives two full TTL loads
- Single supply voltage — +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

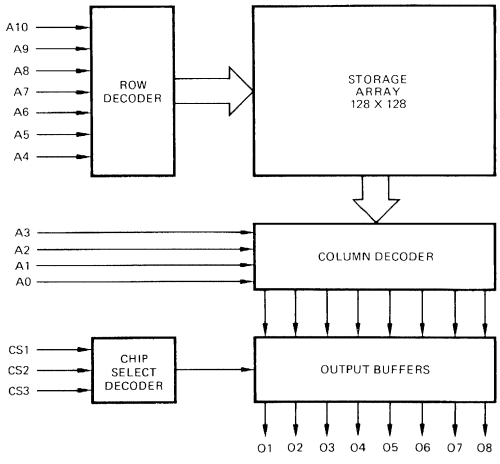
FUNCTIONAL DESCRIPTION

The Am9218 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

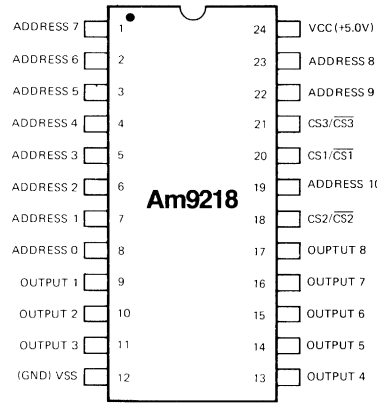
Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9218 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		450 ns	350 ns
Hermetic DIP	$0°C \leq T_A \leq 70°C$	Am9218BDC C8316E	Am9218CDC
	$-55°C \leq T_A \leq 125°C$	Am9218BDM	

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS

Am9218BDC, Am9218CDC, C8316A: $T_A = 0°C$ to $+70°C$, VCC = 5.0V ±5%

Parameters	Description	Test Conditions		Am9218XDC Min.	Am9218XDC Max.	C8316E Min.	C8316E Max.	Units
VOH	Output HIGH Voltage	9218	IOH = −200µA	2.4				Volts
		8316E	IOH = −100µA			2.4		
VOL	Output LOW Voltage	9218	IOL = 3.2mA		0.4			Volts
		8316E	IOL = 2.1mA				0.4	
VIH	Input HIGH Voltage			2.0	VCC + 1.0	2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled			10		10	µA
ILI	Input Leakage Current				10		10	µA
ICC	VCC Supply Current				70		95	mA

ELECTRICAL CHARACTERISTICS

Am9218BDM: $T_A = -55°C$ to $+125°C$, VCC = 5.0V ±10%

Parameters	Description	Test Conditions	Am9218B Min.	Am9218B Max.	Units
VOH	Output HIGH Voltage	IOH = −200µA	2.2		Volts
VOL	Output LOW Voltage	IOL = 3.2mA		0.45	Volts
VIH	Input HIGH Voltage		2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage		−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled		10	µA
ILI	Input Leakage Current			10	µA
ICC	VCC Supply Current			80	mA

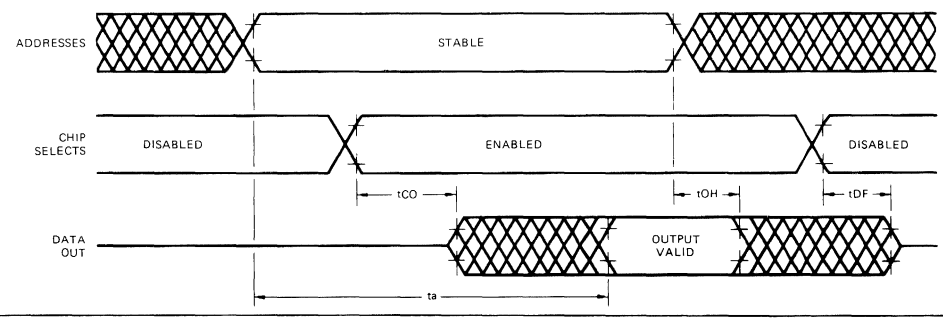
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Am9218XDC/C8316E: $T_A = 0°C$ to $+70°C$, VCC = 5.0V ± 5%
Am9218BDM: $T_A = -55°C$ to $+125°C$, VCC = 5.0V ± 10%

Parameters	Description	Test Conditions	Am9218B Min.	Am9218B Max.	Am9218C Min.	Am9218C Max.	8316E Min.	8316E Max.	Units
ta	Address to Output Access Time	tr = tf = 20ns Output Load: one standard TTL gate plus 100pF (Note 1)		450		350		450	ns
tCO	Chip Select to Output ON Delay			150		130		250	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		–		ns
tDF	Chip Select to Output OFF Delay			150		130		250	ns
CI	Input Capacitance	$T_A = 25°C$, f = 1.0MHz All pins at 0V		7.0		7.0		7.0	pF
CO	Output Capacitance			7.0		7.0		7.0	pF

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

SWITCHING WAVEFORMS



PROGRAMMING INSTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9218 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.
Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0 V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	8316E or 9218
65 thru 72	Optional information

SECOND CARD

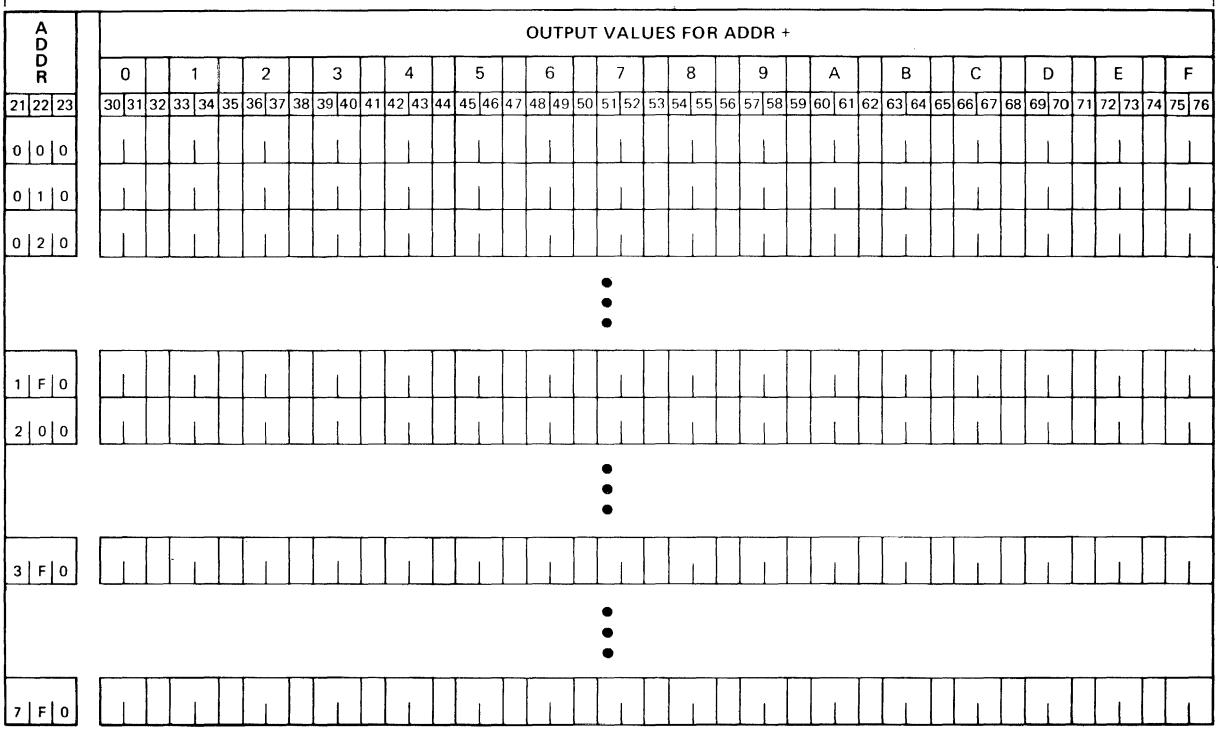
Column Number	Description
29	CS3 input required to select chip (0 or 1)
31	CS2 input required to select chip (0 or 1)
33	CS1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

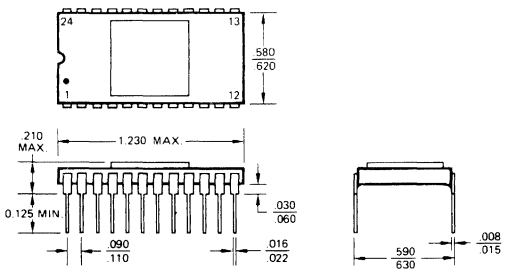
OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

Column Number	
10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data in entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



PHYSICAL DIMENSIONS
Dual-In-Line
24-Pin Side Brazed



Am1702A

256-Word by 8-Bit Programmable ROM's

Distinctive Characteristics

- Field programmable 2048-bit ROM's
- Am1702A can be erased and reprogrammed by UV light
- 100% tested for programmability
- Typical programming time of 2 minutes/device
- Available for operation over full military temperature range
- 100% processing to MIL-STD-883

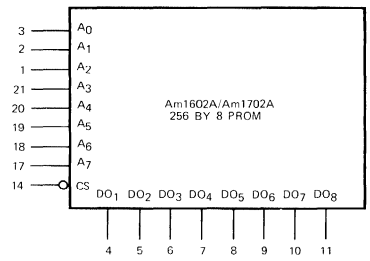
FUNCTIONAL DESCRIPTION

The Am1702A is a 256-word by 8-bit field programmable MOS read-only memory, differing only in the package. The Am1702A package has a quartz lid through which the PROM can be erased by ultraviolet light.

The device is shipped with all outputs at a logic LOW level. Each bit in the memory can be electrically programmed to a HIGH level. The device has three-state outputs which go to a high-impedance OFF state when the chip select is HIGH. When the chip select is LOW, the outputs can drive one TTL unit load.

The Am1702A can directly replace the Intel 1702A. Except for programming procedure, the Am1702A can replace the 1702. (The Am1702A differs from the Am1702 only in the programming method and in the programmed state. The Am1702 is initially all HIGH, and the LOW's are programmed; the Am1602A/1702A is initially all LOW and the HIGH's are programmed. Once programmed, they are identical).

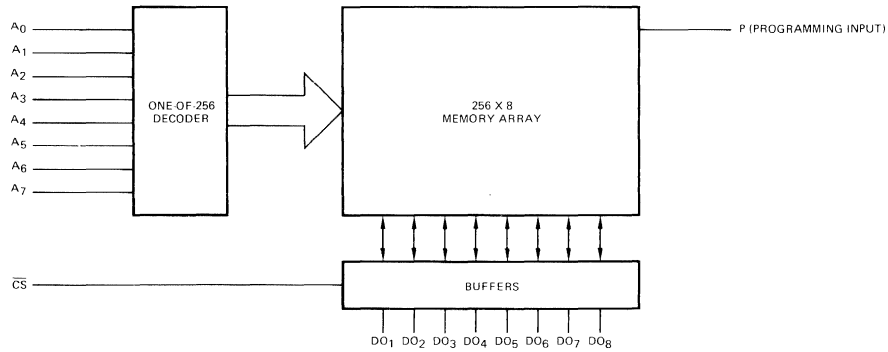
LOGIC SYMBOL



V_{CC} = Pin 12
V_{DD} = Pin 24
V_{GG} = Pin 16
V_{BB} = Pin 15
P = Pin 13

Pins 22 and 23 must be connected to V_{CC}.

LOGIC BLOCK DIAGRAM

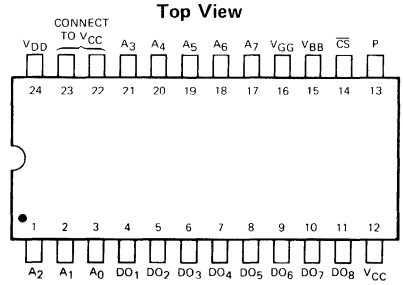


ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP/Quartz Lid	0°C to +70°C	AM1702ADC
Hermetic Dip/Quartz Lid	−55°C to +85°C	AM9702AHDL

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +125°C
Temperature (Ambient) Under Bias	−55°C to +70°C
Power Dissipation	1 W
Input and Supply Voltages (Operating)	V_{CC} −20 V to V_{CC} +0.5 V
Input and Supply Voltages (Programming)	−50 V

OPERATING RANGE

Part Number	V_{CC}	V_{DD}	V_{GG}	Ambient Temperature
C1702A	+5.0 V ± 5%	−9.0 V ± 5%	−9.0 V ± 5%	0°C to +70°C

During operation V_{BB} = P = pin 22 = pin 23 = V_{CC}.

D. C. CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Level	I_{OH} = −200μA	3.5	4.5		V
V_{OL}	Output LOW Level	I_{OL} = 1.6 mA		−.7	0.45	V
I_{OH}	Output HIGH Current	V_{OUT} = 0.0 V	−2.0			mA
I_{OL}	Output LOW Current	V_{OUT} = 0.45 V	1.6	4		mA
V_{IH}	Input HIGH Level		V_{CC}−2.0		V_{CC}+0.3	V
V_{IL}	Input LOW Level		V_{CC}−10.0		V_{CC}−4.2	V
I_{LI}	Input Leakage Current	V_{IN} = 0.0 V			1.0	μA
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{CC}−2.0, V_{OUT} = 0.0 V			1.0	μA
I_{CF1}	Output Clamp Current	T_A = 0°C, V_{OUT} = −1.0 V		8	14	mA
I_{CF2}	Output Clamp Current	T_A = 25°C, V_{OUT} = −1.0 V			13	mA
I_{GG}	V_{GG} Current				1.0	μA
I_{DD0}	V_{DD} Current (Note 1)	V_{GG} = V_{CC}, I_{OL} = 0 $V_{\overline{CS}}$ = V_{CC}−2.0, T_A = 25°C		5	10	mA
I_{DD1}		I_{OL} = 0, $V_{\overline{CS}}$ = V_{CC}−2.0, T_A = 25°C		35	50	mA
I_{DD2}		I_{OL} = 0, $V_{\overline{CS}}$ = 0, T_A = 25°C		32	46	mA
I_{DD3}		I_{OL} = 0, $V_{\overline{CS}}$ = V_{CC}−2.0, T_A = 0°C		38.5	60	mA

Note: 1. I_{DD} may be reduced by pulsing the V_{GG} supply between V_{CC} and −9 V. V_{DD} current will be directly proportional to V_{GG} duty cycle. The data outputs will be unaffected by address or chip select changes while V_{GG} is at V_{CC}. For this option specify Am1702AL.

CAPACITANCE (T_A = 25°C)

(These parameters are guaranteed by design and are not 100% tested)

Parameters	Description	Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	All unused pins are at V_{CC}	8	15	pF
C_{OUT}	Output Capacitance		10	15	pF
C_{VGG}	V_{GG} Capacitance			30	pF

A. C. CHARACTERISTICS OVER OPERATING RANGE

V_{IL} = 0V, V_{IH} = 4.0V, t_r - $t_f \leq$ 50ns, Load = 1 TTL Gate.

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
f_{reg}	Repetition Rate				1.0	MHz
t_{OH}	Previous Read Data Valid				100	ns
t_{ACC}	Address to Output Delay			0.7	1.0	μs
t_{DVGG}	Set-up Time, V_{GG}		0			μs
$t_{\overline{CS}}$	Chip Select Delay				100	ns
t_{CO}	Output Delay from $\overline{CS}$				900	ns
t_{OD}	Output Deselect	T_A - 0°C to +70°C			300	ns
t_{OHC}	Data Out Valid from V_{GG} (Note 2)				5.0	μs

Note: 2. The output will remain valid for t_{OHC} after the V_{GG} pin is raised to V_{CC}, even if address changes occur.

SWITCHING WAVEFORMS

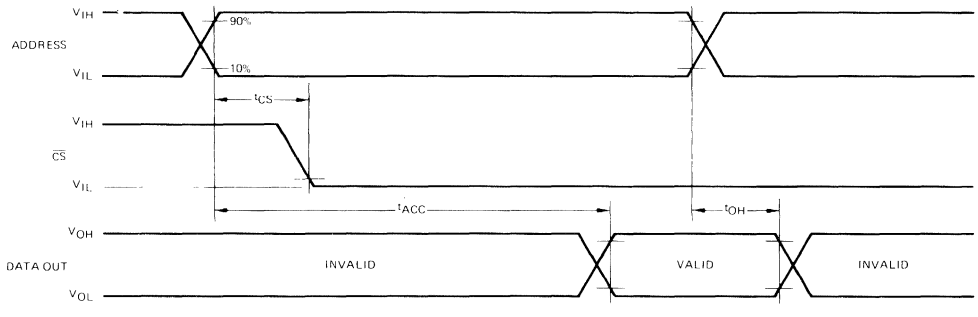


Figure 1. Reading Data

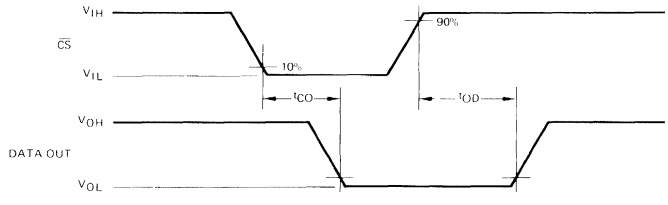


Figure 2. Deselecting Output from Chip Select.

CLOCKED V_{GG} OPERATION

The V_{GG} input may be switched between +5 V (V_{CC}) and −9 V to save power. To read data, the V_{GG} level must be lowered to −9 V at least t_{DVGG} prior to the address selection. Once data has appeared at the output (t_{ACC}), V_{GG} may be raised to +5 V. The data output will remain steady for t_{OHC}. To deselect the chip, $\overline{CS}$ must be raised to V_{IH} prior to raising V_{GG} to +5 V. If $\overline{CS}$ goes HIGH while V_{GG} is at V_{CC}, deselection of the chip will not occur until t_{OD} after V_{GG} goes back to −9 V.

PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage at the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape the gate region, erasing the program and restoring the device to all LOW.

Programming a bit is accomplished by addressing the desired word using negative 44V logic levels, applying a negative voltage to V_{DD}, V_{GG}, and the outputs to be programmed, and then applying a −49 volt pulse to the programming pin. The duty cycle on the programming pin should not exceed 20% to avoid over-heating the device. For long-term data retention, at least 32 program pulses should be applied for each address. All eight outputs are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm² at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficiently in the UV to erase or "soften" the PROM.)

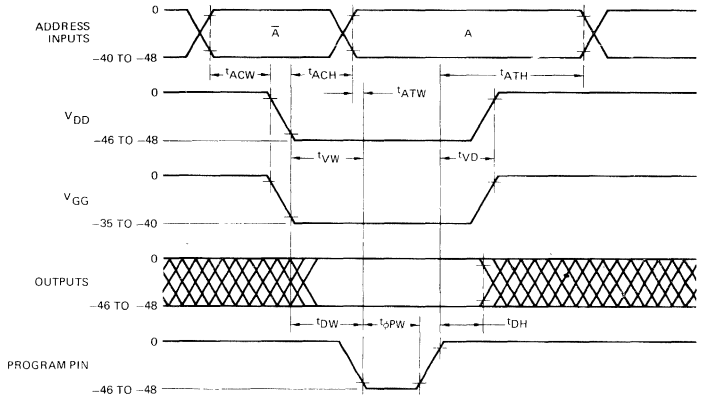
PROGRAMMING REQUIREMENTS (T_A = 25°C, V_{CC} = 0V, CS = 0V, V_{BB} = +12V ± 10%)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
I_{LI1P}	Input Current, Address and Data	V_{IN} = −48V			10	mA
I_{LI2P}	Input Current, Program and V_{GG} Inputs	V_{IN} = −48V			10	mA
I_{BB}	V_{BB} Current	(Note 2)		10		mA
I_{DDP}	I_{DD} Current During Programming Pulse	$V_{DD} = V_{Prog}$ = −48V, V_{GG} = −35V		200	Note 1	mA
V_{IHP}	Input HIGH Voltage				0.3	Volts
V_{IL1P}	Voltage Applied to Output to Program a HIGH		−46		−48	Volts
V_{IL2P}	Input LOW Level on Address Inputs		−40		−48	Volts
V_{IL3P}	Voltage Applied to V_{DD} and Program Inputs		−46		−48	Volts
V_{IL4P}	Voltage Applied to V_{GG} Input		−35		−40	Volts
$t_{\phi PW}$	Programming Pulse Width	V_{GG} = −35V, $V_{DD} = V_{Prog}$ = −48V			3	ms
t_{DW}	Data Set-up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{GG} and V_{DD} Set-up Time		100			μs
t_{VD}	V_{GG} and V_{DD} Hold Time		10		100	μs
t_{ACW}	Address Set-up Time (Complement)		25			μs
t_{ACH}	Address Hold Time (Complement)		25			μs
t_{ATW}	Address Set-up Time (True)		10			μs
t_{ATH}	Address Hold Time (True)		10			μs
	Duty Cycle				20	%

Note: 1. Do not allow I_{DD} to exceed 300mA for more than 100μs.

2. V_{BB} supply must be current limited to 100mA max.

PROGRAMMING WAVEFORMS

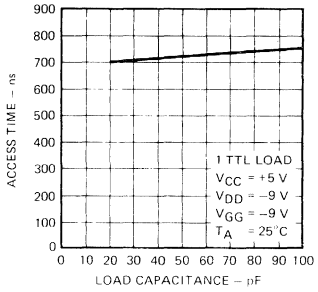


$\overline{A}$ = binary complement of address to be programmed.

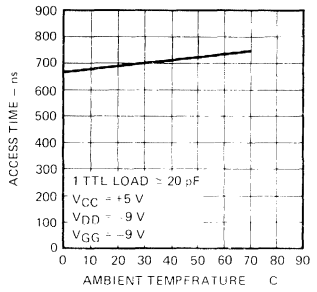
A = binary address to be programmed.

TYPICAL PERFORMANCE CURVES

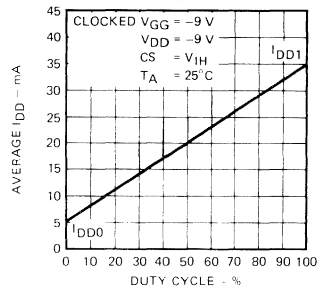
Access Time Versus Load Capacitance



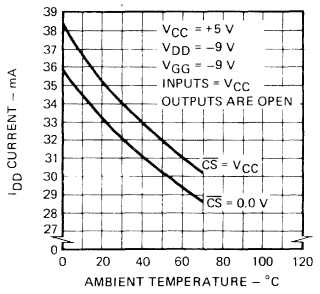
Access Time Versus Temperature



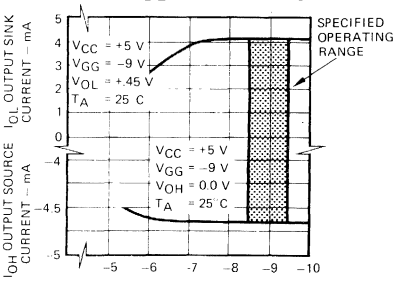
Average Current Versus Duty Cycle for Clocked V_{GG}



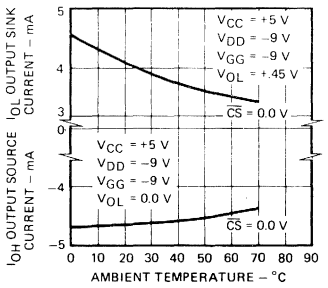
I_{DD} Current Versus Temperature



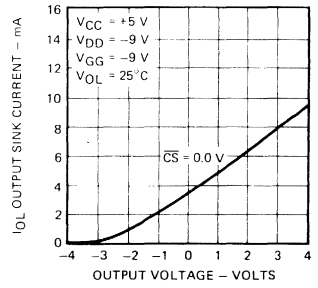
Output Current Versus V_{DD} Supply Voltage



Output Current Versus Temperature



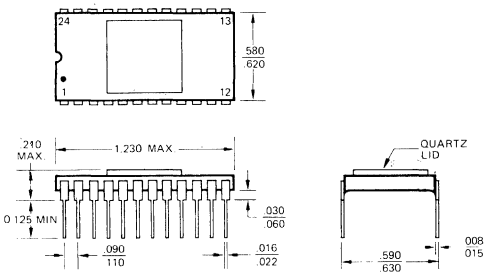
Output Sink Current Versus Output Voltage



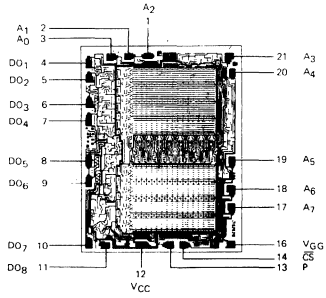
PHYSICAL DIMENSIONS
Dual-In-Line

24-Pin Side Brazed

Quartz Lid



Metallization and Pad Layout



DIE SIZE
0.109" X 0.142"

Am2708

1024 x 8 Erasable Read Only Memory

DISTINCTIVE CHARACTERISTICS

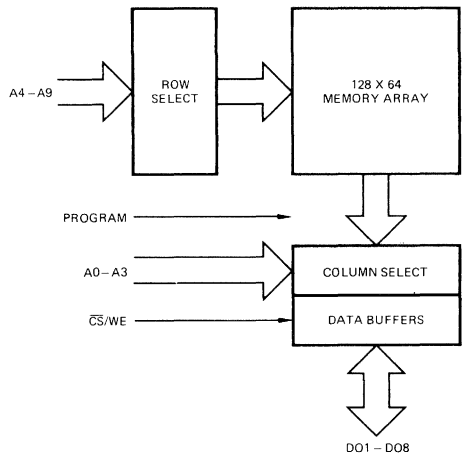
- Direct replacement for Intel 2708/8708
- Interchangeable with Am9208, Am9216 masked ROMs
- Fast programming time – typically 100 sec.
- TTL compatible interface signals
- Fully static operation – no clocks
- Fast access time – 450 ns
- Three-state outputs
- Tested for 100% programmability
- N-channel, silicon-gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

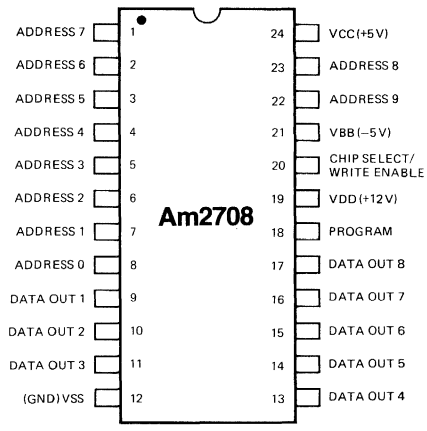
The Am2708 is an 8,192-bit erasable and programmable MOS read-only memory. It is organized as 1024 words by 8 bits per word. Erasing the data in the EROM is accomplished by projecting ultra-violet light through a transparent quartz lid for a predetermined time period.

When the Chip Select/Write Enable input is at the high logic level, the device is unselected and the data lines are in their high impedance state. The device is selected when $\overline{CS}$/WE is at the low logic level. The contents of a particular memory location, specified by the 10 address lines, will be available on the data lines after the access time has elapsed. For programming, $\overline{CS}$/WE is connected to +12V and is used in conjunction with the Program input. The Address and Data lines are TTL compatible for all operating and programming modes.

BLOCK DIAGRAM



CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time 450ns
Hermetic DIP/ Quartz Lid	$0°C \leqslant T_A \leqslant +70°C$	AM2708DC

Chapter 12
CLOCK GENERATION

The Am9080A microprocessor requires a two-phase clock signal with specific amplitude and timing relationships. The Am8224 clock generator circuit provides clock signals that meet specifications for any Am9080A microprocessor; however, in many cases it may be desirable to construct a clock circuit specifically for the application. This chapter describes the standard clock signals and methods of generating them.

The standard Am9080A clock signals, represented by the symbols Φ1, and Φ2, are defined in Figure 12-1.

The Am8224 Clock Generator is shown in Figure 12-2. It contains a crystal controlled oscillator, a clock generator circuit, and output buffers that produce the required Φ1 and Φ2 amplitudes. It also contains Reset and Ready synchronization circuits to ensure that these signals are timed correctly with the internal operating sequences of the CPU. A detailed description of the Am8224 is included elsewhere in this handbook.

When designing an alternate clock circuit, there are three areas that must be considered. These are:

- Oscillator circuit design
- Clock waveform generator design
- Clock driver circuit design

Each of these considerations is handled independently in the rest of this chapter, but all three functions must be present in order to replace the Am8224.

CLOCK GENERATORS

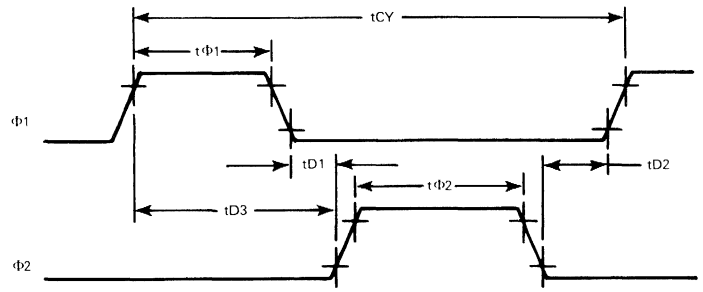
Observe that the clock period, tCY, in Figure 12-1 is the interval between the leading edges of Φ1. It can be expressed as a sum of time intervals as follows:

$$tCY = tD3 + trΦ2 + tΦ2 + tfΦ2 + tD2 + trΦ1$$

The minimum specifications for each of these timing parameters are contained in the table included with Figure 12-1. The standard Am9080A processor has a minimum clock cycle (tCY) of 480 ns. The Am9080A-4 has a minimum clock period of 250 ns. Other requirements are:

- Φ1 and the Φ2 clock pulses must not be high simultaneously.
- Both clock pulses must be low simultaneously after the trailing edge of Φ2 and prior to the next leading edge of Φ1.

CLOCK WAVEFORM DETAIL



CLOCK SWITCHING CHARACTERISTICS over operating range

		Am9080A-4		Am9080A-1 C8080A-1		Am9080A-2 C8080A-2		Am9080A C8080A		
Parameters	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
tCY	Clock Period	250	2000	320	2000	380	2000	480	2000	ns
tr, tf	Clock Transition Times	0	15	0	25	0	50	0	50	ns
tΦ1	Clock Φ1 Pulse Width	50		50		60		60		ns
tΦ2	Clock Φ2 Pulse Width	120		145		175		220		ns
tD1	Φ1 to Φ2 Offset	0		0		0		0		ns
tD2	Φ2 to Φ1 Offset	50		60		70		70		ns
tD3	Φ1 to Φ2 Delay	50		60		70		80		ns

FIGURE 12-1 Am9080A CLOCK REQUIREMENTS

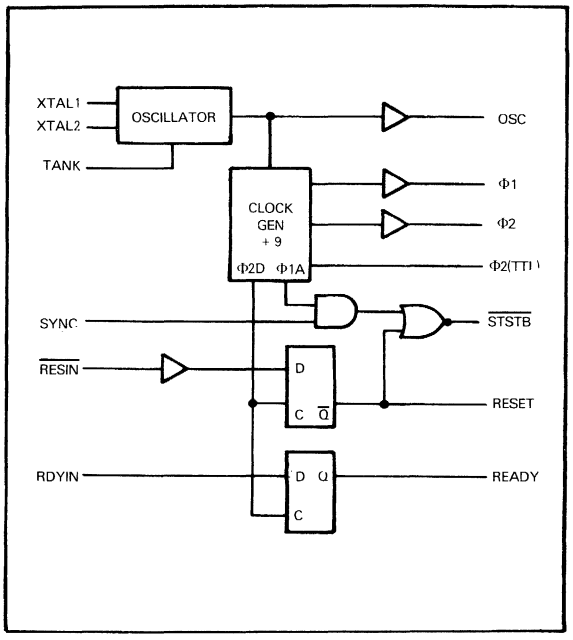


FIGURE 12-2 Am8224 CLOCK GENERATOR BLOCK DIAGRAM

Several approaches can be used to generate satisfactory waveforms. One method divides the clock period, tCY, into n equal segments. One or more consecutive segments are detected to activate Φ1, Φ2, and the delay following Φ2. One design technique uses a modulo n counter operating from an oscillator set to the frequency:

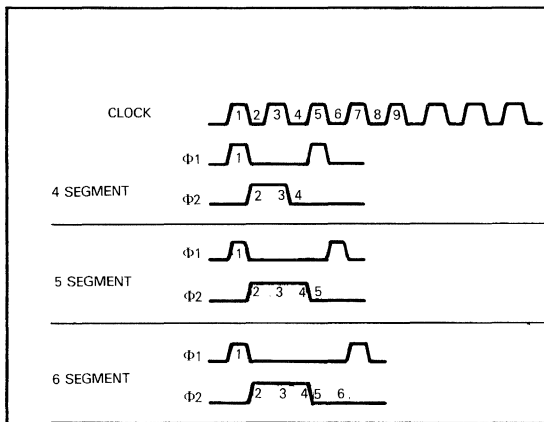
$$\frac{n}{tCY}$$

Figure 12-3 shows the timing waveforms for generating Φ1 and Φ2 using several different modulo n counter techniques.

Any of the waveforms shown in Figure 12-3 will drive an Am9080A microprocessor, but not necessarily at the minimum rated tCY. The minimum clock period attainable for each waveform is given in Figure 12-3. The four-segment clock meets minimum timing parameters of Figure 12-1 with the widest margins for each version of the Am9080A. The four-segment clock also has the advantage of requiring an oscillator frequency which is only four times the Φ1 clock frequency.

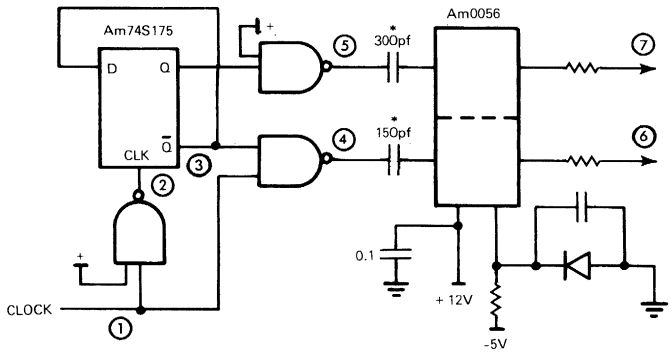
FOUR-SEGMENT CLOCKS

An inexpensive four-segment clock generator not based on a modulo four counter is shown in Figure 12-4. The amplitudes and pulse widths of the clock are determined by a pulse circuit consisting of the Am0056 level converter and input coupling capacitors. The D flip-flop connected to the inputs of the pulse circuit provides alternate phase pulses from which the



	MINIMUM CLOCK CYCLE TIMING				
	Am9080A-4	Am9080A-1	Am9080A-2	Am9080A	UNITS
4 SEGMENT	250	320	380	480	nsec
5 SEGMENT	250	320	380	480	nsec
6 SEGMENT	300	320	380	480	nsec
7 SEGMENT	280 nsec	340 nsec	410 nsec	515 nsec	nsec
8 SEGMENT	250	320	380	480	nsec

FIGURE 12-3 N SEGMENT CLOCK GENERATOR TECHNIQUES



* These values of C are for 4 MHz operation with the Am9080A-4.
Other values of C can be approximated from C = (3×10^{-3}) x required pulse width.

FIGURE 12-4 FOUR-SEGMENT CLOCK CIRCUIT TO GENERATE Φ1 Φ2 CLOCKS FOR Am9080A MICROPROCESSOR

Φ1 and Φ2 pulses are generated. The Φ1 and Φ2 clocks go to the high level when the capacitive coupled input changes from high to low. The duration of the pulse width is determined by the value of the capacitor and is approximated by the equation:

$$C = (3 \times 10^{-3}) \times \text{pulse width out}$$

The circuit in Figure 12-4 has the advantage of requiring an input oscillator frequency which is only two times the frequency of the Φ1 pulse. Therefore, the 9080A microprocessor can use an operating oscillator frequency of only 4 MHz, and the Am9080A-4 requires just 8 MHz.

Figure 12-5 shows the waveforms generated by the circuit in Figure 12-4.

Another four-segment circuit for generating Φ1 and Φ2 uses a two-stage Johnson counter as shown in Figure 12-6. The width of the Φ1 and Φ2 clock pulses are precisely determined from the crystal controlled clock frequency applied to the circuit. However, the oscillator must be four times the frequency of the Φ1 clock period.

The two series gates at the output of Φ2 insert extra propagation delay to compensate for the delay in generating phase one. This eliminates overlap in the generation of phase one and phase two.

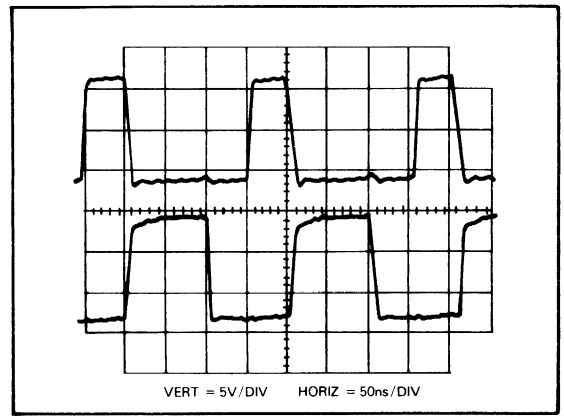


FIGURE 12-5 WAVEFORMS GENERATED BY CIRCUIT OF FIGURE 12-4

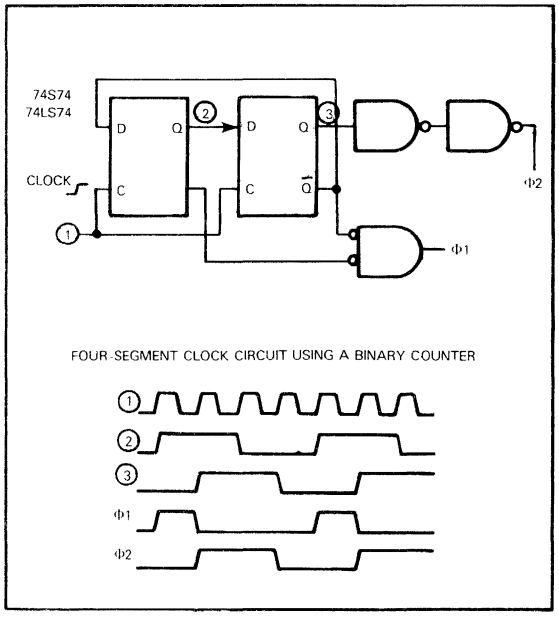


FIGURE 12-6 FOUR-SEGMENT CLOCK WAVEFORM GENERATOR

FIVE-SEGMENT CLOCKS

A five-segment clock circuit can be constructed using the divide-by-five counter shown in Figure 12-7.

Although three flip-flops are used in a divide-by-five counter, the diagram of Figure 12-7B show that when the counter is initialized in one of the unused states, (two, five, or seven) the counter progresses through the non-used states to a valid operating sequence. The count sequence of the circuit is shown in Figure 12-7C. This circuit, as in all other clock generators based on a counter, has the advantage of generating precisely controlled Φ1 and Φ2 clock pulse widths.

The input frequency from the oscillator must be $\frac{5}{tCY}$.

EIGHT-SEGMENT CLOCKS

A suggested circuit for an eight-segment clock generator is shown in Figure 12-8. This circuit is based on a four-stage Johnson counter. Although the Johnson counter uses one more flip-flop than a three-stage divide-by-eight binary counter, it has the advantage of extreme simplicity. The oscillator frequency applied must be eight times tCY. The standard Am9080A using this circuit and operating at the minimum clock period will require an oscillator operating at 16-2/3 MHz.

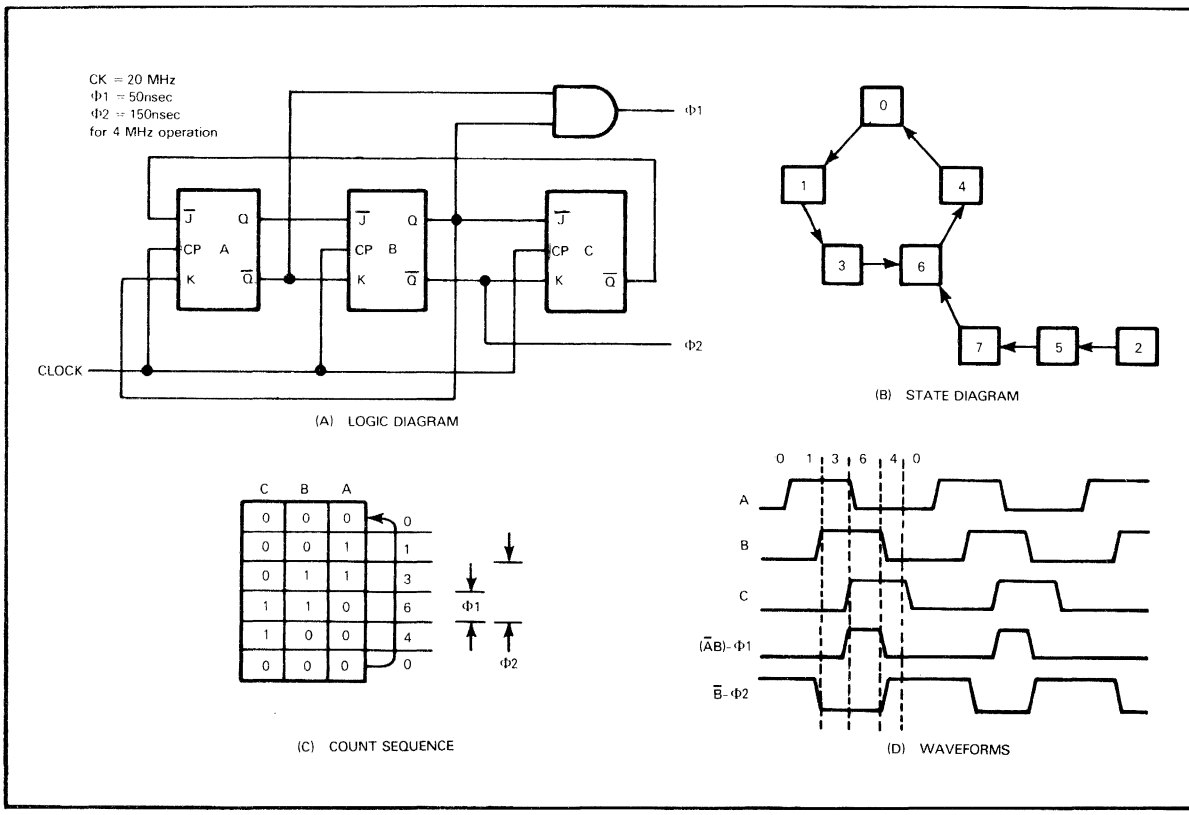


FIGURE 12-7 A FIVE-SEGMENT CLOCK

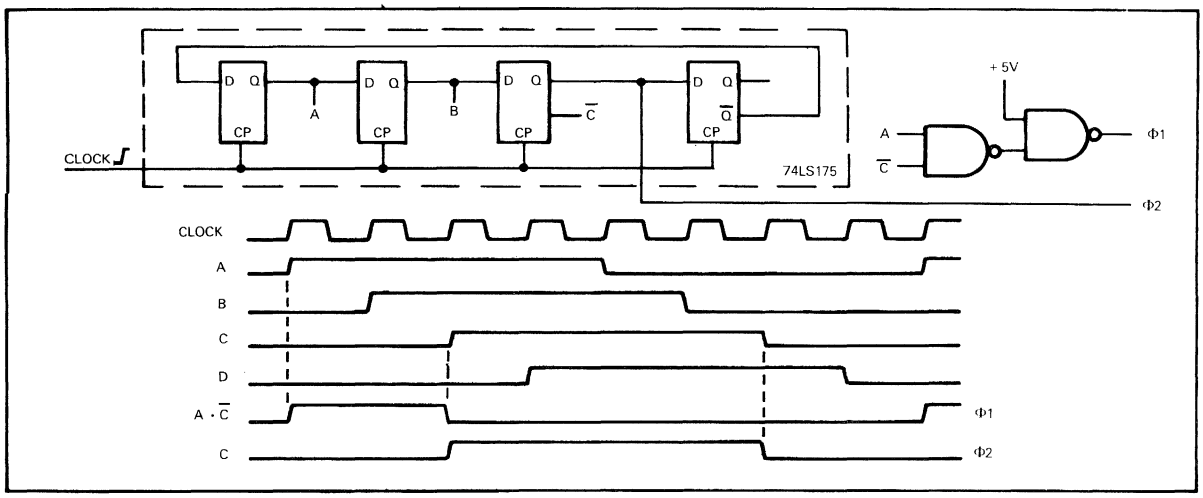


FIGURE 12-8 AN EIGHT-SEGMENT CLOCK

MONOSTABLE MULTIVIBRATOR

It is not necessary to use counters for the generation of Φ1 and Φ2 in an Am9080A microprocessor system. A clock circuit based on the Am26S02 monostable multivibrator is shown in Figure 12-9. The advantage of this circuit is that the input clock frequency needs only to be equal to the operating clock frequency of the microprocessor. The values for R1, C1, C2 and R2 are shown in Figure 12-9 for a microprocessor with a one microsecond clock period.

Figure 12-10 shows waveforms from a clock generator constructed from the circuit of Figure 12-9, after being amplified by a clock driver.

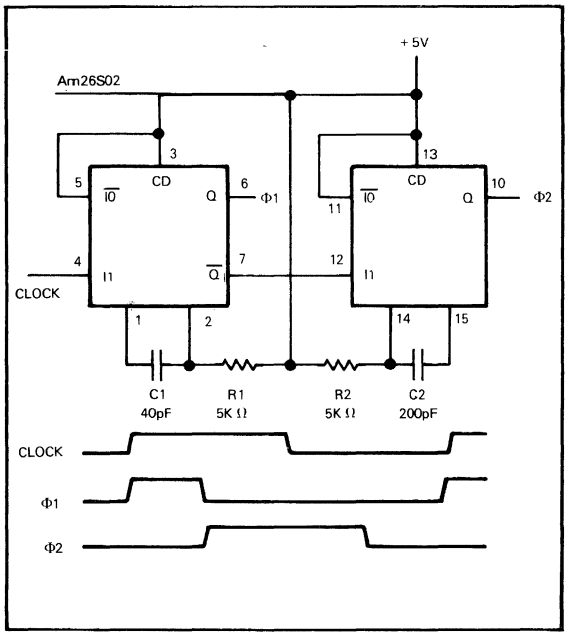


FIGURE 12-9 A MONOSTABLE MULTIVIBRATOR-BASED CLOCK

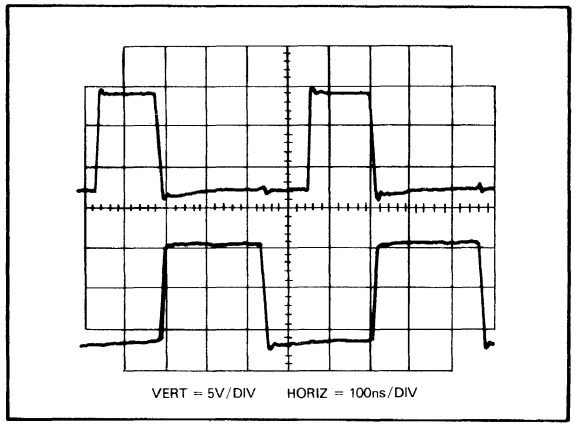


FIGURE 12-10 WAVEFORMS GENERATED BY CIRCUIT OF FIGURE 12-9

CLOCK DRIVER CIRCUITS

All of the clock circuits discussed so far except Figure 12-4 need buffer amplifiers or clock drivers to ensure appropriate logic levels and signal characteristics. The circuit of Figure 12-11, based on the Am0056, is a recommended clock driver.

Capacitors C1 and C2 couple the TTL Φ1 and Φ2 clocks generated at the inputs to the Am0056. C1 and C2 can be selected so that the pulse width is determined by the RC time constants formed with the value of the input capacitors. The pulse width is determined approximately by the equation:

$$C = (3 \times 10^{-3}) \times \text{the pulse width desired}$$

However, when this clock driver circuit is used in conjunction with one of the n segment clock generation techniques based on a counter circuit, the value of C may be set slightly larger than required to ensure that the input clock pulse controls the width of the output of the Am0056. This eliminates variations in pulse width due to changes in input capacitance over the operating temperature range.

The 47 ohm resistors shown in series with the Φ1 and Φ2 outputs of the Am0056 dampen ringing that may occur just after the leading and trailing edges of the clock pulses. Any resistor from 10 ohms to 51 ohms may be used. The resistor will affect the rise and fall times of the clock pulses as a function of series resistance and load capacitance as follows:

$$tr = tf = 2.2RSCL$$

Where:

tr = clock pulse rise time
tf = clock pulse fall time
RS = resistance in series with clock pulse output
CL = load capacitance

A low logic level of the clock pulses that is near or at 0V is established by developing a slightly negative power supply with a diode clamp circuit. This is connected to the minus voltage Am0056 input.

High frequency decoupling capacitors are incorporated on both the positive and negative supply inputs to the clock driver.

OSCILLATOR CIRCUITS

An oscillator circuit based on the Am686 high speed comparator does not require a crystal to maintain a stable operating frequency. This circuit is shown in Figure 12-12. The circuit is a relaxation oscillator providing a squarewave frequency with minimal drift and pulse position jitter over an operating range of 1 MHz to 30 MHz. Symmetry of the output waveform is better than 1% at 1 MHz and better than 5% at 25 MHz. Frequency stability is accurate to within 1% of 1 MHz and less than 4% at 25 MHz. These accuracies hold for an operating temperature range between -55°C to + 125°C. When operating the circuit over a restricted temperature range of 0°C to 70°C, the accuracies are improved by a factor of two to one over those stated above.

For the clock rates of interest here:

$$fosc = \frac{1}{2.556\ CR}$$

The oscillator output is compatible with TTL signals.

Increased accuracy of the circuit can be obtained when a crystal is used. The crystal is connected either across resistor R or from the (+) input to ground.

Since the oscillator circuit shown in Figure 12-12 is a high performance linear circuit, care should be taken when designing the printed circuit to ensure that all connections within and around the oscillator are as short as possible. The power supplies that operate the high frequency comparator should be decoupled at the circuits. A ground plane on the printed circuit board is desirable.

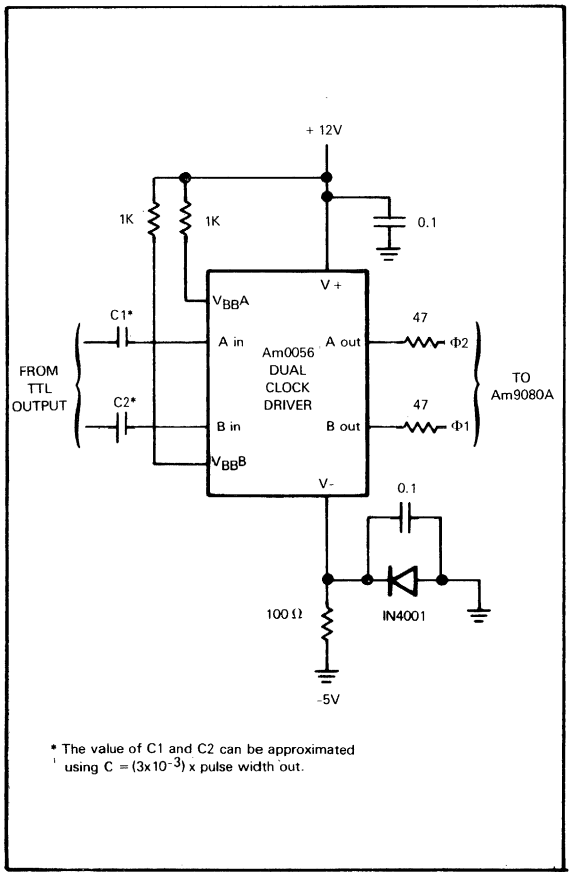


FIGURE 12-11 A CLOCK DRIVER CIRCUIT

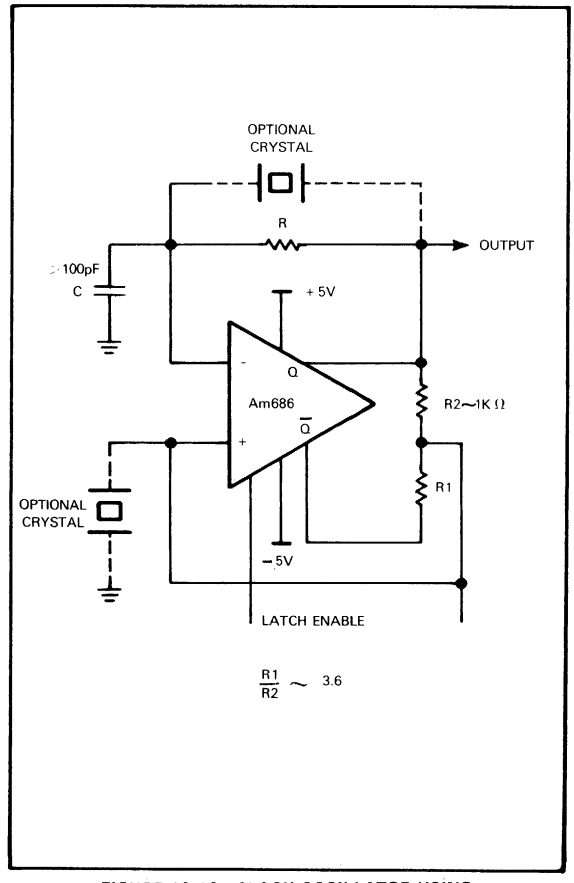


FIGURE 12-12 CLOCK OSCILLATOR USING THE Am686 HIGH SPEED COMPARATOR

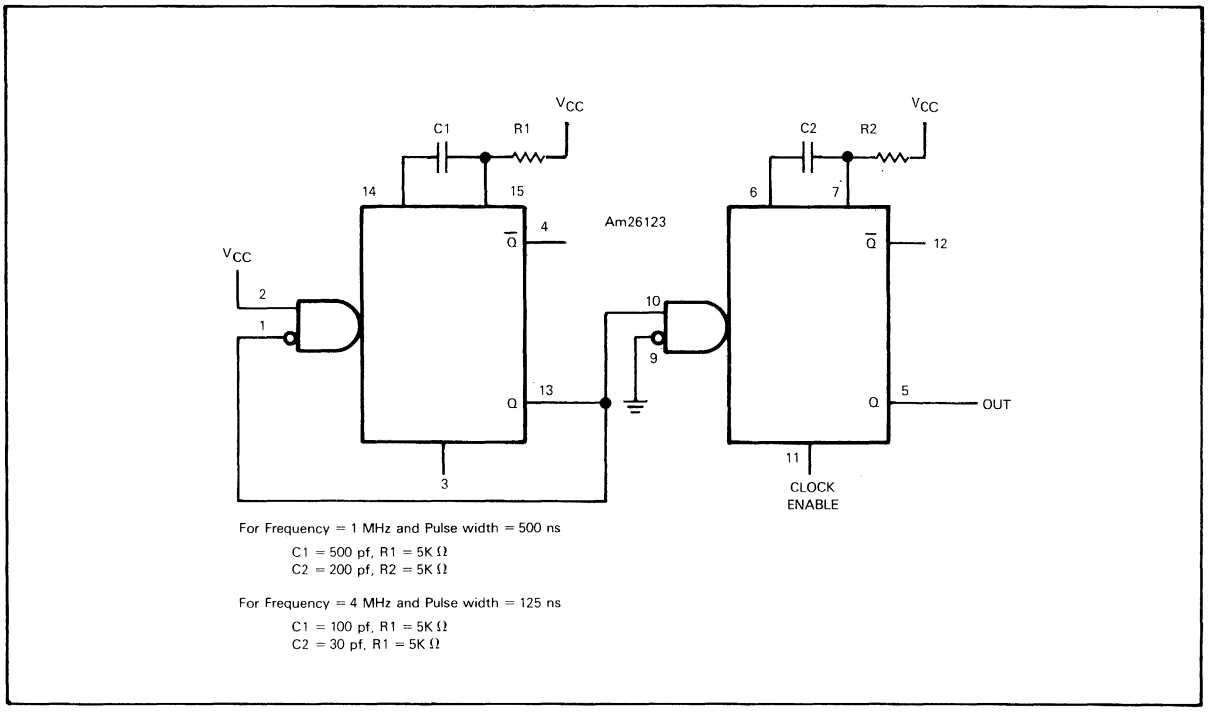


FIGURE 12-13 OSCILLATOR DESIGN USING A DUAL MONOSTABLE MULTIVIBRATOR Am26123

Another oscillator incorporates dual Am26123 multivibrators as illustrated in Figure 12-13. The frequency of the output is determined by the values of C1 and R1. C2 and R2 determine the pulse width. Accuracies in both frequency and pulse width stability can be achieved to better than $\pm 1°$ within the operating temperature range of 0°C to 70°C.

Output waveforms for the circuit are shown in Figure 12-14.

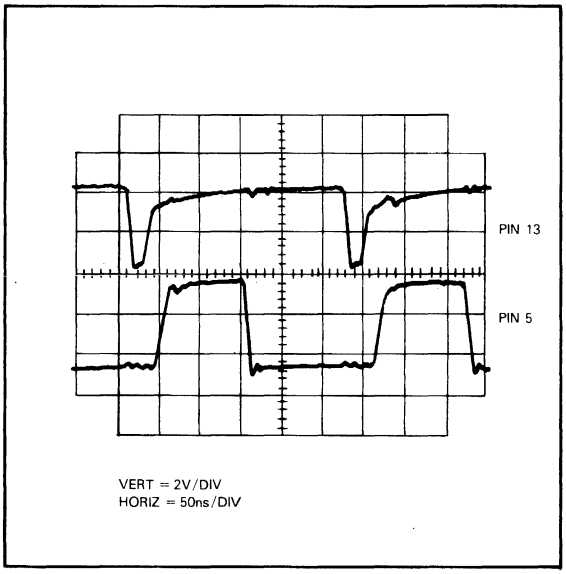


FIGURE 12-14 WAVEFORMS GENERATED BY CIRCUIT OF FIGURE 12-13

Figure 12-15 shows an oscillator which is designed with the Am555 precision timer circuit. The duty cycle for this circuit is determined as follows:

$$D = \frac{RB}{RA + 2\,RB}$$

The frequency in Hz for the output is given by:

$$F = \frac{1}{0.693\,(RA + 2RB)\,C}$$

When RA = RB the oscillator circuit has a duty cycle of 0.25.

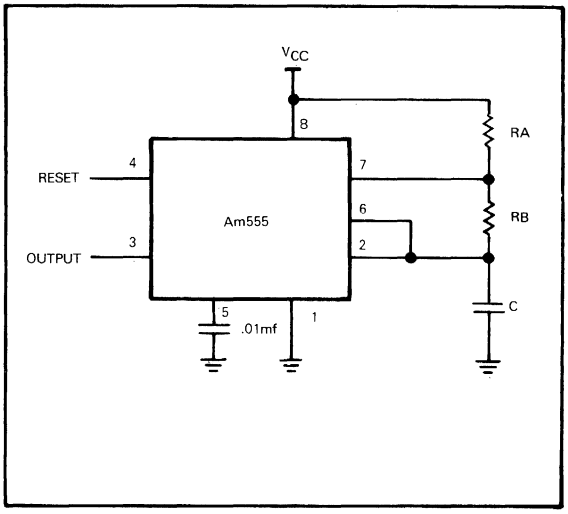


FIGURE 12-15 OSCILLATOR DESIGN USING THE Am555 TIMER

Chapter 13
MEMORY SYSTEM DESIGN

Memories are a major subsection of the hardware in every microcomputer system. The typical system uses memory for storage of both programs and data. In the typical application it is usual to use both RAM and ROM components in the design of the memory. The variety of memory components available gives the microprocessor designer a wide latitude in configuring his memory systems to best meet his requirements.

RAM memory components are available in both static and dynamic organizations. However, the ease of use of static RAMs have made these devices popular for microcomputer applications. Static RAMs are also much more economical in the capacities normally found with microcomputers.

Many of the techniques and considerations for organizing static RAM configurations in this chapter apply to all types of random access memories, including semiconductor ROMs, EROMs, and dynamic RAMs.

Figure 13-1 shows the general organization of memory constructed with static RAM and/or ROM. The CPU supplies 16 address lines to the memory to be used to access a specific 8-bit memory location during a memory access cycle. Any one of 65,536 locations can be uniquely accessed. An 8-bit Data Bus is provided for the transfer of information between the CPU and memory.

Two signals, $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$, cause the memory to perform active cycles, and control the direction in which data is to be transmitted between the CPU and the memory.

CHIP SELECT DECODING

The number of chip selects that must be provided is a function of the total memory required and the number of addressable locations in the memory devices. For example, if a RAM memory is to be provided with 16K bytes and the memory components to be used are organized as 1K x 1 (e.g., the Am9102 RAM), a total of 128 devices will be required, organized in 16 groups of eight. Each group of eight devices will be connected in parallel thus forming the 8-bit wide memory byte. For convenience we will refer to this group as a memory page.

Sixteen similar groups, each with its own chip select signal, are required to form the memory.

One hundred and twenty eight devices will still be required if the Am9111 (organized as 256 x 4) is used instead of the 1K x 1 devices; however, the memory will be designed as 64 groups of two devices. Thus 64 chip select signals will be required with a correspondingly greater amount of logic.

The 16 bits of the Address Bus are divided into two groups of signals. The low order bits of the bus are applied directly to the memory chips as address inputs, while the high order bits are applied to the chip select logic. How many bits are assigned to each group is a function of the number of addressable locations contained in the memory devices used. Thus, the Am9102 mentioned earlier has 1024 addressable locations and therefore requires that the ten least significant

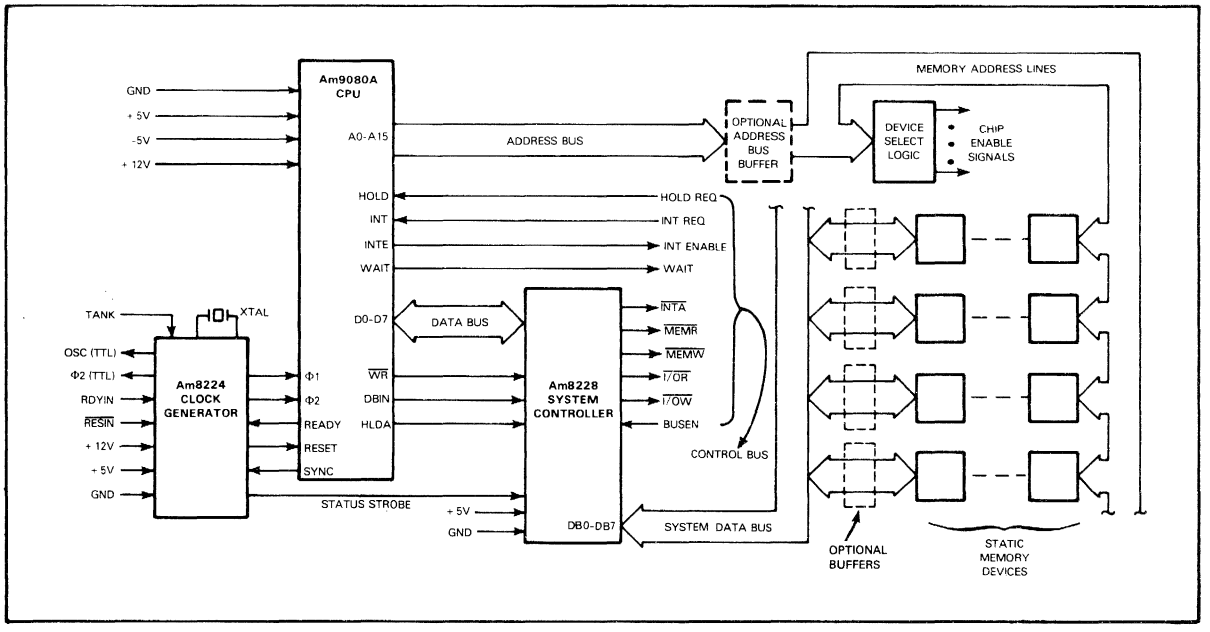


FIGURE 13-1 AN Am9080A STATIC MEMORY GENERAL CONFIGURATION

bits of the CPU Address Bus be applied to all 128 memory devices in parallel. Four of the most significant six bits of the Address Bus are applied to the chip select logic to generate the 16 chip select signals. In the case of the Am9111, only eight of the least significant bits are applied to all devices (2^8=256). However, since a 16K byte memory requires 64 chip select signals, six of the most significant eight bits of the Address Bus are applied to the chip select logic. In both cases 14 of the address bits are required.

ADDRESS BUFFERS

Additional Address Bus buffers may be necessary to provide the required drive. The need for buffers depends on the total number of memory components used and the system operation speed. Memory system timing is considered in Chapter 14.

Tables 13-1 and 13-2 show the input and output capacitance and current specifications for a selection of memory devices that may be used in the design of a memory.

TABLE 13-1 STATIC RAM CAPACITANCE SPECIFICATIONS

	Am9101	Am9111	Am9112	Am9130	Am9102	Am9140
	256x4	256x4	256x4	1Kx4	1Kx1	4Kx1
Address Inputs	6 pf	6 pf	6 pf	6 pf	5 pf	6 pf
Data Input	6 pf	---	---	---	5 pf	6 pf
Data Output	9 pf	---	---	---	6 pf	9 pf
Data I/O	---	11 pf	11pf	9 pf	---	---

Since all memory devices are connected to the Address Bus, the input current (I_{LI}) must be summed for all memory devices and compared with the specific source current for the Am9080A. The critical load is usually determined by the ability of the Am9080A to supply source current at the rated V_{IH} of the memories.

When the microcomputer is to be operated near its maximum operating frequency for the system design, the read and write cycle times become critical. Then the capacitive load on the Address Bus must also be considered. The capacitive loads of the address inputs of all memories must be calculated and compared with the rated capacitive load that can be driven by the Address Bus at the required "Address Output Delay From Φ2" (tDA) of the Am9080A. This specification is rated at a capacitive load of 100 pf. However, larger capacitive loads can be driven by the Address Bus if an increase in the tDA specification can be tolerated.

Tables 13-1 and 13-2 show the current and capacitance ratings of RAM memory products. Typical microprocessor systems may use a combination of other memory products, however.

DATA BUFFERS

Extra Data Bus buffers may be required in addition to those contained in the Am8228 as shown in Figure 13-1.

Since the CPU Data Bus is bidirectional, the Data Inputs and Data Outputs of the memories must be connected. In order to prevent bus conflict, many memories with separate Inputs and Outputs have an Output Disable signal provided which causes output to be active only when this signal is active. Otherwise the outputs are in the high impedance state. Normally this signal will be connected to the $\overline{MEMR}$ signal from the Am8228 so that the outputs will only drive the Data Bus during a read cycle.

The Am9102 does not have the output disable function. Therefore, when designing with this part, separate Data Bus buffers should be provided on the Data Output with a 3-state control input to function as the output disable.

During a memory read cycle, the actively addressed memories must drive not only the load presented by the Data Bus or the Data Bus buffers, but also must supply the leakage current to all non-active memory circuits connected to the corresponding bits. If the memories used have separate Data In and Data Out, the leakage current for both must be supplied by the driving memory. When using N-MOS memories, it is generally the ability of the memory to supply source current to all other memories at the V_{OH} level that determines how large the memory system can be without the additional Data Bus buffer. When large memories are required, the memory system should be partitioned into blocks with separate Data Bus buffers assigned to each block.

When designing memory systems for microcomputers that are operating at or near the limits of their read or write cycle time, the capacitive load presented by the Data Inputs and Data Outputs must also be considered. The data access time of the memory is typically specified at 50 or 100 pf of total load. However, RAM memories with separate Data Inputs and

TABLE 13-2 STATIC RAM INTERFACE CURRENT SPECIFICATIONS

PARAMETER	DESCRIPTION	TEST CONDITION	Am9130	Am9140	Am9101	Am9102	Am9111	Am9112	UNITS
I_{OH}	Output source current (min)	$V_{OH} \geq 2.4V$	-200	-200	-200	-200	-200	-200	μA
I_{OL}	Output sink current (min)	$V_{IL} \leq 0.4V$	3.2	3.2	3.2	3.2	3.2	3.2	mA
I_{LI}	Input load current (min)	$0V \leq V_{IN} \leq 5.25V$	10	10	10	10	10	10	μA
I_{LO}	Output leakage current	$V_{OUT} = V_{CC}$			5	5	5	5	μA
		$V_{OUT} = 0.4V$			-10	-10	-10	-10	μA
I_{LO}	Output leakage current	$V_{SS} \leq V_{OUT} \leq V_{CC}$	10	10					μA

All specifications have been rearranged to show the available current as a function of the rated output voltage. The data sheet guarantees the voltage parameter at a specified current.

Data Outputs connected together to the Data Bus can present 15 pf or 20 pf for each circuit connected to a common bit of the Data Bus. Then the number of memories connected to the Data Bus may be restricted and additional buffers incorporated to break up and isolate capacitive loads.

Generally, when system access time is critical, capacitive load considerations rather than static load will dictate the size of the memory block that can be constructed before additional buffers are required.

The foregoing discussion is of necessity rather general. The wide selection of different memory types and organizations, each with dissimilar specifications, make rules-of-thumb about when to use separate Address and Data Bus buffers impossible. Each application must be configured to meet the specific objectives of that system, and the component specifications for the parts used consulted.

CHIP SELECTION CONSIDERATIONS

Microcomputers with large memory systems, or in which a memory section must be generalized to operate anywhere in the memory map, are best designed to use all 16 address bits for memory address signals and chip selection. Decoder circuits, such as the Am25LS138 and Am25LS139, are an efficient way to decode the chip selects. These circuits present a minimum load to the Address Bus and generate several chip select signals with a minimum number of logic packages.

Other systems in which the total amount of memory to be used is a small portion of the 64K addressable memory space of the Am9080A, and in which the memory is preassigned to fixed address locations within the memory map can use less than the full 16 lines for address and chip select decoding. The advantages are that fewer interconnections need to be made between the CPU and the memory modules. However, the designer must be careful that no two assigned memory sections will respond simultaneously to any valid address which may be generated by the program.

The Am9080A obtains the first instruction from address location 0000 after reset is applied to the circuit. Thus, the first instruction of the program must be located in page 0. There are no constraints on where the remaining ROM and RAM may be placed in the memory map, and locations should be selected for the convenience of both the hardware and program design. Memory device select logic is discussed elsewhere in this handbook.

SOME MEMORY CONFIGURATIONS

Figure 13-2 shows a 256 x 8 memory constructed with Am9111 static RAM devices. Each circuit contains 1K bits of storage organized as 256 x 4. Two circuits thus provide the required 256 x 8-bit storage. No Address or Data Bus buffers are provided since the small memory will not impose a load condition beyond the capabilities of the system. Address bits A0 through A7 are connected directly to the address inputs of both memory circuits. Address A15 is inverted and applied to $\overline{CE2}$ of both memories. $\overline{CE1}$ is not needed in a small memory system for chip select decoding and is therefore permanently enabled by connecting it to ground. $\overline{MEMR}$ connected to Output Disable ($\overline{OD}$) causes the output drivers in the Data Bus to become active only when a Memory Read function is requested by the CPU. At all other times the output drivers are in the high impedance state.

The memory map in Figure 13-2 shows the address assignments for the RAM, as configured. Address bit A15 causes the RAM to respond to all memory locations from address 8000_{16} through $80FF_{16}$. Since none of the high order address bits other than A15 are used in the chip enable generation, redundant addresses above $80FF_{16}$ will also cause the RAM to respond. Consequently, ROM, which may also be mapped in the memory space, cannot use addresses above 8000_{16} in this configuration.

Three different configurations for a 1K x 8-bit memory system are given in Figures 13-3, 13-4A and 13-5. Figure 13-3 uses

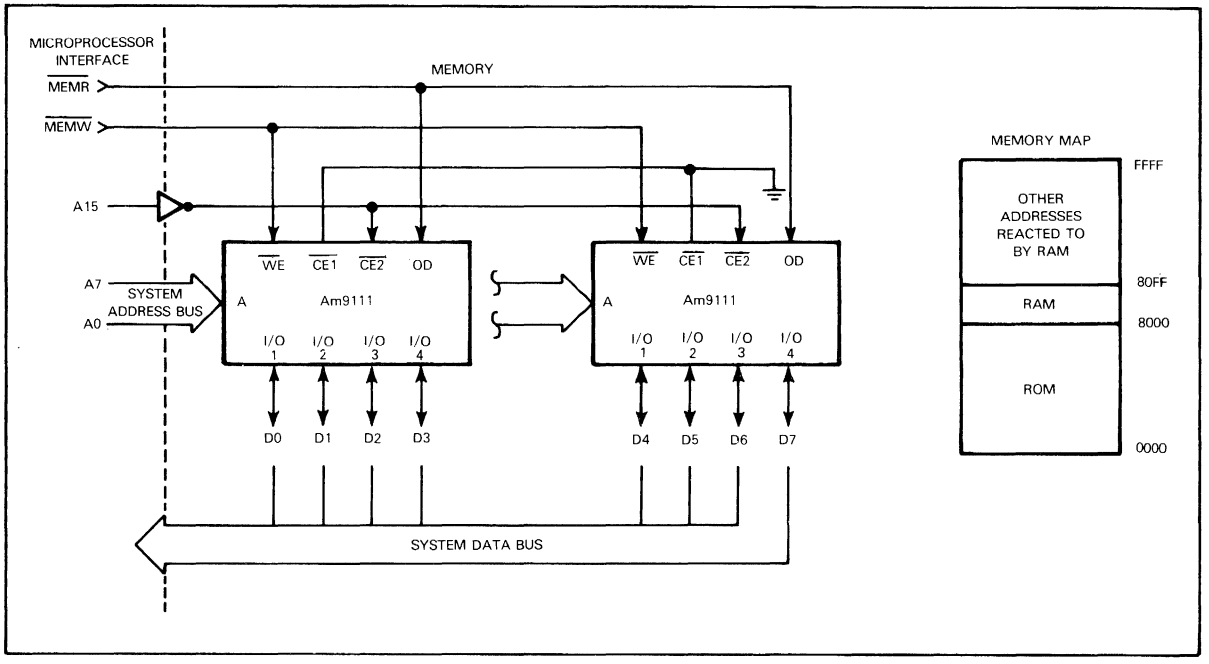


FIGURE 13-2 Am9111 DEVICES USED TO CREATE A 256 x 8-BIT STATIC RAM MEMORY

the Am9102 to form the 1K by 8-bit memory. Note that the Am9102 has separate data inputs and data outputs. Since no output disable control signal is available in the Am9102, a unidirectional output data buffer such as the Am25LS241 should be connected between the data outputs from the RAM circuits and the bidirectional system Data Bus. The buffer is controlled by the $\overline{\text{MEMR}}$ signal. When active, this signal allows memory data outputs to drive the bidirectional Data Bus. Address lines A0 through A9 from the system Address Bus are applied to the address inputs of all eight Am9102 memories. Address A15 is inverted and supplied to the chip enable inputs, causing the RAM to respond to primary addresses 8000_{16} through $83FF_{16}$.

Figure 13-4A is an alternate construction for the 1K byte RAM memory using the Am9111 memories. There are two differences between this circuit and that of Figure 13-3.

First, four chip select signals must be generated from the Address Bus to activate one of the four 256 byte groups that make up the memory. Second, since there are four devices connected to each bit, the Data Bus signals have more capacitive load than in the example of Figure 13-3. Consequently, in systems where memory access timing is critical, less margin is available when using the Am9111 than with the Am9102. Notice in Table 13-1 that the input/output capacity of the Am9111 is 11 pf. Thus, the circuit of Figure 13-4A provides 44 pf of load capacity plus the additional distributed load capacitance of the interconnections to the Data Bus. However, the Am9102 of Figure 13-3 imposes only 5 pf of load capacity on each one of the Data Bus signals. As a consequence, much larger memories can be constructed with the Am9102 before the capacitive drive capability of the driving memory is exceeded. The circuit of Figure 13-4A could be expanded to a practical limit of approximately 2K bytes of memory before additional bidirectional bus buffers would be required to isolate the increased capacitive load from the memory components. If larger memory systems are constructed with the Am9111, memory should be divided into blocks of 2K bytes each, with each block isolated through a separate set of bidirectional system Data Bus buffers.

The memory map of Figure 13-4B shows the same 1K address assignment as Figure 13-3; however, the memory is subdivided into four equal pages of 256 bytes each.

A third configuration of the 1K x 8-bit memory is shown in Figure 13-5. This circuit uses the Am9130, 4K-bit memories.

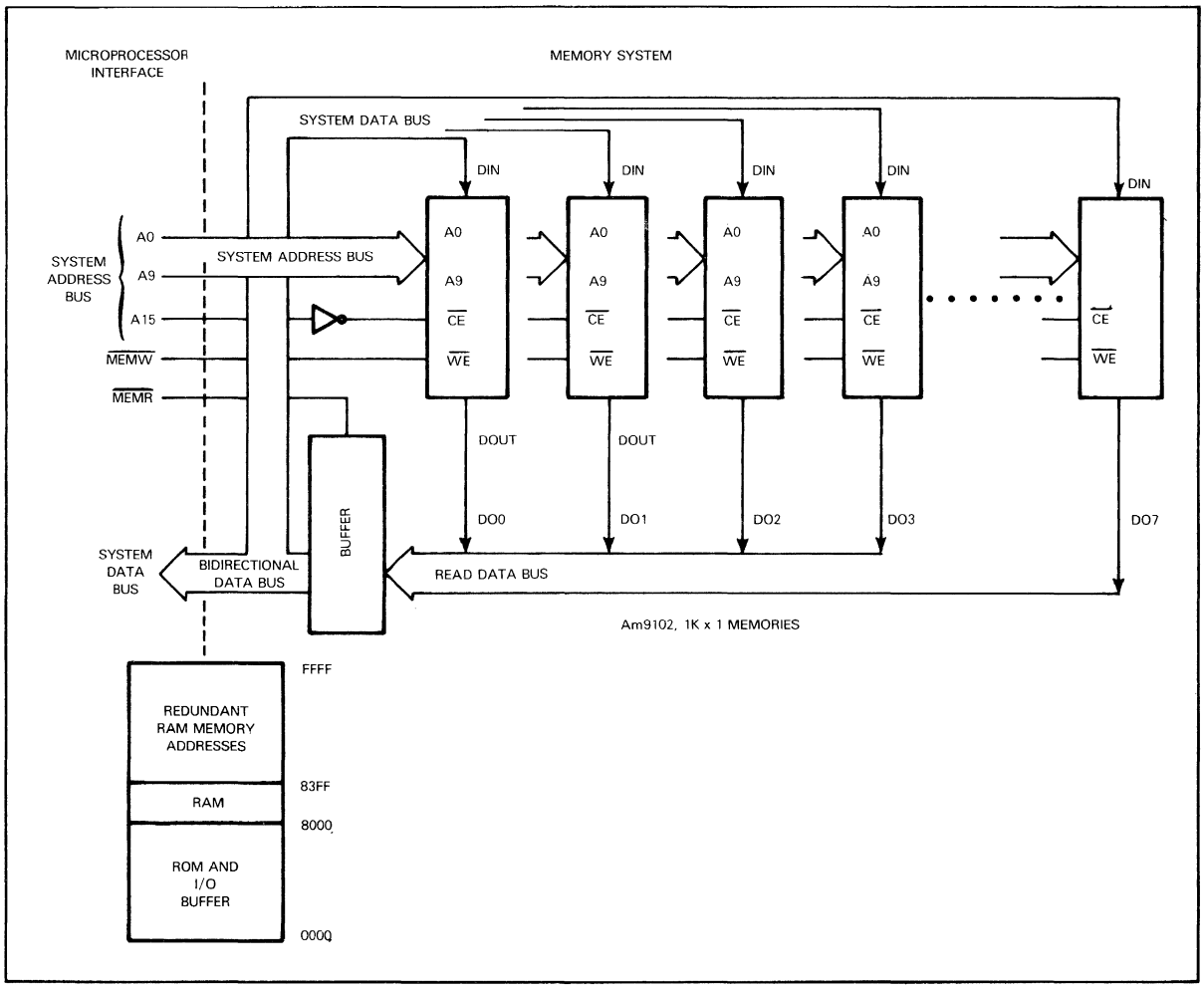


FIGURE 13-3 A 1K BYTE STATIC RAM USING Am9102 1K x 1-BIT MEMORY DEVICES

Because of the small number of chips connected to the Data Bus, no bidirectional bus buffers are included in the circuit diagram. Address lines A0 through A9 are applied directly to the address inputs of the Am9130. Address A15 is inverted and applied as the chip select so that this memory responds to the same addresses as the memories of Figure 13-4 and 13-3. The output disable signal is connected to $\overline{MEMR}$, causing the I/O pins to drive the Data Bus only during memory read functions. An output enable signal is not needed in the small memory configuration shown and is permanently activated with +5 volts.

The Am9130 requires address and chip select signals to be active at the input before the Chip Enable signal switches from low to a high logic level. The Chip Enable causes the address and the chip select inputs to be latched internally. $\overline{MEMR}$ and $\overline{MEMW}$ are "ORed" together and applied to the Chip Enable to generate this function.

The Am9140 4K static memory, organized as 4K x 1-bits, may be preferred in static memory systems where 4K bytes or more are required. An 8K byte static memory using the Am9140 is shown in Figure 13-6A. The Am9140 memories require 12 address bits to select the desired location. Address

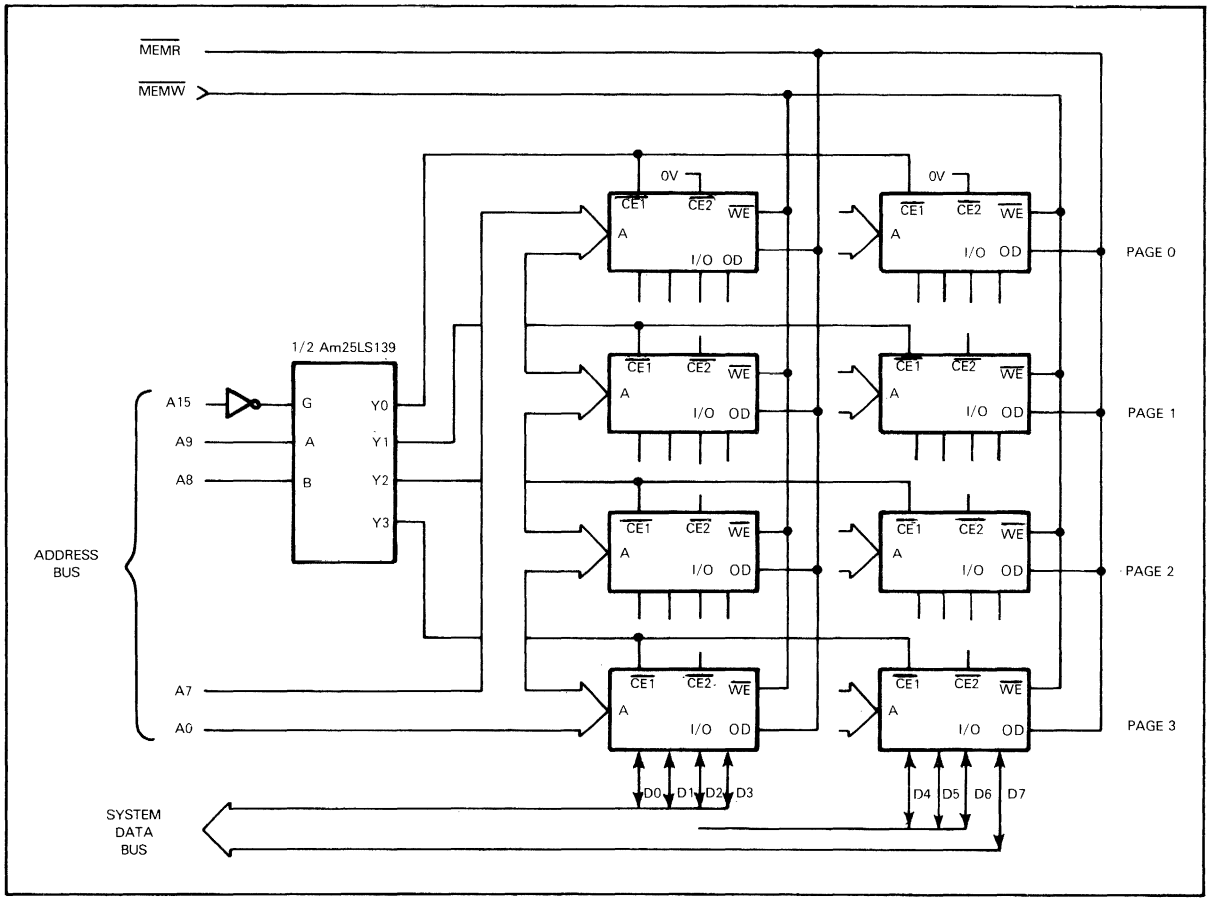


FIGURE 13-4A 1K x 8 RAM MEMORY CONSTRUCTED WITH Am9111 MEMORIES

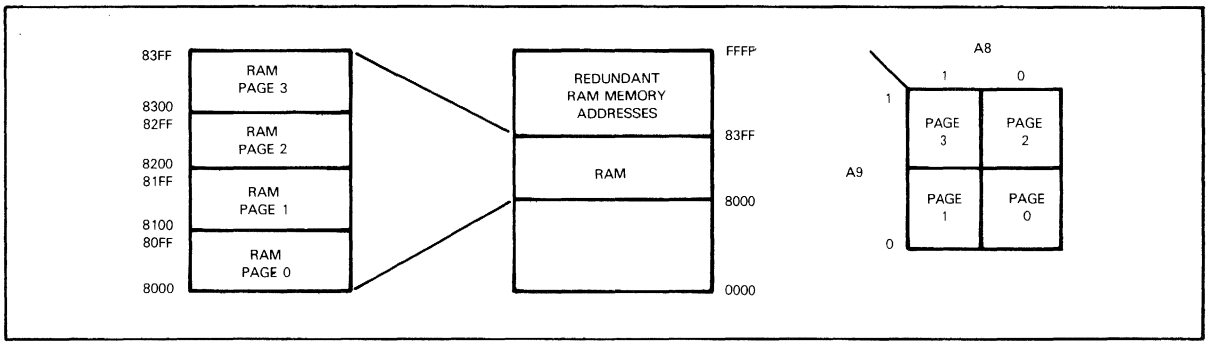


FIGURE 13-4B MEMORY MAP FOR FIGURE 13-4A

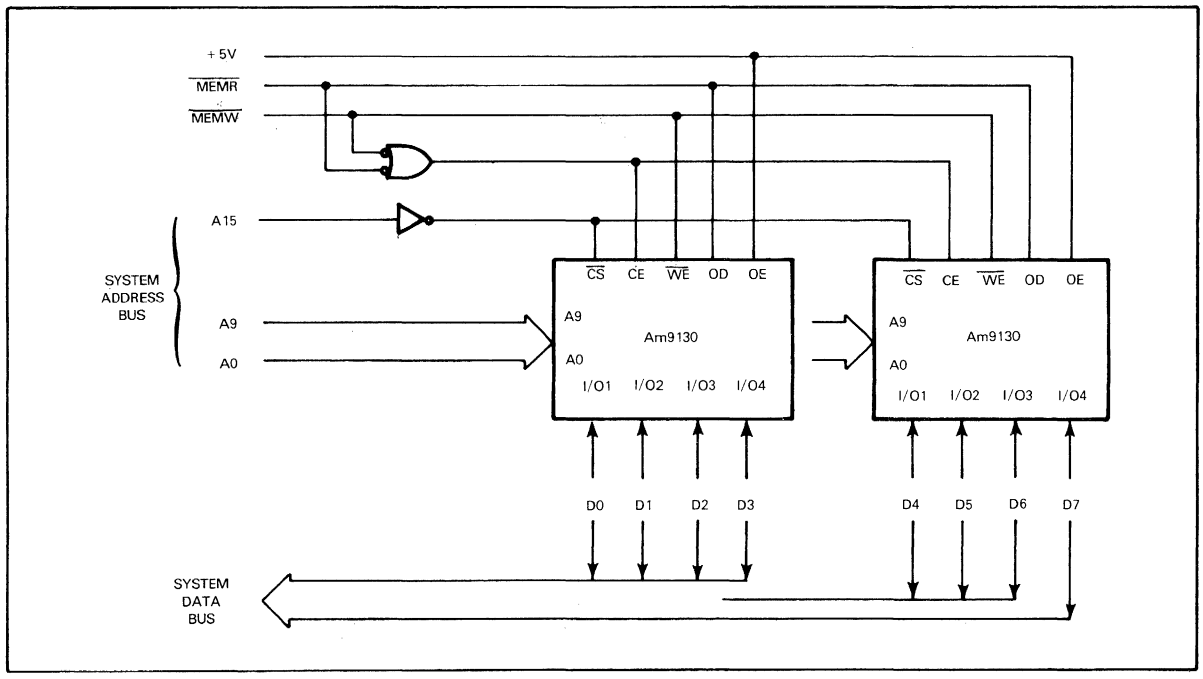


FIGURE 13-5 A 1K X 8-BIT STATIC RAM USING Am9130 MEMORY DEVICES

bits A12 and A15 from the system Address Bus are used in generating the chip select signals to the two pages of memory. A15 has been arbitrarily selected to ensure that the RAM will respond only to addresses at location 8000_{16} or greater. Notice that Figure 13-6A does not use bidirectional Data Bus buffers to isolate the memory from the system Data Bus, nor are Address Bus buffers required between the CPU and memory.

If the memory is to be expanded beyond 8K bytes, the following consideration must be observed.

The data inputs of each data line in memory are connected together as are the outputs. Thus the input/output load capacity presented to the Data Bus is 21 pf. However, the Am9140 has a rated maximum access time with a capacitive load of 50 pf.

A memory circuit that is accessed must drive the load capacity of additional nonactive memories that are connected to the Data Bus as well as the distributed capacity of the interconnections and input capacity of other circuits connected to the Data Bus. Therefore, practical considerations may make it desirable to divide the memory into blocks of 12K bytes each with separate Data Bus buffers.

Address assignments for the memory are shown in Figure 13-6B. The memory map shows that page 0 consists of address 8000_{16} through $8FFF_{16}$. Page 1 responds to all addresses between 9000_{16} and $9FFF_{16}$. Both page 0 and page 1 respond to several additional groups of addresses above 8000_{16}.

A 16K-byte memory using the 4K Am9140 memory is shown in Figure 13-7A. The system Address and Data Busses are fully buffered to isolate the loads. Transmission line impedances on the System Busses can be expected to be different from those on a printed circuit module that might contain the 16K memory section. The buffers serve to interface between the two different impedances, thereby reducing both the loading and noise on the System Busses. Address selection is accomplished with most significant bits, A15 and A14. This allows the independent selection of any of the four 16K memory sections that can be addressed within 65,536 bytes of memory space.

The bidirectional system Data Bus is split into unidirectional Write and Read Data Busses. Isolating these two sets of signals splits the capacitive load that is connected to each of the two busses. The capacitive load presented by the data output connections from the Am9140s limits the number of 4K pages that may be included in a RAM memory section. Each data output presents 9 pf of capacity, as shown in Table 13-1. An active memory page within a memory section must drive the I/O capacity of the three circuits which are in the high impedance state plus the interconnection capacity of the printed circuit module plus the input capacitance of the buffer.

Thus, a practical limit on the size of a memory section constructed with the Am9140 is 16K total bytes with individual Data Bus buffers and address buffers. When more than 16K bytes of memory are required in a system, two similar modules, each with 16K bytes, may be connected to the system Address and Data Busses in parallel. The appropriate address connections are made on the module to ensure that each memory section responds to a unique set of memory addresses. Addresses are fully decoded in this configuration and no redundant memory addresses are detected by the memory pages.

When designing memory systems that operate at or near the minimum memory access time possible, the choice of the type

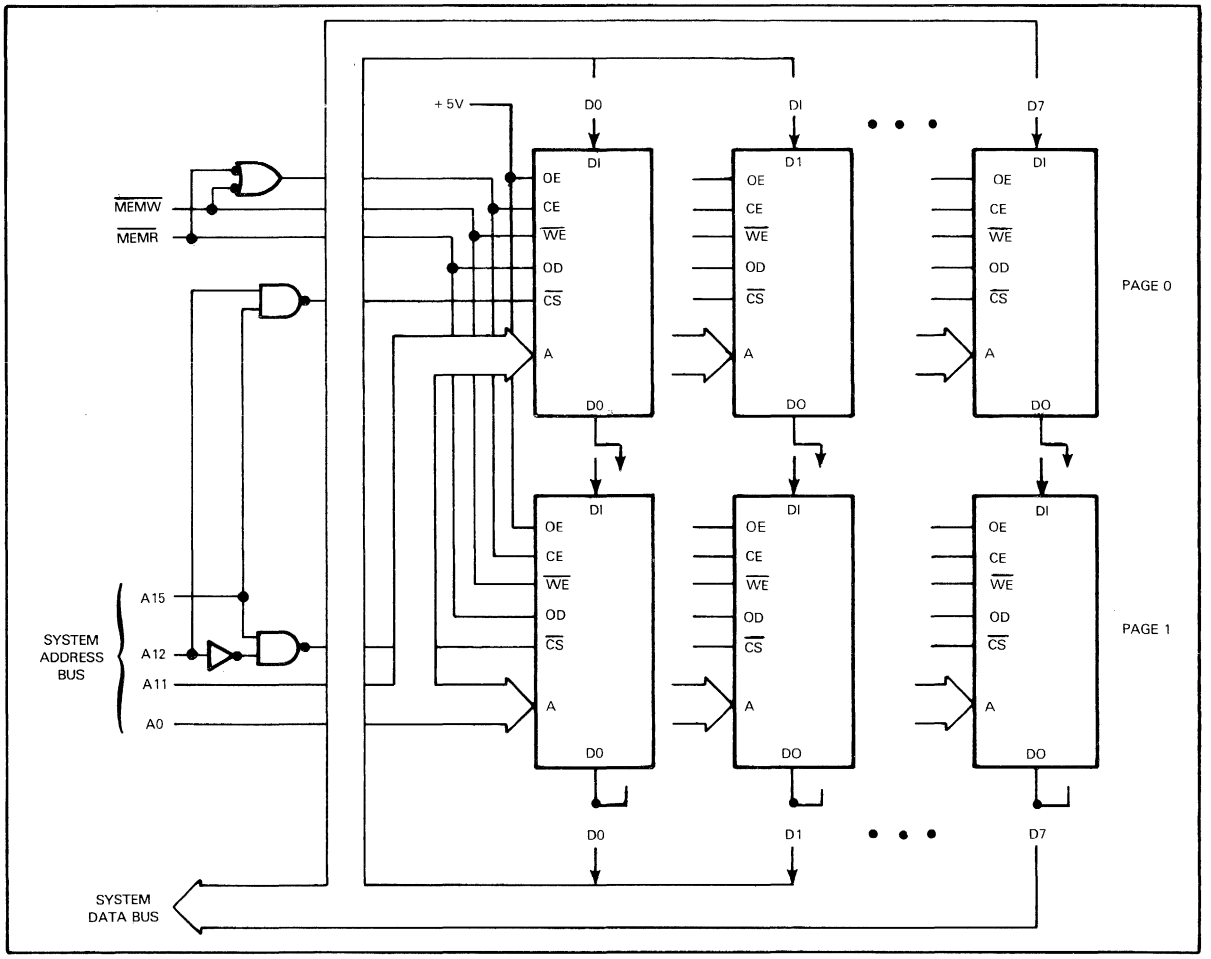


FIGURE 13-6A AN 8K x 8-BIT STATIC RAM USING Am9140 MEMORY DEVICES

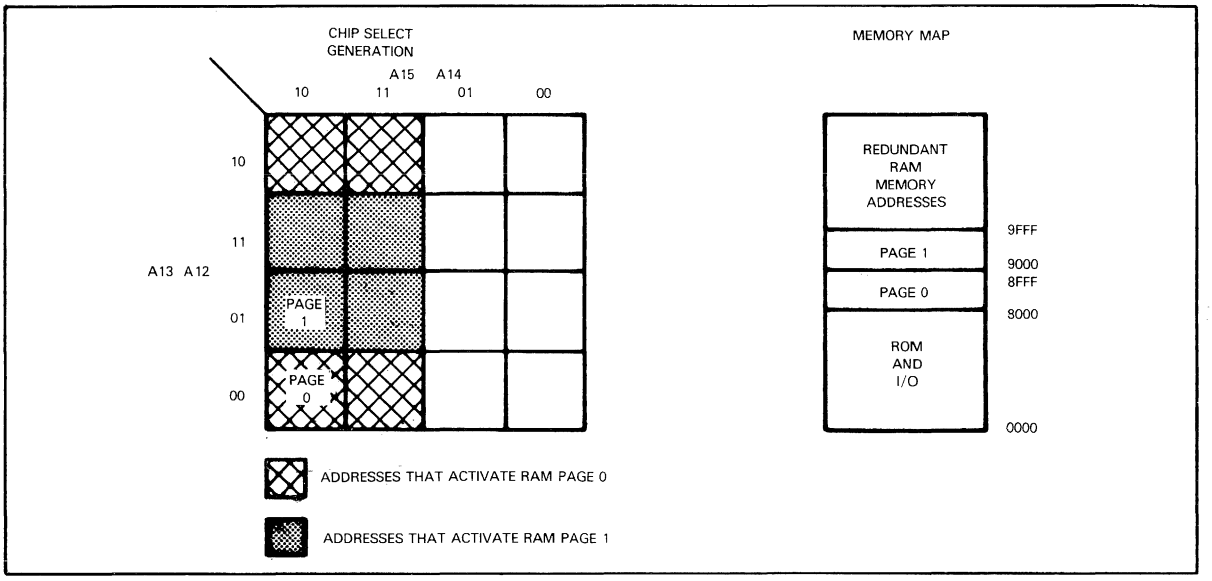


FIGURE 13-6B ADDRESS ASSIGNMENTS FOR THE MEMORY OF FIGURE 13-6A

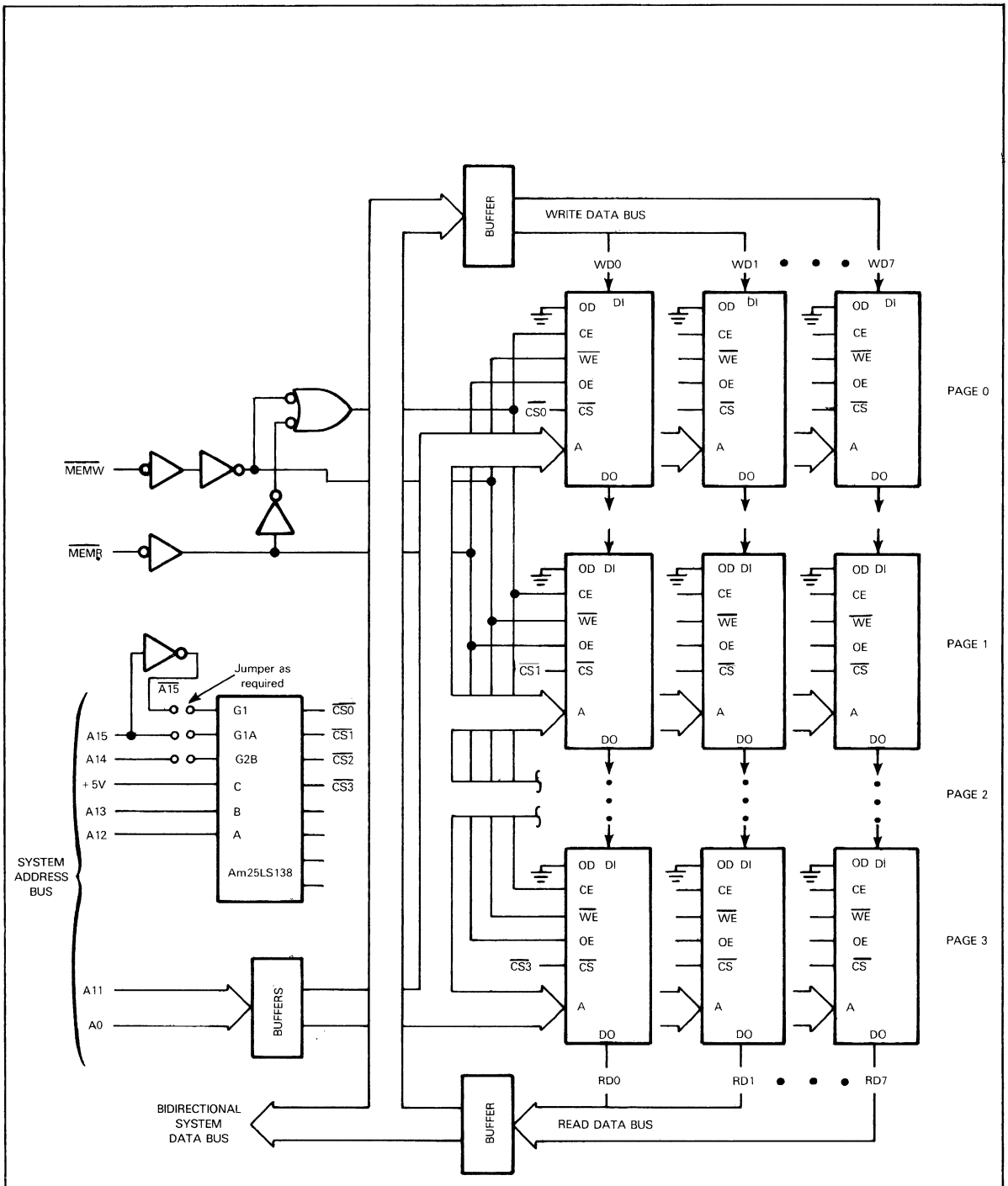


FIGURE 13-7A A 16K x 8-BIT MEMORY USING Am9140 MEMORY DEVICES

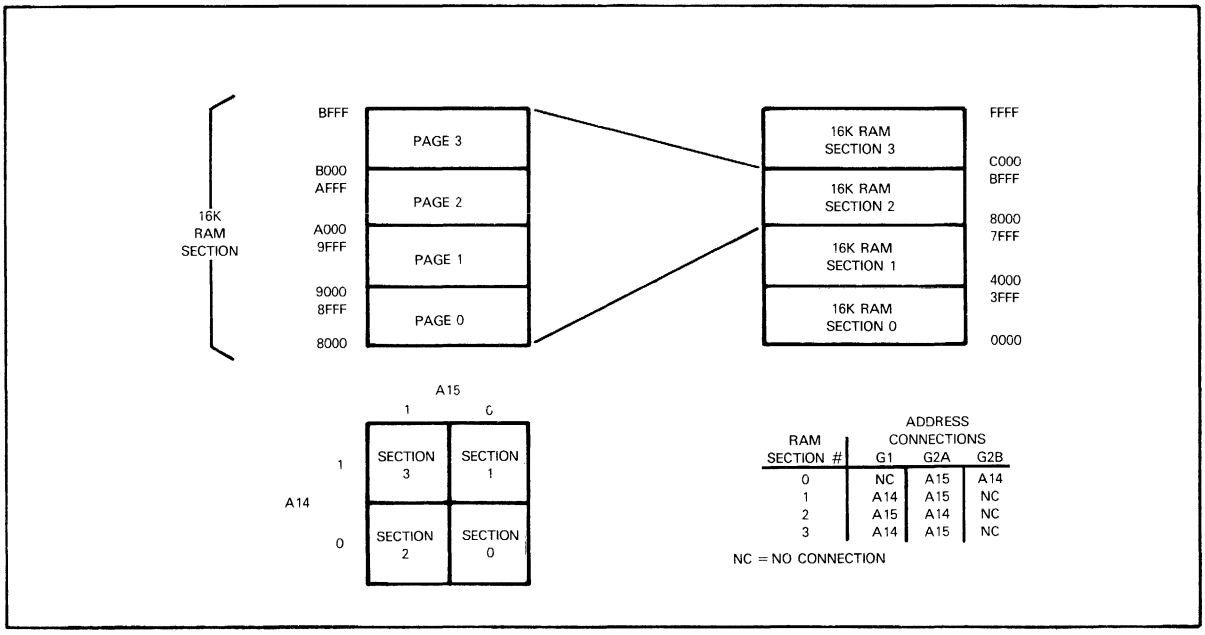


FIGURE 13-7B MEMORY MAP FOR FIGURE 13-7A

of memories to be used, and the size of the memory section that can be constructed before appropriate Address and Data Bus buffers are included, is dominated by the capacitive loads that are imposed by other memory circuits connected to the data inputs and outputs.

The need for extra Address and Data Bus buffers in microcomputers with ample read and write access times will usually be determined by the D.C. load conditions presented to these two busses. Generally, the load imposed on source current capability of a memory when its output is at V_{OH} is the limiting factor.

Failure to design for the maximum load conditions, both A.C. and D.C. of the operating conditions of the microcomputer, may cause the incidence of soft failure (error in reading or writing) to increase at the limits of the environmental operating conditions. Because of the random nature and infrequency of such errors, the problem is difficult to isolate. The difficulty lies not with the incompatibility of the devices used in the construction of the microcomputer; but, with the inadequacy of the design.

Chapter 14
PROCESSOR/MEMORY TIMING

There are many memory products that can be used with the Am9080A microprocessor. In addition to different forms of memory organization, each type of memory is available in versions with different guaranteed access times. To ensure operation of the microcomputer over the full range of environmental conditions, it is necessary that the appropriate memory type be chosen to function with the Am9080A. This chapter discusses the basic timing requirements for the Am9080A instruction cycle, plus the timing parameters that must be considered when designing microcomputer memory systems.

A typical Am9080A microcomputer block diagram is shown in Figure 14-1. The memory system may be composed of random access (RAM) memory products as well as read only (ROM) memory products.

The microcomputer initiates a memory access cycle by generating an address that is transmitted to the memory system via the Address Bus. Address Bus buffers may or may not be required, depending on the design of the memory system. Control signals originating in the Am8228 System Controller control both the time at which the memory access will be executed and the direction in which information is to be transmitted on the Data Bus. A typical microcomputer configuration will have bidirectional Data Bus buffers to isolate the data signals from the memory and provide the necessary signal amplitude to interface to the Am9080A. Address and Data Bus buffers are discussed in greater detail in Chapter 13, which discusses static memory organization.

Memory Read Cycle

The memory read cycle for an Am9080A using non-clocked memories is shown in Figure 14-2. Notice that two clock cycles are used by the CPU to generate an address and read the data at the addressed memory location. Figure 14-2 shows maximum available memory access timing within which the Am9080A microprocessor will function over the full environmental operating range. The maximum allowable memory access time is the interval between the memory address becoming available to the memory circuits and the output from the memory becoming available to the Data Bus.

The time delay for chip select decode logic is not included in the access time calculation. Typical chip select decode logic circuits will introduce delays that are generally on the order of 15 to 30 ns. However, the specifications for typical memory products show that the chip select signal can be applied somewhat later than the address without introducing extra delays in the availability of data. The critical memory accesd path for the read cycle is from the time that the memory address is available until the data read from the selected location is available to the microprocessor.

The equation for calculating the maximum allowable memory access time can be derived from timing parameters as follows:

$$tACC = 2tCY - (tr + tDA + tBA + tDS2 + tMB)$$

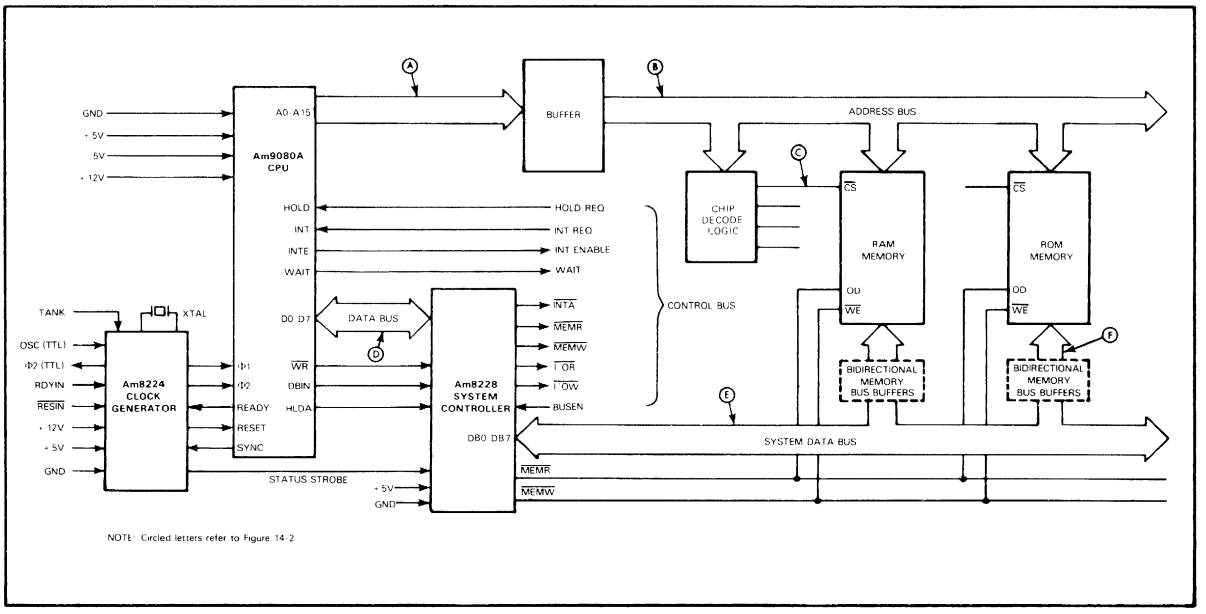


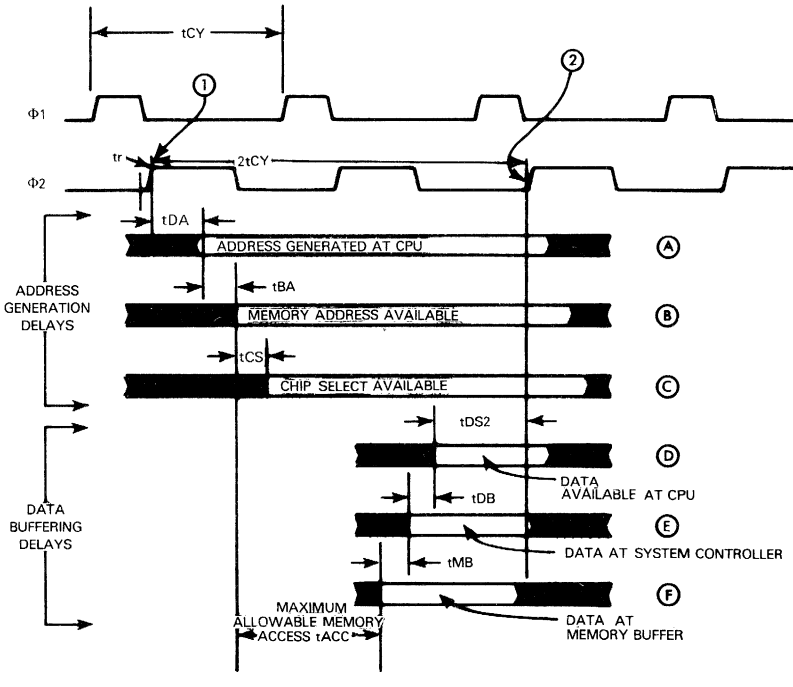
FIGURE 14-1 TYPICAL Am9080A SYSTEM ORGANIZATION

This equation is quite general for 8080A/9080A-based microcomputers using non-clocked memories and includes allowance for both address and memory data buffers.

In the smallest memory systems, (that is, memories that are typically less than 2K bytes), when using 1K memory circuits, Address buffers and extra memory Data Bus buffers other than those incorporated in the Am8228 will not be required. Larger memory systems (those requiring approximately 2K bytes of memory or more) may require the use of Address Bus buffers. Additional Data Bus buffers may also be required depending on the type of memory circuits that are used and the capacitive and DC load conditions presented by the memory circuits to the Data Bus. The corresponding delays in propagating signals (addresses, and data) through these buffers must be subtracted from the maximum available memory access time. This means that microprocessors with larger memory systems have tighter constraints on the maximum allowable memory access time in order to ensure reliable operation over the full environmental conditions.

Table 14-1 shows assumed delay parameters for each version of the Am9080A microprocessor. Three sets of parameters are listed for each version. The first set assumes that no Address Bus buffers, nor separate memory block Data Bus buffers are required. This will be characteristic of small to moderate memory systems. The second entry for each microprocessor includes allowance for address buffers. Larger memory systems will require that the memory be partitioned into blocks with separate Data Bus buffers for each block to isolate the DC and capacitive loads from the Data Bus system; this is shown as the third entry. Table 14-1 shows that as additional memory buffers are included, their propagation delays subtract from the minimum allowable memory access time of the circuits used in the memory. For example, the Am9080A with a minimal memory system operating with a 480 ns clock period can accept a memory circuit with an access time of 560 ns or less. However, when the same microprocessor is used with a large memory system, memory components with a minimum access time of 500 ns must be used if the clock period is to be retained at 480 ns.

The tACC equation given earlier in this chapter shows that there is a linear relationship between all the timing parameters and the minimum allowable memory access time. Thus, it is possible to increase one of the timing parameters in order to decrease another parameter, without altering the maximum allowable access time.



PARAMETER	DEFINITION	CIRCUIT	MINIMUM	MAXIMUM	UNITS	COMMENTS
tr	Φ2 RISE TIME	Am8224		20	ns	
tDA	CLOCK Φ2 TO ADD OUT DELAY	Am9080A	200		ns	
tBA	ADDRESS BUFFER DELAY	ADD BUFFER		30	ns	EXPECTED MAXIMUM
tCS	CHIP SELECT DELAY	CHIP ENABLE LOGIC	15	50	ns	EXPECTED DEPENDING ON CIRCUIT
tDS2	DATA IN TO Φ2 CLOCK SET UP	Am9080A		150	ns	
tDB	DATA BUS PROPAGATION DELAY	Am8228		30	ns	
tMB	MEMORY BUFFER DELAY	MEMORY BUFFER		30	ns	EXPECTED MAXIMUM
tACC	MEMORY ACCESS TIME	MEMORY				

FIGURE 14-2 READ CYCLE TIMING FOR NON-CLOCKED MEMORIES

TABLE 14-1 MAXIMUM AVAILABLE MEMORY ACCESS TIME FOR VARIOUS SYSTEM CONFIGURATIONS

SYSTEM		MIN tCY	MAX(1) tr	MAX tDA	MAX(2) tBA	MIN tDS2	MAX tDB	MAX(2) tMB	MIN tACC
1	Am9080A	480	20	200	0	150	30	0	560
2					30			0	530
3					30			30	500
4	Am9080A-2	380	20	175	0	130	30	0	405
5					30			0	375
6					30			30	345
7	Am9080A-1	320	20	150	0	120	30	0	320
8					30			0	290
9					30			30	260

1) Φ2 generated by the Am8224 has a max rated tr of 20 nsec.

2) Address Buffers are assumed for medium to large memory systems and separate memory block Data Buffers are assumed only for larger memories.

The tACC equation may be rearranged to solve for the minimum microprocessor cycle time (tCY) as a function of the memory circuit access time. tCY is given as follows:

$$tCY = 1/2(tACC + tr + tDA + tBA + tDS2 + tDB + tMB)$$

Figure 14-3 shows the minimum allowable processor cycle time (tCY) for the Am9080A versus available memory access time for three different system configurations. Each of the curves terminates in the lower left-hand corner at 480 ns tCY which corresponds to the minimum allowable microprocessor cycle time for the Am9080A.

The curves can be used in two ways.

- The required maximum memory access time can be determined from the curves if the microprocessor clock period (tCY) is known.
- If the memory system is constructed with components having a known maximum address access time, the minimum usable microprocessor clock period can be determined.

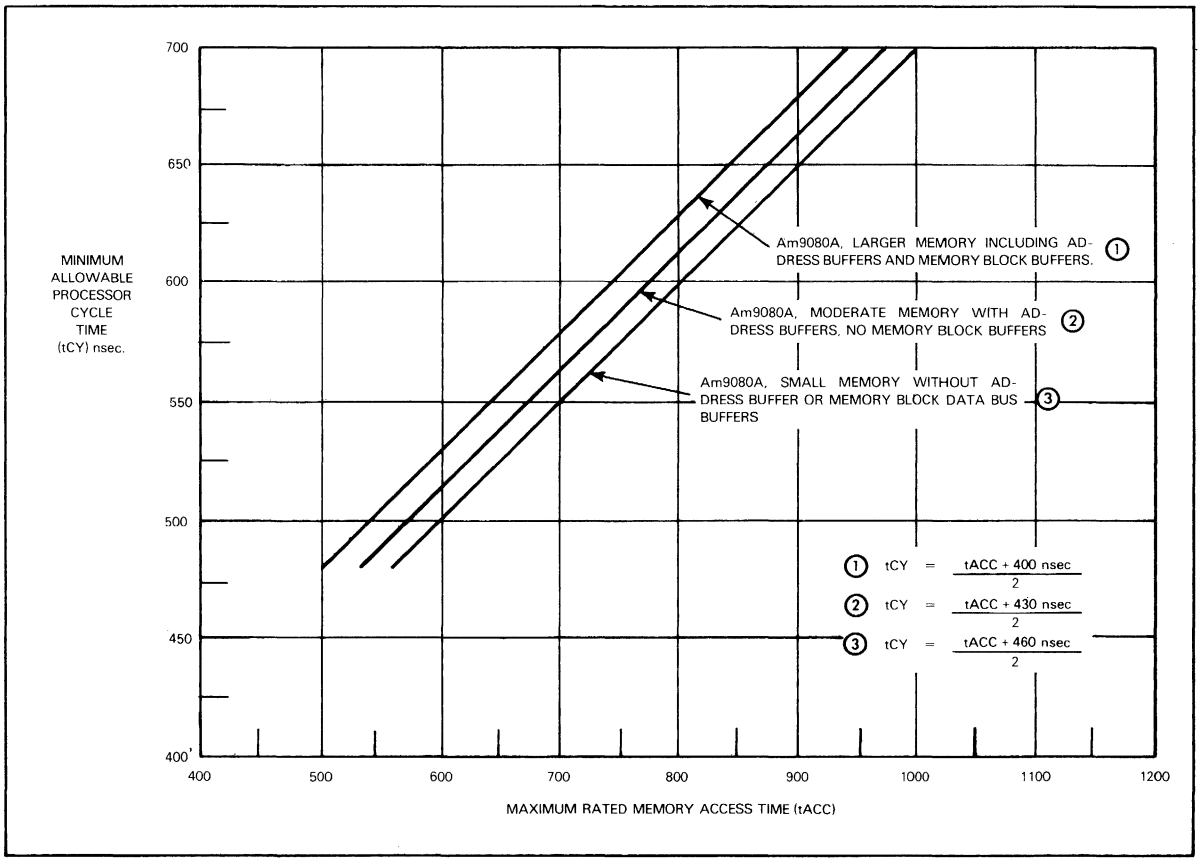


FIGURE 14-3 MINIMUM Am9080A CYCLE TIME VS MEMORY ACCESS TIME FOR THREE MEMORY CONFIGURATIONS

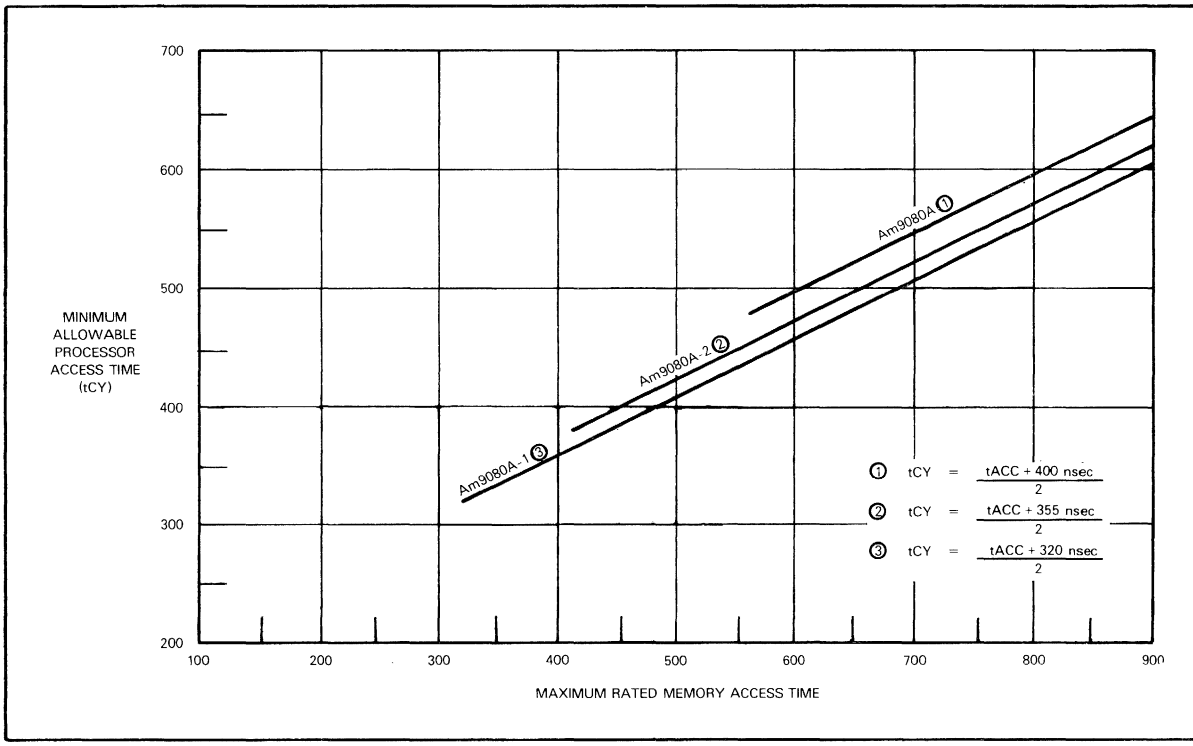


FIGURE 14-4 MINIMUM CYCLE TIMES OF DIFFERENT Am9080A MICROPROCESSORS WITH SMALL MEMORIES

Figure 14-4 shows the minimum cycle time of different versions of the Am9080A microprocessor configured with minimal memory systems versus memory access time. Each one of the curves terminates at the minimum rated clock period at which the corresponding microprocessor can be operated.

Timing for the memory read cycle is slightly different when constructing memory systems with clocked memories like the Am9130 and Am9140 4K static memories. Figure 14-5 shows the organization of the microcomputer using these devices. Figure 14-6 shows the timing for memory read operations. The maximum allowable memory access time (tA) is calculated as follows:

$$tA = 2tCY - (tr + tDS2 + tDB + tMB + tDSS + tDC + tCB)$$

tr = Φ2 rise time

tDS2 = data input to Φ2 set up time of Am9080A

tDB = propagation delay through the Am8228 Bus Driver

tMB = propagation delay through memory Data Buffers

tDSS = Φ2 to $\overline{STSTB}$ delay (Am8224)

tDC = $\overline{STSTB}$ to $\overline{MEMR}$ delay (Am8228)

tCB = CE gating delay

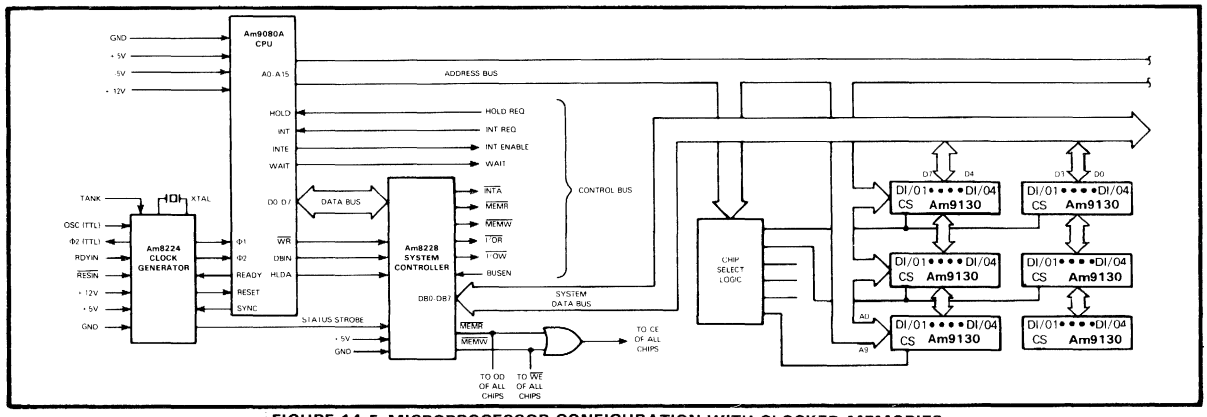


FIGURE 14-5 MICROPROCESSOR CONFIGURATION WITH CLOCKED MEMORIES

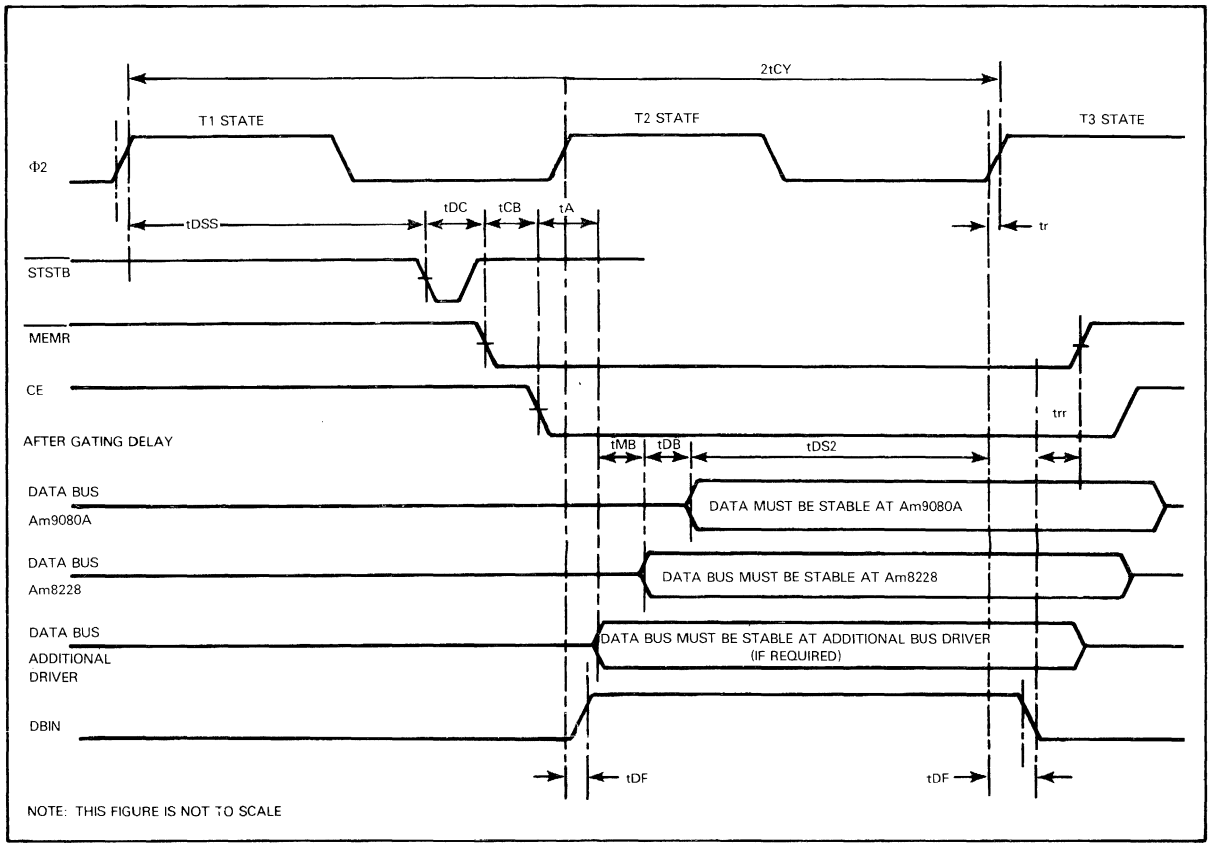


FIGURE 14-6 MEMORY READ OPERATION WITH CLOCKED MEMORIES

The critical timing for memory systems constructed with the Am9130 and Am9140 consists of the delays that accumulate until the Chip Enable signal is activated, the access time of the memory, and the delay in propagating the output back to the microprocessor Data Bus. Addresses are applied to the address inputs of the memories and are used for chip select decoding in the same way as for non-clocked static memories discussed earlier. However, the address generation is not the critical path for memory timing with this configuration.

Figure 14-5 shows that the $\overline{\text{STSTB}}$ signal, generated in the Am8224, is delayed from the leading edge of Φ2. $\overline{\text{STSTB}}$ latches the status bits from the CPU and causes the $\overline{\text{MEMR}}$ signal to be activated during a memory read cycle. However, additional delays are encountered in the Am8228 in generating the $\overline{\text{MEMR}}$ signal as indicated in the parameter tDC. The Am9080A timing is such that the address outputs will be stable to the memories well before the $\overline{\text{MEMR}}$ signal is energized. However, memory access time for the clocked memories is measured as the interval between the Chip Enable signal becoming active high and data being available at the output of the memory circuit.

The delays corresponding to propagation of signals through memory data buffers in larger systems is reflected in the timing parameter tMB. Parameter tDF describes DBIN delayed from the rising edge of Φ2. This signal is used to gate the outputs from the memory through the Data Bus buffers contained in the Am8228 to the CPU. The system timing is, however, such that this delay will be considerably shorter than the access time of the memory and therefore will not appear in the critical path. For this reason it does not appear as a term in the tA equation for calculating memory access time.

The equation is rearranged to solve for tCY as follows:

$$tCY = 3/4(tA + tDC + tCB + tDB + tDS2 + tr)$$

Table 14-2 shows worst case timing parameters for each of these terms.

The equation is plotted in Figure 14-7 for the different Am9080A microprocessors configured with different speed versions of the Am9130/9140 memories.

The timing diagram of Figure 14-8 shows the memory write ($\overline{\text{MEMW}}$) signal as having the same shape but delayed from the write pulse ($\overline{\text{WR}}$). $\overline{\text{WR}}$ is generated whenever an output from the microprocessor is generated regardless of whether that output is to be written into memory or I/O. The $\overline{\text{MEMW}}$ signal is generated from the $\overline{\text{WR}}$ signal only during those machine cycles in which a write is to be performed to the memory. This signal can be used to activate the read/write line of the memory circuits.

Memory Write Cycle

The memory write operation requires an address to be generated by the CPU; data must be placed on the Data Bus, and a write pulse must be applied after both the address and the data are stable. A typical configuration for a microprocessor system incorporating non-clocked memories is shown in Figure 14-1. The write cycle timing for this circuit is shown in Figure 14-8. The critical timing delays are the length of time it

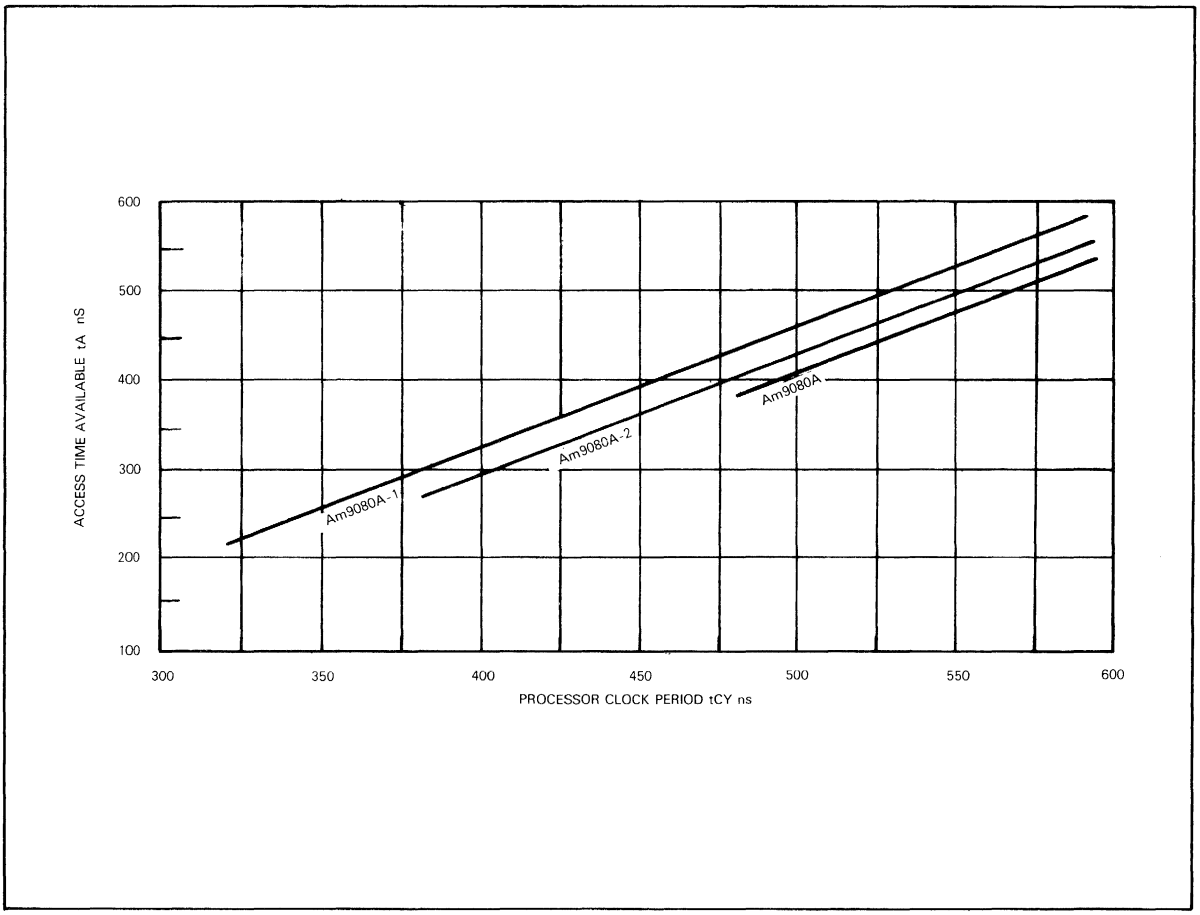


FIGURE 14-7 PROCESSOR CLOCK PERIOD AS A FUNCTION OF ACCESS TIME FOR THE Am9130/9140 CLOCKED MEMORIES

TABLE 14-2 TIMING PARAMETERS ASSUMED FOR FIGURE 14-7

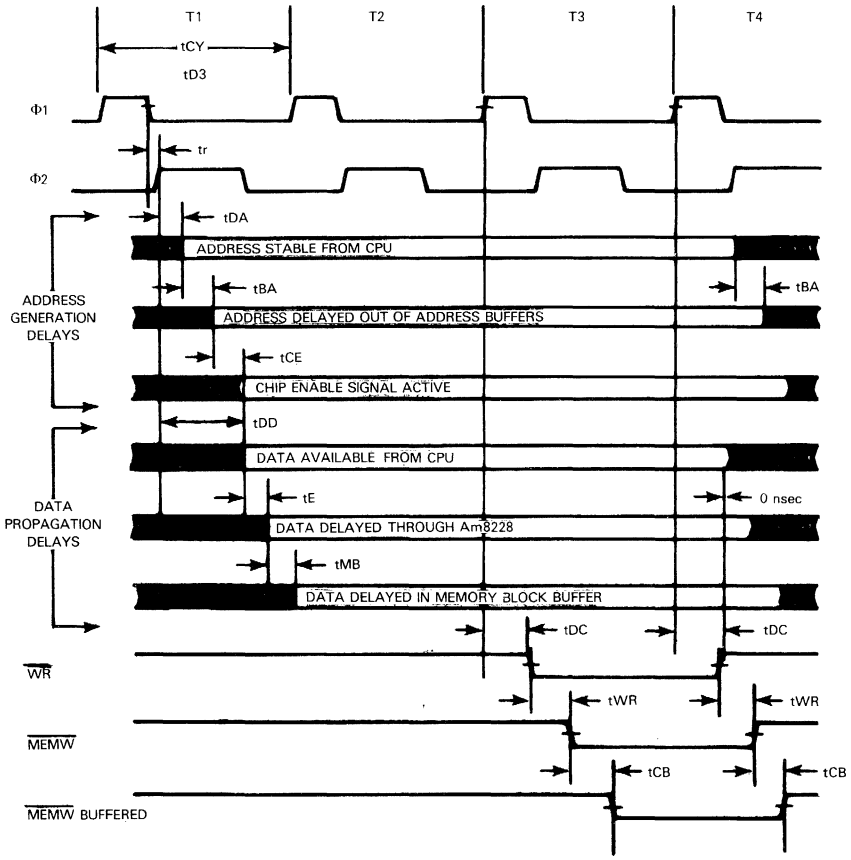
PROCESSOR	CLOCK PERIOD ns	TIMING PARAMETERS (ns)							ACCESS tA ns
		2tCY	tDSS	tDC	tCB	tDB	tDS2	tr	
Am9080A	480	960	320	45	10	30	150	20	385
	491	982	325	45	10	30	150	20	400
	566	1132	375	45	10	30	150	20	500
Am9080A-2	380	760	253	45	10	30	130	20	272
	401	802	265	45	10	30	130	20	300
	476	952	315	45	10	30	130	20	400
	551	1102	365	45	10	30	130	20	500
Am9080A-1	320	640	213	40*	10	20*	120	20	217
	382	764	260	40*	10	20*	120	20	300
	457	914	310	40*	10	20*	120	20	400
	532	1064	360	40*	10	20*	120	20	500

*From Am8238-4 spec

takes to generate the address and decode the chip select signals to the memory circuits, and the length of time it takes to make data available from the CPU to the memory inputs. Both of these delays must be completed, and the address and data to the memories must be stable before the write pulse is initiated. In the circuit diagram of Figure 14-1, the memory circuit write control signal is operated by the $\overline{\text{MEMW}}$ signal originating in the Am8228. The minimum and maximum time delays specified for the components shown in Figure 14-1 are contained in the table at the bottom of Figure 14-8. An analysis of these timing parameters will indicate that there is sufficient time for both the address and data to become stable before write pulses apply to ensure that there is no critical timing path during the memory write cycle.

When constructing memory systems with the Am9080A microprocessors, care must be exercised to ensure that data is not removed from the memories significantly before the write pulse is deactivated. When the microprocessor consists of the Am9080A CPU, Am8228 Clock Generator, and Am8228 System Controller, proper operation of the memory write cycle over the full environmental operating conditions is assured.

The foregoing discussions are centered on memory speeds necessary to allow the microprocessor to operate at its minimum rated clock period. However, it is possible with the Am9080A to construct a microcomputer that uses memory products with slower memory cycle times than those that allow the microprocessor to run at its full operating speed. To



PARAMETER	DESCRIPTION	CIRCUIT	MIN.	MAX.	UNITS	COMMENTS
tCY	CLOCK PERIOD	Am9080A	250	2000	nsec	
tr	CLOCK RISE TIME	Am8224	20		nsec	
tDA	CLOCK Φ2 TO ADD DELAY	Am9080A		200	nsec	
tBA	ADDRESS BUFFER DELAY	ADD BUFFERS		30	nsec	EXPECTED MAX.
tCE	CHIP ENABLE LOGIC DELAY	C.E. LOGIC		30	nsec	EXPECTED MAX.
tDD	CLOCK Φ2 TO DATA DELAY	Am9080A		220	nsec	
tE	DATA PROPAGATION DELAY	Am8228		30	nsec	
tMB	MEMORY BUFFER DELAY	MEMORY BUFFERS		30	nsec	
tDC	CLOCK TO CONTROL DELAY	Am9080A		120	nsec	
tWR	WR TO MEMW DELAY	Am8228	5	45	nsec	
tCB	CONTROL BUFFER DELAY			30	nsec	WHERE REQUIRED

FIGURE 14-8 MEMORY WRITE CYCLE TIMING

ensure that information is not lost, the memory system can request that the Am9080A temporarily suspend its operation and wait until the memory has completed its access. This is accomplished by applying a Ready signal to the Am9080A CPU. A memory read cycle begins with the Ready line normally high. The CPU initiates a memory access cycle and supplies the address to the memory system. The memory responds by deactivating the Ready line with a low level input for a time sufficient to allow the memory system to complete the access. After the appropriate time delay, the Ready signal would be returned to the high level and the microprocessor resumes its normal operation. Figure 14-9 shows the timing required to inject the Wait state into the machine cycle with the deactivation of the Ready input. The Ready input must be deactivated for the minimum period labeled tRS prior to the trailing edge of Φ2. The Wait state is entered on the next following leading edge of Φ1. Wait is shown delayed from the leading edge of Φ1 by the time period tDC. The Am9080A remains in the Wait state until the Ready line is returned high. During the time that the CPU is in the Wait state, the Address Bus will hold its output to the memory system. If a write cycle is in progress the Data Bus outputs will remain stable for the duration of the Wait state. $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signals also remain stable.

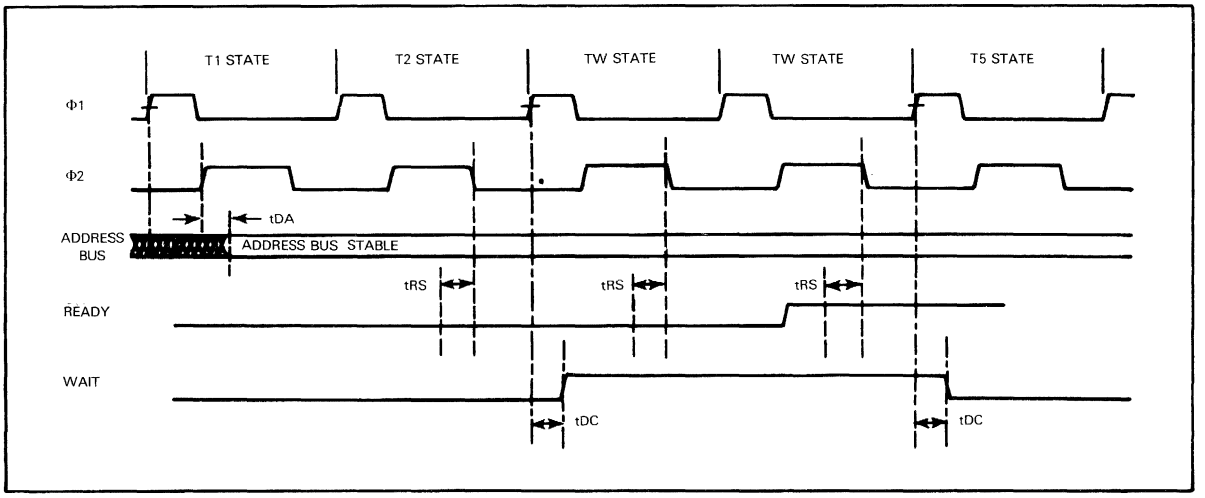


FIGURE 14-9 WAIT CYCLE OPERATION

Chapter 15
INTRODUCTION TO INTERRUPTS

A program is executed by a microprocessor in order to implement the transfer functions required in the microcomputer system. Most programs obtain information from external devices (inputs) and transfer results to external circuits (outputs).

The service requirements for input/output devices, however, have a wide latitude. For example, a telecommunication terminal operating at 110 baud generates or requires a new information bit every 9.09 milliseconds; a limit switch in an industrial process may only actuate once a day or less; a CRT display may need service every microsecond. After a data bit is presented to a communication channel, the program has about 9 milliseconds in which to prepare the next bit of presentation. However, in the latter example, the closure of a limit switch may require immediate attention. Thus, the methods of servicing the I/O devices by the program must be tailored to the characteristics and requirements of the devices.

There are two general ways in which a program services I/O circuits.

- Program Controlled I/O
- Interrupt Driven I/O

PROGRAMMED I/O

Programmed I/O exists when the program is structured to periodically test I/O circuits to determine their operational condition. With more than one I/O circuit, the process of testing each I/O in sequence is known as polling. If an I/O needs service when polled, the program may record this event for later processing or may immediately enter the I/O service routine.

Programmed I/O techniques are best used when:

- The frequency of service required by an I/O device is known and the service time required is relatively long, or
- The program has few other tasks that can be performed while waiting for I/O operations.

The frequency at which an I/O circuit is polled is determined principally by the time required to completely service it. Thus, if a device must be serviced within one millisecond after it is ready, it must be polled at a frequency greater than one kHz. The polling frequency of the device is calculated as follows:

$$fP = \frac{1}{tF + tP + tS}$$

where: tF is the maximum time to complete the current program task subsequent to the I/O device becoming ready for service.

tP is the maximum time for the program to complete the polling subroutine and identify the I/O device that needs service.

tS is the time required to execute the I/O service subroutine (or a portion of the subroutine required).

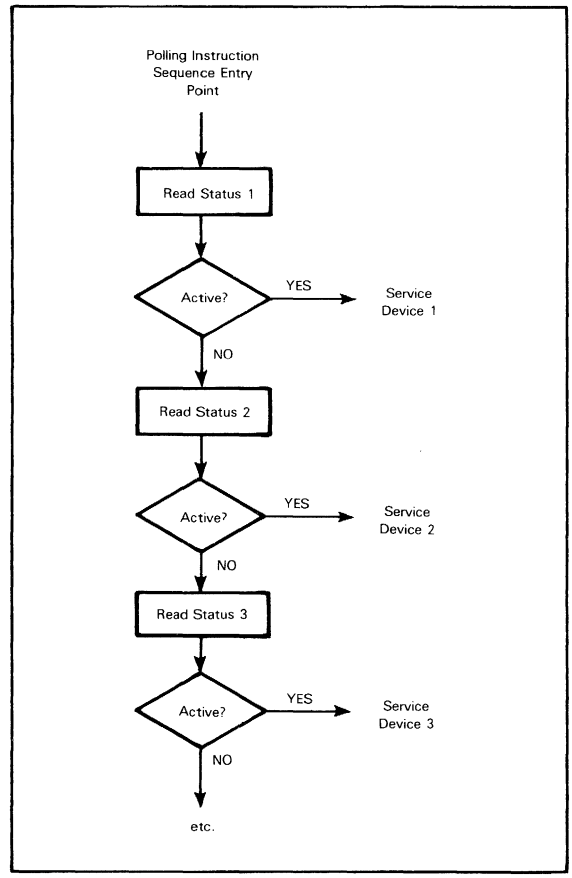


FIGURE 15-1 POLLING PROGRAM LOGIC

Assume an I/O device generates a service requirement once every second and requires service within one millisecond after the request.

The I/O device must be polled at a frequency greater than 1,000 times a second. However, only when the device requires service will an I/O subroutine be executed. The remaining polling sequences consume microprocessor execution cycles with no useful transfer functions being executed. Implementing programmed I/O consists of including an instruction sequence which periodically scans external I/O device status conditions. The program which tests the status must contain logic which branches to an appropriate I/O service routine upon detecting the appropriate status.

If a number of different external logic sources need to be serviced by a single microprocessor, the program being executed by the microprocessor will contain an instruction sequence which checks the status of each external logic device in turn.

This is the polling subroutine. Programmed logic associated with polling is illustrated in Figure 15-1.

Each polling step in Figure 15-1 can be implemented, with the 8080A/9080A I/O instructions, as follows:

```
-
-
IN      STATX   Input Device Status
JNZ     PROGX   If not zero, branch to device
                service routine
-
-
```

For the usual case where the non-zero condition exists, these two instructions execute in 20 machine cycles, which require between 3.75 and 10 μsec, depending on the microprocessor and clock period in use. If a microcomputer system must service ten different external logic sources, and each poll requires 7.5 μsec all ten external sources can be polled in 75 μsec.

In many microcomputer systems, the program receives data from the I/O sub-system before proceeding and may be sufficiently lightly loaded that the polling overhead is not a problem.

INTERRUPT I/O

In contrast to programmed I/O, where the microprocessor schedules all events, interrupt I/O allows external logic to force program execution sequence changes. Figure 15-2 illustrates the logical concept of an interrupt.

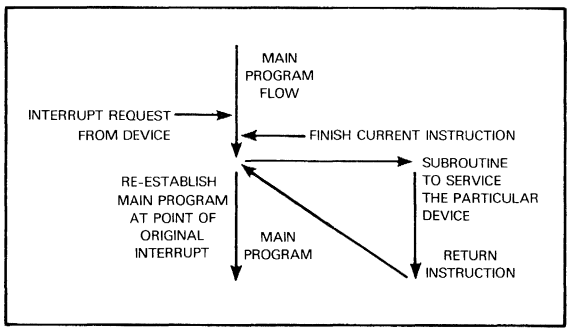


FIGURE 15-2 PROGRAM FLOW SHOWING THE MAIN PROGRAM BEING INTERRUPTED

A microprocessor that supports interrupts will have a specific signal or signals via which external logic can request an interrupt. The microprocessor will acknowledge an interrupt upon completing execution of one instruction and before starting execution of a new instruction. At its most elementary level, the process of acknowledging an interrupt involves saving the Program Counter contents - which addresses the object code for the instruction which was about to be executed - then loading some new address into the Program Counter. These steps are illustrated in Figure 15-3.

The interrupt occurs at A while the instruction location MR is executing. When the instruction is completed, the CPU disables further interrupts and generates an Interrupt Acknowledge machine cycle during which the interrupting device inserts an extra instruction to be processed (shown at B). This instruction is usually a Restart (RST) or a Call. Either of these instructions causes the Program Counter contents (now MR + 1) to be saved (C) in the area of memory pointed to by the contents of the Stack Pointer + 1. The RST or Call instruction causes the Program Counter to be loaded with the location of the first instruction (SR) shown at D. The interrupt service routine is executed and control passed back to the main routine. Interrupts are re-enabled at E if not re-enabled earlier (instruction at location SR + k-1). A Return (RTN) instruction is executed at F (instruction in location SR + k). This causes the Program Counter contents to be read from Stack locations SP + 1 and SP + 2 and loaded to the Program Counter. The next instruction of the main routine (at location MR + 1) is now loaded (G) to the Instruction register and executed.

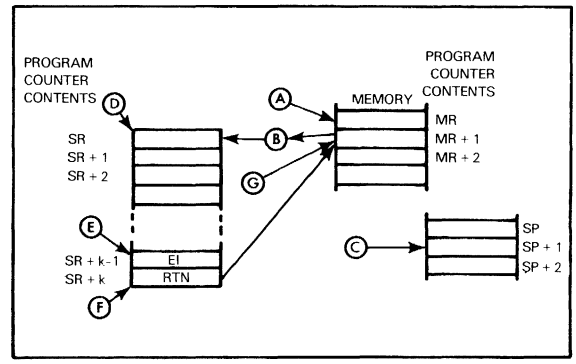


FIGURE 15-3 SEQUENCE OF EVENTS FOR INTERRUPT PROCESSING

An interrupt subroutine in which only the Program Counter is saved is limited to processing instructions which do not disturb the contents of CPU registers which may be in use by the main routine; more commonly, registers are used by both the main routine and the service routine. In this case, it is frequently necessary to save the contents of the A, B, C, D, E, H and L registers as well as the contents of the program status word before servicing an interrupt. Once the interrupt service routine has completed execution, all these register contents must be restored. If Stack instructions are used to save and restore register contents in pairs, then the following instruction sequence represents the overhead associated with every interrupt service routine:

```
PUSH    PSW     Save PSW and A
PUSH    B       Save B and C
PUSH    D       Save D and E
PUSH    H       Save H and L
Start of interrupt service routine
-
-
-
-
End of interrupt service routine
POP     H       Restore registers
POP     D
POP     B
POP     PSW
```

These eight instructions execute in 84 machine cycles. In addition, the Enable Interrupts and Return Instructions, when used, add 15 cycles.

Provided that a single external logic source can request interrupts, the interrupt acknowledge process is very straightforward. By way of contrast, the polling overhead is 20 machine cycles per interrupting source.

When more than one external logic source may request an interrupt, three additional considerations need to be addressed:

1) Following an interrupt acknowledge, the microprocessor must have some means of identifying which external source requested the interrupt.
2) In the event that more than one external logic source is requesting interrupt service simultaneously, interrupt request priorities must be arbitrated.
3) Some method to selectively enable and disable interrupt requests from specific devices may be desired.

SOURCE IDENTIFICATION IN MULTIPLE INTERRUPT CONFIGURATIONS

When dealing with multiple interrupts, microcomputer systems in general provide two methods of determining their interrupting source: polling and vectoring.

Polling is similar to the program sequence illustrated in Figure 15-1; however, the instruction sequence is executed following an interrupt acknowledge, that is, at the beginning of the interrupt service routine.

If, following an interrupt acknowledge, instructions have to be executed to determine the source of the interrupt request, then interrupt logic has enabled the asynchronous execution of the polling sequence -- and that is all. The fact that the polling sequence follows an interrupt request means that at least one active interrupt request is present. In programmed I/O, the polling instruction sequence may be executed many times when no external logic is requesting I/O service. Therefore, initiating execution of the polling sequence has merit, even though response time to a service request is still long.

Vectoring is a far more efficient method of handling interrupts. Vectored interrupt logic requires that the device requesting interrupt service identify itself by contributing to the address which is loaded into the Program Counter following the interrupt acknowledge. Thus, vectored interrupt acknowledge logic causes different addresses to be loaded into the Program Counter such that each address is specific to a single external interrupt request. Now program logic spends no time determining the source of the interrupt and can service the interrupt immediately. Figure 15-4 illustrates vectored interrupt logic.

The 8080A/9080A provides two means of implementing vectored interrupt logic. When the Am9080A acknowledges an interrupt, it outputs an interrupt acknowledge status (INTA); in response to INTA, the microprocessor anticipates receiving, on the Data Bus, the object code for one instruction to be executed in response to the interrupt acknowledge. Typically this instruction will be a Restart (RST) or a Call.

8080A/9080A interrupt logic has been described in detail in the processor description elsewhere in this Handbook. The following is a summary of the interrupt acknowledge event sequence:

1) External logic requests an interrupt by placing a high signal at the microprocessor INT input.
2) Provided that interrupts have been enabled, the microprocessor will acknowledge the interrupt upon completing execution of the current instruction.
3) Interrupts are disabled.
4) Upon acknowledging an interrupt, the microprocessor executes a special interrupt acknowledge Instruction Fetch sequence. During this Instruction Fetch sequence, the Program Counter contents are not incremented, and an INTA status is output on the Data Bus during the second clock period of the INTA machine cycle. The Am8228/38 System Controller device automatically converts this INTA status into an INTA control signal.
5) INTA causes an instruction to be placed on the Data Bus.
6) The instruction inserted by the interrupting device during the active INTA signal is executed.

External logic must sense the INTA status or control signal and respond to it by performing whatever priority arbitration or interrupting device identification steps may be required. It must also generate the instruction code required by the microprocessor during the interrupt acknowledge sequence and must place it on the Data Bus. Any instruction, with the exception of the XTHL instruction, may be returned by external logic during the interrupt acknowledge Intruction Fetch sequence. Most frequently the Restart or Call instructions are used.

Microcomputer systems with only one interrupting device may have the RST 7 instruction inserted automatically by the Am8228/38 System Controller. Thus, no external logic is required. This application of the System Controller is described in Chapter 5.

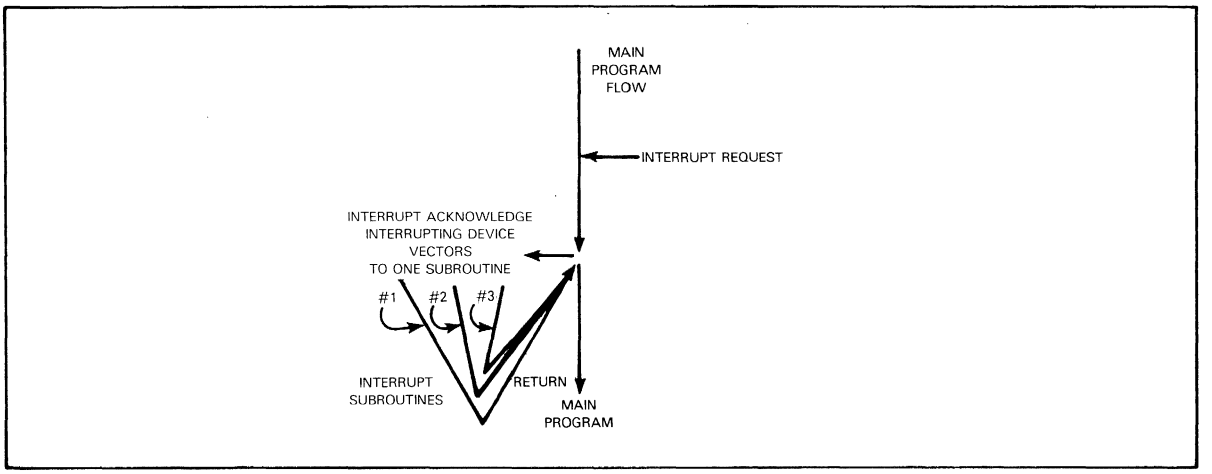


FIGURE 15-4 PROGRAM FLOW WITH SEVERAL INTERRUPTING DEVICES

The circuit of Figure 15-5 generates one of three interrupts using only one additional buffer circuit (Am25LS240) and an "OR" gate. When multiple interrupts occur concurrently, the resulting combined Restart instruction will load the Program Counter with the address of a location other than one of the three desired interrupt subroutines. A service routine would then be programmed at this location to determine which of the concurrent interrupts should be serviced first.

The circuit of Figure 15-6 expands the Am9080A microcomputer to provide for eight interrupting devices using the Am25LS2513 priority encoder. Three-state output circuits allow the encoder to connect directly to the System Data Bus.

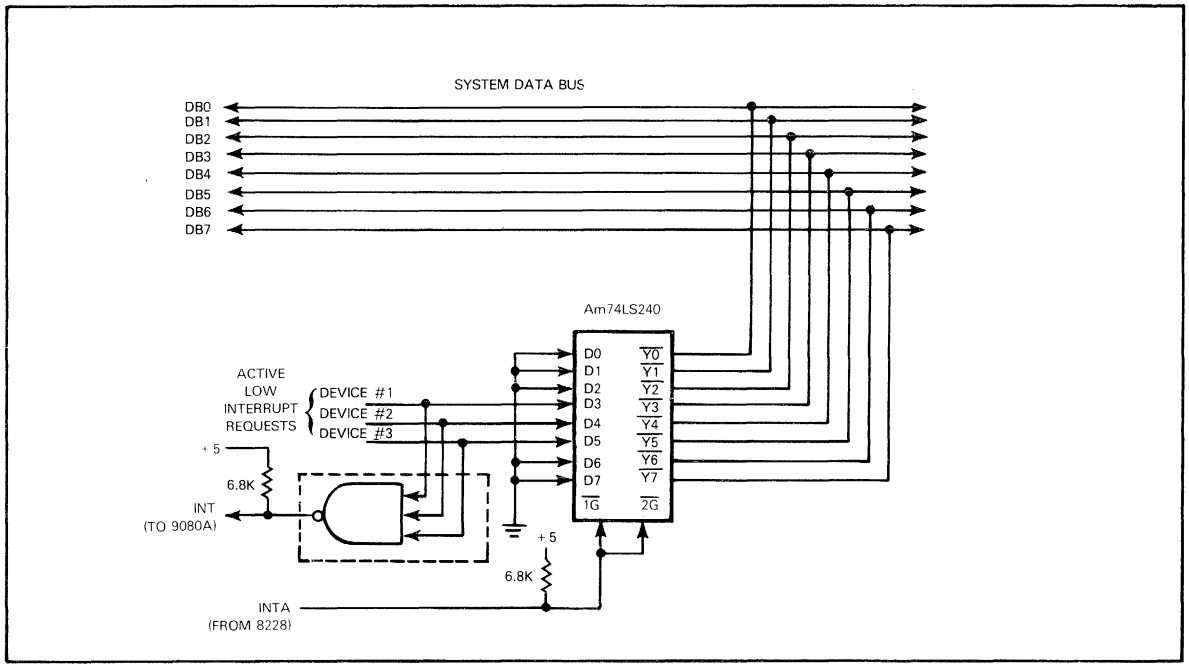


FIGURE 15-5 Am9080A MICROCOMPUTER WITH THREE INTERRUPTS

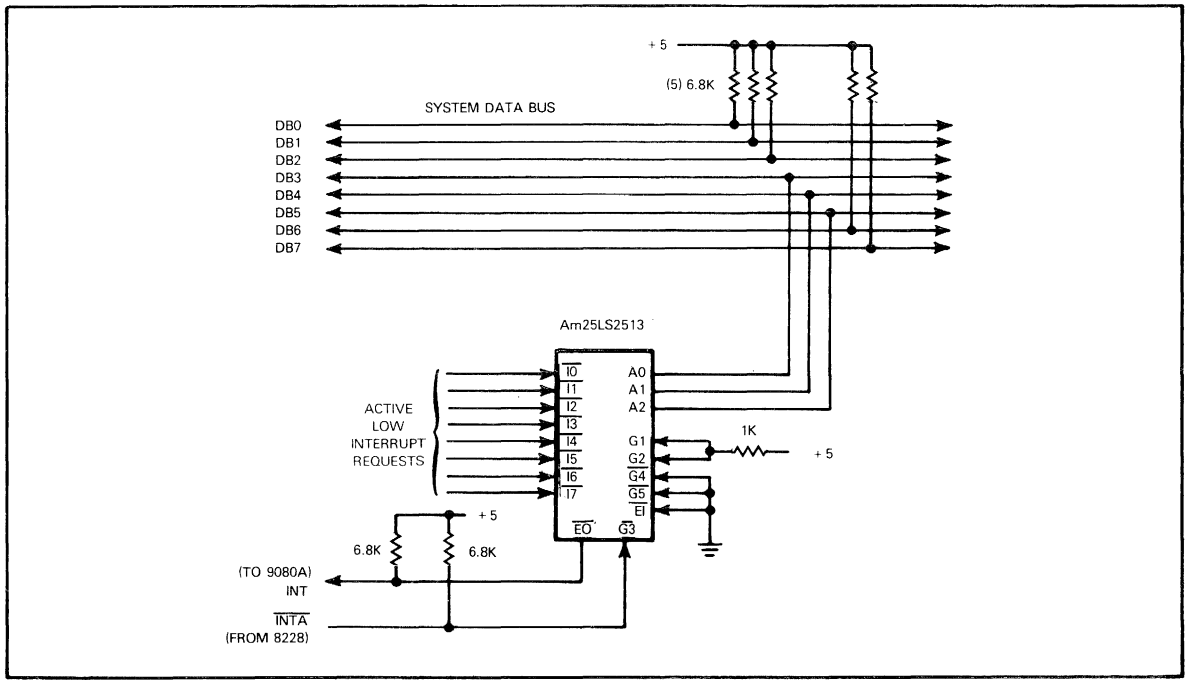


FIGURE 15-6 PRIORITY ENCODED RST INTERRUPT INSTRUCTION

The other five Data Bus signals are returned to V_{CC} through pull-up resistors to ensure that the full 8-bit Restart vector is generated when the INTA signal is active. The resistor values shown are representative only and must be selected independently for each system to provide the optimum trade off between fast capacitive charge time and minimum D.C. load on the bus.

Chapter 16
BASIC TIME DELAYS

The generation of time delays represents an important part of many microcomputer systems. This is particularly true of the on-line control of industrial processes into which so many microprocessors are incorporated. Film developing, copy machines, chemical reactions, heat treatment, space vehicle guidance, home appliance control, etc. are examples of applications in which timing becomes a significant part of the control process. Even in conventional data processing and display terminals, time delays are an important function. The generation of time delays and recording of real time events is a requirement of the microcomputer in these and other applications.

There are two commonly used methods of generating time delays.

- Programmed timing loop
- Externally generated timing

The principal advantages of the programmed timing loop are the ease with which it can be created and the elimination of any additional external circuits to generate the time delays. Program generated time delays are based on executing an instruction sequence, where the time taken to execute instructions can be computed exactly. In the simplest case, an elementary instruction loop is executed some fixed number of times. Consider the following instruction sequence:

```
                                                    Clock
                                                    Periods
        MVI     A,COUNT   Load initial counter value   7
LOOP    DCR     A         Decrement Counter           5
        JNZ     LOOP      Repeat if not zero          10
```

An initial constant, represented by the label COUNT, is loaded into the Accumulator. The next two instructions decrement the Accumulator contents and test for zero. When the Accumulator contains 0, execution falls through the delay sequence. The DCR and JNZ instructions form a loop which executes in 15 clock periods. The initial MVI instruction executes in 7 clock periods, so the total time delay is given by the equation:

$$DELAY = [\,15(COUNT) + 7]tCY$$

Where: COUNT is the value loaded to the Accumulator at the start of the delay.

tCY is the microprocessor operating clock period.

tCY typically varies between 250 and 500 nsec depending on the Am9080A version used. The maximum time delay is generated when COUNT initially equals 0, since the Accumulator will contain FF_{16} following the first decrement. Thus, assuming a 500 nsec clock, the instruction sequence illustrated above will generate time delays ranging from 11 through 1923.5 μsec, in increments of 7.5 μsec.

The length of the time delay can be increased in several ways including:

- Insert more instructions in the basic timing loop.
- Use counts which are greater than eight bits in length.
- Repeat the delay routine several times.

Longer timing loops can be programmed with the use of nonfunctional instructions such as NOP, ANA A, ORA A, as in the following sequence.

```
                                                    Clock
                                                    Periods
        MVI     A,COUNT   Load initial counter value   7
LOOP    NOP               Pause                       4
        NOP               Pause                       4
        DCR     A         Decrement Counter           5
        JNZ     LOOP      Return if not zero          10
```

This routine has a delay which is:

$$DELAY = [\,23(COUNT) + 7]tCY$$

The minimum and maximum delays achievable with this loop using an 8-bit value for COUNT are 15 μsec and 2947.5 μsec respectively, assuming tCY is 500 nsec. The delay time increment is 11.5 μsec.

Rather than using longer strings of NOP instructions to increase the delay, nonfunctional instructions with longer execution times may be used as in the following example.

```
                                                    Clock
                                                    Periods
        MVI     A,COUNT   Load initial counter value   7
LOOP    ANI     0FFH      Pause                       7
        ANI     0FFH      Pause                       7
        DCR     A         Decrement Counter           5
        JNZ     LOOP      Return if not zero          10
```

The delay generated by this routine is 18 μsec minimum and 3715.5 μsec maximum assuming a tCY of 500 nsec and an 8-bit value for COUNT. The minimum increment is 14.5 μsec.

The disadvantage of increasing the timing delay by inserting nonfunctional instructions in the loop is that the minimum increment of delay is increased. However, the resolution, expressed as a per cent of maximum delay, is constant.

Delays that must be implemented with a small incremental value, but which must be capable of large delay intervals, can be implemented with larger binary numbers for COUNT.

Here is a possible instruction sequence based on a 16-bit value for COUNT.

```
                                                    Clock
                                                    Periods
        LXI     B,CNT16                             10
LOOP    DCX     B                                   5
        MOV     A,B                                 5
        ORA     C                                   7
        JNZ     LOOP                                10
```

The time delay is computed by the following equation:

$$DELAY = [\,27(CNT16) + 10]tCY$$

CNT16 can assume any value in the range 0 through 65,536.

Assuming a 500 nsec clock, the total time delay computed will vary between 18.5 μsec and 0.884741 seconds, in increments of 13.5 μsec.

The maximum time delay is generated by loading 0 into the B and C Registers with the LXI instruction. Following the first execution of DCX, 0000 will decrement to $FFFF_{16}$.

The DCX instruction does not set any status flags. Therefore, the following MOV and ORA instructions are required. These two instructions OR the contents of the B and C Registers, leaving the results in the Accumulator. If both the B and C Registers contain 0, then the ORA instruction will set the 0 status flag and cause execution of the time delay loop to terminate.

The disadvantages of using program generated time delays are that no otherwise useful instruction sequences can be executed during the time delay, and multiple time delays are difficult, if not impossible, to generate simultaneously.

Both of these objections are avoided if time delays are generated externally to the microprocessor. Additional circuits are added to the I/O system to generate the required delays under program control. If additional delays are required by the logic of the program, additional circuits are added as required. The program sets or initiates the time delays by setting specific flags in preassigned I/O ports as shown in Figures 16-1 and 16-2. When the delay terminates, it sets an input bit in a preassigned I/O port.

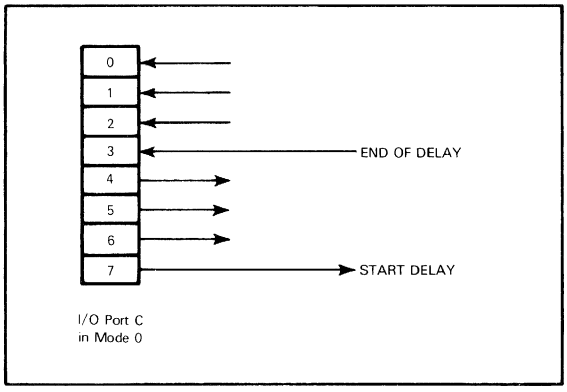


FIGURE 16-1 USING AN Am9555 PPI IN MODE 0 TO CONTROL A TIME DELAY

The program can be alerted by the timer that the delay has terminated in one of the following ways.

- The program may periodically test the input bit to determine if the delay has terminated.
- The timer may activate the interrupt request line to the CPU.

In the former case, the same problems with sampling the timer status flag (i.e., resolution is dependent on the length of the sampling programs, and the program is not completely free to process other functions) exist. Activating the interrupt with the termination of the time delay frees the microprocessor to perform other functions without the overhead of periodically sampling the timer status at the I/O port; however, additional I/O circuits must be provided for the timer interrupts.

External timers may be constructed with any of the usual techniques for generating time delays such as:

- Monostable multivibrators (one-shots)
- Counter operation from a predetermined clock source.

When several time delays are to be generated concurrently, these methods have the disadvantage of requiring more I/O circuitry.

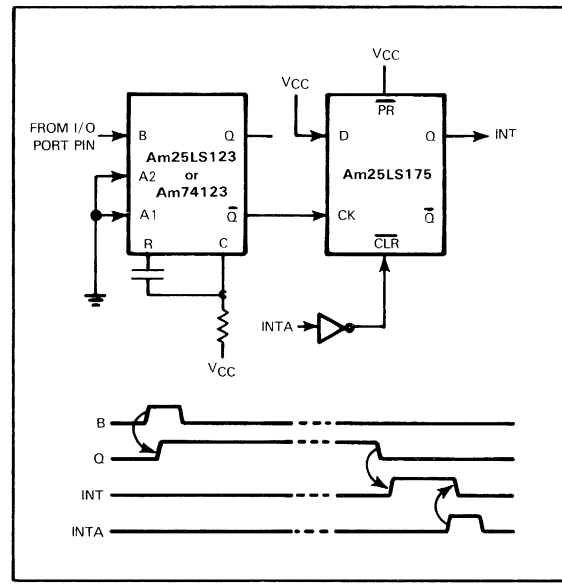


FIGURE 16-2 USING A MONOSTABLE MULTIVIBRATOR TO GENERATE A TIME DELAY

An alternative technique is to use memory locations that are incremented or decremented to perform the time delay counter functions as in the technique used by the programmed delay loop discussed earlier. The difference is that no delay loop is incorporated to generate delay time. Rather, an external clock source is provided which is connected to the INT line of the CPU to signal the program that a time mark has occurred. Figure 16-3 shows how this approach may be implemented.

Multiple time delays and real time counters are easily incorporated in this technique by assigning additional memory locations as required. Each time the time mark generator (÷N counter) causes an interrupt, the program stops its current task, increments or decrements each assigned timer location and tests for terminal counts. If one or more timers have terminated, the interrupt subroutine which decrements the timer locations sets flags to be tested and acted on by the main routine after the interrupt subroutine has completed. The main routine may initiate time delays asynchronously at any point in the program where required by setting the delay count value in the assigned timer memory location. The program control sequence to initiate a time delay is as follows:

1) The main program sets the desired time delay count into the assigned memory location.
2) An assigned bit is set in a special memory location that stores flags to indicate when timers are active.
3) The main routine continues normal processing until the timer interrupt occurs.
4) The interrupt subroutine decrements each currently active timer memory location and tests each for zero count.

5) The interrupt subroutine resets the timer flag for each timer memory location which is detected to be zero.

6a) Control is passed back to the main routine to resume normal processing; or,

6b) The interrupt subroutine performs whatever special processing is required by the application at the end of the time delay before returning control to the main program.

This method allows inclusion of additional timers and real time clocks to the application without expansion of I/O circuits, yet avoids utilizing the CPU processing capability to generate time delays.

The interval between time marks should be as long as practical to minimize the amount of processor capacity that is required to maintain the interval timers. On the other hand, the time marks must be generated by the ÷N counter frequently enough to provide the resolution needed by the timer requiring the smallest interval. Generally, when all timers are muliples of a single time mark interval, the interval can be made longer than when a completely nonsynchronous relationship exists between timer intervals.

If several timers must be used with one or a few having much higher resolution than the rest, two or more time mark generators can be incorporated in the external logic. Each mark is associated with a separate time delay subroutine which maintains interval timers only requiring high resolution or low resolution. The processing overhead associated with maintaining timers is therefore reduced.

In summary, use of program instruction sequences to generate time delays is recommended when the microprocessor is under-utilized in a microcomputer system. If the microprocessor has no useful instruction sequences to execute during a delay, then generating time delays using external logic simply represents additional hardware and fabrication expense. The use of external logic to generate time delays should be confined to applications where the microprocessor is pressed for time or where multiple parallel time delays are needed.

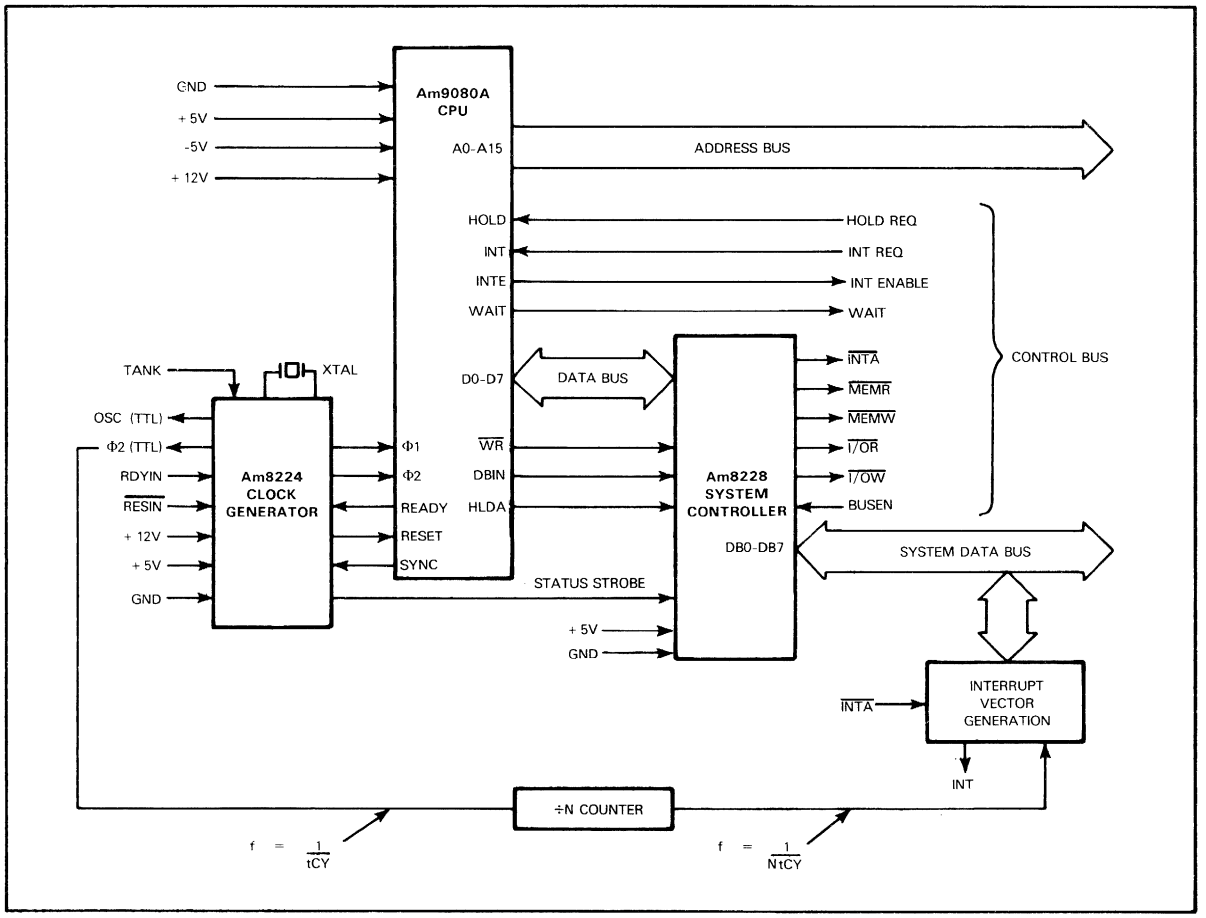


FIGURE 16-3 USE OF AN EXTERNAL COUNTER TO PROVIDE A TIME MARK FOR GENERATING SOFTWARE CONTROLLED DELAY LOOPS

Chapter 17
MULTIPLICATION

Many microprocessor applications need to multiply binary numeric data. In some cases, since execution speed is not a problem, software multiply routines will suffice. But many times the throughput requirements are so demanding that only external hardware can do the job. This chapter suggests methods to handle both types of requirements.

SOFTWARE MULTIPLICATION

There are several methods for programming simple multiplication. Figure 17-1 shows a conventional approach using a shift-and-add algorithm. This routine multiplies two 8-bit values located in Registers C and D and provides a 16-bit result in the BC register pair. The routine is 21 bytes long. Its execution time, in processor clock periods, is 477 + 4N, where N is the number of 1s in the C register operand. The average execution time (N=4) will be 493 periods which translates to 247 μsec for a 500 ns clock. Faster execution times can be achieved by using higher speed processors that can run with faster clocks.

Another multiply routine is shown in Figure 17-2. This routine simply adds the multiplicand to itself the number of times indicated by the value of the multiplier. The 8-bit multiplicand is located in Register E and the 8-bit multiplier in the Accumulator. The 16-bit result is formed in the HL register pair. This simple routine is only 14 bytes long, but is usually quite slow. Execution time in processor clock periods is 31 + 25M, where M is the value of the multiplier. The average execution time (M=128) is 3231 periods which translates to 1616 μsec for a 500 ns clock. Note, however, that for small values of the multiplier the performance improves significantly.

For example, when M=8, execution time drops to only 116 μsec with a 500 ns clock, less than half the average execution time of the shift-and-add approach.

Expansion of these types of software routines to higher numerical values — for example, 16 X 16 with 32-bit result — is not difficult, but will extend execution times dramatically. For many applications the speeds will still be quite reasonable.

```
                                                BYTES  #EXECUTIONS  CLOCK PERIODS
        MVI   B,0     ;CLEAR PARTIAL SUM          2        1            7
        MVI   E,9     ;LOAD LOOP COUNTER          2        1            7
        JMP   MID                                 3        1           10
LOOP:
        MOV   A,B                                 1        8            5
        JNC   MULT1   ;LSB OF C=0                 3        8           10
        ADD   D       ;LSB=1.  ADD  TO  PARTIAL   1      0 → 8          4
MULT1:
        RAR           ;SHIFT SUM FROM B TO  C     1        8            4
        MOV   B,A                                 1        8            5
MID:
        MOV   A,C                                 1        9            5
        RAR           ;CRY=LSB OF C               1        9            4
        MOV   C,A                                 1        9            5
        DCR   E                                   1        9            5
        JNZ   LOOP                                3        9           10
DONE:
```

FIGURE 17-1 A SHIFT-AND-ADD MULTIPLICATION PROGRAM

```
                                                BYTES  #EXECUTIONS  CLOCK PERIODS
        LXI   H,0     ;CLEAR H,L PAIR             3        1           10
        MVI   D,0     ;CLEAR MSB OF DE            2        1            7
        ORA   A       ;TEST FOR 0                 1        1            4
        JZ    DONE                                3        1           10
LOOP:
        DAD   D       ;ADD DE TO                  1        M           10
        DCR   A       ;HL A TIMES                 1        M            5
        JNZ   LOOP                                3        M           10
DONE:
```

FIGURE 17-2 REPEATING ADDITION MULTIPLICATION PROGRAM

But some applications will require considerable more performance, which can be provided only by external hardware multiplication. The Am25LS14 Serial-Parallel Multiplier is well-suited for the needs of very high speed designs.

SUMMARY OF THE Am25LS14 DEVICE

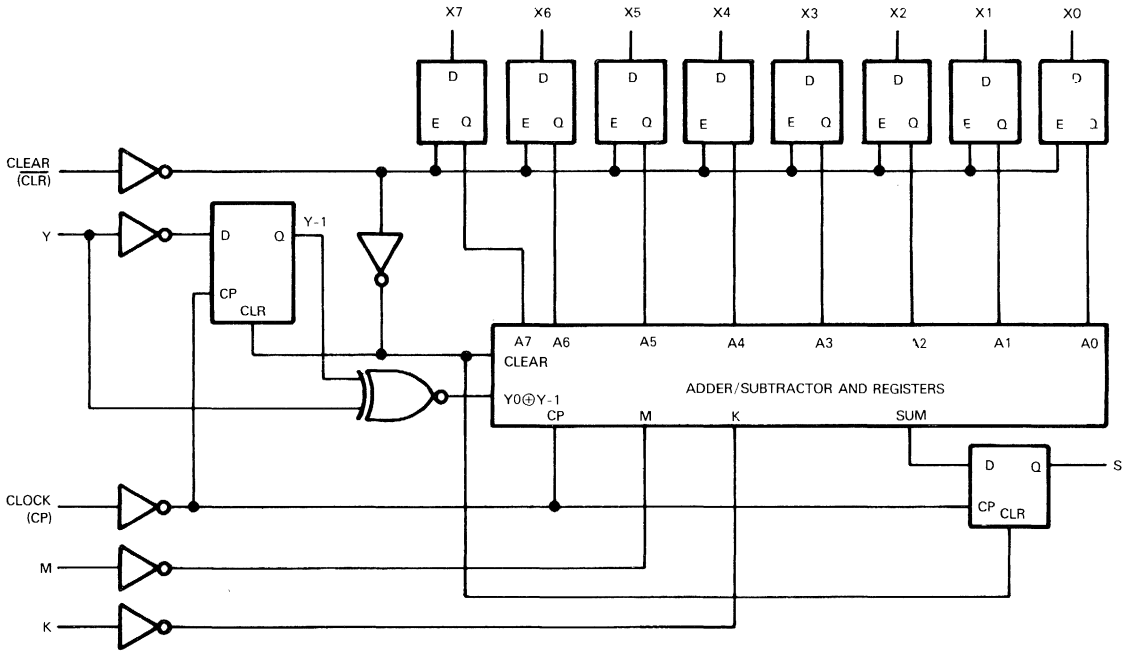
Conceptually the operation of the Am25LS14 device is quite straightforward. Consider the following very elementary multiplication:

```
    1 1 0 1   Multiplicand
  x 0 1 0 1   Multiplier
  ---------
    1 1 0 1 )
    0 0 0 0 )
  1 1 0 1 0 0 ) Partial Products
  0 0 0 0 0 0 0 )
  ---------
  1 0 0 0 0 0 1   Product
```

The Am25LS14 device illustrated in Figure 17-3 performs binary multiplications as illustrated above by applying a parallel multiplicand at the X input. The multiplier is applied serially to the Y input, least significant bit first. The product appears serially at the S output, least significant bit first.

The Am25LS14 handles 8-bit parallel multiplicands. Four-bit binary data has been illustrated above in order to keep the illustration simple.

Upon examining the binary multiplication illustrated above, it can be seen that if the low order bit of the multiplier is applied first, then the first line of the partial product will be created; the low order bit of this partial product may be output at the S pin since it plays no further part in generating the product result. When the next bit of the multiplier is input at Y, the second line of the partial product is created. Once again the second bit of the product may be output at S; it consists of



INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CP	K	M	Xi	Y	Y-1	S	
-	-	L	L	-	-	-	-	Most Significant Multiplier Device
-	-	CS	H	-	-	-	-	Devices Cascaded in Multiplier String
L	-	-	-	OP	-	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	-	-	-	-	-	-	-	Device Enabled
H	↑	-		-	L	L	AR	Shift Sum Register
H	↑	-	-	-	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	-	-	-	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	-	-	-	H	H	AR	Shift Sum Register

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device

OP = Xi latches open for new data (i = 0,7)
AR = Output as required per Booth's algorithm

FIGURE 17-3 Am25LS14 FUNCTIONAL LOGIC DIAGRAM

the low order bit of the partial product second line added to the retained lowest order bit of the first partial product line. In this fashion, multiplier bits may be applied at the Y inputs, one at a time, beginning with the low order bit; as each multiplier bit is applied an additional product bit is generated for output at the S pin.

The clock input to the multiplier device is used to time multiplication steps. With each clock pulse an additional bit of the multiplier must be input at Y and an additional bit of the product will be generated at S.

If the multiplicand is greater than eight bits wide, then multiplier devices can be cascaded together. All that is needed is for the S output of a high order device to be connected to the K input of the next low order device. The final product will be created at the S output of the lowest order device.

The multiplier device will also handle signed binary data. In this case a low input must be applied at the M pin of the multiplier device; in the event that more than one multiplier device has been cascaded together a low M input must be applied to the high order multiplier device only.

The clear input of the multiplier device must be input low preceding any multiplication. This low input clears all internal registers.

The operation of the Am25LS14 and Am25LS22 chips are described in detail in the AMD "Digital Signal Processing Handbook".

A SYSTEM CONFIGURATION

The logic diagram in Figure 17-4 shows how the hardware for an 8 X 8 multiply is organized. The basic operational sequence is:

1) The processor writes the two's complement multiplicand byte into the Am25LS14.
2) The processor writes the two's complement multiplier byte into one of the Am25LS22 shift registers.
3) The external hardware shifts the multiplier byte into the Am25LS14 and accumulates 16 bits of result in the two Am25LS22 registers.
4) When the operation is complete, the processor reads the least significant byte of the result from one Am25LS22.
5) The processor then reads the most significant byte of the result from the other Am25LS22.

The interface and control logic performs several important functions:

1) Decoding the read and write addresses.
2) Synchronizing control lines with the multiplier clock.
3) Generating appropriate control pulses for loading, initializing and reading the Am25LS14 and Am25LS22 chips.
4) Start, count and stop the clock pulse train to the multiplier chip.
5) Controlling the Sign Extend input on an Am25LS22.

The Select signal is derived from the processor Address Bus and will depend on how the I/O system is organized. The low order address line serves to select between the two address locations used by the multiplier.

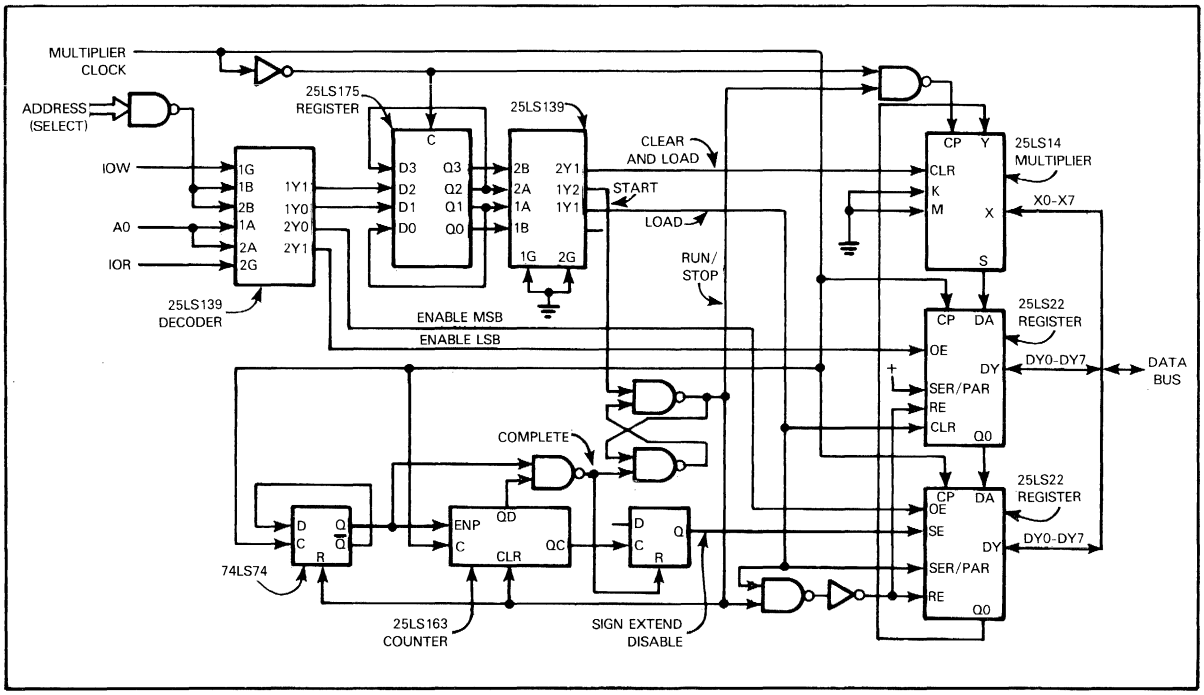


FIGURE 17-4 8-BIT X 8-BIT MULTIPLICATION USING THE Am25LS14 DEVICES

The multiplier clock can be any convenient clock signal up to a frequency of about 24 MHz. Φ2 (TTL) or OSC output from the Am8224 may be used. Where the frequency is too high, it may be simply divided by two with a flip-flop.

Total multiply times will include the times necessary for passing operands and results, and will vary depending on the application. The actual hardware execution time will be 17 times the multiplier clock period. With a 20 MHz clock, for example, multiplication will be complete in only 850 ns, easily within an instruction cycle for the processor. Thus, as far as the program is concerned, results are available for reading as soon as the last operand has been written. When the multiplier clock is too slow for this to be true, a NOP may be inserted in the program before results are retrieved.

Appendix A
INSTRUCTION SUMMARIES

This Appendix summarizes all of the instruction opcodes for convenient reference. Instructions are listed (I) by functional categories, (II) in ascending order of hex opcode value, and (III) alphabetically by standard mnemonic. The 8080A/9080A Instruction Description in Chapter 3 of this Handbook provides detailed descriptions of the operation of each processor instruction.

There are 256 possible combinations of the eight bits of the instruction opcode. Twelve are unassigned and should not be used. They are:

HEX	BINARY
08	00001000
10	00010000
18	00011000
20	00100000
28	00101000
30	00110000
38	00111000
CB	11001011
D9	11011001
DD	11011101
ED	11101101
FD	11111101

I 8080A/9080A INSTRUCTION SUMMARY BY FUNCTIONAL GROUPS

Data Transfer

HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC
40	MOV B,B	58	MOV E,B	70	MOV M,B	1A	LDAX D
41	MOV B,C	59	MOV E,C	71	MOV M,C	2A	LHLD
42	MOV B,D	5A	MOV E,D	72	MOV M,D	3A	LDA
43	MOV B,E	5B	MOV E,E	73	MOV M,E	02	STAX B
44	MOV B,H	5C	MOV E,H	74	MOV M,H	12	STAX D
45	MOV B,L	5D	MOV E,L	75	MOV M,L	22	SHLD
46	MOV B,M	5E	MOV E,M	77	MOV M,A	32	STA
47	MOV B,A	5F	MOV E,A	78	MOV A,B	01	LXI B
48	MOV C,B	60	MOV H,B	79	MOV A,C	11	LXI D
49	MOV C,C	61	MOV H,C	7A	MOV A,D	21	LXI H
4A	MOV C,D	62	MOV H,D	7B	MOV A,E	31	LXI SP
4B	MOV C,E	63	MOV H,E	7C	MOV A,H	F9	SPHL
4C	MOV C,H	64	MOV H,H	7D	MOV A,L	E3	XTHL
4D	MOV C,L	65	MOV H,L	7E	MOV A,M	EB	XCHG
4E	MOV C,M	66	MOV H,M	7F	MOV A,A	D3	OUT
4F	MOV C,A	67	MOV H,A	06	MVI B	DB	IN
50	MOV D,B	68	MOV L,B	0E	MVI C	C5	PUSH B
51	MOV D,C	69	MOV L,C	16	MVI D	D5	PUSH D
52	MOV D,D	6A	MOV L,D	1E	MVI E	E5	PUSH H
53	MOV D,E	6B	MOV L,E	26	MVI H	F5	PUSH PSW
54	MOV D,H	60	MOV L,H	2E	MVI L	C1	POP B
55	MOV D,L	6D	MOV L,L	36	MVI M	D1	POP D
56	MOV D,M	6E	MOV L,M	3E	MVI A	E1	POP H
57	MOV D,A	6F	MOV L,A	0A	LDAX B	F1	POP PSW

Arithmetic

HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC
80	ADD B	C6	ADI	9E	SBB M	3C	INR A
81	ADD C	CE	ACI	9F	SBB A	03	INX B
82	ADD D	90	SUB B	D6	SUI	13	INX D
83	ADD E	91	SUB C	DE	SBI	23	INX H
84	ADD H	92	SUB D	09	DAD B	33	INX SP
85	ADD L	93	SUB E	19	DAD D	05	DCR B
86	ADD M	94	SUB H	29	DAD H	0D	DCR C
87	ADD A	95	SUB L	39	DAD SP	15	DCR D
88	ADC B	96	SUB M	27	DAA	1D	DCR E
89	ADC C	97	SUB A	04	INR B	25	DCR H
8A	ADC D	98	SBB B	0C	INR C	2D	DCR L
8B	ADC E	99	SBB C	14	INR D	35	DCR M
8C	ADC H	9A	SBB D	1C	INR E	3D	DCR A
8D	ADC L	9B	SBB E	24	INR H	0B	DCX B
8E	ADC M	9C	SBB H	2C	INR L	1B	DCX D
8F	ADC A	9D	SBB L	34	INR M	2B	DCX H
						3B	DCX SP

Logical

HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC
A0	ANA B	A9	XRA C	B2	ORA D	BB	CMP E
A1	ANA C	AA	XRA D	B3	ORA E	BC	CMP H
A2	ANA D	AB	XRA E	B4	ORA H	BD	CMP L
A3	ANA E	AC	XRA H	B5	ORA L	BE	CMP M
A4	ANA H	AD	XRA L	B6	ORA M	BF	CMP A
A5	ANA L	AE	XRA M	B7	ORA A	FE	CPI
A6	ANA M	AF	XRA A	F6	ORI	07	RLC
A7	ANA A	EE	XRI	B8	CMP B	0F	RRC
E6	ANI	B0	ORA B	B9	CMP C	17	RAL
A8	XRA B	B1	ORA C	BA	CMP D	1F	RAR
						2F	CMA

Branching

HEX	MNEMONIC	HEX	MNEMONIC	HEX	MNEMONIC
C3	JMP	D7	RST 2	EC	CPE
C2	JNZ	DF	RST 3	F4	CP
CA	JZ	E7	RST 4	FC	CM
D2	JNC	EF	RST 5	C9	RET
DA	JC	F7	RST 6	C0	RNZ
E2	JPO	FF	RST 7	C8	RZ
EA	JPE	CD	CALL	D0	RNC
F2	JP	C4	CNZ	D8	RC
FA	JM	CC	CZ	E0	RPO
E9	PCHL	D4	CNC	E8	RPE
C7	RST 0	DC	CC	F0	RP
CF	RST 1	E4	CPO	F8	RM

Control

HEX	MNEMONIC
00	NOP
76	HLT
F3	DI
FB	EI
37	STC
3F	CMC

II 8080A/9080A INSTRUCTION SUMMARY
HEXADECIMAL ORDER

HEX	MNEMONIC
00	NOP
01	LXI B
02	STAX B
03	INX B
04	INR B
05	DCR B
06	MVI B
07	RLC
09	DAD B
0A	LDAX B
0B	DCX B
0C	INR C
0D	DCR C
0E	MVI C
0F	RRC
11	LXI D
12	STAX D
13	INX D
14	INR D
15	DCR D
16	MVI D
17	RAL
19	DAD D
1A	LDAX D
1B	DCX D
1C	INR E
1D	DCR E
1E	MVI E
1F	RAR
21	LXI H
22	SHLD
23	INX H
24	INR H
25	DCR H
26	MVI H
27	DAA
29	DAD H
2A	LHLD
2B	DCX H
2C	INR L
2D	DCR L
2E	MVI L
2F	CMA
31	LXI SP
32	STA
33	INX SP
34	INR M
35	DCR M
36	MVI M
37	STC
39	DAD SP
3A	LDA
3B	DCX SP
3C	INR A
3D	DCR A
3E	MVI A
3F	CMC
40	MOV B,B
41	MOV B,C
42	MOV B,D
43	MOV B,E
44	MOV B,H
45	MOV B,L
46	MOV B,M
47	MOV B,A
48	MOV C,B
49	MOV C,C
4A	MOV C,D
4B	MOV C,E
4C	MOV C,H
4D	MOV C,L
4E	MOV C,M
4F	MOV C,A
50	MOV D,B
51	MOV D,C
52	MOV D,D
53	MOV D,E
54	MOV D,H
55	MOV D,L
56	MOV D,M
57	MOV D,A
58	MOV E,B
59	MOV E,C
5A	MOV E,D
5B	MOV E,E
5C	MOV E,H
5D	MOV E,L
5E	MOV E,M
5F	MOV E,A
60	MOV H,B
61	MOV H,C
62	MOV H,D
63	MOV H,E
64	MOV H,H
65	MOV H,L
66	MOV H,M
67	MOV H,A
68	MOV L,B
69	MOV L,C
6A	MOV L,D
6B	MOV L,E
6C	MOV L,H
6D	MOV L,L
6E	MOV L,M
6F	MOV L,A
70	MOV M,B
71	MOV M,C
72	MOV M,D
73	MOV M,E
74	MOV M,H
75	MOV M,L
76	HLT
77	MOV M,A
78	MOV A,B
79	MOV A,C
7A	MOV A,D
7B	MOV A,E
7C	MOV A,H
7D	MOV A,L
7E	MOV A,M
7F	MOV A,A
80	ADD B
81	ADD C
82	ADD D
83	ADD E
84	ADD H
85	ADD L
86	ADD M
87	ADD A
88	ADC B
89	ADC C
8A	ADC D
8B	ADC E
8C	ADC H
8D	ADC L
8E	ADC M
8F	ADC A
90	SUB B
91	SUB C
92	SUB D
93	SUB E
94	SUB H
95	SUB L
96	SUB M
97	SUB A
98	SBB B
99	SBB C
9A	SBB D
9B	SBB E
9C	SBB H
9D	SBB L
9E	SBB M
9F	SBB A
A0	ANA B
A1	ANA C
A2	ANA D
A3	ANA E
A4	ANA H
A5	ANA L
A6	ANA M
A7	ANA A
A8	XRA B
A9	XRA C
AA	XRA D
AB	XRA E
AC	XRA H
AD	XRA L
AE	XRA M
AF	XRA A
B0	ORA B
B1	ORA C
B2	ORA D
B3	ORA E
B4	ORA H
B5	ORA L
B6	ORA M
B7	ORA A
B8	CMP B
B9	CMP C
BA	CMP D
BB	CMP E
BC	CMP H
BD	CMP L
BE	CMP M
BF	CMP A
C0	RNZ
C1	POP B
C2	JNZ
C3	JMP
C4	CNZ
C5	PUSH B
C6	ADI
C7	RST 0
C8	RZ
C9	RET
CA	JZ
CC	CZ
CD	CALL
CE	ACI
CF	RST 1
D0	RNC
D1	POP D
D2	JNC
D3	OUT
D4	CNC
D5	PUSH D
D6	SUI
D7	RST 2
D8	RC
DA	JC
DB	IN
DC	CC
DE	SBI
DF	RST 3
E0	RPO
E1	POP H
E2	JPO
E3	XTHL
E4	CPO
E5	PUSH H
E6	ANI
E7	RST 4
E8	RPE
E9	PCHL
EA	JPE
EB	XCHG
EC	CPE
EE	XRI
EF	RST 5
F0	RP
F1	POP PSW
F2	JP
F3	DI
F4	CP
F5	PUSH PSW
F6	ORI
F7	RST 6
F8	RM
F9	SPHL
FA	JM
FB	EI
FC	CM
FE	CPI
FF	RST 7

III 8080A/9080A INSTRUCTION SUMMARY
ALPHABETICAL ORDER

HEX	MNEMONIC	
CE	ACI	
8F	ADC	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
87	ADD	A
80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
C6	ADI	
A7	ANA	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
E6	ANI	
CD	CALL	
DC	CC	
FC	CM	
2F	CMA	
3F	CMC	
BF	CMP	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
D4	CNC	
C4	CNZ	
F4	CP	
EC	CPE	
FE	CPI	
E4	CPO	
CC	CZ	
27	DAA	
09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP
3D	DCR	A
05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP
F3	DI	
FB	EI	
76	HLT	
DB	IN	
3C	INR	A
04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
03	INX	B
13	INX	D
23	INX	H
33	INX	SP
DA	JC	
FA	JM	
C3	JMP	
D2	JNC	
C2	JNZ	
F2	JP	
EA	JPE	
E2	JPO	
CA	JZ	
3A	LDA	
0A	LDAX	B
1A	LDAX	D
2A	LHLD	
01	LXI	B
11	LXI	D
21	LXI	H
31	LXI	SP
7F	MOV	A,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
47	MOV	B,A
40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
4F	MOV	C,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
57	MOV	D,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
5F	MOV	E,A
58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
67	MOV	H,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
6F	MOV	L,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
77	MOV	M,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L
3E	MVI	A
06	MVI	B
0E	MVI	C
16	MVI	D
1E	MVI	E
26	MVI	H
2E	MVI	L
36	MVI	M
00	NOP	
B7	ORA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
F6	ORI	
D3	OUT	
E9	PCHL	
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW
C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
17	RAL	
1F	RAR	
D8	RC	
C9	RET	
07	RLC	
F8	RM	
D0	RNC	
C0	RNZ	
F0	RP	
E8	RPE	
E0	RPO	
0F	RRC	
C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7
C8	RZ	
9F	SBB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
DE	SBI	
22	SHLD	
F9	SPHL	
32	STA	
02	STAX	B
12	STAX	D
37	STC	
97	SUB	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
D6	SUI	
EB	XCHG	
AF	XRA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
EE	XRI	
E3	XTHL	

Appendix B
ASCII CODE TABLE

ANSI X3.4 1968 VERSION

HEX CODE	ASCII CHARACTER	HEX CODE	ASCII CHARACTER	HEX CODE	ASCII CHARACTER
00	NUL	2B	+	56	V
01	SOH	2C	,	57	W
02	STX	2D	-	58	X
03	ETX	2E	.	59	Y
04	EOT	2F	/	5A	Z
05	ENQ	30	0	5B	[
06	ACK	31	1	5C	\
07	BEL	32	2	5D	]
08	BS	33	3	5E	^
09	HT	34	4	5F	_
0A	LF	35	5	60	`
0B	VT	36	6	61	a
0C	FF	37	7	62	b
0D	CR	38	8	63	c
0E	SO	39	9	64	d
0F	SI	3A	:	65	e
10	DLE	3B	;	66	f
11	DC1	3C	<	67	g
12	DC2	3D	=	68	h
13	DC3	3E	>	69	i
14	DC4	3F	?	6A	j
15	NAK	40	@	6B	k
16	SYN	41	A	6C	l
17	ETB	42	B	6D	m
18	CAN	43	C	6E	n
19	EM	44	D	6F	o
1A	SUB	45	E	70	p
1B	ESC	46	F	71	q
1C	FS	47	G	72	r
1D	GS	48	H	73	s
1E	RS	49	I	74	t
1F	US	4A	J	75	u
20	SP	4B	K	76	v
21	!	4C	L	77	w
22	"	4D	M	78	x
23	#	4E	N	79	y
24	$	4F	O	7A	z
25	%	50	P	7B	{
26	&	51	Q	7C	|
27	'	52	R	7D	}
28	(	53	S	7E	~
29	)	54	T	7F	DEL
2A	*	55	U		

Appendix C
AMD TECHNICAL PUBLICATIONS

There is a continuing flow of technical information available from Advanced Micro Devices. In addition to this 8080A/9080A Handbook, the following major publicatons are available at press time:

1. Bipolar Memory, Logic and Interface catalog
2. Bipolar Logic catalog supplement
3. Am2900 Bipolar Microprocessor Family
4. Am2900 Design for a 16-bit Minicomputer
5. Am2914 Priority Interrupt
6. Microprogramming Handbook
7. Digital Signal Processing Handbook
8. Linear Catalog
9. MOS/LSI Catalog