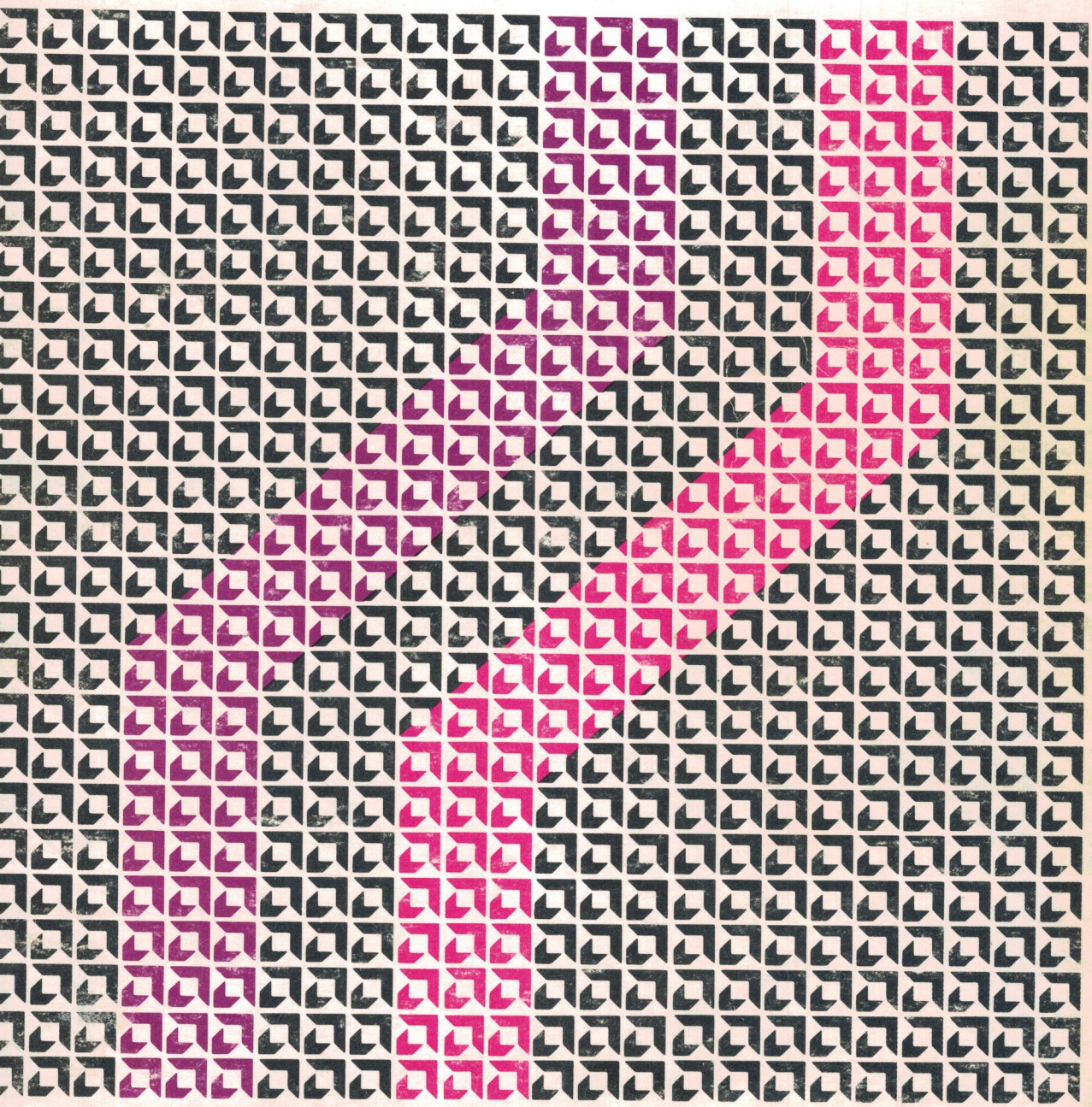
# Advanced Micro Devices, Inc.

# Schottky And Low-Power Schottky Data Book



# Advanced Micro Devices

# Schottky and Low-power Schottky Data Book Including Digital Signal Processing Handbook

Second Edition

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## LOW-POWER SCHOTTKY MSI/LSI AND INTERFACE PRODUCTS

# SCHOTTKY AND LOW-POWER SCHOTTKY FUNCTIONAL SELECTOR GUIDE

This guide divides the AMD Low-Power Schottky and Schottky TTL Product Line by function into three basic performance categories indicated by the examples below.

1. High-Performance, Low-Power Schottky Ex. 25LS174 Six Bit Register. $f_{max}$ = 40MHz (Min.)
2. Standard Low-Power Schottky Ex. 74LS174 Six Bit Register. $f_{max}$ = 30MHz (Min.)
3. High-Speed Schottky Ex. 74S174 Six Bit Register. $f_{max}$ = 75MHz (Min.)



| DESCRIPTION | HIGH-PERFORMANCE LOW-POWER SCHOTTKY | STANDARD LOW-POWER SCHOTTKY | HIGH-SPEED SCHOTTKY |
|---|---|---|---|
| **DECADE (BCD) COUNTERS** | | | |
| Asynchronous Clear, Synchronous Preset | 25LS160A | 54/74LS160A | 54/74S160/93S10 |
| Synchronous Clear, Synchronous Preset | 25LS162A | 54/74LS162A | |
| Up-Down, Synchronous Preset | 25LS168A | 54/74LS168A | |
| Up-Down, Asynchronous Preset, Single Clock | 25LS190 | 54/74LS190 | |
| Up-Down, Asynchronous Preset, Dual Clock | 25LS192 | 54/74LS192 | |
| Up-Down, Synchronous Preset, Three-State | 25LS2568 | | |
| **BINARY HEXADECIMAL COUNTERS** | | | |
| Asynchronous Clear, Synchronous Preset | 25LS161A | 54/74LS161A | 54/74S161/93S16 |
| Synchronous Clear, Synchronous Preset | 25LS163A | 54/74LS163A | |
| Up-Down, Synchronous Preset | 25LS169A | 54/74LS169A | |
| Up-Down, Asynchronous Preset, Single Clock | 25LS191 | 54/74LS191 | |
| Up-Down, Asynchronous Preset, Dual Clock | 25LS193 | 54/74LS193 | |
| Up-Down, Synchronous Preset, Three-State | 25LS2569 | | |
| **DECODER/DEMULTIPLEXERS** | | | |
| One-of-Ten Decoder/Demultiplexer, Polarity Control | 25LS2537 | | |
| One-of-Eight Decoder/Demultiplexer | 25LS138 | 54/74LS138 | 54/74S138 |
| One-of-Eight Decoder/Demultiplexer with Control Storage | 25LS2536 | | |
| Dual One-of-Four Decoder/Demultiplexer | 25LS139 | 54/74LS139 | 54/74S139/93S21 |
| One-of-Eight Decoder/Demultiplexer, Polarity Control | 25LS2538 | | |
| Dual One-of-Four Decoder/Demultiplexer, Polarity Control | 25LS2539 | | |
| **MULTIPLEXERS** | | | |
| Eight-Input Multiplexer | 25LS151 | 54/74LS151 | 54/74S151 |
| Eight-Input Multiplexer with Control Storage | 25LS2535 | | |
| Three-State Eight-Input Multiplexer | 25LS251 | 54/74LS251 | 54/74S251 |
| Dual Four-Input Multiplexer | 25LS153 | 54/74LS153 | 54/74S153 |
| Three-State Dual Four-Input Multiplexer | 25LS253 | 54/74LS253 | 54/74S253 |
| Quad Two-Input Multiplexer; Non-Inverting | 25LS157 | 54/74LS157 | 54/74S157/93S22 |
| Three-State Quad Two-Input Multiplexer; Non-Inverting | 25LS257 | 54/74LS257 | 54/74S257 |
| Quad Two-Input Multiplexer; Inverting | 25LS158 | 54/74LS158 | 54/74S158 |
| Three-State Quad Two-Input Multiplexer; Inverting | 25LS258 | 54/74LS258 | 54/74S258 |
| **MONOSTABLE (ONE-SHOT)** | | | |
| Dual Retriggerable, Resettable Monostable Multivibrator | | | 26S02 |
| **OPERATORS (ALU, MULTIPLIER, PRIORITY ENCODER, etc.)** | | | |
| Four by Two Two's Complement Multiplier | | | 25S05 |
| Four-Bit, Four-Way Shifter | | | 25S10/54/74S350 |
| Four-Bit ALU/Function Generator | 25LS181 | 54/74LS181 | 54/74S181 |
| Four-Bit ALU/Function Generator | 25LS2517 | | |
| Four-Bit ALU/Function Generator | 25LS381 | 54/74LS381 | |
| Four-Bit Parallel Accumulator | 25LS281 | 54/74LS281 | |
| Priority Encoder, Eight Line to Three Line | 25LS148 | 54/74LS148 | |
| Four-Bit Serial Adder/Subtractor | 25LS15 | | |
| Priority Encoder, Three State | 25LS2513 | | |
| Eight by One Serial/Parallel Two's Complement Multiplier | 25LS14 | | |
| Eight-Bit by Eight-Bit Multiplier/Accumulator | 25LS2516 | | |
| Eight-Bit Comparator | 25LS2521 | | |
| Eight-Bit Registered Comparator | 25LS2524 | | |
| System Clock Generator and Driver | 25LS2525 | | |

## FUNCTIONAL SELECTOR GUIDE (Cont.)

| DESCRIPTION | HIGH-PERFORMANCE LOW-POWER SCHOTTKY | STANDARD LOW-POWER SCHOTTKY | HIGH-SPEED SCHOTTKY |
|---|---|---|---|
| **PARITY CHECKER/GENERATORS** | | | |
| Nine-Input Parity Checker/Generator | | | 82S62 |
| Twelve-Input Parity Checker/Generator | | | 93S48 |
| **REGISTERS** | | | |
| Four-Bit Register with Common Clock Enable | 25LS08 | 54/74LS379 | 25S08/54/74S379 |
| Four-Bit Register with Two-Input Multiplexers on Inputs | 25LS09 | 54/74LS399 | 25S09/54/74S388 |
| Four-Bit Register with Standard and Three-State Outputs | 25LS2518 | | 25S18/54/74S388 |
| Four-Bit, Two-Output Three-State Register | 25LS2519 | | |
| Four-Bit Register with Common Clear | 25LS175 | 54/74LS175 | 54/74S175 |
| Four-Bit Register; Shift Right, Left or Parallel Load | 25LS194A | 54/74LS194A | 54/74S194 |
| Four-Bit Register; Shift Right or Parallel Load | 25LS195A | 54/74LS195A | 54/74S195 |
| Six-Bit Register with Common Clock Enable | 25LS07 | 54/74LS378 | 25S07/54/74S378 |
| Six-Bit Register with Common Clear | 25LS174 | 54/74LS174 | 54/74S174 |
| Eight-Bit, Serial-In, Parallel-Out Register | 25LS164 | 54/74LS164 | |
| Eight-Bit Shift/Storage Register; Synchronous Clear | 25LS23 | | |
| Eight-Bit Shift/Storage Register; Asynchronous Clear | 25LS299 | 54/74LS299 | |
| Eight-Bit Shift-Storage Register with Sign Extend | 25LS22 | | |
| Octal D-Type Register, Common Clear | 25LS273B | 54/74LS273B | |
| Octal Transparent Latch (Three State, non-inverting) | 25LS373 | 54/74LS373 | *54/74S373 |
| Octal Transparent Latch (Three-state, inverting) | *25LS533 | *54/74LS533 | *54/74S533 |
| Octal D-Type Register (Three State, non-inverting) | 25LS374 | 54/74LS374 | *54/74S374 |
| Octal D-Type Register (Three-state, inverting) | *25LS534 | *54/74LS534 | *54/74S534 |
| Octal D-Type Register, Common Enable | 25LS377B | 54/74LS377B | |
| Octal D-Type Register, Common Enable and Clear, Three-State | 25LS2520 | | |
| **BUS INTERFACE** | | | |
| Quad Bus Transceiver, Inverting (100mA) | | | 26S10 |
| Quad Bus Transceiver, Non-Inverting (100mA) | | | 26S11 |
| Quad Bus Transceiver, Inverting | 25LS242 | 54/74LS242 | 54/74S242 |
| Quad Bus Transceiver, Non-Inverting | 25LS243 | 54/74LS243 | 54/74S243 |
| Quad Open-Collector Bus Transceiver | | | 26S12/12A |
| Quad Three-State Bus Transceiver (Inverting) | | | 8TS12/12A |
| Quad Three-State Bus Transceiver (Non-Inverting) | | | 8T28 |
| Quad Two I/P Transceiver with Three-State Receiver (O.C.) | 2905 | | |
| Quad Two I/P Transceiver with Parity (O.C.) | 2906 | | |
| Quad Two I/P Transceiver with Parity (O.C.) | 2907 | | |
| Quad Two I/P Transceiver with Three-State Receiver (Three-State) | 2915A | | |
| Quad Two I/P Transceiver with Parity (Three-State) | 2916A | | |
| Quad Two I/P Transceiver with Parity (Three-State) | 2917A | | |
| Octal Bus Driver, Inverting | 25LS240 | 54/74LS240 | 54/74S240 |
| Octal Bus Driver, Non-Inverting (Complementary G, G inputs) | 25LS241 | 54/74LS241 | 54/74S241 |
| Octal Bus Driver, Non-Inverting | 25LS244 | 54/74LS244 | 54/74S244 |
| Octal Bus Driver, Low-Power. | 71/81LS95 | | |
| Octal Bus Driver, Low-Power, Inv. | 71/81LS96 | | |
| Octal Bus Driver, Low-Power. | 71/81LS97 | | |
| Octal Bus Driver, Low-Power, Inv. | 71/81LS98 | | |
| Octal Bidirectional Bus Transceiver | 8304 | | |

*In development.

# Introduction to Low-Power Schottky

# ADVANCED MICRO DEVICES
# SCHOTTKY AND LOW-POWER SCHOTTKY MSI

Advanced Micro Devices offers a complete line of Schottky and Low-Power Schottky MSI products. On the following pages are a selector guide for these products and brief data on several of the most useful parts. For complete data refer to our Schottky and Low-Power Schottky Data Book.

Advanced Micro Devices offers two LS Logic families.

- Am25LS – High Performance
- Am54/74LS – Standard Performance

Similar elements of both families are described on the same data sheet. Key parameters are compared below.

All Advanced Micro Devices' products are manufactured to the quality assurance requirements of MIL-STD-883, Level C. According to Handbook 217B published by the Rome Air Development Center, the Air Force's principal authority on component reliability, Level C integrated circuits are up to ten times more reliable than normal industry commercial parts.

10X MORE RELIABLE

Even if you don't need the performance features of Am25LS, you can buy our versions of 54/74LS devices with the assurance that they are manufactured to the stringent quality standards of MIL-STD-883.

50mV MORE NOISE MARGIN

## Am25LS IMPROVED PERFORMANCE

- Noise Margin
  At $I_{OL}$ = 8mA, Am25LS guarantees $V_{OL}$ = 0.45V compared to 0.50V for 54/74LS.
- Fan Out
  Over the military temperature range, Am25LS is specified at $I_{OL}$ = 8mA, for a F.O. of 22 (8mA/0.36mA). 54LS is guaranteed at $I_{OL}$ = 4mA only, for F.O. = 11 (4mA/0.36mA).
- $I_{SC}$ (Max.)
  Am25LS has $I_{SC}$ upper limit controlled to 85mA (Max.).
- Speed
  In this example, Am25LS164 has worst case clock to output delay specified at up to 45% faster and $f_{MAX}$ at more than 40% faster than 54/74LS164: Most Am25LS devices offer similar improvements.

TWICE THE FAN-OUT

REDUCED SUPPLY CURRENT SPIKING

FASTER

## SWITCHING SPEED SPECIFIED AT TEMPERATURE AND POWER SUPPLY EXTREMES

The switching speeds of all new Am25LS devices are now being specified at:

- Full 50pF load
- Over the operating temperature range
  - Military –55°C to +125°C
  - Commercial 0°C to +70°C
- Over the operating power supply range
  - Military 5.0V ± 10%
  - Commercial 5.0V ± 5%

MORE FULLY SPECIFIED

## PRICE

Most Am25LS device list prices are the same or less than the equivalent 54/74LS standard performance device.

# Am25LS164 • Am54LS/74LS164

**8-Bit Serial-In, Parallel-Out Shift Register**

## DISTINCTIVE CHARACTERISTICS

- Gated serial inputs
- Asynchronous clear
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440µA source current at HIGH output
- 100% product assurance testing to MIL-STD-883 requirements

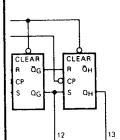
## FUNCTIONAL DESCRIPTION

The Am25LS164 and Am54LS/74LS164 are eight-bit, serial in/parallel out shift registers built using advanced Low-Power Schottky processing. A gated input provides enable/disable control over incoming data such that the data can be entered or logic zeros can be entered into the register.

An asynchronous clear input can be used to simultaneously clear the eight flip-flops in the device. When the clear input is LOW, all internal flip-flops are forced LOW independent of the clock input. An incoming data bit is entered into the $Q_a$ flip-flop and the data in all internal flip-flops is shifted right on the LOW-to-HIGH transition of the clock input.

The Am54LS/74LS164 is a standard performance version of the Am25LS164. See appropriate electrical characteristic tables for detailed Am25LS improvements.

## LOGIC DIAGRAM




## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

## DC CHARACTERISTICS OVER OPERATING RANGE

**Am25LS164**

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440µA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | 0.25 | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | Clock, Clear | | | −0.36 | mA |
| | | | A, B | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | | | | | | |

Notes: 1. For conditions shown as MIN. or MAX
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C
3. Not more than one output should be sh
4. Measured with outputs open, serial inp

**Am54LS/74LS164**

MAX. = 5.25V
MAX. = 5.50V

| ditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|
| 400µA | MIL | 2.5 | 3.4 | | Volts |
| | COM'L | 2.7 | 3.4 | | |
| All, $I_{OL}$ = 4.0mA | | | 0.25 | 0.4 | Volts |
| 74LS only, $I_{OL}$ = 8.0mA | | | 0.35 | 0.5 | |
| ical HIGH | | 2.0 | | | Volts |
| | | | | 0.7 | Volts |
| | | | | 0.8 | |
| | | | | −1.5 | Volts |
| | | | | −0.4 | mA |
| | | | | 20 | µA |
| | | | | 0.1 | mA |
| | | | | −100 | mA |
| | | | | 27 | mA |

cable device type.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 14 | 20 | | 17 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 16 | 22 | | 20 | 32 | ns | |
| $t_{PHL}$ | Clear to Output | | 19 | 29 | | 24 | 36 | ns | |
| $t_{pw}$ | Clock or Clear | 17 | | | 20 | | | ns | |
| $t_s$ | Data | 10 | | | 15 | | | ns | |
| $t_h$ | Data | 5.0 | | | 5.0 | | | ns | |
| $t_s$ | Clear Recovery Time | 20 | | | – | – | | ns | |
| $f_{max}$ | Maximum Clock Frequency | 35 | 42 | | 25 | 36 | | MHz | |

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 26 | | 30 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 30 | | 35 | ns | |
| $t_{PHL}$ | Clear to Output | | 30 | | 42 | ns | |
| $t_{pw}$ | Clock or Clear | 22 | | 25 | | ns | |
| $t_s$ | Data | 13 | | 15 | | ns | |
| $t_h$ | Data | 5 | | 5 | | ns | |
| $t_s$ | Clear Recovery Time | 25 | | 30 | | ns | |
| $f_{max}$ | Maximum Clock Frequency | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS•Am54LS/74LS CROSS REFERENCE GUIDE

Advanced Micro Devices offers both Am25LS, High Performance, and 54LS/74LS Standard Performance, low-power Schottky families. Am25LS devices may be substituted for 54LS/74LS devices as shown in the table below.

Products with different numbers corresponding to the similar Am25LS and 54LS/74LS functions are Texas Instruments second source part numbers to Advanced Micro Devices products.

| Am25LS HIGH PERFORMANCE LS | Am54/74LS STANDARD LS | DESCRIPTION | PACKAGE PINS |
|---|---|---|---|
| AM25LS07 | AM54/74LS378 | Six-Bit Register; Common Enable | 16 |
| AM25LS08 | AM54/74LS379 | Four-Bit Register; Common Enable | 16 |
| AM25LS09 | AM54/74LS399 | Four-Bit Register; Multiplexed Inputs | 16 |
| AM25LS14 | AM54/74LS384 | Eight-Bit Serial/Parallel Two's Complement Multiplier | 16 |
| AM25LS15 | AM54/74LS385 | Four-Bit Serial/Parallel Adder Subtracter | 20 |
| AM25LS22 | AM54/74LS322 | Eight-Bit Serial/Parallel Register; Sign Extend | 20 |
| AM25LS23 | AM54/74LS323 | Eight-Bit Universal Shift Register; Synchronous Clear | 20 |
| AM25LS138 | AM54/74LS138 | One-of-Eight Decoder/Demultiplexer | 16 |
| AM25LS139 | AM54/74LS139 | Dual One-of-Four Decoder/Demultiplexer | 16 |
| AM25LS148 | AM54/74LS148 | Priority Encoder; Eight-Line to Three-Line | 16 |
| AM25LS151 | AM54/74LS151 | Eight-Input Multiplexer | 16 |
| AM25LS153 | AM54/74LS153 | Dual-Four-Input Multiplexer | 16 |
| AM25LS157 | AM54/74LS157 | Quad Two-Input Multiplexer; Non-Inverting | 16 |
| AM25LS158 | AM54/74LS158 | Quad Two-Input Multiplexer; Inverting | 16 |
| AM25LS160A | AM54/74LS160A | Synchronous BCD Decade Counter; Asynchronous Clear | 16 |
| AM25LS161A | AM54/74LS161A | Synchronous Four-Bit Binary Counter; Asynchronous Clear | 16 |
| AM25LS162A | AM54/74LS162A | Synchronous BCD Decade Counter; Synchronous Clear | 16 |
| AM25LS163A | AM54/74LS163A | Synchronous Four-Bit Binary Counter; Synchronous Clear | 16 |
| AM25LS164 | AM54/74LS164 | Eight-Bit Serial-In, Parallel-Out Shift Register | 14 |
| AM25LS168A | AM54/74LS168A | Synchronous BCD Decade Up-Down Counter; Programmable | 16 |
| AM25LS169A | AM54/74LS169A | Synchronous Four-Bit Binary Up-Down Counter; Programmable | 16 |
| AM25LS174 | AM54/74LS174 | Six-Bit Register; Common Clear | 16 |
| AM25LS175 | AM54/74LS175 | Quad Register; Common Clear | 16 |
| AM25LS181 | AM54/74LS181 | Four-Bit ALU/Function Generator | 24 |
| AM25LS190 | AM54/74LS190 | BCD Decade Up-Down Counter; Down-Up Mode Control | 16 |
| AM25LS191 | AM54/74LS191 | Four-Bit Binary Up-Down Counter; Down-Up Mode Control | 16 |
| AM25LS192 | AM54/74LS192 | BCD Decade Up-Down Counter; Dual Clocks | 16 |
| AM25LS193 | AM54/74LS193 | Four-Bit Binary Up-Down Counter; Dual Clocks | 16 |
| AM25LS194A | AM54/74LS194A | Four-Bit Register; Shift Right, Left or Parallel Load | 16 |
| AM25LS195A | AM54/74LS195A | Four-Bit Register; Shift Right or Parallel Load | 16 |
| AM25LS240 | AM54/74LS240 | Octal Bus Driver; Inverting, Three State Outputs | 20 |
| AM25LS241 | AM54/74LS241 | Octal Bus Driver; Non-Inverting, Three State Outputs (G, G inputs) | 20 |
| AM25LS242 | AM54/74LS242 | Quad Bus Transceiver; Inverting | 14 |
| AM25LS243 | AM54/74LS243 | Quad Bus Transceiver; Non-Inverting | 14 |
| AM25LS244 | AM54/74LS244 | Octal Bus Driver; Non-Inverting, Three State Outputs | 20 |
| AM25LS251 | AM54/74LS251 | Eight-Input Multiplexer; Three State Outputs | 16 |
| AM25LS253 | AM54/74LS253 | Dual Four-Input Multiplexer; Three State Outputs | 16 |
| AM25LS257 | AM54/74LS257 | Quad Two-Input Multiplexer; Non-Inverting, Three State Outputs | 16 |
| AM25LS258 | AM54/74LS258 | Quad Two-Input Multiplexer; Inverting, Three State Outputs | 16 |
| AM25LS273 | AM54/74LS273 | Octal D-Register; Common Clear | 20 |
| *AM25LS281 | *AM54/74LS281 | Four-Bit Parallel Accumulator | 24 |
| AM25LS299 | AM54/74LS299 | Eight-Bit Universal Shift Register, Asynchronous Clear | 20 |
| – | AM54/74LS322 | See Am25LS22 | 20 |
| – | AM54/74LS323 | See Am25LS23 | 20 |
| AM25LS373 | AM54/74LS373 | Octal Transparent Latch; Three State Outputs | 20 |
| AM25LS374 | AM54/74LS374 | Octal D-Register; Three State Outputs | 20 |
| AM25LS377 | AM54/74LS377 | Octal D-Register; Common Enable | 20 |
| AM25LS378 | AM54/74LS378 | Six-Bit Register, Common Enable (25LS07) | 16 |
| AM25LS379 | AM54/74LS379 | Four-Bit Register, Common Enable (25LS08) | 16 |
| AM25LS381 | AM54/74LS381 | Four-Bit ALU/Function Generator (20 pin 25LS181) | 20 |

*In development.

## Am25LS•Am54LS/74LS CROSS REFERENCE GUIDE (Cont.)

| Am25LS HIGH PERFORMANCE LS | Am54/74LS STANDARD LS | DESCRIPTION | PACKAGE PINS |
|---|---|---|---|
| – | AM54/74LS382 | See Am25LS2517 | 20 |
| – | AM54/74LS384 | See Am25LS14 | 16 |
| – | AM54/74LS385 | See Am25LS15 | 20 |
| – | AM54/74LS388 | See Am25LS2518 | 16 |
| AM25LS399 | AM54/74LS399 | Four-Bit Register, Multiplexed Inputs (25LS09) | 16 |
| – | *AM54/74LS533 | Inverting version of Am25/54/74LS373 | 20 |
| – | *AM54/74LS534 | Inverting version of Am25/54/74LS374 | 20 |
| – | AM54/74LS568 | See Am25LS2568 | 20 |
| – | AM54/74LS569 | See Am25LS2569 | 20 |
| – | AM54/74LS668 | Slow Version of Am25/54/74LS168A | 16 |
| – | AM54/74LS669 | Slow Version of Am25/54/74LS169A | 16 |
| AM25LS2513 | – | Priority Encoder; Three State Outputs, Eight-Line to Three-Line | 20 |
| AM25LS2516 | – | Eight-Bit by Eight-Bit Serial/Parallel Multiplier/Accumulator | 40 |
| AM25LS2517 | – | Four-Bit ALU/Function Generator; Overflow Detection | 20 |
| AM25LS2518 | AM54/74LS388 | Quad Register with Standard and Three State Outputs | 16 |
| AM25LS2519 | – | Quad Register with Dual Three State Outputs | 20 |
| AM25LS2520 | – | Octal D-Register; Common Clear and Enable, Three State Outputs | 22 |
| AM25LS2521 | – | Eight-Bit Comparator | 20 |
| *AM25LS2524 | – | Registered Comparator | 20 |
| *AM25LS2525 | – | System Clock Generator and Driver | 20 |
| AM25LS2535 | – | Eight-Bit Multiplexer; Control Storage | 20 |
| AM25LS2536 | – | Eight-Bit Decoder; Control Storage | 20 |
| AM25LS2537 | – | One-of-Ten Decoder; Three State Outputs | 20 |
| AM25LS2538 | – | One-of-Eight Decoder; Three State Outputs | 20 |
| AM25LS2539 | – | Dual One-of-Four Decoder; Three State Outputs | 20 |
| AM25LS2568 | – | BCD Decade Up-Down Counter; Three State Outputs | 20 |
| AM25LS2569 | – | Four-Bit Binary Up-Down Counter; Three State Outputs | 20 |

*In development.

# DESIGNER'S GUIDE TO HIGH PERFORMANCE LOW-POWER SCHOTTKY LOGIC

By David A. Laws and Roy J. Levy.

## 1.

### THE NEW STANDARD LOGIC

Low-power Schottky TTL integrated circuits are now firmly established as the standard logic configuration for new high performance system designs. They have essentially entirely replaced standard "gold-doped" TTL devices in all applications. In addition, they have relegated the other logic families to specialized needs where the ultimate in high speed (ECL) or low power for battery operated operation (CMOS) is mandatory.

This wide acceptance has been achieved because LS offered all of the important features of the earlier TTL families with two significant advantages:

- LS circuits provide performance equal to that of standard TTL at between 20% and 50% of the power requirements. As a result, considerable system cost savings have been made in bulky power supplies and fans.
- LS technology allows more complex designs to be fabricated on a given die size. A far wider selection of systems oriented MSI and LSI functions have therefore been developed in the LS family.

Additional factors in their popularity is that the devices are implemented with the same technology, and are therefore totally compatible with the LSI bit-slice processors and supporting memories which today form the heart of most new high speed designs. Users of LS devices have been able to exploit these features to improve the performance and enhance the functional capability of their systems. In many cases this has been achieved at a lower total cost.

Advanced Micro Devices is a leading supplier of low-power Schottky MSI and LSI devices. Two basic families of product are offered:

AM54/74LS Series

- Typical tpd 10ns/gate at 2mW
- Typical Register fmax = 40MHz

Pin for pin and electrical alternate source devices to the standard performance LS logic family.

AM25LS Series

- Typical tpd 5ns/gate at 2mW
- Typical Register fmax = 65MHz

Advanced Micro Devices' proprietary high performance LS logic family. This includes both original designs and enhanced specification versions of the AM54/74LS devices. Improvements include twice the fan-out over the military temperature range, higher noise margin and faster switching speeds.

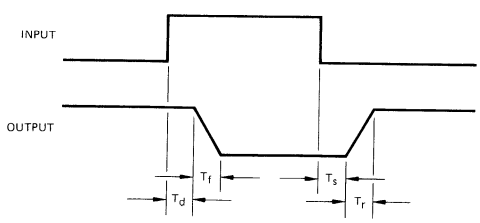
The AM25LS improved performance devices are offered by Raytheon Semiconductor and identified by 25LS part numbers. Equivalent Fairchild and Motorola 9LS functions will come close to meeting AM25LS switching speeds on certain products.

The AM25LS proprietary designs have been carefully chosen to improve operation and reduce the cost of building high performance digital systems. A good example is the set of AM25LS14, 15 and 22 digital signal processing elements. Fairchild, Motorola and Texas Instruments have announced plans to alternate source many of the new Advanced Micro Devices' designs.

Both the Am25LS and the Am54LS/74LS families can be freely intermixed. Together with the Am2900 series of bipolar microprocessor functions they will satisfy most of the design requirements of today's advanced systems.

### THE SCHOTTKY DIODE STRUCTURE

The major components of switching delays in digital integrated circuits are listed in Figure 1. One of the most significant of these is the storage time constant of a transistor driven into saturation Ts. Standard TTL circuits minimize this parameter with a process technique known as gold doping. This increases the rate of recombination of charge stored in the base region.




| PARAMETERS | DETERMINING FACTORS |
|---|---|
| $T_d$ | R, C |
| $T_f$ | $\beta$, Cob, Base Drive, Signal Amplitude |
| $T_s$ | Storage Time Constant of a Saturated Transistor |
| $T_r$ | Cob, Signal Amplitude |

**Figure 1. Major Causes of Propagation Delay.**

The desired result of improved speed is achieved. Unfortunately it also reduces available design $\beta$ at low temperatures and is marginally effective when hot. This results in lowered performance over the full military temperature range.

The development of the Schottky diode provides a more effective solution. A feature of the Schottky diode is its lower forward voltage at a given current level compared to a diffused (P-N) diode of the same area, Figure 2. Connecting a Schottky diode between the base and collector of a transistor, Figure 3, will shunt excess base current drive from the base to the collector, once the collector drops to a low enough voltage to forward bias the Schottky. This prevents the build up of stored charge and eliminates the Ts component of the delay.

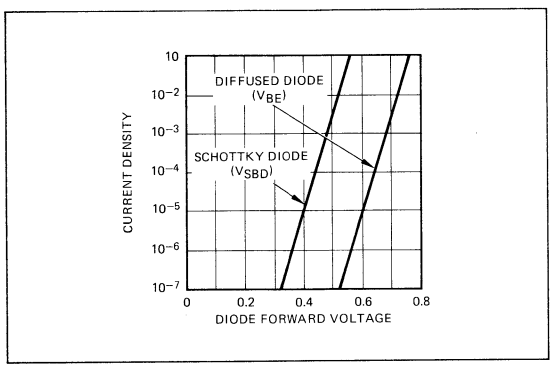



**Figure 2. Comparison of $V_F$ for Schottky and Diffused Diodes.**

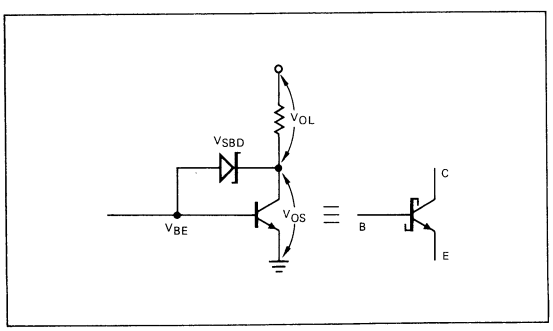



**Figure 3. Schottky Clamped Transistor and its Conventional Circuit Symbol.**

A Schottky diode is formed at a metal to semiconductor junction when the semiconductor doping is at the level normally found in the collector region of TTL devices. A Schottky-clamped transistor is constructed by extending the metal contact for the base region over the collector as shown in Figure 4. The same metallization structure forms a simple ohmic contact at the base, collector and emitter contact windows because of the higher doping levels in the silicon at these locations.

The selection of the forward voltage drop across the Schottky diode, $V_{SBD}$, is a compromise between a high value to insure a minimum $V_{OL}$ but low enough to prevent charge storage in the base. Platinum silicide Schottky diodes provide this optimum voltage drop. Platinum is deposited and platinum-silicide is formed by sintering and annealing. As aluminum has a high affinity for silicon, in order to prevent the aluminum interconnect metallization from diffusing through the platinum material, with resulting lower $V_{SBD}$, a barrier of tungsten-titanium is evaporated after the platinum and before the aluminum metallization. This structure has been extensively evaluated and proven to have excellent reliability characteristics. It is now widely employed in the manufacture of Schottky devices. Reliability data is available from Advanced Micro Devices on request.

## CHARACTERISTICS OF SCHOTTKY DEVICES

The primary reason for the development of Schottky devices was to improve AC (switching) performance and the first integrated circuits to employ this technique offered propagation delays as fast as 3ns. However, their fast rise and fall times and high power requirements have restricted their application to highest performance systems. More recently it was realized that the technique could be used to decrease the charging current required to achieve the 10ns speed specification of standard TTL gates. This insures considerably lower operating power requirements. The resulting family of devices are known as Low-Power Schottky (LS) circuits.

While the low current characteristics of LS devices are extremely important, other features of Schottky devices have contributed significantly to improved overall performance;

- Improved yield can be obtained to higher $\beta$ specifications which reduces the variation of a.c. performance at low temperatures.
- Elimination of the marginal effect of gold doping at high temperature improves switching speed at the upper end.
- PNP transistors with useful $\beta$ can now be fabricated. Since they reduce input load current requirements, they can be employed on inputs where loading is critical.

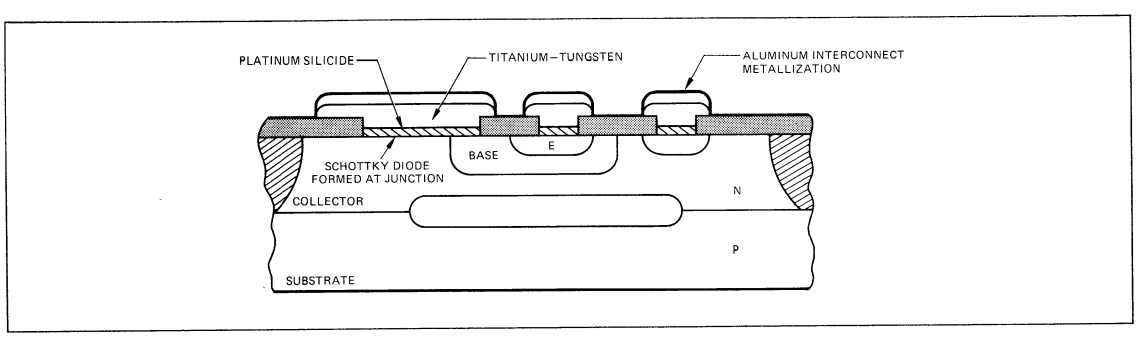



**Figure 4. Schottky Diode Clamped Transistor Structure.**

- The shallow epitaxial layers employed (around 3.5μm) considerably reduce on chip capacitance and series resistance. This is a significant contributor to improved speed performance at low-power.
- Other improvements in general circuit design flexibility include improved control over internal waveform amplitudes, lower junction leakage currents and location of parasitic capacitances at low impedance nodes.

## LOW-POWER SCHOTTKY FAMILIES

The first application of the low power technology to a commercially available product was to redesign the most popular elements of the standard, gold-doped 54/74 TTL family in LS. This provided a set of functions pin-for-pin and speed compatible with the earlier TTL parts, but requiring as little as 20% of the power. The basic gate design for a 54LS/74LS element is shown in Figure 5. This offers a typical propagation delay of 10ns at 2mW power dissipation. Similar improvements have been made in power requirements for flip-flops and MSI functions.

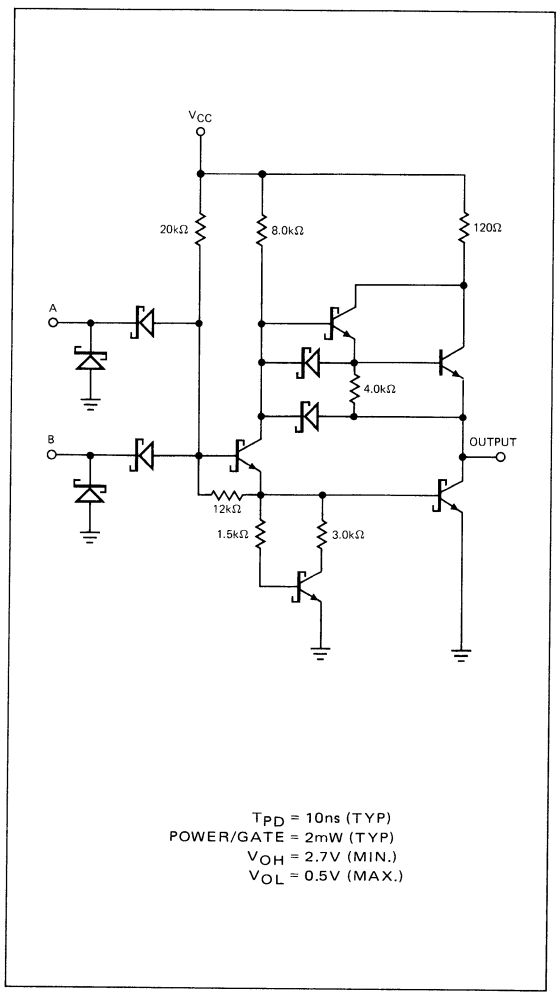



**Figure 5. Low-Power Schottky "74LS" TTL Gate.**

This LS family offers many advantages to the system designers over the older standard TTL functions.

- Lower supply currents permit the use of smaller, lower cost power supplies.
- Reduced power dissipation generates less heat and simplifies cooling needs and allows increased board packing density.
- Lower on-chip operating temperatures decrease IC failure rates, thus improving system reliability.
- Lower operating currents reduce output spiking, leading to a decrease in noise generation and associated system problems.
- As the input load current requirements of Low-Power Schottky are only 25% of standard TTL, the new circuits are easier to interface with MOS elements, such as memories and microprocessors.
- Provided input and output loading rules are obeyed, as the functions and pin-outs are identical to those of the earlier TTL families, it is easy to upgrade existing systems.

In addition, no retraining of personnel is necessary before proceeding with a new design using these improved circuits as most engineers are already familiar with the logic functions and capabilities of TTL.

Later improvements in process technology and design techniques have led to what is essentially a second generation of LS devices. Generally described as high-performance LS, these products maintain the same power requirements as 54LS/74LS but offer such improvements as:

- Up to 50% faster speed
- Improved DC noise margin (50mV at full drive)
- Twice the fan-out over the military temperature range

The Advanced Micro Devices' Am25LS Family combines all these high-performance features into products which are direct replacements for the equivalent Am54LS/74LS MSI functions.

## INCREASED FUNCTIONAL COMPLEXITY

As devices are operating at lower current levels, smaller area geometries can be employed. Thus, an LS design can often be produced on a smaller die than the equivalent standard TTL function. Further, the recent development of composite and self-aligning masking techniques allows even further reductions in device geometry sizes. These in turn result in faster speeds and the ability to manufacture more complex die.

Lower power dissipation also allows considerably more components to be incorporated onto a single chip without exceeding the recommended chip operating temperature.

The ability to produce large die at economical prices has improved the functional capability and variety of elements available in the LS family compared to standard TTL. Thus, LS technology is being used to implement many high-performance LSI functions in memory, interface and microprocessor, as well as logic families.

An important feature of all LS families is the new 20-pin Dual In-Line Package. This configuration fills the need for a package having the number of terminals necessary to accommodate the more complex products possible with LS, without the physical and cost disadvantages of the older 24-pin outline.

The 20-pin DIP has the same 300-mil center to center spacing between rows of pins as the popular 16-pin package. It therefore occupies about one third the board space of the 24-pin DIP with only a minor trade-off in functional capability. For both user and manufacturer this package is also considerably easier and lower cost to handle and test.

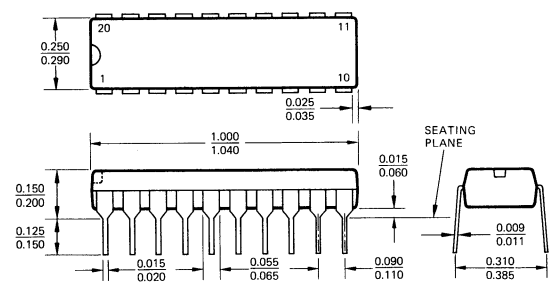
The 20-pin DIP is supplied in molded epoxy and hermetic ceramic versions. An hermetic ceramic flat pack is also available for military temperature range devices.

Functionally the 20-pin configuration is optimum for building octal functions. Eight input lines, eight output lines, power supply and ground, leaves two pins available for control signals. Eight-bit devices are ideal for interfacing with popular eight-bit fixed instruction set MOS microprocessors. They are also useful in micro-programmable machines using bit slice processors implemented in multiples of eight-bits. An octal register device in a 20-pin package can reduce count by 50% over the two quad, or even more wasteful, two hex elements frequently used today.

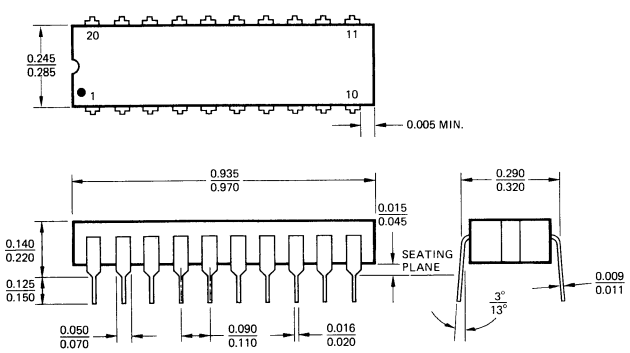
A significant proportion of new Advanced Micro Devices' LS products introduced recently are in the 20-pin package.

## PHYSICAL DIMENSIONS
### 20-Pin Package

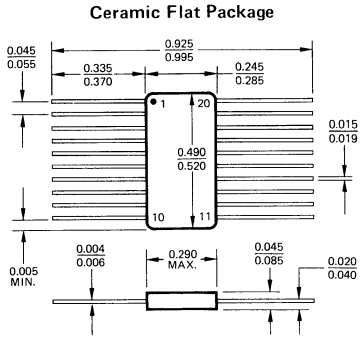
#### Molded Dual-In-Line




#### Ceramic Dual-In-Line




#### Ceramic Flat Package



# 2. D.C. Circuit Characteristics

## CIRCUIT CONFIGURATIONS

The basic circuit design configuration of a Low-Power Schottky gate is similar to that of the original standard TTL elements. However, certain refinements have been made to optimize device performance when fabricated with the LS process.

In order to analyze the circuit configuration, Table 1 shows terms used in describing Advanced Micro Devices' LS circuits:

TABLE 1
D.C. CIRCUIT PARAMETER DEFINITIONS

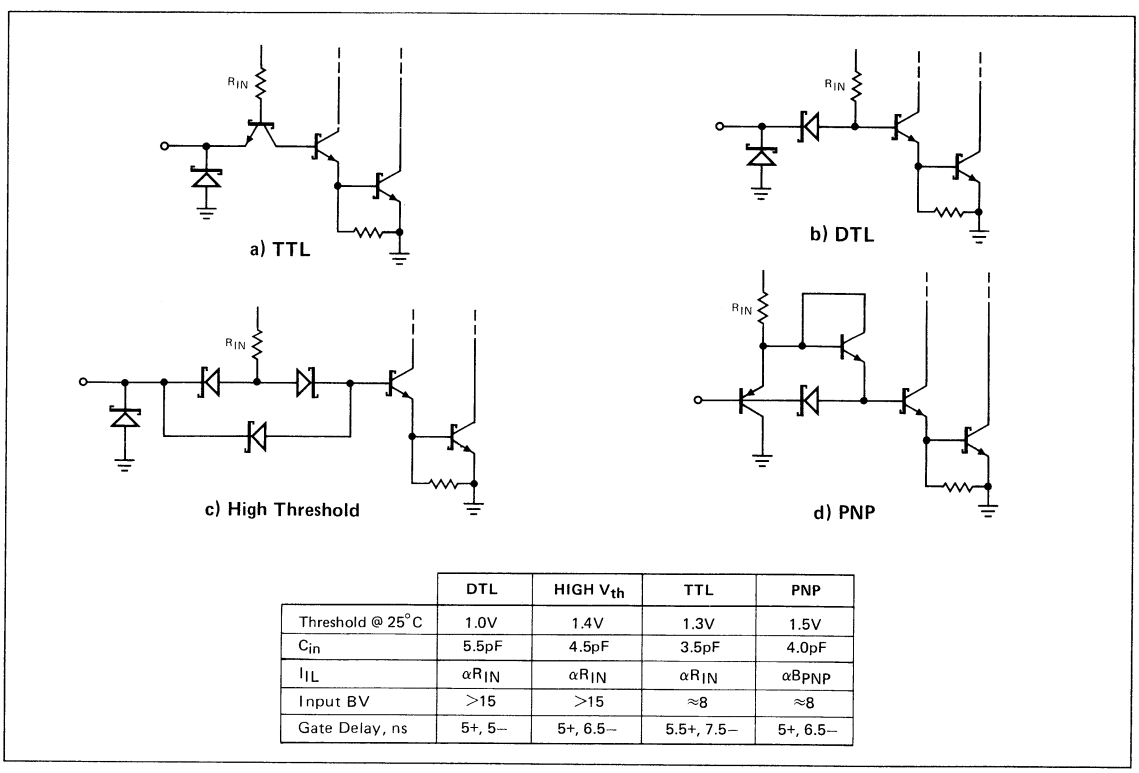
| | |
|---|---|
| $I_{IL}$ | The current out of an input at a specified LOW voltage. |
| $I_{IH}$ | The current into an input at a specified HIGH voltage. |
| $I_{OL}$ | The current into an output when in the LOW state. |
| $I_{OH}$ | The current out of an output when in the HIGH state (pull-up circuit only). |
| $I_{SC}$ | The current out of an output in the HIGH state when shorted to ground. (Also called $I_{OS}$) |
| $V_{CC}$ | The range of supply voltage over which the device is guaranteed to operate. |
| $V_{IL}$ | The guaranteed maximum input voltage that will be recognized by the device as a logic LOW. |
| $V_{IH}$ | The guaranteed minimum input voltage that will be recognized by the device as a logic HIGH. |
| $V_{OL}$ | The maximum guaranteed logic LOW voltage at the output terminal while sinking the specified load current $I_{OL}$. |
| $V_{OH}$ | The minimum guaranteed logic HIGH voltage at the output terminal when sourcing the specified source current $I_{OH}$. |

Both the input and output structures of the LS devices themselves have evolved through a number of configurations as designers have attempted to optimize circuit performance.

Depending on the function of the device any one of four commonly used inputs may be employed. The significant characteristics of each of these configurations are summarized in Figure 6.

The first LS designs used the familiar multi-emitter TTL input of Figure 6a. However because of low breakdown voltage and slow speed it is now used only where the geometry offers a significant advantage in circuit mask layout.

The second and still most widely used structure is the simple DTL style input of Figure 6b. This is the fastest version and it has good input breakdown voltage. In output functions having only a single gate delay between input and output, such as a three-state enable input, the low threshold of the DTL configuration causes the output node to be at a sufficiently low voltage to risk leakage problems at high temperature. The input of Figure 6c raises the threshold by one diode to overcome this problem (Figure 7). However because it is slower and uses more silicon area, its use is limited to special situations. A PNP input, Figure 6d, insures low d.c. loading for devices with common input/output pins such as the Am25LS23. However it is slow and has low breakdown voltage, comparable to the multi-emitter TTL structure.




| | DTL | HIGH $V_{th}$ | TTL | PNP |
|---|---|---|---|---|
| Threshold @ 25°C | 1.0V | 1.4V | 1.3V | 1.5V |
| $C_{in}$ | 5.5pF | 4.5pF | 3.5pF | 4.0pF |
| $I_{IL}$ | $\alpha R_{IN}$ | $\alpha R_{IN}$ | $\alpha R_{IN}$ | $\alpha B_{PNP}$ |
| Input BV | >15 | >15 | ≈8 | ≈8 |
| Gate Delay, ns | 5+, 5– | 5+, 6.5– | 5.5+, 7.5– | 5+, 6.5– |

**Figure 6. Low-Power Schottky Input Configurations.**

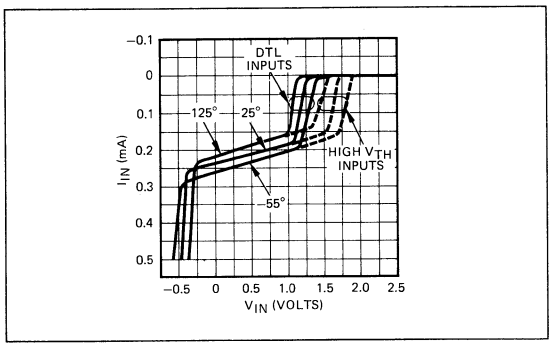



**Figure 7. LS Input Characteristics for DTL and High Threshqld Inputs.**

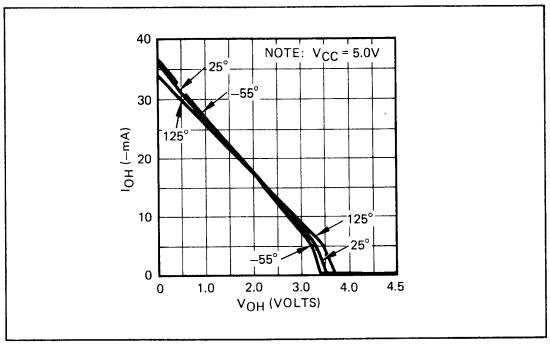



**Figure 9. Typical $V_{OH}$ Versus $I_{OH}$ for Low-Power Schottky.**

Figure 8 compares the early LS output configuration with the design most frequently used today. The change was made to provide clamping of positive ringing and to allow the higher $I_{SC}$ currents now specified (see section 3). The typical $V_{OH}$ versus $I_{OH}$ curves of Figure 9 are similar for both versions.

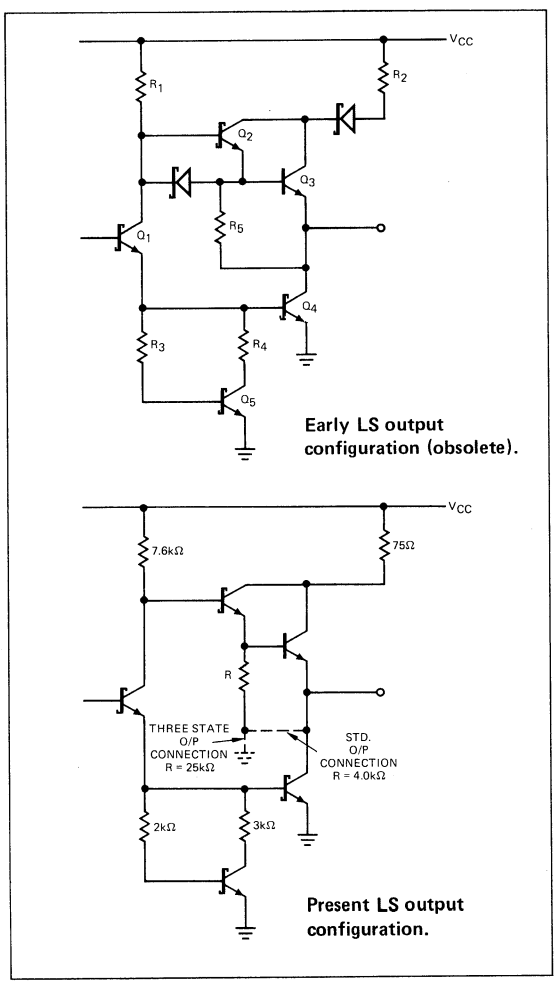



**Figure 8. Low-Power Schottky Output Configurations.**

This example displays an $I_{SC}$ of approximately 35mA. Note that both of these designs include the "squaring" network ($R_3$, $R_4$ and $Q_5$) at the base of the output pulldown transistor, $Q_4$, which was not included on standard TTL families. The result of this is a sharp transition of $V_{OUT}$ with $V_{IN}$ shown in Figure 10 for a simple gate function.

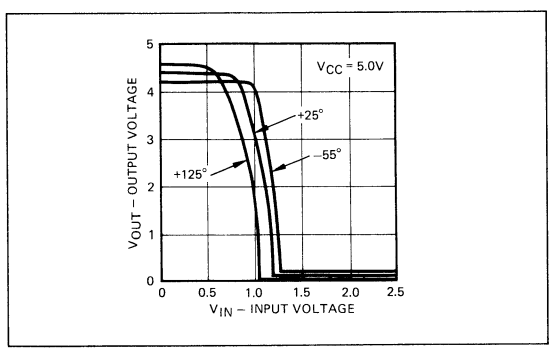



**Figure 10. Typical Output Versus Input Voltage Characteristic.**

The typical $V_{OL}$ versus $I_{OL}$ output characteristics of LS devices are shown in Figure 11. Most 74LS functions are specified at $V_{OL}$ = 0.4V at $I_{OL}$ = 4mA and 0.5V at 8mA. Am25LS are specified at 0.45V for $I_{OL}$ = 8mA. Some newer designs are being guaranteed at $I_{OL}$ of 12mA and 24mA. This curve indicates that lack of $\beta$ at low temperature will not permit existing designs to be guaranteed to these higher values without severe yield loss.

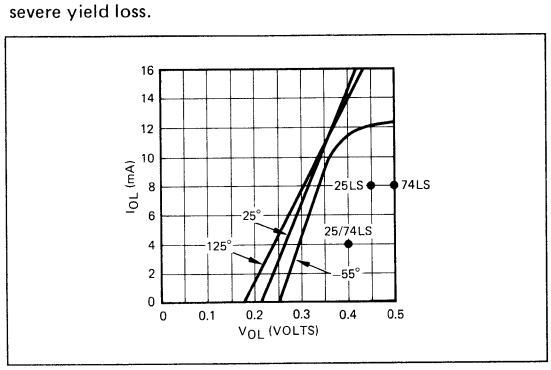



**Figure 11. Typical LS $V_{OL}$ Versus $I_{OL}$ Characteristics.**

TABLE 2

COMPARISON OF TTL DC PARAMETERS

| Parameters | 54LS/74LS LOW-POWER SCHOTTKY Conditions | | Min. | Typ. | Max. | 25LS LOW-POWER SCHOTTKY Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | $I_{OL}$ = 4.0mA | | | | 0.4 | $I_{OL}$ = 4.0mA | | | | 0.4 | V |
| | $I_{OL}$ = 8.0mA (COM'L Only) | | | | 0.5 | $I_{OL}$ = 8.0mA (MIL, COM'L) | | | | 0.45 | |
| $V_{OH}$ | $I_{OH}$ = −400μA | MIL | 2.5 | 3.4 | | $I_{OH}$ = −440μA | MIL | 2.5 | 3.4 | | V |
| | | COM'L | 2.7 | 3.4 | | | COM'L | 2.7 | 3.4 | | |
| $V_{IL}$ | Logic LOW | MIL | | | 0.7 | Logic LOW | MIL | | | 0.7 | V |
| | | COM'L | | | 0.8 | | COM'L | | | 0.8 | |
| $V_{IH}$ | Logic HIGH | | 2.0 | | | Logic HIGH | | 2.0 | | | V |
| $I_{IL}$ | $V_{IN}$ = 0.4V | | | | −0.36 | $V_{IN}$ = 0.4V | | | | −0.36 | mA |
| $I_{IH}$ | $V_{IN}$ = 2.7V | | | | 20 | $V_{IN}$ = 2.7V | | | | 20 | μA |

| Parameter | 54S/74S AND 25S SCHOTTKY TTL Condition | | Min. | Typ. | Max. | STANDARD TTL Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | $I_{OL}$ = 20mA | | | 0.3 | 0.5 | $I_{OL}$ = 16mA | | 0.2 | 0.4 | Volts |
| $V_{OH}$ | $I_{OH}$ = −1.0mA | MIL | 2.5 | 3.4 | | $I_{OH}$ = −300μA | 2.4 | 3.4 | | Volts |
| | | COM'L | 2.7 | 3.4 | | | | | | |
| $V_{IL}$ | Logic LOW | | | | 0.8 | Logic LOW | | | 0.8 | Volts |
| $V_{IH}$ | Logic HIGH | | 2.0 | | | Logic HIGH | 2.0 | | | Volts |
| $I_{IL}$ | $V_{IN}$ = 0.5V | | | | −2.0 | $V_{IN}$ = 0.4V | | | −1.6 | mA |
| $I_{IH}$ | $V_{IN}$ = 2.7V | | | | 50 | $V_{IN}$ = 2.4V | | | 40 | μA |

## INPUT/OUTPUT LEVELS

The input thresholds and output logic levels of LS circuits have been designed as far as possible to be compatible with those of standard TTL. Table 2 shows the guaranteed d.c. parameters of the Am54/74LS and second generation Am25LS families. Input current requirements ($I_{IH}$, $I_{IL}$) and therefore output drive needs ($I_{OH}$, $I_{OL}$) are significantly reduced over standard TTL.

A one unit load input current at logic HIGH, $I_{IH}$, for Am54LS/74LS is 20μA, compared with 40μA for Am54/74 standard TTL. Similarly at logic LOW, $I_{IL}$ is reduced to −0.36mA from −1.6mA.

Corresponding reductions in the output drive requirements are $I_{OL}$ = 4mA vs. 16mA at $V_{OL}$ = 0.4V and $I_{OH}$ = −400μA compared to 800μA.

## FAN-OUT CAPABILITY

The fan-out capability of a logic family indicates the number of inputs which can be driven by a single output. It is defined as the maximum output drive current divided by the input current available.

Logic HIGH Fan-out = $I_{OH}/I_{IH}$
Logic LOW fan-out = $I_{OL}/I_{IL}$

Table 3 shows the fan-out capabilities of typical functions from the three families. The lower current operating levels of LS devices allow them to be specified at a logic LOW fan-out over the commercial range of more than twice that of standard TTL (22 vs. 10). The Am25LS family allows this advantage to be extended to the military range.

## D.C. NOISE MARGIN

The D.C. noise margins of a digital system are defined from Figure 12 as follows:

Logic HIGH Noise Margin = $V_{OH1} - V_{IH2}$
Logic LOW Noise Margin = $V_{IL2} - V_{OL1}$

These parameters for LS devices are shown in Table 2. LS has a minimum logic HIGH output voltage of $V_{OH}$ = 2.5V for military and 2.7V for the commercial temperature range. For standard TTL, $V_{OH}$ is 2.4V. $V_{IH}$ is 2.0V for both families.

Table 3 compares the guaranteed noise margin values for the standard TTL and LS devices. LS devices offer improved margin over standard TTL in the logic HIGH state, which is the most critical with regard to noise generation. At a similar fan-out, 10 for standard TTL and 11 for LS, noise margins in the LOW state are the same over the commercial range.

TABLE 3
FAN-OUT AND NOISE MARGIN
COMPARISON OF TTL AND LS FAMILIES.

a) LOGIC "HIGH" STATE

| FAMILY | INPUT CURRENT $I_{IH}$ | OUTPUT CURRENT $I_{OH}$ | FAN-OUT | | NOISE MARGIN | |
|---|---|---|---|---|---|---|
| | | | MILITARY | COMMERCIAL | MILITARY | COMMERCIAL |
| 54/74 | 40μA | −800μA | 20 | 20 | 400mV | 400mV |
| 54LS/74LS | 20μA | −400μA | 20 | 20 | 500mV | 700mV |
| 25LS | 20μA | −440μA | 22 | 22 | 500mV | 700mV |

b) LOGIC "LOW" STATE

| FAMILY | INPUT CURRENT $I_{IL}$ | OUTPUT CURRENT $I_{OL}$ | FAN-OUT | | NOISE MARGIN | |
|---|---|---|---|---|---|---|
| | | | MILITARY | COMMERCIAL | MILITARY | COMMERCIAL |
| 54/74 | −1.6mA | 16mA | 10 | 10 | 400mV | 400mV |
| 54LS/74LS | −0.36mA | 4mA | 11 | 11 | 300mV | 400mV |
| | | 8mA | No Spec. | 22 | No Spec. | 300mV |
| 25LS | −0.36mA | 4mA | 11 | 11 | 300mV | 400mV |
| | | 8mA | 22 | 22 | 250mV | 350mV |

Military LS devices have a 100mV lower noise margin in the LOW state than standard TTL. In most systems, this does not present a problem as the lower power supply currents being switched with LS generally result in lower system noise generation.

The logic levels guaranteed over the operating temperature ranges are of course worst case. Figures 13 and 14 show the typical values to be considerably better than these.

## Am25LS D.C. FEATURES

The D.C. advantages offered by second generation Am25LS over 54/74LS devices can be seen from Table 3 as:

1. In the logic LOW state at a fan-out of 22 (8mA), Am25LS has 50mV greater noise margin (350mV vs. 300mV).
2. Am25LS products are guaranteed at a fan-out of 22 (8mA) over the military range. Am54LS is specified at fan-out of 10 (4mA) only.
3. Am25LS offers a symmetrical fan-out of 22 in both logic HIGH and logic LOW states, allowing full use of the logic LOW drive capability.

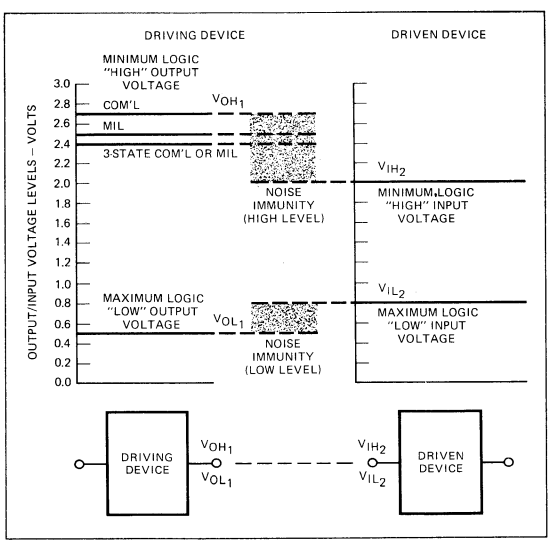



Figure 12. Input/Output Voltage Interface Conditions.

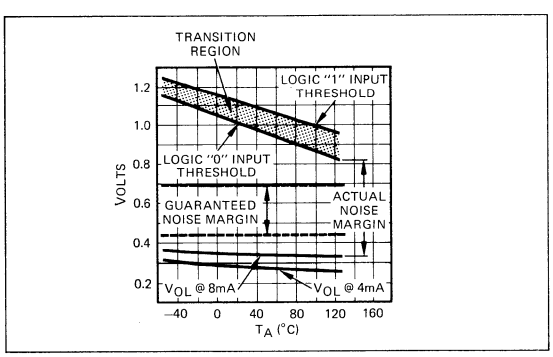



Figure 13. LS Logic "0" Noise Margin.

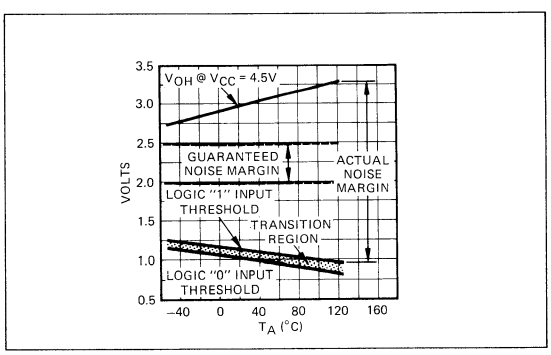



Figure 14. LS Logic "1" Noise Margin.

# 3. A.C. Characteristics

## INTRODUCTION

Many Low-Power Schottky functions have been designed specifically to replace standard TTL elements in existing system designs. Their A.C. performance characteristics usually meet or exceed the limits of the earlier devices. The switching terms which are used on data sheets to describe the A.C. performance of these designs are summarized in Table 4. The more important parameters are discussed in detail in this section.

### TABLE 4
### DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.3V logic level unless otherwise noted.)

$f_{MAX}$ The highest operating clock frequency.

$t_{PLH}$ The propagation delay time from an input change to an output LOW-to-HIGH transition.

$t_{PHL}$ The propagation delay time from an input change to an output HIGH-to-LOW transition.

$t_{PW}$ Pulse width. The time between the leading and trailing edges of a pulse, measured at the 50% points.

$t_r$ Rise time. The time required for a signal to change from 10% to 90% of its measured values.

$t_f$ Fall time. The time required for a signal to change from 90% to 10% of its measured values.

$t_s$ Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

$t_h$ Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

$t_R$ Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

$t_{HZ}$ also $t_{PHZ}$ HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5V change).

$t_{LZ}$ also $t_{PLZ}$ LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).

$t_{ZH}$ also $t_{PZH}$ Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

$t_{ZL}$ also $t_{PZL}$ Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

## PROPAGATION DELAYS

The standard designations for delays through combinatorial logic networks are $t_{PHL}$ and $t_{PLH}$. A delay from an input change to an output going LOW is called $t_{PHL}$, while $t_{PLH}$ is the delay from an input change to an output going HIGH.

Figure 15 shows a typical waveform with the output changing during the interval indicated by the diagonal, sloping line. Note that all switching times shown are measured at the 1.3 volt logic level.

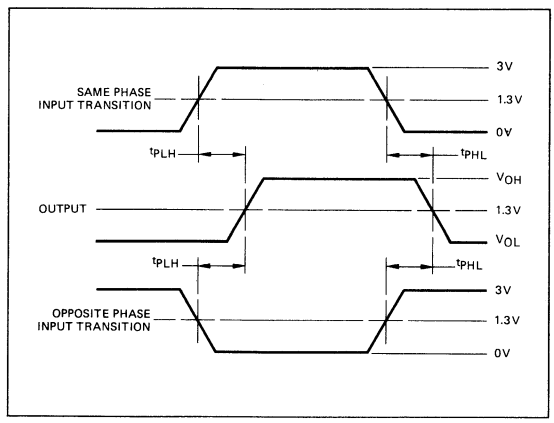



**Figure 15. Propagation Delay.**

Typical values for a single gate propagation delay $t_{PHL}$ in Low-Power Schottky functions are 8–10ns into a 15pF load. Higher performance LS families, such as Am25LS, exhibit delays in the 4 – 6ns range. These propagation delays will increase by 2 – 4ns at an output loading of 50pF or approximately 0.1ns per pF. See Figure 16.

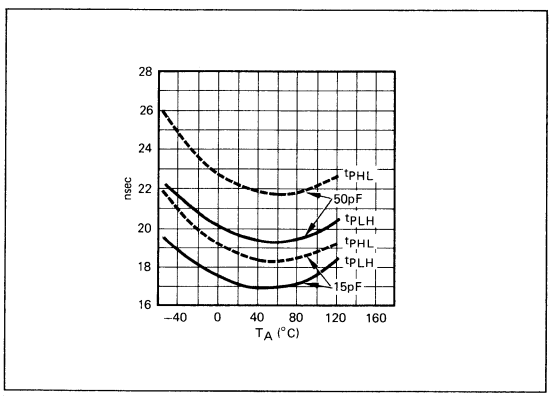



**Figure 16. Am25LS138 Typical Propagation Delays Address to Output (3 Levels).**

Table 5 shows the worst case delays through typical two and three deep gate MSI functions such as multiplexers and decoders. Speed improvements attainable with the Am25LS higher performance LS devices at this level of complexity are shown to be in the range of 20 to 40%. Guaranteed delays into 50pF loads are being specified on all new Am25LS data sheets. See Table 8.

TABLE 5
COMPARISON OF AC PARAMETERS ($T_A$ = +25°C)

**LS138 3-Line to 8-Line Decoder/Demultiplexer**

| Parameters | Description | Test Conditions | Am25LS138 Min. | Am25LS138 Max. | Am54LS138 Am74LS138 Min. | Am54LS138 Am74LS138 Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Two Level Delay Select to Output | $V_{CC}$ = 5.0V, $R_L$ = 2kΩ, $C_L$ = 15pF | | 15 | | 20 | ns |
| $t_{PHL}$ | | | | 21 | | 41 | |
| $t_{PLH}$ | Three Level Delay Select to Output | | | 23 | | 27 | ns |
| $t_{PHL}$ | | | | 27 | | 39 | |
| $t_{PLH}$ | G2A or G2B to Output | | | 15 | | 18 | ns |
| $t_{PHL}$ | | | | 23 | | 32 | |
| $t_{PLH}$ | G1 to Output | | | 18 | | 26 | ns |
| $t_{PHL}$ | | | | 27 | | 38 | |

**LS158 Quadruple 2-Line to 1-Line Data Selectors/Multiplexers**

| Parameters | Description | Test Conditions | Am25LS158 Min. | Am25LS158 Max. | Am54LS158 Am74LS158 Min. | Am54LS158 Am74LS158 Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | $V_{CC}$ = 5.0V, $R_L$ = 2kΩ, $C_L$ = 15pF | | 9 | | 12 | ns |
| $t_{PHL}$ | | | | 11 | | 12 | |
| $t_{PLH}$ | Strobe to Output | | | 12 | | 17 | ns |
| $t_{PHL}$ | | | | 17 | | 18 | |
| $t_{PLH}$ | Select to Output | | | 20 | | 20 | ns |
| $t_{PHL}$ | | | | 21 | | 24 | |

2

## EDGE RATES

The rise and fall times of Low-Power Schottky devices are similar to those of standard TTL. Into a 50pF load fall time, $t_f$, is typically 6-8ns, while rise time, $t_r$, is in the 9-12ns range. A.C. parameters are measured at $t_f \leqslant 6$ns and $t_r \leqslant 15$ns.

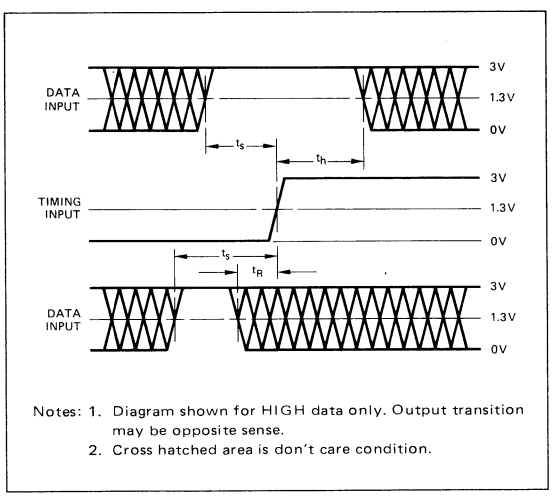
As with standard TTL, careful P.C. board layout rules should be employed to avoid problems which can occur at these relatively fast edge rates. In particular, precautions should be taken to insure that transmission line effects do not cause false switching or ringing and oscillation problems on lines longer than 18 inches. See Section 4 for more information.

## SEQUENTIAL DEVICES

Set-up time, $t_s$, hold time, $t_h$, and release time, $t_R$, are the most important parameters for specifying sequential elements such as latches, flip-flops and registers.

For these synchronous devices, inputs must be stable for a certain period of time before the clock or enable pulse. This interval is the region in time during which devices are "sampling" their inputs. As an example, consider a latch with a D input and an active LOW clock. The latch will store the information present on its input just before the clock goes HIGH. The question is, how long does the input level have to be present and stable before the clock goes HIGH? A particular device will "sample" its input at some exact instant, but in a group of devices some are slower than others. The result is an interval of some time called set-up time during which all devices, fast or slow, will "sample" their inputs.

All devices exhibit a hold time. That is a period of time after the clock or enable pulse transition during which the data cannot be changed without loss of input intelligence. This hold time occurs after the clock goes HIGH. Figure 17 shows the input requirements and definitions for data entry. Release time is negative hold time or the time period prior to the clock input after which the data can be released. Typical examples of LS characteristics and the improvements attainable with high performance Am25LS sequential devices are shown in Table 6.




Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

**Figure 17. Set-up, Hold, and Release Time Definitions.**

## $f_{MAX}$.

A frequently misunderstood parameter on data sheets is maximum clock frequency $f_{MAX}$. This was defined by the early TTL manufacturers as the maximum toggle frequency which can be attained by the device under ideal conditions with no constraints on $t_r$, $t_f$, pulse width, or duty cycle. Although $f_{MAX}$ as specified cannot usually be attained in an operating system, it is a relatively easy parameter to test and provides a convenient measure of comparative performance between different devices. For instance, Table 6 shows the Am54/74LS174 at $f_{MAX}$ = 30MHz (min.) while the high-performance Am25LS is specified at 40MHz (min.). Actual toggle frequency in a system must be determined from the specific signal conditions presented to the device.

TABLE 6
SWITCHING CHARACTERISTICS ($T_A$ = 25°C)

**LS174/LS175 Hex/Quadruple D-Type Flip-Flops with Clear**

| Parameters | Description | | Test Conditions | Am25LS174 Am25LS175 Min. | Am25LS174 Am25LS175 Max. | Am54LS174 Am54LS175 Am74LS174 Am74LS175 Min. | Am54LS174 Am54LS175 Am74LS174 Am74LS175 Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | $V_{CC}$ = 5.0V, $R_L$ = 2kΩ, $C_L$ = 15pF | | 23 | | 30 | ns |
| $t_{PHL}$ | | | | | 22 | | 35 | |
| $t_{PLH}$ | Clear to $\overline{Q}$ Output, LS175 only | | | | 25 | | 25 | ns |
| $t_{PHL}$ | Clear to Output | | | | 35 | | 35 | |
| $t_{pw}$ | Pulse Width | Clock | | 17 | | 20 | | ns |
| | | Clear | | 20 | | 20 | | |
| $t_s$ | Data Set-up Time | | | 20 | | 20 | | ns |
| $t_s$ | Set-up Time Clear Recovery (in-active) to Clock | | | 20 | | 25 | | ns |
| $t_h$ | Data Hold Time | | | 5 | | 5 | | ns |
| $f_{MAX.}$ | Maximum Clock Frequency | | | 40 | | 30 | | MHz |

## EFFECTS OF TEMPERATURE AND POWER SUPPLY VARIATIONS

Standard TTL devices exhibit severe degradation in A.C. performance towards the recommended limits of the operating temperature and power supply voltage ranges.

At elevated temperature and/or high $V_{CC}$ levels, charge storage begins to slow down A.C. response. At the other extreme, low temperature and/or low $V_{CC}$, the loss of $\beta$ causes a similar problem. These combined effects can cause more than 50% degradation in performance over the full military temperature and power supply extremes.

As noted in Section 1, Low-Power Schottky technology reduces the impact of both of these effects on performance. $\beta$ degradation at cold temperatures is far less severe and Schottky clamping largely eliminates the effects of charge storage at high temperature.

General guidelines for variation in the AC response over temperature and power supply variations are not easy to specify. Typical measured variations for a combinatorial and a sequential device are shown in Figures 16 and 18.

The system's designer would like a factor which will allow his system to meet specification with minimum design overkill. However, the component engineer often requires maximum delays to be guaranteed. For system design guidelines, the AC derating factors of Table 7 may be useful.

It must be emphasized that the values of Table 7 are typical. However as it is unlikely that any given system will contain all worst case devices they will usually yield a fairly safe prediction of the system performance which can be achieved.

Individual components will of course be slower than these typical numbers. These must be reflected on procurement specifications. A general rule of thumb would be to double the system design guidelines of Table 7. New Am25LS specifications are now being published with worst case parameters guaranteed over the operating power supply and temperature ranges, as well as at a realistic system load condition of 50pF. A typical example of this format is shown in Table 8.

## SHORT CIRCUIT OUTPUT CURRENT

To improve performance, in 1975 TI lowered the short-circuit current limiting resistor value. This increased the $I_{SC}$ ($I_{OS}$) range from −6 to −42mA up to −30 to −130mA. The overall

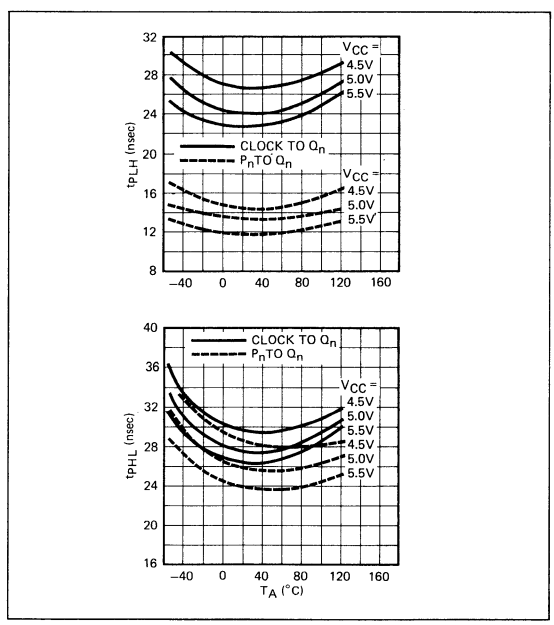



**Figure 18. Typical A.C. Variations with Temperature and Power Supply for Am25LS193 Counter.**

TABLE 7
GUIDELINES FOR TYPICAL VARIATION OF A.C. PARAMETERS WITH COMBINED TEMPERATURE AND $V_{CC}$ VARIATION

| Temperature Range | $V_{CC}$ Variation (Nominal 5V) | AC Derating Factor System | AC Derating Factor Component |
|---|---|---|---|
| COM'L, 0°C to +70°C | None | 5% | 10% |
| COM'L, 0°C to +70°C | ±0.25V | 15% | 30% |
| MIL, −55°C to +125°C | None | 15% | 30% |
| MIL, −55°C to +125°C | ±0.5V | 25% | 50% |

delay when driving very large capacitive loads (>150pF) was reduced somewhat as a result. However, the inherent circuit performance still dominates in normal applications such that the Am25LS and other high performance families remain faster even when driving large capacitive loads.

As an attempt to offer standardized specifications, most manufacturers, including Advanced Micro Devices, Fairchild, Motorola, Raytheon, and Signetics, also lowered their short-circuit current limiting resistor values on new designs to provide a typical $I_{SC}$ of −60mA. Most manufacturers now specify −15 to −100mA to accommodate both old and new circuits. The maximum value of −100mA was chosen, as −130mA was felt to be too high for a noise sensitive system design. The Am25LS high performance family is specified even tighter, with the maximum $I_{SC}$ limited to −85mA.

Early in 1977 TI changed their data sheets yet again to specify $I_{SC}$ from −20mA to −100mA on regular outputs and −30mA to −130mA on three-state outputs.

**TABLE 8**
**Am25LS2513 THREE-STATE PRIORITY ENCODER**
**A.C. SPECIFICATION FORMAT FOR $V_{CC}$ AND TEMPERATURE EXTREMES AND 50pF LOAD CONDITION**

**SWITCHING CHARACTERISTICS**
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_i}$ to An (In-phase) | $C_L$ = 15pF, $R_L$ = 2.0kΩ | | 17 | 25 | ns |
| $t_{PHL}$ | | | | 17 | 25 | |
| $t_{PLH}$ | $\overline{I_i}$ to An (Out-phase) | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | 12 | 18 | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{EO}$ | | | 7.0 | 11 | ns |
| $t_{PHL}$ | | | | 24 | 36 | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{EO}$ | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | 23 | 34 | |
| $t_{PLH}$ | $\overline{EI}$ to An | | | 12 | 18 | ns |
| $t_{PHL}$ | | | | 14 | 21 | |
| $t_{ZH}$ | $G_1$ or $G_2$ to An | | | 23 | 40 | ns |
| $t_{ZL}$ | | | | 20 | 37 | |
| $t_{ZH}$ | $\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to An | | | 20 | 30 | ns |
| $t_{ZL}$ | | | | 18 | 27 | |
| $t_{HZ}$ | $G_1$ or $G_2$ to An | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ | | 17 | 27 | ns |
| $t_{LZ}$ | | | | 19 | 28 | |
| $t_{HZ}$ | $\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to An | | | 16 | 24 | ns |
| $t_{LZ}$ | | | | 18 | 27 | |

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

| Parameters | Description | Test Conditions | Am25LS COM'L: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL: $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_i}$ to An (In-phase) | $C_L$ = 50pF, $R_L$ = 2.0kΩ | | 31 | | 37 | ns |
| $t_{PHL}$ | | | | 30 | | 34 | |
| $t_{PLH}$ | $\overline{I_i}$ to An (Out-phase) | | | 22 | | 27 | ns |
| $t_{PHL}$ | | | | 22 | | 25 | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{EO}$ | | | 15 | | 18 | ns |
| $t_{PHL}$ | | | | 48 | | 60 | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{EO}$ | | | 19 | | 21 | ns |
| $t_{PHL}$ | | | | 46 | | 57 | |
| $t_{PLH}$ | $\overline{EI}$ to An | | | 22 | | 25 | ns |
| $t_{PHL}$ | | | | 27 | | 32 | |
| $t_{ZH}$ | $G_1$ or $G_2$ to An | | | 42 | | 49 | ns |
| $t_{ZL}$ | | | | 43 | | 49 | |
| $t_{ZH}$ | $\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to An | | | 36 | | 43 | ns |
| $t_{ZL}$ | | | | 35 | | 43 | |
| $t_{HZ}$ | $G_1$ or $G_2$ to An | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ | | 34 | | 40 | ns |
| $t_{LZ}$ | | | | 34 | | 40 | |
| $t_{HZ}$ | $\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to An | | | 30 | | 35 | ns |
| $t_{LZ}$ | | | | 31 | | 35 | |

# 4. Design Guidelines

## POWER SUPPLY CONSIDERATIONS

The recommended power supply voltage ($V_{CC}$) for all TTL circuits, including LS, is +5V. Commercial temperature range devices, designated 74LS or in the case of Am25LS with the suffix C, are specified with a ±5% supply tolerance (±250mV) over the ambient range 0°C to 70°C. Military range parts, designated 54LS or in the case of Am25LS with the suffix M, are guaranteed with a ±10% supply tolerance (±500mV) over an ambient temperature range of −55°C to +125°C. The power supply should be well regulated with a ripple less than 5% and with regulation better than 5%. Even though LS devices generate significantly smaller power supply spikes when switching than standard TTL, on-board regulation is still preferable to isolate this noise to one board.

A low-inductance transmission line power distribution bus with good RF decoupling is necessary for large systems. On all boards, ceramic decoupling capacitors of 0.01μF to 0.1μF should be used at least one for every five packages, and one for every one-shot (monostable), line driver and line receiver package. In addition, a larger tantalum capacitor of 20μF to 100μF should be included on each card. On boards containing a large number of packages, a low impedance ground system is essential. The ground can either be a bus or a ground which is incorporated with the $V_{CC}$ supply to form a transmission line power system. Separate power transmission systems can be attached to the board to provide this same feature without the cost of a multi-layer PC card.

## UNUSED INPUTS

An unused input to an AND or NAND gate should not be left floating as it can act as an antenna for noise. On devices with storage, such as latches, registers and counters, it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. This technique optimizes switching speed as the distributed capacitance associated with the floating input, bond wire and package leads is eliminated. To terminate, the input should be held between 2.4V and the maximum input voltage. One method of achieving this is to connect the unused input to $V_{CC}$. Most LS inputs have a breakdown voltage >7V and require no series resistor. Devices specified with a maximum 5.5 volt breakdown should use a 1kΩ to 10kΩ current limiting series resistor to protect against $V_{CC}$ transients. Another method is to connect the unused input to the output of an unused gate that is forced HIGH. Do not connect an unused input to another input of the same NAND or AND function. Although recommended for standard TTL, with LS this increases the input coupling capacitance and reduces A.C. noise immunity.

## TRANSMISSION LINE EFFECTS

The relatively fast rise and fall times of Low-Power Schottky TTL (5 to 15ns) can cause transmission line effects with interconnections as short as 18 inches. With one TTL device driving another and the driver switching from LOW to HIGH, if the propagation delay of the interconnection is long compared to the signal rise time, the arrangement can behave like a transmission line driven by a generator with a non-linear output. The initial voltage step at the output, just after the driver has switched, propagates down the line and reflects at the end. In the typical case where the line is open ended or terminated in an impedance greater than its characteristics impedance ($Z_{OL}$), the reflected wave arrives back at the source and increases $V_{OUT}$. If the total round-trip delay is longer than the rise time of the driving signal, a staircase response results at the driver output and along the line. If one of the driven devices is connected close to the driver, the initial output voltage ($V_{OUT}$) seen by it might not exceed $V_{IH}$. The state of the input is undetermined until after the round trip of the transmission line, thus slowing down the response of the system.

The longest interconnection that should be used with LS devices without incurring problems due to line effects is in the 10–12 inch range.

With longer interconnections, transmission line techniques should be used for maximum speed. Good system operation can be obtained by designing around 100 ohm lines. A 0.026 inch (0.65mm) trace on a 0.062 inch epoxy-glass board ($E_r$ = 4.7) with a ground plane on the other side represents a 100Ω line. 28 to 30 gauge wire (0.25 to 0.30mm) twisted pair line has a characteristic impedance of 100 to 115Ω.

## LINE DRIVING AND RECEIVING

For lines longer than 2 feet, twisted pairs of coaxial cable should be used. The characteristic impedance or the transmission media should be approximately 120Ω such as twisted pairs of #26 wire or 100Ω coax. A possible choice is cables with a characteristic impedance $R_O$ of 100Ω such as ribbon cable or flat cable with controlled impedance. Resistive pull-ups at the receiving end can be used to increase noise margin. Where reflection effects are unacceptable, the line must be terminated in its characteristic impedance. A method shown in Figure 19

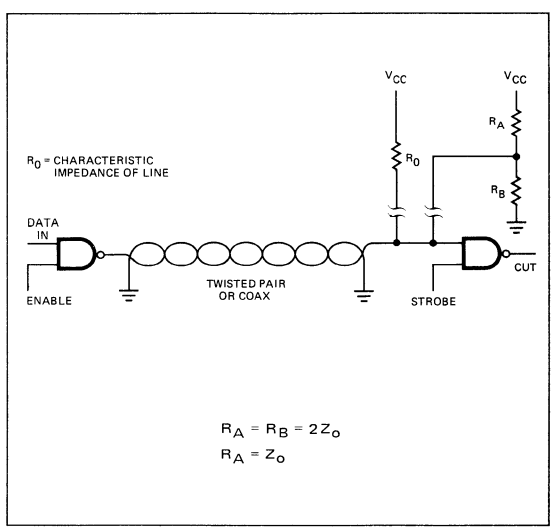



**Figure 19. LS Driving Twisted Pair.**

has the output of the line tied to $V_{CC}$ through a resistor equivalent to the characteristic impedance of the line. As the output impedance of the LS driver is low and must sink the current through it, in addition to the current from the inputs being driven, a useful technique is to terminate the line in a voltage divider with two resistors, each twice the line impedance. This reduces the extra sink current by 50%. Where the line exceeds five feet in length it is preferable to dedicate gates solely to line driving.

For additional noise immunity when driving long lines, a differential line driver and line receiver may be used. These dedicated line interface circuits drive a twisted pair of wires differentially, permit easy termination of lines and provide excellent common mode noise rejection.

The Am26LS31 driver and Am26LS32 and Am26LS33 are quad differential line drivers and receivers satisfying the interface requirements of EIA RS-422 and 423 as well as military applications, Figure 20. They are designed to operate off the standard 5V power supplies of the LS logic devices. More applications information on line termination techniques is provided on the above mentioned device data sheets.

## CROSS-TALK AND RINGING

These two problems may be experienced with all forms of high speed digital logic. Crosstalk is the coupling of energy from one circuit to another via real or parasitic capacitance and inductance. Ringing is the possible rebound of the signal into the input threshold region (0.8 – 2.0V) following a HIGH-to-LOW level change. When a driver switches from a HIGH-to-LOW state the output voltage should fall below the threshold value. However, a line having a very low characteristic impedance does not allow transistor Q5 in the NAND gate example to saturate, and the resulting output voltage may not be low enough to switch an adjacent device until two or more line delay times. The low current levels at which LS devices operate, coupled with the low output impedance in both HIGH and LOW Logic states, minimize crosstalk effects. Input clamp diodes provided on all LS devices are extremely effective in reducing ringing phenomenon.

Care should be taken to insure that signals with falling edges faster than 2.5-3ns/volt are not coupled into the input of an LS function. Even though the signal may not pass into the threshold region, if the pulse edge is fast enough, sufficient energy may be capacitively coupled into a sequential device to cause it to change state: High speed Schottky elements in a test setup can exceed this limit. However in an active system, the edges will generally be slowed sufficiently to eliminate any problem.



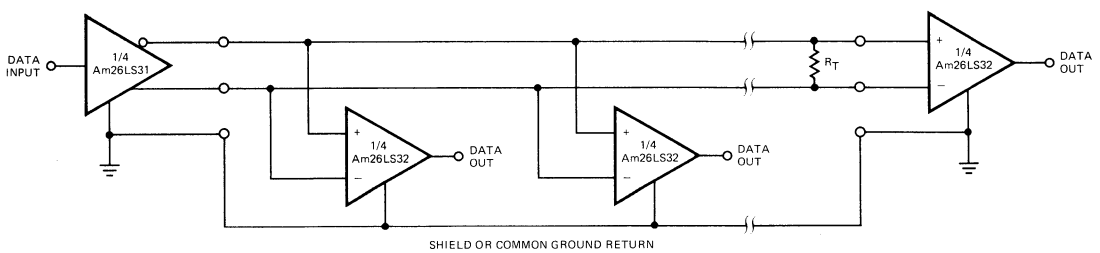



**Figure 20. Differential Line Driving and Receiving with the Am26LS31 and Am26LS32.**

# RELIABILITY REPORT SCHOTTKY AND LOW-POWER SCHOTTKY TTL DEVICES

**By Lawrence Drake and Jeff Kersey**

## RELIABILITY TESTING OF SCHOTTKY DEVICES

Reliability testing of AMD TTL devices using gold-doped and Schottky (S and LS) processes shows both technologies to be extremely stable. Life test data (MIL-STD-883, Method 1005 for Group C, subgroup 5 testing 1000 hours, 125°C Operating Life) for 3610 parts yielded two failures – one slightly out of specification at 25°C only, the other suspected to have been damaged by handling. Even considering the two failures, the failure rate is only 0.05% per thousand hours at 125°C or 0.0005% per thousand equivalent at 70°C (1 e v acceleration activation energy). Three lots (231 parts) were Schottky TTL devices.

The basic design reliability of Schottky technology has been demonstrated in an extended life test on special circuit patterns devised so that individual circuit elements could be measured. Two groups of 22 of these special test patterns were stressed as indicated in Table 1 at 125°C. Change in the parameters were recorded at 11,000 hours for Group I and 10,000 hours for Group II and are presented in Tables II and III. No device failures occured during these tests and no significant drifts or trends are evident. Several leakage parameters ($I_{IH}$, $I_{CEO}$, $I_{LK}$) have high percentage changes but the absolute values are in the nanoamp range and approach the measurement systems resolution limit. Decreases as well as increases in these currents occurred so trends are not indicated.

Several devices (74LS174, 74LS175 and 25LS161) were checked for parameter drift during 1000 hour Life Tests at 125°C using a MIL-STD-883, Method 1005, Condition C (Steady-State, Power and Reverse Bias) circuit. As can be seen from Tables IV, V and VI, no significant change occurred; again no device failures in any of these tests. The tests for the 74LS174's and 74LS175 contained 4 reference or control units, not subjected to the test, but included in the pre and post-test measurements. In most instances the test parts parameter shift was within measurement spread for the control units.

Several Group C tests as previously mentioned have been run on Schottky devices. These tests as well as the ones previously discussed are presented in Table VII.

## FAILURE MECHANISM OF TTL MSI/LSI CIRCUITS

Standard TTL circuits: AMD's experience as well as that of the Military as reported in RADC Reports and other sources indicate that bond lead wire and package defects account for more than half of device failures. Diffusion and other bulk defect, oxide faults, metallization damage and other die fabrication anomalies cause 10 to 15% of failures. Surface problems contribute 20 to 40%. Die fabrication problems do cause some yield loss but are not time-stress dependent failure mechanisms. Thus assembly anomalies and surface effects are the usual life limiting items.

Schottky/LS Circuits: Schottky diodes made by a simple metal-semiconductor contact have a reverse characteristic that is predominantly edge leakage, Figure 1a. Most Schottky diodes have superimposed on them an annular diffused junction diode of a higher breakdown than that expected of the Schottky diode. This "guard ring" allows the Schottky diode to avalanche breakdown as expected by theory, Figure 1b. In addition non-guard ring Schottky diodes suffer degradation of the reverse leakage characteristics if biased into breakdown repeatly; for this reason our devices are designed so that no user accessible non-guard ring Schottky diodes exist. Other than this anticipated potential problem corrected by design there appear to be no distinct Schottky failure mechanisms in non-aluminum contact Schottky devices.

## SCHOTTKY PROCESSING DETAILS

Processing of Schottky devices is identical to that of TTL devices, with the exception of the gold doping steps, to the point where contact openings have been etched. Following the contact etch, platinum is sputtered to form a uniform deposition across the surface of the wafer. This is followed by a high-temperature sinter to form platinum silicide in each contact window. All unreacted platinum is stripped with an etchant not active on the platinum silicide. Platinum silicide remains in the contact windows and no photomasking was involved, just a selective etch.

The next step is the deposition of the titanium tungsten barrier material followed by the aluminum layer. Both layers are then etched to delineate the circuit intra-connect pattern using standard photomasking techniques.

The entire process seems complicated at first glance because of the three-layer structure that results, but each layer serves a definite purpose.

Platinum silicide forms the actual Schottky barrier junction and produces a reliable diode with stable and predictable characteristics. Platinum could conceivably be used as the current carrying intra-connect metallization but there is no platinum etch compatible with current photomasking materials.

Tungsten is required to prevent the diffusion of aluminum into the platinum silicide junction; however, tungsten alone has a tendency to peel because of poor adherence to the $SiO_2$. The addition of titanium solves the adhesion problem and the resulting composite material has etch characteristics similar to aluminum so that only one photomasking and etch operation is necessary to define the intra-connects, rather than separate operations for Ti-W and A1.

Surface passivation and scratch protection is applied and etched in exactly the same manner as those devices using aluminum metallization only.

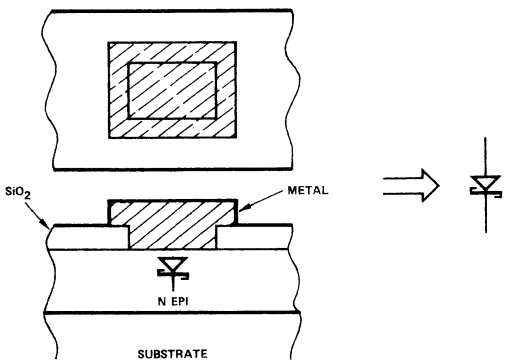
Extensive life test data on this structure proves that it is a repeatable, stable, and reliable process.

## COMMENTS

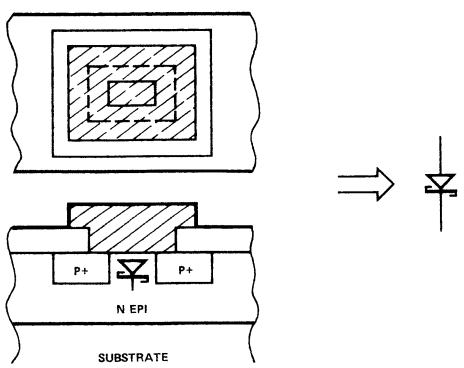
Data has been presented from an ongoing reliability program for Schottky devices. No device failures have occurred in nearly one-half million unit hours of life testing at 125°C. Current data from various sources indicate that I e v is a conservative value for activation energy in calculating acceleration factors. Using this value and a Poisson distribution an equivalent 70°C failure rate of no worse than 0.001% per thousand hours is estimated at a 90% confidence.

Schottky and LS integrated circuits provide improved performance over standard gold-doped TTL devices at the same high reliability experienced with these non-Schottky parts.

a) Discrete Schottky Diode.




b) Discrete Schottky "Guard-Ring" Diode.




c) Schottky Clamped Transistor.

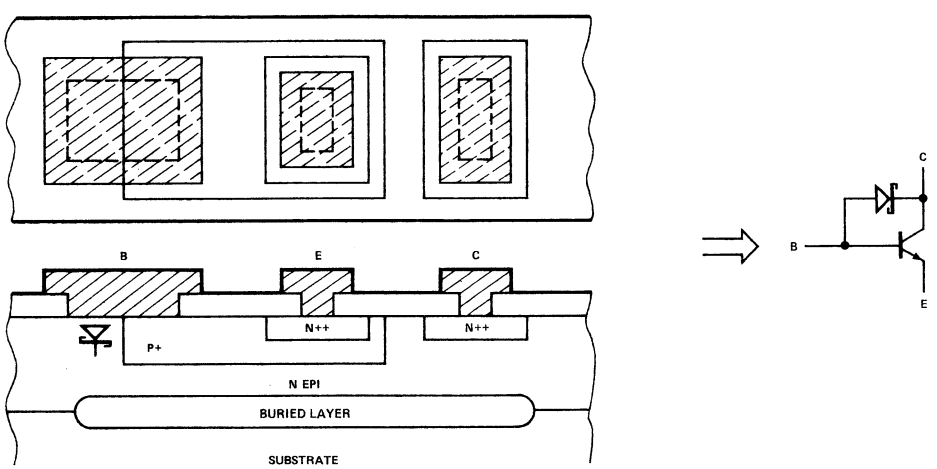



Figure 1. Schottky Device Construction.

TABLE I
LIFE TEST BIAS CONDITIONS

| | |
|---|---|
| Standard Gate<br>Schottky-clamped 2-input TTL NAND gate | Gate ON<br>Output open<br>$V_{CC}$ = 5.0V |
| Phase-Splitter Geometry<br>1.0 mil emitter, non-guard ring Schottky clamp diode | $I_B$ = 1mA<br>$I_C$ = 5mA<br>Emitter = GND |
| Output Geometry<br>4.5 mil emitter, guard-ring Schottky clamp diode | $I_B$ = 4mA<br>$I_C$ = 20mA<br>Emitter = GND |
| Resistors<br>600Ω base resistor in series with a 40Ω emitter resistor. | $I_R$ = 7.8mA |
| Schottky Diode<br>0.5 mil x 3.0 mil, non-guard ring structure | $I_D$ = 10mA |
| Metallization Run<br>0.2 mil by approximately 60 mil | I = 10mA |
| Ambient Temperature | 125°C |

TABLE II
TEST PATTERN GROUP I
11,000 HR DATA SUMMARY

| Structure | Parameter | Average Initial Value | Average \|Delta\| | % Average Delta |
|---|---|---|---|---|
| Standard Gate | $V_{OS}$ | .179V | (−) 1.1mV | .61 |
| | $V_{OL}$ | .398V | (−) 8.3mV | 2.1 |
| | $V_{OH}$ | 2.954V | (+) 6.3mV | .21 |
| | $I_{IH}$ | .317μA | (+) .34μA | 107.0 |
| Phase-Splitter Geometry | $V_{BC}$ | .626V | (+) 5.0mV | .8 |
| | $V_{BE}$ | .827V | (+) 1.4mV | .17 |
| | $V_{SAT}$ | .518V | (+) 1.7mV | .33 |
| | $h_{FE}$ | 58.00 | (−) 3.2 | 5.5 |
| | $I_{CEO}$ | .04μA | .03μA | 83.0 |
| Output Geometry | $V_{BC}$ | .621V | (+) 2.1mV | .34 |
| | $V_{BE}$ | .848V | (+) 2.0mV | .24 |
| | $V_{SAT}$ | .345V | 3.4mV | .99 |
| | $h_{FE}$ | 66.00 | (−) 1.3 | 1.97 |
| | $I_{CEO}$ | .025μA | (−) .023μA | 92.0 |
| Resistors | V | .527V | (+) 4.7mV | .89 |
| Schottky Diode | $V_{SBD}$ @ 100μA | .398V | (+) 8.0V | 2.0 |
| | $V_{SBD}$ @ 10mA | .630V | (+) 3.0mV | .48 |
| | $I_{LK}$ | .08μA | (−) .06μA | 79.0 |
| | $V_{BR}$ | 24.5V | (+) 1.56V | 6.4 |
| Metal Run | V | 117.0mV | (+)42mV | 35.9 |

TABLE III
TEST PATTERN GROUP II
10,000 HR DATA SUMMARY

| Structure | Parameter | Average Initial Value | Average \|Delta\| | % Average Delta |
|---|---|---|---|---|
| Standard Gate | $V_{OS}$ | .249V | (+) 2.3mV | .92 |
| | $V_{OL}$ | .489V | 1.7mV | .35 |
| | $V_{OH}$ | 2.958V | 3.6mV | .12 |
| | $I_{IH}$ | .114μA | (+) .09μA | 81.0 |
| Phase-Splitter Geometry | $V_{BC}$ | .563V | (−) 2.0mV | .36 |
| | $V_{BE}$ | .841V | (+) 2.5mV | .3 |
| | $V_{SAT}$ | .718V | 1.4mV | .19 |
| | $h_{FE}$ | 28.4 | .2 | .7 |
| | $I_{CEO}$ | .298μA | (−) .3μA | 101.0 |
| Output Geometry | $V_{BC}$ | .551V | (+) 4.5mV | .82 |
| | $V_{BE}$ | .849V | (+) 1.9mV | .22 |
| | $V_{SAT}$ | .432V | 1.1mV | .25 |
| | $h_{FE}$ | 62.0 | .5 | .8 |
| | $I_{CEO}$ | 2.03μA | (−) .32μA | 15.8 |
| Resistors | V | .562V | (−) 2.4mV | .46 |
| Schottky Diode | $V_{SBD}$ @ 100μA | .328V | (+) 2.1mV | .64 |
| | $V_{SBD}$ @ 10mA | .566V | (+) 3.0mV | .53 |
| | $I_{LK}$ | .09μA | .09μV | 100.0 |
| | $V_{BR}$ | 24.9V | 97mV | .39 |
| Metal Run | V | 124.0mV | 6.4mV | 5.2 |

TABLE IV
1000 HOUR LIFE TEST DATA
FOR Am25LS161

| Test No. | Parameter | Limit | | Initial Value | | | Delta @ 1000 Hrs. | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| 101 | Input Clamp Voltage | | −1.5 | −.822 | −.839 | −.921 | −.019 | −.027 | −.113 | Volts |
| 141 | Input LOW Current | | −800 | −493 | −576 | −656 | +1.0 | −1.0 | −2.3 | μA |
| 143 | Input HIGH Current @ 2.7V | | 40 | 0 | 0 | 0 | 0 | 0 | 0 | μA |
| 144 | Input HIGH Current @ 7.0V | | 200 | 0 | 0 | 0.9 | 0 | 0 | 1.4 | μA |
| 200 | Output HIGH Voltage | 2.5 | | 3.04 | 3.07 | 3.11 | −.01 | 0 | +.03 | Volts |
| 202 | Output Short-Circuit Current | −15 | −85 | −32.0 | −35.9 | −42.5 | −.8 | −1.4 | −4.2 | mA |
| 204 | Output Leakage Current | − | − | 0 | 0 | 1.0 | 0 | 0 | −1.0 | μA |
| 205 | Output LOW Voltage at $I_{OL}$ = 3mA | | 0.4 | .271 | .295 | .328 | −.007 | 0 | .005 | Volts |
| 206 | Output LOW Voltage at $I_{OL}$ = 4mA | | 0.45 | .223 | .242 | .265 | −.008 | 0 | .005 | Volts |
| 300 | Power-Supply Current, all Outputs HIGH | | 31 | 18.0 | 21.2 | 24.2 | −.20 | 0 | .60 | mA |
| 302 | Power-Supply Current, all Outputs LOW | | 32 | 19.5 | 22.9 | 25.7 | −.20 | 0 | .80 | mA |

## TABLE V
## 1000 HOUR LIFE TEST DATA
## FOR Am74LS174

| Parameter | Typical Initial Value | Average Percent Change |
|---|---|---|
| Substrate Leakage | 0μA | 0 |
| Min $V_{CC}$ to Function | 2.19V | 0 |
| Schottky Voltage @ 100μA | .484V | 0 |
| $V_{OH}$, Output High Voltage | 2.92V | −.11 |
| $I_{SC}$, Short-Circuit Output Current | 26.38mA | 0.3 |
| $I_{CEX}$, Output Leakage | 7.85μA | 0 |
| $V_{OL1}$, Output Low Voltage @ 4mA | .270V | 0.05 |
| $V_{OL2}$, Output Low Voltage @ 8mA | .328V | 0 |
| $I_{IL}$, Input Low Current | 171μA | −0.9 |
| $V_{th}$, Input Threshold Voltage | 1.015V | 0.2 |
| $I_{IH}$, Input Leakage | .04μA | −12 |
| $I_{IB}$, Input Breakdown Current | 0μA | 0 |
| $V_{IC}$, Input Clamp Diode | .894V | 0.6 |
| $I_{CC}$, Supply Current @ 5.5V | 13.54mA | 0.3 |
| $I_{CM}$, Supply Current @ 7V | 18.46mA | 0 |
| $t_{pd+}$, CP to $Q_o$ | 11.99ns | 0 |
| $t_{pd-}$, CP to $Q_o$ | 11.44ns | 0.1 |

## TABLE VI
## 1000 HOUR LIFE TEST DATA
## FOR Am74LS157

| Parameter | Typical Initial Value | Average Percent Change |
|---|---|---|
| Substrate Leakage | .7μA | 0 |
| Min $V_{CC}$ to Function | 2.84V | 0.09 |
| Schottky Voltage @ 100μA | .452V | 0.2 |
| $V_{OH}$, Output HIGH Voltage 2.92V | 2.92V | 0 |
| $I_{SC}$, Short-Circuit Output Current | 26.4mA | 0.3 |
| $I_{CEX}$, Output Leakage | 0μA | 0 |
| $V_{OL1}$, Output Low Voltage @ 4mA | .277V | 0 |
| $V_{OL2}$, Output Low Voltage @ 8mA | .331V | 0 |
| $I_{IL}$, Input Low Current | 313μA | 0.3 |
| $V_{th}$, Input Threshold Voltage | 1.08V | 0 |
| $I_{IH}$, Input Leakage | 0.5μA | 0 |
| $I_{IB}$, Input Breakdown Current | 0μA | 0 |
| $V_{IC}$, Input Clamp Diode | .837V | 0 |
| $I_{CC}$, Supply Current @ 5.5V | 10.1mA | 0 |
| $I_{CM}$, Supply Current @ 7V | 13.48mA | 0 |
| $t_{pd+}$, 1A to 1Y | 5.1ns | 0.3 |
| $t_{pd-}$, 1A to 1Y | 5.4ns | 0 |

## TABLE VII
## 125°C LIFE TEST DATA

| Device | Test Type | No. Parts | Hours on Test | Thousand Unit Hours | Failures | 70°C Equivalent Failure Rate* |
|---|---|---|---|---|---|---|
| Test Pattern I | Design | 22 | 11,000 Hr. | 242 | 0 | 0.008% per thousand hours |
| Test Pattern II | Design | 22 | 10,000 Hr. | 220 | 0 | 0.009 |
| 74LS174 | Param. Drift | 20 | 2,000 Hr. | 80 | 0 | 0.02 |
| 74LS175 | Param. Drift | 20 | 2,000 Hr. | 80 | 0 | 0.02 |
| 25LS161 | Param. Drift | 100 | 1,000 Hr. | 100 | 0 | 0.02 |
| 74LS157 | Group C Life | 77 | 1,000 Hr. | 77 | 0 | 0.02 |
| 74LS161 | Group C Life | 77 | 1,000 Hr. | 77 | 0 | 0.02 |
| 74LS193 | Group C Life | 77 | 1,000 Hr. | 77 | 0 | 0.02 |
| TOTAL DEVICE – 371 | | | | 491 | 0 | 0.001 |

*Equivalent failure rate at 70°C calculated from Poisson distribution of a zero defect sample and activation energy or 1.0 ev for acceleration factor. Equivalent failure is not greater than the quoted value at 90% confidence.

2

# LOW-POWER SCHOTTKY LS-MSI/LSI DATA SHEETS



## APPLICATION NOTES

## DEFINITION OF A.C. SWITCHING TERMS

(All switching times are measured at the 1.3V logic level unless otherwise noted.)

$f_{MAX}$ The highest operating clock frequency.

$t_{PLH}$ The propagation delay time from an input change to an output LOW-to-HIGH transition.

$t_{PHL}$ The propagation delay time from an input change to an output HIGH-to-LOW transition.

$t_{PW}$ Pulse width. The time between the leading and trailing edges of a pulse.

$t_r$ Rise time. The time required for a signal to change from 10% to 90% of its measured values.

$t_f$ Fall time. The time required for a signal to change from 90% to 10% of its measured values.

$t_s$ Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

$t_h$ Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

$t_R$ Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

$t_{HZ}$ HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5 V change).

$t_{LZ}$ LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5 V change).

$t_{ZH}$ Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

$t_{ZL}$ Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

## DEFINITION OF D.C. TERMS

**H** HIGH, applying to a HIGH voltage level.

**L** LOW, applying to a LOW voltage level.

**I** Input.

**O** Output.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

$I_{IL}$ LOW-level input current with a specified LOW-level voltage applied.

$I_{IH}$ HIGH-level input current with a specified HIGH-level voltage applied.

$I_{OL}$ LOW-level output current.

$I_{OH}$ HIGH-level output current.

$I_{SC}$ Output short-circuit source current.

$I_{CC}$ The supply current drawn by the device from the $V_{CC}$ power supply.

$V_{IL}$ Logic LOW input voltage.

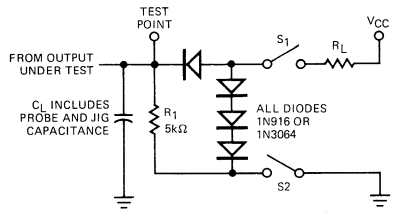
$V_{IH}$ Logic HIGH input voltage.

$V_{OL}$ LOW-level output voltage with $I_{OL}$ applied.

$V_{OH}$ HIGH-level output voltage with $I_{OH}$ applied.

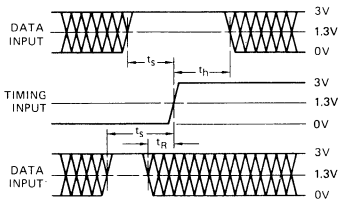
## LOW-POWER SCHOTTKY PARAMETER MEASUREMENTS

### LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



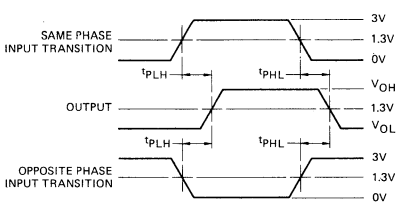

Note: For standard totem-pole outputs, remove $R_1$; $S_1$ and $S_2$ closed.

### SET-UP, HOLD, AND RELEASE TIMES

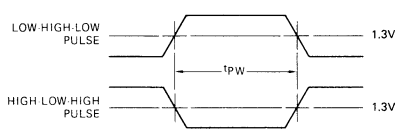



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

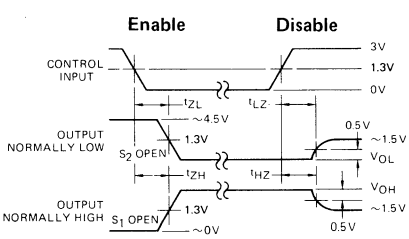
### PROPAGATION DELAY




### PULSE WIDTH




### ENABLE AND DISABLE TIMES




Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. $S_1$ and $S_2$ of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o$ = 50Ω; $t_r$ ≤ 15ns; $t_f$ ≤ 6ns.

3

# Am25LS07•Am25LS08

## Hex/Quad Parallel D Registers With Register Enable

### DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit parallel registers
- Common Clock and Common Enable
- Positive edge triggered D flip flops
- Am25LS d. c. parameters including:
  $V_{OL}$ = 0.45V at $I_{OL}$ = 8mA
  Fan-out over military range = 22
  440$\mu$A source current
- Second sourced by TI as 54LS/74LS378 and 379
- 100% product assurance screening to MIL-STD-883 requirements

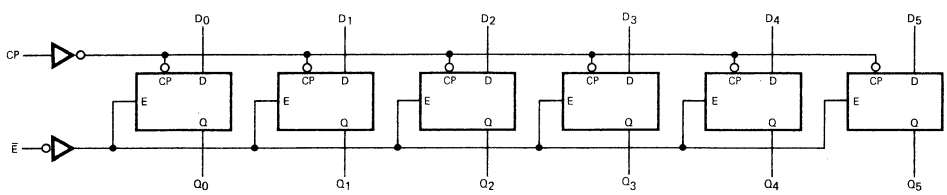
### FUNCTIONAL DESCRIPTION

The Am25LS07 is a 6-bit Low Power Schottky register with a buffered common register enable. The Am25LS08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54LS/74LS174 and Am54LS/74LS175 but feature the common register enable rather than common clear.

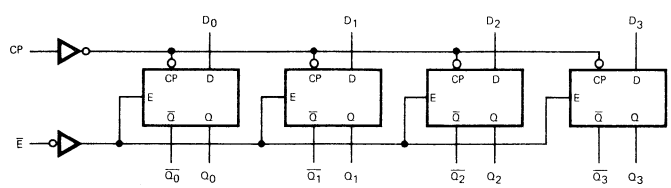
Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

### LOGIC DIAGRAMS

**Am25LS07**

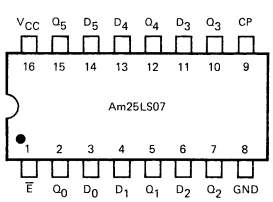



**Am25LS08**

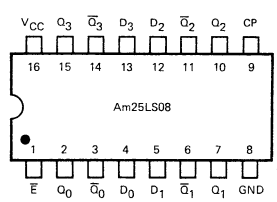



### CONNECTION DIAGRAMS
**Top Views**

**Am25LS07**



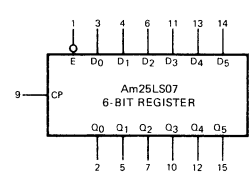

**Am25LS08**



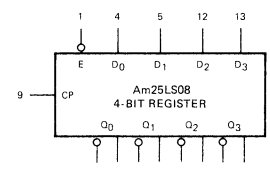

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOLS

**Am25LS07**




**Am25LS08**




$V_{CC}$ = Pin 16
GND = Pin 8

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | COM'L | 2.7 | 3.4 | | Volts |
| | | | MIL | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Clock, $\overline{E}$ | | | −0.36 | mA |
| | | | Others | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Clock, $\overline{E}$ | | | 20 | μA |
| | | | Others | | | 14 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | LS07 | | 16 | 22 | mA |
| | | | LS08 | | 11 | 18 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

3

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 13 | 20 | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | Clock to Output | | 13 | 20 | ns | |
| $t_{pw}$ | Clock Pulse Width | 17 | | | ns | |
| $t_s$ | Data | 20 | | | ns | |
| $t_s$ | Enable | 30 | | | ns | |
| $t_h$ | Data | 5.0 | | | ns | |
| $t_h$ | Enable | 5.0 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 40 | 65 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 30 | | 35 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Output | | 30 | | 35 | ns | |
| $t_{pw}$ | Clock Pulse Width | 26 | | 30 | | ns | |
| $t_s$ | Data | 30 | | 35 | | ns | |
| $t_s$ | Enable | 43 | | 50 | | ns | |
| $t_h$ | Data | 11 | | 12 | | ns | |
| $t_h$ | Enable | 11 | | 12 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 30 | | 25 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The D flip-flop data inputs.

**$\overline{E}$** Enable. When the enable is LOW, data on the $D_i$ inputs is transferred to the $Q_i$ outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the $Q_i$ outputs do not change regardless of the data or clock input transitions.

**CP** Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

**$Q_i$** The TRUE register outputs.

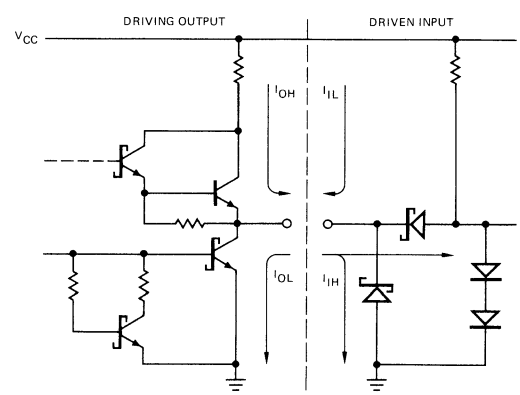
**$\overline{Q}_i$** The complement register outputs

## FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{E}$ | $D_i$ | CP | $Q_i$ | $\overline{Q}_i$ |
| H | X | X | NC | NC |
| L | X | H | NC | NC |
| L | X | L | NC | NC |
| L | L | ↑ | L | H |
| L | H | ↑ | H | L |

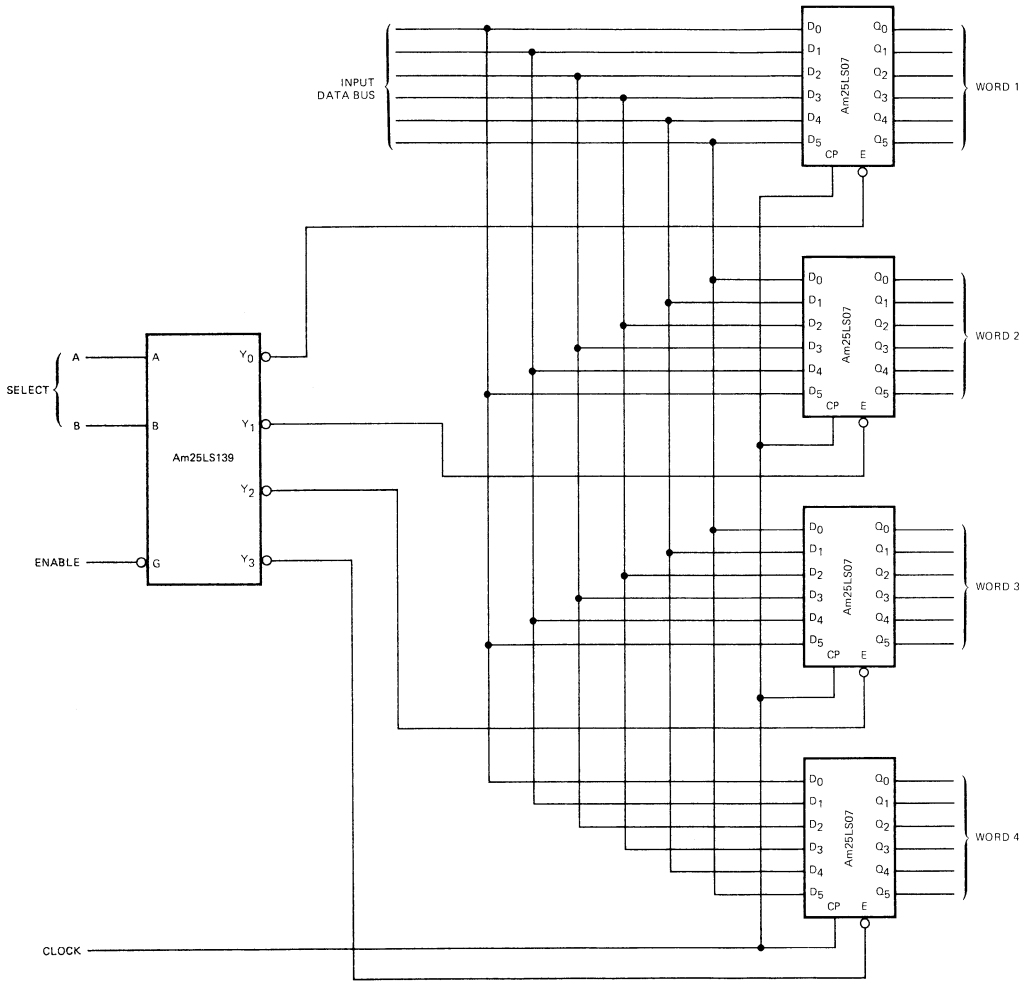
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25LS08 Only

## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

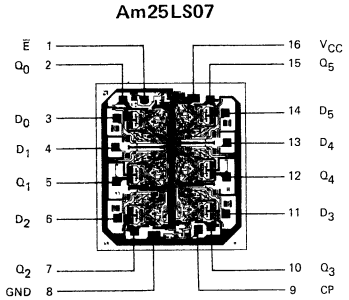
## APPLICATION




**Selective Register Loading of Data on Synchronous Clock.**

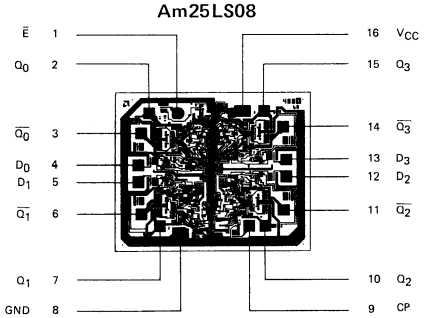
## Metallization and Pad Layout

### Am25LS07




DIE SIZE 0.075" X 0.084"

### Am25LS08




DIE SIZE 0.075" X 0.061"

# Am25LS09

## Quad Two-Input, High-Speed Register

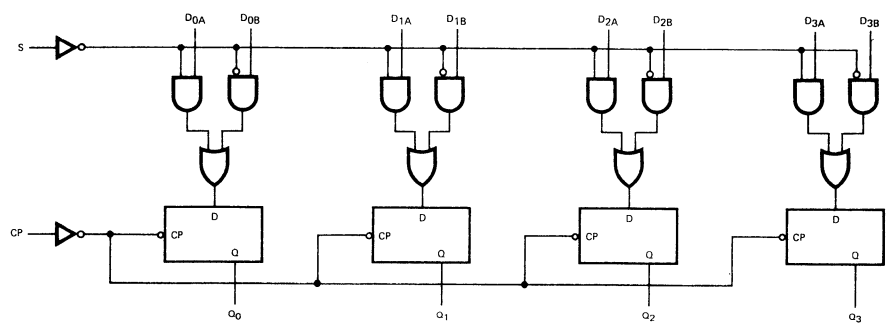
### DISTINCTIVE CHARACTERISTICS

- 4-bit register accepts data from one-of-two 4-bit input fields
- Edge triggered clock action
- Second sourced by T.I. as 54LS/74LS399
- Am25LS d.c. parameters including:
  - $V_{OL}$ = 0.45V at $I_{OL}$ = 8mA
  - Fan-out over military range = 22
  - 440$\mu$A source current
- 100% product assurance screening to MIL-STD-883 requirements

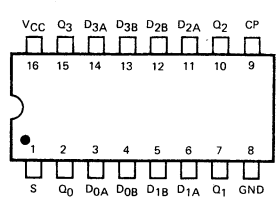
### FUNCTIONAL DESCRIPTION

The Am25LS09 is a dual port four-bit register using advanced Low Power Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the $D_{iA}$ input data will be stored in the register. When the S input is HIGH, the $D_{iB}$ input data will be stored in the register.

### LOGIC DIAGRAM

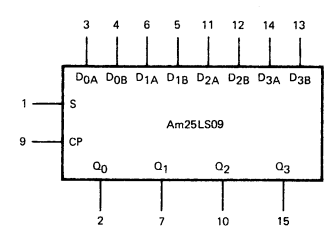



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | COM'L | 2.7 | 3.4 | | Volts |
| | | | MIL | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Clock, S | | | −0.36 | mA |
| | | | Others | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Clock, S | | | 20 | μA |
| | | | Others | | | 14 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 11 | 18 | mA |

Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

3

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Q HIGH | | 13 | 20 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Q LOW | | 13 | 20 | ns | |
| $t_{pw}$ | Clock Pulse Width | 17 | | | ns | |
| $t_s$ | Data Set-up Time | 20 | | | ns | |
| $t_s$ | Select Input Set-up Time | 30 | | | ns | |
| $t_h$ | Data Hold Time | 5 | | | ns | |
| $t_h$ | Select Input Hold Time | 0 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 40 | | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Q HIGH | | 30 | | 35 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Q LOW | | 30 | | 35 | ns | |
| $t_{pw}$ | Clock Pulse Width | 26 | | 30 | | ns | |
| $t_s$ | Data Set-up Time | 30 | | 35 | | ns | |
| $t_s$ | Select Input Set-up Time | 43 | | 50 | | ns | |
| $t_h$ | Data Hold Time | 11 | | 12 | | ns | |
| $t_h$ | Select Input Hold Time | 4 | | 5 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 30 | | 25 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

$D_{0A}$, $D_{1A}$, $D_{2A}$, $D_{3A}$ The "A" word into the two-input multiplexer of the D flip-flops.

$D_{0B}$, $D_{1B}$, $D_{2B}$, $D_{3B}$ The "B" word into the two-input multiplexer of the D flip-flops.

$Q_0$, $Q_1$, $Q_2$, $Q_3$ The outputs of the four D-type flip-flops of the register.

**S** Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

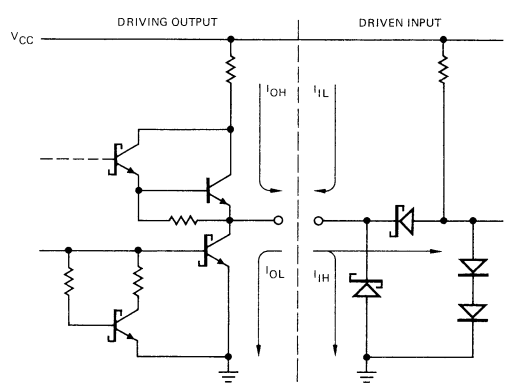
**CP** Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

## FUNCTION TABLE

| SELECT S | CLOCK CP | DATA $D_{iA}$ | INPUTS $D_{iB}$ | OUTPUT $Q_i$ |
|---|---|---|---|---|
| L | ↑ | L | X | L |
| L | ↑ | H | X | H |
| H | ↑ | X | L | L |
| H | ↑ | X | H | H |

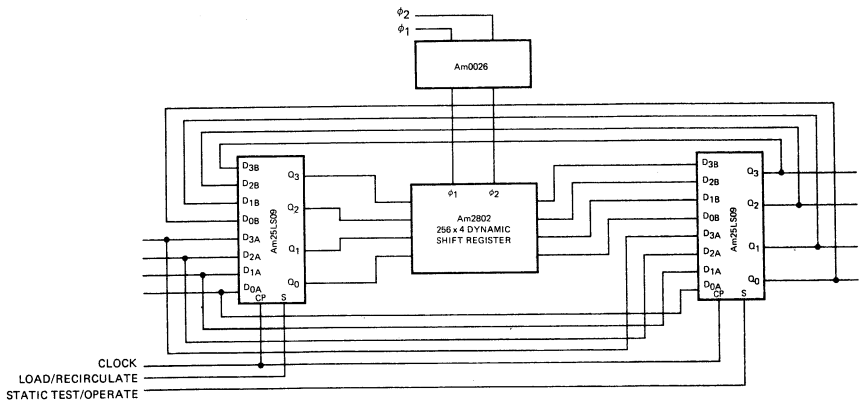
H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

## Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

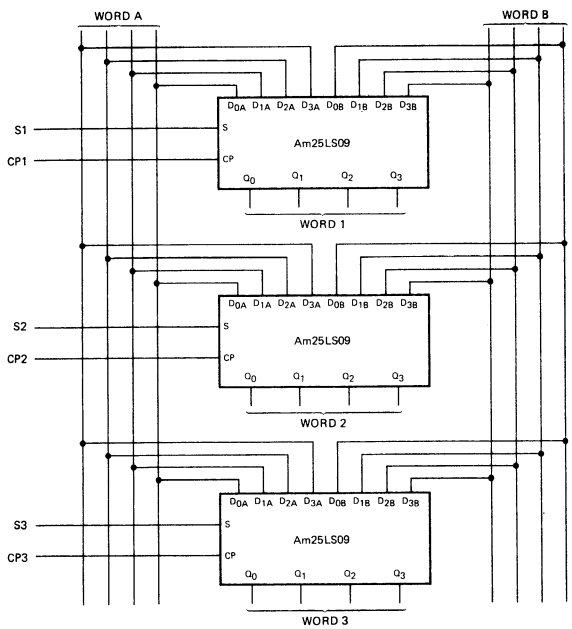



Note: Actual current flow direction shown.

## APPLICATIONS

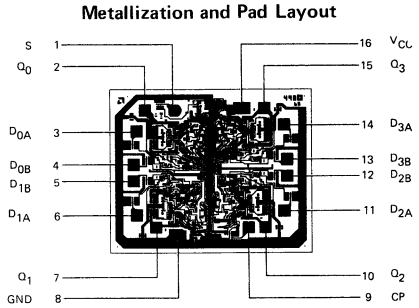



Am25LS09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.




Am25LS09 used to store a word from either data bus A or data bus B.

### Metallization and Pad Layout




DIE SIZE 0.075" X 0.061"

# Am25LS14

## 8-Bit Serial/Parallel Two's Complement Multiplier

### DISTINCTIVE CHARACTERISTICS

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-bit parallel multiplicand data input
- 25MHz minimum clock frequency
- Second sourced by T.I. as the SN54LS/74LS384
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

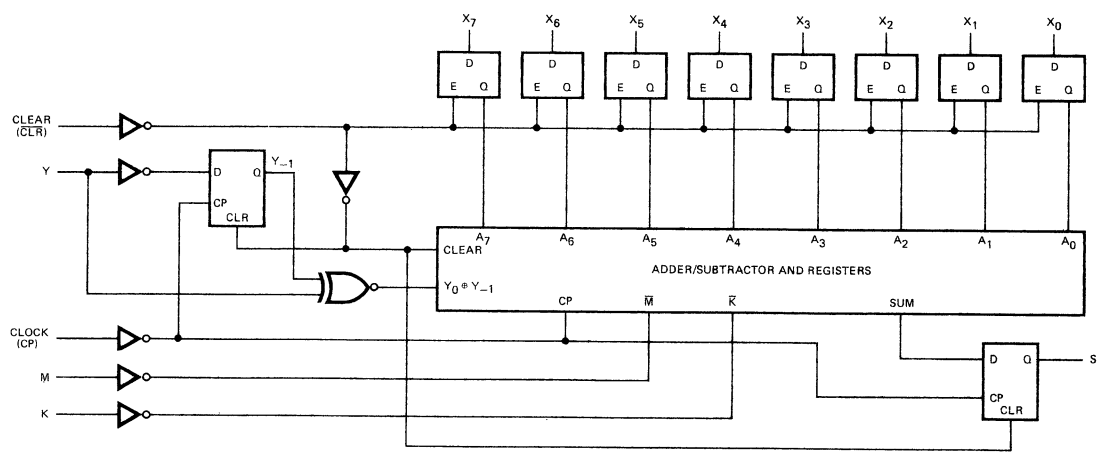
The Am25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream — least significant bit first. The product is clocked out the S output least significant bit first.

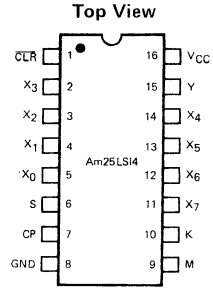
The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

### LOGIC DIAGRAM

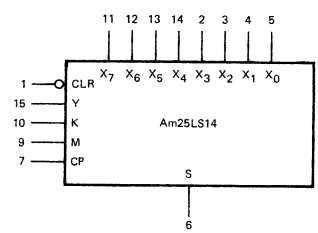



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am25LS14XC | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am25LS14XM | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -1.0mA$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 8.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 12mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | X, M | | | −0.48 | mA |
| | | | K, $\overline{CLR}$ | | | −1.2 | |
| | | | CP | | | −1.6 | |
| | | | Y | | | −3.2 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | X, M | | | 20 | μA |
| | | | K, $\overline{CLR}$ | | | 30 | |
| | | | CP | | | 40 | |
| | | | Y | | | 80 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 5.5V$ | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | | 91 | 155 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Duration of the short circuit test should not exceed one second.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 13 | 20 | ns | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 13 | 20 | | |
| $t_{PHL}$ | Clear to Output | | 17 | 25 | ns | |
| $t_s$ | Y to Clock | 32 | | | ns | |
| $t_h$ | | 0 | | | | |
| $t_s$ | K to Clock | 18 | | | ns | |
| $t_h$ | | 0 | | | | |
| $t_s$ | $X_i$ to Clear | 13 | | | ns | |
| $t_h$ | | 0 | | | | |
| $t_{pw}$ | Clock (HIGH) | 15 | | | ns | |
| | Clock (LOW) | 15 | | | | |
| $t_{pw}$ | Clear Pulse Width | 20 | | | ns | |
| $t_s$ | Clear Recovery Time (Inactive State) | 18 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 25 | 30 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L<br>$T_A$ = 0°C to +70°C<br>$V_{CC}$ = 5.0V ± 5% | | Am25LS MIL<br>$T_A$ = −55°C to +125°C<br>$V_{CC}$ = 5.0V ± 10% | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ | Clock to Output | | 24 | | 27 | ns | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 27 | | 30 | | |
| $t_{PHL}$ | Clear to Output | | 33 | | 37 | ns | |
| $t_s$ | Y to Clock | 38 | | 45 | | ns | |
| $t_h$ | | 0 | | 0 | | | |
| $t_s$ | K to Clock | 24 | | 30 | | ns | |
| $t_h$ | | 0 | | 0 | | | |
| $t_s$ | $X_i$ to Clear | 19 | | 23 | | ns | |
| $t_h$ | | 0 | | 0 | | | |
| $t_{pw}$ | Clock (HIGH) | 18 | | 22 | | ns | |
| | Clock (LOW) | 18 | | 22 | | | |
| $t_{pw}$ | Clear Pulse Width | 33 | | 38 | | ns | |
| $t_s$ | Clear Recovery Time (Inactive State) | 20 | | 30 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 20 | | 15 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$X_0$, $X_1$, $X_2$, $X_3$, $X_4$, $X_5$, $X_6$, $X_7$** The eight data inputs for the multiplicand (X) data.

**Y** The serial input for the multiplier (Y) data—least significant bit first.

**S** The serial output for the product of X • Y—least significant bit first.

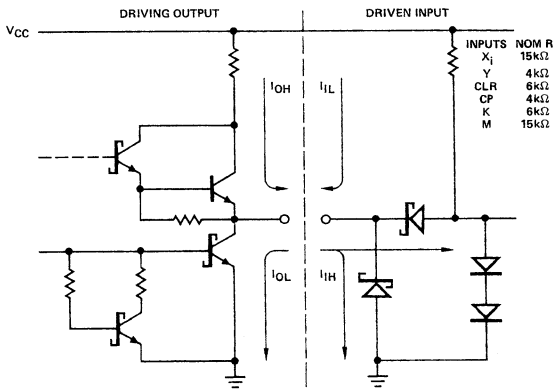
**CP** Clock. The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.

**CLR** Clear. The buffered common clear for all flip-flops within the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.

**K** The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.

**M** The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



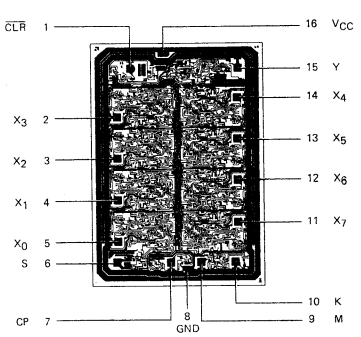

Note: Actual current flow direction shown.

## FUNCTION TABLE

| INPUTS | | | | | | INTERNAL | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CP | K | M | $X_i$ | Y | $Y_{-1}$ | S | |
| – | – | L | L | – | – | – | – | Most Significant Multiplier Device |
| – | – | CS | H | – | – | – | – | Devices Cascaded in Multiplier String |
| L | – | – | – | OP | – | L | L | Load New Multiplicand and Clear Internal Sum and Carry Registers |
| H | – | – | – | – | – | – | – | Device Enabled |
| H | ↑ | – | – | – | L | L | AR | Shift Sum Register |
| H | ↑ | – | – | – | L | H | AR | Add Multiplicand to Sum Register and Shift |
| H | ↑ | – | – | – | H | L | AR | Subtract Multiplicand from Sum Register and Shift |
| H | ↑ | – | – | – | H | H | AR | Shift Sum Register |

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = $X_i$ latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

### Metallization and Pad Layout



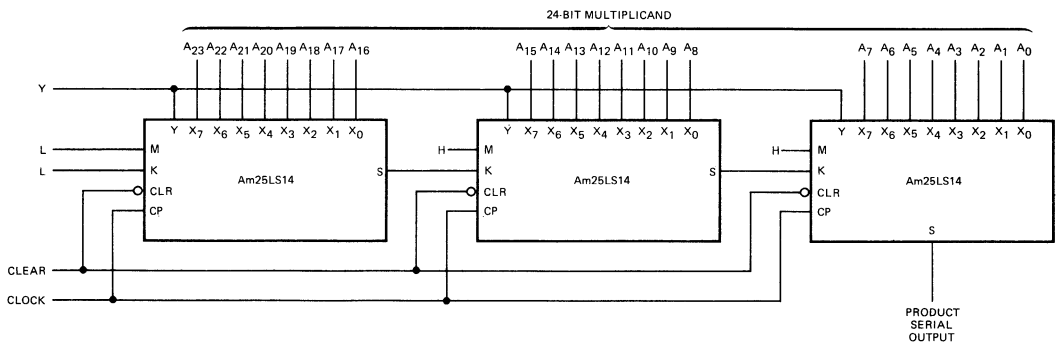

DIE SIZE 0.097" X 0.137"

## ORDERING INFORMATION

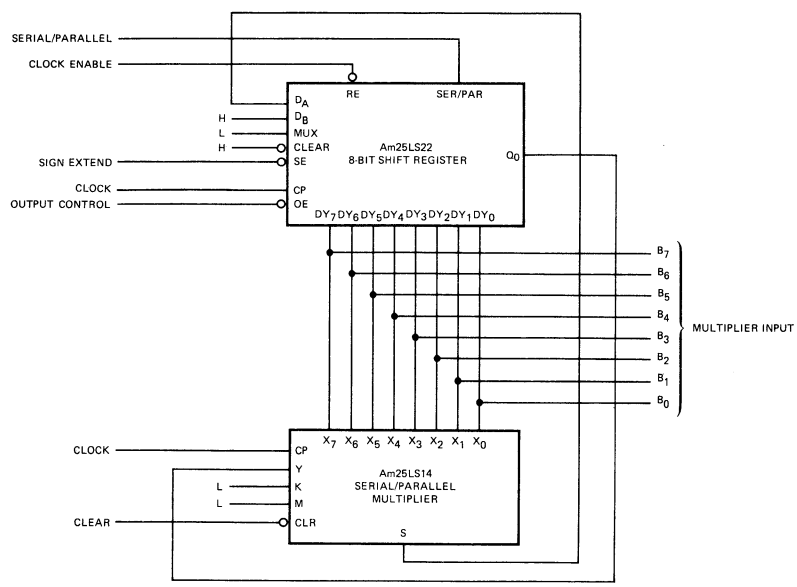
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS14PC |
| Hermetic DIP | 0°C to +70°C | AM25LS14DC |
| Dice | 0°C to +70°C | AM25LS14XC |
| Hermetic DIP | −55°C to +125°C | AM25LS14DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS14FM |
| Dice | −55°C to +125°C | AM25LS14XM |

## APPLICATIONS

See also Digital Signal Processing Applications Section for more information.




**Basic 24-Bit Serial/Parallel Connection**




**8-Bit by 8-Bit Multiplier, Bus Organized, with 8-Bit Truncated Product**

# Am25LS15
## Quad Serial Adder/Subtractor

### DISTINCTIVE CHARACTERISTICS

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Second sourced by T.I. as Am54LS/74LS385
- 100% product assurance screening to MIL-STD-883 requirements

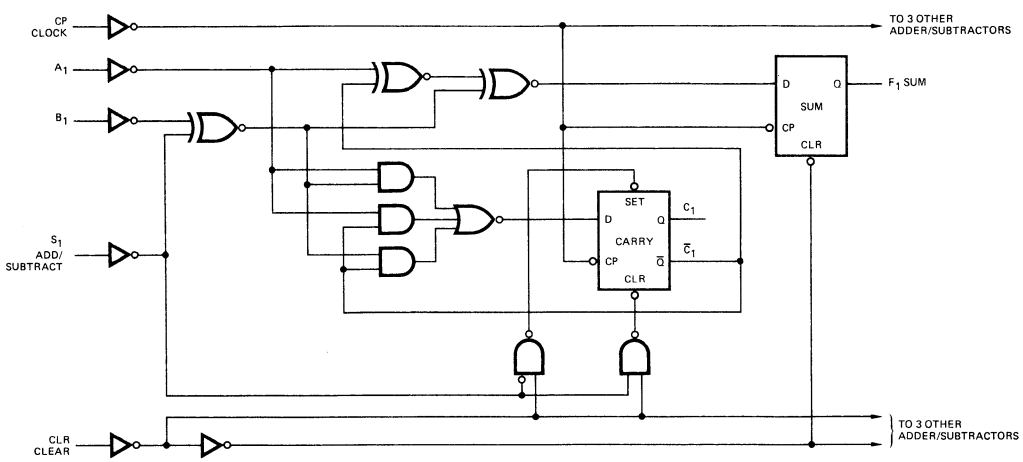
### FUNCTIONAL DESCRIPTION

The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

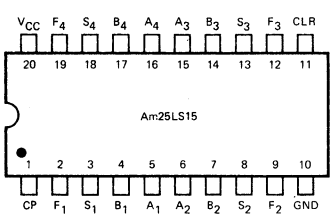
Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

### LOGIC DIAGRAM
(One of Four Similar Functions)

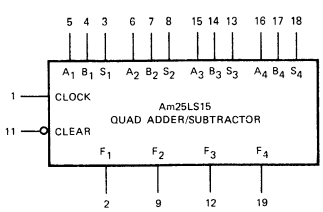



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | |
|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | (MIN. = 4.75V MAX. = 5.25V) |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | (MIN. = 4.50V MAX. = 5.50V) |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | | | Volts |
| | | | COM'L | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 48 | 75 | mA |

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 14 | 22 | ns | $C_L = 15pF$<br>$R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | | 14 | 22 | | |
| $t_{PHL}$ | Clear to Output | | | 20 | 30 | ns | |
| $t_s$ | A, B, S | | 10 | | | ns | |
| $t_h$ | | | 0 | | | | |
| $t_s$ | Clear Recovery | | 25 | | | ns | |
| $t_h$ | Clear Hold Time | | 0 | | | ns | |
| $t_{pw}$ | Clock | HIGH | 17 | | | ns | |
| | | LOW | 17 | | | | |
| $t_{pw}$ | Clear LOW | | 20 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | | 30 | 40 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on the $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 33 | | 38 | ns | $C_L$ = 50pF $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 33 | | 38 | | |
| $t_{PHL}$ | Clear to Output | | | 43 | | 50 | ns | |
| $t_s$ | A, B, S | | 17 | | 20 | | ns | |
| $t_h$ | | | 4 | | 5 | | | |
| $t_s$ | Clear Recovery | | 37 | | 42 | | ns | |
| $t_h$ | Clear Hold Time | | 4 | | 5 | | ns | |
| $t_{pw}$ | Clock | HIGH | 26 | | 30 | | ns | |
| | | LOW | 26 | | 30 | | | |
| $t_{pw}$ | Clear LOW | | 30 | | 35 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | | 23 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$A_1$, $A_2$, $A_3$, $A_4$** The "A" input into each adder/subtractor

**$B_1$, $B_2$, $B_3$, $B_4$** The "B" input into each adder/subtractor

**$S_1$, $S_2$, $S_3$, $S_4$** The add subtract control for each adder/subtractor. When S is LOW, the F function is A+B. When S is HIGH, the F function is A−B.

**$F_1$, $F_2$, $F_3$, $F_4$** The four independent serial outputs of the adder/subtractor.

**CP Clock** The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

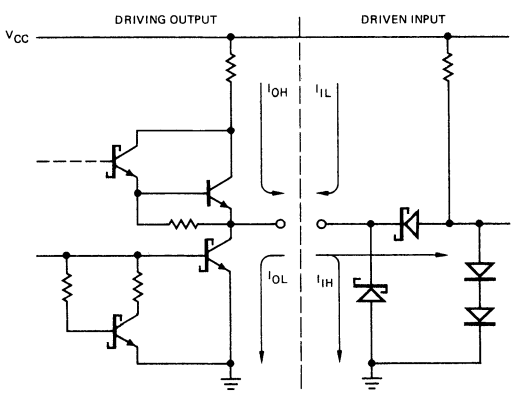
**CLR Clear** When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

## FUNCTION TABLE

| External Inputs | | | | | Internal Point | | Output | |
|---|---|---|---|---|---|---|---|---|
| CP | CLR | S | A | B | C | $C_1$ | F | Function |
| X | L | L | X | X | L | L | L | Clear |
| X | L | H | X | X | H | H | L | |
| L | H | X | X | X | NC | NC | NC | |
| H | H | X | X | X | NC | NC | NC | |
| ↑ | H | L | L | L | L | L | L | |
| ↑ | H | L | L | L | H | L | H | |
| ↑ | H | L | L | H | L | L | H | |
| ↑ | H | L | L | H | H | H | L | Add |
| ↑ | H | L | H | L | L | L | H | |
| ↑ | H | L | H | L | H | H | L | |
| ↑ | H | L | H | H | L | H | L | |
| ↑ | H | L | H | H | H | H | H | |
| ↑ | H | H | L | L | L | L | H | |
| ↑ | H | H | L | L | H | H | L | |
| ↑ | H | H | L | H | L | L | L | |
| ↑ | H | H | L | H | H | L | H | Subtract |
| ↑ | H | H | H | L | L | H | L | |
| ↑ | H | H | H | L | H | H | H | |
| ↑ | H | H | H | H | L | L | H | |
| ↑ | H | H | H | H | H | H | L | |

C = Data In the Carry Flip-Flop Before the Clock Transition
$C_1$ = Data In the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## APPLICATIONS

The normal butterfly network associated with the Cooley-Tukey Fast Fourier Transform (FFT) algorithm is shown below. Here we assume A, B, C, D and W are all complex numbers such that:

$A = A_R + jA_I$

$B = B_R + jB_I$

$W = W_R + jW_I$

The outputs C and D are also complex numbers and are evaluated as:

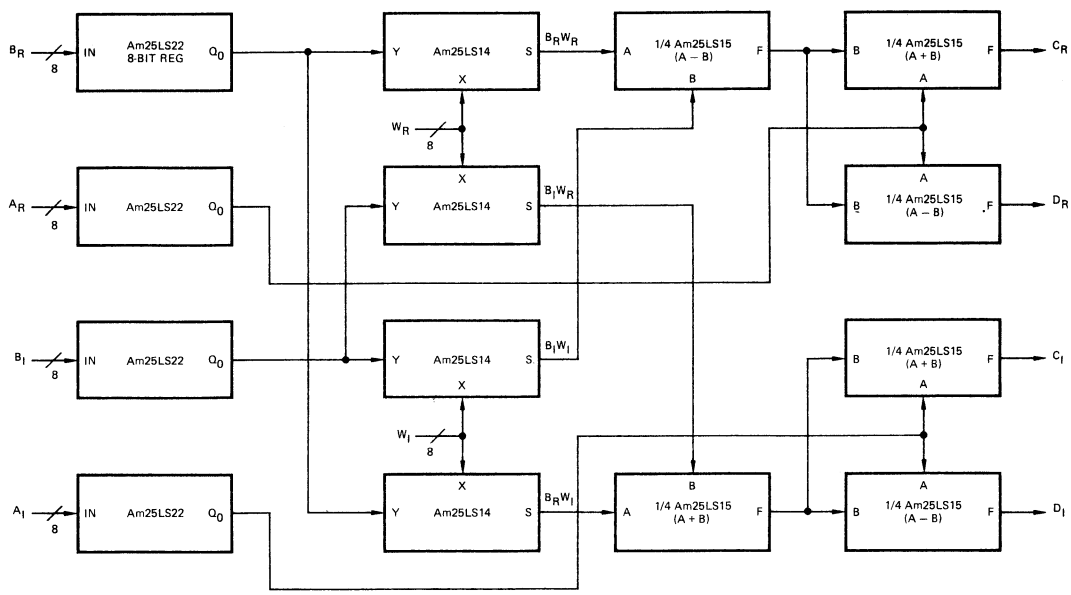
$C = C_R + jC_I = (A_R + B_R W_R - B_I W_I) + j(A_I + B_R W_I + B_I W_R)$

$D = C_R + jD_I = (A_R - B_R W_R + B_I W_I) + j(A_I - B_R W_I - B_I W_R)$

The four multiplications can be implemented using four Am25LS14 serial-parallel multipliers (the appropriate number of bits must, of course, be used). The additions and the subtractions are implemented using the Am25LS15 quad serial adder/subtractors. This diagram depicts only the basic data flow; binary weighting of the numbers, rounding, truncation, etc. must be handled as required by the individual design parameters.

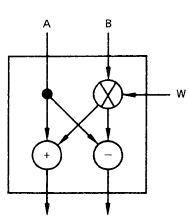
Also see Digital Signal Processing Applications section for more information.

### FAST FOURIER TRANSFORM (FFT) BUTTERFLY

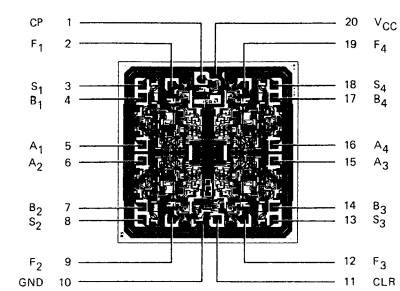



An FFT butterfly connection for complex arithmetic inputs and outputs.

### Functional Diagram for FFT Butterfly Connection




### Metallization and Pad Layout




DIE SIZE 0.095" X 0.095"

# Am25LS22

## 8-Bit Serial/Parallel Register With Sign Extend

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322
- 100% product assurance screening to MIL-STD-883 requirements

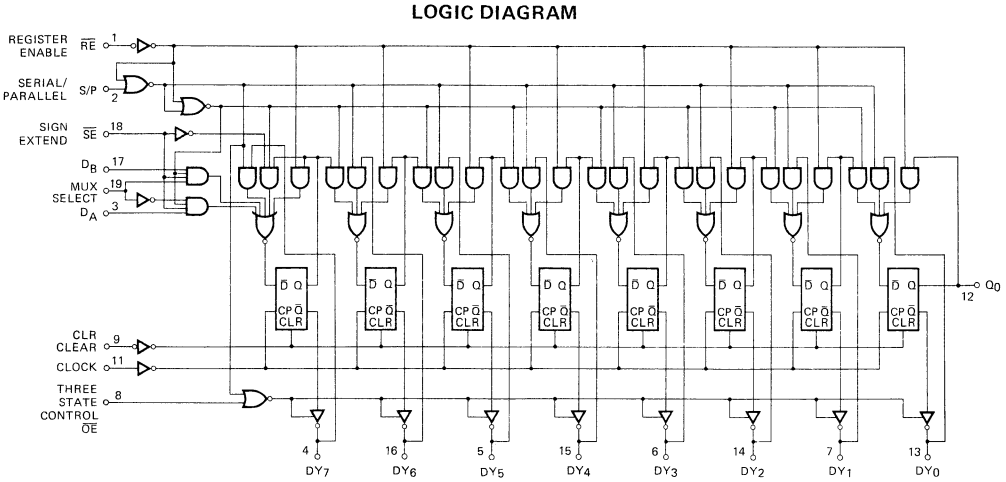
### FUNCTIONAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input $D_A$ or $D_B$. A serial output, $Q_0$, is also provided.

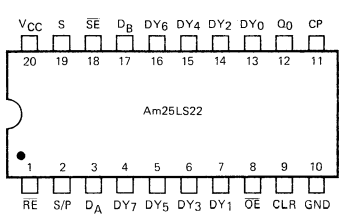
The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines ($DY_i$) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the $Q_7$ flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either $D_A$ or $D_B$ can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

### LOGIC DIAGRAM

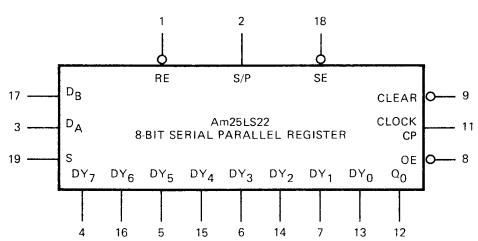



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $Q_0$, $I_{OH} = -440\mu A$ | MIL | 2.5 | | | Volts |
| | | | | COM'L | 2.7 | | | |
| | | | $DY_i$, $I_{OH} = -1.0mA$ | MIL | 2.4 | | | |
| | | | $DY_i$, $I_{OH} = -2.6mA$ | COM'L | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | $\overline{SE}$ | | | −1.08 | mA |
| | | | | S | | | −0.72 | |
| | | | | Others | | | −0.36 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ (Except $DY_i$) | | $\overline{SE}$ | | | 60 | µA |
| | | | | S | | | 40 | |
| | | | | Others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., (Except $DY_i$) | $V_{IN} = 7.0V$ | $\overline{OE}$, S/P, RE, CP, CLR | | | 0.1 | mA |
| | | | $V_{IN} = 5.5V$ | $\overline{SE}$ | | | 0.3 | |
| | | | | S | | | 0.2 | |
| | | | | Others | | | 0.1 | |
| $I_{OZ}$ | Off State (High Impedance) Output Current ($DY_i$) | $V_{CC}$ = MAX. | | $V_O = 2.4V$ | | | 40 | µA |
| | | | | $V_O = 0.4V$ | | | −100 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | | | 40 | 65 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage ($\overline{OE}$, S/P, RE, CP, CLR) | −0.5V to +7.0V |
| DC Input Voltage (Others) | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $DY_i$ | | 16.5 | 24 | ns | $R_L$ = 2.0kΩ, $C_L$ = 15pF |
| $t_{PHL}$ | | | 18 | 26 | | |
| $t_{PHL}$ | Clear to $DY_i$ | | 23 | 30 | ns | |
| $t_{PLH}$ | Clock to $Q_0$ | | 16.5 | 24 | ns | |
| $t_{PHL}$ | | | 18 | 26 | | |
| $t_{PHL}$ | Clear to $Q_0$ | | 23 | 30 | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $DY_i$ | | 13 | 21 | ns | |
| $t_{ZL}$ | | | 18 | 26 | | |
| $t_{HZ}$ | | | 13 | 21 | | $R_L$ = 2.0kΩ, $C_L$ = 5pF |
| $t_{LZ}$ | | | 18 | 26 | | |
| $t_{ZH}$ | SER/PAR to $DY_i$ | | 18 | 26 | ns | $R_L$ = 2.0kΩ, $C_L$ = 15pF |
| $t_{ZL}$ | | | 23 | 32 | | |
| $t_{HZ}$ | | | 18 | 26 | | $R_L$ = 2.0kΩ, $C_L$ = 5pF |
| $t_{LZ}$ | | | 23 | 32 | | |
| $t_s$ | RE to Clock | 20 | | | ns | $R_L$ = 2.0kΩ, $C_L$ = 15pF |
| $t_s$ | SE to Clock | 10 | | | | |
| $t_s$ | S to Clock | 15 | | | | |
| $t_s$ | $D_A$ and $D_B$ to Clock | 15 | | | | |
| $t_s$ | $DY_i$ (Load) to Clock | 15 | | | | |
| $t_s$ | Clear Recovery to Clock | 8.0 | | | | |
| $t_s$ | S/P to Clock | 15 | | | ns | |
| $t_h$ | Any Input | 0 | | | | |
| $t_h$ | Clear Hold | 0 | | | ns | |
| $t_{pw}$ | Clock HIGH | 8.0 | | | ns | |
| | Clock LOW | 8.0 | | | | |
| $t_{pw}$ | Clear | 20 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 35 | 50 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

3

## FUNCTION TABLE

| Mode | INPUTS | | | | | | | OUTPUTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Clear | Register Enable | Serial/ Parallel | Sign Extend | Mux Select | $\overline{OE}$* | Clock | $DY_7$ | $DY_6$ | $DY_5$ | $DY_4$ | $DY_3$ | $DY_2$ | $DY_1$ | $DY_0$ | $Q_0$ |
| Clear | L | X | X | X | X | L | X | L | L | L | L | L | L | L | L | L |
| | L | X | X | X | X | H | X | Z | Z | Z | Z | Z | Z | Z | Z | L |
| Parallel Load | H | L | L | X | X | X | ↑ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_0$ |
| Shift Right | H | L | H | H | L | L | ↑ | $D_A$ | $Y_{7n}$ | $Y_{6n}$ | $Y_{5n}$ | $Y_{4n}$ | $Y_{3n}$ | $Y_{2n}$ | $Y_{1n}$ | $Y_{1n}$ |
| | H | L | H | H | H | L | ↑ | $D_B$ | $Y_{7n}$ | $Y_{6n}$ | $Y_{5n}$ | $Y_{4n}$ | $Y_{3n}$ | $Y_{2n}$ | $Y_{1n}$ | $Y_{1n}$ |
| Sign Extend | H | L | H | L | X | L | ↑ | $Y_{7n}$ | $Y_{7n}$ | $Y_{6n}$ | $Y_{5n}$ | $Y_{4n}$ | $Y_{3n}$ | $Y_{2n}$ | $Y_{1n}$ | $Y_{1n}$ |
| Hold | H | H | X | X | X | L | ↑ | NC | NC | NC | NC | NC | NC | NC | NC | NC |

L = LOW
H = HIGH
↑ = Clock LOW-to-HIGH Transition
NC = No Change
X = Don't Care
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

$D_7$, $D_6$. . . $D_0$ = the level of the steady-state input at the respective $DY_n$ terminal is loaded into the flip-flop while the flip-flop outputs (except $Q_0$) are isolated from the $DY_n$ terminal.

$D_A$, $D_B$ = the level of the steady-state inputs to the serial multiplexer input.

$Y_{7n}$, $Y_{6n}$. . . $Y_{0n}$ = the level of the respective $Q_n$ flip-flop prior to the last Clock LOW-to-HIGH transition.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $DY_i$ | | | 35 | | 41 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 38 | | 44 | | |
| $t_{PHL}$ | Clear to $DY_i$ | | | 43 | | 50 | ns | |
| $t_{PLH}$ | Clock to $Q_0$ | | | 35 | | 41 | ns | |
| $t_{PHL}$ | | | | 38 | | 44 | | |
| $t_{PHL}$ | Clear to $Q_0$ | | | 43 | | 50 | ns | |
| $t_{ZH}$ | OE to $DY_i$ | | | 32 | | 36 | ns | |
| $t_{ZL}$ | | | | 38 | | 44 | | |
| $t_{HZ}$ | | | | 28 | | 31 | | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 34 | | 39 | | |
| $t_{ZH}$ | SER/PAR to $DY_i$ | | | 38 | | 44 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{ZL}$ | | | | 46 | | 53 | | |
| $t_{HZ}$ | | | | 34 | | 39 | | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 42 | | 48 | | |
| $t_s$ | RE to Clock | | 30 | | 35 | | | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_s$ | SE to Clock | | 17 | | 20 | | | |
| $t_s$ | S to Clock | | 24 | | 27 | | ns | |
| $t_s$ | $D_A$ and $D_B$ to Clock | | 24 | | 27 | | | |
| $t_s$ | $DY_i$ (Load) to Clock | | 24 | | 27 | | | |
| $t_s$ | Clear Recovery to Clock | | 15 | | 17 | | | |
| $t_s$ | S/P to Clock | | 24 | | 27 | | ns | |
| $t_h$ | Any Input | | 4 | | 5 | | | |
| $t_h$ | Clear Hold | | 4 | | 5 | | ns | |
| $t_{pw}$ | Clock | HIGH | 15 | | 17 | | ns | |
| | | LOW | 15 | | 17 | | | |
| $t_{pw}$ | Clear | | 30 | | 35 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | | 26 | | 23 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$DY_i$** The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, i = 0 through 7.

**$Q_0$** The continuous output from the $Q_0$ flip-flop of the register. This output is used for serial shifting.

**$\overline{RE}$** Register Enable. When $\overline{RE}$ is LOW, the register functions are enabled. When $\overline{RE}$ is HIGH, the register functions (parallel load, shift right and sign extend) are inhibited.

**S/P** Serial/Parallel. When S/P is LOW, the register can be synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the $\overline{OE}$ input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition.

**$\overline{SE}$** Sign Extend. When the $\overline{SE}$ input is LOW, the contents of the $Q_7$ flip-flop will be repeated in the $Q_7$ flip-flop as the register is shifted right. When $\overline{SE}$ is HIGH, the two-input multiplexer ($D_A$ and $D_B$) is enabled to enter data during the serial shift right. The $Q_7$ flip-flop ($DY_7$) is normally considered the MSB of the register for arithmetic definitions.

**$D_A$, $D_B$** The serial inputs to the device.

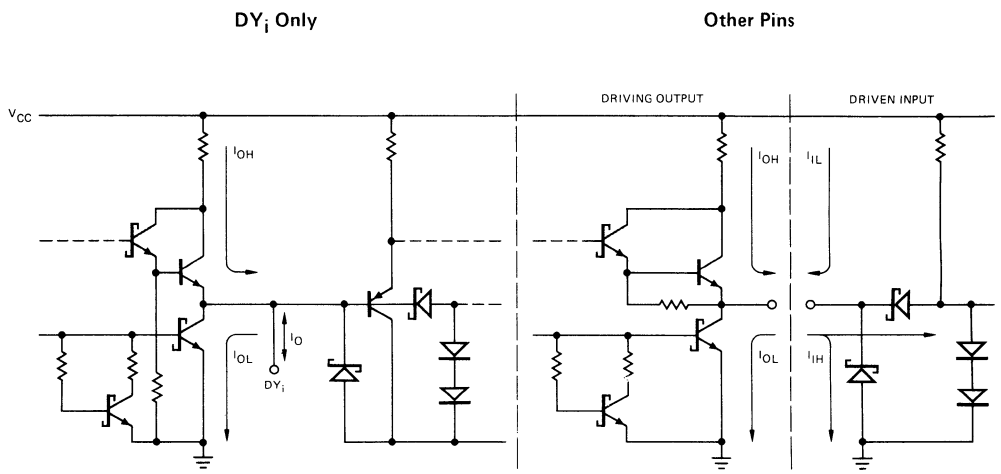
**S** Multiplexer Select. When S is LOW, the $D_A$ serial input is selected. When S is HIGH, the $D_B$ serial input is selected.

**CLR** Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function.

**CP** Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse.

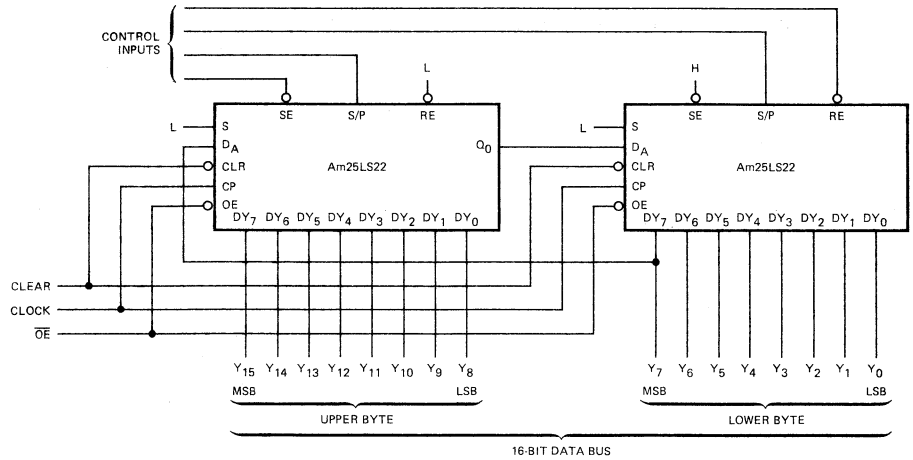
**$\overline{OE}$** Output Control. When the $\overline{OE}$ input is HIGH, the eight $DY_i$ outputs are in the high-impedance state. When $\overline{OE}$ is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

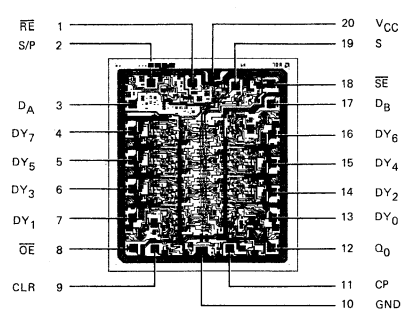
## APPLICATION




| SYSTEM OPERATION | Am25LS22 UPPER BYTE | | | | Am25LS22 LOWER BYTE | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{SE}$ | S/P | $\overline{RE}$ | $\overline{OE}$ | $\overline{SE}$ | S/P | $\overline{RE}$ | $\overline{OE}$ | Description |
| Load lower byte and extend lower byte sign to upper byte | H | H | L | X | X | L | L | X | Load from Bus |
| | L | H | L | H | X | X | H | H | 7 clock cycles to extend sign |
| Load upper byte and extend upper byte sign while shifting value to lower byte position | X | L | L | X | X | X | X | X | Load from Bus |
| | H | H | L | H | H | H | L | H | 8 clock cycles to extend upper byte sign and shift upper byte into lower byte position |
| Read 16-bit word to Bus | X | X | X | L | X | X | X | L | Unload |

Two Am25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

### Metallization and Pad Layout




DIE SIZE 0.096" X 0.112"

# Am25LS23

## 8-Bit Shift/Storage Register with Synchronous Clear

### DISTINCTIVE CHARACTERISTICS

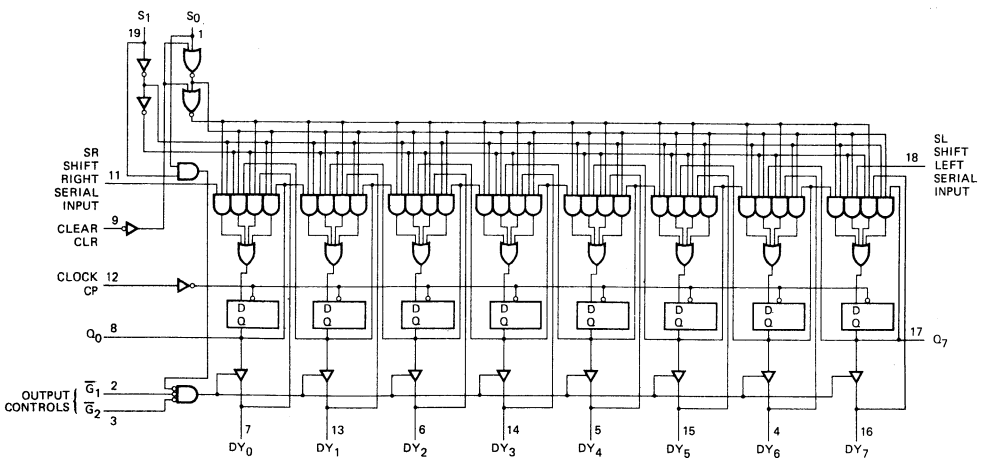
- Synchronous clear
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Second sourced by T.I. as 54LS/74LS323
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

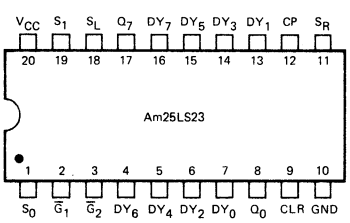
The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops $Q_0$ and $Q_7$.

Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

### LOGIC DIAGRAM

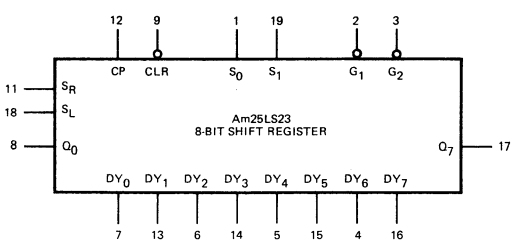



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{OL}$ | $Q_0$, $Q_7$ | $I_{OH} = -440\mu A$ | MIL | 2.5 | | | Volts |
| | | | | | COM'L | 2.7 | | | |
| | | | $DY_0-DY_7$ | MIL, $I_{OH} = -1.0mA$ | | 2.4 | | | |
| | | | | COM'L, $I_{OH} = -2.6mA$ | | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | | $I_{OL} = 4.0mA$ | | | 0.25 | 0.4 | Volts |
| | | | | $I_{OL} = 8.0mA$ | | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | MIL | | | 0.7 | Volts |
| | | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | $S_0$, $S_1$ | | | −0.8 | mA |
| | | | | | All others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ (Except $DY_i$) | | | $S_0$, $S_1$ | | | 40 | μA |
| | | | | | All others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., (Except $DY_i$) | $V_{IN} = 7V$ | | $S_0$, $S_1$ | | | 0.2 | mA |
| | | | | | $\overline{G}_1$, $\overline{G}_2$, CLR, CP | | | 0.1 | |
| | | | $V_{IN} = 5.5V$ | | Others | | | 0.1 | |
| $I_{OZ}$ | Off-State (High Impedance) Output Current | $V_{CC}$ = MAX. | | | $V_O = 0.4V$ | | | −100 | μA |
| | | | | | $V_O = 2.4V$ | | | 40 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | | | 38 | 60 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time.
4. $I_{CC}$ – measured with clock input HIGH and output controls HIGH.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage ($S_0$, $S_1$, $\overline{G}_1$, $\overline{G}_2$, CLR, CP) | −0.5V to +7.0V |
| DC Input Voltage (Others) | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Q_0$ or $Q_7$ | | 18 | 26 | ns | $C_L = 15pF$ $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | 23 | 28 | | |
| $t_{PLH}$ | Clock to $DY_i$ | | 18 | 26 | ns | |
| $t_{PHL}$ | | | 21 | 28 | | |
| $t_s$ | $S_1$, $S_0$ Set-up Prior to Clock | 12 | | | ns | |
| $t_s$ | $DY_i$ or $S_R$, $S_L$ Set-up Prior to Clock | 12 | | | ns | |
| $t_{PW}$ | Pulse Width (Clock) | 15 | | | ns | |
| $t_s$ | Clear to Clock | 15 | | | ns | |
| $t_{ZH}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 18 | 30 | ns | |
| $t_{ZL}$ | | | 20 | 30 | | |
| $t_{LZ}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$, to $DY_i$ | | 22 | 33 | ns | $C_L = 5.0pF$ $R_L = 2.0k\Omega$ |
| $t_{HZ}$ | | | 16 | 23 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 35 | 50 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Q_0$ or $Q_7$ | | 38 | | 44 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 40 | | 47 | | |
| $t_{PLH}$ | Clock to $DY_i$ | | 38 | | 44 | ns | |
| $t_{PHL}$ | | | 40 | | 47 | | |
| $t_S$ | $S_1$, $S_0$ Set-up Prior to Clock | 20 | | 23 | | ns | |
| $t_S$ | $DY_i$ or $S_R$, $S_L$ Set-up Prior to Clock | 20 | | 23 | | ns | |
| $t_{pw}$ | Pulse Width (Clock) | 24 | | 27 | | ns | |
| $t_S$ | Clear to Clock | 24 | | 27 | | ns | |
| $t_{ZH}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 43 | | 50 | ns | |
| $t_{ZL}$ | | | 43 | | 50 | | |
| $t_{LZ}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 43 | | 50 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{HZ}$ | | | 30 | | 35 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 26 | | 23 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$S_R$** Shift right data input to $Q_7$

**$S_L$** Shift left data input to $Q_0$

**Clear** Active LOW synchronous input forcing the $Q_0$ through $Q_7$ register to see LOW conditions, visable only if outputs are enabled

**Clock** A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition

**$S_0$, $S_1$** Mode selection control lines used to control input (output during load) conditions

**$\overline{G}_1$, $\overline{G}_2$** Active LOW input to control three-state output in active LOW AND configuration

**$Q_0$, $Q_7$** The only two direct outputs; used to cascade shift operations

**$DY_0$–$DY_7$** Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($\overline{G}_1$, $\overline{G}_2$).

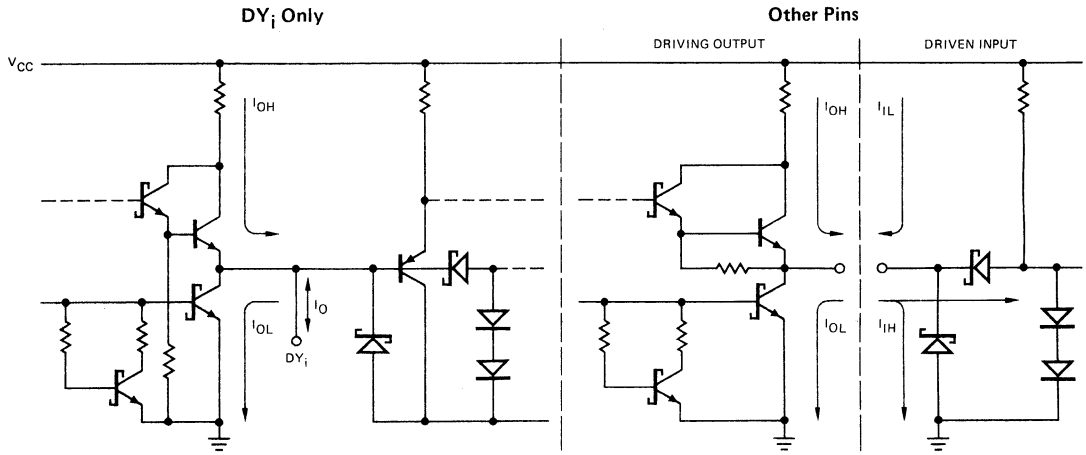
## TRUTH TABLE

| FUNCTION | | $S_R$ | $S_L$ | CLEAR | CLOCK | $S_0$ | $S_1$ | $\overline{G}_1$ | $\overline{G}_2$ | $Q_0$ | $Q_7$ | $DY_0$ | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ | $DY_7$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | | X | X | L | ↑ | (Note 1) | | L | L | L | L | L | L | L | L | L | L | L | L |
| Output Control | | X | X | X | X | X | X | H | L | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |
| | | X | X | X | X | X | X | L | H | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |
| | | X | X | X | X | X | X | H | H | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |
| M O D E | Hold | X | X | H | X | L | L | L | L | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC |
| | Load (Note 2) | X | X | H | ↑ | H | H | L | L | A | H | A | B | C | D | E | F | G | H |
| | Shift Right | L | X | H | ↑ | H | L | L | L | L | $DY_6$ | L | $DY_0$ | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ |
| | Shift Right | H | X | H | ↑ | H | L | L | L | H | $DY_6$ | H | $DY_0$ | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ |
| | Shift Left | X | L | H | ↑ | L | H | L | L | $DY_1$ | L | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ | $DY_7$ | L |
| | Shift Left | X | H | H | ↑ | L | H | L | L | $DY_1$ | H | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ | $DY_7$ | H |

L = LOW, H = HIGH, Z = High Impedance, X = Don't Care, ↑ = Transition LOW-to-HIGH, NC = No Change

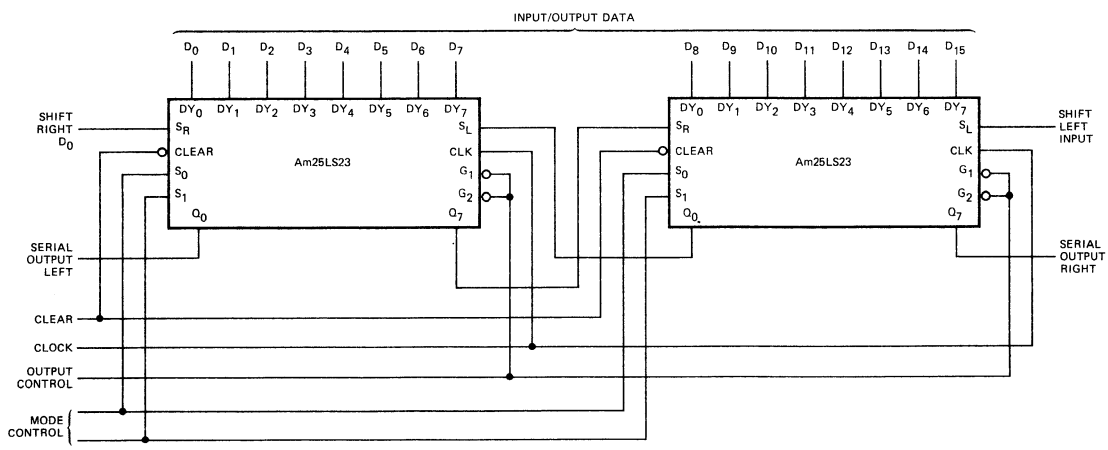
Notes: 1. Either LOW to observe outputs.
2. In this mode $DY_i$ are inputs.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



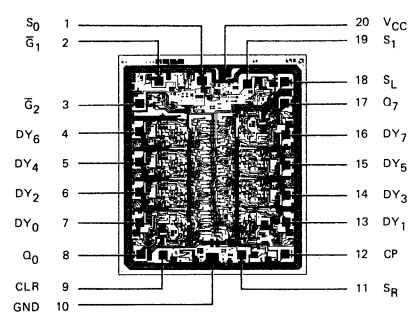

Note: Actual current flow direction shown.

## APPLICATION




16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

### Metallization and Pad Layout




DIE SIZE
0.096" X 0.112"

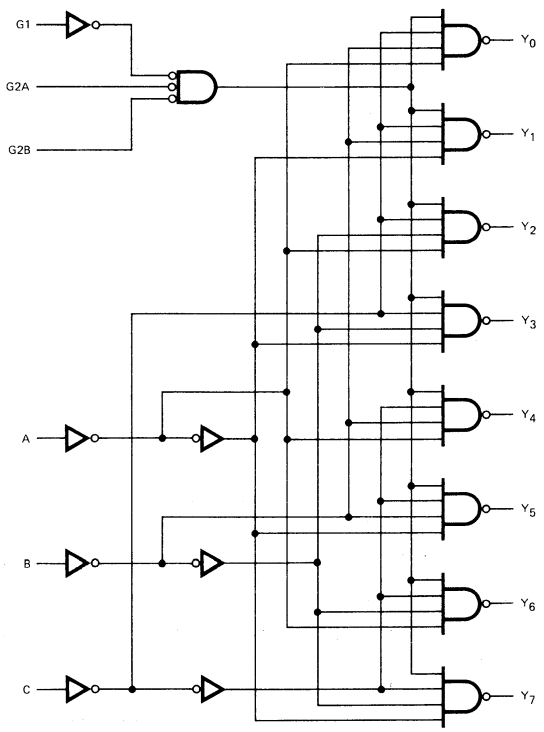
# Am25LS138 • Am54LS/74LS138

## 3-Line To 8-Line Decoder/Demultiplexer

### DISTINCTIVE CHARACTERISTICS

- Inverting and non-inverting enable inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

### LOGIC DIAGRAM



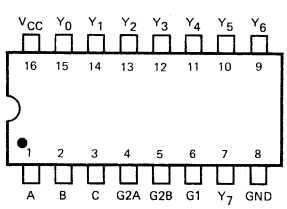

### FUNCTIONAL DESCRIPTION

The Am25LS138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

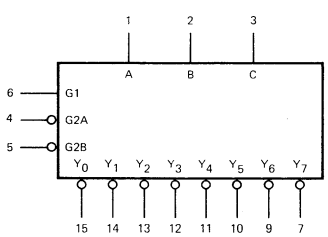
The Am54LS/74LS138 is a standard performance version of the Am25LS138. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## ELECTRICAL CHARACTERISTICS Am25LS138

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 6.3 | 10 | mA |

## ELECTRICAL CHARACTERISTICS Am54LS/74LS138

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 6.3 | 10 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs enabled and open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +Vcc max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Two Level Delay Select to Output | | 10 | 15 | | 13 | 20 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 14 | 21 | | 27 | 41 | | |
| $t_{PLH}$ | Three Level Delay Select to Output | | 15 | 23 | | 18 | 27 | ns | |
| $t_{PHL}$ | | | 18 | 27 | | 26 | 39 | | |
| $t_{PLH}$ | G2A or G2B to Output | | 10 | 15 | | 12 | 18 | ns | |
| $t_{PHL}$ | | | 15 | 23 | | 21 | 32 | | |
| $t_{PLH}$ | G1 to Output | | 12 | 18 | | 17 | 26 | ns | |
| $t_{PHL}$ | | | 18 | 27 | | 25 | 38 | | |

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Two Level Delay Select to Output | | 24 | | 27 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 31 | | 36 | | |
| $t_{PLH}$ | Three Level Delay Select to Output | | 34 | | 39 | ns | |
| $t_{PHL}$ | | | 39 | | 45 | | |
| $t_{PLH}$ | G2A or G2B to Output | | 24 | | 27 | ns | |
| $t_{PHL}$ | | | 34 | | 39 | | |
| $t_{PLH}$ | G1 to Output | | 27 | | 32 | ns | |
| $t_{PHL}$ | | | 39 | | 45 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

## DEFINITION OF FUNCTIONAL TERMS

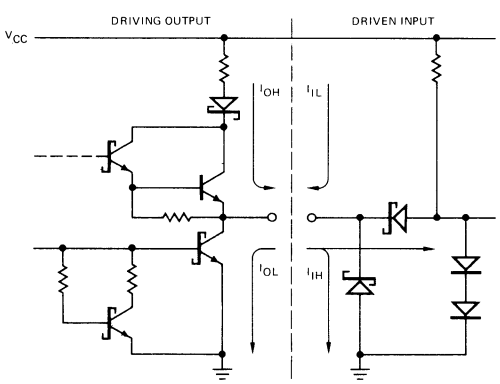
**A, B, C** Select. The three select inputs to the decoder.

**G1** The active-HIGH enable input. A LOW on the G1 input forces all Y outputs HIGH regardless of any other inputs.

**G2A, G2B** The active-LOW enable input. A HIGH on either the G2A or G2B input forces all Y outputs HIGH regardless of any other inputs.

$Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7$ The eight decoder outputs.

### Am25LS • Am54LS/74LS LOW POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



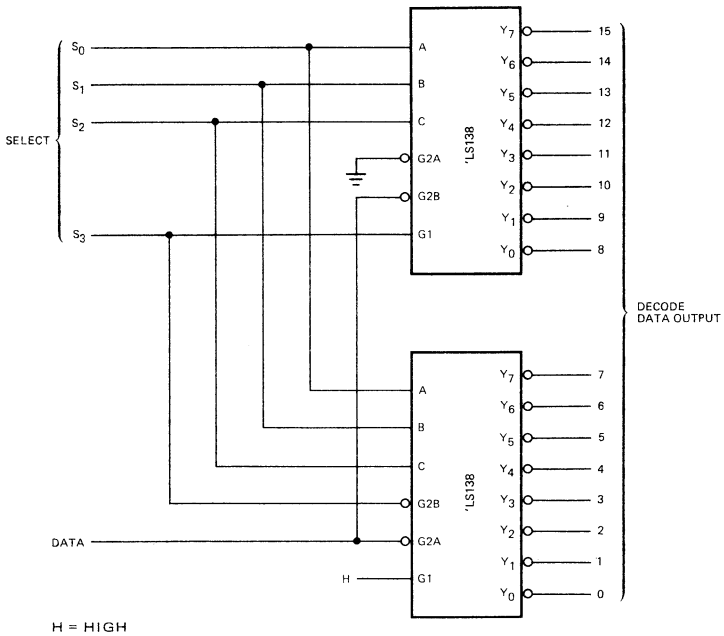

Note: Actual current flow direction shown.

### FUNCTION TABLE

| Inputs Enable G1 | G2A | G2B | Select C | B | A | Outputs $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH L = LOW X = Don't care

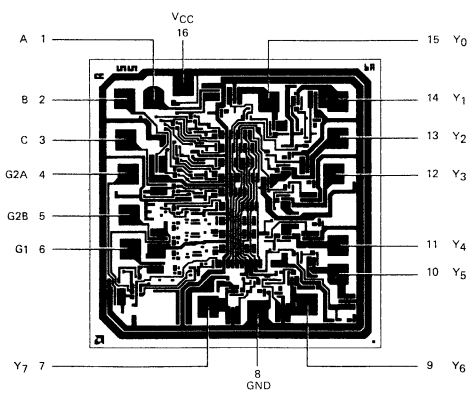
## APPLICATION




H = HIGH

**ONE-OF-SIXTEEN DEMULTIPLEXER**

### Metallization and Pad Layout




DIE SIZE 0.065" X 0.065"

# Am25LS139 • Am54LS/74LS139

## Dual 2-Line To 4-Line Decoder/Demultiplexer

### DISTINCTIVE CHARACTERISTICS

- Two independent decoders/demultiplexers
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

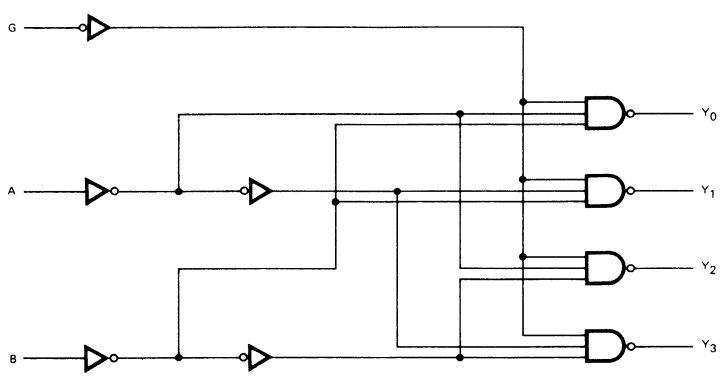
### FUNCTIONAL DESCRIPTION

The Am25LS139 is a dual 2-line to 4-line decoder/demultiplexer unit fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs A and B which are decoded to one of four Y outputs.

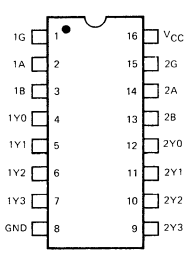
An active LOW enable can be used for gating or can be used as a data input for demultiplexing applications. When the enable is HIGH, all four Y outputs are HIGH, regardless of the A and B inputs.

The Am54LS/74LS139 is a standard performance version of the Am25LS139. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM
(One Decoder Shown)

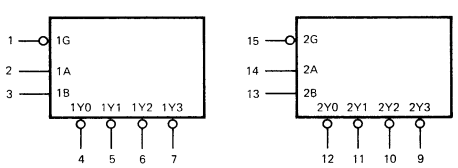



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## Am25LS139

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 6.8 | 11 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs enabled and open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS139
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 6.8 | 11 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs enabled and open.

3

## SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Select to Output, 2 Levels of Delay | | 8 | 12 | | 13 | 20 | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | 12 | 18 | | 22 | 33 | | |
| $t_{PLH}$ | Select to Output, 3 Levels of Delay | | 13 | 20 | | 18 | 29 | ns | |
| $t_{PHL}$ | | | 14 | 21 | | 25 | 38 | | |
| $t_{PLH}$ | Enable to Output, 2 Levels of Delay | | 8 | 12 | | 16 | 24 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | 21 | 32 | | |

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Select to Output 2 Levels of Delay | | 20 | | 23 | ns | $C_L = 50pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | 27 | | 32 | | |
| $t_{PLH}$ | Select to Output 3 Levels of Delay | | 30 | | 35 | ns | |
| $t_{PHL}$ | | | 31 | | 36 | | |
| $t_{PLH}$ | Enable to Output 2 Levels of Delay | | 20 | | 23 | ns | |
| $t_{PHL}$ | | | 27 | | 32 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**A, B** Select. The two select inputs to the decoder.

**G** Enable. The enable input to the decoder. A HIGH input forces all four Y outputs HIGH regardless of the A and B inputs.

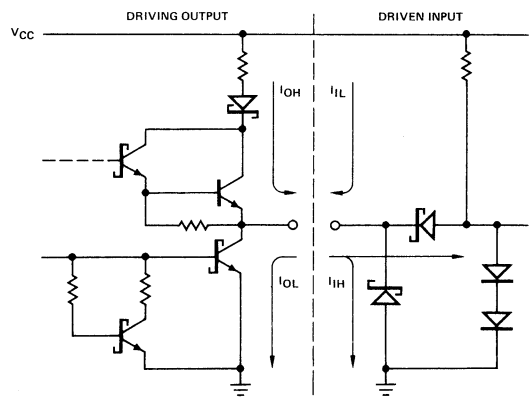
$Y_0$, $Y_1$, $Y_2$, $Y_3$ The four decoder outputs.

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE G | SELECT B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

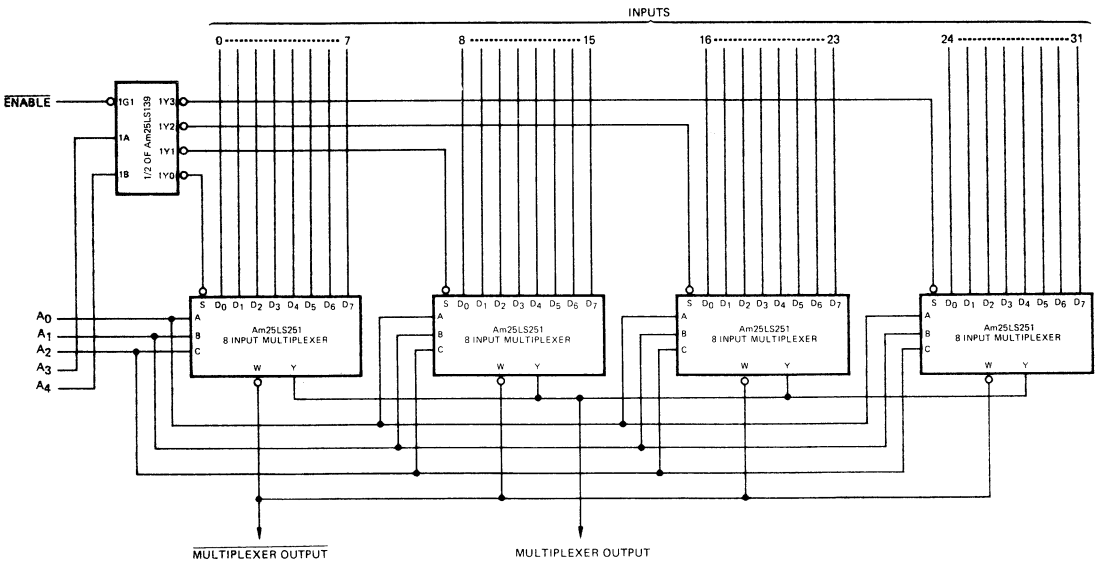
H = HIGH L = LOW X = Don't care

### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT
### CURRENT INTERFACE CONDITIONS

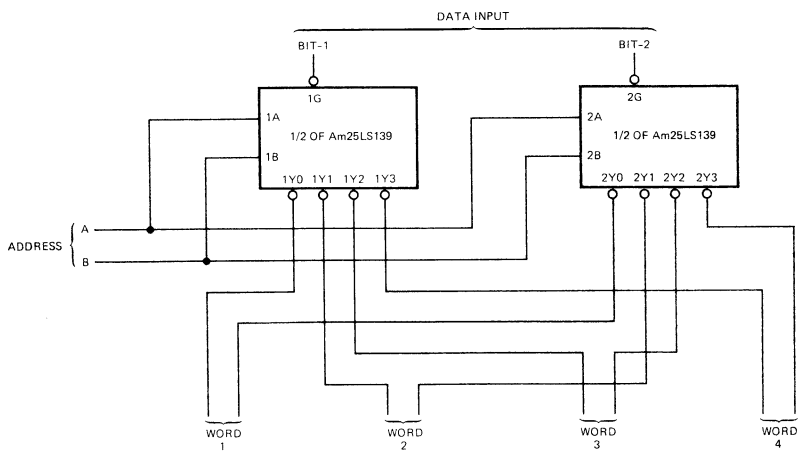



Note: Actual current flow direction shown.

## APPLICATIONS

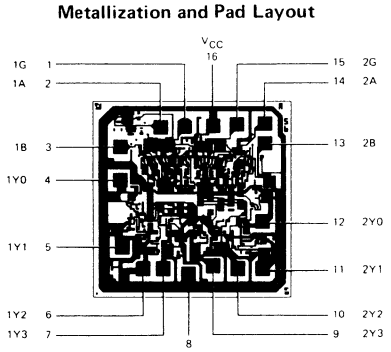



32-INPUT DEMULTIPLEXER




DATA ROUTING USING ONE Am25LS139 AS A DEMULTIPLEXER FOR TWO BITS

### Metallization and Pad Layout




DIE SIZE 0.065" X 0.065"

# Am25LS148 • Am54LS/74LS148

## Eight-Line To Three-Line Priority Encoder

### DISTINCTIVE CHARACTERISTICS

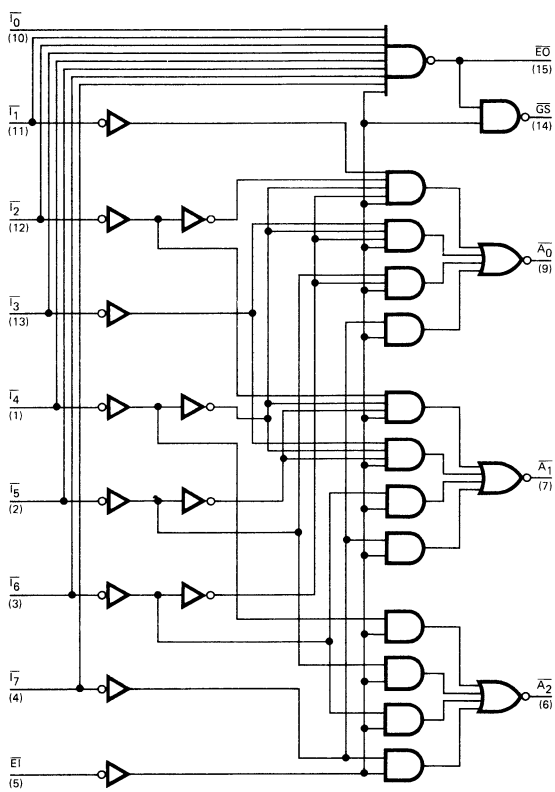
- Encodes eight inputs in priority
- Provides a 3-bit binary vector
- Indicates data present for all inputs
- Cascadable using available signals
- See Am25LS2513 for three-state output version of the Am25LS148
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440μA source current at high output
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

These TTL Encoders perform priority decoding from 8 inputs and provide a binary weighted code of the priority order of the inputs on three active LOW outputs ($\overline{A}_2$, $\overline{A}_1$, $\overline{A}_0$). An active LOW enable input ($\overline{EI}$) and enable output ($\overline{EO}$) allows cascading without the need for external circuitry. Enable input $\overline{EI}$ HIGH will force all outputs HIGH. The enable output is LOW when all inputs ($\overline{I}_0$ to $\overline{I}_7$) are HIGH and the enable input is LOW. A LOW group signal ($\overline{GS}$) indicates that one of the 8 inputs is LOW. When the enable input is LOW, the enable output is the logic inverse of the group signal.

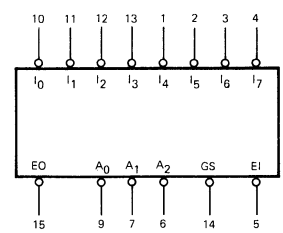
The Am54LS/74LS148 is a standard performance version of the Am25LS148. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM



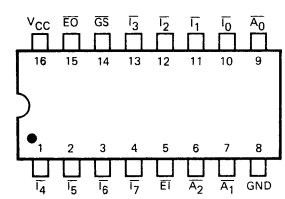

Note: The Advanced Micro Devices' LS148 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

## Am25LS148
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | $\overline{EI}, \overline{I_0}$ | | | −0.4 | mA |
| | | | All others | | | −0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | $\overline{EI}, \overline{I_0}$ | | | 20 | μA |
| | | | All others | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | $\overline{EI}, \overline{I_0}$ | | | 0.1 | mA |
| | | | All others | | | 0.2 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | Condition a | | 11 | 19 | mA |
| | | | Condition b | | 10 | 16 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. a. $\overline{I_7}$, $\overline{EI}$ Gnd all others open.
b. $\overline{I_0} \rightarrow \overline{I_7}$, $\overline{EI}$ open.



## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS148
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | | |
|---|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −400μA, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8.0mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | $\overline{EI}, \overline{I_0}$ | | | −0.4 | mA |
| | | | All others | | | −0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | $\overline{EI}, \overline{I_0}$ | | | 20 | μA |
| | | | All others | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | $\overline{EI}, \overline{I_0}$ | | | 0.1 | mA |
| | | | All others | | | 0.2 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | Condition a | | 12 | 20 | mA |
| | | | Condition b | | 10 | 17 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. a. $\overline{I_7}$, $\overline{EI}$ Gnd all others open.
b. $\overline{I_0} \rightarrow \overline{I_7}$, $\overline{EI}$ open.

### TRUTH TABLE

| ENABLE IN | INPUTS | | | | | | | | GROUP SELECT | OUTPUTS | | | ENABLE OUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{EI}$ | $\overline{I_0}$ | $\overline{I_1}$ | $\overline{I_2}$ | $\overline{I_3}$ | $\overline{I_4}$ | $\overline{I_5}$ | $\overline{I_6}$ | $\overline{I_7}$ | $\overline{GS}$ | $\overline{A_0}$ | $\overline{A_1}$ | $\overline{A_2}$ | $\overline{EO}$ |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | H | L | L | H |
| L | X | X | X | X | X | L | H | H | L | L | H | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | L | L | L | H | H |
| L | X | X | L | H | H | H | H | H | L | H | L | H | H |
| L | X | L | H | H | H | H | H | H | L | L | H | H | H |
| L | L | H | H | H | H | H | H | H | L | H | H | H | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{A_n}$ (In Phase Output) | | 12 | 18 | | 12 | 18 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 9 | 14 | | 17 | 25 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{A_n}$ (Out-of-Phase Output) | | 16 | 24 | | 24 | 36 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | 19 | 29 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{EO}$ | | 7 | 11 | | 12 | 18 | ns | |
| $t_{PHL}$ | | | 23 | 35 | | 23 | 40 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{GS}$ | | 32 | 48 | | 32 | 55 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | 14 | 21 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{A_i}$ | | 13 | 20 | | 13 | 25 | ns | |
| $t_{PHL}$ | | | 8 | 12 | | 17 | 25 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{GS}$ | | 12 | 17 | | 12 | 17 | ns | |
| $t_{PHL}$ | | | 9 | 14 | | 24 | 36 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{EO}$ | | 9 | 14 | | 14 | 21 | ns | |
| $t_{PHL}$ | | | 25 | 35 | | 25 | 35 | | |

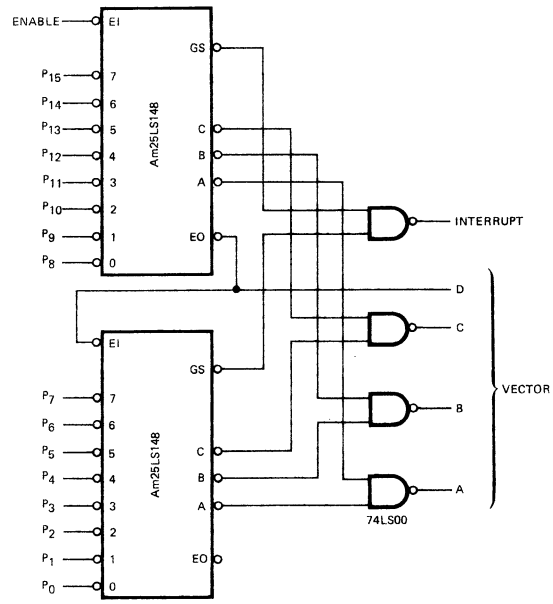
3

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{A_n}$ (In Phase Output) | | 23 | | 27 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 21 | | 27 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{A_n}$ (Out-of-Phase Output) | | 33 | | 39 | ns | |
| $t_{PHL}$ | | | 30 | | 34 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{EO}$ | | 15 | | 16 | ns | |
| $t_{PHL}$ | | | 50 | | 60 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{GS}$ | | 75 | | 90 | ns | |
| $t_{PHL}$ | | | 30 | | 33 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{A_i}$ | | 28 | | 33 | ns | |
| $t_{PHL}$ | | | 21 | | 25 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{GS}$ | | 26 | | 30 | ns | |
| $t_{PHL}$ | | | 26 | | 30 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{EO}$ | | 19 | | 22 | ns | |
| $t_{PHL}$ | | | 60 | | 75 | | |

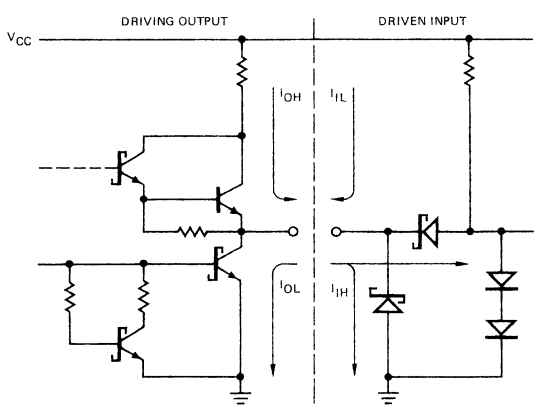
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## APPLICATION




Priority interrupt encoding expanded to 16.

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

### DEFINITION OF FUNCTIONAL TERMS

$\overline{A_n}$ Address Data Outputs. Low address of most significant low data input (n = 0, 2).

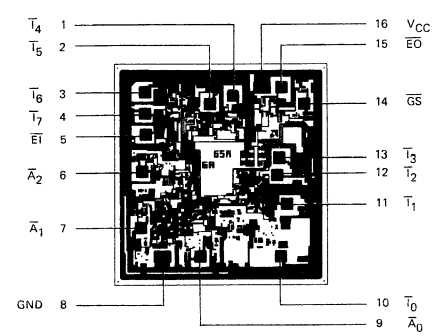
$\overline{EI}$ Low Enable Input. Enable input HIGH forces all outputs HIGH.

$\overline{EO}$ Low Enable Output. Indicates that enable input is LOW and no input is active.

$\overline{GS}$ Low Group Signal. If enable input is LOW, indicates when any input is active.

$\overline{I_i}$ Data Inputs. Designates one of the eight active LOW inputs (i = 0–7).

### Metallization and Pad Layout




DIE SIZE 0.082" X 0.085"

# Am25LS151 • Am54LS/74LS151
# Am25LS251 • Am54LS/74LS251

## Eight-Input Multiplexers

### DISTINCTIVE CHARACTERISTICS

- Switches one-of-eight inputs to two complementary outputs
- Standard, 'LS151 and three-state, 'LS251 output versions
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440$\mu$A source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

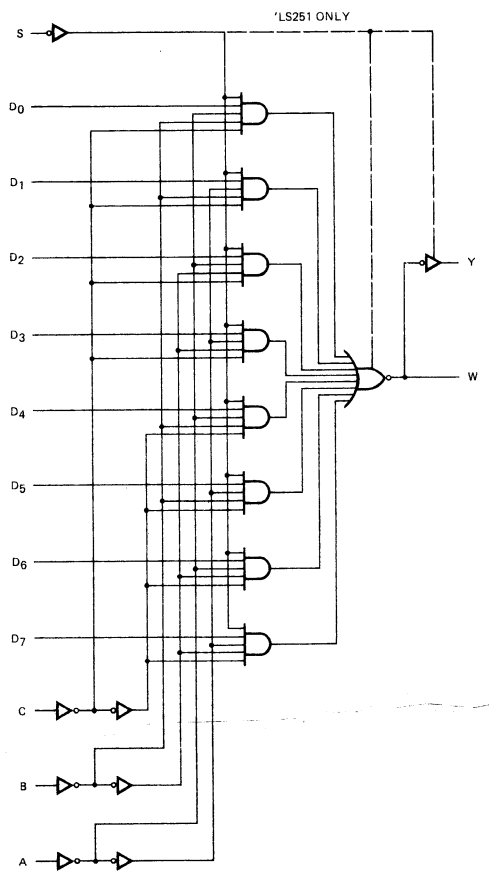
The Am25LS151 and the Am25LS251 are eight-input multiplexers that switch one of eight inputs onto the inverting and non-inverting outputs under the control of a three-bit select code. The inverting output W is one gate delay faster than the non-inverting output Y.

The Am25LS151 provides an active-LOW strobe. When the strobe is HIGH, the inverting output (W) is HIGH and the non-inverting output (Y) is LOW.

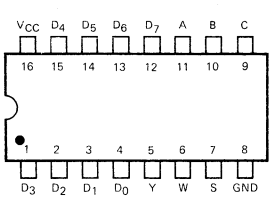
The Am25LS251 features a three-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

The Am54LS/74LS151 is a standard performance version of the Am25LS151. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

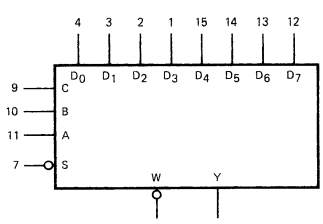



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




VCC = Pin 16
GND = Pin 8

## Am25LS151 • Am25LS251

### ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | LS151XM | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -440\mu A$ | | 2.5 | 3.4 | | Volts |
| | | LS151XC | | | | 2.7 | 3.4 | | |
| | | LS251XM | | $I_{OH} = -1mA$ | | 2.4 | 3.4 | | |
| | | LS251XC | | $I_{OH} = -2.6mA$ | | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | | $I_{OL} = 4mA$ | | | | 0.4 | Volts |
| | | | | $I_{OL} = 8mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current (LS251 only) | | $V_{CC}$ = MAX. $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_O = 2.4V$ | | | | 20 | μA |
| | | | | $V_O = 0.4V$ | | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. | LS151 (Note 4) | | | 6.0 | 10 | mA |
| | | | | LS251 (Note 5) | A | | 6.1 | 10 | |
| | | | | | B | | 7.1 | 12 | |

## Am54LS/74LS151 • Am54LS/74LS251

### ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 54LS151 | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -400\mu A$ | | 2.5 | 3.4 | | Volts |
| | | 74LS151 | | | | 2.7 | 3.4 | | |
| | | 54LS251 | | $I_{OH} = -1mA$ | | 2.4 | 3.4 | | |
| | | 74LS251 | | $I_{OH} = -2.6mA$ | | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | | All, $I_{OL} = 4mA$ | | | | 0.4 | Volts |
| | | | | 74LS only, $I_{OL} = 8mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | 54LS | | | 0.7 | Volts |
| | | | | | 74LS | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current (LS251 only) | | $V_{CC}$ = MAX. $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_O = 2.4V$ | | | | 20 | μA |
| | | | | $V_O = 0.4V$ | | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | | $V_{CC}$ = MAX. | | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. | LS151 (Note 4) | | | 6.0 | 10 | mA |
| | | | | LS251 (Note 5) | A | | 6.1 | 10 | |
| | | | | | B | | 7.1 | 12 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.
5. $I_{CC}$ is measured with all outputs open and all data and select inputs at 4.5V under conditions:
   A) Strobe grounded. B) Strobe at 4.5V.

## MAXIMUM RATINGS (Above which the useful life may be impaired).

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to + $V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Output | 30mA |
| DC Input Current | −30mA to +5.0mA |

## Am25LS151 • Am54LS/74LS151 SWITCHING CHARACTERISTICS

($T_A$ = 25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, or C to Y; 4 Levels of Delay | | 27 | 41 | | 27 | 43 | ns | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 20 | 30 | | 18 | 30 | | |
| $t_{PLH}$ | A, B, or C to W; 3 Levels of Delay | | 16 | 23 | | 14 | 23 | ns | |
| $t_{PHL}$ | | | 22 | 32 | | 20 | 32 | | |
| $t_{PLH}$ | Any D to Y | | 16 | 24 | | 20 | 32 | ns | |
| $t_{PHL}$ | | | 11 | 17 | | 16 | 26 | | |
| $t_{PLH}$ | Any D to W | | 7 | 12 | | 13 | 21 | ns | |
| $t_{PHL}$ | | | 10 | 15 | | 12 | 20 | | |
| $t_{PLH}$ | Strobe to Y | | 22 | 33 | | 26 | 42 | ns | |
| $t_{PHL}$ | | | 15 | 23 | | 20 | 32 | | |
| $t_{PLH}$ | Strobe to W | | 11 | 17 | | 15 | 24 | ns | |
| $t_{PHL}$ | | | 16 | 24 | | 18 | 30 | | |

## Am25LS151 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B or C to Y; 4 Levels of Delay | | 57 | | 66 | ns | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 43 | | 50 | | |
| $t_{PLH}$ | A, B or C to W; 3 Levels of Delay | | 34 | | 39 | ns | |
| $t_{PHL}$ | | | 46 | | 53 | | |
| $t_{PLH}$ | Any D to Y | | 35 | | 41 | ns | |
| $t_{PHL}$ | | | 26 | | 30 | | |
| $t_{PLH}$ | Any D to W | | 20 | | 23 | ns | |
| $t_{PHL}$ | | | 24 | | 27 | | |
| $t_{PLH}$ | Strobe to Y | | 47 | | 54 | ns | |
| $t_{PHL}$ | | | 34 | | 39 | | |
| $t_{PLH}$ | Strobe to W | | 26 | | 30 | ns | |
| $t_{PHL}$ | | | 35 | | 41 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## SWITCHING CHARACTERISTICS
($T_A$ = 25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, or C to Y; 4 Levels of Delay | | 29 | 44 | | 29 | 45 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 20 | 30 | | 28 | 45 | | |
| $t_{PLH}$ | A, B, or C to W; 3 Levels of Delay | | 16 | 24 | | 20 | 33 | ns | |
| $t_{PHL}$ | | | 21 | 32 | | 21 | 33 | | |
| $t_{PLH}$ | Any D to Y | | 16 | 24 | | 17 | 28 | ns | |
| $t_{PHL}$ | | | 11 | 17 | | 18 | 28 | | |
| $t_{PLH}$ | Any D to W | | 8 | 12 | | 10 | 15 | ns | |
| $t_{PHL}$ | | | 9 | 14 | | 9 | 15 | | |
| $t_{ZH}$ | Output Enable to Y | | 8 | 12 | | 17 | 45 | ns | |
| $t_{ZL}$ | | | 13 | 19 | | 26 | 40 | | |
| $t_{ZH}$ | Output Enable to W | | 10 | 15 | | 17 | 27 | ns | |
| $t_{ZL}$ | | | 11 | 18 | | 24 | 40 | | |
| $t_{HZ}$ | Output Enable to Y | | 18 | 27 | | 30 | 45 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 12 | 18 | | 15 | 25 | | |
| $t_{HZ}$ | Output Enable to W | | 19 | 29 | | 30 | 55 | ns | |
| $t_{LZ}$ | | | 12 | 18 | | 15 | 25 | | |

## Am25LS251 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B or C to Y; 4 Levels of Delay | | 61 | | 71 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 43 | | 50 | | |
| $t_{PLH}$ | A, B or C to W; 3 Levels of Delay | | 35 | | 41 | ns | |
| $t_{PHL}$ | | | 46 | | 53 | | |
| $t_{PLH}$ | Any D to Y | | 35 | | 41 | ns | |
| $t_{PHL}$ | | | 26 | | 30 | | |
| $t_{PLH}$ | Any D to W | | 20 | | 23 | ns | |
| $t_{PHL}$ | | | 22 | | 26 | | |
| $t_{ZH}$ | Output Enable to Y | | 20 | | 23 | ns | |
| $t_{ZL}$ | | | 29 | | 33 | | |
| $t_{ZH}$ | Output Enable to W | | 24 | | 27 | ns | |
| $t_{ZL}$ | | | 27 | | 32 | | |
| $t_{HZ}$ | Output Enable to Y | | 35 | | 41 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 24 | | 27 | | |
| $t_{HZ}$ | Output Enable to W | | 38 | | 44 | ns | |
| $t_{LZ}$ | | | 24 | | 27 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| SELECT | | | LS151 Strobe | LS251 Output Control | LS151 Output | | LS251 Output | |
| C | B | A | S | S | Y | W | Y | W |
| X | X | X | H | H | L | H | Z | Z |
| L | L | L | L | L | $D_0$ | $\overline{D}_0$ | $D_0$ | $\overline{D}_0$ |
| L | L | H | L | L | $D_1$ | $\overline{D}_1$ | $D_1$ | $\overline{D}_1$ |
| L | H | L | L | L | $D_2$ | $\overline{D}_2$ | $D_2$ | $\overline{D}_2$ |
| L | H | H | L | L | $D_3$ | $\overline{D}_3$ | $D_3$ | $\overline{D}_3$ |
| H | L | L | L | L | $D_4$ | $\overline{D}_4$ | $D_4$ | $\overline{D}_4$ |
| H | L | H | L | L | $D_5$ | $\overline{D}_5$ | $D_5$ | $\overline{D}_5$ |
| H | H | L | L | L | $D_6$ | $\overline{D}_6$ | $D_6$ | $\overline{D}_6$ |
| H | H | H | L | L | $D_7$ | $\overline{D}_7$ | $D_7$ | $\overline{D}_7$ |

H = HIGH  X = Don't Care
L = LOW  Z = High Impedance

$D_0$–$D_7$ = The output will follow the HIGH-level or LOW-level of the selected input.

$\overline{D}_0$–$\overline{D}_7$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

## DEFINITION OF FUNCTIONAL TERMS

**A, B, C** The three select inputs of the multiplexer.

**$D_0$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$, $D_6$, $D_7$** The eight data inputs of the multiplexer.

**Y** The true multiplexer output.

**W** The complement multiplexer output.

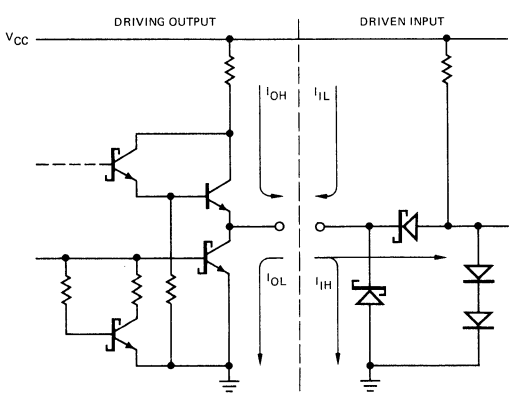
**S** Strobe. On the Am25LS151, a HIGH on the strobe forces the Y output LOW and the W output HIGH.

**S** Output Control. On the Am25LS251, a HIGH on the output control (or strobe) forces both the W and Y outputs to the high-impedance (off) state.

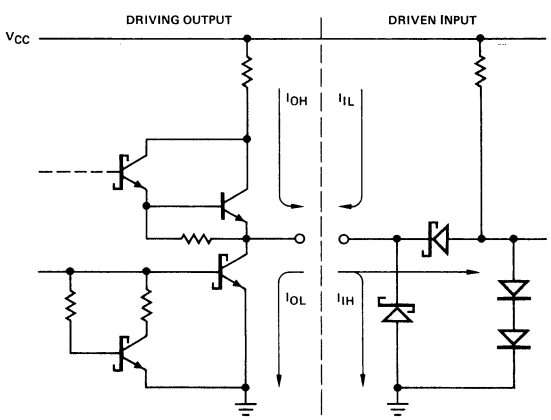
3

### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

'LS251
THREE-STATE OUTPUT



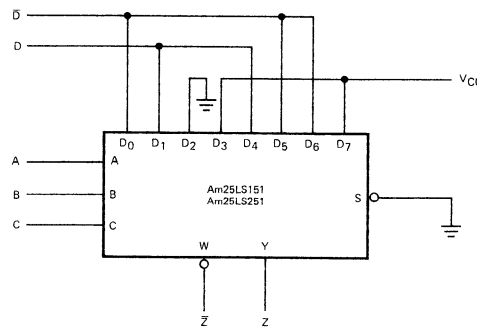

'LS151
STANDARD OUTPUT




Note: Actual current flow direction shown.

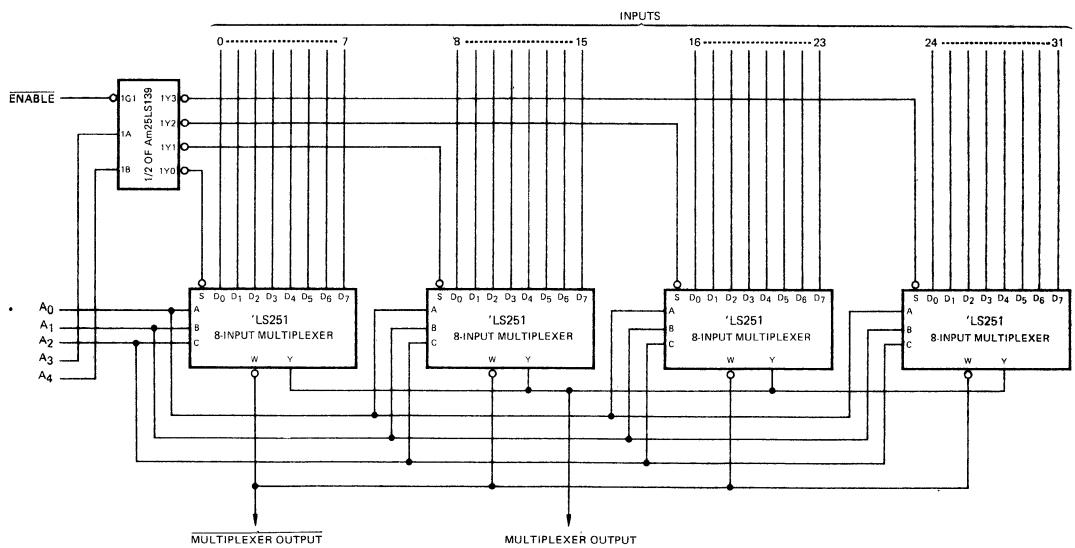
# APPLICATIONS

## LOGIC FUNCTION GENERATION



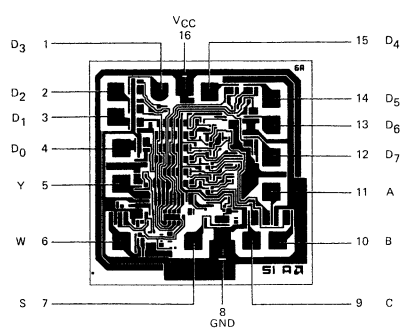

$$Z = \overline{A}\overline{B}CD + \overline{A}BC\overline{D} + A\overline{C}D + AB + AC\overline{D} + B\overline{C}\overline{D}$$

## 32-INPUT MULTIPLEXER



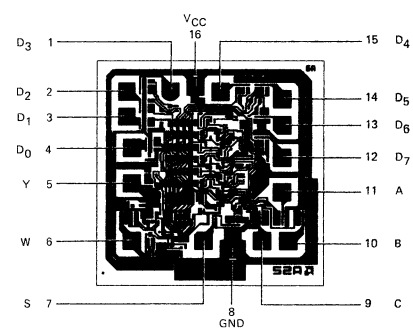

## Metallization and Pad Layouts

### 'LS151




DIE SIZE 0.057" X 0.057"

### 'LS251




DIE SIZE 0.057" X 0.057"

# Am25LS153 • Am54LS/74LS153
# Am25LS253 • Am54LS/74LS253

## Dual 4-Line To 1-Line Data Selectors/Multiplexers

### DISTINCTIVE CHARACTERISTICS

- Performs serial to parallel conversion
- Standard, 'LS153, and three-state, 'LS253, output versions
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

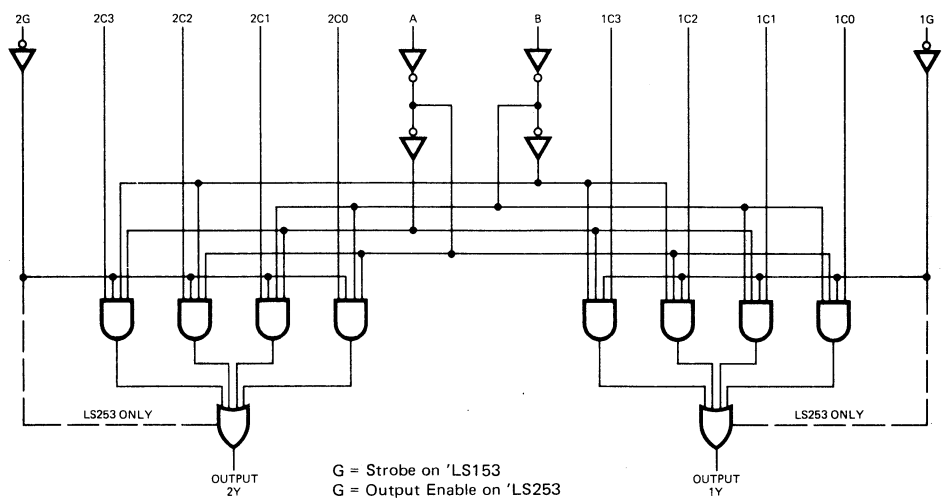
### FUNCTIONAL DESCRIPTION

These dual four-input multiplexers provide the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am25LS153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

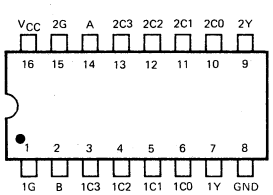
The Am25LS253 features a three-state output to interface with bus-organized systems. Each section of the Am25LS253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

The Am54LS/74LS153 and 253 are standard performance versions of the Am25LS153 and 253. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

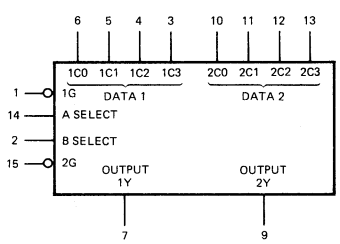



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




VCC = Pin 16
GND = Pin 8

## Am25LS153 • Am25LS253

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | LS153XM | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -440\mu A$ | | 2.5 | 3.4 | | Volts |
| | | LS153XC | | | | 2.7 | 3.4 | | |
| | | LS253XM | | $I_{OH} = -1mA$ | | 2.4 | 3.4 | | |
| | | LS253XC | | $I_{OH} = -2.6mA$ | | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | | $I_{OL} = 4mA$ | | | | 0.4 | Volts |
| | | | | $I_{OL} = 8mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (HIGH Impedance) Output Current Am25LS253 Only | | $V_{CC}$ = MAX. | $V_O = 2.4V$ | | | | 20 | μA |
| | | | | $V_O = 0.4V$ | | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. (Note 4) | | LS153 | | 6.2 | 10 | mA |
| | | | | | LS253 | | 7 | 12 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and all inputs grounded.

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

### DEFINITION OF FUNCTIONAL TERMS

**$1C_i$, $2C_i$** Data Inputs. The four data inputs to each multiplexer; i = 0, 1, 2, and 3.

**1Y, 2Y** Multiplexer Outputs. The output of each four-input multiplexer.

**A, B** Select Inputs. The inputs used to determine which of the four data inputs are selected for the output.

**G** (Am25LS153) Strobe. An active-LOW strobe used to enable the output. A HIGH level input forces the output LOW regardless of the other inputs.

**G** (Am25LS253) Output Control. An active-LOW three-state control used to enable the output. A HIGH level input forces the output to the high-impedance (off) state.

### FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|
| Select | | Data | | | | LS153 Strobe | LS253 Output Control | LS153 Output | LS253 Output |
| B | A | $C_0$ | $C_1$ | $C_2$ | $C_3$ | G | G | Y | Y |
| X | X | X | X | X | X | H | H | L | Z |
| L | L | L | X | X | X | L | L | L | L |
| L | L | H | X | X | X | L | L | H | H |
| L | H | X | L | X | X | L | L | L | L |
| L | H | X | H | X | X | L | L | H | H |
| H | L | X | X | L | X | L | L | L | L |
| H | L | X | X | H | X | L | L | H | H |
| H | H | X | X | X | L | L | L | L | L |
| H | H | X | X | X | H | L | L | H | H |

H = HIGH L = LOW X = Don't Care Z = High Impedance
Note: A & B are common to both 4 input multiplexers.

## Am54LS/74LS153 • Am54LS/74LS253

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 54LS153 | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -400\mu A$ | 2.5 | 3.4 | | Volts |
| | | 74LS153 | | | 2.7 | 3.4 | | |
| | | 54LS253 | | $I_{OH} = -1mA$ | 2.4 | 3.4 | | |
| | | 74LS253 | | $I_{OH} = -2.6mA$ | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | | All, $I_{OL} = 4mA$ | | | 0.4 | Volts |
| | | | | 74LS only, $I_{OL} = 8mA$ | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | 54LS | | | 0.7 | Volts |
| | | | | 74LS | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $V_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (HIGH Impedance) Output Current Am54LS/74LS253 Only | | $V_{CC}$ = MAX. | $V_O = 2.4V$ | | | 20 | μA |
| | | | | $V_O = 0.4V$ | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. (Note 4) | LS153 | | 6.2 | 10 | mA |
| | | | | LS253 | | 7 | 12 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and all inputs grounded.

3

## Am25LS153/54LS153
## SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | | 10 | 15 | | 10 | 15 | ns | $C_L = 15pF$ $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | 10 | 16 | | 17 | 26 | | |
| $t_{PLH}$ | Select to Output | | 19 | 29 | | 19 | 29 | ns | |
| $t_{PHL}$ | | | 15 | 23 | | 25 | 38 | | |
| $t_{PLH}$ | Strobe to Output | | 16 | 24 | | 16 | 24 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | 21 | 32 | | |

## Am25LS153 ONLY
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min. | Am25LS COM'L Max. | Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | | 24 | | 27 | ns | $C_L = 50pF$ $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | 25 | | 29 | | |
| $t_{PLH}$ | Select to Output | | 42 | | 48 | ns | |
| $t_{PHL}$ | | | 34 | | 39 | | |
| $t_{PLH}$ | Strobe to Output | | 35 | | 41 | ns | |
| $t_{PHL}$ | | | 28 | | 32 | | |

*AC performance over the operating temperature range, is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS253/54LS253 SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | | 10 | 15 | | 17 | 25 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 7 | 12 | | 13 | 20 | | |
| $t_{PLH}$ | Select to Output | | 20 | 30 | | 30 | 45 | ns | |
| $t_{PHL}$ | | | 15 | 23 | | 21 | 32 | | |
| $t_{ZH}$ | Output Control to Output | | 17 | 25 | | 15 | 28 | ns | |
| $t_{ZL}$ | | | 12 | 18 | | 15 | 23 | | |
| $t_{HZ}$ | Output Control to Output | | 12 | 18 | | 27 | 42 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 13 | 18 | | 18 | 27 | | |

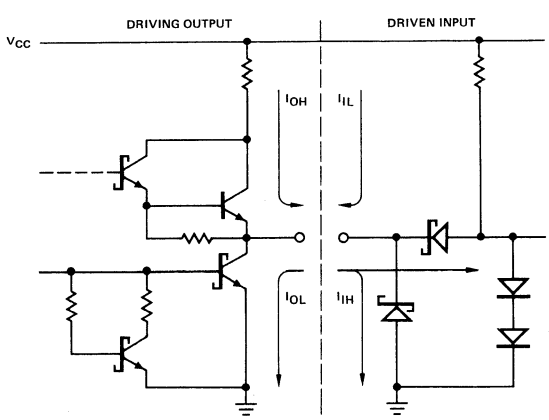
## Am25LS253 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | | 24 | | 27 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 20 | | 23 | | |
| $t_{PLH}$ | Select to Output | | 43 | | 50 | ns | |
| $t_{PHL}$ | | | 34 | | 39 | | |
| $t_{ZH}$ | Output Control to Output | | 37 | | 42 | ns | |
| $t_{ZL}$ | | | 28 | | 32 | | |
| $t_{HZ}$ | Output Control to Output | | 28 | | 32 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 28 | | 32 | | |

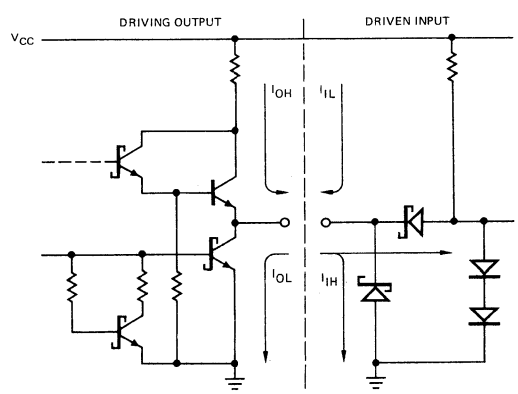
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### Am25LS • 54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

'LS153 STANDARD OUTPUT

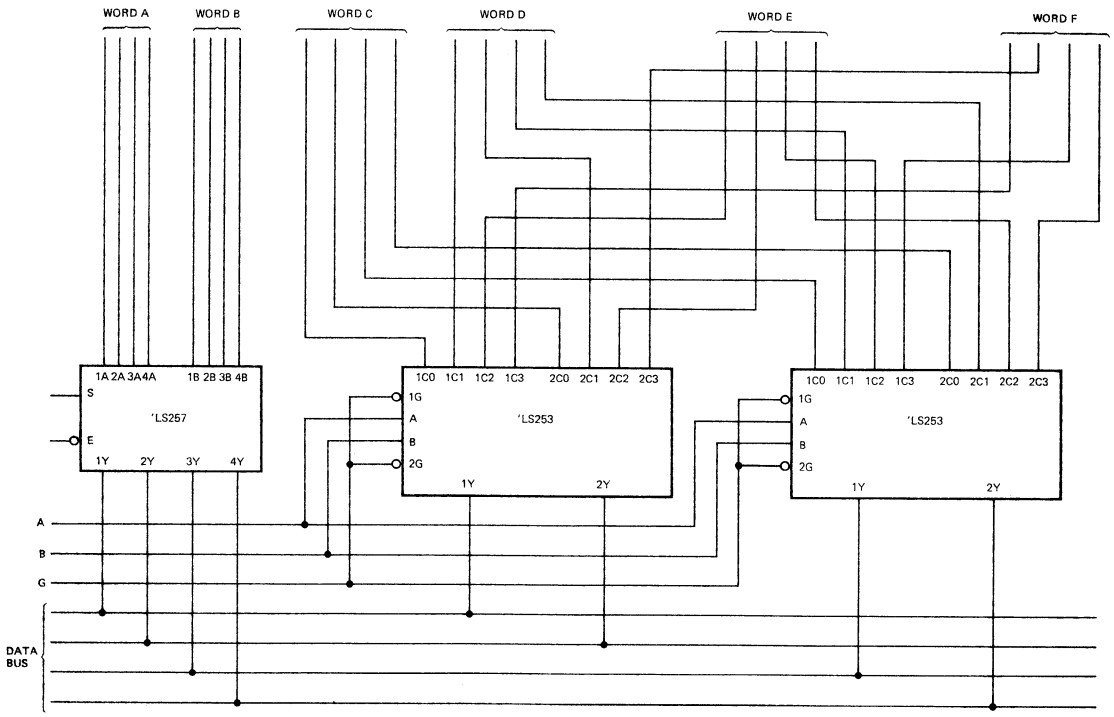



'LS253 THREE-STATE OUTPUT




Note: Actual current flow direction shown.

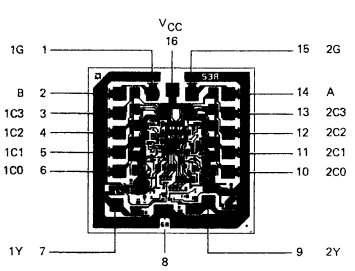
## APPLICATIONS




'LS253 DUAL 4-INPUT MULTIPLEXER IN A BUS-ORGANIZED SYSTEM

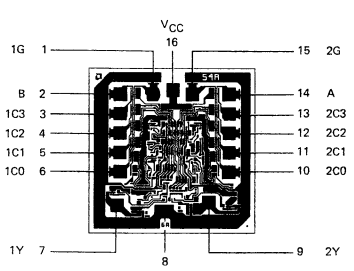
### Metallization and Pad Layout

'LS153




DIE SIZE 0.055" X 0.055"

'LS253




DIE SIZE 0.055" X 0.055"

# Am25LS157 • Am54LS/74LS157
# Am25LS158 • Am54LS/74LS158

## Quadruple 2-Line To 1-Line Data Selectors/Multiplexers

### DISTINCTIVE CHARACTERISTICS

- Selects four of eight data inputs with single select line and overriding strobe
- Inverting 'LS158 and Non-inverting 'LS157 configurations
- Standard TTL outputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

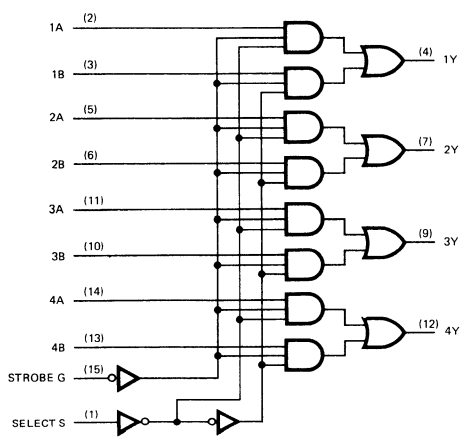
These data selectors/multiplexers are used to select a 4-bit word from one of two sources. The four outputs at the Am25LS157 present true data with respect to the input data. The four outputs of the Am25LS158 present inverted data with respect to the inputs and also minimize propagation delay. A common active-HIGH strobe (active-LOW enable) is provided on all devices.

A single select line, S, is used to select one of the two multiplexer input words. When the select is LOW, the A input word is present at the output. When the select is HIGH, the B input word is present at the output.

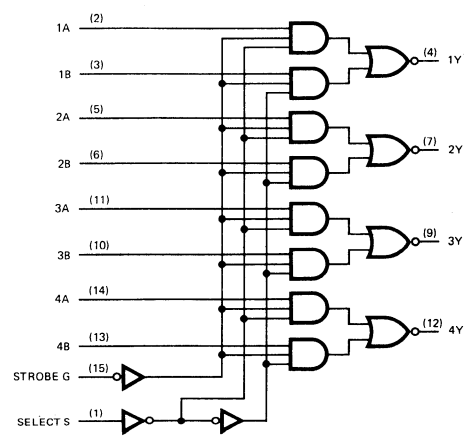
The Am54LS/74LS157 and 158 are standard performance versions of the Am25LS157 and 158. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

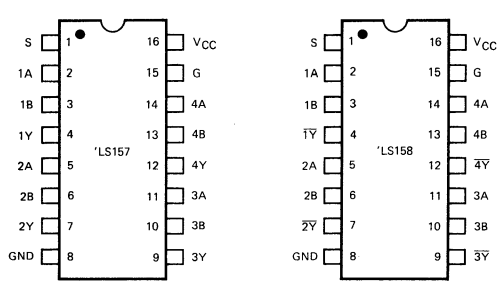
**Am25LS157**
**Am54LS/74LS157**




**Am25LS158**
**Am54LS/74LS158**

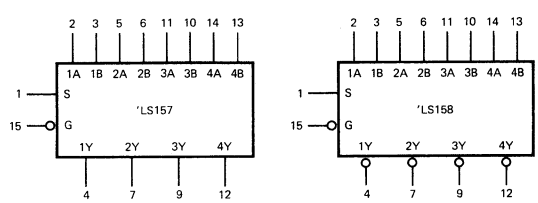



### CONNECTION DIAGRAMS
**Top Views**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## Am25LS157 • Am25LS158

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | S or G | | | −0.36 | mA |
| | | | A or B | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | S or G | | | 20 | μA |
| | | | A or B | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | S or G | | | 0.1 | mA |
| | | | A or B | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | LS157 | | 9.7 | 16 | mA |
| | | | LS158 | | 4.8 | 8 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and 4.5V applied to all inputs.

3

## Am54LS/74LS157 • Am54LS/74LS158

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | Am54LS | 2.5 | 3.4 | | Volts |
| | | | Am74LS | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | Am54LS | | | 0.7 | Volts |
| | | | Am74LS | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | S or G | | | −0.8 | mA |
| | | | A or B | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | S or G | | | 40 | μA |
| | | | A or B | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | S or G | | | 0.2 | mA |
| | | | A or B | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | LS157 | | 9.7 | 16 | mA |
| | | | LS158 | | 4.8 | 8 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and 4.5V applied to all inputs.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am25LS157 • Am54LS/74LS157
## Am25LS158 • Am54LS/74LS158
## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | LS157 | | 8 | 12 | | 9 | 14 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| | | LS158 | | 5 | 9 | | 7 | 12 | | |
| $t_{PHL}$ | Data to Output | LS157 | | 8 | 12 | | 9 | 14 | ns | |
| | | LS158 | | 7 | 11 | | 7 | 12 | | |
| $t_{PLH}$ | Strobe to Output | LS157 | | 12 | 18 | | 13 | 20 | ns | |
| | | LS158 | | 8 | 12 | | 11 | 17 | | |
| $t_{PHL}$ | Strobe to Output | LS157 | | 10 | 16 | | 14 | 21 | ns | |
| | | LS158 | | 11 | 17 | | 12 | 18 | | |
| $t_{PLH}$ | Select to Output | LS157 | | 15 | 23 | | 15 | 23 | ns | |
| | | LS158 | | 13 | 20 | | 13 | 20 | | |
| $t_{PHL}$ | Select to Output | LS157 | | 14 | 21 | | 18 | 27 | ns | |
| | | LS158 | | 14 | 21 | | 16 | 24 | | |

## Am25LS ONLY
## SWITCHING CHARACTERISTICS
## OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL: $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | LS157 | | 20 | | 23 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| | | LS158 | | 16 | | 18 | | |
| $t_{PHL}$ | Data to Output | LS157 | | 20 | | 23 | ns | |
| | | LS158 | | 18 | | 21 | | |
| $t_{PLH}$ | Strobe to Output | LS157 | | 28 | | 32 | ns | |
| | | LS158 | | 20 | | 23 | | |
| $t_{PHL}$ | Strobe to Output | LS157 | | 25 | | 29 | ns | |
| | | LS158 | | 26 | | 30 | | |
| $t_{PLH}$ | Select to Output | LS157 | | 34 | | 39 | ns | |
| | | LS158 | | 30 | | 35 | | |
| $t_{PHL}$ | Select to Output | LS157 | | 31 | | 36 | ns | |
| | | LS158 | | 31 | | 36 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**1A, 2A, 3A, 4A** The data inputs for the 4-bits of the A word.

**1B, 2B, 3B, 4B** The data inputs for the 4-bits of the B word.

**1Y, 2Y, 3Y, 4Y** The four outputs of the multiplexer. The input data is inverted at the output on the Am25LS158 and non-inverted at the output for the Am25LS157.

**G** Strobe. When the strobe is HIGH, the four outputs of the Am25LS157 are LOW and the outputs of the Am25LS158 are HIGH. When the strobe is LOW, the devices are enabled to pass data.

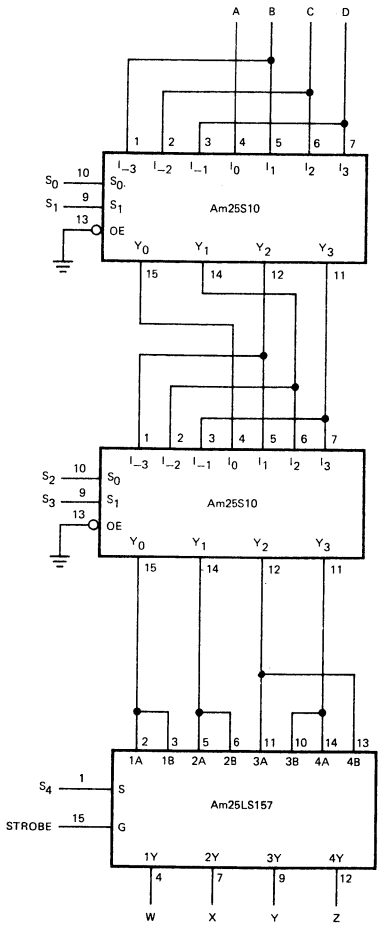
**S** Select. When the select input is LOW, the A word is present at the output. When the select input is HIGH, the B word is present at the output.

## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| Strobe G | Select S | Data A | Data B | LS157 Y | LS158 Y |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = HIGH L = LOW X = Don't Care

## APPLICATION



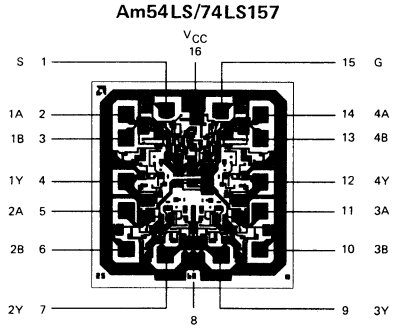

### FUNCTION TABLE

| State Number | Select $S_4$ | $S_3$ | $S_2$ | $S_1$ | $S_0$ | Output W | X | Y | Z |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | A | C | B | D |
| 1 | 0 | 0 | 0 | 0 | 1 | D | B | A | C |
| 2 | 0 | 0 | 0 | 1 | 0 | C | A | D | B |
| 3 | 0 | 0 | 0 | 1 | 1 | B | D | C | A |
| 4 | 0 | 0 | 1 | 0 | 0 | D | A | C | B |
| 5 | 0 | 0 | 1 | 0 | 1 | C | D | B | A |
| 6 | 0 | 0 | 1 | 1 | 0 | B | C | A | D |
| 7 | 0 | 0 | 1 | 1 | 1 | A | B | D | C |
| 8 | 0 | 1 | 0 | 0 | 0 | B | D | A | C |
| 9 | 0 | 1 | 0 | 0 | 1 | A | C | D | B |
| 10 | 0 | 1 | 0 | 1 | 0 | D | B | C | A |
| 11 | 0 | 1 | 0 | 1 | 1 | C | A | B | D |
| 12 | 0 | 1 | 1 | 0 | 0 | C | B | D | A |
| 13 | 0 | 1 | 1 | 0 | 1 | B | A | C | D |
| 14 | 0 | 1 | 1 | 1 | 0 | A | D | B | C |
| 15 | 0 | 1 | 1 | 1 | 1 | D | C | A | B |
| 16 | 1 | 0 | 0 | 0 | 0 | State 9 | | | |
| 17 | 1 | 0 | 0 | 0 | 1 | State 10 | | | |
| 18 | 1 | 0 | 0 | 1 | 0 | State 11 | | | |
| 19 | 1 | 0 | 0 | 1 | 1 | State 8 | | | |
| 20 | 1 | 0 | 1 | 0 | 0 | D | A | B | C |
| 21 | 1 | 0 | 1 | 0 | 1 | C | D | A | B |
| 22 | 1 | 0 | 1 | 1 | 0 | B | C | D | A |
| 23 | 1 | 0 | 1 | 1 | 1 | A | B | C | D |
| 24 | 1 | 1 | 0 | 0 | 0 | State 3 | | | |
| 25 | 1 | 1 | 0 | 0 | 1 | State 0 | | | |
| 26 | 1 | 1 | 0 | 1 | 0 | State 1 | | | |
| 27 | 1 | 1 | 0 | 1 | 1 | State 2 | | | |
| 28 | 1 | 1 | 1 | 0 | 0 | C | B | A | D |
| 29 | 1 | 1 | 1 | 0 | 1 | B | A | D | C |
| 30 | 1 | 1 | 1 | 1 | 0 | A | D | C | B |
| 31 | 1 | 1 | 1 | 1 | 1 | D | C | B | A |

Two Am25S10 four-bit shifters are used in conjunction with an Am25LS157 multiplexer to perform all possible permutations on four inputs. The number of combinations possible on n items is given as n!. Thus, for n equal to 4,24 combinations are possible. The Function Table shows all 32 combinations of the 5-bit select code including the 8 redundant states. This connection can be particularly useful in security systems and certain random number generation schemes. The eight redundant states can be placed at other select field locations through proper design.

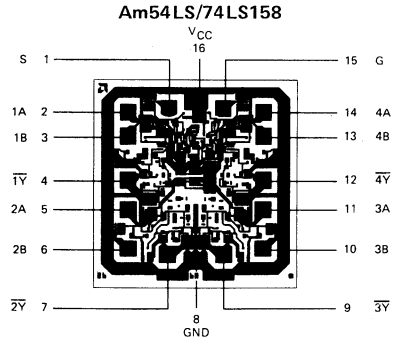
## Metallization and Pad Layouts

**Am25LS157**
**Am54LS/74LS157**




DIE SIZE 0.057" X 0.057"

**Am25LS158**
**Am54LS/74LS158**




DIE SIZE 0.057" X 0.057"

# Am25LS160A/161A/162A/163A
# Am54LS/74LS160A/161A/162A/163A

## Synchronous Four-Bit Counters

### DISTINCTIVE CHARACTERISTICS

- Synchronous presettable counters
- Decade ('LS160A and 'LS162A) and binary ('LS161A and 'LS163A) counters
- Asynchronous ('LS160A and 'LS161A) and synchronous ('LS162A and 'LS163A) clear inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440$\mu$A source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS160A, Am25LS161A, Am25LS162A and Am25LS163A synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am25LS160A and Am25LS162A are decade counters and the Am25LS161A and Am25LS163A are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. The load need meet only the set-up and hold time requirements with respect to the clock.

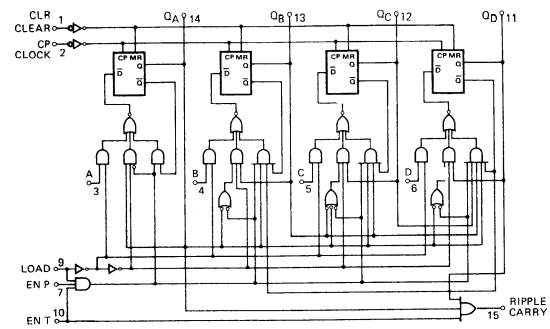
The Am25LS160A and the Am25LS161A feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am25LS 162A and Am25LS163A have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. The enable P or T inputs need meet only the set-up and hold time requirements with respect to the clock.

The Am54LS/74LS160A series are standard performance versions of the Am25LS160A series counters. See appropriate electrical characteristic tables for detailed Am25LS improvements.

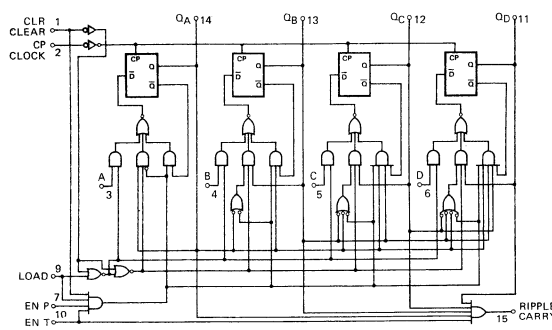
### LOGIC DIAGRAMS

**Am25LS160A Synchronous Decade Counter**




Am25LS162A synchronous decade counters are similar; however, the clear is synchronous as shown for the Am25LS163A binary counters.

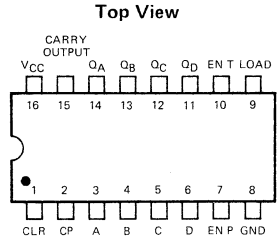
**Am25LS163A Synchronous Binary Counter**




Am25LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the Am25LS160A decade counters.

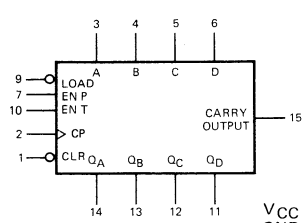
### CONNECTION DIAGRAM

**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## Am25LS160A, 161A, 162A and 163A
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440µA<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | 0.25 | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | A, B, C, D, EN P, CP | | | −0.4 | mA |
| | | | Load, EN T | | | −0.8 | |
| | | | Clear '160A, '161A | | | −0.4 | |
| | | | Clear '162A, '163A | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | A, B, C, D, EN P, CP | | | 20 | µA |
| | | | Load, EN T | | | 40 | |
| | | | Clear '160A, '161A | | | 20 | |
| | | | Clear '162A, '163A | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | A, B, C, D, EN P, CP | | | 0.1 | mA |
| | | | Load, EN T | | | 0.2 | |
| | | | Clear '160A, '161A | | | 0.1 | |
| | | | Clear '162A, '163A | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CCH}$ | Power Supply Current All Outputs HIGH | $V_{CC}$ = MAX. (Note 4) | | | 18 | 31 | mA |
| $I_{CCL}$ | Power Supply Current All Outputs LOW | $V_{CC}$ = MAX. (Note 5) | | | 19 | 32 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CCH}$ is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.
5. $I_{CCL}$ is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

3

## Am54LS/74LS160A, 161A, 162A and 163A

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | 0.25 | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | 0.35 | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | A, B, C, D, EN P | | | −0.4 | mA |
| | | | Load, EN T, CP | | | −0.8 | |
| | | | Clear '160A, '161A | | | −0.4 | |
| | | | Clear '162A, '163A | | | −0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | A, B, C, D, EN P | | | 20 | μA |
| | | | Load, CP, EN T | | | 40 | |
| | | | Clear '160A, '161A | | | 20 | |
| | | | Clear '162A, '163A | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | A, B, C, D, EN P | | | 0.1 | mA |
| | | | Load, CP, EN T | | | 0.2 | |
| | | | Clear '160A, '161A | | | 0.1 | |
| | | | Clear '162A, '163A | | | 0.2 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CCH}$ | Power Supply Current All Outputs HIGH | $V_{CC}$ = MAX. (Note 4) | | | 18 | 31 | mA |
| $I_{CCL}$ | Power Supply Current All Outputs LOW | $V_{CC}$ = MAX. (Note 5) | | | 19 | 32 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CCH}$ is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.
5. $I_{CCL}$ is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Carry Output | | | 20 | 30 | | 20 | 35 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 18 | 28 | | 18 | 35 | | |
| $t_{PLH}$ | Clock to Q Output with Load Input HIGH | | | 10 | 18 | | 13 | 24 | ns | |
| $t_{PHL}$ | | | | 12 | 20 | | 18 | 27 | | |
| $t_{PLH}$ | Enable T to Carry Output | | | 8 | 14 | | 9 | 14 | ns | |
| $t_{PHL}$ | | | | 8 | 14 | | 9 | 14 | | |
| $t_{PLH}$ | Clock to Q Output with Load Input LOW | | | 10 | 18 | | 13 | 24 | ns | |
| $t_{PHL}$ | | | | 12 | 20 | | 18 | 27 | | |
| $t_{PHL}$ | Clear to Q Output (Note 1) | | | 18 | 28 | | 20 | 28 | ns | |
| $t_{pw}$ | Pulse Width | Clock | 25 | | | 25 | | | ns | |
| | | Clear | 20 | | | 20 | | | | |
| $t_s$ | Set-up Time | Data – A, B, C, D | 20 | | | 20 | | | ns | |
| | | Enable P | 20 | | | 20 | | | | |
| | | Load, Enable T | 20 | | | 20 | | | | |
| | | Clear (Note 2) | 20 | | | 20 | | | | |
| $t_h$ | Hold Time – Any Input | | 3 | | | 3 | | | ns | |
| $f_{max}$ (Note 3) | Maximum Clock Frequency | | 35 | 50 | | 25 | 32 | | MHz | |

Notes: 1. Measured from clear input on 'LS160A and 'LS161A. Measured from clock input on 'LS162A and 'LS163A.
2. Applies to 'LS162A and 'LS163A only.
3. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Carry Output | | | 43 | | 50 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 40 | | 47 | | |
| $t_{PLH}$ | Clock to Q Output with Load Input HIGH | | | 28 | | 32 | ns | |
| $t_{PHL}$ | | | | 30 | | 35 | | |
| $t_{PLH}$ | Enable T to Carry Output | | | 18 | | 21 | ns | |
| $t_{PHL}$ | | | | 18 | | 21 | | |
| $t_{PLH}$ | Clock to Q Output with Load Input LOW | | | 28 | | 32 | ns | |
| $t_{PHL}$ | | | | 30 | | 35 | | |
| $t_{PHL}$ | Clear to Q Output (Note 1) | | | 41 | | 47 | ns | |
| $t_{pw}$ | Pulse Width | Clock | 37 | | 42 | | ns | |
| | | Clear | 30 | | 35 | | | |
| $t_s$ | Set-up Time | Data – A, B, C, D | 30 | | 35 | | ns | |
| | | Enable P | 30 | | 35 | | | |
| | | Load, Enable T | 30 | | 35 | | | |
| | | Clear (Note 2) | 30 | | 35 | | | |
| $t_h$ | Hold Time – Any Input | | 8 | | 9 | | ns | |
| $f_{max}$ (Note3) | Maximum Clock Frequency | | 26 | | 23 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

## DEFINITION OF FUNCTIONAL TERMS

**CP** Clock pulse. Enters data or counts on the positive-going edge.

**CLR** Clear. On the Am25LS160A and Am25LS161A, the clear is asynchronous. A LOW on the clear sets all four flip-flops LOW. On the Am25LS162A and Am25LS163A the clear is synchronous. A LOW on the clear sets all four flip-flops LOW after the next positive-going clock edge.

**Load** Load. When the load is LOW, data on the A, B, C and D inputs is transferred to the output on the positive-going clock edge. When the load is HIGH, the counter is enabled.

**EN P** Enable P. Parallel count enable. Must be HIGH to count.

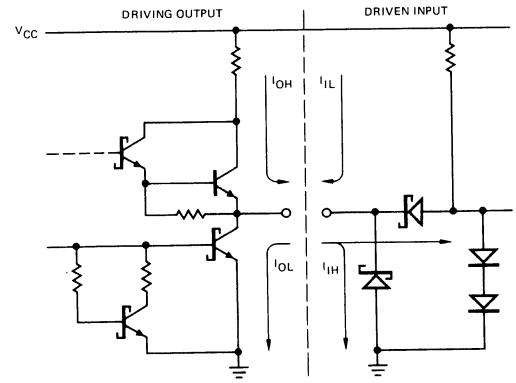
**EN T** Enable T. Serial trickle count enable. Must be HIGH to count.

**A, B, C, D** The four counter parallel inputs.

$Q_A$, $Q_B$, $Q_C$, $Q_D$ The four counter outputs.

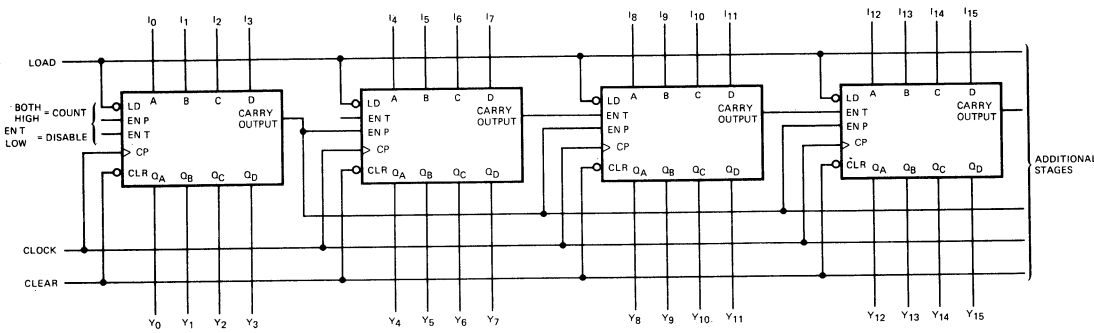
**Carry Output** Carry look-ahead circuitry for cascading. Will be HIGH when the four-bit counter is maximum (1001 for BCD and 1111 for binary).

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



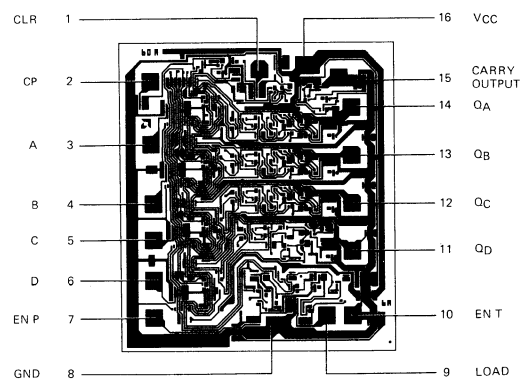

Note: Actual current flow direction shown.

## APPLICATIONS




High-speed, look-ahead carry counter for BCD (Am25LS160A or Am25LS162A) or binary (Am25LS161A or Am25LS163A). Can count modulo N, $N_1$-to-$N_2$, or $N_1$-to-N maximum.

### Metallization and Pad Layout




DIE SIZE 0.072" X 0.082"

# Am25LS164 • Am54LS/74LS164

## 8-Bit Serial-In, Parallel-Out Shift Register

### DISTINCTIVE CHARACTERISTICS

- Gated serial inputs
- Asynchronous clear
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

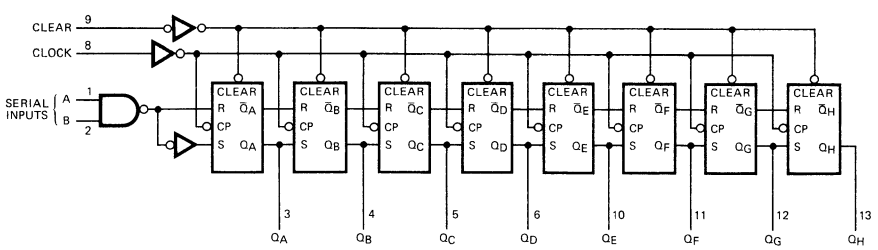
### FUNCTIONAL DESCRIPTION

The Am25LS164 and Am54LS/74LS164 are eight-bit, serial in/parallel out shift registers built using advanced Low-Power Schottky processing. A gated input provides enable/disable control over incoming data such that the data can be entered or logic zeros can be entered into the register.

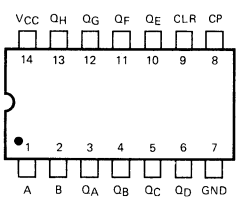
An asynchronous clear input can be used to simultaneously clear the eight flip-flops in the device. When the clear input is LOW, all internal flip-flops are forced LOW independent of the clock input. An incoming data bit is entered into the $Q_a$ flip-flop and the data in all internal flip-flops is shifted right on the LOW-to-HIGH transition of the clock input.

The Am54LS/74LS164 is a standard performance version of the Am25LS164. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

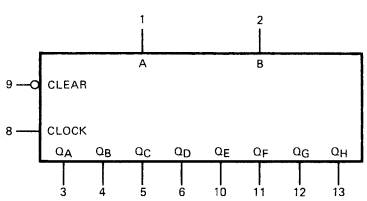



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 14
GND = Pin 7

## Am25LS164

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | 0.25 | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Clock, Clear | | | −0.36 | mA |
| | | | A, B | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 16 | 27 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V applied to the clear input.

## Am25LS • Am54LS/74LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

### DEFINITION OF FUNCTIONAL TERMS

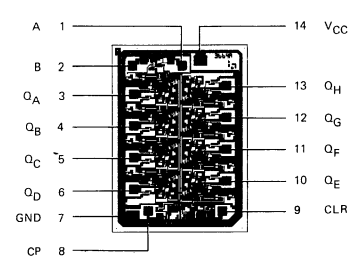
**A, B** The serial inputs to the device. If either the A input is LOW or the B input is LOW, the $Q_A$ flip-flop will be set LOW on the LOW-to-HIGH transition of the clock.

**Clear** An asynchronous master reset for the eight flip-flops in the device. When the clear input is LOW, all internal flip-flops are set LOW independent of the clock.

**$Q_A$-$Q_H$** The eight true outputs of the eight-bit register.

**Clock** The clock input to the register. Data is entered into the register on the LOW-to-HIGH transition of the clock input.

### Metallization and Pad Layout




DIE SIZE 0.066" X 0.090"

## Am54LS/74LS164
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

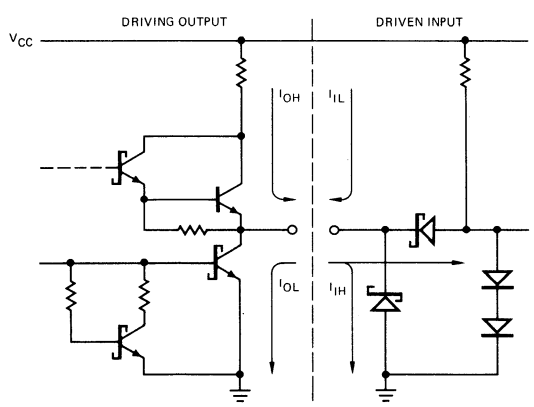
## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0mA | | 0.25 | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8.0mA | | 0.35 | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 16 | 27 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V applied to the clear input.

3

### Am25LS • Am54LS/74LS
### LOW POWER SCHOTTKY INPUT/OUTPUT
### CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 14 | 20 | | 17 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 15 | 22 | | 21 | 32 | | |
| $t_{PHL}$ | Clear to Output | | 19 | 29 | | 24 | 36 | ns | |
| $t_{pw}$ | Clock or Clear | 17 | | | 20 | | | ns | |
| $t_s$ | Data | 10 | | | 15 | | | ns | |
| $t_h$ | Data | 5.0 | | | 5.0 | | | ns | |
| $t_s$ | Clear Recovery Time | 20 | | | — | — | | ns | |
| $f_{max}$(Note 1) | Maximum Clock Frequency | 35 | 42 | | 25 | 36 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS ONLY
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 26 | | 30 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 30 | | 35 | | |
| $t_{PHL}$ | Clear to Output | | 37 | | 42 | ns | |
| $t_{pw}$ | Clock or Clear | 22 | | 25 | | ns | |
| $t_s$ | Data | 13 | | 15 | | ns | |
| $t_h$ | Data | 5 | | 5 | | ns | |
| $t_s$ | Clear Recovery Time | 25 | | 30 | | ns | |
| $f_{max}$(Note 1) | Maximum Clock Frequency | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## TRUTH TABLE

| Function | Clear | Clock | Serial A | Serial B | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ | $Q_H$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | L | X | X | X | L | L | L | L | L | L | L | L |
| Shift Right | H | ↑ | L | L | L | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ |
| | H | ↑ | L | H | L | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ |
| | H | ↑ | H | L | L | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ |
| | H | ↑ | H | H | H | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ |

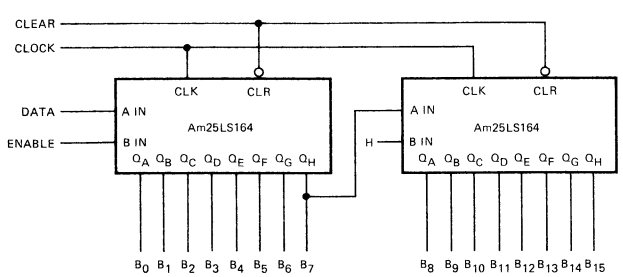
L = LOW
H = HIGH
↑ = LOW-to-HIGH transition
X = Don't care

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS164 Order Number | SN54/74LS164 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS164PC | SN74LS164N |
| Hermetic DIP | 0°C to +70°C | AM25LS164DC | SN74LS164J |
| Dice | 0°C to +70°C | AM25LS164XC | SN74LS164X |
| Hermetic DIP | –55°C to +125°C | AM25LS164DM | SN54LS164J |
| Hermetic Flat Pak | –55°C to +125°C | AM25LS164FM | SN54LS164W |
| Dice | –55°C to +125°C | AM25LS164XM | SN54LS164X |

3

## APPLICATION




**16-Bit Serial In Parallel Out Register.**

# Am25LS168A • Am25LS169A
# Am54LS/74LS168A • Am54LS/74LS169A

## Synchronous Four-Bit Programmable Up-Down Counter

### DISTINCTIVE CHARACTERISTICS

- All operations are synchronous
- Internal look-ahead carry logic for high-speed counting
- Ripple carry output provided for cascading
- One line up/down control
- Changes state on LOW-to-HIGH transition of clock
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440$\mu$A source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

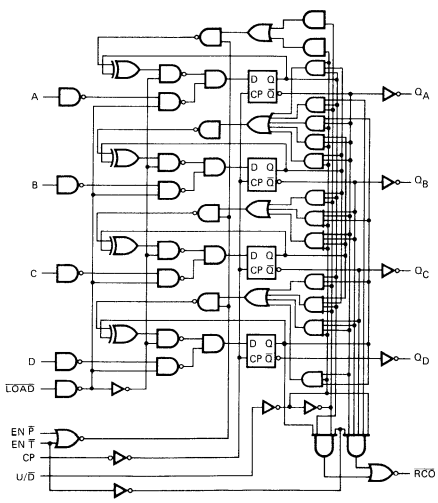
### FUNCTIONAL DESCRIPTION

The 'LS168A and 'LS169A are fully synchronous programmable up/down counters. All operations occur on the positive edge of the clock input. Proper operation only requires the user to meet the set-up and hold times. With the LOAD input LOW the outputs will be programmed by the parallel data inputs on the LOW-to-HIGH transition of the clock. Counting is enabled only when $\overline{EN\ T}$ and $\overline{EN\ P}$ are LOW. The up/down inputs (U/$\overline{D}$) control of the direction of the count. HIGH counts up and LOW counts down. Internal Look-Ahead Carry logic and active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up count, the $\overline{RCO}$ is LOW at binary 9 for the 'LS168A (binary 15 for the 'LS169A) and upon down count, it is LOW at binary 0 (same for the 'LS169A). Cascaded operation requires only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{EN\ T}$.

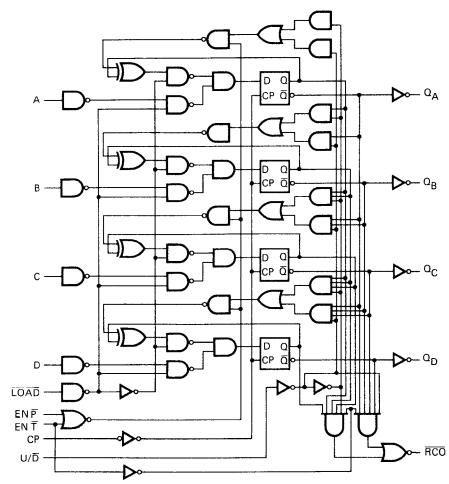
The Am54LS/74LS168A and 169A are standard performance versions of the Am25LS168A and 169A. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

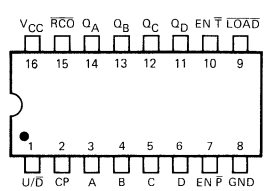
'LS168A




'LS169A

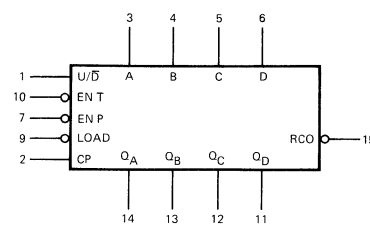



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## Am25LS168A • Am25LS169A
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% | MIN. = 4.50 V | MAX. = 5.50 V |

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | EN $\overline{T}$ | | | −0.6 | mA |
| | | | All others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | EN $\overline{T}$ | | | 30 | μA |
| | | | All others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | EN $\overline{T}$ | | | 0.15 | mA |
| | | | All others | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 20 | 34 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded; outputs open; measured after a ground then 4.5 V on the clock input.

## Am25LS • Am54LS/74LS
## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS168A • Am54LS/74LS169A

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0\,V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\,V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8.0mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4\,V$ | EN $\overline{T}$ | | | −0.6 | mA |
| | | | All others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7\,V$ | EN $\overline{T}$ | | | 30 | µA |
| | | | All others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0\,V$ | EN $\overline{T}$ | | | 0.15 | mA |
| | | | All others | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 20 | 34 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded; outputs open; measured after a ground then 4.5 V on the clock input.

### FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CP | A | B | C | D | $\overline{LOAD}$ | EN $\overline{T}$ | EN $\overline{P}$ | U/$\overline{D}$ | $\overline{RCO}$ | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | COMMENTS |
| ↑ | X | X | X | X | H | L | L | H | A/R(1) | | | $(Q_{T-CK}) + 1$ | | Count Up |
| ↑ | X | X | X | X | H | L | L | L | A/R(2) | | | $(Q_{T-CK}) - 1$ | | Count Down |
| ↑ | X | X | X | X | H | H | X | X | NC | | | NC | | Count Inhibit |
| ↑ | X | X | X | X | H | X | H | X | NC | | | NC | | |
| NC | X | X | X | X | H | L | X | H | L | H | H | H | H | Overflow ('LS169A) |
| | X | X | X | X | H | L | X | H | L | (H | X | X | H) | ('LS168A) |
| NC | X | X | X | X | H | H | X | H | H | H | H | H | H | Overflow Inhibit ('LS169A) |
| | X | X | X | X | H | H | X | H | H | (H | X | X | H) | ('LS168A) |
| NC | X | X | X | X | H | L | X | L | L | L | L | L | L | Underflow |
| NC | X | X | X | X | H | H | X | L | H | L | L | L | L | Underflow Inhibit |
| ↑ | L | H | L | H | L | L | L | X | H | L | H | L | H | Load Example |

Notes: 1. LOW for one clock cycle when maximum count is reached; otherwise HIGH.
2. LOW for one clock cycle when minimum count is reached; otherwise HIGH.

H = HIGH
L = LOW
X = Don't Care

$(Q_{T-CK})$ = Output State Prior to Clock Edge.
A/R = Assumes Required State at Output.
NC = No Change.

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0 V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Ripple Carry | | | 23 | 35 | | 23 | 35 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 19 | 35 | | 23 | 35 | | |
| $t_{PLH}$ | Clock to Any Q | | | 13 | 20 | | 13 | 20 | ns | |
| $t_{PHL}$ | | | | 15 | 23 | | 15 | 23 | | |
| $t_{PLH}$ | Enable $\overline{T}$ to Ripple Carry | | | 10 | 14 | | 10 | 14 | ns | |
| $t_{PHL}$ | | | | 9 | 14 | | 10 | 14 | | |
| $t_{PLH}$ | Up/Down to Ripple Carry | | | 17 | 25 | | 17 | 25 | ns | |
| $t_{PHL}$ | | | | 17 | 29 | | 19 | 29 | | |
| $t_{pw}$ | Clock Pulse Width | | 25 | | | 25 | | | ns | |
| $t_s$ | Set-up | A, B, C, D | 20 | | | 20 | | | ns | |
| | | $\overline{EN}$ P, $\overline{EN}$ $\overline{T}$ | 20 | | | 20 | | | | |
| | | Load | 25 | | | 25 | | | ns | |
| | | Up/Down | 30 | | | 30 | | | | |
| $t_h$ | Hold, any Input | | 0 | | | 0 | | | ns | |
| $f_{max}$(Note 1) | Maximum Clock Frequency | | 25 | 2 | | 25 | 32 | | MHz | |

Note 1. Per industry convention, $f_{max}$ if the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

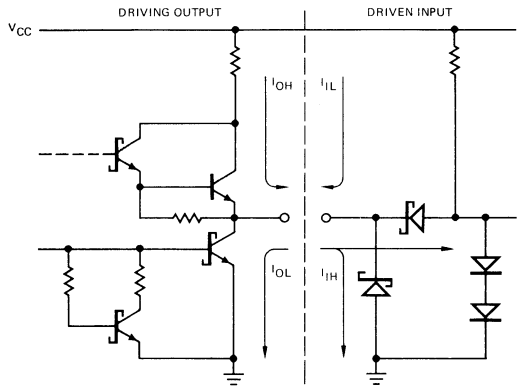
3

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0 V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL: $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0 V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Ripple Carry | | | 49 | | 57 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 49 | | 57 | | |
| $t_{PLH}$ | Clock to Any Q | | | 30 | | 35 | ns | |
| $t_{PHL}$ | | | | 34 | | 39 | | |
| $t_{PLH}$ | Enable $\overline{T}$ to Ripple Carry | | | 22 | | 26 | ns | |
| $t_{PHL}$ | | | | 22 | | 26 | | |
| $t_{PLH}$ | Up/Down to Ripple Carry | | | 36 | | 42 | ns | |
| $t_{PHL}$ | | | | 42 | | 48 | | |
| $t_{pw}$ | Clock Pulse Width | | 36 | | 42 | | ns | |
| $t_s$ | Set-Up | A, B, C, D | 30 | | 35 | | ns | |
| | | EN $\overline{T}$, EN $\overline{P}$ | 30 | | 35 | | | |
| | | Load | 36 | | 42 | | ns | |
| | | Up/Down | 43 | | 50 | | | |
| $t_h$ | Hold | | 0 | | 0 | | ns | |
| $f_{max}$(Note 1) | Maximum Clock Frequency | | 19 | | 17 | | MHz | |

*AC performance over operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



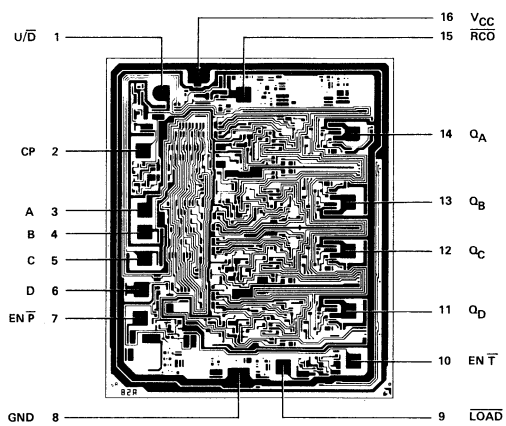

Note: Actual current flow direction shown.

## DEFINITION OF FUNCTIONAL TERMS

| | |
|---|---|
| CP | Clock Pulse. All functions of the counter occurs on the positive edge. |
| A, B, C, D | The four programmable data inputs. |
| EN $\overline{P}$ | Parallel Count Enable. Must be LOW to count. |
| EN $\overline{T}$ | Enables RCO (serial trickle) for cascading counters. Must be LOW to count. |
| $Q_A$, $Q_B$, $Q_C$, $Q_D$ | The four counter outputs. |
| $\overline{LOAD}$ | A LOW enables parallel load of counter outputs from inputs. Must be HIGH to count. |
| $\overline{RCO}$ | Ripple Carry Output. Output will be LOW on the maximum count on up count, and on 0000 on the down count. |
| U/$\overline{D}$ | Up/Down Count Control. HIGH counts up and LOW counts down. |

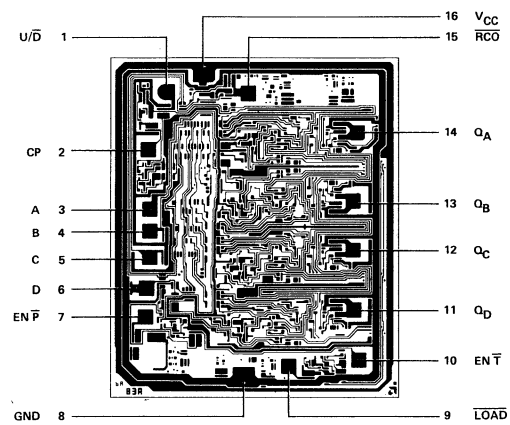
## Metallization and Pad Layouts

### 'LS168A




DIE SIZE 0.084" X 0.099"

### 'LS169A

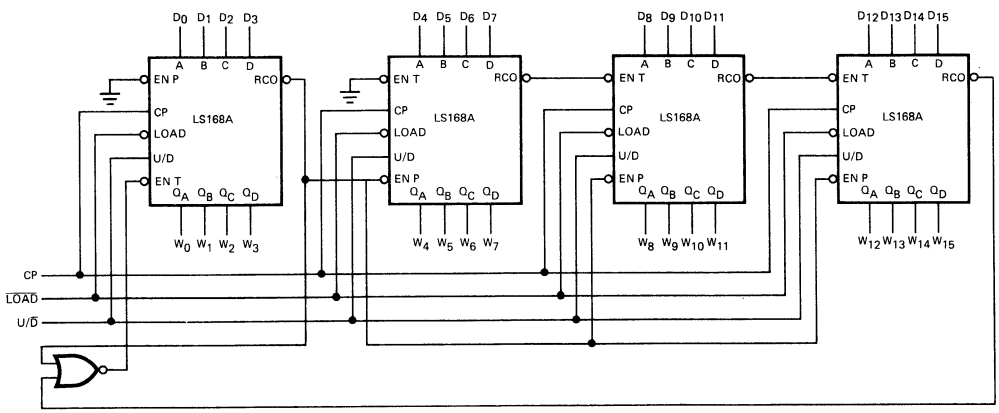



DIE SIZE 0.084" X 0.099"

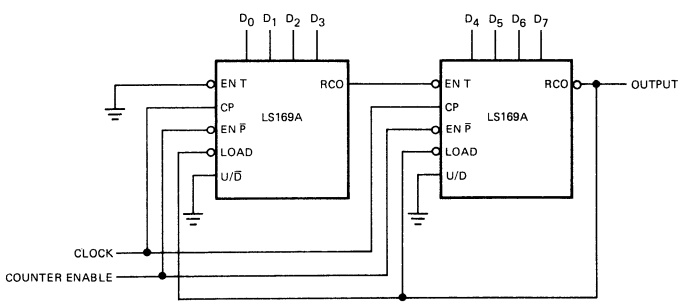
## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS168A Order Number | Am25LS169A Order Number | Am54LS/ 74LS168A Order Number | Am54LS/ 74LS169A Order Number |
|---|---|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS168APC | AM25LS169APC | SN74LS168AN | SN74LS169AN |
| Hermetic DIP | 0°C to +70°C | AM25LS168ADC | AM25LS169ADC | SN74LS168AJ | SN74LS169AJ |
| Dice | 0°C to +70°C | AM25LS168AXC | AM25LS169AXC | SN74LS168AX | SN74LS169AX |
| Hermetic DIP | –55°C to +125°C | AM25LS168ADM | AM25LS169ADM | SN54LS168AJ | SN54LS169AJ |
| Hermetic Flat Pak | –55°C to +125°C | AM25LS168AFM | AM25LS169AFM | SN54LS168AW | SN54LS169AW |
| Dice | –55°C to +125°C | AM25LS168AXM | AM25LS169AXM | SN54LS168AX | SN54LS169AX |

## APPLICATIONS




Synchronous 4-Bit BCD Programmable Up/Down Counter with Hold on Underflow and Overflow, enabled by $\overline{\text{LOAD}}$, Single count sequence per load cycle.




Programmable Divide By N.
Example: Divide By 127, Load (N-1) or 126 = 01111110.

# Am25LS170•Am25LS670
# Am54LS/74LS170•Am54LS/74LS670

## 4-BY-4 Register File with 3-State or Open Collector Outputs

### DISTINCTIVE CHARACTERISTICS

- Separate read/write addressing
- Simultaneous read and write
- 4-word by 4-bit organization
- Am25LS170 has open collector outputs
- Am25LS670 has three-state outputs
- Cascadable to m words of n bits (Mod 4)
- Used as
  - Scratchpad memory
  - Buffer storage with timing synchronizing
  - Storage for fast multiply (signal processing)
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440$\mu$A source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

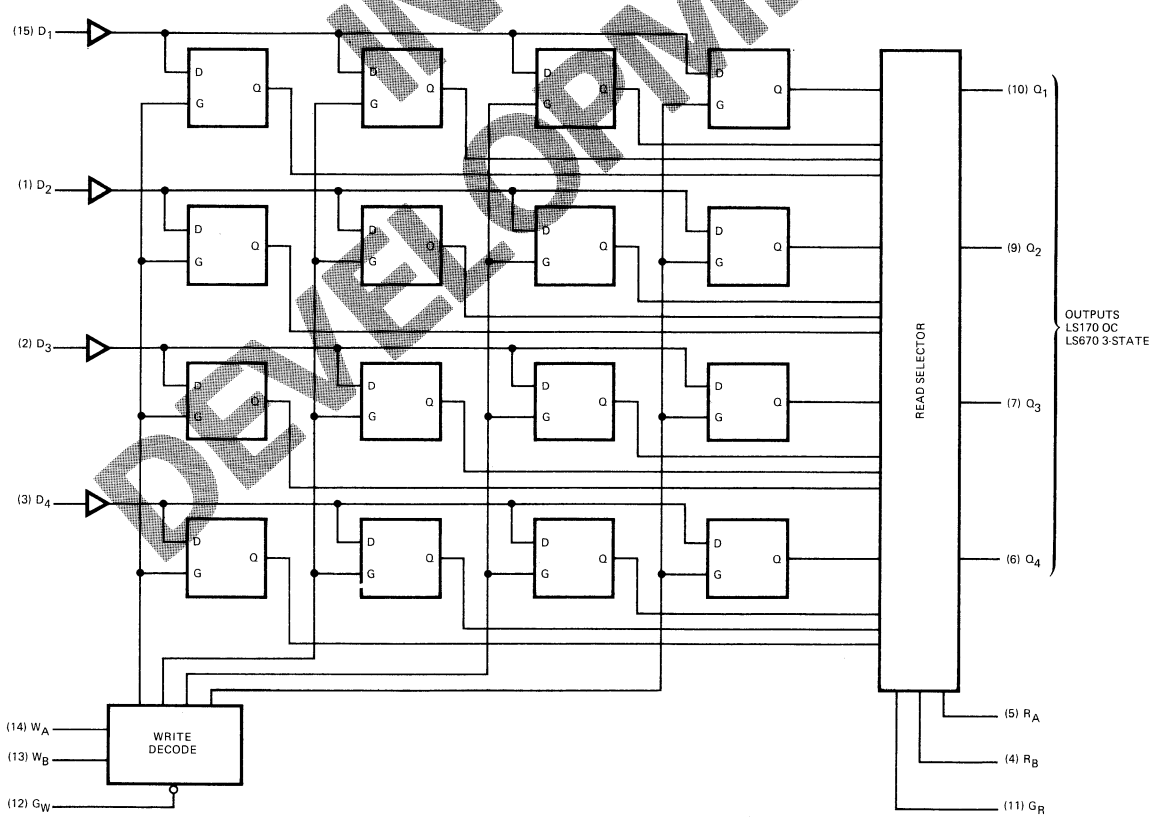
### FUNCTIONAL DESCRIPTION

The Am25LS170 and 670 are 16-bit low-power Schottky register files. The file is organized as 4 words of 4-bits each with separate on-chip address decoding for read and write. This permits simultaneous read and write operations either to the same or different addresses.

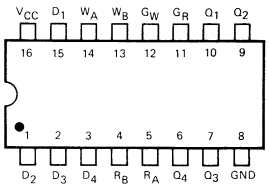
Four data inputs are used to supply the 4-bit data word to be stored. The $W_A$ and $W_B$ inputs supply the write address while the $G_W$ supplies the write enable. Four data outputs ($O_0$ to $O_3$) are selected from data word cells by the $R_A$ and $R_B$ address. The output is available if the read enable $G_R$ is LOW. The register file performs a non-destructive readout. The Am25LS170 has open collector output for convenience of collector ORing while the Am25LS670 provides three-state outputs for bus selection.

The Am54LS/74LS170 and 670 are standard performance versions of the Am25LS160 and 670. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

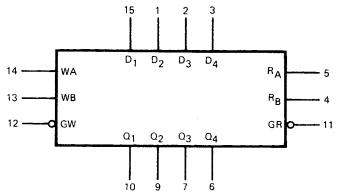


**CONNECTION DIAGRAM**
**Top View**




Note: Pin 1 is marked for orientation.

**LOGIC SYMBOL**




$V_{CC}$ = 16
GND = 8

## Am25LS170 • Am25LS670
## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V, MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V, MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage ('LS670 Only) | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | 2.4 | | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | 0.25 | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Any D, R, or W | | | −0.36 | mA |
| | | | GR (LS170) or GW | | | −0.72 | |
| | | | GR (LS670) | | | −1.08 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Any D, R, or W | | | 20 | µA |
| | | | GR (LS170) or GW | | | 40 | |
| | | | GR (LS670) | | | 60 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | Any D, R, or W | | | 0.1 | mA |
| | | | GR (LS170) or GW | | | 0.2 | |
| | | | GR (LS670) | | | 0.3 | |
| $I_{OH}$ | Output Leakge ('LS170 Only) | $V_{CC}$ = MIN., $V_{OH} = 5.5V$, $V_{IN} = V_{IH}$ or $V_{IL}$ | | | | 20 | µA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current ('LS670 Only) | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | −20 | µA |
| | | | $V_O = 2.7V$ | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | 170 | | 25 | 40 | mA |
| | | | 670 | | 30 | 50 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with 4.5V applied to all data inputs and both enable inputs, all address inputs grounded and all outputs open.

## Am25LS • Am54LS/74LS
## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS170 • Am54LS/74LS670

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V, MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V, MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage ('LS670 Only) | $V_{CC}$ = MIN. $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | 74LS Only, $I_{OL} = 8.0mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | | 0.7 | Volts |
| | | | COM'L | | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Any D, R, or W | | | | −0.4 | mA |
| | | | GR (LS170) or GW | | | | −0.8 | |
| | | | GR (LS670) | | | | −1.2 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Any D, R, or W | | | | 20 | µA |
| | | | GR (LS170) or GW | | | | 40 | |
| | | | GR (LS670) | | | | 60 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | Any D, R, or W | | | | 0.1 | mA |
| | | | GR (LS170) or GW | | | | 0.2 | |
| | | | GR (LS670) | | | | 0.3 | |
| $I_{OH}$ | Output Leakge ('LS170 Only) | $V_{CC}$ = MIN., $V_{OH} = 5.5V$, $V_{IN} = V_{IH}$ or $V_{IL}$ | | | | | 20 | µA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current ('LS670 Only) | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | µA |
| | | | $V_O = 2.7V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | 170 | | 25 | 40 | mA |
| | | | | 670 | | 30 | 50 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with 4.5V applied to all data inputs and both enable inputs, all address inputs grounded and all outputs open.

### DEFINITION OF FUNCTIONAL TERMS

$D_1 - D_4$ Data Input. Input data bit 1 through bit 4 representing one word to be entered into the device.

$R_A$ $R_B$ Read Word Select. Selects word 0 through word 3 to be read out.

$G_R$ **Read Enable. Gates output of LS170 and enables three-state output on LS670.;**

$W_A$ $W_B$ Write Word Select. Selects which word is to be written.

$G_W$ Write Enable. The selected word will be written when the $G_W$ goes LOW.

$Q_1 - Q_4$ Output data bits 1 through 4 available during read select ($G_R$) otherwise HIGH for LS170 (open collector) or high impedance for LS670 (three-state).

### TRUTH TABLE

| WRITE INPUTS | | | WORD | | | |
|---|---|---|---|---|---|---|
| $W_B$ | $W_A$ | $G_W$ | 0 | 1 | 2 | 3 |
| L | L | L | Q=D | NC | NC | NC |
| L | H | L | NC | Q=D | NC | NC |
| H | L | L | NC | NC | Q=D | NC |
| H | H | L | NC | NC | NC | Q=D |
| X | X | H | NC | NC | NC | NC |

| READ INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $R_B$ | $R_A$ | $G_R$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
| L | L | L | $W_0B_0$ | $W_0B_1$ | $W_0B_2$ | $W_0B_3$ |
| L | H | L | $W_1B_0$ | $W_1B_1$ | $W_1B_2$ | $W_1B_3$ |
| H | L | L | $W_2B_0$ | $W_2B_1$ | $W_2B_2$ | $W_2B_3$ |
| H | H | L | $W_3B_0$ | $W_3B_1$ | $W_2B_2$ | $W_3B_3$ |
| LS170 Only: X | X | H | H | H | H | H |
| LS670 Only: X | X | H | Z | Z | Z | Z |

Notes:
1. H = HIGH level, L = LOW level, X = Don't Care, Z = HIGH impedance.
2. (Q=D) the selected F/F will assume the state of $D_{in}$.
3. NC = the level of Q previously established (no change).
4. $W_iB_j$ = i = the word read, j = the bit read.

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Read Select $R_A$, $R_B$ to $Q_i$ | | | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | Write Enable $G_W$ to $Q_i$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | Data $D_i$ to $Q_i$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | Read Enable $G_R$ to $Q_i$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_s$ | $D_i$ to $G_W$ | | | | | | | ns | |
| $t_s$ | $W_A$, $W_B$ to $G_W$ | | | | | | | ns | |
| $t_H$ | $D_i$ to $G_W$ | | | | | | | ns | |
| $t_H$ | $W_A$, $W_B$ to $G_W$ | | | | | | | ns | |
| $t_{pw}$ | $G_W$ or $G_R$ | | | | | | | ns | |
| $T_{LATCH}$ | Latch Time for New Data | | | | | | | ns | |

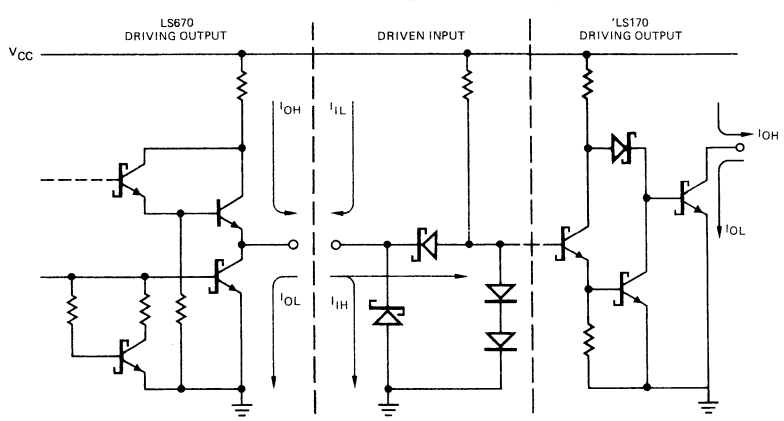
## Am25LS170 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $R_A$, $R_B$, to $Q_i$ | | | | | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $G_W$ to $Q_i$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $D_i$ to $Q_i$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $G_R$ to $Q_i$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_s$ | $D_i$ to $G_W$ | | | | | ns | |
| $t_s$ | $W_A$, $W_B$ to $G_W$ | | | | | ns | |
| $t_H$ | $D_i$ to $G_W$ | | | | | ns | |
| $t_H$ | $W_A$, $W_B$ to $G_W$ | | | | | ns | |
| $t_{pw}$ | $G_W$ or $G_R$ | | | | | ns | |
| $T_{LATCH}$ | Latch Time for New Data | | | | | ns | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## Am25LS670 • Am54LS/74LS670 SWTCHING CHARACTERISTICS

($T_A$ = 25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Read Select $R_A$, $R_B$ to $Q_i$ | | | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | Write Enable $G_W$ to $Q_i$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | Data $D_i$ to $Q_i$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{ZH}$ | Read Enable $G_R$ to $Q_i$ | | | | | | | ns | |
| $t_{ZL}$ | | | | | | | | | |
| $t_{HZ}$ | | | | | | | | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | | | | | | |
| $t_s$ | $D_i$ to $G_W$ | | | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_s$ | $W_A$, $W_B$ to $G_W$ | | | | | | | ns | |
| $t_H$ | $D_i$ to $G_W$ | | | | | | | ns | |
| $t_H$ | $W_A$, $W_B$ to $G_W$ | | | | | | | ns | |
| $t_{pw}$ | $G_W$ or $G_R$ | | | | | | | ns | |
| $T_{LATCH}$ | Latch Time for New Data | | | | | | | ns | |

## Am25LS670 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

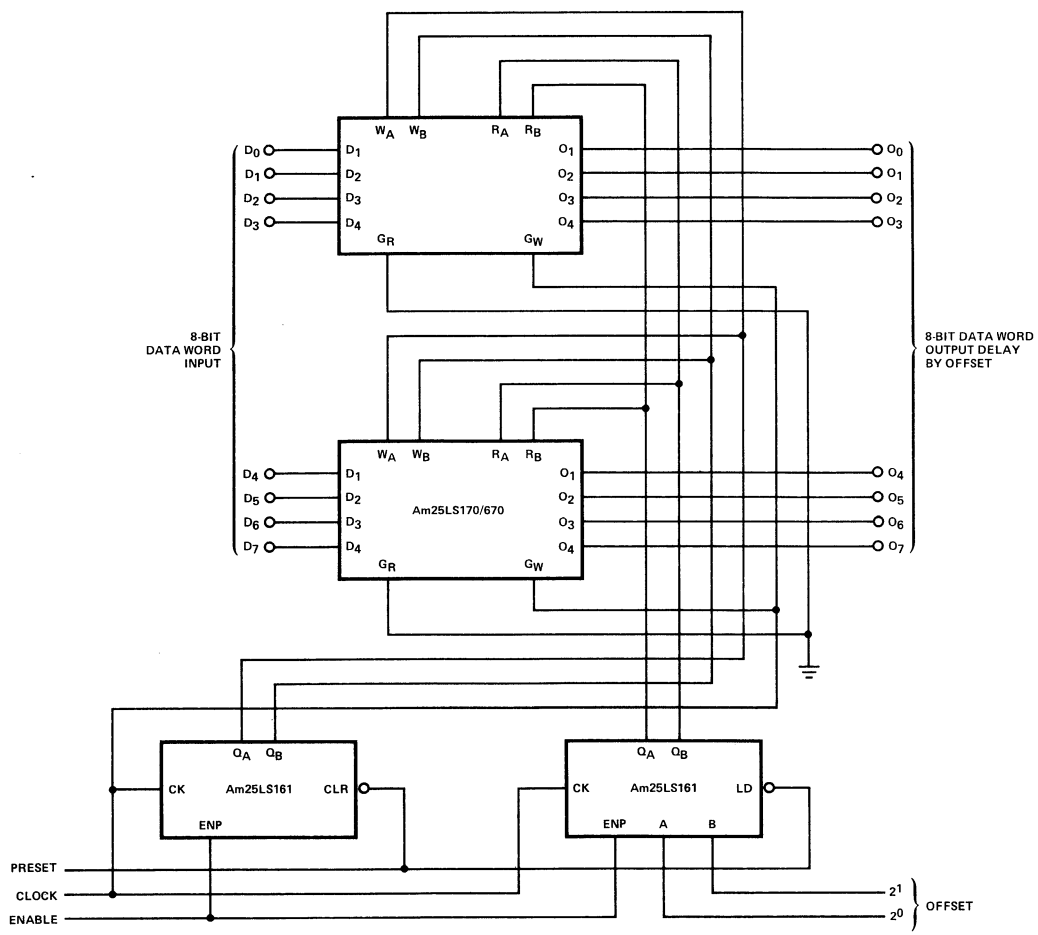
| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Read Select $R_A$, $R_B$, to $Q_i$ | | | | | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | Write Enable $G_W$ to $Q_i$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | Data $D_i$ to $Q_i$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{ZH}$ | Read Enable $G_R$ to $Q_i$ | | | | | ns | |
| $t_{ZL}$ | | | | | | | |
| $t_{HZ}$ | | | | | | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | | | | |
| $t_s$ | $D_i$ to $G_W$ | | | | | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_s$ | $W_A$, $W_B$ to $G_W$ | | | | | ns | |
| $t_H$ | $D_i$ to $G_W$ | | | | | ns | |
| $t_H$ | $W_A$, $W_B$ to $G_W$ | | | | | ns | |
| $t_{pw}$ | $G_W$ or $G_R$ | | | | | ns | |
| $T_{LATCH}$ | Latch Time for New Data | | | | | ns | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS170 Order Number | Am25LS670 Order Number | Am54LS/ 74LS170 Order Number | Am54LS/ 74LS670 Order Number |
|---|---|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS170PC | AM25LS670PC | SN74LS170N | SN74LS670N |
| Hermetic DIP | 0°C to +70°C | AM25LS170DC | AM25LS670DC | SN74LS170J | SN74LS670J |
| Dice | 0°C to +70°C | AM25LS170XC | AM25LS670XC | SN74LS170X | SN74LS670X |
| Hermetic DIP | −55°C to +125°C | AM25LS170DM | AM25LS670DM | SN54LS170J | SN54LS670J |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS170FM | AM25LS670FM | SN54LS170W | SN54LS670W |
| Dice | −55°C to +125°C | AM25LS170XM | AM25LS670XM | SN54LS170X | SN54LS670X |

## APPLICATION




Delay variable by clock times offset 0, 1, 2, 3. System is expandable in width and length and is the basis of a digital auto correlator.

**Variable Digital Delay Buffer (Auto Correlator)**

# Am25LS174 • Am54LS/74LS174
# Am25LS175 • Am54LS/74LS175

## Hex/Quadruple D-Type Flip Flops With Clear

### DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit parallel registers
- Common clock and common clear
- Positive edge-triggered D flip-flops
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440$\mu$A source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS174 is a six-bit register and the Am25LS175 is a four-bit register built using advanced Low Power Schottky technology. The registers consist of D-type flip-flops with a buffered common clock and an asynchronous active LOW buffered clear.

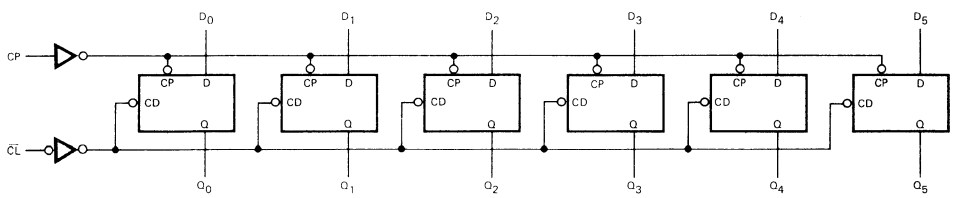
When the clear is LOW, the Q outputs are LOW independent of the other inputs. Information meeting the set-up requirements of the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse.

For versions of these devices having a common enable rather than clear see Am25LS07 and Am25LS08.

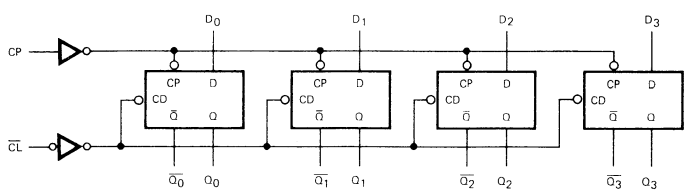
The Am54LS/74LS174 and 175 are standard performance versions of the Am25LS174 and 175. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

'LS174

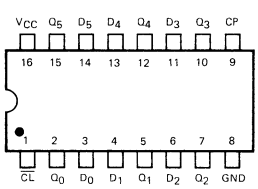



'LS175

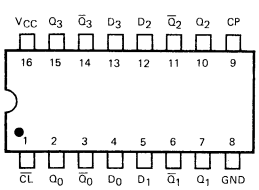



### CONNECTION DIAGRAMS
**Top Views**

'LS174



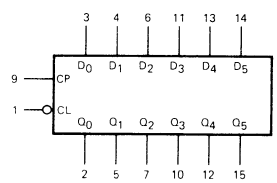

'LS175



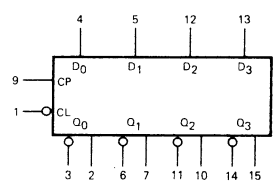

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOLS

'LS174




'LS175




$V_{CC}$ = Pin 16
GND = Pin 8

## ELECTRICAL CHARACTERISTICS The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Clock, $\overline{CL}$ | | | −0.36 | mA |
| | | | Others | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | LS174 | | 16 | 26 | mA |
| | | | LS175 | | 11 | 18 | |

## Am54LS/74LS174/175

## ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | Am74LS | 2.7 | 3.4 | | Volts |
| | | | Am54LS | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | Am54LS | | | 0.7 | Volts |
| | | | Am74LS | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.40 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | LS174 | | 16 | 26 | mA |
| | | | LS175 | | 11 | 18 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open and 4.5V applied to the data and clear inputs. Measured after a momentary ground, then 4.5V applied to the clock input.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 15 | 23 | | 20 | 30 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 13 | 20 | | 23 | 35 | | |
| $t_{PLH}$ | Clear to Q Output, LS175 only | | | 16 | 25 | | 16 | 25 | ns | |
| $t_{PHL}$ | Clear to Output | | | 23 | 35 | | 23 | 35 | | |
| $t_{pw}$ | Pulse Width | Clock | 17 | | | 20 | | | ns | |
| | | Clear | 20 | | | 20 | | | | |
| $t_s$ | Data Set-up Time | | 20 | | | 20 | | | ns | |
| $t_s$ | Set-up Time Clear Recovery (in-active) to Clock | | 20 | | | 25 | | | ns | |
| $t_h$ | Data Hold Time | | 5 | | | 5 | | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 40 | 65 | | 30 | 40 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 34 | | 39 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 30 | | 35 | | |
| $t_{PLH}$ | Clear to Q Output, LS175 only | | | 37 | | 42 | ns | |
| $t_{PHL}$ | Clear to Output | | | 50 | | 57 | ns | |
| $t_{pw}$ | Pulse Width | Clock | 26 | | 30 | | ns | |
| | | Clear | 30 | | 35 | | | |
| $t_s$ | Data Set-up Time | | 30 | | 35 | | ns | |
| $t_s$ | Set-up Time Clear Recovery (In-active) to Clock | | 30 | | 35 | | ns | |
| $t_h$ | Data Hold Time | | 11 | | 12 | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 30 | | 26 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

$D_i$ The D flip-flop data inputs.

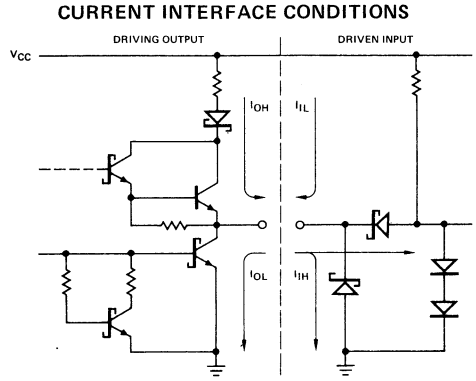
$\overline{CL}$ Clear. When the clear is LOW, the $Q_i$ outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.

CP Clock pulse for the register. Enters data on the positive transition.

$Q_i$ The TRUE register outputs.

$\overline{Q}_i$ The complement register outputs.

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

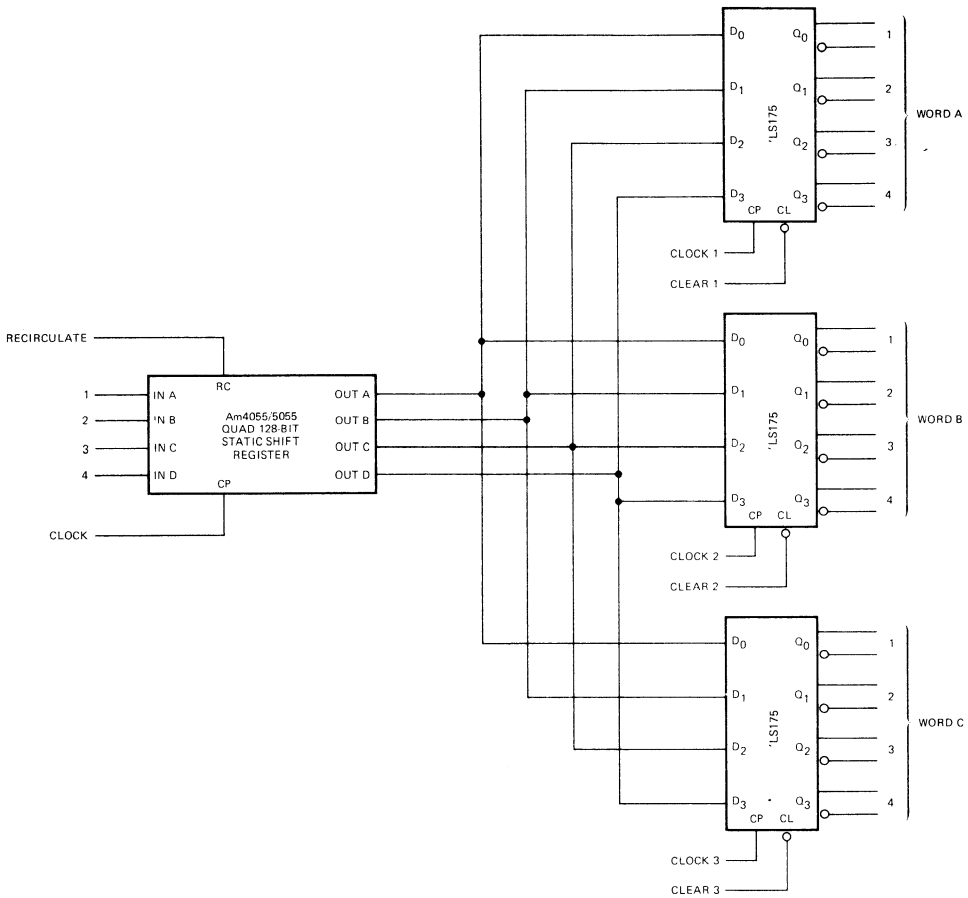
### FUNCTION TABLE

| INPUTS Clear | Clock | $D_i$ | OUTPUTS $Q_i$ | $\overline{Q}_i$ |
|---|---|---|---|---|
| L | X | X | L | H |
| H | L | X | NC | NC |
| H | H | X | NC | NC |
| H | ↑ | L | L | H |
| H | ↑ | H | H | L |

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH Transition

Note: $\overline{Q}_i$ on Am25LS175 only.
$\overline{Q}_i$ on Am54LS/74LS175 only.

## APPLICATION

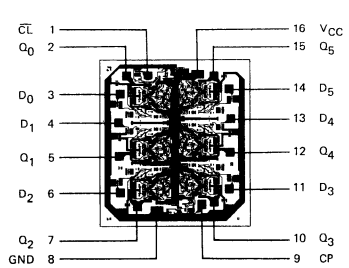



Low-Power Schottky registers interface directly with many MOS shift registers.

3

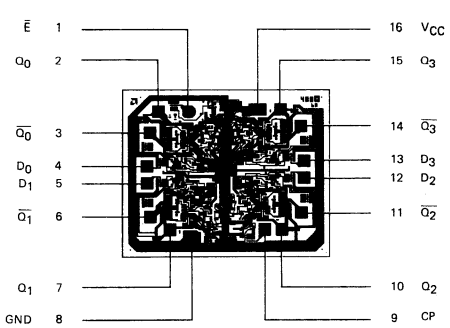
### Metallization and Pad Layouts

**'LS174**




DIE SIZE 0.075" X 0.084"

**'LS175**




DIE SIZE 0.075" X 0.061"

# Am25LS181 • Am54LS/74LS181

## Four-Bit Arithmetic Logic Unit/Function Generator

### DISTINCTIVE CHARACTERISTICS

- Performs 16 arithmetic operations including add, subtract, double and compare
- Full look-ahead capability for high speed arithmetic operation on long words
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS181 is a 4-bit, high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is LOW the 16 arithmetic operations are performed under the control of the four select inputs. When the mode control is HIGH the sixteen logic operations are performed on an individual bit basis between the two 4-bit parallel words under the control of the four select inputs.

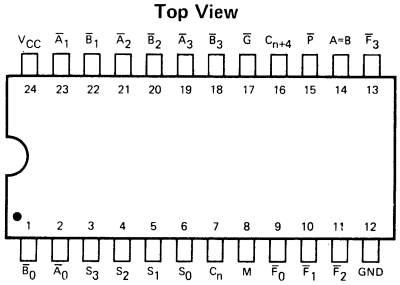
An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by including both carry propagate (P) and carry generate (G) outputs.

An open collector output A = B is used to signal the equivalence of the two parallel words. The open collector feature allows for the equivalence function to be expanded as a wired-AND connection for larger word lengths.

In many systems, the carry output $C_{n+4}$ is connected to the next higher $C_n$ to provide ripple block arithmetic. The ALU can be used with either active HIGH or active LOW inputs and can be ripple expanded or full look-ahead expanded in either mode. The connection pattern is identical for either logic representation.

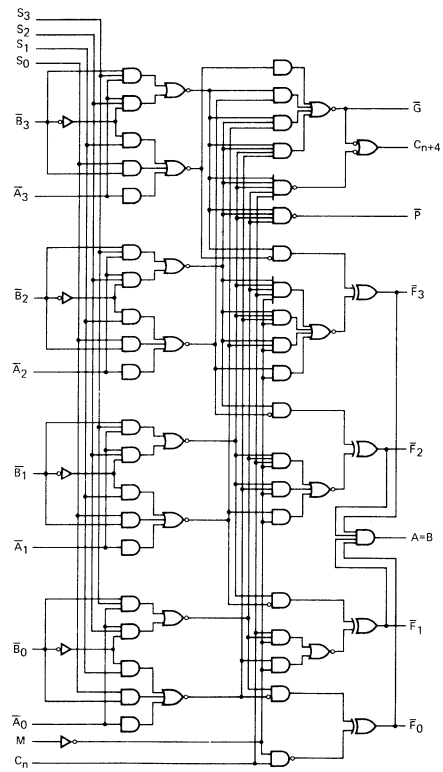
The Am54LS/74LS181 is a standard performance version of the Am25LS181. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### CONNECTION DIAGRAM
**Top View**

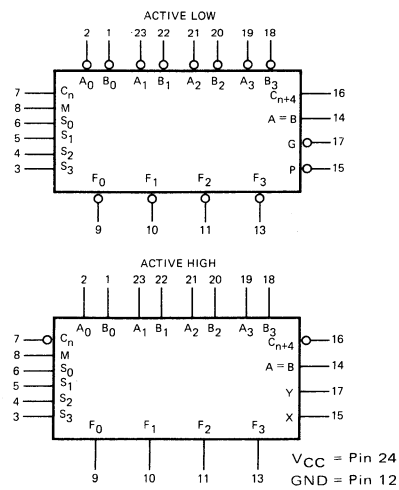



Note: Pin 1 is marked for orientation.

### LOGIC DIAGRAM




### LOGIC SYMBOLS



## Am25LS181
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (Except A = B Output) | $V_{CC}$ = MIN., $I_{OH}$ = −440µA<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | | MIL | 2.5 | 3.4 | | Volts |
| | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | | 0.45 | |
| | | | $\overline{G}$, $I_{OL}$ = 16mA | | | | 0.55 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | | −1.5 | Volts |
| $I_{OH}$ | Output HIGH Current for A = B Output | $V_{CC}$ = MIN., $V_{OH}$ = 5.5V<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | | | | | 100 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | M | | | −0.36 | mA |
| | | | | $\overline{A_i}$ or $\overline{B_i}$ | | | −1.08 | |
| | | | | $S_i$ | | | −1.44 | |
| | | | | $C_n$ | | | −2.0 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | M | | | 20 | µA |
| | | | | $\overline{A_i}$ or $\overline{B_i}$ | | | 60 | |
| | | | | $S_i$ | | | 80 | |
| | | | | $C_n$ | | | 100 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | M | | | 0.1 | mA |
| | | | | $\overline{A_i}$ or $\overline{B_i}$ | | | 0.3 | |
| | | | | $S_i$ | | | 0.4 | |
| | | | | $C_n$ | | | 0.5 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) (Except A = B Output) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | A | MIL | | 20 | 32 | mA |
| | | | | COM'L | | 20 | 34 | |
| | | | B | MIL | | 21 | 35 | |
| | | | | COM'L | | 21 | 37 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured under two conditions — typ. and max. apply to both.
   A. $S_i$, M, $A_i$ at 4.5V; all other inputs grounded; outputs open.
   B. $S_i$, M at 4.5V; all other inputs grounded; outputs open.

## Am25LS • Am54LS/74LS
## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

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## Am54LS/74LS181

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (Except A = B Output) | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | | 2.5 | 3.4 | | Volts |
| | | | COM'L | | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All outputs, $I_{OL}$ = 4mA | | | 0.25 | 0.4 | Volts |
| | | | Am74LS only<br>All outputs, $I_{OL}$ = 8mA | | | 0.35 | 0.5 | |
| | | | $\overline{G}$, $I_{OL}$ = 16 mA | | | 0.47 | 0.7 | |
| | | | $\overline{P}$, $I_{OL}$ = 8mA | | | 0.35 | 0.6 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | | 0.7 | Volts |
| | | | COM'L | | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{OH}$ | Output HIGH Current for A = B Output | $V_{CC}$ = MIN., $V_{OH}$ = 5.5V, $V_{IN} = V_{IH}$ or $V_{IL}$ | | | | | 100 | μA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | M | | | | −0.36 | mA |
| | | | $\overline{A}_i$ or $\overline{B}_i$ | | | | −1.08 | |
| | | | $S_i$ | | | | −1.44 | |
| | | | $C_n$ | | | | −2.0 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | M | | | | 20 | μA |
| | | | $\overline{A}_i$ or $\overline{B}_i$ | | | | 60 | |
| | | | $S_i$ | | | | 80 | |
| | | | $C_n$ | | | | 100 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | M | | | | 0.1 | mA |
| | | | $\overline{A}_i$ or $\overline{B}_i$ | | | | 0.3 | |
| | | | $S_i$ | | | | 0.4 | |
| | | | $C_n$ | | | | 0.5 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) (Except A = B Output) | $V_{CC}$ = MAX. | | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | A | MIL | | 20 | 32 | mA |
| | | | | COM'L | | 20 | 34 | |
| | | | B | MIL | | 21 | 35 | |
| | | | | COM'L | | 21 | 37 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured under two conditions — typ. and max. apply to both.
   A. $S_i$, M, $A_i$ at 4.5V; all other inputs grounded; outputs open.
   B. $S_i$, M at 4.5V; all other inputs grounded; outputs open.

## Am25LS181 • Am54LS/74LS181
## SWITCHING CHARACTERISTICS

($T_A$ = 25°C, $V_{CC}$ = 5.0V)
($C_L$ = 15pF, $R_L$ = 2.0kΩ)

| Parameter | From (Input) | To (Output) | Am25LS181 Min. | Am25LS181 Typ. | Am25LS181 Max. | Am54LS/74LS181 Min. | Am54LS/74LS181 Typ. | Am54LS/74LS181 Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ | $C_{n+4}$ | | | 25 | | 18 | 27 | ns | |
| $t_{PHL}$ | | | | | 14 | | 13 | 20 | | |
| $t_{PLH}$ | $C_n$ | $\overline{F}_i$ | | | 19 | | 17 | 26 | ns | M = 0V (SUM or DIFF mode) |
| $t_{PHL}$ | | | | | 18 | | 13 | 20 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{G}$ | | | 25 | | 19 | 29 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | | 23 | | 15 | 23 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{G}$ | | | 25 | | 21 | 32 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | | 25 | | 17 | 26 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{P}$ | | | 26 | | 20 | 30 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | | 26 | | 20 | 30 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{P}$ | | | 26 | | 20 | 30 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | | 26 | | 22 | 33 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ (j ≥ i) | | | 28 | | 21 | 32 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | | 19 | | 13 | 20 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ (j ≥ i) | | | 30 | | 21 | 32 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | | 19 | | 15 | 23 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ | | | 31 | | 22 | 33 | ns | M = 4.5V (LOGIC mode) |
| $t_{PHL}$ | | | | | 25 | | 19 | 29 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $C_{n+4}$ | | | 33 | | 25 | 38 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ =0V (SUM mode) |
| $t_{PHL}$ | | | | | 31 | | 25 | 38 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $C_{n+4}$ | | | 35 | | 27 | 41 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | | 35 | | 27 | 41 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | A = B | | | 50 | | 33 | 50 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | | 45 | | 41 | 62 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_{i+1}$ | | | 36 | | | | ns | $S_1 = S_2$ = M = 0V $S_0 = S_3$ = 4.5V (SUM mode) |
| $t_{PHL}$ | | | | | 53 | | | | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_{i+1}$ | | | 36 | | | | ns | $S_0 = S_3$ = M = 0V $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | | 53 | | | | | |

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## OPERATION TABLE

| SELECTION | | | | ACTIVE-HIGH DATA | | | ACTIVE-LOW DATA | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | M = H | M = L; Arithmetic Operations | | M = H | M = L; Arithmetic Operations | |
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Logic Functions | $C_n$ = H (No Carry) | $C_n$ = L (With Carry) | Logic Functions | $C_n$ = L (No Carry) | $C_n$ = H (With Carry) |
| L | L | L | L | F = $\overline{A}$ | F = $\overline{A}$ | F = A Plus 1 | F = $\overline{A}$ | F = A Minus 1 | F = A |
| L | L | L | H | F = $\overline{A+B}$ | F = A + B | F = (A + B) Plus 1 | F = $\overline{AB}$ | F = AB Minus 1 | F = AB |
| L | L | H | L | F = $\overline{A}$B | F = A + $\overline{B}$ | F = (A + $\overline{B}$) Plus 1 | F = $\overline{A}$ + B | F = A$\overline{B}$ Minus 1 | F = A$\overline{B}$ |
| L | L | H | H | F = 0 | F = Minus 1 (2's Compl.) | F = Zero | F = 1 | F = Minus 1 (2's Compl.) | F = Zero |
| L | H | L | L | F = $\overline{AB}$ | F = A Plus A$\overline{B}$ | F = A Plus A$\overline{B}$ Plus 1 | F = $\overline{A+B}$ | F = A Plus (A + $\overline{B}$) | F = A Plus (A + $\overline{B}$) Plus 1 |
| L | H | L | H | F = $\overline{B}$ | F = (A + B) Plus A$\overline{B}$ | F = (A + B) Plus A$\overline{B}$ Plus 1 | F = $\overline{B}$ | F = AB Plus (A + $\overline{B}$) | F = AB Plus (A + $\overline{B}$) Plus 1 |
| L | H | H | L | F = A ⊕ B | F = A Minus B Minus 1 | F = A Minus B | F = $\overline{A \oplus B}$ | F = A Minus B Minus 1 | F = A Minus B |
| L | H | H | H | F = A$\overline{B}$ | F = A$\overline{B}$ Minus 1 | F = A$\overline{B}$ | F = A + $\overline{B}$ | F = A + $\overline{B}$ | F = (A + $\overline{B}$) Plus 1 |
| H | L | L | L | F = $\overline{A}$ + B | F = A Plus AB | F = A Plus AB Plus 1 | F = $\overline{A}$B | F = A Plus (A + B) | F = A Plus (A + B) Plus 1 |
| H | L | L | H | F = $\overline{A \oplus B}$ | F = A Plus B | F = A Plus B Plus 1 | F = A ⊕ B | F = A Plus B | F = A Plus B Plus 1 |
| H | L | H | L | F = B | F = (A + $\overline{B}$) Plus AB | F = (A + $\overline{B}$) Plus AB Plus 1 | F = B | F = A$\overline{B}$ Plus (A + B) | F = A$\overline{B}$ Plus (A + B) Plus 1 |
| H | L | H | H | F = AB | F = AB Minus 1 | F = AB | F = A + B | F = A + B | F = (A + B) Plus 1 |
| H | H | L | L | F = 1 | F = A Plus A* | F = A Plus A Plus 1 | F = 0 | F = A Plus A* | F = A Plus A Plus 1 |
| H | H | L | H | F = A + $\overline{B}$ | F = (A + B) Plus A | F = (A + B) Plus A Plus 1 | F = A$\overline{B}$ | F = AB Plus A | F = AB Plus A Plus 1 |
| H | H | H | L | F = A + B | F = (A + $\overline{B}$) Plus A | F = (A + $\overline{B}$) Plus A Plus 1 | F = AB | F = A$\overline{B}$ Plus A | F = A$\overline{B}$ Plus A Plus 1 |
| H | H | H | H | F = A | F = A Minus 1 | F = A | F = A | F = A | F = A Plus 1 |

* Each bit is shifted to the next more significant position.

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

($C_L$ = 50pF, $R_L$ = 2.0kΩ)

| Parameters | From (Input) | To (Output) | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ | $C_{n+4}$ | | 37 | | 42 | ns | |
| $t_{PHL}$ | | | | 22 | | 26 | | |
| $t_{PLH}$ | $C_n$ | $\overline{F}_i$ | | 29 | | 33 | ns | M = 0V (SUM or DIFF mode) |
| $t_{PHL}$ | | | | 28 | | 32 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{G}$ | | 37 | | 42 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | 34 | | 39 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{G}$ | | 37 | | 42 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 0V (DIFF mode) |
| $t_{PHL}$ | | | | 37 | | 42 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{P}$ | | 38 | | 44 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | 38 | | 44 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{P}$ | | 38 | | 44 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | 38 | | 44 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ (j ≥ i) | | 41 | | 47 | ns | M = 0V, $S_0 = S_3$ = 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | 29 | | 33 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ (j ≥ i) | | 43 | | 50 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | 29 | | 33 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ | | 44 | | 51 | ns | M = 4.5V (LOGIC mode) |
| $t_{PHL}$ | | | | 37 | | 42 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $C_{n+4}$ | | 47 | | 54 | ns | M = 0V, $S_0 = S_3$ 4.5V, $S_1 = S_2$ = 0V (SUM mode) |
| $t_{PHL}$ | | | | 44 | | 51 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $C_{n+4}$ | | 50 | | 57 | ns | M = 0V, $S_0 = S_3$ 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | 50 | | 57 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | A = B | | 69 | | 80 | ns | M = 0V, $S_0 = S_3$ = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | 62 | | 72 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_{i+1}$ | | 51 | | 59 | ns | $S_1 = S_2$ = M = 0V, $S_0 = S_3$ = 4.5V (SUM mode) |
| $t_{PHL}$ | | | | 69 | | 80 | | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_{i+1}$ | | 51 | | 59 | ns | $S_0 = S_3$ = M = 0V, $S_1 = S_2$ = 4.5V (DIFF mode) |
| $t_{PHL}$ | | | | 69 | | 80 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

$\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$ The A data inputs.

$\overline{B}_0, \overline{B}_1, \overline{B}_2, \overline{B}_3$ The B data inputs.

$S_0, S_1, S_2, S_3$ The control inputs used to determine the arithmetic or logic function performed.

$\overline{F}_0, \overline{F}_1, \overline{F}_2, \overline{F}_3$ The data outputs of the ALU.

**M** The mode control inputs used to select either the arithmetic or logic operations.

$C_n$ The carry-in input of the ALU.

$C_{n+4}$ The carry-look-ahead output of the four-bit input field.

$\overline{G}$ The carry-generate output for use in multi-level look-ahead schemes.

$\overline{P}$ The carry-propagate output for use in multi-level look-ahead schemes.

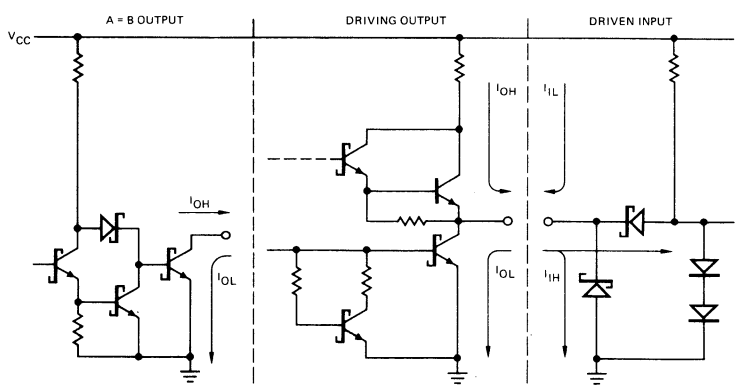
**A = B** The open collector comparator output that can be used to determine equivalence. This output is HIGH whenever the four $\overline{F}$ outputs are HIGH.

## USER NOTES

1. Throughout this data sheet, the active LOW input and output terminology has been used. For the active HIGH definition, the nomenclautre shown under the active HIGH logic symbol should be substituted.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in ($C_n$ = HIGH) for the active LOW case and ($\overline{C}_n$ = LOW) for the active HIGH case.
6. The A = B output only indicates that the four $\overline{F}$ outputs are all HIGH.

3

## LOW POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

| Parameter | Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5V | Apply 0V | Apply 4.5V | Apply 0V | | |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | $\overline{F}_i$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | $\overline{F}_i$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{G}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{G}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | A = B | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | A = B | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $C_{n+4}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | None | None | All $\overline{A}$ and $\overline{B}$ | None | Any $\overline{F}$ or $C_{n+4}$ | In-Phase |

## SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

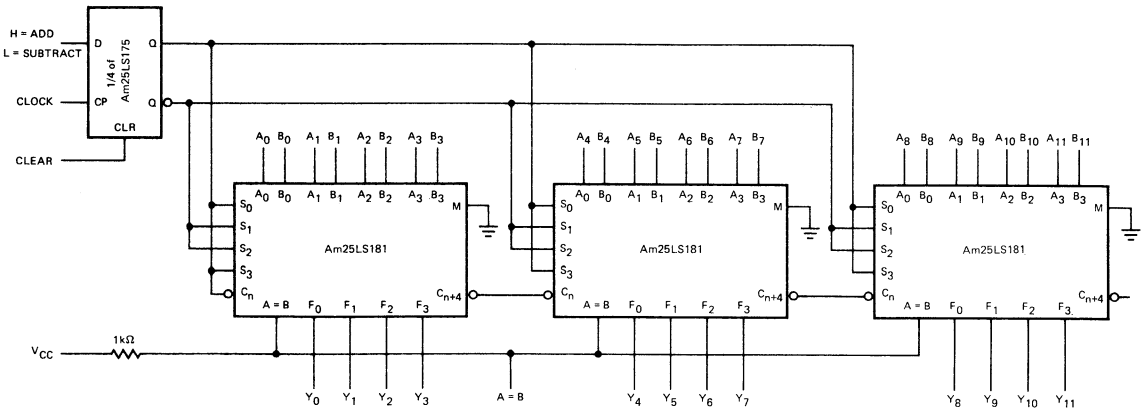
| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5V | Apply 0V | Apply 4.5V | Apply 0V | | |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$ | $C_n$ | $\overline{F}_i$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$ | $C_n$ | $\overline{F}_i$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $\overline{G}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $\overline{G}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | None | None | All $\overline{A}$ | All $\overline{B}$ | Any $\overline{F}$ or $C_{n+4}$ | In-Phase |

## LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5V$, $S_0 = S_3 = 0V$

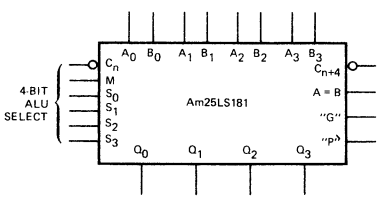
| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5V | Apply 0V | Apply 4.5V | Apply 0V | | |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{F}_i$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{F}_i$ | Out-of-Phase |

## APPLICATIONS




12-BIT ADDER/SUBTRACTOR (2's COMPLEMENT)

If one input is defined active–HIGH and the second input is defined active–LOW, the sixteen arithmetic and logic functions of the ALU are reordered as shown in the function table.



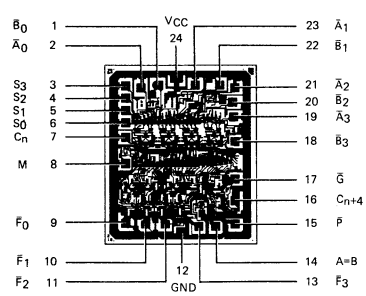

## FUNCTION TABLE

A = Active HIGH  B = Active LOW

| $S_0$ | $S_1$ | $S_2$ | $S_3$ | Arithmetic (M = L, $\overline{C}_n$ = H) | Logic (M = H) |
|---|---|---|---|---|---|
| L | L | L | L | A | $\overline{A}$ |
| H | L | L | L | $A + \overline{B}$ | $\overline{AB}$ |
| L | H | L | L | $A + B$ | $\overline{A}B$ |
| H | H | L | L | minus 1 (2's comp.) | Logic '0' |
| L | L | H | L | A plus AB | AB |
| H | L | H | L | AB plus $[A + \overline{B}]$ | B |
| L | H | H | L | A plus B | $\overline{A \oplus B}$ |
| H | H | H | L | AB minus 1 | AB |
| L | L | L | H | A plus $A\overline{B}$ | $\overline{A} + \overline{B}$ |
| H | L | L | H | A minus B minus 1 | $A \oplus B$ |
| L | H | L | H | $A\overline{B}$ plus $[A + B]$ | $\overline{B}$ |
| H | H | L | H | $A\overline{B}$ minus 1 | $A\overline{B}$ |
| L | L | H | H | A plus A (2 x A) | Logic '1' |
| H | L | H | H | A plus $[A + \overline{B}]$ | $A + B$ |
| L | H | H | H | A plus $[A + B]$ | $A + \overline{B}$ |
| H | H | H | H | A minus 1 | A |

L = Low Voltage Level
H = High Voltage Level

### Metallization and Pad Layout




DIE SIZE: 0.078" X 0.092"

# Am25LS190 • Am54LS/74LS190
# Am25LS191 • Am54LS/74LS191

## Synchronous Counters With Up/Down Mode Control

### DISTINCTIVE CHARACTERISTICS

- Single up/down countline
- Parallel load inputs and parallel count outputs
- Ripple clock output for cascading
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS190 and Am25LS191 are BCD and binary synchronous up/down counters. The counter flip-flops are triggered on the LOW-to-HIGH transition of the clock input if the enable input is LOW. If the enable input is HIGH, counting is inhibited.

The direction of the count sequence is controlled by the up/down input. When the up/down input is LOW, the counter will count up. When the up/down input is HIGH, the counter will count down.

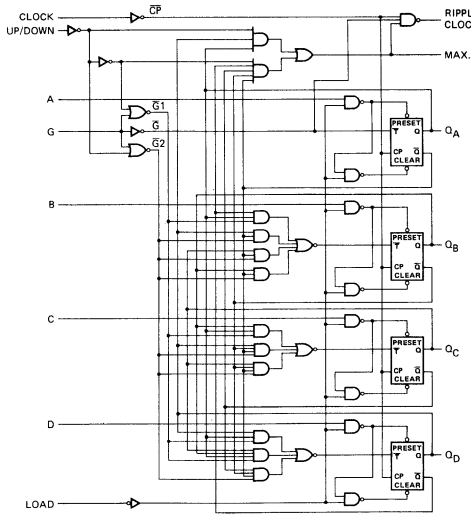
The load input is used to asynchronously jam new data into the counter via the parallel data inputs. When the load input is LOW, the counter flip-flop outputs will follow the parallel data inputs regardless of the clock input.

The max./min. count output is HIGH for a complete clock cycle when the counter overflows (binary 9 or binary 15) or underflows (binary 0). The ripple clock output is LOW for the LOW part of the clock cycle when the overflow or underflow condition exists. The counters are cascaded by connecting the ripple clock output to the enable input of the succeeding counter when parallel counting, or connecting the ripple clock output to the clock input when the parallel enable connection is used. The min./max. count output is used in high-speed look-ahead connection schemes.

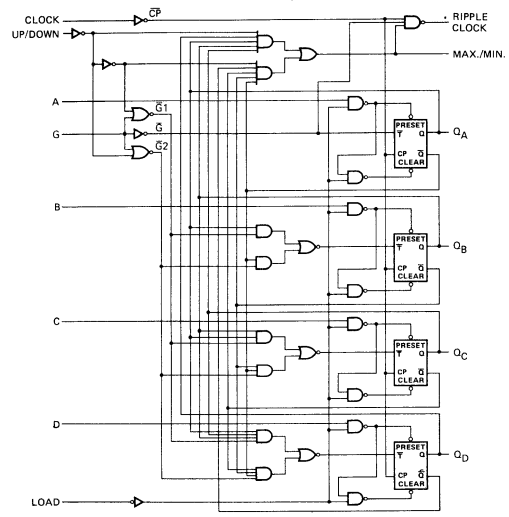
The Am54LS/74LS190 and 191 are standard performance versions of the Am25LS190 and 191. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

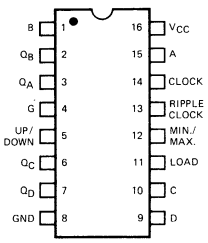
**Am25LS190 Decade Counter**




**Am25LS191 Binary Counter**

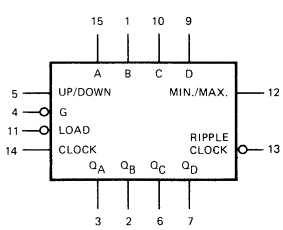



### CONNECTION DIAGRAM — Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## ELECTRICAL CHARACTERISTICS Am25LS190 • Am25LS191

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | 0.2 | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Enable G | | | −1.08 | mA |
| | | | Others | | | −0.36 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Enable G | | | 60 | μA |
| | | | Others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | Enable G | | | 0.3 | mA |
| | | | Others | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 20 | 35 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded and all outputs open.

3

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to + 7.0V |
| DC Output Current, Into to Outputs | 30mA |
| DC Input Current | −30mA to 5.0mA |

## ELECTRICAL CHARACTERISTICS Am54LS/74LS190 • Am54LS/74LS191

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All $I_{OL}$ = 4.0mA | | 0.25 | 0.4 | Volts |
| | | | Am74LS, $I_{OL}$ = 8.0mA | | 0.35 | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Enable G | | | −1.08 | mA |
| | | | Others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Enable G | | | 60 | μA |
| | | | Others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | Enable G | | | 0.3 | mA |
| | | | Others | | | 0.1 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 20 | 35 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded and all outputs open.

## SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Load to Q | | 22 | 33 | | 22 | 33 | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | 26 | 39 | | 33 | 50 | | |
| $t_{PLH}$ | A, B, C, D to $Q_A$, $Q_B$, QC, $Q_D$ Respectively | | 14 | 22 | | 20 | 32 | ns | |
| $t_{PHL}$ | | | 24 | 39 | | 27 | 40 | | |
| $t_{PLH}$ | Clock to Ripple Clock | | 11 | 18 | | 13 | 20 | ns | |
| $t_{PHL}$ | | | 15 | 21 | | 16 | 24 | | |
| $t_{PLH}$ | Clock to Q | | 14 | 21 | | 16 | 24 | ns | |
| $t_{PHL}$ | | | 21 | 30 | | 24 | 36 | | |
| $t_{PLH}$ | Clock to Min./Max. | | 26 | 39 | | 28 | 42 | ns | |
| $t_{PHL}$ | | | 27 | 39 | | 37 | 52 | | |
| $t_{PLH}$ | Up/Down to Ripple Clock | | 30 | 45 | | 30 | 45 | ns | |
| $t_{PHL}$ | | | 30 | 45 | | 30 | 45 | | |
| $t_{PLH}$ | Up/Down to Min./Max. | | 21 | 33 | | 21 | 33 | ns | |
| $t_{PHL}$ | | | 22 | 33 | | 22 | 33 | | |
| $t_{PLH}$ | Enable to Ripple Clock | | 12 | 19 | | 21 | 33 | ns | |
| $t_{PHL}$ | | | 17 | 27 | | 21 | 33 | | |
| $f_{max}$ | Max. Clock Frequency (Note 1) | 25 | 30 | | 20 | 25 | | MHz | |
| $t_{pw}$ | Clock Pulse Width | 25 | | | 25 | | | ns | |
| $t_{pw}$ | Load Pulse Width | 25 | | | 35 | | | ns | |
| $t_s$ | Data Set-up Time | 12 | | | 20 | | | ns | |
| $t_s$ | Count Enable | 30 | | | 40 | | | ns | |
| $t_h$ | Data Hold Time | 0 | | | 0 | | | ns | |
| $t_r$ | MR – CP | 20 | | | | | | ns | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Load to Q | | 47 | | 54 | ns | $R_L$ = 2.0kΩ, $C_L$ = 50pF |
| $t_{PHL}$ | | | 55 | | 63 | | |
| $t_{PLH}$ | A, B, C, D to $Q_A$, $Q_B$ | | 33 | | 38 | ns | |
| $t_{PHL}$ | $Q_C$, $Q_D$ Respectively | | 55 | | 63 | | |
| $t_{PLH}$ | Clock to Ripple Clock | | 28 | | 32 | ns | |
| $t_{PHL}$ | | | 31 | | 36 | | |
| $t_{PLH}$ | Clock to Q | | 31 | | 36 | ns | |
| $t_{PHL}$ | | | 43 | | 50 | | |
| $t_{PLH}$ | Clock to Min./Max. | | 55 | | 63 | ns | |
| $t_{PHL}$ | | | 55 | | 63 | | |
| $t_{PLH}$ | Up/Down to Ripple Clock | | 63 | | 72 | ns | |
| $t_{PHL}$ | | | 63 | | 72 | | |
| $t_{PLH}$ | Up/Down to Min./Max. | | 47 | | 54 | ns | |
| $t_{PHL}$ | | | 47 | | 54 | | |
| $t_{PLH}$ | Enable to Ripple Clock | | 29 | | 33 | ns | |
| $t_{PHL}$ | | | 39 | | 45 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 19 | | 16 | | ns | |
| $t_{pw}$ | Clock Pulse Width | 37 | | 42 | | ns | |
| $t_{pw}$ | Load Pulse Width | 37 | | 42 | | ns | |
| $t_s$ | Data Set-up Time | 20 | | 23 | | ns | |
| $t_s$ | Count Enable | 39 | | 45 | | ns | |
| $t_h$ | Data Hold Time | 4 | | 5 | | ns | |
| $t_r$ | MR − CP | 30 | | 35 | | ns | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

## DEFINITION OF FUNCTIONAL TERMS

**A, B, C, D** The four parallel data inputs to the counter flip-flops.

**$Q_A$, $Q_B$, $Q_C$, $Q_D$** The four outputs of the counter.

**Clock** The clock input causes the counter to change state in the count mode. The counter flip-flops trigger on the LOW-to-HIGH transition of the clock.

**Enable** The enable input can be used to enable or inhibit counting. When the enable input is HIGH, counting is inhibited.

**Up/Down** The up/down input controls the direction of the count sequence. When the up/down input is LOW, the counter will count up (positive logic definitions).

**Load** The load input is used to parallel enter new data via the A, B, C and D inputs. When the load input is LOW, the counter will follow the parallel inputs regardless of the clock input.

**Min./Max.** The min./max. output is HIGH when the counter is in either the overflow or underflow state.

**Ripple Clock** The ripple clock output is LOW when the counter is in either the overflow or underflow state and the clock is LOW.

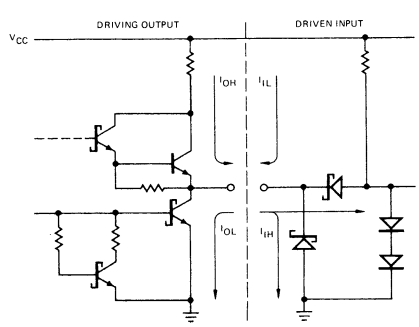
## FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clock | Up/Dn | Enable G | A | B | C | D | Load | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Min./ Max. | Ripple Clock | |
| X | X | H | X | X | X | X | H | NC | NC | NC | NC | NC | NC | Inhibit |
| X | X | X | L | L | L | L | L | L | L | L | L | H | CK | Underflow |
| X | X | X | H | H | H | H | L | H | H | H | H | H | CK | 191 Overflow |
| X | X | X | H | L | L | H | L | H | L | L | H | H | CK | 190 Overflow |
| X | X | X | L | H | L | H | L | L | H | L | H | L | H | Examples of no Overflow |
| X | X | X | H | L | H | L | L | H | L | H | L | L | H | or Underflow |
| ↑ | L | L | X | X | X | X | H | Count Up | | | | A/R | A/R & CK | Count Up |
| ↑ | H | L | X | X | X | X | H | Count Down | | | | A/R | A/R & CK | Count Down |

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH Transition

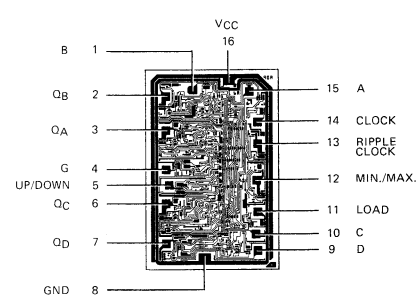
NC = No Change
CK = LOW if Clock is LOW, HIGH if Clock is HIGH
A/R = Assumes State Required by Counter Output

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



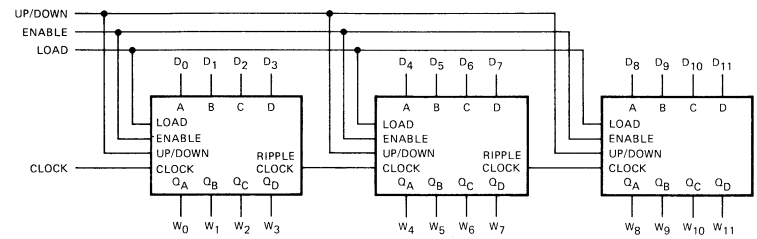

Note: Actual current flow direction shown.

### Metallization and Pad Layout

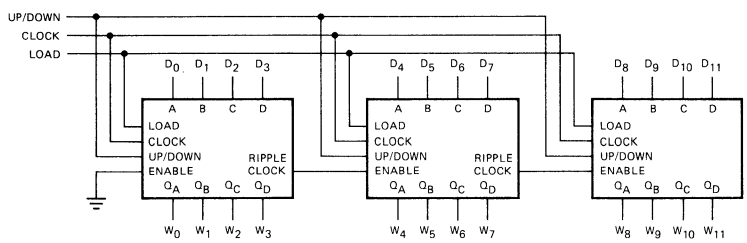



DIE SIZE 0.069" X 0.105"

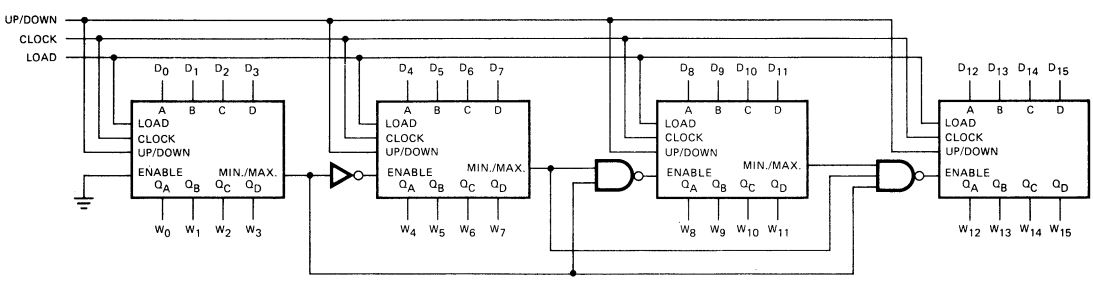
## APPLICATIONS




**PARALLEL ENABLE WITH RIPPLE CLOCK**




**SYNCHRONOUS PARALLEL COUNTING WITH RIPPLE ENABLE**




**SYNCHRONOUS COUNTING WITH FULL LOOK-AHEAD**

# Am25LS192 • Am25LS193
# Am54LS/74LS192 • Am54LS/74LS193

## Decimal and Hexadecimal Up/Down Counters

### DISTINCTIVE CHARACTERISTICS

- Separate up and down clocks
- Asynchronous parallel load
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440$\mu$A source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

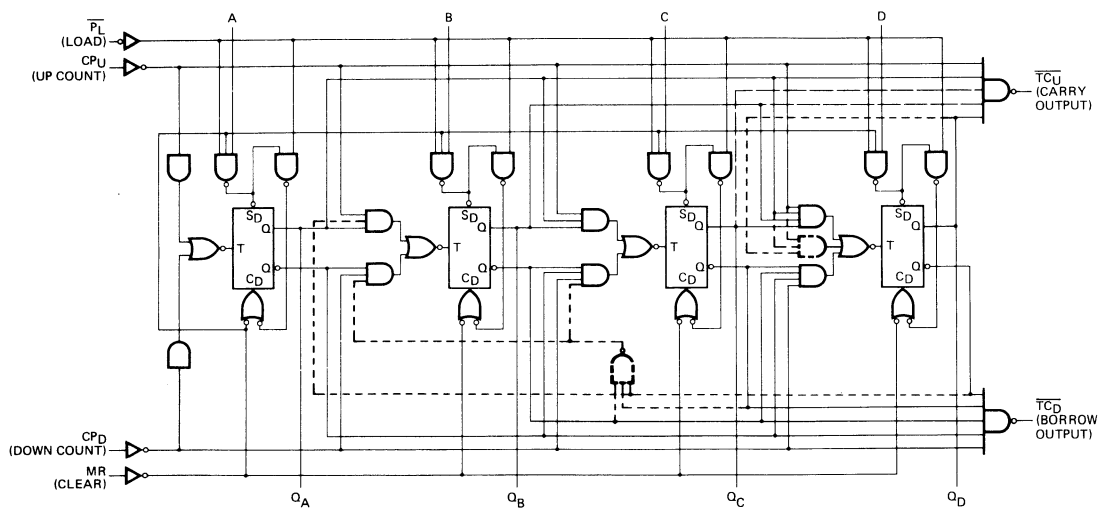
### FUNCTIONAL DESCRIPTION

The 'LS192 and 'LS193 are four-bit up/down counters using advanced Low-Power Schottky processing. The 'LS192 counts in the BCD mode and the 'LS193 counts in the binary mode. These counters have separate count-up and count-down clock inputs ($CP_U$ and $CP_D$, respectively). The $Q_i$ outputs change state synchronously on the LOW-to-HIGH transition on either the up clock input or the down clock input. Only one clock input can be LOW at a time or erroneous counting will result.

Each of the four flip-flops can be preset to a logic HIGH or a logic LOW by means of four parallel inputs (A, B, C, and D). When the parallel load input ($\overline{PL}$) goes LOW, all four flip-flops set to the state of the direct inputs (A, B, C, and D) independent of the clock inputs. An active HIGH master reset (MR) is provided which overrides both the clock and parallel load inputs forcing all $Q_i$ outputs LOW.

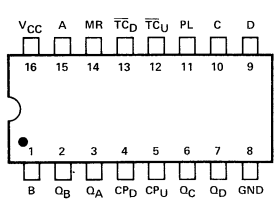
Two terminal count outputs are gated with the clock inputs to provide clock signal to other counters. The $TC_D$ output goes LOW when the counter is in state 0000 and the count down clock goes LOW. The $TC_U$ goes LOW when the count up goes LOW and the counter is in state 1001 ('LS192) or state 1111 ('LS193). The $TC_U$ and $TC_D$ outputs can drive the count up and count down clocks on the next counter in a series. The $Q_i$ outputs of such a connection scheme are not synchronous on cascaded counters in this series.

### LOGIC DIAGRAM



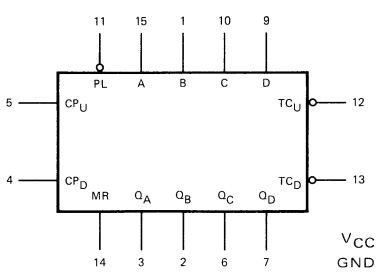

'LS192 Decade Counter only – – – – – – –  'LS193 Hexadecimal Counter only —— —— ——

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



## Am25LS192 • Am25LS193

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | | |
|---|---|---|---|---|---|
| Am25LS192XC/Am25LS193XC | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am25LS192XM/Am25LS193XM | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ (MIL) | MIN. = 4.50V | MAX. = 5.50V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | 0.25 | 0.40 | Volts |
| | | | $I_{OL} = 8.0mA$ | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 19 | 34 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. ICC is measured with all outputs open; clear and load inputs grounded; and all other inputs at 4.5V

3

## Am25LS • Am54LS/74LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS192 • Am54LS/74LS193

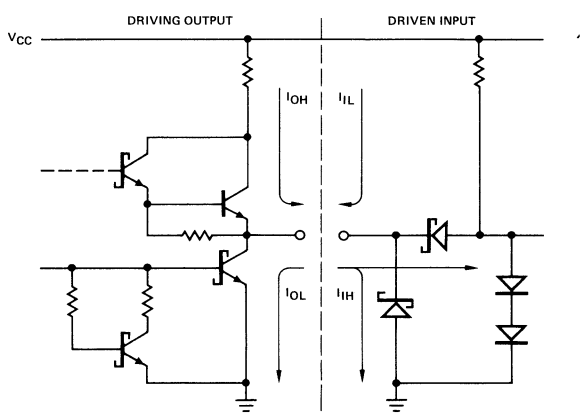
## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | | |
|---|---|---|---|---|---|
| Am74LS192X/74LS193X | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ± 5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am54LS192X/54LS193X | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ± 10% (MIL) | MIN. = 4.50V | MAX. = 5.50V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −400μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0mA | | 0.25 | 0.40 | Volts |
| | | | 74LS only, $I_{OL}$ = 8.0mA | | 0.35 | 0.50 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 19 | 34 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limites are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open; clear and load inputs grounded; and all other inputs at 4.5V

### Am25LS • 54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT
### CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## SWITCHING CHARACTERISTICS

($T_A = 25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $CP_U$ or $CP_D$ to $Q_n$ | | | 24 | 34 | | 25 | 38 | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | | 28 | 39 | | 31 | 47 | | |
| $t_{PLH}$ | $CP_U$ to $TC_U$ | | | 10 | 15 | | 17 | 26 | ns | |
| $t_{PHL}$ | | | | 10 | 15 | | 21 | 33 | | |
| $t_{PLH}$ | $CP_D$ to $TC_D$ | | | 10 | 15 | | 16 | 24 | ns | |
| $t_{PHL}$ | | | | 11 | 17 | | 21 | 33 | | |
| $t_{PLH}$ | A-D to $Q_n$ Output | | | 13 | 18 | | | – | ns | |
| $t_{PHL}$ | | | | 27 | 38 | | | – | | |
| $t_{PLH}$ | A-D to $TC_U$ Output | | | 35 | 49 | | | – | ns | |
| $t_{PHL}$ | | | | 19 | 27 | | | – | | |
| $t_{PLH}$ | A-D to $TC_D$ Output | | | 26 | 36 | | | – | ns | |
| $t_{PHL}$ | | | | 28 | 39 | | | – | | |
| $t_{PHL}$ | MR Input to $Q_n$ Output | | | 20 | 29 | | 22 | 35 | ns | |
| $t_{PLH}$ | MR Input to $TC_U$ Output | | | 25 | 35 | | | – | ns | |
| $t_{PHL}$ | MR Input to $TC_D$ Output | | | 16 | 22 | | | – | ns | |
| $t_{PLH}$ | $P_L$ Input to $Q_n$ Output | | | 20 | 29 | | 27 | 40 | ns | |
| $t_{PHL}$ | | | | 25 | 36 | | 29 | 40 | | |
| $t_{PLH}$ | $P_L$ Input to $TC_U$ Output | | | 31 | 45 | | | – | ns | |
| $t_{PHL}$ | | | | 30 | 42 | | | – | | |
| $t_{PLH}$ | $P_L$ Input to $TC_D$ Output | | | 30 | 42 | | | – | ns | |
| $t_{PHL}$ | | | | 24 | 34 | | | – | | |
| $t_s$ | Data Set-up Time A-D Input to $P_L$ Input | Load 1 | 5.0 | | | – | | | ns | |
| | | Load 0 | 15 | | | 20 | | | ns | |
| $t_s$ | Set-up Time, $P_L$ Input to $CP_U$ or $CP_D$ | | 9.0 | | | – | | | ns | |
| $t_s$ | Set-up Time, Clear Recovery (In-Active) to $CP_U$ or $CP_D$ | | 5.0 | | | – | | | ns | |
| $t_h$ | Data | | 0 | | | 0 | | | ns | |
| $t_{pw(0)}$ | Pulse Width | $CP_U$ | 11 | | | 20 | | | ns | |
| | | $CP_D$ | 11 | | | 20 | | | | |
| | | $P_L$ | 9.0 | | | 20 | | | | |
| $t_{pw(1)}$ | Pulse Width | MR | 15 | | | 20 | | | ns | |
| $f_{max}$ | Maximum Clock Frequency, Count Up or Down (Note 1) | | 35 | 45 | | 25 | 32 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

3

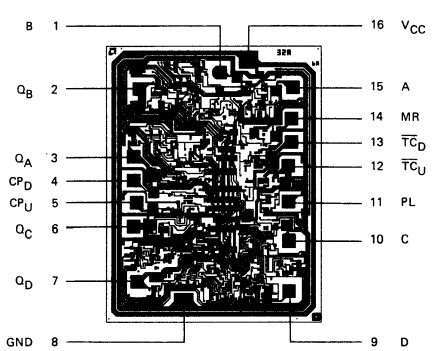
## Am25LS192, Am25LS193 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min. | Am25LS COM'L Max. | Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $CP_U$ or $CP_D$ to $Q_n$ | | | 44 | | 52 | ns | $C_L = 50pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | | 54 | | 67 | | |
| $t_{PLH}$ | $CP_U$ to $TC_U$ | | | 22 | | 26 | ns | |
| $t_{PHL}$ | | | | 23 | | 27 | | |
| $t_{PLH}$ | $CP_D$ to $TC_D$ | | | 22 | | 26 | ns | |
| $t_{PHL}$ | | | | 23 | | 27 | | |
| $t_{PLH}$ | A-D to $Q_n$ Output | | | 26 | | 31 | ns | |
| $t_{PHL}$ | | | | 52 | | 63 | | |
| $t_{PLH}$ | A-D to $TC_U$ Output | | | 66 | | 80 | ns | |
| $t_{PHL}$ | | | | 38 | | 46 | | |
| $t_{PLH}$ | A-D to $TC_D$ Output | | | 50 | | 60 | ns | |
| $t_{PHL}$ | | | | 54 | | 66 | | |
| $t_{PHL}$ | MR Input to $Q_n$ Output | | | 41 | | 50 | ns | |
| $t_{PLH}$ | MR Input to $TC_U$ Output | | | 49 | | 60 | ns | |
| $t_{PHL}$ | MR Input to $TC_D$ Output | | | 32 | | 38 | ns | |
| $t_{PLH}$ | $P_L$ Input to $Q_n$ Output | | | 41 | | 50 | ns | |
| $t_{PHL}$ | | | | 53 | | 67 | | |
| $t_{PLH}$ | $P_L$ Input to $TC_U$ Output | | | 63 | | 79 | ns | |
| $t_{PHL}$ | | | | 60 | | 75 | | |
| $t_{PLH}$ | $P_L$ Input to $TC_D$ Output | | | 60 | | 75 | ns | |
| $t_{PHL}$ | | | | 48 | | 60 | | |
| $t_s$ | Data Set-up Time A-D Input to $P_L$ Input | Load 1 | 5.0 | | 5.0 | | ns | |
| | | Load 0 | 20 | | 23 | | | |
| $t_s$ | Set-up Time, $P_L$ Input to $CP_U$ or $CP_D$ | | 13 | | 18 | | ns | |
| $t_s$ | Set-up Time, Clear Recovery (In-Active) to $CP_U$ or $CP_D$ | | 7.0 | | 9.0 | | ns | |
| $t_h$ | Data | | 0 | | 0 | | ns | |
| $t_{pw(0)}$ | Pulse Width | $CP_U$ | 15 | | 17 | | ns | |
| | | $CP_D$ | 15 | | 17 | | | |
| | | $P_L$ | 13 | | 17 | | | |
| $t_{pw(1)}$ | Pulse Width | MR | 18 | | 21 | | | |
| $f_{max}$ | Maximum Clock Frequency, Count Up or Down (Note 1) | | 25 | | 20 | | MHz | |

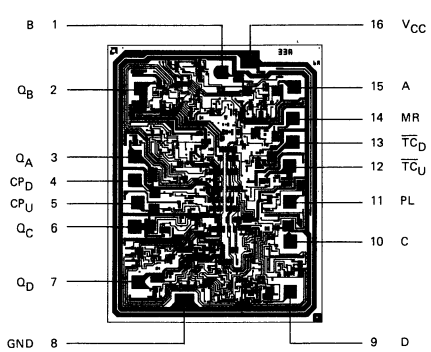
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### Metallization and Pad Layout

'LS192




'LS193




DIE SIZE 0.075" X 0.096"

## FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | | | | | | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clock | | | | Data | | | | | | | | | | |
| Up | Down | Clear | Load | A | B | C | D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | Borrow | Carry | |
| X | L | H | X | X | X | X | X | L | L | L | L | L | H | Clear |
| X | H | H | X | X | X | X | X | L | L | L | L | H | H | |
| X | X | L | L | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | X | X | Load |
| H | ↑ | L | H | X | X | X | X | Count Down | | | | H | H | Except at borrow |
| H | L | L | H | X | X | X | X | L | L | L | L | L | H | Borrow |
| H | H | L | H | X | X | X | X | L | L | L | L | H | H | |
| ↑ | H | L | H | X | X | X | X | Count up | | | | H | H | Except at carry |
| L | H | L | H | X | X | X | X | H | H | H | H | H | L | Carry (193 only) |
| H | H | L | H | X | X | X | X | H | H | H | H | H | H | |
| L | H | L | H | X | X | X | X | H | L | L | H | H | L | Carry (192 only) |
| H | H | L | H | X | X | X | X | H | L | L | H | H | H | |

H = HIGH  X = Don't care  D = A LOW or a HIGH and the respective output will assume the same state.
L = LOW  ↑ = LOW-to-HIGH transition

## DEFINITION OF FUNCTIONAL TERMS

**MR** Clear. The clear input to the counter overrides all other inputs. When the clear input is HIGH, the Q outputs are set LOW independent of the other inputs.

**$\overline{PL}$** Load. The load input performs asynchronous parallel load of the data on the A, B, C, and D inputs. When the load input is LOW, the $Q_i$ outputs will follow the parallel inputs regardless of the clock inputs.

**A, B, C, D** The four parallel inputs to the counter flip-flops.

**$CP_U$** Count up. A clock input causing the counter to change state in an increasing binary number direction. Counting occurs on the LOW-to-HIGH transition of the clock.

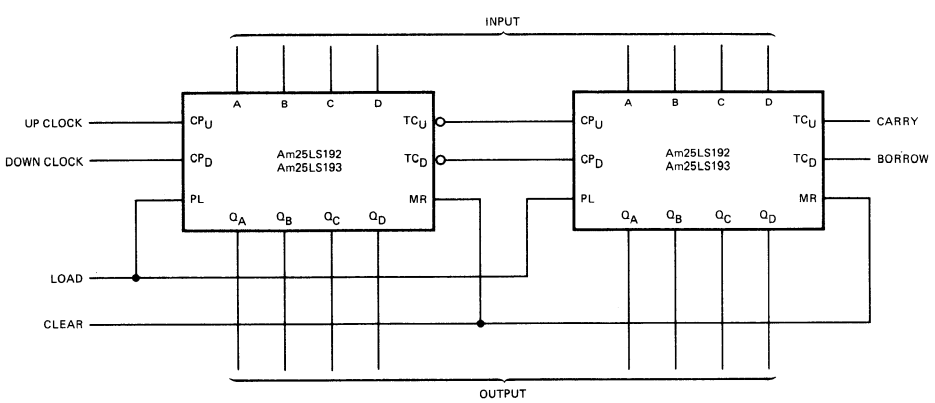
**$CP_D$** Count down. A clock input causing the counter to change state in a decreasing binary number direction. The state change occurs on the LOW-to-HIGH transition.

**$Q_A$, $Q_B$, $Q_C$, $Q_D$** The four outputs of the counter representing the LSB to MSB, respectively.

**$\overline{TC_U}$** Carry output. A clock output that indicates the maximum upper binary number has been reached. For the 'LS192, $TC_U$ indicates that the "9" state has been reached and the up clock is LOW. For the 'LS193, $TC_U$ indicates that the "15" state has been reached and the up clock is LOW.

**$\overline{TC_D}$** Borrow output. A clock output indicating that the "0" state has been reached and the down clock is LOW.

## APPLICATION




8-Bit Up/Down Counter with Parallel Load

# Am25LS194A • Am54LS/74LS194A
# Am25LS195A • Am54LS/74LS195A

## Four-Bit High-Speed Shift Registers

### DISTINCTIVE CHARACTERISTICS

- Shift right or parallel load with JK inputs on Am25LS195A
- Shift left, right, parallel load or do nothing on Am25LS194A
- Fully synchronous shifting and parallel loading
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440$\mu$A source current
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS194A and Am25LS195A are 4-bit registers that exhibit fully synchronous operation in all operating modes. The Am25LS195A can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, $Q_A$, is loaded via the J and $\overline{K}$ inputs in the shift mode.

The Am25LS194A operates in four modes under control of the two select inputs, $S_0$ and $S_1$. The four modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the $Q_A$ bit input from R), shift left (data comes from the flip-flop to the right, with the $Q_D$ input from L), and hold or do nothing (each flip-flop receives data from its own output).

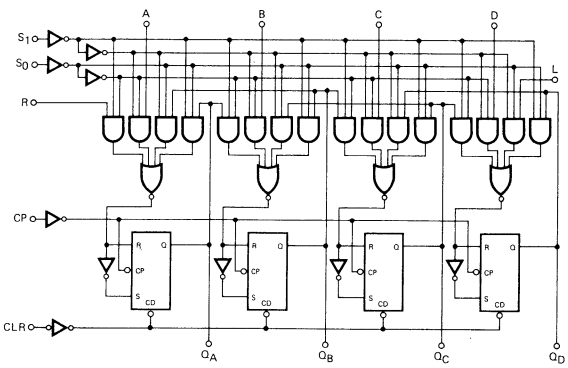
For both devices the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW synchronous clear (CLR) which forces all outputs to the LOW state ($\overline{Q}_D$ HIGH) independent of any other inputs.

Because all the flip-flops are D-type they do not catch 0's or 1's, and the only requirements on any inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

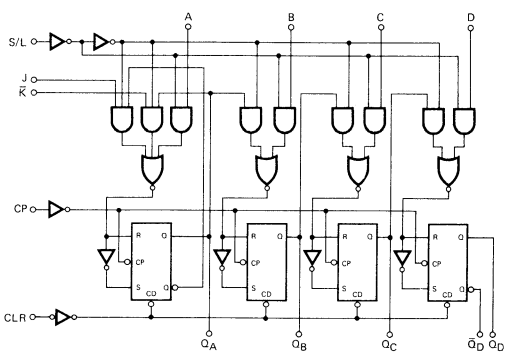
The Am54LS/74LS194A and 195A are standard performance versions of the Am25LS194A and 195A. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

'LS194A



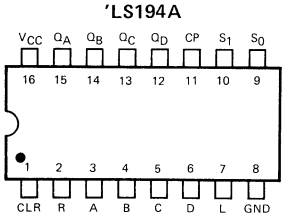

'LS195A



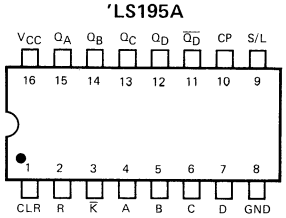

### CONNECTION DIAGRAMS

Top Views

'LS194A

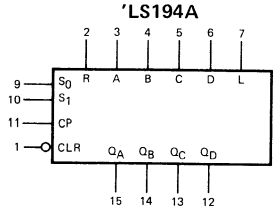



'LS195A

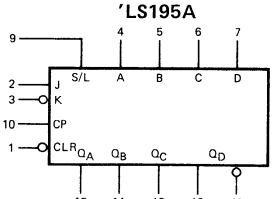



### LOGIC SYMBOLS

'LS194A




'LS195A




VCC = Pin 16
GND = Pin 8

## Am25LS194A • Am25LS195A

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | LS194A (Note 4) | | 15 | 23 | mA |
| | | | LS195A (Note 5) | | 14 | 21 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open. Inputs A, B, C, D grounded. Inputs $S_0$, $S_1$, Clear, L, R, at 4.5V. Measured after a momentary ground, then 4.5V applied to clock.
5. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5V. Measured after applying a momentary ground then 4.5V to the clear followed by ground then 4.5V to clock.

3

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS194A • Am54LS/74LS195A
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −400μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | Am74LS | 2.7 | 3.4 | | Volts |
| | | | Am54LS | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | Am54LS | | | 0.7 | Volts |
| | | | Am74LS | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | LS194A (Note 4) | | 15 | 23 | mA |
| | | | LS195A (Note 5) | | 14 | 21 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open. Inputs A, B, C, D grounded. Inputs $S_0$, $S_1$, Clear, L, R, at 4.5V. Measured after a momentary ground, then 4.5V applied to clock.
5. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5V. Measured after applying a momentary ground then 4.5V to the clear followed by ground then 4.5V to clock.

## Am25LS194A • Am54LS/74LS194A
## SWITCHING CHARACTERISTICS

($T_A = 25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 13 | 21 | | 14 | 22 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Output | | 12 | 18 | | 17 | 26 | ns | |
| $t_{PHL}$ | Clear to Output | | 17 | 26 | | 19 | 30 | ns | |
| $t_{pw}$ | Clock Pulse Width | 17 | | | 20 | | | ns | |
| $t_{pw}$ | Clear Pulse Width | 17 | | | 20 | | | ns | |
| $t_s$ | Mode Control Set-up Time | 25 | | | 30 | | | ns | |
| $t_s$ | Data Input Set-up Time | 16 | | | 20 | | | ns | |
| $t_s$ | Clear Recovery to Clock | 20 | | | 25 | | | ns | |
| $t_h$ | Data Hold Time | 0 | | | 0 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 35 | 55 | | 25 | 36 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS194A ONLY
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 31 | | 36 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Output | | 28 | | 32 | ns | |
| $t_{PHL}$ | Clear to Output | | 38 | | 44 | ns | |
| $t_{pw}$ | Clock Pulse Width | 26 | | 30 | | ns | |
| $t_{pw}$ | Clear Pulse Width | 26 | | 30 | | ns | |
| $t_s$ | Mode Control Set-up Time | 37 | | 42 | | ns | |
| $t_s$ | Data Input Set-up Time | 25 | | 29 | | ns | |
| $t_s$ | Clear Recovery to Clock | 30 | | 35 | | ns | |
| $t_h$ | Data Hold Time | 4 | | 5 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 26 | | 23 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS195A • Am54LS/74LS195 SWITCHING CHARACTERISTICS

($T_A = 25°C$, $V_{CC} = 5.0V$)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 13 | 21 | | 14 | 22 | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | Clock to Output | | 12 | 18 | | 17 | 26 | ns | |
| $t_{PHL}$ | Clear to Output | | 17 | 26 | | 19 | 30 | ns | |
| $t_{pw}$ | Clock Pulse Width | 16 | | | 16 | | | ns | |
| $t_{pw}$ | Clear Pulse Width | 12 | | | 12 | | | ns | |
| $t_s$ | Mode Control Set-up Time | 25 | | | 25 | | | ns | |
| $t_s$ | Data Input Set-up Time | 15 | | | 15 | | | ns | |
| $t_s$ | Clear Recovery to Clock | 20 | | | 25 | | | ns | |
| $t_h$ | Data Hold Time | 0 | | | 0 | | | ns | |
| $t_R$ | Shift/Load Release Time Am54LS/74LS195A Only | | | 0 | | | 0 | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 35 | 55 | | 30 | 39 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS195A ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L Min. ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$) | Am25LS COM'L Max. | Am25LS MIL Min. ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$) | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 31 | | 36 | ns | $C_L = 50pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | Clock to Output | | 27 | | 32 | ns | |
| $t_{PHL}$ | Clear to Output | | 38 | | 44 | ns | |
| $t_{pw}$ | Clock Pulse Width | 25 | | 29 | | ns | |
| $t_{pw}$ | Clear Pulse Width | 20 | | 23 | | ns | |
| $t_s$ | Mode Control Set-up Time | 37 | | 42 | | ns | |
| $t_s$ | Data Input Set-up Time | 24 | | 27 | | ns | |
| $t_s$ | Clear Recovery to Clock | 30 | | 35 | | ns | |
| $t_h$ | Data Hold Time | 4 | | 5 | | ns | |
| $t_R$ | Shift/Load Release Time Am54LS/74LS195A Only | | 4 | | 5 | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | 26 | | 23 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

### 'LS194A FUNCTION TABLE

| FUNCTION | Clear | Mode $S_1$ | Mode $S_0$ | Clock | Serial Left | Serial Right | Parallel A | Parallel B | Parallel C | Parallel D | OUTPUTS $Q_A$ | OUTPUTS $Q_B$ | OUTPUTS $Q_C$ | OUTPUTS $Q_D$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| No Change | H | X | X | L | X | X | X | X | X | X | NC | NC | NC | NC |
| | H | X | X | H | X | X | X | X | X | X | NC | NC | NC | NC |
| Parallel Load | H | H | H | ↑ | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| Shift Right | H | L | H | ↑ | X | L | X | X | X | X | L | $Q_A$ | $Q_B$ | $Q_C$ |
| | H | L | H | ↑ | X | H | X | X | X | X | H | $Q_A$ | $Q_B$ | $Q_C$ |
| Shift Left | H | H | L | ↑ | L | X | X | X | X | X | $Q_B$ | $Q_C$ | $Q_D$ | L |
| | H | H | L | ↑ | H | X | X | X | X | X | $Q_B$ | $Q_C$ | $Q_D$ | H |
| Hold | H | L | L | X | X | X | X | X | X | X | NC | NC | NC | NC |

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition.
$D_i$ = May be a HIGH or a LOW and the respective output will assume the same state.
X = Don't Care
NC = No Change

### 'LS195A FUNCTION TABLE

| Clear | Shift/Load | Clock | Serial J | Serial $\overline{K}$ | Parallel A | Parallel B | Parallel C | Parallel D | OUTPUTS $Q_A$ | OUTPUTS $Q_B$ | OUTPUTS $Q_C$ | OUTPUTS $Q_D$ | OUTPUTS $\overline{Q}_D$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | X | L | X | X | X | X | X | X | NC | NC | NC | NC | NC |
| H | X | H | X | X | X | X | X | X | NC | NC | NC | NC | NC |
| H | L | ↑ | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $\overline{D}_3$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_A$ | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_A$ | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition.
$D_i$ = May be a HIGH or a LOW and the respective output will assume the same state.
X = Don't Care
NC = No Change

Notes: 1. If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.
2. Linear feedback shift counters can be made by connecting the $Q_D$ and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

## DEFINITION OF FUNCTIONAL TERMS

**J, $\overline{K}$** The logic inputs used for controlling the $Q_A$ flip-flop of the Am25LS195A register when S/L is HIGH.

**CLR** Clear. The asynchronous master reset input.

**CP** Clock pulse for the register. Enters data on the LOW-to-HIGH transition.

**S/L** Shift/Load. The input for selection of parallel or serial shifting for the Am25LS195A register. S/L LOW selects parallel entry.

**$S_0$, $S_1$** The mode select inputs of the Am25LS194A.

**A, B, C, D** The four parallel data inputs for the register.

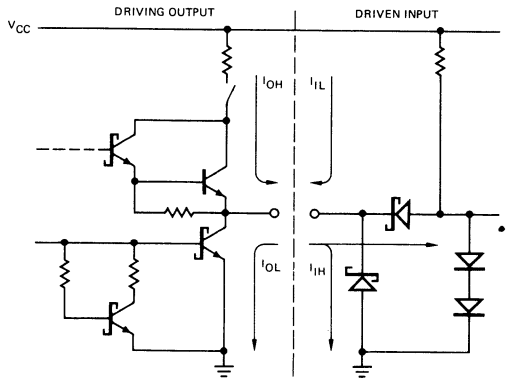
**R** The serial input to the $Q_A$ flip-flop of the Am25LS194A in the right shift mode.

**L** The serial input to the $Q_D$ flip-flop of the Am25LS194A in the left shift mode.

**$Q_A$, $Q_B$, $Q_C$, $Q_D$** The four true outputs of the register.

**$\overline{Q}_D$** The complement output of the $Q_D$ flip-flop. (Am25LS 195A only).

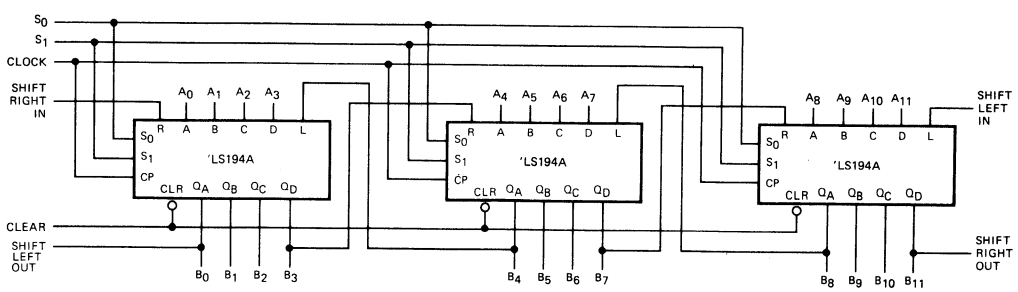
### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

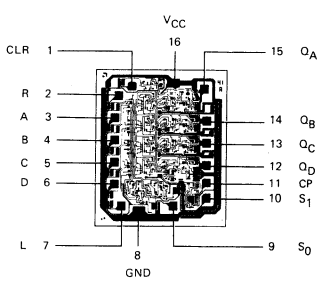
## APPLICATION

### 12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL LOAD REGISTER



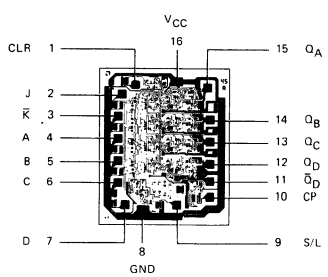

### Metallization and Pad Layouts

#### 'LS194A




DIE SIZE 0.067" X 0.080"

#### 'LS195A




DIE SIZE 0.067" X 0.080"

# Am25LS240 • Am54LS/74LS240

## Octal Three-State Inverting Drivers

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS240 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

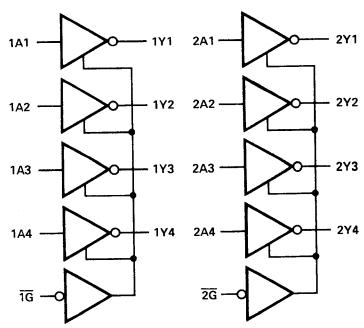
### FUNCTIONAL DESCRIPTION

The 'LS240 is an octal inverting line driver fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

Three-state outputs are provided to drive bus lines directly. The Am25LS240 is specified at 48mA and 24mA output sink current, while the Am54/74LS240 is guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

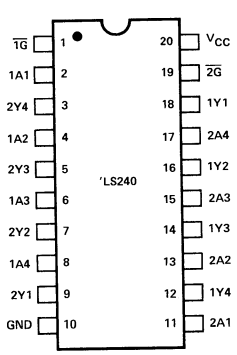
### LOGIC DIAGRAM




| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

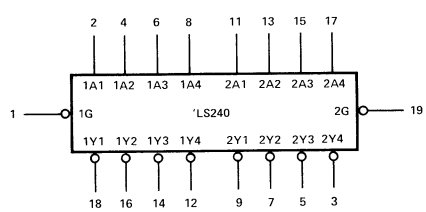
Note: All devices have input hysteresis.

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## Am25LS240
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2.0V<br>$I_{OH}$ = −3.0mA, $V_{IL}$ = $V_{IL}$MAX. | | 2.4 | 3.4 | | Volts |
| | | | $V_{CC}$ = MIN., | MIL, $I_{OH}$ = −12mA | 2.0 | | | |
| | | | $V_{IL}$ = 0.5V | COM'L, $I_{OH}$ = −15mA | 2.0 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_{CC}$ = MIN. | All $I_{OL}$ = 12mA | | 0.25 | 0.4 | Volts |
| | | | | All $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| | | | | COM'L $I_{OL}$ = 48mA | | | 0.55 | |
| $V_{IH}$ | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| $V_{IK}$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | −1.5 | Volts |
| | Hysteresis ($V_{T+}$ − $V_{T-}$) | | $V_{CC}$ = MIN. | | 0.2 | 0.4 | | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = MAX.<br>$V_{IH}$ = 2.0V<br>$V_{IL}$ = $V_{IL}$MAX. | $V_O$ = 2.7V | | | 20 | μA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.4V | | | −20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = MAX., $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | | $V_{CC}$ MAX., $V_{IH}$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | | $V_{CC}$ = MAX., $V_{IL}$ = 0.4V | | | | −200 | μA |
| $I_{SC}$ | Short Circuit Output Current (Note 3) | | $V_{CC}$ = MAX. | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX. Outputs open | All Outputs HIGH | | | 13 | 23 | mA |
| | | | All Outputs LOW | | | 26 | 44 | |
| | | | Outputs at Hi-Z | | | 29 | 50 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

**MAXIMUM RATINGS** above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current | 150mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS240
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

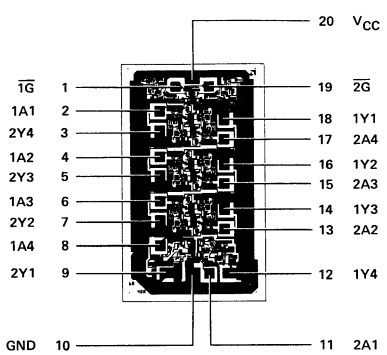
## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2.0V<br>$I_{OH}$ = −3.0mA, $V_{IL}$ = $V_{IL}$MAX. | | 2.4 | 3.4 | | Volts |
| | | | $V_{CC}$ = MIN., | MIL, $I_{OH}$ = −12mA | 2.0 | | | |
| | | | $V_{IL}$ = 0.5V | COM'L, $I_{OH}$ = −15mA | 2.0 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_{CC}$ = MIN. | All, $I_{OL}$ = 12mA | | 0.25 | 0.4 | Volts |
| | | | | COM'L, $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| $V_{IH}$ | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| $V_{IK}$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | −1.5 | Volts |
| | Hysteresis ($V_{T+}$ − $V_{T-}$) | | $V_{CC}$ = MIN. | | 0.2 | 0.4 | | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = MAX.<br>$V_{IH}$ = 2.0V<br>$V_{IL}$ = $V_{IL}$MAX. | $V_O$ = 2.7V | | | 20 | μA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.4V | | | −20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = MAX., $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | | $V_{CC}$ MAX., $V_{IH}$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | | $V_{CC}$ = MAX., $V_{IL}$ = 0.4V | | | | −200 | μA |
| $I_{SC}$ | Short Circuit Output Current (Note 3) | | $V_{CC}$ = MAX. | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX. Outputs open | All Outputs HIGH | | | 13 | 23 | mA |
| | | | All Outputs LOW | | | 26 | 44 | |
| | | | Outputs at Hi-Z | | | 29 | 50 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

3

### Metallization and Pad Layout




DIE SIZE 0.060" X 0.103"

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

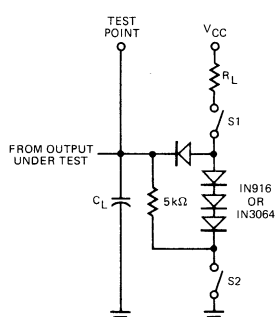
| Parameters | Description | Am25LS240 Min. | Am25LS240 Typ. | Am25LS240 Max. | Am54LS/74LS240 Min. | Am54LS/74LS240 Typ. | Am54LS/74LS240 Max. | Units | Test Conditions (Notes 1–5) |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 8.0 | 12 | | 9.0 | 14 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 12 | 16 | | 12 | 18 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 19 | 27 | | 20 | 30 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 14 | 20 | | 15 | 23 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 14 | 23 | | 15 | 25 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{PHZ}$ | Output Disable Time from High Level | | 10 | 18 | | 10 | 18 | ns | |

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

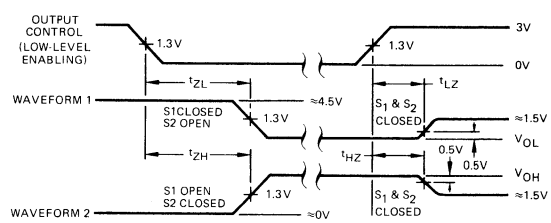
| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 16 | | 19 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 22 | | 25 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 37 | | 42 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 27 | | 31 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 31 | | 36 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{PHZ}$ | Output Disable Time from High Level | | 25 | | 28 | ns | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### LOAD CIRCUIT FOR THREE-STATE OUTPUTS




### VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS




Notes:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT}$ ≈ 50Ω and $t_r$ ≤ 2.5ns, $t_f$ ≤ 2.5ns.

# Am25LS241 • Am54LS/74LS241
# Am25LS244 • Am54LS/74LS244

## Octal Three-State Buffers

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS241 and 244 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The 'LS241 and 'LS244 are octal buffers fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

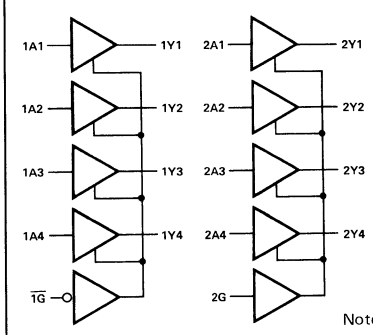
Three-state outputs are provided to drive bus lines directly. The Am25LS241 and Am25LS244 are specified at 48mA and 24mA output sink current, while the Am54LS/74LS241 and Am54LS/74LS244 are guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

The 'LS241 has enable inputs of opposite polarity to allow use as a transceiver without overlap. The 'LS244 enables are of similar polarity for use as a unidirectional buffer in which both halves are enabled simultaneously.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

### LOGIC DIAGRAMS

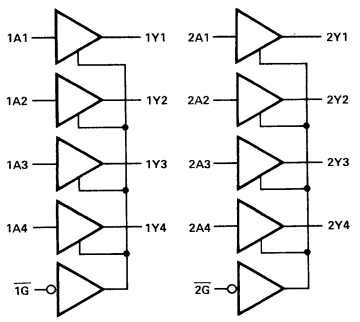
'LS241




'LS241

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{1G}$ | 2G | A | Y |
| H | L | X | Z |
| L | H | H | H |
| L | H | L | L |

'LS244

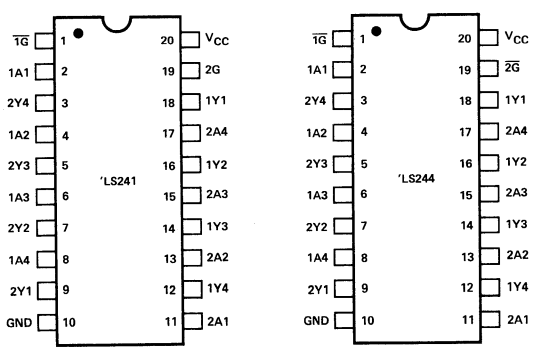



'LS244

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | |
| H | X | Z |
| L | H | H |
| L | L | L |

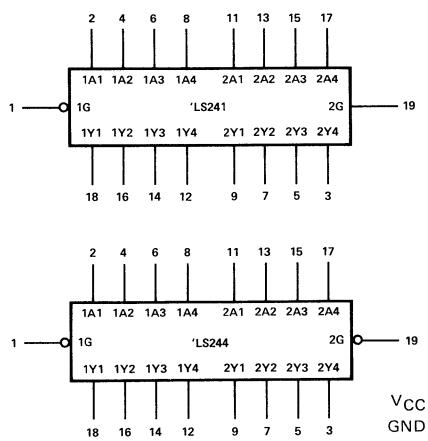
Note: All devices have input hysteresis.

### CONNECTION DIAGRAMS
Top Views




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOLS




$V_{CC}$ = Pin 20
GND = Pin 10

## Am25LS241•Am25LS244
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2.0V<br>$I_{OH}$ = −3.0mA, $V_{IL}$ = $V_{IL}$MAX. | | 2.4 | 3.4 | | Volts |
| | | | $V_{CC}$ = MIN., $V_{IL}$ = 0.5V | MIL, $I_{OH}$ = −12mA | 2.0 | | | |
| | | | | COM'L, $I_{OH}$ = −15mA | 2.0 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_{CC}$ = MIN. | All $I_{OL}$ = 12mA | | 0.25 | 0.4 | Volts |
| | | | | All $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| | | | | COM'L, $I_{OL}$ = 48mA | | | 0.55 | |
| $V_{IH}$ | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| $V_{IK}$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | −1.5 | Volts |
| | Hysteresis ($V_{T+}$ − $V_{T-}$) | | $V_{CC}$ = MIN. | | 0.2 | 0.4 | | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = MAX.<br>$V_{IH}$ = 2.0V<br>$V_{IL}$ = $V_{IL}$MAX. | $V_O$ = 2.7V | | | 20 | μA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.4V | | | −20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = MAX., $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | | $V_{CC}$ = MAX., $V_{IH}$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | | $V_{CC}$ = MAX., $V_{IL}$ = 0.4V | | | | −200 | μA |
| $I_{SC}$ | Short Circuit Output Current (Note 3) | | $V_{CC}$ = MAX. | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX. Outputs open | All Outputs HIGH | | | 13 | 23 | mA |
| | | | All Outputs LOW | | | 27 | 46 | |
| | | | Outputs at Hi-Z | | | 32 | 54 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

**MAXIMUM RATINGS** above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current | 150mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS241•Am54LS/74LS244
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

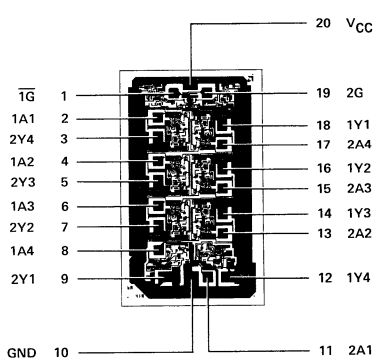
## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2.0V<br>$I_{OH}$ = −3.0mA, $V_{IL}$ = $V_{IL}$MAX. | | 2.4 | 3.4 | | Volts |
| | | | $V_{CC}$ = MIN., $V_{IL}$ = 0.5V | MIL, $I_{OH}$ = −12mA | 2.0 | | | |
| | | | | COM'L, $I_{OH}$ = −15mA | 2.0 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_{CC}$ = MIN. | All, $I_{OL}$ = 12mA | | 0.25 | 0.4 | Volts |
| | | | | COM'L, $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| $V_{IH}$ | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| $V_{IK}$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | −1.5 | Volts |
| | Hysteresis ($V_{T+}$ − $V_{T-}$) | | $V_{CC}$ = MIN. | | 0.2 | 0.4 | | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = MAX. $V_{IH}$ = 2.0V $V_{IL}$ = $V_{IL}$MAX. | $V_O$ = 2.7V | | | 20 | μA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.4V | | | −20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = MAX., $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | | $V_{CC}$ = MAX., $V_{IH}$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | | $V_{CC}$ = MAX., $V_{IL}$ = 0.4V | | | | −200 | μA |
| $I_{SC}$ | Short Circuit Output Current (Note 3) | | $V_{CC}$ = MAX. | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX. Outputs open | All Outputs HIGH | | | 13 | 23 | mA |
| | | | All Outputs LOW | | | 27 | 46 | |
| | | | Outputs at Hi-Z | | | 32 | 54 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

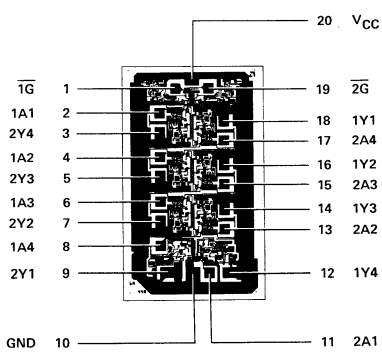
### Metallization and Pad Layouts

'LS241




DIE SIZE 0.060" X 0.103"

'LS244




DIE SIZE 0.060" X 0.103"

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

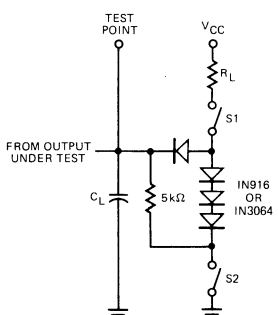
| Parameters | Description | Am25LS241 Am25LS244 Min. | Typ. | Max. | Am54LS/74LS241 Am54LS/74LS244 Min. | Typ. | Max. | Units | Test Conditions (Notes 1–5) |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 10 | 15 | | 12 | 18 | ns | $C_L$ = 45pF $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 12 | 18 | | 12 | 18 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 20 | 30 | | 20 | 30 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 15 | 23 | | 15 | 23 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 15 | 25 | | 15 | 25 | ns | $C_L$ = 5.0pF |
| $t_{PHZ}$ | Output Disable Time from High Level | | 10 | 18 | | 10 | 18 | ns | $R_L$ = 667Ω |

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

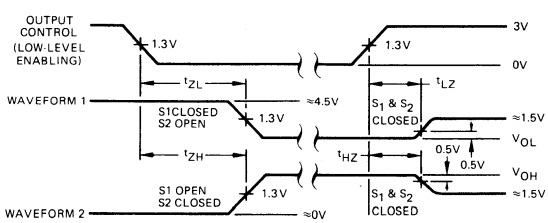
| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% Min. | Max. | Am25LS MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 21 | | 24 | ns | $C_L$ = 45pF $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 25 | | 28 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 41 | | 47 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 31 | | 47 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 34 | | 36 | ns | $C_L$ = 5.0pF |
| $t_{PHZ}$ | Output Disable Time from High Level | | 25 | | 28 | ns | $R_L$ = 667Ω |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS




VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS




Notes:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1.0MHz, $Z_{OUT}$ ≈ 50Ω, $t_r$ ≤ 15ns, $t_f$ ≤ 6ns.
5. When measuring $t_{PLH}$ and $t_{PHL}$, switches $S_1$ and $S_2$ are closed.

# Am25LS242 • Am54LS/74LS242
# Am25LS243 • Am54LS/74LS243

## Quad Bus Transceivers with Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data to output propagation delay times – 18ns MAX.
- Enable to output – 30ns MAX.
- Am25LS242 and Am25LS243 are specified at 48mA output current
- 100% product assurance testing to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The 'LS242 and 'LS243 are quad bus transceivers designed for asynchronous two-way communications between data buses.

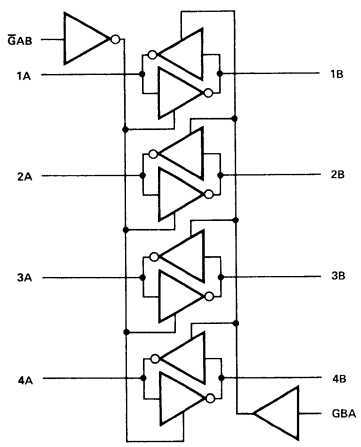
The 'LS242 and 'LS243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The 'LS242 is inverting, while the 'LS243 presents non-inverting data at the outputs.

Three-state outputs are provided to drive bus lines directly. The Am25LS242 and Am25LS243 are specified at 48mA and 24mA output sink current, while the Am54/74LS242 and 243 are guaranteed at 12mA over the military range and 24mA over the commercial range.

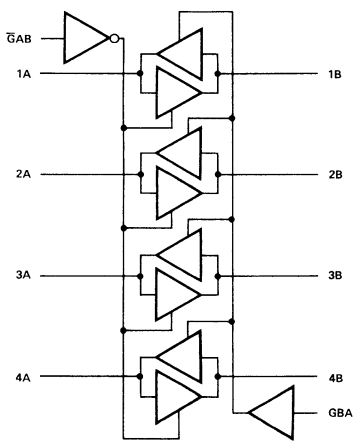
Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

### LOGIC DIAGRAMS

Am54LS/74LS242



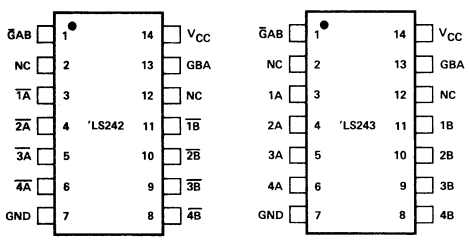

Am54LS/74LS243




Note: All devices have input hysteresis.

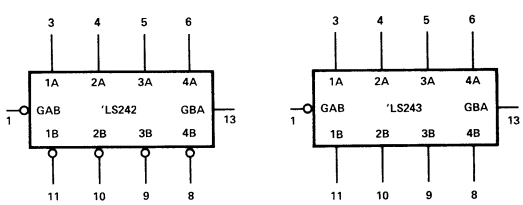
### CONNECTION DIAGRAMS

Top Views




Note: Pin 1 is marked for orientation

### LOGIC SYMBOLS




$V_{CC}$ = Pin 14
GND = Pin 7

## Am25LS242 • Am25LS243
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2.0V<br>$I_{OH}$ = −3.0mA, $V_{IL}$ = $V_{IL}$MAX. | | 2.4 | 3.4 | | Volts |
| | | | $V_{CC}$ = MIN., $V_{IL}$ = 0.5V | MIL, $I_{OH}$ = −12mA | 2.0 | | | |
| | | | | COM'L, $I_{OH}$ = −15mA | 2.0 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_{CC}$ = MIN. | All $I_{OL}$ = 12mA | | 0.25 | 0.4 | Volts |
| | | | | All $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| | | | | COM'L, $I_{OL}$ = 48mA | | | 0.55 | |
| $V_{IH}$ | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| $V_{IK}$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | −1.5 | Volts |
| | Hysteresis ($V_{T+}$ − $V_{T-}$) | | $V_{CC}$ = MIN. | | 0.2 | 0.4 | | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = MAX. $V_{IH}$ = 2.0V $V_{IL}$ = $V_{IL}$MAX. | $V_O$ = 2.7V | | | 20 | μA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.4V | | | −20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = MAX., $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | | $V_{CC}$ = MAX., $V_{IH}$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | | $V_{CC}$ = MAX., $V_{IL}$ = 0.4V | | | | −200 | μA |
| $I_{SC}$ | Short Circuit Output Current (Note 3) | | $V_{CC}$ = MAX. | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX. Outputs open (Note 4) | All Outputs HIGH | 'LS242, 'LS243 | | 22 | 38 | mA |
| | | | All Outputs LOW | 'LS242, 'LS243 | | 29 | 50 | |
| | | | Outputs at Hi-Z | 'LS242 | | 29 | 50 | |
| | | | | 'LS243 | | 32 | 54 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.

2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.

3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

4. For 'LS242 and 'LS243 $I_{CC}$ is measured with transceivers enabled in one direction only, or with all transceivers disabled.

**MAXIMUM RATINGS** above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current | 150mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS242 • Am54LS/74LS243
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5% (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2.0V, $I_{OH}$ = −3.0mA, $V_{IL}$ = $V_{IL}$MAX. | | 2.4 | 3.4 | | Volts |
| | | | $V_{CC}$ = MIN., $V_{IL}$ = 0.5V | MIL, $I_{OH}$ = −12mA | 2.0 | | | |
| | | | | COM'L, $I_{OH}$ = −15mA | 2.0 | | | |
| $V_{OL}$ | Low-Level Output Voltage | | $V_{CC}$ = MIN. | All, $I_{OL}$ = 12mA | | 0.25 | 0.4 | Volts |
| | | | | COM'L, $I_{OL}$ = 24mA | | 0.35 | 0.5 | |
| $V_{IH}$ | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| $V_{IK}$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | −1.5 | Volts |
| | Hysteresis ($V_{T+}$ − $V_{T-}$) | | $V_{CC}$ = MIN. | | 0.2 | 0.4 | | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | | $V_{CC}$ = MAX., $V_{IH}$ = 2.0V, $V_{IL}$ = $V_{IL}$MAX. | $V_O$ = 2.7V | | | 20 | μA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.4V | | | −20 | |
| $I_I$ | Input Current at Maximum Input Voltage | | $V_{CC}$ = MAX., $V_I$ = 7.0V | | | | 0.1 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | | $V_{CC}$ MAX., $V_{IH}$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low-Level Input Current | | $V_{CC}$ = MAX., $V_{IL}$ = 0.4V | | | | −200 | μA |
| $I_{SC}$ | Short Circuit Output Current (Note 3) | | $V_{CC}$ = MAX. | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX. Outputs open (Note 4) | All Outputs HIGH | 'LS242, 'LS243 | | 22 | 38 | mA |
| | | | All Outputs LOW | 'LS242, 'LS243 | | 29 | 50 | |
| | | | Outputs at Hi-Z | 'LS242 | | 29 | 50 | |
| | | | | 'LS243 | | 32 | 54 | |

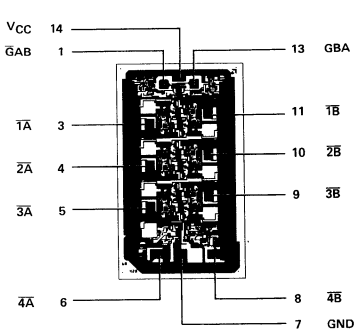
Notes: 1. For conditions shown as MIN' or MAX., use the appropriate value specified under recommended operating conditions.

2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.

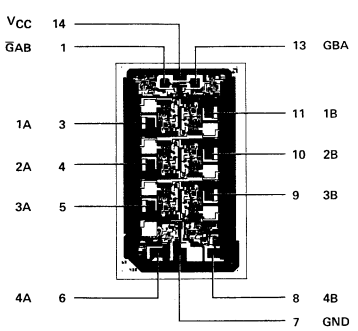
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

4. For 'LS242 and 'LS243 $I_{CC}$ is measured with transceivers enabled in one direction only, or with all transceivers disabled.

### Metallization and Pad Layouts




DIE SIZE 0.060" x 0.103"




DIE SIZE 0.060" x 0.103"

## Am25LS242•Am54LS/74LS242 SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS242 Min. | Am25LS242 Typ. | Am25LS242 Max. | Am54LS/74LS242 Min. | Am54LS/74LS242 Typ. | Am54LS/74LS242 Max. | Units | Test Conditions (Notes 1–5) |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 8.0 | 12 | | 9.0 | 14 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 12 | 16 | | 12 | 18 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 20 | 30 | | 20 | 30 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 15 | 23 | | 15 | 23 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 15 | 25 | | 15 | 25 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{PHZ}$ | Output Disable Time from High Level | | 10 | 18 | | 10 | 18 | ns | |

## Am25LS242 ONLY SWITCHING CHARACTERISTICS OVER OPERATION RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 16 | | 19 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 22 | | 25 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 37 | | 42 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 29 | | 33 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 33 | | 38 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{PHZ}$ | Output Disable Time from High Level | | 25 | | 28 | ns | |

## Am25LS243•Am54LS/74LS243 SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

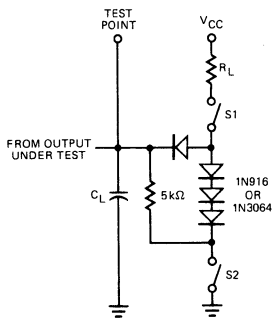
| Parameters | Description | Am25LS243 Min. | Am25LS243 Typ. | Am25LS243 Max. | Am54LS/74LS243 Min. | Am54LS/74LS243 Typ. | Am54LS/74LS243 Max. | Units | Test Conditions (Notes 1–5) |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 10 | 15 | | 12 | 18 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 12 | 18 | | 12 | 18 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 20 | 30 | | 20 | 30 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 15 | 23 | | 15 | 23 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 15 | 25 | | 15 | 25 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{PHZ}$ | Output Disable Time from High Level | | 10 | 18 | | 10 | 18 | ns | |

## Am25LS243 ONLY SWITCHING CHARACTERISTICS OVER OPERATION RANGE*

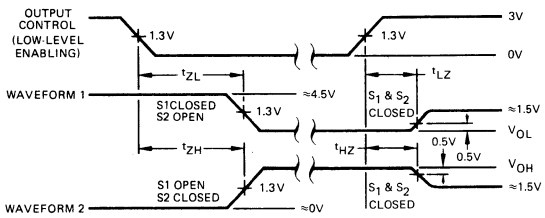
| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | | 21 | | 24 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | 25 | | 28 | ns | |
| $t_{PZL}$ | Output Enable Time to Low Level | | 41 | | 47 | ns | |
| $t_{PZH}$ | Output Enable Time to High Level | | 33 | | 49 | ns | |
| $t_{PLZ}$ | Output Disable Time from Low Level | | 36 | | 38 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{PHZ}$ | Output Disable Time from High Level | | 25 | | 28 | ns | |

## SWITCHING CHARACTERISTICS TEST CONDITIONS

### LOAD CIRCUIT FOR THREE-STATE OUTPUTS




### VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS




Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1MHz, $Z_{OUT} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.
5. When measuring $t_{PLH}$ and $t_{PHL}$, switches $S_1$ and $S_2$ are closed.

3

## FUNCTION TABLES

### Am54LS/74LS242

| CONTROL INPUTS | | DATA OUTPUTS | |
|---|---|---|---|
| $\overline{G}AB$ | GBA | A | B |
| H | H | $\overline{O}$ | I |
| L | H | * | * |
| H | L | ISOLATED | |
| L | L | I | $\overline{O}$ |

I = Input
O = Output
$\overline{O}$ = Inverting Output

H = HIGH
L = LOW

### Am54LS/74LS243

| CONTROL INPUTS | | DATA OUTPUTS | |
|---|---|---|---|
| $\overline{G}AB$ | GBA | A | B |
| H | H | O | I |
| L | H | * | * |
| H | L | ISOLATED | |
| L | L | I | O |

*Possible destructive oscillation may occur if the transceivers are enable in both directions at once.

# Am54LS/74LS245

Octal Bus Transceiver

**Advanced Micro Devices has no current plans to manufacture this product.**

**See the Am8304 for a recommended improved Octal Bus Transceiver.**

# Am25LS251 • Am54LS/74LS251

## Eight-Input Multiplexers

**Am25LS251•Am54LS/74LS251 data is combined with the Am25LS151.**

**See Am25LS151 data sheet for full information.**

### FUNCTIONAL DESCRIPTION

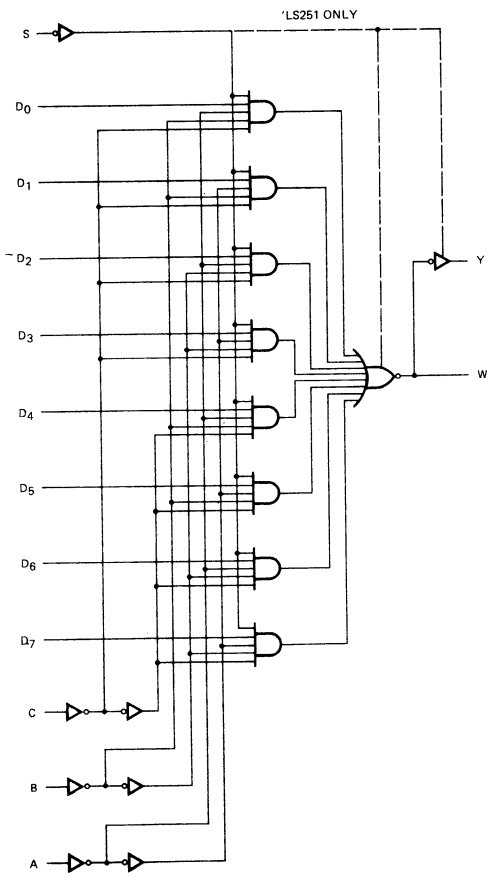
The Am25LS151 and the Am25LS251 are eight-input multiplexers that switch one of eight inputs onto the inverting and non-inverting outputs under the control of a three-bit select code. The inverting output W is one gate delay faster than the non-inverting output Y.

The Am25LS251 provides an active-LOW strobe. When the strobe is HIGH, the inverting output (W) is HIGH and the non-inverting output (Y) is LOW.

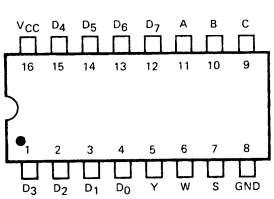
The Am25LS251 features a three-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

The Am54LS/74LS251 is a standard performance version of the Am25LS251. See appropriate electrical characteristics tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

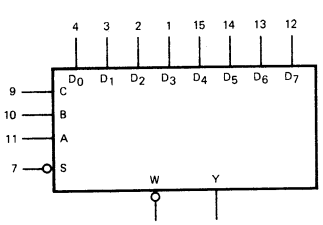



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




VCC = Pin 16
GND = Pin 8

# Am25LS253 • Am54LS/74LS253

## Dual 4-Line to 1-Line Data Selectors/Multiplexers

**Am25LS253•Am54LS/74LS253 data is combined with the Am25LS153.**

**See Am25LS153 data sheet for full information**

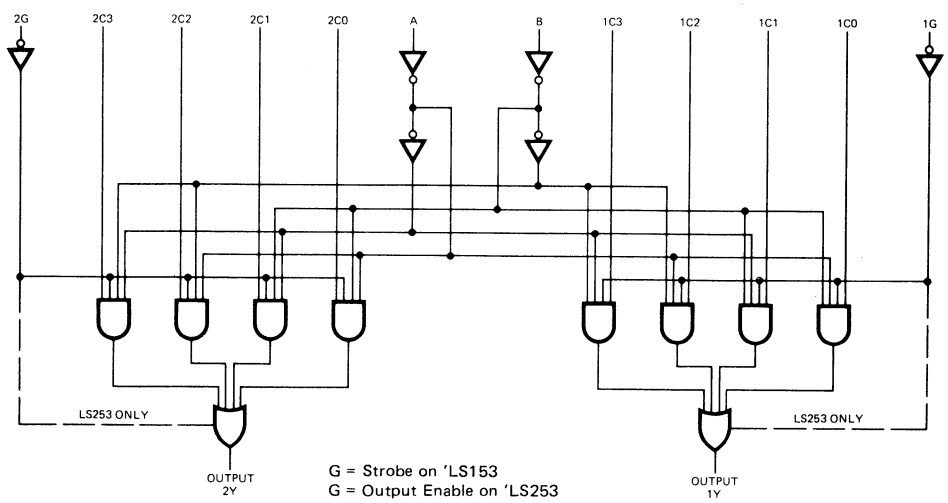
### FUNCTIONAL DESCRIPTION

These dual four-input multiplexers provide the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am25LS153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

The Am25LS253 features a three-state output to interface with bus-organized systems. Each section of the Am25LS253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

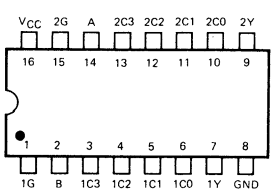
The Am54LS/74LS153 and 253 are standard performance versions of the Am25LS153 and 253. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM



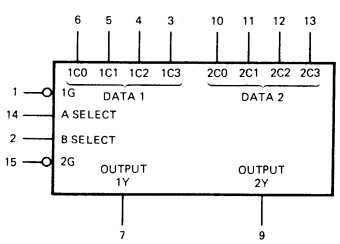

G = Strobe on 'LS153
G = Output Enable on 'LS253

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




VCC = Pin 16
GND = Pin 8

# Am25LS257 • Am54LS/74LS257
# Am25LS258 • Am54LS/74LS258

## Quadruple 2-Line To 1-Line Data Selectors/Multiplexers With 3-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs
- Pin-outs identical to standard TTL 'LS157 and 'LS158 devices
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$
  - Twice the fan-out over military range
  - 440$\mu$A source current
- 100% product assurance screening to MIL-STD-883 requirements

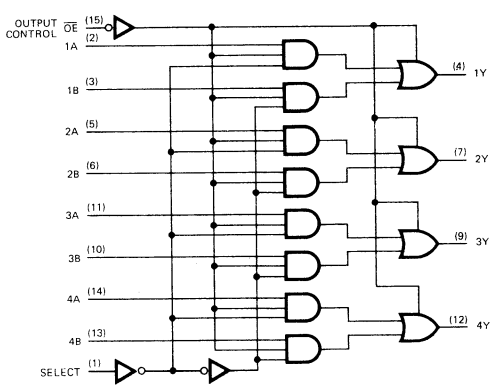
### FUNCTIONAL DESCRIPTION

The 2-line to 1-line data selector multiplexer can be used to transfer data to a common data bus directly by using the three-state capability of the device. With the output control ($\overline{OE}$) HIGH, the four outputs of the data selector are in the high impedance state. With the output control LOW, the selected four bits (A or B inputs) are bussed onto the four data lines.

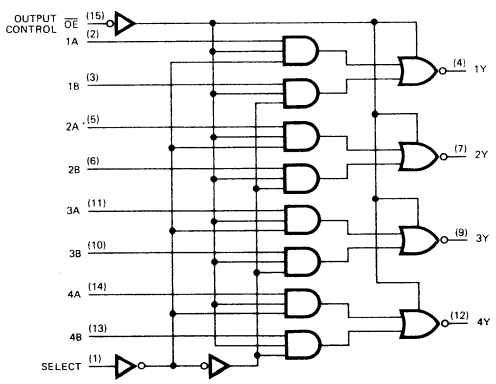
The Am54LS/74LS257 and 258 are standard performance versions of the Am25LS257 and 258. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAMS

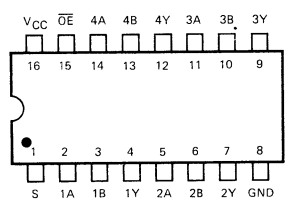
'LS257




'LS258



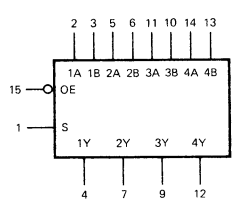

### CONNECTION DIAGRAM
Top View



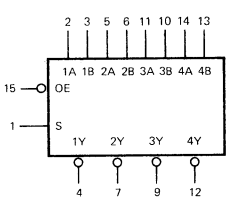

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOLS

'LS257




'LS258




VCC = Pin 16
GND = Pin 8

## Am25LS257 • Am25LS258

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1mA$ | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | $I_{OL} = 4mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | S, $\overline{OE}$ | | | −0.36 | mA |
| | | | Others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | S, $\overline{OE}$ | | | 20 | µA |
| | | | Others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | S, $\overline{OE}$ | | | 0.1 | mA |
| | | | Others | | | 0.1 | |
| $I_{OZ}$ | Off-State (HIGH Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 2.4V$ | | | 20 | µA |
| | | | $V_O = 0.4V$ | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current — All Outputs HIGH | $V_{CC}$ = MAX. (Note 4) | LS257 | | 6.3 | 10.0 | mA |
| | | | LS258 | | 4.3 | 8.0 | |
| | Power Supply Current — All Outputs LOW | | LS257 | | 8.2 | 13.5 | mA |
| | | | LS258 | | 6.1 | 11.0 | |
| | Power Supply Current — All Outputs OFF | | LS257 | | 9.7 | 15.3 | mA |
| | | | LS258 | | 7.2 | 11.2 | |

Notes:
1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS257 • Am54LS/74LS258

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | 54LS, $I_{OH} = -1mA$ | 2.4 | 3.4 | | Volts |
| | | | 74LS, $I_{OH} = -2.6mA$ | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | All, $I_{OL} = 4mA$ | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL} = 8mA$ | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | 54LS | | | 0.7 | Volts |
| | | | 74LS | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | S | | | −0.8 | mA |
| | | | Others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | S | | | 40 | μA |
| | | | Others | | | 20 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | S | | | 0.2 | mA |
| | | | Others | | | 0.1 | |
| $I_{OZ}$ | Off-State (HIGH Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 2.4V$ | | | 20 | μA |
| | | | $V_O = 0.4V$ | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | All Outputs HIGH | LS257 | | 5.9 | 10 | mA |
| | | | LS258 | | 4.1 | 8 | |
| | | All Outputs LOW | LS257 | | 9.2 | 16 | mA |
| | | | LS258 | | 6.2 | 11 | |
| | | All Outputs OFF | LS257 | | 10 | 17 | mA |
| | | | LS258 | | 7.0 | 12 | |

Notes:
1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

3

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | LS257 | | 8 | 12 | | 12 | 18 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| | | LS258 | | 6 | 12 | | 12 | 18 | | |
| $t_{PHL}$ | Data to Output | LS257 | | 8 | 12 | | 12 | 18 | ns | |
| | | LS258 | | 7 | 12 | | 12 | 18 | | |
| $t_{PLH}$ | Select to Output | LS257 | | 14 | 21 | | 14 | 21 | ns | |
| | | LS258 | | 14 | 21 | | 14 | 21 | | |
| $t_{PHL}$ | Select to Output | LS257 | | 14 | 21 | | 14 | 21 | ns | |
| | | LS258 | | 14 | 21 | | 14 | 21 | | |
| $t_{ZH}$ | Control to Output | | | 13 | 20 | | 20 | 30 | ns | |
| $t_{ZL}$ | | | | 13 | 20 | | 20 | 30 | | |
| $t_{HZ}$ | Control to Output | | | 12 | 20 | | 14 | 21 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 13 | 20 | | 14 | 21 | | |

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L Min. ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) | Am25LS COM'L Max. | Am25LS MIL Min. ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | LS257 | | 20 | | 23 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| | | LS258 | | 20 | | 23 | | |
| $t_{PHL}$ | Data to Output | LS257 | | 20 | | 23 | ns | |
| | | LS258 | | 20 | | 23 | | |
| $t_{PLH}$ | Select to Output | LS257 | | 31 | | 36 | ns | |
| | | LS258 | | 31 | | 36 | | |
| $t_{PHL}$ | Select to Output | LS257 | | 31 | | 36 | ns | |
| | | LS258 | | 31 | | 36 | | |
| $t_{ZH}$ | Control to Output | | | 30 | | 35 | ns | |
| $t_{ZL}$ | | | | 30 | | 35 | | |
| $t_{HZ}$ | Control to Output | | | 26 | | 30 | ns | $R_L$ = 2.0kΩ, $C_L$ = 5.0pF |
| $t_{LZ}$ | | | | 26 | | 30 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**1A, 2A, 3A, 4A** The data inputs for the 4-bits of the A word.

**1B, 2B, 3B, 4B** The data inputs for the 4-bits of the B word.

**1Y, 2Y, 3Y, 4Y** The four outputs of the multiplexer.

**$\overline{OE}$ Output Control** When the output control is HIGH, the four outputs are in the high impedance state. When the output control is LOW, the selected A or B input is present at the output.

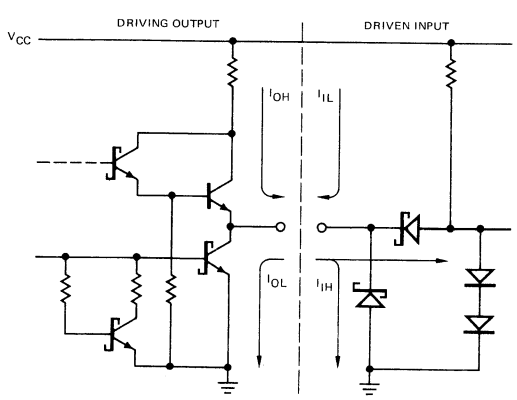
**S Select** When the select input is LOW, the A word is present at the output. When the select input is HIGH, the B word is present at the output.

## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| Output Control | Select | A | B | 'LS257 | 'LS258 |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

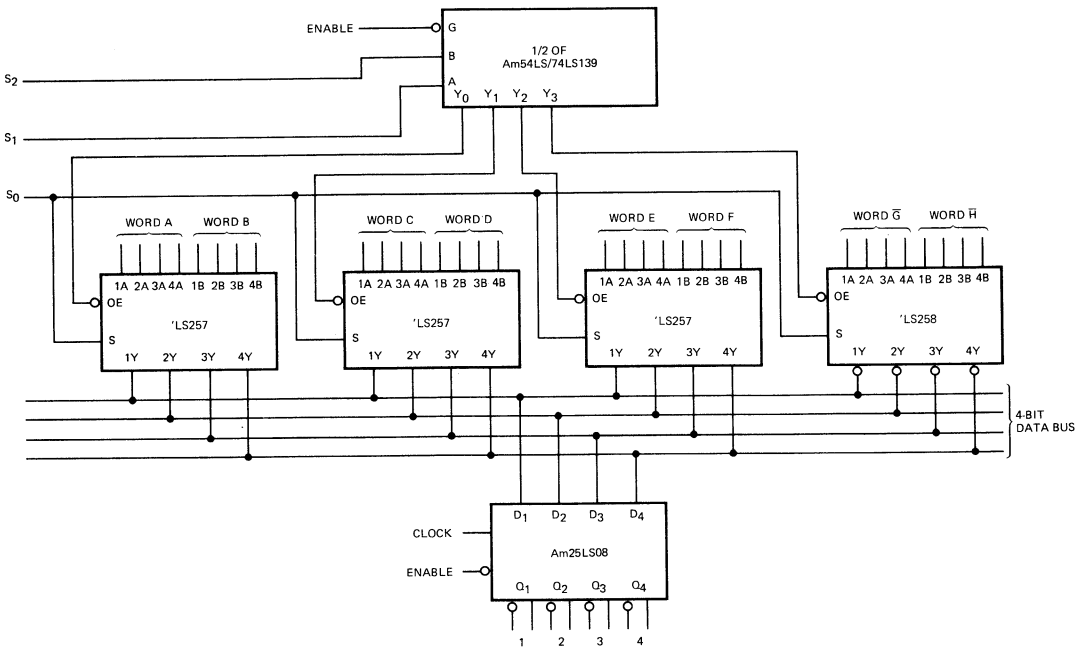
H = HIGH L = LOW X = Don't Care Z = High Impedance

## Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## APPLICATION

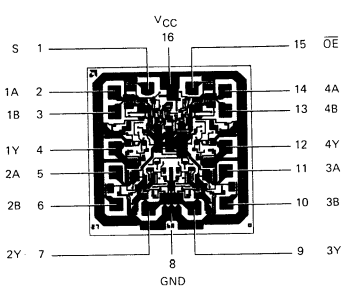



8-Word, 4-Bit Multiplexer

3

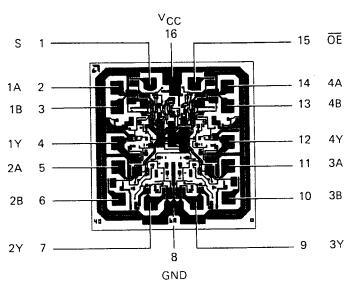
### Metallization and Pad Layout

**'LS257**




DIE SIZE 0.057" X 0.057"

**'LS258**




DIE SIZE 0.057" X 0.057"

# Am25LS273B • Am54LS/74LS273B

## 8-Bit Register with Clear

### DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Buffered outputs to eliminate output commutation
- Positive edge-triggered D-type flip-flops
- Common clock and common clear
- Am25LS devices offer the following improvements over Am54/74LS
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440µA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

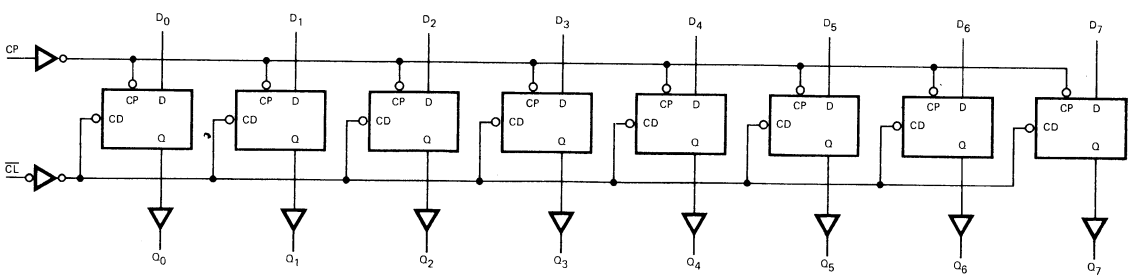
### FUNCTIONAL DESCRIPTION

The Am25LS273B and the Am54LS/74LS273B are eight-bit registers built using Advanced Low-Power Schottky Technology. These registers consist of D-type flip-flops with a buffer common clock and an asynchronous active LOW buffered common clear.

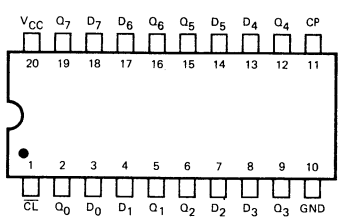
When the clear input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input. These devices are supplied in the 20-pin space saving package featuring 0.3-inch centers between rows of leads.

**Note: The B designation identifies buffered output versions provided to eliminate output commutation.**

### LOGIC DIAGRAM

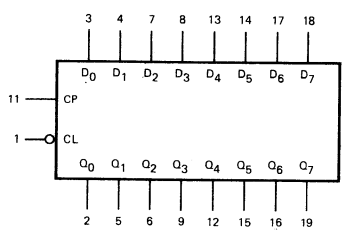



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## Am25LS273B
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440 µA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 4.0 mA | | | | 0.4 | Volts |
| | | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 8.0 mA | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18 mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 17 | 27 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open and 4.5 V applied to the data and clear input. Measured after a momentary ground, then 4.5 V applied to the clock input.

3

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS273B

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0 mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8.0 mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18$ mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 17 | 27 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open and 4.5 V applied to the data and clear input. Measured after a momentary ground, then 4.5 V applied to the clock input.

### DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The D flip-flop data inputs.

**$\overline{CL}$** Clear. When the clear is LOW, the $Q_i$ outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.

**CP** Clock pulse for the register. Enters data on the positive transition.

**$Q_i$** The TRUE register outputs.

### FUNCTION TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| Clear | Clock | $D_i$ | $Q_i$ |
| L | X | X | L |
| H | L | X | NC |
| H | H | X | NC |
| H | ↑ | L | L |
| H | ↑ | H | H |

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care
NC = No Change

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 21 | 32 | | 21 | 32 | ns | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 26 | 38 | | 26 | 38 | | |
| $t_{PHL}$ | Clear to Output | | | 28 | 39 | | 28 | 39 | ns | |
| $t_{pw}$ | Clock Pulse Width | HIGH | 20 | | | 20 | | | ns | |
| | | LOW | 25 | | | 25 | | | | |
| $t_{pw}$ | Clear Pulse Width | | 25 | | | 25 | | | ns | |
| $t_s$ | Data Set-up | | 20 | | | 20 | | | ns | |
| $t_h$ | Data Hold | | 10 | | | 10 | | | ns | |
| $t_s$ | Set-up, Clear Recovery (In-Active) to Clock | | 25 | | | 25 | | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | | 30 | 40 | | 30 | | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constaints on $t_r$, $t_f$, pulse width or duty cycle.

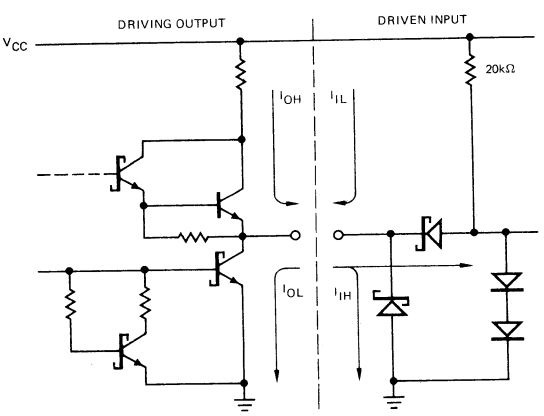
## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 36 | | 40 | ns | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 49 | | 60 | | |
| $t_{PHL}$ | Clear to Output | | | 50 | | 60 | ns | |
| $t_{pw}$ | Clock Pulse Width | HIGH | 25 | | 30 | | ns | |
| | | LOW | 30 | | 35 | | | |
| $t_{pw}$ | Clear Pulse Width | | 25 | | 25 | | ns | |
| $t_s$ | Data Set-up | | 20 | | 20 | | ns | |
| $t_h$ | Data Hold | | 12 | | 15 | | ns | |
| $t_s$ | Set-up, Clear Recovery (In-Active) to Clock | | 25 | | 25 | | ns | |
| $f_{max}$ (Note 1) | Maximum Clock Frequency | | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

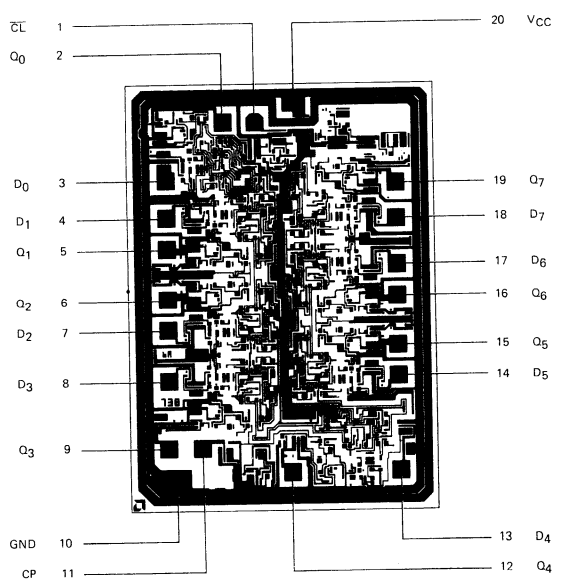
3

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

### Metallization and Pad Layout

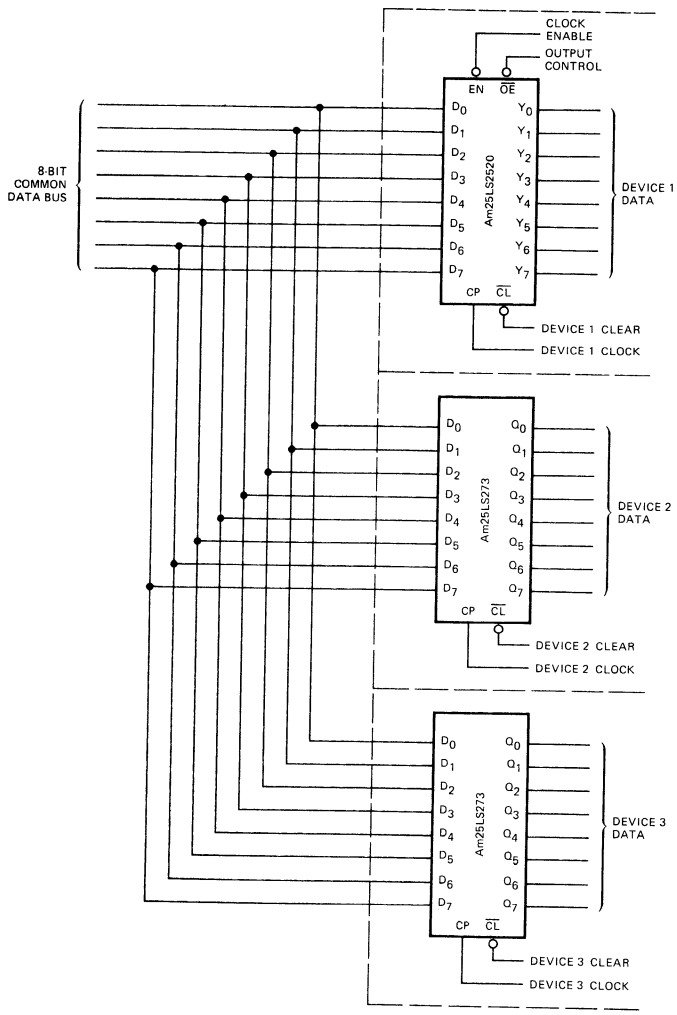



DIE SIZE 0.080" X 0.111"

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS273B Order Number | Am54LS/ 74LS273B Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS273BPC | SN74LS273BN |
| Hermetic DIP | 0°C to+70°C | AM25LS273BDC | SN74LS273BJ |
| Dice | 0°C to +70°C | AM25LS273BXC | SN74LS273BX |
| Hermetic DIP | −55°C to +125°C | AM25LS273BDM | SN54LS273BJ |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS273BFM | SN54LS273BW |
| Dice | −55°C to +125°C | AM25LS273BXM | SN54LS273BX |

## APPLICATION




Am25LS273 8-bit registers are shown used as device data input registers on a common 8-bit data bus.

# Am25LS281 • Am54LS/74LS281

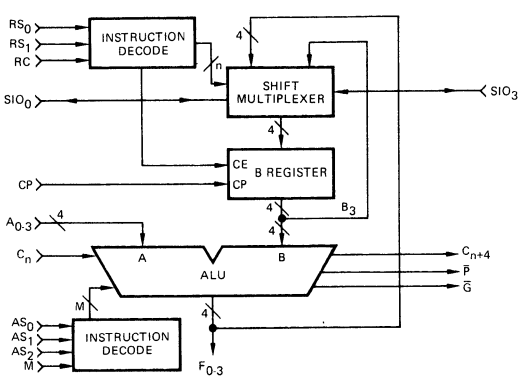
## 4-Bit Parallel Binary Accumulator

### DISTINCTIVE CHARACTERISTICS

- Four-bit binary accumulator
- Fifteen-function ALU
  - 8 arithmetic functions
  - 7 logic functions
- Edge-triggered register
- Full shifting capability
  - Logical shift up
  - Logical shift down
  - Arithmetic shift up
  - Arithmetic shift down
  - Parallel load
  - Hold
- Expandable
  - Ripple expansion with $C_n$, $C_{n+4}$
  - Look-ahead carry expansion with $\overline{P}$, $\overline{G}$, $C_n$ and Am2902 high-speed look-ahead carry generator
- No dynamic hazard
  - The Am25LS281 and Am54LS/74LS281 do not have the dynamic hazard found on the A inputs of the SN54S/74S281.

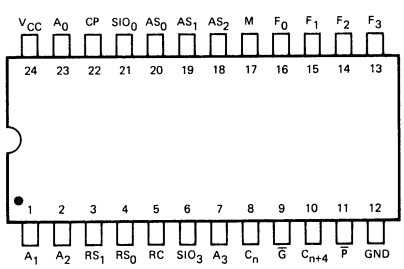
Note: The Advanced Micro Devices: LS281 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

### BLOCK DIAGRAM




### CONNECTION DIAGRAM

**Top View**




Note: Pin 1 is marked for orientation.

### FUNCTIONAL DESCRIPTION

The Am25LS281 • Am54LS/74LS281 is a four-bit parallel binary accumulator. As shown in the block diagram, it consists of an ALU, a shift multiplexer, an edge-triggered B register, and the necessary instruction decoding logic.

The ALU performs 15 functions, 8 arithmetic and 7 logical, as defined by Tables 1 and 2. All ALU operations are performed on the $A_0$-$A_3$ inputs and/or the internal B register. The 7 logical functions are performed on an individual bit basis between the $A_0$-$A_3$ inputs and the internal B register. The result of the ALU operation is available at the $F_0$-$F_3$ outputs.

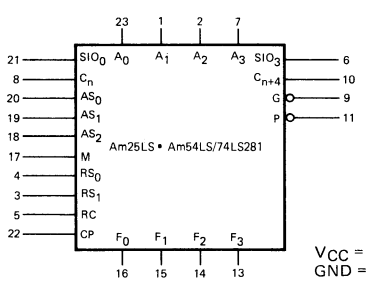
An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. In slower systems, the carry output $C_{n+4}$ can be connected to the next higher $C_n$ to provide ripple block arithmetic.

The $F_0$-$F_3$ outputs are also used as inputs to the shift multiplexer which either performs one of four shift functions on the data or passes the data unaltered. The outputs of the shift multiplexer are loaded into the internal B register on the LOW-to-HIGH transition of the clock input unless both register select inputs ($RS_0$, $RS_1$) are high. As shown in Table 3, the shift multiplexer and clock enable for the B register are controlled by the register select ($RS_0$, $RS_1$) and register control (RC) inputs. The shift multiplexer is expanded by connecting the $SIO_3$ input/output to the $SIO_0$ of the next most significant device.

The arithmetic shift functions allow the shifting of a number without effecting the sign bit, the most significant bit of the most significant device. When cascading devices, the RC input of all the devices except the most significant device should be connected to ground. The RC input of the most significant device then determines whether an arithmetic shift or a logical shift is performed on the entire word.

The ALU section of the device has been redesigned to eliminate the dynamic hazard present at the A inputs on the SN54S/74S (T.I.) device. On the AMD device, any time a function is performed using only the B register as an input, the A input is inhibited at the ALU input.

### LOGIC SYMBOL




VCC = Pin 24
GND = Pin 12

## Am25LS281

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| | | | $I_{OL}$ = 16mA ($\overline{G}$ only) | | | 0.55 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | $A_0$-$A_3$, $RS_0$, $RS_1$, RC, $SIO_0$ | | | −0.36 | mA |
| | | | CP, $SIO_3$ | | | −0.72 | |
| | | | $AS_0$-$AS_2$, M, $C_n$ | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | $A_0$-$A_3$, $RS_0$, $RS_1$, RC, $SIO_0$, $AS_0$-$AS_2$, M, $C_n$ | | | 20 | μA |
| | | | CP, $SIO_3$ | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | Clock, $SIO_0$, $SIO_3$ | | | 1.0 | mA |
| | | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | Others | | | 1.0 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 5) | $V_{CC}$ = MAX. | | | 43 | 71 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with $RS_0$, $RS_1$ in a state such that the three-state output is OFF.
5. Test Conditions: $AS_0$, $AS_1$, $AS_2$ = HIGH. $RS_0$, $RS_1$, RC, $C_n$, M, CP, $A_0$, $A_1$, $A_2$, $A_3$ = GND.

## Am25LS • Am54LS/74LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage (Clock, $SIO_0$, $SIO_3$) | −0.5V to +5.5V |
| DC Input Voltage (Others) | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## Am54LS/74LS281
## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8.0mA | | | 0.5 | |
| | | | All, $I_{OL}$ = 16mA ($\overline{G}$ only) | | | 0.55 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | $A_0$-$A_3$, $RS_0$, $RS_1$, RC, $SIO_0$ | | | −0.36 | mA |
| | | | CP, $SIO_3$ | | | −0.72 | |
| | | | $AS_0$-$AS_2$, M, $C_n$ | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | $A_0$-$A_3$, $RS_0$, $RS_1$, RC, $SIO_0$, $AS_0$-$AS_2$, M, $C_n$ | | | 20 | μA |
| | | | CP, $SIO_3$ | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX. $V_{IN}$ = 5.5V | Clock, $SIO_0$, $SIO_3$ | | | 1.0 | mA |
| | | $V_{IN}$ = 7.0V | Others | | | 1.0 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 5) | $V_{CC}$ = MAX. | | | 43 | 71 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C, ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with $RS_0$, $RS_1$ in a state such that the three-state output is OFF.
5. Test Conditions: $AS_0$, $AS_1$, $AS_2$ = HIGH. $RS_0$, $RS_1$, RS, $C_n$, M, CP, $A_0$, $A_1$, $A_2$, $A_3$ = GND.

3

### DEFINITION OF FUNCTIONAL TERMS

**$A_0$, $A_1$, $A_2$, $A_3$** The A data inputs to the ALU.

**$AS_0$, $AS_1$, $AS_2$** The control inputs used to determine the arithmetic or logic function performed by the ALU.

**$F_0$, $F_1$, $F_2$, $F_3$** The data outputs of the ALU.

**M** The mode control input used to select either the arithmetic or logic operations of the ALU.

**$C_n$** The carry-in input of the ALU.

**$C_{n+4}$** The carry-look-ahead output of the four-bit field.

**$\overline{G}$** The carry-generate output for use in multi-level look-ahead schemes.

**$\overline{P}$** The carry-propagate output for use in multi-level look-ahead schemes.

**$RS_0$, $RS_1$, RC** The control inputs used to determine the shift function performed by the shift multiplexer and generate the clock enable signal for the B register.

**$SIO_0$** The low order serial input/output used to expand the shift multiplexer.

**$SIO_3$** The high order serial input/output used to expand the shift multiplexer.

**CP** The clock input. The internal B register is loaded on the low-to-high transition of the clock input.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ to $C_{n+4}$ | | | 16 | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 15 | | | | | | |
| $t_{PLH}$ | $A_0$-$A_3$ to $C_{n+4}$ | | | 25 | | | | | ns | |
| $t_{PHL}$ | | | | 23 | | | | | | |
| $t_{PLH}$ | $C_n$ to $F_0$-$F_3$ | | | 34 | | | | | ns | |
| $t_{PHL}$ | | | | 28 | | | | | | |
| $t_{PLH}$ | $A_0$-$A_3$ to $\overline{G}$ | | | 18 | | | | | ns | |
| $t_{PHL}$ | | | | 17 | | | | | | |
| $t_{PLH}$ | $A_0$-$A_3$ to $\overline{P}$ | | | 21 | | | | | ns | |
| $t_{PHL}$ | | | | 23 | | | | | | |
| $t_{PLH}$ | $A_n$ to $F_n$ | | | 29 | | | | | ns | |
| $t_{PHL}$ | | | | 23 | | | | | | |
| $t_{PLH}$ | $A_0$ to $SIO_0$ | | | 38 | | | | | ns | |
| $t_{PHL}$ | | | | 36 | | | | | | |
| $t_{PLH}$ | $A_2$, $A_3$ to $SIO_3$ | | | 39 | | | | | ns | |
| $t_{PHL}$ | | | | 36 | | | | | | |
| $t_{PLH}$ | $F_0$ to $SIO_0$ | | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | | |
| $t_{PLH}$ | $F_2$, $F_3$ to $SIO_3$ | | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | | |
| $t_{PLH}$ | RC to $SIO_3$ | | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $F_0$-$F_3$ | | | 40 | | | | | ns | |
| $t_{PHL}$ | | | | 33 | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $C_{n+4}$ | | | 41 | | | | | ns | |
| $t_{PHL}$ | | | | 40 | | | | | | |
| $t_s$ | $A_0$-$A_3$ to CP | | | | | | | | ns | |
| $t_h$ | | | | | | | | | | |
| $t_s$ | $C_n$ to CP | | | | | | | | ns | |
| $t_h$ | | | | | | | | | | |
| $t_s$ | $AS_0$-$AS_2$, M to CP | | | | | | | | ns | |
| $t_h$ | | | | | | | | | | |
| $t_s$ | $SIO_0$ to CP | | | | | | | | ns | |
| $t_h$ | | | | | | | | | | |
| $t_s$ | $SIO_3$ to CP | | | | | | | | ns | |
| $t_h$ | | | | | | | | | | |
| $t_s$ | $RS_0$, $RS_1$, RC to CP | | | | | | | | ns | |
| $t_h$ | | | | | | | | | | |
| $t_{pw}$ | CP Pulse Width | HIGH | | | | | | | ns | |
| | | LOW | | | | | | | | |
| $f_{max}$ (Note 1) | Clock Frequency (Shift Mode) | | | | | | | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{ZH}$ | $RS_0$, $RS_1$ to $SIO_0$ | | 9 | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{ZL}$ | | | 8 | | | | | | |
| $t_{HZ}$ | | | 29 | | | | | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 18 | | | | | | |
| $t_{ZH}$ | $RS_0$, $RS_1$ to $SIO_3$ | | 9 | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{ZL}$ | | | 8 | | | | | | |
| $t_{HZ}$ | | | 25 | | | | | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 17 | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $\overline{P}$ | | 32 | | | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 30 | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $\overline{G}$ | | 33 | | | | | ns | |
| $t_{PHL}$ | | | 32 | | | | | | |
| $t_{PLH}$ | CP to $F_0$-$F_3$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CP to $C_{n+4}$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CP to $\overline{P}$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CP to $\overline{G}$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CP to $SIO_0$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | CP to $SIO_3$ | | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | | |

3

## FUNCTION TABLES

### TABLE1
### ARITHMETIC FUNCTIONS
Mode Control (M) = Low

| ALU SELECTION $AS_2$ | $AS_1$ | $AS_0$ | ACTIVE-HIGH DATA $C_n$ = H (with carry) | $C_n$ = L (no carry) |
|---|---|---|---|---|
| L | L | L | $F_0$ = L, $F_1$ = $F_2$ = $F_3$ = H | $F_n$ = H |
| L | L | H | F = B Minus A | F = B Minus A Minus 1 |
| L | H | L | F = A Minus B | F = A Minus B Minus 1 |
| L | H | H | F = A Plus B Plus 1 | F = A Plus B |
| H | L | L | F = B Plus 1 | $F_n = B_n$ |
| H | L | H | F = $\overline{B}$ Plus 1 | $F_n = \overline{B}_n$ |
| H | H | L | F = A Plus 1 | $F_n = A_n$ |
| H | H | H | F = $\overline{A}$ Plus 1 | $F_n = \overline{A}_n$ |

### TABLE 2
### LOGIC FUNCTIONS
Mode Control (M) = High
Carry Input ($C_n$) = X (Irrelevant)

| ALU SELECTION $AS_2$ | $AS_1$ | $AS_0$ | ACTIVE-HIGH DATA FUNCTION |
|---|---|---|---|
| L | L | L | $F_n = L$ |
| L | X | H | $F_n = \overline{A_n \oplus B_n}$ |
| L | H | L | $F_n = \overline{A_n \oplus B_n}$ |
| H | L | L | $F_n = \overline{A_n B_n}$ |
| H | L | H | $F_n = \overline{A_n + B_n}$ |
| H | H | L | $F_n = \overline{A_n B_n}$ |
| H | H | H | $F_n = A_n + B_n$ |

### TABLE 3
### SHIFT MODE FUNCTIONS

| REG. SEL. INPUTS $RS_1$ | $RS_0$ | RC | OPERATION | B REGISTER AFTER L → H CLOCK TRANSITION $Q_{B0}$ | $Q_{B1}$ | $Q_{B2}$ | $Q_{B3}$ | SERIAL INPUTS/OUTPUTS $SIO_0$ | $SIO_3$ |
|---|---|---|---|---|---|---|---|---|---|
| L | L | X | Load B Reg. (F → B) | $f_0$ | $f_1$ | $f_2$ | $f_3$ | Z | Z |
| L | H | L | Shift Up (2F → B) | $SIO_0$ | $f_0$ | $f_1$ | $f_2$ | Z | $F_3$ |
| L | H | H | Arith. Shift Up | $SIO_0$ | $f_0$ | $f_1$ | $B_3$ | Z | $F_2$ |
| H | L | L | Shift Down (F/2 → B) | $f_1$ | $f_2$ | $f_3$ | $SIO_3$ | $F_0$ | Z |
| H | L | H | Arith. Shift Down | $f_1$ | $f_2$ | $SIO_3$ | $B_3$ | $F_0$ | Z |
| H | H | X | Hold | $B_0$ | $B_1$ | $B_2$ | $B_3$ | Z | Z |

$Q_{Bn}$ = Output of the B register (internal).
$f_n$ = Quiescent state of $F_n$ output prior to L → H CP transition.
$B_n$ = Quiescent state of $Q_{Bn}$ output prior to L → H CP transition.
Z = High impedance state (output OFF).

## Am25LS ONLY
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min. | Am25LS COM'L Max. | Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ to $C_{N+4}$ | | | | | | ns | $C_L = 50pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $A_0$-$A_3$ to $C_{n+4}$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $C_n$ to $F_0$-$F_3$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $A_0$-$A_3$ to $\overline{G}$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $A_0$-$A_3$ to $\overline{P}$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $A_n$ to $F_n$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $A_0$ to $SIO_0$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $A_2$, $A_3$ to $SIO_3$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $F_0$ to $SIO_0$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $F_2$, $F_3$ to $SIO_3$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | RC to $SIO_3$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $F_0$-$F_3$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $C_{n+4}$ | | | | | | ns | |
| $t_{PHL}$ | | | | | | | | |
| $t_s$ | $A_0$-$A_3$ to CP | | | | | | ns | |
| $t_h$ | | | | | | | | |
| $t_s$ | $C_n$ to CP | | | | | | ns | |
| $t_h$ | | | | | | | | |
| $t_s$ | $AS_0$-$AS_2$, M to CP | | | | | | ns | |
| $t_h$ | | | | | | | | |
| $t_s$ | $SIO_0$ to CP | | | | | | ns | |
| $t_h$ | | | | | | | | |
| $t_s$ | $SIO_3$ to CP | | | | | | ns | |
| $t_h$ | | | | | | | | |
| $t_s$ | $RS_0$, $RS_1$, RC to CP | | | | | | ns | |
| $t_h$ | | | | | | | | |
| $t_{pw}$ | CP Pulse Width | HIGH | | | | | ns | |
| | | LOW | | | | | | |
| $f_{Max.}$ | Clock Frequency (Shift Mode) | | | | | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min. | Am25LS COM'L Max. | Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{ZH}$ | $RS_0$, $RS_1$ to $SIO_0$ | | | | | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{ZL}$ | | | | | | | |
| $t_{HZ}$ | | | | | | ns | $C_L = 5.0pF$, $R_L = 2.0k\Omega$ |
| $t_{LZ}$ | | | | | | | |
| $t_{ZH}$ | $RS_0$, $RS_1$ to $SIO_3$ | | | | | ns | $C_L = 15pF$, $R_L = 2.0k\Omega$ |
| $t_{ZL}$ | | | | | | | |
| $t_{HZ}$ | | | | | | ns | $C_L = 5.0pF$, $R_L = 2.0k\Omega$ |
| $t_{LZ}$ | | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $\overline{P}$ | | | | | ns | $C_L = 50pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | $AS_0$-$AS_2$, M to $\overline{G}$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | CP to $F_0$-$F_3$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | CP to $C_{n+4}$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | CP to $\overline{P}$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | CP to $\overline{G}$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | CP to $SIO_0$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | CP to $SIO_3$ | | | | | ns | |
| $t_{PHL}$ | | | | | | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

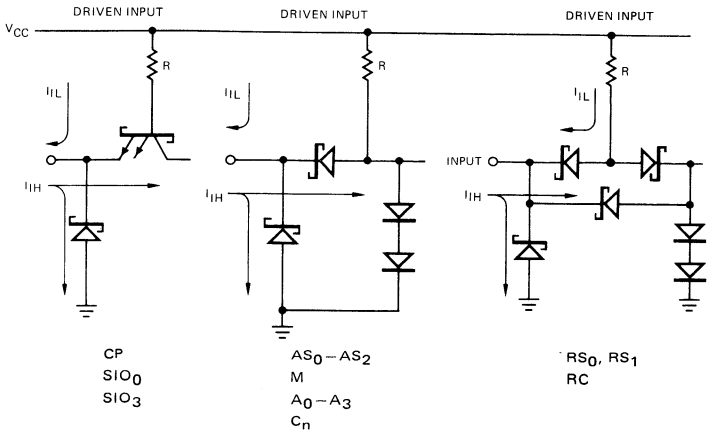
3

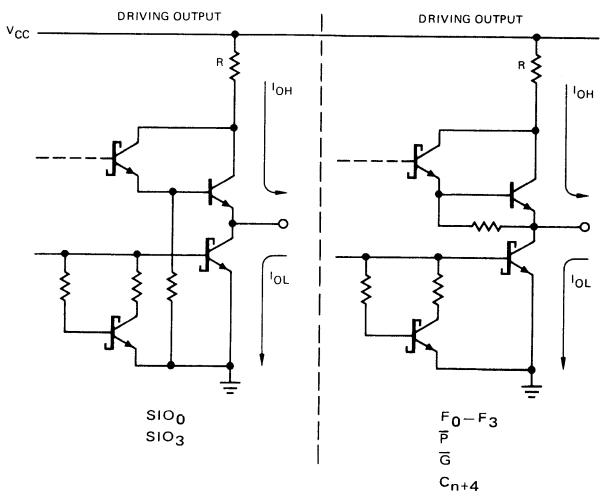
### TABLE 4. $\overline{G}$, $\overline{P}$ AND CARRY FUNCTIONS FOR OUTPUTS

| INPUTS M | $AS_2$ | $AS_1$ | $AS_0$ | DEFINITION OF TERMS $P_n$ | $G_n$ | OUTPUTS $\overline{P}$ | $\overline{G}$ | $C_{n+4}$ |
|---|---|---|---|---|---|---|---|---|
| L | L | L | L | N.A. | N.A. | L | H | $C_n$ |
| L | L | L | H | $\overline{A}_n + B_n$ | $\overline{A}_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| L | L | H | L | $A_n + \overline{B}_n$ | $A_n \cdot \overline{B}$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| L | L | H | H | $A_n + B_n$ | $A_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| L | H | L | L | $B_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| L | H | L | H | $\overline{B}_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| L | H | H | L | $A_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| L | H | H | H | $\overline{A}_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| H | L | L | L | N.A. | N.A. | L | H | $C_n$ |
| H | L | L | H | $\overline{A}_n + B_n$ | $\overline{A}_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| H | L | H | L | $A_n + B_n$ | $A_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| H | L | H | H | $\overline{A}_n + B_n$ | $\overline{A}_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| H | H | L | L | N.A. | $A_n \cdot B_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |
| H | H | L | H | N.A. | $\overline{A}_n \cdot \overline{B}_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |
| H | H | H | L | N.A. | $A_n \cdot B_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |
| H | H | H | H | N.A. | $\overline{A}_n \cdot \overline{B}_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |

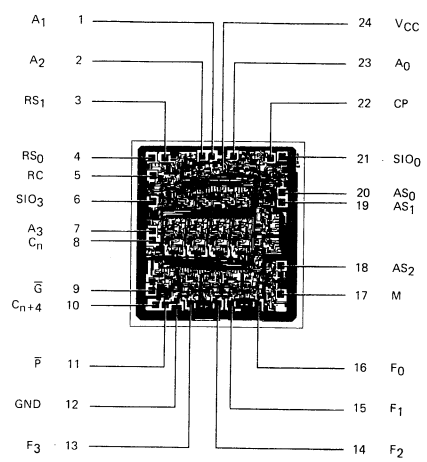
N.A. = Not Applicable.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




## Metallization and Pad Layout

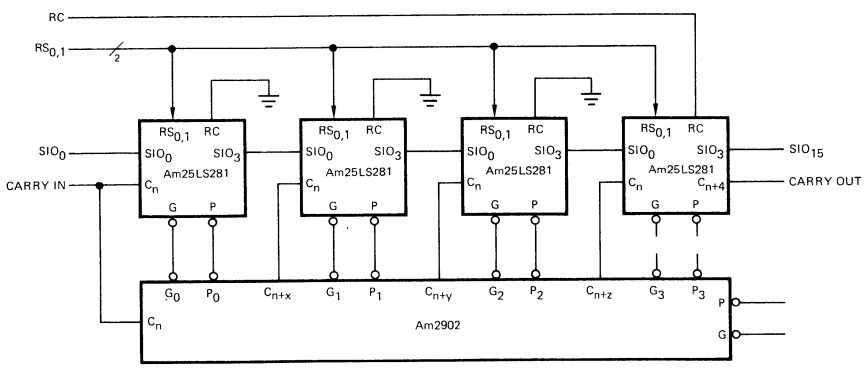



DIE SIZE 0.111" X 0.121"

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS281 Order Number | Am54LS/ 74LS281 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS281PC | SN74LS281N |
| Hermetic DIP | 0°C to +70°C | AM25LS281DC | SN74LS281J |
| Dice | 0°C to +70°C | AM25LS281XC | SN74LS281X |
| Hermetic DIP | −55°C to +125°C | AM25LS281DM | SN54LS281J |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS281FM | SN54LS281W |
| Dice | −55°C to +125°C | AM25LS281XM | SN54LS281X |

## APPLICATION




**16-Bit Binary ALU/Accumulator with Full Look-Ahead Carry.**

## TABLE 4. $\overline{G}$, $\overline{P}$ AND CARRY FUNCTIONS FOR OUTPUTS

| INPUTS | | | | DEFINITION OF TERMS | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|
| M | $AS_2$ | $AS_1$ | $AS_0$ | $P_n$ | $G_n$ | $\overline{P}$ | $\overline{G}$ | $C_{n+4}$ |
| L | L | L | L | N.A. | N.A. | L | H | $C_n$ |
| L | L | L | H | $\overline{A}_n + B_n$ | $\overline{A}_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| L | L | H | L | $A_n + \overline{B}_n$ | $A_n \cdot \overline{B}$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| L | L | H | H | $A_n + B_n$ | $A_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| L | H | L | L | $B_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| L | H | L | H | $\overline{B}_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| L | H | H | L | $A_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| L | H | H | H | $\overline{A}_n$ | N.A. | $\overline{P_3P_2P_1P_0}$ | H | $P \cdot C_n$ |
| H | L | L | L | N.A. | N.A. | L | H | $C_n$ |
| H | L | L | H | $\overline{A}_n + B_n$ | $\overline{A}_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| H | L | H | L | $A_n + B_n$ | $A_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| H | L | H | H | $\overline{A}_n + B_n$ | $\overline{A}_n \cdot B_n$ | $\overline{P_3P_2P_1P_0}$ | $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$ | $G + P \cdot C_n$ |
| H | H | L | L | N.A. | $A_n \cdot B_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |
| H | H | L | H | N.A. | $\overline{A}_n \cdot \overline{B}_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |
| H | H | H | L | N.A. | $A_n \cdot B_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |
| H | H | H | H | N.A. | $\overline{A}_n \cdot \overline{B}_n$ | L | $\overline{G_3 + G_2 + G_1 + G_0}$ | $G + C_n$ |

N.A. = Not Applicable.

# Am25LS299 • Am54LS/74LS299

## 8-Bit Universal Shift/Storage Register

### DISTINCTIVE CHARACTERISTICS

- Four operational modes: shift left, shift right, parallel load, hold
- Common input/output pins
- Three-state outputs
- Buffered asynchronous master clear
- Separate shift right serial input and shift left serial input for easy cascadability
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

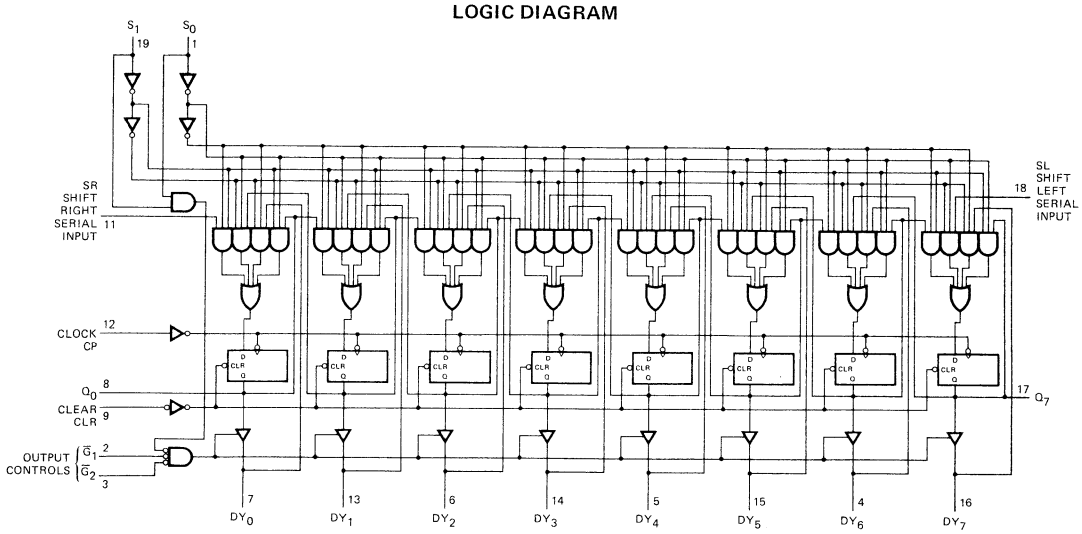
The Am25LS299 and Am54LS/74LS299 are eight-bit universal shift/storage registers with three-state outputs. Four modes of operation are possible: hold (store), shift left, shift right, and load data.

Parallel load inputs and register outputs are multiplexed to reduce the total number of package pins. Separate continuous outputs are also provided for flip-flop A and H. These devices can be cascaded to N-bit words easily.

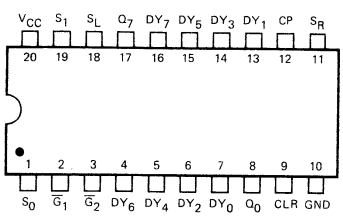
A separate active low asynchronous clear input is used to reset the register. Whenever the clear input is LOW, all internal flip-flops are set LOW independent of all other inputs. See the Am25LS23 for the identical logic function to the Am25LS299 and Am54LS/74LS299, but with synchronous clear capability.

Note: The Advanced Micro Devices' LS299 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

### LOGIC DIAGRAM

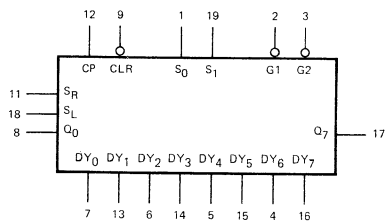



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## Am25LS299

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $Q_0, Q_7$ | $I_{OH}$ = −440μA | MIL | 2.5 | | | Volts |
| | | | | | COM'L | 2.7 | | | |
| | | | $DY_0$–$DY_7$ | MIL, $I_{OH} = -1.0mA$ | | 2.4 | | | |
| | | | | COM'L, $I_{OH} = -2.6mA$ | | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | | $I_{OL} = 4.0mA$ | | | 0.25 | 0.4 | Volts |
| | | | | $I_{OL} = 8.0mA$ | | | 0.35 | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | MIL | | | 0.7 | Volts |
| | | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | $S_0, S_1$ | | | −0.8 | mA |
| | | | | | All Others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current (Except $DY_i$) | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | $S_0, S_1$ | | | 40 | μA |
| | | | | | All Others | | | 20 | |
| $I_I$ | Input HIGH Current (Except $DY_i$) | $V_{CC}$ = MAX., | $V_{IN} = 7.0V$ | $S_0, S_1$ | | | | 0.2 | μA |
| | | | | $\overline{G}_1, \overline{G}_2$, CLR, CP | | | | 0.1 | |
| | | | $V_{IN} = 5.5V$ | All Others | | | | 0.1 | |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current at $DY_i$ | $V_{CC}$ = MAX. | | | $V_O = 0.4V$ | | | −100 | μA |
| | | | | | $V_O = 2.4V$ | | | 40 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | | 38 | 60 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ measured with clock input HIGH and output controls HIGH.

3

## Am25LS • Am54LS/74LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage ($\overline{G}_1, \overline{G}_2$, CLR, CP, $S_0, S_1$) | −0.5V to +7.0V |
| DC Input Voltage (Others) | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

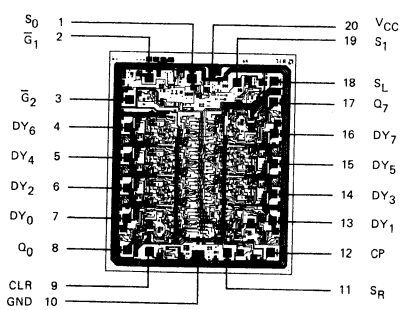
| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $Q_0, Q_7$ | $I_{OH}$ = −400 µA MIL | 2.5 | | | Volts |
| | | | | $I_{OH}$ = −400 µA COM'L | 2.7 | | | |
| | | | $DY_0$–$DY_7$ | MIL, $I_{OH}$ = −1.0mA | 2.4 | | | |
| | | | | COM'L, $I_{OH}$ = −2.6mA | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | | $I_{OL}$ = 4.0mA | | 0.25 | 0.4 | Volts |
| | | | | $I_{OL}$ = 8.0mA 74LS only | | 0.35 | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | $S_0, S_1$ | | | −0.8 | mA |
| | | | | All Others | | | −0.4 | |
| $I_{IH}$ | Input HIGH Current (Except $DY_i$) | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | $S_0, S_1$ | | | 40 | µA |
| | | | | All Others | | | 20 | |
| $I_I$ | Input HIGH Current (Except $DY_i$) | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | $S_0, S_1$ | | | 0.2 | mA |
| | | | | All Others | | | 0.1 | |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current at $DY_i$ | $V_{CC}$ = MAX. | | $V_O$ = 0.4 V | | | −100 | µA |
| | | | | $V_O$ = 2.4 V | | | 40 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 35 | 60 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ measured with clock input HIGH and output controls HIGH.

## DEFINITION OF FUNCTIONAL TERMS

| | |
|---|---|
| $S_R$ | Shift right data input to $Q_0$ |
| $S_L$ | Shift left data input to $Q_7$ |
| Clear | Active LOW synchronous input forcing the $Q_0$ through $Q_7$ register to see LOW conditions, visable only if outputs are enabled |
| Clock | A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition |
| $S_0, S_1$ | Mode selection control lines used to control input (output during load) conditions |
| $\overline{G}_1, \overline{G}_2$ | Active LOW input to control three-state output in active LOW AND configuration |
| $Q_0, Q_7$ | The only two direct outputs; used to cascade shift operations |
| $DY_0$–$DY_7$ | Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($G_1$, $G_2$). |

### Metallization and Pad Layout




DIE SIZE 0.096" X 0.112"

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Q_i$ | | 18 | 26 | | | 30 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 22 | 28 | | | 34 | | |
| $t_{PLH}$ | Clock to $DY_i$ | | 18 | 26 | | | 30 | ns | |
| $t_{PHL}$ | | | 22 | 28 | | | 34 | | |
| $t_{PHL}$ | Clear to $DY_0$ - $DY_7$ | | 25 | 35 | | | 35 | ns | |
| $t_{PHL}$ | Clear to $Q_0$ or $Q_7$ | | 25 | 35 | | | 35 | ns | |
| $t_{pw}$ | Pulse Width (Clock) | 15 | | | 20 | | | ns | |
| $t_s$ | $S_1$, $S_0$ Set-up Time | 12 | | | 15 | | | ns | |
| $t_s$ | $DY_i$ or $S_R$, $S_L$ Data Set-up Time | 12 | | | 15 | | | ns | |
| $t_h$ | Hold Time | 3.0 | | | 3.0 | | | ns | |
| $t_{ZH}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 20 | 30 | | | 40 | ns | |
| $t_{ZL}$ | | | 20 | 30 | | | 40 | | |
| $t_{LZ}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 22 | 33 | | | 40 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{HZ}$ | | | 15 | 23 | | | 30 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 30 | 45 | | 25 | | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

3

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Q_i$ | | 38 | | 44 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 41 | | 47 | | |
| $t_{PLH}$ | Clock to $DY_i$ | | 38 | | 44 | ns | |
| $t_{PHL}$ | | | 41 | | 47 | | |
| $t_{PHL}$ | Clear to $DY_0$ - $DY_7$ | | 50 | | 57 | ns | |
| $t_{PHL}$ | Clear to $Q_0$ - $Q_7$ | | 50 | | 57 | ns | |
| $t_{pw}$ | Pulse Width (Clock) | 24 | | 27 | | ns | |
| $t_s$ | $S_1$, $S_0$ Set-up Time | 20 | | 23 | | ns | |
| $t_s$ | $DY_i$ or $S_R$, $S_L$ Data Set-up Time | 20 | | 23 | | ns | |
| $t_h$ | Hold Time | 8 | | 9 | | ns | |
| $t_{ZH}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 43 | | 50 | ns | |
| $t_{ZL}$ | | | 43 | | 50 | | |
| $t_{LZ}$ | $S_1$, $S_0$, $\overline{G}_1$, $\overline{G}_2$ to $DY_i$ | | 43 | | 50 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{HZ}$ | | | 34 | | 39 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 23 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

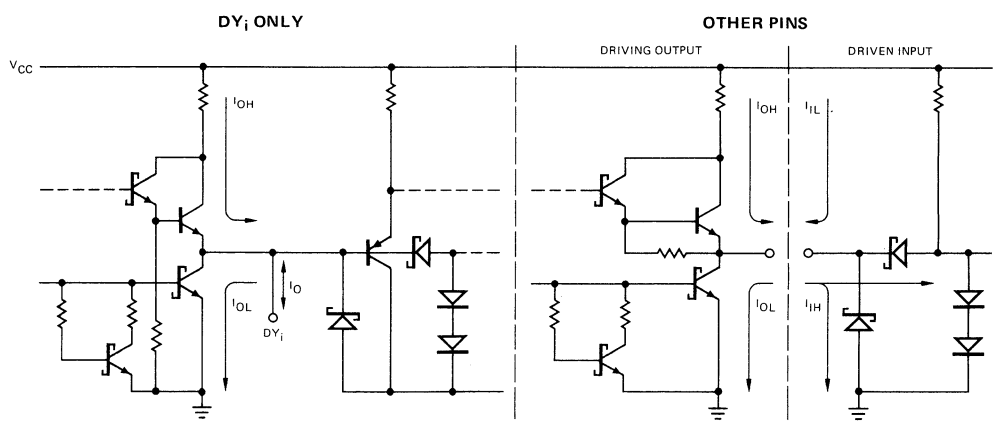
## TRUTH TABLE

| FUNCTION | | INPUTS | | | | | | | | OUTPUTS | | INPUTS/OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $S_R$ | $S_L$ | CLEAR | CLOCK | $S_0$ | $S_1$ | $\overline{G}_1$ | $\overline{G}_2$ | $Q_0$ | $Q_7$ | $DY_0$ | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ | $DY_7$ |
| Clear | | X | X | L | X | (Note 1) | | L | L | L | L | L | L | L | L | L | L | L | L |
| Output Control | | X | X | X | X | X | X | H | L | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |
| | | X | X | X | X | X | X | L | H | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |
| | | X | X | X | X | X | X | H | H | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |
| M O D E | Hold | X | X | H | X | L | L | L | L | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC |
| | Load (Note 2) | X | X | H | ↑ | H | H | L | L | A | H | A | B | C | D | E | F | G | H |
| | Shift Right | L | X | H | ↑ | H | L | L | L | L | $DY_6$ | L | $DY_0$ | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ |
| | Shift Right | H | X | H | ↑ | H | L | L | L | H | $DY_6$ | H | $DY_0$ | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ |
| | Shift Left | X | L | H | ↑ | L | H | L | L | $DY_1$ | L | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ | $DY_7$ | L |
| | Shift Left | X | H | H | ↑ | L | H | L | L | $DY_1$ | H | $DY_1$ | $DY_2$ | $DY_3$ | $DY_4$ | $DY_5$ | $DY_6$ | $DY_7$ | H |

L = LOW  Z = High Impedance  ↑ = Transition LOW-to-HIGH
H = HIGH  X = Don't Care  NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode $DY_i$ are inputs.

### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

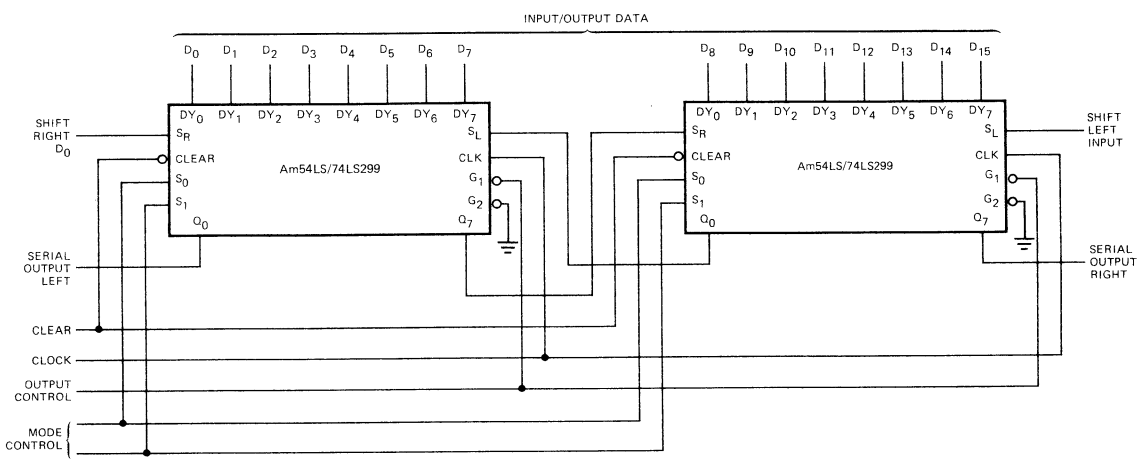



Note: Actual current flow direction shown.

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS299 Order Number | Am54LS/ 74LS299 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +75°C | AM25LS299PC | SN74LS299N |
| Hermetic DIP | 0°C to +75°C | AM25LS299DC | SN74LS299J |
| Dice | 0°C to +75°C | AM25LS299XC | SN74LS299X |
| Hermetic DIP | −55°C to +125°C | AM25LS299DM | SN54LS299J |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS299FM | SN54LS299W |
| Dice | −55°C to +125°C | AM25LS299XM | SN54LS299X |

## APPLICATION




16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

# Am25LS322 • Am54LS/74LS322

## 8-Bit Serial/Parallel Register with Sign Extend

**The 'LS322 is Texas Instruments' planned second source to Advanced Micro Devices' Am25LS22.**

**See Am25LS22 data sheet for full information.**

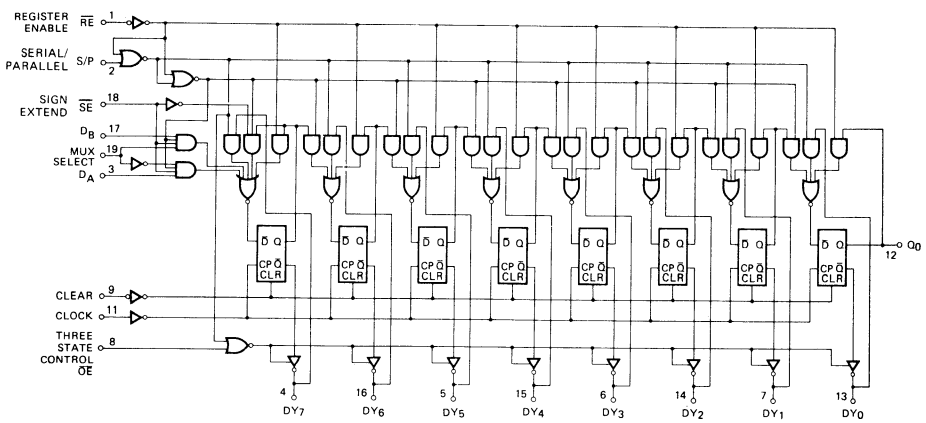
### FUNCTIONAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input $D_A$ or $D_B$. A serial output, $Q_0$, is also provided.

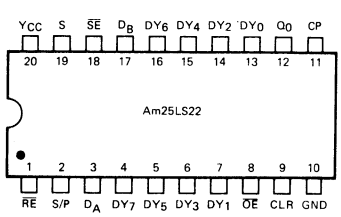
The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines ($DY_i$) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the $Q_7$ flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either $D_A$ or $D_B$ can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

### LOGIC DIAGRAM

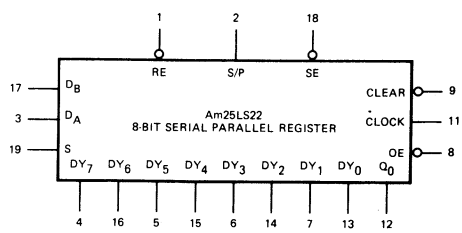



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

# Am25LS323 • Am54LS/74LS323

## 8-Bit Shift/Storage Register with Synchronous Clear

**The 'LS323 is Texas Instruments' planned second source to Advanced Micro Devices' Am25LS23.**

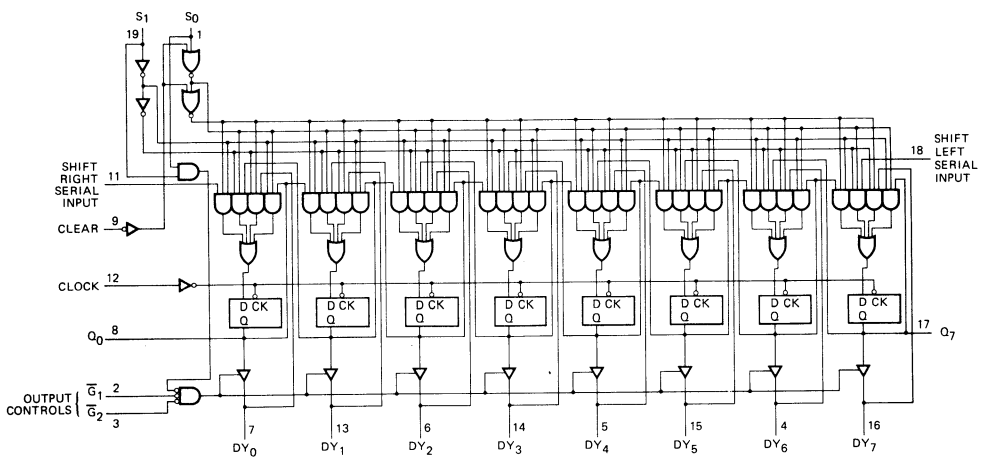
**See Am25LS23 data sheet for full information.**

### FUNCTIONAL DESCRIPTION

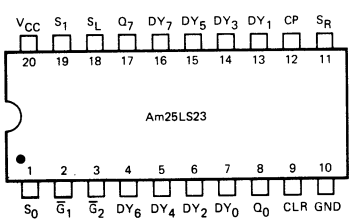
The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops $Q_0$ and $Q_7$.

Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

### LOGIC DIAGRAM

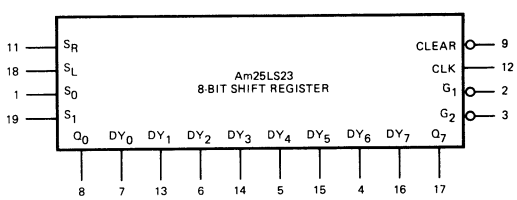



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




VCC = Pin 20
GND = Pin 10

# Am54LS/74LS348

**Three-State Priority Encoder**

**Advanced Micro Devices has no current plans to manufacture this product.**

**See the Am25LS2513 for a recommended alternative Three-State Priority Encoder offering greater functional flexibility.**

# Am25LS373 • Am54LS/74LS373

## Octal Latches with Three-State Output

### DISTINCTIVE CHARACTERISTICS

- 8 latches in a single package
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - Twice the fan-out over military range
- 100% product assurance screening to MIL-STD-883 requirements

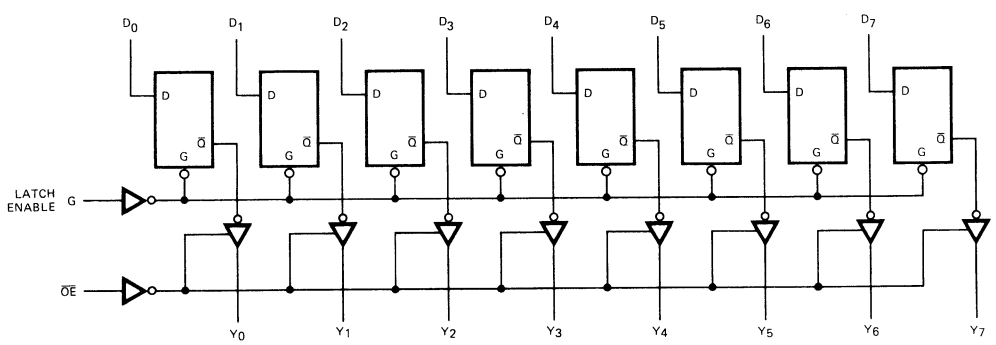
### FUNCTIONAL DESCRIPTION

The Am25LS373 and Am54LS/74LS373 are octal latches with three-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

**Note: An inverting version of this device, to be called Am54LS/74LS533, is also in development.**

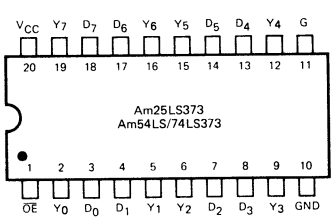
### LOGIC DIAGRAM

**Am25LS/54LS/74LS373**



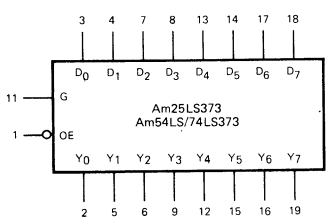

Outputs $Y_0$ through $Y_7$ are inverted on the Am25LS/54LS/74LS533.

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | | |
|---|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$ | MIL | 2.4 | 3.4 | | Volts |
| | | | $I_{OH} = -2.6mA$ | COM'L | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 12mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 24mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 24 | 40 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS373

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0$ mA | MIL | 2.4 | 3.4 | | Volts |
| | | | $I_{OH} = -2.6$mA | COM'L | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 12mA | | | 0.25 | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 24mA | | | 0.35 | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18$mA | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_O$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 24 | 40 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

3

### FUNCTION TABLE

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| OE | G | $D_i$ | $Q_i$ | $Y_i$ | |
| H | X | X | X | Z | Hi-Z |
| L | H | L | H | L | Transparent |
| L | H | H | L | H | |
| L | L | X | NC | NC | Latched |

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

### DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The latch data inputs.

**G** The latch enable input. Data is latched upon and set-up and hold times are referenced to the HIGH-to-LOW transition of G.

**$Y_i$** The three-state latch outputs.

**OE** The output enable control. When OE is LOW, the outputs $Y_i$ are enabled. When OE is HIGH, the outputs $Y_i$ are in the high impedance (off) state.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

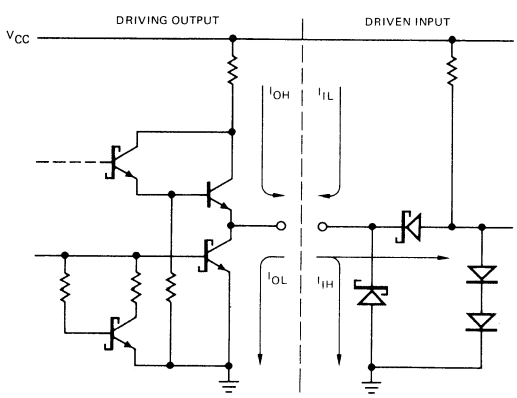
| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Enable to Output | | | | | 20 | 30 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | | | | | | 18 | 30 | | |
| $t_{PLH}$ | Data Input to Output | | | | | 12 | 18 | ns | |
| $t_{PHL}$ | | | | | | 12 | 18 | | |
| $t_s(H)$ | HIGH Data to Enable | | | | 0 | | | ns | |
| $t_s(L)$ | LOW Data to Enable | | | | 0 | | | | |
| $t_h(H)$ | HIGH Data to Enable | | | | 10 | | | ns | |
| $t_h(L)$ | LOW Data to Enable | | | | 10 | | | | |
| $t_{pw}$ | Enable Pulse Width | | | | 15 | | | ns | |
| $t_{ZH}$ | OE to $Y_i$ | | | | | 15 | 28 | ns | |
| $t_{ZL}$ | | | | | | 25 | 36 | | |
| $t_{HZ}$ | OE to $Y_i$ | | | | | 12 | 20 | ns | $C_L$ = 5pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | | | 15 | 25 | | |

## Am25LS ONLY
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Am25LS COM'L: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL: $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Enable to Output | | | | | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | | | | | | | |
| $t_{PLH}$ | Data Input to Output | | | | | ns | |
| $t_{PHL}$ | | | | | | | |
| $t_s(H)$ | HIGH Data to Enable | | | | | ns | |
| $t_s(L)$ | LOW Data to Enable | | | | | | |
| $t_h(H)$ | HIGH Data to Enable | | | | | ns | |
| $t_h(L)$ | LOW Data to Enable | | | | | | |
| $t_{pw}$ | Enable Pulse Width | | | | | ns | |
| $t_{ZH}$ | OE to $Y_i$ | | | | | ns | |
| $t_{ZL}$ | | | | | | | |
| $t_{HZ}$ | OE to $Y_i$ | | | | | ns | $C_L$ = 5pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | | | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

# Am25LS374 • Am54LS/74LS374

## 8-Bit Register With Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Eight-bit, high speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Am25LS devices offer the following improvements over Am54/74LS
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS374 and Am54LS/74LS374 are eight-bit registers built using advanced Low-Power Schottky technology. These registers consist of eight D-type flip-flops with a buffered common clock and a buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

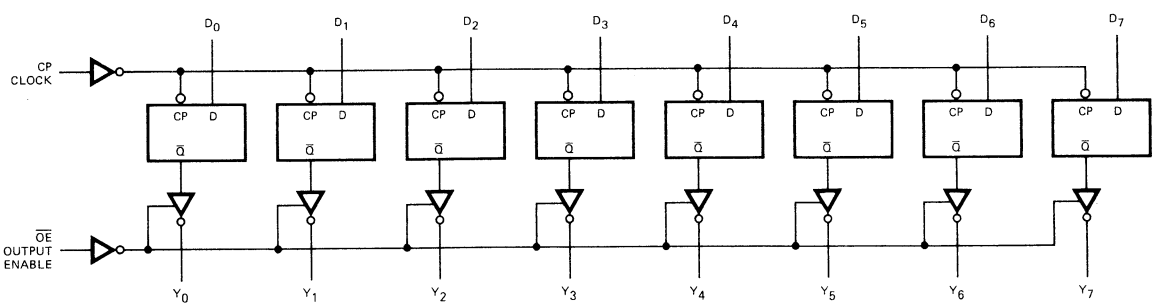
Note: The Advanced Micro Devices: LS374 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

Note: An inverting version of this device, to be called Am54LS/74LS534, is also in development.

3

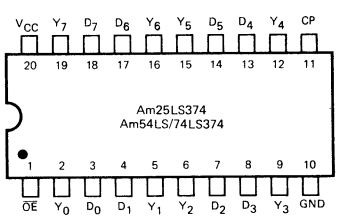
### LOGIC DIAGRAM

**Am25LS/54LS/74LS374**



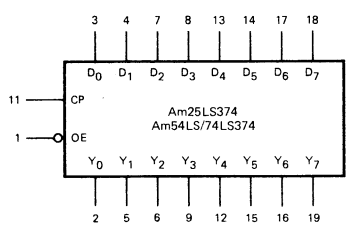

Outputs $Y_0$ through $Y_7$ are inverted on the Am25LS/54LS/74LS534.

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$, MIL | | 2.4 | 3.4 | | Volts |
| | | | $I_{OH} = -2.6mA$, COM'L | | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.7V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 27 | 45 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open; all $D_i$ inputs and $\overline{OE} = 4.5V$. Apply momentary ground, then 4.5V to clock input.

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS374

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$ | MIL | 2.4 | 3.4 | | Volts |
| | | | $I_{OH} = -2.6mA$ | COM'L | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL} = 8.0mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.5V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 27 | 45 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open; all $D_i$ inputs and $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

3

### DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The D flip-flop data inputs.

**CP** Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

**$Y_i$** The register three-state outputs.

**$\overline{OE}$** Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

### FUNCTION TABLE

| FUNCTION | INPUTS | | | INTERNAL | OUTPUTS |
|---|---|---|---|---|---|
| | $\overline{OE}$ | Clock | $D_i$ | $Q_i$ | $Y_i$ |
| Hi-Z | H | L | X | NC | Z |
| | H | H | X | NC | Z |
| LOAD REGISTER | L | ↑ | L | L | L |
| | L | ↑ | H | H | H |
| | H | ↑ | L | L | Z |
| | H | ↑ | H | H | Z |

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Y_i$ | | | 18 | 28 | | | 28 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 22 | 37 | | | 37 | | |
| $t_{PW}$ | Clock Pulse Width | LOW | 25 | | | 25 | | | ns | |
| | | HIGH | 20 | | | 20 | | | | |
| $t_s$ | Data | | 20 | | | 20 | | | ns | |
| $t_h$ | Data | | 10 | 1 | | 10 | | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 11 | 14 | | | 28 | ns | |
| $t_{ZL}$ | | | | 14 | 21 | | | 36 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 20 | 30 | | | 29 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 25 | 36 | | | 35 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 30 | 45 | | 30 | | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.



## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

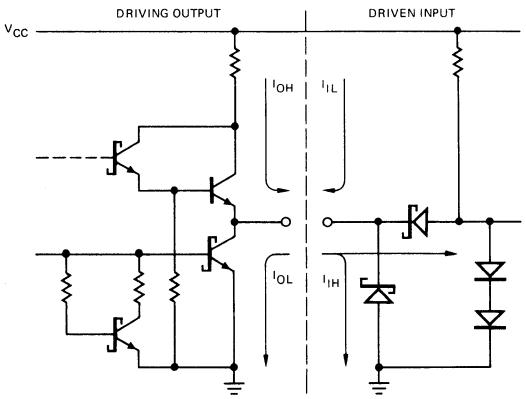
| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Y_i$ | | | 36 | | 44 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 47 | | 57 | | |
| $t_{PW}$ | Clock Pulse Width | LOW | 30 | | 35 | | ns | |
| | | HIGH | 25 | | 30 | | | |
| $t_s$ | Data | | 15 | | 20 | | ns | |
| $t_h$ | Data | | 12 | | 15 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 20 | | 25 | ns | |
| $t_{ZL}$ | | | | 30 | | 39 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 35 | | 40 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 39 | | 42 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## ORDERING INFORMATION

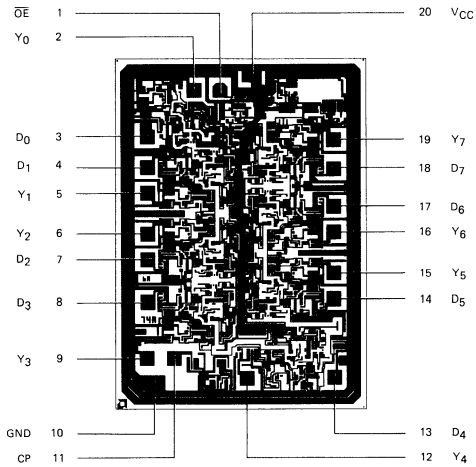
| Package Type | Temperature Range | Am25LS374 Order Number | Am54LS/74LS374 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS374PC | SN74LS374N |
| Hermetic DIP | 0°C to +70°C | AM25LS374DC | SN74LS374J |
| Dice | 0°C to +70°C | AM25LS374XC | SN74LS374X |
| Hermetic DIP | −55°C to +125°C | AM25LS374DM | SN54LS374J |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS374FM | SN54LS374W |
| Dice | −55°C to +125°C | AM25LS374XM | SN54LS374X |

## Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



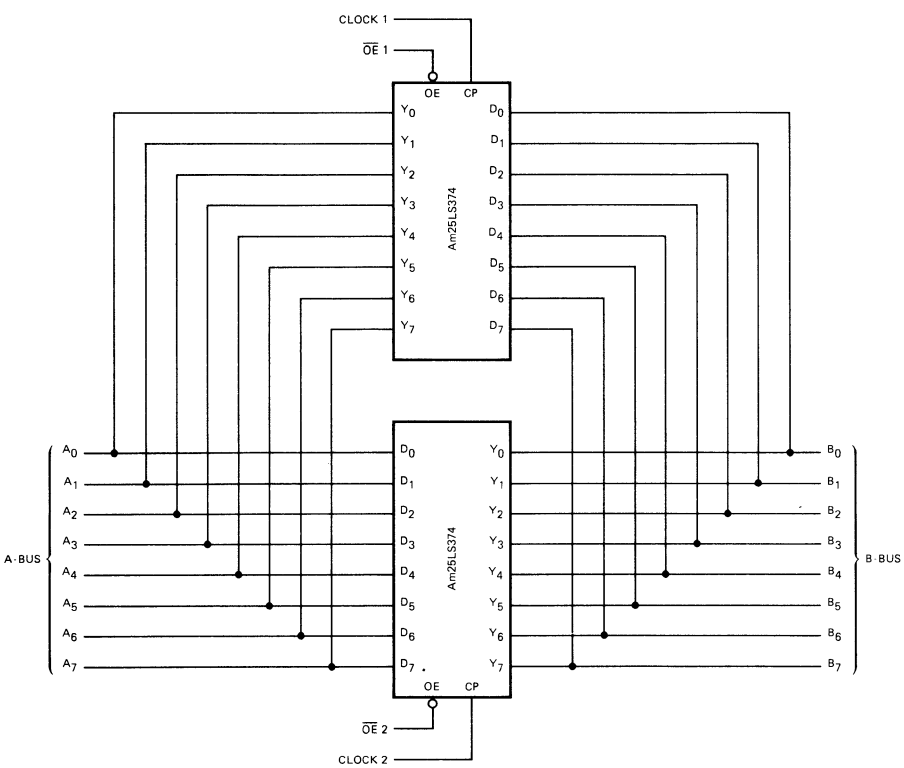

Note: Actual current flow direction shown.

## Metallization and Pad Layout




DIE SIZE 0.080" X 0.111"

## APPLICATIONS




Two Am25LS374's can be used as a bi-directional bus driver/register. The above connection shows separate clocks and three-state controls.

3

# Am25LS377B • Am54LS/74LS377B

## 8-Bit Register With Register Enable

### DISTINCTIVE CHARACTERISTICS

- Eight-bit, high speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common clock enable
- Am25LS devices offer the following improvements over Am54/74LS
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440$\mu$A source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

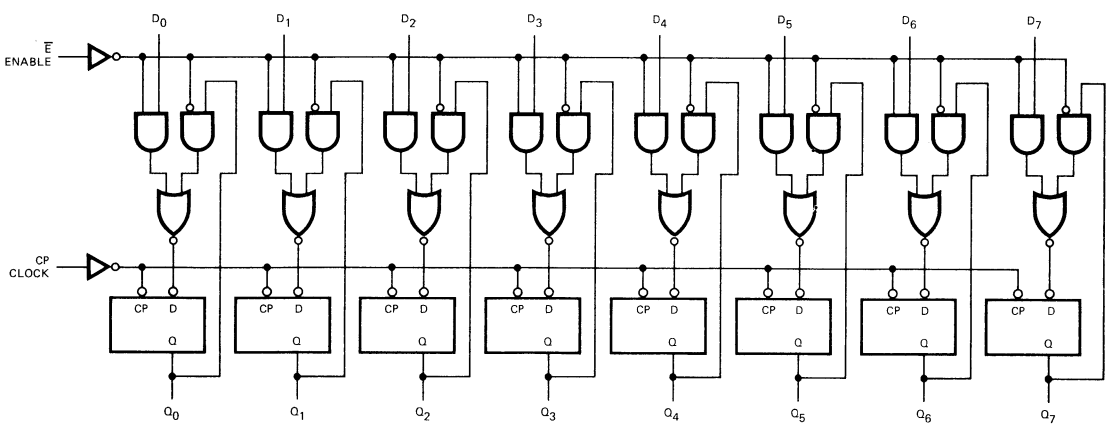
The Am25LS377B and the Am54LS/74LS377B are eight-bit registers built using advanced Low-Power Schottky technology. These registers consist of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

When the clock enable ($\overline{E}$) input is LOW, new data is entered into the flip-flop register on the LOW-to-HIGH transition of the clock input. When the ($\overline{E}$) input is HIGH, the register will retain the present data independent of the clock inputs.

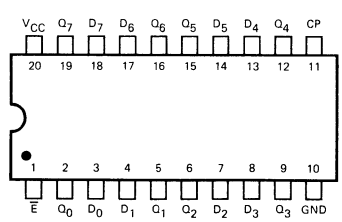
The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

**Note:** The B designation identifies buffered output versions provided to eliminate output commutation.

### LOGIC DIAGRAM

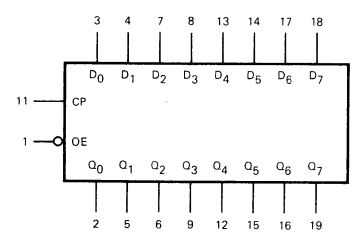



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## Am25LS377B
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | | | Volts |
| | | | COM'L | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 17 | 28 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, E = GND, all Di inputs = 4.5V. Apply momentary ground, then 4.5V to clock input.

3

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS377B
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −400μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | | | Volts |
| | | | COM'L | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 17 | 28 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, E = GND, all Di inputs = 4.5V. Apply momentary ground, then 4.5V to clock input.

### FUNCTION TABLE

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{E}$ | $D_i$ | CP | $Q_i$ |
| H | X | X | NC |
| L | X | H | NC |
| L | X | L | NC |
| L | L | ↑ | L |
| L | H | ↑ | H |

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
NC = No Change
X = Don't Care

### DEFINITION OF FUNCTIONAL TERMS

$D_i$ The D flip-flop data inputs.
$\overline{E}$ Enable. When the enable is LOW, data on the $D_i$ inputs is transferred to the $Q_i$ outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the $Q_i$ outputs do not change regardless of the data or clock input transitions.
CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
$Q_i$ The TRUE register outputs.

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 18 | 27 | | 18 | 27 | ns | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 23 | 35 | | 23 | 35 | | |
| $t_{PW}$ | Clock Pulse Width | HIGH | 20 | | | 20 | | | ns | |
| | | LOW | 25 | | | 25 | | | | |
| $t_s$ | Data | | 20 | | | 20 | | | ns | |
| $t_h$ | Data | | 10 | | | 10 | | | ns | |
| $t_s$ | Clock Enable | Active State | 25 | | | 25 | | | ns | |
| | | Inactive State | 20 | | | 20 | | | | |
| $t_h$ | Clock Enable | | 5 | | | 5 | | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 30 | 40 | | 30 | 40 | | ns | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

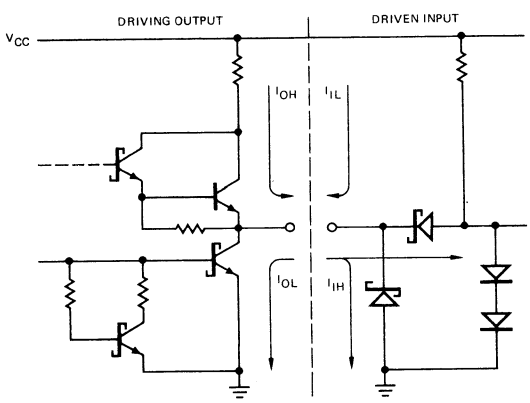
## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | | 32 | | 37 | ns | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 45 | | 54 | | |
| $t_{PW}$ | Clock Pulse Width | HIGH | 25 | | 25 | | ns | |
| | | LOW | 25 | | 30 | | | |
| $t_s$ | Data | | 20 | | 20 | | ns | |
| $t_h$ | Data | | 12 | | 15 | | ns | |
| $t_s$ | Clock Enable | Active | 27 | | 30 | | ns | |
| | | Inactive | 22 | | 25 | | | |
| $t_h$ | Clock Enable | | 5 | | 5 | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

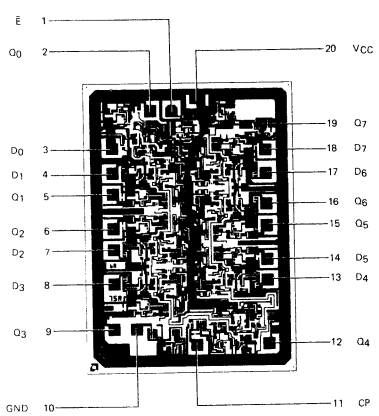
3

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



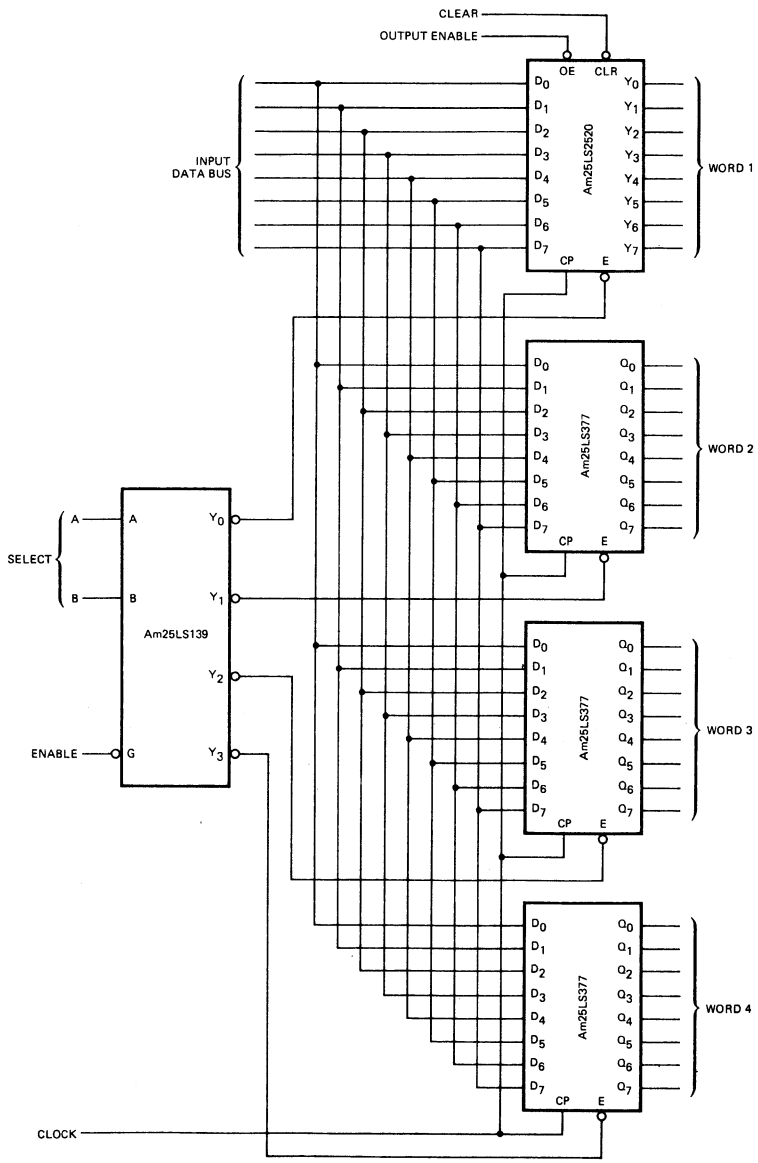

Note: Actual current flow direction shown.

### Metallization and Pad Layout




DIE SIZE 0.080" X 0.111"

## APPLICATION




Selective Register Loading of Data on Synchronous Clock.

# Am25LS378 • Am25LS379
# Am54LS/74LS378 • Am54LS/74LS379

## Hex/Quad Register With Register Enable

### DISTINCTIVE CHARACTERISTICS

- Four-bit and six-bit high-speed parallel registers
- Common clock and common register enable
- Positive edge-triggered D flip-flops
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440$\mu$A source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

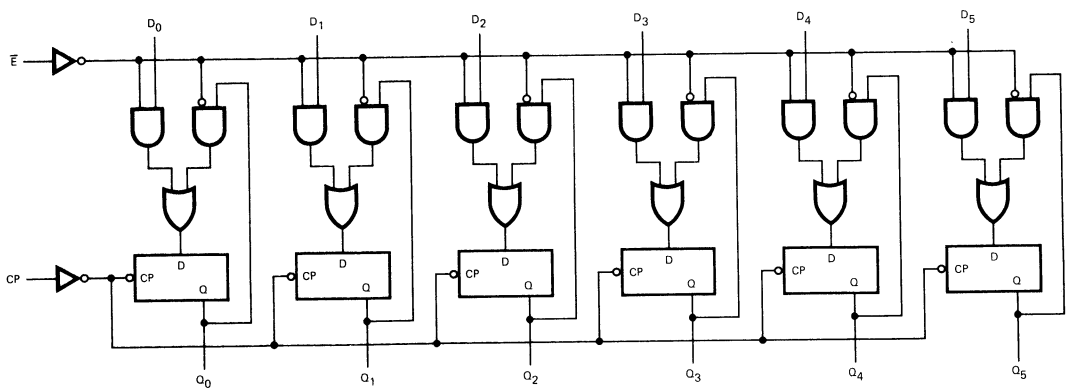
### FUNCTIONAL DESCRIPTION

These four-bit and six-bit registers are built using advanced Low-Power Schottky processing. Each register features a buffered common clock as well as a buffered common register enable. These devices are second source versions of the popular Am25LS07 and Am25LS08.

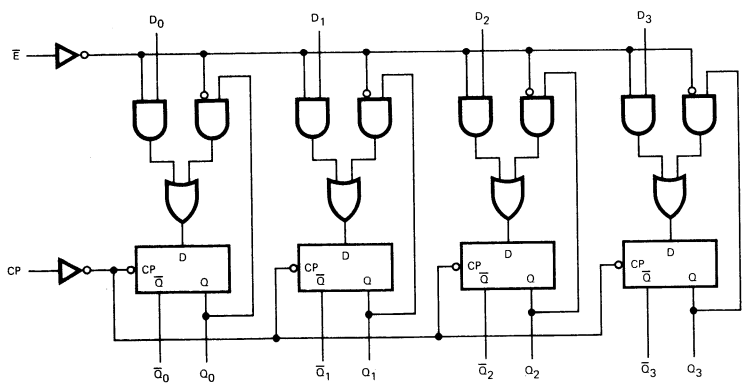
Both registers will find application in digital systems where the information is associated with a logic gating signal. They are ideally suited for a microprogrammed machine where a microprogram control bit provides the register enable signal. When the register enable is LOW, data on the D inputs is stored in the register on the LOW-to-HIGH transition of the clock. When the enable input is HIGH, the register will not change state regardless of the clock or data input transitions.

### LOGIC DIAGRAMS

**Am25LS378 • Am54LS/74LS378**



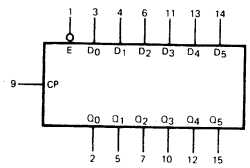

**Am25LS379 • Am54LS/74LS379**



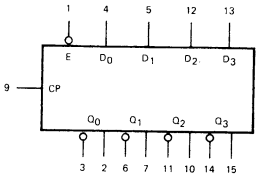

3

## LOGIC SYMBOLS

LS378



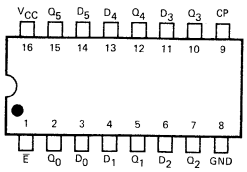

LS379



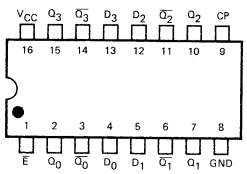

$V_{CC}$ = Pin 16
GND = Pin 8

## CONNECTION DIAGRAMS
Top Views

LS378




LS379




Note: Pin 1 is marked for orientation.

## Am25LS378 • Am25LS379

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75 V MAX. = 5.25 V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50 V MAX. = 5.50 V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −440μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | Clock, $\overline{E}$ | | | −0.36 | mA |
| | | | Others | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | Clock | | | 20 | μA |
| | | | Others | | | 14 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | LS378 | | 16 | 22 | mA |
| | | | LS379 | | 11 | 18 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS378 • Am54LS/74LS379

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75 V MAX. = 5.25 V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50 V MAX. = 5.50 V)

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −400μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | All, $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | LS378 | | 16 | 22 | mA |
| | | | LS379 | | 11 | 18 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to a clock input.

3

### DEFINITION OF FUNCTIONAL TERMS

$D_i$ The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the $D_i$ inputs is transferred to the $Q_i$ outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the $Q_i$ outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

$Q_i$ The TRUE register outputs.

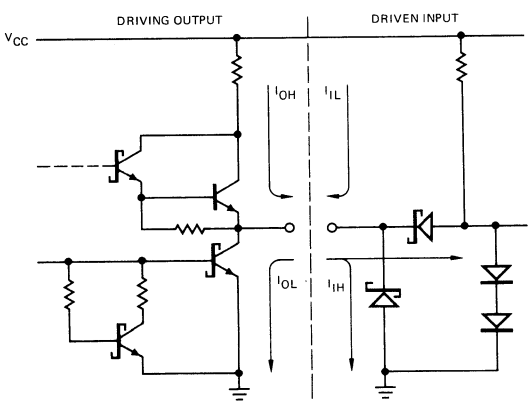
$\overline{Q}_i$ The complement register outputs

### FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{E}$ | $D_i$ | CP | $Q_i$ | $\overline{Q}_i$ |
| H | X | X | NC | NC |
| L | X | H | NC | NC |
| L | X | L | NC | NC |
| L | L | ↑ | L | H |
| L | H | ↑ | H | L |

H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on LS379 Only

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0 V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 13 | 20 | | 17 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Output | | 13 | 20 | | 18 | 27 | ns | |
| $t_{PW}$ | Clock Pulse Width | 17 | | | 20 | | | ns | |
| $t_s$ | Data | 20 | | | 20 | | | ns | |
| $t_h$ | Data | 5.0 | | | 5.0 | | | ns | |
| $t_s$ | Clock Enable | 25 | | | 25 | | | ns | |
| $t_h$ | Clock Enable | 5.0 | | | 5.0 | | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 40 | 65 | | 30 | 40 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

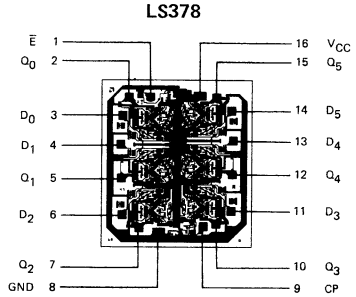
## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 30 | | 35 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | Clock to Output | | 30 | | 35 | ns | |
| $t_{PW}$ | Clock Pulse Width | 26 | | 30 | | ns | |
| $t_s$ | Data | 30 | | 35 | | ns | |
| $t_h$ | Data | 11 | | 12 | | ns | |
| $t_s$ | Clock Enable | 33 | | 38 | | ns | |
| $t_h$ | Clock Enable | 11 | | 12 | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 30 | | 26 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

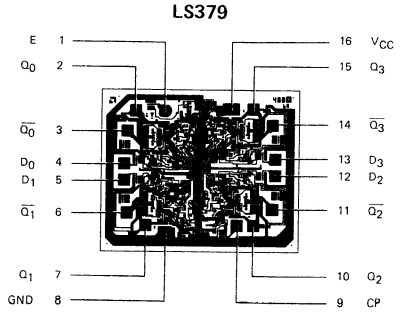
### Metallization and Pad Layout

**LS378**




DIE SIZE 0.075" X 0.084"

**LS379**

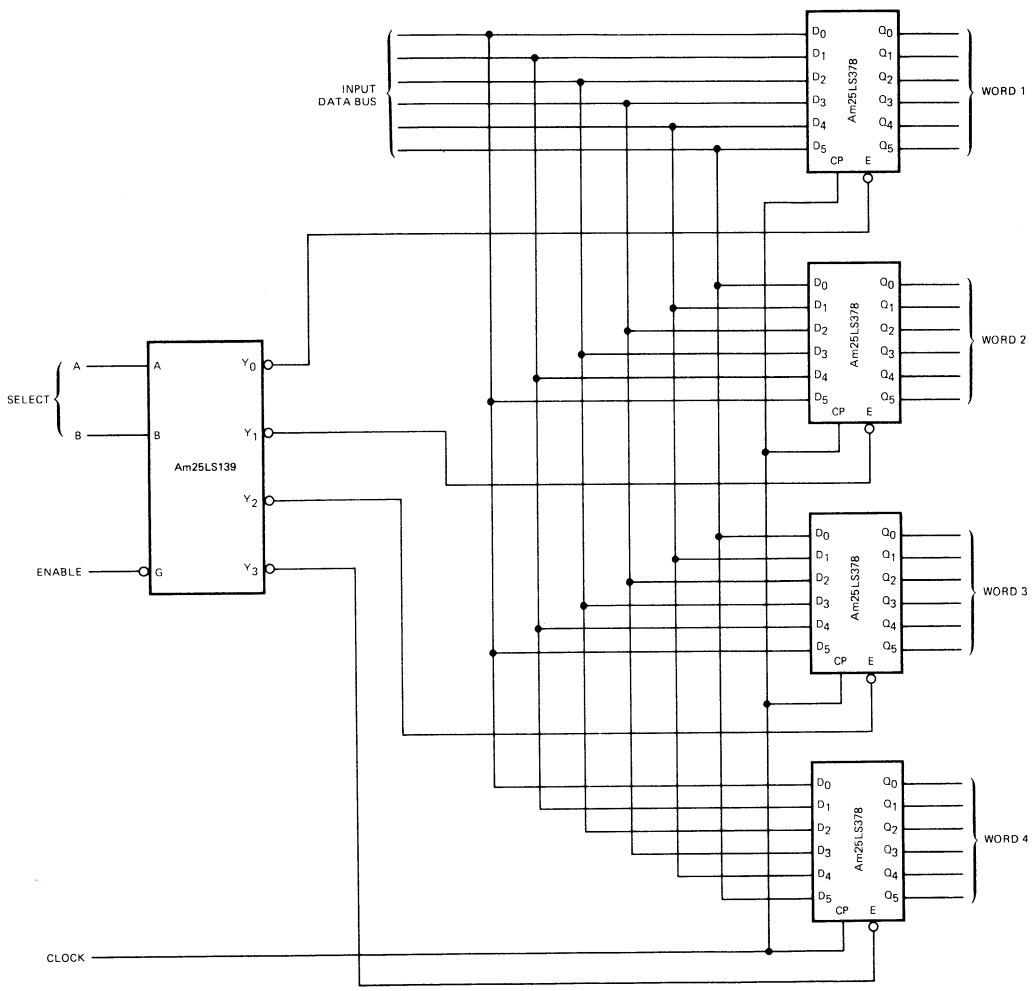



DIE SIZE 0.061" X 0.075"

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS378 Order Number | Am25LS379 Order Number | Am54LS/ 74LS378 Order Number | Am54LS/ 74LS379 Order Number |
|---|---|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS378PC | AM25LS379PC | SN74LS378N | SN74LS379N |
| Hermetic DIP | 0°C to +70°C | AM25LS378DC | AM25LS379DC | SN74LS378J | SN74LS379J |
| Dice | 0°C to +70°C | AM25LS378XC | AM25LS379XC | SN74LS378X | SN74LS379X |
| Hermetic DIP | –55°C to +125°C | AM25LS378DM | AM25LS379DM | SN54LS378J | SN54LS379J |
| Hermetic Flat Pak | –55°C to +125°C | AM25LS378FM | AM25LS379FM | SN54LS378W | SN54LS379W |
| Dice | –55°C to +125°C | AM25LS378XM | AM25LS379XM | SN54LS378X | SN54LS379X |

## APPLICATION




**Selective Register Loading of Data on Synchronous Clock.**

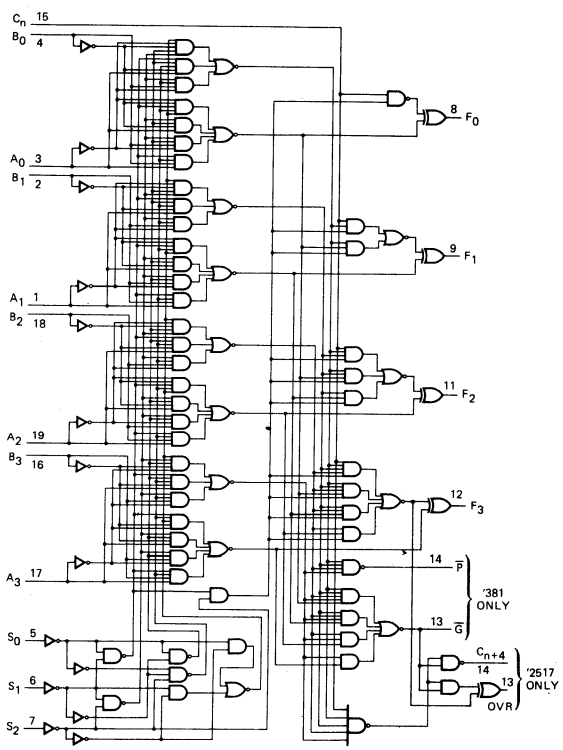
# Am25LS381 • Am54LS/74LS381
# Am25LS2517

## Arithmetic Logic Unit/Function Generator

### DISTINCTIVE CHARACTERISTICS

- Three arithmetic functions
- Three logic functions
- Preset and clear functions
- Space-saving 20-pin package
- Carry output ($C_{n+4}$) and overflow (OVR) outputs on Am25LS2517
- Generate and propagate outputs for full lookahead carry on Am25LS381
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance testing to MIL-STD-883 requirements

### LOGIC DIAGRAM




Note: The Advanced Micro Devices' LS381 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences. Am25LS2517 has been second sourced as the 54/74LS382.

### FUNCTIONAL DESCRIPTION

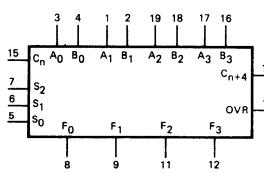
The Am25LS381 and Am54LS/74LS381 are arithmetic logic units (ALU)/function generators that perform three arithmetic operations and three logic operations on two 4-bit words. The device can also output forced 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs $S_0$, $S_1$ and $S_2$ as shown in the function table. Full carry look ahead is used over the four-bit field within the device. When devices are cascaded, multi-level full carry look-ahead is implemented using a '182 carry look ahead generator and the $\overline{G}$ and $\overline{P}$ outputs on the Am25LS381 or Am54LS/74LS381. The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. If the $C_{n+4}$ carry output function is required, the Am25LS2517 should be used.

The Am25LS381 is a high-performance version of the Am54LS/74LS381. Improvements include faster a. c. specifications, higher noise margin and twice the fan-out over the military temperature range.

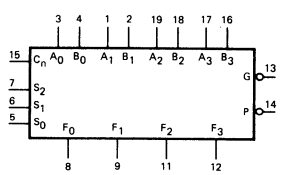
The Am25LS2517 is an arithmetic logic unit (ALU)/function generator that performs three arithmetic operations and three logic operations on two 4-bit words. The device can also force output 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs $S_0$, $S_1$ and $S_2$ as shown in the function table. Full carry look-ahead is used over the four-bit field within the device. When devices are cascaded, the carry output ($C_{n+4}$) is connected to the carry input ($C_n$) of the next device. The Am25LS2517 can also detect two's complement overflow. The overflow output (OVR) is defined logically as $C_{n+3} \oplus C_{n+4}$.

### LOGIC SYMBOLS

**Am25LS2517**



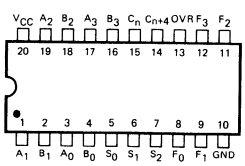

**Am25LS381**
**Am54LS/74LS381**



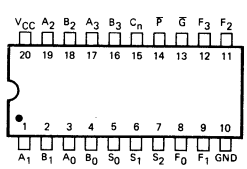

$V_{CC}$ = Pin 20
GND = Pin 10

### CONNECTION DIAGRAMS
**Top Views**

**Am25LS2517**




**Am25LS381**
**Am54LS/74LS381**




Note: Pin 1 is marked for orientation.

## Am25LS381•Am25LS2517
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | | MIL | 2.5 | 3.4 | | Volts |
| | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | | 0.45 | |
| | | | $\overline{G}$, $I_{OL}$ = 16mA | | | | 0.55 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | Any S | | | −0.36 | mA |
| | | | | Any A or B | | | −1.44 | |
| | | | | 'LS381, $C_n$ | | | −1.08 | |
| | | | | 'LS2517, $C_n$ | | | −1.44 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | Any S | | | 20 | µA |
| | | | | Any A or B | | | 80 | |
| | | | | 'LS381, $C_n$ | | | 60 | |
| | | | | 'LS2517, $C_n$ | | | 80 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | Any S | | | 0.1 | mA |
| | | | | Any A or B | | | 0.4 | |
| | | | | 'LS381, $C_n$ | | | 0.3 | |
| | | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | 'LS2517, $C_n$ | | | 0.4 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | MIL | Am25LS381 | | | 40 | mA |
| | | | | Am25LS2517 | | | 43 | |
| | | | COM'L | Am25LS381 | | 25 | 43 | |
| | | | | Am25LS2517 | | 27 | 47 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: $S_0 = S_1 = S_2$ = GND, all other inputs open.
LS2517: $S_0 = C_n$ = open, all other inputs = GND.

## Am25LS • Am54LS/74LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage (Except Am25LS2517, $C_n$ input = 5.5V) | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS381
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −400μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4mA | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL}$ = 8mA | | | 0.5 | |
| | | | $\overline{P}$, $I_{OL}$ = 8.0mA | | | 0.5 | |
| | | | $\overline{G}$, $I_{OL}$ = 16mA | | | 0.65 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current (Note 5) | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | Any S | | | −0.4 | mA |
| | | | Others | | | −1.6 | |
| $I_{IH}$ | Input HIGH Current (Note 5) | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | Any S | | | 20 | μA |
| | | | Others | | | 80 | |
| $I_I$ | Input HIGH Current (Note 5) | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | Any S | | | 0.1 | mA |
| | | | Others | | | 0.4 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 25 | 43 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: $S_0 = S_1 = S_2$ = GND, all other inputs open.
LS2517: $S_0 = C_n$ = open, all other inputs = GND.
5. Limits chosen by AMD based on SN54S/74S381, T.I. LS data unavailable.

## DEFINITION OF FUNCTIONAL TERMS

**$A_0, A_1, A_2, A_3$** The A data inputs.

**$B_0, B_1, B_2, B_3$** The B data inputs.

**$S_0, S_1, S_2, S_3$** The control inputs used to determine the arithmetic or logic function performed.

**$F_0, F_1, F_2, F_3$** The data outputs of the ALU.

**$C_n$** The carry-in input of the ALU.

**$C_{n+4}$** The carry-look-ahead output of the four-bit input field.

**$\overline{G}$** The carry-generate output for use in multi-level look-ahead schemes.

**$\overline{P}$** The carry-propagate output for use in multi-level look-ahead schemes.

**OVR** Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

## FUNCTION TABLE

| Selection $S_2$ | Selection $S_1$ | Selection $S_0$ | Arithmetic/Logic Operation |
|---|---|---|---|
| L | L | L | Clear |
| L | L | H | B Minus A |
| L | H | L | A Minus B |
| L | H | H | A Plus B |
| H | L | L | A ⊕ B |
| H | L | H | A + B |
| H | H | L | AB |
| H | H | H | Preset |

H = High Level, L = Low Level

See Truth Table for full description.

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ to $F_i$ | | 14 | 19 | | | 26 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 16 | 23 | | | 30 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $F_i$ | | 16 | 24 | | | 30 | ns | |
| $t_{PHL}$ | | | 23 | 35 | | | 40 | | |
| $t_{PLH}$ | $S_i$ to $F_i$ | | 20 | 30 | | | 35 | ns | |
| $t_{PHL}$ | | | 25 | 37 | | | 40 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{G}$ ('LS381 Only) | | 20 | 27 | | | 35 | ns | |
| $t_{PHL}$ | | | 15 | 22 | | | 30 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{P}$ ('LS381 Only) | | 17 | 24 | | | 34 | ns | |
| $t_{PHL}$ | | | 15 | 23 | | | 30 | | |
| $t_{PLH}$ | $S_i$ to $\overline{G}$ or $\overline{P}$ ('LS381 Only) | | 32 | 48 | | | 55 | ns | |
| $t_{PHL}$ | | | 23 | 35 | | | 42 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to OVR ('LS2517 Only) | | 23 | 34 | | | – | ns | |
| $t_{PHL}$ | | | 24 | 36 | | | – | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $C_{n+4}$ ('LS2517 Only) | | 21 | 32 | | | – | ns | |
| $t_{PHL}$ | | | 24 | 36 | | | – | | |
| $t_{PLH}$ | $S_i$ to OVR or $C_{n+4}$ ('LS2517 Only) | | 27 | 41 | | | – | ns | |
| $t_{PHL}$ | | | 37 | 55 | | | – | | |
| $t_{PLH}$ | $C_n$ to $C_{n+4}$ ('LS2517 Only) | | 14 | 21 | | | – | ns | |
| $t_{PHL}$ | | | 15 | 22 | | | – | | |
| $t_{PLH}$ | $C_n$ to OVR ('LS2517 Only) | | 15 | 22 | | | – | ns | |
| $t_{PHL}$ | | | 15 | 22 | | | – | | |

3

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ to $F_i$ | | 27 | | 30 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 35 | | 42 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $F_i$ | | 32 | | 36 | ns | |
| $t_{PHL}$ | | | 44 | | 50 | | |
| $t_{PLH}$ | $S_i$ to $F_i$ | | 38 | | 42 | ns | |
| $t_{PHL}$ | | | 48 | | 55 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{G}$ ('LS381 Only) | | 37 | | 40 | ns | |
| $t_{PHL}$ | | | 31 | | 36 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{P}$ ('LS381 Only) | | 34 | | 39 | ns | |
| $t_{PHL}$ | | | 34 | | 42 | | |
| $t_{PLH}$ | $S_i$ to $\overline{G}$ or $\overline{P}$ ('LS381 Only) | | 57 | | 63 | ns | |
| $t_{PHL}$ | | | 47 | | 55 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to OVR ('LS2517 Only) | | 41 | | 45 | ns | |
| $t_{PHL}$ | | | 47 | | 55 | | |
| $t_{PLH}$ | $A_i$ or $B_i$ to $C_{n+4}$ ('LS2517 Only) | | 38 | | 40 | ns | |
| $t_{PHL}$ | | | 46 | | 52 | | |
| $t_{PLH}$ | $S_i$ to OVR or $C_{n+4}$ ('LS2517 Only) | | 52 | | 60 | ns | |
| $t_{PHL}$ | | | 66 | | 75 | | |
| $t_{PLH}$ | $C_n$ to $C_{n+4}$ ('LS2517 Only) | | 28 | | 32 | ns | |
| $t_{PHL}$ | | | 28 | | 30 | | |
| $t_{PLH}$ | $C_n$ to OVR ('LS2517 Only) | | 30 | | 35 | ns | |
| $t_{PHL}$ | | | 28 | | 30 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS/54LS/74LS381
## TEST TABLE

| Path | | | | | | Same Bit | | Other Data Bits | | Output |
|---|---|---|---|---|---|---|---|---|---|---|
| In | Out | $S_0$ | $S_1$ | $S_2$ | $C_n$ | 4.5 V | GND | 4.5 V | GND | Waveform |
| $C_n$ | Any F | 1 | 0 | 0 | – | – | – | All A's & B's | – | out-of-phase |
| $C_n$ | $F_i$ | 1 | 0 | 0 | – | $B_i$ | Ai | All A's & B's | – | in-phase |
| $A_i$ | $\overline{G}$ | 1 | 1 | 0 | X | $B_i$ | – | All B's | All A's | out-of-phase |
| $B_i$ | $\overline{G}$ | 1 | 1 | 0 | X | $A_i$ | – | All B's | All A's | out-of-phase |
| $A_i$ | $\overline{P}$ | X | X | 1 | X | $B_i$ | – | All A's & B's | – | out-of-phase |
| $B_i$ | $\overline{P}$ | 1 | 1 | 0 | X | $A_i$ | – | All B's | All A's | out-of-phase |
| $A_i$ | $F_i$ | 0 | 1 | 0 | 0 | – | $B_i$ | – | A's & B's | out-of-phase |
| $A_i$ | $F_i$ | 0 | 1 | 0 | 1 | – | $B_i$ | – | A's & B's | in-phase |
| $B_i$ | $F_i$ | 0 | 1 | 0 | 0 | – | $A_i$ | – | A's & B's | out-of-phase |
| $B_i$ | $F_i$ | 0 | 1 | 0 | 1 | – | $A_i$ | – | A's & B's | in-phase |
| $A_i$ | $F_{i+1}$ | 0 | 1 | 0 | 1 | $B_i$ | – | A's & B's | – | out-of-phase |
| $B_i$ | $F_{i+1}$ | 1 | 0 | 0 | 1 | $A_i$ | – | A's & B's | – | out-of-phase |
| $S_0$ | $F_i$ | – | 0 | 0 | 1 | $B_i$ | $A_i$ | All B's | All A's | in-phase |
| $S_0$ | $\overline{G}$ | – | 1 | 0 | X | – | – | A's & B's | – | out-of-phase |
| $S_0$ | $\overline{P}$ | – | 1 | 0 | X | – | – | All B's | All A's | out-of-phase |
| $S_1$ | $F_i$ | 0 | – | 0 | 1 | $A_i$ | $B_i$ | All A's | All B's | in-phase |
| $S_1$ | $\overline{G}$ | 1 | – | 0 | X | – | – | A's & B's | – | out-of-phase |
| $S_1$ | $\overline{P}$ | 1 | – | 0 | X | – | – | All A's | All B's | out-of-phase |
| $S_2$ | $F_i$ | 0 | 1 | – | 1 | $A_i$ | $B_i$ | All A's | All B's | in-phase |
| $S_2$ | $\overline{G}$ | 1 | 1 | – | X | – | – | A's & B's | – | in-phase |
| $S_2$ | $\overline{P}$ | 1 | 1 | – | X | – | – | All A's | All B's | out-of-phase |

X = Don't care

## TRUTH TABLE

| | INPUTS | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FUNCTION | $S_0$ | $S_1$ | $S_2$ | $C_n$ | $A_n$ | $B_n$ | $F_0$ | $F_1$ | $F_2$ | $F_3$ | $\overline{G}$ | $\overline{P}$ |
| CLEAR | 0 | 0 | 0 | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| B MINUS A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| A MINUS B | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| | | | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| A PLUS B | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| A ⊕ B | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | X | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | | | X | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| A + B | 1 | 0 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | X | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| AB | 0 | 1 | 1 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | X | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| PRESET | 1 | 1 | 1 | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | X | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

## Am25LS2517
## TEST TABLE

| Path | | | | | | Same Bit | | Other Data Bits | | Output |
|---|---|---|---|---|---|---|---|---|---|---|
| In | Out | $S_0$ | $S_1$ | $S_2$ | $C_n$ | 4.5 V | GND | 4.5 V | GND | Waveform |
| $C_n$ | Any F | 1 | 0 | 0 | – | – | – | A's & B's | None | out-of-phase |
| $C_n$ | $F_i$ | 1 | 0 | 0 | – | $B_i$ | $A_i$ | A's & B's | None | in-phase |
| $A_i$ | $F_i$ | 0 | 1 | 0 | 0 | – | $B_i$ | None | A's & B's | out-of-phase |
| $A_i$ | $F_i$ | 0 | 1 | 0 | 1 | – | $B_i$ | None | A's & B's | in-phase |
| $A_i$ | OVRF | 0 | 1 | 1 | 1 | $B_i$ | – | A's & B's | None | in-phase |
| $A_i$ | $C_{n+4}$ | 0 | 1 | 1 | 1 | $B_i$ | – | A's & B's | None | in-phase |
| $B_i$ | $F_i$ | 0 | 1 | 0 | 0 | – | $A_i$ | None | A's & B's | out-of-phase |
| $B_i$ | $F_i$ | 0 | 1 | 0 | 1 | – | $A_i$ | – | A's & B's | in-phase |
| $B_i$ | OVRF | 0 | 1 | 1 | 0 | $A_i$ | – | A's & B's | None | out-of-phase |
| $B_i$ | $C_{n+4}$ | 0 | 1 | 1 | 0 | $A_i$ | – | A's & B's | None | out-of-phase |
| $A_i$ | $F_{i+1}$ | 0 | 1 | 0 | 1 | $B_i$ | – | A's & B's | None | out-of-phase |
| $B_i$ | $F_{i+1}$ | 1 | 0 | 0 | 1 | $A_i$ | – | A's & B's | None | out-of-phase |
| $S_0$ | $F_i$ | – | 0 | 0 | 1 | $B_i$ | $A_i$ | All B's | All A's | in-phase |
| $S_0$ | OVRF | – | 1 | 1 | 0 | – | – | A's & B's | None | out-of-phase |
| $S_0$ | $C_{n+4}$ | – | 1 | 1 | 0 | – | – | None | A's & B's | out-of-phase |
| $S_1$ | $F_i$ | 0 | – | 0 | 1 | $A_i$ | $B_i$ | All A's | All B's | in-phase |
| $S_1$ | OVRF | 0 | – | 1 | X | – | – | None | A's & B's | in-phase |
| $S_1$ | $C_{n+4}$ | 0 | – | 1 | X | – | – | None | A's & B's | in-phase |
| $S_2$ | $F_i$ | 0 | 1 | – | 1 | $A_i$ | $B_i$ | All A's | All B's | in-phase |
| $S_2$ | OVRF | 0 | 1 | – | 0 | – | – | None | A's & B's | in-phase |
| $S_2$ | $C_{n+4}$ | 0 | 1 | – | 0 | – | – | None | A's & B's | in-phase |

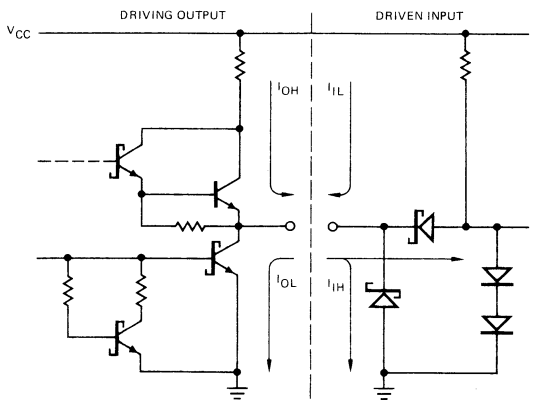
X = Don't care

## TRUTH TABLE

| | INPUTS | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FUNCTION | $S_0$ | $S_1$ | $S_2$ | $C_n$ | $A_n$ | $B_n$ | $F_0$ | $F_1$ | $F_2$ | $F_3$ | OVR | $C_{n+4}$ |
| CLEAR | 0 | 0 | 0 | 0 | X | X | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | 1 | X | X | 0 | 0 | 0 | 0 | 1 | 1 |
| B MINUS A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| A MINUS B | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| A PLUS B | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | | | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| A ⊕ B | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | | | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| A + B | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | | | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| AB | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| PRESET | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

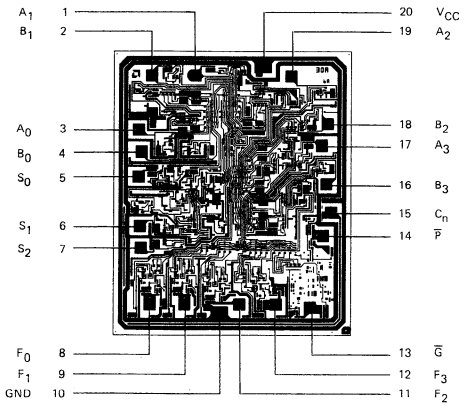
3

### Am25LS • Am54LS/74LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT
### CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

### Metallization and Pad Layout

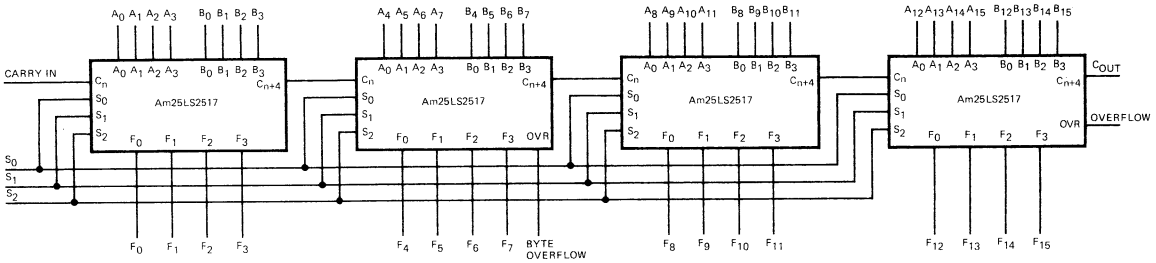



DIE SIZE 0.091" X 0.108"

## USER NOTES

1. Throughout this data sheet, the active HIGH input and output terminology has been used.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in ($C_n$ = HIGH) for the active HIGH case.

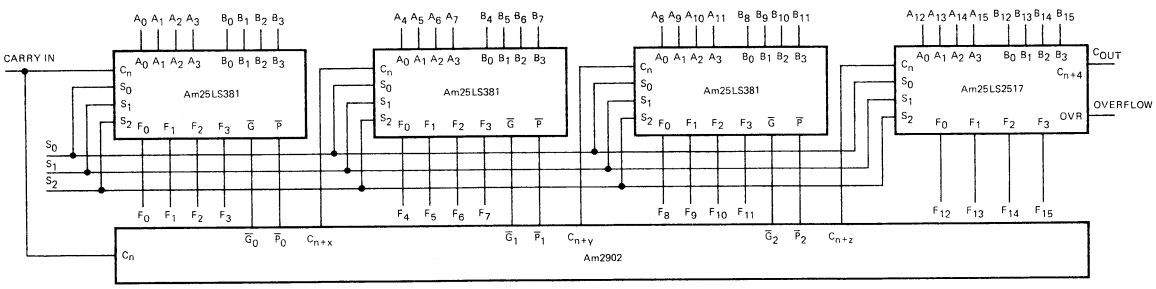
## APPLICATIONS




### TYPICAL SPEED CALCULATIONS

| | Output | |
|---|---|---|
| **Path** | **F** | **$C_{n+4}$, OVR** |
| $A_i$ or $B_i$ to $C_{n+4}$ | 24 ns | 24 ns |
| $C_n$ to $C_{n+4}$ | 15 ns | 15 ns |
| $C_n$ to $C_{n+4}$ | 15 ns | 15 ns |
| $C_n$ to $F_i$ | 16 ns | – |
| $C_n$ to $C_{n+4}$, OVR | – | 15 ns |
| 16-Bit Speed | 70 ns | 69 ns |

The Am25LS2517 in a 16-Bit Ripple Carry ALU Connection.




### TYPICAL SPEED CALCULATIONS

| | Output | |
|---|---|---|
| **Path** | **F** | **$C_{n+4}$, OVR** |
| $A_i$ or $B_i$ to $\overline{G}$ or $\overline{P}$ | 20 ns* | 20 ns* |
| $\overline{G}_i$ or $\overline{P}_i$ to $C_{i+j}$ (Am 2902) | 8 ns | 8 ns |
| $C_n$ to F | 16 ns | – |
| $C_n$ to $C_{n+4}$, OVR | – | 15 ns |
| 16-Bit Speed | 44 ns | 43 ns |

* Note that $S_i$ to G or P may be longer path.

The Am25LS2517 and Am25LS381 in a 16-Bit Carry Lookahead ALU Connection.

# UNDERSTANDING THE Am25LS2517 AND THE Am25LS381

By John R. Mick

## INTRODUCTION

The heart of most digital arighmetic processors is the arithmetic logic unit (ALU). The ALU can be thought of as a digital subsystem that performs various arithmetic and logic operations on two digital input variables. The Am25LS2517 and the Am25LS381 are Schottky TTL arithmetic logic units/function generators that perform eight arithmetic/logic operations on two four-bit input variables. In most ALU's, speed is generally a key ingredient. Therefore, as much parallelism in the operation of the arithmetic logic unit as possible is desired. The Am25LS381 ALU is designed to operate with a '182 carry lookahead generator to perform multi-level full carry lookahead over any number of bits. Therefore, the Am25LS381 has both the carry generate and carry propagate outputs required by the '182 carry lookahead generator. The Am25LS2517, on the other hand, does not have the carry generate and carry propagate functions, but rather has the carry output ($C_{n+4}$) and a two's complement overflow detection signal (OVR) available at the output. The net result is that a very high-speed 16-bit arithmetic logic unit/function generator can be designed and assembled using three Am25LS381's, one Am25LS2517, and one Am2902 (the Am2902 is a high-speed version of the '182 carry lookahead generator).

## UNDERSTANDING THE FULL ADDER

The results of an arithmetic operation in any position in a word depends not only on the two-input operand bits at that position, but also on all the lesser significant operand bits of the two input variables. The final result for any bit, therefore, is not available until the carries of all the previous bits have rippled through the logic array starting from the least significant bit and propagating through to the most significant bit. A full adder is a device that accepts two individual operand bits at the same binary weight, and also accepts a carry input bit from the next lesser significant weight full adder. The full adder then produces the sum bit for this bit position and also produces a carry bit to be used in the next more significant weight full adder carry input. The truth table for a full adder is shown in Figure 1. From this truth table, the equations for the full adder:

$S = A \oplus B \oplus C$

$C_0 = AB + BC + AC,$

where A and B are the input operands to the full adder and C is the carry input into the adder.

The sum output, S, represents the sum of the A and B operand inputs and the carry input. The carry output, $C_0$, represents the carry out of this cell and can be used in the next more significant cell of the adder. Full adder cells can be cascaded as depicted in Figure 2 to form a four-bit ripple carry parallel adder.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | C | S | $C_0$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Figure 1. Full Adder Truth Table.**

Note that once we have cascaded devices as shown in Figure 2, we may wish to discuss the equations for the i-th bit of the adder. In so doing, we might describe the equations of the full adder as follows:

$S_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = A_iB_i + B_iC_i + A_iC_i$

where the $A_i$ and $B_i$ are the input operands at the i-th bit, and the $C_i$ is the carry input to the i-th bit. (Note that the equations for this adder are iterative in nature and each depends on the result of the previous lesser significant bits of the adder array.)

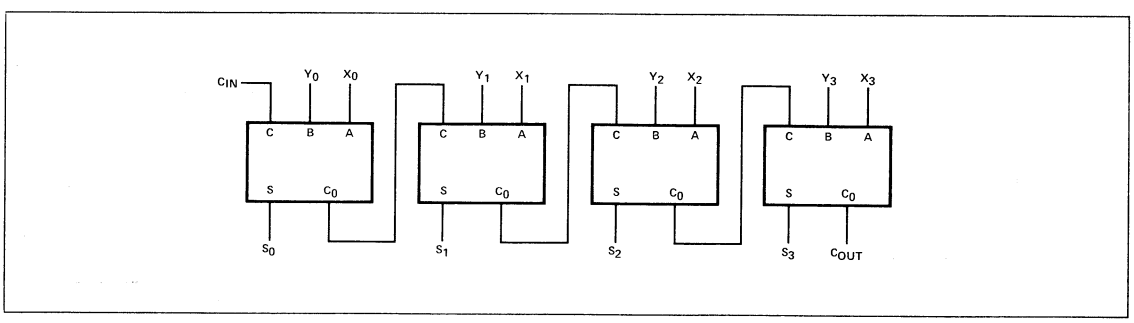



**Figure 2. Cascaded Full Adder Cells Connected as a Four-Bit Ripple-Carry Full Adder.**

The connection scheme shown in Figure 2 requires a ripple propagation time through each full adder cell. If a 16-bit adder is to be assembled, the carry will have to propagate through all 16 full adder cells. What is desired is some technique for anticipating the carry such that we will not have to wait for a ripple carry to progagate through the entire network. By using some additional logic, such an adder array can be constructed. This type of adder is usually called a carry lookahead adder.

## A FOUR-BIT CARRY LOOKAHEAD ADDER

Looking back to the equations developed for i-th bit of an adder, let us now rewrite the carry equation in a slightly different form. When we factor the $C_i$ in this equation, the new equation becomes:

$$C_{i+1} = A_iB_i + C_i (A_i + B_i)$$

From the above equation, let us now define two additional equations. These are:

$$G_i = A_iB_i$$

$$P_i = A_i + B_i$$

With these two new auxiliary equations, we can now rewrite the carry equation for the i-th bit as follows:

$$C_{i+1} = G_i + P_iC_i$$

Note that we have now developed two terms: the $P_i$ term is known as carry propagate and the $G_i$ term is known as carry generate. An anticipated carry can be generated at any stage of the adder by implementing the above equations and using the auxiliary functions $P_i$ and $G_i$ as required.

It is interesting to note that the sum equation can also be written in terms of these two auxiliary equations, $P_i$ and $G_i$. For this case, the equation is:

$$S_i = (A_i + B_i) (A_iB_i) \oplus C_i$$

The auxiliary function $G_i$ is called carry generate, because if it is true, then a carry is immediately produced for the next adder stage. The function $P_i$ is called carry propagate because it implies there will be a carry into the next stage of the adder if there is a carry into this stage of the adder. That is, $G_i$ causes a carry signal at the i-th stage of the adder to be generated and presented to the next stage of the adder while $P_i$ causes an existing carry at the input to the i-th stage of the adder to propagate to the next stage of the adder.

Let us now write all of the sum and carry equations required for a full four-bit lookahead carry adder.

$$S_0 = A_0 \oplus B_0 \oplus C_0$$
$$S_1 = A_1 \oplus B_1 \oplus [G_0 + P_0C_0]$$
$$S_2 = A_2 \oplus B_2 \oplus [G_1 + P_1G_0 + P_1P_0C_0]$$
$$S_3 = A_3 \oplus B_2 \oplus [G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0]$$
$$C_{i+4} = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

An important point to note is that all of the sum equations and the final carry output equation, $C_{i+4}$, can be written in terms of the $A_i$, $B_i$, and $C_0$ inputs to the four-bit adder. The configuration as described above is shown in Figure 3. This figure is divided into two parts — the upper blocks show the auxiliary function generator circuitry required to implement the $P_i$ and $G_i$ equations while the lower block implements the logic required to generate the sum output at each bit position.

A serious drawback to the lookahead carry adder is that as the word length is increased, the carry functions become more and more complex, eventually becoming impractical due to the large number of interconnections and heavy loading of the $G_i$ and $P_i$ functions. The auxiliary function concept can be extended, however, by dividing the word length into fairly small increments and defining blocks of auxiliary functions G and P.

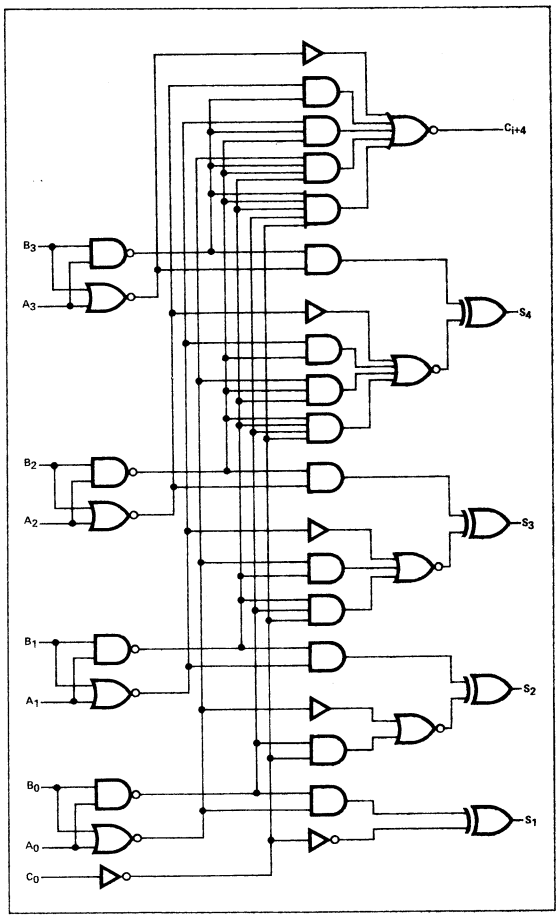



**Figure 3. Full Four-Bit Carry-Lookahead Adder.**

It is possible for a given block, to define a function G as the carry out generated with the block; and P can be defined as the carry propagate over the block. If the block size is set at four bits, then the functions for G and P for this block can be defined as follows:

$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

It is important to note that neither of these terms involves a carry-in ($C_0$) to the block, so no matter how many blocks are tied in an adder, all the blocks have stable G and P functions available in a minimum number of gate delays.

The G and P functions can be gated to produce a carry-in to each four-bit block, as a function of the lesser significant blocks. The carry-in to a block in is therefore:

$$C_n = G_{n-1} + P_{n-1}G_{n-2} + P_{n-1}P_{n-2}G_{n-3} + \ldots + P_{n-1}P_{n-2}P_{n-3} \ldots P_2P_1P_0C_0$$

Finally, the carry-in to each of the bits in a four-bit block must include a term for the actual least significant carry-in; note, therefore, that the equations for the four-bit full adder presented above include a term for carry-in at each bit position. Figure 4 shows the logic diagram for the Am25LS381 arithmetic logic unit/function generator while Figure 5 shows the logic diagram for the Am25LS2517 arithmetic logic unit/function generator. Note the generate and propagate outputs

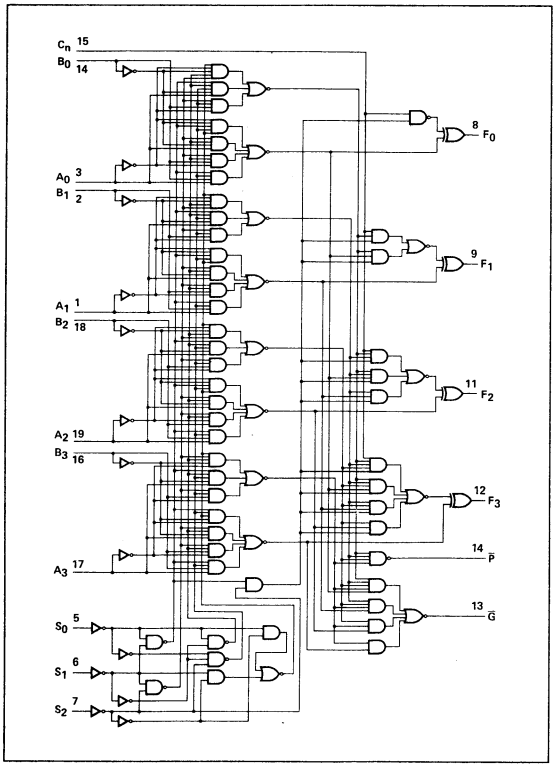



Figure 4. Logic Diagram of The Am25LS381.

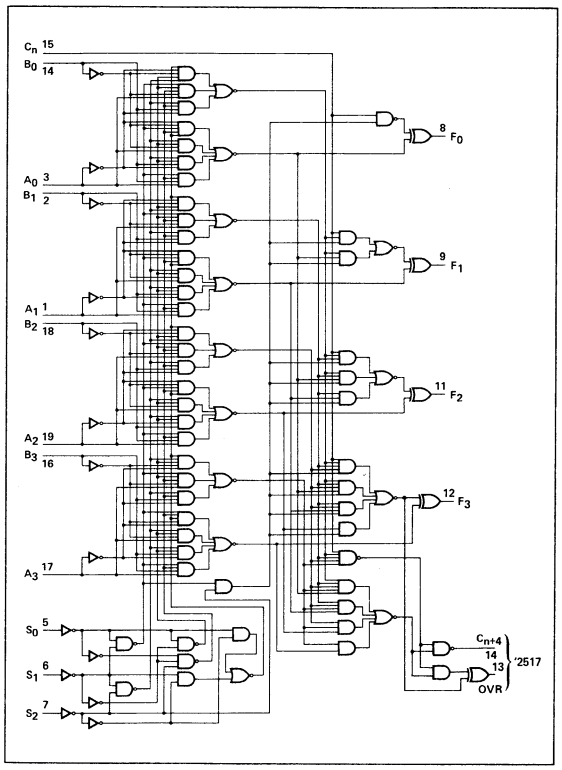



Figure 5. Logic Diagram of the Am25LS2517.

on the Am25LS381, and the carry output and overflow output on the Am25LS2517. Figure 6 gives the function table for both the Am25LS2517 and Am25LS381. Figure 7 shows the technique for cascading three Am25LS381's, one Am25LS2517, and one Am2902 in a full 16-bit high-speed carry lookahead connection. Figure 8 shows a connection scheme using only four Am25LS2517's in a 16-bit arithmetic logic unit connection where the carries are rippled between the devices. Each Am25LS2517 does use internal carry lookahead over the four-bit block.

In summary, the ripple carry method can be used in conjunction with the lookahead technique in several ways.

1. Lookahead carry over sections of the adder and ripple carry between these sections of the adder can be used. This method is often the most efficient in terms of hardware for

| Selection | | | Arithmetic/Logic Operation |
|---|---|---|---|
| $S_2$ | $S_1$ | $S_0$ | |
| L | L | L | Clear |
| L | L | H | B Minus A |
| L | H | L | A Minus B |
| L | H | H | A Plus B |
| H | L | L | A ⊕ B |
| H | L | H | A + B |
| H | H | L | AB |
| H | H | H | Preset |

H = High Level, L = Low Level

Figure 6. Function Table for the Am25LS2517 and Am25LS381.

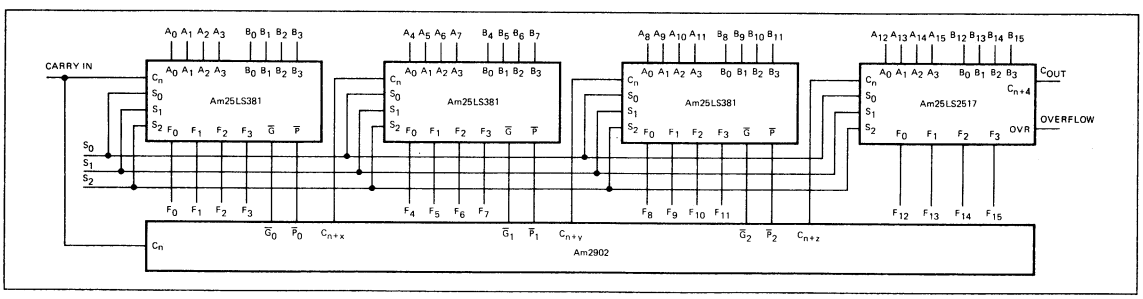



Figure 7. Full Lookahead Carry 16-Bit Adder.

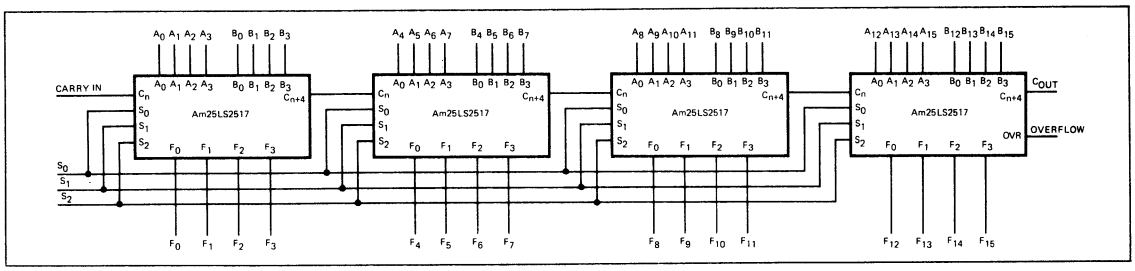



**Figure 8. Connection of 16-Bit ALU Using Ripple Carry.**

a given speed requirement. It does not require the use of a lookahead carry generator such as the Am2902.

2. Lookahead carry across 16-bit blocks with a ripple carry between 16-bit blocks can be used. This technique is usually called two-level carry lookahead addition. This technique results in very high-speed arithmetic function generation and makes a reasonable tradeoff between the speed and hardware for word lengths greater than 16 bits.
3. Full lookahead carry across all levels and all block sizes can be used. This is the highest speed arithmetic logic unit connection scheme. For word sizes up to 64 bits, it is referred to as three-level lookahead carry addition. Such a 64-bit ALU requires the use of five Am2902 carry lookahead generator units in addition to the 15 Am25LS381 devices and one Am25LS2517 as shown in Figure 9.

## OVERFLOW

When two's complement numbers are added or subtracted, the result must lie within the range of the numbers that can be handled by the operand word length. Numbers are normally represented either as fractions with a binary point between the sign bit and the rest of the word, or as integers where the binary point is after the least significant bit. The actual choice for the location of the binary point is really up to the design engineer, as the hardware configuration required for either technique is identical. It is also possible to use number notations that include both integer and fractional representations in the same numbering scheme. Overflow is defined as the situation where the result of an arithmetic operation lies outside of the number range that can be represented by the number of bits in the word. For example, if two eight-bit numbers are added and the result does not lie within the number range that can be represented by an eight-bit word, we say that an overflow has occured. This can happen at either the positive end of the number range or at the negative end of the number range. The logic function that indicates that the result of an operation is outside of the representable number range is:

$$OVR = C_S \oplus C_{S+1}$$

where $C_S$ is the carry-in to the sign bit and $C_{S+1}$ is the carry-out of the sign bit.

Thus, for a four-bit ALU with the sign bit in the most significant bit position, the overflow can be defined as the $C_{n+4}$ term exclusive OR'ed with the $C_{n+3}$ term.

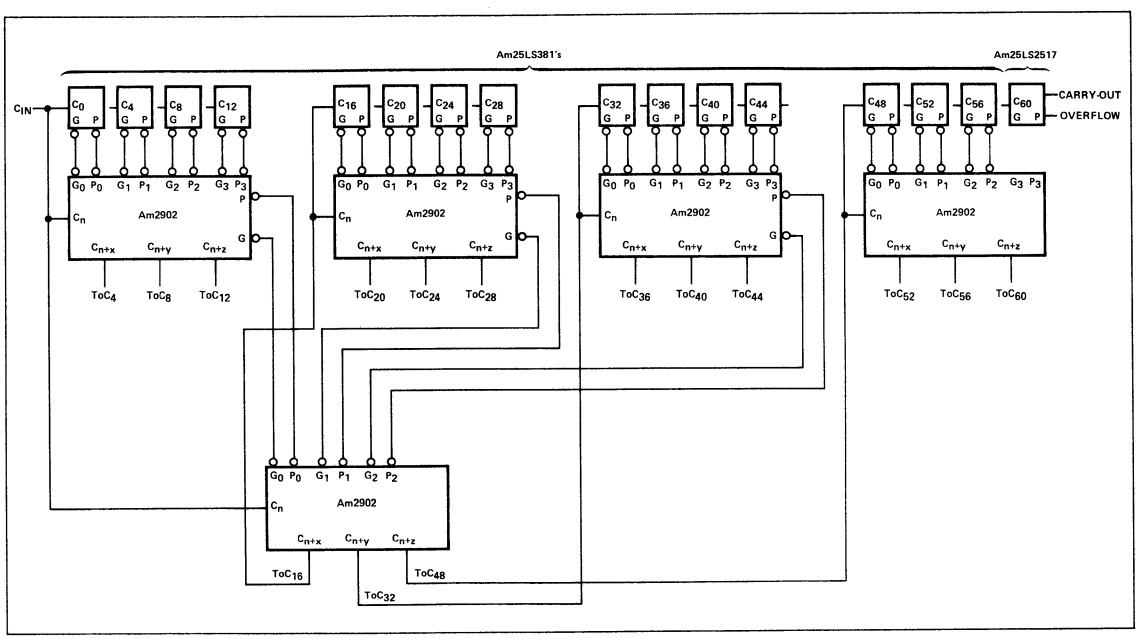



**Figure 9. 64-Bit ALU with Full Carry Lookahead Using 5 Am2902's, 15 Am25LS381's and 1 Am25LS2517.**

## SPEED OR DELAY

Usually, the most important parameter in the design of any arithmetic logic unit is speed. How fast can two numbers be added? Is ripple carry sufficient or should carry lookahead over the entire adder array be used? In order to answer these questions, the design engineer must first evaluate the speed of the ALU required in his system. Then he can evaluate the various alternatives based on the number of bits in the word being used in the design.

The calculation of the speed (add or subtract time) of a 16-bit adder is straightforward and will be discussed in detail. It should be mentioned that the speed of the adder while in the logic mode is simply the propagation delay from the $A_i$ or $B_i$ inputs to the $F_i$ outputs (35ns maximum at 25°C and 5V for the Am25LS2517).

## LOOKAHEAD CARRY

The typical method for building 16-bit ALU's is to employ a carry lookahead generator such as the Am2902. Such a 16-bit design would incorporate three Am25LS381's, one Am25LS 2517, and one Am2902. For the 16-bit full carry lookahead adder in the add or subtract mode as shown in Figure 7, the maximum propagation delay for data-in to data-out is calculated as follows:

**DATA PATH DELAY**
**16-BIT LOOKAHEAD ADDER/SUBTRACTOR**
**(+5V and 25°C Maximum Delays)**

| Path | Output | | | Units |
|---|---|---|---|---|
| | $F_i$ | $C_{n+4}$ | OVR | |
| $A_i$ or $B_i$ to $\overline{G}$ or $\overline{P}$ | 27 | 27 | 27 | ns |
| $G_i$ or $P_i$ to $C_{i+j}$ (Am2902) | 10 | 10 | 10 | ns |
| $C_n$ to $F_i$ | 23 | – | – | ns |
| $C_n$ to $C_{n+4}$ or OVR | – | 22 | 22 | ns |
| TOTAL 16-bit delay | 60 | 59 | 59 | ns |

The data path for this computation begins at the least significant 4-bit device, propagates through the Am2902, and then ends at the most significant 4-bit device. Actually, the delay to the outputs of the most significant device (MSD), then second MSD, or third MSD is identical.

Thus, the above speed is identical if a 12-bit ALU is fabricated. This results because the same types of combinatorial propagation delays are involved.

We should also investigate the delay of this adder with regard to the select inputs as shown in Figure 7. Again, we may calculate the 16-bit full carry lookahead add/subtract delay as follows:

**16-BIT LOOKAHEAD ADDER DELAY**
**FOR SELECT INPUTS**
**(+5V and 25°C Maximum Delays)**

| Path | Output | | | Units |
|---|---|---|---|---|
| | $F_i$ | $C_{n+4}$ | OVR | |
| $S_i$ to $\overline{G}$ or $\overline{P}$ | 48 | 48 | 48 | ns |
| $G_i$ or $P_i$ to $C_{i+j}$ (Am2902) | 10 | 10 | 10 | ns |
| $C_n$ to $F_i$ | 23 | – | – | ns |
| $C_n$ to $C_{n+4}$ or OVR | – | 22 | 22 | ns |
| TOTAL 16-bit delay | 81 | 80 | 80 | ns |

Let us examine the speed of a 64-bit arithmetic logic unit fabricated as shown in Figure 9. The worst case path for this design is as follows:

**DATA PATH DELAY**
**64-BIT LOOKAHEAD ADDER/SUBTRACTOR**
**(+5V and 25°C Maximum Delays)**

| Path | Output | | | Units |
|---|---|---|---|---|
| | $F_i$ | $C_{n+4}$ | OVR | |
| $A_i$ or $B_i$ to $\overline{G}$ or $\overline{P}$ | 27 | 27 | 27 | ns |
| $G_i$ or $P_i$ to $G_i$ or $P_i$ (Am2902) | 14 | 14 | 14 | ns |
| $G_i$ or $P_i$ to $C_{i+j}$ (Am2902) | 10 | 10 | 10 | ns |
| $C_n$ to $C_{i+j}$ (Am2902) | 14 | 14 | 14 | ns |
| $C_n$ to $F_i$ | 23 | – | – | ns |
| $C_n$ to $C_{n+4}$ or OVR | – | 22 | 22 | ns |
| TOTAL 16-bit delay | 88 | 87 | 87 | ns |

The above example demonstrates the speed improvement when using carry lookahead over the entire array. When this 64-bit example is compared with the previous 16-bit example, it will be found that the only difference is the addition of two Am2902 delays.

## RIPPLE CARRY

The slowest speed ALU design employs the ripple carry technique. When four-bit devices such as the Am25LS2517 are employed in such an ALU, the speed is usually computed using the combinatorial delay terms in the following manner.

1. Select the longest combinatorial delay in the least significant device from any input to the carry output, $C_{n+4}$. This is usually from the A or B inputs to the carry output.
2. Add the carry input to carry output propagation delay as many times as required to represent each of the intermediate four-bit ALU's.
3. Finally, take the propagation delay from the carry input to the ALU adder outputs.

When the above rules are followed, the total worst case propagation delay over the entire ALU bit width is derived.

If we consider the ripple carry adder/subtractor configuration as shown in Figure 8, the propagation delay for the data input to data output path is computed as follows:

**DATA PATH DELAY**
**16-BIT RIPPLE CARRY ADDER/SUBTRACTOR**
**(+5V and +25°C Maximum Delays)**

| Path | Output | | | Units |
|---|---|---|---|---|
| | $F_i$ | $C_{n+4}$ | OVR | |
| $A_i$ or $B_i$ to $C_{n+4}$ | 36 | 36 | 36 | ns |
| $C_n$ to $C_{n+4}$ | 22 | 22 | 22 | ns |
| $C_n$ to $C_{n+4}$ | 22 | 22 | 22 | ns |
| $C_n$ to $F_i$ | 23 | – | – | ns |
| $C_n$ to $C_{n+4}$ or OVR | – | 22 | 22 | ns |
| TOTAL 16-bit delay | 103 | 102 | 102 | ns |

In this connection, the maximum delay begins at the least significant device and propagates through the most significant device via the ripple carry path.

The select to output delay is computed in a similar manner using $S_i$ to $C_{n+4}$ as the first term and is found to be:

$S_i$ to $F_i$ = 122ns; $S_i$ to $C_{n+4}$ = 12ns; $S_i$ to OVR = 121ns

The ripple carry computational examples show the speed of a 16-bit ALU function/generator built using four Am25LS 2517's.

## COMPARING THE '2517/'381 WITH THE '181

To compare the performance of the Am25LS2517 and LS381, we should evaluate the various '181 ALU's connected in a 16-bit configuration with the Am2902 carry lookahead generator used in all configurations as shown in Figure 7. The comparison for the $A_i$ or $B_i$ to $F_i$ add/subtract time is as follows:

**COMPARISON OF 16-BIT ADDER/SUBTRACTOR DATA DELAY USING 4 ALU's AND 1 Am2902**

| ALU Device | Maximum Add/Subtract Delay +5V and 25°C | Maximum Power* $V_{CC}$ = +5.25V |
|---|---|---|
| Am74S181 | 37ns | 914mA |
| Am74181 | 64ns | 694mA |
| Am74LS181 | 69ns | 242mA |
| Am25LS181 | 55ns | 242mA |
| Am25LS381/Am25LS2517 | 60ns | 266mA |

*Note: Of this power, 94mA is the Am2902

Even more important is the comparison of "System Speed" normally associated with the ALU function. If we assume the system configuration as shown in Figure 10, then a reasonable comparison of speed for $A_i$ or $B_i$ to OVERFLOW can be made as follows:

**SPEED AND POWER FOR ALU SYSTEMS OF FIGURE 10**

| Path | All "S" | All 25LS | All 74LS | All Gold Doped | 'LS381 'LS2517 | Units |
|---|---|---|---|---|---|---|
| $A_i$ or $B_i$ to $\overline{G}$ or $\overline{P}$ | 15 | 26 | 33 | 25 | 27 | ns |
| $\overline{G}$ or $\overline{P}$ to $C_{i+j}$ (Am2902) | 10 | 10 | 10 | 10 | 10 | ns |
| $C_n$ to OVR | – | – | – | – | 22 | ns |
| $C_n$ to $F_3$ | 12 | 19 | 26 | 19 | – | ns |
| Inverter | 5 | 20* | 20 | 22 | – | ns |
| MUX to OVR ('151) | 12 | 24 | 32 | 27 | – | ns |
| TOTAL | 54 | 99 | 121 | 103 | 59 | ns |
| POWER | 993 | 253 | 253 | 748 | 266 | mA |

*no 25LS

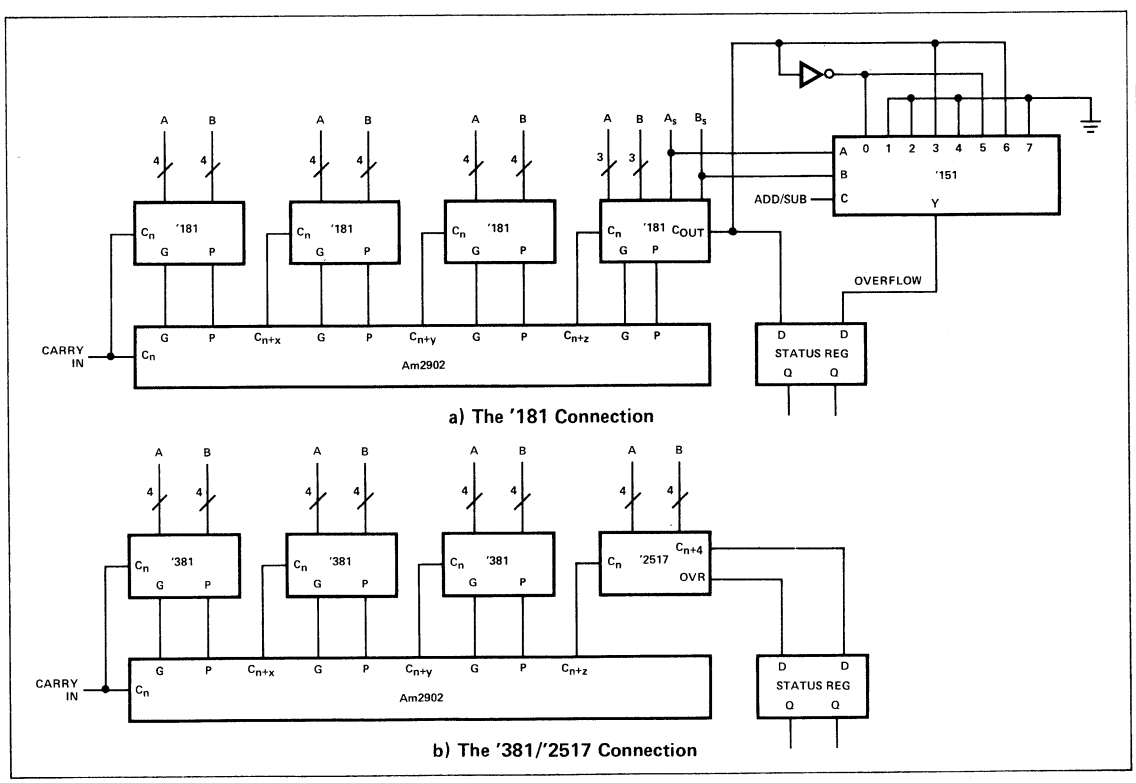



**Figure 10. The Normal ALU System.**

## SUMMARY

The Am25LS381 and Am25LS2517 offer superior performance utilizing the space saving 20-pin package. The data add/subtract time compares very favorably with the 74181 and 74S181 with a considerable reduction (1/3 to 1/4) in dissipated power. The Am25LS381 and Am25LS2517 combination provide the OVR function not currently available or easily to implement on any '181 configuration. The 20-pin package configuration offers at least a 2:1 saving in PC board area compared to the '181 24-pin package approach.

# Am25LS384 • Am54LS/74LS384

## 8-Bit Serial/Parallel Two's Complement Multiplier

**The 'LS384 is Texas Instruments' planned second source to Advanced Micro Devices' Am25LS14. See Am25LS14 data sheet for full information.**

### FUNCTIONAL DESCRIPTION

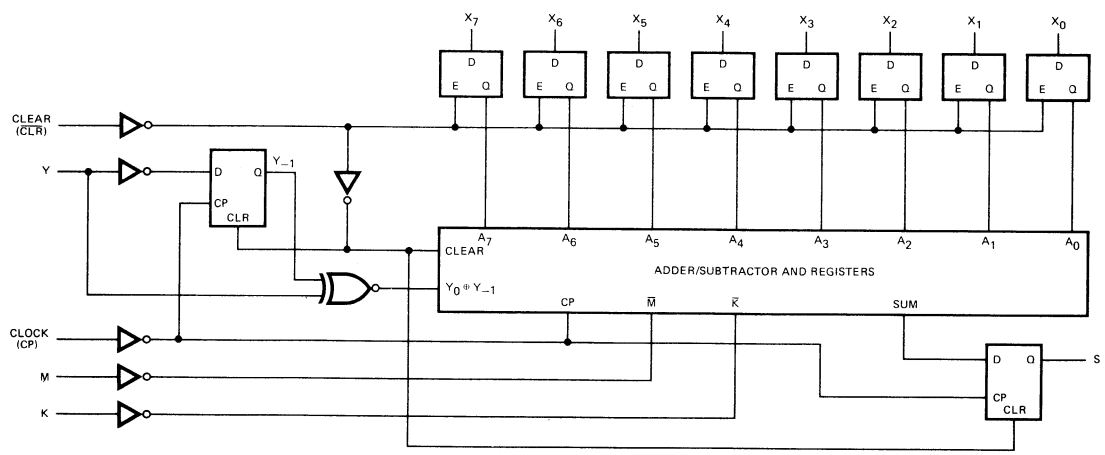
The Am25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream — least significant bit first. The product is clocked out the S output least significant bit first.

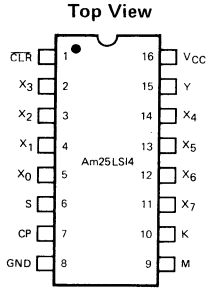
The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

### LOGIC DIAGRAM

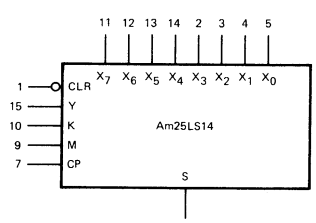



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

# Am25LS385 • Am54LS/74LS385

## Quad Serial Adder/Subtractor

**'LS385 is Texas Instruments' planned second source to Advanced Micro Devices' Am25LS15.**

**See Am25LS15 data sheet for full information.**

### FUNCTIONAL DESCRIPTION

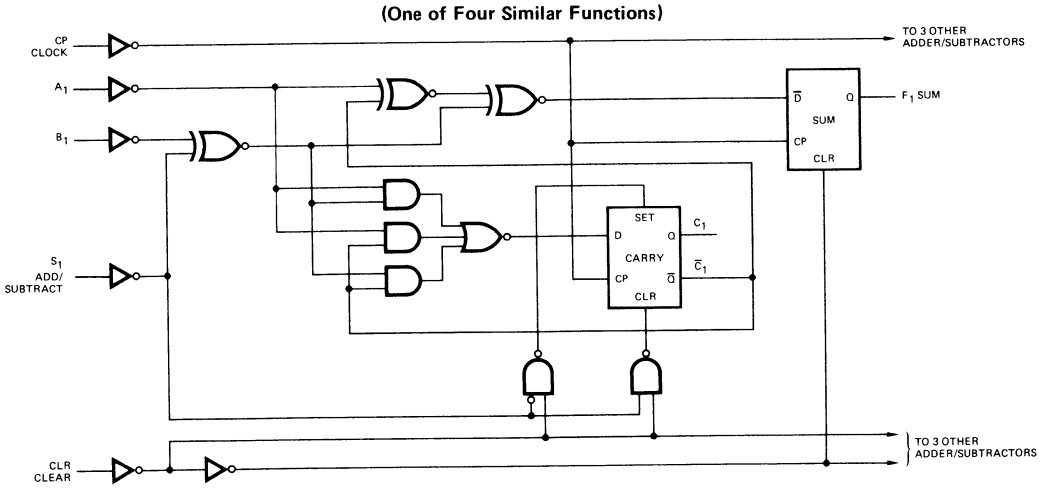
The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

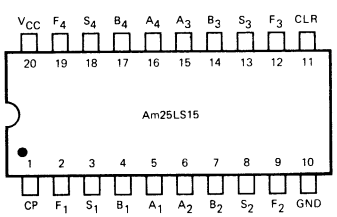
The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

3

### LOGIC DIAGRAM
(One of Four Similar Functions)

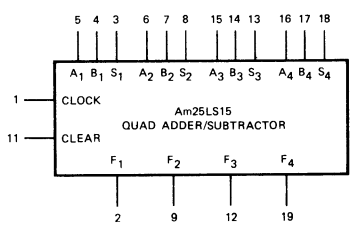



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

# Am25LS388 • Am54LS/74LS388

## Quad D Register with Standard and Three-State Outputs

**The 'LS388 is Texas Instruments' planned second source to Advanced Micro Devices Am25LS2518.**

**See Am25LS2518 data sheet for full information.**

### FUNCTIONAL DESCRIPTION

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

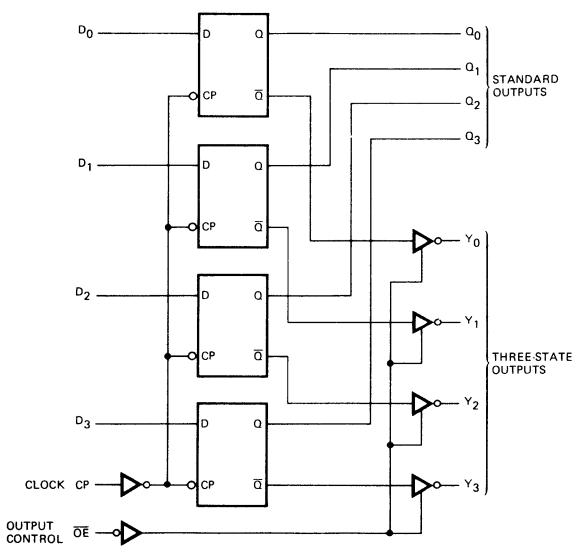
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

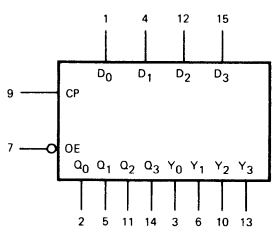
The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

### LOGIC DIAGRAM

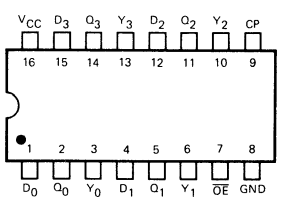



### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

# Am25LS399 • Am54LS/74LS399

## Quad Two-Input Register

### DISTINCTIVE CHARACTERISTICS

- Four-bit register accepts data from one of two 4-bit input fields
- Positive, edge-triggered clock
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower $V_{OL}$ at $I_{OL}$ = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

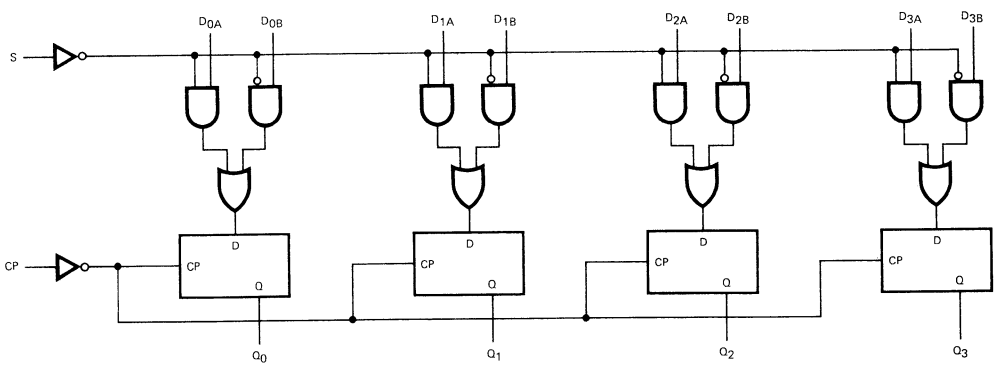
### FUNCTIONAL DESCRIPTION

The Am25LS399 and Am54LS/74LS399 are dual input port, four-bit registers built using advanced Low-Power Schottky processing. The registers consist of four D-type flip-flops with a buffered common clock. Each flip-flop has a two-input multiplexer at its data input such that it can be loaded with incoming data from one of two sources. A buffered common select line, S, controls the four 2-input multiplexers.

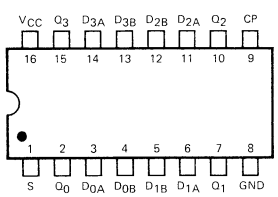
Data on the four inputs selected by the S line is stored in the four flip-flops on the LOW-to-HIGH transition of the clock. When the S input is LOW, the $D_{iA}$ input data will be stored in the register. When the S input is HIGH, the $D_{iB}$ input data will be stored in the register.

The Am54LS/74LS399 is a standard performance version of the Am25LS399. See appropriate electrical characteristic tables for detailed Am25LS improvements.

### LOGIC DIAGRAM

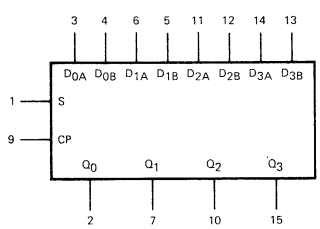



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## Am25LS399

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | Clock | | | −0.36 | mA |
| | | | Others | | | −0.24 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | Clock | | | 20 | μA |
| | | | Others | | | 14 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 11 | 18 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with select and clock inputs at 4.5 V, all data inputs at 0 V, all outputs open.

## Am25LS • Am54LS/74LS

**MAXIMUM RATINGS** (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## Am54LS/74LS399

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | All, $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | 74LS only, $I_{OL} = 8.0mA$ | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 11 | 18 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with select and clock inputs at 4.5 V, all data inputs at 0 V, all outputs open.

3

### FUNCTION TABLE

| SELECT S | CLOCK CP | DATA $D_{iA}$ | INPUTS $D_{iB}$ | OUTPUT $Q_i$ |
|---|---|---|---|---|
| L | ↑ | L | X | L |
| L | ↑ | H | X | H |
| H | ↑ | X | L | L |
| H | ↑ | X | H | H |

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

### DEFINITION OF FUNCTIONAL TERMS

$D_{0A}$, $D_{1A}$, $D_{2A}$, $D_{3A}$ The "A" word into the two-input multiplexer of the D flip-flops.

$D_{0B}$, $D_{1B}$, $D_{2B}$, $D_{3B}$ The "B" word into the two-input multiplexer of the D flip-flops.

$Q_0$, $Q_1$, $Q_2$, $Q_3$ The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Am25LS Min. | Am25LS Typ. | Am25LS Max. | Am54LS/74LS Min. | Am54LS/74LS Typ. | Am54LS/74LS Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 13 | 20 | | 18 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 13 | 20 | | 21 | 32 | | |
| $t_{PW}$ | Clock Pulse Width | 17 | | | 20 | | | ns | |
| $t_s$ | Data | 20 | | | 20 | | | ns | |
| $t_h$ | Data | 5.0 | | | 5.0 | | | ns | |
| $t_s$ | Select | 30 | | | 30 | | | ns | |
| $t_h$ | Select | 0 | | | 0 | | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 40 | 65 | | 30 | 40 | | MHz | |

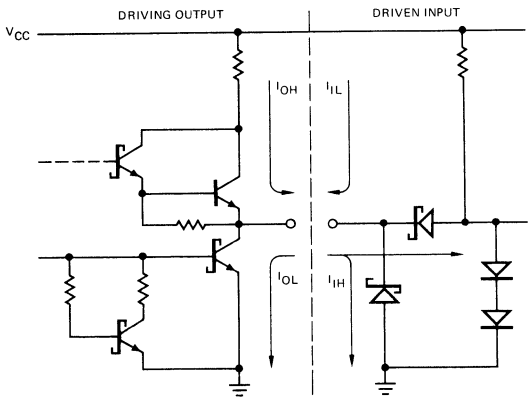
Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no contraints on $t_r$, $t_f$, pulse width or duty cycle.

## Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5%) Min. | Am25LS COM'L Max. | Am25LS MIL ($T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10%) Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | 30 | | 35 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 30 | | 35 | | |
| $t_{PW}$ | Clock Pulse Width | 26 | | 30 | | ns | |
| $t_s$ | Data | 30 | | 35 | | ns | |
| $t_h$ | Data | 11 | | 12 | | ns | |
| $t_s$ | Select | 43 | | 50 | | ns | |
| $t_h$ | Select | 4 | | 5 | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | 30 | | 26 | | MHz | |

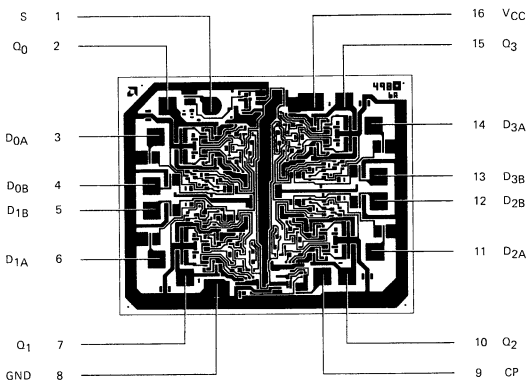
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Am25LS Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



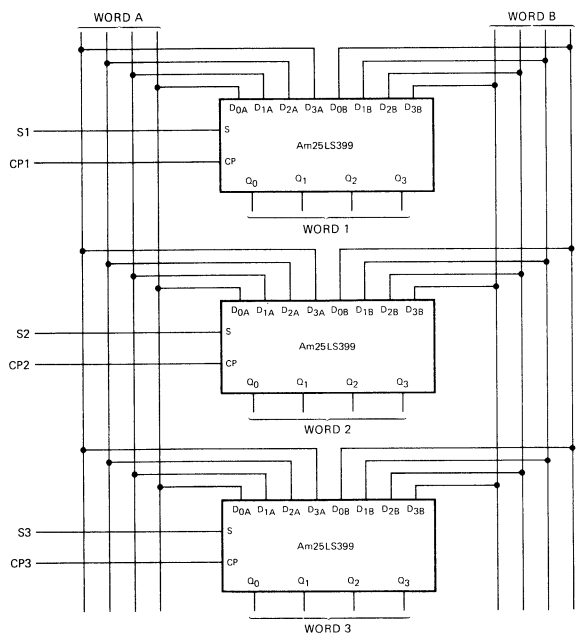

Note: Actual current flow direction shown.

## Metallization and Pad Layout




DIE SIZE 0.075" X 0.061"

## APPLICATION




Am25LS399 used to store a word from either data bus A or data bus B.

# Am54LS/74LS424

**Clock Generator and Driver for 8080A Compatible Microprocessors**

**The SN54LS/74LS424 is Texas Instruments second source part number to the AMD/Intel 8224 device.**

**See the current issue of the Am8224 data sheet for full information.**

# Am54LS/74LS568 • Am54LS/74LS569

**Four-Bit Up/Down Counters with Three State Outputs**

**The 54LS/74LS568 and 54LS/74LS569 are other manufacturers alternate source part numbers to the Advanced Micro Devices' Am25LS2568 and Am25LS2569.**

**See the Am25LS2568 and Am25LS2569 data sheets for full information.**

## The SN54LS/74LS668 and SN54LS/74LS669 are reduced speed versions of the 54LS/74LS168A and 54LS/74LS169A.

### ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ±5% | MIN. = 4.75V | MAX. = 5.25V |
| MIL | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ±10% | MIN. = 4.50V | MAX. = 5.50V |

### DC CHARACTERISTICS OVER OPERATING RANGE

DC Characteristics are the same as the 54LS/74LS168A and 54LS/74LS169A devices.

### SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Am54LS/74LS Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Ripple Carry | | | 26 | 40 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 40 | 60 | | |
| $t_{PLH}$ | Clock to any Q | | | 18 | 27 | ns | |
| $t_{PHL}$ | | | | 18 | 27 | | |
| $t_{PLH}$ | Enable $\overline{T}$ to Ripple Carry | | | 11 | 17 | ns | |
| $t_{PHL}$ | | | | 29 | 45 | | |
| $t_{PLH}$ | Up/Down to Ripple Carry | | | 22 | 35 | ns | |
| $t_{PHL}$ | | | | 26 | 40 | | |
| $t_{pw}$ | Clock Pulse Width | | 25 | | | ns | |
| $t_s$ | Set-up | A, B, C, D | 20 | | | ns | |
| | | $\overline{EN}$ P, $\overline{EN}$ $\overline{T}$ | 20 | | | | |
| | | Load | 25 | | | ns | |
| | | Up/Down | 30 | | | | |
| $t_h$ | Hold, any Input | | 0 | | | ns | |
| $f_{max}$(Note 1) | Maximum Clock Frequency | | 25 | | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## Three-state output, 20-pin versions are also available as the Am25LS2568 and Am25LS2569.

# Am25LS670 • Am54LS/74LS670

**4-By-4 Register File with 3-State or Open Collector Outputs**

**Am25LS670 • Am54LS/74LS670 data is combined with the Am25LS170.**

**See Am25LS170 data sheet for full information.**

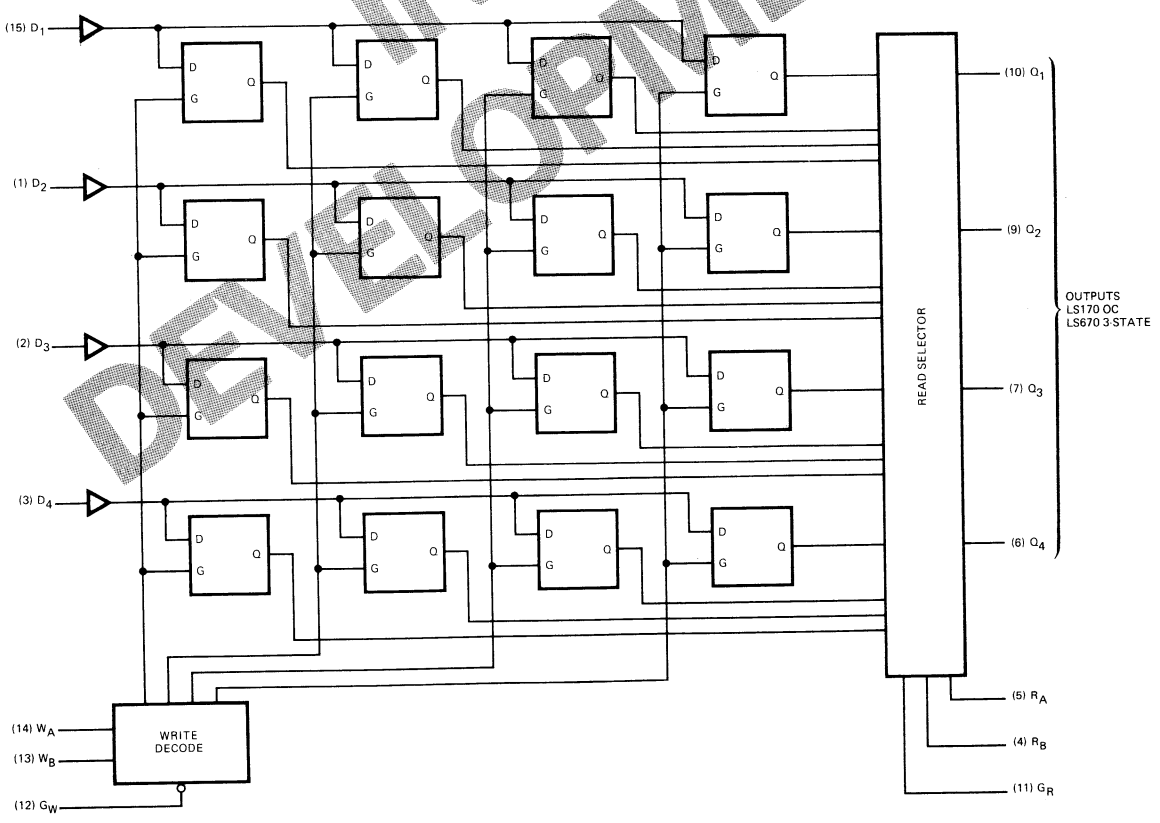
## FUNCTIONAL DESCRIPTION

The Am25LS170 and 670 are 16-bit low-power Schottky register files. The file is organized as 4 words of 4-bits each with separate on-chip address decoding for read and write. This permits simultaneous read and write operations either to the same or different addresses.

Four data inputs are used to supply the 4-bit data word to be stored. The $W_A$ and $W_B$ inputs supply the write address while the $G_W$ supplies the write enable. Four data outputs ($O_0$ to $O_3$) are selected from data word cells by the $R_A$ and $R_B$ address. The output is available if the read enable $G_R$ is LOW. The register file performs a non-destructive readout. The Am25LS170 has open collector output for convenience of collector ORing while the Am25LS670 provides three-state outputs for bus selection.

The Am54LS/74LS170 and 670 are standard performance versions of the Am25LS160 and 670. See appropriate electrical characteristic tables for detailed Am25LS improvements.

## LOGIC DIAGRAM






3

# Am25LS2513
## Three-State Priority Encoder

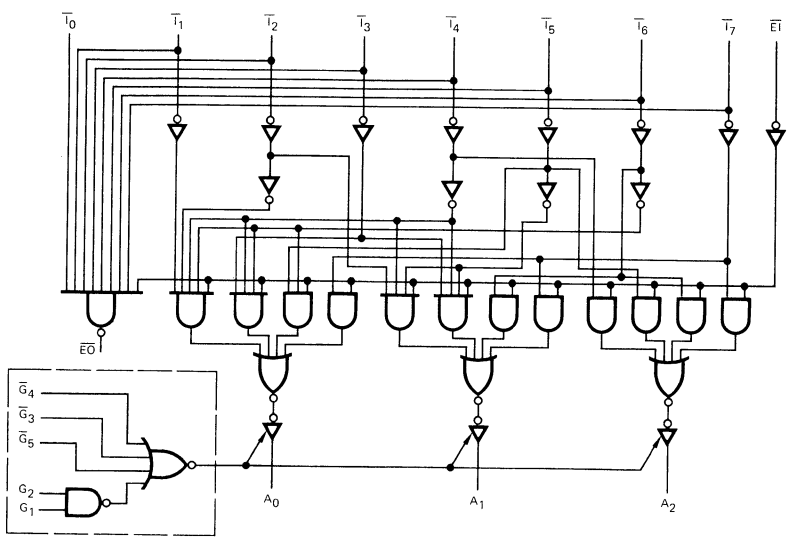
### DISTINCTIVE CHARACTERISTICS

- Encodes eight lines to three-line binary
- Expandable
- Cascadable
- Three State inverted output version of Am54LS/74LS/25LS148
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

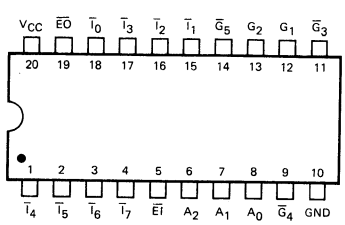
### FUNCTIONAL DESCRIPTION

The Am25LS2513 Low-Power Schottky Priority Encoder performs priority encoding of 8 inputs to provide a binary-weighted code of the priority order of the 3 tri-state active HIGH outputs $A_0$, $A_1$, $A_2$. Three active LOW and two active HIGH inputs in AND-OR configuration allow control of the tri-state outputs. The use of the input enable ($\overline{EI}$) combined with the enable output ($\overline{EO}$) permits cascading without additional circuitry. Enable input ($\overline{EI}$) HIGH will force all outputs LOW subject to the tri-state control. The enable output is LOW when all inputs $\overline{I_0}$ through $\overline{I_7}$ are HIGH and the enable input is LOW.

### LOGIC DIAGRAM

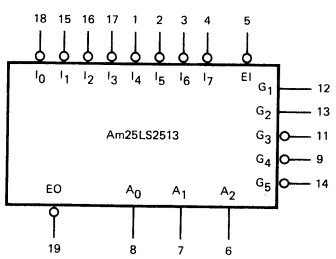



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



## Am25LS2513

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | | 2.4 | 3.2 | | |
| | | | $\overline{EO}$, $I_{OH} = -440\mu A$ | MIL | 2.5 | 3.4 | | |
| | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| | | | $I_{OL} = 12mA (A_n$ Outputs) | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | $\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$ | | | | 0.4 | mA |
| | | | All others | | | | 0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | $\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$ | | | | 20 | μA |
| | | | All others | | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | $\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$ | | | | 0.1 | mA |
| | | | All others | | | | 0.2 | |
| $I_O$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 15 | 24 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

## Am25LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0 V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_i}$ to $A_n$ (In-phase) | | 17 | 25 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 17 | 25 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $A_n$ (Out-phase) | | 11 | 17 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{EO}$ | | 7.0 | 11 | ns | |
| $t_{PHL}$ | | | 24 | 36 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{EO}$ | | 11 | 17 | ns | |
| $t_{PHL}$ | | | 23 | 34 | | |
| $t_{PLH}$ | $\overline{EI}$ to $A_n$ | | 12 | 18 | ns | |
| $t_{PHL}$ | | | 14 | 21 | | |
| $t_{ZH}$ | $G_1$ or $G_2$ to $A_n$ | | 23 | 40 | ns | |
| $t_{ZL}$ | | | 20 | 37 | | |
| $t_{ZH}$ | $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to $A_n$ | | 20 | 30 | ns | |
| $t_{ZL}$ | | | 18 | 27 | | |
| $t_{HZ}$ | $G_1$ or $G_2$ to $A_n$ | | 17 | 27 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 19 | 28 | | |
| $t_{HZ}$ | $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to $A_n$ | | 16 | 24 | ns | |
| $t_{LZ}$ | | | 18 | 27 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL: $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_i}$ to $A_n$ (In-phase) | | 31 | | 37 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 30 | | 34 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $A_n$ (Out-phase) | | 22 | | 27 | ns | |
| $t_{PHL}$ | | | 22 | | 25 | | |
| $t_{PLH}$ | $\overline{I_i}$ to $\overline{EO}$ | | 15 | | 18 | ns | |
| $t_{PHL}$ | | | 48 | | 60 | | |
| $t_{PLH}$ | $\overline{EI}$ to $\overline{EO}$ | | 19 | | 21 | ns | |
| $t_{PHL}$ | | | 46 | | 57 | | |
| $t_{PLH}$ | $\overline{EI}$ to $A_n$ | | 22 | | 25 | ns | |
| $t_{PHL}$ | | | 27 | | 32 | | |
| $t_{ZH}$ | $G_1$ or $G_2$ to $A_n$ | | 42 | | 49 | ns | |
| $t_{ZL}$ | | | 43 | | 49 | | |
| $t_{ZH}$ | $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to $A_n$ | | 36 | | 43 | ns | |
| $t_{ZL}$ | | | 35 | | 43 | | |
| $t_{HZ}$ | $G_1$ or $G_2$ to $A_n$ | | 34 | | 40 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 34 | | 40 | | |
| $t_{HZ}$ | $\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to $A_n$ | | 30 | | 35 | ns | |
| $t_{LZ}$ | | | 31 | | 35 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

## DEFINITIONS OF FUNCTIONAL TERMS

| | |
|---|---|
| $A0, A1, A2$ | Three-state, active high encoder outputs |
| $\overline{EI}$ | Enable input provided to allow cascaded operation |
| $\overline{EO}$ | Enable output provided to enable the next lower order priority chip |
| $G_1, G_2$ | Active high three-state output controls |
| $\overline{G}_3, \overline{G}_4, \overline{G}_5$ | Active low three-state output controls |
| $\overline{I}_{0-7}$ | Active low encoder inputs |

## TRUTH TABLE

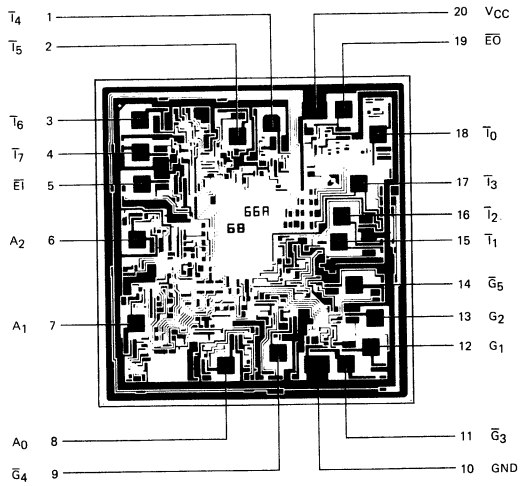
| Inputs | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{EI}$ | $\overline{I}_0$ | $\overline{I}_1$ | $\overline{I}_2$ | $\overline{I}_3$ | $\overline{I}_4$ | $\overline{I}_5$ | $\overline{I}_6$ | $\overline{I}_7$ | $A_0$ | $A_1$ | $A_2$ | $\overline{EO}$ |
| H | X | X | X | X | X | X | X | X | L | L | L | H |
| L | H | H | H | H | H | H | H | H | L | L | L | L |
| L | X | X | X | X | X | X | X | L | H | H | H | H |
| L | X | X | X | X | X | X | L | H | L | H | H | H |
| L | X | X | X | X | X | L | H | H | H | L | H | H |
| L | X | X | X | X | L | H | H | H | L | L | H | H |
| L | X | X | X | L | H | H | H | H | H | H | L | H |
| L | X | X | L | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | L | L | L | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For $G_1$ = H, $G_2$ = H, $G_3$ = L, $G_4$ = L, $G_5$ = L

| G1 | G2 | $\overline{G3}$ | $\overline{G4}$ | $\overline{G5}$ | $A_0$ | $A_1$ | $A_2$ |
|---|---|---|---|---|---|---|---|
| H | H | L | L | L | Enabled | | |
| L | X | X | X | X | Z | Z | Z |
| X | L | X | X | X | Z | Z | Z |
| X | X | H | X | X | Z | Z | Z |
| X | X | X | H | X | Z | Z | Z |
| X | X | X | X | H | Z | Z | Z |

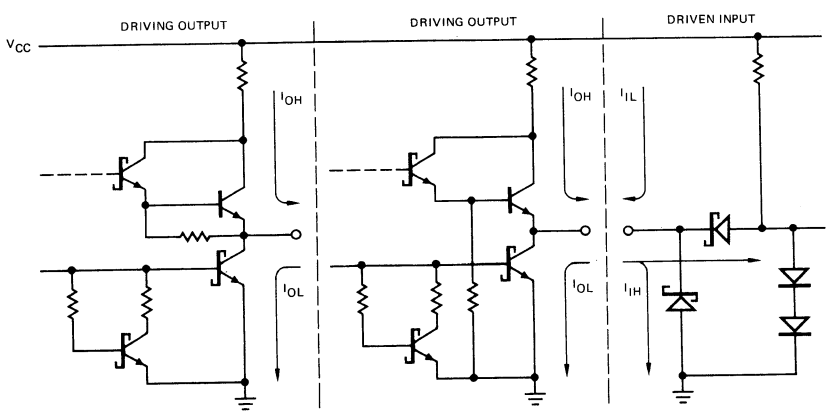
Z = HIGH Impedance

## Metallization and Pad Layout



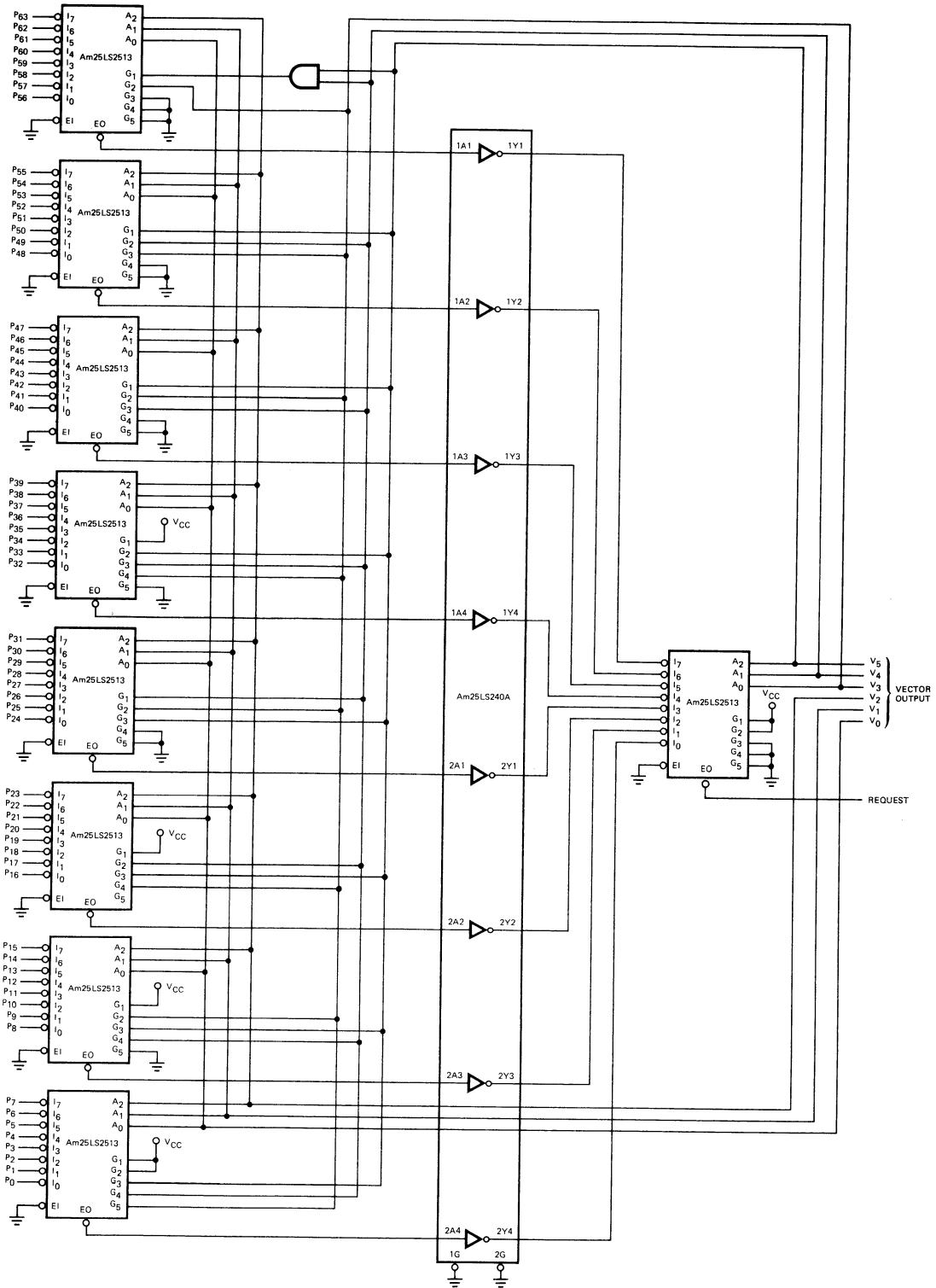

DIE SIZE 0.082 X 0.085

## Am25LS
## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## APPLICATION

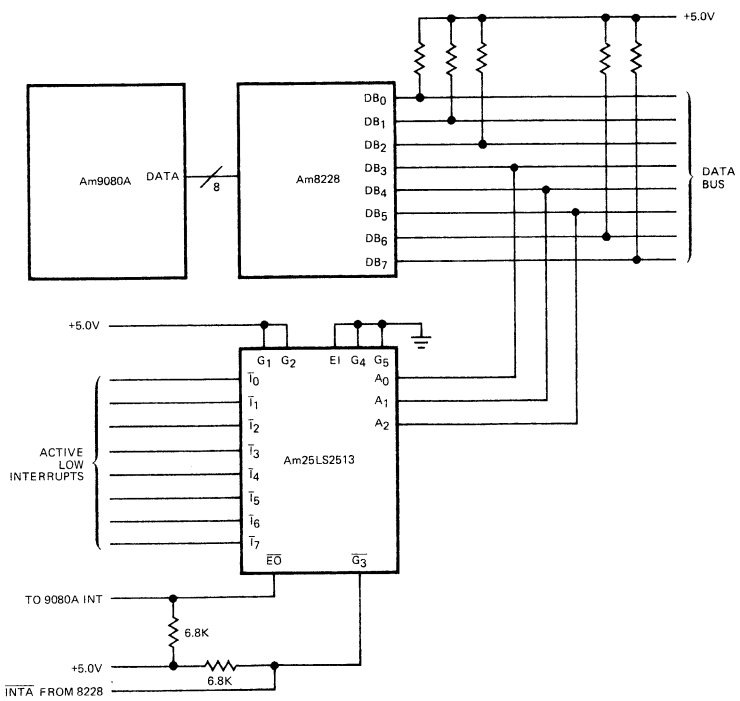



64 Input Priority Encoder Connected for Parallel Enable

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS2513 Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS2513PC |
| Hermetic DIP | 0°C to +70°C | AM25LS2513DC |
| Dice | 0°C to +70°C | AM25LS2513XC |
| Hermetic DIP | −55°C to +125°C | AM25LS2513DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS2513FM |
| Dice | −55°C to +125°C | AM25LS2513XM |

## PRIORITY ENCODED RST INTERRUPT INSTRUCTION FOR THE Am9080A



# Am25LS2516

## Eight-Bit By Eight-Bit Serial/Parallel Multiplier with Accumulator

### DISTINCTIVE CHARACTERISTICS

- Two's complement, two-bit lookahead carry-save arithmetic
- Microprogrammable — four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- Eight-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz (Typ)
- 100% product assurance screening to MIL-STD-883 requirements

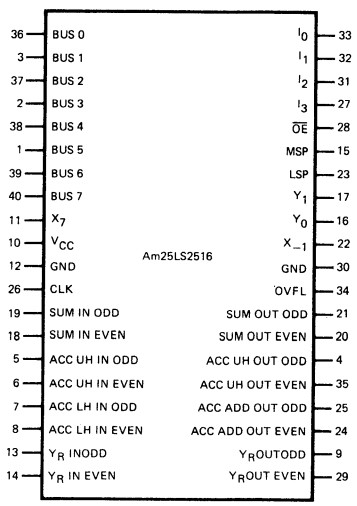
### FUNCTIONAL DESCRIPTION

The Am25LS2516 is an eight-bit by eight-bit multiplier and accumulator employing serial/parallel, two's complement, carry-save arithmetic to deliver a 16-bit product in eight clock cycles. The device is fully cascadable for use in high-speed, real-time, digital signal processing applications.

The device includes an eight-bit X Register prior to the X latch providing X hold for chain or overlapping calculations. The X and Y registers are loaded by clocking prior to the beginning of a multiply cycle, the data supplied by the bidirectional bus or the accumulator register. The double length, 16-bit output is multiplexed onto the eight-bit bus; either the upper or lower halves of the result can be read at any one time.

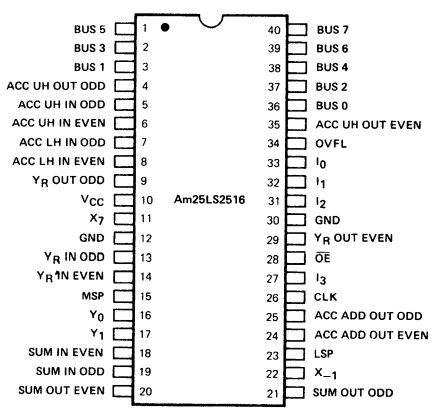
The accumulator and the Y register are both organized as dual-rank shift registers, allowing them to shift two bits at a time. The serial inputs and outputs of the Y register, the low and high order halves of the accumulator and the two-bit serial accumulator adder output, both serially and in parallel, are all available at external pins to provide cascadability.

### LOGIC SYMBOL



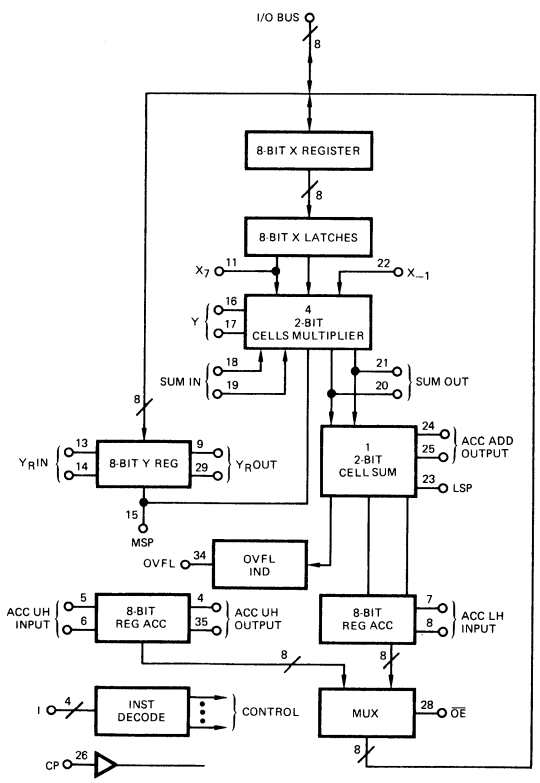

MPR-336

### CONNECTION DIAGRAM




MPR-337

### LOGIC DIAGRAM

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## Am25LS2516
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

## DC CHARACTERISTICS OVER OPERATING RANGE

### (Bus Inputs/Outputs)

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$ | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.8 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 60 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 5.5V$ | | | | 0.2 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −30 | | −100 | mA |

### (Non-Bus Inputs/Outputs)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$ | 2.5 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $Y_{ROUT}$, $I_{OL} = 15mA$ | | | 0.5 | Volts |
| | | | Others $I_{OL} = 4.0mA$ | | | 0.4 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | $Y_0$, $Y_1$ | | | 0.8 | Volts |
| | | | Others, MIL | | | 0.7 | |
| | | | Others, COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | See Table 1 | | | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | See Table 1 | | | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 5.5V$ | | See Table 1 | | | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −30 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 230 | 315 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## TABLE 1

| Terminals | $I_{IL}$ | $I_{IH}$ | $I_I$ |
|---|---|---|---|
| Y in, $I_0$, $I_1$, $I_3$, OE | 0.4mA | 20μA | 0.1mA |
| Sum in, $X_{-1}$, $I_2$, | 0.8mA | 40μA | 0.2mA |
| Bus 0-7 | 0.8mA | 50μA | 0.3mA |
| CP, LSP | 1.6mA | 80μA | 0.4mA |
| ACC in all | 2.0mA | 120μA | 0.6mA |
| MSP | 2.6mA | 140μA | 0.7mA |
| $Y_0$, $Y_1$ | 7.2mA | 360μA | −2.0mA |

## SWITCHING CHARACTERISTICS

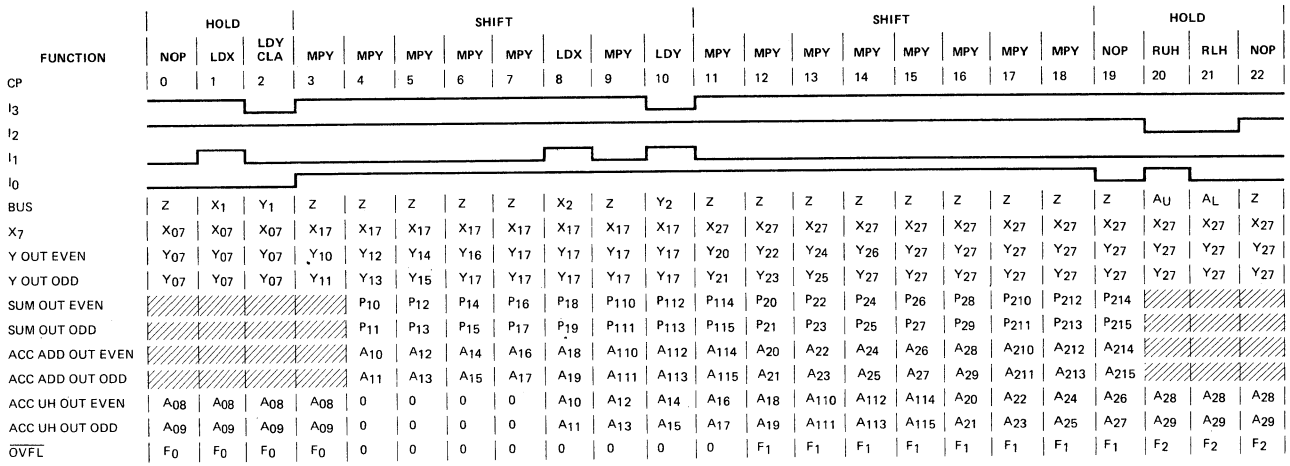
($T_A$ = +25°C, $V_{CC}$ = 5.0 V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | $Y_R$ Register Out | | 15 | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PLH}$ | | | 12 | | | |
| $t_{PHL}$ | Sum Out | | 13 | | ns | |
| $t_{PLH}$ | | | 13 | | | |
| $t_{PHL}$ | ACC Adder Out | | 20 | | ns | |
| $t_{PLH}$ | | | 27 | | | |
| $t_{PHL}$ | ACC UH Out | | 13 | | ns | |
| $t_{PLH}$ | | | 12 | | | |
| $t_{PHL}$ | ACC Bus | | 22 | | ns | |
| $t_{PLH}$ | | | 25 | | | |
| $t_{PHL}$ | $\overline{OVFL}$ | | 17 | | ns | |
| $t_{PLH}$ | | | 16 | | | |
| $t_{PHL}$ | $X_7$ | | 20 | | ns | |
| $t_{PLH}$ | | | 15 | | | |
| $t_{ZH}$ | $\overline{OE}$ to Bus | | 11 | | ns | |
| $t_{ZL}$ | | | 8 | | | |
| $t_{HZ}$ | | | 28 | | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 22 | | | |
| $t_S$ | X Register (Bus) | 25 | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_S$ | Y Register (Bus) | 25 | | | ns | |
| $t_S$ | X − 1 | 33 | | | ns | |
| $t_S$ | Sum In | 33 | | | ns | |
| $t_S$ | Y Register (Serial) | 25 | | | ns | |
| $t_S$ | ACC LH In | 8 | | | ns | |
| $t_S$ | ACC UH In | 8 | | | ns | |
| $t_S$ | Y EVEN and Y ODD | 33 | | | ns | |
| $t_S$ | Instruction | | | | ns | |
| $t_h$ | Hold Time on All Inputs | 5 | | | ns | |

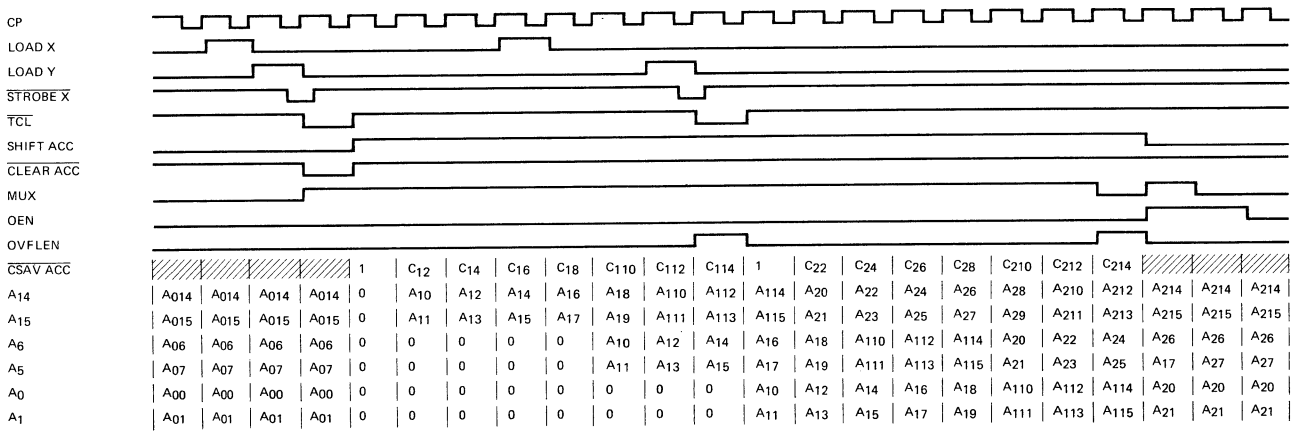
## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +6.3V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage (Pins 5, 6, 7, 8, 18, 19, 26) | −0.5V to +5.5V |
| DC Input Voltage (Other pins) | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

# TIMING DIAGRAMS



| | HOLD | | | SHIFT | | | | | | | | SHIFT | | | | | | | | HOLD | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FUNCTION | NOP | LDX | LDY CLA | MPY | MPY | MPY | MPY | MPY | LDX | MPY | LDY | MPY | MPY | MPY | MPY | MPY | MPY | MPY | MPY | NOP | RUH | RLH | NOP |
| CP | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
| $I_3$ | | | | | | | | | | | | | | | | | | | | | | | |
| $I_2$ | | | | | | | | | | | | | | | | | | | | | | | |
| $I_1$ | | | | | | | | | | | | | | | | | | | | | | | |
| $I_0$ | | | | | | | | | | | | | | | | | | | | | | | |
| BUS | Z | $X_1$ | $Y_1$ | Z | Z | Z | Z | Z | $X_2$ | Z | $Y_2$ | Z | Z | Z | Z | Z | Z | Z | Z | Z | $A_U$ | $A_L$ | Z |
| $X_7$ | $X_{07}$ | $X_{07}$ | $X_{07}$ | $X_{17}$ | $X_{17}$ | $X_{17}$ | $X_{17}$ | $X_{17}$ | $X_{17}$ | $X_{17}$ | $X_{17}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ | $X_{27}$ |
| Y OUT EVEN | $Y_{07}$ | $Y_{07}$ | $Y_{07}$ | $Y_{10}$ | $Y_{12}$ | $Y_{14}$ | $Y_{16}$ | $Y_{17}$ | $Y_{17}$ | $Y_{17}$ | $Y_{17}$ | $Y_{20}$ | $Y_{22}$ | $Y_{24}$ | $Y_{26}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ |
| Y OUT ODD | $Y_{07}$ | $Y_{07}$ | $Y_{07}$ | $Y_{11}$ | $Y_{13}$ | $Y_{15}$ | $Y_{17}$ | $Y_{17}$ | $Y_{17}$ | $Y_{17}$ | $Y_{17}$ | $Y_{21}$ | $Y_{23}$ | $Y_{25}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ | $Y_{27}$ |
| SUM OUT EVEN | | | | | $P_{10}$ | $P_{12}$ | $P_{14}$ | $P_{16}$ | $P_{18}$ | $P_{110}$ | $P_{112}$ | $P_{114}$ | $P_{20}$ | $P_{22}$ | $P_{24}$ | $P_{26}$ | $P_{28}$ | $P_{210}$ | $P_{212}$ | $P_{214}$ | | | | |
| SUM OUT ODD | | | | | $P_{11}$ | $P_{13}$ | $P_{15}$ | $P_{17}$ | $P_{19}$ | $P_{111}$ | $P_{113}$ | $P_{115}$ | $P_{21}$ | $P_{23}$ | $P_{25}$ | $P_{27}$ | $P_{29}$ | $P_{211}$ | $P_{213}$ | $P_{215}$ | | | | |
| ACC ADD OUT EVEN | | | | | $A_{10}$ | $A_{12}$ | $A_{14}$ | $A_{16}$ | $A_{18}$ | $A_{110}$ | $A_{112}$ | $A_{114}$ | $A_{20}$ | $A_{22}$ | $A_{24}$ | $A_{26}$ | $A_{28}$ | $A_{210}$ | $A_{212}$ | $A_{214}$ | | | | |
| ACC ADD OUT ODD | | | | | $A_{11}$ | $A_{13}$ | $A_{15}$ | $A_{17}$ | $A_{19}$ | $A_{111}$ | $A_{113}$ | $A_{115}$ | $A_{21}$ | $A_{23}$ | $A_{25}$ | $A_{27}$ | $A_{29}$ | $A_{211}$ | $A_{213}$ | $A_{215}$ | | | | |
| ACC UH OUT EVEN | $A_{08}$ | $A_{08}$ | $A_{08}$ | $A_{08}$ | 0 | 0 | 0 | 0 | $A_{10}$ | $A_{12}$ | $A_{14}$ | $A_{16}$ | $A_{18}$ | $A_{110}$ | $A_{112}$ | $A_{114}$ | $A_{20}$ | $A_{22}$ | $A_{24}$ | $A_{26}$ | $A_{28}$ | $A_{28}$ | $A_{28}$ |
| ACC UH OUT ODD | $A_{09}$ | $A_{09}$ | $A_{09}$ | $A_{09}$ | 0 | 0 | 0 | 0 | $A_{11}$ | $A_{13}$ | $A_{15}$ | $A_{17}$ | $A_{19}$ | $A_{111}$ | $A_{113}$ | $A_{115}$ | $A_{21}$ | $A_{23}$ | $A_{25}$ | $A_{27}$ | $A_{29}$ | $A_{29}$ | $A_{29}$ |
| $\overline{OVFL}$ | $F_0$ | $F_0$ | $F_0$ | $F_0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $F_1$ | $F_1$ | $F_1$ | $F_1$ | $F_1$ | $F_1$ | $F_1$ | $F_1$ | $F_2$ | $F_2$ | $F_2$ |



| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{CSAV\ ACC}$ | | | | | 1 | $C_{12}$ | $C_{14}$ | $C_{16}$ | $C_{18}$ | $C_{110}$ | $C_{112}$ | $C_{114}$ | 1 | $C_{22}$ | $C_{24}$ | $C_{26}$ | $C_{28}$ | $C_{210}$ | $C_{212}$ | $C_{214}$ | | | | |
| $A_{14}$ | $A_{014}$ | $A_{014}$ | $A_{014}$ | $A_{014}$ | 0 | $A_{10}$ | $A_{12}$ | $A_{14}$ | $A_{16}$ | $A_{18}$ | $A_{110}$ | $A_{112}$ | $A_{114}$ | $A_{20}$ | $A_{22}$ | $A_{24}$ | $A_{26}$ | $A_{28}$ | $A_{210}$ | $A_{212}$ | $A_{214}$ | $A_{214}$ | $A_{214}$ |
| $A_{15}$ | $A_{015}$ | $A_{015}$ | $A_{015}$ | $A_{015}$ | 0 | $A_{11}$ | $A_{13}$ | $A_{15}$ | $A_{17}$ | $A_{19}$ | $A_{111}$ | $A_{113}$ | $A_{115}$ | $A_{21}$ | $A_{23}$ | $A_{25}$ | $A_{27}$ | $A_{29}$ | $A_{211}$ | $A_{213}$ | $A_{215}$ | $A_{215}$ | $A_{215}$ |
| $A_6$ | $A_{06}$ | $A_{06}$ | $A_{06}$ | $A_{06}$ | 0 | 0 | 0 | 0 | 0 | $A_{10}$ | $A_{12}$ | $A_{14}$ | $A_{16}$ | $A_{18}$ | $A_{110}$ | $A_{112}$ | $A_{114}$ | $A_{20}$ | $A_{22}$ | $A_{24}$ | $A_{26}$ | $A_{26}$ | $A_{26}$ |
| $A_5$ | $A_{07}$ | $A_{07}$ | $A_{07}$ | $A_{07}$ | 0 | 0 | 0 | 0 | 0 | $A_{11}$ | $A_{13}$ | $A_{15}$ | $A_{17}$ | $A_{19}$ | $A_{111}$ | $A_{113}$ | $A_{115}$ | $A_{21}$ | $A_{23}$ | $A_{25}$ | $A_{17}$ | $A_{27}$ | $A_{27}$ |
| $A_0$ | $A_{00}$ | $A_{00}$ | $A_{00}$ | $A_{00}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_{10}$ | $A_{12}$ | $A_{14}$ | $A_{16}$ | $A_{18}$ | $A_{110}$ | $A_{112}$ | $A_{114}$ | $A_{20}$ | $A_{20}$ | $A_{20}$ |
| $A_1$ | $A_{01}$ | $A_{01}$ | $A_{01}$ | $A_{01}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_{11}$ | $A_{13}$ | $A_{15}$ | $A_{17}$ | $A_{19}$ | $A_{111}$ | $A_{113}$ | $A_{115}$ | $A_{21}$ | $A_{21}$ | $A_{21}$ |

KEY:
////// Data invalid

Note: Variables shown are general.
For this example:

$P_1 = X_1Y_1$ $A_1 = P_1$ $F_1 = 0$
$P_2 = X_2Y_2$ $A_2 = P_1 + P_2$

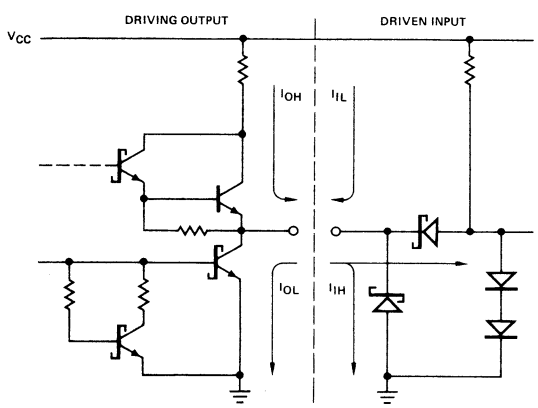
## FUNCTION TABLE

| Mnemonic | $I_3$ $I_2$ $I_1$ $I_0$ | Function | CLR M | LOAD X | LOAD Y | XFER X | CLR A* | SHFT A | MUX | OE | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| YLHC | 0 0 0 0 | LHA → Y, XFER X, CLR A CLR M, READ OVFL | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| YUHC | 0 0 0 1 | UHA → Y, XFER X, CLR A CLR M, READ OVFL | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| YLHA | 0 0 1 0 | LHA → Y, XFER X CLR M, READ OVFL | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | |
| YUHA | 0 0 1 1 | UHA → Y, XFER X CLR M, READ OVFL | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | |
| LYCA | 0 1 0 0 | LOAD Y, XFER X, CLR A, CLR M | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Same Func. as 0101 |
| LYCA | 0 1 0 1 | CLR A LOAD Y, XFER X, CLR M | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Same Func. as 0100 |
| LYHA | 0 1 1 0 | LOAD Y, XFER X, HOLD A, CLR M | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | |
| LYSA | 0 1 1 1 | LOAD Y, XFER X, SHIFT A CLR M, MULTIPLY | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | OVFLEN in Next State |
| RLHA | 1 0 0 0 | READ LHA READ OVFL | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | |
| RUHA | 1 0 0 1 | READ UHA READ OVFL | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | |
| XLHA | 1 0 1 0 | LHA → X READ OVFL | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | |
| XUHA | 1 0 1 1 | UHA → X READ OVFL | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| NOOP | 1 1 0 0 | NO OP OVFLEN AFTER MULT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Must Prc'd Any Output |
| MULT | 1 1 0 1 | MULTIPLY SHIFT A | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | |
| LXHA | 1 1 1 0 | LOAD X, HOLD A | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | |
| LXSA | 1 1 1 1 | LOAD X, SHIFT A MULTIPLY | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | |

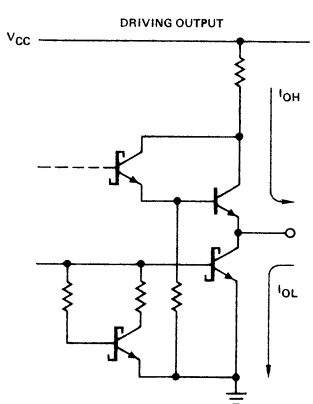
*Active LOW

## Am25LS
## LOW-POWER SCHOTTKY INPUT/OUTPUT
## CURRENT INTERFACE CONDITIONS

### Other Outputs




### Bus Outputs




Note: Actual current flow direction shown

## DEFINITION OF FUNCTIONAL TERMS

**Bus 0-Bus 7** – Bi-directional 8-bit data bus.

**X7** – Interconnection link from more significant byte if cascading (output).

**X1** – Interconnecting link between devices to least significant byte if cascading (input) link X7 to X1 to cascade - must be ground if not used.

**Accum Upper Half out, even** – Accumulator output upper byte, even bit.

**Accum Upper Half out, odd** – Accumulator output upper byte, odd bit.

**Accum Upper Half input even** – Accumulator input, upper byte, even bit.

**Accum Upper Half input odd** – Accumulator input, upper byte, odd bit.

**Accum Lower Half input even** – Accumulator input, lower byte, even bit.

**Accum Lower Half input odd** – Accumulator input, lower byte, odd bit.

**YR out even** – "Y" register output, even (link to "$Y_0$").

**YR out odd** – "Y" register output, odd (link to "$Y_1$").

**YR in even** – "Y" register input, even (link for cascading) ground when not used.

**YR in odd** – "Y" register input, odd (link for cascading) ground when not used.

**$Y_0$** – Multiplier odd input (link to Y reg. odd).

**$Y_1$** – Multiplier even input (link to Y reg. even).

**Sum in even** – Multiplier input even for cascading link to more significant byte, for standalone, ground.

**Sum in odd** – Multiplier input odd for cascading link to more significant byte, for standalone, ground.

**Sum out even** – Multiplier output even (link to sum in even for cascading) can be used directly.

**Sum out odd** – Multiplier output odd (link to sum output odd for cascading) can be used directly.

**Acc Add out, even** – Adder output even, for LSB (Hi) output equal sum of Accum and multiplier, for LSB (low) output equal sum of accumulator and zero.

**Acc Add out, odd** – Same as above except odd bit instead of even.

**LSB** – Control for summing adder – See Accumulator Add outputs for definition.

**$I_0$-$I_3$** – 4-bit instruction field – provide cycle for cycle control of device function.

**onfl** – Stored overflow indicator used only on least significant byte. Requires proper execution of instruction to operate.

**MSB** – Control for "Y" reg. and multiplier to indicate Most Significant Byte – Activates sign extension and negative waiting for 2's compliment – Low for lesser significant bytes and High for Most Significant Byte only.

**CP** – Clock Pulse

**$\overline{OE}$** – 3 state enable for Bus 0-Bus 7 outputs.

3

# THE Am25LS2516 LSI MULTIPLIER/ACCUMULATOR

By Roy Levy

The Am25LS2516 is an 8-bit Multiplier/Accumulator designed for medium performance, minimum power, real time signal processing applications such as digital filtering, Fast Fourier Transforms, and statistical correlation. Using two's complement carry-save arithmetic, this 40-pin LSI device delivers a 16-bit product in eight clock cycles. This will permit two devices to be cascaded to achieve a 16-bit by 16-bit multiplication in 940ns when used over the full military operating range.

A functional block diagram of the Am25LS2516 is shown in Figure 1. The key elements are an 8-bit X input register followed by an 8-bit X latch, an 8-bit Y register, four 2-bit multipliers, a 2-bit adder, two 8-bit accumulators (high order and low order), a byte selecting multiplexer and instruction decode logic. These components, equivalent to approximately 625 gate elements, are integrated onto a single chip fabricated using Advanced Micro Devices' high-performance, Low-Power Schottky technology. The on-chip accumulator is provided to minimize component count and power dissipation in a high density system. It also allows completion of a multiply and accumulate operation in the same time normally required for a multiply only. Other LSI multipliers currently available require the accumulator function to be provided externally.

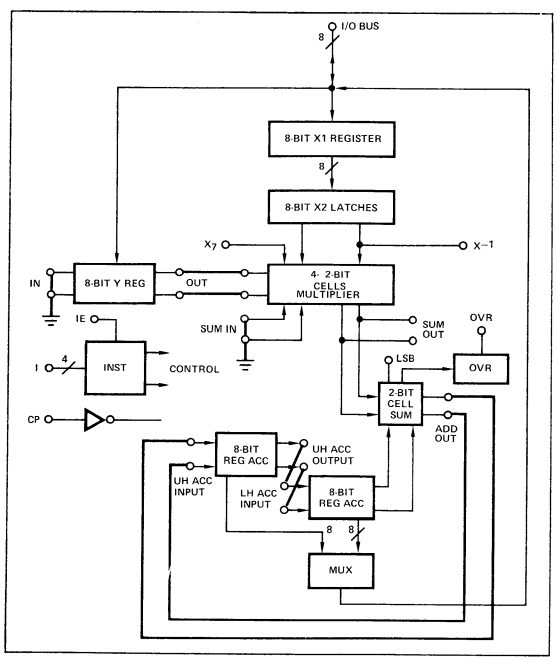



**Figure 1. 8-Bit by 8-Bit Multiplier Block Diagram with External Connections Required to Accumulate A 16-Bit Product.**

## MULTIPLIER OPERATION

The Am25LS2516 is configured around an eight-line common input/output bidirectional bus. X and Y input and accumulator output data are routed via these bus lines. A two-rank register/latch combination is used for the X input to allow chaining of successive multiplies without losing a clock pulse; i.e., multiply and load vs. multiply. The latch holds the "X" data for the multiplier, allowing the X register to be loaded during any remaining multiply cycles. The "Y" Register can be parallel loaded, by command, from the 8-bit, on-chip bus from either the incoming 8 bits, or the Accumulator High or Accumulator Low Register (separate commands). The "Y" Register provides the 2-bit-at-a-time shift and the sign extend which allows the four 2-bit cells to operate in a serial by parallel mode. The multiplier produces a 2-bit product for each clock, LSB's first. Its output is accepted by the 2-bit adder as well as presented to external pins for expansion. A control gating array is provided to test for overflow during the last add cycle of the operation; i.e., cycle 8 for 8-bit multiply and cycle 16 for 16-bit multiply. The timing and control of this specific cycle is accomplished by the microcode chosen. The "no-op" and "LYSA" instructions are provided for this purpose. The first cycle of a no-op following a multiply will cause the results of the overflow test to be stored. Two 8-bit accumulators are provided which must be externally connected in either an 8-bit, 16-bit, or greater configuration.

These accumulators as well as the Y Register, are both organized as dual-rank shift registers, which allow them to shift two bits at a time. The serial inputs and outputs of the Y Register and the low and high order halves of the accumulator are all brought out to external pins for cascading the device.

The accumulator output is available both serially and in parallel. The accumulator results are available one bit later than the multiply cycle and the accumulator stops shifting during read cycles. If the device is used to compute X • Y products without accumulation, a minimum of two overhead cycles must accompany each multiply - - one for reading the upper (lower) half of the accumulator and one for clearing of the accumulator during the loading of the X or Y Registers. An output multiplixer selects the high or low order accumulator contents for presentation to the bus in parallel 8 bits at a time.

The heart of this device is an 8-bit multiplier (Figure 2) made up of four 2-bit cells. Each cell has three inputs (2 bits wide), two dual carry-save full adders, with four flip-flops for temporary storage (two for carry-save and two for partial product). The multiplier is actually subdivided into two separate adders with appropriate carry-save. The last adder forms a partial sum representing 0, 1X, 2X, or 3X by using combinations of X and 2X. The control of this combination is $Y_0$ and $Y_1$, respectively, to form $Y_0X_n + Y_iX_{n+1}$. This sum (nX) is the input for the second adder. The second adder combines the first adder (nX) sum with the stored partial product

shifted two places plus carry to form a new partial product.

$$P_{0MSB} + \Sigma_0 + C = P_{0LSB}$$

$$P_{1MSB} + \Sigma_1 + C = P_{1LSB}$$

The two partial product bits of the least significant cell are made available to the SUMmer and the SUM out terminals. The LSB input controls the SUM out providing a pass through or add dependent on polarity.

## PROGRAMMING THE MULTIPLIER

The Am25LS2516 is an externally programmed device controlled by four instruction lines. This programmability provides a key to its flexibility. Sixteen microinstructions (see Table 1) are provided, which can be grouped into three major functions: Data Move, Read, and Multiply.

Instruction 0-4: The first instructions ("0", "1", "2", "3") load the "Y" Register from the Accumulator (high or low), load the "X" Register while either clearing or not clearing, respectively, the Accumulator.

The next four instructions ("4", "5", "6", "7") load the "Y" Register from external "bus" and Holds on the accumulators and multiplier.

Instruction "7" is unique and is used to execute a chain multiply. It provides the last multiply operation while loading the "Y" Register, transferring the "X", and clearing the multiplier.

Instructions "8" and "9" provide the read-out (upper and lower halves) of the Accumulator.

Instructions "A" and "B" internally transfer the respective halves of the Accumulator to the "X" Register – another method of chain calculating.

Instruction "C" is a true no-op and provides an idling instruction without disabling the clock. NOTE: The operations of the instruction are in some cases stored by clocking the instructions into an instruction register, accounting for a clocked delay in operations. Specifically, the shifting of the Accumulator is an internally stored command and as such is started and stopped one clock cycle late, allowing the Accumulator to complete its data shifting during the first no-op cycle following a multiply and starting it one clock cycle after the multiplying cycle is started.

Instruction "D" is a single iteration of the multiply and must be used for each bit in the multiplier minus one. The last bit of the multiplier will be handled by a no-op ("C") or a load Y and multiply (7).

**TABLE I**

| MNEMONIC | INSTRUCTION $I_3I_2I_1I_0$ IN HEX | FUNCTION | REMARKS | |
|---|---|---|---|---|
| YLHC | 0 | LHA→Y, XFER X, CLR A<br>CLR M, READ OVFL | | |
| YUHC | 1 | UHA→Y, XFER X, CLR A<br>CLR M, READ OVFL | | |
| YLHA | 2 | LHA→Y, XFER X<br>CLR M, READ OVFL | | |
| YUHA | 3 | UHA→Y, XFER X<br>CLR M, READ OVFL | | |
| LYCA | 4 | LOAD Y, XFER X, CLR A<br>CLR M | Same function as 5 | |
| LYCA | 5 | CLR A<br>LOAD Y, XFER X, CLR M | Same function as 4 | |
| LYHA | 6 | LOAD Y, XFER X, HOLD A<br>CLR M | | |
| LYSA | 7 | LOAD Y, XFER X, SHIFT A<br>CLR M, MULTIPLY | Enables overflow store in next state | * |
| RLHA | 8 | READ LHA<br>READ OVFL | | |
| RUHA | 9 | READ UHA<br>READ OVFL | | |
| XLHA | A | LHA→X<br>READ OVFL | | |
| XUHA | B | UHA→Y<br>READ OVFL | | |
| NOOP | C | NO OP | Enable overflow store | |
| MULT | D | MULTIPLY<br>SHIFT A | | * |
| LXHA | E | LOAD X, HOLD A | | |
| LXSA | F | LOAD X, SHIFT A<br>MULTIPLY | | * |

*Continue multiplying instructions

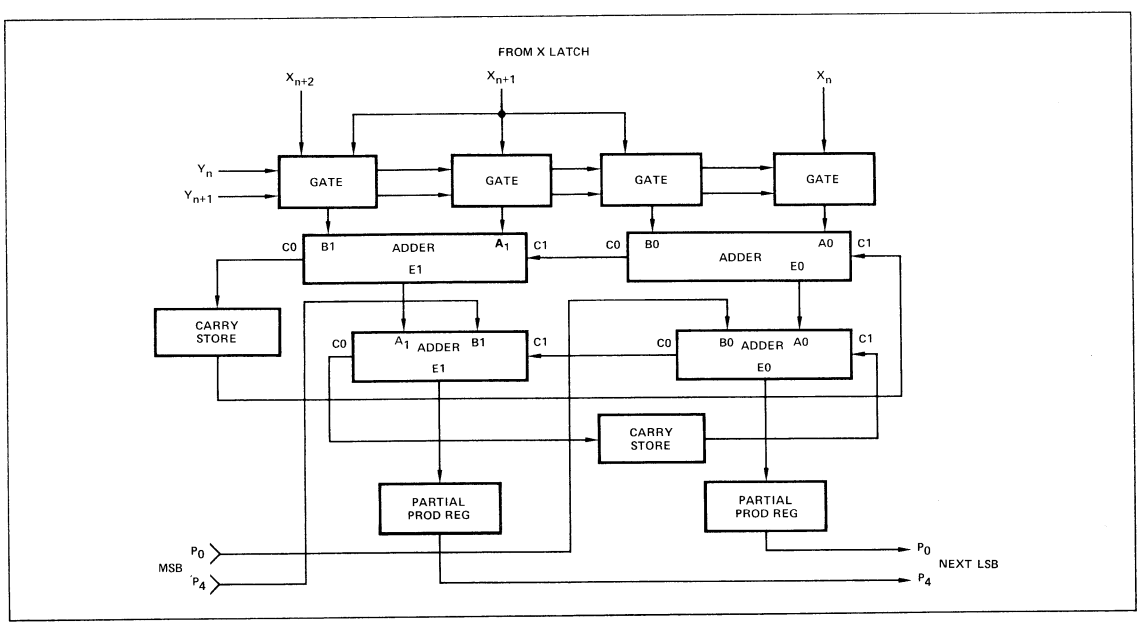



**Figure 2. Am25LS2516 Multiplier Cell.**

Instruction "E" provides a load "X" Register and Hold.

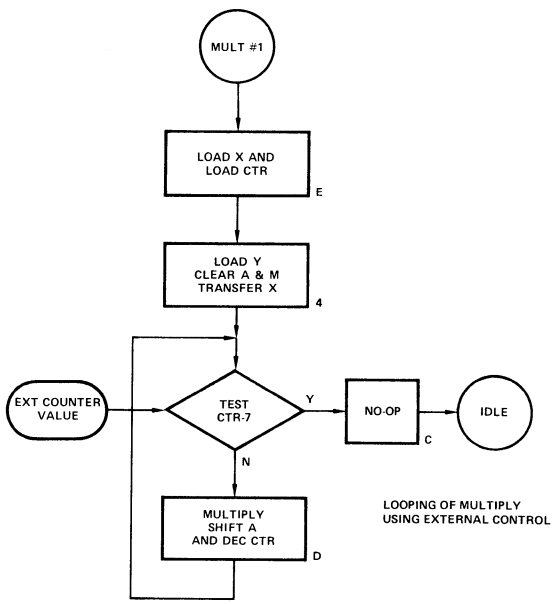
Instruction "F" provides an intermediate instruction which can be executed during a multiply. It allows the "X" Register to load without disturbing the "X" Latch, while continuing the iteration of the multiply.

Instructions "C" and "7" also provide sampling and storage of the overflow condition.

## APPLICATION OF THE MULTIPLIER

The flow diagram for an 8-bit two's complement multiply is shown in Figure 3, together with the required program micro-steps. Figure 4 extends this to include accumulate, intermediate load of X and chain calculations. Figures 5a and b show the external connection of two Am25LS2516 devices to execute a 16-bit by 16-bit multiplication. A 32-bit product is completed in 16 clock cycles. This same technique may be extended in a similar fashion to longer word lengths. The flowchart of Figure 6 demonstrates a 16-bit two's complement multiply without accumulate, modified to a 12-bit by 12-bit function.

The Am25LS2516 Multiplier/Accumulator is the most complex LSI product manufactured to date with Low Power Schottky technology. It will be extremely useful in high-density applications where minimum package count is a primary consideration. The device itself performs an 8 x 8 or 16 x 16 multiplication in approximately twice the time of parallel multipliers currently available, but using only one quarter the power in the multiplier portion of the function. In a fully configured system using both techniques, the Am25LS2516 performance begins to approach that of the parallel multiplier plus supporting devices.




PROGRAM MICRO STEPS

| # | INST IN HEX |
|---|---|
| 1 | E |
| 2 | 4 |
| 3 | D |
| 4 | D |
| 5 | D |
| 6 | D |
| 7 | D |
| 8 | D |
| 9 | D |
| 10 | C |
| | IDLE |

**Figure 3. 8-Bit Two's Complement Multiply without Accumulate or Chain.**

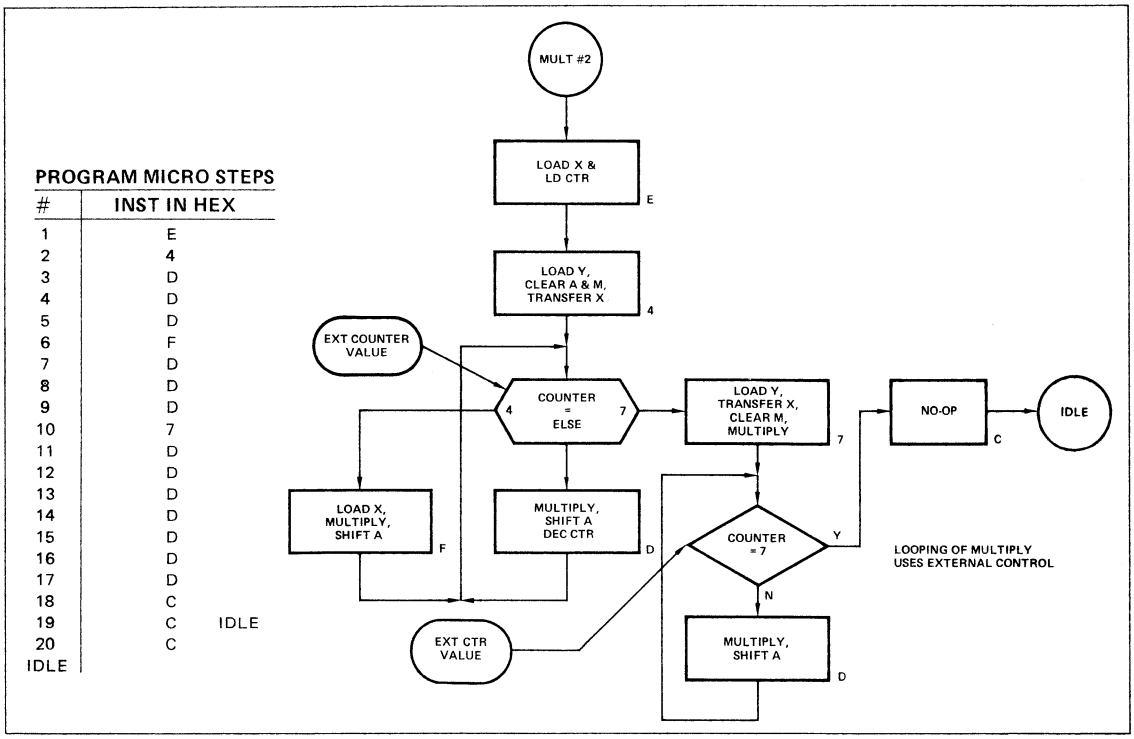



**Figure 4. 8-Bit Two's Complement Multiply with Accumulate, Intermediate Load and Chain Calculations.**

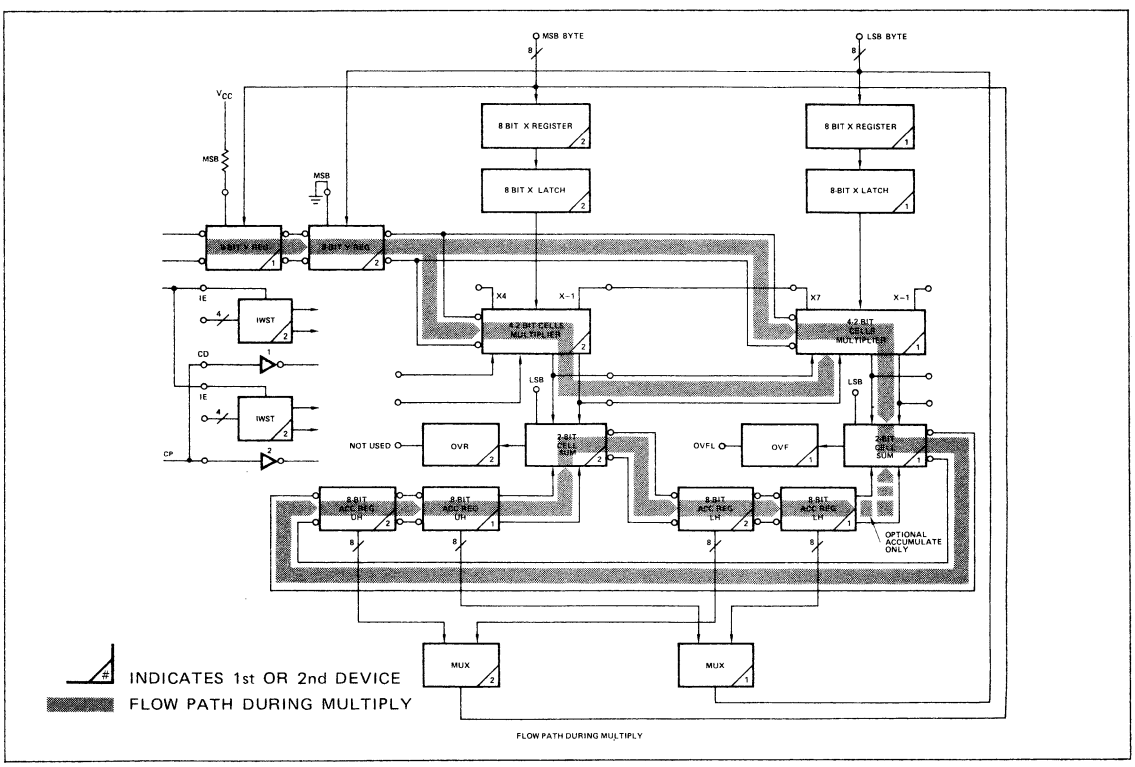



**Figure 5a. Interconnection of Two Am25LS2516 (8 x 8 Multiplier) Devices to Execute a 16 x 16 Multiply.**

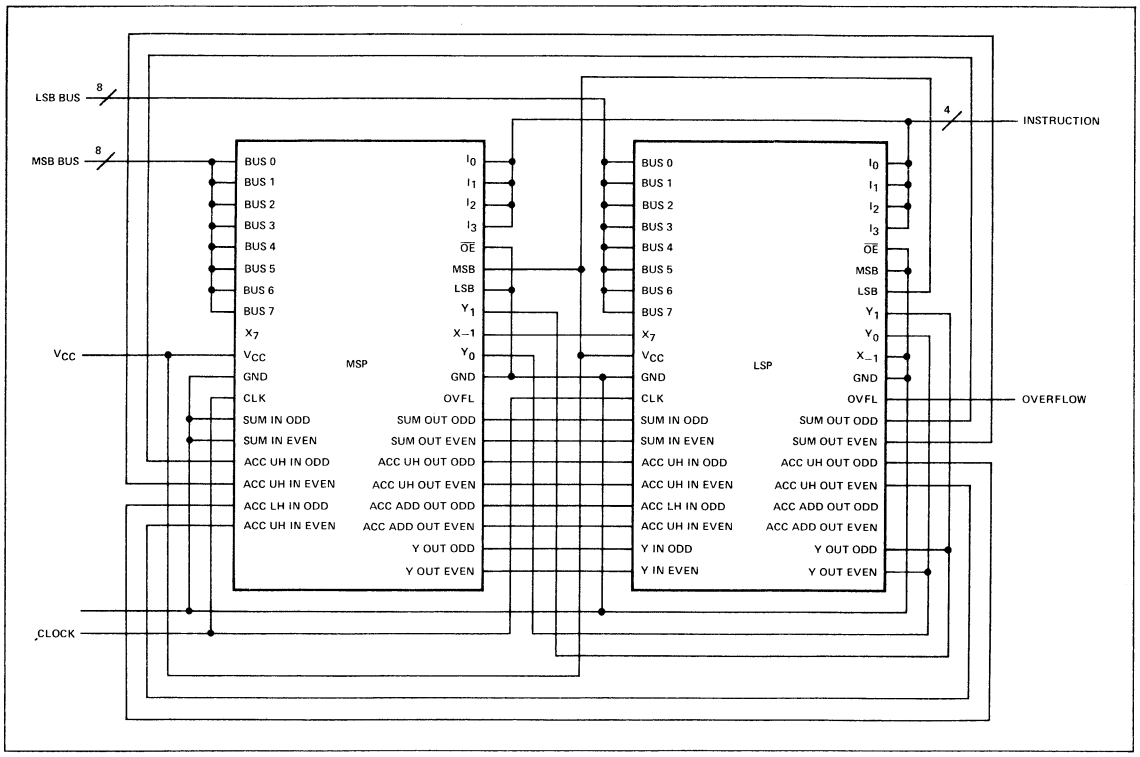



**Figure 5b. Two Devices Cascaded in 16-Bit by 16-Bit Multiplier Application with 32-Bit Accumulated Product.**

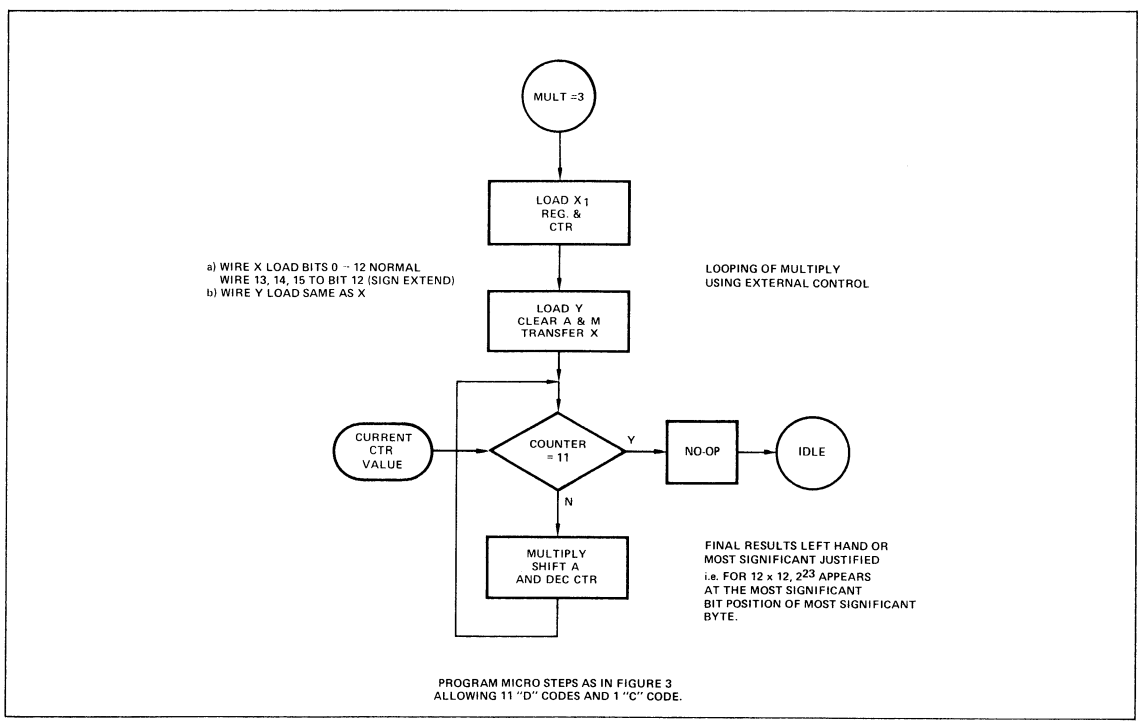



**Figure 6. 16 Bit Two's Complement Multiply without Accumulate Modified to 12 x 12 (Using Two Am25LS2516 Devices Interconnected).**

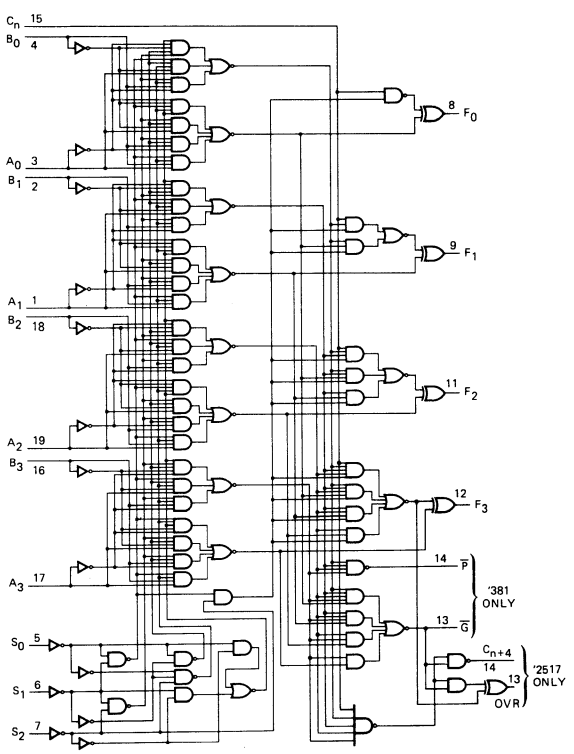
# Am25LS2517

## Arithmetic Logic Unit/Function Generator

**Am25LS2517 data is combined with the Am25LS381.**

**See Am25LS381 data sheet for full information.**

### LOGIC DIAGRAM




Note: The Advanced Micro Devices' LS381 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

### FUNCTIONAL DESCRIPTION

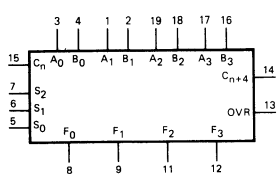
The Am25LS381 and Am54LS/74LS381 are arithmetic logic units (ALU)/function generators that perform three arithmetic operations and three logic operations on two 4-bit words. The device can also output forced 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs $S_0$, $S_1$ and $S_2$ as shown in the function table. Full carry look ahead is used over the four-bit field within the device. When devices are cascaded, multi-level full carry look-ahead is implemented using a '182 carry look ahead generator and the $\overline{G}$ and $\overline{P}$ outputs on the Am25LS381 or Am54LS/74LS381. The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. If the $C_{n+4}$ carry output function is required, the Am25LS2517 should be used.

The Am25LS381 is a high-performance version of the Am54LS/74LS381. Improvements include faster a. c. specifications, higher noise margin and twice the fan-out over the military temperature range.

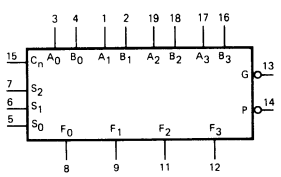
The Am25LS2517 is an arithmetic logic unit (ALU)/function generator that performs three arithmetic operations and three logic operations on two 4-bit words. The device can also force output 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs $S_0$, $S_1$ and $S_2$ as shown in the function table. Full carry look-ahead is used over the four-bit field within the device. When devices are cascaded, the carry output ($C_{n+4}$) is connected to the carry input ($C_n$) of the next device. The Am25LS2517 can also detect two's complement overflow. The overflow output (OVR) is defined logically as $C_{n+3} \oplus C_{n+4}$.

### LOGIC SYMBOLS

**Am25LS2517**



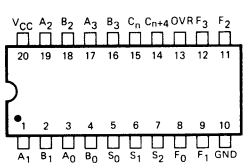

**Am25LS381**
**Am54LS/74LS381**



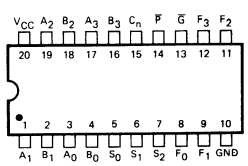

$V_{CC}$ = Pin 20
GND = Pin 10

### CONNECTION DIAGRAMS
Top Views

**Am25LS2517**




**Am25LS381**
**Am54LS/74LS381**




Note: Pin 1 is marked for orientation.

# Am25LS2518

## Quad D Register With Standard And Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918 and Am25S18
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- Second sourced by T. I. as the SN54/74LS388
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

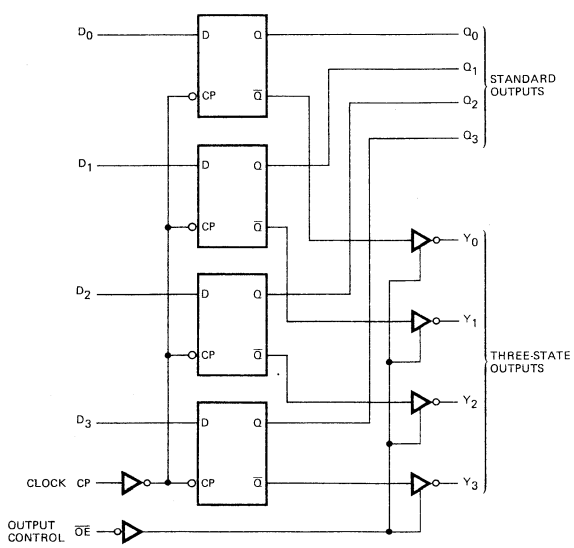
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

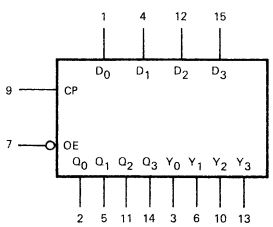
The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

### LOGIC DIAGRAM

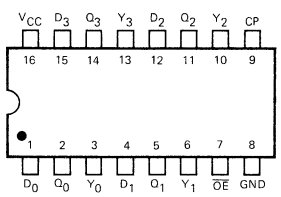



### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## Am25LS2518

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | Q, $I_{OH} = -660\mu A$ | MIL | 2.5 | 3.4 | | Volts |
| | | | | COM'L | 2.7 | 3.4 | | |
| | | | Y | MIL, $I_{OH} = -1.0mA$ | 2.4 | 3.4 | | |
| | | | | COM'L, $I_{OH} = 2.6mA$ | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| | | | $I_{OL} = 12mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 17 | 28 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $I_{CC}$ is measured with all inputs at 4.5V and all outputs open.

## Am25LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Q_i$ | | | 18 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 18 | 27 | | |
| $t_{PLH}$ | Clock to $Y_i$ ($\overline{OE}$ LOW) | | | 18 | 27 | ns | |
| $t_{PHL}$ | | | | 18 | 27 | | |
| $t_{pw}$ | Clock Pulse Width | LOW | 18 | | | ns | |
| | | HIGH | 15 | | | | |
| $t_s$ | Data | | 15 | | | ns | |
| $t_h$ | Data | | 5.0 | | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 7.0 | 11 | ns | |
| $t_{ZL}$ | | | | 8 | 12 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 14 | 21 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 12 | 18 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 35 | 50 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% | | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10% | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ | Clock to $Q_i$ | | | 38 | | 45 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 38 | | 45 | | |
| $t_{PLH}$ | Clock to $Y_i$ ($\overline{OE}$ LOW) | | | 35 | | 40 | ns | |
| $t_{PHL}$ | | | | 35 | | 40 | | |
| $t_{pw}$ | Clock Pulse Width | LOW | 20 | | 20 | | ns | |
| | | HIGH | 20 | | 20 | | | |
| $t_s$ | Data | | 15 | | 15 | | ns | |
| $t_h$ | Data | | 5.0 | | 5.0 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 15 | | 17 | ns | |
| $t_{ZL}$ | | | | 16 | | 17 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 27 | | 30 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 24 | | 30 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 30 | | 25 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The four data inputs to the register.

**$Q_i$** The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

**$Y_i$** The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the $Y_i$ outputs to the high-impedance state.

**CP** Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

**$\overline{OE}$** Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the $Y_i$ outputs.

## TRUTH TABLE

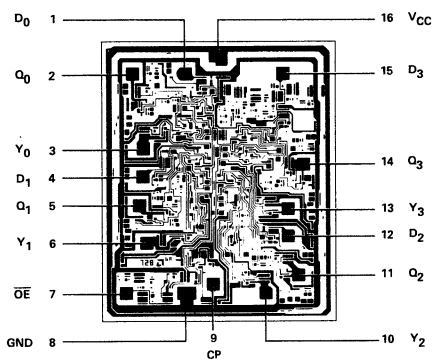
| INPUTS | | | OUTPUTS | | NOTES |
|---|---|---|---|---|---|
| $\overline{OE}$ | CLOCK CP | D | Q | Y | |
| H | L | X | NC | Z | – |
| H | H | X | NC | Z | – |
| H | ↑ | L | L | Z | – |
| H | ↑ | H | H | Z | – |
| L | ↑ | L | L | L | – |
| L | ↑ | H | H | H | – |
| L | – | – | L | L | 1 |
| L | – | – | H | H | 1 |

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

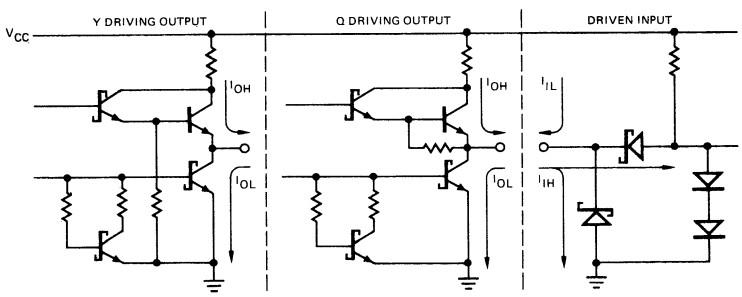
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

### Metallization and Pad Layout




DIE SIZE 0.083" X 0.099"

### Am25LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

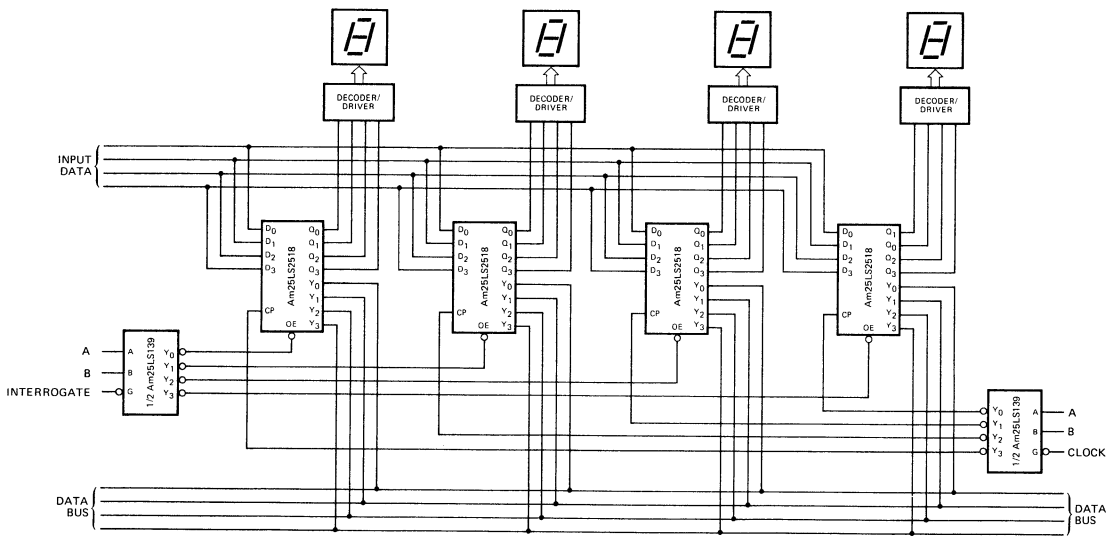



Note: Actual current flow direction shown.

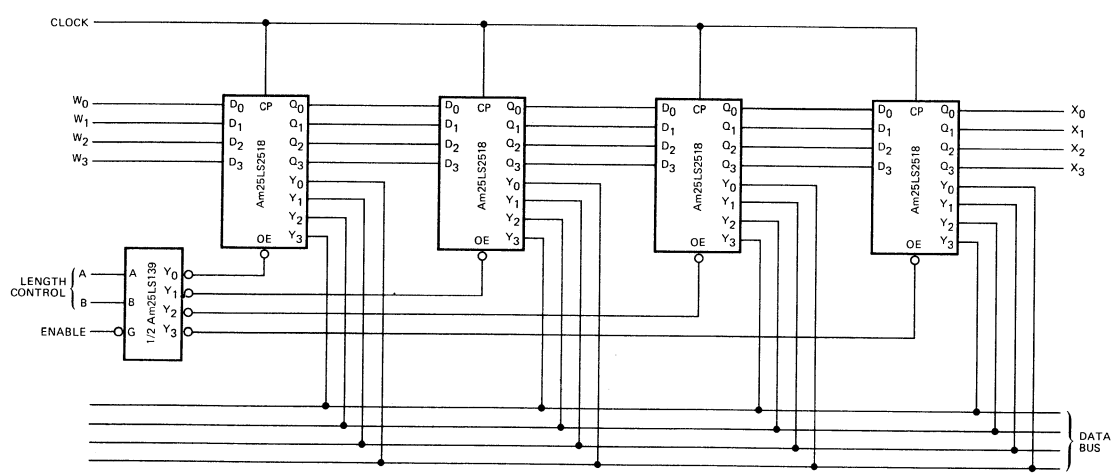
## ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS2518PC |
| Hermetic DIP | 0°C to +70°C | AM25LS2518DC |
| Dice | 0°C to +70°C | AM25LS2518XC |
| Hermetic DIP | −55°C to +125°C | AM25LS2518DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS2518FM |
| Dice | −55°C to +125°C | AM25LS2518XM |

## APPLICATIONS




The Am25LS2518 used as display register with bus interrogate capability.




The Am25LS2518 as a variable length (1, 2, 3 or 4 word)shift register.

# Am25LS2519

## Quad Register With Two Independently Controlled Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs
- 100% product assurance screening to MIL-STD-883 requirements

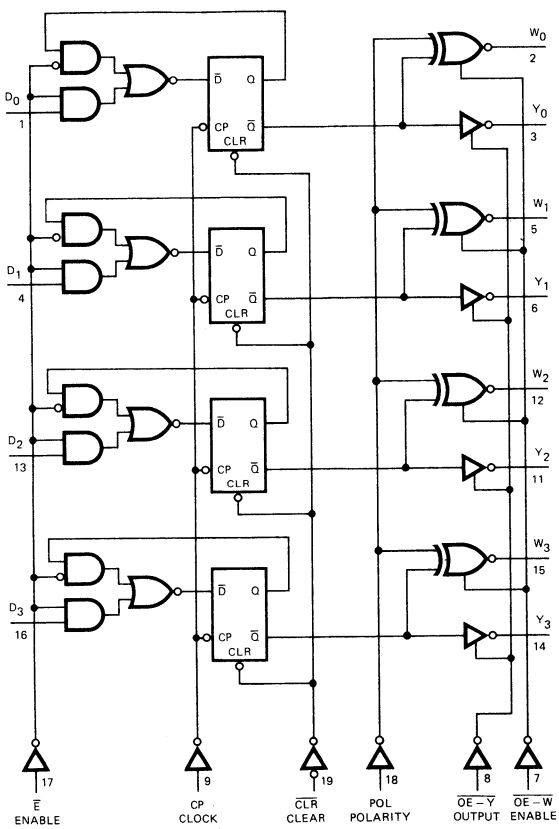
### FUNCTIONAL DESCRIPTION

The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

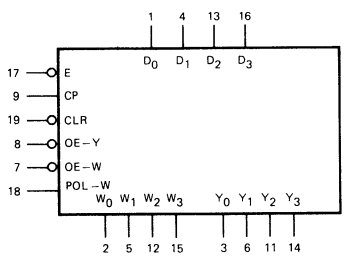
The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

3

### LOGIC DIAGRAM

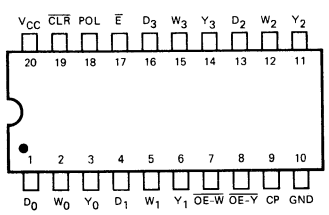



### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| | | | $I_{OL} = 12mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | MIL | | 24 | 36 | mA |
| | | | | COM'L | | 24 | 39 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

## Am25LS

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Clock to $Y_i$ | | | 22 | 33 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 20 | 30 | | |
| $t_{PLH}$ | Clock to $W_i$ (Either Polarity) | | | 24 | 36 | ns | |
| $t_{PHL}$ | | | | 24 | 36 | | |
| $t_{PHL}$ | Clear to $Y_i$ | | | 29 | 43 | ns | |
| $t_{PLH}$ | Clear to $W_i$ | | | 25 | 37 | ns | |
| $t_{PHL}$ | | | | 30 | 45 | | |
| $t_{PLH}$ | Polarity to $W_i$ | | | 23 | 34 | ns | |
| $t_{PHL}$ | | | | 25 | 37 | | |
| $t_{pw}$ | Clear | | 18 | | | ns | |
| $t_{pw}$ | Clock Pulse Width | LOW | 15 | | | ns | |
| | | HIGH | 18 | | | | |
| $t_s$ | Data | | 15 | | | ns | |
| $t_h$ | Data | | 5 | | | ns | |
| $t_s$ | Data Enable | | 20 | | | ns | |
| $t_h$ | Data Enable | | 0 | | | ns | |
| $t_s$ | Set-up Time, Clear Recovery (Inactive) to Clock | | 20 | 15 | | ns | |
| $t_{ZH}$ | Output Enable to W or Y | | | 11 | 17 | ns | |
| $t_{ZL}$ | | | | 13 | 20 | | |
| $t_{HZ}$ | Output Enable to W or Y | | | 13 | 20 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 11 | 17 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 35 | 45 | | MHz | $C_L$ = 15pF, $R_L$ = 2.0kΩ |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

3

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Y_i$ | | | 39 | | 42 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 39 | | 45 | | |
| $t_{PLH}$ | Clock to $W_i$ (Either Polarity) | | | 41 | | 43 | ns | |
| $t_{PHL}$ | | | | 44 | | 48 | | |
| $t_{PHL}$ | Clear to $Y_i$ | | | 52 | | 58 | ns | |
| $t_{PLH}$ | Clear to $W_i$ | | | 42 | | 43 | ns | |
| $t_{PHL}$ | | | | 51 | | 53 | | |
| $t_{PLH}$ | Polarity to $W_i$ | | | 41 | | 45 | ns | |
| $t_{PHL}$ | | | | 42 | | 44 | | |
| $t_{pw}$ | Clear | | 20 | | 20 | | ns | |
| $t_{pw}$ | Clock | LOW | 20 | | 20 | | ns | |
| | | HIGH | 20 | | 20 | | | |
| $t_s$ | Data | | 15 | | 15 | | ns | |
| $t_h$ | Data | | 10 | | 10 | | ns | |
| $t_s$ | Data Enable | | 25 | | 25 | | ns | |
| $t_h$ | Data Enable | | 0 | | 0 | | ns | |
| $t_s$ | Set-up Time, Clear Recovery (Inactive) to Clock | | 23 | | 24 | | ns | |
| $t_{ZH}$ | Output Enable to $W_i$ or $Y_i$ | | | 24 | | 27 | ns | |
| $t_{ZL}$ | | | | 29 | | 35 | | |
| $t_{HZ}$ | Output Enable to $W_i$ or $Y_i$ | | | 33 | | 45 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 22 | | 26 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 30 | | 25 | | MHz | $C_L$ = 50pF, $R_L$ = 2.0kΩ |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## FUNCTION TABLE

| FUNCTION | INPUTS | | | | | | | INTERNAL | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | CP | $D_i$ | $\overline{E}$ | $\overline{CLR}$ | POL | $\overline{OE\text{-}W}$ | $\overline{OE\text{-}Y}$ | Q | $W_i$ | $Y_i$ |
| Output Three-State Control | X | X | X | X | X | H | L | NC | Z | Enabled |
| | X | X | X | X | X | L | H | NC | Enabled | Z |
| | X | X | X | X | X | H | H | NC | Z | Z |
| | X | X | X | X | X | L | L | NC | Enabled | Enabled |
| $W_i$ Polarity | X | X | X | X | L | L | L | NC | Non-Inverting | Non-Inverting |
| | X | X | X | X | H | L | L | NC | Inverting | Non-Inverting |
| Asynchronous Clear | X | X | X | L | L | L | L | L | L | L |
| | X | X | X | L | H | L | L | L | H | L |
| Clock Enabled | ↑ | X | H | H | X | X | X | NC | NC | NC |
| | ↑ | L | L | H | L | L | L | L | L | L |
| | ↑ | L | L | H | H | L | L | L | H | L |
| | ↑ | H | L | H | L | L | L | H | H | H |
| | ↑ | H | L | H | H | L | L | H | L | H |

L = LOW
H = HIGH
Z = High Impedance
X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

## DEFINITION OF FUNCTIONAL TERMS

**$D_i$** — Any of the four D flip-flop data lines.

**$\overline{E}$** — Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.

**CP** — Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.

**$\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$** — Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.

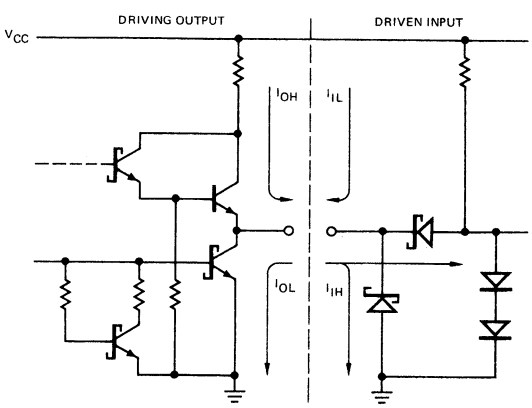
**$Y_i$** — Any of the four non-inverting three-state output lines.

**$W_i$** — Any of the four three-state outputs with polarity control.

**POL** — Polarity Control. The $W_i$ outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.

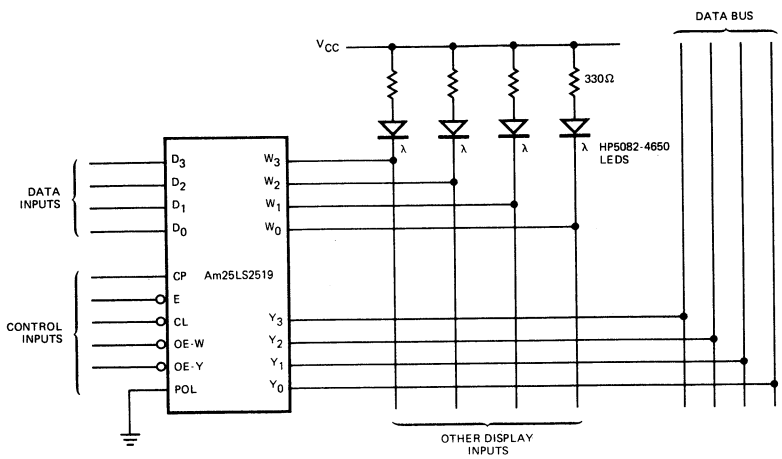
**$\overline{CLR}$** — Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

### Am25LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

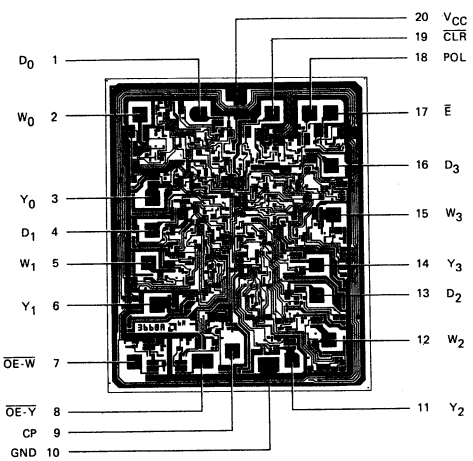
## APPLICATION




**Convenient Register Content Monitor or Test Point**

3

**Metallization and Pad Layout**




DIE SIZE 0.083" X 0.099"

# Am25LS2520

## Octal D-Type Flip-Flop With Clear, Clock Enable And Three-State Control

### DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- Am25LS Family offers improved sink current, source current and noise margin
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS2520 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

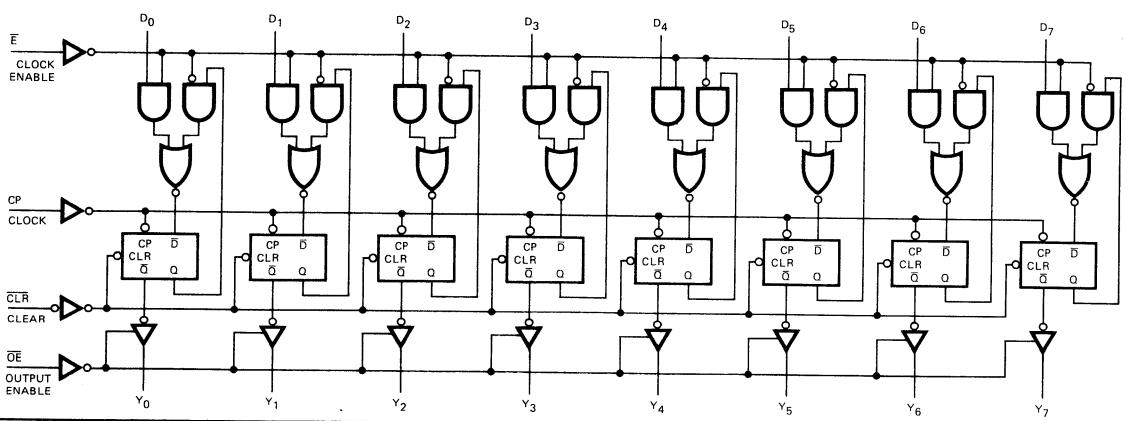
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

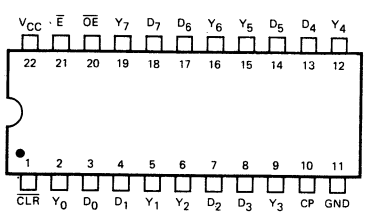
The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package.

### LOGIC DIAGRAM

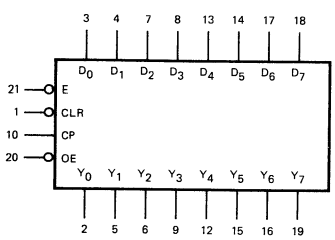



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 22
GND = Pin 11

## Am25LS2520
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_O$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 24 | 37 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

3

## Am25LS
## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Y_i$ (OE LOW) | | | 18 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 24 | 36 | | |
| $t_{PHL}$ | Clear to Y | | | 22 | 35 | ns | |
| $t_s$ | Data ($D_i$) | | 10 | 3 | | ns | |
| $t_h$ | Data ($D_i$) | | 10 | 3 | | ns | |
| $t_s$ | Enable ($\overline{E}$) | Active | 15 | 10 | | ns | |
| | | Inactive | 20 | 12 | | | |
| $t_h$ | Enable ($\overline{E}$) | | 0 | 0 | | ns | |
| $t_s$ | Clear Recovery (In-Active) to Clock | | 11 | 7 | | ns | |
| $t_{pw}$ | Clock | HIGH | 20 | 14 | | ns | |
| | | LOW | 25 | 13 | | | |
| $t_{pw}$ | Clear | | 20 | 13 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 9 | 13 | ns | |
| $t_{ZL}$ | | | | 14 | 21 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 20 | 30 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 24 | 36 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | | 40 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5% | | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10% | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ | Clock to $Y_i$ (OE LOW) | | | 33 | | 39 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 45 | | 54 | | |
| $t_{PHL}$ | Clear to Y | | | 43 | | 51 | ns | |
| $t_s$ | Data ($D_i$) | | 12 | | 15 | | ns | |
| $t_h$ | Data ($D_i$) | | 12 | | 15 | | ns | |
| $t_s$ | Enable ($\overline{E}$) | Active | 17 | | 20 | | ns | |
| | | Inactive | 20 | | 23 | | | |
| $t_h$ | Enable ($\overline{E}$) | | 0 | | 0 | | ns | |
| $t_s$ | Clear Recovery (In-Active) to Clock | | 13 | | 15 | | ns | |
| $t_{pw}$ | Clock | HIGH | 25 | | 30 | | ns | |
| | | LOW | 30 | | 35 | | | |
| $t_{pw}$ | Clear | | 22 | | 25 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 19 | | 25 | ns | |
| $t_{ZL}$ | | | | 30 | | 39 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 35 | | 40 | ns | $C_L$ = 5.0 pF, $R_L$ = 2.0 kΩ |
| $t_{LZ}$ | | | | 39 | | 42 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The D flip-flop data inputs.

**$\overline{CLR}$** When the clear input is LOW, the $Q_i$ outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

**CP** Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

**$Y_i$** The register three-state outputs.

**$\overline{E}$** Clock Enable, When the clock enable is LOW, data on the $D_i$ input is transferred to the $Q_i$ output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the $Q_i$ outputs do not change state, regardless of the data or clock input transitions.

**$\overline{OE}$** Output Control. When the $\overline{OE}$ input is HIGH, the $Y_i$ outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the $Y_i$ outputs.

## FUNCTION TABLE

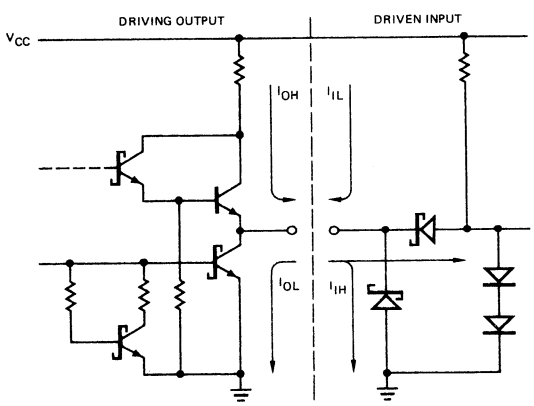
| | Inputs | | | | | Internal | Outputs |
|---|---|---|---|---|---|---|---|
| Function | $\overline{OE}$ | $\overline{CLR}$ | $\overline{E}$ | $D_i$ | CP | $Q_i$ | $Y_i$ |
| Hi-Z | H | X | X | X | X | X | Z |
| Clear | H | L | X | X | X | L | Z |
| | L | L | X | X | X | L | L |
| Hold | H | H | H | X | X | NC | Z |
| | L | H | H | X | X | NC | NC |
| Load | H | H | L | L | ↑ | L | Z |
| | H | H | L | H | ↑ | H | Z |
| | L | H | L | L | ↑ | L | L |
| | L | H | L | H | ↑ | H | H |

H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

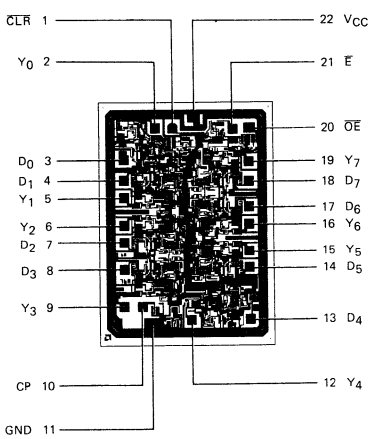
3

## Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## Metallization and Pad Layout

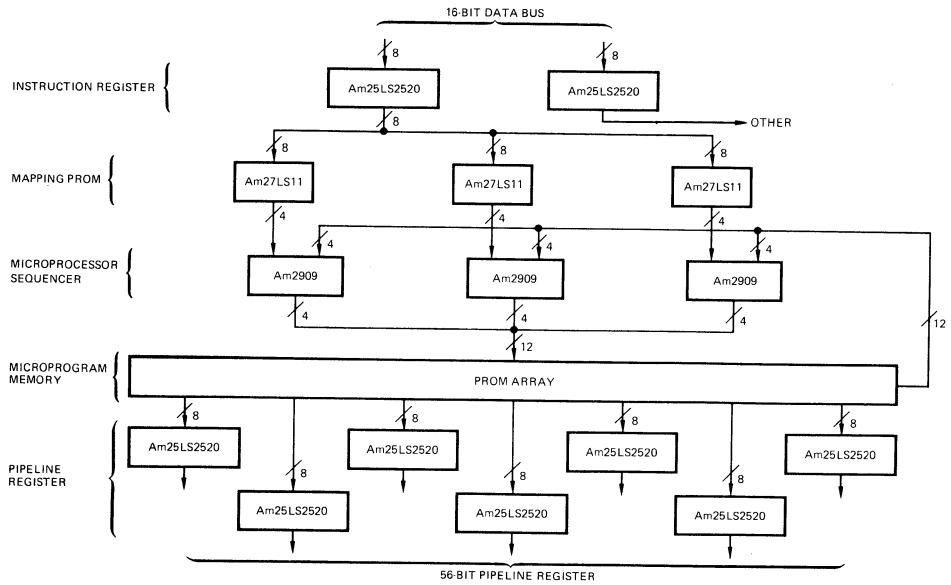



DIE SIZE 0.080" x 0.111"

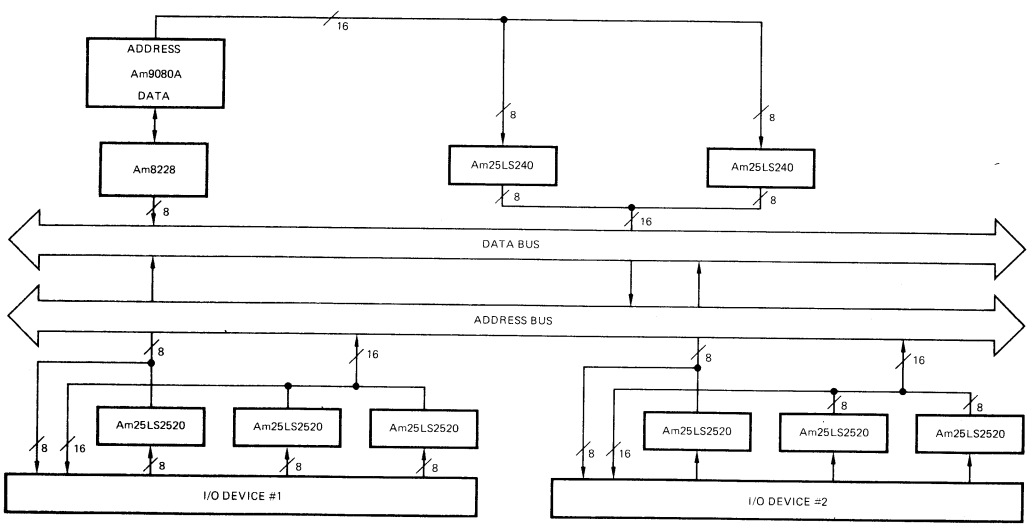
## ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS2520PC |
| Hermetic DIP | 0°C to +70°C | AM25LS2520DC |
| Dice | 0°C to +70°C | AM25LS2520XC |
| Hermetic DIP | −55°C to +125°C | AM25LS2520DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS2520FM |
| Dice | −55°C to +125°C | AM25LS2520XM |

## APPLICATIONS




A typical Computer Control Unit for a microprogrammed machine.




The Am25LS2520 is a useful device in interfacing with the Am9080A system buses.

# Am25LS2521
## Eight-Bit Equal-To Comparator

### DISTINCTIVE CHARACTERISTICS

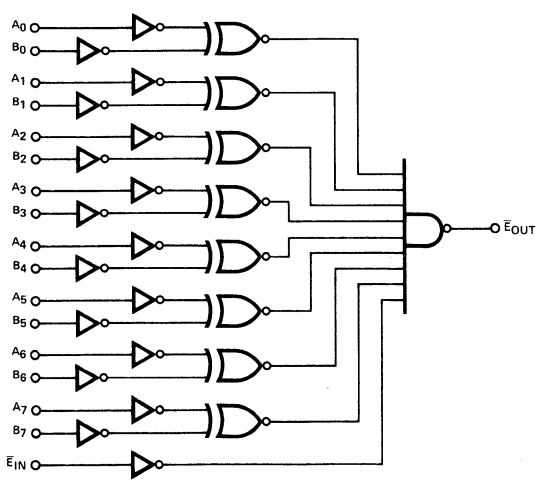
- 8-bit byte oriented equal comparator
- Cascadable using $\overline{E}_{IN}$
- High-speed, Low-Power Schottky technology
- $t_{pd}$ A • B to $\overline{E}_{OUT}$ in 9ns
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

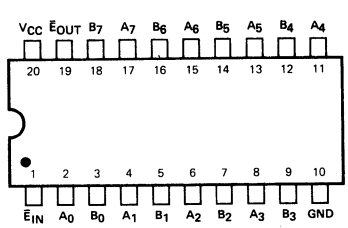
The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{E}_{IN}$ produces an active LOW on the output $\overline{E}_{OUT}$.

The logic expression for the device can be expressed as: $\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\ (A_1 \odot B_1)\ (A_2 \odot B_2)\ (A_3 \odot B_3)\ (A_4 \odot B_4)\ (A_5 \odot B_5)\ (A_7 \odot B_7)\ E_{IN}}$. It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. $A_0$ can be compared with $B_0$ at the same time $\overline{A}_1$ is compared with $\overline{B}_1$. It is only essential that the polarity of the paired terms be maintained.

### LOGIC DIAGRAM

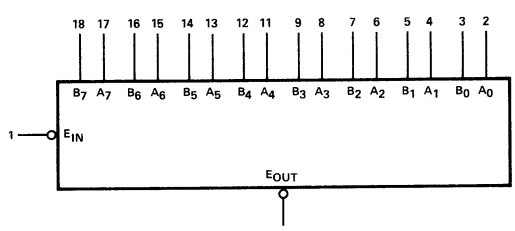



### CONNECTION DIAGRAM




Note: Pin 1 is marked for orientation

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OH} = -440\mu A$ | MIL | 2.5 | | | Volts |
| | | | COM'L | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| | | $I_{OL} = 12mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | $A_i$, $B_i$ | | | −0.36 | mA |
| | | | $\overline{E}$ | | | −0.72 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | $A_i$, $B_i$ | | | 20 | μA |
| | | | $\overline{E}$ | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | $A_i$, $B_i$ | | | 0.1 | mA |
| | | | $\overline{E}$ | | | 0.2 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 27 | 40 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{E}$ = GND, all other inputs and outputs open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{Equal}$ | | 9 | 15 | ns | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 9 | 15 | | |
| $t_{PLH}$ | $\overline{E}$ to $\overline{Equal}$ | | 5 | 7 | ns | |
| $t_{PHL}$ | | | 6 | 8 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE *

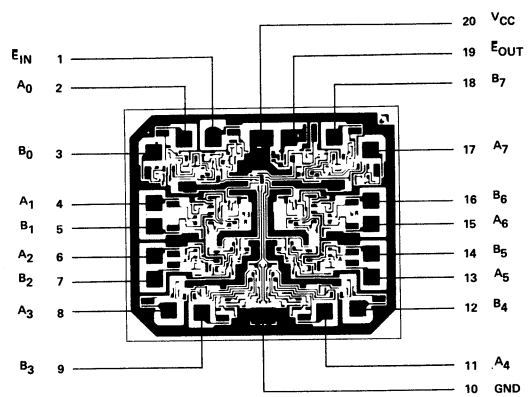
| Parameters | Description | Am25LS COM'L<br>$T_A$ = 0°C to +70°C<br>$V_{CC}$ = 5.0V ±5%<br>Min. | Max. | Am25LS MIL<br>$T_A$ = −55°C to +125°C<br>$V_{CC}$ = 5.0V ±10%<br>Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $A_i$ or $B_i$ to | | 20 | | 22 | ns | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | $\overline{Equal}$ Output | | 19 | | 21 | | |
| $t_{PLH}$ | $\overline{E}$ to $\overline{Equal}$ Output | | 10.5 | | 12 | ns | |
| $t_{PHL}$ | | | 12.5 | | 15 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### DEFINITION OF FUNCTIONAL TERMS

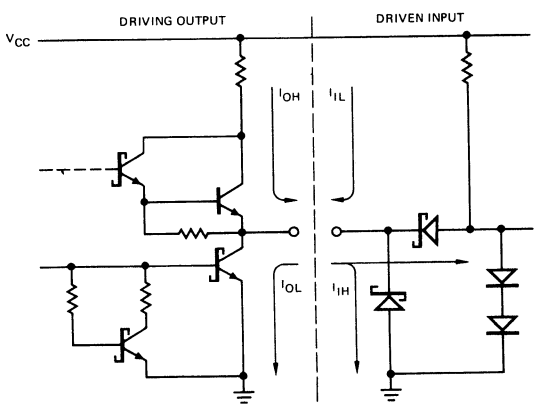
| | |
|---|---|
| $A_0$–$A_7$ | A input to comparator |
| $B_0$–$B_7$ | B input to comparator |
| $\overline{E}_{IN}$ | Enable active LOW |
| $\overline{E}_{OUT}$ | $\overline{EQUAL}$ output active LOW |

Metallization and Pad Layout




DIE SIZE 0.063" x 0.074"

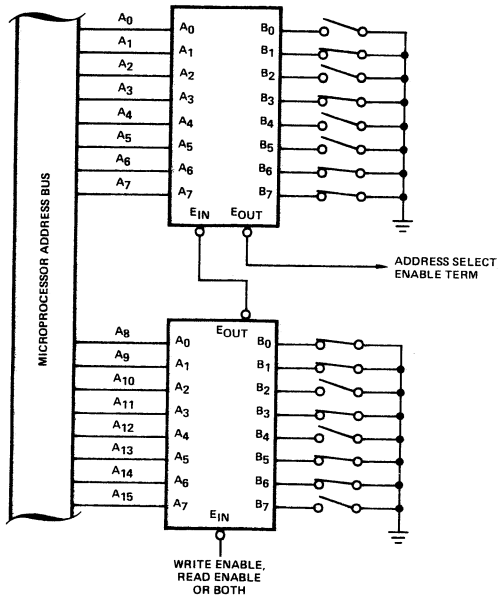
Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

3

## APPLICATION




**MAX. $\overline{\text{ENABLE}}$ (HIGH-to-LOW) DELAY OVER 16-BITS**
**(Commercial Range)**

| | | |
|---|---|---|
| $t_{PHL}$ | $A_i$ or $B_i$ to $\overline{E}_{OUT}$ | 19ns |
| $t_{PHL}$ | $\overline{E}_{IN}$ to $\overline{E}_{OUT}$ | 12.5ns |
| Total | | 31.5ns |

**MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER**

## ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS2521PC |
| Hermetic DIP | 0°C to +70°C | AM25LS2521DC |
| Dice | 0°C to +70°C | AM25LS2521XC |
| Hermetic DIP | −55°C to +125°C | AM25LS2521DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS2521FM |
| Dice | −55°C to +125°C | AM25LS2521XM |

# Am25LS2524
## Registered Comparator

### DISTINCTIVE CHARACTERISTICS

- Eight-bit bi-directional register with bus oriented input-output
- Independent serial input-output to register
- Register to bus comparator with equal to greater than and less than outputs
- Cascadable in groups of eight bits
- Comparator has open collector status outputs controlled by status enable
- Compare performed at 2's complement or magnitude
- Controlled by 2-bit function code
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

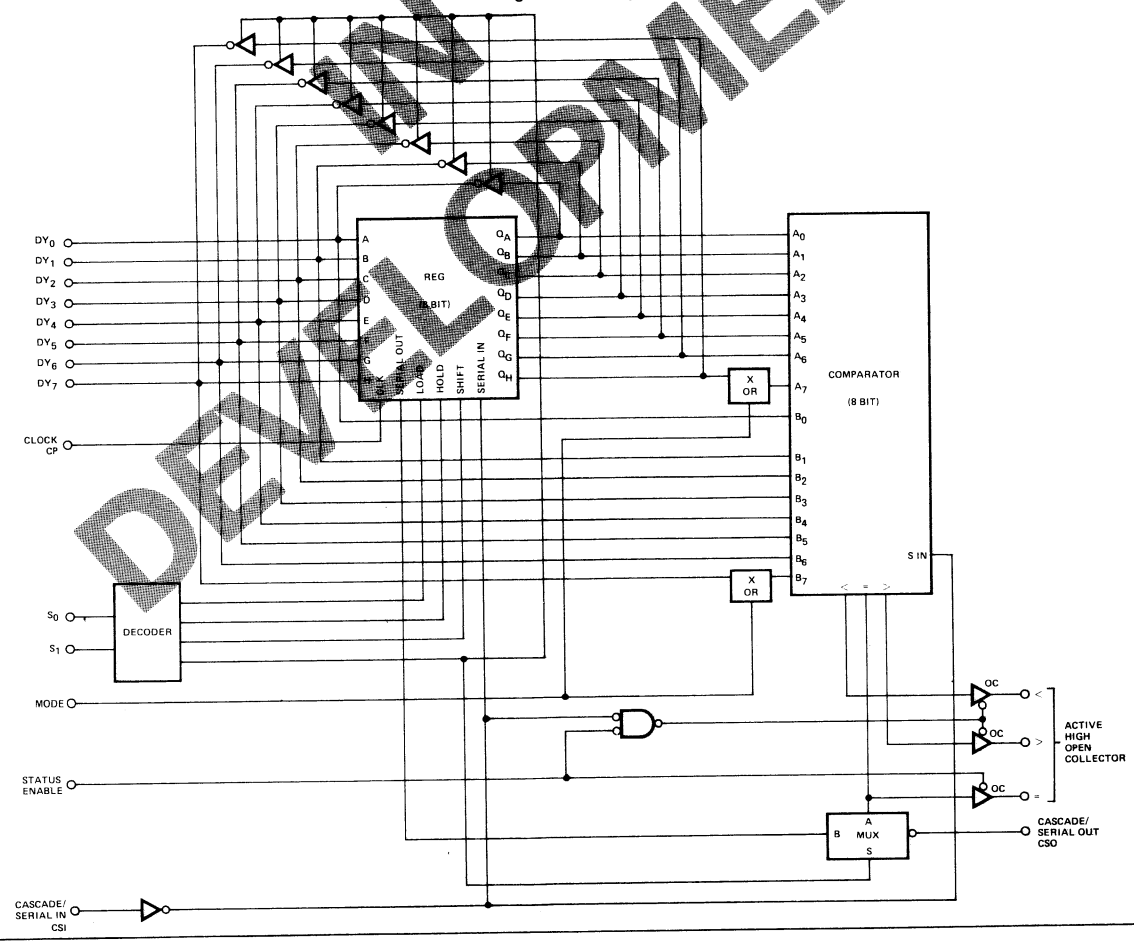
### FUNCTIONAL DESCRIPTION

The Am25LS2524 is an eight-bit bi-directional register with parallel input and output plus serial input and output progressing from LSB to MSB. Also attached to the input/output is an eight-bit comparator with one port tied to the register output and the other port tied to the input/output pins. The device outputs are three open collector, active HIGH outputs representing "equal to", "greater than", "less than". Provision has been made to disable these outputs (to OFF state) by the use of Status Enable. The device functions are controlled by two control lines, $S_0S_1$, to execute shift, load, hold, and readout.

A mode control has been provided to allow two's complement as well as magnitude compare. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. An output is also provided for cascading the device to accommodate wider bit fields in groups of eight bits per device.



### LOGIC DIAGRAM
8-Bit Registered Comparator



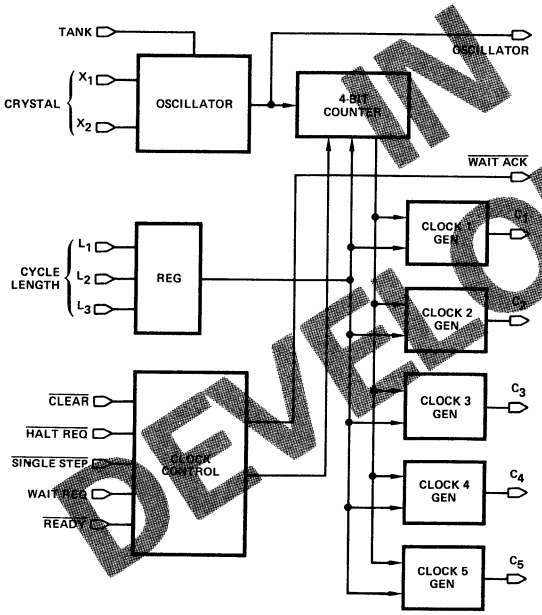
# Am25LS2525

## System Clock Generator and Driver

### DISTINCTIVE CHARACTERISTICS

- Single chip clock generator and driver
- Five different clock output waveforms for Am2900 and other bipolar and MOS systems
- Crystal controlled for stable system operation
- Oscillator to 33MHz – oscillator output for external system timing
- Clock halt, single-step and wait controls
- Variable cycle lengths – 1-of-8 different cycle lengths may be programmed
- 20-Pin package
- 100% product assurance screening to MIL-STD-883 requirements

### LOGIC DIAGRAM






### FUNCTIONAL DESCRIPTION

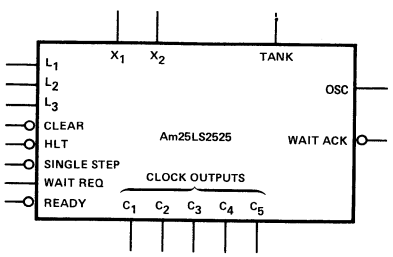
The Am25LS2525 is a single-chip general purpose clock generator/driver. It is controlled by a crystal, selected by the designer, and is microprogrammable to meet a variety of system speed requirements. The Am25LS2525 generates five different clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. Also, variable cycle lengths may be generated under microprogram control. One-of-eight different cycle lengths may be microprogrammed using the Cycle Length inputs L1, L2, and L3.

The Am25LS2525 oscillator runs at frequencies up to 33 MHz. An input pin is provided for a tank circuit which allows the use of overtone mode crystals. A buffered oscillator output is provided for external system timing.

Clock halt, single-step and wait controls are provided for the Am25LS2525. The HALT REQ input halts the clocks; the clocks resume when the HALT REQ input is deactivated. The SINGLE-STEP input, which operates only when the clocks are halted, generates the clocks for a single cycle. The WAIT REQ input stops the clocks and puts the Am25LS2525 in a "wait" state. In this state, the clocks remain stopped until an asynchronous READY input signal is received. The WAIT ACK output indicates when the Am25LS2525 is in the "wait" state. The WAIT REQ and READY inputs are pulse sensitive and are overridden by the HALT REQ input.

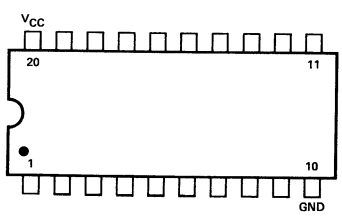
One-of-eight cycle lengths may be microprogrammed using the L1, L2, and L3 inputs. There are five clock output waveforms for each of the eight possible cycle lengths.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

# Am25LS2535

## Eight Input Multiplexer With Control Register

### DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- Am25LS features improved noise margin, higher drive, and faster operation
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am25LS2535 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

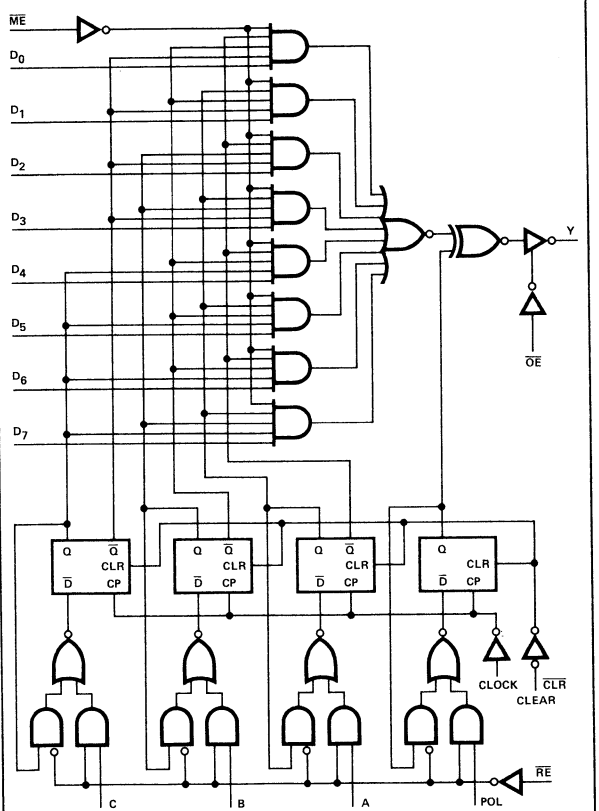
The Am25LS2535 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

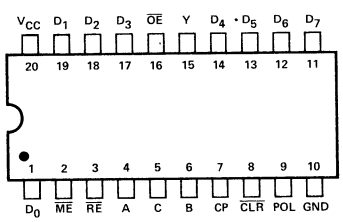
An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am25LS2535 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

### LOGIC DIAGRAM

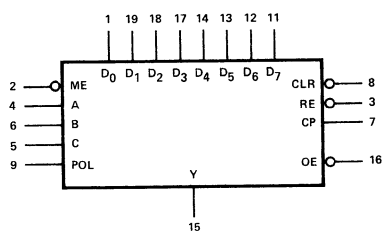



### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




VCC = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | | |
|---|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -2.0mA$ | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -6.5mA$ | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| | | | $I_{OL} = 20mA$ | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | $\overline{ME}$, $\overline{OE}$, $\overline{RE}$ | | | −0.72 | mA |
| | | | $D_N$, A, B, C, POL, CP, $\overline{CLR}$ | | | −2.0 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | $\overline{ME}$, $\overline{OE}$, $\overline{RE}$ | | | 40 | μA |
| | | | $D_N$, A, B, C, POL, CP, $\overline{CLR}$ | | | 50 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 5.5V$ | $\overline{ME}$, $\overline{OE}$, $\overline{RE}$ | | | 0.1 | mA |
| | | | $D_N$, A, B, C, POL, CP, $\overline{CLR}$ | | | 1.0 | |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | −50 | μA |
| | | | $V_O = 2.4V$ | | | 50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 97 | 148 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $D_1 - D_7$, A, B, C, POL, $\overline{ME}$, CLR at GND. All other inputs and outputs open.
Measured after a momentary ground then 4.5 V applied to clock input.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Y POL – LOW | | 21 | 32 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 19 | 29 | | |
| $t_{PLH}$ | Clock to Y POL – HIGH | | 16 | 24 | ns | |
| $t_{PHL}$ | | | 19 | 29 | | |
| $t_{PLH}$ | $D_n$ to Y | | 10 | 16 | ns | |
| $t_{PHL}$ | | | 13 | 19 | | |
| $t_{PLH}$ | $\overline{CLR}$ to Y | | 22 | 33 | ns | |
| $t_{PHL}$ | | | 22 | 33 | | |
| $t_{PLH}$ | $\overline{ME}$ to Y | | 12 | 18 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | |
| $t_{ZL}$ | $\overline{OE}$ to Y | | 8 | 14 | ns | |
| $t_{ZH}$ | | | 8 | 14 | | |
| $t_{LZ}$ | | | 10 | 17 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{HZ}$ | | | 10 | 17 | | |
| $t_S$ | A, B, C, POL | 10 | | | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| | $\overline{RE}$ | 15 | | | | |
| $t_S$ | $\overline{CLR}$ Recovery | 5 | | | ns | |
| $t_{pw}$ | Clock | 10 | | | ns | |
| | $\overline{Clear}$ (LOW) | 10 | | | | |
| $t_h$ | A, B, C, POL, $\overline{RE}$ | 0 | | | ns | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Y, POL-L | | 40 | | 47 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 34 | | 38 | | |
| $t_{PLH}$ | Clock to Y, POL-H | | 29 | | 33 | ns | |
| $t_{PHL}$ | | | 35 | | 41 | | |
| $t_{PLH}$ | $D_N$ to Y | | 19 | | 21 | ns | |
| $t_{PHL}$ | | | 22 | | 24 | | |
| $t_{PLH}$ | $\overline{CLR}$ to Y | | 39 | | 45 | ns | |
| $t_{PHL}$ | | | 39 | | 45 | | |
| $t_{PLH}$ | $\overline{ME}$ to Y | | 22 | | 26 | ns | |
| $t_{PHL}$ | | | 19 | | 20 | | |
| $t_{ZL}$ | $\overline{OE}$ to Y | | 19 | | 24 | ns | |
| $t_{ZH}$ | | | 22 | | 29 | | |
| $t_{LZ}$ | OE to Y | | 24 | | 30 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{HZ}$ | | | 24 | | 30 | | |
| $t_S$ | A, B, C POL | 11 | | 12 | | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| | $\overline{RE}$ | 18 | | 20 | | | |
| $t_S$ | $\overline{CLR}$ Recovery | 6 | | 7 | | ns | |
| $t_{pw}$ | Clock | 11 | | 12 | | ns | |
| | $\overline{Clear}$ (LOW) | 11 | | 12 | | | |
| $t_H$ | A, B, C, POL, $\overline{RE}$ | 3 | | 3 | | ns | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

## FUNCTION TABLE

| MODE | INPUTS | | | | | | | INTERNAL | | | | INPUTS | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C | B | A | POL | $\overline{RE}$ | $\overline{CLR}$ | CP | $Q_C$ | $Q_B$ | $Q_A$ | $Q_{POL}$ | $\overline{ME}$ | $\overline{OE}$ | Y |
| Clear | X | X | X | X | X | L | X | L | L | L | L | H | L | H |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | L | $\overline{D}_0$ |
| | | | | | | | | | | | | X | H | Z |
| Reg. Disable | X | X | X | X | H | H | X | NC | NC | NC | NC | L | L | $D_i/D_i$ (Note 1) |
| Select (Multiplex) | L | L | L | L/H | L | H | ↑ | L | L | L | L/H | L | L | $\overline{D}_0/D_0$ |
| | L | L | H | ↓ | ↓ | ↓ | ↓ | L | L | H | ↓ | ↓ | ↓ | $\overline{D}_1/D_1$ |
| | L | H | L | | | | | L | H | L | | | | $\overline{D}_2/D_2$ |
| | L | H | H | | | | | L | H | H | | | | $\overline{D}_3/D_3$ |
| | H | L | L | | | | | H | L | L | | | | $\overline{D}_4/D_4$ |
| | H | L | H | | | | | H | L | H | | | | $\overline{D}_5/D_5$ |
| | H | H | L | | | | | H | H | L | | | | $\overline{D}_6/D_6$ |
| | H | H | H | ↓ | ↓ | ↓ | ↓ | H | H | H | ↓ | ↓ | ↓ | $\overline{D}_7/D_7$ |
| Multiplexer Disable | X | X | X | X | X | H | X | X | X | X | L | H | L | H |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | X | X | X | H | H | L | L |
| Tri-state Output Disable | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | X | X | X | X | X | H | Z |

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, $D_i$, or its complement depending on the state of the POL flip-flop.

## DEFINITION OF FUNCTIONAL TERMS

**A, B, C** Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

**POL** Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

**$\overline{ME}$** Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

**$\overline{RE}$** Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

**$\overline{CLR}$** Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

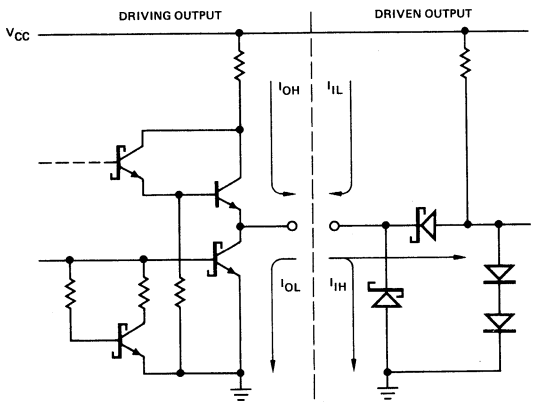
**$D_1$-$D_8$** Data Inputs to the 8-input multiplexer.

**CP** Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

**$\overline{OE}$** Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

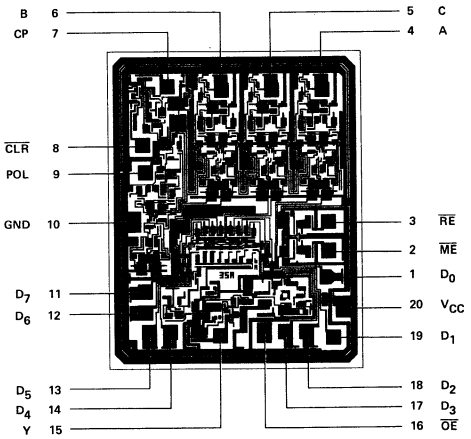
**Y** The chip output.

## Am25LS
## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



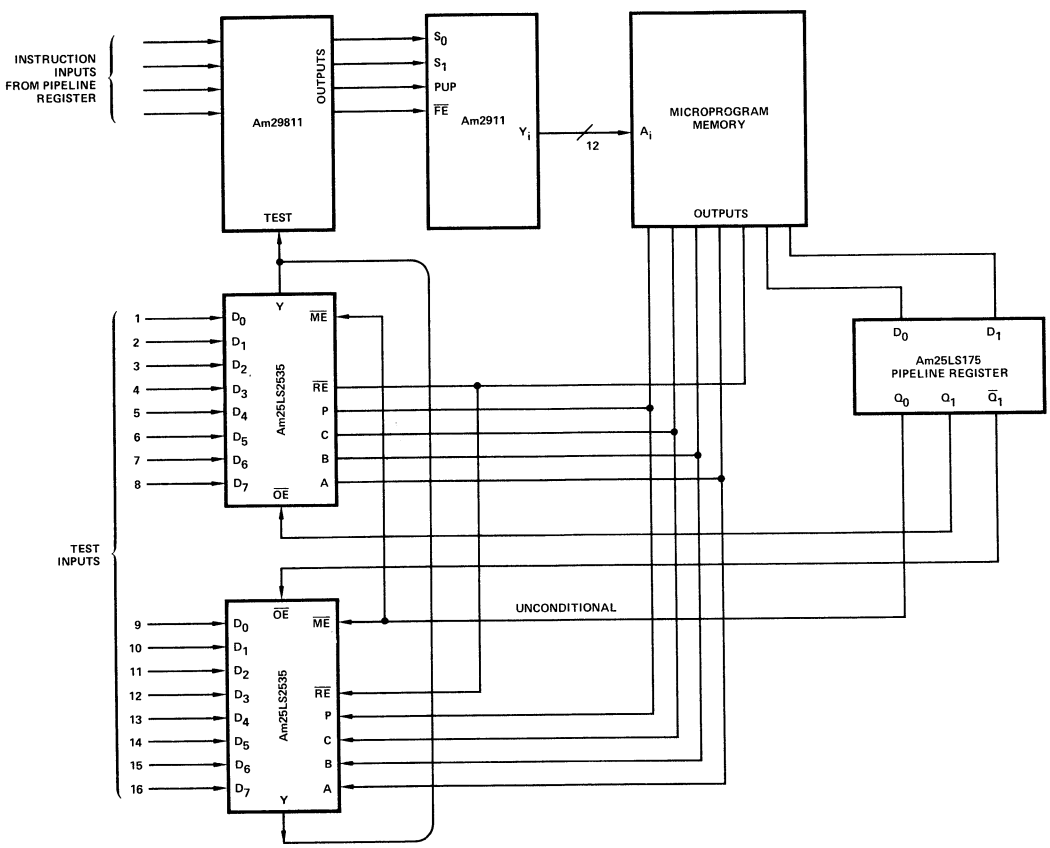

Note: Actual current flow direction shown.

## Metallization and Pad Layout




DIE SIZE 0.080" X 0.099"

## APPLICATION




A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

# Am25LS2536

## Eight-Bit Decoder With Control Storage

### DISTINCTIVE CHARACTERISTICS

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control
- Advanced Low Power Schottky Process
- 100% product assurance screening to MIL-STD-883 requirements

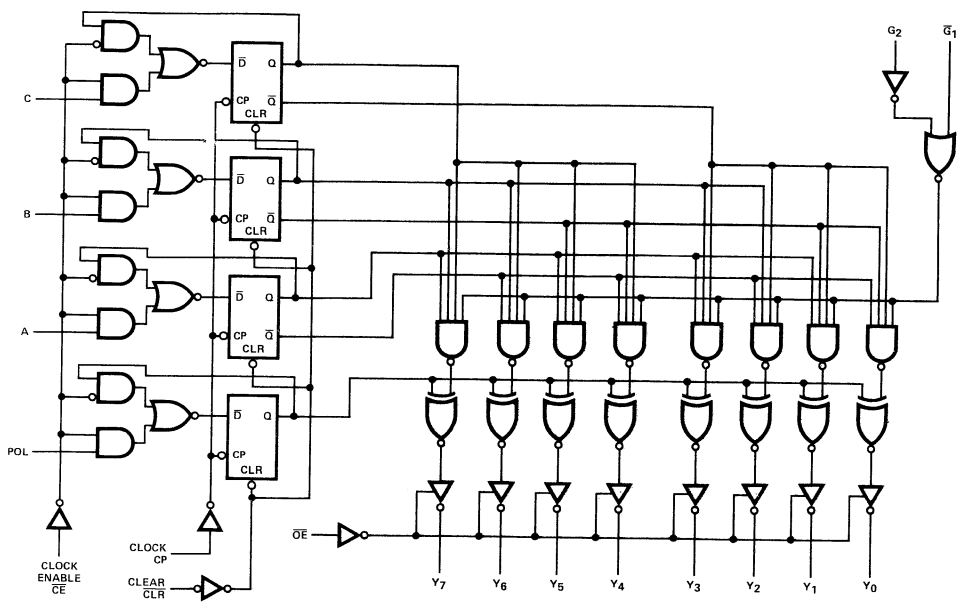
### FUNCTIONAL DESCRIPTION

The Am25LS2536 is an eight-bit decoder with control storage. It provides a conventional 8-bit decoder function with two enable inputs which may also be used for data input. This can be used to implement a demultiplexer function. In addition, the exclusive "OR" gate allows for polarity control of the selected output. The 3-state outputs are enabled by a LOW on the ($\overline{OE}$) output enable.

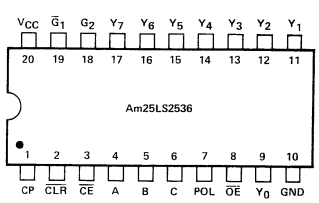
The three control bits representing the output selection and the single bit polarity control are stored in "D" type flip-flops. These flip-flops have both Clear, Clock, and Clock Enable functions provided. The $G_1$ and $\overline{G_2}$ input provide either polarity for input control or data.

### LOGIC DIAGRAM

8-Bit Decoder/Demultiplexer with Control Storage

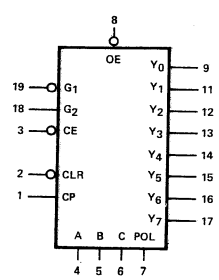



### CONNECTION DIAGRAM




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = 20
GND = 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -2.6mA$, COM'L | 2.4 | 3.2 | | Volts |
| | | | $I_{OH} = -1.0mA$, MIL | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 24mA$, COM'L | | 0.4 | 0.5 | Volts |
| | | | $I_{OL} = 12mA$, MIL | | 0.35 | 0.4 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_O$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 37 | 56 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test Conditions: A = B = C = $\overline{G}_1$ = $G_2$ = $\overline{OE}$ = $\overline{CE}$ = GND; CLK = $\overline{CLR}$ = POL = 4.5V.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

3

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $G_1$ to $Y_0$ – $Y_7$ | | | 17 | 25 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PLH}$ | | | | 23 | 34 | | |
| $t_{PLH}$ | $G_2$ to $Y_0$ – $Y_7$ | | | 20 | 30 | ns | |
| $t_{PHL}$ | | | | 26 | 39 | | |
| $t_{PLH}$ | CP to $Y_0$ – $Y_7$ | | | 24 | 36 | ns | |
| $t_{PHL}$ | | | | 30 | 45 | | |
| $t_{PLH}$ | CLR to $Y_0$ – $Y_7$ | | | 24 | 36 | ns | |
| $t_{PHL}$ | | | | 31 | 46 | | |
| $t_s$ | Clock Enable to CP | | 25 | | | ns | |
| $t_h$ | | | 0 | | | | |
| $t_s$ | A, B, C, POL to CP | | 15 | | | ns | |
| $t_h$ | | | 0 | | | | |
| $t_{HZ}$ | OE to $Y_0$ – $Y_7$ | | | 9 | 14 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | 11 | 17 | | |
| $t_{ZH}$ | OE to $Y_0$ – $Y_7$ | | | 15 | 22 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{ZL}$ | | | | 16 | 24 | | |
| $t_s$ | Set-up Time, Clear Recovery to CP | | 20 | | | ns | |
| $t_{pw}$ | Pulse Width | Clock | 15 | | | ns | |
| | | Clear | 15 | | | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am26LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | Am26LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $G_1$ to $Y_0$ – $Y_7$ | | | 29 | | 31 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | | | | 39 | | 42 | | |
| $t_{PLH}$ | $G_2$ to $Y_0$ – $Y_7$ | | | 34 | | 37 | ns | |
| $t_{PHL}$ | | | | 44 | | 48 | | |
| $t_{PLH}$ | CP to $Y_0$ – $Y_7$ | | | 40 | | 42 | ns | |
| $t_{PHL}$ | | | | 51 | | 55 | | |
| $t_{PLH}$ | CLR to $Y_0$ – $Y_7$ | | | 47 | | 54 | ns | |
| $t_{PHL}$ | | | | 58 | | 66 | | |
| $t_s$ | Clock Enable to CP | | 27 | | 30 | | ns | |
| $t_h$ | | | 0 | | 0 | | | |
| $t_s$ | A, B, C, POL to CP | | 17 | | 20 | | ns | |
| $t_h$ | | | 0 | | 0 | | | |
| $t_{HZ}$ | OE to $Y_0$ – $Y_7$ | | | 17 | | 18 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | 27 | | 34 | | |
| $t_{ZH}$ | OE to $Y_0$ – $Y_7$ | | | 25 | | 27 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{ZL}$ | | | | 28 | | 30 | | |
| $t_s$ | Set-up Time, Clear Recovery to CP | | 23 | | 25 | | ns | |
| $t_{pw}$ | Pulse Width | Clock | 17 | | 20 | | ns | |
| | | Clear | 15 | | 15 | | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## FUNCTION TABLE

| Mode | Inputs | | | | | | | | | Internal Registers | | | | Three-State Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C | B | A | POL | $\overline{CE}$ | $\overline{CLR}$ | G* | $\overline{OE}$ | CP | $Q_C$ | $Q_B$ | $Q_A$ | $Q_{POL}$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| Clear | X | X | X | X | X | L | L | L | X | L | L | L | L | H | H | H | H | H | H | H | H |
| | X | X | X | X | X | L | H | L | X | L | L | L | L | L | H | H | H | H | H | H | H | H |
| Hold | X | X | X | X | H | H | NC | L | ↑ | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC |
| Select | L | L | L | H | L | H | H | L | ↑ | L | L | L | H | H | L | L | L | L | L | L | L |
| | L | L | H | H | L | H | H | L | ↑ | L | L | H | H | L | H | L | L | L | L | L | L |
| | L | H | L | H | L | H | H | L | ↑ | L | H | L | H | L | L | H | L | L | L | L | L |
| | L | H | H | H | L | H | H | L | ↑ | L | H | H | H | L | L | L | H | L | L | L | L |
| | H | L | L | H | L | H | H | L | ↑ | H | L | L | H | L | L | L | L | H | L | L | L |
| | H | L | H | H | L | H | H | L | ↑ | H | L | H | H | L | L | L | L | L | H | L | L |
| | H | H | L | H | L | H | H | L | ↑ | H | H | L | H | L | L | L | L | L | L | H | L |
| | H | H | H | H | L | H | H | L | ↑ | H | H | H | H | L | L | L | L | L | L | L | H |
| | L | L | L | L | L | H | H | L | ↑ | L | L | L | L | L | H | H | H | H | H | H | H |
| | L | L | H | L | L | H | H | L | ↑ | L | L | H | L | H | L | H | H | H | H | H | H |
| | L | H | L | L | L | H | H | L | ↑ | L | H | L | L | H | H | L | H | H | H | H | H |
| | L | H | H | L | L | H | H | L | ↑ | L | H | H | L | H | H | H | L | H | H | H | H |
| | H | L | L | L | L | H | H | L | ↑ | H | L | L | L | H | H | H | H | L | H | H | H |
| | H | L | H | L | L | H | H | L | ↑ | H | L | H | L | H | H | H | H | H | L | H | H |
| | H | H | L | L | L | H | H | L | ↑ | H | H | L | L | H | H | H | H | H | H | L | H |
| | H | H | H | L | L | H | H | L | ↑ | H | H | H | L | H | H | H | H | H | H | H | L |
| | X | X | X | H | L | H | L | L | ↑ | X | X | X | H | L | L | L | L | L | L | L | L |
| | X | X | X | L | L | H | L | L | ↑ | X | X | X | L | H | H | H | H | H | H | H | H |
| Output Disable | X | X | X | X | X | X | X | H | X | NC | NC | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |

* 

| $\overline{G}_1$ | $G_2$ | G |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | L |
| H | H | L |

NC = No Change  X = Don't Care  Z = High-Impedance  ↑ = Low-to-High Transition

3

### DEFINITION OF TERMS

**$\overline{CLR}$** CLEAR – When the CLEAR input is LOW, the control register outputs ($Q_A$, $Q_B$, $Q_C$, $Q_{POL}$) are set LOW regardless of any other inputs.

**CP** CLOCK – Enters data into the control register on the LOW-to-HIGH transition.

**$\overline{CE}$** CLOCK ENABLE – Allows data to enter the control register when $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH, the $Q_i$ outputs do not change state, regardless of data or clock input transitions.

**A,B,C** Inputs to the control register which are entered on the LOW-to-HIGH clock transition if $\overline{CE}$ is LOW.

**POL** Input to the control register bit used for determining the polarity of the selected output.

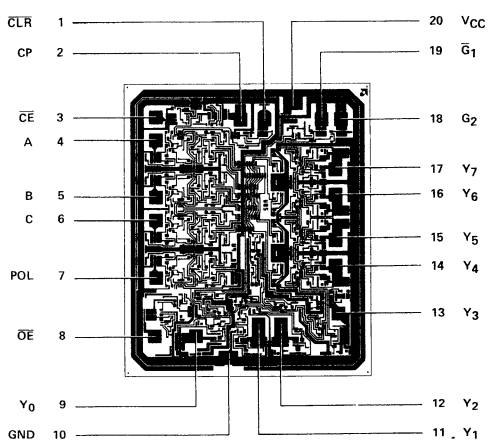
**$\overline{G}_1$** Active LOW part of the expression $G = G_1G_2$ [or $G = (\overline{G}_1)\,G_2$] where G is either data input for the selected $Y_n$ or is used as an input enable.

**$G_2$** Active HIGH part of the expression $G = G_1G_2$.

**$Y_n$** The three-state outputs. When active ($\overline{OE}$ = LOW), one of eight outputs is selected by the code stored in the control register, with the polarity of all eight determined by the bit stored in the POL flip-flop of the control register. The selected output can further be controlled by G according to the expression $Y_{SELECTED} = \overline{G \oplus Q_{POL}}$.

**$\overline{OE}$** OUTPUT ENABLE. When $\overline{OE}$ is HIGH the $Y_n$ outputs are in the high impedance state; when $\overline{OE}$ is LOW the $Y_n$'s are in their active state as determined by the other control logic. The $\overline{OE}$ input affects the $Y_n$ output buffers only and has no effect on the control register or any other logic.

### Metallization and Pad Layout




DIE SIZE 0.084" X 0.099"

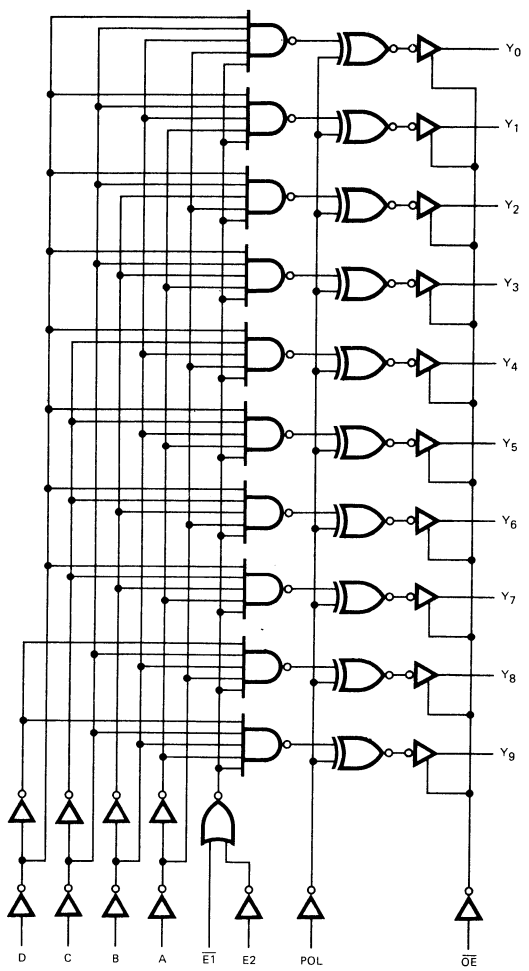
# Am25LS2537

## One-Of-Ten Decoder With Three-State Outputs And Polarity Control

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs
- Separate output polarity control
- Inverting and non-inverting enable inputs
- Does not respond to codes above nine
- A.C. parameters specified over operating temperature and power supply ranges
- 100% product assurance screening to MIL-STD-883 requirements

### LOGIC DIAGRAM



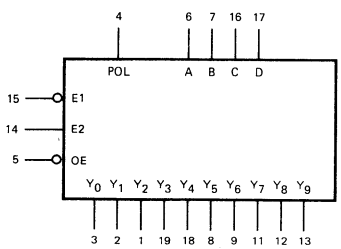

### FUNCTIONAL DESCRIPTION

The Am25LS2537 is a demultiplexer/one-of-ten decoder that accepts four active high BCD inputs and selects one-of-ten mutually exclusive outputs. The device features three-state outputs as well as a buffered common polarity control such that the outputs are mutually exclusive active-low or mutually exclusive active-high. The logic design of the Am25LS2537 ensures that all outputs are unselected when the binary codes greater than nine are applied to the inputs. The inputs A, B, C, and D of the Am25LS2537 correspond to the respective binary weight of 1, 2, 4, and 8.

The output enable ($\overline{OE}$) input controls the three-state outputs. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the outputs are enabled. The polarity (POL) input is used to drive the Y outputs to either the active-HIGH state or the active-LOW state. When the POL input is LOW, the outputs are active-HIGH. When the POL input is HIGH, the Y outputs are active-LOW. The device features one active-HIGH and one active-LOW enable input which can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

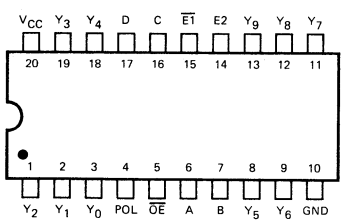
The Am25LS2537 is packaged in a space saving (0.3-inch row spacing) 20-pin package. The device also features Am25LS family faster switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L = $T_A$ = 0°C to +70°C  $V_{CC}$ = 5.0 V ±5%  MIN. = 4.75 V  MAX. = 5.25 V
MIL = $T_A$ = −55°C to +125°C  $V_{CC}$ = 5.0 V ±10%  MIN. = 4.50 V  MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL, $I_{OH}$ = −1.0mA | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH}$ = −2.6mA | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Note 5) | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| | | | $I_{OL}$ = 12mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O$ = 0.4 V | | | −20 | μA |
| | | | $V_O$ = 2.4 V | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 25 | 40 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = D = E1 = GND; E2 = POL = $\overline{OE}$ = 4.5 V.
5. $V_{OL}$ is specified with total device $I_{OL}$ = 60mA (max.).

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, C, D to $Y_i$ | | 22 | 33 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 17 | 25 | | |
| $t_{PLH}$ | $E_1$ to $Y_i$ | | 19 | 28 | ns | |
| $t_{PHL}$ | | | 21 | 31 | | |
| $t_{PLH}$ | $\overline{E_2}$ to $Y_i$ | | 21 | 31 | ns | |
| $t_{PHL}$ | | | 23 | 34 | | |
| $t_{PLH}$ | POL to $Y_i$ | | 18 | 27 | ns | |
| $t_{PHL}$ | | | 21 | 31 | | |
| $t_{ZH}$ | $\overline{OE}$ Control to $Y_i$ | | 22 | 33 | ns | |
| $t_{ZL}$ | | | 14 | 21 | | |
| $t_{HZ}$ | $\overline{OE}$ Control to $Y_i$ | | 19 | 28 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 23 | 34 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, C, D to $Y_i$ | | 41 | | 48 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 32 | | 39 | | |
| $t_{PLH}$ | $E_1$ to $Y_i$ | | 34 | | 40 | ns | |
| $t_{PHL}$ | | | 38 | | 45 | | |
| $t_{PLH}$ | $\overline{E_2}$ to $Y_i$ | | 38 | | 45 | ns | |
| $t_{PHL}$ | | | 42 | | 49 | | |
| $t_{PLH}$ | POL to $Y_i$ | | 32 | | 37 | ns | |
| $t_{PHL}$ | | | 42 | | 52 | | |
| $t_{ZH}$ | $\overline{OE}$ Control to $Y_i$ | | 44 | | 55 | ns | |
| $t_{ZL}$ | | | 23 | | 25 | | |
| $t_{HZ}$ | $\overline{OE}$ Control to $Y_i$ | | 33 | | 37 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 38 | | 42 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## FUNCTION TABLE

| FUNCTION | INPUTS | | | | | | | | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OE}$ | $\overline{E_1}$ | $E_2$ | POL | D | C | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ | $Y_8$ | $Y_9$ |
| 3-State | H | X | X | X | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z |
| Disable | L | H | X | L | X | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | H | X | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H |
| | L | X | L | L | X | X | X | X | L | L | L | L | L | L | L | L | L | L |
| | L | X | L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H |
| Active-HIGH Output | L | L | H | L | L | L | L | L | H | L | L | L | L | L | L | L | L | L |
| | L | L | H | L | L | L | L | H | L | H | L | L | L | L | L | L | L | L |
| | L | L | H | L | L | L | H | L | L | L | H | L | L | L | L | L | L | L |
| | L | L | H | L | L | L | H | H | L | L | L | H | L | L | L | L | L | L |
| | L | L | H | L | L | H | L | L | L | L | L | L | H | L | L | L | L | L |
| | L | L | H | L | L | H | L | H | L | L | L | L | L | H | L | L | L | L |
| | L | L | H | L | L | H | H | L | L | L | L | L | L | L | H | L | L | L |
| | L | L | H | L | L | H | H | H | L | L | L | L | L | L | L | H | L | L |
| | L | L | H | L | H | L | L | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | H | L | H | L | L | H | L | L | L | L | L | L | L | L | L | H |
| | L | L | H | L | H | L | H | L | L | L | L | L | L | L | L | L | L | L |
| | L | L | H | L | H | L | H | H | L | L | L | L | L | L | L | L | L | L |
| | L | L | H | L | H | H | L | L | L | L | L | L | L | L | L | L | L | L |
| | L | L | H | L | H | H | L | H | L | L | L | L | L | L | L | L | L | L |
| | L | L | H | L | H | H | H | L | L | L | L | L | L | L | L | L | L | L |
| | L | L | H | L | H | H | H | H | L | L | L | L | L | L | L | L | L | L |
| Active-LOW Output | L | L | H | H | L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| | L | L | H | H | L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| | L | L | H | H | L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| | L | L | H | H | L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| | L | L | H | H | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| | L | L | H | H | L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| | L | L | H | H | L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| | L | L | H | H | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| | L | L | H | H | H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| | L | L | H | H | H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| | L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | L | L | H | H | H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

## DEFINITION OF FUNCTIONAL TERMS

**A, B, C, D** To select inputs to the decoder.

**E1** The active-LOW enable input. A HIGH on the E1 input inhibits the decoder function regardless of any other inputs.

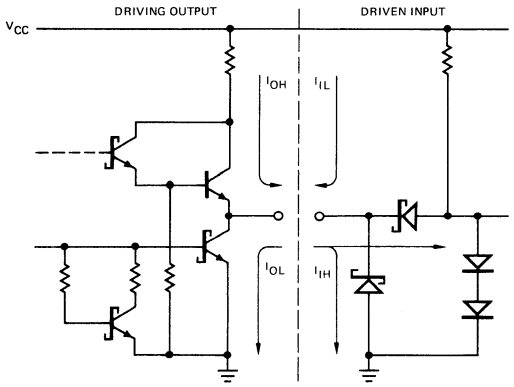
**$\overline{E2}$** The active-HIGH enable input. A LOW on the $\overline{E2}$ input forces all the decoder functions to the inactive state regardless of any other inputs.

**POL** The polarity control for the output function. When the polarity control is HIGH, the outputs are active-LOW. When the POL input is LOW, the outputs are active-HIGH.

**$\overline{OE}$** Output Enable. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the output to the high impedance (off) state.

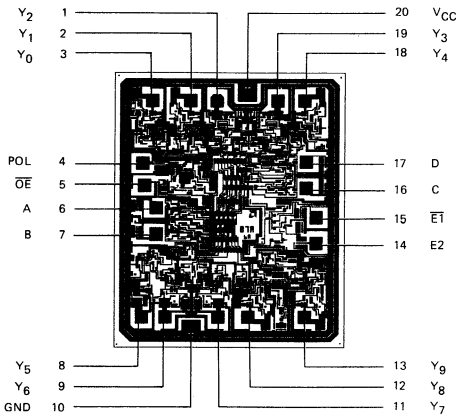
**$Y_i$** Decoder outputs. The ten outputs of the decoder.

## Am25LS
## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



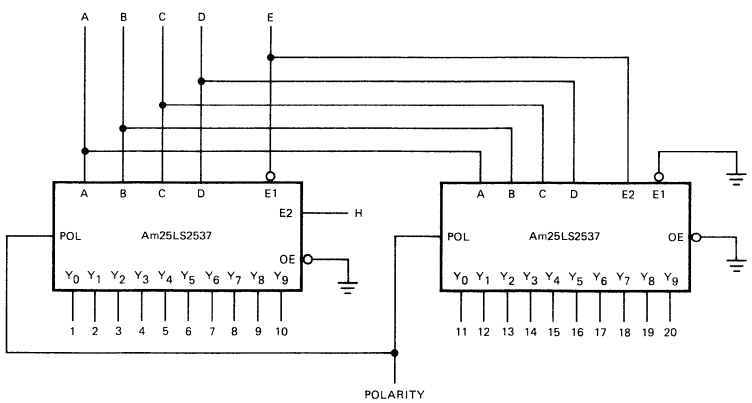

Note: Actual current flow direction shown.

## Metallization and Pad Layout

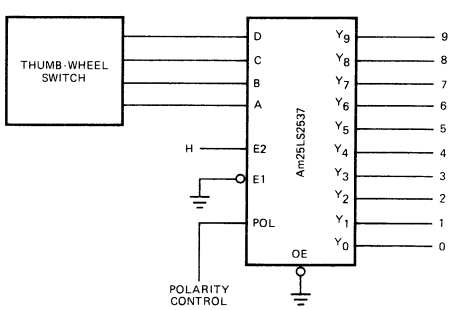



DIE SIZE 0.081" X 0.096"

## APPLICATIONS




One-of-Twenty Decoder with Active-High or Active-Low Output Polarity.
Could be used for I/O Decoding in an Am9080A system.




BCD to Decimal (One-of-Ten) Decoder.

# Am25LS2538 = 74ALS538

## One-of-Eight Decoder
## With Three-State Outputs And Polarity Control

### DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- A. C. parameters specified over operating temperature and power supply ranges
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

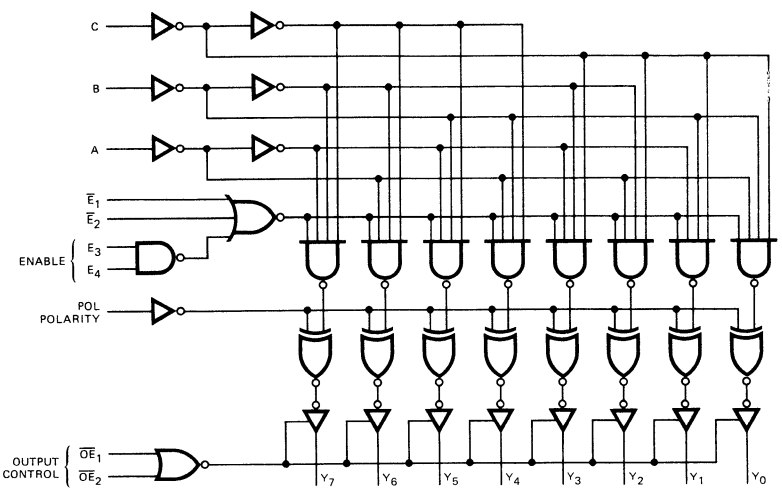
The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs—A, B, and C—that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

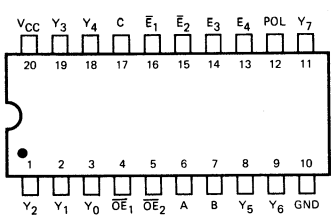
The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features Am25LS family improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

3

### LOGIC DIAGRAM
**One-of-Eight Decoder**

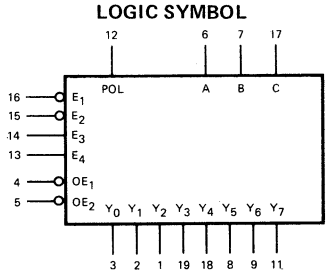



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$ (MIL) | | 2.4 | 3.4 | | Volts |
| | | | $I_{OH} = -2.6mA$ (COM'L) | | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Note 5) | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| | | | $I_{OL} = 12mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 21 | 34 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND : $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2 = 4.5V$.
5. $V_{OL}$ is specified with total device $I_{OL} = 60mA$ (max.).

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, C to $Y_i$ | | 20 | 30 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 15 | 22 | | |
| $t_{PLH}$ | $\overline{E_1}$, $\overline{E_2}$ to $Y_i$ | | 19 | 28 | ns | |
| $t_{PHL}$ | | | 20 | 30 | | |
| $t_{PLH}$ | $E_3$, $E_4$ to $Y_i$ | | 21 | 31 | ns | |
| $t_{PHL}$ | | | 23 | 34 | | |
| $t_{PLH}$ | POL to $Y_i$ | | 16 | 24 | ns | |
| $t_{PHL}$ | | | 20 | 30 | | |
| $t_{ZH}$ | $\overline{OE_1}$, $\overline{OE_2}$ to $Y_i$ | | 17 | 25 | ns | |
| $t_{ZL}$ | | | 14 | 21 | | |
| $t_{HZ}$ | $\overline{OE_1}$, $\overline{OE_2}$ to $Y_i$ | | 17 | 25 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 20 | 30 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5% Min. | Am25LS COM'L Max. | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10% Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, C to $Y_i$ | | 36 | | 42 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 29 | | 37 | | |
| $t_{PLH}$ | $\overline{E_1}$, $\overline{E_2}$ to $Y_i$ | | 34 | | 39 | ns | |
| $t_{PHL}$ | | | 38 | | 45 | | |
| $t_{PLH}$ | $E_3$, $E_4$ to $Y_i$ | | 38 | | 45 | ns | |
| $t_{PHL}$ | | | 43 | | 52 | | |
| $t_{PLH}$ | POL to $Y_i$ | | 29 | | 34 | ns | |
| $t_{PHL}$ | | | 39 | | 49 | | |
| $t_{ZH}$ | $\overline{OE_1}$, $\overline{OE_2}$ to $Y_i$ | | 38 | | 45 | ns | |
| $t_{ZL}$ | | | 23 | | 25 | | |
| $t_{HZ}$ | $\overline{OE_1}$, $\overline{OE_2}$ to $Y_i$ | | 29 | | 33 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 33 | | 36 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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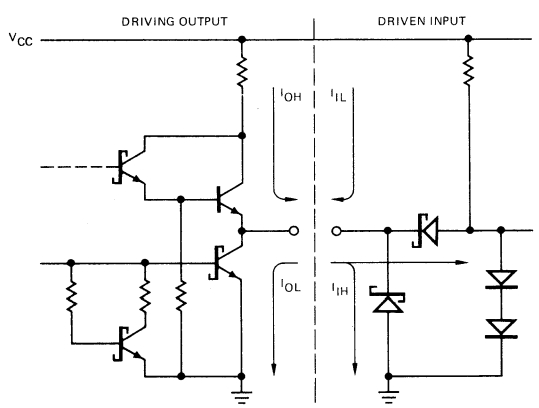
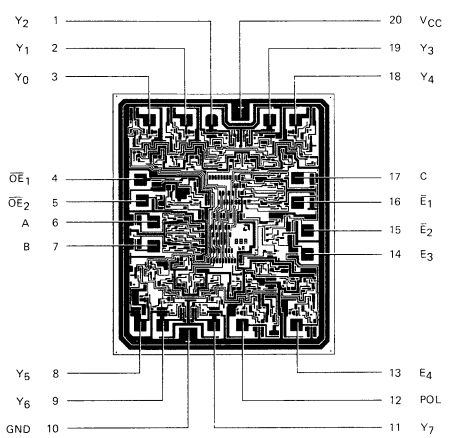
### Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

### Metallization and Pad Layout




DIE SIZE 0.081" X 0.096"

## DEFINITION OF FUNCTIONAL TERMS

**A, B, C, D** The three select inputs to the decoder/demultiplexer.

**$\overline{E}_1$, $\overline{E}_2$** The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

**$E_3$, $E_4$** The active LOW enable inputs. A LOW on either $E_3$ or $E_4$ inputs forces all the decoded functions to be inhibited.

POL Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

**$\overline{OE}_1$, $\overline{OE}_2$** Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

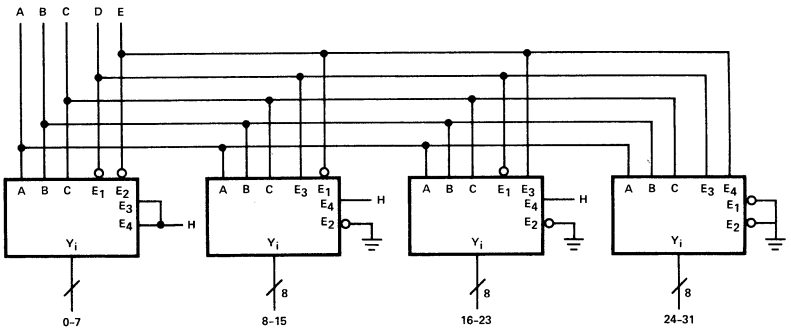
$Y_i$ The eight outputs for the decoder/demultiplexer.

## FUNCTION TABLE

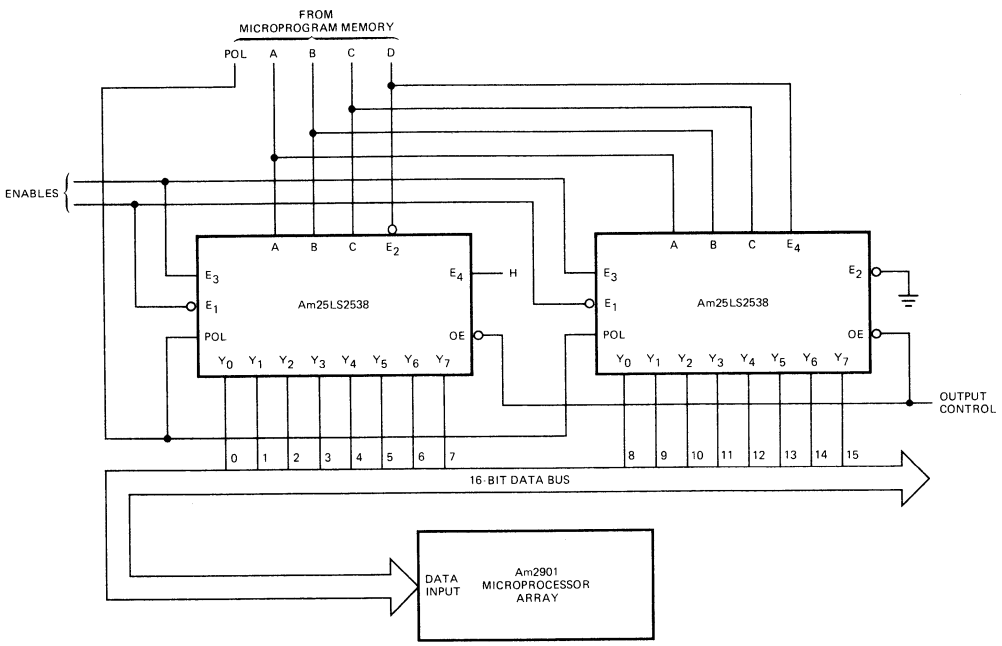
| FUNCTION | INPUTS | | | | | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OE}_1$ | $\overline{OE}_2$ | $\overline{E}_1$ | $\overline{E}_2$ | $E_3$ | $E_4$ | POL | C | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| High Impedance | H | X | X | X | X | X | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z |
| | X | H | X | X | X | X | X | X | X | X | Z | Z | Z | Z | Z | Z | Z | Z |
| Disable | L | L | H | X | X | X | L | X | X | X | L | L | L | L | L | L | L | L |
| | L | L | H | X | X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| | L | L | X | H | X | X | L | X | X | X | L | L | L | L | L | L | L | L |
| | L | L | X | H | X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| | L | L | X | X | L | X | L | X | X | X | L | L | L | L | L | L | L | L |
| | L | L | X | X | L | X | H | X | X | X | H | H | H | H | H | H | H | H |
| | L | L | X | X | X | L | L | X | X | X | L | L | L | L | L | L | L | L |
| | L | L | X | X | X | L | H | X | X | X | H | H | H | H | H | H | H | H |
| Active-HIGH Output | L | L | L | L | H | H | L | L | L | L | H | L | L | L | L | L | L | L |
| | L | L | L | L | H | H | L | L | L | H | L | H | L | L | L | L | L | L |
| | L | L | L | L | H | H | L | L | H | L | L | L | H | L | L | L | L | L |
| | L | L | L | L | H | H | L | L | H | H | L | L | L | H | L | L | L | L |
| | L | L | L | L | H | H | L | H | L | L | L | L | L | L | H | L | L | L |
| | L | L | L | L | H | H | L | H | L | H | L | L | L | L | L | H | L | L |
| | L | L | L | L | H | H | L | H | H | L | L | L | L | L | L | L | H | L |
| | L | L | L | L | H | H | L | H | H | H | L | L | L | L | L | L | L | H |
| Active-LOW Output | L | L | L | L | H | H | H | L | L | L | L | H | H | H | H | H | H | H |
| | L | L | L | L | H | H | H | L | L | H | H | L | H | H | H | H | H | H |
| | L | L | L | L | H | H | H | L | H | L | H | H | L | H | H | H | H | H |
| | L | L | L | L | H | H | H | L | H | H | H | H | H | L | H | H | H | H |
| | L | L | L | L | H | H | H | H | L | L | H | H | H | H | L | H | H | H |
| | L | L | L | L | H | H | H | H | L | H | H | H | H | H | H | L | H | H |
| | L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | L | H |
| | L | L | L | L | H | H | H | H | H | H | L | L | L | L | L | L | L | H |

H = HIGH L = LOW X = Don't Care Z = High Impedance

## APPLICATIONS




One-of-thirty two decoder without additional decoding devices.
Can be used for I/O decoding in an Am9080A system.




Two Am25LS2538s can be used to perform a one-of-sixteen-bit mask function or a one-of-sixteen-bit select function to perform bit manipulation in a microprocessor system.

Examples:

| D | C | B | A | POL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Bit Select |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Bit Select |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Bit Mask |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | Bit Mask |

# Am25LS2539

## Dual One-Of-Four Decoder With Three-State Outputs And Polarity Control

### DISTINCTIVE CHARACTERISTICS

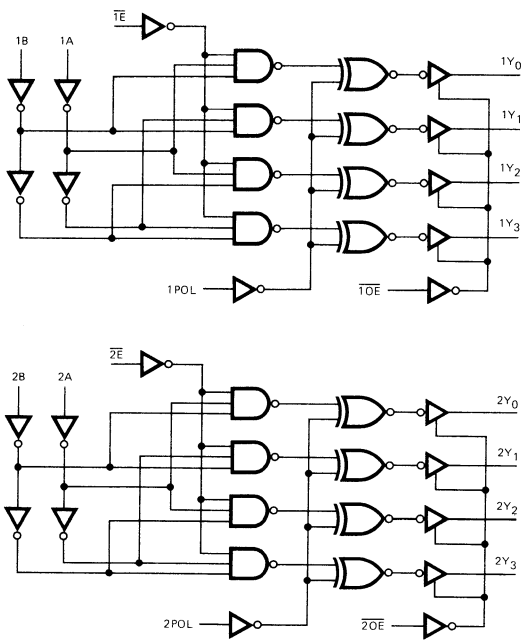
- Two independent decoders/demultiplexers
- Three-state outputs
- Buffered common polarity control
- A. C. parameters specified over operating temperature and power supply ranges
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

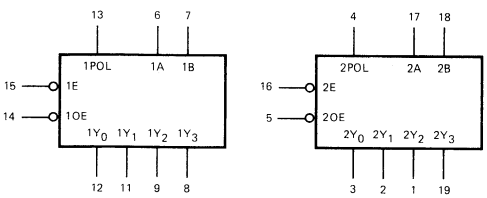
The Am25LS2539 is a dual two-line to four-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs—A and B which are decoded to one-of-four Y outputs. An enable input ($\overline{E}$) is used for gating or can be used as a data input for demultiplexing applications. When the enable input goes HIGH, all four decoder functions are inhibited.

An output enable ($\overline{OE}$) input is used to control the three-state outputs of the device. When the $\overline{OE}$ input is LOW, the outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance (off) state. The device also has separate buffered polarity (POL) inputs to force the outputs to either an active-HIGH state or an active-LOW state. When the POL input is LOW, the outputs are active-HIGH and when the POL input is HIGH, the outputs are active-LOW. The device is packaged in a space saving (0.3 inch row spacing) 20-pin package. The device features Am25LS family improved switching specification, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

### LOGIC DIAGRAM

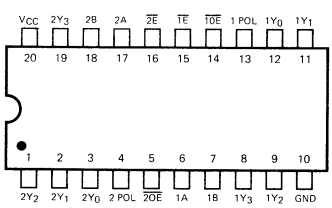



### LOGIC SYMBOLS




$V_{CC}$ = Pin 20
GND = Pin 10

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | | |
|---|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Note 5) | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| | | | $I_{OL} = 12mA$ | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 22 | 37 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = $\overline{E}$ = GND; POL = $\overline{OE}$ = 4.5V.
5. $V_{OL}$ is specified with total device $I_{OL} = 60mA$ (max.).

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

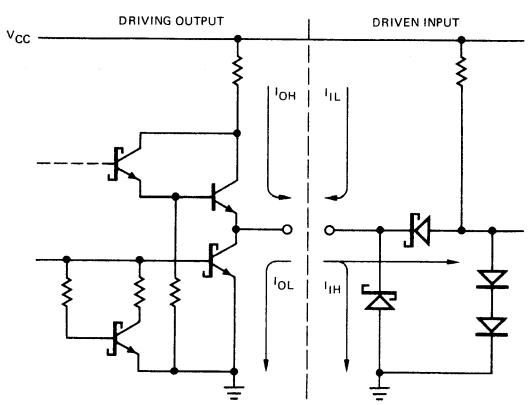
| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B to $Y_i$ | | 22 | 33 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 17 | 25 | | |
| $t_{PLH}$ | $\overline{E}$ to $Y_i$ | | 19 | 28 | ns | |
| $t_{PHL}$ | | | 21 | 31 | | |
| $t_{PLH}$ | POL to $Y_i$ | | 16 | 24 | ns | |
| $t_{PHL}$ | | | 19 | 28 | | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | 15 | 23 | ns | |
| $t_{ZL}$ | | | 15 | 22 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | 19 | 28 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 23 | 34 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | Am25LS COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5% | | Am25LS MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10% | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ | A, B, to $Y_i$ | | 41 | | 48 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 34 | | 42 | | |
| PLH | $\overline{E}$ to $Y_i$ | | 34 | | 40 | ns | |
| $t_{PHL}$ | | | 38 | | 45 | | |
| $t_{PLH}$ | POL to $Y_i$ | | 29 | | 34 | ns | |
| $t_{PHL}$ | | | 39 | | 49 | | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | 38 | | 45 | ns | |
| $t_{ZL}$ | | | 24 | | 25 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | 33 | | 37 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | 36 | | 37 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## DEFINITION OF FUNCTIONAL TERMS

**A, B** — Select the two select inputs to the decoder/demultiplexer.

**$\overline{E}$ Enable** — The enable input to the decoder. A HIGH input forces the decoding functions to be inhibited regardless of the A and B inputs.

**POL** — Polarity Input. The polarity input forces the outputs either an active-HIGH state or an active-LOW state. A LOW on the polarity input forces the output active-HIGH. A HIGH on the polarity input forces the outputs active-LOW.

**$\overline{OE}$** — Output Enable. A LOW on the $\overline{OE}$ input enables the outputs. A HIGH on the $\overline{OE}$ inputs forces the outputs to the high impedance (off) state.

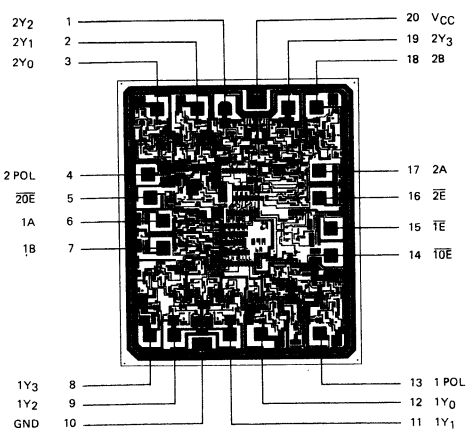
**$Y_0$, $Y_1$, $Y_2$, $Y_3$** — The four decoder/demultiplexer outputs.

## FUNCTION TABLE

| Function | Inputs | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{OE}$ | $\overline{E}$ | POL | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
| High Impedance | H | X | X | X | X | Z | Z | Z | Z |
| Disable | L | H | L | X | X | L | L | L | L |
| | L | H | H | X | X | H | H | H | H |
| Active-High Output | L | L | L | L | L | H | L | L | L |
| | L | L | L | L | H | L | H | L | L |
| | L | L | L | H | L | L | L | H | L |
| | L | L | L | H | H | L | L | L | H |
| Active-Low Output | L | L | H | L | L | L | H | H | H |
| | L | L | H | L | H | H | L | H | H |
| | L | L | H | H | L | H | H | L | H |
| | L | L | H | H | H | H | H | H | L |

H = HIGH X = Don't Care
L = LOW Z = High Impedance

### Metallization and Pad Layout

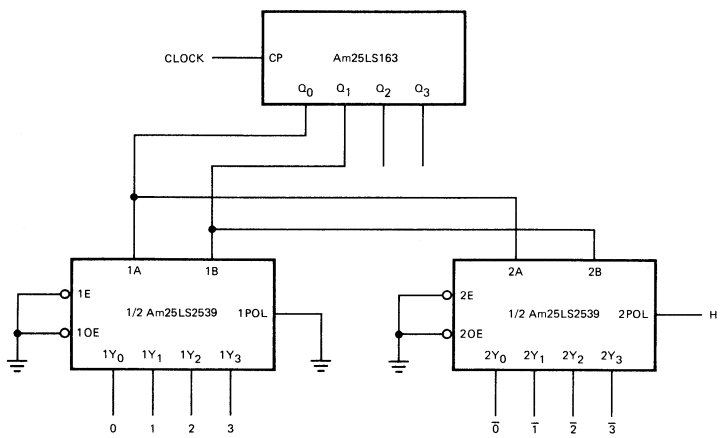


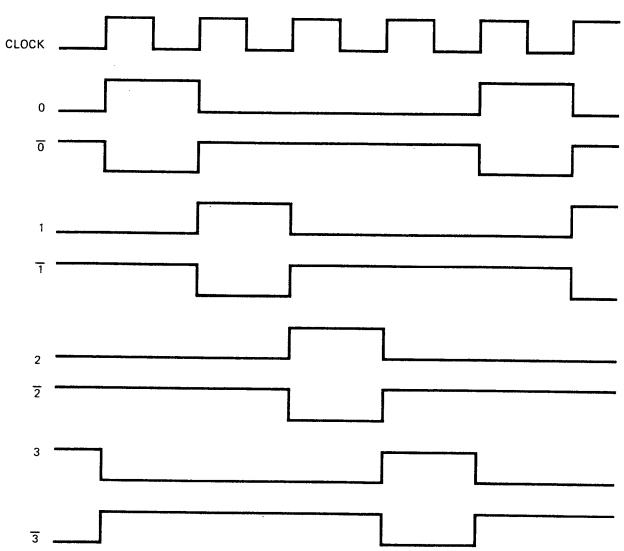

DIE SIZE 0.081" X 0.096"

## ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS2539PC |
| Hermetic DIP | 0°C to +70°C | AM25LS2539DC |
| Dice | 0°C to +70°C | AM25LS2539XC |
| Hermetic DIP | –55°C to +125°C | AM25LS2539DM |
| Hermetic Flat Pak | –55°C to +125°C | AM25LS2539FM |
| Dice | –55°C to +125°C | AM25LS2539XM |

## APPLICATIONS




FOUR PHASE CLOCK GENERATOR

# Am25LS2568 • Am25LS2569

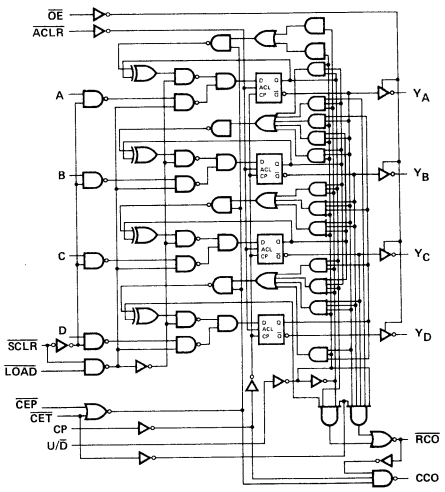
## Four-Bit Up/Down Counters With Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

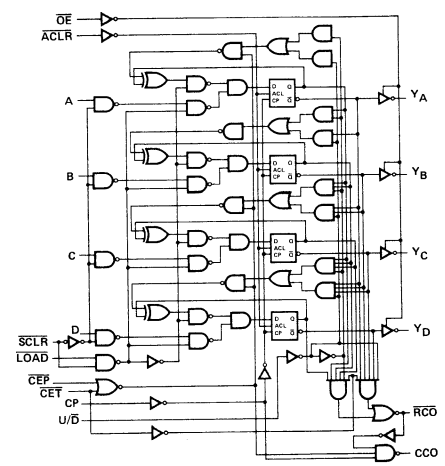
- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced low-power Schottky technology
- 100% product assurance screening to MIL-STD-883 requirements

### LOGIC DIAGRAMS

**Am25LS2568**




**Am25LS2569**

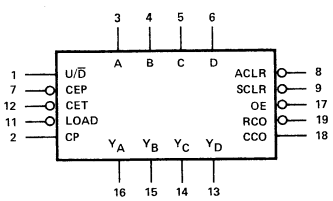



### FUNCTIONAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable ($\overline{OE}$) and asynchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock input (CP).

With the $\overline{LOAD}$ input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH. The up-down input (U/$\overline{D}$) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations requires only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CET}$. When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when $\overline{RCO}$ is LOW. Two active LOW reset lines are available, synchronous clear ($\overline{SCLR}$) and a master reset asynchronous clear ($\overline{ACLR}$). The output control ($\overline{OE}$) input forces the counter output into the high imepdance state when HIGH and when LOW, the counter outputs are enabled.

### LOGIC SYMBOL

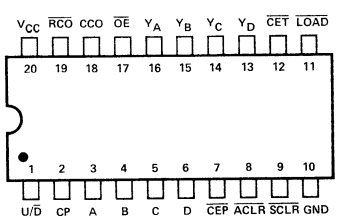



$V_{CC}$ = Pin 20

GND = Pin 10

### CONNECTION DIAGRAM

**Top View**




Note: Pin 1 is marked for orientation.

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | |
|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $Y_i$ | MIL, $I_{OH} = -1.0mA$ | | 2.4 | 3.4 | | Volts |
| | | | | COM'L, $I_{OH} = -2.6mA$ | | 2.4 | 3.2 | | |
| | | | $\overline{RCO}$, CCO | $I_{OH} = -440\mu A$ | MIL | 2.5 | 3.4 | | |
| | | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | MIL | | | 0.7 | Volts |
| | | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | $\overline{ACLR}$, $\overline{OE}$, U/$\overline{D}$, $\overline{Load}$ | | | | | 0.3 | mA |
| | | | A, B, C, D, CP, $\overline{CEP}$ | | | | | 0.4 | |
| | | | $\overline{CET}$, $\overline{SCLR}$ | | | | | 0.65 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | | 28 | 43 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ = HIGH, all other inputs = GND, all outputs open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Any Q; $\overline{Load}$ = LOW | | | 12 | 18 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 18 | 27 | | |
| $t_{PLH}$ | Clock to Any Q; $\overline{Load}$ = HIGH | | | 12 | 18 | ns | |
| $t_{PHL}$ | | | | 18 | 27 | | |
| $t_{PLH}$ | $\overline{CET}$ to $\overline{RCO}$ | | | 11 | 16 | ns | |
| $t_{PHL}$ | | | | 6 | 10 | | |
| $t_{PLH}$ | U/$\overline{D}$ to $\overline{RCO}$ | | | 15 | 23 | ns | |
| $t_{PHL}$ | | | | 13 | 20 | | |
| $t_{PLH}$ | Clock to $\overline{RCO}$ | | | 24 | 35 | ns | |
| $t_{PHL}$ | | | | 16 | 24 | | |
| $t_{PLH}$ | Clock to CCO | | | 10 | 15 | ns | |
| $t_{PHL}$ | | | | 8 | 13 | | |
| $t_{PLH}$ | $\overline{CET}$ or $\overline{CEP}$ to CCO | | | 8 | 12 | ns | |
| $t_{PHL}$ | | | | 17 | 25 | | |
| $t_{PLH}$ | $\overline{ACLR}$ to Any Q | | | N.A. | N.A. | ns | |
| $t_{PHL}$ | | | | 17 | 26 | | |
| $t_s$ | Set-up | A, B, C, D | 20 | | | ns | |
| | | $\overline{SCLR}$ | 20 | | | | |
| | | $\overline{Load}$ | 30 | | | | |
| | | U/$\overline{D}$ | 30 | | | | |
| | | $\overline{CET}$, $\overline{CEP}$ | 25 | | | | |
| $t_s$ | $\overline{SCLR}$ Recovery (inactive) to Clock | | 28 | | | ns | |
| $t_h$ | Data Hold | | 0 | | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 25 | 40 | | MHz | |
| $t_{pw}$ | Clock Pulse Width | | 20 | | | ns | |
| $t_{PZH}$ | $\overline{OE}$ to Any Q; Enable | | | | 11 | ns | |
| $t_{PZL}$ | | | | | 19 | | |
| $t_{PHZ}$ | $\overline{OE}$ to Any Q; Disable | | | | 18 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{PLZ}$ | | | | | 24 | | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | OUTPUTS | | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CP | D | C | B | A | $\overline{LOAD}$ | $\overline{CET}$ | $\overline{CEP}$ | V/$\overline{D}$ | $\overline{ACLR}$ | $\overline{SCLR}$ | $\overline{OE}$ | $\overline{RCO}$ | CCO | $Y_D$ | $Y_C$ | $Y_B$ | $Y_A$ | |
| ↑ | X | X | X | X | H | L | L | H | H | H | L | A/R | A/R | ($Q_T$ − CP) + 1 | | | | Count up |
| ↑ | X | X | X | X | H | L | L | L | H | H | L | A/R | A/R | ($Q_T$ − CP) − 1 | | | | Count Down |
| ↑ | X | X | X | X | H | H | X | X | H | H | L | H | H | NC | NC | NC | NC | Count Inhibit |
| ↑ | X | X | X | X | H | L | H | X | H | H | L | A/R | H | NC | NC | NC | NC | Count Inhibit |
| ⊓ | X | X | X | X | X | L | L | H | H | H | L | L | ⊓ | H | H | H | H | Overflow (LS2569) |
| ↑ | X | X | X | X | X | L | H | H | H | H | L | L | H | H | H | H | H | Overflow (LS2569) |
| ⊓ | X | X | X | X | X | L | L | H | H | H | L | L | ⊓ | H | L | L | H | Overflow (LS2568) |
| ↑ | X | X | X | X | X | L | H | H | H | H | L | L | H | H | L | L | H | Overflow (LS2568) |
| ↑ | X | X | X | X | X | H | X | H | H | H | L | H | H | H | H | H | H | Overflow Inhibit (LS2569) |
| ↑ | X | X | X | X | X | H | X | H | H | H | L | H | H | H | L | L | H | Overflow Inhibit (LS2568) |
| ⊓ | X | X | X | X | X | L | L | L | H | H | L | L | ⊓ | L | L | L | L | Underflow |
| ↑ | X | X | X | X | X | L | H | L | H | H | L | L | H | L | L | L | L | Underflow |
| ↑ | X | X | X | X | X | H | X | L | H | H | L | H | H | L | L | L | L | Underflow Inhibit |
| ↑ | L | H | L | H | L | X | X | X | H | H | L | H | H | L | H | L | H | Load Example |
| ↑ | X | X | X | X | X | X | X | H | L | L | L | H | H | L | L | L | L | Clear (Synchronous) |
| ⊓ | X | X | X | X | X | L | L | L | H | L | L | L | ⊓ | L | L | L | L | Clear (Synchronous) |
| ↑ | X | X | X | X | X | L | H | L | H | L | L | L | H | L | L | L | L | Clear (Synchronous) |
| ↑ | X | X | X | X | X | H | X | L | H | L | L | H | H | L | L | L | L | Clear (Synchronous) |
| X | X | X | X | X | X | X | X | H | L | X | L | H | H | L | L | L | L | Asynchronous Clear |
| ⊓ | X | X | X | X | X | L | L | L | L | X | L | L | ⊓ | L | L | L | L | Asynchronous Clear |
| X | X | X | X | X | X | L | H | L | L | X | L | L | H | L | L | L | L | Asynchronous Clear |
| X | X | X | X | X | X | H | X | L | L | X | L | H | H | L | L | L | L | Asynchronous Clear |
| X | X | X | X | X | X | X | X | X | X | X | H | X | X | Hi-Z | | | | Output Disabled |

($Q_T$ − CP) = Output state prior to clock edge
NC = No change

A/R = Assumes required output state; High except during Overflow and Underflow

X = Don't care

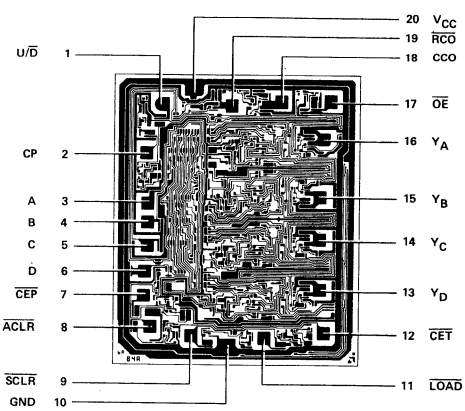
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min. | Am25LS COM'L Max. | Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min. | Am25LS MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Any Q; $\overline{Load}$ = LOW | | | 22 | | 24 | ns | $C_L = 50pF$, $R_L = 2.0k\Omega$ |
| $t_{PHL}$ | | | | 35 | | 40 | | |
| $t_{PLH}$ | Clock to Any Q; $\overline{Load}$ = HIGH | | | 22 | | 24 | ns | |
| $t_{PHL}$ | | | | 35 | | 40 | | |
| $t_{PLH}$ | $\overline{CET}$ to $\overline{RCO}$ | | | 18 | | 19 | ns | |
| $t_{PHL}$ | | | | 17 | | 21 | | |
| $t_{PLH}$ | U/$\overline{D}$ to $\overline{RCO}$ | | | 26 | | 28 | ns | |
| $t_{PHL}$ | | | | 26 | | 30 | | |
| $t_{PLH}$ | Clock to $\overline{RCO}$ | | | 39 | | 40 | ns | |
| $t_{PHL}$ | | | | 33 | | 39 | | |
| $t_{PLH}$ | Clock to CCO | | | 17 | | 18 | ns | |
| $t_{PHL}$ | | | | 22 | | 27 | | |
| $t_{PLH}$ | $\overline{CET}$ or $\overline{CEP}$ to CCO | | | 16 | | 17 | ns | |
| $t_{PHL}$ | | | | 36 | | 45 | | |
| $t_{PLH}$ | $\overline{ACLR}$ to Any Q | | | N.A. | | N.A. | ns | |
| $t_{PHL}$ | | | | 37 | | 45 | | |
| $t_s$ | Set-up | A, B, C, D | 25 | | 30 | | ns | |
| | | $\overline{SCLR}$ | 25 | | 30 | | | |
| | | $\overline{Load}$ | 38 | | 45 | | | |
| | | U/$\overline{D}$ | 40 | | 50 | | | |
| | | $\overline{CET}$, $\overline{CEP}$ | 33 | | 40 | | | |
| $t_s$ | SCLR Recovery (inactive) to Clock | | 39 | | 50 | | ns | |
| $t_h$ | Data Hold | | 0 | | 5 | | ns | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 20 | | 18 | | MHz | |
| $t_{pw}$ | Clock Pulse Width | | 27 | | 35 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to Any Q; Enable | | | 15 | | 17 | ns | |
| $t_{ZL}$ | | | | 26 | | 19 | | |
| $t_{HZ}$ | $\overline{OE}$ to Any Q; Disable | | | 23 | | 27 | ns | $C_L = 5.0pF$, $R_L = 2.0k\Omega$ |
| $t_{LZ}$ | | | | 30 | | 36 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
N.A. not applicable.

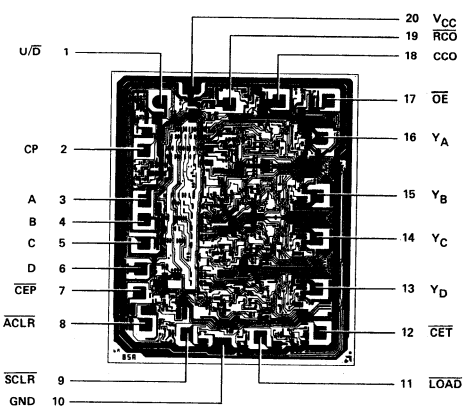
### Metallization and Pad Layouts

**Am25LS2568**




DIE SIZE 0.087" X 0.103"

**Am25LS2569**



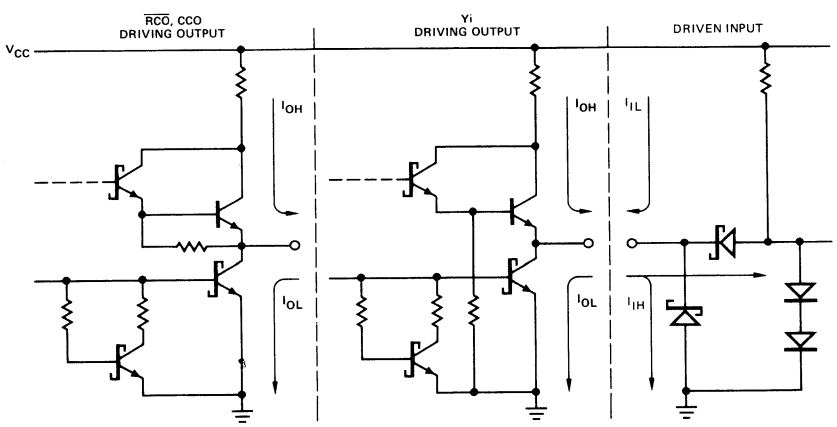

DIE SIZE 0.087" X 0.103"

## DEFINITION OF FUNCTIONAL TERMS

| | |
|---|---|
| **A, B, C, D** | The four programmable data inputs. |
| **$\overline{CEP}$** | Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{CEP}$ must be LOW to count. |
| **$\overline{CET}$** | Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count. |
| **CP** | Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock. |
| **$\overline{LOAD}$** | Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count. |
| **U/$\overline{D}$** | Up/Down Count Control. HIGH counts up and LOW counts down. |
| **$\overline{ACLR}$** | Asynchronous Clear. Master reset of counters to zero when $\overline{ACLR}$ is LOW, independent of the clock. |
| **$\overline{SCLR}$** | Synchronous clear of counters to zero on the next clock edge when $\overline{SCLR}$ is LOW. |
| **$\overline{OE}$** | A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output. |
| **$Y_A, Y_B, Y_C, Y_D$** | The four counter outputs. |
| **$\overline{RCO}$** | Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, $\overline{RCO}$ is LOW at 0000. |
| **CCO** | Clock Carry Output. While counting and $\overline{RCO}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition. |

3

### Am25LS
### LOW-POWER SCHOTTKY INPUT/OUTPUT
### CURRENT INTERFACE CONDITIONS

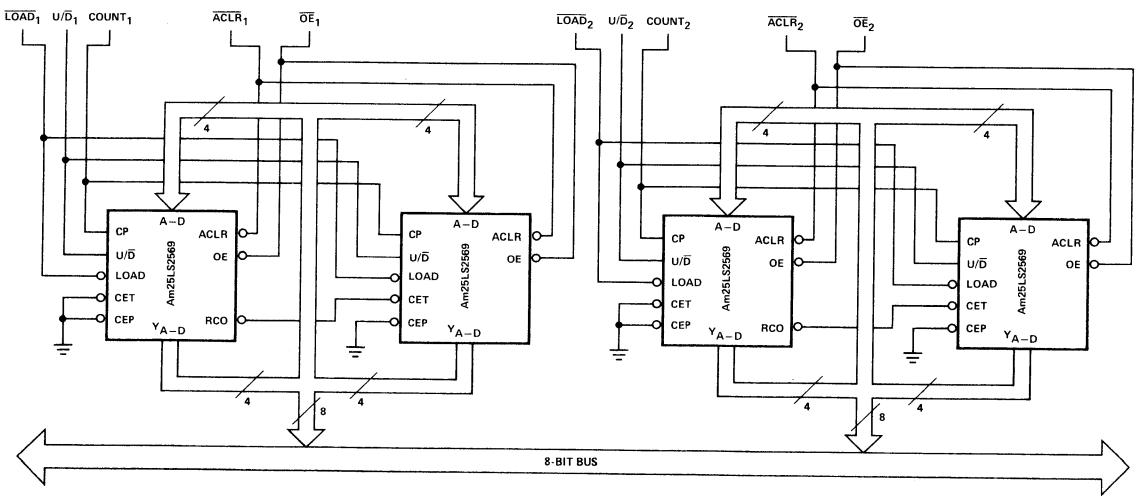



Note: Actual current flow direction shown.

## ORDERING INFORMATION

| Package Type | Temperature Range | Am25LS2568 Order Number | Am25LS2569 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25LS2568PC | AM25LS2569PC |
| Hermetic DIP | 0°C to +70°C | AM25LS2568DC | AM25LS2569DC |
| Dice | 0°C to +70°C | AM25LS2568XC | AM25LS2569XC |
| Hermetic DIP | −55°C to +125°C | AM25LS2568DM | AM25LS2569DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25LS2568FM | AM25LS2569FM |
| Dice | −55°C to +125°C | AM25LS2568XM | AM25LS2569XM |

## APPLICATION




MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS

# Am26LS29

## Quad Three-State Single Ended RS-423 Line Driver

### DISTINCTIVE CHARACTERISTICS

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- 50Ω transmission line drive capability
- High capacitive load drive capability
- Low $I_{CC}$ and $I_{EE}$ power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in hi-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

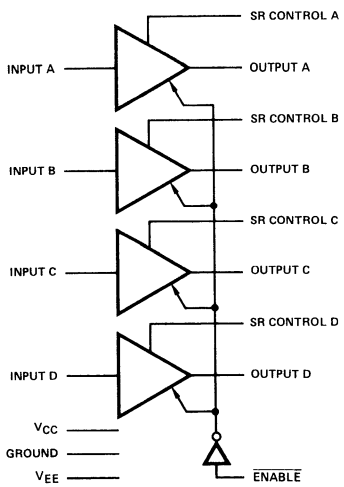
The Am26LS29 is a quad single ended line driver, designed for digital data transmission. The Am26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS29 has three-state outputs for bus oriented systems. The outputs in the hi-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the Am26LS29 line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

The Am26LS29 is constructed using advanced low-power Schottky processing.

### LOGIC DIAGRAM

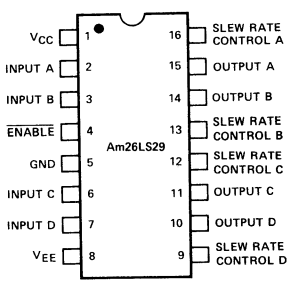



BLI-001

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | −55°C to +125°C | AM26LS29DM |
| Hermetic Flat Pak | −55°C to +125°C | AM26LS29FM |
| Dice | −55°C to +125°C | AM26LS29XM |
| Hermetic DIP | 0°C to +70°C | AM26LS29DC |
| Molded DIP | 0°C to +70°C | AM26LS29PC |
| Dice | 0°C to +70°C | AM26LS29XC |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

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## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Supply Voltage | |
| V+ | 7.0V |
| V− | −7.0V |
| Power Dissipation | 600mW |
| Input Voltage | −0.5 to +15.0V |
| Output Voltage (Power Off) | ±15V |
| Lead Soldering Temperature (10 seconds) | 300°C |

## ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS29XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = -5.0V \pm 5\%$
Am26LS29XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = -5.0V \pm 5\%$

## DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output Voltage | $R_L = \infty$ | $V_{IN} = 2.4V$ | 4.0 | 4.4 | 6.0 | Volts |
| $\overline{V_O}$ | | | $V_{IN} = 0.4V$ | −4.0 | −4.4 | −6.0 | Volts |
| $V_T$ | Output Voltage | $R_L = 450\Omega$ | $V_{IN} = 2.4V$ | 3.6 | 4.1 | | Volts |
| $\overline{V_T}$ | | | $V_{IN} = 0.4V$ | −3.6 | −4.1 | | Volts |
| $\lvert V_T \rvert - \lvert \overline{V_T} \rvert$ | Output Unbalance | $\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, $R_L = 450\Omega$ | | | 0.02 | 0.4 | Volts |
| $I_{X+}$ | Output Leakage Power Off | $V_{CC} = V_{EE} = 0V$ | $V_O = 10V$ | | 2.0 | 100 | μA |
| $I_{X-}$ | | | $V_O = -10V$ | | −2.0 | −100 | μA |
| $I_{S+}$ | Output Short Circuit Current | $V_O = 0V$ | $V_{IN} = 2.4V$ | | −70 | −150 | mA |
| $I_{S-}$ | | | $V_{IN} = 0.4V$ | | 60 | 150 | mA |
| $I_{Slew}$ | Slew Control Current | $V_{SLEW} = V_{EE} + 0.9V$ | | | ±110 | | μA |
| $I_{CC}$ | Positive Supply Current | $V_{IN} = 2.4V$, $R_L = \infty$ | | | 15 | 25 | mA |
| $I_{EE}$ | Negative Supply Current | $V_{IN} = 0.4V$, $R_L = \infty$ | | | −9 | −10 | mA |
| $I_O$ | Off State (High Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 10V$ | | 2.0 | 100 | μA |
| | | | $V_O = -10V$ | | −2.0 | −100 | μA |
| $V_{IH}$ | High Level Input Voltage | | | 2.0 | | | Volts |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | Volts |
| $I_{IH}$ | High Level Input Current | $V_{IN} = 2.4V$ | | | 1.0 | 40 | μA |
| | | $V_{IN} \leq 15V$ | | | 10 | 100 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{IN} = 0.4V$ | | | −30 | −200 | μA |
| $V_I$ | Input Clamp Voltage | $I_{IN} = -12mA$ | | | | −1.5 | Volts |

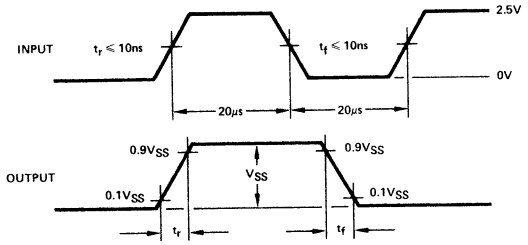
## AC CHARACTERISTICS

$V_{CC} = 5.0V$, $V_{EE} = -5.0V$, $T_A = 25°C$

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| Sr+ | Positive Slew Rate | $R_L = 450\Omega$, $C_L = 500pF$, Fig. 1 | $C_C = 50pF$ | | 3.0 | | μs |
| | | | $C_C = 0pF$ | | 120 | 300 | ns |
| Sr− | Negative Slew Rate | $R_L = 450\Omega$, $C_L = 500pF$, Fig. 1 | $C_C = 50pF$ | | 3.0 | | μs |
| | | | $C_C = 0pF$ | | 120 | 300 | ns |
| Src | Slew Rate Coefficient | $R_L = 450\Omega$, $C_L = 500pF$, Fig. 1 | | | .06 | | μs/pF |
| $t_{LZ}$ | Output Enable to Output | $R_L = 450\Omega$, $C_L = 5.0pF$, $C_C = 0pF$ | | | 180 | 300 | ns |
| $t_{HZ}$ | | | | | 250 | 350 | |
| $t_{ZL}$ | | $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$ | | | 250 | 350 | |
| $t_{ZH}$ | | | | | 180 | 300 | |

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.

## SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

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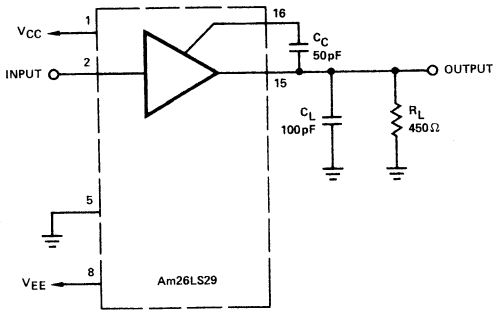
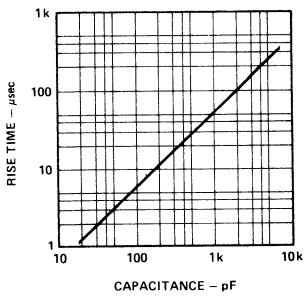



BLI-007

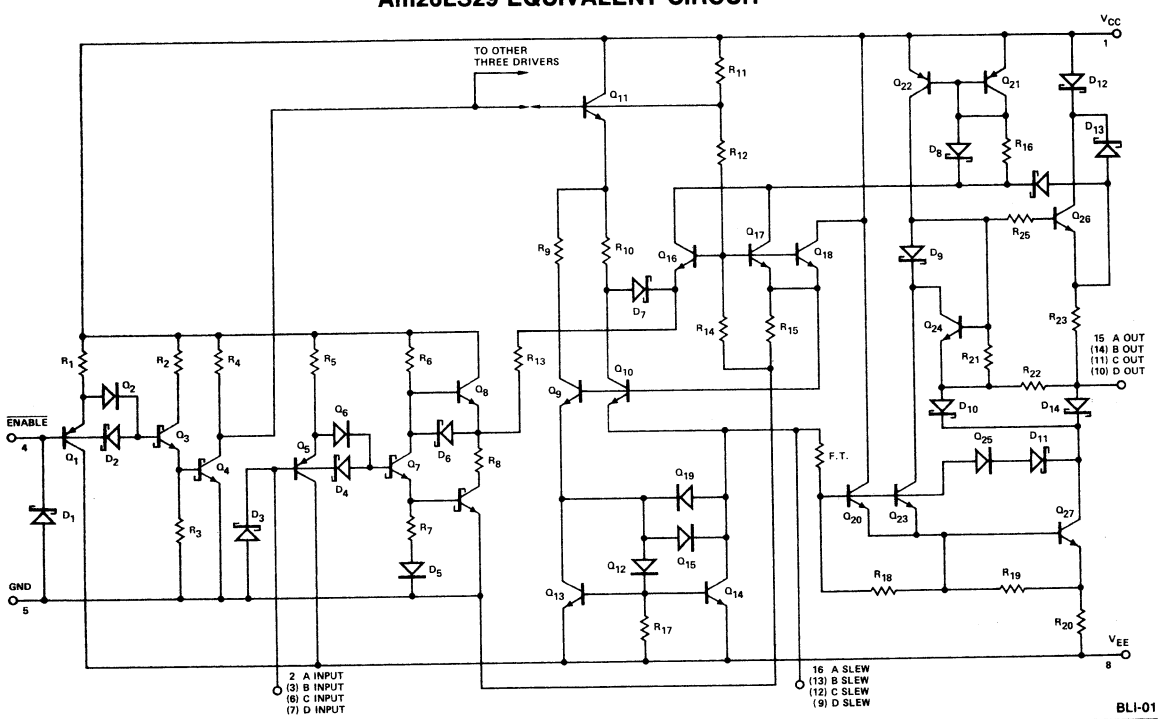
**Figure 1. Rise Time Control.**

### Slew Rate (Rise or Fall Time) Versus External Capacitor




BLI-010

### Am26LS29 EQUIVALENT CIRCUIT




BLI-011

# Am26LS30

## Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

### DISTINCTIVE CHARACTERISTICS

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in hi-impedance state
- Individually three-state drivers when used in differential mode
- Low $I_{CC}$ and $I_{EE}$ power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all of the requirements of EIA Standard RS-422 or four independent single-ended RS-423 line drivers.

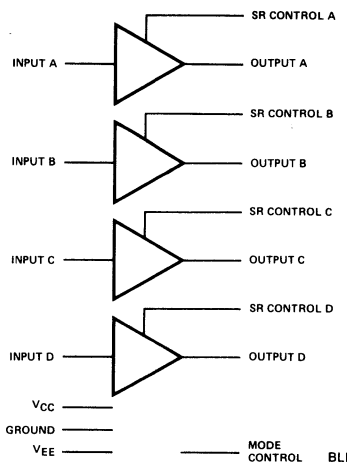
In the differential mode the outputs have individual three-state controls. In the hi-impedance state these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system would be the Am26LS30 differential line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS30 differential drivers.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS30 is constructed using Advanced Low Power Schottky processing.

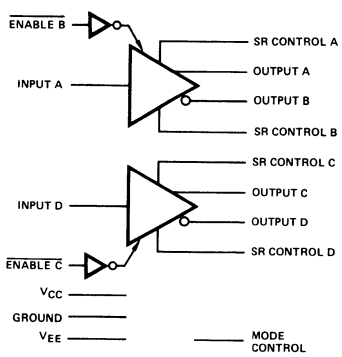
### LOGIC DIAGRAMS

**Logic for Am26LS30 with Mode Control HIGH (RS-423)**




BLI-002

**Logic for Am26LS30 with Mode Control LOW (RS-422)**

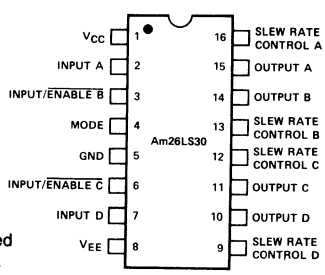



BLI-003

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | −55°C to +125°C | AM26LS30DM |
| Hermetic Flat Pak | −55°C to +125°C | AM26LS30FM |
| Dice | −55°C to +125°C | AM26LS30XM |
| Hermetic DIP | 0°C to +70°C | AM26LS30DC |
| Molded DIP | 0°C to +70°C | AM26LS30PC |
| Dice | 0°C to +70°C | AM26LS30XC |

### CONNECTION DIAGRAM – Top View




Note:
Pin 1 is marked for orientation.

BLI-005

## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Supply Voltage | |
| V+ | 7.0V |
| V− | −7.0V |
| Power Dissipation | 600mW |
| Input Voltage | −0.5 to +15.0V |
| Output Voltage (Power Off) | ±15V |
| Lead Soldering Temperature (10 seconds) | 300°C |

## ELECTRICAL CHARACTERISTICS over the operating temperature range

The Following Conditions Apply Unless Otherwise Specified:

Am26LS30XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = GND$
Am26LS30XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$
EIA RS-422 Connection, Mode Voltage = 0.8V

## DC CHARACTERISTICS over the operating temperature range

| Parameters | Description | Test Conditions (Note 3) | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_O$ | Differential Output Voltage, $V_{A, B}$ | $R_L = \infty$ | $V_{IN} = 2.0V$ | | 3.6 | 6.0 | Volts |
| $\overline{V_O}$ | | | $V_{IN} = 0.8V$ | | −3.6 | −6.0 | Volts |
| $V_T$ | Differential Output Voltage, $V_{A, B}$ | $R_L = 100\Omega$ | $V_{IN} = 2.0V$ | 2.0 | 2.4 | | Volts |
| $\overline{V_T}$ | | | $V_{IN} = 0.8V$ | −2.0 | −2.4 | | Volts |
| $V_{OS}$, $\overline{V_{OS}}$ | Common Mode Offset Voltage | $R_L = 100\Omega$ | | | 2.5 | 3.0 | Volts |
| $\lvert V_T \rvert - \lvert \overline{V_T} \rvert$ | Difference in Differential Output Voltage | $R_L = 100\Omega$ | | | 0.005 | 0.4 | Volts |
| $\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$ | Difference in Common Mode Offset Voltage | $R_L = 100\Omega$ | | | 0.005 | 0.4 | Volts |
| $V_{SS}$ | $\lvert V_T - \overline{V_T} \rvert$ | $R_L = 100\Omega$ | | 4.0 | 4.8 | | Volts |
| $V_{CMR}$ | Output Voltage Common Mode Range | $\overline{V_{ENABLE}} = 2.4V$ | | ±10 | | | Volts |
| $I_{XA}$ | Output Leakage Current | $V_{CC} = 0V$ | $V_{CMR} = 10V$ | | | 100 | μA |
| $I_{XB}$ | | | $V_{CMR} = -10V$ | | | −100 | μA |
| $I_{OX}$ | Off State (High Impedance) Output Current | $V_{CC} = MAX.$ | $V_{CMR} \leq 10V$ | | | 100 | μA |
| | | | $V_{CMR} \geq -10V$ | | | −100 | μA |
| $I_{SA}$, $I_{SB}$ | Output Short Circuit Current | $V_{IN} = 2.4V$ | $V_{OA} = 6.0V$ | | 80 | 150 | mA |
| | | | $V_{OB} = 0V$ | | −80 | −150 | mA |
| | | $V_{IN} = 0.4V$ | $V_{OA} = 0V$ | | −80 | −150 | mA |
| | | | $V_{OB} = 6.0V$ | | 80 | 150 | mA |
| $I_{CC}$ | Supply Current | | | | 18 | 30 | mA |
| $V_{IH}$ | High Level Input Voltage | | | 2.0 | | | Volts |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | Volts |
| $I_{IH}$ | High Level Input Current | $V_{IN} = 2.4V$ | | | 1.0 | 40 | μA |
| | | $V_{IN} \leq 15V$ | | | 10 | 100 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{IN} = 0.4V$ | | | −30 | −200 | μA |
| $V_I$ | Input Clamp Voltage | $I_{IN} = -12mA$ | | | | −1.5 | Volts |

## AC CHARACTERISTICS

EIA RS-422 Connection, $V_{CC} = 5.0V$, $V_{EE} = GND$, Mode = 0.4V, $T_A = 25°C$

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $t_r$ | Differential Output Rise Time | Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$ | | 120 | 200 | ns |
| $t_f$ | Differential Output Fall Time | Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$ | | 120 | 200 | ns |
| $t_{PDH}$ | Output Propagation Delay | Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$ | | 120 | 200 | ns |
| $t_{PDL}$ | Output Propagation Delay | Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$ | | 120 | 200 | ns |

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = GND$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. $R_L$ connected between each output and its complement.

## ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS30XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = -5.0V \pm 10\%$
Am26LS30XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = -5.0V \pm 5\%$
RS-423 Connection, Mode Voltage $\geq 2.0V$

## DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output Voltage | $R_L = \infty$ | $V_{IN} = 2.4V$ | 4.0 | 4.4 | 6.0 | Volts |
| $\overline{V_O}$ | | | $V_{IN} = 0.4V$ | −4.0 | −4.4 | −6.0 | Volts |
| $V_T$ | Output Voltage | $R_L = 450\Omega$ | $V_{IN} = 2.4V$ | 3.6 | 4.1 | | Volts |
| $\overline{V_T}$ | | | $V_{IN} = 0.4V$ | −3.6 | −4.1 | | Volts |
| $\lvert V_T \rvert - \lvert \overline{V_T} \rvert$ | Output Unbalance | $\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, $R_L = 450\Omega$ | | | 0.02 | 0.4 | Volts |
| $I_{X+}$ | Output Leakage Power Off | $V_{CC} = V_{EE} = 0V$ | $V_O = 6.0V$ | | 2.0 | 100 | μA |
| $I_{X-}$ | | | $V_O = -6.0V$ | | −2.0 | −100 | μA |
| $I_{S+}$ | Output Short Circuit Current | $V_O = 0V$ | $V_{IN} = 2.4V$ | | −80 | −150 | mA |
| $I_{S-}$ | | | $V_{IN} = 0.4V$ | | 80 | 150 | mA |
| $I_{Slew}$ | Slew Control Current | $V_{SLEW} = V_{EE} + 0.9V$ | | | ±140 | | μA |
| $I_{CC}$ | Positive Supply Current | $V_{IN} = 2.4V$, $R_L = \infty$ | | | 18 | 30 | mA |
| $I_{EE}$ | Negative Supply Current | $V_{IN} = 0.4V$, $R_L = \infty$ | | | −10 | −22 | mA |
| $V_{IH}$ | High Level Input Voltage | | | 2.0 | | | Volts |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | Volts |
| $I_{IH}$ | High Level Input Current | $V_{IN} = 2.4V$ | | | 1.0 | 40 | μA |
| | | $V_{IN} \leq 15V$ | | | 10 | 100 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{IN} = 0.4V$ | | | −30 | −200 | μA |
| $V_I$ | Input Clamp Voltage | $I_{IN} = -12mA$ | | | | −1.5 | Volts |

## AC CHARACTERISTICS

RS-423 Connection, $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, Mode = 2.4V, $T_A = 25°C$

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| Sr+ | Positive Slew Rate | Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$ | $C_C = 50pF$ | | 3.0 | | μs |
| | | | $C_C = 0$ | | 120 | 300 | ns |
| Sr− | Negative Slew Rate | Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$ | $C_C = 50pF$ | | 3.0 | | μs |
| | | | $C_C = 0$ | | 120 | 300 | ns |
| Src | Slew Rate Coefficient | Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$ | | | .06 | | μs/pF |
| $t_{PDH}$ | Output Propagation Delay | Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0$ | | | 180 | 300 | ns |
| $t_{PDL}$ | Output Propagation Delay | Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0$ | | | 180 | 300 | ns |

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.

# Am26LS31

## Quad High Speed Differential Line Driver

### DISTINCTIVE CHARACTERISTICS

- Output skew — 2.0ns typical
- Input to output delay — 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

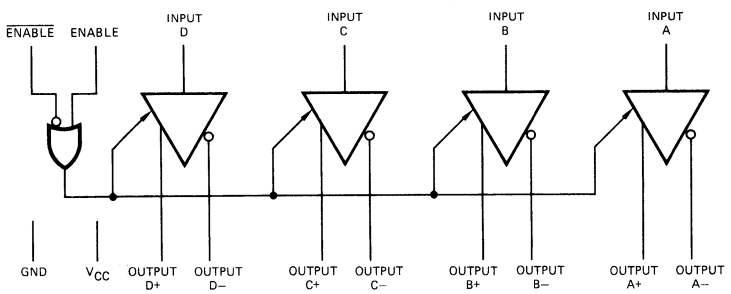
### FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

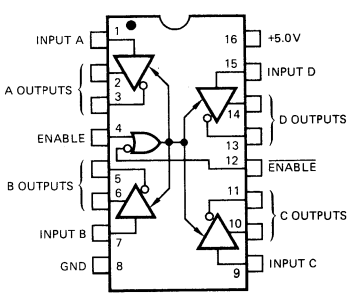
### LOGIC DIAGRAM




### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | –55°C to +125°C | AM26LS31DM |
| Flat Pak | –55°C to +125°C | AM26LS31FM |
| Dice | –55°C to +125°C | AM26LS31XM |
| Hermetic DIP | 0°C to +70°C | AM26LS31DC |
| Molded DIP | 0°C to +70°C | AM26LS31PC |
| Dice | 0°C to +70°C | AM26LS31XC |

### CONNECTION DIAGRAM
(Top View)




Note: Pin 1 is marked for orientation.

## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Supply Voltage | 7.0V |
| Input Voltage | 7.0V |
| Output Voltage | 5.5V |
| Storage Temperature Range | −65°C to +150°C |

## ELECTRICAL CHARACTERISTICS over the operating temperature range

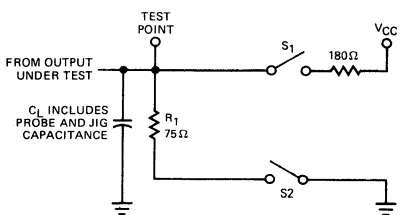
The following conditions apply unless otherwise specified:

Am26LS31XM (MIL) $T_A$ = −55°C to +125°C $V_{CC}$ = 5V ± 10%
Am26LS31XC (COM'L) $T_A$ = 0°C to +70°C $V_{CC}$ = 5V ± 5%

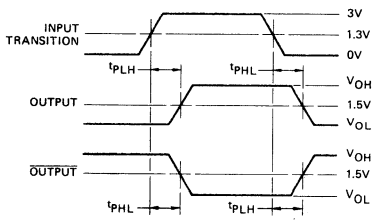
| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −20mA | | 2.5 | 3.2 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 20mA | | | 0.32 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Min. | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4V | | | −0.20 | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7V | | | 0.5 | 20 | µA |
| $I_I$ | Input Reverse Current | $V_{CC}$ = Max., $V_{IN}$ = 7.0V | | | 0.001 | 0.1 | mA |
| $I_O$ | Off-State (High Impedance) Output Current | $V_{CC}$ = Max. | $V_O$ = 5.5V | | 0.5 | 20 | µA |
| | | | $V_O$ = 0.5V | | 0.5 | −20 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min., $I_{IN}$ = 18mA | | | −0.8 | −1.5 | Volts |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max. | | −30 | −60 | −150 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max., all outputs disabled | | | 60 | 80 | mA |
| $t_{PLH}$ | Input to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, Load = Note 2 | | | 12 | 20 | ns |
| $t_{PHL}$ | Input to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, Load = Note 2 | | | 12 | 20 | ns |
| SKEW | Output to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, Load = Note 2 | | | 2.0 | 6.0 | ns |
| $t_{LZ}$ | Enable to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, $C_L$ = 10pF | | | 23 | 35 | ns |
| $t_{HZ}$ | Enable to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, $C_L$ = 10pF | | | 17 | 30 | ns |
| $t_{ZL}$ | Enable to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, Load = Note 2 | | | 35 | 45 | ns |
| $t_{ZH}$ | Enable to Output | $V_{CC}$ = 5.0V, $T_A$ = 25°C, Load = Note 2 | | | 30 | 40 | ns |

Notes: 1. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25°C.
2. $C_L$ = 30pF, $V_{IN}$ = 1.3V to $V_{OUT}$ = 1.3V, $V_{PULSE}$ = 0V to +3.0V, See Below.

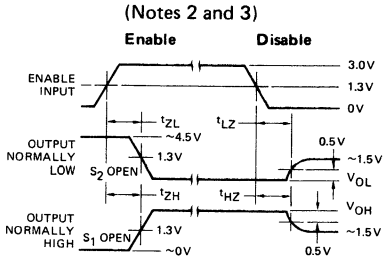
### AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS




### PROPAGATION DELAY (Notes 1 and 3)

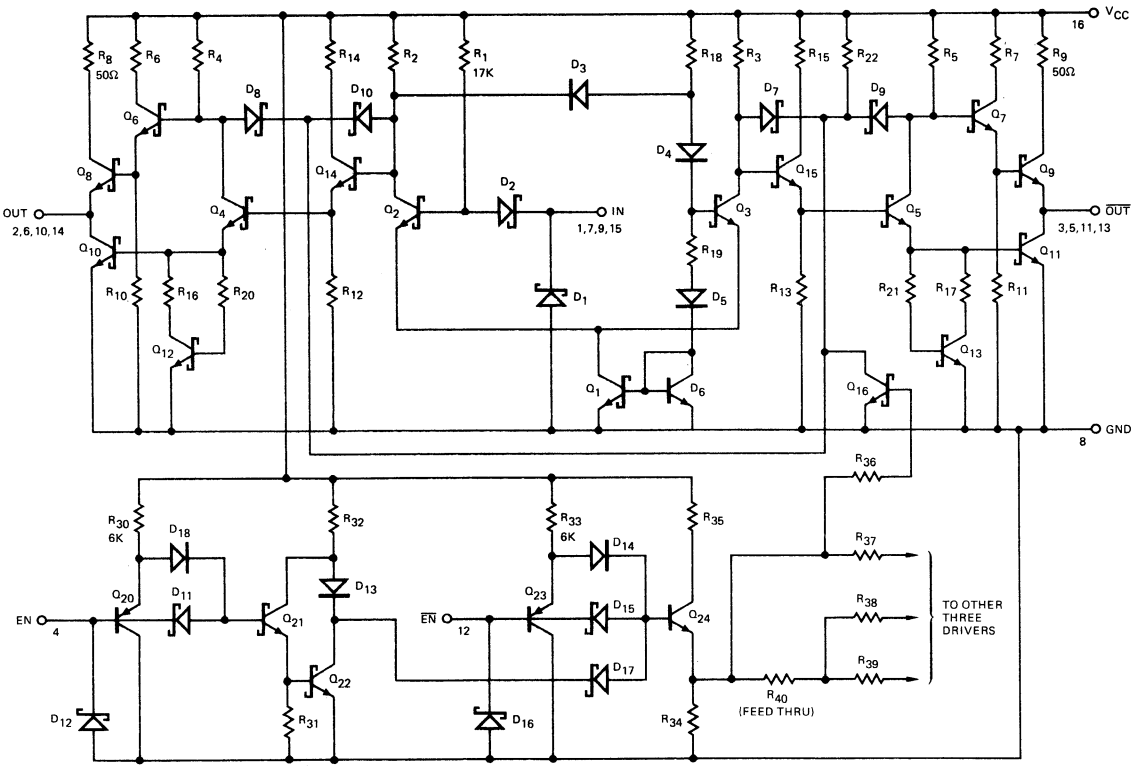



### ENABLE AND DISABLE TIMES (Notes 2 and 3)

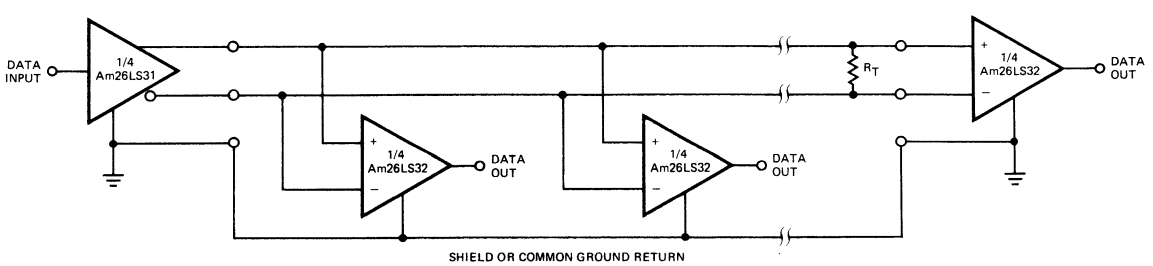



Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. $S_1$ and $S_2$ of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_O$ = 50Ω; $t_r$ ≤ 15ns; $t_f$ ≤ 6.0ns.

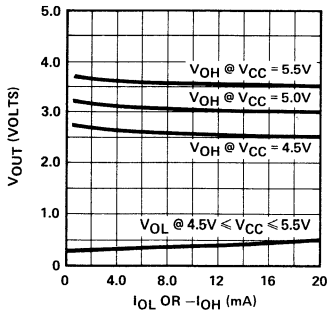
## EQUIVALENT CIRCUIT (1/4 Am26LS31)



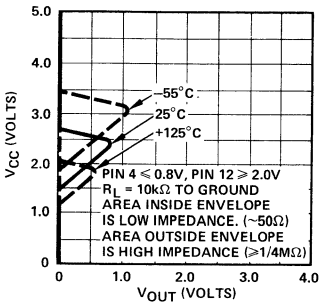

## TYPICAL APPLICATION



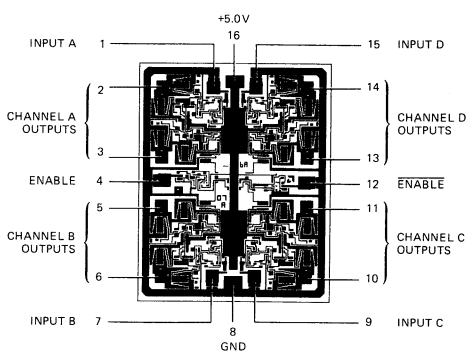
**Guaranteed $V_{OH}$ and $V_{OL}$**
**($T_A$ = –55°C to +125°C)**




**$V_{OUT}$ Versus $V_{CC}$**




**Metallization and Pad Layout**




DIE SIZE 0.067" X 0.084"

# Am26LS32 • Am26LS33

## Quad Differential Line Receivers

### DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

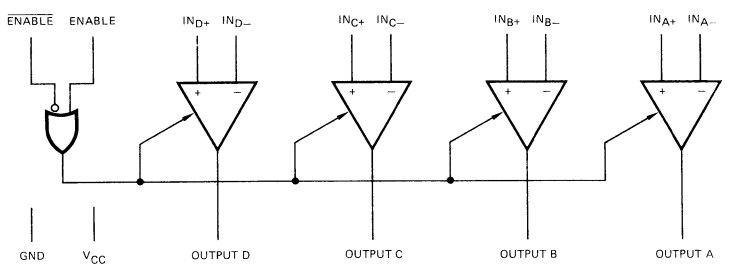
The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

3

### LOGIC DIAGRAM

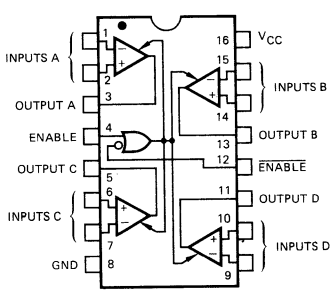



### ORDERING INFORMATION

| Package Type | Temperature Range | Am26LS32 Order Number | Am26LS33 Order Number |
|---|---|---|---|
| Hermetic DIP | −55°C to +125°C | AM26LS32DM | AM26LS33DM |
| Flat Pak | −55°C to +125°C | AM26LS32FM | AM26LS33FM |
| Dice | −55°C to +125°C | AM26LS32XM | AM26LS33XM |
| Hermetic DIP | 0°C to +70°C | AM26LS32DC | AM26LS33DC |
| Molded DIP | 0°C to +70°C | AM26LS32PC | AM26LS33PC |
| Dice | 0°C to +70°C | AM26LS32XC | AM26LS33XC |

### CONNECTION DIAGRAM

Top View




Note: Pin 1 is marked for orientation.

## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Supply Voltage | 7.0V |
| Common Mode Range | ±25V |
| Differential Input Voltage | ±25V |
| Enable Voltage | 7.0V |
| Output Sink Current | 50mA |
| Storage Temperature Range | −65°C to +165°C |

## ELECTRICAL CHARACTERISTICS Over the operating temperature range

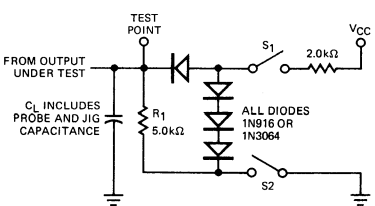
The following conditions apply unless otherwise specified:

Am26LS32XM, Am26LS33XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$
Am26LS32XC, Am26LS33XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

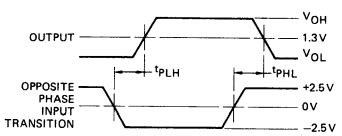
| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{TH}$ | Differential Input Voltage | $V_{OUT} = V_{OL}$ or $V_{OH}$ | Am26LS32, $-7V \leq V_{CM} \leq +7V$ | 0.2 | 0.06 | 0.2 | Volts |
| | | | Am26LS33, $-15V \leq V_{CM} \leq +15V$ | 0.5 | 0.12 | 0.5 | |
| $R_{IN}$ | Input Resistance | $-15V \leq V_{CM} \leq +15V$ (One input AC ground) | | 6.0k | 8.5k | | Ω |
| $I_{IN}$ | Input Current (Under Test) | $V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$ | | | | 2.3 | mA |
| $I_{IN}$ | Input Current (Under Test) | $V_{IN} = -15V$, Other Input $-15V \leq V_{IN} \leq +15V$ | | | | −2.8 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $\Delta V_{IN} = +1.0V$ | COM'L | 2.7 | 3.4 | | Volts |
| | | $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\mu A$ | MIL | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $\Delta V_{IN} = -1.0V$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | $V_{\overline{ENABLE}} = 0.8V$ | $I_{OL} = 8.0mA$ | | | 0.45 | |
| $V_{IL}$ | Enable LOW Voltage | | | | | 0.8 | Volts |
| $V_{IH}$ | Enable HIGH Voltage | | | 2.0 | | | Volts |
| $V_I$ | Enable Clamp Voltage | $V_{CC}$ = Min., $I_{IN} = -18mA$ | | | | −1.5 | Volts |
| $I_O$ | Off-State (High Impedance) Output Current | $V_{CC}$ = Max. | $V_O = 2.4V$ | | | 20 | μA |
| | | | $V_O = 0.4V$ | | | −20 | |
| $I_{IL}$ | Enable LOW Current | $V_{IN} = 0.4V$ | | | −0.2 | −0.36 | mA |
| $I_{IH}$ | Enable HIGH Current | $V_{IN} = 2.7V$ | | | 0.5 | 20 | μA |
| $I_I$ | Enable Input High Current | $V_{IN} = 5.5V$ | | | 1 | 100 | μA |
| $I_{SC}$ | Output Short Circuit Current | $V_O = 0V$, $V_{CC}$ = Max., $\Delta V_{IN} = +1.0V$ | | −15 | −50 | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max., All $V_{IN}$ = GND, Outputs Disabled | | | 52 | 70 | mA |
| $V_{HYST}$ | Input Hysteresis | $T_A = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$ | | | 30 | | mV |
| $t_{PLH}$ | Input to Output | $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below | | | 17 | 25 | ns |
| $t_{PHL}$ | Input to Output | $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below | | | 17 | 25 | ns |
| $t_{LZ}$ | Enable to Output | $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below | | | 20 | 30 | ns |
| $t_{HZ}$ | Enable to Output | $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below | | | 15 | 22 | ns |
| $t_{ZL}$ | Enable to Output | $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below | | | 15 | 22 | ns |
| $t_{ZH}$ | Enable to Output | $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below | | | 15 | 22 | ns |

Note: 1. All typical values are $V_{CC} = 5.0V$, $T_A = 25°C$.

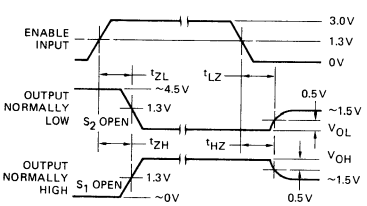
### LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS




### PROPAGATION DELAY (Notes 1 and 3)

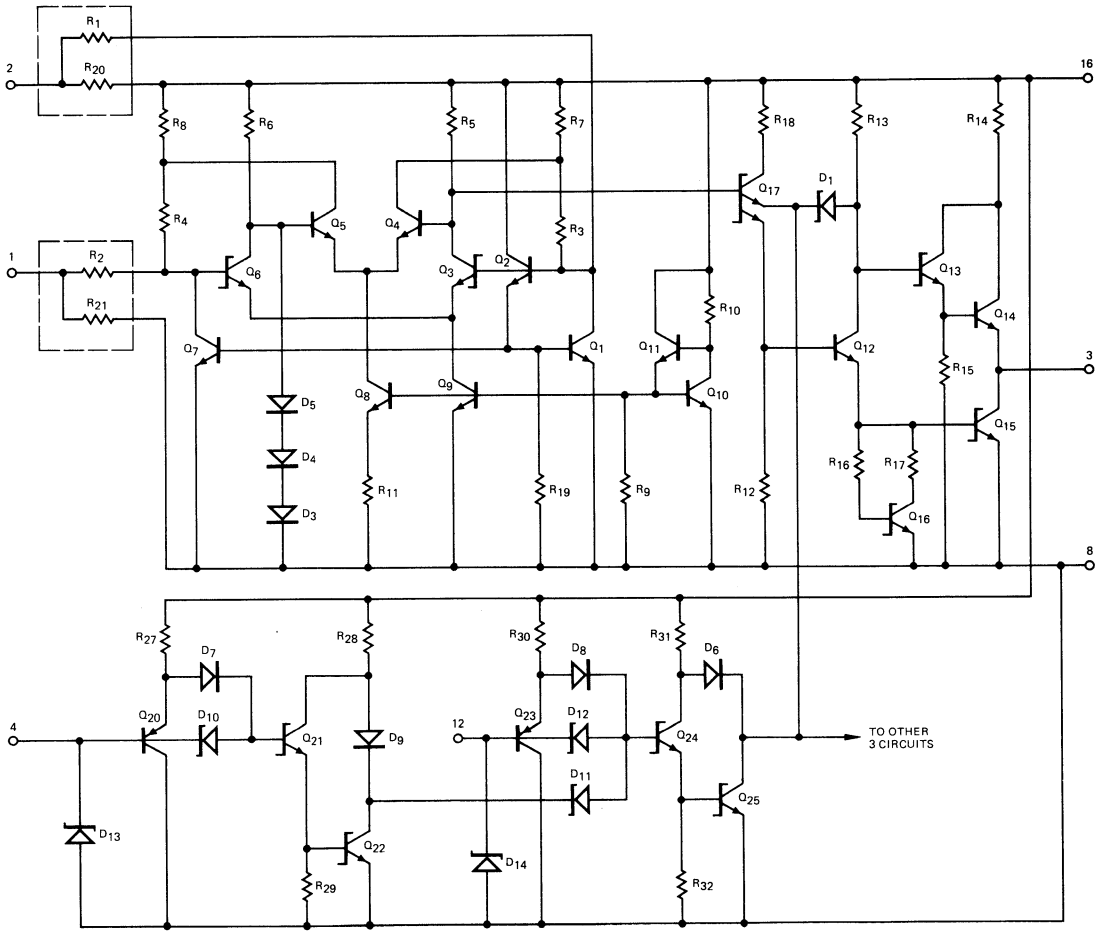



### ENABLE AND DISABLE TIMES (Notes 2 and 3)



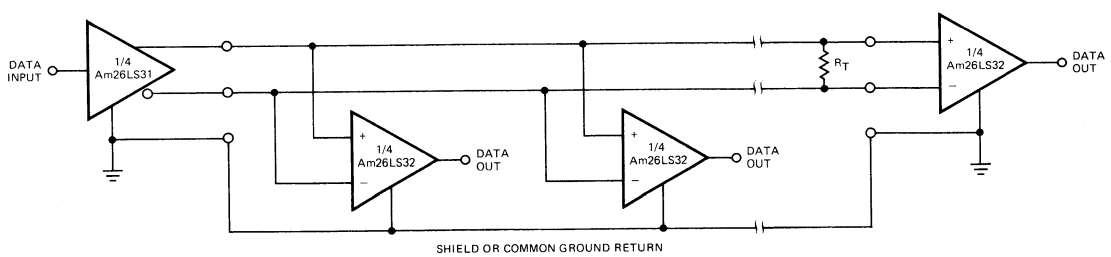

Notes:
1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. $S_1$ and $S_2$ of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_O = 50\Omega$; $t_r \leq 15ns$; $t_f \leq 6.0ns$.

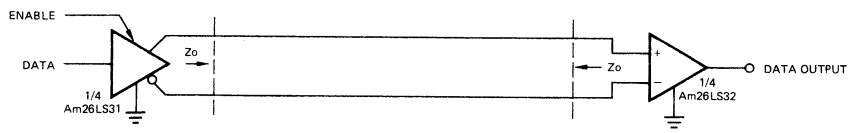
## EQUIVALENT CIRCUIT (1/4 Am26LS32 OR Am26LS33)



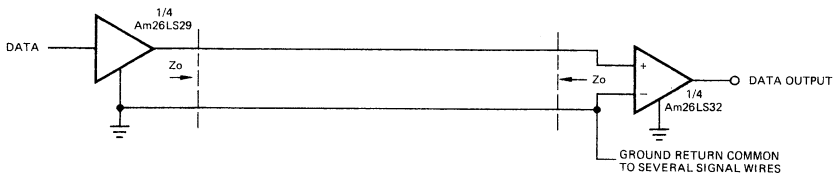

Note: $R_3$ and $R_4$ value for Am26LS32 is 2 times Am26LS33 value.

## TYPICAL APPLICATION






Two Wire Balanced System.




Single Wire With Common Ground Unbalanced System.

## LINE TERMINATION

It is important in a digital communication system to have the minimum amount of noise generated by undesired reflections at the driver and receiver. There are numerous ways of matching to the line. The line can be matched at the driver, at the receiver or both, each method has advantages and disadvantages. Generally for any but the longest lines it is sufficient to match at one place, and only when there are discontinuities in the line, party line operation, or lack of a reasonable match at the opposite end of the line is the extra hardware of matching at both ends justified. The majority of transmission lines have fairly low characteristic impedances (in the range of 50 to 200 ohms) and the currents involved for a reasonable voltage swing are quite large. It is more difficult to couple noise into this low impedance, but it is also more difficult to drive, and line drivers must have the ability to supply large currents.

Various matching techniques that can be employed are shown in Figure 1. These impedance charts are useful in showing what happens to wave fronts traveling down a line, when the line delay is longer than the wave front transition. The DC input characteristic of the receiver, including any external components, is plotted on the V-I graph together with the output characteristic of the driver, including any external components used at the driving end. There are always quiescent points – points where the driver and receiver characteristics cross. These points represent the DC voltage/current conditions, which must eventually be satisfied. To determine the effect of switching from one quiescent point to the other, a line with a slope equal to the characteristic impedance of the transmission line is plotted, starting at the initial quiescent point and ending at the applicable output impedance characteristic. The point of intersection gives the voltage and current at the output of the driver (and the input of the transmission line immediately after the driver switched states). From this point a line having an equal but opposite slope is drawn to the input characteristic and, at the intersection shows the voltage/current conditions of the wave front at the input of the receiver. This procedure is repeated to the output characteristic and so on at each intersection of the characteristic, the voltage/current relationship for a particular reflection is given. The resulting time/voltage relationships for the traveling wavefront at the two ends of the transmission line are shown alongside.

From the graphs several important features can be seen. If the line is not matched at either end considerable transient voltage swings can occur. In fact if the input and output characteristics are at right angles to one another, the reflections continue for an infinite time if the line is assumed to have zero loss. Most lines have extremely low losses, and, therefore, a very undesirable situation exists if the line is not matched at either end.

If the line is matched at the receiver, a voltage wave of constant amplitude travels down the line and is absorbed at the termination. Note whether the line is terminated to ground or to the power supply the system consumes DC power, either in the HIGH logic level or in the LOW logic level. In order to reduce the power dissipation, a blocking capacitor can be used in series with the receiver termination. The capacitor can be chosen to look like a short circuit to the voltage wavefront but stop DC (current) flow. Since the capacitor must be charged and discharged through the line, the data rate is reduced, when this technique is employed.

If the line is matched with a series resistor at the driver, then the line input initially rises to one half the final voltage. This wave front travels down the line and is reflected at the receiver. When the reflection reaches the driver the voltage at the driver rises to its final amplitude. The receiver, however, sees one transition from the initial to the final amplitude. When the driver switches from HIGH to LOW a similar situation occurs, in which the input of the line sees at first a step to one half the final value and, two line delays later, the final LOW condition. This back matching mode of operation consumes no DC power if the input impedance of the receiver is infinite. The advantage of the method is that if the input impedance of the receiver is high, very little power is dissipated and current only flows during the transition time, which is twice the line delay time. If back matching is used in a balanced system the terminating series resistance must be divided into two equal resistances with resistors inserted in series with each wire in order to maintain a balanced system.

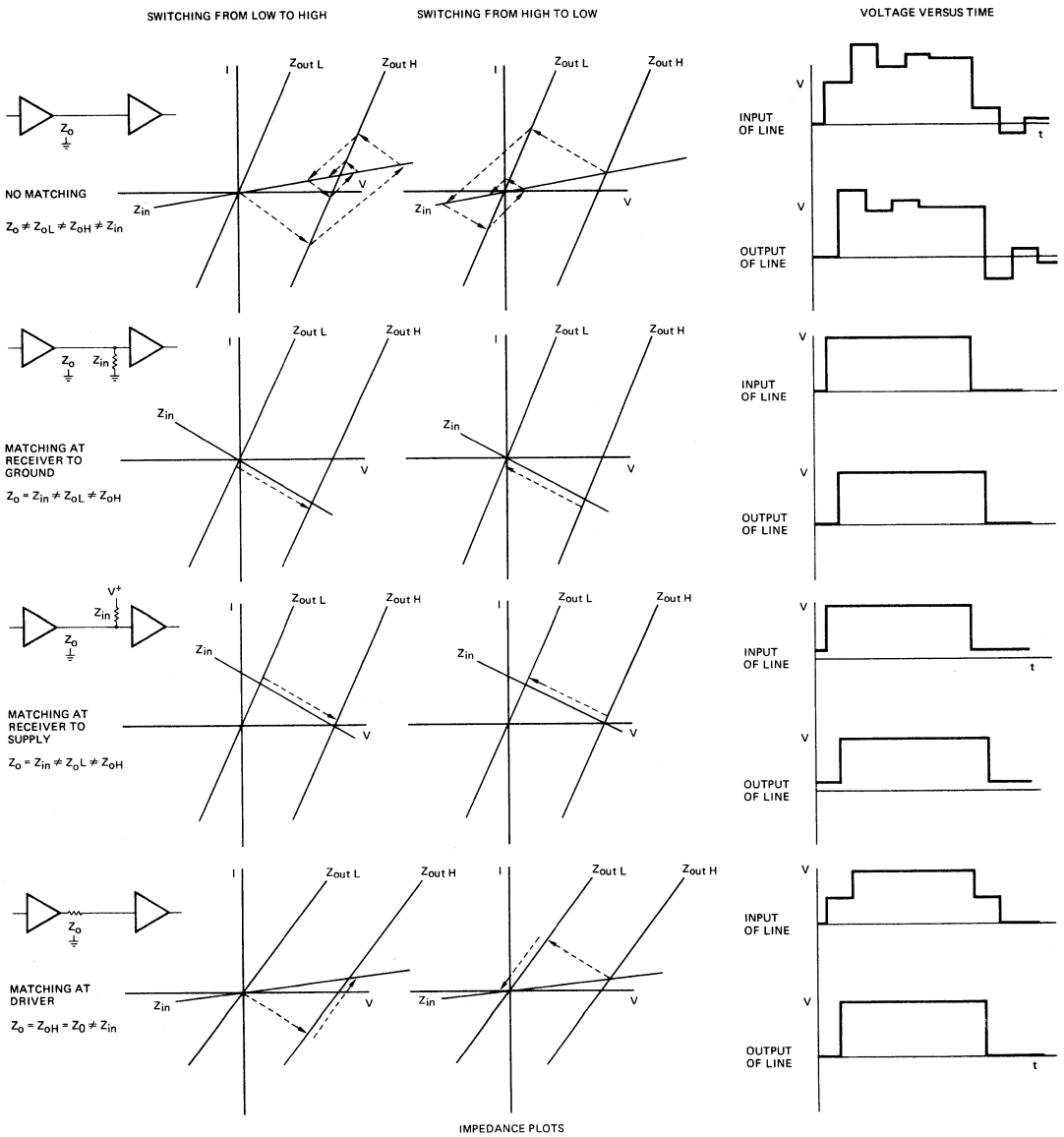
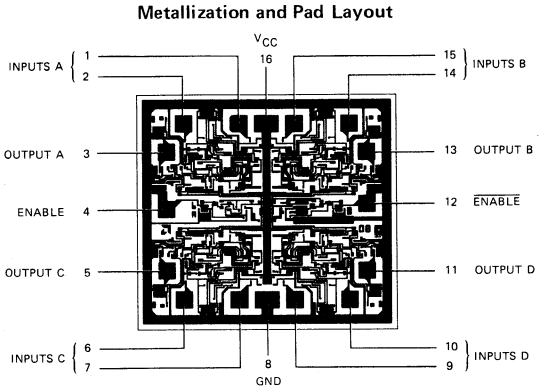



**Figure 1. Line Matching Methods**

## Metallization and Pad Layout




DIE SIZE
0.063" X 0.069"

# USE OF THE Am26LS30, 31 AND 32 QUAD DRIVER/RECEIVER FAMILY IN EIA RS-422 and 423 APPLICATIONS

By David A. Laws and Roy J. Levy

## INTRODUCTION

Today's high-performance data processing systems demand significantly faster data communications rates than are possible with the EIA RS-232 specifications in use for the past ten years.

Two new standards prepared by the Electronic Industries Association address this need. EIA RS-423 is an unbalanced, bipolar voltage specification designed to interface with RS-232C, while greatly enhancing its operation. It permits the communication of digital information over distances of up to 2000 feet and at data rates of up to 300 Kilobaud. EIA RS-422 is a balanced voltage digital interface for communicaton of digital data over distances of 4000 feet or data rates of up to 10 megabaud.

Advanced Micro Devices has developed a family of monolithic Low-power Schottky quad line drivers and receivers to meet the requirements of these specifications.

The Am26LS29 and 30 line drivers and the Am26LS32 receiver meet all requirements of RS-423 while the Am26LS31 differential line driver and the Am26LS32 receiver meet the requirements of RS-422.

A second receiver element, the Am26LS33 is available for use in high common mode noise environments, exceeding the common mode voltage requirements of RS-422 and RS-423.

This application note reviews the use of these devices in implementing the new standards. Emphasis is given to the EIA RS-422 balanced interface.

## EIA STANDARD SPECIFICATIONS

Two basic forms of operation are available for transmission of digital data over interconnecting lines. These are the single ended and differential techniques.

The single-ended form uses a single conductor to carry the signal with the voltage referenced to a single return conductor. This may also be the common return for other signal conductors. Figure 1a.

The single-ended form is the simplest way to send data as it requires only one signal line per circuit. This simplicity, however, is often offset by the inability of this form to allow discrimination between a valid signal produced by the driver, and the sum of the driver signal plus externally induced noise signals.

A solution to some of the problems inherent in the single-ended form of operation is offered by the differential form of operation. Figure 1b. This consists of a differential driver (essentially two single-ended drivers with one driver always producing the complementary output signal level to the other driver), a twisted pair transmission line and a differential line receiver. The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a common mode signal. The two signals, therefore, can be discriminated by a line receiver with a sufficient common mode voltage operating range.

The Electronic Industries Association, EIA, has defined a number of specifications standardizing the interface between data terminal equipment and data circuit terminating equipment based on both single-ended and differential operation.

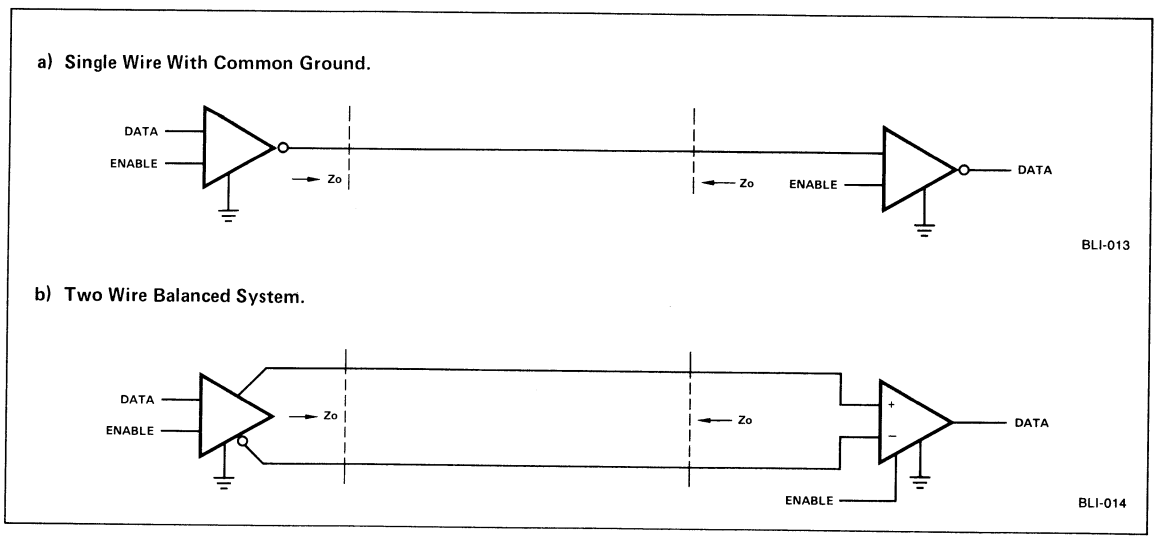


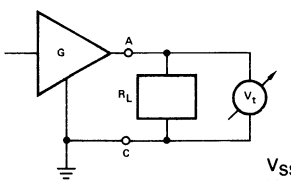

Figure 1. Data Communication Techniques.

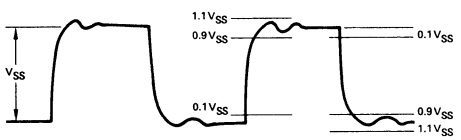
The most widely used standard for interfacing between data terminal equipment and data communications equipment today, is EIA RS-232C, issued in August 1969. The RS-232C electrical interface is a single-ended, bipolar-voltage, unterminated circuit. This specification is for serial binary data interchange over short distances (up to 50 feet) at low rates (up to 20 Kilobaud). It is a protocol standard as well as an electrical standard, specifying hand shaking signals and functions between terminal and the communications equipment. As already noted, single-ended circuits are susceptible to all forms of electromagnetic interference. Noise and cross talk susceptibility are proportional to length and bandwidth. RS-232C places restrictions on both. It limits slew rate of the drivers (30V/$\mu$s) to control radiated emission on neighboring circuits and allows bandwidth limiting on the receivers to reduce susceptibility to cross talk. The length and slew rate limits can adequately control reflections on unterminated lines, and the length and bandwidth limits are more than adequate to reduce susceptibility to noise.

Like EIA RS-232C, the new EIA RS-423 is also a single-ended, bipolar-voltage unterminated circuit. It extends the distance and data rate capabilities of this technique to distances of up to 4000 feet at data rates of 3000 baud, or at higher rates of up to 300 Kilobaud over a maximum distance of 40 feet.

EIA RS-422 is a differential, balanced voltage interface capable of significantly higher data rates over longer distances. It can accommodate rates of 100 Kilobaud over a distance of 4000 feet or rates of up to 10 megabaud. These performance improvements stem from the advantages of a balanced configuration which is isolated from ground noise currents. It is also immune to fluctuating voltage potentials between system ground references and to common mode electromagnetic interference. Figure 2 compares the driver output waveforms for the three EIA standard configurations, while Table I compares the key characteristics required by drivers and receivers intended for these applications. Since RS-232C has been in use for many years, RS-422 and 423 parameter values have been selected to facilitate an orderly transition from existing designs to new equipment.

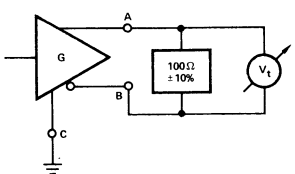
a) EIA RS-232C Generator Output.

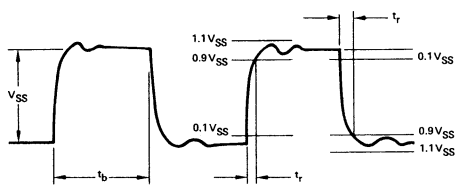



$V_{SS} = |V_t - \overline{V}_t|$
$V_{SS}$ = Difference in steady state voltages
$R_L$ = 3KΩ to 7KΩ
$V_{SS}$ min. = ±5V; $V_{SS}$ max. = ±25V

b) EIA RS-422 Generator Output.

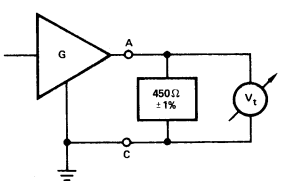


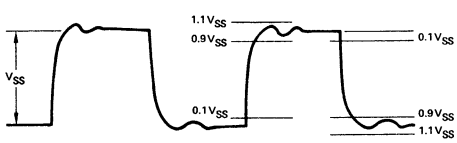




$t_D$ = Time duration of the unit interval at the applicable modulation rate
$t_r \leq 0.1t_D$ when $t_D \geq 200ns$
$t_r \leq 20ns$ when $t_D < 200ns$

$V_{SS}$ = Difference in steady state voltages
$V_{SS} = |V_t - \overline{V}_t|$
$V_{SS}$ min. = 2V; $V_{SS}$ max. = 6V

c) EIA RS-423 Generator Output.




$V_{SS} = |V_t - \overline{V}_t|$
$V_{SS}$ = Difference in steady state voltages
$V_{SS}$ min. = ±3.6V; $V_{SS}$ max. = ±6V

Figure 2. Driver Output Waveforms.

**TABLE I**
**KEY PARAMETERS OF EIA SPECIFICATIONS**

| Characteristics | EIA RS-232C | EIA RS-423 | EIA RS-422 | Units |
|---|---|---|---|---|
| Form of Operation | Single Ended | Single Ended | Differential | |
| Max. cable length | 50 | 2000 | 4000 | Feet |
| Max. data rate | 20K | 300K | 10M | Baud |
| Driver output voltage, open circuit* | ±25 | ±6 | 6 volts between outputs | Volts (Max.) |
| Driver output voltage, Loaded output* | ±5 to ±15 | ±3.6 | 2 volts between outputs | Volts (Min.) |
| Driver output resistance power off | Ro = 300Ω | 100μA between −6 to +6V | 100μA between +6 and −.25V | Min. |
| Driver output short circuit current $I_{SC}$ | ±500 | ±150 | ±150 | mA (Max.) |
| Driver output slew rate | 30 V/μsec Max. | Slew rate must be controlled based upon cable length and modulation rate | No control necessary | |
| Receiver input resistance $R_{in}$ | 3K to 7K | ≥4K | ≥4K | Ω |
| Receiver input thresholds | −3 to +3 | −0.2 to +0.2 | −0.2 to +0.2 | Volts (Max.) |
| Receiver input voltage | −25 to +25 | −12 to +12 | −12 to +12 | Volts (Max.) |

*± indicates polarity switched output.

## INTEGRATED CIRCUIT CHARACTERISTICS

Most semiconductor manufacturers offer integrated circuits designed to satisfy the old RS-232C standard. A number of them have designs in progress to meet the new EIA specifications. Products available from Advanced Micro Devices to meet these needs are shown in Table II.

The Am26LS29, 30, 31 and 32 are a family of quad drivers and receivers designed specifically to meet the new EIA standards. These products utilize Low-Power Schottky technology to incorporate four drivers or four receivers, together with control logic, in the standard 16-pin package outlines.

The Am26LS29/30 and the Am26LS32 are driver and receiver pairs designed to implement the single-ended EIA RS-423 standard. The Am26LS31 is a differential line driver designed for use with the Am26LS32 receiver in a differential mode to meet EIA RS-422.

## Am26LS29 AND Am26LS30 QUAD RS-423 LINE DRIVERS

The Am26LS29 and 30 consist of four single-ended line drivers designed to meet or exceed the requirements of RS-423. The buffered driver outputs are provided with sufficient source and sink current capability to drive 50 ohm to a virtual ground transmission line and high capacitive loads. The Am26LS29 has a three-state output control while the Am26LS30 has a Mode Control input that allows it to operate as a dual RS-422 driver (with suitable power supply changes), Figure 3.

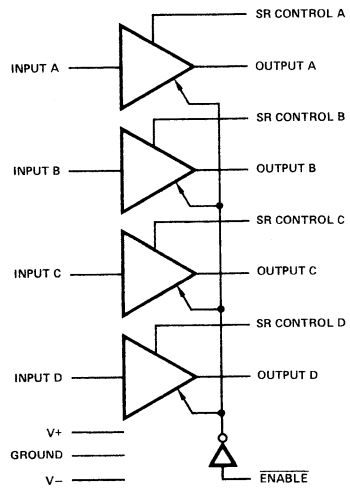
Each of the four driver inputs, as well as the $\overline{\text{Enable}}$/Mode Control input is a PNP Low-Power Schottky input for reduced input loading, one-half the normal fan-in. Since there are two inverters from each input to output, the driver is non-inverting. When operating in the RS-423 mode, the Am26LS29 and 30 require both +5V and −5V nominal value power supplies. This allows the outputs to swing symmetrically about ground – producing a true bipolar output. The Mode Control (Pin 4) of the Am26LS30 should be HI or tied to

**TABLE II**
**ADVANCED MICRO DEVICES' EIA COMPATIBLE DEVICES**

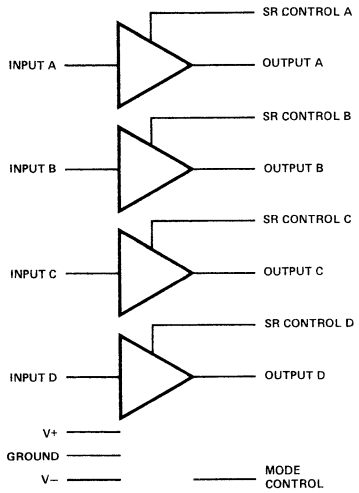
| EIA Standard | Drivers | Receivers |
|---|---|---|
| RS-232C | Am1488<br>Quad Driver | Am1489, 1489A<br>Quad Receivers with response control pin |
| | Am9616<br>Triple Driver with logic control | Am9617<br>Triple Receiver with optional hysteresis |
| | Am2616<br>Quad Driver also specified for CCITT V.24 and MIL-188C | Am2617<br>Quad Receiver specified over MIL range |
| RS-422 | Am26LS31<br>Quad Differential with three-state control gating | Am26LS32<br>Quad Differential Driver single-ended Receiver |
| RS-423 | Am26LS29<br>Quad Driver with three-state output<br>Am26LS30<br>Quad Driver with slew rate control | Am26LS32<br>Quad single-ended/ Differential Receiver |

a) Logic Diagrams

Am26LS29




Am26LS30
RS-423 Operation (Mode Control HIGH)




b) Circuit Diagram for Am26LS30

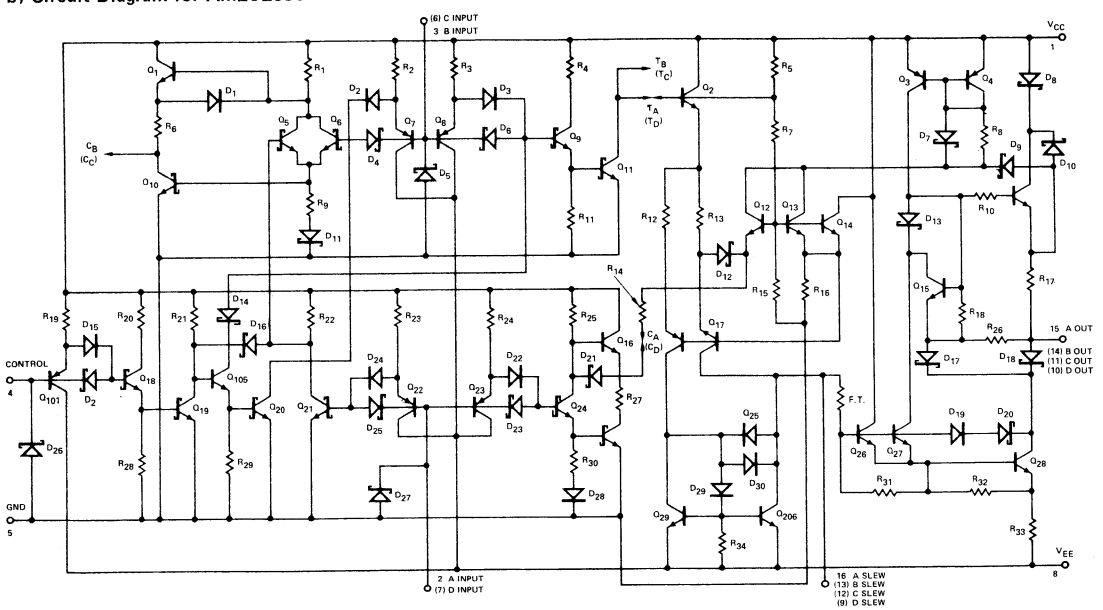



Figure 3. Am26LS29 and Am26LS30 Drivers.

$V_{CC}$. Each output is designed to drive the RS-423 load of 50 ohms with an output voltage equal or greater than +3.6 volts in the HI state and −3.6 volts in the LO state. Each output is current limited to 150mA max. in either logic state. A Slew Rate control pin is brought out separately for each output to allow output ramp rate (rise and fall time) control. This provides suppression of near end cross talk to other receivers in the cable. Connecting a capacitor from this node to that driver's respective output will produce a ramp (10% to 90%) of 50ns typical for each picofarad of capacitance in that capacitor. RS-423 establishes recommended ramp rates versus length of line driven and modulation rate, Figure 4.

The Am26LS30 can be used at low data rates as a dual EIA RS-422 driver with three-state outputs by connecting the $V_{EE}$ supply and the mode control input to ground.

## Am26LS31 QUAD RS-422 DRIVER

The Am26LS31 is a quad differential line driver designed to meet the RS-422 specification while operating with a single +5 volt supply. A common enable and disable function controls all four drivers, Figure 5. The driver features high speed, de-skewed differential outputs with typical propagation delays of 12ns and residual skew of 2ns. Both differential line outputs are designed for three-state operation to allow two-way half duplex and multiplex, data bus applications.

Table III is a summary of the essential requirements of the RS-422 standard. Section A describes the key characteristics satisfied by the Am26LS31 driver.

The balanced differential line driver consists of two halves, each of which is similar to a Low-power Schottky TTL gate with equal source and sink current capability. The two halves are emitter coupled in a differential input configuration. One side of the input circuit is tied to a fixed TTL bias threshold and the other side is tied to a sink diode in normal DTL/TTL fashion. This configuration offers complementary outputs with very low skew, dependent only upon component matching, a necessity to meet RS-422.

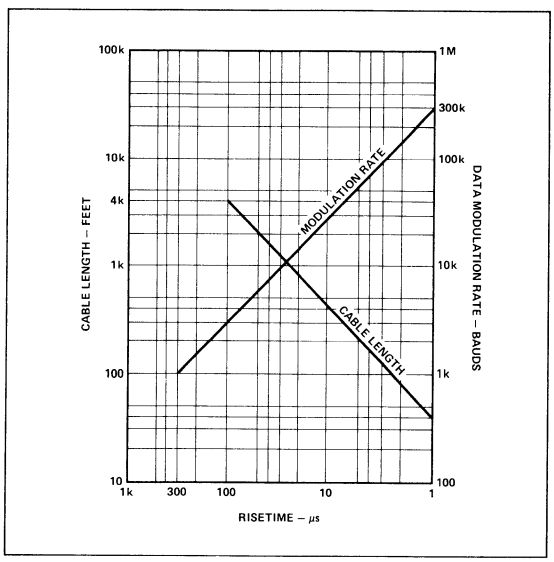



Figure 4. Data Modulation Rate or Cable Length Versus Risetime for EIA RS-423.

The circuit diagram of the driver is shown in Figure 6. The emitter-coupled input circuit is formed by Q2 and Q3, which are biased by a current source. This source is a current mirror, formed by Q1 which supplies the current, and D6 which is diode connected transistor matched to Q1. The fixed bias for Q3, formed by D5 and D6, is $2V_{BE}$. A $2V_{BE}$ bias, less the D2 Schottky diode drop, provides the normal Low-power Schottky TTL threshold, $V_{IL}$ = 0.7V. R19 provides a boost to 0.8V for a full 400mV TTL noise margin. The differential outputs of the emitter coupled stage, A and $\overline{A}$, drive emitter followers Q14 and Q15, which provide the required speed and matching characteristics. The emitter followers, drive phase splitters Q4 and Q5, which in turn drive totem-pole outputs. The outputs at the line interface are of standard Low-power Schottky TTL configuration, except that circuit values are modified to provide high sourcing capability. The outputs are designed to source or sink 20mA each, so that they can generate a voltage of at least 2.0V across a 100 ohm load, as required by RS-422. Additional circuitry has been included to make the line outputs three-state for two-way bus applications. The Am26LS31 meets the RS-422 requirement that the driver not load the line in the powered down condition ($I_X \leq 100\mu A$) or if the power supply to that device should fail.

## Am26LS32 QUAD RS-422 AND 423 RECEIVER

The Am26LS32 is a quad line receiver which, operating from a single 5 volt supply, can be used in either differential or single-ended modes to satisfy RS-422 and 423 applications respectively. A complementary enable and disable feature, similar to that on the driver, controls all four receivers, Figure 7. The device's three-state outputs, which can sink 8mA, incorporate a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 meets the receiver input specification of Table III, a 200mV threshold sensitivity with common mode rejection exceeding the supply line potentials, (greater than 7 volts). The same design feature of the input circuit which provides the common mode rejection also insures excellent power supply ripple rejection, which is important when switching the high currents involved in a system's interfaces. Furthermore, unlike operational amplifiers, where the DC common mode and power supply rejection ratios roll off with open loop gain, the full rejection capability of this line receiver is maintained at high frequencies. The receiver hysteresis of typically 30mV, provides differential noise immunity. Signals received on long lines can have slow transition times, and without hysteresis, a small amount of noise around the switching threshold can cause errors in the receiver output.

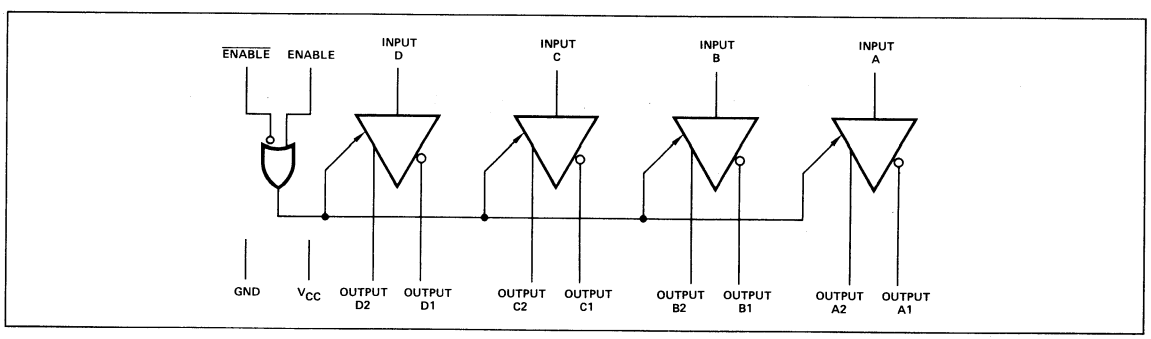



Figure 5. Am26LS31 Logic Diagram.

## TABLE III
## SUMMARY OF EIA RS-422 STANDARD FOR A BALANCED DIFFERENTIAL INTERFACE

### A. Line Driver

Open Circuit Voltage (either logic state)
- Differential: $|V_{do}| \leq 6.0V$
- Common Mode: $|V_{cmo}| \leq 3.0V$

Differential Output Voltage (across 100 ohm load)
- Either logic state: $|V_d| \geq \max(0.5V_{do}, 2.0V)$

Output Impedance
- Either logic state: $R_G \leq 100$ ohms

Mark-Space Level Symmetry (across 100 ohm load)
- Differential: $|V_{dS}| - |V_{dM}| \leq 0.4V$
- Common Mode: $|V_{cmS}| - |V_{cmM}| \leq 0.4V$

Output Short Circuit Current (to ground)
- Either Output: $|I_{SC}| \leq 150mA$

Output Leakage Current (power off)
- Voltage Range: $-0.25V \leq V_x \leq +6.0V$
- Either Output at $V_x$: $|I_X| \leq 100\mu A$

Rise and Fall Times (across 100 ohm load)
- T = Baud Interval: $(t_r, t_f) \leq \max(0.1T, 20ns)$

Ringing (across 100 ohm load)

Definitions

$V_{dSS} = V_d$ (steady state)

$V_{SS} = V_{dS} - V_{dM}$ (steady state)

Limits (either logic state)
- Percentage: $|V_d - V_{dSS}| \leq 0.1V_{SS}$
- Absolute: $2.0V \leq |V_d| \leq 6.0V$

### B. Line Receiver

Signal Voltage Range
- Differential: $|V_d| \leq 6.0V$
- Common Mode: $|V_{cM}| \leq 7.0V$

Single-Ended Input Current (power ON or OFF)
- Either Input at $V_x$: $|V_x| = 10V$
- Other Input Grounded: $|I_V| \leq 3.25mA$

Single-Ended Input Bias Voltage (other input grounded)
- Either Input Open Circuit: $|V_B| \leq 3.0V$

Single-Ended Input Impedance (other input grounded)
- Either Input: $R_L \geq 4000$ ohms

Differential Threshold Sensitivity
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Either Logic State: $|V_T| \leq 200mV$

Absolute Maximum Input Voltage
- Differential: $|V_d| \leq 12V$
- Single-Ended: $|V_x| \leq 10V$

Input Balance (threshold shift)
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$

Differential Threshold (500 ohms in series with each input)
- Either Logic State: $|V_t| \leq 400mV$

Termination (optional)
- Total Load Resistance (differential): $R_T > 90$ ohms

Multiple Receivers (bus applications)

Up to 10 receivers allowed. Differential threshold sensitivity of 200mV must be maintained.

Hysteresis (optional)

As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)

As required by application to provide a steady MARK or SPACE condition under open connector or driver power OFF condition.

### C. Interconnecting Cable

Type
- Twisted Pair Wire or Flat Cable Conductor Pair

Conductor Size
- Copper Wire (solid or stranded): 24 AWG or larger
- Other (per conductor): $R \leq 30$ ohms/1000 ft.

Capacitance
- Mutual Pair: $C \leq 20pF/ft.$
- Stray: $C \leq 40pF/ft.$

Pair-to-Pair Cross Talk (balanced)
- Attenuation at 150KHz: $A \geq 40dB$

3

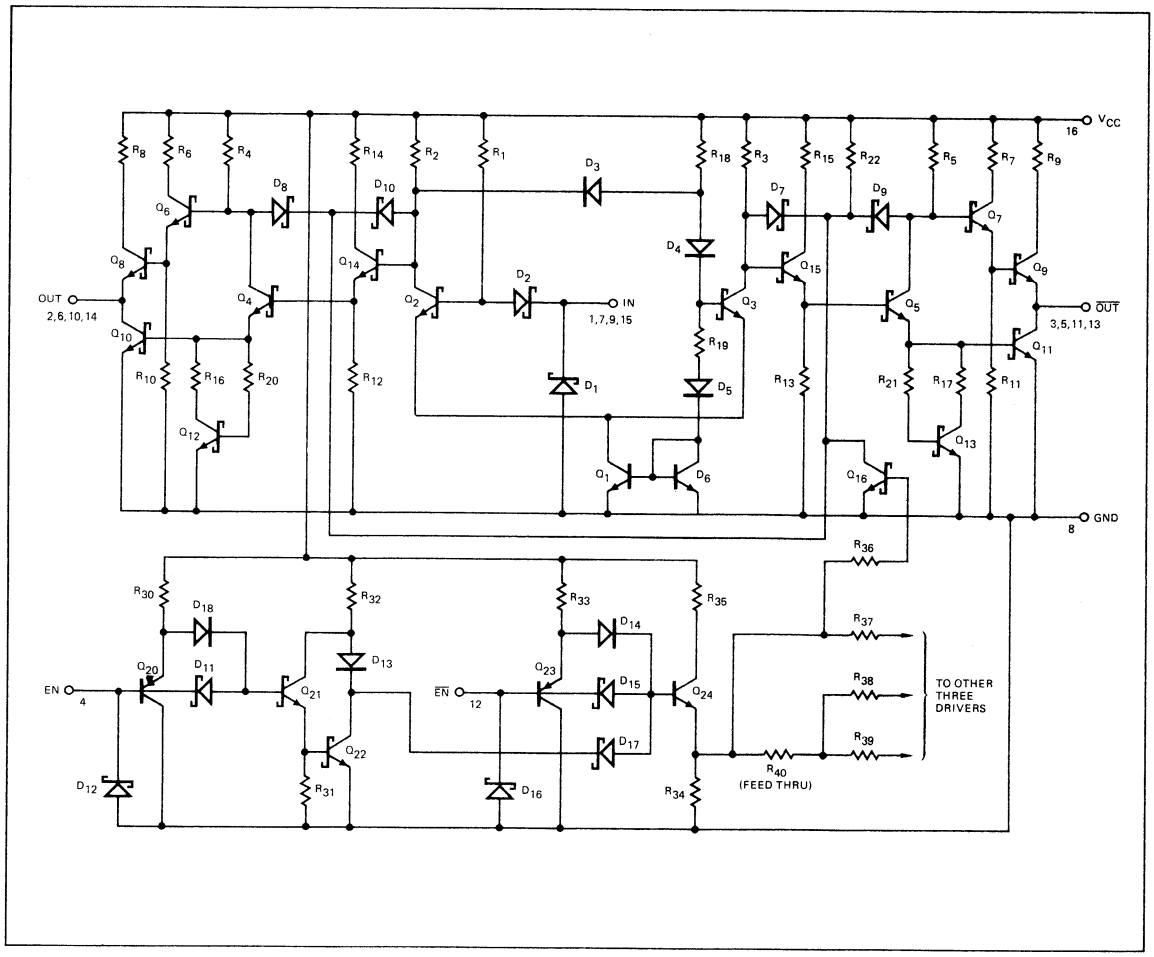



Figure 6. Am26LS31 Circuit Diagram (Only one driver shown).

The balanced differential line receiver is a three-stage circuit. The input stage consists of a low-impedance differential current amplifier with series resistor inputs to convert line signal voltage to current and provide a moderate input impedance. The input resistors provide an impedance greater than 6K on each input, power on or power off, which exceeds the requirements of RS-422 and RS-423. This is one advantage of the current amplifier input circuit. Another advantage is that is can operate with immunity to common mode voltages above $V_{CC}$ and below ground. The differential threshold sensitivity of this circuit is 200mV, as required by RS-422. The second stage is a differential voltage amplifier, which interfaces to the single-ended output stage through an emitter follower. The output stage is a standard Low-power Schottky TTL totem-pole output with three-state capability.

The full circuit is shown in Figure 8. Resistors $R_{20}$ and $R_{21}$, which connect the non-inverting input to $V_{CC}$ and the inverting input to ground, provide the fail-safe feature, which guarantees a HIGH logic state for the receiver output when there is no signal on the line. The differential voltage amplifier in the second stage is formed by Q6 and Q3 which are biased by current source Q9. The hysteresis in the receiver switching characteristic is provided by Q4 and Q5, a differential pair biased by current source Q6, whose collectors are connected in positive feedback to the input pull-up circuits. A small amount of current is switched by Q4 and Q5, which must be overcome by the different voltage signal, resulting in the hysteresis. The output stage is driven from one side of the differential second stage by emitter follower Q17, which is a multiple emitter transistor. the second emitter is the control point for the three-state output.Q17 drives the phase splitter Q12, which in turn drives the three-state totempole output. The remainder of the circuit is the output enable control logic. This three-state capability on the receiver TTL side of the interface is a useful feature for modularizing two-way bus design.

A mask option of the input resistors ($R_1$, $R_2$, $R_{20}$ and $R_{21}$) modifies the receiver characteristics to improve operation in high common mode noise environments. This device, known as the Am26LS33, has these resistors at twice the value of the Am26LS32. An input differential or common mode voltage range of ±15 volts is achieved at the expense of a minor decrease of input threshold sensitivity, to ±500mV from ±200mV.

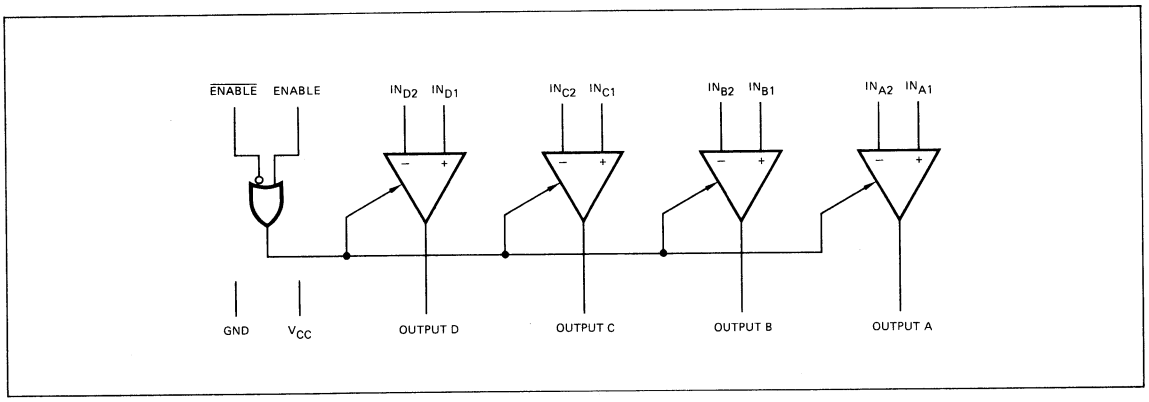
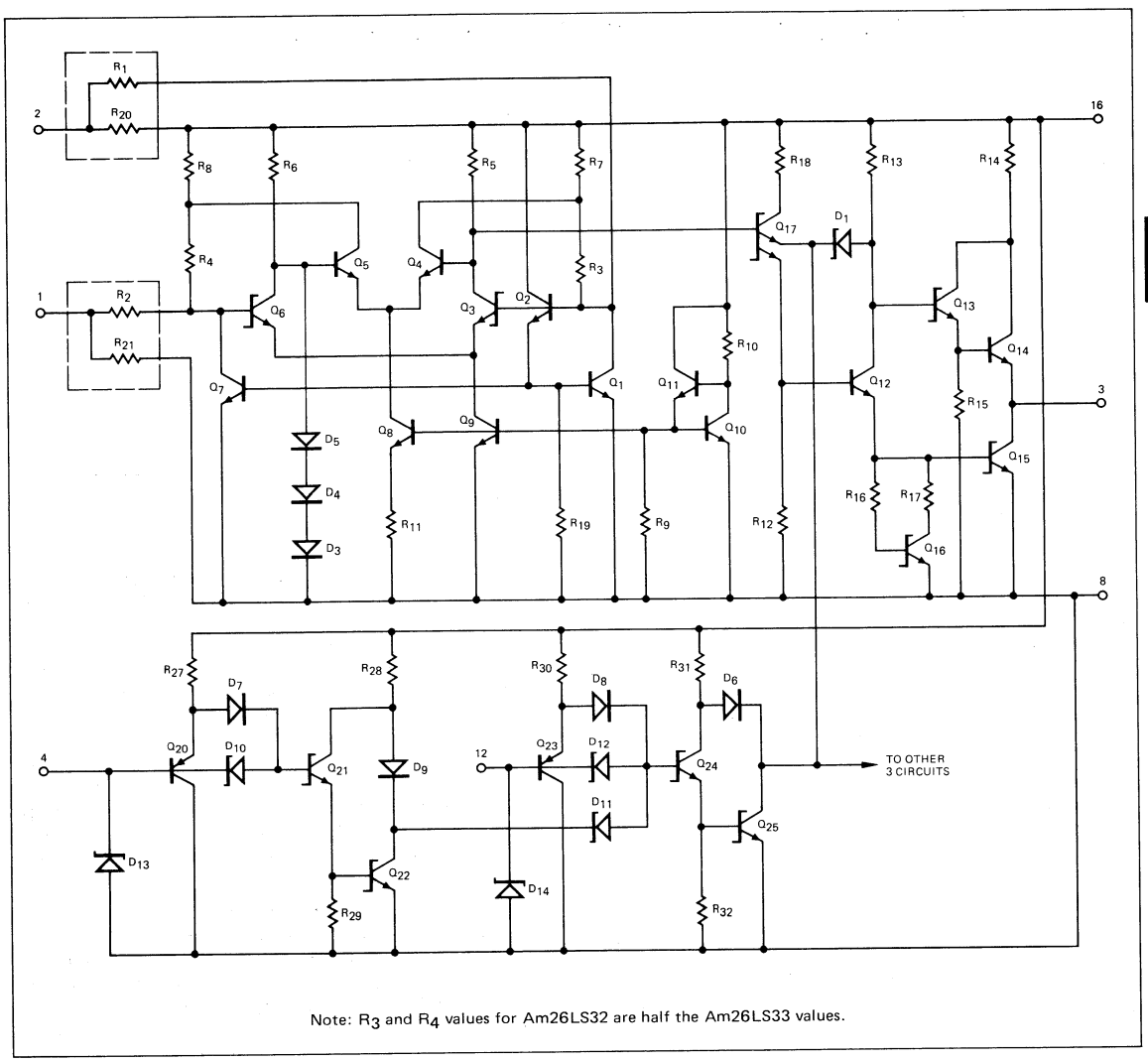



Figure 7. Am26LS32 Logic Diagram.




Note: $R_3$ and $R_4$ values for Am26LS32 are half the Am26LS33 values.

Figure 8. Am26LS32 and Am26LS33 Circuit Diagram (Only one receiver shown).

## APPLICATIONS IN MIXED RS-232 AND 422/3 SYSTEMS

A system implemented with the RS-422 differential output cannot be used to drive an RS-232C system directly. An RS-423 single-ended driver, such as the Am26LS29 or Am26LS30, may be used provided certain precautions are observed.

1. Although the RS-423 driver output specification of between 4 to 5V does not meet the RS-232C specification of 6V, operation is usually satisfactory with RS-232C receivers. This is achieved because the short cable lengths permitted by RS-232C cause very little signal degredation and because of the low source impedance of the RS-423 driver.
2. RS-232C specifies that the rise time for the signal to pass through the ±3.0V transition region shall not exceed 4% of the signal element duration. RS-423 requires much slower rise times, specified from 10% to 90% of the total signal amplitude, to reduce cross talk for operation over longer distances. Therefore, the RS-423 driver in the equipment must be waveshaped. This is achieved by selection of a capacitor value for the Am26LS30 to simultaneously meet the requirements of both RS-423 and RS-232C for data rates covered by RS-232C.
3. RS-423 specifies one common return ground for each direction of transmission, RS-232C requires only one for both directions of transmission. Care must be taken to insure that a return ground path has been created when interfacing between the two systems.
4. RS-232C does not require termination, while it may be necessary for RS-422 and 423. Detailed consideration of termination is covered in the next section.

Note that RS-422 and RS-423 specifies that receivers should not be damaged by voltages up to 12V, while RS-232C allows drivers to produce output voltages up to 25V. The Am26LS32 receiver has been designed to avoid this hazard and can withstand input voltages of ±25 volts.

## RS-422 TRANSMISSION LINE FEATURES

Any time a receiver and transmitter are connected with more than a few inches of a wire, problems due to reflections can arise if care is not exercised to terminate the line correctly. RS-422 describes the cable as a twisted pair of approximately 120Ω impedance terminated in a resistor $R_T$. $R_T$ is not specified because there are two extreme values which may be chosen for the two following general classes of usage: (1) single direction transmission; and (2) multi-direction and multiple source transmission (party line). Considering the cable impedance only, the termination should equal the cable impedance of 120Ω. However this reduces the terminated cable resistance as seen by the driver to only 60Ω, with resulting loading of the output signal. This loading causes a reduction of S/N ratio at the received terminal due to the decrease in signal voltage swing. The solution lies in a compromise between an $R_T$ of 120Ω which provides maximum power transfer at a reduced S/N ratio or $R_T$ of 240Ω which causes a mis-match of 2-to-1 but no S/N reduction. The choice is left to the user as it is system dependent. Both schemes will work for an average line length and should only approach the margins at maximum line length and maximum bit rates.

Electronic Industries Association, when preparing EIA Standard RS-422 conducted their tests with 24 gauge twisted pair wire. The resulting length vs. data rate, is published as a guideline in RS-422 (Figure 9). This shows two important results: (1) Unmodulated baseband (NRZ) signalling is not recommended at distances greater than 4000 feet; (2) At data rates above about 100KHz, the maximum cable length for acceptable signal quality is inversely proportional to data rate.

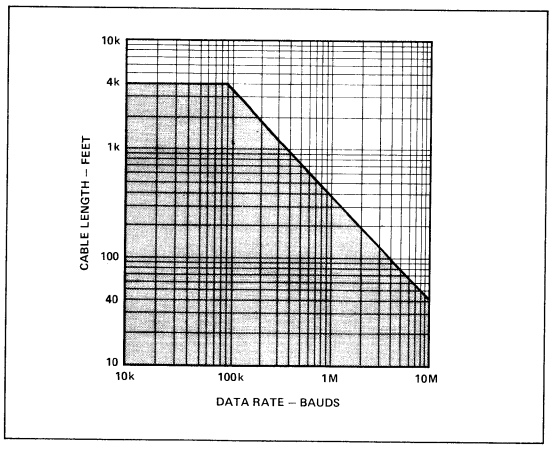



Figure 9. Data Rate Versus Cable Length for Balanced, Twisted Pair Cable (From EIA RS-422).

Result (1) above is due to the DC resistance of the cable. For a 4000 foot cable with a DC resistance of 30 ohms/1000 feet, the DC series loop resistance is 240Ω. The minimum allowable terminated differential load impedance is 90Ω. The DC voltage attentuation is 90/(90 – 240) = 1/4(6db), which is arbitrarily chosen as the maximum allowable limit.

Result (2) is due to line losses. Laboratory tests using the 26LS31 Line Driver connected to the 26LS32 Line Receiver by 800 feet of ordinary 20 AWG twisted pair (Beldon #8205 plastic-jacketed wire), terminated in its characteristic impedance of 100Ω were evaluated. The input waveform was a 500KHz square wave with (10% to 90%) rise and fall times of less than 10ns. The output waveform produced rise and fall times which together accounted for approximately one-half the period ($t_r + t_f$ = 500ns). This was due to line loss and constant capacity. The energy per cycle of the output waveform is approximately 25% lower than that of the input. The input rise and fall times are not a function of line length, assuming matching termination. The output rise and fall times are dependent upon length in a complex manner. Furthermore, it can be shown by observation that they build up along the line.

Many good reference sources are available on the subject of transmission lines (References 1, 2, 3 and 4). These will provide background information to the following discussion.

Seshadri in Reference (1) has analyzed a line with series resistance losses and has shown that rise time varies with the square of the length. This shows series resistance to be a function of the square root of frequency. However when one tries to use this result in combination with the previous result, it becomes apparent just how difficult the problem is. In Reference (2), the authors point out that skin depth implies a frequency dependent series inductance as well as resistance, and that one cannot be considered without the other.

They go on to show how this leads to the same result; namely that rise and fall times vary with the square of distance.

No attempt will be made to explain here why Figure 5 shows maximum length varying inversely with frequency rather than with the square of frequency. Certainly many complex factors are involved. Our laboratory observations showed a dependence somewhere in between linear and square law.

The Am26LS31 Quad Line Driver and the Am26LS32 Quad Line Receiver are capable of good, clean operation to the distance limits and data rate limits of RS-422.

## SYSTEM APPLICATIONS

The Am26LS30, 31, 32 and 33 can be combined in various signaling networks. Using Am26LS29, Am26LS30 and Am26LS32, Figure 10, a unidirectional RS-423 communication can be constructed. Allowing for the voltage variation described earlier, RS-232C requirements can be satisfied. It should be noted that the Am26LS29 or Am26LS30 is used above to meet the bipolar requirements. If a single-ended line, Figure 11, is required without a bipolar requirement, the Am26LS31 can be used by biasing the reference terminal of the receiver to approximately 1.5 volts. Note that additional resistors will enhance fail safe operation.

Figure 12 shows the use of the Am26LS31 and Am26LS32 to meet a balanced line, single direction RS-422 application. If bidirectionality is required, an additional termination should be added as shown in Figure 13.

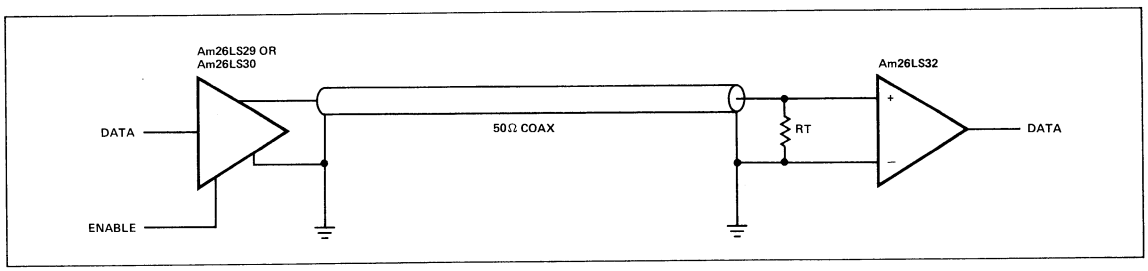



Figure 10. Unidirectional RS-423 (partial RS-232C).

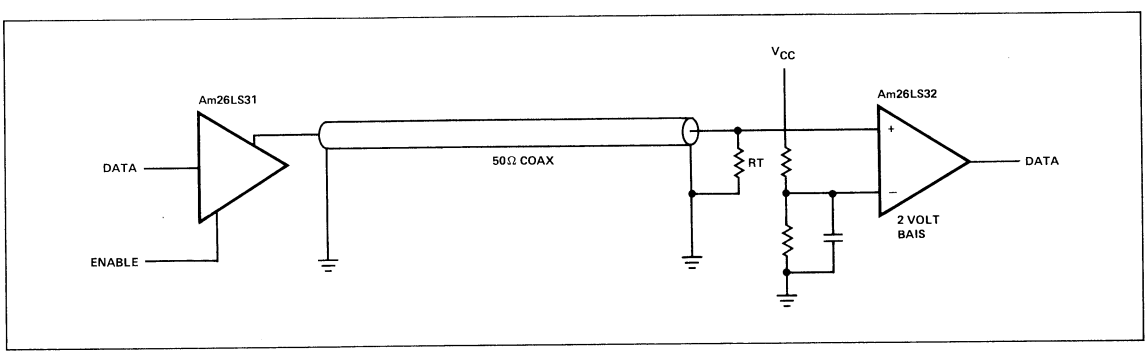



Figure 11. Single-Ended Line Without Bipolar Requirement.

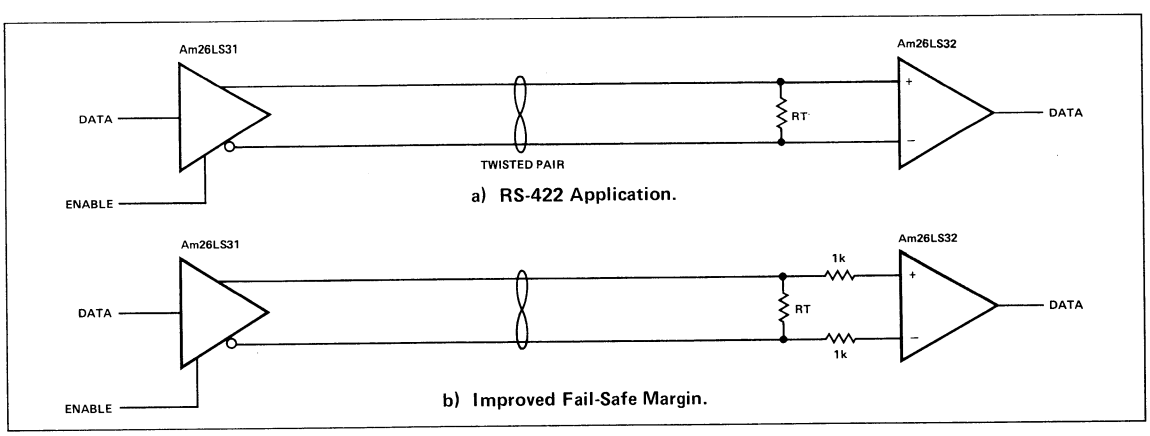



Figure 12.

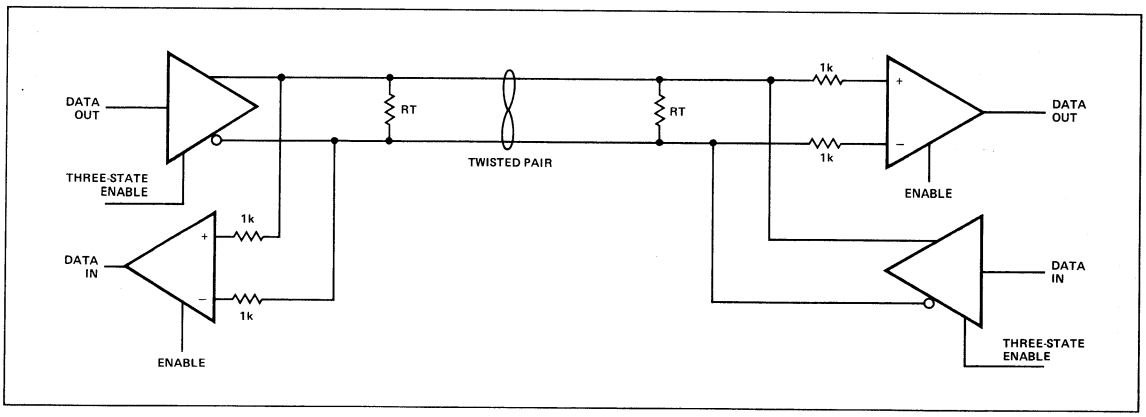



Figure 13. Bidirectional RS-422.

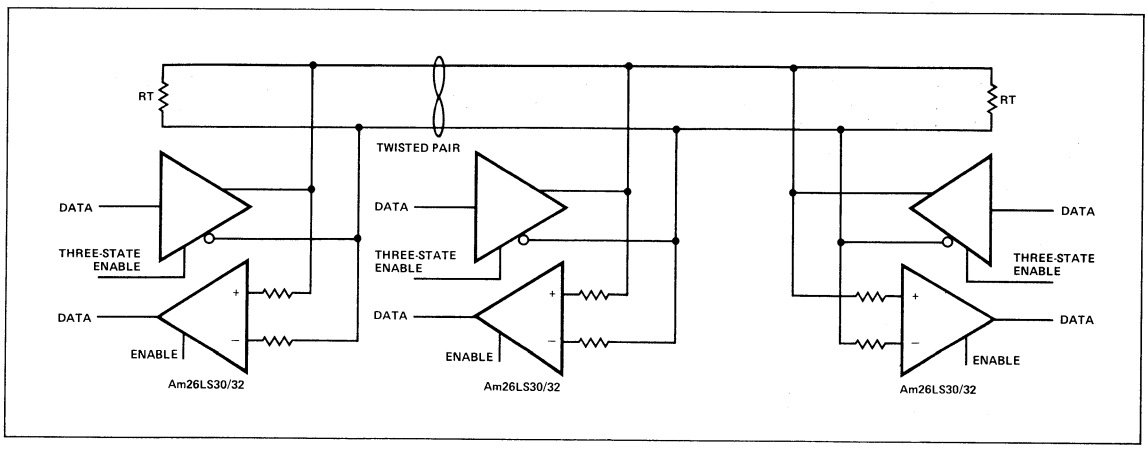



Figure 14. Party Line Configuration.

a) Full Duplex Four-Wire Data Communication RS-422 Interface (with Data Modem).

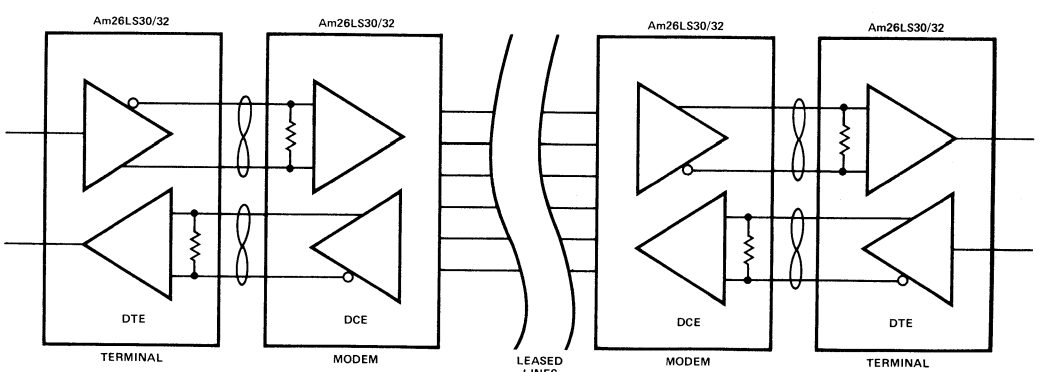



Figure 15.

b) Full Duplex Four-Wire Data Communication RS-422 Interface (without Data Modem).

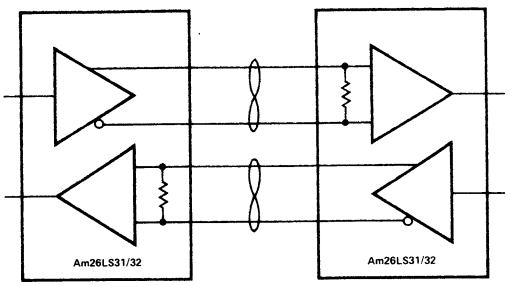



Figure 15. (Cont.)

The high speed capability of RS-422 has attracted the interest of many computer designers for use in the party line mode (Figure 14). The most common usage is that of a four wire full duplex exchange system (Figure 15). This mode of operation involves two pairs of wires each handling a single direction of traffic. The outgoing direction consists of one driver (Am26LS30 or Am26LS31) and n receivers (Am26LS32 or Am26LS33). The incoming direction consists of one receiver (Am26LS32 or Am26LS33) and n drivers (Am26LS30 or Am26LS31). This seems extremely simple to organize. However, problems arise when system ground is considered. If the network of receiver and driver span a moderate to long physical distance, ground loop noise or differences are developed changing the voltage that appears at the terminals of all receivers and drivers except for the one driver that is active. It remains the system reference as long as it is active. This induced or system developed voltage is referred to as Common Mode voltage (CMV) and as such must be considered as a device parameter. All manufacturers specify CMV capability of their receiver in compliance with RS-422 (approx. 7 volts plus signal) but there is no specification for drivers. If the dimensions of the system are short compared to 1/4 wave length of the maximum date rise and fall times, the CMV can be assumed to be minimal and drivers with single voltage supply and limited negative CMV can be used, i.e., Am26LS31. If the system dimensions are large, the CMV will cause problems in that the driver will clamp to the ground the moment the collective or apparent voltage swings below minus 0.5 volts relative to the driver ground, causing a short in the line and increasing level shift and noise. The clamping is caused in part by conduction of the I/C substrate diode. The problem can be avoided by using a driver with an output common mode range (Am26LS30). The Am26LS30 guarantees an output CMV range of ±10 volts about the driver ground reference. New international standards are under consideration to specify this mode of operation. In conclusion, a good system of 4 wire full duplex for data communication would use as an outgoing pair an Am26LS30 line driver and up to 12 – Am26LS32 line receivers, with a termination at the near and far ends of the cable. The same system would use as an incoming pair an Am26LS32 line receiver and up to 32 – Am26LS30 line drivers with only one enabled at a time and all others in three-state mode with cable termination at both near and far ends of the cable.

Many other applications are possible using this family of devices. Although the designs are based on the requirements of the EIA data communications specifications, they are not limited to these situations. Aircraft buses and internal equipment interconnections will benefit from the features offered by these products.



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# Am2905

## Quad Two-Input OC Bus Transceiver With Three-State Receiver

### Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

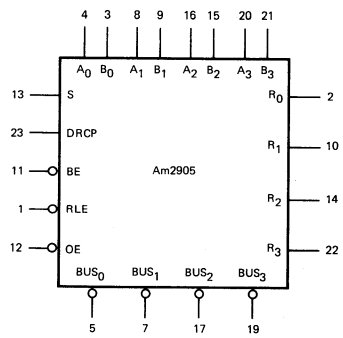
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the $A_i$ data is stored in the register and when S is HIGH, the $B_i$ data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

### ORDERING INFORMATION

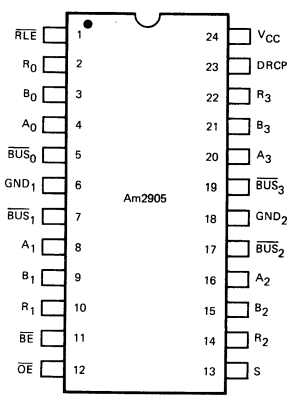
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2905PC |
| Hermetic DIP | 0°C to +70°C | AM2905DC |
| Dice | 0°C to +70°C | AM2905XC |
| Hermetic DIP | −55°C to +125°C | AM2905DM |
| Hermetic Flat Pak | −55°C to +125°C | AM2905FM |
| Dice | −55°C to +125°C | AM2905XM |

### LOGIC SYMBOL



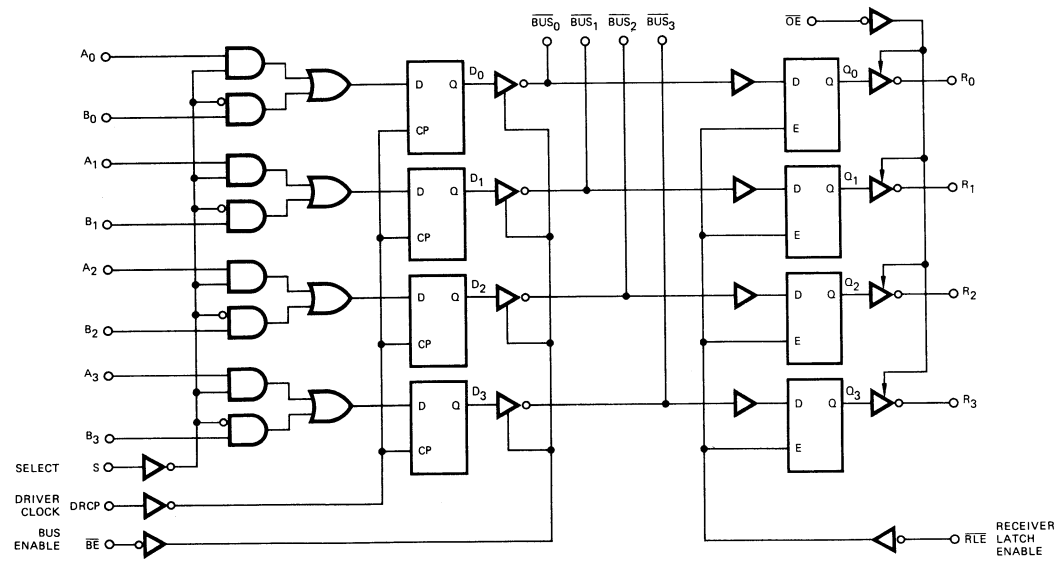

$V_{CC}$ = Pin 24
$GND_1$ = Pin 6
$GND_2$ = Pin 18

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

## LOGIC DIAGRAM




MPR-065

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7V |
| DC Output Current, Into Outputs (Except Bus) | 30mA |
| DC Output Current, Into Bus | 200mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A$ = 0°C to +70°C $V_{CC}$MIN. = 4.75V $V_{CC}$MAX. = 5.25V
Am2905XM (MIL) $T_A$ = −55°C to +125°C $V_{CC}$MIN. = 4.50V $V_{CC}$MAX. = 5.50V

## BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | $V_{CC}$ = MIN. | $I_{OL}$ = 40mA | | | 0.32 | 0.5 | Volts |
| | | | $I_{OL}$ = 70mA | | | 0.41 | 0.7 | |
| | | | $I_{OL}$ = 100mA | | | 0.55 | 0.8 | |
| $I_O$ | Bus Leakage Current | $V_{CC}$ = MAX. | $V_O$ = 0.4V | | | | −50 | µA |
| | | | $V_O$ = 4.5V | MIL | | | 200 | |
| | | | | COM'L | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power OFF) | $V_O$ = 4.5V | | | | | 100 | µA |
| $V_{TH}$ | Receiver Input HIGH Threshold | Bus enable = 2.4V | | MIL | 2.4 | 2.0 | | Volts |
| | | | | COM'L | 2.3 | 2.0 | | |
| $V_{TL}$ | Receiver Input LOW Threshold | Bus enable = 2.4V | | MIL | | 2.0 | 1.5 | Volts |
| | | | | COM'L | | 2.0 | 1.6 | |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$ MIN. = 4.75 V $V_{CC}$ MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$ MIN. = 4.50 V $V_{CC}$ MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

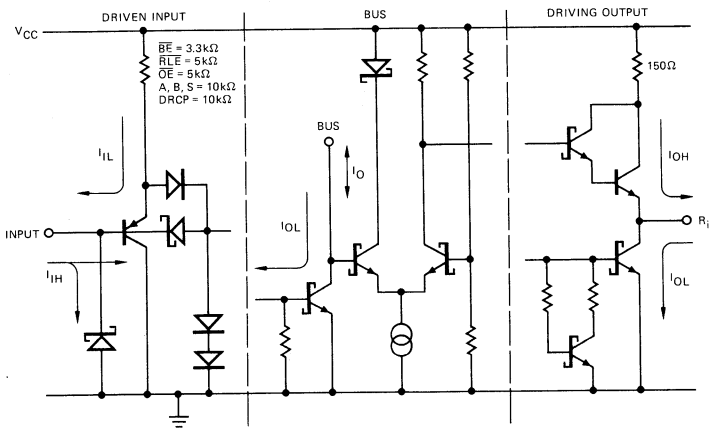
| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or $V_{IH}$ | MIL, $I_{OH} = -1.0$mA | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6$mA | 2.4 | 3.4 | | |
| $V_{OL}$ | Receiver Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | $I_{OL}$ = 4mA | | 0.27 | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | 0.32 | 0.45 | |
| | | | $I_{OL}$ = 12mA | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN} = -18$mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 0.4$V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 2.7$V | | | | 20 | µA |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 5.5$V | | | | 100 | µA |
| $I_O$ | Receiver Off-State Output Current | $V_{CC}$ = MAX. | $V_O = 2.4$V | | | 20 | µA |
| | | | $V_O = 0.4$V | | | −20 | |
| $I_{SC}$ | Receiver Output Short Circuit Current | $V_{CC}$ = MAX. | | −12 | | −65 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., All inputs = GND | | | 69 | 105 | mA |

## SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am2905XM Min. | Am2905XM Typ. (Note 2) | Am2905XM Max. | Am2905XC Min. | Am2905XC Typ. (Note 2) | Am2905XC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50pF, $R_L$ (BUS) = 50Ω | | 21 | 40 | | 21 | 36 | ns |
| $t_{PLH}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PHL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 26 | | 13 | 23 | ns |
| $t_{PLH}$ | | | | 13 | 26 | | 13 | 23 | |
| $t_s$ | Data Inputs (A or B) | $C_L$ = 15pF, $R_L$ = 2.0kΩ | 25 | | | 23 | | | ns |
| $t_h$ | | | 8.0 | | | 7.0 | | | |
| $t_s$ | Select Input (S) | | 33 | | | 30 | | | ns |
| $t_h$ | | | 8.0 | | | 7.0 | | | |
| $t_{PW}$ | Driver Clock (DRCP) Pulse Width (HIGH) | | 28 | | | 25 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enable) | | | 18 | 37 | | 18 | 34 | ns |
| $t_{PHL}$ | | | | 18 | 37 | | 18 | 34 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 37 | | 21 | 34 | ns |
| $t_{PHL}$ | | | | 21 | 37 | | 21 | 34 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 21 | | | 18 | | | ns |
| $t_h$ | | | 7.0 | | | 5.0 | | | |
| $t_{ZH}$ | Output Control to Receiver Output | | | 14 | 28 | | 14 | 25 | ns |
| $t_{ZL}$ | | | | 14 | 28 | | 14 | 25 | |
| $t_{HZ}$ | Output Control to Receiver Output | | | 14 | 28 | | 14 | 25 | ns |
| $t_{LZ}$ | | | | 14 | 28 | | 14 | 25 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

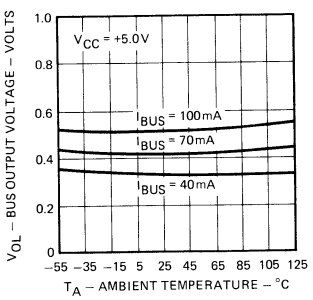
## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



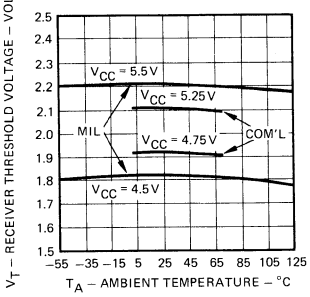

Note: Actual current flow direction shown.

## TYPICAL PERFORMANCE CURVES

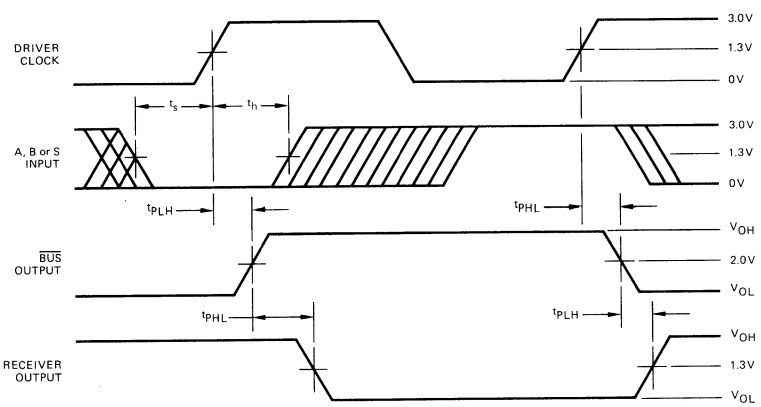
### Bus Output Low Voltage Versus Ambient Temperature




### Receiver Threshold Variation Versus Ambient Temperature




## SWITCHING WAVEFORMS




Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

## FUNCTION TABLE

| INPUTS | | | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | $A_i$ | $B_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $\overline{BUS}_i$ | $R_i$ | |
| X | X | X | X | H | X | X | X | X | Z | X | Driver output disable |
| X | X | X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X | X | X | X | H | L | L | X | L | L | H | Driver output disable and receive data via Bus input |
| X | X | X | X | H | L | L | X | H | H | L | |
| X | X | X | X | X | H | X | X | NC | X | X | Latch received data |
| L | L | X | ↑ | X | X | X | L | X | X | X | Load driver register |
| L | H | X | ↑ | X | X | X | H | X | X | X | |
| H | X | L | ↑ | X | X | X | L | X | X | X | |
| H | X | H | ↑ | X | X | X | H | X | X | X | |
| X | X | X | L | X | X | X | NC | X | X | X | No driver clock restrictions |
| X | X | X | H | X | X | X | NC | X | X | X | |
| X | X | X | X | L | X | X | L | X | H | X | Drive Bus |
| X | X | X | X | L | X | X | H | X | L | X | |

H = HIGH, L = LOW; Z = HIGH Impedance, NC = No change; X = Don't care, ↑ = LOW-to-HIGH transition; i = 0, 1, 2, 3

## DEFINITION OF FUNCTIONAL TERMS

**$A_0$, $A_1$, $A_2$, $A_3$** — The "A" word data input into the two input multiplexer of the driver register.

**$B_0$, $B_1$, $B_2$, $B_3$** — The "B" word data input into the two input multiplexers of the driver register.

**S** — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

**DRCP** — Driver Clock Pulse. Clock pulse for the driver register.

**$\overline{BE}$** — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

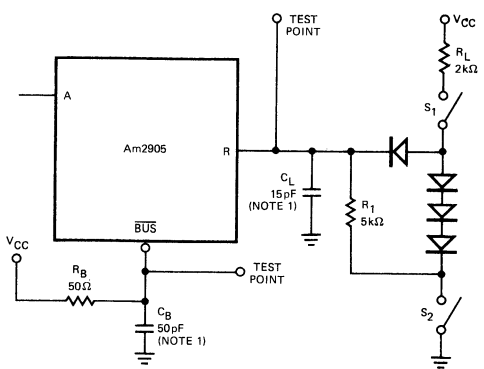
**$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$** — The four driver outputs and receiver inputs (data is inverted).

**$R_0$, $R_1$, $R_2$, $R_3$** — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

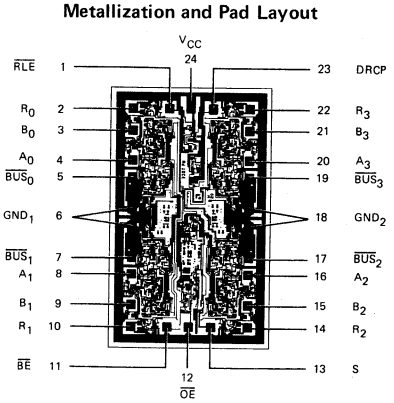
**$\overline{RLE}$** — Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

**$\overline{OE}$** — Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

### LOAD TEST CIRCUIT

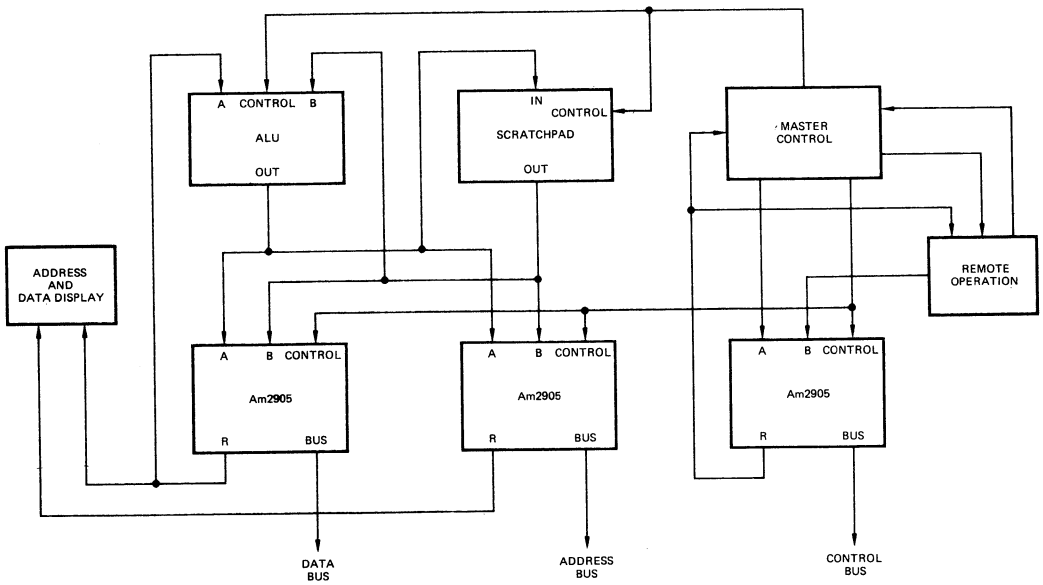



### Metallization and Pad Layout

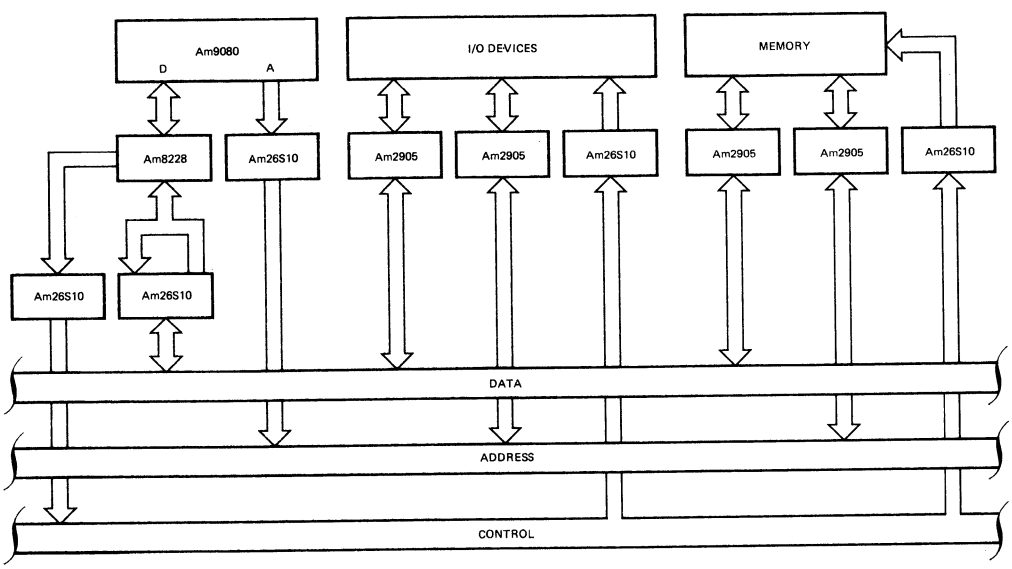



DIE SIZE 0.080" X 0.130"

## APPLICATIONS




The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.




Using the Am2905 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

# Am2906

## Quad Two-Input OC Bus Transceiver With Parity

### Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

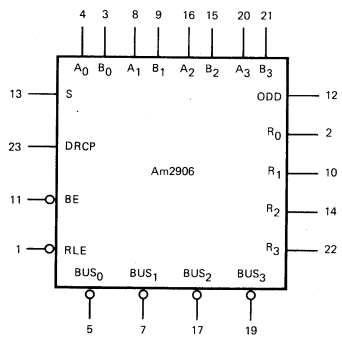
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the $A_i$ data is stored in the register and when S is HIGH, the $B_i$ data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

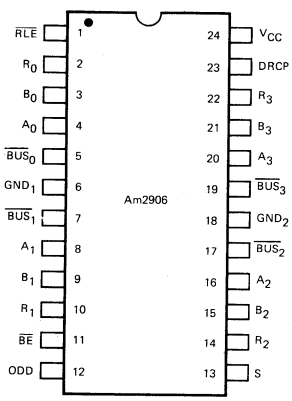
The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

### LOGIC SYMBOL




$V_{CC}$ = Pin 24
$GND_1$ = Pin 6
$GND_2$ = Pin 18

### CONNECTION DIAGRAM
Top View

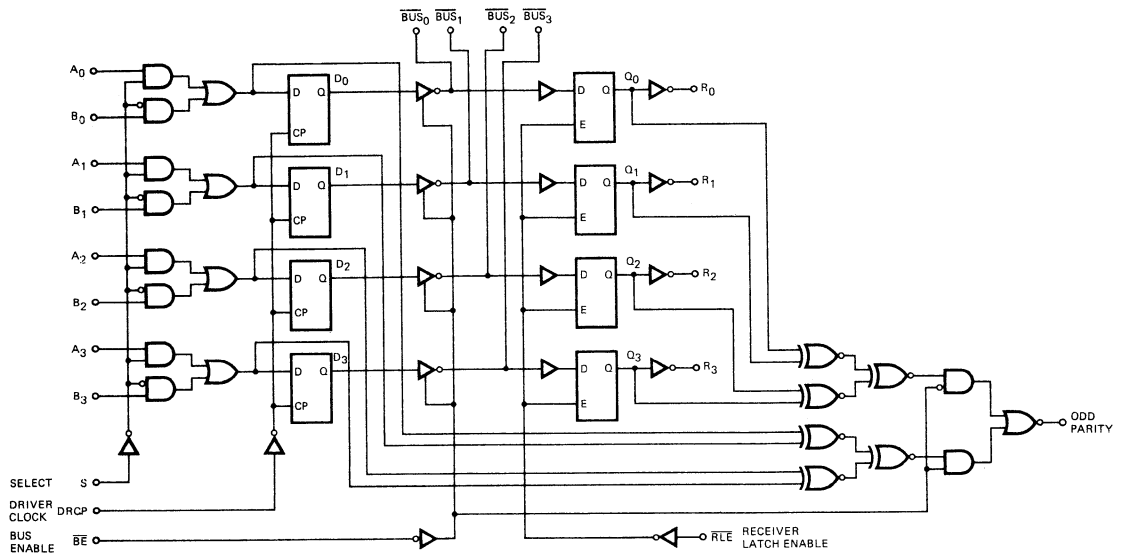



Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2906PC |
| Hermetic DIP | 0°C to +70°C | AM2906DC |
| Dice | 0°C to +70°C | AM2906XC |
| Hermetic DIP | −55°C to +125°C | AM2906DM |
| Hermetic Flat Pak | −55°C to +125°C | AM2906FM |
| Dice | −55°C to +125°C | AM2906XM |

## LOGIC DIAGRAM




## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs (Except Bus) | 30mA |
| DC Output Current, Into Bus | 200mA |
| DC Input Current | −30mA to +5.0mA |

3

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

| | | | |
|---|---|---|---|
| Am2906XC (COM'L) | $T_A$ = 0°C to +70°C | $V_{CC}$ MIN. = 4.75V | $V_{CC}$ MAX. = 5.25V |
| Am2906XM (MIL) | $T_A$ = −55°C to +125°C | $V_{CC}$ MIN. = 4.50V | $V_{CC}$ MAX. = 5.50V |

## BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | | $I_{OL}$ = 40mA | | | 0.32 | 0.5 | Volts |
| | | | $I_{OL}$ = 70mA | | | 0.41 | 0.7 | |
| | | | $I_{OL}$ = 100mA | | | 0.55 | 0.8 | |
| $I_O$ | Bus Leakage Current | $V_{CC}$ = MAX. | $V_O$ = 0.4V | | | | −50 | µA |
| | | | $V_O$ = 4.5V | MIL | | | 200 | |
| | | | | COM'L | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power OFF) | $V_O$ = 4.5V | | | | | 100 | µA |
| $V_{TH}$ | Receiver Input HIGH Threshold | Bus enable = 2.4V | | MIL | 2.4 | 2.0 | | Volts |
| | | | | COM'L | 2.3 | 2.0 | | |
| $V_{TL}$ | Receiver Input LOW Threshold | Bus enable = 2.4V | | MIL | | 2.0 | 1.5 | Volts |
| | | | | COM'L | | 2.0 | 1.6 | |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

| | | | |
|---|---|---|---|
| Am2906XC (COM'L) | $T_A = 0°C$ to $+70°C$ | $V_{CC}$ MIN. = 4.75V | $V_{CC}$ MAX. = 5.25V |
| Am2906XM (MIL) | $T_A = -55°C$ to $+125°C$ | $V_{CC}$ MIN. 4.5V | $V_{CC}$ MAX. = 5.5V |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

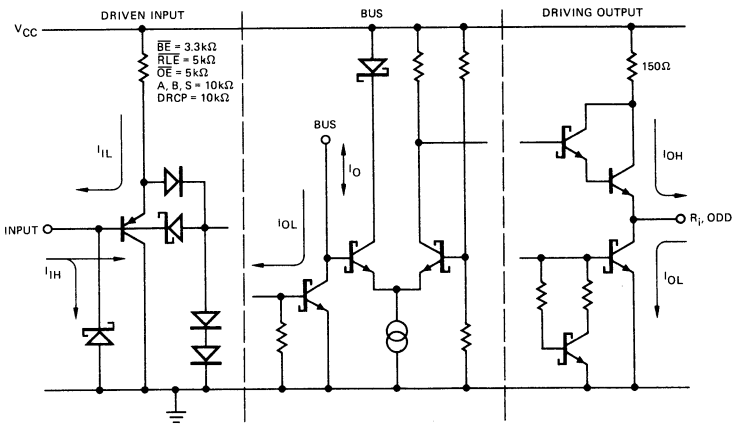
| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | MIL | $I_{OH} = -1mA$ | 2.4 | 3.4 | | Volts |
| | | | COM'L | $I_{OH} = -2.6mA$ | 2.4 | 3.4 | | |
| | Parity Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or $V_{IL}$ | | MIL | 2.5 | 3.4 | | |
| | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Except Bus) | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | | $I_{OL} = 4mA$ | | 0.27 | 0.4 | Volts |
| | | | | $I_{OL} = 8mA$ | | 0.32 | 0.45 | |
| | | | | $I_{OL} = 12mA$ | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 5.5V$ | | | | | 100 | μA |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX. | | | −12 | | −65 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., All inputs = GND | | | | 72 | 105 | mA |

## SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am2906XM Min. | Am2906XM Typ. (Note 2) | Am2906XM Max. | Am2906XC Min. | Am2906XC Typ. (Note 2) | Am2906XC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50pF, $R_L$ (BUS) = 50Ω | | 21 | 40 | | 21 | 36 | ns |
| $t_{PLH}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PHL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 26 | | 13 | 23 | ns |
| $t_{PLH}$ | | | | 13 | 26 | | 13 | 23 | |
| $t_s$ | Data Inputs (A or B) | $C_L$ = 15pF, $R_L$ = 2.0kΩ | 25 | | | 23 | | | ns |
| $t_h$ | | | 8.0 | | | 7.0 | | | |
| $t_s$ | Select Inputs (S) | | 33 | | | 30 | | | ns |
| $t_h$ | | | 8.0 | | | 7.0 | | | |
| $t_{PW}$ | Clock Pulse Width (HIGH) | | 28 | | | 25 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enabled) | | | 18 | 37 | | 18 | 34 | ns |
| $t_{PHL}$ | | | | 18 | 37 | | 18 | 34 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 37 | | 21 | 34 | ns |
| $t_{PHL}$ | | | | 21 | 37 | | 21 | 34 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 21 | | | 18 | | | ns |
| $t_h$ | | | 7.0 | | | 5.0 | | | |
| $t_{PLH}$ | A or B Data to Odd Parity Output (Driver Enabled) | | | 21 | 40 | | 21 | 36 | ns |
| $t_{PHL}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PLH}$ | Bus to Odd Parity Output (Driver Inhibited, Latch Enabled) | | | 21 | 40 | | 21 | 36 | ns |
| $t_{PHL}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PLH}$ | Latch Enable ($\overline{RLE}$) to Odd Parity Output | | | 21 | 40 | | 21 | 36 | ns |
| $t_{PHL}$ | | | | 21 | 40 | | 21 | 36 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

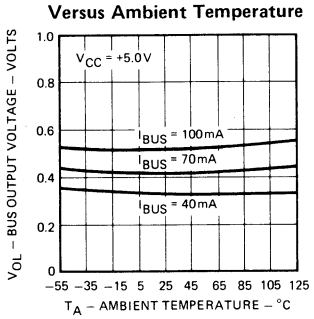
## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



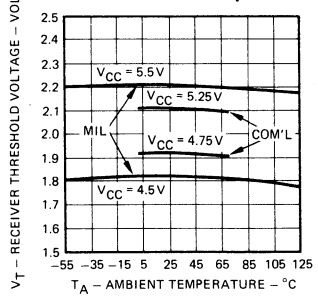

Note: Actual current flow direction shown.

## TYPICAL PERFORMANCE CURVES

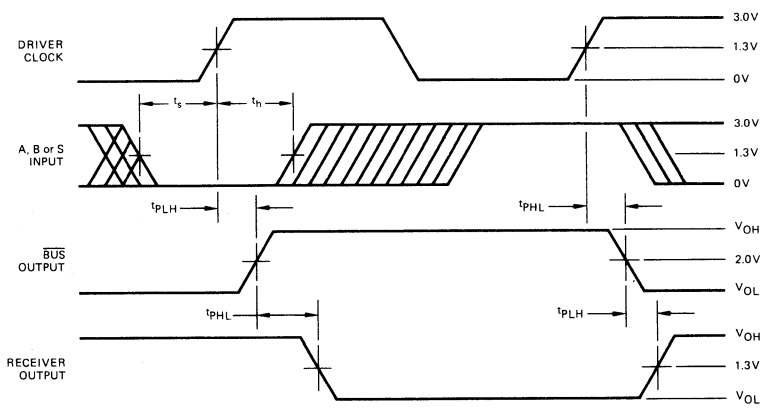
### Bus Output Low Voltage Versus Ambient Temperature




### Receiver Threshold Variation Versus Ambient Temperature




## SWITCHING WAVEFORMS




Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

## FUNCTION TABLE

| INPUTS | | | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | $A_i$ | $B_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $\overline{BUS}_i$ | $R_i$ | |
| X | X | X | X | H | X | X | X | X | Z | X | Driver output disable |
| X | X | X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X | X | X | X | H | L | L | X | L | L | H | Driver output disable and receive data via Bus input |
| X | X | X | X | H | L | L | X | H | H | L | |
| X | X | X | X | X | H | X | X | NC | X | X | Latch received data |
| L | L | X | ↑ | X | X | X | L | X | X | X | Load driver register |
| L | H | X | ↑ | X | X | X | H | X | X | X | |
| H | X | L | ↑ | X | X | X | L | X | X | X | |
| H | X | H | ↑ | X | X | X | H | X | X | X | |
| X | X | X | L | X | X | X | NC | X | X | X | No driver clock restrictions |
| X | X | X | H | X | X | X | NC | X | X | X | |
| X | X | X | X | L | X | X | L | X | H | X | Drive Bus |
| X | X | X | X | L | X | X | H | X | L | X | |

H = HIGH, L = LOW; Z = HIGH Impedance, NC = No change; X = Don't care, ↑ = LOW-to-HIGH transition; i = 0, 1, 2, 3

## DEFINITION OF FUNCTIONAL TERMS

**$A_0$, $A_1$, $A_2$, $A_3$** — The "A" word data input into the two input multiplexer of the driver register.

**$B_0$, $B_1$, $B_2$, $B_3$** — The "B" word data input into the two input multiplexers of the driver register.

**S** — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

**DRCP** — Driver Clock Pulse. Clock pulse for the driver register.

**$\overline{BE}$** — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

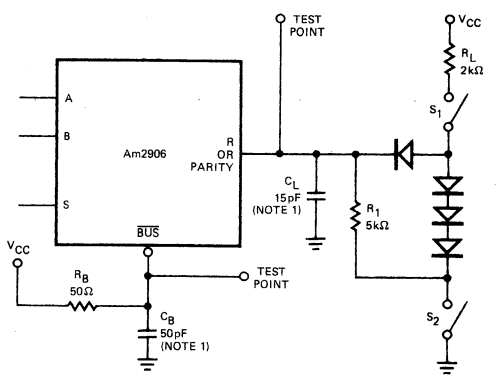
**$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$** — The four driver outputs and receiver inputs (data is inverted).

**$R_0$, $R_1$, $R_2$, $R_3$** — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

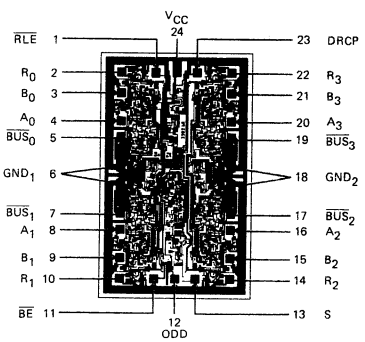
**$\overline{RLE}$** — Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

**$\overline{OE}$** — Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

### LOAD TEST CIRCUIT

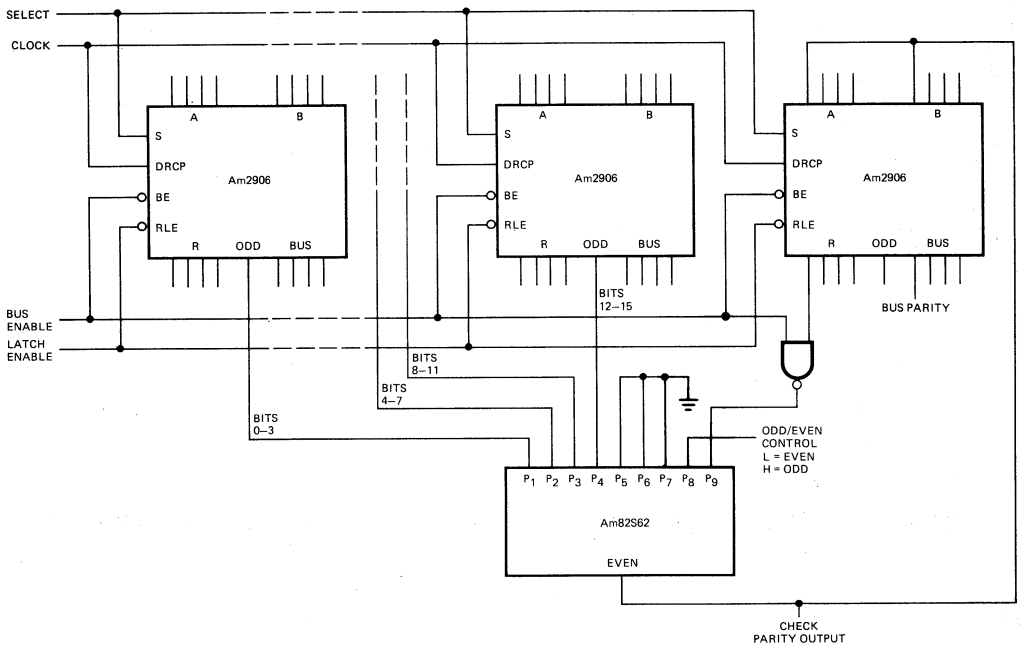



### Metallization and Pad Layout

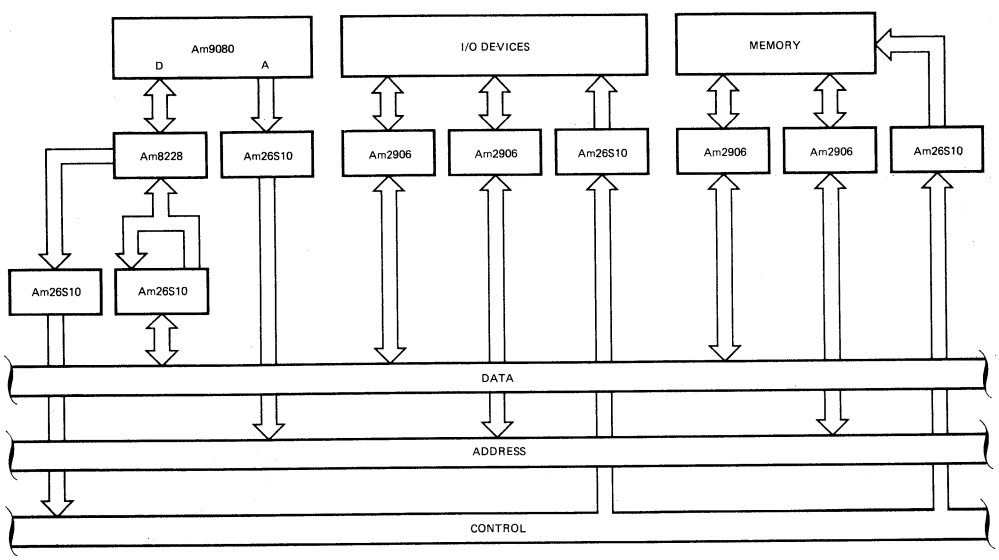



DIE SIZE 0.080" X 0.130"

## APPLICATIONS




Generating or checking parity for 16 data bits.




Using the Am2906 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

# Am2907

## Quad Bus Transceiver With Three-State Receiver And Parity

### Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

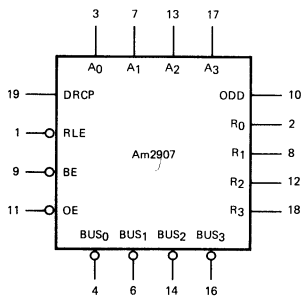
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the $A_i$ data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

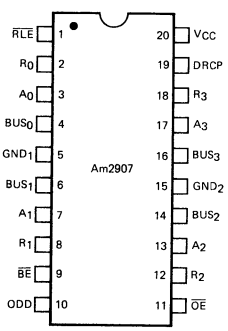
### LOGIC SYMBOL




$V_{CC}$ = Pin 20
$GND_1$ = Pin 5
$GND_2$ = Pin 15

### CONNECTION DIAGRAMS
**Top Views**

**DIP**



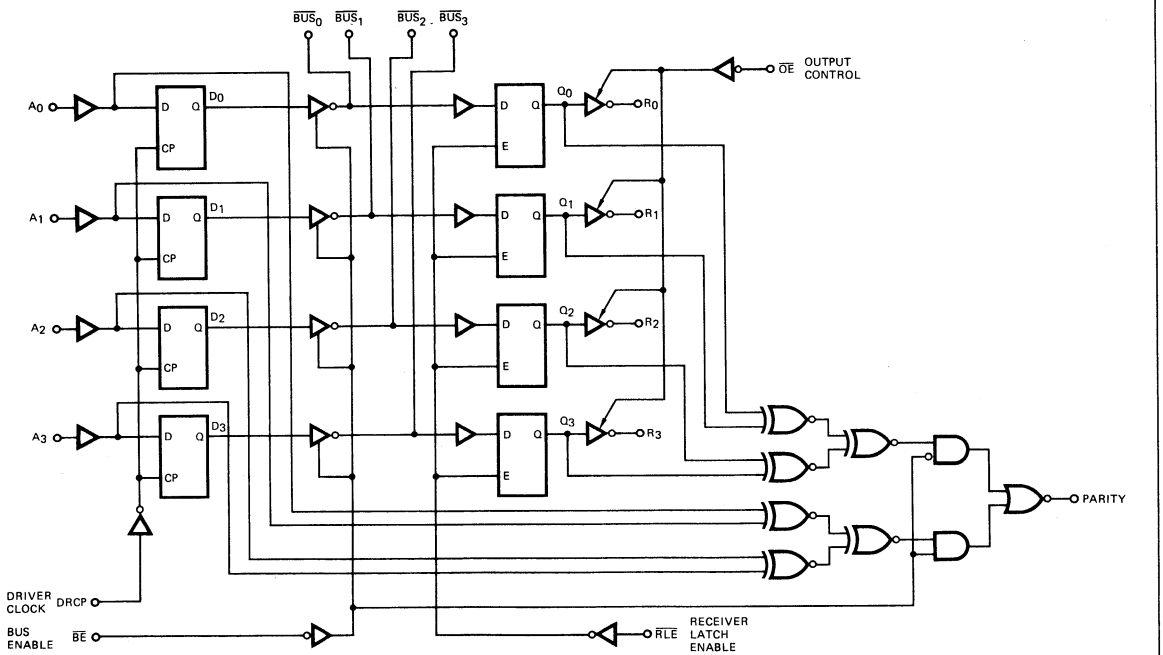

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2907PC |
| Hermetic DIP | 0°C to +70°C | AM2907DC |
| Dice | 0°C to +70°C | AM2907XC |
| Hermetic DIP | -55°C to +125°C | AM2907DM |
| *Hermetic Flat Pak | -55°C to +125°C | AM2907FM |
| Dice | -55°C to +125°C | AM2907XM |

*Available on special order

## LOGIC DIAGRAM




3

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs (Except BUS) | 30 mA |
| DC Output Current, Into Bus | 200 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

| | | | |
|---|---|---|---|
| Am2907XC (COM'L) | $T_A$ = 0°C to +70°C | $V_{CC}$ MIN. = 4.75V | $V_{CC}$ MAX. = 5.25V |
| Am2907XM (MIL) | $T_A$ = −55°C to +125°C | $V_{CC}$ MIN. = 4.50V | $V_{CC}$ MAX. = 5.50V |

## BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | $V_{CC}$ = MIN. | $I_{OL}$ = 40mA | | | 0.32 | 0.5 | Volts |
| | | | $I_{OL}$ = 70mA | | | 0.41 | 0.7 | |
| | | | $I_{OL}$ = 100mA | | | 0.55 | 0.8 | |
| $I_O$ | Bus Leakage Current | $V_{CC}$ = MAX. | $V_O$ = 0.4V | | | | −50 | μA |
| | | | $V_O$ = 4.5V | MIL | | | 200 | |
| | | | | COM'L | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power Off) | $V_O$ = 4.5V | | | | | 100 | μA |
| $V_{TH}$ | Receiver Input HIGH Threshold | Bus Enable = 2.4V | | MIL | 2.4 | 2.0 | | Volts |
| | | | | COM'L | 2.3 | 2.0 | | |
| $V_{TL}$ | Receiver Input LOW Threshold | Bus Enable = 2.4V | | MIL | | 2.0 | 1.5 | Volts |
| | | | | COM'L | | 2.0 | 1.6 | |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$ MIN. = 4.75V $V_{CC}$ MAX. = 5.25V
Am2907XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$ MIN. = 4.50V $V_{CC}$ MAX. = 5.50V

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

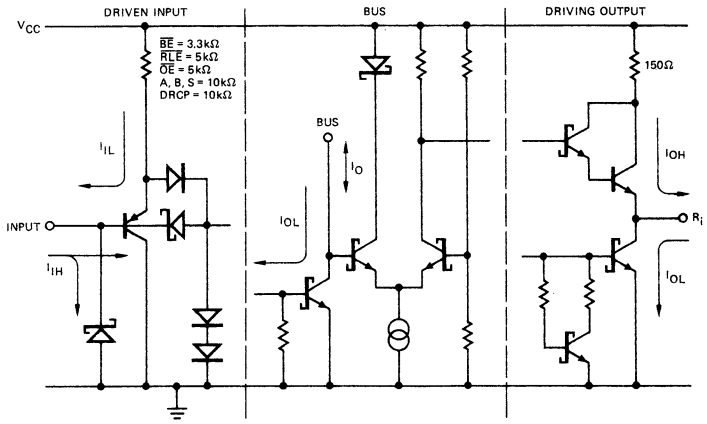
| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN. $V_{IN} = V_{IL}$ or $V_{IH}$ | MIL: $I_{OH} = -1mA$ | | 2.4 | 3.4 | | Volts |
| | | | COM'L: $I_{OH} = -2.6mA$ | | 2.4 | 3.4 | | |
| $V_{OH}$ | Parity Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -660\mu A$ $V_{IN} = V_{IH}$ or $V_{IL}$ | | MIL | 2.5 | 3.4 | | Volts |
| | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Except Bus) | $V_{CC}$ = MIN. $V_{IN} = V_{IL}$ or $V_{IH}$ | $I_{OL} = 4mA$ | | | 0.27 | 0.4 | Volts |
| | | | $I_{OL} = 8mA$ | | | 0.32 | 0.45 | |
| | | | $I_{OL} = 12mA$ | | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 0.4$ V | | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 2.7$ V | | | | | 20 | μA |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 5.5$ V | | | | | 100 | μA |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX. | | | −12 | | −65 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., All Inputs = GND | | | | 75 | 110 | mA |
| $I_O$ | Off-State Output Current (Receiver Outputs) | $V_{CC}$ = MAX. | $V_O = 2.4$ V | | | | 20 | μA |
| | | | $V_O = 0.4$ V | | | | −20 | |

## SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am2907XM Min. | Am2907XM Typ. (Note 2) | Am2907XM Max. | Am2907XC Min. | Am2907XC Typ. (Note 2) | Am2907XC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50pF $R_L$ (BUS) = 50Ω | | 21 | 40 | | 21 | 36 | ns |
| $t_{PLH}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PHL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 26 | | 13 | 23 | ns |
| $t_{PLH}$ | | | | 13 | 26 | | 13 | 23 | |
| $t_s$ | A Data Inputs | $C_L = 15$pF $R_L = 2.0$kΩ | 25 | | | 23 | | | ns |
| $t_h$ | | | 8.0 | | | 7.0 | | | |
| $t_{PW}$ | Clock Pulse Width (HIGH) | | 28 | | | 25 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enabled) | | | 18 | 37 | | 18 | 34 | ns |
| $t_{PHL}$ | | | | 18 | 37 | | 18 | 34 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 37 | | 21 | 34 | ns |
| $t_{PHL}$ | | | | 21 | 37 | | 21 | 34 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 21 | | | 18 | | | ns |
| $t_h$ | | | 7.0 | | | 5.0 | | | |
| $t_{PLH}$ | A Data to Odd Parity Out (Driver Enabled) | | | 21 | 40 | | 21 | 36 | ns |
| $t_{PHL}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PLH}$ | Bus to Odd Parity Out (Driver Inhibit) | | | 21 | 40 | | 21 | 36 | ns |
| $t_{PHL}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{PLH}$ | Latch Enable ($\overline{RLE}$) to Odd Parity Output | | | 21 | 40 | | 21 | 36 | ns |
| $t_{PHL}$ | | | | 21 | 40 | | 21 | 36 | |
| $t_{ZH}$ | Output Control to Output | | | 14 | 28 | | 14 | 25 | ns |
| $t_{ZL}$ | | | | 14 | 28 | | 14 | 25 | |
| $t_{HZ}$ | Output Control to Output | $C_L = 5.0$pF $R_L = 2.0$kΩ | | 14 | 28 | | 14 | 25 | ns |
| $t_{LZ}$ | | | | 14 | 28 | | 14 | 25 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

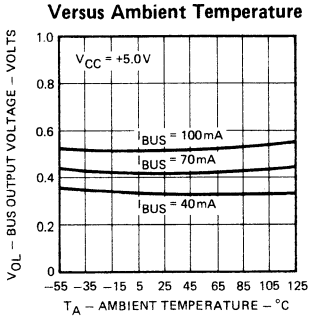
## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



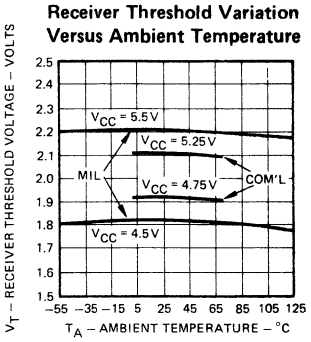

Note: Actual current flow direction shown.

## TYPICAL PERFORMANCE CURVES

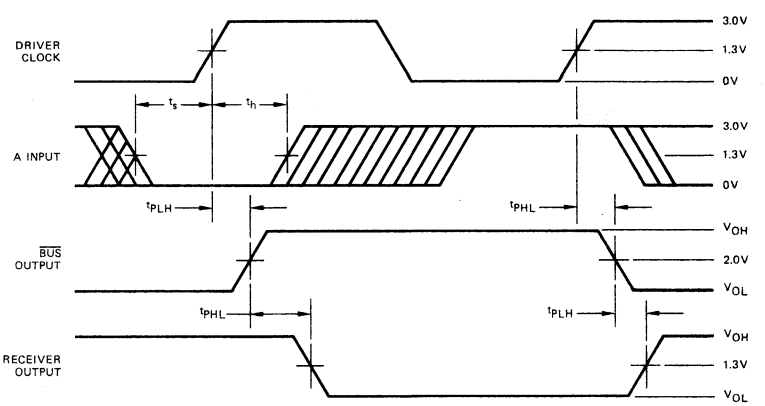
### Bus Output Low Voltage Versus Ambient Temperature




### Receiver Threshold Variation Versus Ambient Temperature




## SWITCHING WAVEFORMS




Note: Bus to Reciever output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

## TRUTH TABLE

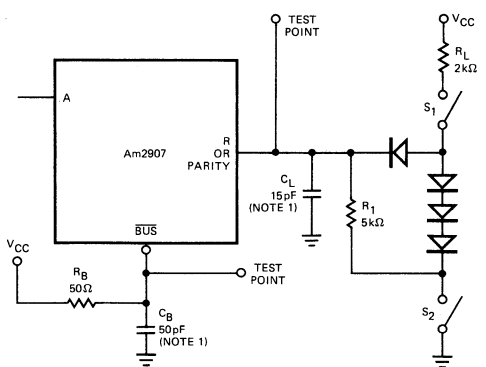
| INPUTS | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| $A_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $B_i$ | $R_i$ | |
| X | X | H | X | X | X | X | H | X | Driver output disable |
| X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X | X | H | L | L | X | L | L | H | Driver output disable and receive data via Bus input |
| X | X | H | L | L | X | H | H | L | |
| X | X | X | H | X | X | NC | X | X | Latch received data |
| L | ↑ | X | X | X | L | X | X | X | Load driver register |
| H | ↑ | X | X | X | H | X | X | X | |
| X | L | X | X | X | NC | X | X | X | No driver clock restrictions |
| X | H | X | X | X | NC | X | X | X | |
| X | X | L | X | X | L | X | H | X | Drive Bus |
| X | X | L | X | X | H | X | L | X | |

H = HIGH  Z = High Impedance  X = Don't Care  i = 0, 1, 2, 3
L = LOW  NC = No Change  ↑ = LOW-to-HIGH Transition

## PARITY OUTPUT FUNCTION TABLE

| $\overline{BE}$ | ODD PARITY OUTPUT |
|---|---|
| L | ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$ |
| H | ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$ |

## LOAD TEST CIRCUIT




## DEFINITION OF FUNCTIONAL TERMS

**DRCP** Driver Clock Pulse. Clock pulse for the driver register.

**$\overline{BE}$** Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

**$BUS_0$, $BUS_1$, $BUS_2$, $BUS_3$** The four driver outputs and receiver inputs (data is inverted).

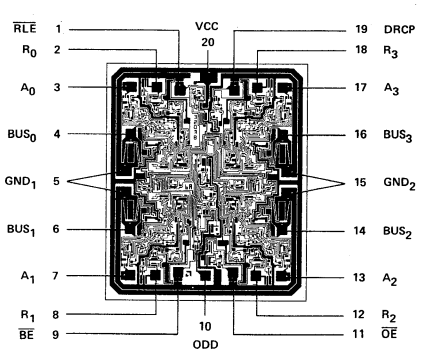
**$R_0$, $R_1$, $R_2$, $R_3$** The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

**$\overline{RLE}$** Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

**ODD** Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

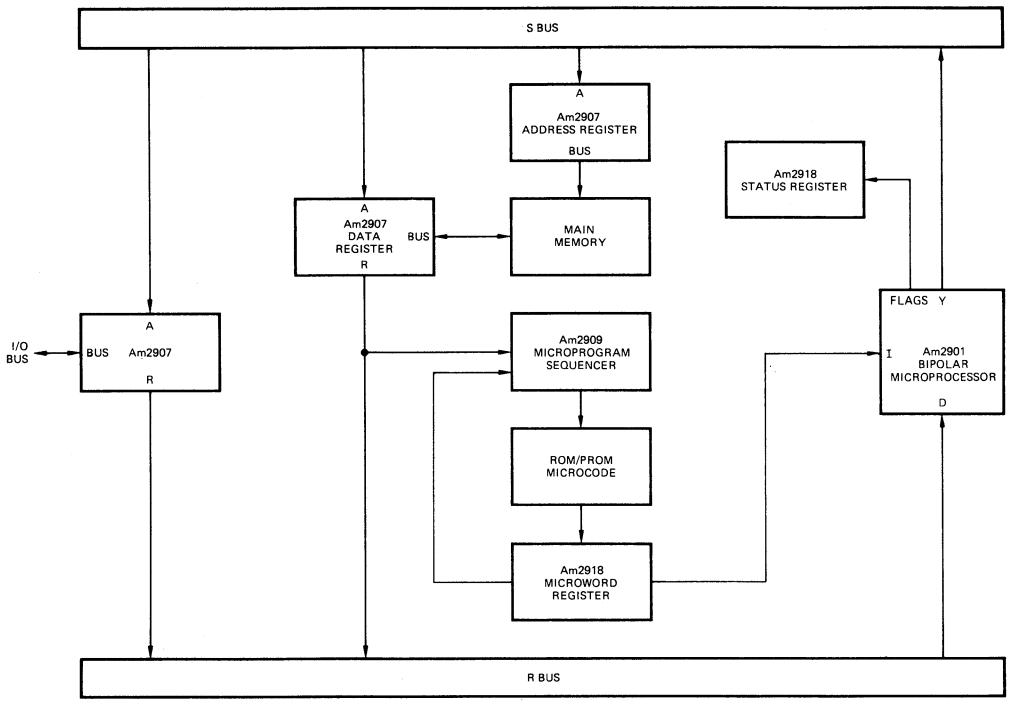
**$\overline{OE}$** Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

### Metallization and Pad Layout

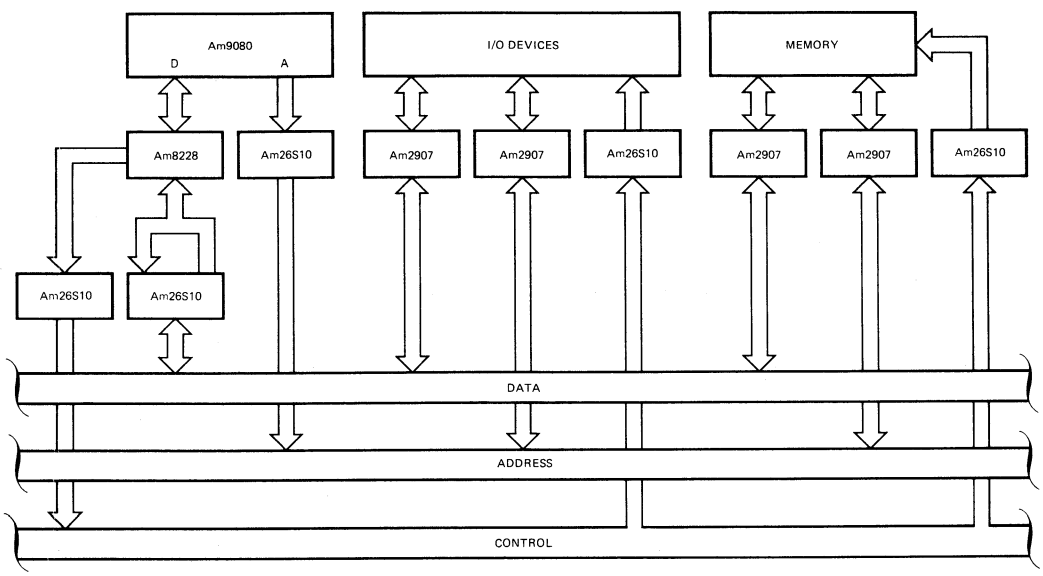



DIE SIZE 0.088" X 0.103"

## APPLICATIONS




The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.




Using the Am2907 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

# Am2915A

## Quad Three-State Bus Transceiver With Interface Logic

### Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

### FUNCTIONAL DESCRIPTION

The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input (BE) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The $V_{OH}$ and $V_{OL}$ of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

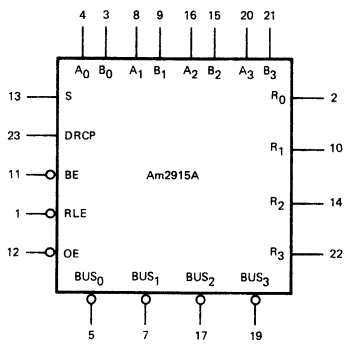
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the $A_i$ data is stored in the register and when S is HIGH, the $B_i$ data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

### ORDERING INFORMATION

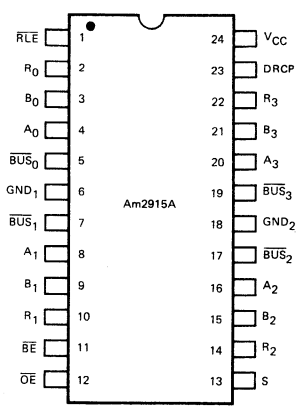
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2915APC |
| Hermetic DIP | 0°C to +70°C | AM2915ADC |
| Dice | 0°C to +70°C | AM2915AXC |
| Hermetic DIP | −55°C to +125°C | AM2915ADM |
| Hermetic Flat Pak | −55°C to +125°C | AM2915AFM |
| Dice | −55°C to +125°C | AM2915AXM |

### LOGIC SYMBOL



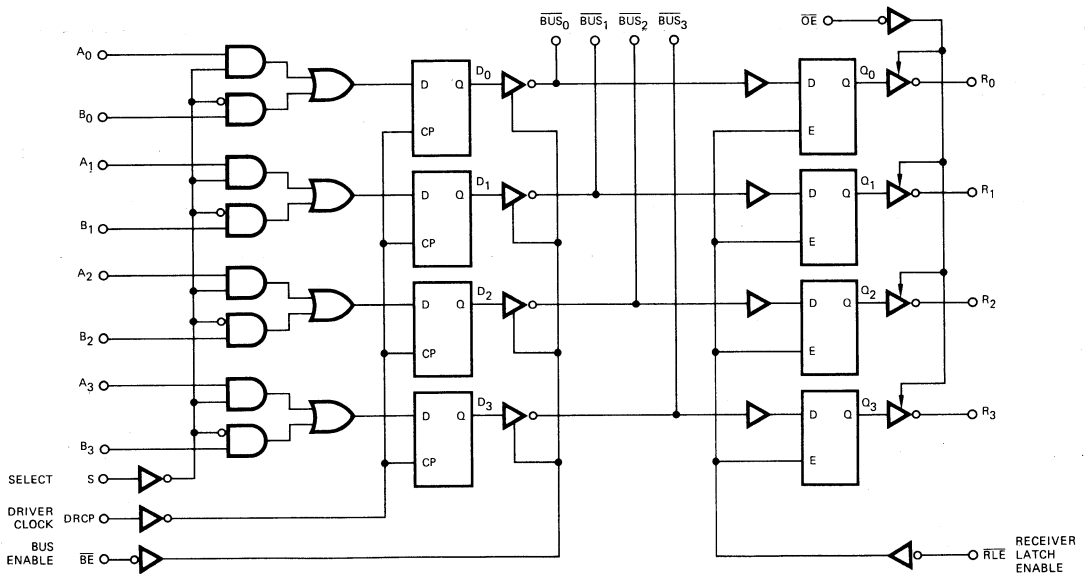

$V_{CC}$ = Pin 24
$GND_1$ = Pin 6
$GND_2$ = Pin 18

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## LOGIC DIAGRAM




## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7V |
| DC Output Current, Into Outputs (Except Bus) | 30mA |
| DC Output Current, Into Bus | 100mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A$ = 0°C to +70°C $V_{CC}$ MIN. = 4.75V $V_{CC}$ MAX. = 5.25V
Am2915AXM (MIL) $T_A$ = −55°C to +125°C $V_{CC}$ MIN. = 4.50V $V_{CC}$ MAX. = 5.50V

## BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | $V_{CC}$ = MIN. | $I_{OL}$ = 24mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 48mA | | | 0.5 | |
| $V_{OH}$ | Bus Output HIGH Voltage | $V_{CC}$ = MIN. | COM'L, $I_{OH}$ = −20mA | 2.4 | | | Volts |
| | | | MIL, $I_{OH}$ = −15mA | | | | |
| $I_O$ | Bus Leakage Current (High Impedance) | $V_{CC}$ = MAX. Bus enable = 2.4V | $V_O$ = 0.4V | | | −200 | μA |
| | | | $V_O$ = 2.4V | | | 50 | |
| | | | $V_O$ = 4.5V | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power OFF) | $V_O$ = 4.5V, $V_{CC}$ = 0V | | | | 100 | μA |
| $V_{IH}$ | Receiver Input HIGH Threshold | Bus enable = 2.4V | | 2.0 | | | Volts |
| $V_{IL}$ | Receiver Input LOW Threshold | Bus enable = 2.4V | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $I_{SC}$ | Bus Output Short Circuit Current | $V_{CC}$ = MAX., $V_O$ = 0V | | −50 | −120 | −225 | mA |

## ELECTRICAL CHARACTERISTICS

**The following conditions apply unless otherwise noted:**

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$ MIN. = 4.75 V $V_{CC}$ MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$ MIN. = 4.50 V $V_{CC}$ MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

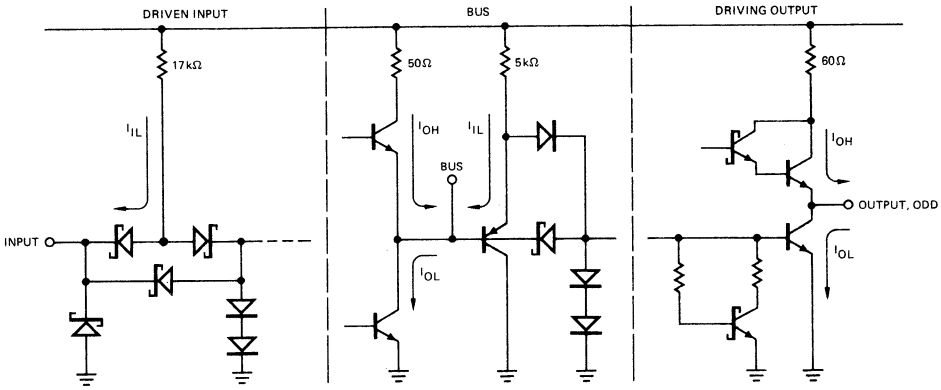
| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | MIL: $I_{OH} = -1.0$mA | 2.4 | 3.4 | | Volts |
| | | | COM'L: $I_{OH} = -2.6$mA | 2.4 | 3.4 | | |
| | | $V_{CC} = 5.0$V, $I_{OH} = -100\mu$A | | 3.5 | | | |
| $V_{OL}$ | Output LOW Voltage (Except Bus) | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | $I_{OL} = 4.0$mA | | 0.27 | 0.4 | Volts |
| | | | $I_{OL} = 8.0$mA | | 0.32 | 0.45 | |
| | | | $I_{OL} = 12$mA | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN} = -18$mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 0.4$V | $\overline{BE}$, $\overline{RLE}$ | | | −0.72 | mA |
| | | | All other inputs | | | −0.36 | |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 2.7$V | | | | 20 | μA |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN} = 7.0$V | | | | 100 | μA |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX. | | −30 | | −130 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | | 63 | 95 | mA |
| $I_O$ | Off-State Output Current (Receiver Outputs) | $V_{CC}$ = MAX. | $V_O = 2.4$V | | | 50 | μA |
| | | | $V_O = 0.4$V | | | −50 | |

## SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am2915AXM Min. | Am2915AXM Typ. (Note 2) | Am2915AXM Max. | Am2915AXC Min. | Am2915AXC Typ. (Note 2) | Am2915AXC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50pF, $R_L$ (BUS) = 130Ω | | 21 | 36 | | 21 | 32 | ns |
| $t_{PLH}$ | | | | 21 | 36 | | 21 | 32 | |
| $t_{ZH}$, $t_{ZL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 26 | | 13 | 23 | ns |
| $t_{HZ}$, $t_{LZ}$ | | | | 13 | 21 | | 13 | 18 | |
| $t_s$ | Data Inputs (A or B) | $C_L$ = 15pF, $R_L$ = 2.0kΩ | 15 | | | 12 | | | ns |
| $t_h$ | | | 8.0 | | | 6.0 | | | |
| $t_s$ | Select Input (S) | | 28 | | | 25 | | | ns |
| $t_h$ | | | 8.0 | | | 6.0 | | | |
| $t_{PW}$ | Driver Clock (DRCP) Pulse Width (HIGH) | | 20 | | | 17 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enable) | | | 18 | 33 | | 18 | 30 | ns |
| $t_{PHL}$ | | | | 18 | 30 | | 18 | 27 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 33 | | 21 | 30 | ns |
| $t_{PHL}$ | | | | 21 | 30 | | 21 | 27 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 15 | | | 13 | | | ns |
| $t_h$ | | | 6.0 | | | 4.0 | | | |
| $t_{ZH}$, $t_{ZL}$ | Output Control to Receiver Output | $C_L$ = 5pF, $R_L$ = 2.0kΩ | | 14 | 26 | | 14 | 23 | ns |
| $t_{HZ}$, $t_{LZ}$ | | | | 14 | 26 | | 14 | 23 | |

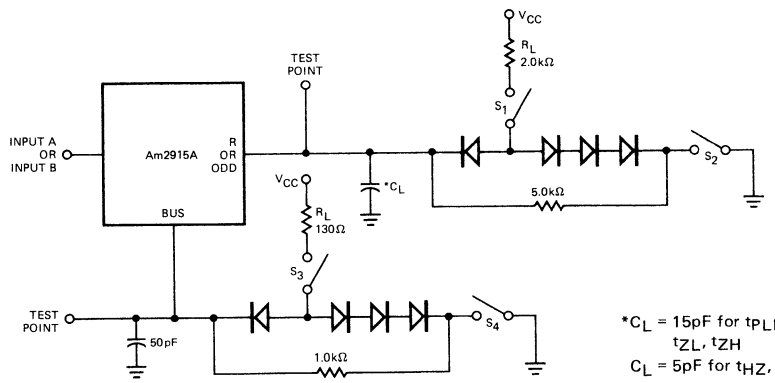
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



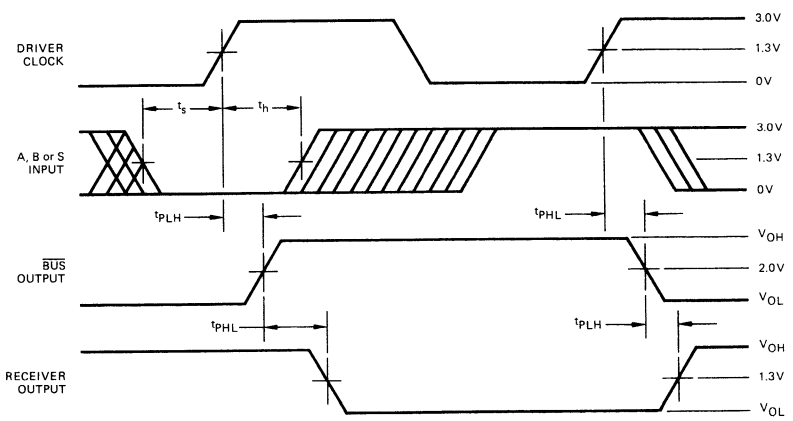

Note: Actual current flow direction shown.

## SWITCHING TEST CIRCUIT




*$C_L$ = 15pF for $t_{PLH}$, $t_{PHL}$, $t_{ZL}$, $t_{ZH}$
$C_L$ = 5pF for $t_{HZ}$, $t_{LZ}$

## SWITCHING WAVEFORMS




Note: Bus to Reciver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

## FUNCTIONAL TABLE

| INPUTS | | | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | $A_i$ | $B_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $\overline{BUS}_i$ | $R_i$ | |
| X | X | X | X | H | X | X | X | X | Z | X | Driver output disable |
| X | X | X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X | X | X | X | H | L | L | X | L | L | H | Driver output disable and receive data via Bus input |
| X | X | X | X | H | L | L | X | H | H | L | |
| X | X | X | X | X | H | X | X | NC | X | X | Latch received data |
| L | L | X | ↑ | X | X | X | L | X | X | X | Load driver register |
| L | H | X | ↑ | X | X | X | H | X | X | X | |
| H | X | L | ↑ | X | X | X | L | X | X | X | |
| H | X | H | ↑ | X | X | X | H | X | X | X | |
| X | X | X | L | X | X | X | NC | X | X | X | No driver clock restrictions |
| X | X | X | H | X | X | X | NC | X | X | X | |
| X | X | X | X | L | X | X | L | X | H | X | Drive Bus |
| X | X | X | X | L | X | X | H | X | L | X | |

H = HIGH  Z = HIGH Impedance  X = Don't Care  i = 0, 1, 2, 3
L = LOW  NC = No Change  ↑ = LOW-to-HIGH Transition

## DEFINITION OF FUNCTIONAL TERMS

**$A_0$, $A_1$, $A_2$, $A_3$** The "A" word data input into the two input multiplexer of the driver register.

**$B_0$, $B_1$, $B_2$, $B_3$** The "B" word data input into the two input multiplexers of the driver register.

**S** Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

**DRCP** Driver Clock Pulse. Clock pulse for the driver register.

**$\overline{BE}$** Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

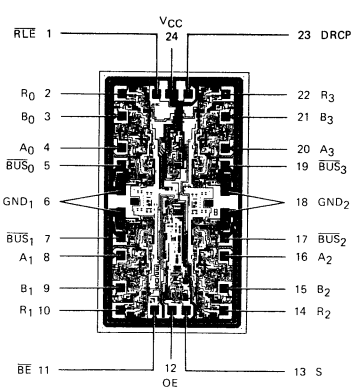
**$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$** The four driver outputs and receiver inputs (data is inverted).

**$R_0$, $R_1$, $R_2$, $R_3$** The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

**$\overline{RLE}$** Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

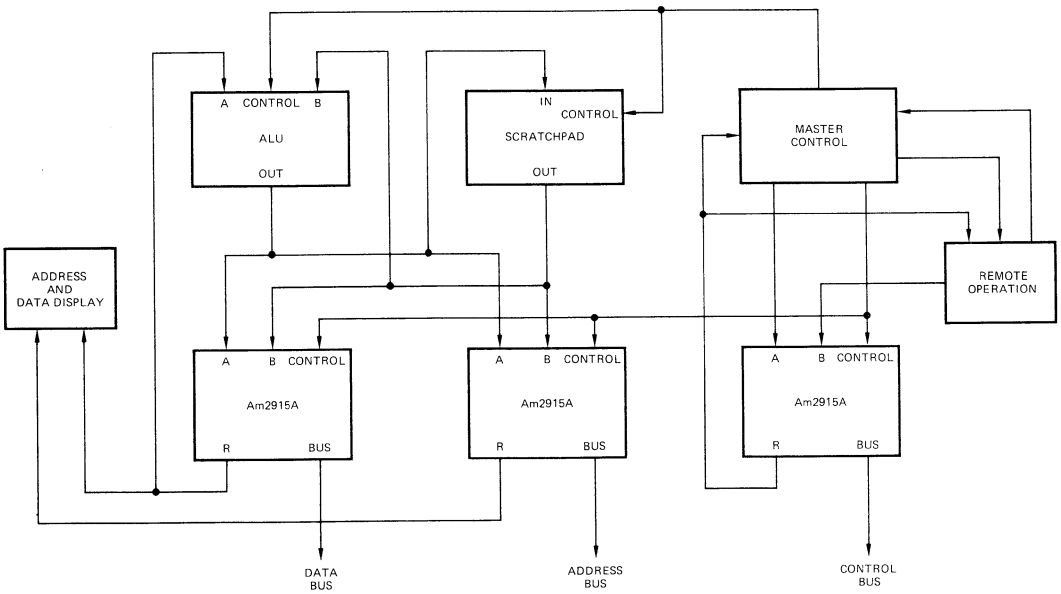
**$\overline{OE}$** Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

### Metallization and Pad Layout

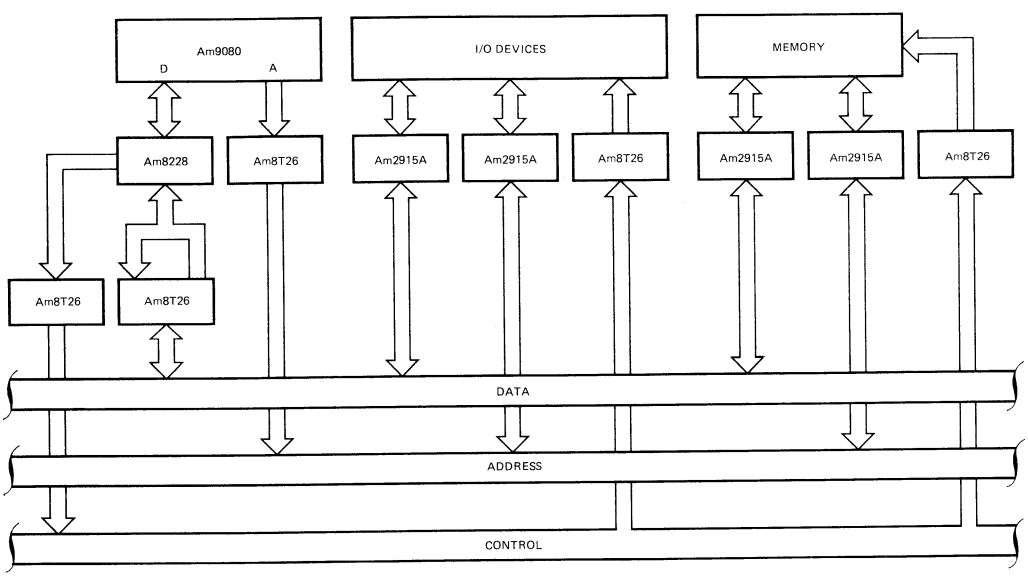



DIE SIZE .074" X .130"

## APPLICATIONS




The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.




Using the Am2915A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

# Am2916A

## Quad Three-State Bus Transceiver With Interface Logic

### Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

### FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

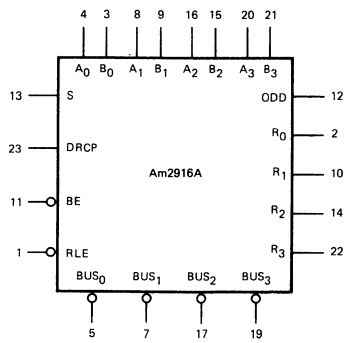
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the $A_i$ data is stored in the register and when S is HIGH, the $B_i$ data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

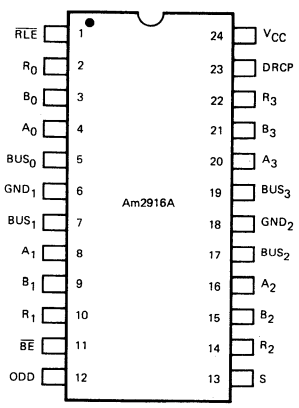
The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

### LOGIC SYMBOL




$V_{CC}$ = Pin 24
$GND_1$ = Pin 6
$GND_2$ = Pin 18

### CONNECTION DIAGRAM
**Top View**

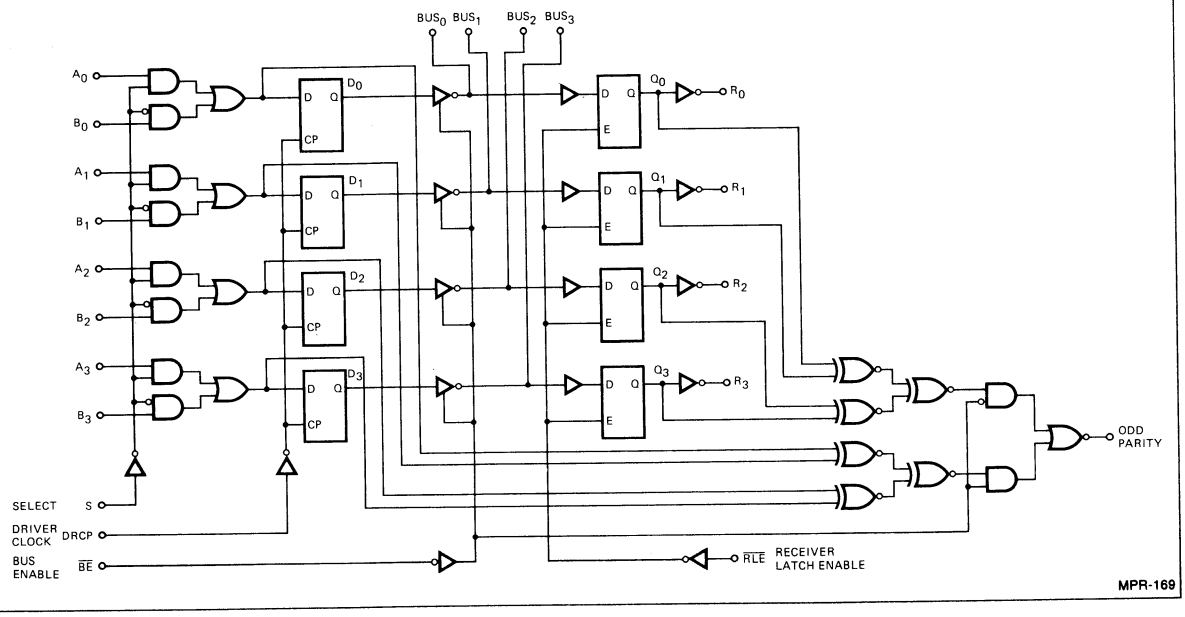



Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2916APC |
| Hermetic DIP | 0°C to +70°C | AM2916ADC |
| Dice | 0°C to +70°C | AM2916AXC |
| Hermetic DIP | −55°C to +125°C | AM2916ADM |
| Hermetic Flat Pak | −55°C to +125°C | AM2916AFM |
| Dice | −55°C to +125°C | AM2916AXM |

## LOGIC DIAGRAM




## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7V |
| DC Output Current, Into Outputs (Except Bus) | 30mA |
| DC Output Current, Into Bus | 100mA |
| DC Input Current | −30mA to +5.0mA |

3

## ELECTRICAL CHARACTERISTICS

**The following conditions apply unless otherwise noted:**

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$MIN. = 4.75V $V_{CC}$MAX. = 5.25V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$MIN. = 4.50V $V_{CC}$MAX. = 5.50V

## BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | $V_{CC}$ = MIN. | $I_{OL}$ = 24mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 48mA | | | 0.5 | |
| $V_{OH}$ | Bus Output HIGH Voltage | $V_{CC}$ = MIN. | COM'L, $I_{OH}$ = −20mA | 2.4 | | | Volts |
| | | | MIL, $I_{OH}$ = −15mA | | | | |
| $I_O$ | Bus Leakage Current (High Impedance) | $V_{CC}$ = MAX. Bus enable = 2.4V | $V_O$ = 0.4V | | | −200 | μA |
| | | | $V_O$ = 2.4V | | | 50 | |
| | | | $V_O$ = 4.5V | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power OFF) | $V_O$ = 4.5V, $V_{CC}$ = 0V | | | | 100 | μA |
| $V_{IH}$ | Receiver Input HIGH Threshold | Bus enable = 2.4V | | 2.0 | | | Volts |
| $V_{IL}$ | Receiver Input LOW Threshold | Bus enable = 2.4V | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $I_{SC}$ | Bus Output Short Circuit Current | $V_{CC}$ = MAX., $V_O$ = 0V | | −50 | −120 | −225 | mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$ MIN. = 4.75 V $V_{CC}$ MAX. = 5.25 V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$ MIN. = 4.50 V $V_{CC}$ MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

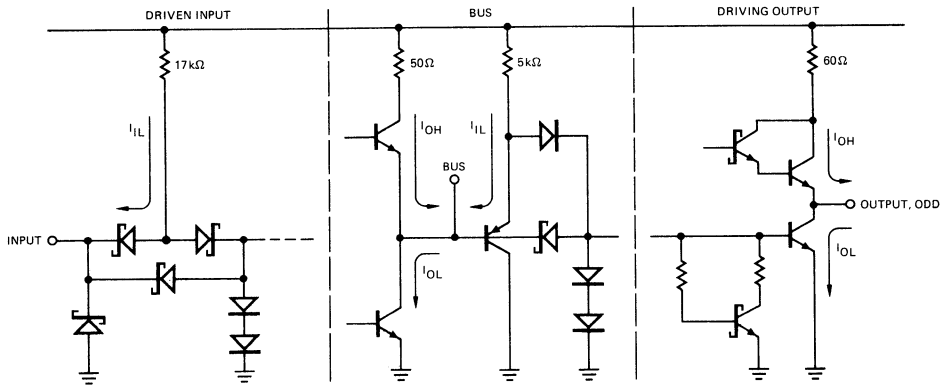
| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | MIL: $I_{OH} = -1.0$ mA | 2.4 | 3.4 | | Volts |
| | | | COM'L: $I_{OH} = -2.6$ mA | 2.4 | 3.4 | | |
| | | $V_{CC}$ = 5.0 V, $I_{OH} = -100\mu$A | | 3.5 | | | |
| $V_{OH}$ | Parity Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Except Bus) | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | $I_{OL}$ = 4.0 mA | | 0.27 | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0 mA | | 0.32 | 0.45 | |
| | | | $I_{OL}$ = 12 mA | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN} = -18$ mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | $\overline{BE}$, $\overline{RLE}$ | | | −0.72 | mA |
| | | | All other inputs | | | −0.36 | |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | $\mu$A |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 100 | $\mu$A |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX. | RECEIVER | −30 | | −130 | mA |
| | | | PARITY | −20 | | −100 | |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., All Inputs = GND | | | 75 | 110 | mA |

## SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am2916AXM Min. | Am2916AXM Typ. (Note 2) | Am2916AXM Max. | Am2916AXC Min. | Am2916AXC Typ. (Note 2) | Am2916AXC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50 pF, $R_L$ (BUS) = 130 Ω | | 21 | 36 | | 21 | 32 | ns |
| $t_{PLH}$ | | | | 21 | 36 | | 21 | 32 | |
| $t_{ZH}$, $t_{ZL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 26 | | 13 | 23 | ns |
| $t_{HZ}$, $t_{LZ}$ | | | | 13 | 21 | | 13 | 18 | |
| $t_s$ | Data Inputs (A or B) | | 15 | | | 12 | | | ns |
| $t_h$ | | | 8.0 | | | 6.0 | | | |
| $t_s$ | Select Inputs (S) | | 28 | | | 25 | | | ns |
| $t_h$ | | | 8.0 | | | 6.0 | | | |
| $t_{PW}$ | Clock Pulse Width (HIGH) | | 20 | | | 17 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enabled) | $C_L$ = 15 pF, $R_L$ = 2.0 kΩ | | 18 | 33 | | 18 | 30 | ns |
| $t_{PHL}$ | | | | 18 | 30 | | 18 | 27 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 33 | | 21 | 30 | ns |
| $t_{PHL}$ | | | | 21 | 30 | | 21 | 27 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 15 | | | 13 | | | ns |
| $t_h$ | | | 6.0 | | | 4.0 | | | |
| $t_{PLH}$ | A or B Data to Odd Parity Output (Driver Enabled) | | | 32 | 46 | | 32 | 42 | ns |
| $t_{PHL}$ | | | | 26 | 40 | | 26 | 36 | |
| $t_{PLH}$ | Bus to Odd Parity Output (Driver Inhibited, Latch Enabled) | | | 21 | 36 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 32 | |
| $t_{PLH}$ | Latch Enable ($\overline{RLE}$) to Odd Parity Output | | | 21 | 36 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 32 | |

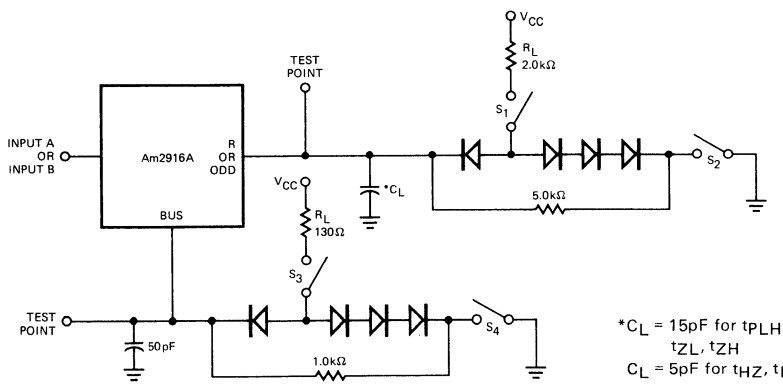
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



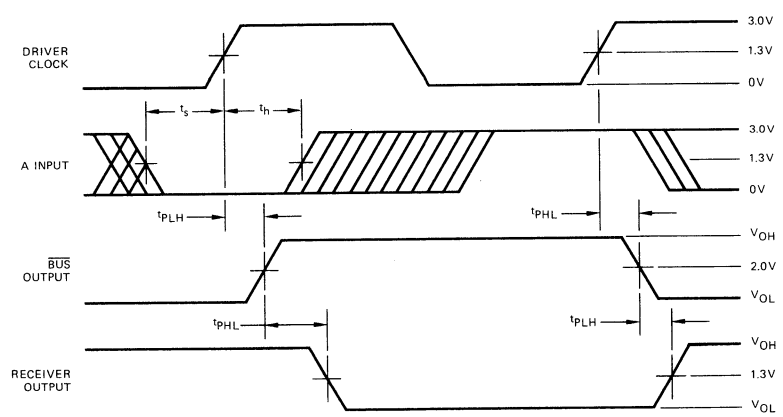

Note: Actual current flow direction shown.

## SWITCHING TEST CIRCUIT




*$C_L$ = 15pF for $t_{PLH}$, $t_{PHL}$, $t_{ZL}$, $t_{ZH}$
$C_L$ = 5pF for $t_{HZ}$, $t_{LZ}$

## SWITCHING WAVEFORMS




Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

## FUNCTION TABLE

| INPUTS | | | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | $A_i$ | $B_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $\overline{BUS}_i$ | $R_i$ | |
| X | X | X | X | H | X | X | X | X | Z | X | Driver output disable |
| X | X | X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X | X | X | X | H | L | L | X | L | L | H | Driver output disable and receive data via Bus input |
| X | X | X | X | H | L | L | X | H | H | L | |
| X | X | X | X | X | H | X | X | NC | X | X | Latch received data |
| L | L | X | ↑ | X | X | X | L | X | X | X | Load driver register |
| L | H | X | ↑ | X | X | X | H | X | X | X | |
| H | X | L | ↑ | X | X | X | L | X | X | X | |
| H | X | H | ↑ | X | X | X | H | X | X | X | |
| X | X | X | L | X | X | X | NC | X | X | X | No driver clock restrictions |
| X | X | X | H | X | X | X | NC | X | X | X | |
| X | X | X | X | L | X | X | L | X | H | X | Drive Bus |
| X | X | X | X | L | X | X | H | X | L | X | |

H = HIGH, L = LOW; Z = HIGH Impedance, NC = No change; X = Don't care, ↑ = LOW-to-HIGH transition; i = 0, 1, 2, 3

## DEFINITION OF FUNCTIONAL TERMS

**$A_0$, $A_1$, $A_2$, $A_3$** The "A" word data input into the two input multiplexer of the driver register.

**$B_0$, $B_1$, $B_2$, $B_3$** The "B" word data input into the two input multiplexers of the driver register.

**S** Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

**DRCP** Driver Clock Pulse. Clock pulse for the driver register.

**$\overline{BE}$** Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

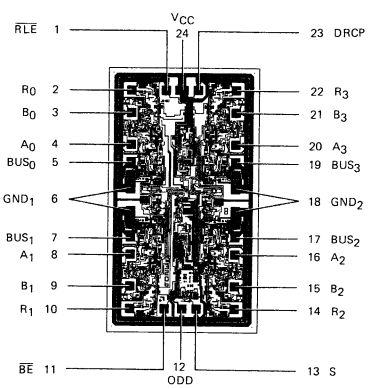
**$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$** The four driver outputs and receiver inputs (data is inverted).

**$R_0$, $R_1$, $R_2$, $R_3$** The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

**$\overline{RLE}$** Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

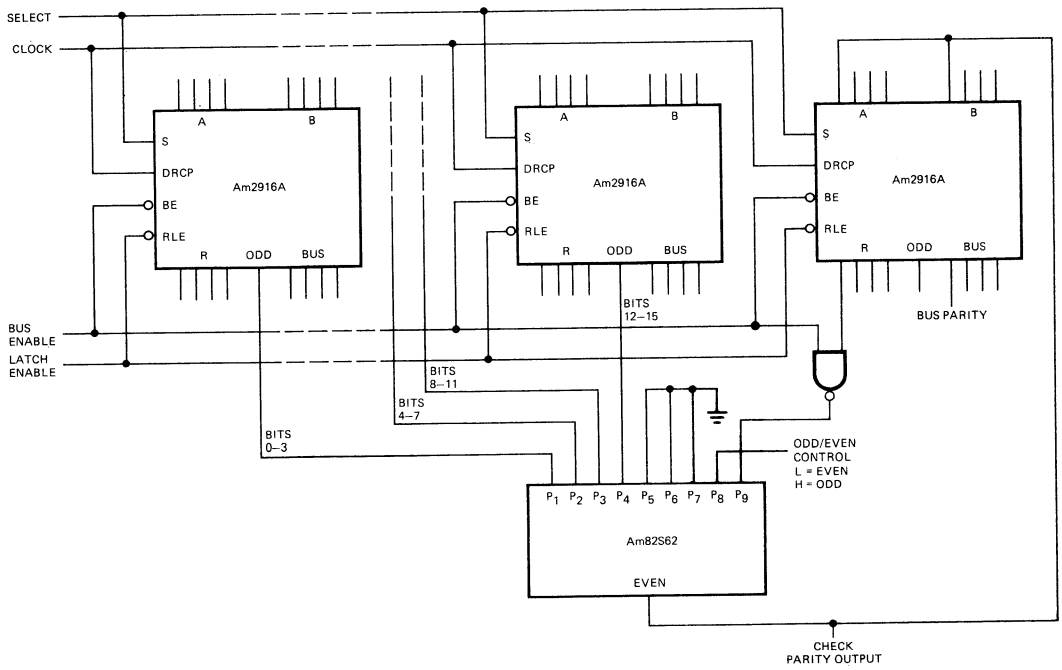
**$\overline{OE}$** Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

### Metallization and Pad Layout

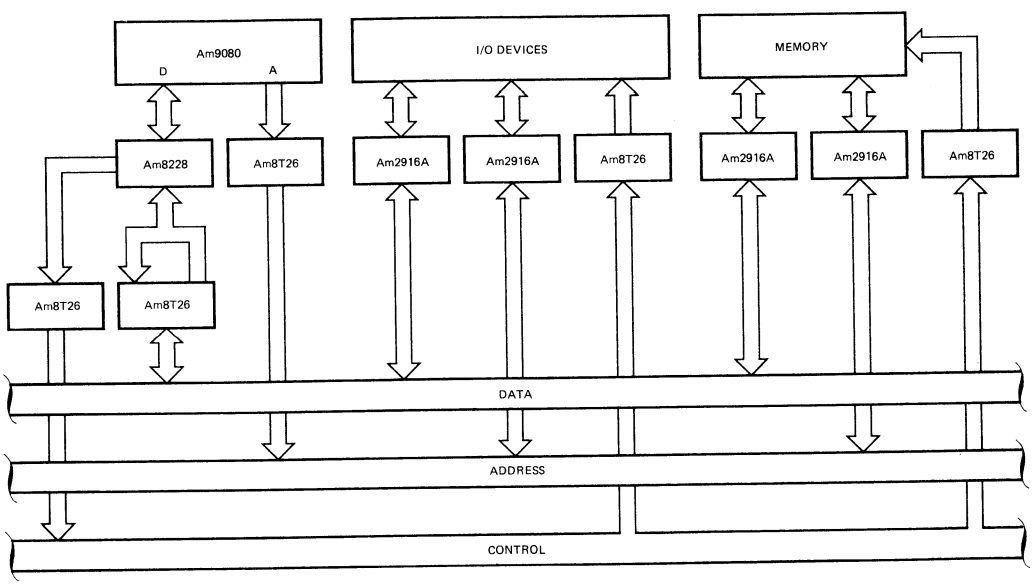



DIE SIZE .074" X .130"

## APPLICATIONS




Generating or checking parity for 16 data bits.




Using the Am2916A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

# Am2917A

## Quad Three-State Bus Transceiver With Interface Logic

### Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

### UNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

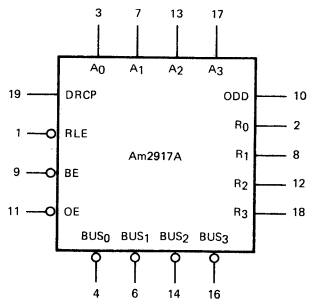
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the $A_i$ data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

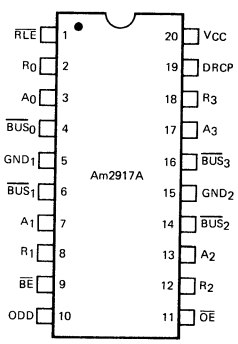
The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
$GND_1$ = Pin 5
$GND_2$ = Pin 15

### CONNECTION DIAGRAM
**Top View**

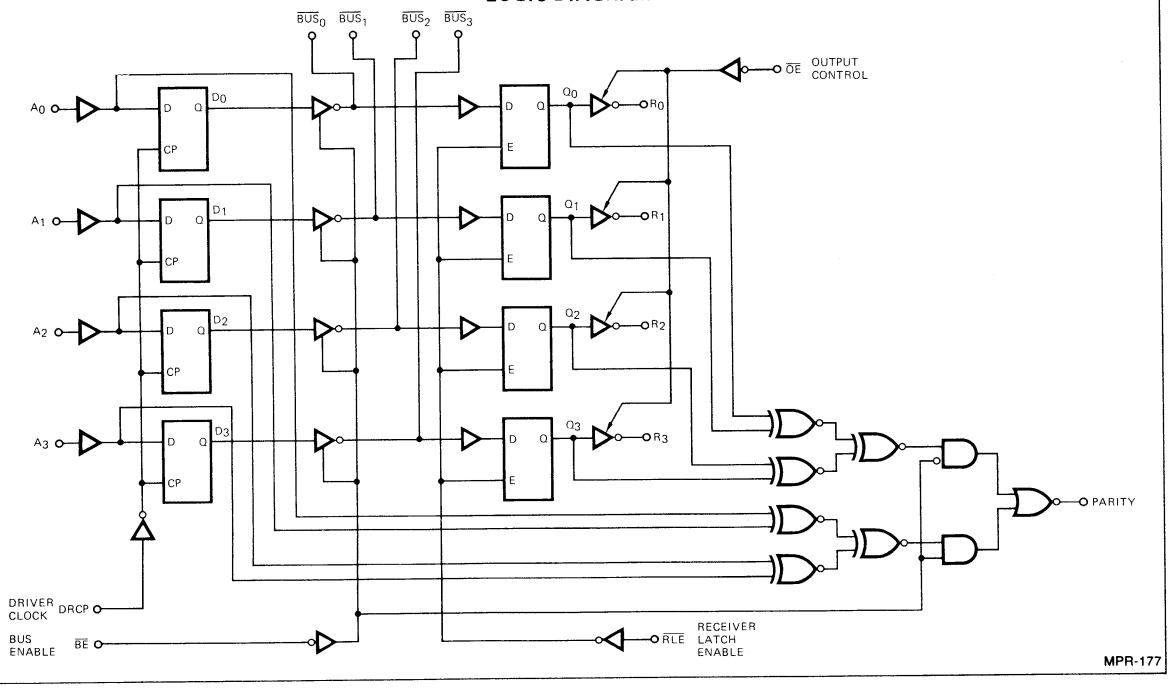



Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2917APC |
| Hermetic DIP | 0°C to +70°C | AM2917ADC |
| Dice | 0°C to +70°C | AM2917AXC |
| Hermetic DIP | −55°C to +125°C | AM2917ADM |
| Hermetic Flat Pak | −55°C to +125°C | AM2917AFM |
| Dice | −55°C to +125°C | AM2917AXM |

## LOGIC DIAGRAM




## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7 V |
| DC Output Current, Into Outputs (Except BUS) | 30 mA |
| DC Output Current, Into Bus | 100 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$ MIN. = 4.75 V $V_{CC}$ MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$ MIN. = 4.50 V $V_{CC}$ MAX. = 5.50 V

## BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | $V_{CC}$ = MIN. | $I_{OL}$ = 24 mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 48 mA | | | 0.5 | |
| $V_{OH}$ | Bus Output HIGH Voltage | $V_{CC}$ = MIN. | COM'L, $I_{OH}$ = −20 mA | 2.4 | | | Volts |
| | | | MIL, $I_{OH}$ = −15 mA | | | | |
| $I_O$ | Bus Leakage Current (High Impedance) | $V_{CC}$ = MAX. Bus enable = 2.4 V | $V_O$ = 0.4 V | | | −200 | μA |
| | | | $V_O$ = 2.4 V | | | 50 | |
| | | | $V_O$ = 4.5 V | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power OFF) | $V_O$ = 4.5 V, $V_{CC}$ = 0 V | | | | 100 | μA |
| $V_{IH}$ | Receiver Input HIGH Threshold | Bus enable = 2.4 V | | 2.0 | | | Volts |
| $V_{IL}$ | Receiver Input LOW Threshold | Bus enable = 2.4 V | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $I_{SC}$ | Bus Output Short Circuit Current | $V_{CC}$ = MAX., $V_O$ = 0 V | | −50 | −120 | −225 | mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC}$ MIN. = 4.75 V $V_{CC}$ MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC}$ MIN. = 4.50 V $V_{CC}$ MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

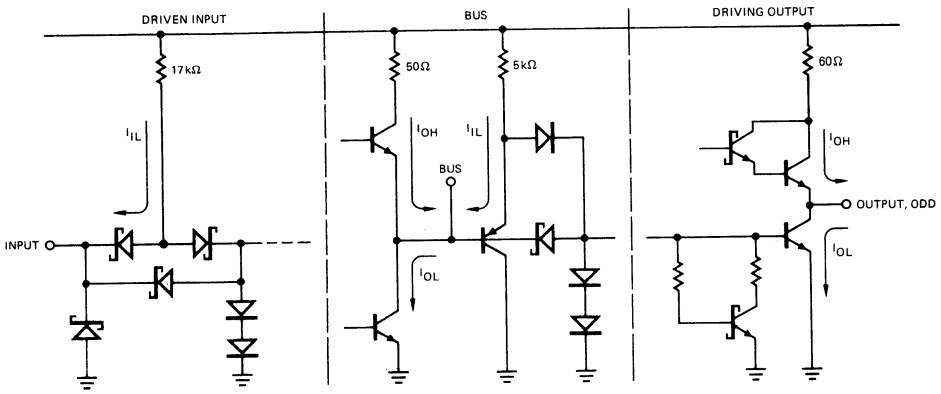
| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | MIL: $I_{OH} = -1.0$mA | 2.4 | 3.4 | | Volts |
| | | | COM'L: $I_{OH} = -2.6$mA | 2.4 | 3.4 | | |
| | | $V_{CC}$ = 5.0 V, $I_{OH} = -100\mu$A | | 3.5 | | | |
| $V_{OH}$ | Parity Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Except Bus) | $V_{CC}$ = MIN., $V_{IN} = V_{IL}$ or $V_{IH}$ | $I_{OL}$ = 4.0mA | | 0.27 | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | 0.32 | 0.45 | |
| | | | $I_{OL}$ = 12mA | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN} = -18$mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 0.4 V | $\overline{BE}$, $\overline{RLE}$ | | | −0.72 | mA |
| | | | All other inputs | | | −0.36 | |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 20 | μA |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 7.0 V | | | | 100 | μA |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX. | RECEIVER | −30 | | −130 | mA |
| | | | PARITY | −20 | | −100 | |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | | 63 | 95 | mA |
| $I_O$ | Off-State Output Current (Receiver Outputs) | $V_{CC}$ = MAX. | $V_O$ = 2.4 V | | | 50 | μA |
| | | | $V_O$ = 0.4 V | | | −50 | |

## SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am2917AXM Min. | Am2917AXM Typ. (Note 2) | Am2917AXM Max. | Am2917AXC Min. | Am2917AXC Typ. (Note 2) | Am2917AXC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50pF, $R_L$ BUS) = 130Ω | | 21 | 36 | | 21 | 32 | ns |
| $t_{PLH}$ | | | | 21 | 36 | | 21 | 32 | |
| $t_{ZH}$, $t_{ZL}$ | Bus Enable ($\overline{BE}$) to Bus | $C_L$ = 15pF, $R_L$ = 2.0kΩ | | 13 | 26 | | 13 | 23 | ns |
| $t_{HZ}$, $t_{LZ}$ | | | | 13 | 21 | | 13 | 18 | |
| $t_s$ | A Data Inputs | | 15 | | | 12 | | | ns |
| $t_h$ | | | 8.0 | | | 6.0 | | | |
| $t_{PW}$ | Clock Pulse Width (HIGH) | | 20 | | | 17 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enabled) | | | 18 | 33 | | 18 | 30 | ns |
| $t_{PHL}$ | | | | 18 | 30 | | 18 | 27 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 33 | | 21 | 30 | ns |
| $t_{PHL}$ | | | | 21 | 30 | | 21 | 27 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 15 | | | 13 | | | ns |
| $t_h$ | | | 6.0 | | | 4.0 | | | |
| $t_{PLH}$ | A Data to Odd Parity Out (Driver Enabled) | | | 32 | 46 | | 32 | 42 | ns |
| $t_{PHL}$ | | | | 26 | 40 | | 26 | 36 | |
| $t_{PLH}$ | Bus to Odd Parity Out (Driver Inhibit) | | | 21 | 36 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 32 | |
| $t_{PLH}$ | Latch Enable ($\overline{RLE}$) to Odd Parity Output | | | 21 | 36 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 32 | |
| $t_{ZH}$, $t_{ZL}$ | Output Control to Output | | | 14 | 26 | | 14 | 23 | ns |
| $t_{HZ}$, $t_{LZ}$ | | $C_L$ = 5pF, $R_L$ = 2.0kΩ | | 14 | 26 | | 14 | 23 | |

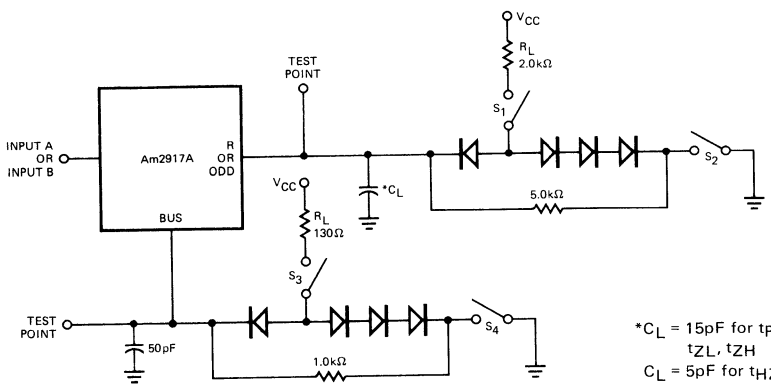
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



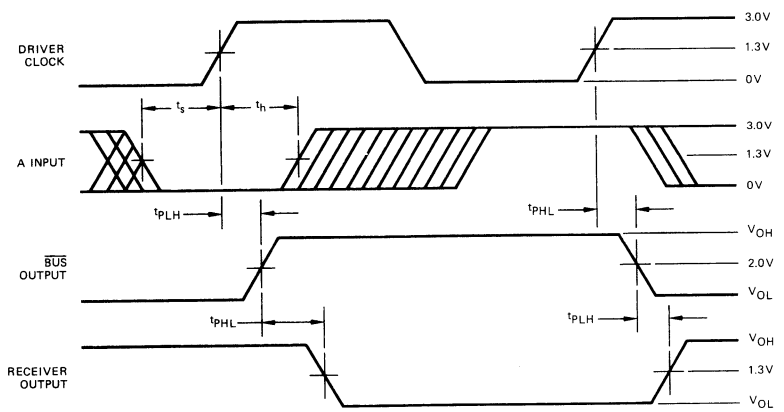

Note: Actual current flow direction shown.

## SWITCHING TEST CIRCUIT




*$C_L$ = 15pF for $t_{PLH}$, $t_{PHL}$, $t_{ZL}$, $t_{ZH}$
$C_L$ = 5pF for $t_{HZ}$, $t_{LZ}$

## SWITCHING WAVEFORMS




Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

## FUNCTION TABLE

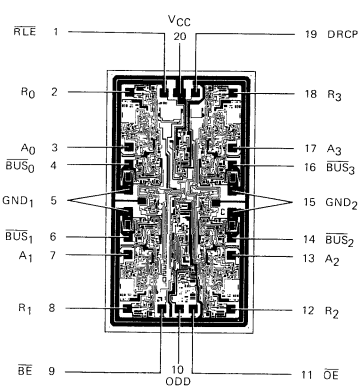
| INPUTS | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| $A_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $BUS_i$ | $R_i$ | |
| X | X | H | X | X | X | X | Z | X | Driver output disable |
| X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X | X | H | L | L | X | L | L | H | Driver output disable and receive data via Bus input |
| X | X | H | L | L | X | H | H | L | |
| X | X | X | H | X | X | NC | X | X | Latch received data |
| L | ↑ | X | X | X | L | X | X | X | Load driver register |
| H | ↑ | X | X | X | H | X | X | X | |
| X | L | X | X | X | NC | X | X | X | No driver clock restrictions |
| X | H | X | X | X | NC | X | X | X | |
| X | X | L | X | X | L | X | H | X | Drive Bus |
| X | X | L | X | X | H | X | L | X | |

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

## PARITY OUTPUT FUNCTION TABLE

| $\overline{BE}$ | ODD PARITY OUTPUT |
|---|---|
| L | ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$ |
| H | ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$ |

### Metallization and Pad Layout




DIE SIZE .074" X .130"

## DEFINITION OF FUNCTIONAL TERMS

**DRCP** Driver Clock Pulse. Clock pulse for the driver register.

**$\overline{BE}$** Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

**$BUS_0$, $BUS_1$, $BUS_2$, $BUS_3$** The four driver outputs and receiver inputs (data is inverted).

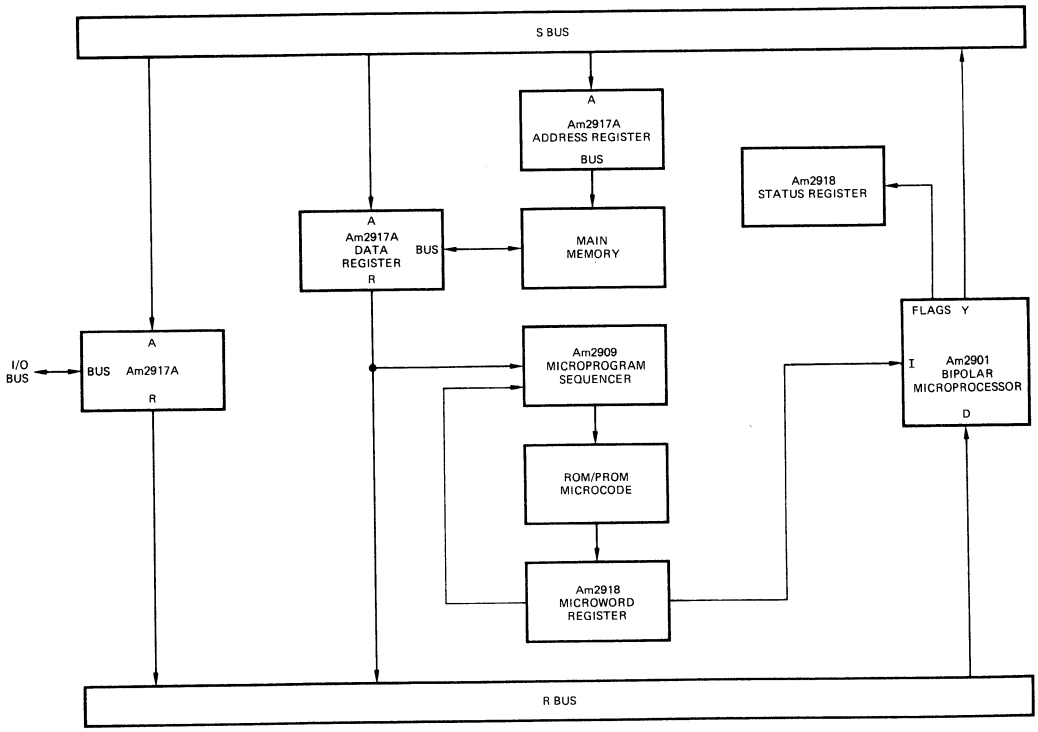
**$R_0$, $R_1$, $R_2$, $R_3$** The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

**$\overline{RLE}$** Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

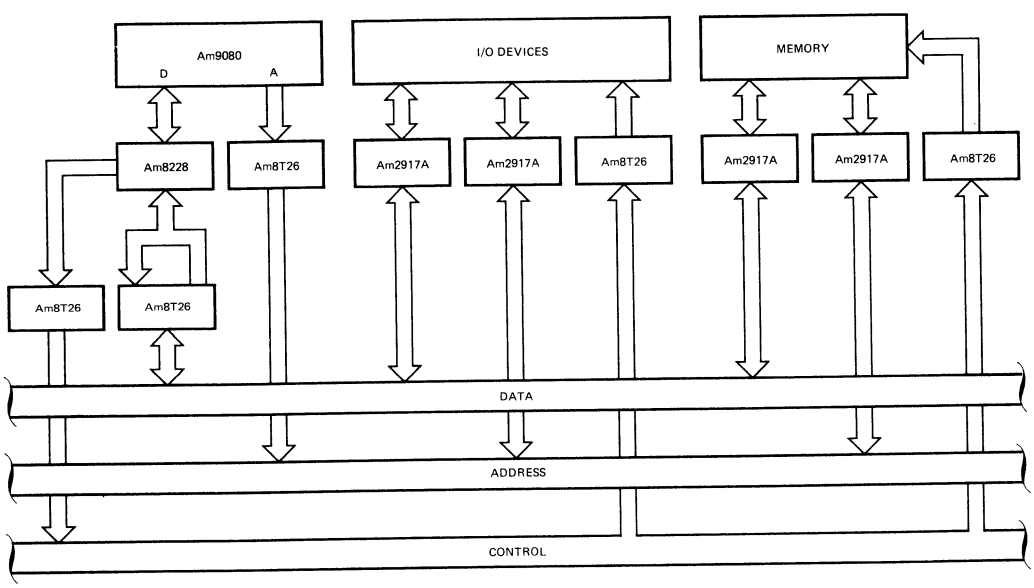
**ODD** Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

**$\overline{OE}$** Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

## APPLICATIONS




The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.




Using the Am2917A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

# HIGH SPEED SCHOTTKY S-MSI AND INTERFACE DATA SHEETS



## APPLICATION NOTES

## DEFINITION OF A.C. (SWITCHING) TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

$f_{MAX}$ The highest operating clock frequency.

$t_{PLH}$ The propagation delay time from an input change to an output LOW-to-HIGH transition.

$t_{PHL}$ The propagation delay time from an input change to an output HIGH-to-LOW transition.

$t_{PW}$ Pulse width. The time between the leading and trailing edges of a pulse.

$t_r$ Rise time. The time required for a signal to change from 10% to 90% of its measured values.

$t_f$ Fall time. The time required for a signal to change from 90% to 10% of its measured values.

$t_s$ Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

$t_h$ Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

$t_R$ Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

$t_{HZ}$ HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5 V change).

$t_{LZ}$ LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5 V change).

$t_{ZH}$ Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

$t_{ZL}$ Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

## DEFINITION OF D.C. TERMS

**H** HIGH, applying to a HIGH voltage level.

**L** LOW, applying to a LOW voltage level.

**I** Input.

**O** Output.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

$I_{IL}$ LOW-level input current with a specified LOW-level voltage applied.

$I_{IH}$ HIGH-level input current with a specified HIGH-level voltage applied.

$I_{OL}$ LOW-level output current.

$I_{OH}$ HIGH-level output current.

$I_{SC}$ Output short-circuit source current.

$I_{CC}$ The supply current drawn by the device from the $V_{CC}$ power supply.

$V_{IL}$ Logic LOW input voltage.

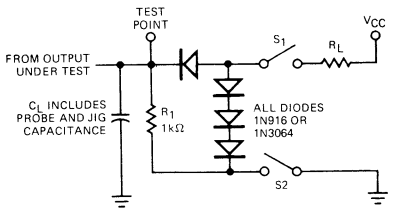
$V_{IH}$ Logic HIGH input voltage.

$V_{OL}$ LOW-level output voltage with $I_{OL}$ applied.

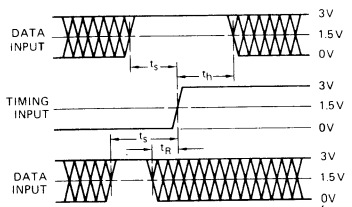
$V_{OH}$ HIGH-level output voltage with $I_{OH}$ applied.

## SCHOTTKY PARAMETER MEASUREMENTS FOR THREE-STATE OUTPUTS

### LOAD TEST CIRCUIT

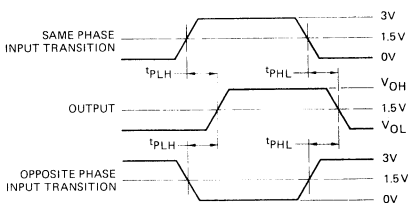



### SET-UP, HOLD, AND RELEASE TIMES

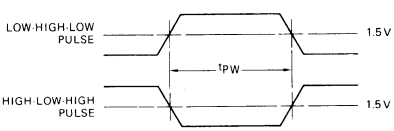



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

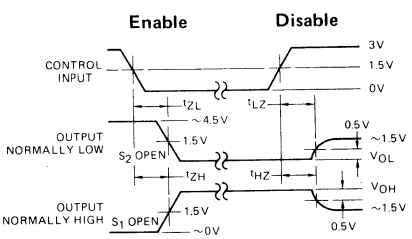
### PROPAGATION DELAY




### PULSE WIDTH




### ENABLE AND DISABLE TIMES




Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. $S_1$ and $S_2$ of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o$ = 50Ω; $t_r$ ≤ 2.5 ns; $t_f$ ≤ 2.5 ns.

4

# Am25S05

## Four-Bit by Two-Bit 2's Complement Multiplier

### Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.
- 100% reliability assurance testing in compliance with MIL-STD-883.

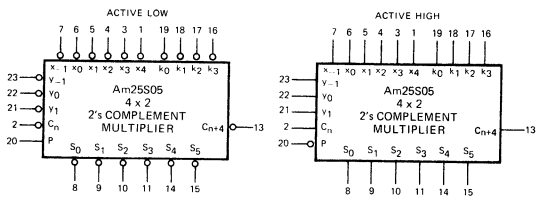
### FUNCTIONAL DESCRIPTION

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

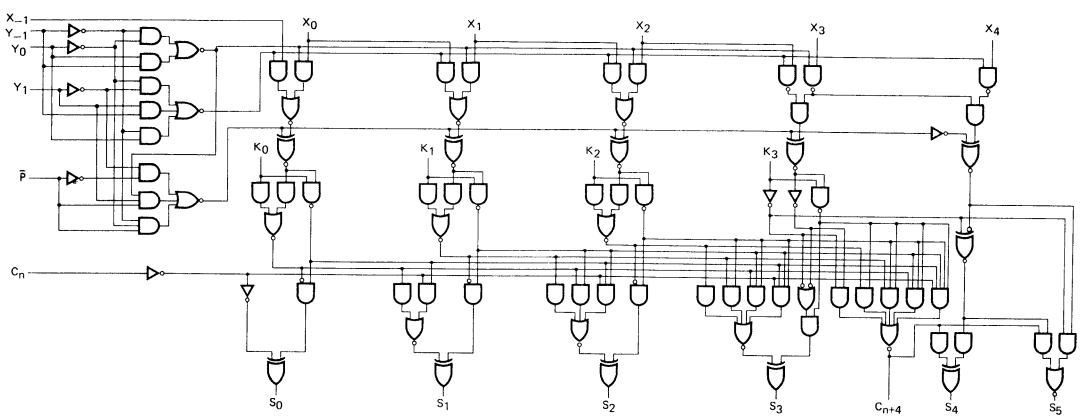
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$.

### LOGIC SYMBOLS




$V_{CC}$ = Pin 24
GND = Pin 12

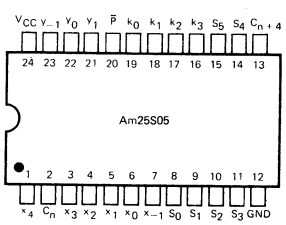
### LOGIC DIAGRAM



### Am25S05 ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +75°C | AM25S05PC |
| Hermetic DIP | 0°C to +75°C | AM25S05DC |
| Dice | 0°C to +75°C | AM25S05XC |
| Hermetic DIP | −55°C to +125°C | AM25S05DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25S05FM |
| Dice | −55°C to +125°C | AM25S05XM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | |
|---|---|---|
| Am25S05XC, DC, PC | $T_A$ = 0°C to +75°C | $V_{CC}$ = 4.75 V to 5.25 V |
| Am25S05XM, DM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 4.50 V to 5.50 V |
| Am25S05FM | $T_C$ = −55°C to +125°C | $V_{CC}$ = 4.50 V to 5.50 V |

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | XM | 2.5 | 3.3 | | Volts |
| | | | XC | 2.7 | 3.3 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.3 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $I_{IL}$ (Note 2) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −2.0 | mA |
| $I_{IH}$ (Note 2) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 50 | μA |
| | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., $Y_1$ =.0V | | | 120 | 175 | mA |

Note 1. Typical Limits are at $V_{CC}$ = 5.0V, 25°C Ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the input load factor. (See loading rules)

## Switching Characteristics ($V_{CC}$ = 5 V, $T_A$ = 25°C, $C_L$ = 15 pF, $R_L$ = 280Ω )

| Parameters | From (Input) | To (Output) | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | $C_n$ | $C_{n+4}$ | See Test Table | 4<br>4 | 8<br>9 | 12<br>14 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | $C_n$ | $S_{0,1,2,3}$ | | 6<br>5 | 12<br>10 | 18<br>15 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | $C_n$ | $S_{4,5}$ | | 7<br>6 | 15<br>13 | 22<br>20 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any k | $C_{n+4}$ | | 3<br>5 | 6.5<br>10 | 12<br>15 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any k | $S_{0,1,2,3}$ | | 6<br>4 | 13.5<br>9.5 | 20<br>14 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any k | $S_{4,5}$ | | 3<br>3 | 15.5<br>12.5 | 23<br>19 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any x | $C_{n+4}$ | | 8<br>9 | 17<br>18 | 26<br>27 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any x | $S_{0,1,2,3}$ | | 10<br>10 | 21<br>21 | 32<br>32 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any x | $S_{4,5}$ | | 6<br>5 | 23.5<br>21.5 | 35<br>32 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any y | $C_{n+4}$ | | 11<br>10 | 23<br>20 | 34<br>30 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any y | $S_{0,1,2,3}$ | | 11<br>11 | 23<br>23 | 34<br>34 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Any y | $S_{4,5}$ | | 12<br>12 | 25<br>25 | 37<br>37 | ns |

## SWITCHING TIME TEST TABLE

| Input | Outputs | Inputs at 0V (remaining inputs at 4.5V) |
|---|---|---|
| $C_n$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All X |
| $k_0$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All X |
| $k_1$ | $C_{n+4}$, $S_{123}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All X |
| $k_2$ | $C_{n+4}$, $S_{23}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All X |
| $k_3$ | $S_3$ | P, $Y_{-1}$, $Y_1$, All X |
| $k_3$ | $S_{45}$ | P, $Y_{-1}$, $Y_1$, All X, $C_n$ |
| $x_{-1}$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | P, $Y_1$, All k |
| $x_0$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All k |
| $x_1$ | $C_{n+4}$, $S_{123}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All k |
| $x_2$ | $C_{n+4}$, $S_{123}$, $S_{45}$ | P, $Y_{-1}$, $Y_1$, All k |
| $x_3$ | $S_3$ | P, $Y_{-1}$, $Y_1$, All k |
| $x_3$ | $S_{45}$ | P, $Y_{-1}$, $Y_1$, All k, $C_n$ |
| $x_4$ | $S_{45}$ | P, $Y_1$, All k, $C_n$ |
| $y_{-1}$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | P, $X_1$, $X_2$, $X_3$, $X_4$, All k |
| $y_0$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | P, $X_1$, $X_2$, $X_3$, $X_4$, All k |
| $y_1$ | $C_{n+4}$, $S_{0123}$, $S_{45}$ | $X_0$, $X_1$, $X_2$, $X_3$, $X_4$, All k |

## DEFINITION OF TERMS

### SUBSCRIPT TERMS:

**H** HIGH, applying to a HIGH logic level or when used with $V_{CC}$ to indicate high $V_{CC}$ value.

**I** Input.

**L** LOW, applying to LOW logic level or when used with $V_{CC}$ to indicate low $V_{CC}$ value.

**O** Output.

### FUNCTIONAL TERMS

**$C_n$** The carry input to the high-speed adder.

**$C_{n+4}$** The carry output from the high-speed adder.

**$k_i$** The constant field used for accumulating partial products.

$i = 0, 1, 2, 3$. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.

**$\overline{P}$** The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.

**$S_i$** The product outputs. $i = 0, 1, 2, 3, 4, 5$.

**$x_i$** The multiplicand inputs. $i = -1, 0, 1, 2, 3, 4$. At the first column of the array $x_{-1}$ must be held at logic '0', and at the last column of the array $x_4$ is connected to $x_3$.

**$y_i$** The multiplier inputs. $i = -1, 0, 1$. At the first row of the array $y_{-1}$ must be held at logic '0'.

### OPERATIONAL TERMS:

**$I_{IL}$** Forward input load current.

**$I_{OH}$** Output HIGH current, forced out of output in $V_{OH}$ test.

**$I_{OL}$** Output LOW current, forced into the output in $V_{OL}$ test.

**$I_{CC}$** The current drawn by the device from $V_{CC}$ power supply with input and output terminals open.

**$I_{IH}$** Reverse input load current.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

**$V_{IH}$** Minimum logic HIGH input voltage.

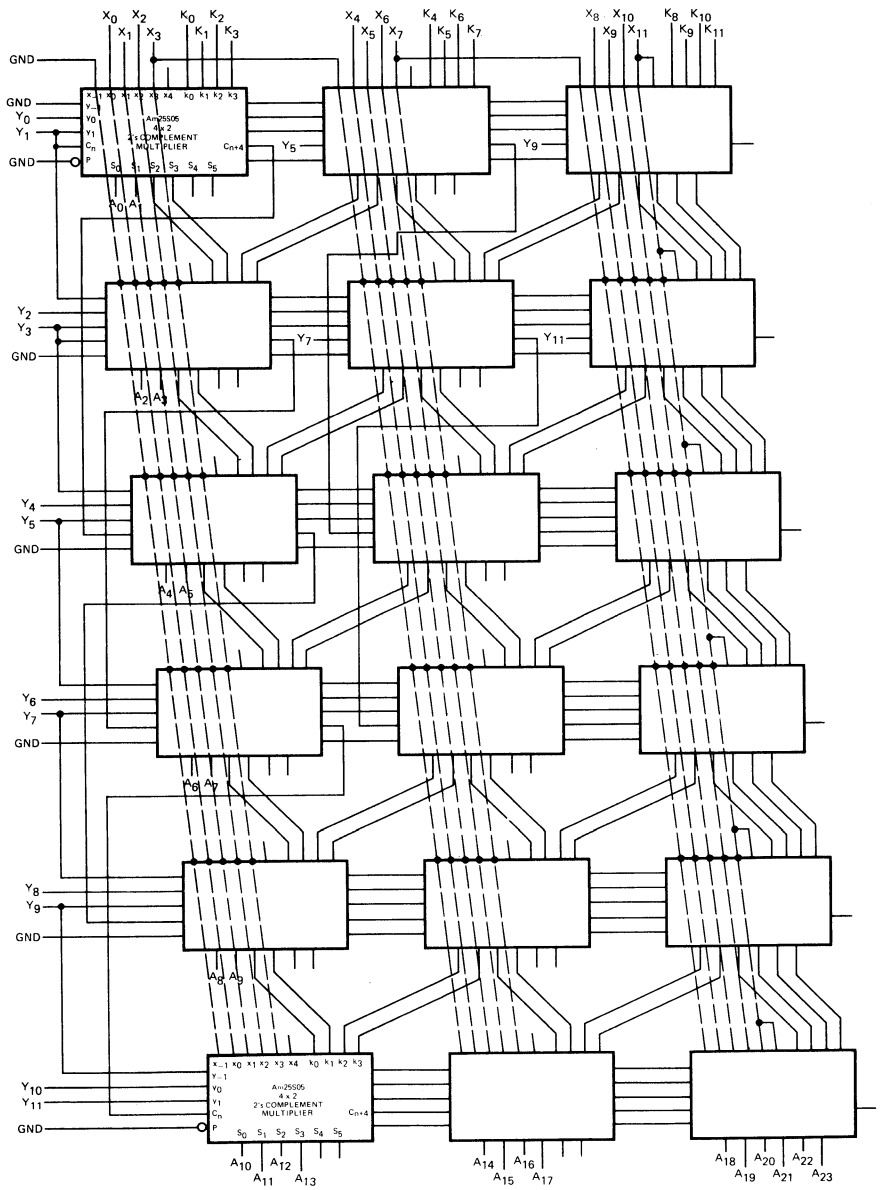
**$V_{IL}$** Maximum logic LOW input voltage.

**$V_{IN}$** Input voltage applied in $I_{IL}$, $I_{IH}$ tests.

**$V_{OH}$** Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

**$V_{OL}$** Maximum logic LOW output voltage with output LOW current $I_{OL}$ flowing into output.

## APPLICATION




Critical speed carries between columns have been interchanged with 2's complement carry-ins $Y_5$, $Y_7$, $Y_9$, $Y_{11}$ for highest speed.

**Figure 1. High Speed 12x12 2's Complement Multiplication**

## MSI INTERFACING RULES

| Interfacing Digital Family | Equivalent Input Unit Load HIGH | LOW |
|---|---|---|
| Advanced Micro Devices 54/7400 Series | 1.25 | 1.25 |
| Advanced Micro Devices 9300/2500 Series | 1.25 | 1.25 |
| FSC Series 9300 | 1.25 | 1.25 |
| TI Series 54/7400 | 1.25 | 1.25 |
| Signetics Series 8200 | 2.5 | 2.5 |
| National Series DM 75/85 | 1.25 | 1.25 |
| DTL Series 930 | 15 | 1.25 |

## OPERATION TABLE

| Y Multiplier | | | Operation X Multiplicand |
|---|---|---|---|
| $y_{-1}$ | $y_0$ | $y_1$ | |
| 0 | 0 | 0 | K + 0 |
| 1 | 0 | 0 | K + X |
| 0 | 1 | 0 | K + X |
| 1 | 1 | 0 | K + 2X |
| 0 | 0 | 1 | K – 2X |
| 1 | 0 | 1 | K – X |
| 0 | 1 | 1 | K – X |
| 1 | 1 | 1 | K – 0 |

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

## Am25S05 LOADING RULES IN UNIT LOADS

| Input/Output | Pin No.'s | Input Unit Load Input HIGH | Input LOW | Fanout Output HIGH | Output LOW |
|---|---|---|---|---|---|
| $x_4$ | 1 | 0.2 | 0.2 | – | – |
| $C_n$ | 2 | 0.2 | 0.2 | – | – |
| $x_3$ | 3 | 0.2 | 0.2 | – | – |
| $x_2$ | 4 | 0.4 | 0.4 | – | – |
| $x_1$ | 5 | 0.4 | 0.4 | – | – |
| $x_0$ | 6 | 0.4 | 0.4 | – | – |
| $x_{-1}$ | 7 | 0.2 | 0.2 | – | – |
| $S_0$ | 8 | – | – | 20 | 10 |
| $S_1$ | 9 | – | – | 20 | 10 |
| $S_2$ | 10 | – | – | 20 | 10 |
| $S_3$ | 11 | – | – | 20 | 10 |
| GND | 12 | – | – | – | – |
| $C_{n+4}$ | 13 | – | – | 20 | 10 |
| $S_4$ | 14 | – | – | 20 | 10 |
| $S_5$ | 15 | – | – | 20 | 10 |
| $k_3$ | 16 | 2 | 2 | – | – |
| $k_2$ | 17 | 2 | 2 | – | – |
| $k_1$ | 18 | 2 | 2 | – | – |
| $k_0$ | 19 | 2 | 2 | – | – |
| $\overline{P}$ | 20 | 1 | 1 | – | – |
| $y_1$ | 21 | 0.6 | 0.6 | – | – |
| $y_0$ | 22 | 0.6 | 0.6 | – | – |
| $y_{-1}$ | 23 | 0.6 | 0.6 | – | – |
| $V_{CC}$ | 24 | – | – | – | – |

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH Logic Level and –2.0 mA at 0.5 V at the LOW Logic Level.

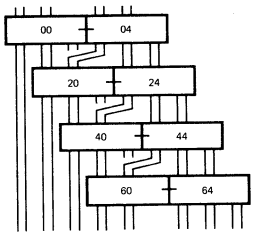
## USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the $y_i$ multiplier bit to the appropriate carry input terminal i = 1, 3, 5 . . .
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$

| Number representation | Correction |
|---|---|
| 2's complement | None |
| 1's complement | Add $x_s Y_2 + y_s X_2 + x_s y_s$ at k inputs |
| Unsigned (magnitude) | Extend multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force $k_s, y_s, x_s = 0$. |
| Sign magnitude | $x_s = 0, y_s = 0$ None |
| | $x_s = 1, y_s = 0$ Form $[(XY)_2 + 2^{n-1} y]$ |
| | $x_s = 0, y_s = 1$ Form $[(XY)_2 + 2^{n-1} x]$ |
| | $x_s = 1, y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$ |

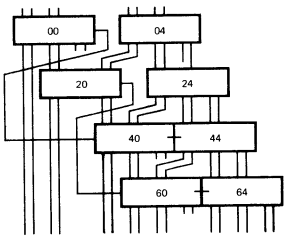
4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

## CONNECTION SCHEMES



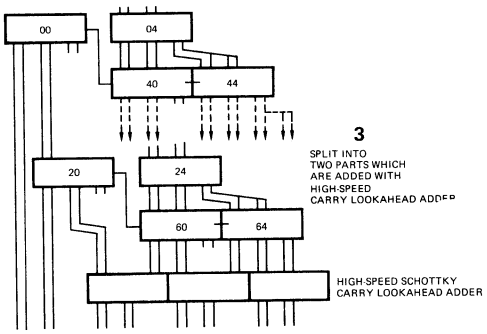

**1**

PARALLELOGRAM CARRIES STAY IN SAME ROW




**2**

PARALLELOGRAM CARRIES FROM LOWER ORDER MULTIPLIERS SKIP TO ALTERNATE ROWS WHERE POSSIBLE




**3**

SPLIT INTO TWO PARTS WHICH ARE ADDED WITH HIGH-SPEED CARRY LOOKAHEAD ADDER

## TYPICAL MULTIPLICATION TIMES

| Array Size Bits | Total Multiplication Time (ns) | Package Count | |
|---|---|---|---|
| | | Am25S05 | Am54S/74S181 |
| 4x4 | 35 | 2 | |
| 8x8 | 75 | 8 | |
| 12x12 | 115 | 18 | |
| 12x12 | 82 | 18 | 5 |
| 16x16 | 155 | 32 | |
| 16x16 | 111 | 32 | 7 |
| 16x16 | 98 | 32 | 16 |
| 20x20 | 195 | 50 | |
| 20x20 | 130 | 50 | 9 |
| 24x24 | 235 | 72 | |
| 24x24 | 149 | 72 | 11 |
| 24x24 | 125 | 72 | 24 |
| 28x28 | 275 | 98 | |
| 28x28 | 168 | 98 | 13 |
| 32x32 | 315 | 128 | |
| 32x32 | 187 | 128 | 15 |
| 32x32 | 152 | 128 | 32 |

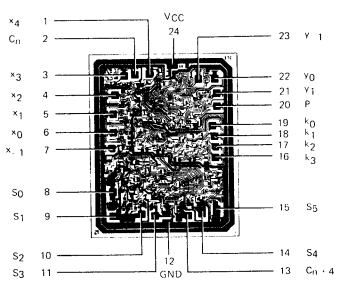

Am25S05

$Y = (y_{-1}\, y_0\, y_1)\, 2^A$

$X = (x_{-1}\, x_0\, x_1\, x_2\, x_3)\, 2^B$

Fig. 2

### Metallization and Pad Layout




DIE SIZE 0.088" X 0.110"

# Am25S07•Am25S08

## Hex/Quad Parallel D Registers With Register Enable

### Distinctive Characteristics

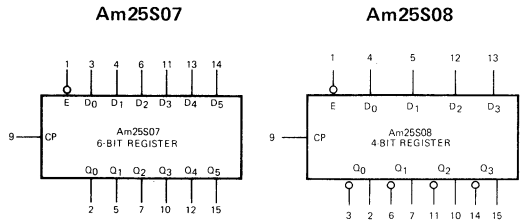
- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

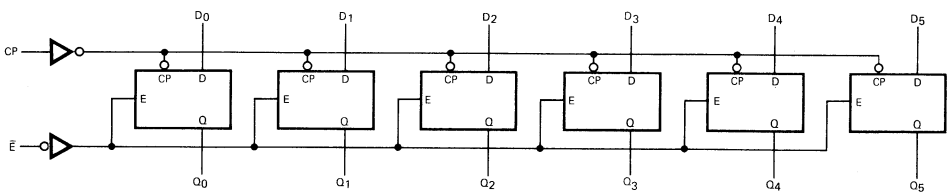
### LOGIC SYMBOLS



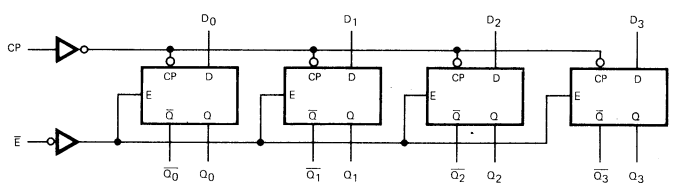

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

Am25S07




Am25S08

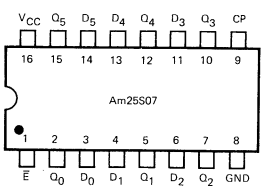



### ORDERING INFORMATION

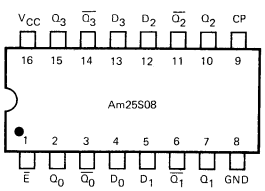
| Package Type | Temperature Range | Am25S07 Order Number | Am25S08 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM25S07PC | AM25S08PC |
| Hermetic DIP | 0°C to +70°C | AM25S07DC | AM25S08DC |
| Dice | 0°C to +70°C | AM25S07XC | AM25S08XC |
| Hermetic DIP | −55°C to +125°C | AM25S07DM | AM25S08DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25S07FM | AM25S08FM |
| Dice | −55°C to +125°C | AM25S07XM | AM25S08XM |

### CONNECTION DIAGRAMS
Top Views

Am25S07




Am25S08




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S07XC, Am25S08XC $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am25S07XM, Am25S08XM $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | XC | 2.7 | 3.4 | | Volts |
| | | | XM | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 5) | $V_{CC}$ = MAX. | S07 | | 90 | 144 | mA |
| | | | S08 | | 60 | 96 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | $V_{CC}$ = 5.0V, $C_L$ = 15pF, $R_L$ = 280Ω | 4 | 8 | 12 | ns |
| $t_{PHL}$ | Clock to Output | | 4 | 11.5 | 17 | ns |
| $t_{pw}$ | Clock Pulse Width | | 7 | | | ns |
| $t_s$ | Data | | 5.5 | | | ns |
| $t_s$ | Enable | | 9 | | | ns |
| $t_h$ | Data | | 3 | | | ns |
| $t_h$ | Enable | | 3 | | | ns |

## Am25S07 LOADING RULES (In STTL Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $\overline{E}$ | 1 | 1 | – | – |
| $Q_0$ | 2 | – | 20 | 10 |
| $D_0$ | 3 | 1 | – | – |
| $D_1$ | 4 | 1 | – | – |
| $Q_1$ | 5 | – | 20 | 10 |
| $D_2$ | 6 | 1 | – | – |
| $Q_2$ | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| CP | 9 | 1 | – | – |
| $Q_3$ | 10 | – | 20 | 10 |
| $D_3$ | 11 | 1 | – | – |
| $Q_4$ | 12 | – | 20 | 10 |
| $D_4$ | 13 | 1 | – | – |
| $D_5$ | 14 | 1 | – | – |
| $Q_5$ | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## Am25S08 LOADING RULES (In STTL Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $\overline{E}$ | 1 | 1 | – | – |
| $Q_0$ | 2 | – | 20 | 10 |
| $\overline{Q}_0$ | 3 | – | 20 | 10 |
| $D_0$ | 4 | 1 | – | – |
| $D_1$ | 5 | 1 | – | – |
| $\overline{Q}_1$ | 6 | – | 20 | 10 |
| $Q_1$ | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| CP | 9 | 1 | – | – |
| $Q_2$ | 10 | – | 20 | 10 |
| $\overline{Q}_2$ | 11 | – | 20 | 10 |
| $D_2$ | 12 | 1 | – | – |
| $D_3$ | 13 | 1 | – | – |
| $\overline{Q}_3$ | 14 | – | 20 | 10 |
| $Q_3$ | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

## DEFINITION OF FUNCTIONAL TERMS

$D_i$ The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the $D_i$ inputs is transferred to the $Q_i$ outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the $Q_i$ outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

$Q_i$ The TRUE register outputs.

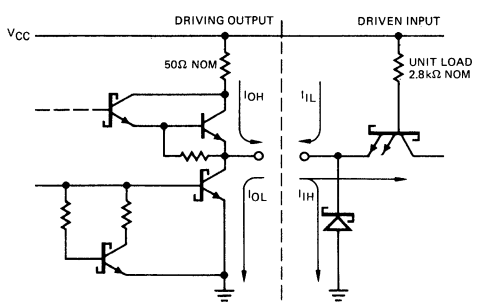
$\overline{Q}_i$ The complement register outputs

## FUNCTION TABLE

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{E}$ | $D_i$ | CP | $Q_i$ | $\overline{Q}_i$ |
| H | X | X | NC | NC |
| L | X | H | NC | NC |
| L | X | L | NC | NC |
| L | L | ↑ | L | H |
| L | H | ↑ | H | L |

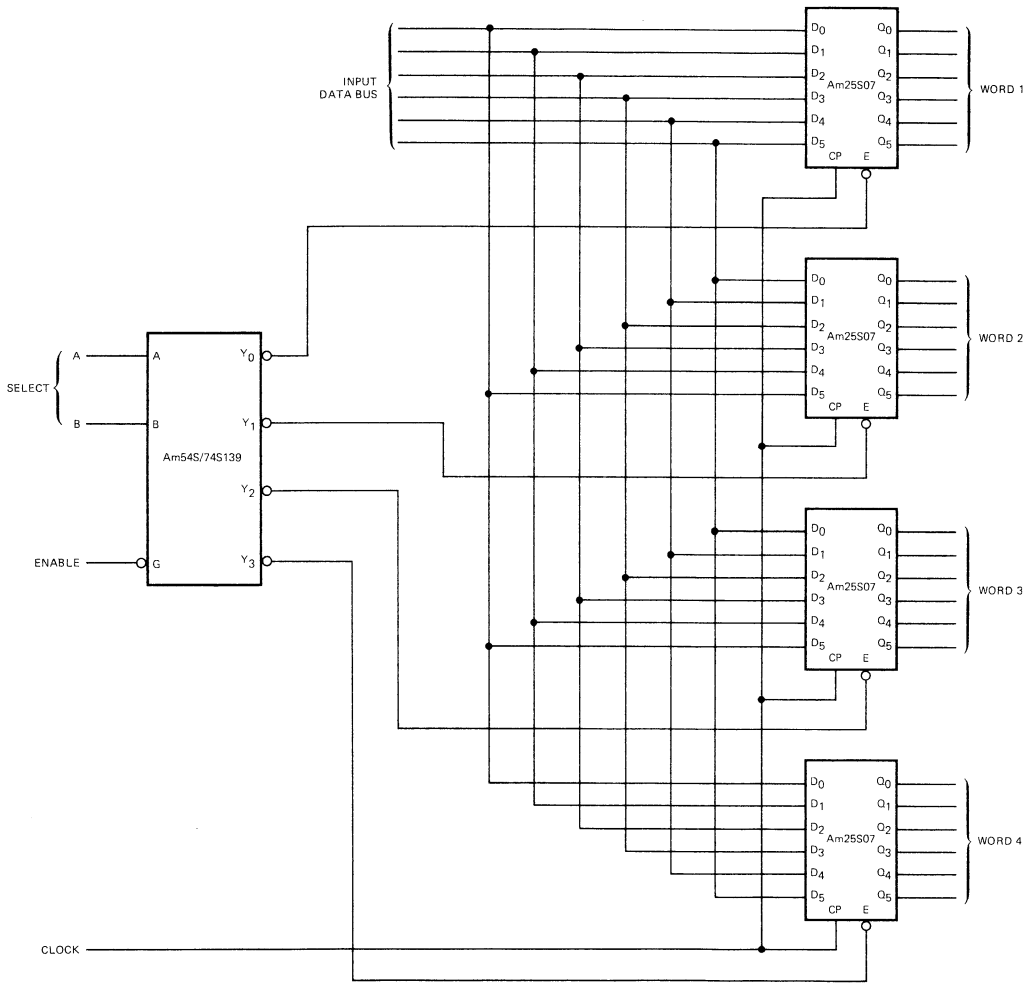
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

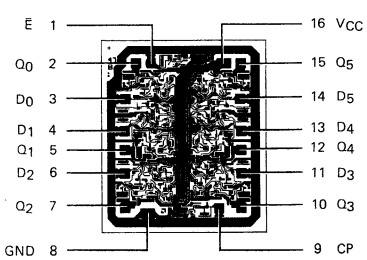
## APPLICATIONS




**Selective Register Loading of Data on Synchronous Clock.**

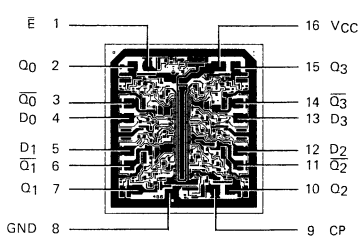
### Metallization and Pad Layout

**Am25S07**




DIE SIZE: 0.070" X 0.083"

**Am25S08**




DIE SIZE: 0.067" X 0.073"

# SCHOTTKY TTL MSI REGISTERS

By John R. Mick

## INTRODUCTION

There is a continual emphasis on higher and higher speed digital systems. Many TTL MSI functional blocks are now standard items and most high speed digital systems use large numbers of these devices for storage and control. With the advent of Schottky technology, the most popular of these functional storage and control blocks are now available at still higher speeds. In addition, several new, very useful variations of these products are available so that the digital systems designer now has a comprehensive set of register functions available for todays high speed designs.

## THE Am54S/74S194 AND Am54S/74S195 SHIFT REGISTERS

The logic diagrams of these advanced Schottky registers together with the logic symbol representing their logic function are shown in Figure 1. These devices are perhaps the most popular four bit shift registers and are useful for a variety of storage and control functions.

For both registers, the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW synchronous clear (CLR) which forces all outputs to the LOW state ($\overline{Q}_D$ HIGH) independent of any other inputs. All control inputs are buffered to present only one Schottky TTL load to the system, and all outputs can drive 10 Schottky loads in the LOW state and 20 in the HIGH state. Because all the flip-flops are D-type, they do not catch 0's or 1's, and the only requirements on any of the inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

The Am54S/74S194 shift register operates in four modes under control of the two select inputs, $S_0$ and $S_1$. The four

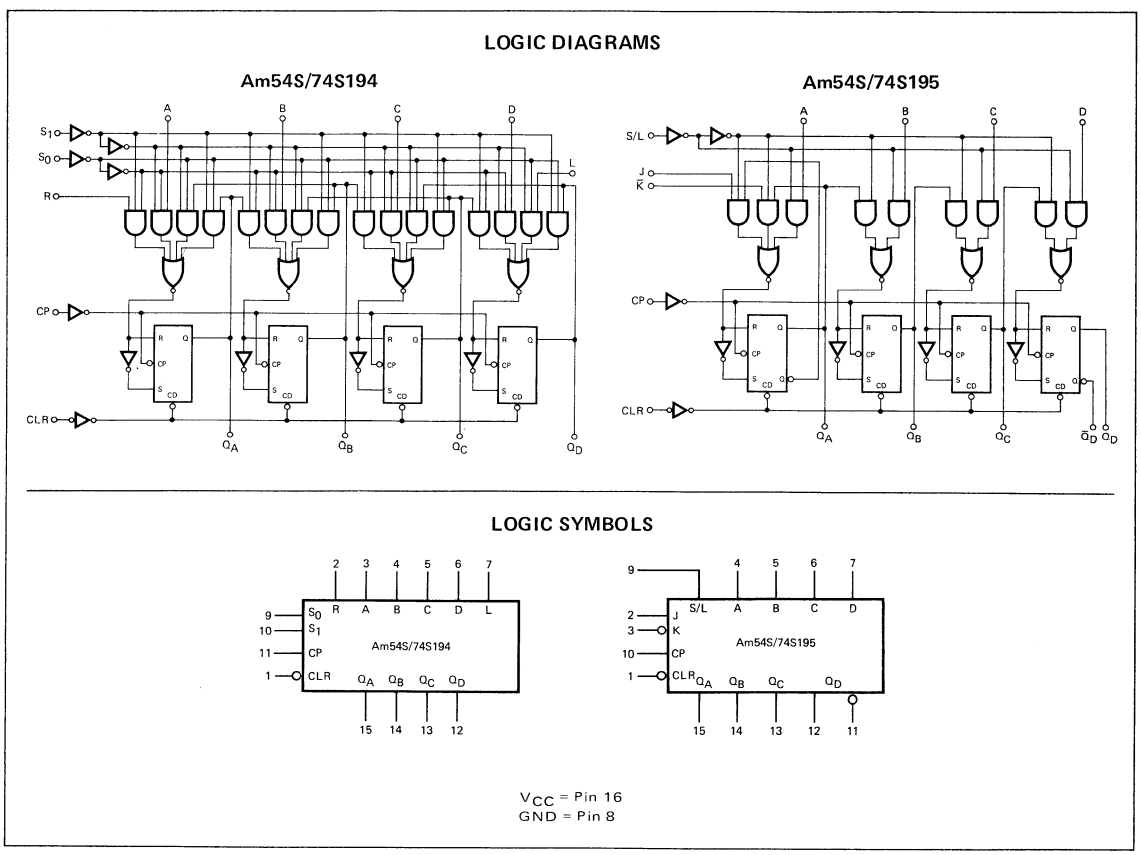



Figure 1. Logic Diagrams and Logic Symbols for the Am54S/74S194 and Am54S/74S195 Shift Registers.

modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the $Q_A$ bit input from R), shift left (data comes from the flip-flop to the right, with the $Q_D$ input from L), and hold or do nothing (each flip-flop receives data from its own output). It should be noted that on the Am54S/74S194 register there are *no restrictions* on the $S_0$ and $S_1$ select inputs when the clock is LOW as there are on the Am54/74194 shift register.

The Am54S/74S195 can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, $Q_A$, is loaded via the J and $\overline{K}$ inputs in the shift mode. The Function Tables for the Am54S/74S194 and Am54S/74S195 registers are shown in Figure 2.

### THE Am25S07 AND Am54S/74S174 SIX-BIT REGISTERS

The logic diagrams and logic symbols representing these 6-bit registers are shown in Figure 3. Both devices consist of six D-type positive edge triggered flip-flops with a buffered common clock. Each flip-flop has a separate D input and a separate Q output.

The Am54S/74S174 register has an asynchronous active-LOW buffered clear input. When the clear input is LOW, the Q outputs are LOW independent of the clock or D inputs.

The Am25S07 is similar to the Am54S/74S174 except the common clear input is replaced by a common active-LOW clock enable ($\overline{E}$). When the clock enable input is LOW, the data on the D inputs are stored in the register on the positive going edge of the clock. When the clock enable is HIGH, the register will not change state regardless of the clock or data inputs transitions.

This clock enable (or strobe) is extremely useful in many applications since it removes the necessity of gating the clock line of the register. Thus, the register can be controlled to enter data as required without additional clock propagation delay. There are no restrictions on this clock enable. The only requirement is that the clock enable input and data inputs meet the set-up and hold times with respect to the clock LOW-to-HIGH transition. The Function Tables for the Am54S/74S174 and Am25S07 registers are shown in Figure 4.

### THE Am25S08 AND Am54S/74S175 FOUR-BIT REGISTERS

The logic diagrams for these four-bit registers and the logic symbols representing them are shown in Figure 5. Both devices consist of four D-type positive edge triggered flip-flops with a buffered common clock. Each flip-flop has a separate D input and separate Q and $\overline{Q}$ outputs. Having both outputs available makes these registers particularly useful for general purpose decoding and control applications.

These devices are similar to the Am25S07 and Am54S/74S174 registers in that the Am25S08 has a buffered clock enable input and the Am54S/74S175 has an asynchronous active-LOW buffered clear input. The operation is similar to that described in the previous section and the Function Tables are as shown in Figure 4.

## FUNCTION TABLES

### Am54S/74S194

| FUNCTION | INPUTS: Clear | Mode: $S_1$ | Mode: $S_0$ | Clock | Serial: Left | Serial: Right | Parallel: A | Parallel: B | Parallel: C | Parallel: D | OUTPUTS: $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| No Change | H | X | X | L | X | X | X | X | X | X | NC | NC | NC | NC |
| | H | X | X | H | X | X | X | X | X | X | NC | NC | NC | NC |
| Parallel Load | H | H | H | ↑ | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| Shift Right | H | L | H | ↑ | X | L | X | X | X | X | L | $Q_A$ | $Q_B$ | $Q_C$ |
| | H | L | H | ↑ | X | H | X | X | X | X | H | $Q_A$ | $Q_B$ | $Q_C$ |
| Shift Left | H | H | L | ↑ | L | X | X | X | X | X | $Q_B$ | $Q_C$ | $Q_D$ | L |
| | H | H | L | ↑ | H | X | X | X | X | X | $Q_B$ | $Q_C$ | $Q_D$ | H |
| Hold | H | L | L | X | X | X | X | X | X | X | NC | NC | NC | NC |

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
$D_i$ = May be a HIGH or a LOW and the respective output will assume the same state.

### Am54S/74S195

| INPUTS: Clear | Shift/Load | Clock | Serial: J | Serial: $\overline{K}$ | Parallel: A | Parallel: B | Parallel: C | Parallel: D | OUTPUTS: $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | X | L | X | X | X | X | X | X | NC | NC | NC | NC | NC |
| H | X | H | X | X | X | X | X | X | NC | NC | NC | NC | NC |
| H | L | ↑ | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $\overline{D}_3$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_A$ | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_A$ | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |

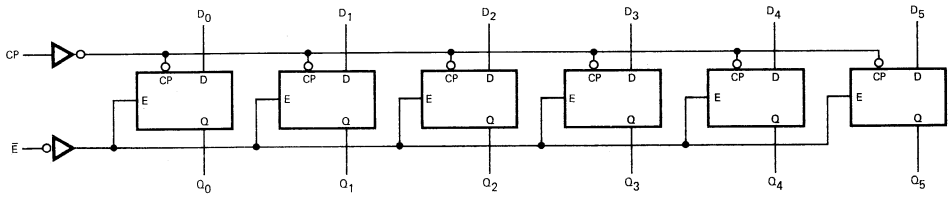
H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
$D_i$ = May be a HIGH or a LOW and the respective output will assume the same state.

Notes: 1. If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.
2. Linear feedback shift counters can be made by connecting the $Q_D$ and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

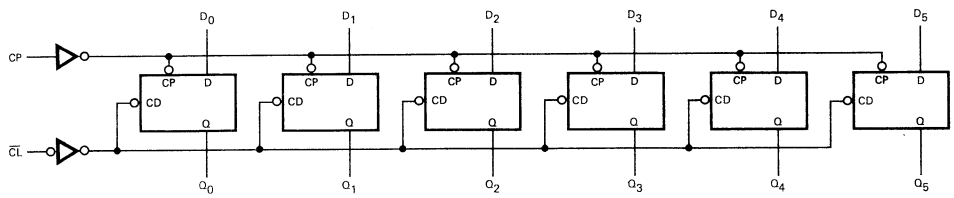
**Figure 2. Function Tables for the Am54S/74S194 and Am54S/74S195 Shift Registers.**

## LOGIC DIAGRAMS

### Am25S07




### Am54S/74S174




## LOGIC SYMBOLS

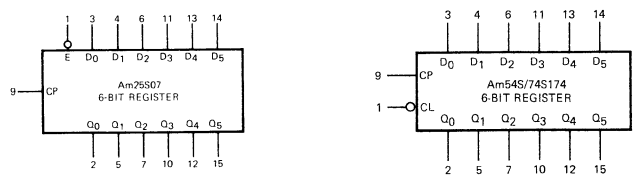



Figure 3. Logic Diagram and Logic Symbols for Am25S07 and Am54S/74S174 Registers.

## FUNCTION TABLES

### Am25S07, Am25S08

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{E}$ | $D_i$ | CP | $Q_i$ | $\overline{Q}_i$ |
| H | X | X | NC | NC |
| L | X | H | NC | NC |
| L | X | L | NC | NC |
| L | L | ↑ | L | H |
| L | H | ↑ | H | L |

H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

### Am54S/74S174, Am54S/74S175

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| Clear | Clock | $D_i$ | $Q_i$ | $\overline{Q}_i$ |
| L | X | X | L | H |
| H | L | X | NC | NC |
| H | H | X | NC | NC |
| H | ↑ | L | L | H |
| H | ↑ | H | H | L |

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH Transition
Note: $\overline{Q}_i$ on Am54S/74S175 only

Figure 4. Function Tables for Am25S07, Am25S08, Am54S/74S174 and Am54S/74S175 Registers.

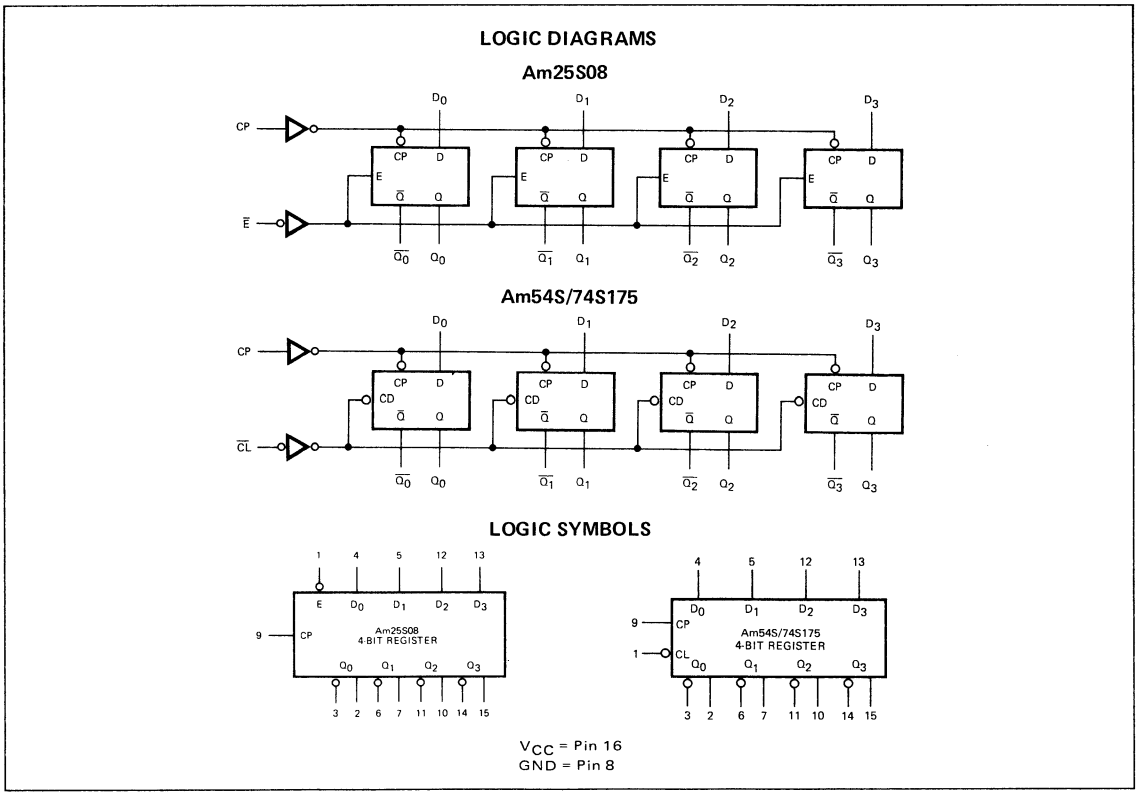



Figure 5. Logic Diagrams and Logic Symbols for Am25S08 and Am54S/74S175 Registers.

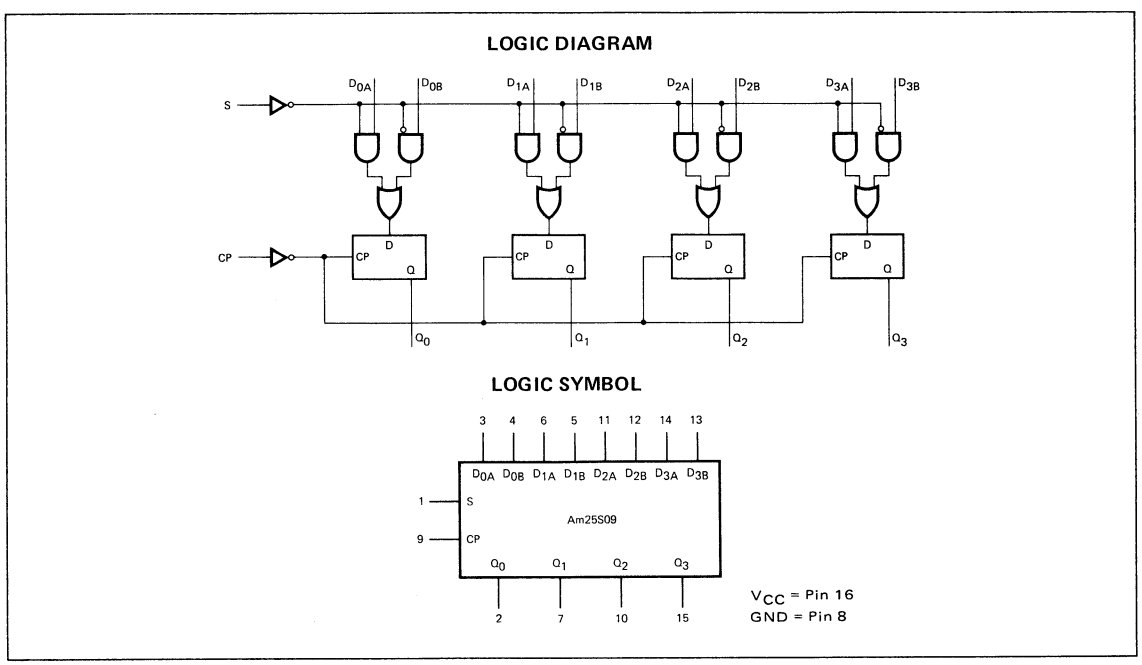



Figure 6. Logic Diagram and Logic Symbol for the Am25S09 Register.

## THE Am25S09 FOUR-BIT REGISTER

This device is a four-bit register that features a quad two input multiplexer at the input of the register. This allows data to be stored in the register from either of two different data inputs. The logic diagram and logic symbol for this device is shown in Figure 6.

The register consists of four D-type positive edge triggered flip-flops with a buffered common clock and a two-input multiplexer connected to the D input of each flip-flop. A buffered common select line, S, controls the state of the four multiplexers. When the S select input is LOW, the A input word will be stored in the register. When the S select input is HIGH, the B input word will be stored in the register as shown in the Function Table of Figure 7. This ability to select the register input from either of two data sources is particularly useful in many applications. The data from one of two sources may be programmed or perhaps an operate/manual test capability is performed.

## APPLICATIONS

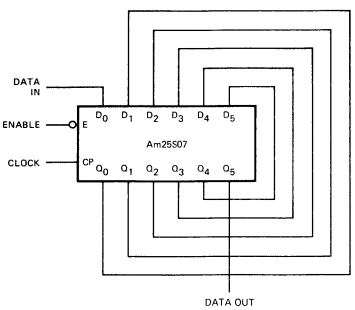
Applications for these registers are numerous. By having both four-bit and six-bit versions available, many general and special data storage applications are easily handled. Also, the registers with the clock enable input provide a unique capability for many high-speed synchronous systems. With so many Schottky TTL registers available, the digital designer now has the right register for each data storage application. Applications for the registers previously described are shown on the remaining pages.

**FUNCTION TABLE**

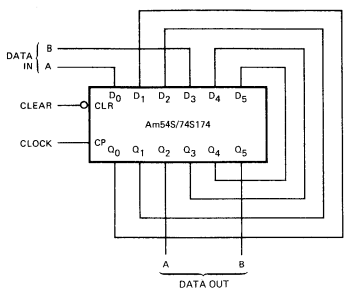
| SELECT S | CLOCK CP | DATA $D_{iA}$ | INPUTS $D_{iB}$ | OUTPUT $Q_i$ |
|---|---|---|---|---|
| L | ↑ | L | X | L |
| L | ↑ | H | X | H |
| H | ↑ | X | L | L |
| H | ↑ | X | H | H |

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

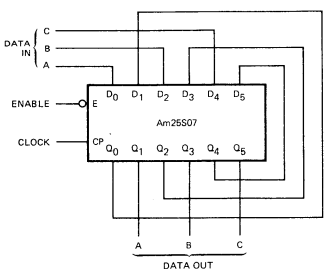
**Figure 7. Function Table for the Am25S09 Register.**



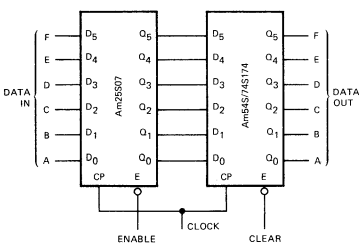

**Six-Bit Shift Register with Clock Enable.**




**Dual Three-Bit Shift Register with Clear.**



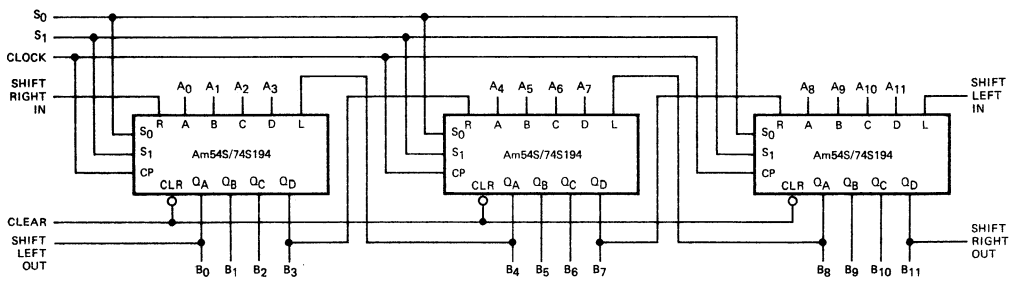

**Triple Two-Bit Register with Clock Enable.**




**Two-Word Six-Bit Register with Clock Enable Load on the First Word and a Clear on the Second Word.**

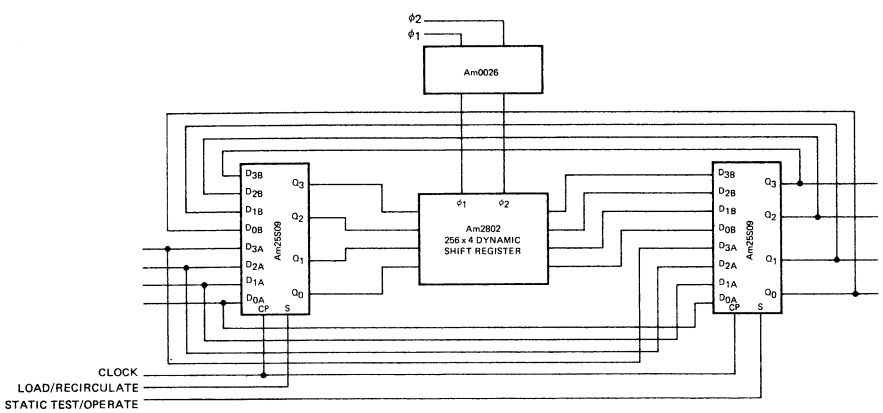
One useful but often overlooked application for the Am25S07 and Am54S/74S174 is in a shift register connection with the output of one register stage acting as the input of the next register stage. Shift right (or left) connections for these devices are shown. If the Am25S08 or Am54S/74S175 four-bit registers are connected in a similar fashion, both the true and complement outputs are available. This is especially useful in some decoder applications.

**Figure 8. D-Type Registers Connected for Shifting.**



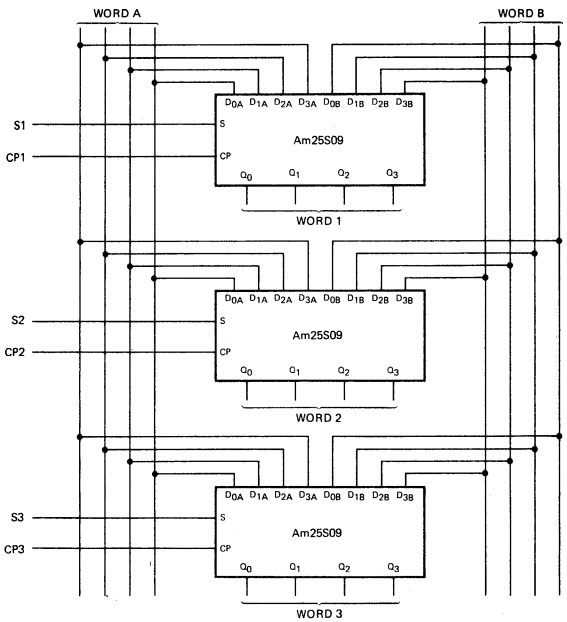

The normal shift register connection for long words using the Am54S/74S194 features shift-right, shift-left, parallel load or hold data modes. It can be connected to circulate data in either direction or shift in 0's or 1's at either end. The Am54S/74S195 is connected in a similar fashion, however, the device can shift data in only one direction. Although the Am54S/74S195 is called a shift-right register, it can be used to shift data left by relabeling the shift and parallel inputs and the Q outputs.

**Figure 9. Connecting the Am54S/74S194 Shift Register for Longer Words.**



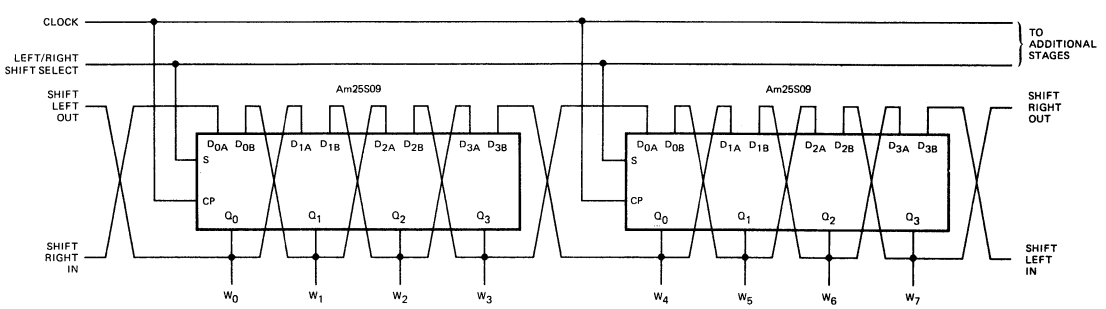

The Am25S09 can be used in a 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes. MOS interface is one STTL unit load at each end. The required pull-up and pull-down resistors are not shown.

**Figure 10. Using the Am25S09 with Dynamic Shift Registers.**



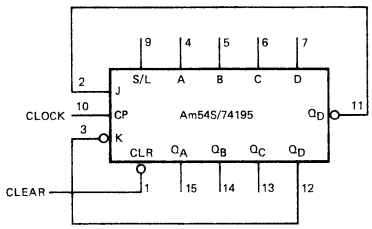

The Am25S09 used to store a word from either data bus A or data bus B.

**Figure 11. Selective Bus Storage with the Am25S09 Register.**




The Am25S09 can be used as a shift-left, shift-right register under control of a single select input. This connection can also be used as a clocked last-in, first-out (LIFO) memory. The output data is available in either serial or parallel form.

**Figure 12. The Am25S09 as a LIFO Memory.**




**NORMAL DEFINITIONS**

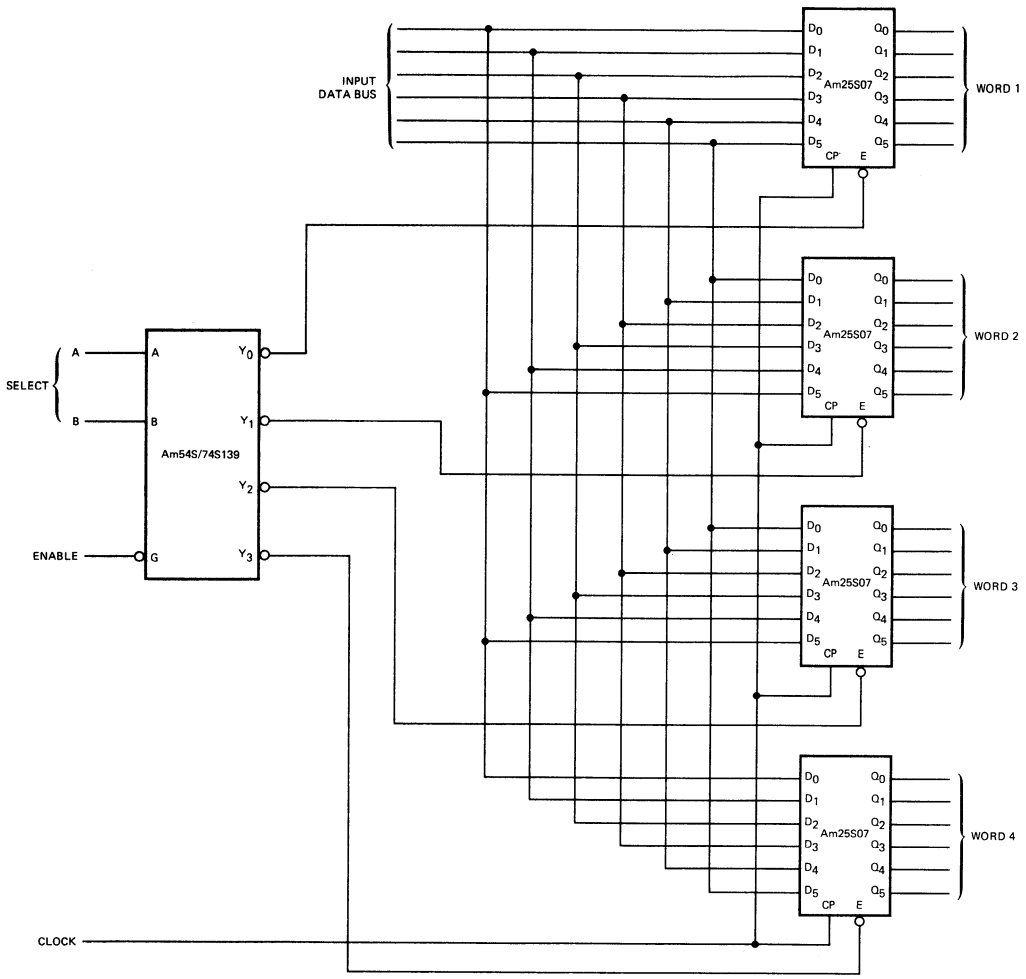
| PIN NO. | | | | Decimal |
|---|---|---|---|---|
| 12 | 13 | 14 | 15 | |
| $2^3$ | $2^2$ | $2^1$ | $2^0$ | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 0 | 0 | 4 |
| 1 | 0 | 0 | 1 | 9 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 1 | 0 | 6 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 0 | 1 | 1 | 11 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 0 | 0 | 0 |

**ALTERNATE DEFINITIONS**

| PIN NO. | | | | Decimal |
|---|---|---|---|---|
| 12 | 13 | 14 | 15 | |
| $2^0$ | $2^1$ | $2^2$ | $2^3$ | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 8 |
| 0 | 0 | 1 | 0 | 4 |
| 0 | 1 | 0 | 1 | 10 |
| 1 | 0 | 1 | 0 | 5 |
| 0 | 1 | 0 | 0 | 2 |
| 1 | 0 | 0 | 1 | 9 |
| 0 | 0 | 1 | 1 | 12 |
| 0 | 1 | 1 | 0 | 6 |
| 1 | 1 | 0 | 1 | 11 |
| 1 | 0 | 1 | 1 | 13 |
| 0 | 1 | 1 | 1 | 14 |
| 1 | 1 | 1 | 0 | 7 |
| 1 | 1 | 0 | 0 | 3 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

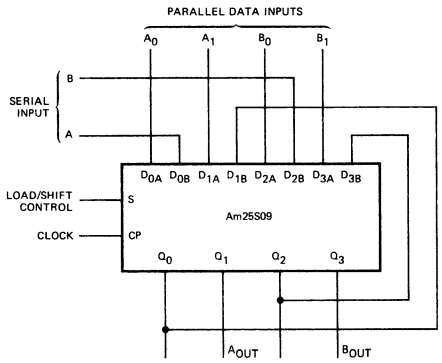
A high-speed modulo 15 linear feedback shift register takes advantage of the J and $\overline{K}$ inputs on the Am54S/74S195. The "decimal" sequence is determined by the weight assigned to the output pins and many alternate definitions are possible. Registers of longer length can be built by cascading additional Am54S/74S195's. Binary state 15 (all 1's) is not self-correcting. The clear or parallel load should be used to initialize the register.

**Figure 13. Pseudo-Random Feedback Registers.**



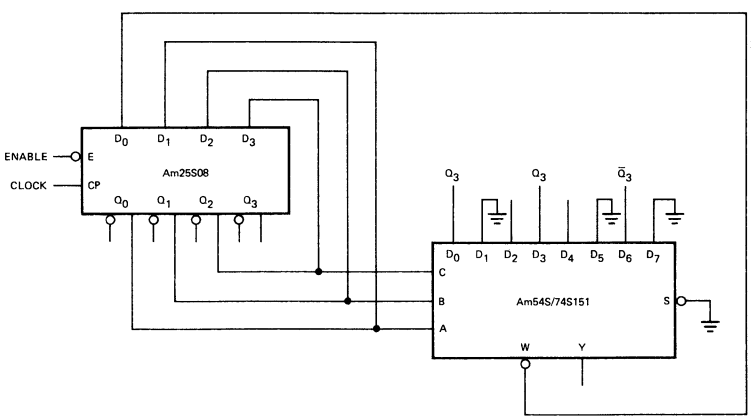

The clock enable on the Am25S07 or Am25S08 can be used to perform selective register loading from a common data bus. One-half of an Am54S/74S139 dual one-of-four decoder provides the select signals as controlled by the two-bit select field (A and B). The enable input (G) on the Am54S/74S139 can be used to inhibit loading of any of the four registers.

**Figure 14. Selecting Data for One Register.**




Often a need occurs to delay one or two signals by a few clock cycles. This example shows the Am25S09 providing two clock delays for two input data paths. In addition, a parallel preset (or clear) is available via the load/shift control for initialization. Also, the data delayed by one clock cycle is available if needed.

**Figure 15. Dual Two-Bit Right-Shift Register with Full Parallel Load.**

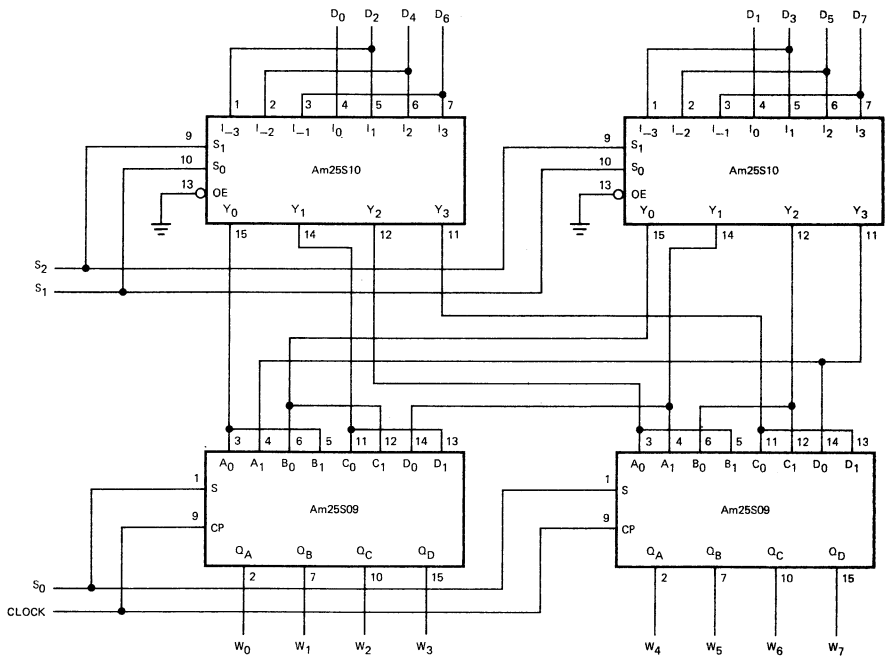



**FUNCTION TABLE**

| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | $D_0$ | Mplx. State | Mplx. Input |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | $Q_3$ |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 3 | $Q_3$ |
| 0 | 1 | 1 | 1 | 0 | 7 | 0 |
| 1 | 1 | 1 | 0 | 1 | 6 | $\overline{Q}_3$ |
| 1 | 1 | 0 | 1 | 1 | 5 | 0 |
| 1 | 0 | 1 | 1 | 0 | 3 | $Q_3$ |
| 0 | 1 | 1 | 0 | 0 | 6 | $\overline{Q}_3$ |
| 1 | 1 | 0 | 0 | 0 | 4 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | $Q_3$ |
| 0 | 0 | 0 | 0 | 1 | 0 | $Q_3$ |

The Am25S08 is shown combined with an Am54S/74S151 eight-input multiplexer to build a 4-bit shift counter. This technique provides the ability to design many unique codes. By using the Am54S/74S251 eight-input multiplexer with three state outputs, the same register can be used with interchangeable codes depending on which multiplexer output is enabled. The Am54S/74S195 can also be very useful in this application since both the $Q_D$ and $\overline{Q}_D$ outputs are available and the J and $\overline{K}$ inputs can be tied to the multiplexer output to provide a D-type input. This device offers a direct clear as well as a parallel load for initialization to any counter state. However, the true and complement outputs are not available with the Am54S/74S195.

**Figure 16. Shift Register Generates Unique Counting Codes.**

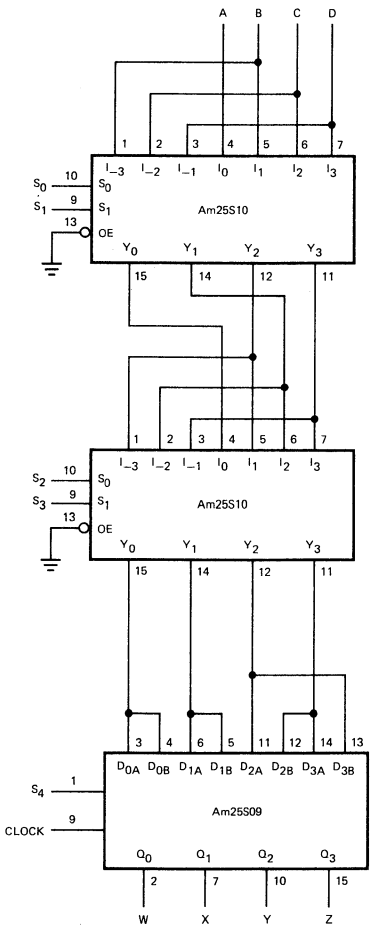



**FUNCTION TABLE**

| $S_2$ $S_1$ $S_0$ | $W_0$ | $W_1$ | $W_2$ | $W_3$ | $W_4$ | $W_5$ | $W_6$ | $W_7$ |
|---|---|---|---|---|---|---|---|---|
| 0 0 0 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
| 0 0 1 | $D_7$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ |
| 0 1 0 | $D_6$ | $D_7$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ |
| 0 1 1 | $D_5$ | $D_6$ | $D_7$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ |
| 1 0 0 | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| 1 0 1 | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_0$ | $D_1$ | $D_2$ |
| 1 1 0 | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_0$ | $D_1$ |
| 1 1 1 | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_0$ |

Two Am25S09 registers with the two input multiplexer can be used in conjunction with two Am25S10 four-bit shifters to implement an eight-bit full end around shifter (barrel shifter) with storage. The Function Table shows the data rotation for the various three-bit select field states.

**Figure 17. Eight-Bit Full End Around Shift with Storage.**

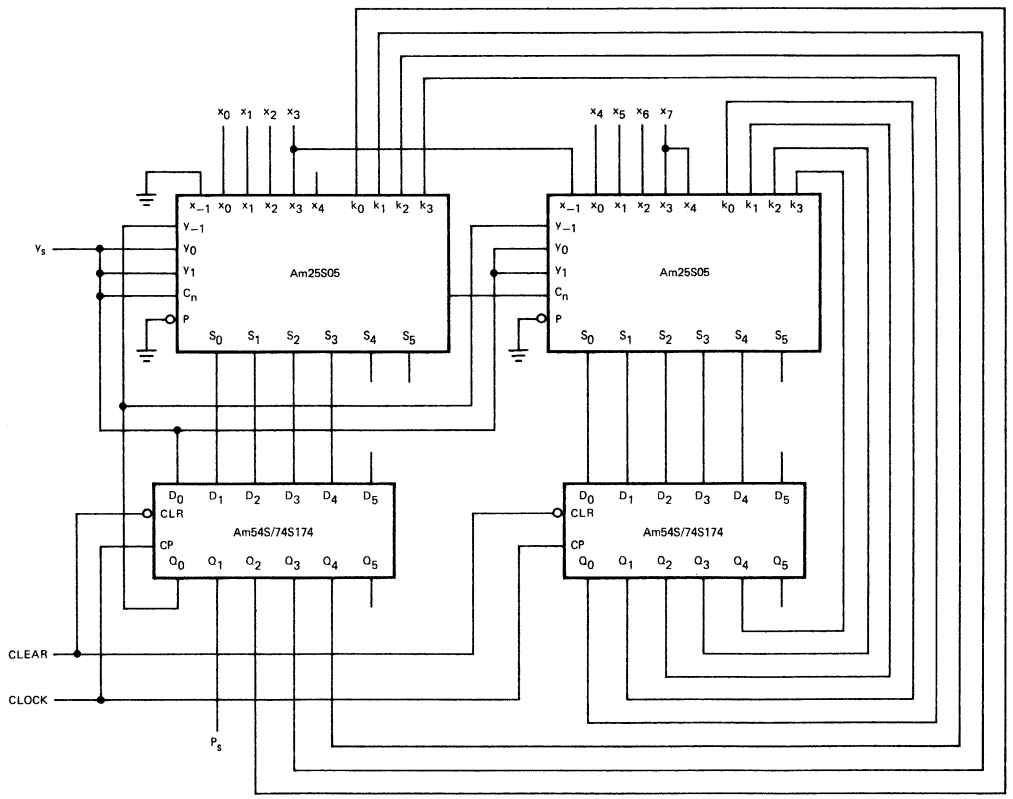



**FUNCTION TABLE**

| State Number | Select $S_4$ | $S_3$ | $S_2$ | $S_1$ | $S_0$ | Output W | X | Y | Z |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | A | C | B | D |
| 1 | 0 | 0 | 0 | 0 | 1 | D | B | A | C |
| 2 | 0 | 0 | 0 | 1 | 0 | C | A | D | B |
| 3 | 0 | 0 | 0 | 1 | 1 | B | D | C | A |
| 4 | 0 | 0 | 1 | 0 | 0 | D | A | C | B |
| 5 | 0 | 0 | 1 | 0 | 1 | C | D | B | A |
| 6 | 0 | 0 | 1 | 1 | 0 | B | C | A | D |
| 7 | 0 | 0 | 1 | 1 | 1 | A | B | D | C |
| 8 | 0 | 1 | 0 | 0 | 0 | B | D | A | C |
| 9 | 0 | 1 | 0 | 0 | 1 | A | C | D | B |
| 10 | 0 | 1 | 0 | 1 | 0 | D | B | C | A |
| 11 | 0 | 1 | 0 | 1 | 1 | C | A | B | D |
| 12 | 0 | 1 | 1 | 0 | 0 | C | B | D | A |
| 13 | 0 | 1 | 1 | 0 | 1 | B | A | C | D |
| 14 | 0 | 1 | 1 | 1 | 0 | A | D | B | C |
| 15 | 0 | 1 | 1 | 1 | 1 | D | C | A | B |
| 16 | 1 | 0 | 0 | 0 | 0 | State 9 | | | |
| 17 | 1 | 0 | 0 | 0 | 1 | State 10 | | | |
| 18 | 1 | 0 | 0 | 1 | 0 | State 11 | | | |
| 19 | 1 | 0 | 0 | 1 | 1 | State 8 | | | |
| 20 | 1 | 0 | 1 | 0 | 0 | D | A | B | C |
| 21 | 1 | 0 | 1 | 0 | 1 | C | D | A | B |
| 22 | 1 | 0 | 1 | 1 | 0 | B | C | D | A |
| 23 | 1 | 0 | 1 | 1 | 1 | A | B | C | D |
| 24 | 1 | 1 | 0 | 0 | 0 | State 3 | | | |
| 25 | 1 | 1 | 0 | 0 | 1 | State 0 | | | |
| 26 | 1 | 1 | 0 | 1 | 0 | State 1 | | | |
| 27 | 1 | 1 | 0 | 1 | 1 | State 2 | | | |
| 28 | 1 | 1 | 1 | 0 | 0 | C | B | A | D |
| 29 | 1 | 1 | 1 | 0 | 1 | B | A | D | C |
| 30 | 1 | 1 | 1 | 1 | 0 | A | D | C | B |
| 31 | 1 | 1 | 1 | 1 | 1 | D | C | B | A |

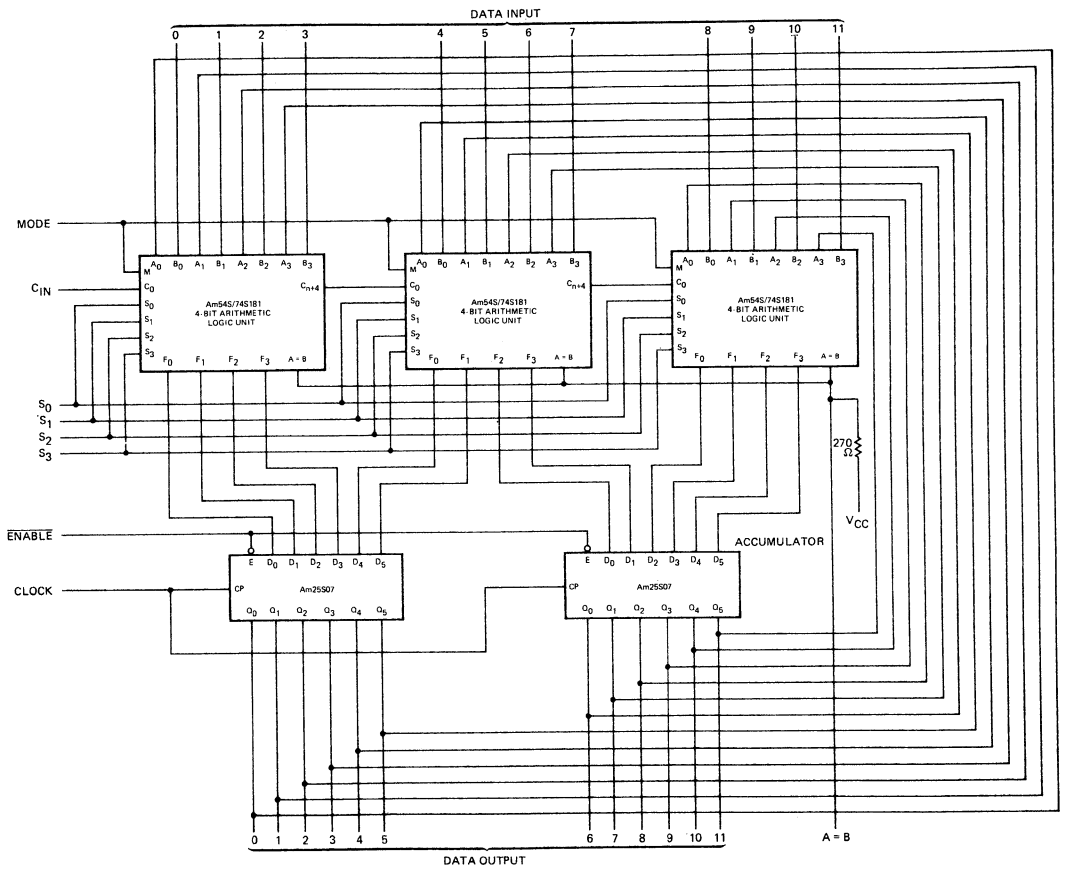
Two Am25S10 four-bit shifters are used in conjunction with an Am25S09 register to perform all possible permutations on four inputs. The number of combinations possible on n items is given as n!. Thus, for n equal to 4, 24 combinations are possible. The Function Table shows all 32 combinations of the 5-bit select code including the 8 redundant states. The four outputs are stored via the Am25S09 register. This connection can be particularly useful in security systems and certain random number generation schemes. The eight redundant states can be placed at other select field locations through proper design.

**Figure 18. Perform all Permutations on Four Inputs.**



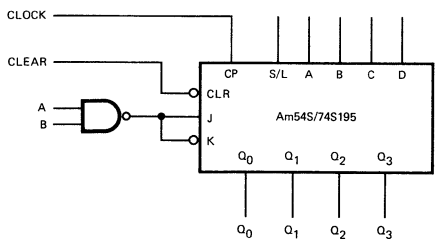

The Am54S/74S174 register is used to hold the running partial product of an 8-bit serial-parallel 2's complement multiplier. The Am25S05 2's complement multiplier provides the combinatorial logic of Booth's algorithm. This connection multiplies a parallel X word by a serial Y word (LSB first) to give a resultant serial product word P (LSB first). If the entire product is to be taken in serial form, the Y input sign bit must be extended for the total number of clock cycles. For example, an 8-bit X multiplied by an 8-bit Y requires 16 clock cycles and the Y's sign must be extended for the last eight clock cycles.

**Figure 19. Serial-Parallel Multiplication.**




The clock enable feature of the Am25S07 can be used to advantage in a high-speed arithmetic logic accumulator. Clearing is accomplished via one of the 16 select states of the Am54S/74S181.

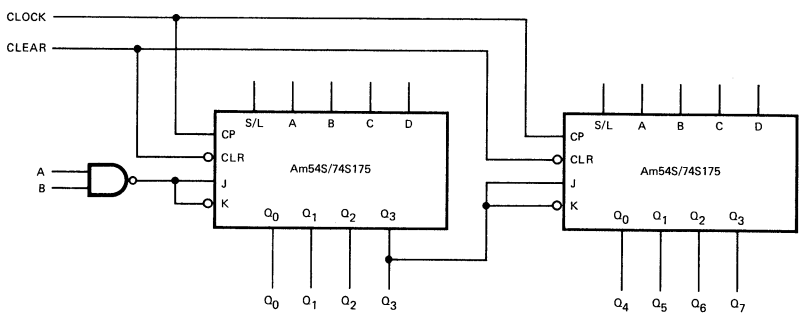
**Figure 20. High-Speed Arithmetic Accumulator.**




**FUNCTION TABLE**

| Divide By | Input A | Input B | Output |
|---|---|---|---|
| 2 | $Q_0$ | H | $Q_0$ |
| 3 | $Q_0$ | $Q_1$ | $Q_1$ |
| 4 | $Q_1$ | H | $Q_1$ |
| 5 | $Q_1$ | $Q_2$ | $Q_2$ |
| 6 | $Q_2$ | H | $Q_2$ |
| 7 | $Q_2$ | $Q_3$ | $Q_3$ |
| 8 | $Q_3$ | H | $Q_3$ |

H = HIGH



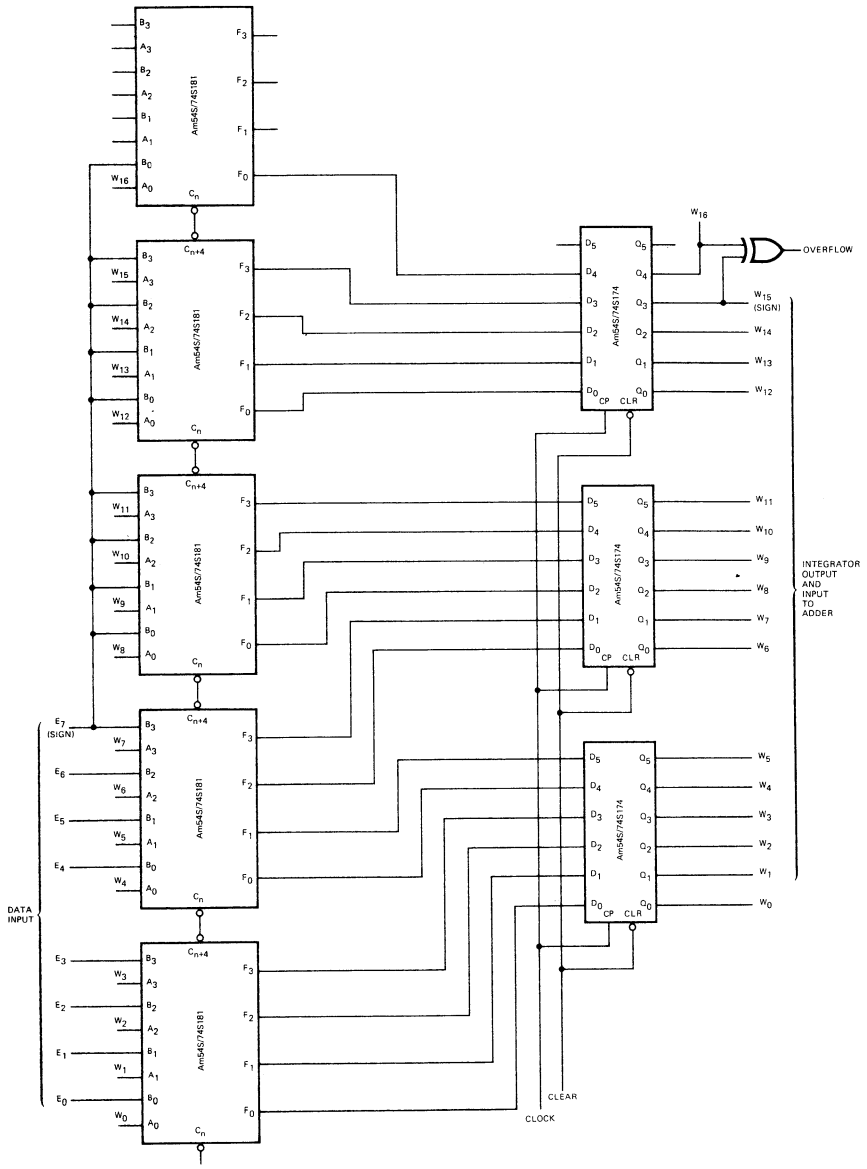

**FUNCTION TABLE**

| Divide By | Input A | Input B | Output |
|---|---|---|---|
| 9 | $Q_3$ | $Q_4$ | $Q_4$ |
| 10 | $Q_4$ | H | $Q_4$ |
| 11 | $Q_4$ | $Q_5$ | $Q_5$ |
| 12 | $Q_5$ | H | $Q_5$ |
| 13 | $Q_5$ | $Q_6$ | $Q_6$ |
| 14 | $Q_6$ | H | $Q_6$ |
| 15 | $Q_6$ | $Q_7$ | $Q_7$ |
| 16 | $Q_7$ | H | $Q_7$ |

H = HIGH

The Am54S/74S195 shift register can be used in conjunction with one two input NAND gate to form a divider chain of any length. The output waveform will be approximately a 50% duty cycle. One shift register can be used to cover the range of ÷ 2 through ÷ 8. Using two shift registers, the range of ÷ 9 through ÷ 16 is covered. If three shift registers are used, the range of ÷ 17 through ÷ 24 is possible; and so forth.

**Figure 21. Shift Register Counter of any Length.**




**Am54S/74S181 in Add Mode.**

The Am54S/74S174 can be used as the accumulator register in a high-speed digital integrator. The data input is an 8-bit two's complement number while the data output is a 16-bit two's complement number. Provision is made to detect integrator overflow. The DC gain of the integrator for a single input sample is $\frac{1}{256}$. Thus, the transfer function of this integrator is given as

$$W = \sum_{n=0}^{\infty} \frac{E_n}{256}$$

A typical application for such an integrator is to smooth a video signal. For example, a bipolar analog signal is converted to an eight-bit 2's complement representation, via an A/D converter, passed through the integrator, and then reconverted to an analog signal via a D/A converter.

**Figure 22. Digital Integrator.**

# Am25S09

## Quad Two-Input, High-Speed Register

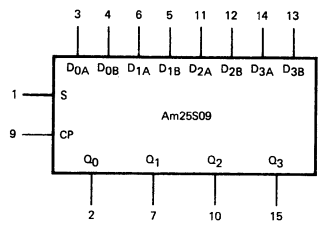
### Distinctive Characteristics

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge triggered clock action
- High-speed Schottky technology.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

### FUNCTIONAL DESCRIPTION

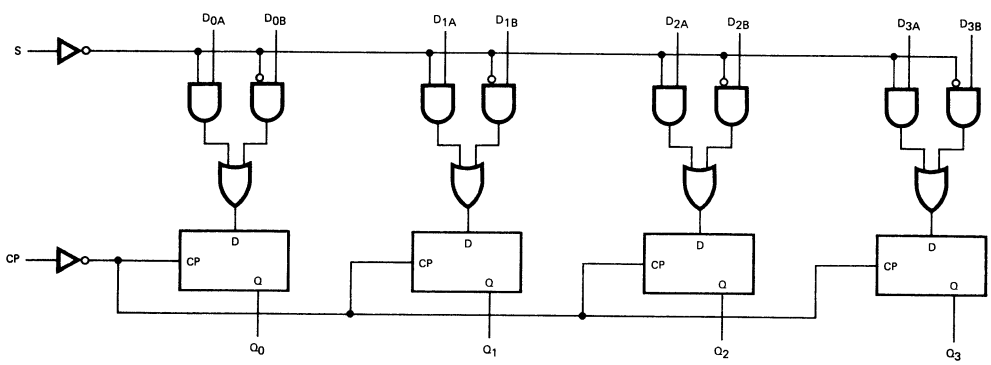
The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the $D_{iA}$ input data will be stored in the register. When the S input is HIGH, the $D_{iB}$ input data will be stored in the register.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

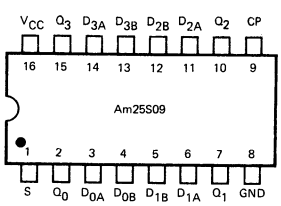
### LOGIC DIAGRAM




### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25S09PC |
| Hermetic DIP | 0°C to +70°C | AM25S09DC |
| Dice | 0°C to +70°C | AM25S09XC |
| Hermetic DIP | −55°C to +125°C | AM25S09DM |
| Hermetic Flat Pak | −55°C to +125°C | AM25S09FM |
| Dice | −55°C to +125°C | AM25S09XM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am25S09XC | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% (COM'L) | MIN. = 4.75 V | MAX. = 5.25 V |
| Am25S09XM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% (MIL) | MIN. = 4.5 V | MAX. = 5.5 V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L | 2.7 | 3.4 | | Volts |
| | | | MIL | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.3 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2.0 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | 75 | 120 | mA |

Notes:
1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Q HIGH | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| $t_{PHL}$ | Clock to Q LOW | | | 11.5 | 17 | ns |
| $t_{pw}$ | Clock Pulse Width | | 7 | | | ns |
| $t_s$ | Data Set-up Time | | 5.5 | | | ns |
| $t_s$ | Select Input Set-up Time | | 10 | | | ns |
| $t_h$ | Data Hold Time | | 3 | | | ns |
| $t_h$ | Select Input Hold Time | | 3 | | | ns |

## FUNCTION TABLE

| SELECT S | CLOCK CP | DATA $D_{iA}$ | INPUTS $D_{iB}$ | OUTPUT $Q_i$ |
|---|---|---|---|---|
| L | ↑ | L | X | L |
| L | ↑ | H | X | H |
| H | ↑ | X | L | L |
| H | ↑ | X | H | H |

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

L = LOW Voltage Level
i = 0, 1, 2, or 3

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| S | 1 | 1 | – | – |
| $Q_0$ | 2 | – | 20 | 10 |
| $D_{0A}$ | 3 | 1 | – | – |
| $D_{0B}$ | 4 | 1 | – | – |
| $D_{1B}$ | 5 | 1 | – | – |
| $D_{1A}$ | 6 | 1 | – | – |
| $Q_1$ | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| CP | 9 | 1 | – | – |
| $Q_2$ | 10 | – | 20 | 10 |
| $D_{2A}$ | 11 | 1 | – | – |
| $D_{2B}$ | 12 | 1 | – | – |
| $D_{3B}$ | 13 | 1 | – | – |
| $D_{3A}$ | 14 | 1 | – | – |
| $Q_3$ | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and −2.0 mA measured at 0.5 V LOW.

## DEFINITION OF FUNCTIONAL TERMS

$D_{0A}$, $D_{1A}$, $D_{2A}$, $D_{3A}$ The "A" word into the two-input multiplexer of the D flip-flops.

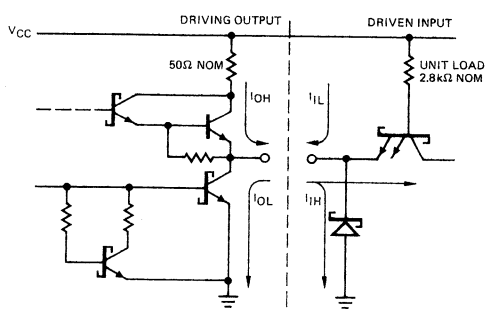
$D_{0B}$, $D_{1B}$, $D_{2B}$, $D_{3B}$ The "B" word into the two-input multiplexer of the D flip-flops.

$Q_0$, $Q_1$, $Q_2$, $Q_3$ The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

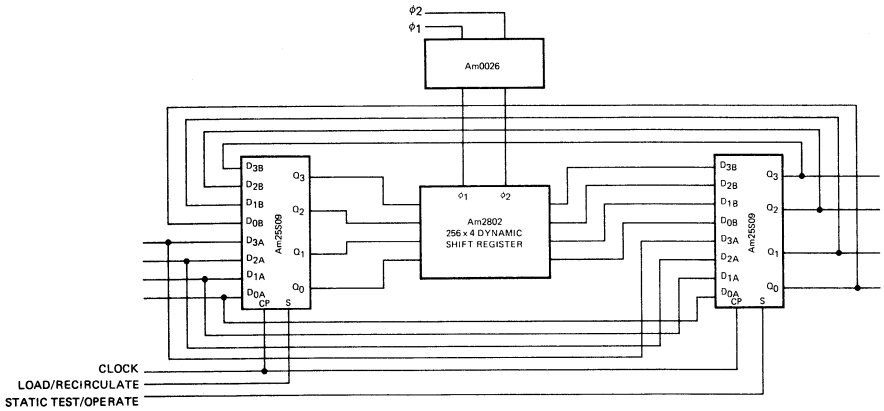
CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

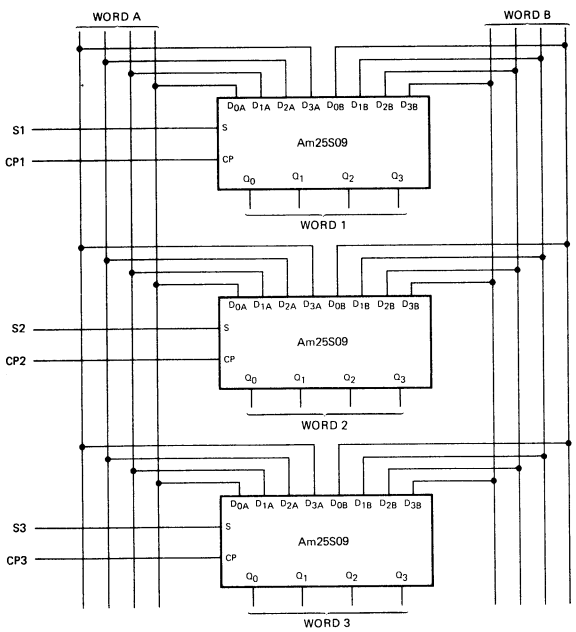



Note: Actual current flow direction shown

## APPLICATIONS

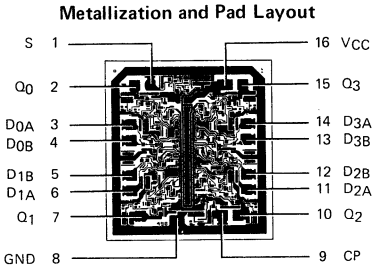



Am25S09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.




Am25S09 used to store a word from either data bus A or data bus B.

### Metallization and Pad Layout




DIE SIZE: 0.067" X 0.073"

# Am25S10

## Four-Bit Shifter With Three-State Outputs

### Distinctive Characteristics

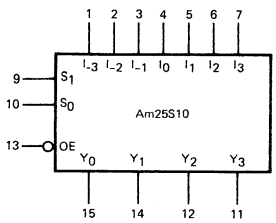
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5 ns typical data propagation delay
- Alternate source is 54S/74S350
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field $S_0$ and $S_1$. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

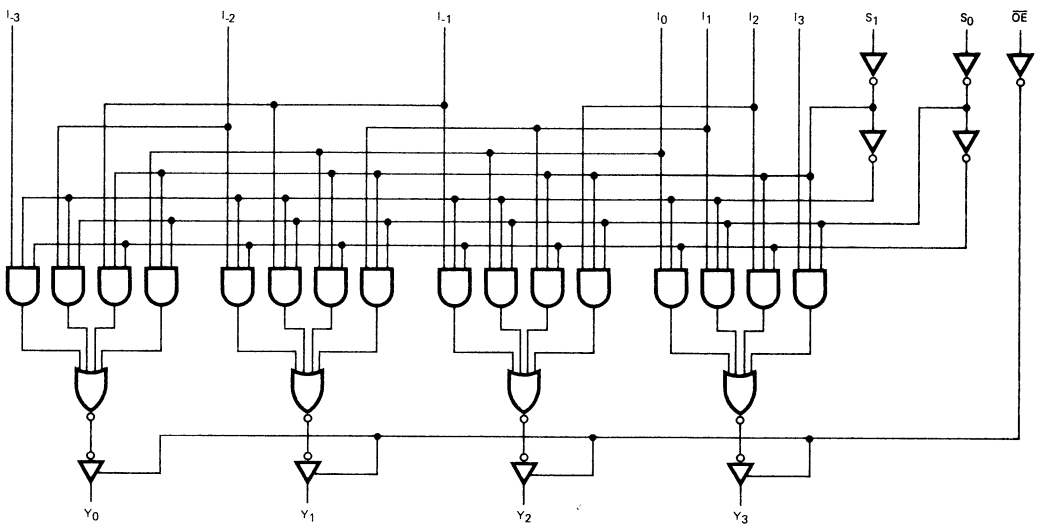
By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

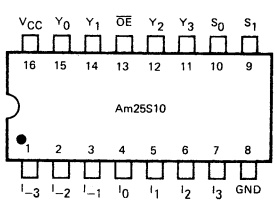
### LOGIC DIAGRAM




### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25S10PC |
| Hermetic DIP | 0°C to +70°C | AM25S10DC |
| Dice | 0°C to +70°C | AM25S10XC |
| Hermetic DIP | -55°C to +125°C | AM25S10DM |
| Hermetic Flat Pak | -55°C to +125°C | AM25S10FM |
| Dice | -55°C to +125°C | AM25S10XM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am25S10XC | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% (COM'L) | MIN. = 4.75 V | MAX. = 5.25 V |
| Am25S10XM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% (MIL) | MIN. = 4.5 V | MAX. = 5.5 V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | XM $I_{OH}$ = −2mA | 2.4 | 3.4 | | Volts |
| | | | XC $I_{OH}$ = −6.5mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2.0 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | µA |
| $I_O$ | Off State (High Impedance) Output Current | $V_{CC}$ = MAX. | $V_O$ = 2.4 V | | | 50 | µA |
| | | | $V_O$ = 0.5 V | | | −50 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., All outputs open, All inputs = GND | | | 60 | 85 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data Input to Output | $V_{CC}$ = 5.0 V, $C_L$ = 15pF, $R_L$ = 280Ω | | 5 | 7.5 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | Select to Output | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | 13 | 20 | |
| $t_{ZH}$ | Output Control $\overline{OE}$ to Output | | | | 19.5 | ns |
| $t_{ZL}$ | | | | | 21 | |
| $t_{HZ}$ | Output Control $\overline{OE}$ to Output | $V_{CC}$ = 5 V, $C_L$ = 5pF, $R_L$ = 280Ω | | 5 | 8 | ns |
| $t_{LZ}$ | | | | 10 | 15 | |

## DEFINITION OF FUNCTIONAL TERMS

$I_i$ The seven data inputs of the shifter.

$\overline{OE}$ Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected $I_i$ inputs are present at the outputs.

$S_0$, $S_1$ Select inputs. Controls the number of places the inputs are shifted.

$Y_i$ The four outputs of the shifter.

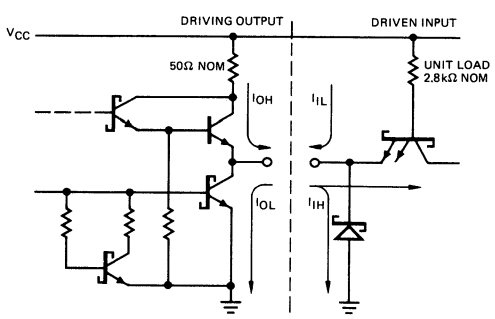
## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load (Note 1) | Fan-out Output HIGH XM | Fan-out Output HIGH XC | Fan-out Output LOW |
|---|---|---|---|---|---|
| $I_{-3}$ | 1 | 1 | – | – | – |
| $I_{-2}$ | 2 | 1.5 | – | – | – |
| $I_{-1}$ | 3 | 1.5 | – | – | – |
| $I_0$ | 4 | 1.5 | – | – | – |
| $I_1$ | 5 | 1.5 | – | – | – |
| $I_2$ | 6 | 1.5 | – | – | – |
| $I_3$ | 7 | 1 | – | – | – |
| GND | 8 | – | – | – | – |
| $S_1$ | 9 | 1 | – | – | – |
| $S_0$ | 10 | 1 | – | – | – |
| $Y_3$ | 11 | – | 40 | 130 | 10 |
| $Y_2$ | 12 | – | 40 | 130 | 10 |
| $\overline{OE}$ | 13 | 1 | – | – | – |
| $Y_1$ | 14 | – | 40 | 130 | 10 |
| $Y_0$ | 15 | – | 40 | 130 | 10 |
| $V_{CC}$ | 16 | – | – | – | – |

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and –2.0mA measured at 0.5V LOW.

Note: 1. The fan-in on $I_{-2}$, $I_{-1}$, $I_0$, $I_1$ and $I_2$ will not exceed 1.5 Unit Loads when measured at $V_{IL}$ = 0.5 V. As $V_{IL}$ is decreased to 0 V, the input current $I_{IL}$ MAX. increases to –4, –6, –8, –6 and –4 mA respectively due to the decrease in current sharing with the internal select buffer outputs.

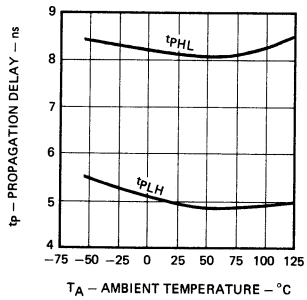
## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



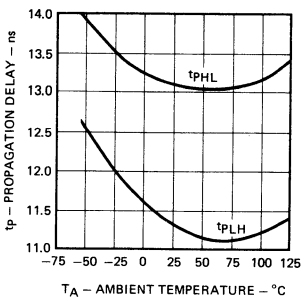

Note: Actual current flow direction shown.

## PERFORMANCE CURVES
### SWITCHING CHARACTERISTICS

**Data to Output (Typical)**




**Select to Output (Typical)**




## LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \overline{S}_1 I_0 + S_0 \overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$Y_1 = \overline{S}_0 \overline{S}_1 I_1 + S_0 \overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$Y_2 = \overline{S}_0 \overline{S}_1 I_2 + S_0 \overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$

$$Y_3 = \overline{S}_0 \overline{S}_1 I_3 + S_0 \overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

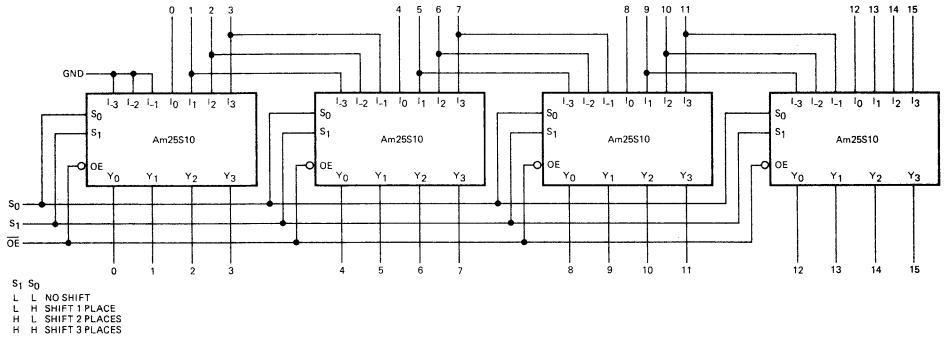
Note: For additional information, see page 5-54

## TRUTH TABLE

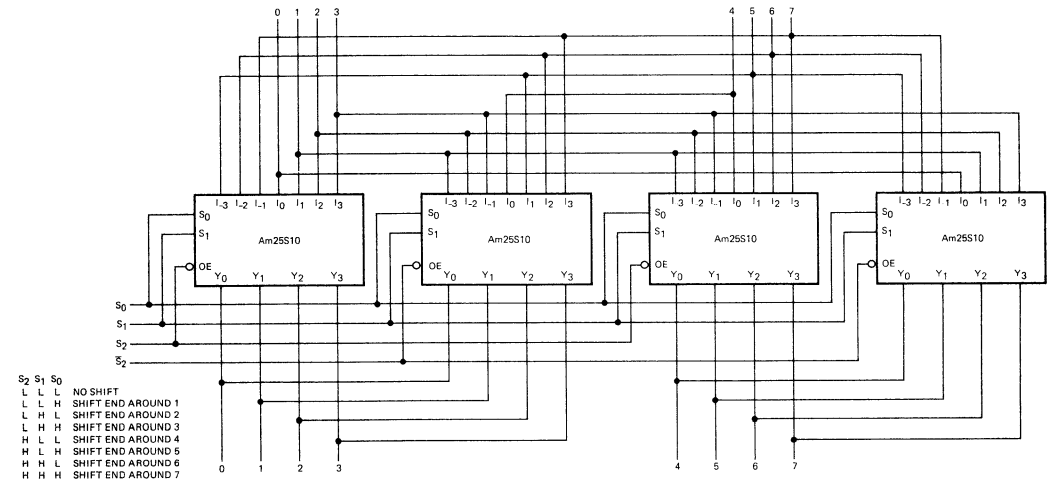
| $\overline{OE}$ | $S_1$ | $S_0$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $I_{-1}$ | $I_{-2}$ | $I_{-3}$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | X | X | X | X | Z | Z | Z | Z |
| L | L | L | $D_3$ | $D_2$ | $D_1$ | $D_0$ | X | X | X | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| L | L | H | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ | X | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ |
| L | H | L | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ |
| L | H | H | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ |

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State
$D_n$ at input $I_n$ may be either HIGH or LOW and output $Y_m$ will follow the selected $D_n$ input level.

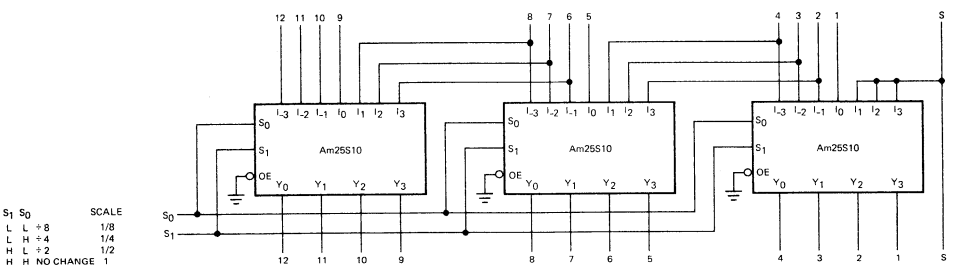
## APPLICATIONS




**16-Bit Shift-Up 0, 1, 2, or 3 Places**

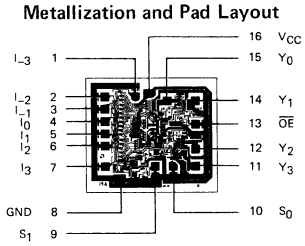



**8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places**




**13-Bit 2's Complement Scaler**

### Metallization and Pad Layout




DIE SIZE 0.056" X 0.066"

# Am25S10
# FOUR-BIT SHIFTER

**By John R. Mick**

## INTRODUCTION

The Am25S10 is a high-speed MSI combinatorial logic block built using advanced Schottky technology. The device has the ability to shift four bits of data 0, 1, 2 or 3 places. The Am25S10 has two select lines that are decoded internally to determine the number of places the data is shifted. The device has seven data inputs $I_{-3}$, $I_{-2}$, $I_{-1}$, $I_0$, $I_1$, $I_2$, and $I_3$ and 4 three-state data outputs $Y_0$, $Y_1$, $Y_2$, and $Y_3$ as shown in the logic symbol diagram of Figure 1. The three-state outputs allow several devices to be bus organized for shifts of more than three places with a single level device propagation delay time. The three-state outputs are controlled by a single buffered active-LOW output control $\overline{OE}$. When the output control is LOW, the data outputs will follow the selected data inputs. When the output control is HIGH, the data outputs offer a high-impedance to the data bus.

## FUNCTIONAL DESCRIPTION

The logic equations describing the output shifting capability of the Am25S10 when the output control is LOW are:

$$Y_0 = \overline{S}_0\,\overline{S}_1\,I_0 + S_0\,\overline{S}_1\,I_{-1} + \overline{S}_0\,S_1\,I_{-2} + S_0\,S_1\,I_{-3}$$
$$Y_1 = \overline{S}_0\,\overline{S}_1\,I_1 + S_0\,\overline{S}_1\,I_0 + \overline{S}_0\,S_1\,I_{-1} + S_0\,S_1\,I_{-2}$$
$$Y_2 = \overline{S}_0\,\overline{S}_1\,I_2 + S_0\,\overline{S}_1\,I_1 + \overline{S}_0\,S_1\,I_0 + S_0\,S_1\,I_{-1}$$
$$Y_3 = \overline{S}_0\,\overline{S}_1\,I_3 + S_0\,\overline{S}_1\,I_2 + \overline{S}_0\,S_1\,I_1 + S_0\,S_1\,I_0$$

From these equations it is seen that each output is operationally equivalent to a four-input multiplexer with the inputs connected such that the select code generates successive one-bit shifts of the input data word. The logic diagram of Figure 2 shows the internal connection of each multiplexer with respect to the seven data inputs. Because of this internal connection scheme, several devices can be connected to perform shifts of 0, 1, 2, or 3 places on words of any length.

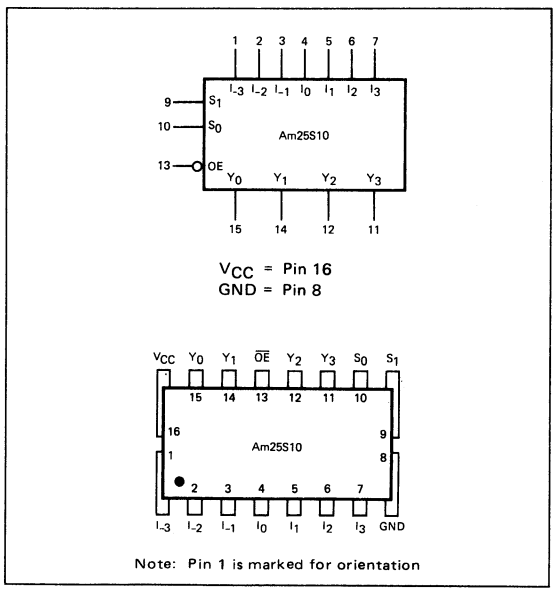



**Figure 1. Logic Symbol and Connection Diagram.**

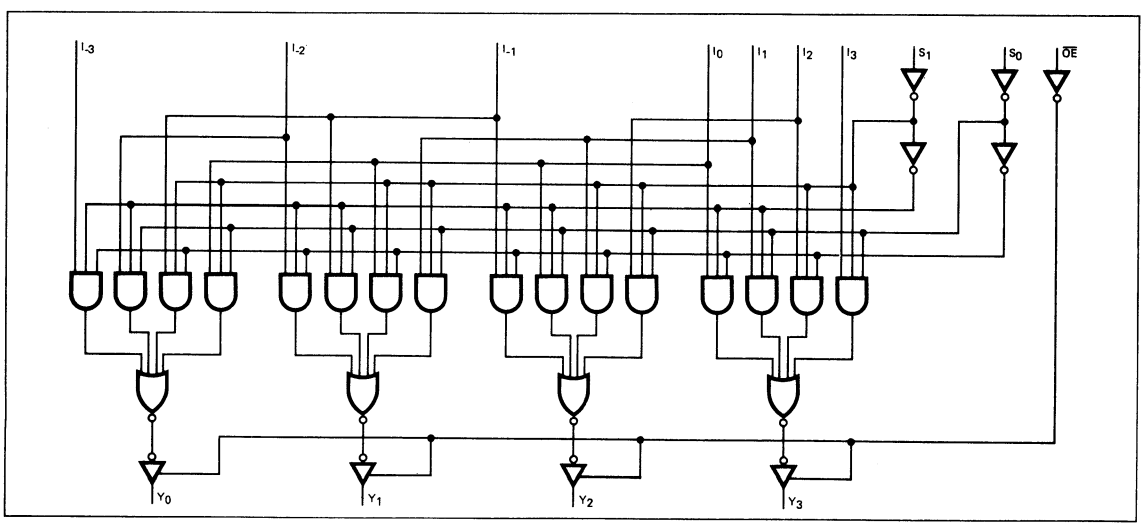



**Figure 2. Logic Diagram of the Am25S10.**

The operation of the Am25S10 is pictorially depicted in Figure 3. Here, the four shift positions of the data outputs with respect to the data inputs are shown via the dashed lines for the four possible select codes. Figure 4 shows a similiar operation only the notation now represents a seven-bit input word $A_0$ through $A_6$. The output code for each of the select field combinations applied to the $S_0$ and $S_1$ inputs is shown in the accompanying Function Table. In addition, the four outputs $Y_0$ through $Y_3$ can be forced to the high-impedance state by applying a HIGH to the "output control" input. This allows additional shifters to be cascaded on the same output lines, or the shifter array to be connected to a common data bus.

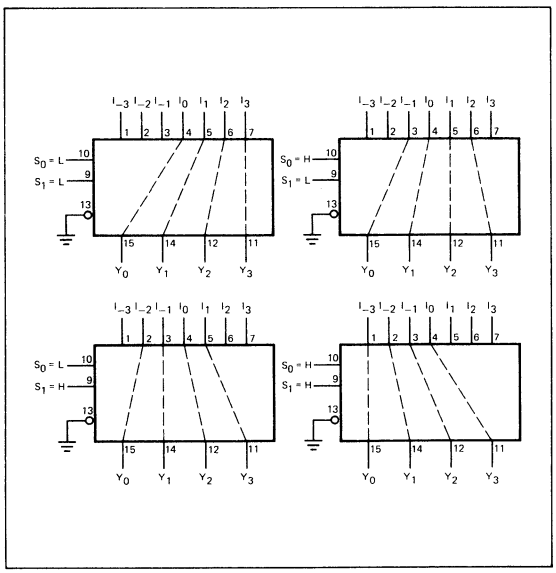
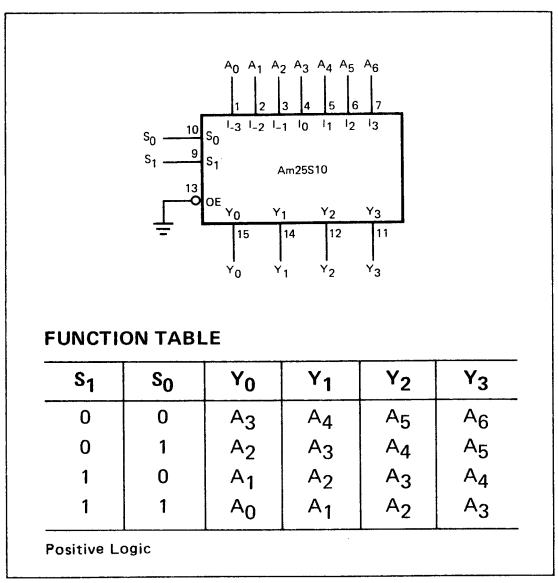



**Figure 3. The Four Shift Positions of the Am25S10.**




**FUNCTION TABLE**

| $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
|---|---|---|---|---|---|
| 0 | 0 | $A_3$ | $A_4$ | $A_5$ | $A_6$ |
| 0 | 1 | $A_2$ | $A_3$ | $A_4$ | $A_5$ |
| 1 | 0 | $A_1$ | $A_2$ | $A_3$ | $A_4$ |
| 1 | 1 | $A_0$ | $A_1$ | $A_2$ | $A_3$ |

Positive Logic

**Figure 4. The Am25S10 4-Bit Shifter Operation.**

## INPUT LOADING

The logic diagram of Figure 2 shows the input connection scheme for the seven data inputs of the Am25S10. Table I shows the number of multiplexer inputs connected to each data input as well as the expected an actual Unit Load weighting on each input.

**TABLE I**

| Pin # | Data Input | Number of Multiplexer Inputs Connected | Expected Unit Loads | Actual Unit Loads |
|---|---|---|---|---|
| 1 | $I_{-3}$ | 1 | 1 | 1 |
| 2 | $I_{-2}$ | 2 | 2 | 1.5 |
| 3 | $I_{-1}$ | 3 | 3 | 1.5 |
| 4 | $I_0$ | 4 | 4 | 1.5 |
| 5 | $I_1$ | 3 | 3 | 1.5 |
| 6 | $I_2$ | 2 | 2 | 1.5 |
| 7 | $I_3$ | 1 | 1 | 1 |

Since the number of gate inputs for $I_{-2}$, $I_{-1}$, $I_0$, $I_1$ and $I_2$ data inputs is 2, 3, 4, 3, and 2 respectively, this could be expected to be the unit load fan-in for these data inputs. However, $I_{IL}$ current sharing occurs internally with the select buffer outputs to reduce the external fan-in. Since a Schottky TTL unit load is defined as −2.0mA measured at 0.5V LOW, the maximum $I_{IL}$ when measured at $V_{IL}$ = 0.5V is −3mA or 1.5 STTL unit loads. As the measure voltage $V_{IL}$ on these data inputs is decreased to 0V, the measured input current on $I_{-2}$, $I_{-1}$, $I_0$, $I_1$, and $I_2$ can increase to an $I_{IL}$ maximum of −4, −6, −8, −6 and −4 mA respectively because of the decrease in current sharing with the internal select buffer outputs.

A plot of the typical input voltage versus input current for the data inputs is shown in Figure 5. This Figure shows the increased input current flow (negative current) as the input voltage is decreased. It also shows the effect of the input clamp diode as forward bias in applied.

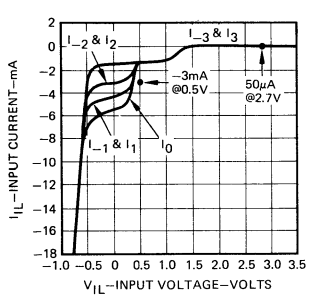


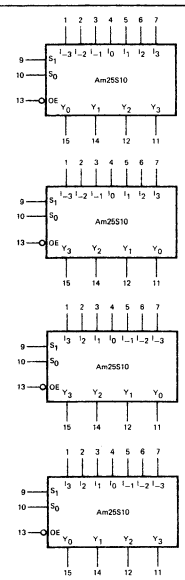

**Figure 5. Typical Input Current Characteristics.**

4

## LOGIC EQUIVALENTS OF THE Am25S10

The Am25S10 exhibits several symmetrical properties that may be of advantage in some designs. These symmetrical properties involve the labeling of the inputs and outputs and the polarity of the select inputs. By relabeling the inputs in reverse order, labeling the outputs in reverse order, and considering the select inputs in positive logic (active-HIGH) or negative logic (active-LOW), eight logic equivalents for the device are possible. Figure 6 shows the operation of the device for the four combinations of input and output definitions for the positive logic notation while Figure 7 shows the operation of the device for the four combinations for the negative logic notation. The logic symbol for each set of definitions for the input pins and output pins is shown adjacent to the truth table.

This relabeling of pins can provide the designer with some flexibility in printed circuit board layout. Likewise, the select code can be either positive logic or negative logic and the input data will be passed non-inverted. In some cases, the redefinition allows the designer to visualize shifting up versus shifting down for the same select code.




| SELECT PINS | | DATA INPUT PINS | | | | | | | DATA OUTPUT PINS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | 10 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 11 | 12 | 14 | 15 |
| $S_1$ | $S_0$ | $I_{-3}$ | $I_{-2}$ | $I_{-1}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | 0 | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 1 | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ |
| 1 | 0 | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ |
| 1 | 1 | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ |

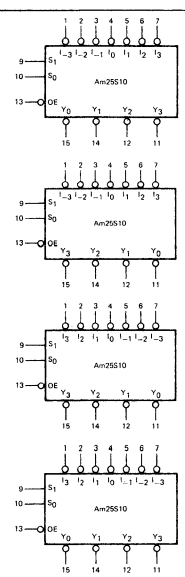
| $S_1$ | $S_0$ | $I_{-3}$ | $I_{-2}$ | $I_{-1}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 0 | 1 | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ |
| 1 | 0 | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ |
| 1 | 1 | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ |

| $S_1$ | $S_0$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $I_{-1}$ | $I_{-2}$ | $I_{-3}$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ |
| 0 | 1 | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ |
| 1 | 0 | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ |
| 1 | 1 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ |

| $S_1$ | $S_0$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $I_{-1}$ | $I_{-2}$ | $I_{-3}$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ |
| 0 | 1 | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ |
| 1 | 0 | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ |
| 1 | 1 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ |

Positive Logic (HIGH = 1, LOW = 0) for the select inputs.

**Figure 6. Four Possible Input and Output Combinations for the Positive Logic Definition.**




| SELECT PINS | | DATA INPUT PINS | | | | | | | DATA OUTPUT PINS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | 10 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 11 | 12 | 14 | 15 |
| $S_1$ | $S_0$ | $I_{-3}$ | $I_{-2}$ | $I_{-1}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | 0 | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ |
| 0 | 1 | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ |
| 1 | 0 | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ |
| 1 | 1 | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |

| $S_1$ | $S_0$ | $I_{-3}$ | $I_{-2}$ | $I_{-1}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ |
| 0 | 1 | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ |
| 1 | 0 | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ |
| 1 | 1 | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |

| $S_1$ | $S_0$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $I_{-1}$ | $I_{-2}$ | $I_{-3}$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| 0 | 1 | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ |
| 1 | 0 | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ |
| 1 | 1 | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ |

| $S_1$ | $S_0$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $I_{-1}$ | $I_{-2}$ | $I_{-3}$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | X | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| 0 | 1 | X | $D_2$ | $D_1$ | $D_0$ | $D_{-1}$ | X | X | $D_{-1}$ | $D_0$ | $D_1$ | $D_2$ |
| 1 | 0 | X | X | $D_1$ | $D_0$ | $D_{-1}$ | $D_{-2}$ | X | $D_{-2}$ | $D_{-1}$ | $D_0$ | $D_1$ |
| 1 | 1 | X | X | X | $D_0$ | $D_{-1}$ | $D_{-2}$ | $D_{-3}$ | $D_{-3}$ | $D_{-2}$ | $D_{-1}$ | $D_0$ |

Negative Logic (LOW = 1, HIGH = 0) for the select inputs.

**Figure 7. Four Possible Input and Output Combinations for the Negative Logic Definition.**

## Am25S10 APPLICATIONS

The four-bit shifter is an ideal MSI element for high-speed shifting and scaling in digital systems. By suitable interconnection of the inputs and outputs, shifts of any number of places up or down can be made with a propagation delay of only one device. Shifting can be logical, with zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop. The three-state outputs can be used to increase the number of places shifted and also facilitate rapid data bus access in bus organized systems.

The Connection Diagram and Function Table of Figure 8 show a 16-bit word shifted up 0, 1, 2 or 3 places. In this example, the most significant bits ($A_{13}$, $A_{14}$, $A_{15}$) are discarded and logic zeroes are shifted in at the least significant end.

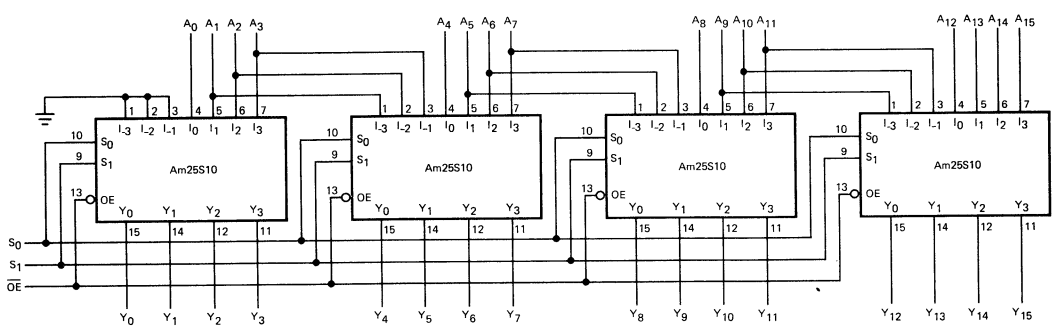
Figure 9 shows a Connection Diagram and Function Table for a 12-bit word shifted down 0, 1, 2 or 3 places. In this example, zeroes are shifted into the most significant bits and the least significant bits are discarded. Notice that one of the alternate definitions and pin assignments has been used to define the Am25S10.

A complete end-around barrel shift of 0, 1, 2, 3, 4, 5, 6 or 7 places is shown in Figure 10. In this configuration, the three-state capability of the outputs is used to connect one of two Am25S10's to the data output under the control of the $S_2$ and $\overline{S_2}$ select inputs. This technique can be expanded for longer word lengths by using one-of-four or one-of-eight decoders to control the active-LOW "output control" input.

A 13-bit two's complement scaler is shown in Figure 11. For this connection, the sign bit is pulled in at the most significant end and the least significant bits are truncated. Thus, the 13-bit two's complement binary output number is scaled to 1, 1/2, 1/4, or 1/8 of its input value.

A two-level 16-bit barrel shifter and its associated Function Table are shown in Figure 12. Only eight Am25S10's are required to perform this function. For clarity, the intermediate level of inputs and outputs have been labeled $B_i$. The sixteen-bit output word can be bus connected and controlled via the $\overline{OE}$ input.

Figure 13 demonstrates a unique way to convert a fixed point positive number to a floating-point mantisa and exponent. The priority encoder is used to determine the most significant bit position of the input word with a binary "1". The priority encoder output is a binary weighted code representing the number of places the input word is to be shifted up. This code controls the Am25S10 shifting array and shifts the input word such that the $Y_7$-bit of the mantisa is always a binary one (except for A = 0). The exponent is of the form $2^{-n}$ where n is the value of the binary weighted code from the priority encoder. Thus, the output of this functional block is of the form $Y2^{-n}$.

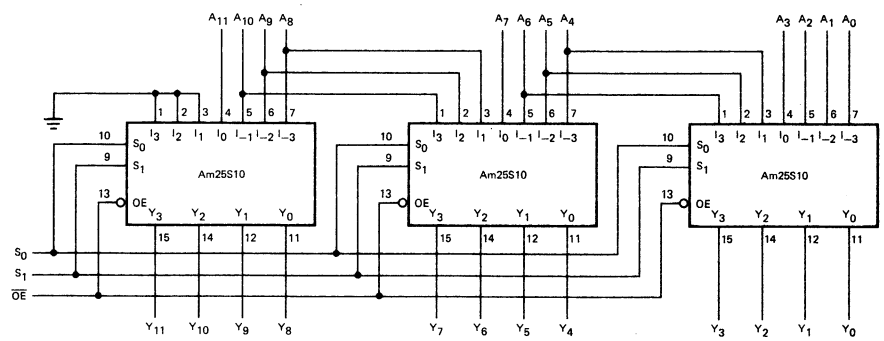



**FUNCTION TABLE**

| $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ | $Y_8$ | $Y_9$ | $Y_{10}$ | $Y_{11}$ | $Y_{12}$ | $Y_{13}$ | $Y_{14}$ | $Y_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ |
| 0 | 1 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ |
| 1 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ |
| 1 | 1 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ |

Positive Logic

**Figure 8. 16-Bit Shift-Up 0, 1, 2 or 3 Places.**

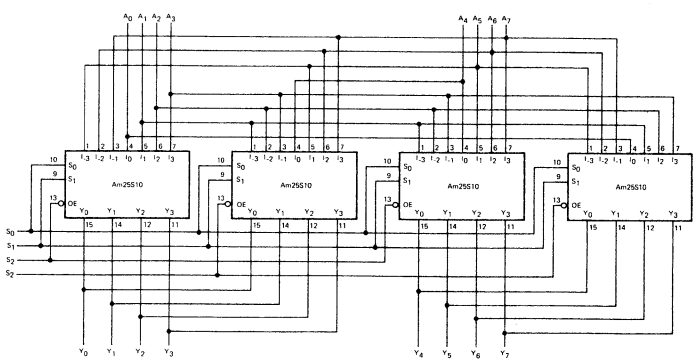



**FUNCTION TABLE**

| $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ | $Y_8$ | $Y_9$ | $Y_{10}$ | $Y_{11}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ |
| 0 | 1 | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | 0 |
| 1 | 0 | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | 0 | 0 |
| 1 | 1 | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | 0 | 0 | 0 |

Positive Logic (Alternate Definitions)

**Figure 9. 12-Bit Shift-Down 0, 1, 2 or 3 Places.**

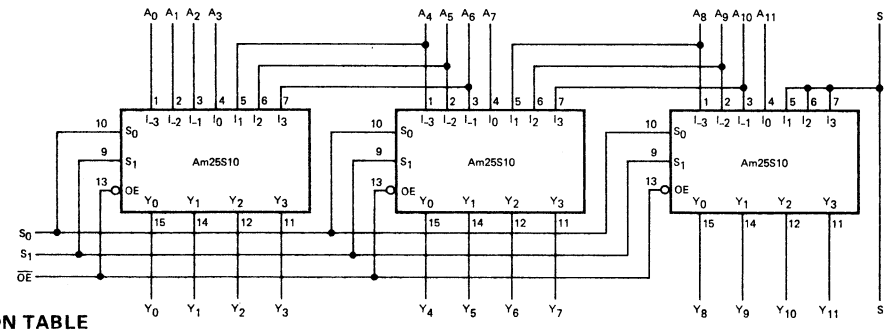



**FUNCTION TABLE**

| $S_2$ | $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ |
| 0 | 0 | 1 | $A_7$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ |
| 0 | 1 | 0 | $A_6$ | $A_7$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ |
| 0 | 1 | 1 | $A_5$ | $A_6$ | $A_7$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ |
| 1 | 0 | 0 | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ |
| 1 | 0 | 1 | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_0$ | $A_1$ | $A_2$ |
| 1 | 1 | 0 | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_0$ | $A_1$ |
| 1 | 1 | 1 | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_0$ |

Positive Logic

**Figure 10. Eight-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6 or 7 Places.**

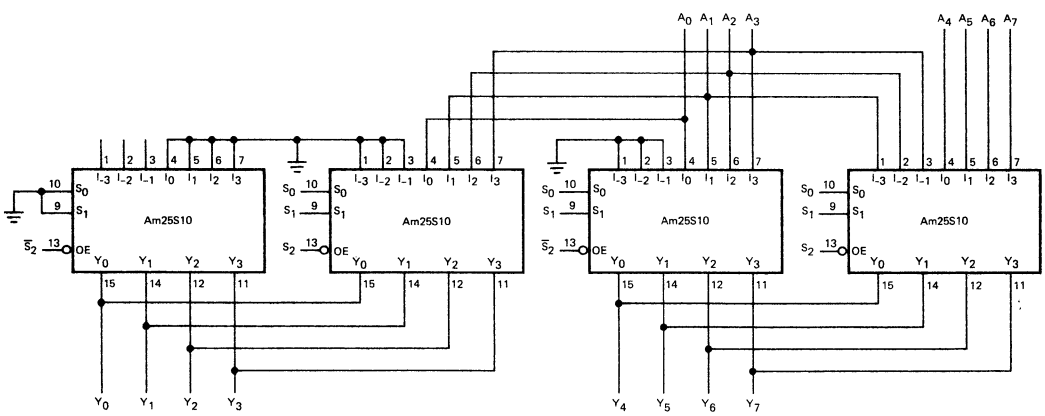


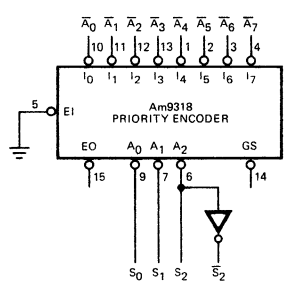

**FUNCTION TABLE**

| SCALE | $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ | $Y_8$ | $Y_9$ | $Y_{10}$ | $Y_{11}$ | S |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1/8 | 0 | 0 | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | S | S | S | S |
| 1/4 | 0 | 1 | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | S | S | S |
| 1/2 | 1 | 0 | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | S | S |
| 1 | 1 | 1 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | S |

Positive Logic

**Figure 11. 13-Bit 2's Complement Scaler.**



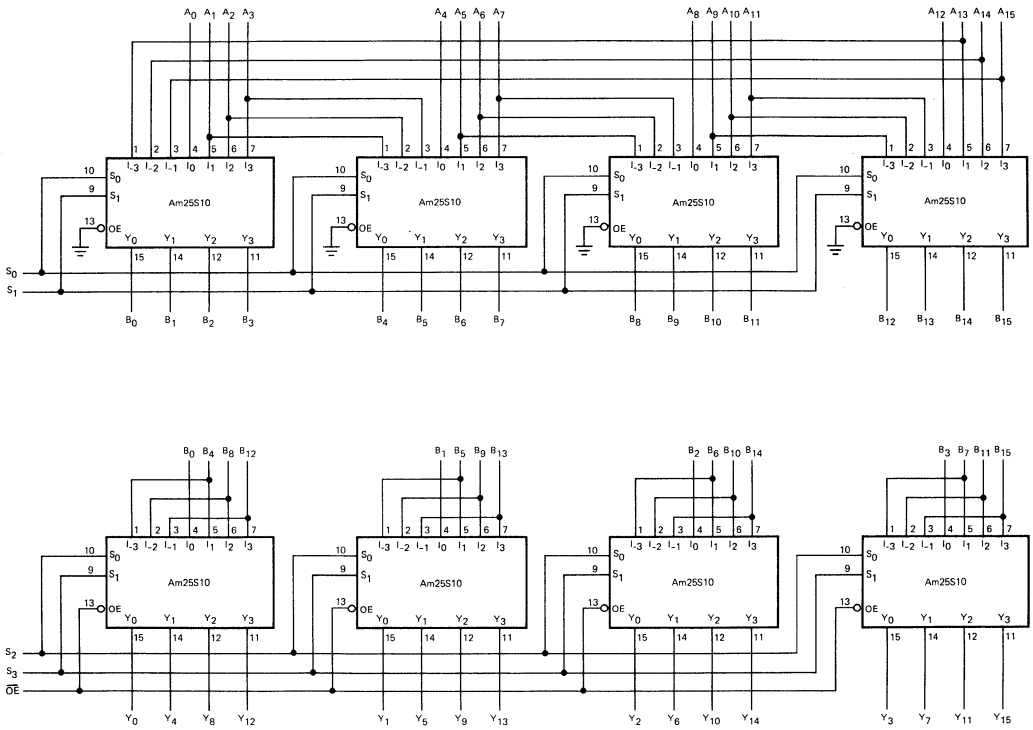




**FUNCTION TABLE**

| EXPONENT | | | MANTISSA | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $S_2$ | $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ |
| 0 | 0 | 1 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ |
| 0 | 1 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ |
| 0 | 1 | 1 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_0$ | $A_1$ |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $A_0$ |

Positive Logic

**Figure 13. Binary Scaling to Give Mantissa and Exponent.**




## FUNCTION TABLE

| $S_3$ | $S_2$ | $S_1$ | $S_0$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ | $Y_8$ | $Y_9$ | $Y_{10}$ | $Y_{11}$ | $Y_{12}$ | $Y_{13}$ | $Y_{14}$ | $Y_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ |
| 0 | 0 | 0 | 1 | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ |
| 0 | 0 | 1 | 0 | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ |
| 0 | 0 | 1 | 1 | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ |
| 0 | 1 | 0 | 0 | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ |
| 0 | 1 | 0 | 1 | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ |
| 0 | 1 | 1 | 0 | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ |
| 0 | 1 | 1 | 1 | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ |
| 1 | 0 | 0 | 0 | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ |
| 1 | 0 | 0 | 1 | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ |
| 1 | 0 | 1 | 0 | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ |
| 1 | 0 | 1 | 1 | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ |
| 1 | 1 | 0 | 0 | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ | $A_3$ |
| 1 | 1 | 0 | 1 | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ | $A_2$ |
| 1 | 1 | 1 | 0 | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ | $A_1$ |
| 1 | 1 | 1 | 1 | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ | $A_{15}$ | $A_0$ |

Positive Logic

**Figure 12. Full 16-Bit Barrel Shifter.**

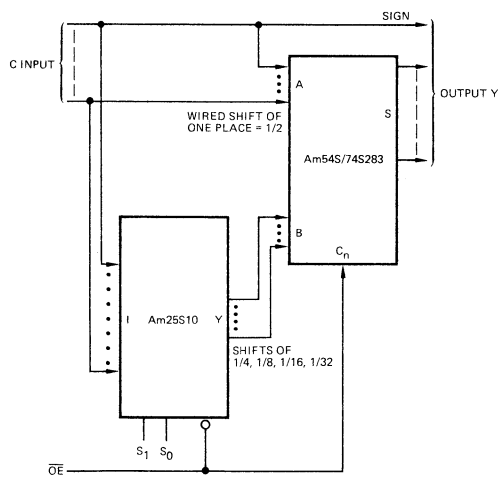
## FIXED MULTIPLIERS

Digital systems requiring multiplication by a constant interger or constant fraction can make effective use of the Am25S10 if the constant must be varied over several values. By using four-bit shifters and high-speed adders, very high-speed "constant coefficient" or fixed multipliers can be built. The technique is shown diagrammatically in Figure 14. Here, the input word C is wired to the adder A inputs such that a shift of $\frac{1}{2}$ C is "built-in". The Am25S10 shifter is wired to the B inputs of the adder such that its four select states represent prescaling of $\frac{1}{4}$C, $\frac{1}{8}$C, $\frac{1}{16}$C, and $\frac{1}{32}$C of the C input word. If the $\overline{OE}$ input is used to disable the outputs (high impedance), the adder B inputs will assume the logical one state (HIGH). By adding a "one" at the adder carry input least significant end, the contribution of the B inputs to the sum output is zero and the adder A input will be passed to the output. Thus, the $\overline{OE}$ input can be used to generate a zero C value from the shifter.

Figure 15 shows the actual connection diagram for a 12-bit two's complement fixed multiplier using the scheme of Figure 14. The Y output weighting is the same as shown in the Function Table of Figure 14. The $\overline{OE}$ input is tied directly to the adder least significant $C_n$ input to complete the shifter "zero" output function.

Figure 16 shows two shifter arrays used in conjunction with one adder. For the shifter A and shifter B select codes shown, twenty multiplication constants are realized with seventeen constants being unique. Other combinations could be used to realize different outputs. The combinations possible can be extended greatly by using multiple adders and multiple shifting arrays. For the example of Figure 16, the zero shifter output (high-impedance state) is used with only one shifter since only one $C_n$ input is available.

This technique for fixed constant multipliers can be applied to two's complement, one's complement, sign-magnitude, or magnitude only arithmetic. In so doing, the sign must be handled appropriately and the adder output word size and number range must be considered. For the one's complement case, the all ones representation for zero must be handled separately.




**FUNCTION TABLE**

| $\overline{OE}$ | $S_1$ | $S_0$ | 4-BIT SHIFTER #SHIFTS | 4-BIT SHIFTER B INPUT OF ADDER | A INPUT OF ADDER | OUTPUT Y |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Two | $\frac{1}{4}$C | $\frac{1}{2}$C | $\frac{3}{4}$C |
| 0 | 0 | 1 | Three | $\frac{1}{8}$C | $\frac{1}{2}$C | $\frac{5}{8}$C |
| 0 | 1 | 0 | Four | $\frac{1}{16}$C | $\frac{1}{2}$C | $\frac{9}{16}$C |
| 0 | 1 | 1 | Five | $\frac{1}{32}$C | $\frac{1}{2}$C | $\frac{17}{32}$C |
| 1 | X | X | Hi-Z | 0C | $\frac{1}{2}$C | $\frac{1}{2}$C |

Positive Logic

**Figure 14. Parallel "Constant Coefficient" Multiplier Block Diagram and Function Table.**

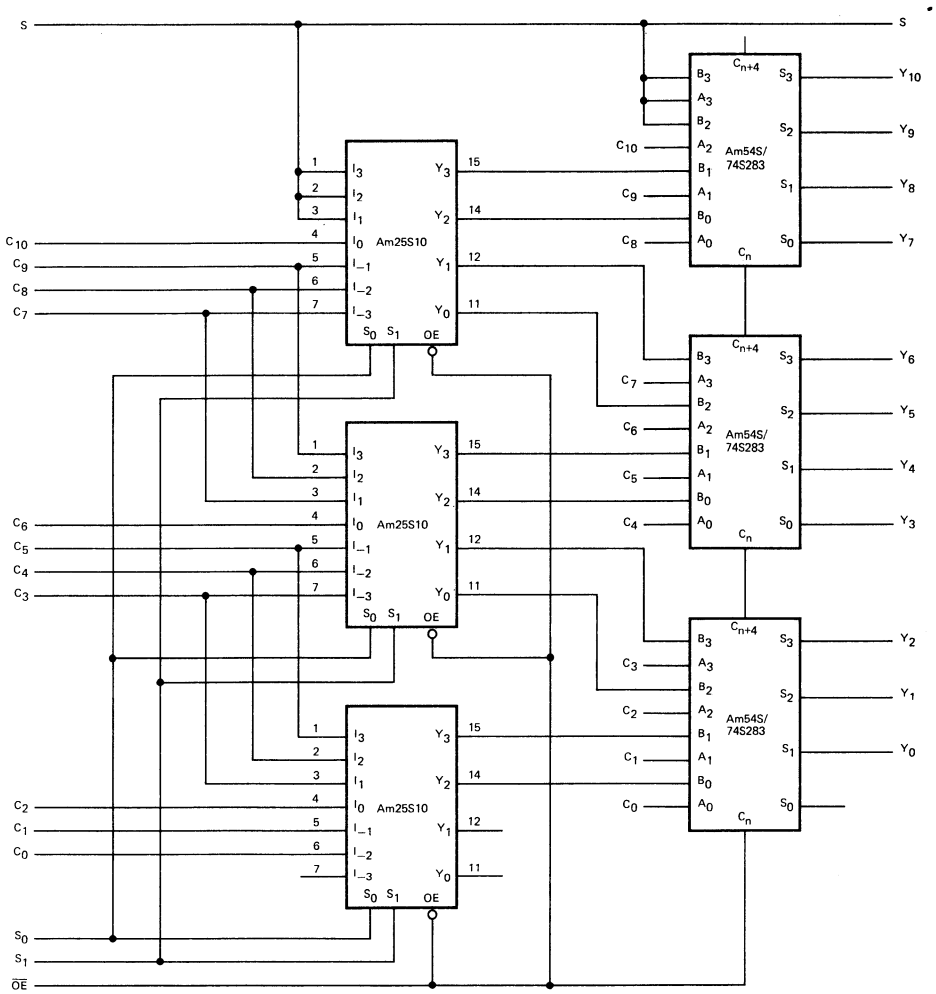
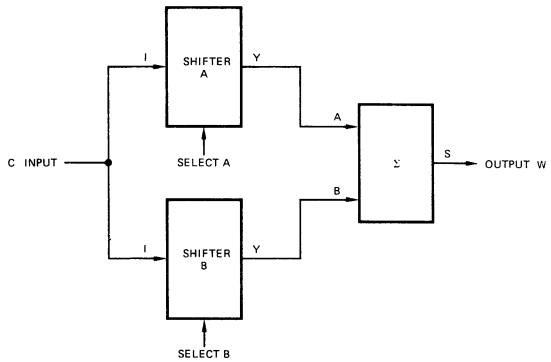



**Figure 15. 12-Bit 2's Complement "Constant Coefficient" Multiplier.**




SHIFTER A = $C, \frac{C}{2}, \frac{C}{4}, \frac{C}{8}$

SHIFTER B = $\frac{C}{4}, \frac{C}{8}, \frac{C}{16}, \frac{C}{32}, 0$

**FIXED MULTIPLIER OUTPUT W**

| SHIFTER A \ SHIFTER B | $\frac{C}{4}$ | $\frac{C}{8}$ | $\frac{C}{16}$ | $\frac{C}{32}$ | 0 |
|---|---|---|---|---|---|
| C | $\frac{5}{4}C$ | $\frac{9}{8}C$ | $\frac{17}{16}C$ | $\frac{33}{32}C$ | C |
| $\frac{C}{2}$ | $\frac{3}{4}C$ | $\frac{5}{8}C$ | $\frac{9}{16}C$ | $\frac{17}{32}C$ | $\frac{1}{2}C$ |
| $\frac{C}{4}$ | $\frac{1}{2}C$ | $\frac{3}{8}C$ | $\frac{5}{16}C$ | $\frac{9}{32}C$ | $\frac{1}{4}C$ |
| $\frac{C}{8}$ | $\frac{3}{8}C$ | $\frac{1}{4}C$ | $\frac{3}{16}C$ | $\frac{5}{32}C$ | $\frac{1}{8}C$ |

**Figure 16. Two Shifter Arrays and One Adder Array in a Fixed Multiplier Connection.**

## CONCLUSION

The Am25S10 four-bit shifter is a new unique combinatorial logic element offering the system designer new shifting and scaling capability not previously available in a single package. The three-state output design of the Am25S10 provides increased flexibility in its use and the advanced Schottky construction offers minimum propagation delay. The device can be used to shift any number of bits any number of places; up, down or end-around.

# Am25S18

## Quad D Register With Standard And Three-State Outputs

### Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am25S18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

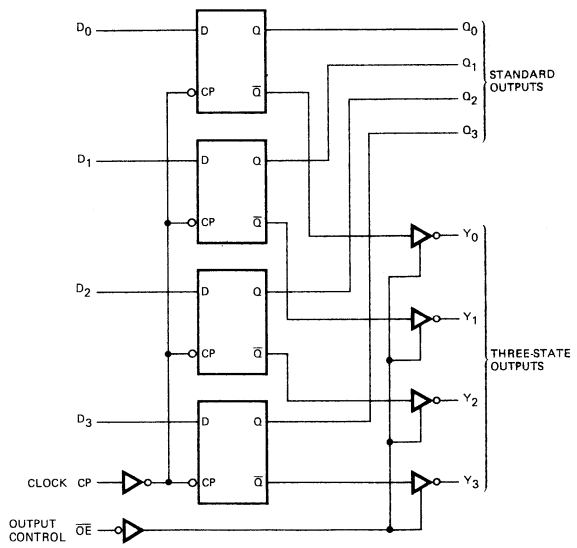
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25S18 is a 4-bit, high speed Schottky register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25S18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

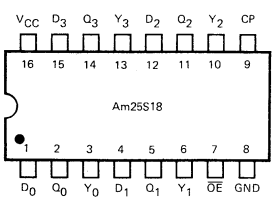
### LOGIC DIAGRAM




### ORDERING INFORMATION

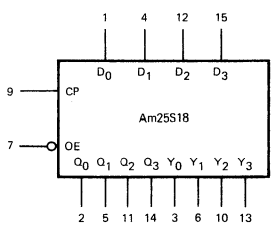
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM25S18PC |
| Hermetic DIP | 0°C to +70°C | AM25S18DC |
| Dice | 0°C to +70°C | AM25S18XC |
| Hermetic DIP | –55°C to +125°C | AM25S18DM |
| Hermetic Flat Pak | –55°C to +125°C | AM25S18FM |
| Dice | –55°C to +125°C | AM25S18XM |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Temperature (Ambient) Under Bias | –55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | –0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | –0.5V to +$V_{CC}$ max. |
| DC Input Voltage | –0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | –30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am25S18XC | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ± 5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am25S18XM | $T_A$ = –55°C to +125°C | $V_{CC}$ = 5.0V ± 10% (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | Q | $I_{OH}$ = –1mA MIL | 2.5 | 3.4 | | Volts |
| | | | | $I_{OH}$ = –1mA COM'L | 2.7 | 3.4 | | |
| | | | Y | XM, $I_{OH}$ = –2mA | 2.4 | 3.4 | | |
| | | | | XC, $I_{OH}$ = –6.5mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage (Note 6) | $V_{CC}$ = MIN., $I_{OL}$ = 20mA; $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = –18mA | | | | | –1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | | –2.0 | mA |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | | 50 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | | 1.0 | mA |
| $I_O$ | Y Output Off-State Leakage Current | $V_{CC}$ = MAX. | | $V_O$ = 2.4V | | | 50 | µA |
| | | | | $V_O$ = 0.4V | | | –50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX. | | | –40 | | –100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | | 80 | 130 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, $T_A$ = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. $I_{CC}$ is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

4

## Switching Characteristics ($T_A$ = +25°C, $V_{CC}$ = 5.0V, $R_L$ = 280Ω)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Q Output | | $C_L$ = 15pF | | 6.0 | 9.0 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13 | |
| $t_{pw}$ | Clock Pulse Width | HIGH | | 7.0 | | | ns |
| | | LOW | | 9.0 | | | |
| $t_s$ | Data | | | 5.0 | | | ns |
| $t_h$ | Data | | | 3.0 | | | ns |
| $t_{PLH}$ | Clock to Y Output ($\overline{OE}$ LOW) | | | | 6.0 | 9.0 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13 | |
| $t_{ZH}$ | Output Control to Output | | $C_L$ = 15pF | | 12.5 | 19 | ns |
| $t_{ZL}$ | | | | | 12 | 18 | |
| $t_{HZ}$ | | | $C_L$ = 5.0pF | | 4.0 | 6.0 | |
| $t_{LZ}$ | | | | | 7.0 | 10.5 | |
| $f_{max}$ | Maximum Clock Frequency | | $C_L$ = 15pF | 75 | 100 | | MHz |

## TRUTH TABLE

| INPUTS | | | OUTPUTS | | NOTES |
|---|---|---|---|---|---|
| $\overline{OE}$ | CLOCK CP | D | Q | Y | |
| H | L | X | NC | Z | – |
| H | H | X | NC | Z | – |
| H | ↑ | L | L | Z | – |
| H | ↑ | H | H | Z | – |
| L | ↑ | L | L | L | – |
| L | ↑ | H | H | H | – |
| L | – | – | L | L | 1 |
| L | – | – | H | H | 1 |

L = LOW
H = HIGH
X = Don't care
NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

## DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The four data inputs to the register.

**$Q_i$** The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

**$Y_i$** The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the $Y_i$ outputs to the high-impedance state.

**CP** Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

**$\overline{OE}$** Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the $Y_i$ outputs.

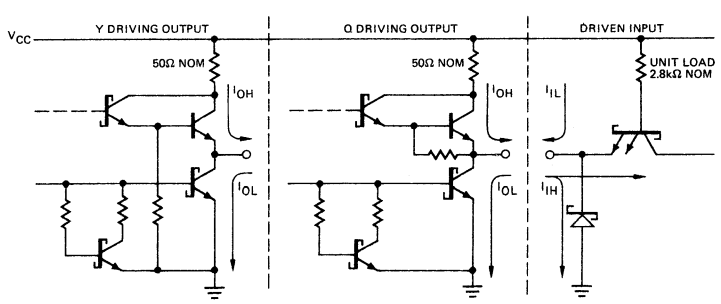
## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $D_0$ | 1 | 1 | – | – |
| $Q_0$ | 2 | – | 20 | 10* |
| $Y_0$ | 3 | – | 40/130 | 10* |
| $D_1$ | 4 | 1 | – | – |
| $Q_1$ | 5 | – | 20 | 10* |
| $Y_1$ | 6 | – | 40/130 | 10* |
| $\overline{OE}$ | 7 | 1 | – | – |
| GND | 8 | – | – | – |
| CP | 9 | 1 | – | – |
| $Y_2$ | 10 | – | 40/130 | 10* |
| $Q_2$ | 11 | – | 20 | 10* |
| $D_2$ | 12 | 1 | – | – |
| $Y_3$ | 13 | – | 40/130 | 10* |
| $Q_3$ | 14 | – | 20 | 10* |
| $D_3$ | 15 | 1 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

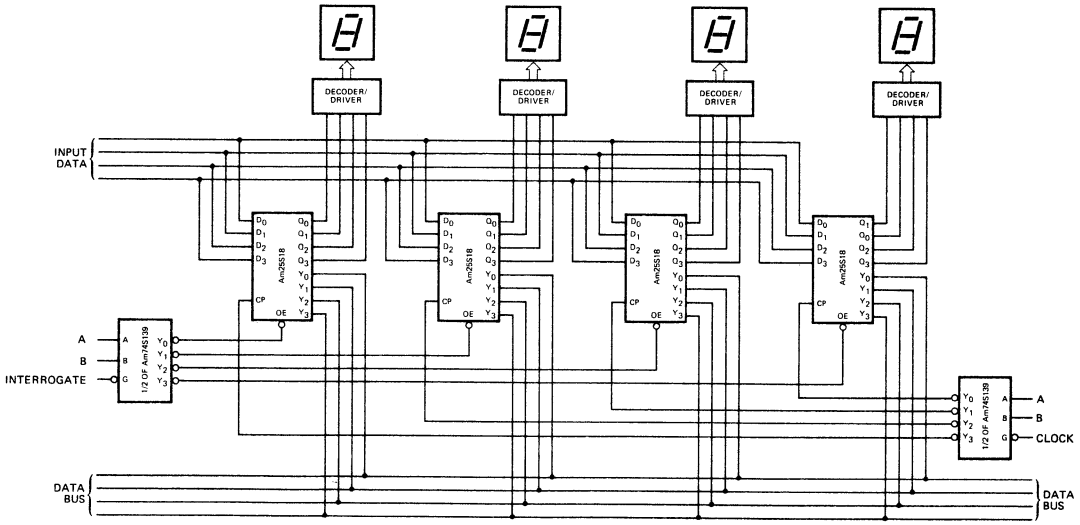
*Fan-out on each $Q_i$ and $Y_i$ output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

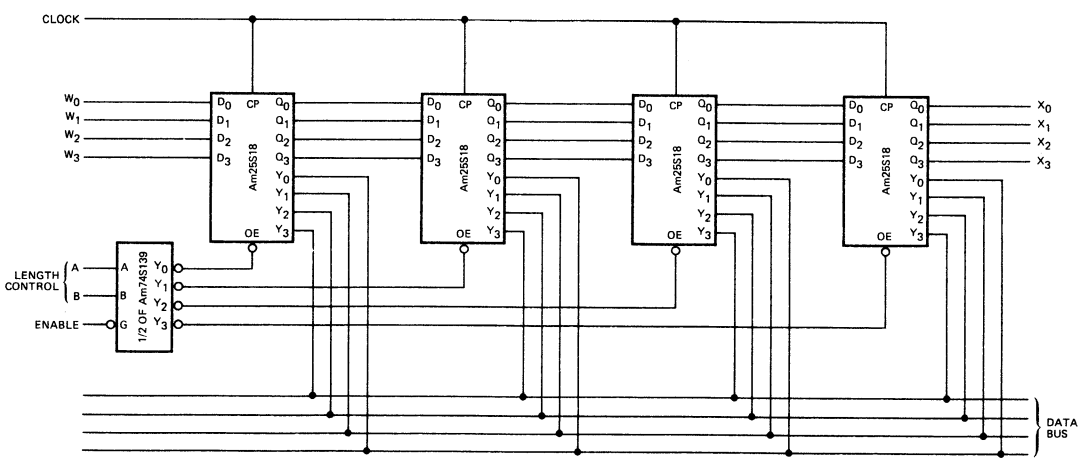



Note: Actual current flow direction shown.

## APPLICATIONS

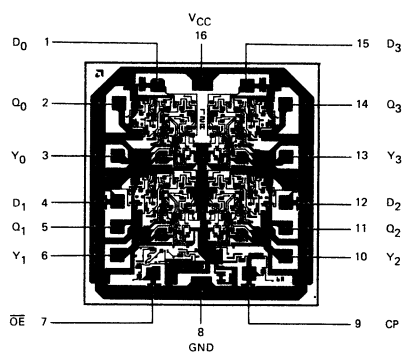



THE Am25S18 USED AS DISPLAY REGISTER WITH BUS INTERROGATE CAPABILITY.




THE Am25S18 AS A VARIABLE LENGTH (1, 2, 3 or 4 WORD) SHIFT REGISTER.

### Metallization and Pad Layout




DIE SIZE
0.077" X 0.079"

# Am26S02

## Schottky Dual Retriggerable, Resettable Monostable Multivibrator

### Distinctive Characteristics

- Advanced Schottky technology with PNP inputs
- Retriggerable 0% to 100% duty cycle
- 28ns to ∞ output pulse width range
- 100kΩ maximum timing resistor value
- Am26S02XM typical pulse width change of only 1.0% over −55°C to +125°C with $R_X$ = 100kΩ.
- Am26S02XC typical pulse width change of only 0.4% over 0°C to +70°C with $R_X$ = 100kΩ

### FUNCTIONAL DESCRIPTION

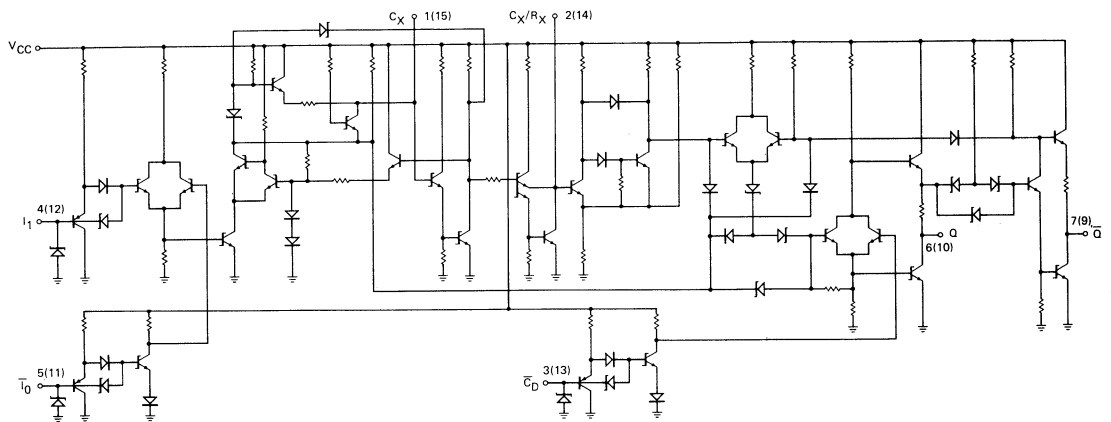
The Am26S02 is a dual DC level sensitive, retriggerable, resettable monostable multivibrator built using advanced Schottky technology. The output pulse duration and accuracy depend on the external timing components of each multivibrator. The Am26S02 features PNP inputs to reduce the input loading.

Provision is made on each multivibrator circuit for triggering the PNP inputs on either the rising or falling edge of an input signal by including an inverting and non-inverting trigger input. These PNP inputs are DC coupled making triggering independent of the input rise or fall time. Each time the monostable trigger input is activated from the OR trigger gate, full pulse length triggering occurs independent of the present state of the monostable.

The direct clear PNP input allows a timing cycle to be terminated at any time during the cycle. A LOW on the clear input forces the Q output LOW regardless of the $\overline{I_0}$ or $I_1$ inputs.

The Am26S02XM has a typical pulse width change of only 1.0% over the full military −55°C to +125°C temperature range and the Am26S02XC has a typical pulse width change of only 0.4% over the commercial 0°C to +70°C temperature range with a $R_X$ = 100kΩ.

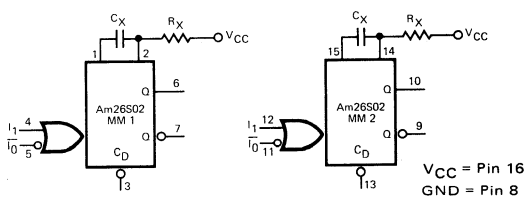
### SCHEMATIC DIAGRAM
(One Monostable Multivibrator Shown)



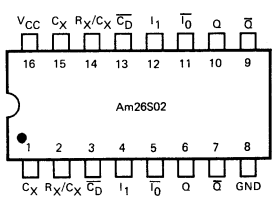

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to + 70°C | AM26S02PC |
| Hermetic DIP | 0°C to + 70°C | AM26S02DC |
| Dice | 0°C to + 70°C | AM26S02XC |
| Hermetic DIP | −55°C to +125°C | AM26S02DM |
| Hermetic Flat Pak | −55°C to +125°C | AM26S02FM |
| Dice | −55°C to +125°C | AM26S02XM |

### LOGIC SYMBOLS




### CONNECTION DIAGRAM




Note:
Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am26S02XC | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% (COM'L) | MIN. = 4.75 V | MAX. = 5.25 V |
| Am26S02XM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% (MIL) | MIN. = 4.5 V | MAX. = 5.5 V |

| Parameters | Description | Test Conditions (Note 1) | Min. | Typ.(Note 2) | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 2.5 | 2.8 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 0.38 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | −0.8 | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | −0.15 | −0.4 | mA |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | 0.1 | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 1.0V<br>$T_A$ = 25°C Only | −8 | −15 | −35 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = 5.0 V, $I_{IX}$ = 0.33 mA (Notes 5 & 6) | | 48 | 69 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured with pin 5 and 11 grounded and $I_{IX}$ applied to pins 2 and 14.
6. $I_{IX}$ is the current into the $R_X C_X$ node to simulate $R_X$.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{I_0}$ to Q | | $V_{CC}$ = 5.0 V, $R_L$ = 280 Ω, $C_L$ = 15 pF, $R_X$ = 5kΩ, $C_X$ = 0 pF | | 13 | 20 | ns |
| $t_{PHL}$ | $\overline{I_0}$ to $\overline{Q}$ | | | | 15 | 23 | ns |
| $t_{PLH}$ | $I_1$ to Q | | | | 12 | 20 | ns |
| $t_{PHL}$ | $I_1$ to $\overline{Q}$ | | | | 12 | 20 | ns |
| $t_{PLH}$ | Clear to $\overline{Q}$ | | | | 21 | | ns |
| $t_{PHL}$ | Clear to Q | | | | 9 | 13 | ns |
| $t_{pw}$ | Pulse Width | $\overline{I_0}$ HIGH or $I_1$ LOW | | 20 | 10 | | ns |
| | | $\overline{I_0}$ LOW or $I_1$ HIGH | | 16 | 7 | | ns |
| | | Clear LOW | | 24 | 16 | | ns |
| $t_s$ | Clear Recovery (inactive) to Trigger | | | −10 | −22 | | ns |
| $t_{pwQ}$ (Min.) | Minimum Pulse Width Q Output | | $V_{CC}$ = 5.0 V, $R_X$ = 5.0 kΩ, $C_X$ = 0 pF<br>$R_L$ = 1.0 kΩ | 27 | 33 | 39 | ns |
| $t_{pwQ}$ | Pulse Width Q Output | | $V_{CC}$ = 5.0 V, $R_L$ = 280 Ω, $C_L$ = 15 pF<br>$R_X$ = 10 kΩ, $C_X$ = 1000 pF (CK05 Type) | 2.89 | 3.04 | 3.19 | μs |
| $R_X$ | Timing Resistor | | 0°C to 70°C | 5 | | 100 | kΩ |
| | | | −55°C to +125°C | 5 | | 50 | |

## DEFINITION OF FUNCTIONAL TERMS:

$\overline{C_D}$ Asynchronous direct CLEAR. A LOW on the clear input resets the monostable regardless of the other inputs.

$\overline{I_0}$ Active-LOW input. With $I_1$ LOW, a HIGH-to-LOW transition will trigger the monostable.

$I_1$ Active-HIGH input. With $\overline{I_0}$ HIGH, a LOW-to-HIGH transition will trigger the monostable.

Q The TRUE monostable output.

$\overline{Q}$ The Complement monostable output.

### FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{C_D}$ | $I_1$ | $\overline{I_0}$ | Q | $\overline{Q}$ |
| L | X | X | L | H |
| H | H | X | L | H |
| H | L | ↓ | ⎍ | ⎎ |
| H | X | L | L | H |
| H | ↑ | H | ⎍ | ⎎ |

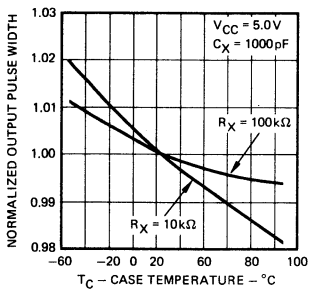
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⎎ = HIGH-LOW-HIGH Pulse
X = Don't Care

## LOADING RULES (In Unit Loads)

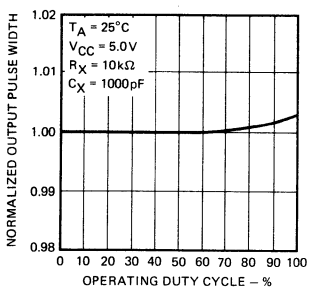
| Input/Output | Pin No.'s | | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|---|
| $C_X$ | Mono 1 | 1 | – | – | – |
| $R_X/C_X$ | | 2 | – | – | – |
| $\overline{C_D}$ | | 3 | 0.4 | – | – |
| $I_1$ | | 4 | 0.4 | – | – |
| $\overline{I_0}$ | | 5 | 0.4 | – | – |
| Q | | 6 | – | 40 | 10 |
| $\overline{Q}$ | | 7 | – | 40 | 10 |
| GND | | 8 | – | – | – |
| $\overline{Q}$ | Mono 2 | 9 | – | 40 | 10 |
| Q | | 10 | – | 40 | 10 |
| $\overline{I_0}$ | | 11 | 0.4 | – | – |
| $I_1$ | | 12 | 0.4 | – | – |
| $\overline{C_D}$ | | 13 | 0.4 | – | – |
| $R_X/C_X$ | | 14 | – | – | – |
| $C_X$ | | 15 | – | – | – |
| $V_{CC}$ | | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

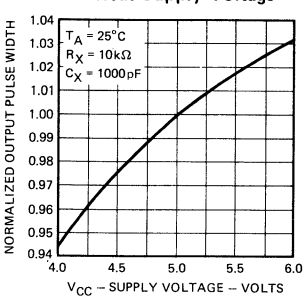
**Typical Normalized Output Pulse Width Versus Case Temperature**



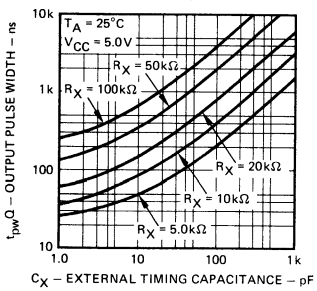

**Normalized Output Pulse Width Versus Operating Duty Cycle**



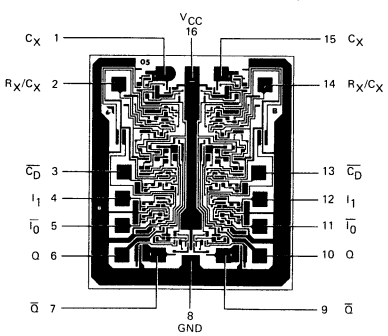

**Typical Normalized Output Pulse Width Versus Supply Voltage**




**Output Pulse Width Versus External Timing Capacitance**




**Metallization and Pad Layout**




DIE SIZE 0.062" X 0.071"

## OPERATION RULES

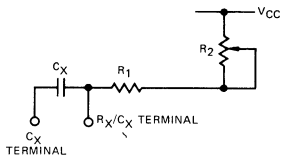
### TIMING

1. Timing components $C_X$ and $R_X$ values.

**Operating Temperature Range**

| | 0°C to 70°C | -55°C to +125°C |
|---|---|---|
| $R_X$ MIN. | 5kΩ | 5kΩ |
| $R_X$ MAX. | 100kΩ | 50kΩ |
| $C_X$ | any value | any value |

2. Remote adjustment of timing.




$R_1 + R_2 = R_X$
$R_1 \geq R_X$ MIN.
$R_2 < R_X$ MAX. $- R_1$

In the above arrangement, $R_1$ and $C_X$ should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor $R_2$ can be located remotely from the device if reasonable care is used.

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly. Note that pulse width temperature stability improves as $R_X$ increases.

4. Timing for $C_X \leq 1000$ pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

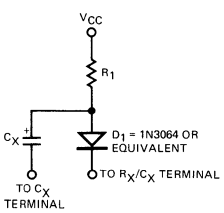
5. Timing for $C_X > 1000$ pF.

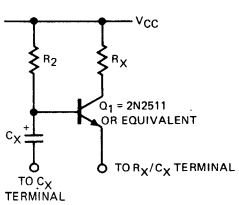
For capacitors of greater than 1000 pF in value, the output pulse width, $t_{pw}Q$, is determined by

$$t_{pw}Q = 0.30\, C_X R_X \left(1 + \frac{0.11}{R_X}\right)$$

where

$R_X$ is in kilohms
$C_X$ is in picofarads
$t_{pw}Q$ is in nanoseconds




$R_1 \leq 0.6 \times R_X$ MAX.

$R_2 < 0.7 \times h_{FEQ1} \times R_X$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as $C_X$ cannot withstand 1.0 volt reverse bias, one of the two circuit techniques shown below should be used to protect the electrolytic capacitor from the reverse voltage. The accuracy of the pulse width may be dependent on the diode (transistor) characteristics.

The output pulse width, $t_{pw}Q$ for the diode circuit modifies the previous timing equation as follows:

$$t_{pw}Q = 0.26\, C_X R_X \left(1 + \frac{0.13}{R_X}\right)$$

The output pulse width for the transistor circuit is

$$t_{pw}Q = 0.21\, C_X R_X \left(1 + \frac{0.16}{R_X}\right)$$

Notice that the transistor circuit allows values of timing resistor $R_2$ larger than the $R_X$ MIN. $< R_X <$ $R_X$ MAX. to obtain longer output pulse widths for a given $C_X$.

### TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input $\overline{I_0}$ or input $I_1$ to cause the device to trigger is 20ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width $t_{pw}Q$ timing equation as follows.

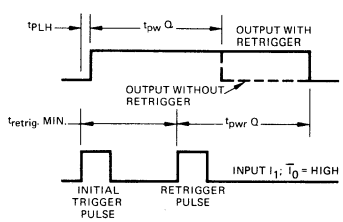
$$t_{pwr}Q = t_{pw}Q + t_{PLH}$$

where $t_{PLH}$ is the propagation delay time from the $\overline{I_0}$ or $I_1$ input to the output. Note that $t_{PLH}$ is typically 14ns and therefore becomes relatively unimportant as $t_{pw}Q$ increases.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is approximately.

$t_{retrig}$ MIN. $= 0.2\, C_X$
C is in picofarads
t is in nanoseconds




### CLEAR

A LOW on the clear inputs terminates the timing cycle. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the $I_1$ and $\overline{I_0}$ inputs.

# Am26S10 • Am26S11

## Quad Bus Transceivers

### Distinctive Characteristics

- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

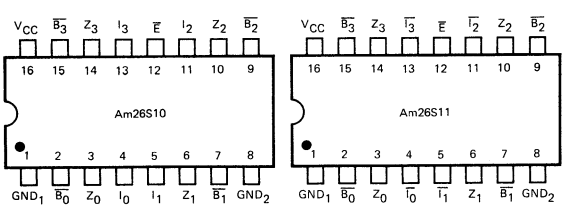
The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between $V_{CC}$ and ground at the package. Both $GND_1$ and $GND_2$ should be tied to the ground bus external to the device package.

### ORDERING INFORMATION

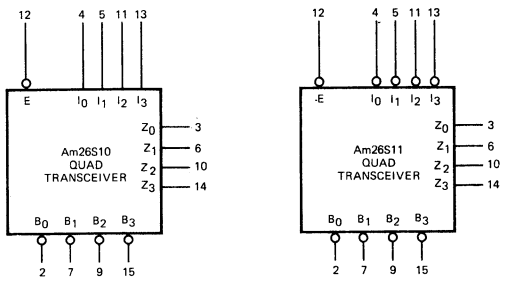
| Package Type | Temperature Range | Am26S10 Order Number | Am26S11 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM26S10PC | AM26S11PC |
| Hermetic DIP | 0°C to +70°C | AM26S10DC | AM26S11DC |
| Dice | 0°C to +70°C | AM26S10XC | AM26S11XC |
| Hermetic DIP | –55°C to +125°C | AM26S10DM | AM26S11DM |
| Hermetic Flat Pack | –55°C to +125°C | AM26S10FM | AM26S11FM |
| Dice | –55°C to +125°C | AM26S10XM | AM26S11XM |

### CONNECTION DIAGRAMS
Top Views




Note: Pin 1 is marked for orientation.

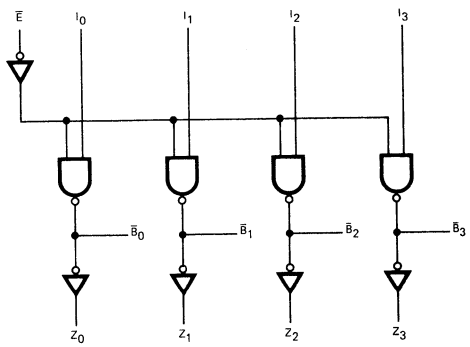
### LOGIC SYMBOLS



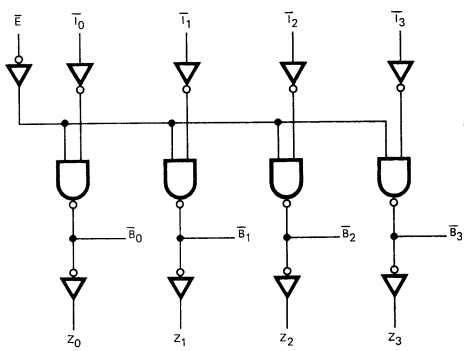

$V_{CC}$ = Pin 16
$GND_1$ = Pin 1
$GND_2$ = Pin 8

### LOGIC DIAGRAMS

**Am26S10**




**Am26S11**



## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| Output Current, Into Bus | 200 mA |
| Output Current, Into Outputs (Except Bus) | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am26S10XC, Am26S11XC $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am26S10XM, Am26S11XM $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (Receiver Outputs) | $V_{CC}$ = MIN., $I_{OH}$ = −1.0mA<br>$V_{IN}$ = $V_{IL}$ or $V_{IH}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage (Receiver Outputs) | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IL}$ or $V_{IH}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus) | Guaranteed input logical LOW for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | Enable | | | −0.36 | mA |
| | | | Data | | | −0.54 | |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | Enable | | | 20 | µA |
| | | | Data | | | 30 | |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 100 | µA |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX. (Note 3) | MIL | −20 | | −55 | mA |
| | | | COM'L | −18 | | −60 | |
| $I_{CCL}$ | Power Supply Current (All Bus Outputs LOW) | $V_{CC}$ = MAX.<br>Enable = GND | Am26S10 | | 45 | 70 | mA |
| | | | Am26S11 | | | 80 | |

## Bus Input/Output Characteristics

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. | MIL | $I_{OL}$ = 40mA | | 0.33 | 0.5 | Volts |
| | | | | $I_{OL}$ = 70mA | | 0.42 | 0.7 | |
| | | | | $I_{OL}$ = 100mA | | 0.51 | 0.8 | |
| | | | COM'L | $I_{OL}$ = 40mA | | 0.33 | 0.5 | |
| | | | | $I_{OL}$ = 70mA | | 0.42 | 0.7 | |
| | | | | $I_{OL}$ = 100mA | | 0.51 | 0.8 | |
| $I_O$ | Bus Leakage Current | $V_{CC}$ = MAX. | | $V_O$ = 0.8V | | | −50 | µA |
| | | | MIL | $V_O$ = 4.5V | | | 200 | |
| | | | COM'L | $V_O$ = 4.5V | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power Off) | $V_O$ = 4.5V | | | | | 100 | µA |
| $V_{TH}$ | Receiver Input HIGH Threshold | Bus Enable = 2.4V<br>$V_{CC}$ = MAX | MIL | | 2.4 | 2.0 | | Volts |
| | | | COM'L | | 2.25 | 2.0 | | |
| $V_{TL}$ | Receiver Input LOW Threshold | Bus Enable = 2.4V<br>$V_{CC}$ = MIN | MIL | | | 2.0 | 1.6 | Volts |
| | | | COM'L | | | 2.0 | 1.75 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## Switching Characteristics ($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data Input to Bus | Am26S10 | $R_B$ = 50Ω, $C_B$ = 50pF (Note 1) | | 10 | 15 | ns |
| $t_{PHL}$ | | | | | 10 | 15 | |
| $t_{PLH}$ | | Am26S11 | | | 12 | 19 | |
| $t_{PHL}$ | | | | | 12 | 19 | |
| $t_{PLH}$ | Enable Input to Bus | Am26S10 | | | 14 | 18 | ns |
| $t_{PHL}$ | | | | | 13 | 18 | |
| $t_{PLH}$ | | Am26S11 | | | 15 | 20 | |
| $t_{PHL}$ | | | | | 14 | 20 | |
| $t_{PLH}$ | Bus to Receiver Out | | $R_B$ = 50Ω, $R_L$ = 280Ω, $C_B$ = 50pF (Note 1), $C_L$ = 15pF | | 10 | 15 | ns |
| $t_{PHL}$ | | | | | 10 | 15 | |
| $t_r$ | Bus | | $R_B$ = 50Ω, $C_B$ = 50pF (Note 1) | 4.0 | 10 | | ns |
| $t_f$ | Bus | | | 2.0 | 4.0 | | ns |

Note 1. Includes probe and jig capacitance.

## TRUTH TABLES

**Am26S10**

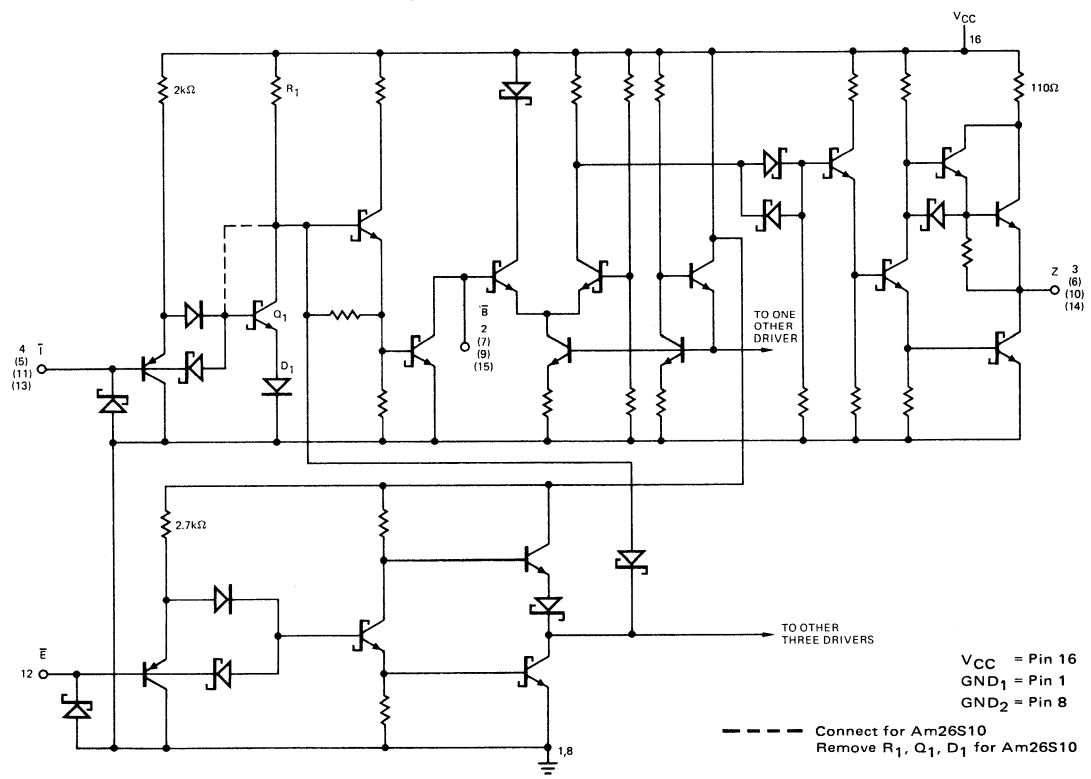
| Inputs | | Outputs | |
|---|---|---|---|
| $\overline{E}$ | I | $\overline{B}$ | Z |
| L | L | H | L |
| L | H | L | H |
| H | X | Y | $\overline{Y}$ |

**Am26S11**

| Inputs | | Outputs | |
|---|---|---|---|
| $\overline{E}$ | $\overline{I}$ | $\overline{B}$ | Z |
| L | L | L | H |
| L | H | H | L |
| H | X | Y | $\overline{Y}$ |

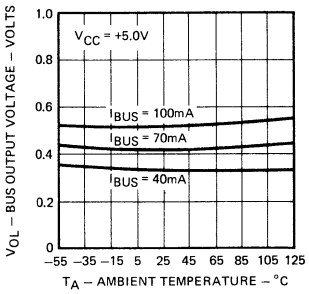
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

## Am26S10/Am26S11 SCHEMATIC DIAGRAM

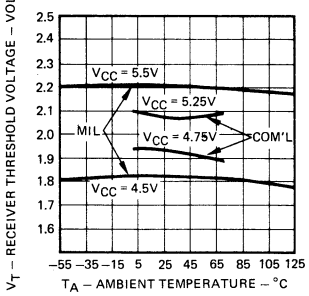


## TYPICAL PERFORMANCE CURVES

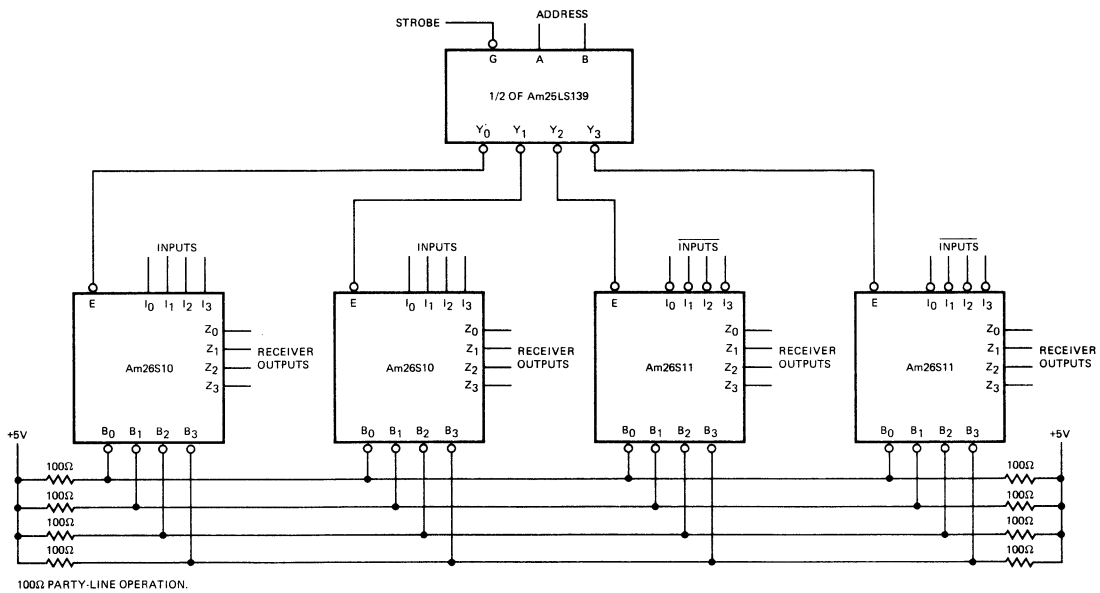
### Typical Bus Output Low Voltage Versus Ambient Temperature




### Receiver Threshold Variation Versus Ambient Temperature



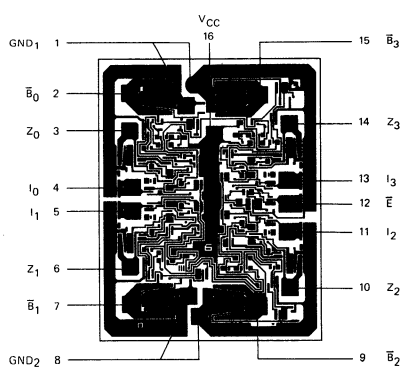

## TYPICAL APPLICATION




100Ω PARTY-LINE OPERATION.

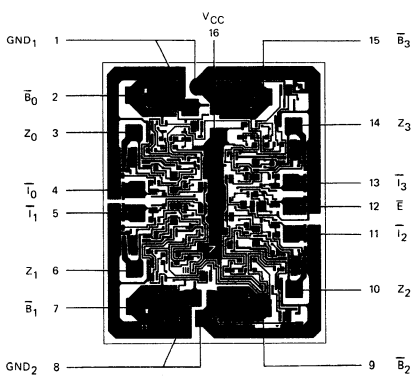
## Metallization and Pad Layout

### Am26S10




DIE SIZE 0.059" X 0.075"

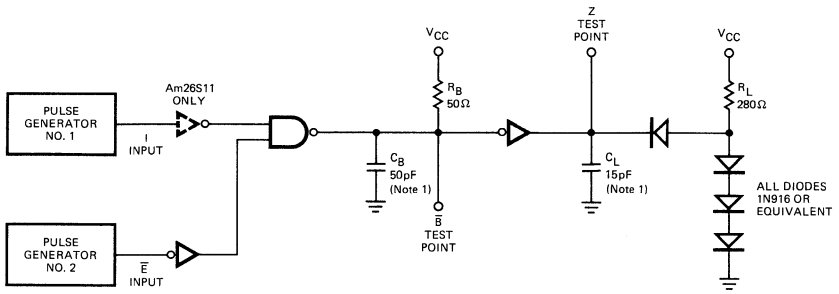
### Am26S11




DIE SIZE 0.059" X 0.075"

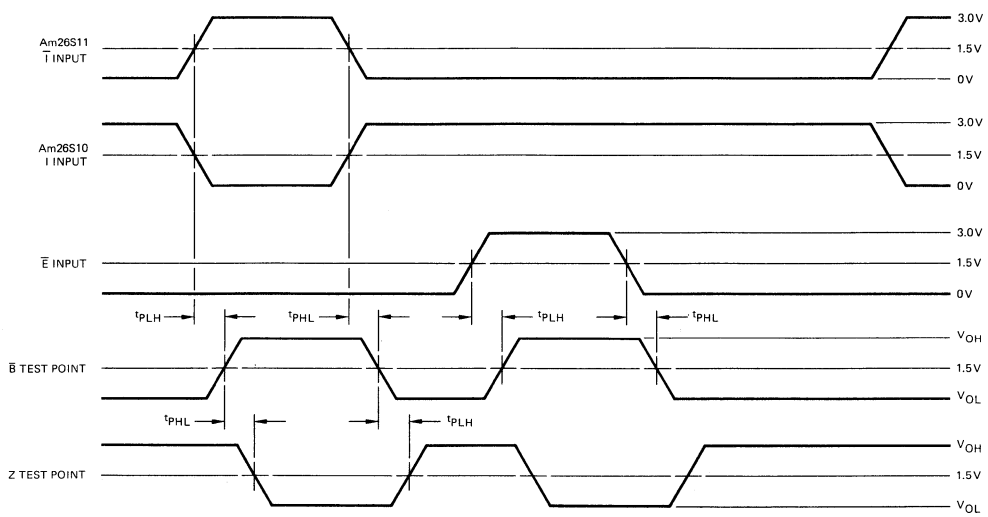
## SWITCHING CHARACTERISTICS

### TEST CIRCUIT




Note 1. Includes Probe and Jig Capacitance.

### WAVEFORMS



# Am26S12•Am26S12A

## Quad Bus Transceiver

### Distinctive Characteristics

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- 100% reliability assurance testing in compliance with MIL-STD-883
- Choice of receiver hysteresis characteristics

### FUNCTIONAL DESCRIPTION

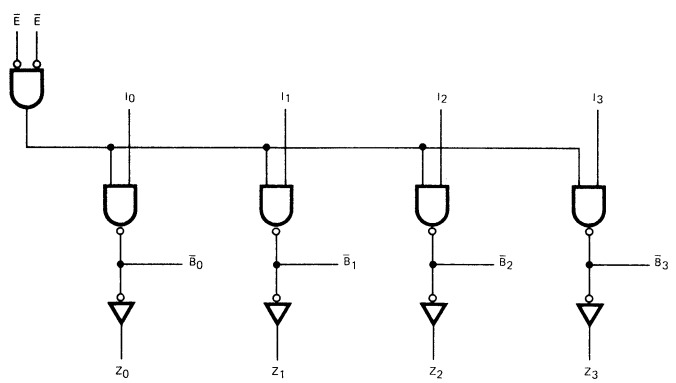
The Am26S12 • Am26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL Loads.

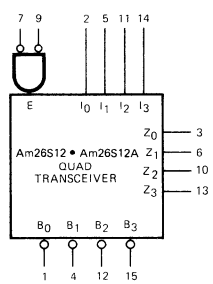
An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

### LOGIC DIAGRAM/SYMBOL



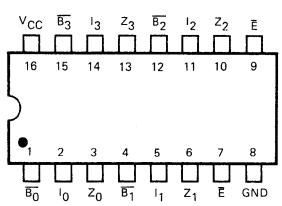




$V_{CC}$ = PIN 16
GND = Pin 8

### ORDERING INFORMATION

| Package Type | Temperature Range | Am26S12 Order Number | Am26S12A Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +75°C | AM26S12PC | AM26S12APC |
| Hermetic DIP | 0°C to +75°C | AM26S12DC | AM26S12ADC |
| Dice | 0°C to +75°C | AM26S12XC | AM26S12AXC |
| Hermetic DIP | −55°C to +125°C | AM26S12DM | AM26S12ADM |
| Flat Pak | −55°C to +125°C | AM26S12FM | AM26S12AFM |
| Dice | −55°C to +125°C | AM26S12XM | AM26S12AXM |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

4

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| Output Current, Into Outputs (BUS) | 200mA |
| Output Current, Into Outputs (Receiver) | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S12XC-Am26S12AXC $T_A$ = 0°C to +75°C $V_{CC}$ = 5.0V ±5% (COM Range)
Am26S12XM-Am26S12AXM $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIL Range) Note 1

| Parameters | Description | Test Conditions | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | 46 | 70 | mA |
| $I_{BUS}$ | Bus Leakage Current | $V_{CC}$ = MAX. or 0V; $V_{BUS}$ = 4.0V; Driver in OFF State | | | 100 | μA |

### Driver Characteristics

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ (Note 1) | Output LOW Voltage | $V_{CC}$ = MIN. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L | $I_{OL}$ = 100mA | | 0.7 | 0.8 | Volts |
| | | | MIL | $I_{OL}$ = 60mA | | 0.55 | 0.7 | Volts |
| | | | | $I_{OL}$ = 100mA | | 0.7 | 0.85 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = MAX., $V_I$ = 5.5V | | | | | 1.0 | mA |
| $I_{IH}$ | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_I$ = 2.4V | | | | 1.0 | 40 | μA |
| $I_{IL}$ | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_I$ = 0.4V | | | | −0.4 | −1.6 | mA |

### Receiver Characteristics

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −800μA $V_{IN}$ = $V_{IL}$ (Receiver) | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA $V_{IN}$ = $V_{IL}$ (Receiver) | | | 0.4 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level Threshold | $\overline{E}$ = H | Am26S12 | 1.8 | 2.0 | 2.2 | Volts |
| | | | Am26S12A | 2.05 | 2.25 | 2.45 | |
| $V_{IL}$ | Input LOW Level Threshold | $\overline{E}$ = H | Am26S12 | 1.2 | 1.4 | 1.6 | Volts |
| | | | Am26S12A | 1.0 | 1.2 | 1.4 | |
| $V_{TM}$ | Input Threshold Margin | $\overline{E}$ = H | | 0.4 | | | Volts |
| $I_{OS}$ | Output Short Circuit Current | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −20 | | −55 | mA |

Notes: 1. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.

### Switching Characteristics ($T_A$ = 25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Turn Off Delay Input to Bus | $C_{LB}$ = 15pF, $R_{LB}$ = 100Ω | | 7 | 11 | ns |
| $t_{PHL}$ | Turn On Delay Input to Bus | $C_{LB}$ = 300pF, $R_{LB}$ = 50Ω | | 14 | 21 | ns |
| $t_{PLH}$ | Turn Off Delay Enable to Bus | $C_{LB}$ = 15pF, $R_{LB}$ = 50Ω | | 10 | 15 | ns |
| $t_{PHL}$ | Turn On Delay Enable to Bus | $C_{LB}$ = 15pF, $R_{LB}$ = 50Ω | | 10 | 15 | ns |
| $t_{PLH}$ | Turn Off Delay Bus to Output | $C_L$ = 15pF | | 18 | 26 | ns |
| $t_{PHL}$ | Turn On Delay Bus to Output | $C_L$ = 15pF | | 18 | 26 | ns |

## SWITCHING CIRCUITS AND WAVEFORMS

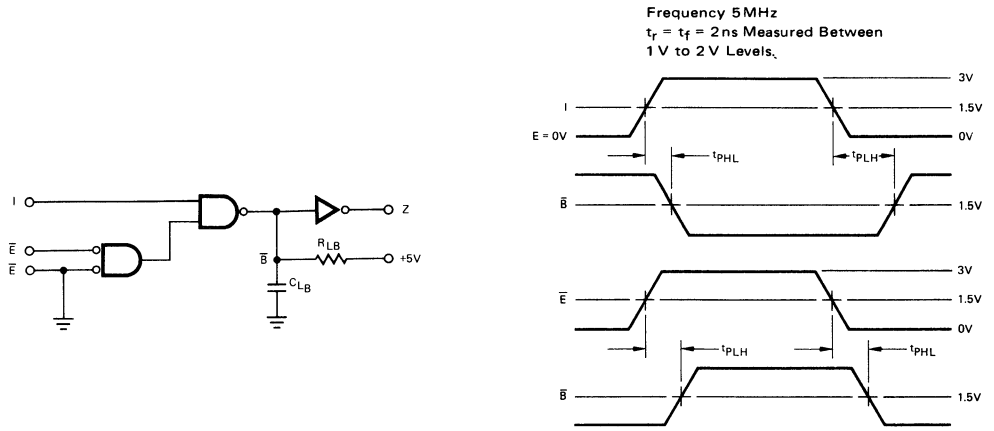



**Figure 1. Bus Propagation Delays**

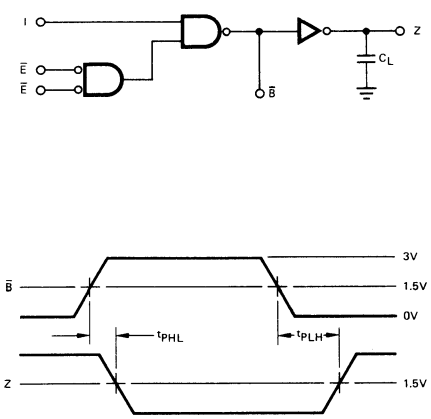



**Figure 2. Receiver Propagation Delays**

## TRUTH TABLE
## Am26S12/26S12A

| Inputs | | Outputs | |
|---|---|---|---|
| $\overline{E}$ | I | $\overline{B}$ | Z |
| L | L | H | L |
| L | H | L | H |
| H | X | Y | $\overline{Y}$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus

**Table I**

## MSI INTERFACING RULES

| Interfacing Digital Family | Equivalent Input Unit Load HIGH | LOW |
|---|---|---|
| Advanced Micro Devices 9300/2500 Series | 1 | 1 |
| FSC Series 9300 | 1 | 1 |
| TI Series 54/7400 | 1 | 1 |
| Signetics Series 8200 | 2 | 2 |
| National Series DM 75/85 | 1 | 1 |
| DTL Series 930 | 12 | 1 |

**Table II**

## PERFORMANCE CURVES

### Am26S12 Typical Receiver Input Characteristic

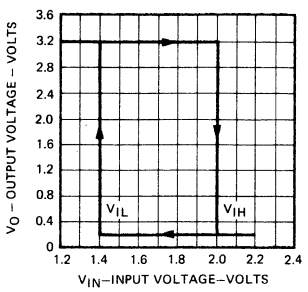



**Figure 3**

### Am26S12A Typical Receiver Input Characteristic

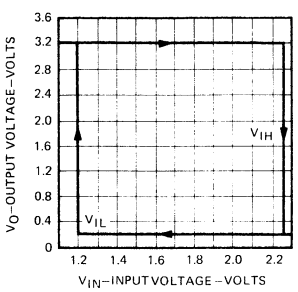



**Figure 4**

## INPUT/OUTPUT CIRCUITRY

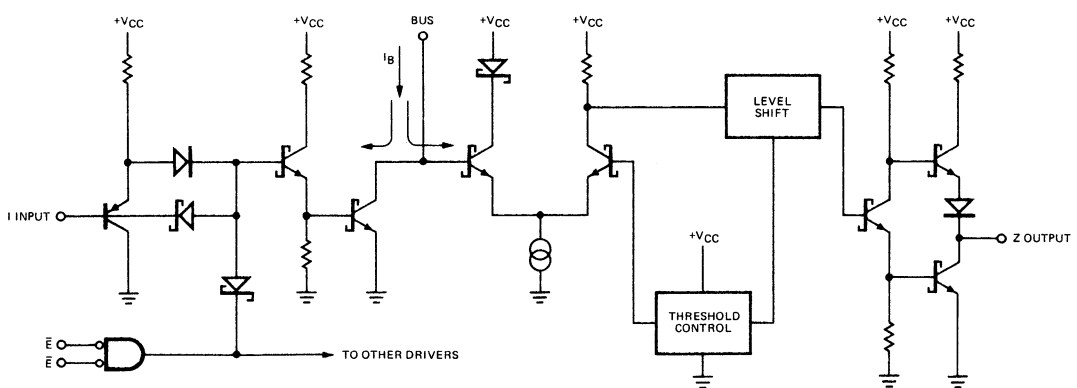



**Figure 5**

## Am26S12/26S12A APPLICATION

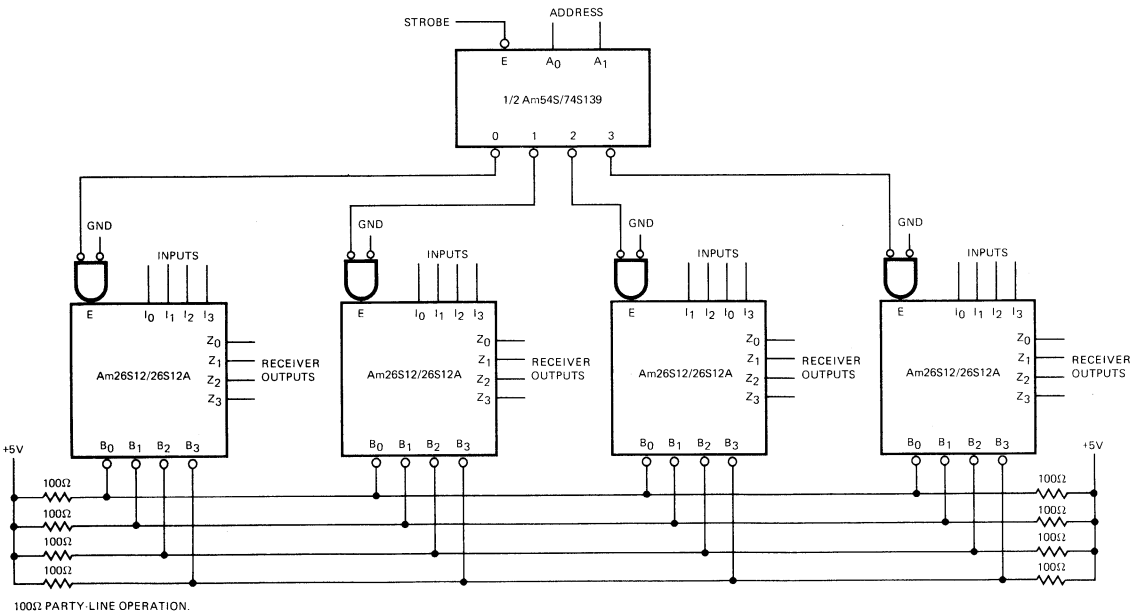
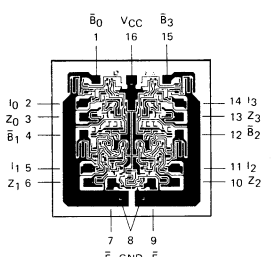



**Figure 6**

### Metallization and Pad Layout




DIE SIZE: 0.071" x 0.072"

# Am54S/74S138

## 3-Line to 8-Line Decoder/Demultiplexer

### Distinctive Characteristics

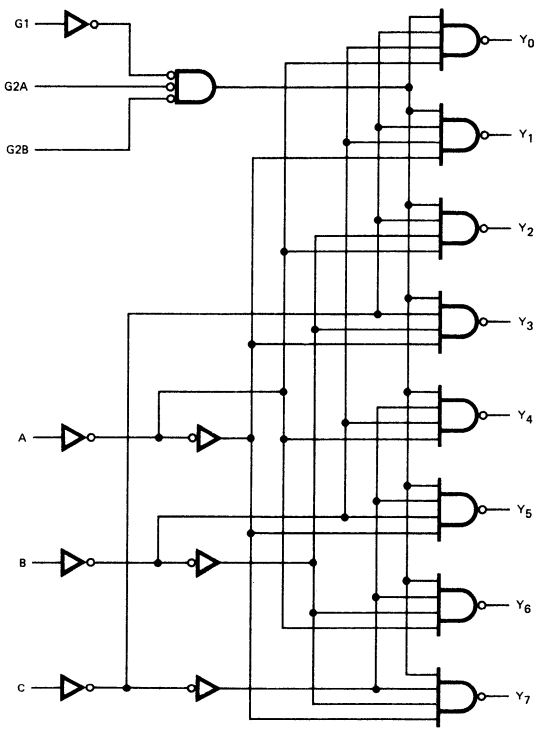
- Advanced Schottky technology
- Inverting and non-inverting enable inputs
- Useful in memory decoders and high-speed data transmission
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am54S/74S138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

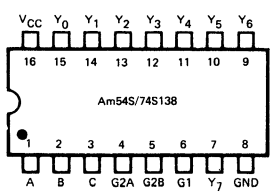
### LOGIC DIAGRAM




### ORDERING INFORMATION

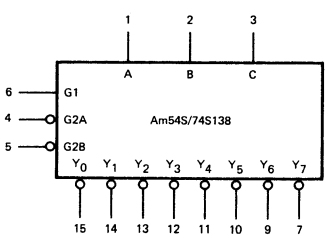
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S138N |
| Hermetic DIP | 0°C to +70°C | SN74S138J |
| Dice | 0°C to +70°C | SN74S138X |
| Hermetic DIP | −55°C to +125°C | SN54S138J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S138W |
| Dice | −55°C to +125°C | SN54S138X |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +Vcc max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S138 $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54S138 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | 49 | 74 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs enabled and open.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Two Level Delay Select to Output | $V_{CC}$ = 5V, $C_L$ = 15pF, $R_L$ = 280Ω | | 4.5 | 7 | ns |
| $t_{PHL}$ | | | | 7 | 10.5 | |
| $t_{PLH}$ | Three Level Delay Select to Output | | | 7.5 | 12 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | G2A or G2B to Output | | | 5 | 8 | ns |
| $t_{PHL}$ | | | | 7 | 11 | |
| $t_{PLH}$ | G1 to Output | | | 7 | 11 | ns |
| $t_{PHL}$ | | | | 7 | 11 | |

## FUNCTION TABLE

| Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | | Select | | | | | | | | | | |
| G1 | G2A | G2B | C | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH
L = LOW
X = Don't care

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| A | 1 | 1 | – | – |
| B | 2 | 1 | – | – |
| C | 3 | 1 | – | – |
| G2A | 4 | 1 | – | – |
| G2B | 5 | 1 | – | – |
| G1 | 6 | 1 | – | – |
| $Y_7$ | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| $Y_6$ | 9 | – | 20 | 10 |
| $Y_5$ | 10 | – | 20 | 10 |
| $Y_4$ | 11 | – | 20 | 10 |
| $Y_3$ | 12 | – | 20 | 10 |
| $Y_2$ | 13 | – | 20 | 10 |
| $Y_1$ | 14 | – | 20 | 10 |
| $Y_0$ | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## DEFINITION OF FUNCTIONAL TERMS:

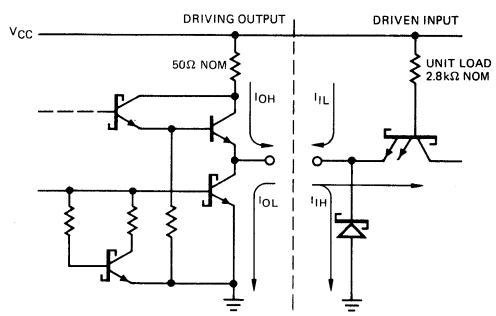
**A, B, C** Select. The three select inputs to the decoder.

**G1** The active-HIGH enable input. A LOW on the G1 input forces all Y outputs HIGH regardless of any other inputs.

**G2A, G2B** The active-LOW enable input. A HIGH on either the G2A or G2B input forces all Y outputs HIGH regardless of any other inputs.

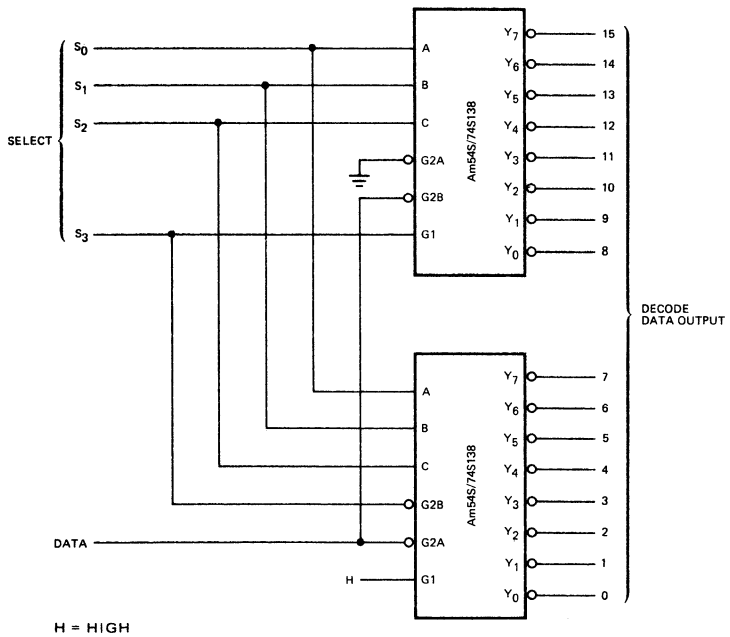
**$Y_0$, $Y_1$, $Y_2$, $Y_3$, $Y_4$, $Y_5$, $Y_6$, $Y_7$** The eight decoder outputs.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

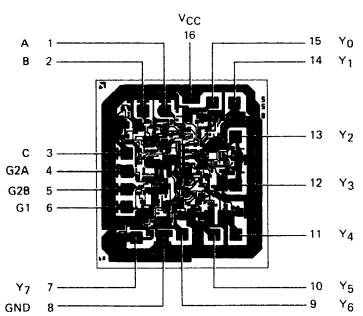
## APPLICATION




**ONE-OF-SIXTEEN DEMULTIPLEXER**

4

### Metallization and Pad Layout




DIE SIZE 0.065" X 0.070"

# Am54S/74S139 • Am93S21

## Dual 2-Line to 4-Line Decoder/Demultiplexer

### Distinctive Characteristics

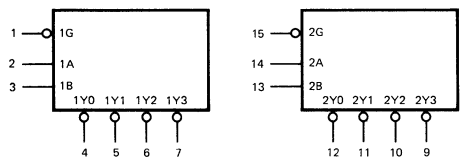
- Advanced Schottky technology
- 7.5ns typical propagation delay
- Two independent decoders/demultiplexers
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am54S/74S139 and Am93S21 are dual 2-line to 4-line decoder/demultiplexer units fabricated using advanced Schottky technology. Each decoder has two buffered select inputs A and B which are decoded to one of four Y outputs.

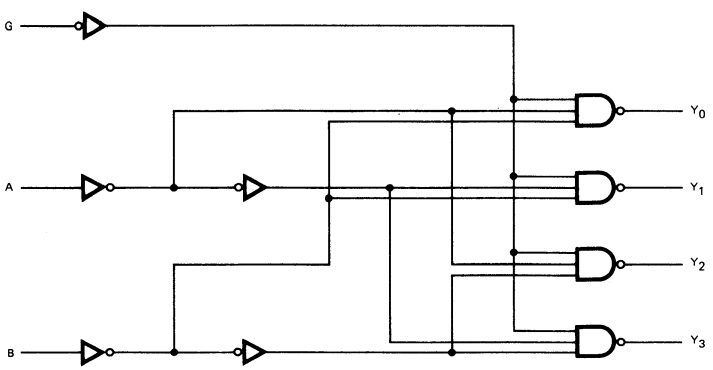
An active LOW enable can be used for gating or can be used as a data input for demultiplexing applications. When the enable is HIGH, all four Y outputs are HIGH, regardless of the A and B inputs.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

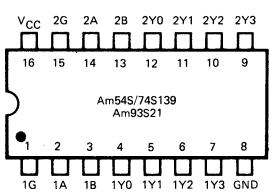
### LOGIC DIAGRAM
(One Decoder Shown)




### ORDERING INFORMATION

| Package Type | Temperature Range | Am54S/74S139 Order Number | Am93S21 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S139N | 93S21PC |
| Hermetic DIP | 0°C to +70°C | SN74S139J | 93S21DC |
| Dice | 0°C to +70°C | SN74S139X | 93S21XC |
| Hermetic DIP | −55°C to +125°C | SN54S139J | 93S21DM |
| Hermetic Flat Pak | −55°C to +125°C | SN54S139W | 93S21FM |
| Dice | −55°C to +125°C | SN54S139X | 93S21XM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −5.0V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am74S139, Am93S21XC | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ±5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am54S139, Am93S21XM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ±10% (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = − 18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | 60 | 90 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured with all outputs enabled and open.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Select to Output, 2 Levels of Delay | $V_{CC}$ = 5.0V, $R_L$ = 280Ω, $C_L$ = 15pF | | 5 | 7.5 | ns |
| $t_{PHL}$ | | | | 6.5 | 10 | |
| $t_{PLH}$ | Select to Output, 3 Levels of Delay | | | 7 | 12 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | Enable to Output, 2 Levels of Delay | | | 5 | 8 | ns |
| $t_{PHL}$ | | | | 6.5 | 10 | |

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE G | SELECT B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = HIGH
L = LOW
X = Don't Care

## DEFINITION OF FUNCTIONAL TERMS

**A, B** Select. The two select inputs to the decoder.

**G** Enable. The enable input to the decoder. A HIGH input forces all four Y outputs HIGH regardless of the A and B inputs.

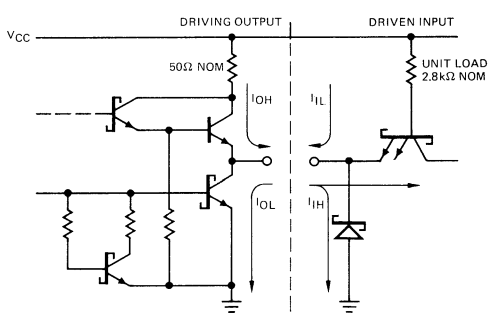
**$Y_0$, $Y_1$, $Y_2$, $Y_3$** The four decoder outputs.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| 1G | 1 | 1 | – | – |
| 1A | 2 | 1 | – | – |
| 1B | 3 | 1 | – | – |
| 1Y0 | 4 | – | 20 | 10 |
| 1Y1 | 5 | – | 20 | 10 |
| 1Y2 | 6 | – | 20 | 10 |
| 1Y3 | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| 2Y3 | 9 | – | 20 | 10 |
| 2Y2 | 10 | – | 20 | 10 |
| 2Y1 | 11 | – | 20 | 10 |
| 2Y0 | 12 | – | 20 | 10 |
| 2B | 13 | 1 | – | – |
| 2A | 14 | 1 | – | – |
| 2G | 15 | 1 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

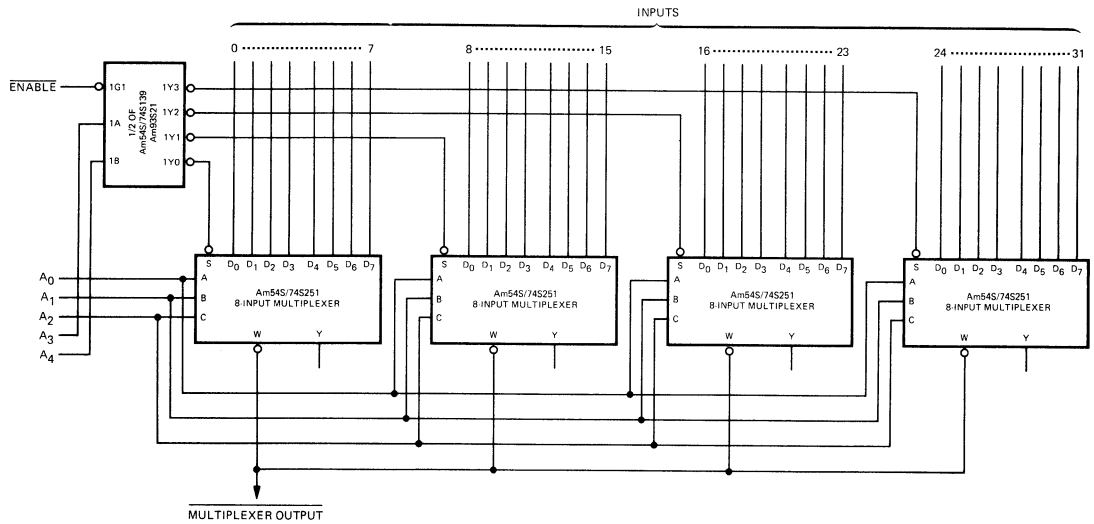
## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

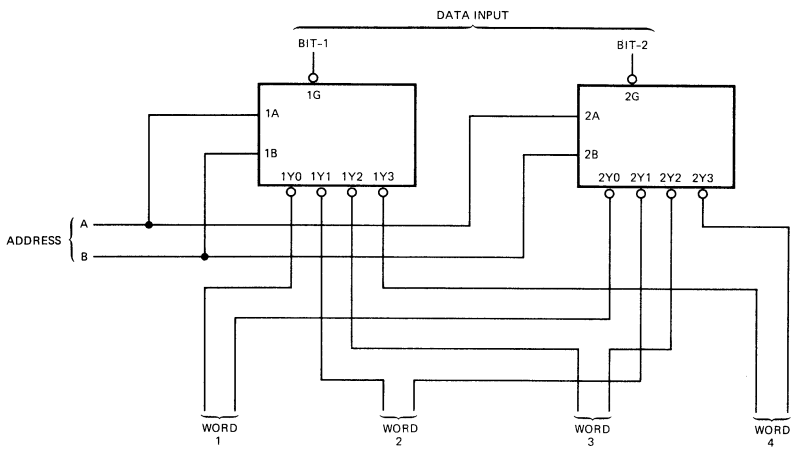



Note: Actual current flow direction shown.

## APPLICATIONS

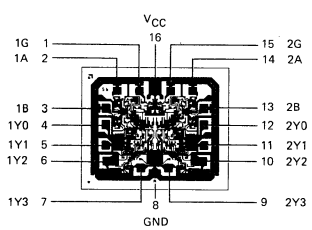
### 32-Input Multiplexer




Data routing using one Am54S/74S139 as a demultiplexer for two bits.

### Metallization and Pad Layout




DIE SIZE 0.073" X 0.060"

# Am54S/74S151•Am54S/74S251

## Eight-Input Multiplexers

### Distinctive Characteristics

- Advanced Schottky technology
- Switches one of eight inputs to two complementary outputs
- Three-state output on Am54S/74S251 for bus organized systems
- 100% reliability assurance testing in compliance with MIL-STD-883

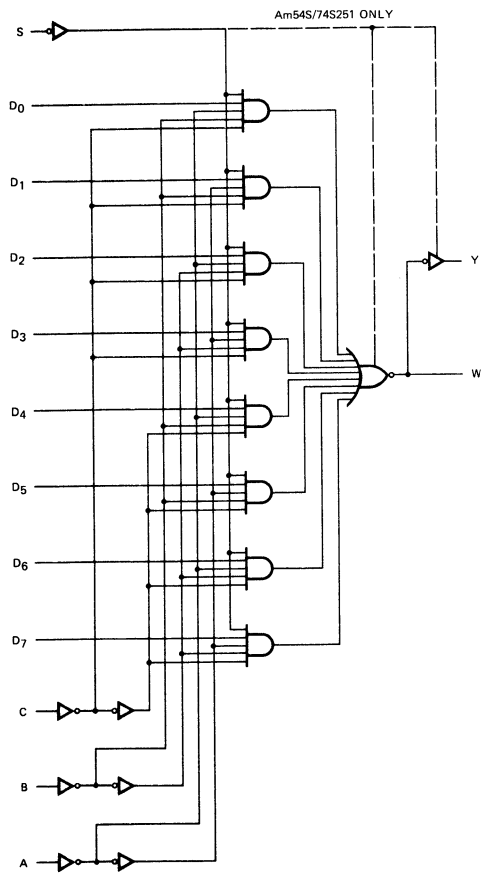
### FUNCTIONAL DESCRIPTION

The Am54S/74S151 and the Am54S/74S251 are eight-input multiplexers that switch one of eight inputs onto the inverting and non-inverting outputs under the control of a three-bit select code. The inverting output is one gate delay faster than the non-inverting output.

The Am54S/74S151 provides an active-LOW strobe. When the strobe is HIGH, the inverting output (W) is HIGH and the non-inverting output (Y) is LOW.

The Am54S/74S251 features a three-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

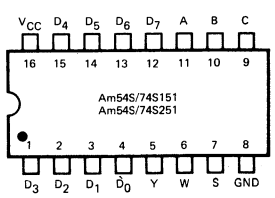
### LOGIC DIAGRAM




### ORDERING INFORMATION

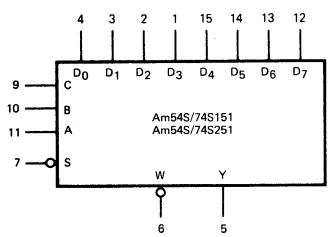
| Package Type | Temperature Range | Am54S/74S151 Order Number | Am54S/74S251 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S151N | SN74S251N |
| Hermetic DIP | 0°C to +70°C | SN74S151J | SN74S251J |
| Dice | 0°C to +70°C | SN74S151X | SN74S251X |
| Hermetic DIP | −55°C to +125°C | SN54S151J | SN54S251J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S151W | SN54S251W |
| Dice | −55°C to +125°C | SN54S151X | SN54S251X |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

## MAXIMUM RATINGS (Above which the useful life may be impaired).

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to + $V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Output | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S151, Am74S251 $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V

Am54S151, Am54S251 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 54S151 | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −1mA | 2.5 | 3.4 | | Volts |
| | | 74S151 | | | 2.7 | 3.4 | | |
| | | 54S251 | | $I_{OH}$ = −2mA | 2.4 | 3.4 | | |
| | | 74S251 | | $I_{OH}$ = −6.5mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ = MIN., $I_{OL}$ = 20mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 50 | µA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1 | mA |
| $I_{O(off)}$ | Off-State (High-Impedance) Output Current (S251 only) | | $V_{CC}$ = MAX. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $V_O$ = 2.4V | | | 50 | µA |
| | | | | $V_O$ = 0.5V | | | −50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. (Note 5) | S151 | | 45 | 70 | mA |
| | | | | S251 | | 55 | 85 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured with all outputs open and all inputs at 4.5V.

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, or C to Y; 4 Levels of Delay (S151 only) | $V_{CC}$ = 5.0V, $R_L$ = 280Ω, $C_L$ = 15 pF | | 12 | 18 | ns |
| $t_{PHL}$ | | | | 12 | 18 | |
| $t_{PLH}$ | A, B, or C to Y; 4 Levels of Delay (S251 only) | | | 12 | 18 | ns |
| $t_{PHL}$ | | | | 13 | 19.5 | |
| $t_{PLH}$ | A, B, or C to W; 3 Levels of Delay | | | 10 | 15 | ns |
| $t_{PHL}$ | | | | 9 | 13.5 | |
| $t_{PLH}$ | Any D to Y | | | 8 | 12 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | Any D to W | | | 4.5 | 7 | ns |
| $t_{PHL}$ | | | | 4.5 | 7 | |
| $t_{PLH}$ | Strobe to Y (S151 only) | | | 11 | 16.5 | ns |
| $t_{PHL}$ | | | | 12 | 18 | |
| $t_{PLH}$ | Strobe to W (S151 only) | | | 9 | 13 | ns |
| $t_{PHL}$ | | | | 8.5 | 12 | |
| $t_{ZH}$ | Output Enable to Y (S251 only) | $V_{CC}$ = 5.0V, $R_L$ = 280Ω, $C_L$ = 15pF | | 13 | 19.5 | ns |
| $t_{ZL}$ | | | | 14 | 21 | |
| $t_{ZH}$ | Output Enable to W (S251 only) | | | 13 | 19.5 | ns |
| $t_{ZL}$ | | | | 14 | 21 | |
| $t_{HZ}$ | Output Enable to Y (S251 only) | $V_{CC}$ = 5.0V, $R_L$ = 280Ω, $C_L$ = 5 pF | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | | | | 9 | 14 | |
| $t_{HZ}$ | Output Enable to W (S251 only) | | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | | | | 9 | 14 | |

## FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| SELECT | | | S151 Strobe | S251 Output Control | S151 Output | | S251 Output | |
| C | B | A | S | S | Y | W | Y | W |
| X | X | X | H | H | L | H | Z | Z |
| L | L | L | L | L | $D_0$ | $\overline{D}_0$ | $D_0$ | $\overline{D}_0$ |
| L | L | H | L | L | $D_1$ | $\overline{D}_1$ | $D_1$ | $\overline{D}_1$ |
| L | H | L | L | L | $D_2$ | $\overline{D}_2$ | $D_2$ | $\overline{D}_2$ |
| L | H | H | L | L | $D_3$ | $\overline{D}_3$ | $D_3$ | $\overline{D}_3$ |
| H | L | L | L | L | $D_4$ | $\overline{D}_4$ | $D_4$ | $\overline{D}_4$ |
| H | L | H | L | L | $D_5$ | $\overline{D}_5$ | $D_5$ | $\overline{D}_5$ |
| H | H | L | L | L | $D_6$ | $\overline{D}_6$ | $D_6$ | $\overline{D}_6$ |
| H | H | H | L | L | $D_7$ | $\overline{D}_7$ | $D_7$ | $\overline{D}_7$ |

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

$D_0$–$D_7$ = The output will follow the HIGH-level or LOW-level of the selected input.

$\overline{D}_0$–$\overline{D}_7$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

## DEFINITION OF FUNCTIONAL TERMS

**A, B, C** The three select inputs of the multiplexer.

**$D_0$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$, $D_6$, $D_7$** The eight data inputs of the multiplexer.

**Y** The true multiplexer output.

**W** The complement multiplexer output.

**S** Strobe. On the Am54S/74S151, a HIGH on the strobe forces the Y output LOW and the W output HIGH.

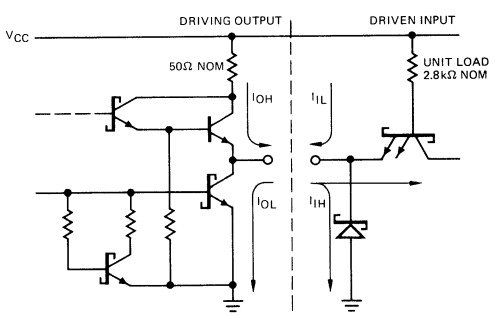
**S** Output Control. On the Am54S/74S251, a HIGH on the output control (or strobe) forces both the W and Y outputs to the high-impedance (off) state.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $D_3$ | 1 | 1 | – | – |
| $D_2$ | 2 | 1 | – | – |
| $D_1$ | 3 | 1 | – | – |
| $D_0$ | 4 | 1 | – | – |
| Y | 5 | – | 20 | 10 |
| W | 6 | – | 20 | 10 |
| S | 7 | 1 | – | – |
| GND | 8 | – | – | – |
| C | 9 | 1 | – | – |
| B | 10 | 1 | – | – |
| A | 11 | 1 | – | – |
| $D_7$ | 12 | 1 | – | – |
| $D_6$ | 13 | 1 | – | – |
| $D_5$ | 14 | 1 | – | – |
| $D_4$ | 15 | 1 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

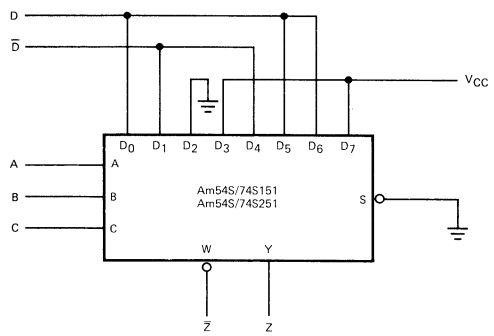
## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

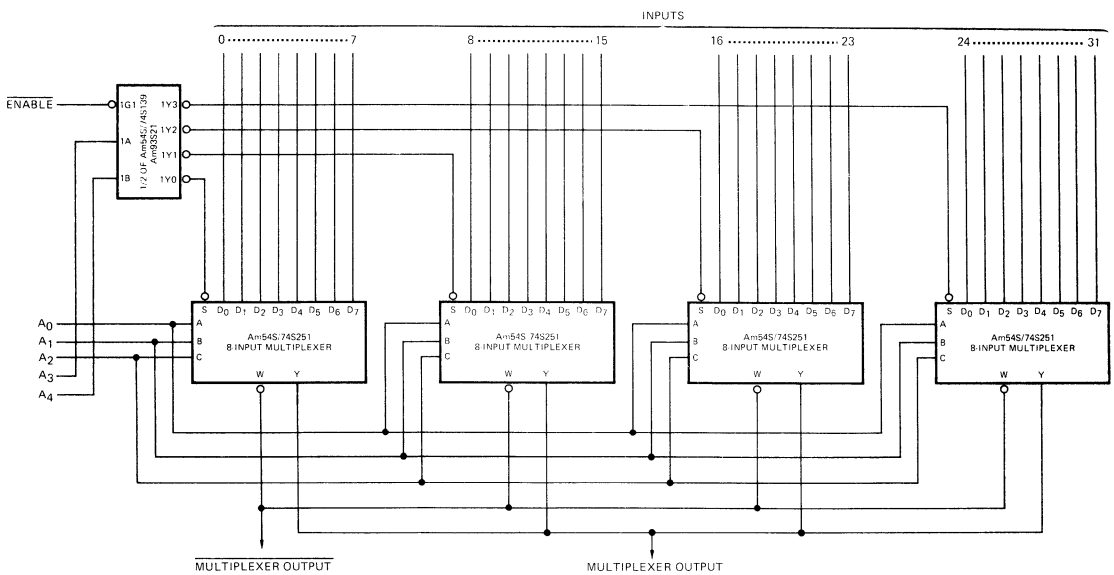
# APPLICATIONS

## LOGIC FUNCTION GENERATION



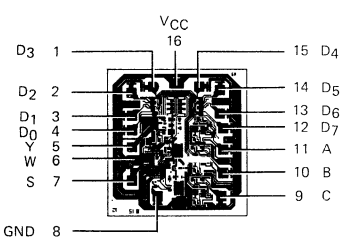

$$Z = \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + A\overline{C}D + AB + AC\overline{D} + BC\overline{D}$$

## 32-INPUT MULTIPLEXER

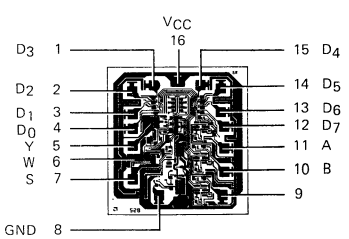



## Metallization and Pad Layout

### Am54S/74S151




### Am54S/74S251




DIE SIZE: 0.064" X 0.067"

# Am54S/74S153 • Am54S/74S253

## Dual 4-Line To 1-Line Data Selectors/Multiplexers

### Distinctive Characteristics

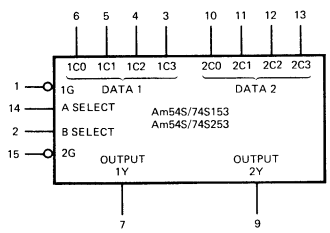
- Permits multiplexing from N lines to 1 line.
- Performs parallel-to-serial conversion.
- Am54S/74S253 provides three-state outputs for data bus organization.
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

These dual four-input multiplexers provide the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am54S/74S153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

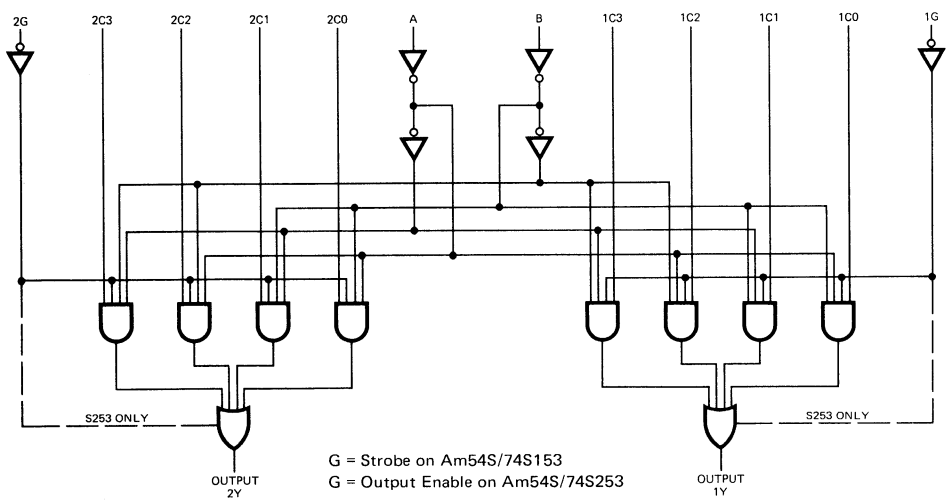
The Am54S/74S253 features a three-state output to interface with bus-organized systems. Each section of the Am54S/74S253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAM

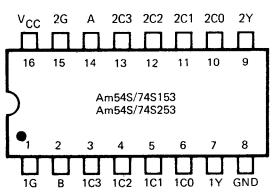



G = Strobe on Am54S/74S153
G = Output Enable on Am54S/74S253

### ORDERING INFORMATION

| Package Type | Temperature Range | Am54S/74S153 Order Number | Am54S/74S253 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S153N | SN74S253N |
| Hermetic DIP | 0°C to +70°C | SN74S153J | SN74S253J |
| Dice | 0°C to +70°C | SN74S153X | SN74S253X |
| Hermetic DIP | −55°C to +125°C | SN54S153J | SN54S253J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S153W | SN54S253W |
| Dice | −55°C to +125°C | SN54S153X | SN54S253X |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S153, Am74S253 $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am54S153, Am54S253 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 54S153 | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −1 mA | 2.5 | 3.4 | | Volts |
| | | 74S153 | | | 2.7 | 3.4 | | |
| | | 54S253 | | $I_{OH}$ = −2 mA | 2.4 | 3.4 | | |
| | | 74S253 | | $I_{OH}$ = −6.5 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ = MIN., $I_{OL}$ = 20 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN}$ = −18 mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | µA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1 | mA |
| $I_O$ | Off-State (HIGH Impedance) Output Current Am54S/74S253 Only | | $V_{CC}$ = MAX. | $V_O$ = 2.4 V | | | 50 | µA |
| | | | | $V_O$ = 0.5 V | | | −50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. (Note 5) | S153 | | 45 | 70 | mA |
| | | | | S253 | | 55 | 85 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured with all outputs open and all inputs grounded.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | | $V_{CC}$ = 5.0 V, $R_L$ = 280Ω, $C_L$ = 15 pF | | 6 | 9 | ns |
| $t_{PHL}$ | | | | | 6 | 9 | |
| $t_{PLH}$ | Select to Output | | | | 11.5 | 18 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | |
| $t_{PLH}$ | Strobe to Output | S153 | | | 10 | 15 | ns |
| $t_{PHL}$ | | S153 | | | 9 | 13.5 | |
| $t_{ZH}$ | Output Control to Output | S253 | $V_{CC}$ = 5.0 V, $R_L$ = 280Ω, $C_L$ = 15 pF | | 13 | 19.5 | ns |
| $t_{ZL}$ | | S253 | | | 14 | 21 | |
| $t_{HZ}$ | Output Control to Output | S253 | $V_{CC}$ = 5.0 V, $R_L$ = 280Ω, $C_L$ = 5 pF | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | | S253 | | | 9 | 14 | |

## FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|
| Select | | Data | | | | S153 Strobe | S253 Output Control | S153 Output | S253 Output |
| B | A | $C_0$ | $C_1$ | $C_2$ | $C_3$ | G | G | Y | Y |
| X | X | X | X | X | X | H | H | L | Z |
| L | L | L | X | X | X | L | L | L | L |
| L | L | H | X | X | X | L | L | H | H |
| L | H | X | L | X | X | L | L | L | L |
| L | H | X | H | X | X | L | L | H | H |
| H | L | X | X | L | X | L | L | L | L |
| H | L | X | X | H | X | L | L | H | H |
| H | H | X | X | X | L | L | L | L | L |
| H | H | X | X | X | H | L | L | H | H |

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
Note: A & B are common to both 4 input multiplexers.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| 1G | 1 | 1 | – | – |
| B | 2 | 1 | – | – |
| 1C3 | 3 | 1 | – | – |
| 1C2 | 4 | 1 | – | – |
| 1C1 | 5 | 1 | – | – |
| 1C0 | 6 | 1 | – | – |
| 1Y | 7 | – | 20* | 10 |
| GND | 8 | – | – | – |
| 2Y | 9 | – | 20* | 10* |
| 2C0 | 10 | 1 | – | – |
| 2C1 | 11 | 1 | – | – |
| 2C2 | 12 | 1 | – | – |
| 2C3 | 13 | 1 | – | – |
| A | 14 | 1 | – | – |
| 2G | 15 | 1 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined at 50μA measured at 2.7V HIGH and -2.0 mA measured at 0.5V LOW.

* 20 for the Am54S/74S153
40 for the Am54S253
130 for the Am74S253

## DEFINITION OF FUNCTIONAL TERMS:

**$1C_i$, $2C_i$** Data Inputs. The four data inputs to each multiplexer; i = 0, 1, 2, and 3.

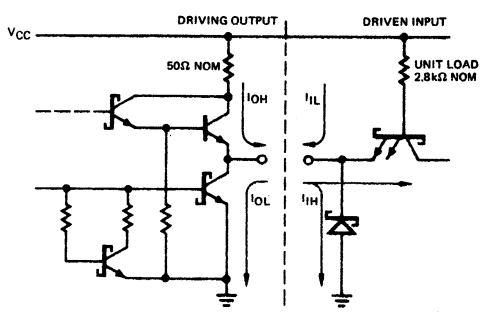
**1Y, 2Y** Multiplexer Outputs. The output of each four-input multiplexer.

**A, B** Select Inputs. The inputs used to determine which of the four data inputs are selected for the output.

**$\overline{G}$** (Am54S/74S153) Strobe. An active-LOW strobe used to enable the output. A HIGH level input forces the output LOW regardless of the other inputs.

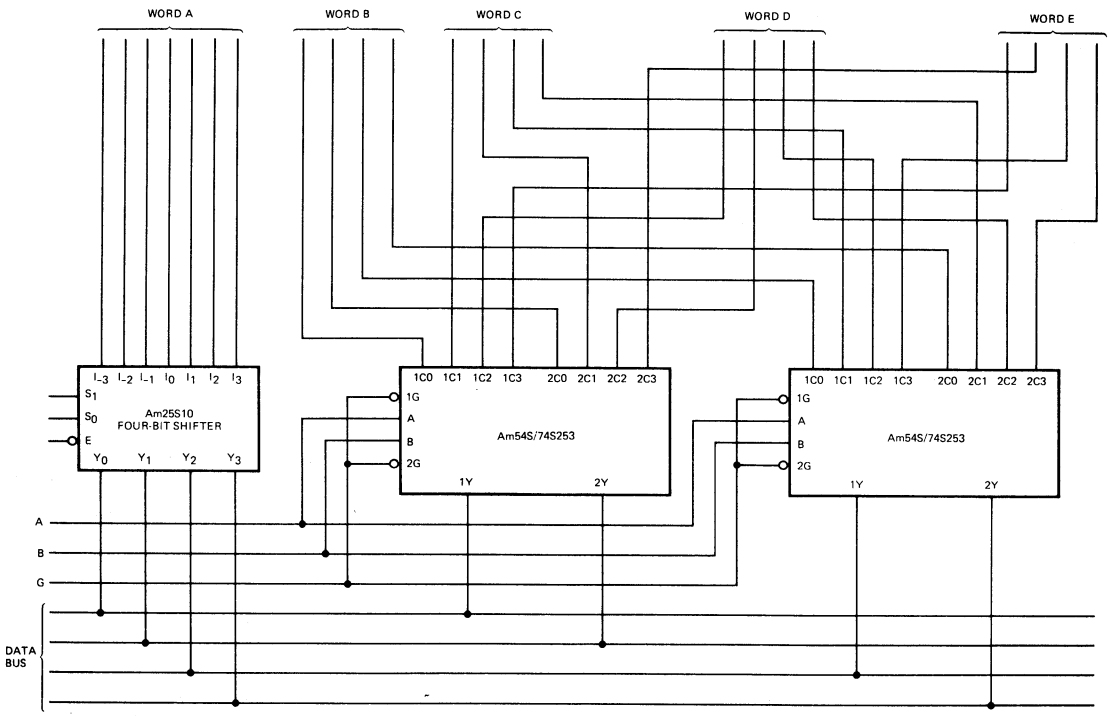
**G** (Am54S/74S253) Output Control. An active-LOW three-state control used to enable the output. A HIGH level input forces the output to the high-impedance (off) state.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown

## APPLICATIONS

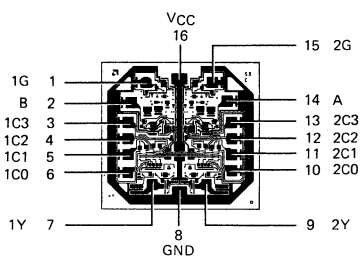



Am54S/74S253 Dual 4-Input Multiplexer in a Bus-Organized System

4

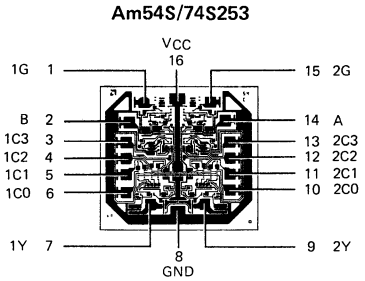
### Metallization and Pad Layout

**Am54S/74S153**




DIE SIZE: 0.059" X 0.062"

**Am54S/74S253**




DIE SIZE: 0.059" X 0.062"

# Am54S/74S157 • Am54S/74S158 • Am93S22

## Quadruple 2-Line To 1-Line Data Selectors/ Multiplexers

### Distinctive Characteristics

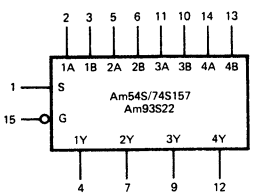
- Schottky clamp provides improved A-C performance.
- Selects four of eight data inputs with single select line and over-riding strobe.
- Inverting or non-inverting data output configurations.
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

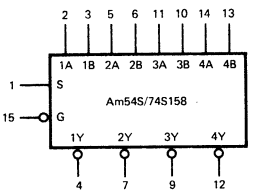
These data selectors/multiplexers are used to select a 4-bit word from one of two sources. The four outputs at the Am54S/74S157 • Am93S22 present true data with respect to the input data. The four outputs of the Am54S/74S158 present inverted data with respect to the inputs and also minimize propagation delay. A common active-HIGH strobe (active-LOW enable) is provided on all devices.

A single select line, S, is used to select one of the two multiplexer input words. When the select is LOW, the A input word is present at the output. When the select is HIGH, the B input word is present at the output.

### LOGIC SYMBOLS



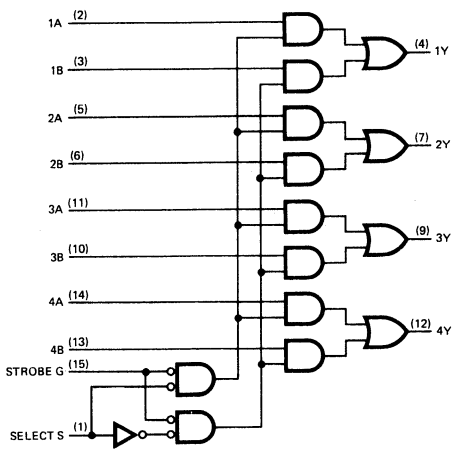

$V_{CC}$ = Pin 16
GND = Pin 8



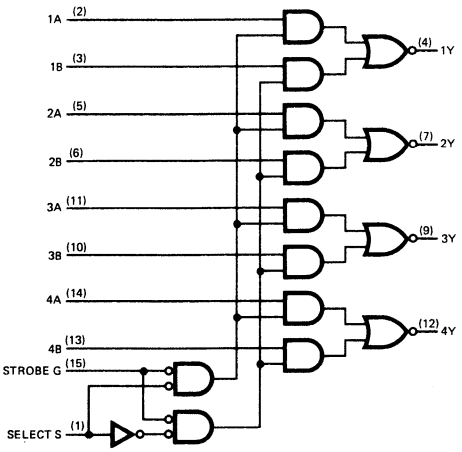

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

Am54S/74S157 • Am93S22



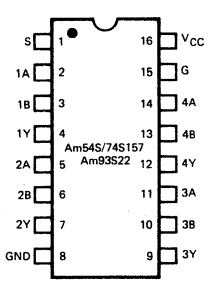

Am54S/74S158

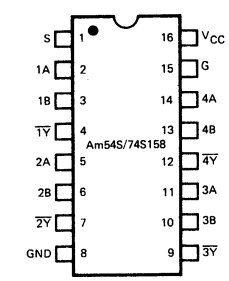



### ORDERING INFORMATION

| Part Number | Package Type | Temperature Range | Order Number |
|---|---|---|---|
| Am54S/ 74S157 | Molded DIP | 0°C to +70°C | SN74S157N |
| | Hermetic DIP | 0°C to +70°C | SN74S157J |
| | Dice | 0°C to +70°C | SN74S157X |
| | Hermetic DIP | −55°C to +125°C | SN54S157J |
| | Hermetic Flat Pak | −55°C to +125°C | SN54S157W |
| | Dice | −55°C to +125°C | SN54S157X |
| Am54S/ 74S158 | Molded DIP | 0°C to +70°C | SN74S158N |
| | Hermetic DIP | 0°C to +70°C | SN74S158J |
| | Dice | 0°C to +70°C | SN74S158X |
| | Hermetic DIP | −55°C to +125°C | SN54S158J |
| | Hermetic Flat Pak | −55°C to +125°C | SN54S158W |
| | Dice | −55°C to +125°C | SN54S158X |
| Am93S22 | Molded DIP | 0°C to +70°C | 93S22PC |
| | Hermetic DIP | 0°C to +70°C | 93S22DC |
| | Dice | 0°C to +70°C | 93S22XC |
| | Hermetic DIP | −55°C to +125°C | 93S22DM |
| | Hermetic Flat Pak | −55°C to +125°C | 93S22FM |
| | Dice | −55°C to +125°C | 93S22XM |

### CONNECTIONS DIAGRAMS
Top Views




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S157, Am74S158, Am93S22XC $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54S157, Am54S158, Am93S22XM $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | | $V_{CC}$ = MIN., $I_{OH}$ = −1mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | S or G | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −4 | mA |
| | | A or B | | | | | −2 | |
| $I_{IH}$ (Note 3) | Input HIGH Current | S or G | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 100 | µA |
| | | A or B | | | | | 50 | |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | | $V_{CC}$ = MAX. (Note 5) | S157 | | 50 | 78 | mA |
| | | | | S158 | | 39 | 61 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured with all outputs open and 4.5V applied to all inputs.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | S157 | $V_{CC}$ = 5.0V, $C_L$ = 15pF, $R_L$ = 280Ω | | 5 | 7.5 | ns |
| | | S158 | | | 4 | 6 | |
| $t_{PHL}$ | Data to Output | S157 | | | 4.5 | 6.5 | ns |
| | | S158 | | | 4 | 6 | |
| $t_{PLH}$ | Strobe to Output | S157 | | | 8.5 | 12.5 | ns |
| | | S158 | | | 6.5 | 11.5 | |
| $t_{PHL}$ | Strobe to Output | S157 | | | 7.5 | 12 | ns |
| | | S158 | | | 7 | 12 | |
| $t_{PLH}$ | Select to Output | S157 | | | 9.5 | 15 | ns |
| | | S158 | | | 8 | 12 | |
| $t_{PHL}$ | Select to Output | S157 | | | 9.5 | 15 | ns |
| | | S158 | | | 8 | 12 | |

## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| Strobe G | Select S | Data A | Data B | S157 Y | S158 Y |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = HIGH
L = LOW
X = Don't Care

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| S | 1 | 2 | – | – |
| 1A | 2 | 1 | – | – |
| 1B | 3 | 1 | – | – |
| 1Y | 4 | – | 20 | 10 |
| 2A | 5 | 1 | – | – |
| 2B | 6 | 1 | – | – |
| 2Y | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| 3Y | 9 | – | 20 | 10 |
| 3B | 10 | 1 | – | – |
| 3A | 11 | 1 | – | – |
| 4Y | 12 | – | 20 | 10 |
| 4B | 13 | 1 | – | – |
| 4A | 14 | 1 | – | – |
| G | 15 | 2 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## DEFINITION OF FUNCTIONAL TERMS

**1A, 2A, 3A, 4A** The data inputs for the 4-bits of the A word.

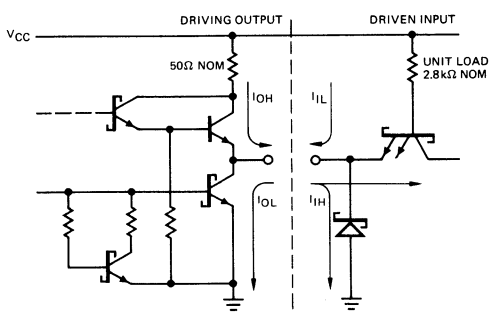
**1B, 2B, 3B, 4B** The data inputs for the 4-bits of the B word.

**1Y, 2Y 3Y, 4Y** The four outputs of the multiplexer.

**G Strobe** When the strobe is HIGH, the four outputs of the Am54S/74S157 (Am93S22) are LOW and the outputs of the Am54S/74S158 are HIGH. When the strobe is LOW, the devices are enable to pass data.

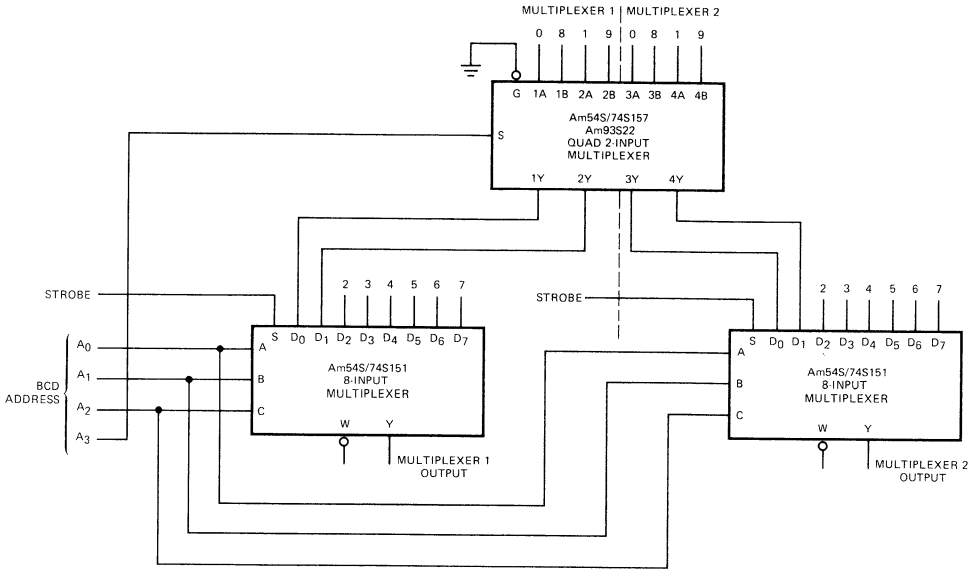
**S Select** When the select input is LOW, the A word is present at the output. When the select input is HIGH, the B word is present at the output.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## APPLICATION



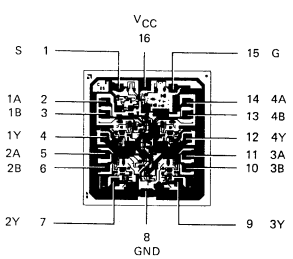

**Dual 10-Input Multiplexer**

Two 10-input multiplexers are shown above with the select lines common to the two multiplexers. Inputs are selected by an 8421 BCD Address.

4

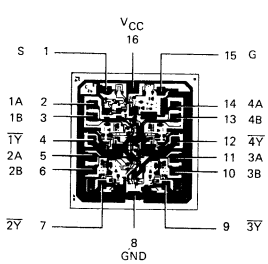
### Metallization and Pad Layouts

**Am54S/74S157**




DIE SIZE 0.065" X 0.069"

**Am54S/74S158**




DIE SIZE 0.065" X 0.069"

# Am54S/74S160 • Am54S/74S161

## BCD Decade/Four-Bit Binary Counters

### Distinctive Characteristics

- Fully synchronous counting
- Fully synchronous parallel loading
- Edge-triggered clock action
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

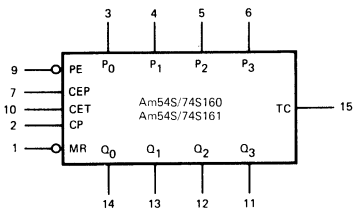
### FUNCTIONAL DESCRIPTION

The Am54S/74S160 and Am54S/74S161 are fully synchronous 4-bit decimal and binary counters. With the parallel enable ($\overline{PE}$) LOW, data on the $P_0$-$P_3$ inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am54S/74S160 and 1111 for the Am54S/74S161) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both counters have an asynchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW independent of all other inputs. The only requirements on the $\overline{PE}$, CEP, CET and $P_0$-$P_3$ inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

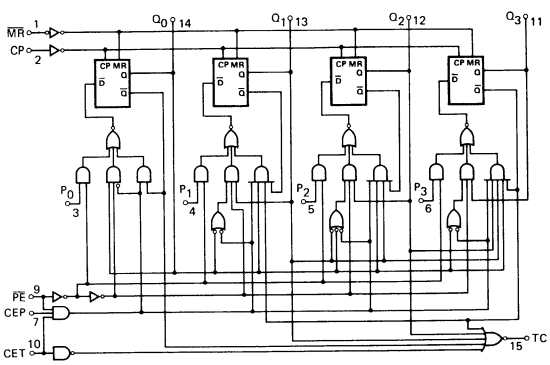
### LOGIC SYMBOL



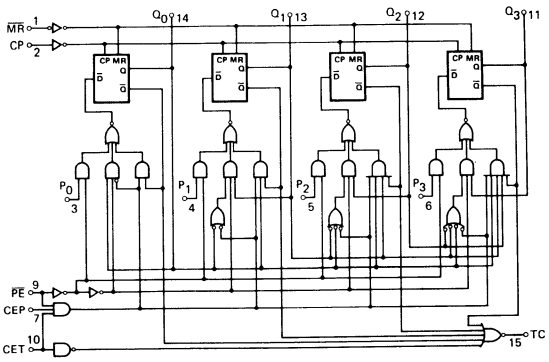

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

#### Am54S/74S160



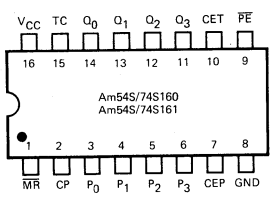

#### Am54S/74S161




### ORDERING INFORMATION

| Package Type | Temperature Range | Am54S/74S160 Order Number | Am54S/74S161 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +75°C | SN74S160N | SN74S161N |
| Hermetic DIP | 0°C to +75°C | SN74S160J | SN74S161J |
| Dice | 0°C to +75°C | SN74S160X | SN74S161X |
| Hermetic DIP | −55°C to +125°C | SN54S160J | SN54S161J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S160W | SN54S161W |
| Dice | −55°C to +125°C | SN54S160X | SN54S161X |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S160X, Am74S161X $T_A$ = 0°C to +75°C $V_{CC}$ = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V

Am54S160X, Am54S161X $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10% (MIL) MIN. = 4.5V MAX. = 5.5V

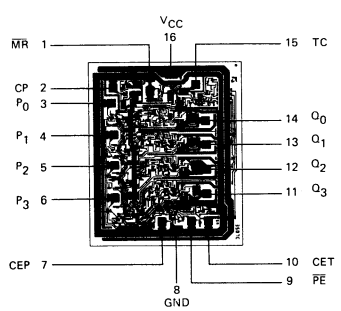
| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL. | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.35 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | P; MR; CEP | | | −2.0 | mA |
| | | | CET | | | −3.0 | |
| | | | $\overline{PE}$ | | | −4.0 | |
| | | | CP | | | −5.0 | |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | P; $\overline{MR}$; CEP | | | 50 | μA |
| | | | CET | | | 75 | |
| | | | $\overline{PE}$ | | | 100 | |
| | | | CP | | | 125 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX. | | −40 | −65 | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | 82 | 127 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; $\overline{MR}$ = 0V; all other inputs HIGH.

4

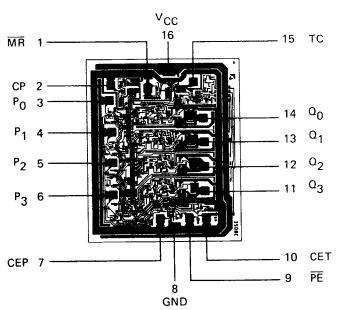
### Metallization and Pad Layouts

Am54S/74S160




DIE SIZE 0.078" X 0.096"

Am54S/74S161



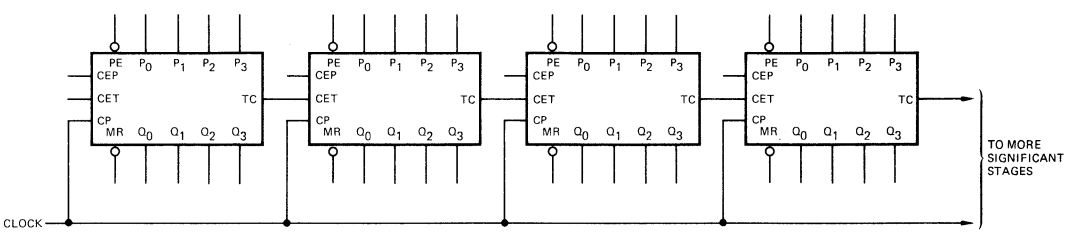

DIE SIZE 0.078" X 0.096"

## SWITCHING CHARACTERISTICS ($T_A$ = +25°)

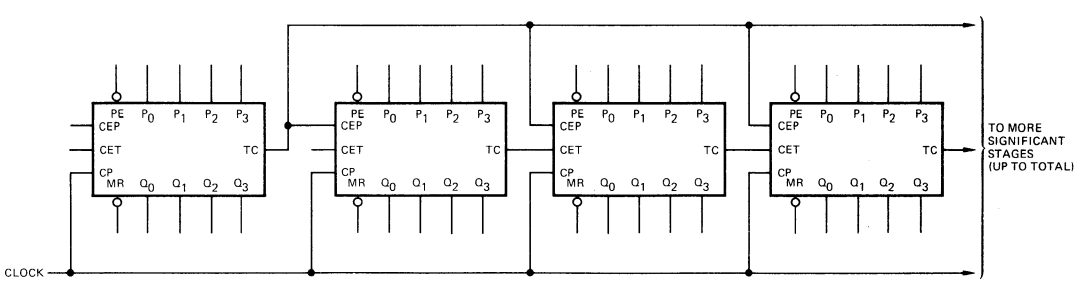
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Count Frequency | $V_{CC}$ = 5.0V, $C_L$ = 15 pF, $R_L$ = 280Ω | 70 | 100 | | MHz |
| $t_{PLH}$ | Clock to Q | | | 6 | 9 | ns |
| $t_{PHL}$ | | | | 8.5 | 13 | |
| $t_{PLH}$ | Clock to TC | | | 12 | 18 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | CET to TC | | | 6.5 | 10 | ns |
| $t_{PHL}$ | | | | 6.5 | 10 | |
| $t_{PHL}$ | $\overline{MR}$ to Q | | | 14 | 20 | ns |
| $t_s$ | Recovery Time for MR (inactive) | | 6 | | | ns |
| $t_{pw}$ | Master Reset Pulse Width | | 13 | | | ns |
| $t_{pw}$ | Clock Pulse Width HIGH | | 6 | | | ns |
| | Clock Pulse Width LOW | | 10 | | | |
| $t_s$ | Data to Clock | | 8 | | | ns |
| $t_h$ | | | 0 | | | |
| $t_s$ | $\overline{PE}$ to Clock | | 16 | | | ns |
| $t_h$ | | | 0 | | | |
| $t_s$ | CEP or CET to Clock | | 12 | | | ns |
| $t_h$ | | | 0 | | | |

## APPLICATIONS

### SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY




### FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS



## DEFINITION OF FUNCTIONAL TERMS

**$\overline{PE}$** Parallel Enable. When $\overline{PE}$ is LOW, the parallel inputs, $P_0$ through $P_3$, are enabled. When $\overline{PE}$ is HIGH, the count function is possible.

**CEP** Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

**CET** Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

**CP** Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

**$\overline{MR}$** Master Reset. When the asynchronous master reset is LOW, the $Q_0$ through $Q_3$ outputs will be LOW regardless of the other inputs.

**$P_0$, $P_1$, $P_2$, $P_3$** The parallel data inputs for the four internal flip-flops.

**$Q_0$, $Q_1$, $Q_2$, $Q_3$** The four parallel outputs from the counter.

**TC** Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am54S/74S160 or CET HIGH and binary 15 on the Am54S/74S161.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $\overline{MR}$ | 1 | 1 | – | – |
| CP | 2 | 2.5 | – | – |
| $P_0$ | 3 | 1 | – | – |
| $P_1$ | 4 | 1 | – | – |
| $P_2$ | 5 | 1 | – | – |
| $P_3$ | 6 | 1 | – | – |
| CEP | 7 | 1 | – | – |
| GND | 8 | – | – | – |
| $\overline{PE}$ | 9 | 2 | – | – |
| CET | 10 | 1.5 | – | – |
| $Q_3$ | 11 | – | 20 | 10 |
| $Q_2$ | 12 | – | 20 | 10 |
| $Q_1$ | 13 | – | 20 | 10 |
| $Q_0$ | 14 | – | 20 | 10 |
| TC | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CP | $\overline{MR}$ | $\overline{PE}$ | CEP | CET | $P_0$ | $P_1$ | $P_2$ | $P_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| X | L | X | X | X | X | X | X | X | L | L | L | L |
| ↑ | H | L | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| ↑ | H | H | L | L | X | X | X | X | NC | NC | NC | NC |
| ↑ | H | H | L | H | X | X | X | X | NC | NC | NC | NC |
| ↑ | H | H | H | L | X | X | X | X | NC | NC | NC | NC |
| ↑ | H | H | H | H | X | X | X | X | COUNT | | | |

H = HIGH
L = LOW
X = Don't Care

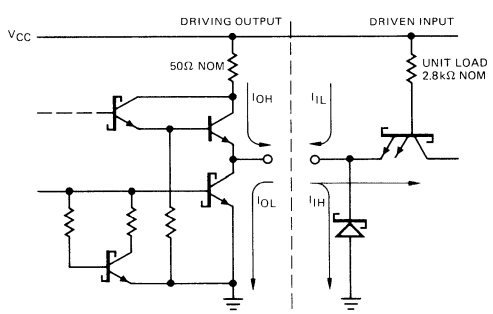
NC = No Change
$D_i$ may be either HIGH or LOW
↑ LOW-to-HIGH Transition

## TERMINAL COUNT (TC) TRUTH TABLE

| Am54S/74S160 | | | | | Am54S/74S161 | | | | | TC |
|---|---|---|---|---|---|---|---|---|---|---|
| CET | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | CET | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | |
| H | H | L | L | H | H | H | H | H | H | H |
| L | X | X | X | X | L | X | X | X | X | L |
| X | L | X | X | X | X | L | X | X | X | L |
| X | X | H | X | X | X | X | L | X | X | L |
| X | X | X | H | X | X | X | X | L | X | L |
| X | X | X | X | L | X | X | X | X | L | L |

H = HIGH
L = LOW
X = Don't Care

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

4

# Am54S/74S174•Am54S/74S175

## Hex/Quadruple D-Type Flip Flops With Clear

### Distinctive Characteristics

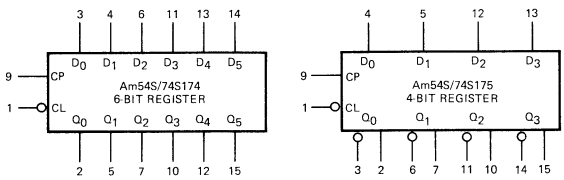
- 4-Bit and 6-Bit high-speed parallel registers.
- Common clock and common clear.
- Positive edge-triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am54S/74S174 is a six-bit, high-speed register and the Am54S/74S175 is a four-bit, high-speed register built using advanced Schottky technology. The registers consist of D-type flip-flops with a buffered common clock and an asynchronous active LOW buffered clear.

When the clear is LOW, the Q outputs are LOW independent of the other inputs. Information meeting the set-up requirements of the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse.

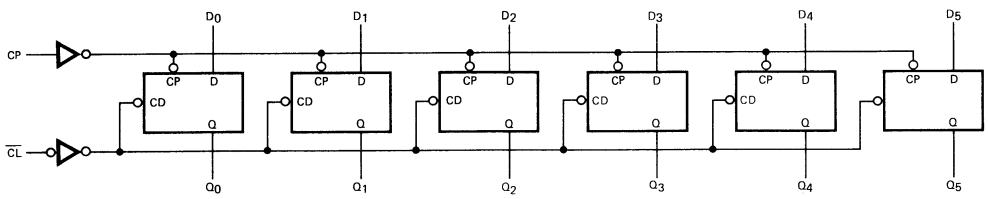
### LOGIC SYMBOLS



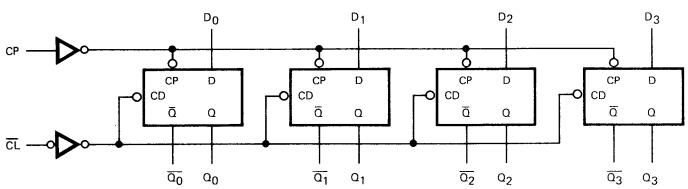

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

Am54S/74S174



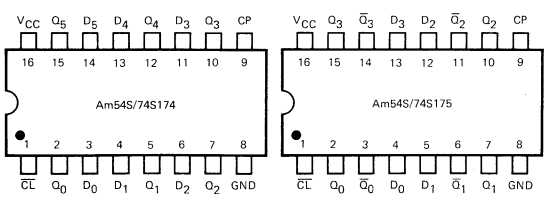

Am54S/74S175




### ORDERING INFORMATION

| Package Type | Temperature Range | Am54S/74S174 Order Number | Am54S/74S175 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S174N | SN74S175N |
| Hermetic DIP | 0°C to +70°C | SN74S174J | SN74S175J |
| Dice | 0°C to +70°C | SN74S174X | SN74S175X |
| Hermetic DIP | −55°C to +125°C | SN54S174J | SN54S175J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S174W | SN54S175W |
| Dice | −55°C to +125°C | SN54S174X | SN54S175X |

### CONNECTION DIAGRAMS
Top Views




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S174, Am74S175 $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am54S174, Am54S175 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 74S | 2.7 | 3.4 | | Volts |
| | | | 54S | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20 mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 5) | $V_{CC}$ = MAX. | S174 | | 90 | 144 | mA |
| | | | S175 | | 60 | 96 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All outputs open and 4.5 V applied to the data and clear inputs. Measured after a momentary ground, then 4.5 V applied to the clock input.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $R_L$ = 280 Ω | | 8 | 12 | ns |
| $t_{PHL}$ | | | | | 11.5 | 17 | |
| $t_{PLH}$ | Clear to Output | | | | 10 | 15 | ns |
| $t_{PHL}$ | | | | | 13 | 22 | |
| $t_{pw}$ | Pulse Width | Clock | | 7 | | | ns |
| | | Clear | | 10 | | | |
| $t_s$ | Data Set-up Time | | | 5 | | | ns |
| $t_s$ | Set-up Time. Clear Recovery (in-active) to Clock | | | 5 | | | ns |
| $t_h$ | Data Hold Time | | | 3 | | | ns |
| $f_{MAX}$ | Maximum Clock Frequency | | | 75 | 110 | | MHz |

## Am54S/74S174 LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $\overline{CL}$ | 1 | 1 | – | – |
| $Q_0$ | 2 | – | 20 | 10 |
| $D_0$ | 3 | 1 | – | – |
| $D_1$ | 4 | 1 | – | – |
| $Q_1$ | 5 | – | 20 | 10 |
| $D_2$ | 6 | 1 | – | – |
| $Q_2$ | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| CP | 9 | 1 | – | – |
| $Q_3$ | 10 | – | 20 | 10 |
| $D_3$ | 11 | 1 | – | – |
| $Q_4$ | 12 | – | 20 | 10 |
| $D_4$ | 13 | 1 | – | – |
| $D_5$ | 14 | 1 | – | – |
| $Q_5$ | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

## Am54S/74S175 LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $\overline{CL}$ | 1 | 1 | – | – |
| $Q_0$ | 2 | – | 20 | 10 |
| $\overline{Q}_0$ | 3 | – | 20 | 10 |
| $D_0$ | 4 | 1 | – | – |
| $D_1$ | 5 | 1 | – | – |
| $\overline{Q}_1$ | 6 | – | 20 | 10 |
| $Q_1$ | 7 | – | 20 | 10 |
| GND | 8 | – | – | – |
| CP | 9 | 1 | – | – |
| $Q_2$ | 10 | – | 20 | 10 |
| $\overline{Q}_2$ | 11 | – | 20 | 10 |
| $D_2$ | 12 | 1 | – | – |
| $D_3$ | 13 | 1 | – | – |
| $\overline{Q}_3$ | 14 | – | 20 | 10 |
| $Q_3$ | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| Clear | Clock | $D_i$ | $Q_i$ | $\overline{Q}_i$ |
| L | X | X | L | H |
| H | L | X | NC | NC |
| H | H | X | NC | NC |
| H | ↑ | L | L | H |
| H | ↑ | H | H | L |

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH Transition
Note: $\overline{Q}_i$ on Am54S/74S175 only

## DEFINITION OF FUNCTIONAL TERMS

$D_i$ The D flip-flop data inputs.

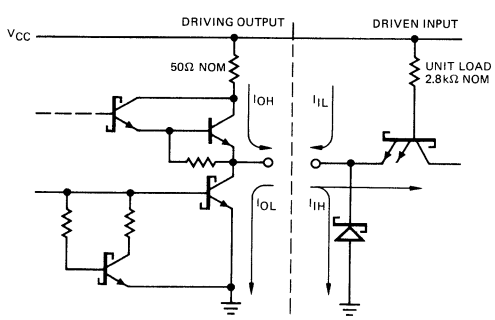
**CL** Clear. When the clear is LOW, the Qi outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.

**CP** Clock pulse for the register. Enters data on the positive transition.

$Q_i$ The TRUE register outputs.

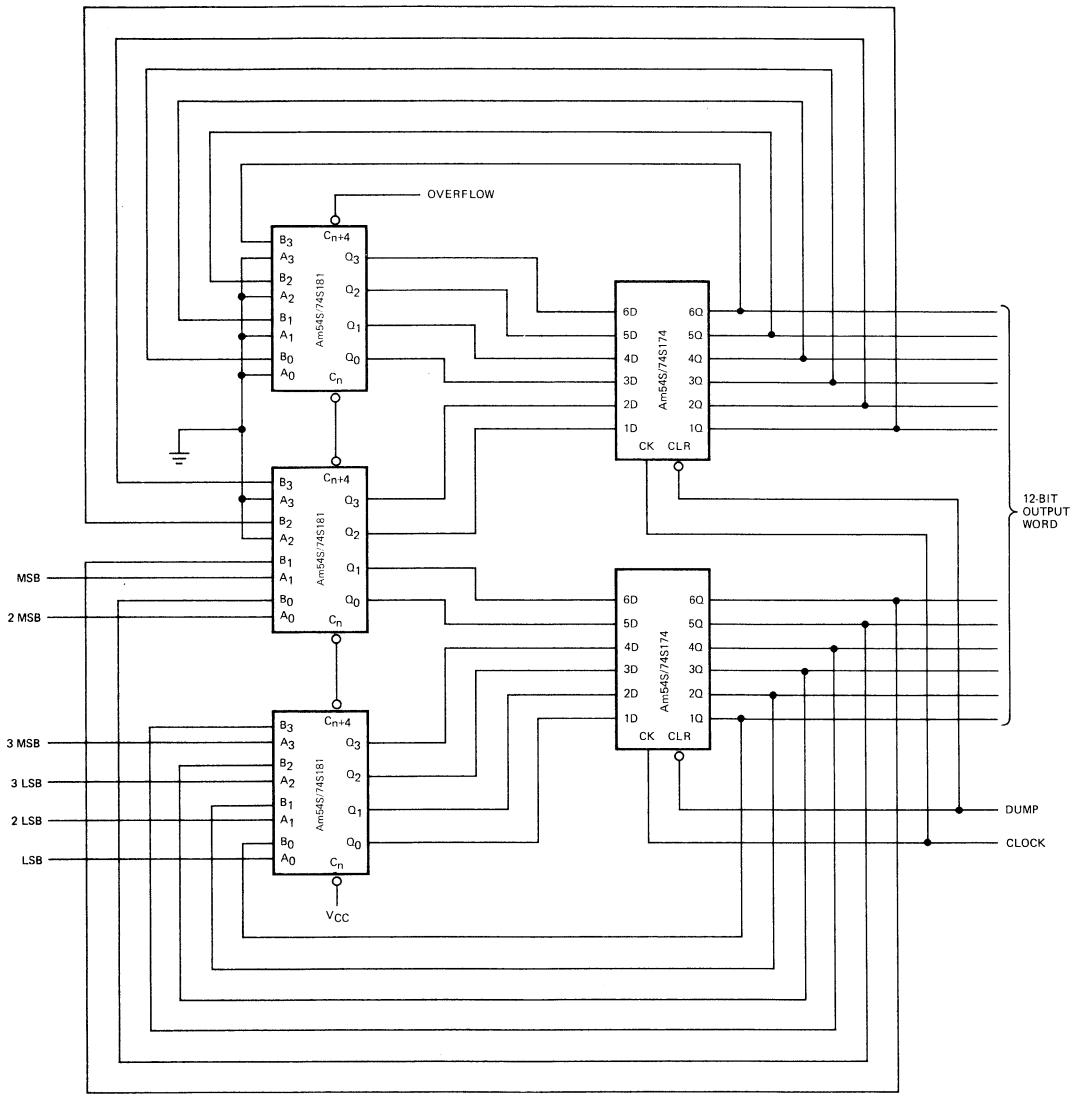
$\overline{Q}_i$ The complement register outputs.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## APPLICATION

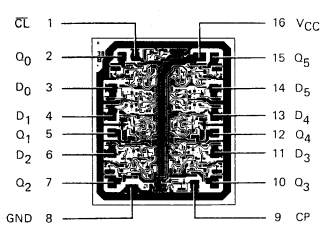



(Am54S/74S181 in ADD mode)

**6-Bit Input, Integrate and Dump for Magnitude-Only Arithmetic (65 samples min. before overflow)**

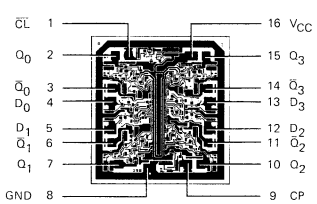
## Metallization and Pad Layouts

### Am54S/74S174




DIE SIZE: 0.070" X 0.083"

### Am54S/74S175




DIE SIZE: 0.067" X 0.073"

# Am54S/74S181

## Four-Bit Arithmetic Logic Unit/Function Generator

### Distinctive Characteristics

- Advanced Schottky technology
- Performs 16 arithmetic operations including add, subtract, double and compare.
- Performs all 16 possible logic operations of two variables in typically 11ns.
- Typical 4-bit add time is 11ns and carry time is 6ns.
- Full look-ahead capability for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

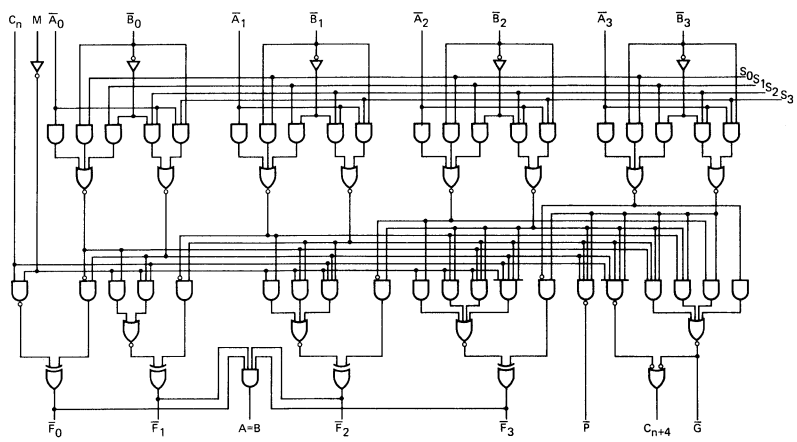
The Am54S/74S181 is a 4-bit, high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is LOW the 16 arithmetic operations are performed under the control of the four select inputs. When the mode control is HIGH the sixteen logic operations are performed on an individual bit basis between the two 4-bit parallel words under the control of the four select inputs.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs.

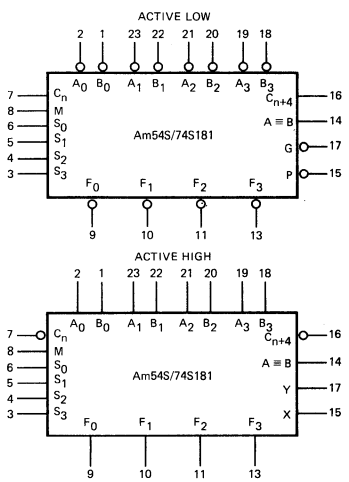
An open collector output A = B is used to signal the equivalence of the two parallel words. The open collector feature allows for the equivalence function to be expanded as a wired-AND connection for larger word lengths.

In many systems, the carry output $C_{n+4}$ is connected to the next higher $C_n$ to provide ripple block arithmetic. The ALU can be used with either active HIGH or active LOW inputs and can be ripple expanded or full look-ahead expanded in either mode. The connection pattern is identical for either logic representation.

### LOGIC DIAGRAM




### LOGIC SYMBOLS

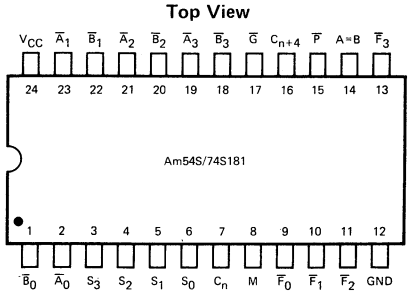



$V_{CC}$ = Pin 24
GND = Pin 12

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S181N |
| Hermetic DIP | 0°C to +70°C | SN74S181J |
| Dice | 0°C to +70°C | SN74S181X |
| Hermetic DIP | −55°C to +125°C | SN54S181J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S181W |
| Dice | −55°C to +125°C | SN54S181X |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

| | | | | | |
|---|---|---|---|---|---|
| Am74S181 | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ±5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am54S181 | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ±10% (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (Except A=B Output) | | $V_{CC}$ = MIN., $I_{OH}$ = −1mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 54S | 2.5 | 3.4 | | Volts |
| | | | | 74S | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{OH}$ | Output HIGH Current for A=B Output | | $V_{CC}$ = MIN., $V_{OH}$ = 5.5V<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 250 | µA |
| $I_{IL}$ (Note 3) | Input LOW Current | M | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −2 | mA |
| | | $\overline{A_i}$ or $\overline{B_i}$ | | | | | −6 | |
| | | $S_i$ | | | | | −8 | |
| | | $C_n$ | | | | | −10 | |
| $I_{IH}$ (Note 3) | Input HIGH Current | M | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 50 | µA |
| | | $\overline{A_i}$ or $\overline{B_i}$ | | | | | 150 | |
| | | $S_i$ | | | | | 200 | |
| | | $C_n$ | | | | | 250 | |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) (Except A = B Output) | | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 5) | | $V_{CC}$ = MAX. | | | 120 | 180 | mA |
| | | | $V_{CC}$ = MAX., $T_A$ = 125°C<br>Am54S Flat Package (W) Only | | | | 159 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured under two conditions — typ. and max. apply to both.
   A. $S_i$, M, $A_i$ at 4.5V; all other inputs grounded; outputs open.
   B. $S_i$, M at 4.5V; all other inputs grounded; outputs open.

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF, $R_L$ = 280Ω)

| Parameter | From (Input) | To (Output) | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $C_n$ | $C_{n+4}$ | | | 5 | 10.5 | ns |
| $t_{PHL}$ | | | | | 7 | 10.5 | |
| $t_{PLH}$ | $C_n$ | $\overline{F}_i$ | M = 0V | | 7 | 12 | ns |
| $t_{PHL}$ | | | (SUM or DIFF mode) | | 6 | 12 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{G}$ | M = 0V, $S_0 = S_3$ = 4.5V, | | 8 | 12 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 0V (SUM mode) | | 7 | 12 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{G}$ | M = 0V, $S_0 = S_3$ = 0V, | | 10 | 15 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 4.5V (DIFF mode) | | 10 | 15 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{P}$ | M = 0V, $S_0 = S_3$ = 4.5V, | | 7.5 | 12 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 0V (SUM mode) | | 7.5 | 12 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{P}$ | M = 0V, $S_0 = S_3$ = 0V, | | 10 | 15 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 4.5V (DIFF mode) | | 10.5 | 15 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $F_j (j \geq i)$ | M = 0V, $S_0 = S_3$ = 4.5V, | | 10 | 16.5 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 0V (SUM mode) | | 7 | 16.5 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $F_j (j \geq i)$ | M = 0V, $S_0 = S_3$ = 0V, | | 12 | 20 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 4.5V (DIFF mode) | | 9 | 22 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_{i+1}$ | M = 0V, $S_0 = S_3$ = 4.5V, | | 11 | 16.5 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 0V (SUM mode) | | 11 | 16.5 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_{i+1}$ | M = 0V, $S_0 = S_3$ = 0V, | | 14 | 20 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 4.5V (DIFF mode) | | 14 | 22 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $\overline{F}_i$ | M = 4.5V (LOGIC mode) | | 12 | 20 | ns |
| $t_{PHL}$ | | | | | 9 | 22 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $C_{n+4}$ | M = 0V, $S_0 = S_3$ = 4.5V, | | 12.5 | 18.5 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 0V (SUM mode) | | 12.5 | 18.5 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | $C_{n+4}$ | M = 0V, $S_0 = S_3$ = 0V, | | 14 | 23 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 4.5V (DIFF mode) | | 15 | 23 | |
| $t_{PLH}$ | $\overline{A}_i$ or $\overline{B}_i$ | A = B | M = 0V, $S_0 = S_3$ = 0V, | | 15 | 23 | ns |
| $t_{PHL}$ | | | $S_1 = S_2$ = 4.5V (DIFF mode) | | 19 | 30 | |

## OPERATION TABLE

| CONTROL INPUTS | | | | ACTIVE LOW INPUTS AND OUTPUTS | | ACTIVE HIGH INPUTS AND OUTPUTS | |
|---|---|---|---|---|---|---|---|
| $S_0$ | $S_1$ | $S_2$ | $S_3$ | Arithmetic (M = L, $C_n$ = L) | Logic (M = H) | Arithmetic (M = L, $\overline{C}_n$ = H) | Logic (M = H) |
| L | L | L | L | A minus 1 | $\overline{A}$ | A | $\overline{A}$ |
| H | L | L | L | AB minus 1 | $\overline{AB}$ | A + B | $\overline{A+B}$ |
| L | H | L | L | $A\overline{B}$ minus 1 | $\overline{A}+B$ | $A+\overline{B}$ | $\overline{AB}$ |
| H | H | L | L | minus 1 (2's comp.) | Logic '1' | minus 1 (2's comp.) | Logic '0' |
| L | L | H | L | A plus [A + $\overline{B}$] | $\overline{A+B}$ | A plus $A\overline{B}$ | $\overline{AB}$ |
| H | L | H | L | AB plus [A + $\overline{B}$] | $\overline{B}$ | $A\overline{B}$ plus [A + B] | $\overline{B}$ |
| L | H | H | L | A minus B minus 1 | $\overline{A \oplus B}$ | A minus B minus 1 | $A \oplus B$ |
| H | H | H | L | A + $\overline{B}$ | A + $\overline{B}$ | $A\overline{B}$ minus 1 | $A\overline{B}$ |
| L | L | L | H | A plus [A + B] | $\overline{AB}$ | A plus AB | $\overline{A}+B$ |
| H | L | L | H | A plus B | $A \oplus B$ | A plus B | $\overline{A \oplus B}$ |
| L | H | L | H | $A\overline{B}$ plus [A + B] | B | AB plus [A + $\overline{B}$] | B |
| H | H | L | H | A + B | A + B | AB minus 1 | AB |
| L | L | H | H | A plus A (2 x A) | Logic '0' | A plus A (2 x A) | Logic '1' |
| H | L | H | H | A plus AB | $A\overline{B}$ | A plus [A + B] | A + $\overline{B}$ |
| L | H | H | H | A plus $A\overline{B}$ | AB | A plus [A + $\overline{B}$] | A + B |
| H | H | H | H | A | A | A minus 1 | A |

L = LOW Voltage Level
H = HIGH Voltage Level

## DEFINITION OF FUNCTIONAL TERMS

$\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$ The A data inputs.

$\overline{B}_0, \overline{B}_1, \overline{B}_2, \overline{B}_3$ The B data inputs.

$S_0, S_1, S_2, S_3$ The control inputs used to determine the arithmetic or logic function performed.

$\overline{F}_0, \overline{F}_1, \overline{F}_2, \overline{F}_3$ The data outputs of the ALU.

**M** The mode control inputs used to select either the arithmetic or logic operations.

$C_n$ The carry-in input of the ALU.

$C_{n+4}$ The carry-look-ahead output of the four-bit input field.

$\overline{G}$ The carry-generate output for use in multi-level look-ahead schemes.

$\overline{P}$ The carry-propagate output for use in multi-level look-ahead schemes.

**A = B** The open collector comparator output that can be used to determine equivalence. This output is HIGH whenever the four $\overline{F}$ outputs are HIGH.

## USER NOTES

1. Throughout this data sheet, the active LOW input and output terminology has been used. For the active HIGH definition, the nomenclautre shown under the active HIGH logic symbol should be substituted.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in ($C_n$ = HIGH) for the active LOW case and ($\overline{C}_n$ = LOW) for the active HIGH case.
6. The A = B output only indicates that the four $\overline{F}$ outputs are all HIGH.

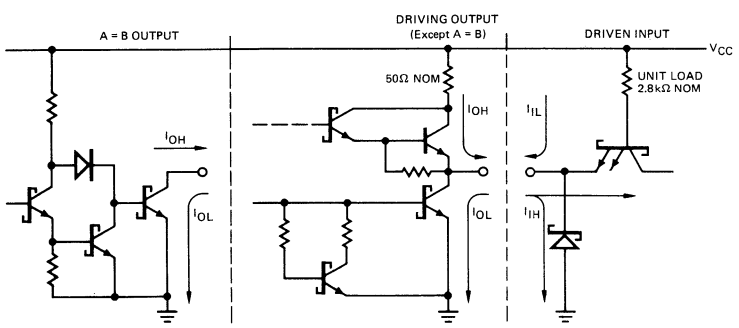
## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Output Drive Output HIGH | Output Drive Output LOW |
|---|---|---|---|---|
| $\overline{B}_0$ | 1 | 3 | – | – |
| $\overline{A}_0$ | 2 | 3 | – | – |
| $S_3$ | 3 | 4 | – | – |
| $S_2$ | 4 | 4 | – | – |
| $S_1$ | 5 | 4 | – | – |
| $S_0$ | 6 | 4 | – | – |
| $C_n$ | 7 | 5 | – | – |
| M | 8 | 1 | – | – |
| $\overline{F}_0$ | 9 | – | 20 | 10 |
| $\overline{F}_1$ | 10 | – | 20 | 10 |
| $\overline{F}_2$ | 11 | – | 20 | 10 |
| GND | 12 | – | – | – |
| $\overline{F}_3$ | 13 | – | 20 | 10 |
| A = B | 14 | – | O/C | 10 |
| $\overline{P}$ | 15 | – | 20 | 10 |
| $C_{n+4}$ | 16 | – | 20 | 10 |
| $\overline{G}$ | 17 | – | 20 | 10 |
| $\overline{B}_3$ | 18 | 3 | – | – |
| $\overline{A}_3$ | 19 | 3 | – | – |
| $\overline{B}_2$ | 20 | 3 | – | – |
| $\overline{A}_2$ | 21 | 3 | – | – |
| $\overline{B}_1$ | 22 | 3 | – | – |
| $\overline{A}_1$ | 23 | 3 | – | – |
| $V_{CC}$ | 24 | – | – | – |

O/C = Open Collector

A Schottky unit load is defined as 50μA measured at 2.7V HIGH and −2.0 mA measured at 0.5V LOW.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5V | Apply 0V | Apply 4.5V | Apply 0V | | |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$ | $C_n$ | $\overline{F}_i (i \geq i)$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$ | $C_n$ | $\overline{F}_i (i \geq i)$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | $C_n$ | Remaining $\overline{A}$ and $\overline{B}$ | $\overline{F}_{i+1}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | $C_n$ | Remaining $\overline{A}$ and $\overline{B}$ | $\overline{F}_{i+1}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $\overline{G}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $\overline{G}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | Remaining $\overline{B}$ | Remaining $\overline{A}$, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | None | None | All $\overline{A}$ | All $\overline{B}$ | Any $\overline{F}$ or $C_{n+4}$ | In-Phase |

## DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

| Parameter | Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5V | Apply 0V | Apply 4.5V | Apply 0V | | |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | $\overline{F}_i (i \geq i)$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | $\overline{F}_i (i \geq i)$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{B}$, $C_n$ | Remaining $\overline{A}$ | $\overline{F}_{i+1}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{B}$, $C_n$ | Remaining $\overline{A}$ | $\overline{F}_{i+1}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{P}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{G}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{G}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | None | $\overline{B}_i$ | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | A = B | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | Remaining $\overline{A}$ | Remaining $\overline{B}$, $C_n$ | A = B | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $C_{n+4}$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | None | $\overline{A}_i$ | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $C_{n+4}$ | In-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $C_n$ | None | None | All $\overline{A}$ and $\overline{B}$ | None | Any $\overline{F}$ or $C_{n+4}$ | In-Phase |

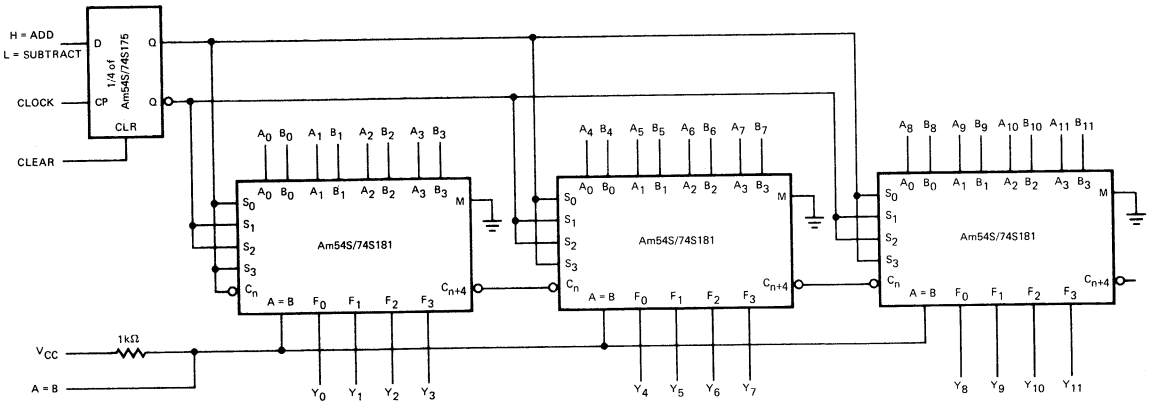
## LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5V$, $S_0 = S_3 = 0V$

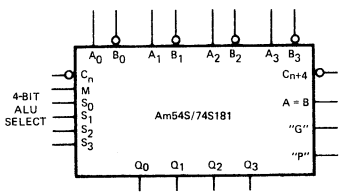
| Parameter | Input Under Test | Other Input Same Bit | | Other Data Inputs | | Output Under Test | Output Waveform |
|---|---|---|---|---|---|---|---|
| | | Apply 4.5V | Apply 0V | Apply 4.5V | Apply 0V | | |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{A}_i$ | $\overline{B}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{F}_i$ | Out-of-Phase |
| $t_{PLH}$ / $t_{PHL}$ | $\overline{B}_i$ | $\overline{A}_i$ | None | None | Remaining $\overline{A}$ and $\overline{B}$, $C_n$ | $\overline{F}_i$ | Out-of-Phase |

## APPLICATIONS

### 12-Bit Adder /Subtractor (2's Complement)




If one input is defined active–HIGH and the second input is defined active–LOW, the sixteen arithmetic and logic functions of the ALU are reordered as shown in the function table.



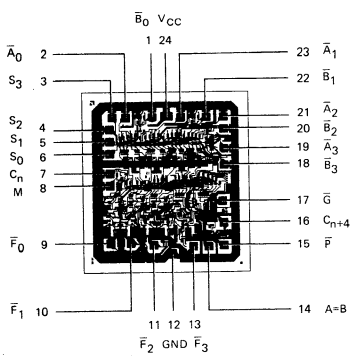

**Function Table**

**A = Active HIGH  B = Active LOW**

| $S_0$ | $S_1$ | $S_2$ | $S_3$ | Arithmetic (M = L, $\overline{C}_n$ = H) | Logic (M = H) |
|---|---|---|---|---|---|
| L | L | L | L | A | $\overline{A}$ |
| H | L | L | L | A + $\overline{B}$ | $\overline{A}B$ |
| L | H | L | L | A + B | $\overline{A}\overline{B}$ |
| H | H | L | L | minus 1 (2's comp.) | Logic '0' |
| L | L | H | L | A plus AB | AB |
| H | L | H | L | AB plus [A + $\overline{B}$] | B |
| L | H | H | L | A plus B | $\overline{A \oplus B}$ |
| H | H | H | L | AB minus 1 | AB |
| L | L | L | H | A plus A$\overline{B}$ | $\overline{A} + \overline{B}$ |
| H | L | L | H | A minus B minus 1 | A $\oplus$ B |
| L | H | L | H | A$\overline{B}$ plus [A + B] | $\overline{B}$ |
| H | H | L | H | A$\overline{B}$ minus 1 | A$\overline{B}$ |
| L | L | H | H | A plus A (2 x A) | Logic '1' |
| H | L | H | H | A plus [A + $\overline{B}$] | A + B |
| L | H | H | H | A plus [A + B] | A + $\overline{B}$ |
| H | H | H | H | A minus 1 | A |

L = Low Voltage Level
H = High Voltage Level

### Metallization and Pad Layout




DIE SIZE: = 0.083" X 0.091"

# Am54S/74S194•Am54S/74S195

## Four-Bit High-Speed Shift Registers

### Distinctive Characteristics

- Parallel load or shift right with $J\overline{K}$ inputs on Am54S/74S195
- Shift left, right, parallel load or do nothing on Am54S/74S194
- Fully synchronous shifting and parallel loading
- Buffered common clock
- Buffered common active-LOW clear
- 100% reliability assurance testing in compliance with MIL-STD-883

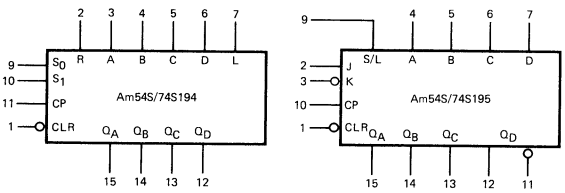
### FUNCTIONAL DESCRIPTION

The Am54S/74S194 and Am54S/74S195 are 4-bit registers that exhibit fully synchronous operation in all operating modes. The Am54S/74S195 can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, $Q_A$, is loaded via the J and $\overline{K}$ inputs in the shift mode.

The Am54S/74S194 operates in four modes under control of the two select inputs, $S_0$ and $S_1$. The four modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the $Q_A$ bit input from R), shift left (data comes from the flip-flop to the right, with the $Q_D$ input from L), and hold or do nothing (each flip-flop receives data from its own output).

For both devices the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW asynchronous clear (CLR) which forces all outputs to the LOW state ($\overline{Q}_D$ HIGH) independent of any other inputs. All control inputs are buffered to present only one Schottky TTL load to the system, and all outputs can drive 10 Schottky loads in the LOW state and 20 in the HIGH state. Because all the flip-flops are D-type they do not catch 0's or 1's, and the only requirements on any inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

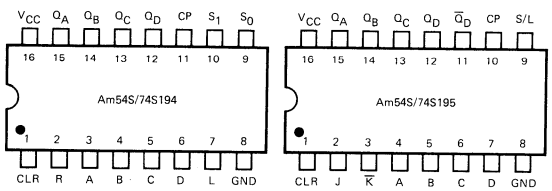
### LOGIC SYMBOLS




$V_{CC}$ = Pin 16
GND = Pin 8

### CONNECTION DIAGRAMS

Top Views



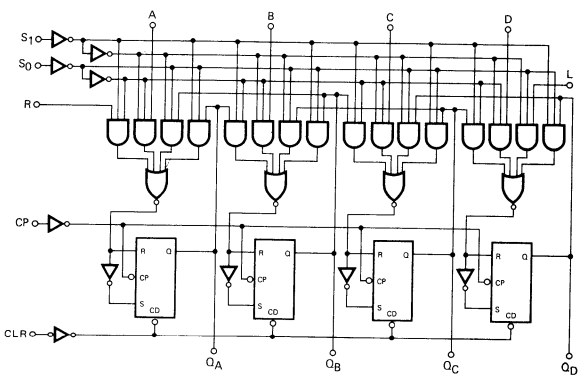

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

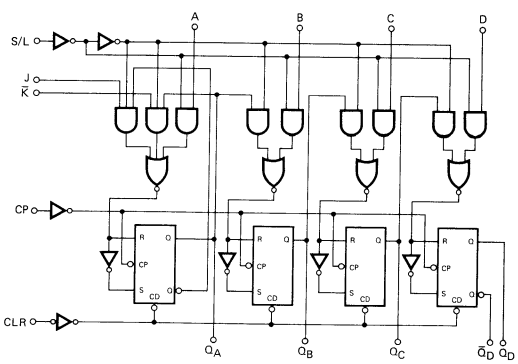
| Package Type | Temperature Range | Am54S/74S194 Order Number | Am54S/74S195 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S194N | SN74S195N |
| Hermetic DIP | 0°C to +70°C | SN74S194J | SN74S195J |
| Dice | 0°C to +70°C | SN74S194X | SN74S195X |
| Hermetic DIP | −55°C to +125°C | SN54S194J | SN54S195J |
| Hermetic Flat Pak | −55°C to +125°C | SN54S194W | SN54S195W |
| Dice | −55°C to +125°C | SN54S194X | SN54S195X |

### LOGIC DIAGRAMS

Am54S/74S194



Am54S/74S195



## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | | |
|---|---|---|---|---|---|
| Am74S194, Am74S195 | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% (COM'L) | MIN. = 4.75 V | MAX. 5.25 V |
| Am54S194, Am54S195 | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% (MIL) | MIN. = 4.5 V | MAX. = 5.5 V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | Am74 | 2.7 | 3.4 | | Volts |
| | | | Am54 | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18 mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2 | mA |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | S194 (Note 5 & 7) | | 85 | 135 | mA |
| | | | 54S195 (Note 6) | | 70 | 99 | |
| | | | 74S195 (Note 6) | | 70 | 109 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open. Inputs A, B, C, D grounded. Inputs $S_0$, $S_1$, Clear, L, R, at 4.5 V. Measured after a momentary ground, then 4.5 V applied to clock.
6. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5 V. Measured after applying a momentary ground then 4.5 V to the clear followed by ground then 4.5 V to clock.
7. For $T_A$ = 125°C; $I_{CC}$ MAX. = 110 mA for Am54S194W.

4

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $R_L$ = 280 Ω | 4 | 8 | 12 | ns |
| $t_{PHL}$ | Clock to Output | | 4 | 11 | 16.5 | ns |
| $t_{PHL}$ | Clear to Output | | | 12.5 | 18.5 | ns |
| $t_{pw}$ | Clock Pulse Width | | 7 | | | ns |
| $t_{pw}$ | Clear Pulse Width | | 12 | | | ns |
| $t_s$ | Mode Control Set-up Time | | 11 | | | ns |
| $t_s$ | Data Input Set-up Time | | 5 | | | ns |
| $t_s$ | Clear Recovery to Clock | | 9 | | | ns |
| $t_h$ | Data Hold Time | | 3 | | | ns |
| $t_R$ | Shift/Load Release Time Am54S/74S195 | | | | 6 | ns |
| $f_{MAX.}$ | Maximum Clock Frequency | | 70 | 105 | | MHz |

## DEFINITION OF FUNCTIONAL TERMS

**J, $\overline{K}$** The logic inputs used for controlling the $Q_A$ flip-flop of the Am54S/74S195 register when S/L is HIGH.

**CLR** Clear. The asynchronous master reset input.

**CP** Clock pulse for the register. Enters data on the LOW-to-HIGH transition.

**S/L** Shift/Load. The input for selection of parallel or serial shifting for the AM54S/74S195 register. S/L LOW selects parallel entry.

**$S_0$, $S_1$** The mode select inputs of the Am54S/74S194.

**A, B, C, D** The four parallel data inputs for the register.

**R** The serial input to the $Q_A$ flip-flop of the Am54S/74S194 in the right shift mode.

**L** The serial input to the $Q_D$ flip-flop of the Am54S/74S194 in the left shift mode.

**$Q_A$, $Q_B$, $Q_C$, $Q_D$** The four true outputs of the register.

**$\overline{Q}_D$** The complement output of the $Q_D$ flip-flop. (Am54S/74S195 only).

## LOADING RULES (In Unit Loads)

| Am54S/74S195 Input/Output | Am54S/74S194 Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|---|
| CLR | CLR | 1 | 1 | – | – |
| J | R | 2 | 1 | – | – |
| $\overline{K}$ | A | 3 | 1 | – | – |
| A | B | 4 | 1 | – | – |
| B | C | 5 | 1 | – | – |
| C | D | 6 | 1 | – | – |
| D | L | 7 | 1 | – | – |
| GND | GND | 8 | – | – | – |
| Shift/Load | $S_0$ | 9 | 1 | – | – |
| CP | $S_1$ | 10 | 1 | – | – |
| $\overline{Q}_D$ | – | 11 | – | 20 | 10 |
| – | CP | | 1 | – | – |
| $Q_D$ | $Q_D$ | 12 | – | 20 | 10 |
| $Q_C$ | $Q_C$ | 13 | – | 20 | 10 |
| $Q_B$ | $Q_B$ | 14 | – | 20 | 10 |
| $Q_A$ | $Q_A$ | 15 | – | 20 | 10 |
| $V_{CC}$ | $V_{CC}$ | 16 | – | – | – |

## FUNCTION TABLE
### Am54S/74S194

| FUNCTION | INPUTS: Clear | Mode $S_1$ | Mode $S_0$ | Clock | Serial Left | Serial Right | Parallel A | Parallel B | Parallel C | Parallel D | OUTPUTS $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | L | X | X | X | X | X | X | X | X | X | L | L | L | L |
| No Change | H | X | X | L | X | X | X | X | X | X | NC | NC | NC | NC |
| | H | X | X | H | X | X | X | X | X | X | NC | NC | NC | NC |
| Parallel Load | H | H | H | ↑ | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| Shift Right | H | L | H | ↑ | X | L | X | X | X | X | L | $Q_A$ | $Q_B$ | $Q_C$ |
| | H | L | H | ↑ | X | H | X | X | X | X | H | $Q_A$ | $Q_B$ | $Q_C$ |
| Shift Left | H | H | L | ↑ | L | X | X | X | X | X | $Q_B$ | $Q_C$ | $Q_D$ | L |
| | H | H | L | ↑ | H | X | X | X | X | X | $Q_B$ | $Q_C$ | $Q_D$ | H |
| Hold | H | L | L | X | X | X | X | X | X | X | NC | NC | NC | NC |

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
$D_i$ = May be a HIGH or a LOW and the respective output will assume the same state.

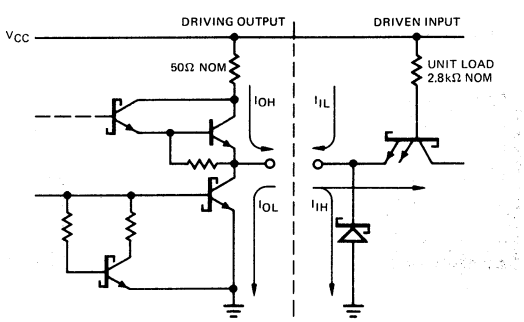
## FUNCTION TABLE
### Am54S/74S195

| Clear | Shift/Load | Clock | Serial J | Serial $\overline{K}$ | Parallel A | Parallel B | Parallel C | Parallel D | OUTPUTS $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $\overline{Q}_D$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | X | X | X | X | X | X | X | X | L | L | L | L | H |
| H | X | L | X | X | X | X | X | X | NC | NC | NC | NC | NC |
| H | X | H | X | X | X | X | X | X | NC | NC | NC | NC | NC |
| H | L | ↑ | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $\overline{D}_3$ |
| H | H | ↑ | L | H | X | X | X | X | $Q_A$ | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | L | L | X | X | X | X | L | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | H | H | X | X | X | X | H | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |
| H | H | ↑ | H | L | X | X | X | X | $\overline{Q}_A$ | $Q_A$ | $Q_B$ | $Q_C$ | $\overline{Q}_C$ |

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
$D_i$ = May be a HIGH or a LOW and the respective output will assume the same state.

Notes: 1. If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.
2. Linear feedback shift counters can be made by connecting the $Q_D$ and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

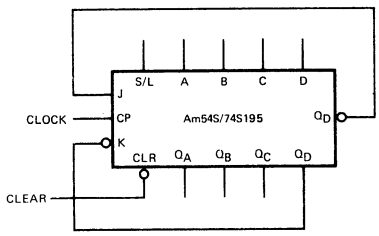



Note: Actual current flow direction shown

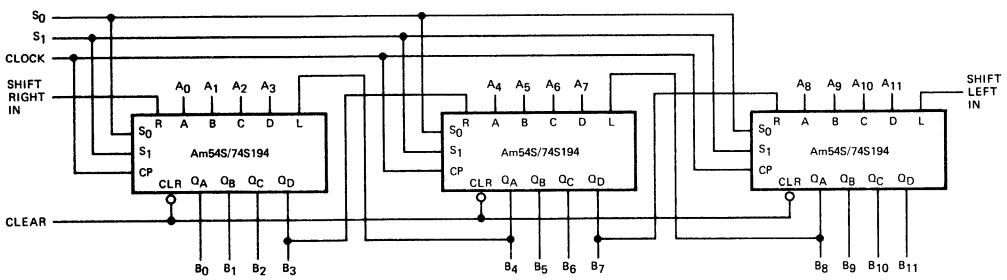
## APPLICATIONS

### HIGH-SPEED MOD 15 LINEAR FEEDBACK SHIFT REGISTER

Sequence is 0, 1, 2, 5, 10, 4, 9, 3, 6, 13, 11, 7, 14, 12, 8, 0 (15 is non-self correcting; use clear to initialize)



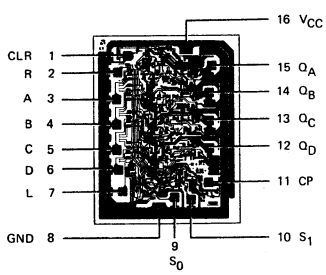

### 12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL-LOAD REGISTER




4

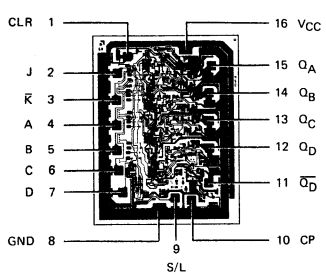
### Metallization and Pad Layouts

**Am54S/74S194**




DIE SIZE 0.072" X 0.093"

**Am54S/74S195**




DIE SIZE 0.072" X 0.093"

# Am54S/74S240 • Am54S/74S241
# Am54S/74S242 • Am54S/74S243
# Am54S/74S244

## Octal Buffers/Line Drivers/Line Receivers With Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- $V_{OL}$ of 0.55V at 64mA for Am74S; 48mA for Am54S
- Data-to-output propagation delay times:
  Inverting – 7.0ns MAX
  Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20 pin hermetic and molded DIP packages for Am54S/74S240, Am54S/74S241, and Am54S/74S244

### FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

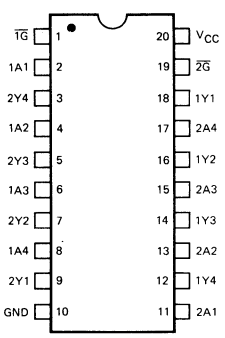
Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

The Am54S/74S240, Am54S/74S241 and Am54S/74S244 have four buffers which are enabled from one common line, and the other four buffers are enabled from another common line. The Am54S/74S240 is inverting, while the Am54S/74S241 and Am54S/74S244 present true data at the outputs.

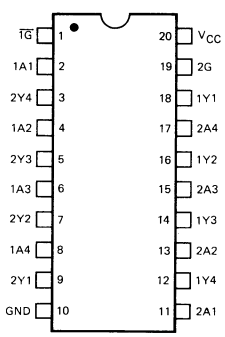
The Am54S/74S242 and Am54S/74S243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The Am54S/74S242 is inverting, while the Am54S/74S243 presents non-inverting data at the outputs.

### CONNECTION DIAGRAMS
**Top Views**

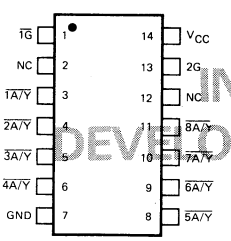
Am54S/74S240



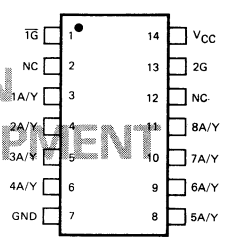

Am54S/74S241



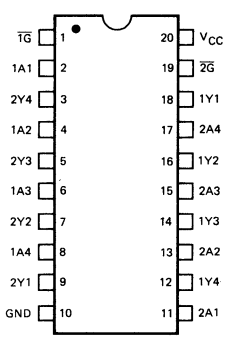

Am54S/74S242




Am54S/74S243




Am54S/74S244





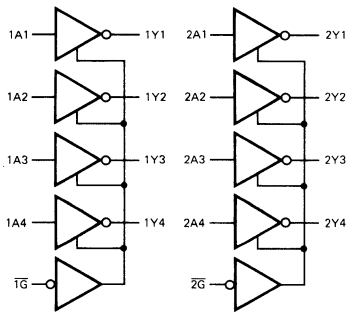

Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

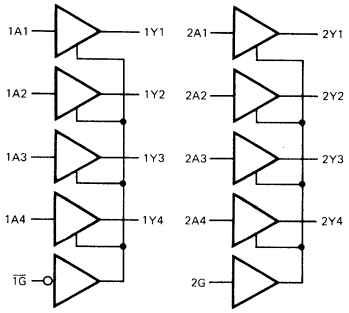
| Package Type | Temperature Range | Order Number Am54S/74S240 | Am54S/74S241 | Am54S/74S242 | Am54S/74S243 | Am54S/74S244 |
|---|---|---|---|---|---|---|
| Hermetic | –55°C to +125°C | SN54S240J | SN54S241J | SN54S242J | SN54S243J | SN54S244J |
| Dice | –55°C to +125°C | AM54S240X | AM54S241X | AM54S242X | AM54S243X | AM54S244X |
| Hermetic | 0°C to +70°C | SN74S240J | SN74S241J | SN74S242J | SN74S243J | SN74S244J |
| Molded | 0°C to +70°C | SN74S240N | SN74S241N | | | SN74S244N |
| Dice | 0°C to +70°C | AM74S240X | AM74S241X | AM74S242X | AM74S243X | AM74S244X |

## LOGIC DIAGRAMS

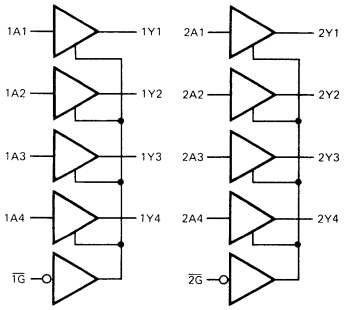
### Am54S/74S240



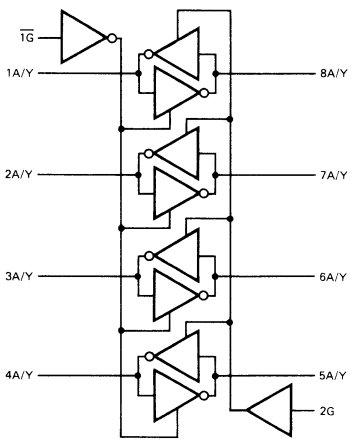

### Am54S/74S241



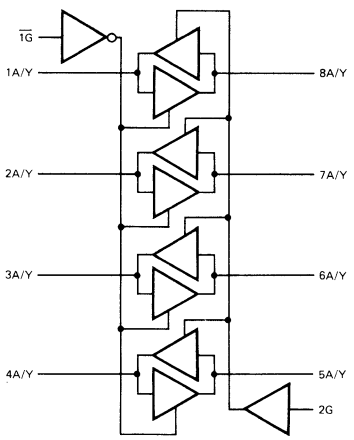

### Am54S/74S244




### Am54S/74S242




### Am54S/74S243




Note: All gates have input hysteresis.

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**MAXIMUM RATINGS** above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current | 150mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS

**The Following Conditions Apply Unless Otherwise Noted:**

| | | | |
|---|---|---|---|
| Am54S240/S241/S242/S243/S244 (MIL) | $T_A = -55°C$ to $+125°C$ | $V_{CC}$(MIN.) = 4.50V | $V_{CC}$(MAX.) = 5.50V |
| Am74S240/S241/S242/S243/S244 (COM'L) | $T_A = 0°C$ to $+70°C$ | $V_{CC}$(MIN.) = 4.75V | $V_{CC}$(MAX.) = 5.25V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

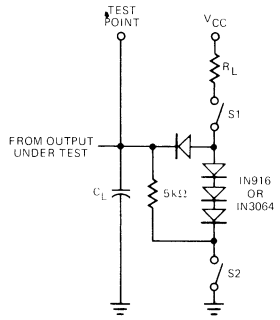
| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-Level Input Voltage | | | | 2.0 | | | Volts |
| $V_{IL}$ | Low-Level Input Voltage | | | | | | 0.8 | Volts |
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_I$ = −18mA | | | | | −1.2 | Volts |
| | Hysteresis ($V_{T+} - V_{T-}$) | $V_{CC}$ = MIN. | | | 0.2 | 0.4 | | Volts |
| $V_{OH}$ | High-Level Output Voltage | $V_{CC}$ = MIN., $V_{IL}$ = 0.8V, $I_{OH}$ = −3.0mA | | | 2.4 | 3.4 | | Volts |
| | | $V_{CC}$ = MIN., $V_{IL}$ = 0.5V | MIL, $I_{OH}$ = −12mA | | 2.0 | | | Volts |
| | | | COM'L, $I_{OH}$ = −15mA | | 2.0 | | | Volts |
| $V_{OL}$ | Low-Level Output Voltage | $V_{CC}$ = MIN., $V_{IL}$ = 0.8V | MIL, $I_{OL}$ = 48mA | | | | 0.55 | Volts |
| | | | COM'L, $I_{OL}$ = 64mA | | | | 0.55 | Volts |
| $I_{OZH}$ | Off-State Output Current, High Level Voltage Applied | $V_{CC}$ = MAX., $V_{IH}$ = 2.0V, $V_{IL}$ = 0.8V | | $V_O$ = 2.4V | | | 50 | µA |
| $I_{OZL}$ | Off-State Output Current, Low-Level Voltage Applied | | | $V_O$ = 0.5V | | | −50 | µA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = MAX., $V_I$ = 5.5V | | | | | 1.0 | mA |
| $I_{IH}$ | High-Level Input Current, Any Input | $V_{CC}$ = MAX., $V_{IH}$ = 2.7V | | | | | 50 | µA |
| $I_{IL}$ | Low-Level Input Current | $V_{CC}$ = MAX., $V_{IL}$ = 0.5V | Any A | | | | −400 | µA |
| | | | Any G | | | | −2.0 | mA |
| $I_{OS}$ | Short-Circuit Output Current (Note 3) | $V_{CC}$ = MAX. | | | −50 | | −225 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX., Outputs open | Am54S/74S240, Am54S/74S242 | All Outputs HIGH | MIL | | 80 | 123 | mA |
| | | | | | COM'L | | 80 | 135 | mA |
| | | | | All Outputs LOW | MIL | | 100 | 145 | mA |
| | | | | | COM'L | | 100 | 150 | mA |
| | | | | Outputs at Hi-Z | MIL | | 100 | 145 | mA |
| | | | | | COM'L | | 100 | 150 | mA |
| | | | Am54S/74S241, Am54S/74S243, Am54S/74S244 | All Outputs HIGH | MIL | | 95 | 147 | mA |
| | | | | | COM'L | | 95 | 160 | mA |
| | | | | All Outputs LOW | MIL | | 120 | 170 | mA |
| | | | | | COM'L | | 120 | 180 | mA |
| | | | | Outputs at Hi-Z | MIL | | 120 | 170 | mA |
| | | | | | COM'L | | 120 | 180 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are $V_{CC}$ = 5.0V, $T_A$ = 25° C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

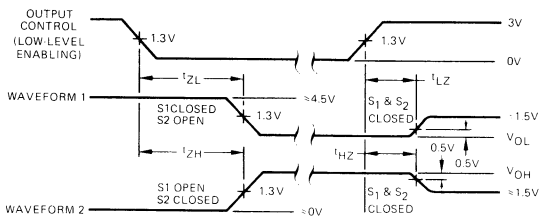
## SWITCHING CHARACTERISTICS ($V_{CC}$ = 5V, $T_A$ = 25°C)

| Parameter | Description | Test Conditions | Am54S/74S240, Am54S/74S242 | | | Am54S/74S241, Am54S/74S243, Am54S/74S244 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High-Level Output | $C_L$ = 50pF, $R_L$ = 90Ω (Note 3) | | 4.5 | 7.0 | | 6.0 | 9.0 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low-Level Output | | | 4.5 | 7.0 | | 6.0 | 9.0 | ns |
| $t_{ZL}$ | Output Enable Time to Low Level | | | 10 | 15 | | 10 | 15 | ns |
| $t_{ZH}$ | Output Enable Time to High Level | | | 6.5 | 10 | | 8.0 | 12 | ns |
| $t_{LZ}$ | Output Disable Time from Low Level | $C_L$ = 5.0pF, $R_L$ = 90Ω (Note 3) | | 10 | 15 | | 10 | 15 | ns |
| $t_{HZ}$ | Output Disable Time from High Level | | | 6.0 | 9.0 | | 6.0 | 9.0 | ns |

### LOAD CIRCUIT FOR THREE-STATE OUTPUTS




### VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS




Notes:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

## FUNCTION TABLES

**Am54S/74S242**

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{1G}$ | 2G | A | Y |
| H | L | X | Z |
| L | H | L | H |
| L | H | H | L |

**Am54S/74S240**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

**Am54S/74S241**
**Am54S/74S243**

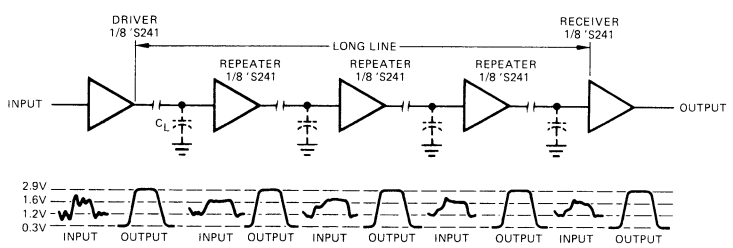
| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{1G}$ | 2G | A | Y |
| H | L | X | Z |
| L | H | H | H |
| L | H | L | L |

**Am54S/74S244**

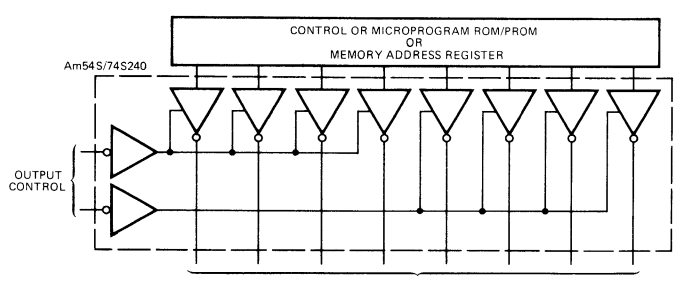
| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{G}$ | A | |
| H | X | Z |
| L | H | H |
| L | L | L |

## APPLICATIONS

### Am54S/74S241'S USED AS REPEATER/LEVEL RESTORER

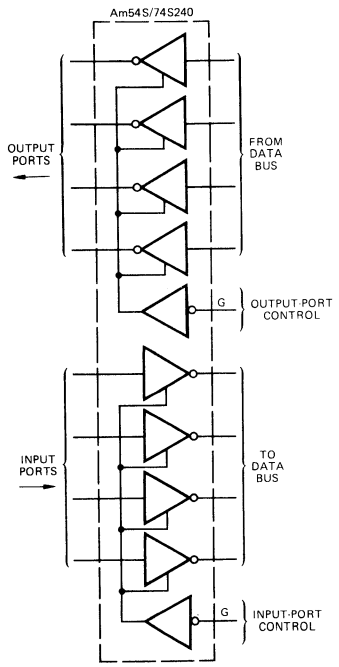



### 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER – 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD

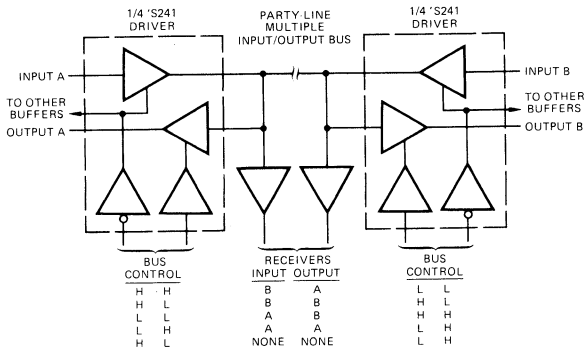


## APPLICATIONS (Cont.)

### INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE

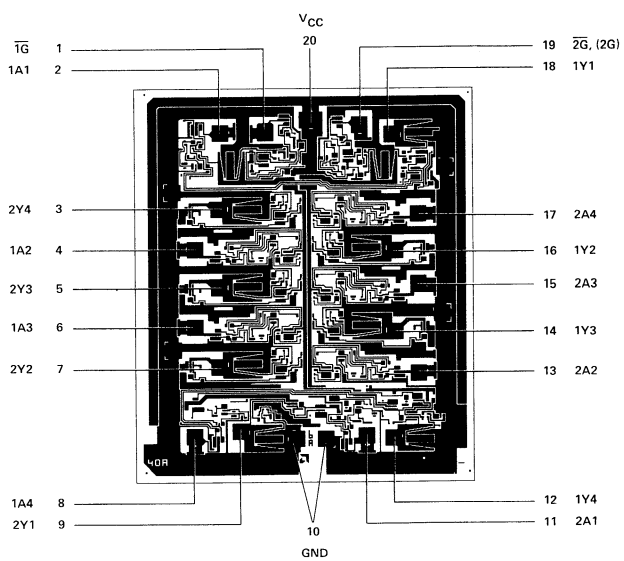



### PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS




### Metallization and Pad Layout

**Am54S/74S240 • Am54S/74S241 • Am54S/74S244**




DIE SIZE 0.093" X 0.109"

# Am54S/74S257•Am54S/74S258

## Quadruple 2-Line To 1-Line Data

### Distinctive Characteristics

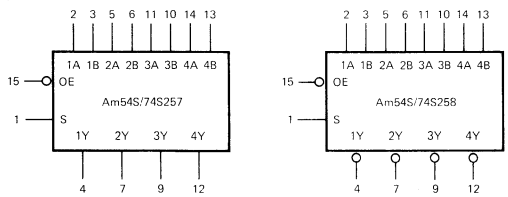
- Three-state outputs interface directly with bus organized systems
- Schottky clamp provides improved AC performance
- Pin assignments identical with Am54S/74S157 and Am54S/74S158
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The 2-line to 1-line data selector multiplexer can be used to transfer data to a common data bus directly by using the three-state capability of the device. With the output control ($\overline{OE}$) HIGH, the four outputs of the data selector are in the high impedance state. With the output control LOW, the selected four bits (A or B inputs) are bussed onto the four data lines.

The typical propagation delay times from data input to output average 4.8ns for the Am54S/74S257 and 4ns for the Am54S/74S258. Also, to minimize the possibility that two outputs will attempt to drive the common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

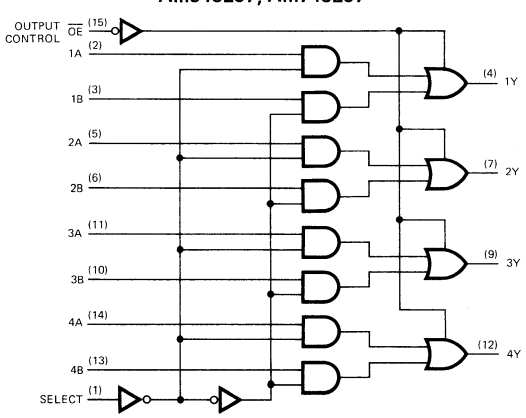
### LOGIC SYMBOL



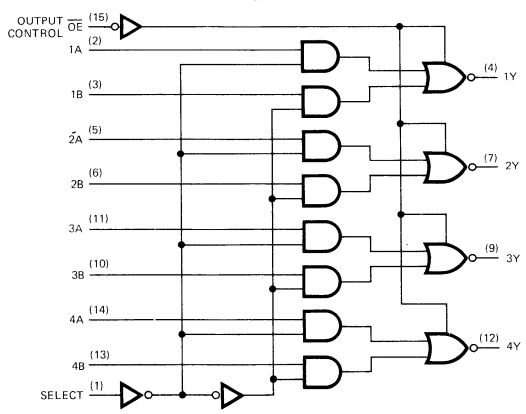

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

Am54S257, Am74S257



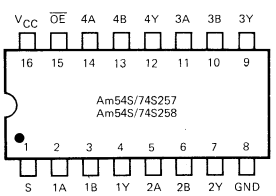

Am54S258, Am74S258




### ORDERING INFORMATION

| Package Type | Temperature Range | Am54S/74S257 Order Number | Am54S/74S258 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | SN74S257N | SN74S258N |
| Hermetic DIP | 0°C to +70°C | SN74S257J | SN74S258J |
| Dice | 0°C to +70°C | SN74S257X | SN74S258X |
| Hermetic DIP | -55°C to +125°C | SN54S257J | SN54S258J |
| Hermetic Flat Pack | -55°C to +125°C | SN54S257W | SN54S258W |
| Dice | -55°C to +125°C | SN54S257X | SN54S258X |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation on flat package only.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | | |
|---|---|---|---|---|---|
| Am74S257/S258 | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% | (Com'l) | Min = 4.75 V | Max = 5.25 V |
| Am54S257/S258 | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% | (Mil) | Min = 4.5 V | Max = 5.5 V |

| Parameters | Description | | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 54S, $I_{OH}$ = −2mA | 2.4 | 3.4 | | Volts |
| | | | | 74S, $I_{OH}$ = −6.5mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ = MIN., $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 20mA | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Unit Load Input LOW Current | S Input | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −4 | mA |
| | | Any Other | | | | | −2 | |
| $I_{IH}$ (Note 3) | Unit Load Input HIGH Current | S Input | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 100 | µA |
| | | Any Other | | | | | 50 | |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1 | mA |
| $I_O$ | Off-State (HIGH Impedance) Output Current | | $V_{CC}$ = MAX. | $V_O$ = 2.4V | | | 50 | µA |
| | | | | $V_O$ = 0.5V | | | −50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | All Outputs HIGH | $V_{CC}$ = MAX. (Note 5) | Am54S/74S257 | | 44 | 68 | mA |
| | | | | Am54S/74S258 | | 36 | 56 | |
| | | All Outputs LOW | | Am54S/74S257 | | 60 | 93 | mA |
| | | | | Am54S/74S258 | | 52 | 81 | |
| | | All Outputs OFF | | Am54S/74S257 | | 64 | 99 | mA |
| | | | | Am54S/74S258 | | 56 | 87 | |

Notes:
1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual Input Currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
5. $I_{CC}$ is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

## Switching Characteristics ($T_A$ = 25°C)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data to Output | S257 | $V_{CC}$ = 5 V, $R_L$ = 280 Ω, $C_L$ = 15 pF | | 5 | 7.5 | ns |
| | | S258 | | | 4 | 6 | |
| $t_{PHL}$ | Data to Output | S257 | | | 4.5 | 6.5 | ns |
| | | S258 | | | 4 | 6 | |
| $t_{PLH}$ | Select to Output | S257 | | | 8.5 | 15 | ns |
| | | S258 | | | 8 | 12 | |
| $t_{PHL}$ | Select to Output | S257 | | | 8.5 | 15 | ns |
| | | S258 | | | 7.5 | 12 | |
| $t_{ZH}$ | Control to Output | | | | 13 | 19.5 | ns |
| $t_{ZL}$ | | | | | 14 | 21 | |
| $t_{HZ}$ | Control to Output | | $V_{CC}$ = 5 V, $R_L$ = 280 Ω, $C_L$ = 5 pF | | 5.5 | 8.5 | ns |
| $t_{LZ}$ | | | | | 9 | 14 | |

## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| Output Control | Select | A | B | Am54S/ 74S257 | Am54S/ 74S258 |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH 54S | Fan-out Output HIGH 74S | Fan-out Output LOW |
|---|---|---|---|---|---|
| **S** | 1 | 2 | – | – | – |
| **1A** | 2 | 1 | – | – | – |
| **1B** | 3 | 1 | – | – | – |
| **1Y** | 4 | – | 40 | 130 | 10 |
| **2A** | 5 | 1 | – | – | – |
| **2B** | 6 | 1 | – | – | – |
| **2Y** | 7 | – | 40 | 130 | 10 |
| **GND** | 8 | – | – | – | – |
| **3Y** | 9 | – | 40 | 130 | 10 |
| **3B** | 10 | 1 | – | – | – |
| **3A** | 11 | 1 | – | – | – |
| **4Y** | 12 | – | 40 | 130 | 10 |
| **4B** | 13 | 1 | – | – | – |
| **4A** | 14 | 1 | – | – | – |
| **$\overline{OE}$** | 15 | 1 | – | – | – |
| **$V_{CC}$** | 16 | – | – | – | – |

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and –2.0mA measured at 0.5V LOW.

## FUNCTIONAL TERMS

**1A, 2A, 3A, 4A** The data inputs for the 4-bits of the A word.

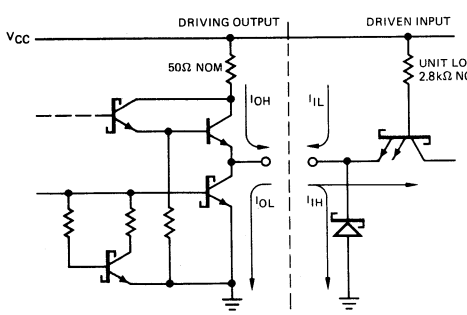
**1B, 2B, 3B, 4B** The data inputs for the 4-bits of the B word.

**1Y, 2Y, 3Y, 4Y** The four outputs of the multiplexer.

**$\overline{OE}$ Output Control** When the output control is HIGH, the four outputs are in the high impedance state. When the output control is LOW, the selected A or B input is present at the output.

**S Select** When the select input is LOW, the A word is present at the output. When the select input is HIGH, the B word is present at the output.

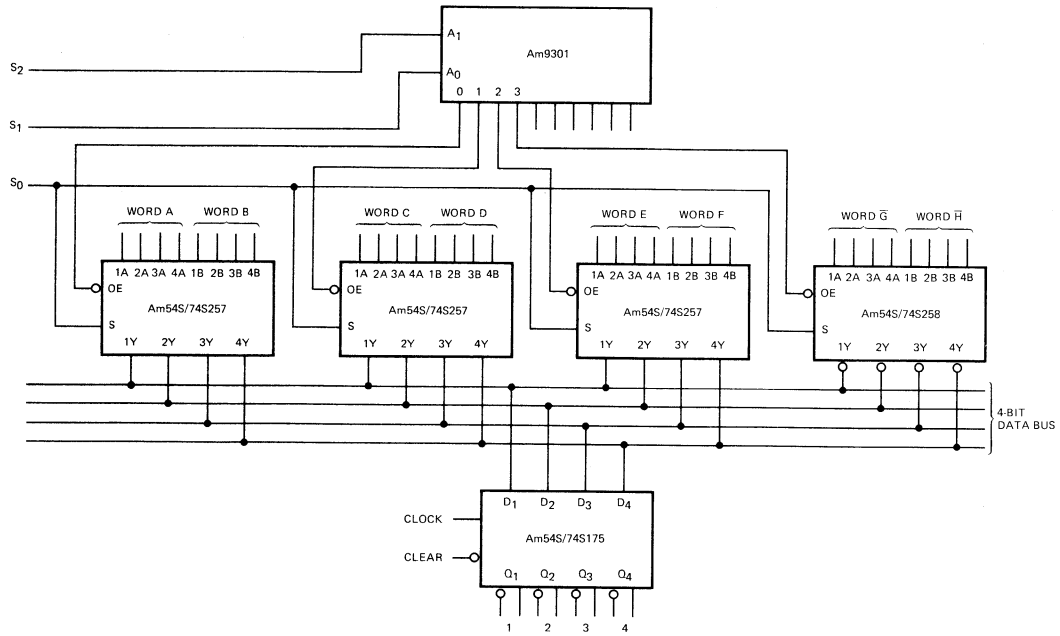
## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown

4

## APPLICATIONS




**8-Word, 4-Bit Multiplexer**

## APPLICATION BRIEF – THREE STATE OUTPUTS

When a three-state Schottky output is in the high-impedance state, the maximum off-state leakage current is specified as 50μA at 2.4V and −50μA at 0.5V. This leakage loading must be added to the input loading of the devices connected to the data bus for worst-case design. For this reason, the output HIGH source current of the three-state devices are specified with $I_{OH}$ = −2mA for the Am54S series and $I_{OH}$ = −6.5 mA for the Am74S series. The output LOW sink current for all Am54S/74S devices is specified as $I_{OL}$ = 20mA at 0.5V.

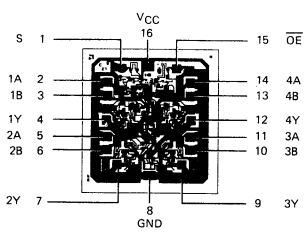
The high current sinking and sourcing capability allows many three-state outputs to be bus-organized and drive several TTL inputs reliably. An example of the $I_{OH}$ and $I_{OL}$ loading calculations is shown in Table I. The important factor for bus-organized three-state outputs is not to exceed either the HIGH-state or the LOW-state maximum loading.

## TABLE I

| NO. OF LOADING DEVICES ON BUS | TYPE LOAD | | DATA BUS HIGH LOAD | DATA BUS LOW LOAD |
|---|---|---|---|---|
| 36 | 54S/74S outputs Hi-Z | | 50μA x 36 = 1.8mA | −50μA x 36 = −1.8mA |
| 4 | 54S/74S inputs | | 50μA x 4 = .2mA | −2mA x 4 = −8.0mA |
| | | | 2.0mA | −9.8mA |
| OUTPUT LOADING USED | | Am54S | MAXIMUM | ~ 50% |
| | | Am74S | ~ 31% | ~ 50% |

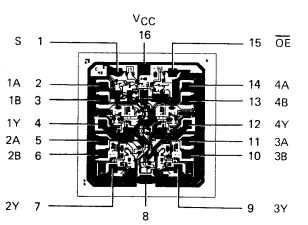
### Metallization and Pad Layouts

**Am54S/74S257**




DIE SIZE 0.065" X 0.069"

**Am54S/74S258**




DIE SIZE 0.065" X 0.069"

# Am54S/74S350

## Four-Bit Shifter With Three-State Outputs

### Distinctive Characteristics

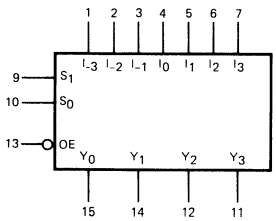
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5ns typical data propagation delay.
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am54S/74S350 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field $S_0$ and $S_1$. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

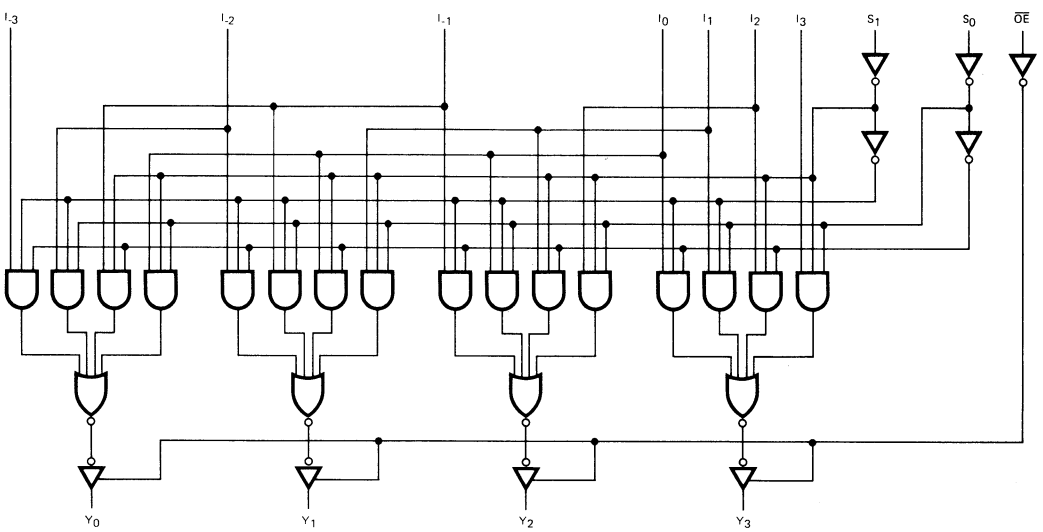
By suitable interconnection, the Am54S/74S350 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

### LOGIC SYMBOL

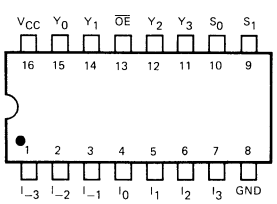



$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAM




### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | | |
|---|---|---|---|---|---|
| SN74S350 | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0 V ±5% (COM'L) | MIN. = 4.75 V | MAX. = 5.25 V |
| SN54S350 | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0 V ±10% (MIL) | MIN. = 4.5 V | MAX. = 5.5 V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL, $I_{OH}$ = −2mA | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH}$ = −6.5mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2.0 | mA |
| $I_{IH}$ | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_O$ | Off State (High Impedance) Output Current | $V_{CC}$ = MAX. | $V_O$ = 2.4 V | | | 50 | μA |
| | | | $V_O$ = 0.5 V | | | −50 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0 V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX., All outputs open, All inputs = GND | | | 60 | 85 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Data Input to Output | $V_{CC}$ = 5.0 V, $C_L$ = 15pF, $R_L$ = 280Ω | | 5 | 7.5 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | Select to Output | | | 11 | 17 | ns |
| $t_{PHL}$ | | | | 13 | 20 | |
| $t_{ZH}$ | Output Control $\overline{OE}$ to Output | | | | 19.5 | ns |
| $t_{ZL}$ | | | | | 21 | |
| $t_{HZ}$ | Output Control $\overline{OE}$ to Output | $V_{CC}$ = 5 V, $C_L$ = 5pF, $R_L$ = 280Ω | | 5 | 8 | ns |
| $t_{LZ}$ | | | | 10 | 15 | |

# Am54S/74S373 • Am54S/74S533

## Octal Latches with Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- 8 latches in a single package
- Am54S/74S373 has non-inverting outputs
- Am54S/74S533 has inverting outputs
- $V_{OL}$ = 0.5V (max) at $I_{OL}$ = 20mA
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- High speed – Clock to output 12ns typical
- 100% product assurance screening to MIL-STD-883 requirements

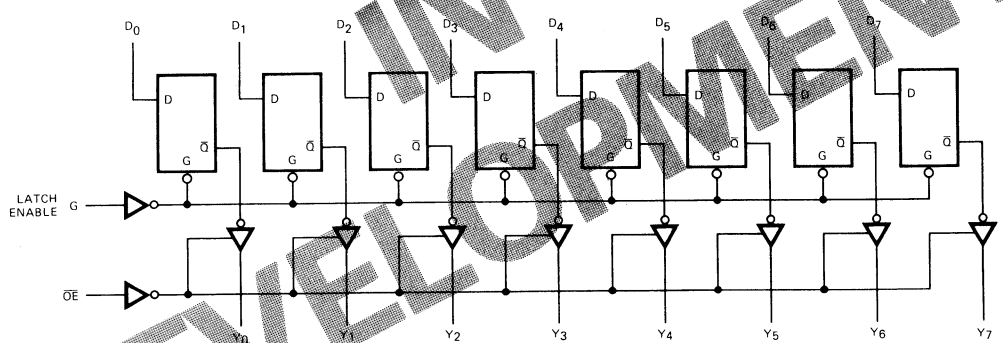
### FUNCTIONAL DESCRIPTION

The Am54S/74S373 is an octal latch with three-state outputs for bus organized system applications. The latching flip-flops appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

Am25S373 and Am25S533 versions are also available offering $V_{OL}$ = 0.5V (max) at $I_{OL}$ = 32mA.



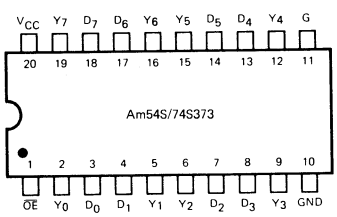
### LOGIC DIAGRAM
**Am54S/74S373**




Outputs $Y_0$ through $Y_7$ are inverted on the Am54S/74S533.

MPR-360

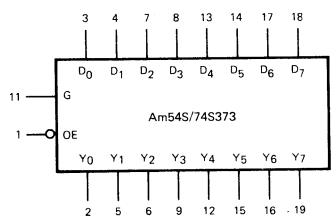
### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

MPR-361

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

MPR-362

4

# Am54S/74S374 • Am54S/74S534

## 8-Bit Registers with Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Eight-bit, high speed parallel registers
- Am54S/74S374 has non-inverting outputs
- Am54S/74S534 has inverting outputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- $V_{OL}$ = 0.5V (max) at $I_{OL}$ = 20mA
- High speed – Clock to output 11ns typical
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The Am54/74S374 and Am54S/74S534 are eight-bit registers built using high speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

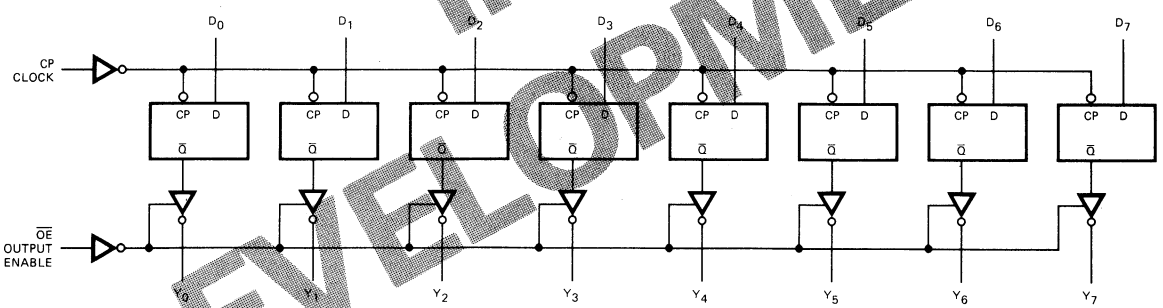
The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

Am25S374 and Am25S534 versions are also available offering $V_{OL}$ = 0.5V (max) at $I_{OL}$ = 32mA.



### LOGIC DIAGRAM

**Am54S/74S374**

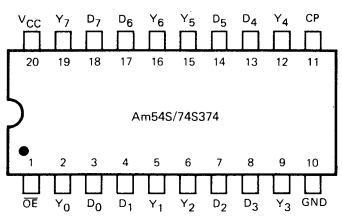



Outputs $Y_0$ through $Y_7$ are inverted on the Am54/74S534.

MPR-363

### CONNECTION DIAGRAM

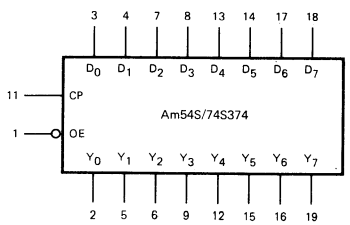
Top View




Note: Pin 1 is marked for orientation.

MPR-364

### LOGIC SYMBOL




$V_{CC}$ = Pin 20

GND = Pin 10

MPR-365

# Am54S/74S378 • Am54S/74S379

## Hex/Quad Parallel D Registers With Register Enable

### Distinctive Characteristics

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

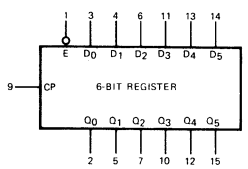
### FUNCTIONAL DESCRIPTION

The Am54S/74S378 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am54S/74S379 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

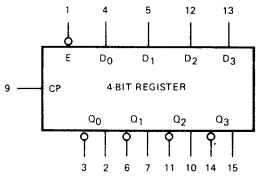
Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

### LOGIC SYMBOLS

Am54S/74S378



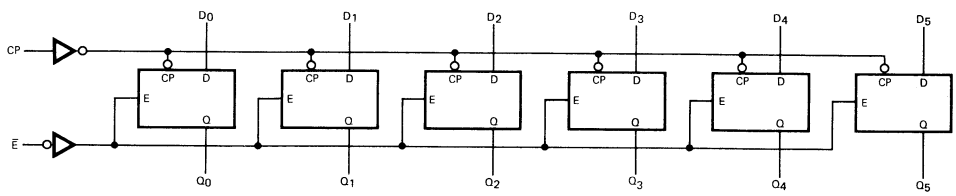

Am54S/74S379



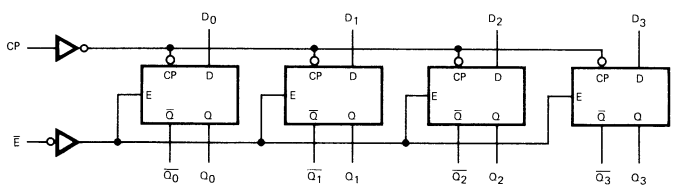

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

Am54S/74S378



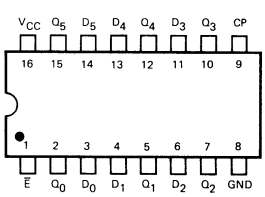

Am54S/74S379



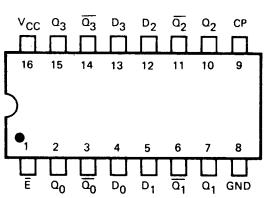

### CONNECTION DIAGRAMS

Top Views

Am54S/74S378




Am54S/74S379




Note: Pin 1 is marked for orientation.

4

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SN74S378, SN74S379 $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
SN54S378, SN54S379 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L | 2.7 | 3.4 | | Volts |
| | | | MIL | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18 mA | | | | −1.2 | Volts |
| $I_{IL}$ | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2 | mA |
| $I_{IH}$ | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | S378 | | 90 | 144 | mA |
| | | | S379 | | 60 | 96 | |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5 V, measured after a momentary ground, then 4.5 V applied to the clock input.

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Output | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF, $R_L$ = 280Ω | 4 | 8 | 12 | ns |
| $t_{PHL}$ | Clock to Output | | 4 | 11.5 | 17 | ns |
| $t_{pw}$ | Clock Pulse Width | | 7 | | | ns |
| $t_s$ | Data | | 5.5 | | | ns |
| $t_s$ | Enable | | 9 | | | ns |
| $t_h$ | Data | | 3 | | | ns |
| $t_h$ | Enable | | 3 | | | ns |

# Am54S/74S388

## Quad D Register With Standard And Three-State Outputs

### Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am54S/74S388 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

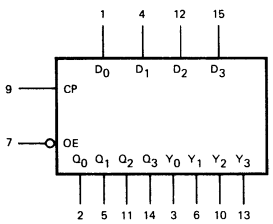
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" (OE) input is LOW. When the OE input is HIGH, the Y ouptuts are in the high-impedance state.

The Am54S/74S388 is a 4-bit, high-speed Schottky register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

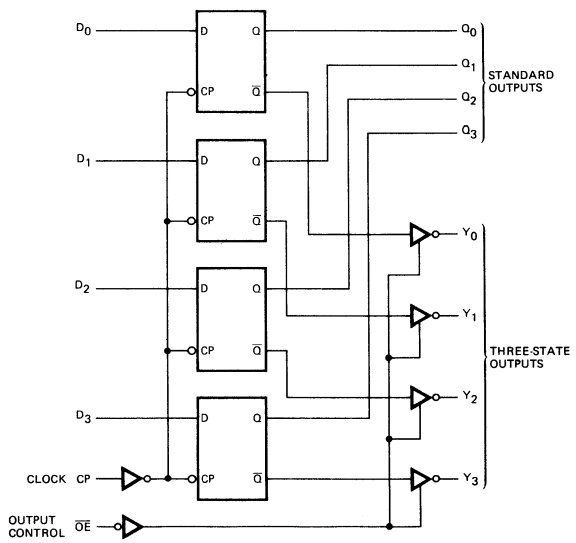
Likewise, the Am54S/74S388 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

### LOGIC SYMBOL

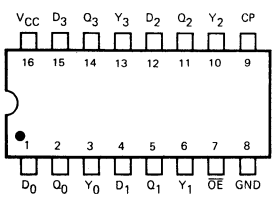



$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAM




### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

4

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| SN74S388 | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ± 5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| SN54S388 | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ± 10% (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | Q | $I_{OH}$ = −1mA MIL | 2.5 | 3.4 | | Volts |
| | | | | $I_{OH}$ = −1mA COM'L | 2.7 | 3.4 | | |
| | | | Y | MIL, $I_{OH}$ = −2mA | 2.4 | 3.4 | | |
| | | | | COM'L, $I_{OH}$ = −6.5mA | 2.4 | 3.2 | | |
| $V_{OL}$ | Output LOW Voltage (Note 6) | $V_{CC}$ = MIN., $I_{OL}$ = 20mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | | −2.0 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | | 50 | µA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | | 1.0 | mA |
| $I_O$ | Y Output Off-State Leakage Current | $V_{CC}$ = MAX. | | $V_O$ = 2.4V | | | 50 | µA |
| | | | | $V_O$ = 0.4V | | | −50 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | | 80 | 130 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, $T_A$ = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
4. $I_{CC}$ is measured with all inputs at 4.5V and all outputs open.
5. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

## Switching Characteristics ($T_A$ = +25°C, $V_{CC}$ = 5.0V, $R_L$ = 280Ω)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Q Output | | $C_L$ = 15pF | | 6.0 | 9.0 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13 | |
| $t_{pw}$ | Clock Pulse Width | HIGH | | 7.0 | | | ns |
| | | LOW | | 9.0 | | | |
| $t_s$ | Data | | | 5.0 | | | ns |
| $t_h$ | Data | | | 3.0 | | | ns |
| $t_{PLH}$ | Clock to Y Output ($\overline{OE}$ LOW) | | | | 6.0 | 9.0 | ns |
| $t_{PHL}$ | | | | | 8.5 | 13 | |
| $t_{ZH}$ | Output Control to Output | | $C_L$ = 15pF | | 12.5 | 19 | ns |
| $t_{ZL}$ | | | | | 12 | 18 | |
| $t_{HZ}$ | | | $C_L$ = 5.0pF | | 4.0 | 6.0 | |
| $t_{LZ}$ | | | | | 7.0 | 10.5 | |
| $f_{max}$ | Maximum Clock Frequency | | $C_L$ = 15pF | 75 | 100 | | MHz |

# Am54S/74S399
## Quad Two-Input, High-Speed Register

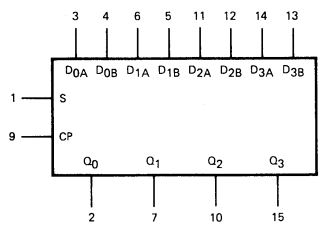
### Distinctive Characteristics

- Four-bit register accepts data from one of two 4-bit input fields
- Edge triggered clock action
- High-speed Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

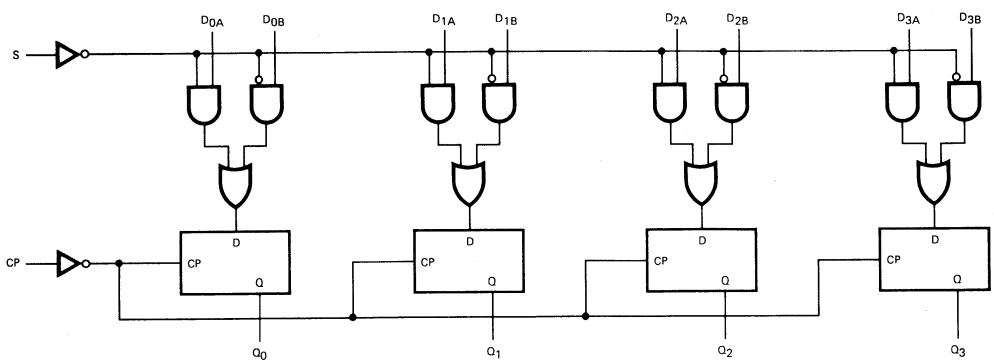
The Am54S/74S399 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the $D_{iA}$ input data will be stored in the register. When the S input is HIGH, the $D_{iB}$ input data will be stored in the register.

### LOGIC SYMBOL

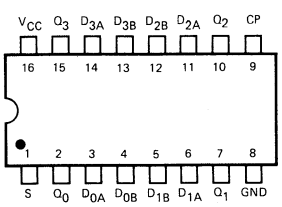



$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAM




### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +5.5 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SN74S399 $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0 V ± 5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
SN54S399 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0 V ± 10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L | 2.7 | 3.4 | | Volts |
| | | | MIL | 2.5 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.3 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5 V | | | | −2.0 | mA |
| $I_{IH}$ | Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 4) | | | 75 | 120 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with Select and Clock inputs at 4.5 V; all data inputs at 0 V; all outputs open.

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to Q HIGH | $V_{CC}$ = 5.0 V, $C_L$ = 15pF, $R_L$ = 280Ω | | 8 | 12 | ns |
| $t_{PHL}$ | Clock to Q LOW | | | 11.5 | 17 | ns |
| $t_{pw}$ | Clock Pulse Width | | 7 | | | ns |
| $t_s$ | Data Set-up Time | | 5.5 | | | ns |
| $t_s$ | Select Input Set-up Time | | 10 | | | ns |
| $t_h$ | Data Hold Time | | 3 | | | ns |
| $t_h$ | Select Input Hold Time | | 3 | | | ns |

# Am54S/74S412

**Eight-Bit Input/Output Port**

**The 54S/74S412 is Texas Instruments' second source part number to the AMD/Intel 8212 device.**

**See the Am8212 data sheet for full information.**

# Am3212•Am8212
## Eight-Bit Input/Output Port

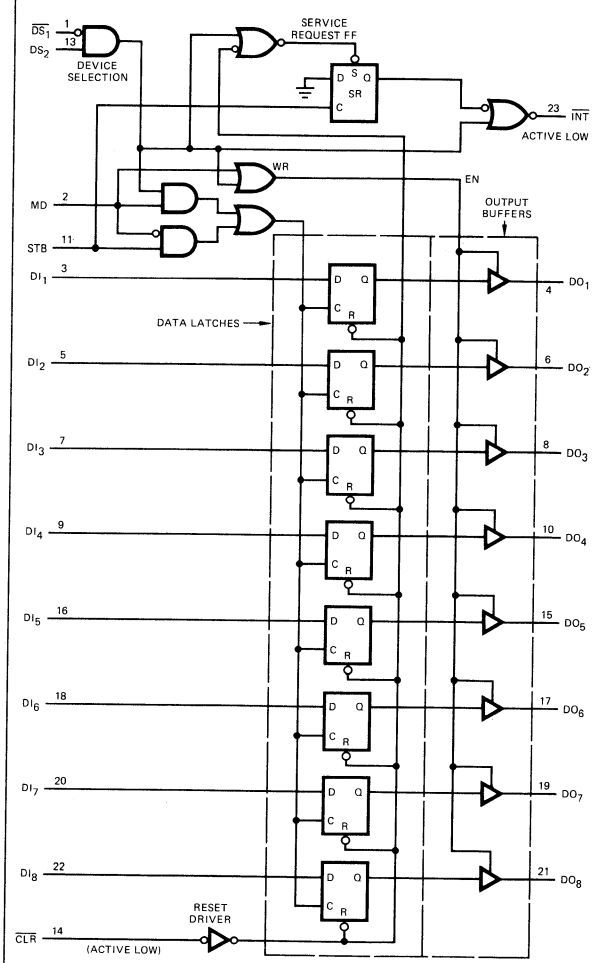
### Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

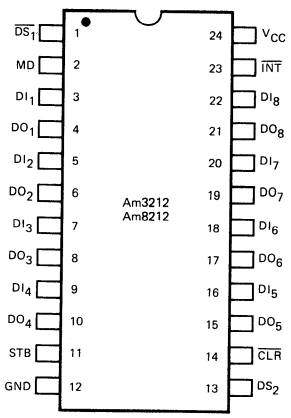
### FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am3212 • Am8212. The Am3212 • Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

### LOGIC DIAGRAM




### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### PIN DEFINITION

| | |
|---|---|
| $DI_1 - DI_8$ | DATA IN |
| $DO_1 - DO_8$ | DATA OUT |
| $\overline{DS_1} - DS_2$ | DEVICE SELECT |
| MD | MODE |
| STB | STROBE |
| $\overline{INT}$ | INTERRUPT (ACTIVE LOW) |
| $\overline{CLR}$ | CLEAR (ACTIVE LOW) |

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | –55°C to +125°C | AM8212DM |
| Hermetic DIP | 0°C to +70°C | D8212 |
| Molded DIP | 0°C to +70°C | P8212 |
| Dice | 0°C to +70°C | AM8212XC |
| Hermetic DIP | 0°C to +70°C | D3212 |
| Hermetic DIP | –55°C to +125°C | MD3212 |
| Molded DIP | 0°C to +70°C | P3212 |

## FUNCTIONAL DESCRIPTION (Cont'd)

### Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

### Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am3212 • Am8212 to be connected directly onto the microprocessor bi-directional data bus.

### Control Logic

The Am3212 • Am8212 has control inputs $\overline{DS}_1$, $DS_2$, MD And STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

### $\overline{DS}_1$, $DS_2$ (Device Select)

These 2 inputs are used for device selection. When $\overline{DS}_1$ is low and $DS_2$ is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

### MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

### STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

### Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

## TRUTH TABLE

| STB | MD | $\overline{DS}_1 - DS_2$ | Data Out Equals |
|---|---|---|---|
| 0 | 0 | 0 | Three-State |
| 1 | 0 | 0 | Three-State |
| 0 | 1 | 0 | Data Latch |
| 1 | 1 | 0 | Data Latch |
| 0 | 0 | 1 | Data Latch |
| 1 | 0 | 1 | Data In |
| 0 | 1 | 1 | Data In |
| 1 | 1 | 1 | Data In |

| CLR | $\overline{DS}_1 - DS_2$ | STB | SR* | $\overline{INT}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | ↓ | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | ↓ | 1 | 0 |
| | | | | |
| | | | | |

$\overline{CLR}$ — Resets Data Latch
— Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

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## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage | −0.5V to +7.0V |
| Output Voltage | −0.5V to +7.0V |
| Input Voltages | −1.0V to +5.5V |
| Output Current (Each Output) | 125mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212, P3212, D3212 (COM'L) $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ± 5%
Am8212DM, MD3212 (MIL) $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ± 10%

### DC CHARACTERISTICS

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_F$ | Input Load Current ACK, $DS_2$, CR, $DI_1$ – $DI_8$ Inputs | $V_F$ = 0.45V | | | | −0.25 | mA |
| $I_F$ | Input Load Current MD Input | $V_F$ = 0.45V | | | | −0.75 | mA |
| $I_F$ | Input Load Current $DS_1$ Input | $V_F$ = 0.45V | | | | −1.0 | mA |
| $I_R$ | Input Leakage Current ACK, DS, CR, $DI_1$ – $DI_8$ Inputs | $V_R$ = 5.25V | | | | 10 | µA |
| $I_R$ | Input Leakage Current MO Input | $V_R$ = 5.25V | | | | 30 | µA |
| $I_R$ | Input Leakage Current $DS_1$ Input | $V_R$ = 5.25V | | | | 40 | µA |
| $V_C$ | Input Forward Voltage Clamp | $I_C$ = −5.0mA | COM'L | | | −1.0 | Volts |
| | | | MIL | | | −1.2 | |
| $V_{IL}$ | Input LOW Voltage | | COM'L | | | 0.85 | Volts |
| | | | MIL | | | 0.80 | |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 15mA | | | | 0.45 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −1.0mA | COM'L | 3.65 | 4.0 | | Volts |
| | | | MIL | 3.3 | 4.0 | | |
| | | $I_{OH}$ = −0.5mA | MIL | 3.5 | 4.0 | | |
| $I_{SC}$ | Short Circuit Output Current | $V_O$ = 0V | | −15 | | −75 | mA |
| $\|I_O\|$ | Output Leakage Current High Impedance | $V_O$ = 0.45V/5.25V | | | | 20 | µA |
| $I_{CC}$ | Power Supply Current | Note 2 | | | 90 | 130 | mA |

### AC CHARACTERISTICS (Note 3)

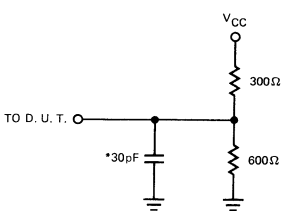
| Parameters | Description | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|
| $t_{pw}$ | Pulse Width | 30 | 8 | | ns |
| $t_{pd}$ | Data to Output Delay | | 12 | 30 | ns |
| $t_{we}$ | Write Enable to Output Delay | | 18 | 40 | ns |
| $t_{set}$ | Data Set-up Time | 15 | | | ns |
| $t_h$ | Data Hold Time | 20 | | | ns |
| $t_r$ | Reset to Output Delay | | 18 | 40 | ns |
| $t_s$ | Set to Output Delay | | 15 | 30 | ns |
| $t_e$ | Output Enable/Disable Time | | 14 | 45 | ns |
| $t_c$ | Clear to Output Delay | | 25 | 55 | ns |

### CAPACITANCE (Note 4)

F = 1.0MHz, $V_{BIAS}$ = 2.5V, $V_{CC}$ = +5.0V, $T_A$ = 25°C

| Parameters | Description | Typ. | Max. | Units |
|---|---|---|---|---|
| $C_{IN}$ | $DS_1$ MD Input Capacitance | 9.0 | 12 | pF |
| $C_{IN}$ | $DS_2$, CK, ACK, $DI_1$–$DI_8$ Input Capacitance | 5.0 | 9.0 | pF |
| $C_{OUT}$ | $DO_1$–$DO_8$ Output Capacitance | 8.0 | 12 | pF |

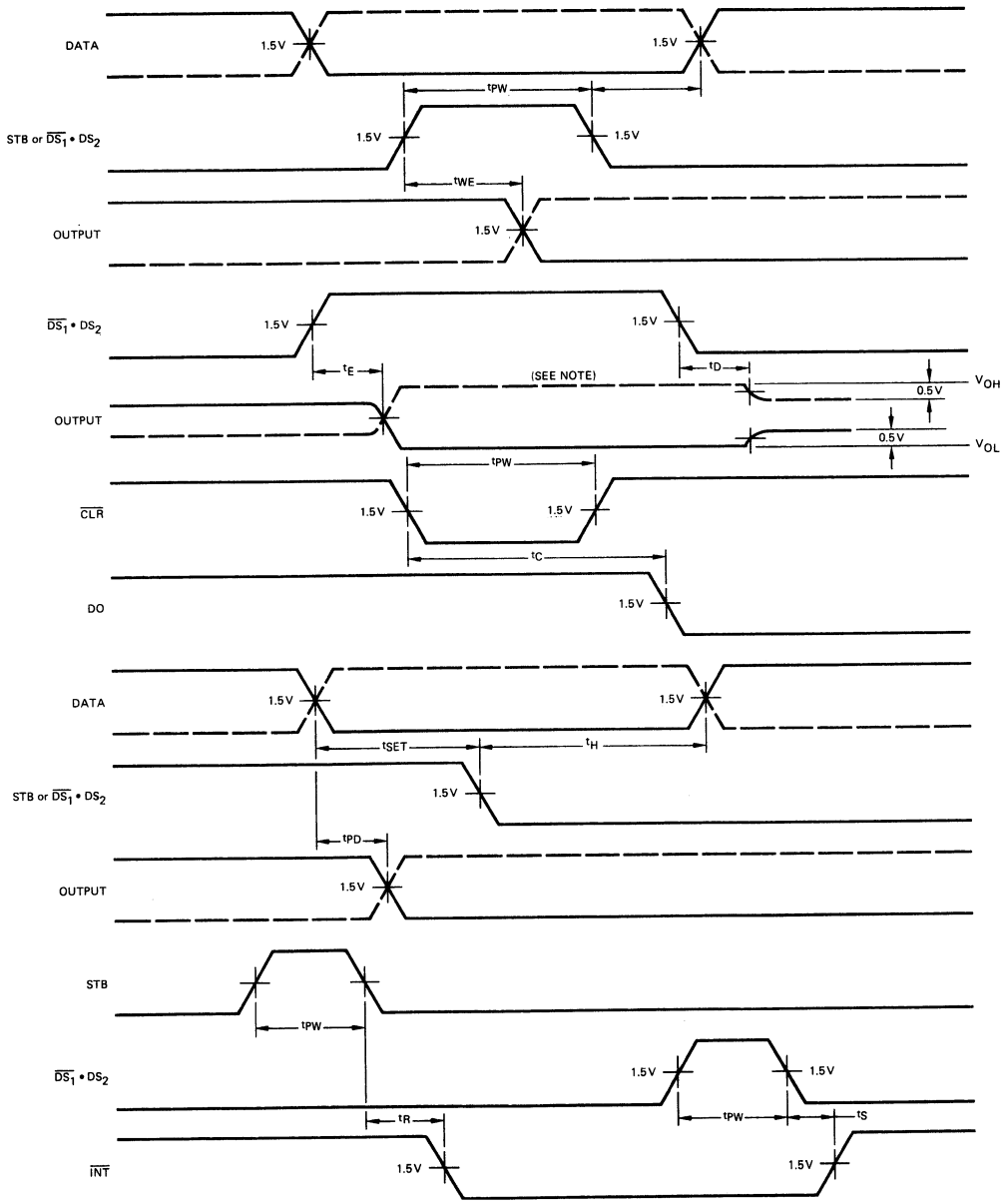
### TEST LOAD (15mA and 30pF)



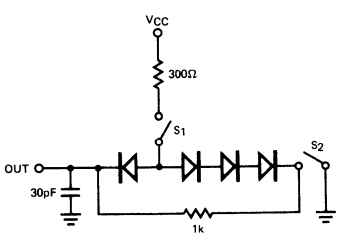

*Including Jig and Probe Capacitance.

Notes: 1. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; $DS_1$ = $DS_2$ = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

## TIMING DIAGRAM




Note: Alternative Test Load.

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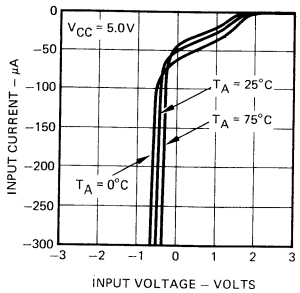
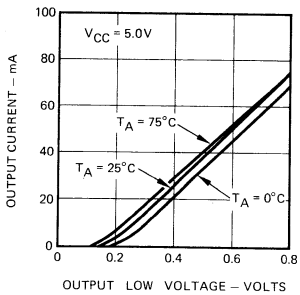
## TYPICAL CHARACTERISTICS

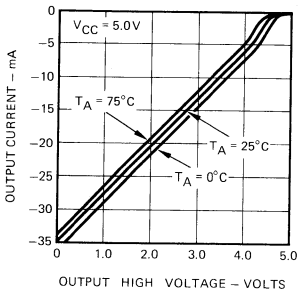
### Input Current Versus Input Voltage



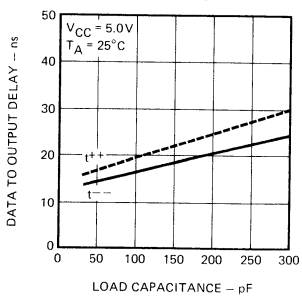

### Output Current Versus Output LOW Voltage



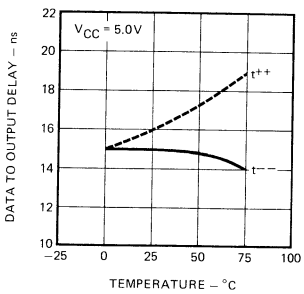

### Output Current Versus Output HIGH Voltage



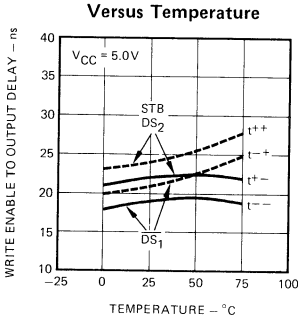

### Data to Output Delay Versus Load Capacitance




### Data to Output Delay Versus Temperature

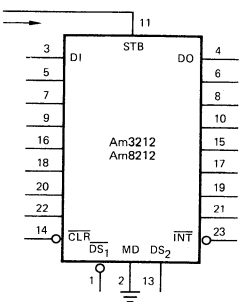



### Write Enable to Output Delay Versus Temperature



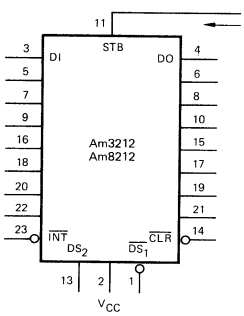

## LOGIC SYMBOLS

### INPUT DEVICE

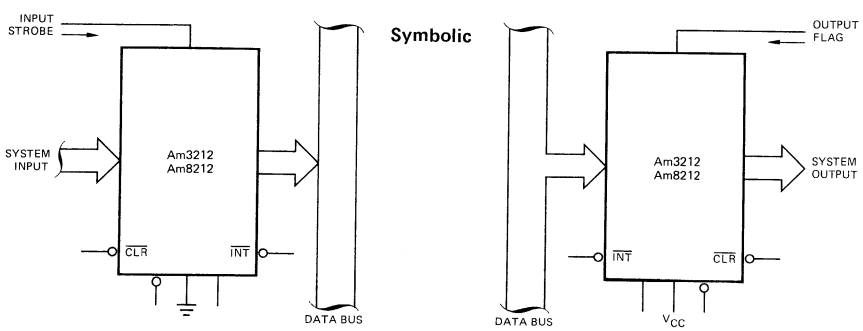



### Detailed

### OUTPUT DEVICE




### Symbolic



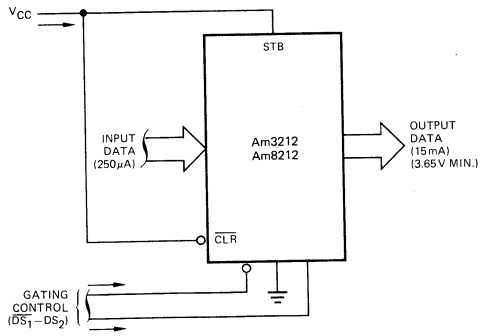
# TYPICAL APPLICATIONS OF THE Am8212

## GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and $DS_2$.

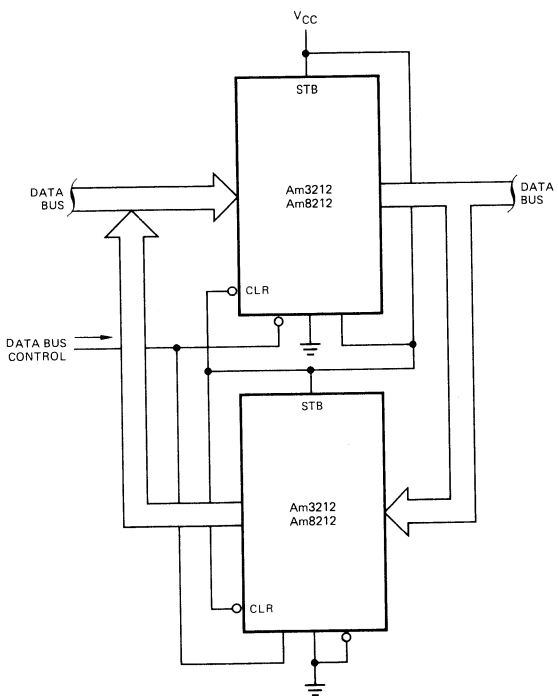
When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output.



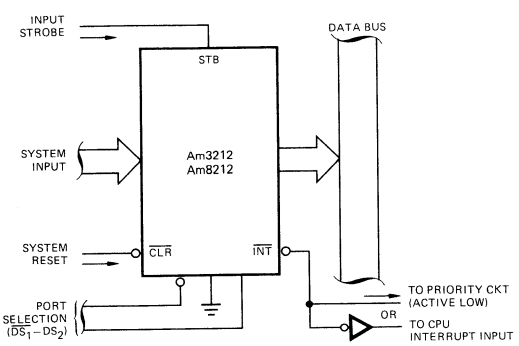

## Bi-Directional Bus Driver

Two Am3212 • Am8212's wired back-to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am3212 • Am8212 and to $DS_2$ on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.




## Interrupting Input Port

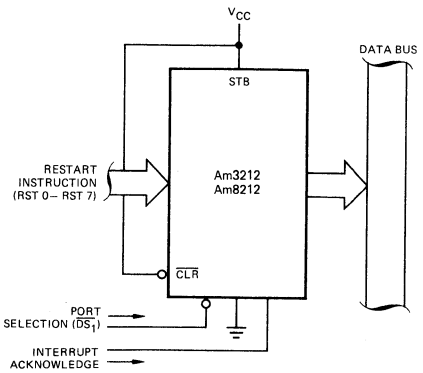
The Am3212 • Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true – enabling the system input data onto the data bus.



## TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

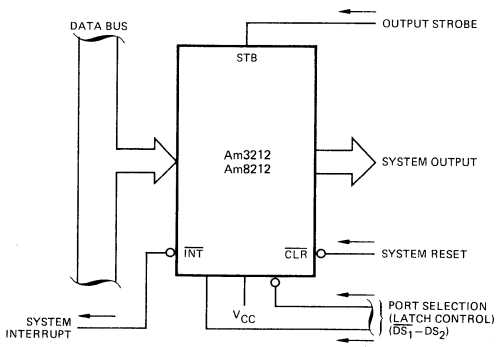
### Interrupt Instruction Port

The Am3212 • Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).



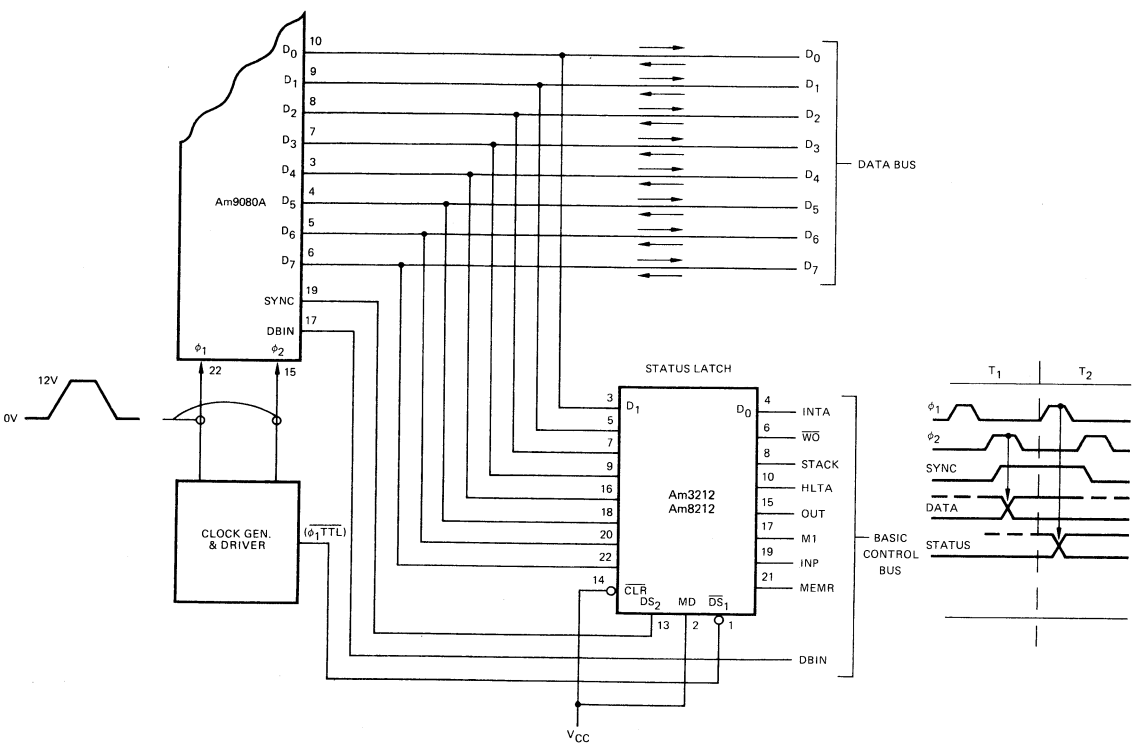

### Output Port (With Hand-Shaking)

The Am3212 • Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of date. The selection of the port comes from the device selection logic. ($\overline{DS_1} \cdot DS_2$).




### Am9080A Status Latch

The input to the Am3212 • Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am3212 • Am8212. The mode signal is tied high so that the output on the latch is active and evabled all the time.



# Am8T26

## Schottky Three-State Quad Bus Driver/Receiver

### Distinctive Characteristics

- Advanced Schottky technology
- 40mA driver sink current
- Three-state outputs on driver and receiver
- PNP inputs
- 20ns max. driver propagation delay
- 18ns max. receiver propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

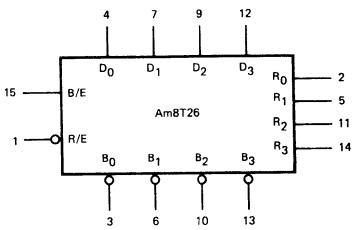
### FUNCTIONAL DESCRIPTION

The Am8T26 is a high speed bus transceiver consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

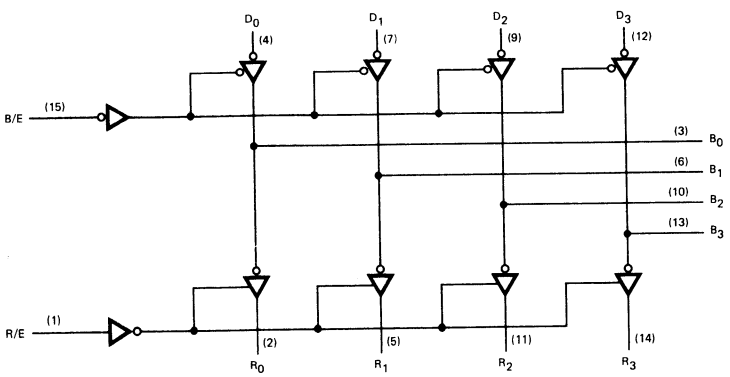
A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

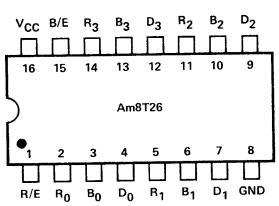
### LOGIC DIAGRAM




### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +75°C | N8T26B |
| Hermetic DIP | 0°C to +75°C | N8T26F |
| Dice | 0°C to +75°C | AM8T26XC |
| Hermetic DIP | −55°C to +125°C | S8T26F |
| Dice | −55°C to +125°C | AM8T26XM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

4

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

N8T26 $T_A$ = 0°C to +75°C
S8T26 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Driver Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −10mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.6 | 3.1 | | Volts |
| $V_{OL}$ | Driver Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 40mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −2mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.6 | 3.1 | | Volts |
| $V_{OL}$ | Receiver Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = −16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.85 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −5mA | | | | −1.0 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.2 | mA |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.25V | | | | 25 | µA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | Driver | −50 | | −150 | mA |
| | | | Receiver | −30 | | −75 | |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | | | 87 | mA |
| $I_O$ | Bus Leakage Current with Driver Off | $V_{CC}$ = MAX., $V_{BUS}$ = 2.6V<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 100 | µA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## Switching Characteristics ($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Driver Input to Bus | Figure 1 | | 16 | 20 | ns |
| $t_{PHL}$ | | | | 16 | 20 | |
| $t_{PLH}$ | Bus to Receiver Output | Figure 2 | | 13 | 18 | ns |
| $t_{PHL}$ | | | | 6 | 10 | |
| $t_{ZL}$ | Driver Enable to Bus | Figure 3 | | 29 | 38 | ns |
| $t_{LZ}$ | | | | 35 | 43 | |
| $t_{ZL}$ | Receiver Enable to Receiver Output | Figure 4 | | 20 | 30 | ns |
| $t_{LZ}$ | | | | 10 | 17 | |

## DEFINITION OF FUNCTIONAL TERMS

**$D_0, D_1, D_2, D_3$** The four driver inputs.

**$B_0, B_1, B_2, B_3$** The four driver outputs and receiver inputs (data is inverted).

**$R_0, R_1, R_2, R_3$** The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

**B/E** Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

**R/E** Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | LOW Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| R/E | 1 | 1/8 | – | – |
| $R_0$ | 2 | – | 50 | 10 |
| $B_0$ | 3 | 1/16 | 250 | 25 |
| $D_0$ | 4 | 1/8 | – | – |
| $R_1$ | 5 | – | 50 | 10 |
| $B_1$ | 6 | 1/16 | 250 | 25 |
| $D_1$ | 7 | 1/8 | – | – |
| GND | 8 | – | – | – |
| $D_2$ | 9 | 1/8 | – | – |
| $B_2$ | 10 | 1/16 | 250 | 25 |
| $R_2$ | 11 | – | 50 | 10 |
| $D_3$ | 12 | 1/8 | – | – |
| $B_3$ | 13 | 1/16 | 250 | 25 |
| $R_3$ | 14 | – | 50 | 10 |
| B/E | 15 | 1/8 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A TTL Unit Load is defined as –1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

## DRIVER FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| B/E | $D_i$ | $B_i$ |
| L | X | Z |
| H | L | H |
| H | H | L |

L = LOW
H = HIGH
i = 0, 1, 2, or 3

X = Don't Care
Z = High Impedance

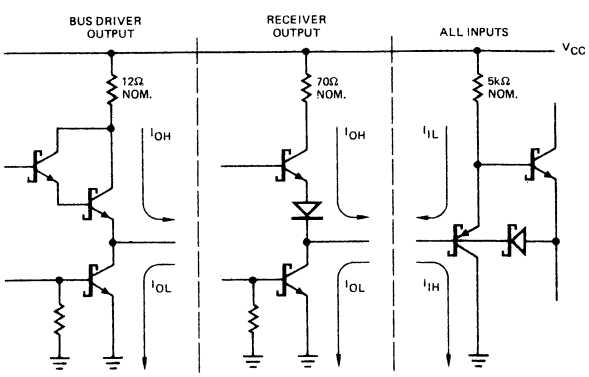
## RECEIVER FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| R/E | $B_i$ | $R_i$ |
| H | X | Z |
| L | L | H |
| L | H | L |

L = LOW
H = HIGH
i = 0, 1, 2, or 3

X = Don't Care
Z = High Impedance

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

# AC TEST CIRCUITS AND WAVEFORMS

## PROPAGATION DELAY (Data In to Bus)

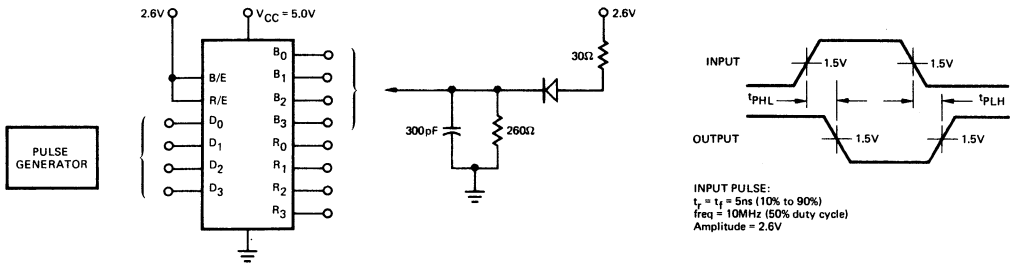



Figure 1

## PROPAGATION DELAY (Bus to Receiver Out)

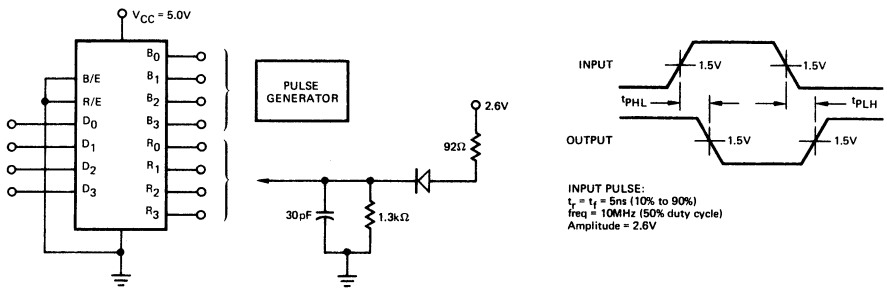



Figure 2

## PROPAGATION DELAY (Bus Enable to Bus Output)

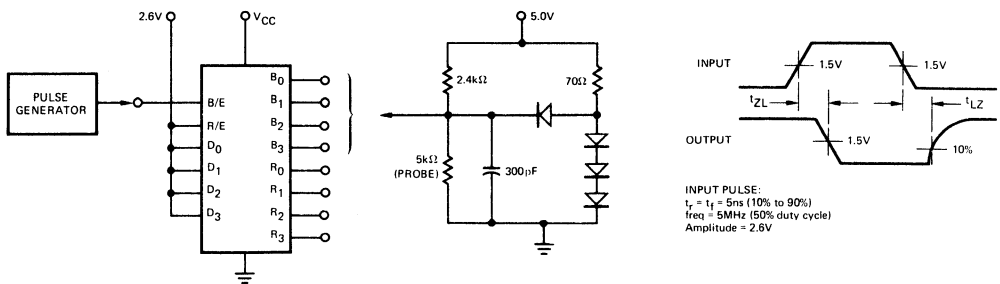



Figure 3

## PROPAGATION DELAY (Receive Enable to Receive Output)

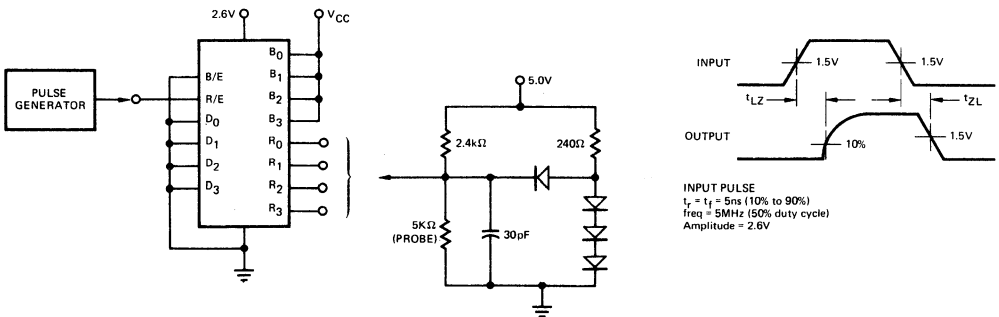
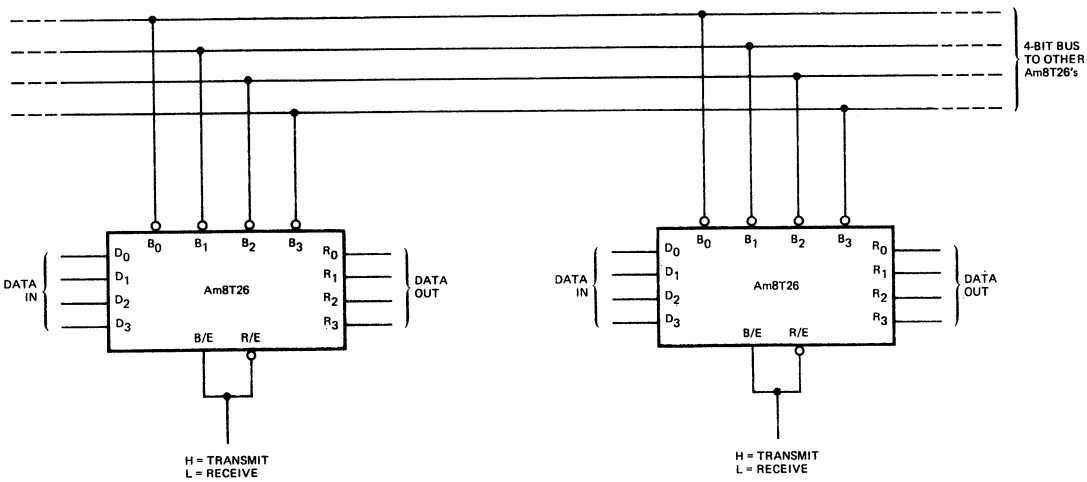
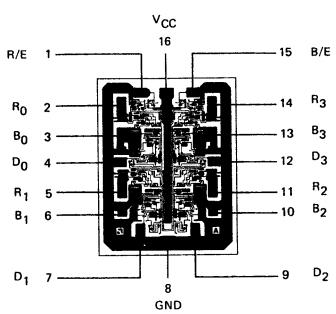



Figure 4

## APPLICATION




## Metallization and Pad Layout




DIE SIZE 0.063" X 0.082"

# Am8T26A·Am8T28

## Schottky Three-State Quad Bus Driver/Receiver

### Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- Three-state outputs on driver and reciever
- PNP inputs
- Am8T26A has inverting outputs
- Am8T28 has non-inverting outputs
- Driver propagation delay — 14ns max. for 8T26A; 17ns max. for 8T28
- Receiver propagation delay — 14ns max. for 8T26A; 17ns max. for 8T28
- 100% reliability assurance testing in compliance with MIL-STD-883

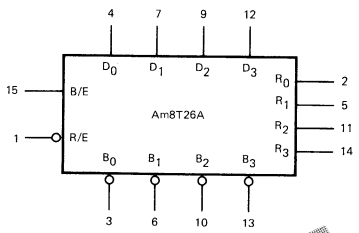
### FUNCTIONAL DESCRIPTION

The Am8T26A/Am8T28 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable (R/E) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

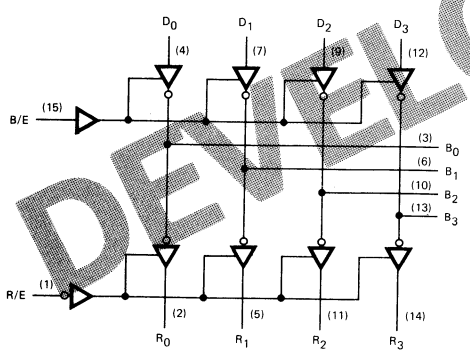
### LOGIC SYMBOL



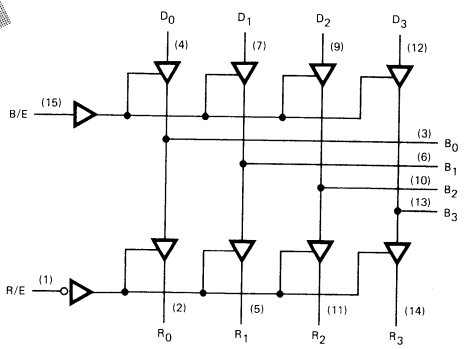

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

**Am8T26A**
**Inverting Output (Three-State)**



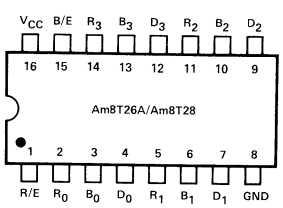

**Am8T28**
**Non-Inverting Output (Three-State)**




### ORDERING INFORMATION

| Package Type | Temperature Range | Am8T26A Order Number | Am8T28 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +75°C | N8T26AB | N8T28B |
| Hermetic DIP | 0°C to +75°C | N8T26AF | N8T28F |
| Dice | 0°C to +75°C | AM8T26AXC | AM8T28XC |
| Hermetic DIP | −55°C to +125°C | S8T26AF | S8T28F |
| Dice | −55°C to +125°C | AM8T26AXM | AM8T28XM |

### CONNECTION DIAGRAM
**(Top View)**




Note: Pin 1 is marked for orientation.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs (Receiver) | 30mA |
| DC Output Current, Into Outputs (BUS) | 80mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

N8T26A, N8T28 $T_A$ = 0°C to +75°C (COM'L) MIN. = 4.75 V MAX. = 5.25 V

S8T26A, S8T28 $T_A$ = −55°C to +125°C (MIL) MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 1) | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|
| **Driver** | | | | | | |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0.4 V | | | −200 | μA |
| $I_{IL}$ | Low Level Input Current (Disabled) | $V_{IN}$ = 0.4 V | | | −25 | μA |
| $I_{IH}$ | High Level Input Current ($D_{IN}$, $D_E$) | $V_{IN}$ = $V_{CC}$ MAX. | | | 25 | μA |
| $V_{OL}$ | Low Level Output Voltage | $I_{OUT}$ = 48 mA (Note 5) | | | 0.5 | Volts |
| $V_{OH}$ | High Level Output Voltage | $I_{OUT}$ = −10 mA, $V_{CC}$ = $V_{CC}$ MIN. (Note 6) | 2.4 | | | Volts |
| $I_{OS}$ | Short Circuit Output Current | $V_{OUT}$ = 0 V, $V_{CC}$ = $V_{CC}$ MAX. (Note 4) | −50 | | −150 | mA |
| **Receiver** | | | | | | |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0.4 V | | | −200 | μA |
| $I_{IH}$ | High Level Input Current ($R_E$) | $V_{IN}$ = $V_{CC}$ MAX. | | | 25 | μA |
| $V_{OL}$ | Low Level Output Voltage | $I_{OUT}$ = 20 mA (Note 5) | | | 0.5 | Volts |
| $V_{OH}$ | High Level Output Voltage | $I_{OUT}$ = −100 μA, $V_{CC}$ = 5.0 V | 3.5 | | | Volts |
| | | $I_{OUT}$ = −2.0 mA (Note 6) | 2.4 | | | |
| $I_{OS}$ | Short Circuit Output Current | $V_{OUT}$ = 0 V, $V_{CC}$ = $V_{CC}$ MAX. | −30 | | −75 | mA |
| **Both Driver and Receiver** | | | | | | |
| $V_{TL}$ | Low Level Input Threshold Voltage | | 0.85 | | | Volts |
| $V_{TH}$ | High Level Input Threshold Voltage | | | | 2.0 | Volts |
| $I_O$ | Low Level Output Off Leakage Current | $V_{OUT}$ = 0.5 V | | | −100 | μA |
| | High Level Output Off Leakage Current | $V_{OUT}$ = 2.4 V | | | 100 | μA |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −12 mA | | | −1.0 | Volts |
| $P_{WR}$/$I_{CC}$ | Power/Current Consumption Am8T26A | $V_{CC}$ = $V_{CC}$ MAX. | | | 457/87 | mW/mA |
| | Power/Current Consumption Am8T28 | $V_{CC}$ = $V_{CC}$ MAX. | | | 578/110 | mW/mA |

## Switching Characteristics ($T_A$ = +25°C, $V_{CC}$ = 5.0 V)

| Parameters | Description | Test Conditions | Am8T26A Min. | Am8T26A Typ. | Am8T26A Max. | Am8T28 Min. | Am8T28 Typ. | Am8T28 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Driver Input to Bus | Figure 1 | | 10 | 14 | | 13 | 17 | ns |
| $t_{PHL}$ | | | | 10 | 14 | | 13 | 17 | |
| $t_{PLH}$ | Bus to Receiver Output | Figure 2 | | 9.0 | 14 | | 12 | 17 | ns |
| $t_{PHL}$ | | | | 6.0 | 14 | | 9.0 | 17 | |
| $t_{ZL}$ | Driver Enable to Bus | Figure 3 | | 19 | 25 | | 21 | 28 | ns |
| $t_{LZ}$ | | | | 15 | 20 | | 18 | 23 | |
| $t_{ZL}$ | Receiver Enable to Receiver Output | Figure 4 | | 15 | 20 | | 18 | 23 | ns |
| $t_{LZ}$ | | | | 10 | 15 | | 13 | 18 | |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to $V_{CC}$.
6. Measurements apply to each output and the associated data input independently.

## DEFINITION OF FUNCTIONAL TERMS

**$D_0, D_1, D_2, D_3$** The four driver inputs.

**$B_0, B_1, B_2, B_3$** The four driver outputs and receiver inputs (data is inverted).

**$R_0, R_1, R_2, R_3$** The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

**B/E** Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

**R/E** Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | LOW Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| R/E | 1 | 1/8 | – | – |
| $R_0$ | 2 | – | 50 | 10 |
| $B_0$ | 3 | 1/16 | 250 | 25 |
| $D_0$ | 4 | 1/8 | – | – |
| $R_1$ | 5 | – | 50 | 10 |
| $B_1$ | 6 | 1/16 | 250 | 25 |
| $D_1$ | 7 | 1/8 | – | – |
| GND | 8 | – | – | – |
| $D_2$ | 9 | 1/8 | – | – |
| $B_2$ | 10 | 1/16 | 250 | 25 |
| $R_2$ | 11 | – | 50 | 10 |
| $D_3$ | 12 | 1/8 | – | – |
| $B_3$ | 13 | 1/16 | 250 | 25 |
| $R_3$ | 14 | – | 50 | 10 |
| B/E | 15 | 1/8 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

## DRIVER FUNCTION TABLE

| INPUTS | | Am8T26A OUTPUT | Am8T28 OUTPUT |
|---|---|---|---|
| B/E | $D_i$ | $B_i$ | $B_i$ |
| L | X | Z | Z |
| H | L | H | L |
| H | H | L | H |

L = LOW
H = HIGH
i = 0, 1, 2, or 3

X = Don't Care
Z = High Impedance

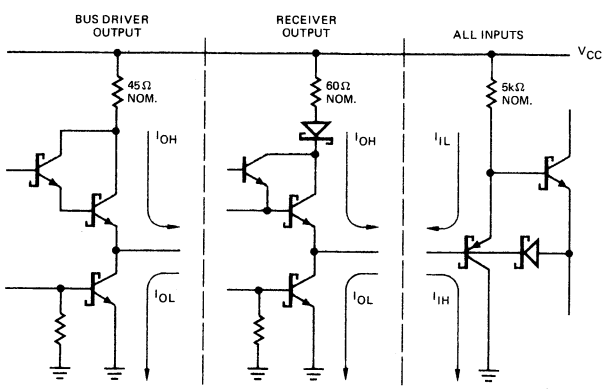
## RECEIVER FUNCTION TABLE

| INPUTS | | Am8T26A OUTPUT | Am8T28 OUTPUT |
|---|---|---|---|
| R/E | $B_i$ | $R_i$ | $R_i$ |
| H | X | Z | Z |
| L | L | H | L |
| L | H | L | H |

L = LOW
H = HIGH
i = 0, 1, 2, or 3

X = Don't Care
Z = High Impedance

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

# AC TEST CIRCUITS AND WAVEFORMS

## PROPAGATION DELAY (Data In to Bus)

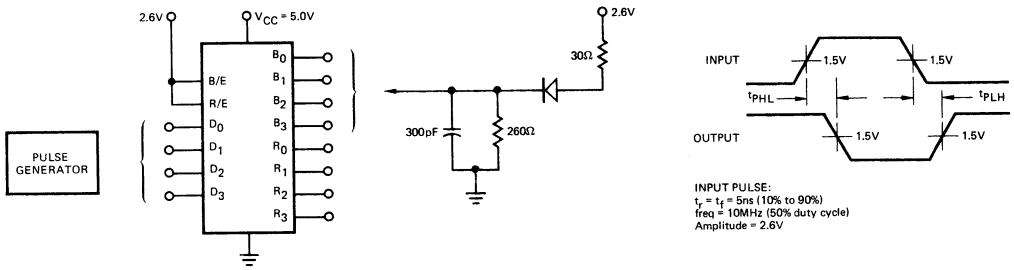



Figure 1

## PROPAGATION DELAY (Bus to Receiver Out)

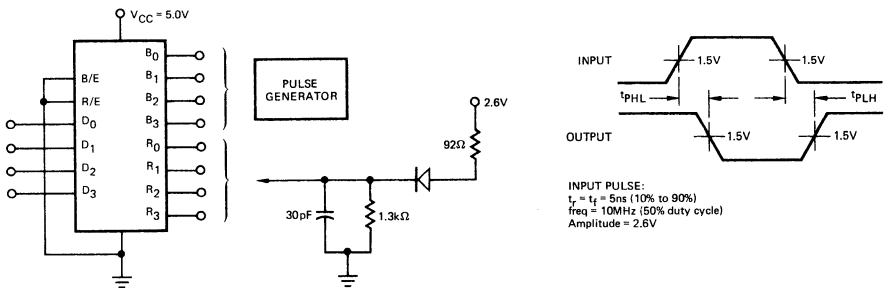



Figure 2

## PROPAGATION DELAY (Bus Enable to Bus Output)

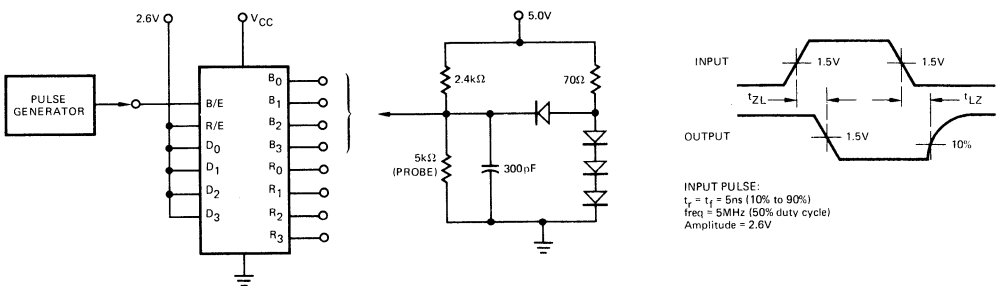



Figure 3

## PROPAGATION DELAY (Receive Enable to Receive Output)

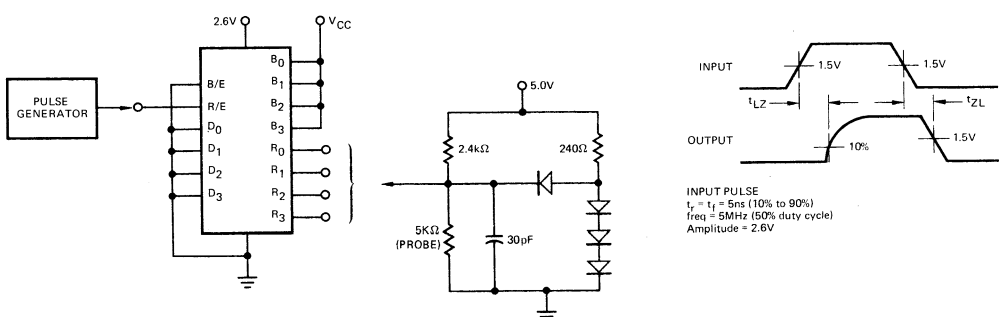



Figure 4

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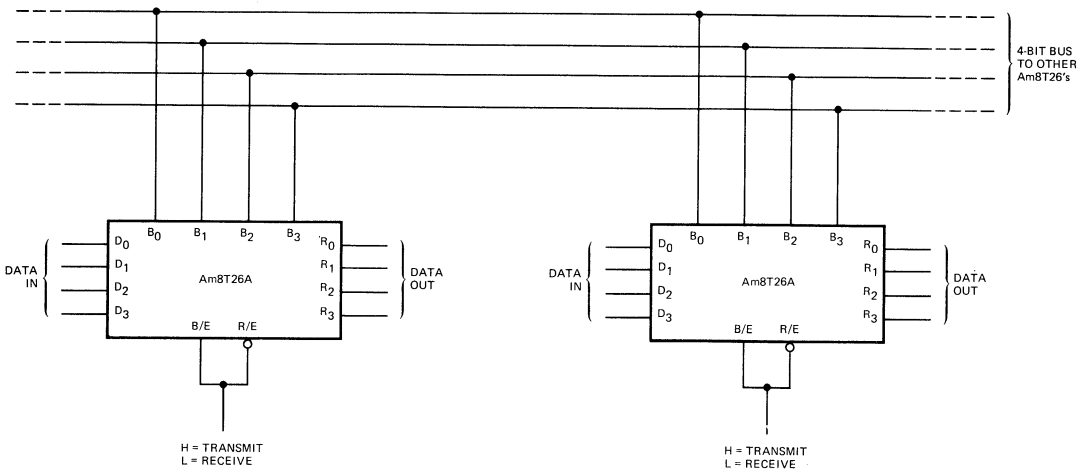
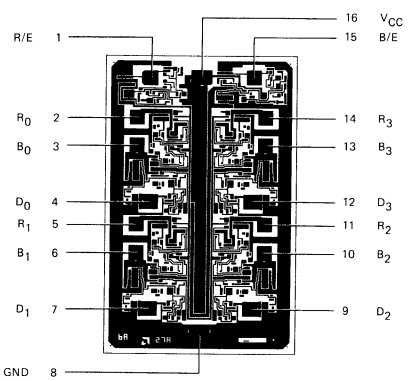
## APPLICATION



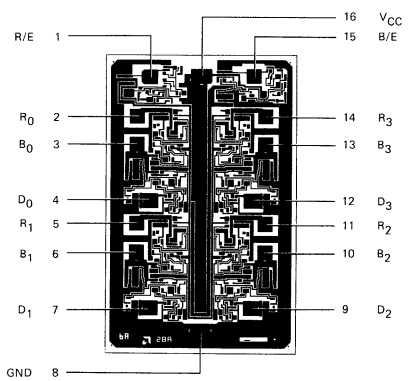

## Metallization and Pad Layouts

### Am8T26A




DIE SIZE 0.058" X 0.091"

### Am8T28




DIE SIZE 0.058" X 0.091"

# Am82S62

## Nine-Input Parity Checker/Generator

### Distinctive Characteristics

- ODD/EVEN parity outputs
- Inhibit input to disable both outputs
- High-speed expansion input – $P_9$
- PNP inputs
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

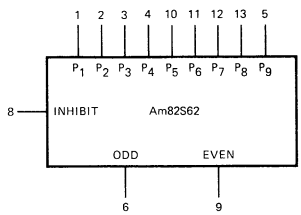
### FUNCTIONAL DESCRIPTION

The Am82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

The Am82S62 features one special high-speed input ($P_9$) to facilitate expansion. The propagation delay to the outputs through this path is considerably reduced when compared to the $P_1$ through $P_8$ paths. This short delay path allows parity checkers/generators of larger size than 9-bits to be built with a minimum of additional delay.

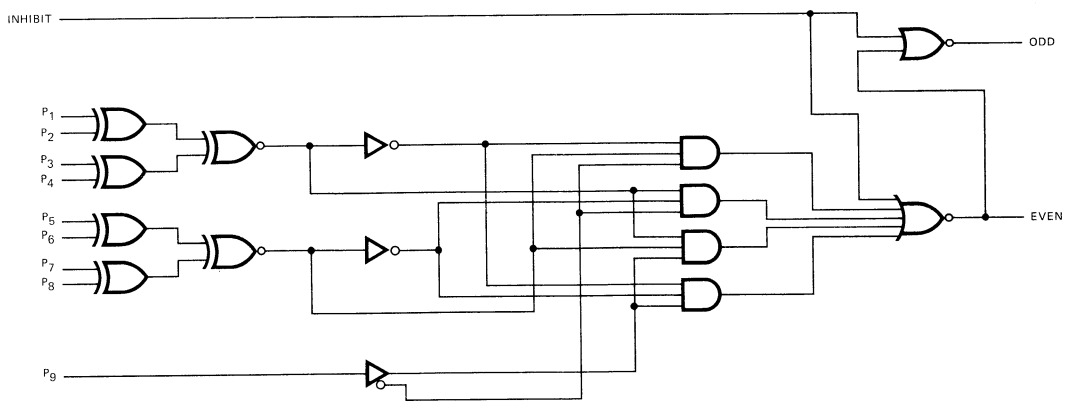
The device is built using advanced Schottky technology and incorporates PNP input transistors to reduce input loading to 0.4 STTL unit loads. The EVEN output is one gate propagation delay time shorter than the ODD output.

### LOGIC SYMBOL




$V_{CC}$ = Pin 14
GND = Pin 7

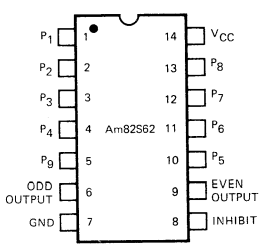
### LOGIC DIAGRAM




### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +75°C | N82S62A |
| Hermetic DIP | 0°C to +75°C | N82S62F |
| Dice | 0°C to +75°C | N82S62X |
| Hermetic DIP | −55°C to +125°C | S82S62F |
| Dice | −55°C to +125°C | S82S62X |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

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## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

N82S62 $T_A$ = 0°C to +75°C
S82S62 $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | S82 | 2.5 | | | Volts |
| | | | N82 | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | P9 | | | −0.4 | mA |
| | | | Others | | | −0.8 | |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 4.5V | | | | 10 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | | 67 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. $P_1$ through $P_9$ grounded; inhibit at 4.5V; outputs open.

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $P_1$ through $P_8$ to Even Output | $V_{CC}$ = 5.0V, $R_L$ = 280Ω, $C_L$ = 15 pF | | | 23 | ns |
| $t_{PHL}$ | | | | | | |
| $t_{PLH}$ | $P_1$ through $P_8$ to Odd Output | | | | 28 | ns |
| $t_{PHL}$ | | | | | | |
| $t_{PLH}$ | $P_9$ to Even Output | | | | 12 | ns |
| $t_{PHL}$ | | | | | | |
| $t_{PLH}$ | $P_9$ to Odd Output | | | | 18 | ns |
| $t_{PHL}$ | | | | | | |
| $t_{PLH}$ | Inhibit to Even Output | | | | 9 | ns |
| $t_{PHL}$ | | | | | | |
| $t_{PLH}$ | Inhibit to Odd Output | | | | 9 | ns |
| $t_{PHL}$ | | | | | | |

## TRUTH TABLE

| INHIBIT | NUMBER OF P INPUTS | | OUTPUT | |
|---|---|---|---|---|
| | LOW | HIGH | ODD | EVEN |
| L | 0 | 9 | H | L |
| L | 1 | 8 | L | H |
| L | 2 | 7 | H | L |
| L | 3 | 6 | L | H |
| L | 4 | 5 | H | L |
| L | 5 | 4 | L | H |
| L | 6 | 3 | H | L |
| L | 7 | 2 | L | H |
| L | 8 | 1 | H | L |
| L | 9 | 0 | L | H |
| H | X | X | L | L |

H = HIGH
L = LOW
X = Don't Care

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $P_1$ | 1 | 0.4 | – | – |
| $P_2$ | 2 | 0.4 | – | – |
| $P_3$ | 3 | 0.4 | – | – |
| $P_4$ | 4 | 0.4 | – | – |
| $P_9$ | 5 | 0.2 | – | – |
| ODD | 6 | – | 20 | 10 |
| GND | 7 | – | – | – |
| INHIBIT | 8 | 0.4 | – | – |
| EVEN | 9 | – | 20 | 10 |
| $P_5$ | 10 | 0.4 | – | – |
| $P_6$ | 11 | 0.4 | – | – |
| $P_7$ | 12 | 0.4 | – | – |
| $P_8$ | 13 | 0.4 | – | – |
| $V_{CC}$ | 14 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## DEFINITION OF FUNCTIONAL TERMS

**$P_1$ through $P_9$** The nine inputs to the parity tree.

**INHIBIT** A HIGH on the inhibit input forces both the odd output and even output LOW regardless of the P inputs. When the inhibit is LOW, the odd and even outputs will always be of opposite phase.

**ODD** The odd parity output of the device. When an odd number of P inputs are at a HIGH level, the odd output will be HIGH.

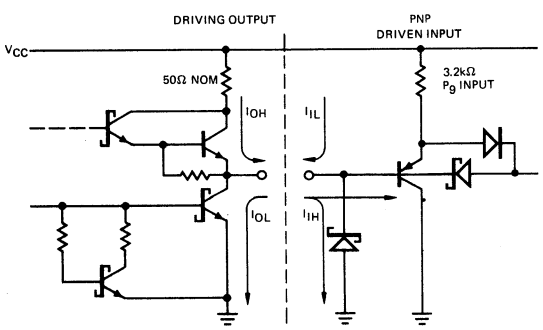
**EVEN** The even parity output of the device. When an even number of P inputs are at a HIGH level, the even output will be HIGH.

## LOGIC EQUATIONS

ODD Output = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

EVEN Output = $\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

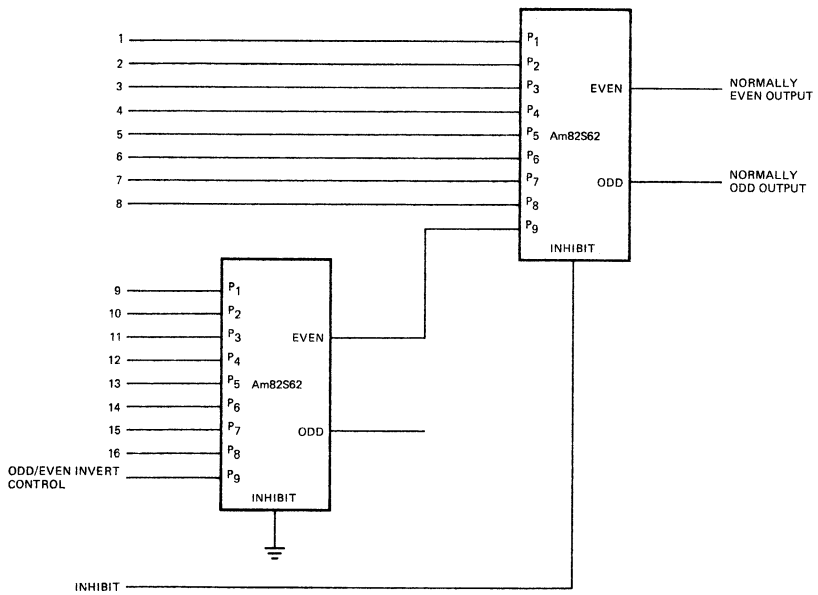



Note: Actual current flow direction shown.

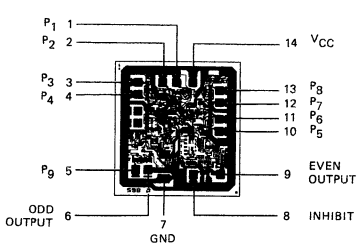
4

## APPLICATION

### 16-BIT PARITY GENERATOR WITH INVERT CONTROL




### Metallization and Pad Layout




DIE SIZE 0.067" X 0.072"

# Am73/8304B

## Octal Three-State Bidirectional Transceiver

### DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- Three-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC}-1.15V$ $V_{OH}$ interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

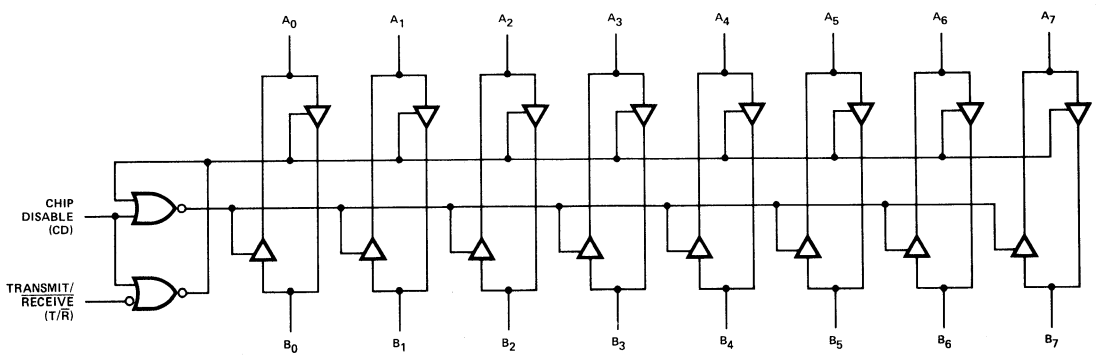
### GENERAL DESCRIPTION

The Am73/8304Bs are 8-bit three-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

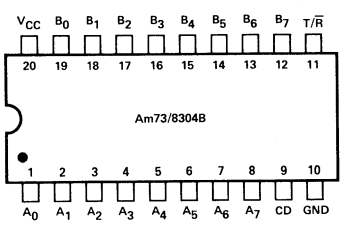
One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a three-state condition.

The output high voltage ($V_{OH}$) is specified at $V_{CC}-1.15V$ minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

### LOGIC DIAGRAM

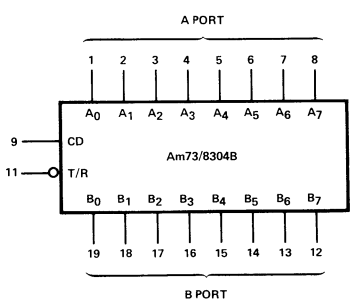



### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Supply Voltage | 7.0V |
| Input Voltage | 5.5V |
| Output Voltage | 5.5V |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am7304B $T_A$ = −55°C to +125°C $V_{CC}$ MIN = 4.5V $V_{CC}$ MAX = 5.5V
Am8304B $T_A$ = 0°C to +70°C $V_{CC}$ MIN = 4.75V $V_{CC}$ MAX = 5.25V

## DC ELECTRICAL CHARACTERISTICS over operating temperature range

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| | | **A PORT ($A_0$-$A_7$)** | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | CD = 0.8V, T/$\overline{R}$ = 2.0V | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | CD = 0.8V, T/$\overline{R}$ = 2.0V | Am83040B | | | 0.8 | Volts |
| | | | Am7304B | | | 0.7 | |
| $V_{OH}$ | Logical "1" Output Voltage | CD = 0.8V, T/$\overline{R}$ = 0.8V | $I_{OH}$ = −0.4mA | $V_{CC}$−1.15 | $V_{CC}$−0.7 | | Volts |
| | | | $I_{OH}$ = −3.0mA | 2.7 | 3.95 | | |
| $V_{OL}$ | Logical "0" Output Voltage | CD = 0.8V, T/$\overline{R}$ = 0.8V | $I_{OL}$ = 8mA | | 0.3 | 0.4 | Volts |
| | | | Am8304B, $I_{OL}$ = 16mA | | 0.35 | 0.50 | |
| $I_{OS}$ | Output Short Circuit Current | CD = 0.8V, T/$\overline{R}$ = 0.8V, $V_O$ = 0V, $V_{CC}$ = MAX., Note 2 | | −10 | −38 | −75 | mA |
| $I_{IH}$ | Logical "1" Input Current | CD = 0.8V, T/$\overline{R}$ = 2.0V, $V_I$ = 2.7V | | | 0.1 | 80 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | CD = 2.0V, $V_{CC}$ = MAX., $V_I$ = $V_{CC}$ MAX. | | | | 1 | mA |
| $I_{IL}$ | Logical "0" Input Current | CD = 0.8V, T/$\overline{R}$ = 2.0V, $V_I$ = 0.4V | | | −70 | −200 | μA |
| $V_C$ | Input Clamp Voltage | CD = 2.0V, $I_{IN}$ = −12mA | | | −0.7 | −1.5 | Volts |
| $I_{OD}$ | Output/Input Three-State Current | CD = 2.0V | $V_O$ = 0.4V | | | −200 | μA |
| | | | $V_O$ = 4.0V | | | 80 | |
| | | **B PORT ($B_0$-$B_7$)** | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | CD = 0.8V, T/$\overline{R}$ = 0.8V | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | CD = 0.8V, T/$\overline{R}$ = 0.8V | Am8304B | | | 0.8 | Volts |
| | | | Am7304B | | | 0.7 | |
| $V_{OH}$ | Logical "1" Output Voltage | CD = 0.8V, T/$\overline{R}$ = 2.0V | $I_{OH}$ = −0.4mA | $V_{CC}$−1.15 | $V_{CC}$−0.8 | | Volts |
| | | | $I_{OH}$ = −5mA | 2.7 | 3.9 | | |
| | | | $I_{OH}$ = −10mA | 2.4 | 3.6 | | |
| $V_{OL}$ | Logical "0" Output Voltage | CD = 0.8V, T/$\overline{R}$ = 2.0V | $I_{OL}$ = 20mA | | 0.3 | 0.4 | Volts |
| | | | $I_{OL}$ = 48mA | | 0.4 | 0.5 | |
| $I_{OS}$ | Output Short Circuit Current | CD = 0.8V, T/$\overline{R}$ = 2.0V, $V_O$ = 0V, $V_{CC}$ = MAX., Note 2 | | −25 | −50 | −150 | mA |
| $I_{IH}$ | Logical "1" Input Current | CD = 0.8V, T/$\overline{R}$ = 0.8V, $V_I$ = 2.7V | | | 0.1 | 80 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | CD = 2.0V, $V_{CC}$ = MAX., $V_I$ = $V_{CC}$ MAX. | | | | 1 | mA |
| $I_{IL}$ | Logical "0" Input Current | CD = 0.8V, T/$\overline{R}$ = 0.8V, $V_I$ = 0.4V | | | −70 | −200 | μA |
| $V_C$ | Input Clamp Voltage | CD = 2.0V, $I_{IN}$ = −12mA | | | −0.7 | −1.5 | Volts |
| $I_{OD}$ | Output/Input Three-State Current | CD = 2.0V | $V_O$ = 0.4V | | | −200 | μA |
| | | | $V_O$ = 4.0V | | | 200 | |
| | | **CONTROL INPUTS CD, T/$\overline{R}$** | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | | | | | 0.8 | Volts |
| $I_{IH}$ | Logical "1" Input Current | $V_I$ = 2.7V | | | 0.5 | 20 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = MAX., $V_I$ = $V_{CC}$ MAX. | | | | 1.0 | mA |
| $I_{IL}$ | Logical "0" Input Current | $V_I$ = 0.4V | T/$\overline{R}$ | | −0.1 | −.25 | mA |
| | | | CD | | −0.25 | −.5 | |
| $V_C$ | Input Clamp Voltage | $I_{IN}$ = −12mA | | | −0.8 | −1.5 | Volts |
| | | **POWER SUPPLY CURRENT** | | | | | |
| $I_{CC}$ | Power Supply Current | CD = 2.0V, $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | 60 | 100 | mA |
| | | CD = $V_{INA}$ = 0.4V, T/$\overline{R}$ = 2V, $V_{CC}$ = MAX. | | | 80 | 130 | |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V, $T_A$ = 25°C)

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | | 14 | 18 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | | 13 | 18 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to Three-State from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | | 11 | 15 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to Three-State from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | | 8 | 15 | ns |
| $t_{PZLA}$ | Propagation Delay from Three-State to a Logical "0" from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | | 27 | 35 | ns |
| $t_{PZHA}$ | Propagation Delay from Three-State to a Logical "1" from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | | 19 | 25 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | | 18 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | | 11 | 18 | |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | | 16 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | | 11 | 18 | |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to Three-State from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | | 13 | 18 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to Three-State from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | | 8 | 15 | ns |
| $t_{PZLB}$ | Propagation Delay from Three-State to a Logical "0" from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | | 32 | 40 | ns |
| | | $S_3$ = 1, $R_5$ = 667Ω, $C_4$ = 45pF | | 16 | 22 | |
| $t_{PZHB}$ | Propagation Delay from Three-State to a Logical "1" from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | | 26 | 35 | ns |
| | | $S_3$ = 0, $R_5$ = 667Ω, $C_4$ = 45pF | | 14 | 22 | |
| **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | | | |
| $t_{PHZR}$ | Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 300pF<br>$S_2$ = 0, $R_3$ = 1k, $C_2$ = 15pF | | 7 | 12 | ns |
| $t_{PLZR}$ | Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 1k, $C_3$ = 300pF<br>$S_2$ = 1, $R_3$ = 1k, $C_2$ = 15pF | | 10 | 14 | ns |
| $t_{PHZT}$ | Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 1k, $C_3$ = 15pF<br>$S_2$ = 1, $R_3$ = 5k, $C_2$ = 30pF | | 16 | 22 | ns |
| $t_{PLZT}$ | Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 1k, $C_3$ = 15pF<br>$S_2$ = 0, $R_3$ = 1k, $C_2$ = 30pF | | 17 | 22 | ns |
| $t_{PRL}$ | Propagation Delay from Transmit Mode to a Logical "0", T/$\overline{R}$ to A Port | $t_{PRL} = t_{PHZT} + t_{PDHLA}$ | | 25 | 40 | ns |
| $t_{PRH}$ | Propagation Delay from Transmit Mode to a Logical "1", T/$\overline{R}$ to A Port | $t_{PRH} = t_{PLZT} + t_{PDLHA}$ | | 30 | 40 | ns |
| $t_{PTL}$ | Propagation Delay from Receive Mode to a Logical "0", T/$\overline{R}$ to B Port | $t_{PTL} = t_{PHZR} + t_{PDHLB}$ | | 25 | 35 | ns |
| $t_{PTH}$ | Propagation Delay from Receive Mode to a Logical "1", T/$\overline{R}$ to B Port | $t_{PTH} = t_{PLZR} + t_{PDLHB}$ | | 26 | 35 | ns |

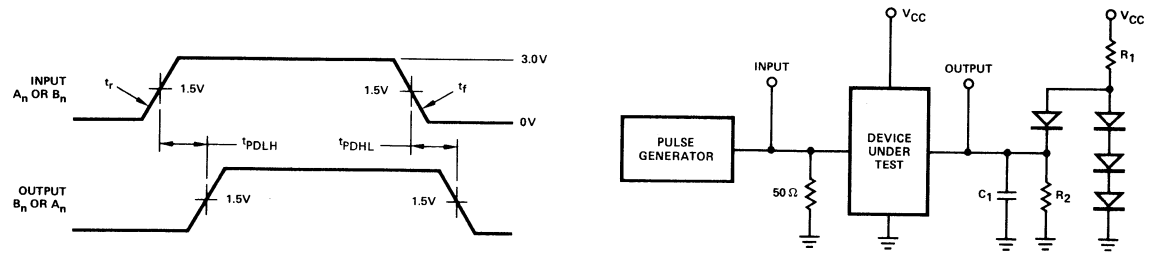
Notes: 1. All typical values given are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Only one output at a time should be shorted.

### FUNCTIONAL TABLE

| Inputs | Conditions | | |
|---|---|---|---|
| Chip Disable | 0 | 0 | 1 |
| Transmit/$\overline{Receive}$ | 0 | 1 | X |
| A Port | Out | In | HI-Z |
| B Port | In | Out | HI-Z |

4

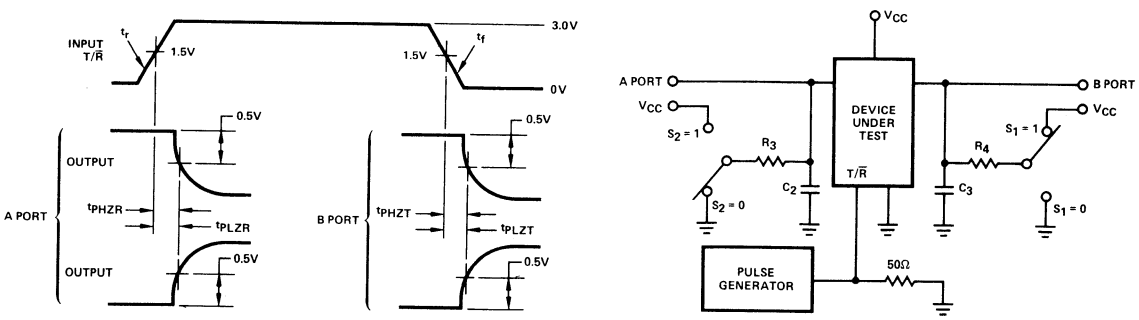
## SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS




$t_r = t_f < 10ns$
10% to 90%

Note: $C_1$ includes test fixture capacitance.

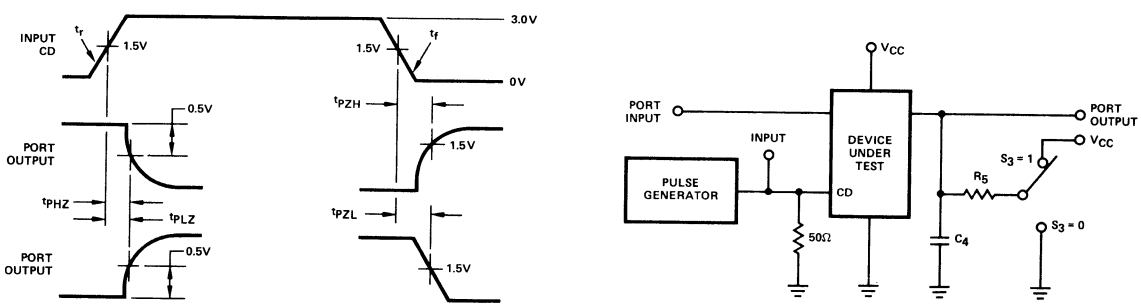
**Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.**




$t_r = t_f < 10ns$
10% to 90%

Note: $C_2$ and $C_3$ include test fixture capacitance.

**Figure 2. Propagation Delay from T/R̄ to A Port or B Port.**




$t_r = t_f < 10ns$
10% to 90%

Note: $C_4$ includes test fixture capacitance.
Port input is in a fixed logical condition.

**Figure 3. Propagation Delay from CD to A Port or B Port.**

# Am93S10 • Am93S16

## BCD Decade/Four-Bit Binary Counters

### Distinctive Characteristics

- Fully synchronous counting
- Fully synchronous parallel loading
- Edge-triggered clock action
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

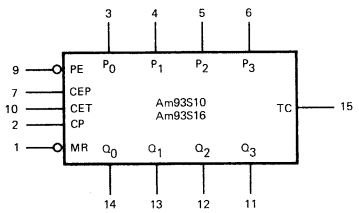
### FUNCTIONAL DESCRIPTION

The Am93S10 and Am93S16 are fully synchronous 4-bit decimal and binary counters. With the parallel enable ($\overline{PE}$) LOW, data on the $P_0$-$P_3$ inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am93S10 and 1111 for the Am93S16) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both counters have an asynchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW independent of all other inputs. The only requirements on the $\overline{PE}$, CEP, CET and $P_0$-$P_3$ inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

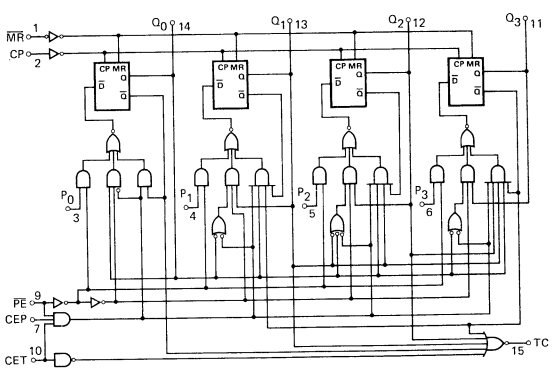
### LOGIC SYMBOL



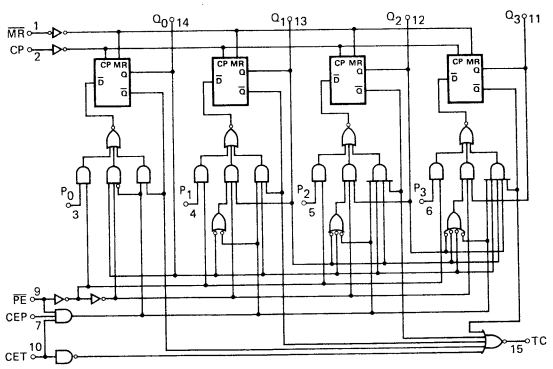

$V_{CC}$ = Pin 16
GND = Pin 8

### LOGIC DIAGRAMS

**Am93S10**



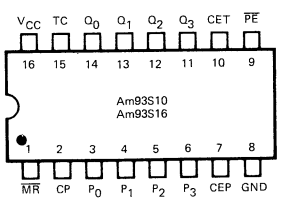

**Am93S16**




### ORDERING INFORMATION

| Package Type | Temperature Range | *Am93S10 Order Number | Am93S16 Order Number |
|---|---|---|---|
| Molded DIP | 0° C to +75° C | 93S10PC | 93S16PC |
| Hermetic DIP | 0° C to +75° C | 93S10DC | 93S16DC |
| Dice | 0° C to +75° C | 93S10XC | 93S16XC |
| Hermetic DIP | −55° C to +125° C | 93S10DM | 93S16DM |
| Hermetic Flat Pak | −55° C to +125° C | 93S10FM | 93S16FM |
| Dice | −55° C to +125° C | 93S10XM | 93S16XM |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

4

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

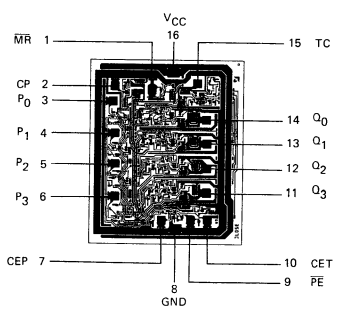
| | | | | |
|---|---|---|---|---|
| Am93S10XC, Am93S16XC | $T_A$ = 0°C to 75°C | $V_{CC}$ = 5.0V ±5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am93S10XM, Am93S16XM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ±10% (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | XM | 2.5 | 3.4 | | Volts |
| | | | XC | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.35 | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | P; MR; CEP | | | −2.0 | mA |
| | | | CET | | | −3.0 | |
| | | | $\overline{PE}$ | | | −4.0 | |
| | | | CP | | | −5.0 | |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | P; $\overline{MR}$; CEP | | | 50 | µA |
| | | | CET | | | 75 | |
| | | | $\overline{PE}$ | | | 100 | |
| | | | CP | | | 125 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX. | | −40 | −65 | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | 82 | 127 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; $\overline{MR}$ = 0V; all other inputs HIGH.

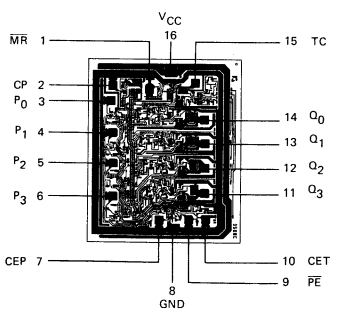
### Metallization and Pad Layouts

**Am93S10**




DIE SIZE 0.078" X 0.096"

**Am93S16**



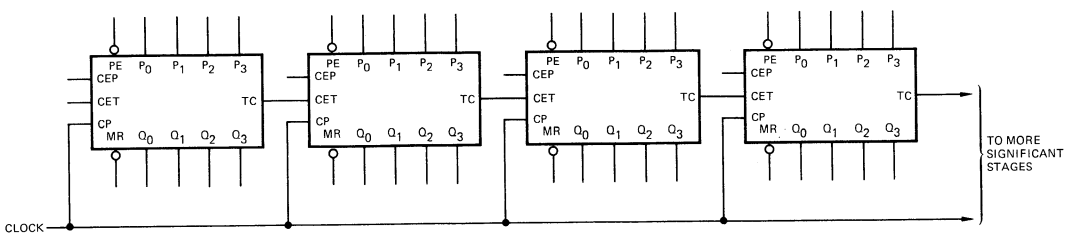

DIE SIZE 0.078" X 0.096"

## SWITCHING CHARACTERISTICS ($T_A$ = +25°)

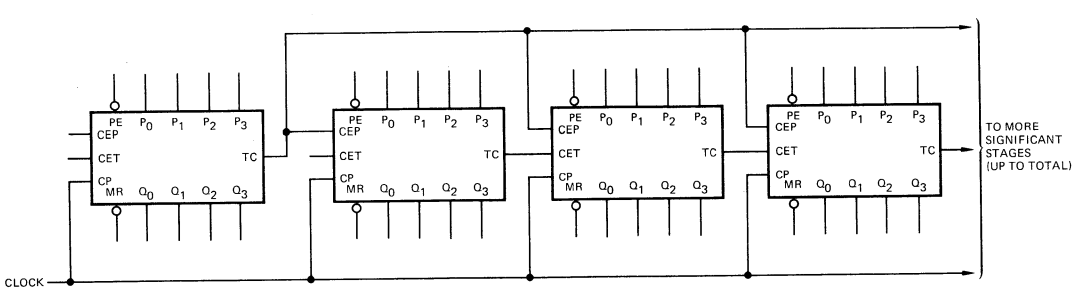
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Count Frequency | $V_{CC}$ = 5.0V, $C_L$ = 15 pF, $R_L$ = 280Ω | 70 | 100 | | MHz |
| $t_{PLH}$ | Clock to Q | | | 6 | 9 | ns |
| $t_{PHL}$ | | | | 8.5 | 13 | |
| $t_{PLH}$ | Clock to TC | | | 12 | 18 | ns |
| $t_{PHL}$ | | | | 8 | 12 | |
| $t_{PLH}$ | CET to TC | | | 6.5 | 10 | ns |
| $t_{PHL}$ | | | | 6.5 | 10 | |
| $t_{PHL}$ | $\overline{MR}$ to Q | | | 14 | 20 | ns |
| $t_s$ | Recovery Time for MR (inactive) | | 6 | | | ns |
| $t_{pw}$ | Master Reset Pulse Width | | 13 | | | ns |
| $t_{pw}$ | Clock Pulse Width HIGH | | 6 | | | ns |
| | Clock Pulse Width LOW | | 10 | | | |
| $t_s$ | Data to Clock | | 8 | | | ns |
| $t_h$ | | | 0 | | | |
| $t_s$ | $\overline{PE}$ to Clock | | 16 | | | ns |
| $t_h$ | | | 0 | | | |
| $t_s$ | CEP or CET to Clock | | 12 | | | ns |
| $t_h$ | | | 0 | | | |

## APPLICATIONS

### SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY




### FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS




4

## DEFINITION OF FUNCTIONAL TERMS

**$\overline{PE}$** Parallel Enable. When $\overline{PE}$ is LOW, the parallel inputs, $P_0$ through $P_3$, are enabled. When $\overline{PE}$ is HIGH, the count function is possible.

**CEP** Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

**CET** Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

**CP** Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

**$\overline{MR}$** Master Reset. When the asynchronous master reset is LOW, the $Q_0$ through $Q_3$ outputs will be LOW regardless of the other inputs.

**$P_0$, $P_1$, $P_2$, $P_3$** The parallel data inputs for the four internal flip-flops.

**$Q_0$, $Q_1$, $Q_2$, $Q_3$** The four parallel outputs from the counter.

**TC** Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am93S10 or CET HIGH and binary 15 on the Am93S16.

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $\overline{MR}$ | 1 | 1 | – | – |
| CP | 2 | 2.5 | – | – |
| $P_0$ | 3 | 1 | – | – |
| $P_1$ | 4 | 1 | – | – |
| $P_2$ | 5 | 1 | – | – |
| $P_3$ | 6 | 1 | – | – |
| CEP | 7 | 1 | – | – |
| GND | 8 | – | – | – |
| $\overline{PE}$ | 9 | 2 | – | – |
| CET | 10 | 1.5 | – | – |
| $Q_3$ | 11 | – | 20 | 10 |
| $Q_2$ | 12 | – | 20 | 10 |
| $Q_1$ | 13 | – | 20 | 10 |
| $Q_0$ | 14 | – | 20 | 10 |
| TC | 15 | – | 20 | 10 |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CP | $\overline{MR}$ | $\overline{PE}$ | CEP | CET | $P_0$ | $P_1$ | $P_2$ | $P_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| X | L | X | X | X | X | X | X | X | L | L | L | L |
| ↑ | H | L | X | X | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ |
| ↑ | H | H | L | L | X | X | X | X | NC | NC | NC | NC |
| ↑ | H | H | L | H | X | X | X | X | NC | NC | NC | NC |
| ↑ | H | H | H | L | X | X | X | X | NC | NC | NC | NC |
| ↑ | H | H | H | H | X | X | X | X | COUNT | | | |

H = HIGH
L = LOW
X = Don't Care

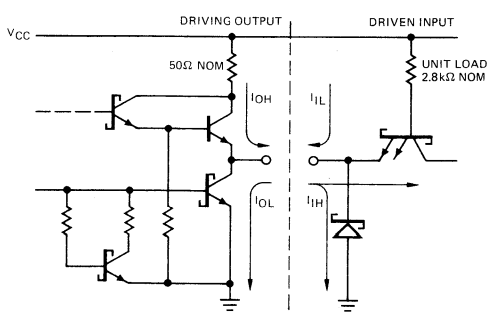
NC = No Change
$D_i$ may be either HIGH or LOW
↑ LOW-to-HIGH Transition

## TERMINAL COUNT (TC) TRUTH TABLE

| Am93S10 | | | | | Am93S16 | | | | | TC |
|---|---|---|---|---|---|---|---|---|---|---|
| CET | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | CET | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | |
| H | H | L | L | H | H | H | H | H | H | H |
| L | X | X | X | X | L | X | X | X | X | L |
| X | L | X | X | X | X | L | X | X | X | L |
| X | X | H | X | X | X | X | L | X | X | L |
| X | X | X | H | X | X | X | X | L | X | L |
| X | X | X | X | L | X | X | X | X | L | L |

H = HIGH
L = LOW
X = Don't Care

## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

# Am93S48

## Twelve-Input Parity Checker/Generator

### Distinctive Characteristics

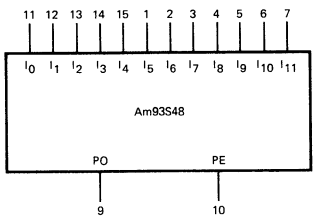
- Generates or checks parity over 12 bits
- Advanced Schottky technology
- Same delay to EVEN and ODD parity outputs
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

The Am93S48 is a high-speed, 12-input parity checker or parity generator. The device is built using advanced Schottky technology and also incorporates PNP input transistors to reduce the input loading to only 0.4 STTL Unit Loads.

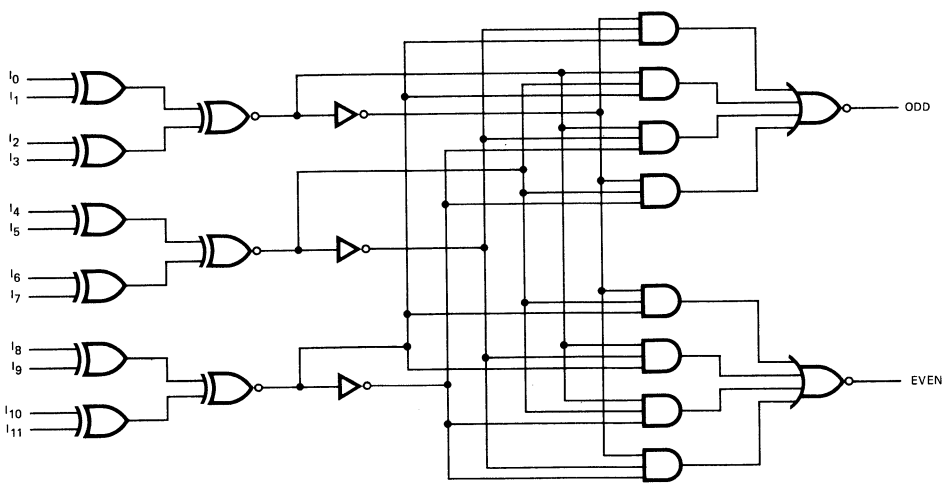
Both an ODD parity output and an EVEN parity output are obtained with the same propagation delay. This is accomplished by using an output structure that looks at the input as three 4-bit parity trees.

### LOGIC SYMBOL




$V_{CC}$ = Pin 16
GND = Pin 8

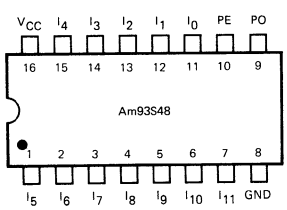
### LOGIC DIAGRAM




### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | 93S48PC |
| Hermetic DIP | 0°C to +70°C | 93S48DC |
| Dice | 0°C to +70°C | 93S48XC |
| Hermetic DIP | −55°C to +125°C | 93S48DM |
| Hermetic Flat Pak | −55°C to +125°C | 93S48FM |
| Dice | −55°C to +125°C | 93S48XM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

4

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5V to +7V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +5.5V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

| | | | | |
|---|---|---|---|---|
| Am93S48XC | $T_A$ = 0°C to +70°C | $V_{CC}$ = 5.0V ±5% (COM'L) | MIN. = 4.75V | MAX. = 5.25V |
| Am93S48XM | $T_A$ = −55°C to +125°C | $V_{CC}$ = 5.0V ±10% (MIL) | MIN. = 4.5V | MAX. = 5.5V |

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −1mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | XC | 2.7 | | | Volts |
| | | | XM | 2.5 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 20mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ (Note 3) | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.5V | | | | −0.8 | mA |
| $I_{IH}$ (Note 3) | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V | | −40 | | −100 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 5) | | | 57 | 80 | mA |

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Both outputs open; all inputs at 4.5V.

## Switching Characteristics ($T_A$ = +25°C)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $I_0$ through $I_{11}$ to Even Output | $V_{CC}$ = 5.0V, $C_L$ = 15 pF, $R_L$ = 280Ω | | 19 | 28 | ns |
| $t_{PHL}$ | | | | 19 | 28 | ns |
| $t_{PLH}$ | $I_0$ through $I_{11}$ to Odd Output | | | 19 | 28 | ns |
| $t_{PHL}$ | | | | 19 | 28 | ns |

## TRUTH TABLE

| NUMBER OF I INPUTS | | OUTPUT | |
|---|---|---|---|
| LOW | HIGH | ODD | EVEN |
| 0 | 12 | L | H |
| 1 | 11 | H | L |
| 2 | 10 | L | H |
| 3 | 9 | H | L |
| 4 | 8 | L | H |
| 5 | 7 | H | L |
| 6 | 6 | L | H |
| 7 | 5 | H | L |
| 8 | 4 | L | H |
| 9 | 3 | H | L |
| 10 | 2 | L | H |
| 11 | 1 | H | L |
| 12 | 0 | L | H |

H = HIGH
L = LOW
X = Don't Care

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $I_5$ | 1 | 0.4 | – | – |
| $I_6$ | 2 | 0.4 | – | – |
| $I_7$ | 3 | 0.4 | – | – |
| $I_8$ | 4 | 0.4 | – | – |
| $I_9$ | 5 | 0.4 | – | – |
| $I_{10}$ | 6 | 0.4 | – | – |
| $I_{11}$ | 7 | 0.4 | – | – |
| GND | 8 | – | – | – |
| PO | 9 | – | 20 | 10 |
| PE | 10 | – | 20 | 10 |
| $I_0$ | 11 | 0.4 | – | – |
| $I_1$ | 12 | 0.4 | – | – |
| $I_2$ | 13 | 0.4 | – | – |
| $I_3$ | 14 | 0.4 | – | – |
| $I_4$ | 15 | 0.4 | – | – |
| $V_{CC}$ | 16 | – | – | – |

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

## DEFINITION OF FUNCTIONAL TERMS

**$I_0$ through $I_{11}$** The twelve inputs to the parity tree.

**ODD** The ODD parity output of the device. When an ODD number of I inputs are at a HIGH level, the ODD output will be HIGH.

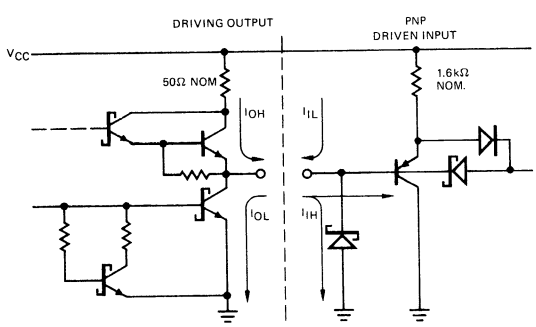
**EVEN** The EVEN parity output of the device. When an EVEN number of I inputs are at a HIGH level, the EVEN output will be HIGH.

## LOGIC EQUATIONS

Odd Output = $I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$

Even Output = $\overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$

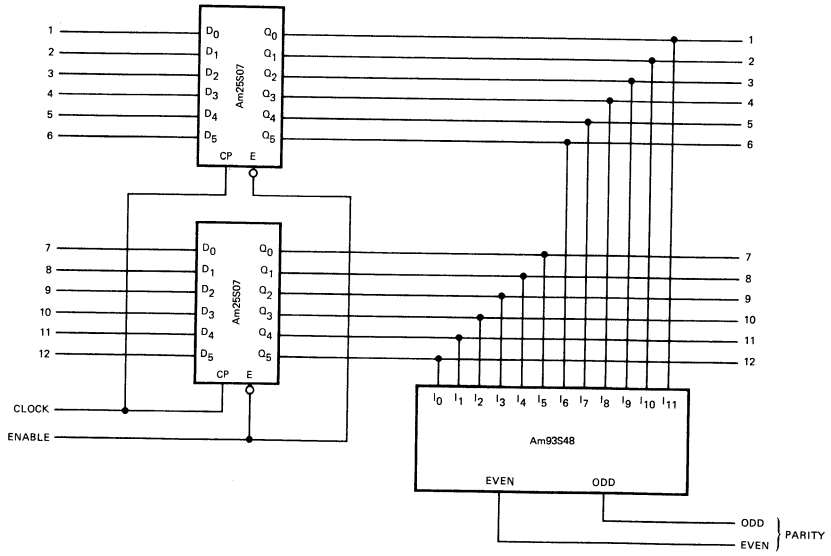
## SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



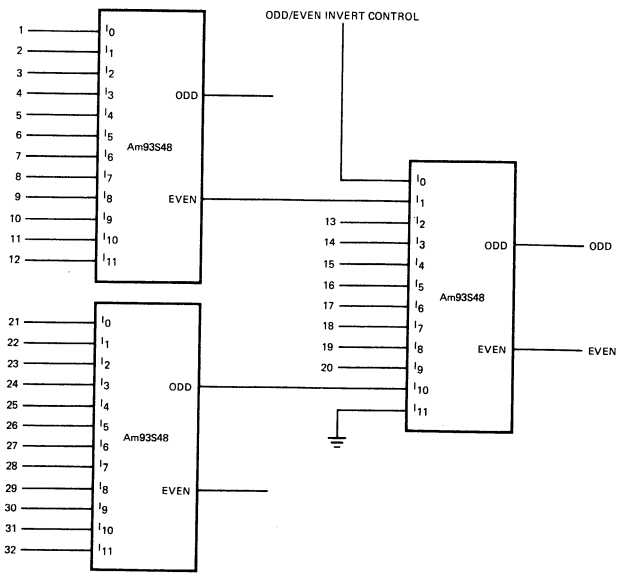

Note: Actual current flow direction shown.

## APPLICATIONS

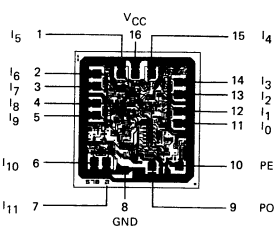
### 12-BIT PARALLEL ODD/EVEN PARITY CHECKER/GENERATOR




### 32-BIT PARITY CHECKER/GENERATOR




### Metallization and Pad Layout




DIE SIZE 0.067" X 0.072"

# Digital Signal Processing Handbook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## TABLE OF CONTENTS

# INTRODUCTION

The significant cost reductions which have been achieved with digital integrated circuits in recent years have allowed digital processing techniques to be applied in many new fields. One of the most important of these is digital signal processing.

Digital arithmetic processors are now used to perform frequency analysis, correlation and filtering functions which, at one time, were the exclusive province of analog systems. Digital signal processors have several obvious advantages over analog approaches. These include precision and programmability as well as insensitivity to temperature, power supply variations, and component aging.

Digital signal processors are similar to general-purpose digital computers except for the need to perform large numbers of multiplications. The first digital signal processors frequently used general-purpose adders programmed to do the multiplication. More recently, integrated circuits such as the Advanced Micro Devices' Am2505 two's complement multiplier were introduced specifically for this function. The Am2505 was quickly accepted as the industry standard device for military applications. It was soon followed by high-speed, Am2505, and low-power, Am25L05, versions. Although these devices significantly reduced the cost and improved the performance of signal processors used for digital filters and Fast Fourier Transform analyzers, digital techiques were still only economically viable for very sophisticated applications.

The development of low-power Schottky technology, which provides the same performance as standard TTL at up to one-fifth the power dissipation, now permits the design of low-cost MSI and LSI devices suitable for use in general commercial digital signal processing systems. Advanced Micro Devices has recently introduced a number of products designed specifically for these applications. They include the Am25LS14 Serial/Parallel Multiplier, Am25LS15 Quad Adder/Subtractor and the Am25LS22 8-Bit Serial/Parallel Register.

This handbook offers a general introduction to digital signal processing techniques. Particular emphasis has been given to the application of low-power Schottky integrated circuits in the design of digital filters.

We hope that this information will aid engineers in implementing digital signal processing methods in cost conscious commercial systems. Typical applications include process control, data compression, data transmission, spectrum analyzers, medical electronics and special purpose instrumentation as well as hardware multiplication and division in high-speed minicomputer designs.

# BASIC DIGITAL FILTER THEORY

By John R. Mick

## INTRODUCTION

Digital filtering applications are rapidly expanding as new developments in technology provide increased packing density in complex integrated circuits. Until recently digital filter processing algorithms have been used primarily in computer simulations, sampled data analysis and data reduction computations. The variety of complex integrated circuits suitable in size, weight, power and cost for real-time processing of video signals by digital techniques is increasing steadily. With the increasingly extensive application of digital processors to many systems, more and more importance is placed on the development of mathematical tools for the analysis and design of sampled data systems. In particular the classical methods of difference equation solutions are available to the designer as well as the "z-transform" calculus solutions. The latter analytical method results in considerable simplification and understanding of the problems associated with sampled-data systems.

This application note presents a brief review of these concepts. A brief introduction to sampling theory is presented and a review of the difference equation as applicable to digital filtering follows. Several digital filter configurations are outlined and a summary of the most useful transforms for designing digital filters is also presented.

### Definition

The term "digital filter" refers to a computational algorithm performed on a sampled input signal resulting in a transformed output signal. The input signal is a sequence of numbers from either an analog-to-digital converter or a direct digital input source. The computational process can correspond to high-pass filtering, low-pass filtering, band-pass filtering, integration, differentiation etc. The output signal is either a direct digital sequence or a regenerated analog signal from a digital-to-analog converter.

### Advantages

Several unique advantages are offered by the digital approach to signal processing. These include:

1. Performance from unit to unit is stable and repeatable.
2. Arbitrarily high precision is achieved that is limited only by the number of bits carried in memory and by the input and output resolution capabilities.
3. No impedance matching problems exist in the digital domain.
4. Critical filter break frequencies can be placed without restriction (influences the precision required).
5. Component value variation problems normally associated with capacitors and resistors due to temperature changes or age are nonexistent.
6. Greater flexibility is achieved since filter response can be changed by varying the proper arithmetic coefficients.
7. The intrinsic possibility of time-sharing major implementation sections exists (adders, subtractors, multipliers etc).
8. Small size results from integrated circuit implementation.
9. Periodic calibration as is required with analog circuits is eliminated.
10. Performance limitations of physical analog components are avoided.

## THE SAMPLING PROCESS

It's convenient to think of the sampling process as an impulse modulation of a continuous input signal. Accordingly if the input signal v(t) is sampled every T seconds, an output signal results denoted $v^*(t)$. This is shown in Figure 1.

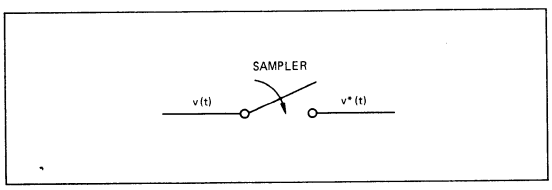



**Figure 1. Sampler Representation.**

The ideal sampler is represented by using the Dirac delta function to express a unit impulse train $\delta(t\text{-}nT)$. This notation represents impulses occurring at each t = nT seconds for n equal to positive integers. The ideal sampler $\delta_T(t)$ for a continuous train of regularly spaced pulses is described for positive time sequences by the following equation:

$$\delta_T(t) = \sum_{n=0}^{\infty} \delta(t-nT) \tag{1}$$

The sampler output signal is written in terms of a continuous input signal and the ideal sampler unit impulse train as

$$v^*(t) = v(t) \sum_{n=0}^{\infty} \delta(t-nT) \tag{2}$$

This equation is rewritten to include the input signal as a time function when t = nT as

$$v^*(t) = \sum_{n=0}^{\infty} v(nT)\,\delta(t-nT) \tag{3}$$

This equation shows that the sampler output is an impulse train with an amplitude equal to the continuous input signal amplitude at the sampling instant.

The Laplace transform of the ideal sampler is the Laplace transform of the Dirac impulse train $\delta_T(t)$ and is given by

$$\mathcal{L}[\delta_T(t)] = \mathcal{L}\left[\sum_{n=0}^{\infty} \delta(t-nT)\right] = \sum_{n=0}^{\infty} e^{-nTs} \tag{4}$$

since the Laplace transform of the unit impulse function $\delta(t-nT)$ is $e^{-nTs}$.

Using equation 4, the Laplace transform of equation 3, the sampler output becomes

$$V^*(s) = \sum_{n=0}^{\infty} v(nT)e^{-nTs} \quad (5)$$

This is very similar to the definition of the continuous Laplace transform

$$V(s) = \int_0^{\infty} v(t)e^{-st}dt \quad (6)$$

except that the integral is replaced by a summation evaluated at the sampling instants $t = nT$ of the unit impulse train.

### Time Domain Sampling

The time domain analysis of the above described sampler is best understood by considering a continuous sinusoidal input signal

$$v(t) = A \sin(wt) \quad (7)$$

Using equation 3, the sampler output for the sinusoidal input is

$$V^*(t) = \sum_{n=0}^{\infty} A \sin(wnT)\ \delta(t-nT) \quad (8)$$

Figure 2 shows the time domain response of a sinusoidal input signal, a sampler, and a sampler output as described by the above equations, where the sampling rate is considerably higher than the continuous input frequency.

Using equation 5, the Laplace transform of equation 8 describing the sampler output for the sinusoidal input is

$$V^*(s) = \sum_{n=0}^{\infty} A \sin(wnT)e^{-nTs} \quad (9)$$

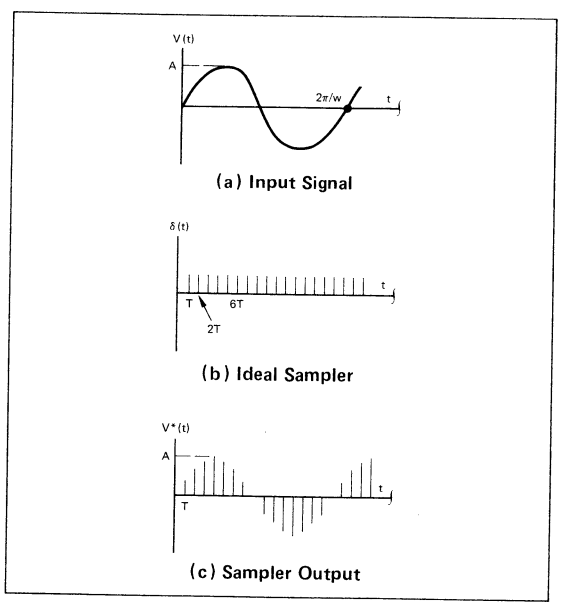



**Figure 2. Time Domain Sampling.**

The time domain analysis gives a useful picture of the sampler characteristics as a function of time; however, the complete picture also requires an analysis of the sampler in the frequency domain.

### Frequency Domain Sampling

To examine the characteristics of the ideal sampler in the frequency domain, the Laplace transform of the ideal sampler as established in equation 4 is expanded as

$$\sum_{n=0}^{\infty} e^{-nTs} = 1+e^{-st}+e^{-2sT}+e^{-3sT}+\ldots \quad (10)$$

The closed form of this geometric series is

$$\sum_{n=0}^{\infty} e^{-nTs} = \frac{1}{1-e^{-sT}} \quad (11)$$

Thus the Laplace transform of the sampler output is given by the convolution of the ideal sampler and the continuous input signal as

$$V^*(s) = V(s)^*\left[\frac{1}{1-e^{-sT}}\right] \quad (12)$$

Since convolution in the s-domain requires contour integration[21], only the result is stated; the sampler output for a continuous input is

$$V^*(s) = \frac{1}{T}\sum_{n=-\infty}^{\infty} V(s+jnw_s) \quad (13)$$

It is important to note that the sampler and its output are periodic with period $jw_s$. This means $V^*(s)$ is equal to $V^*(s+jw_s)$ and is represented in the s-plane by periodic strips along the jw axis. As a result, the sampler causes a periodic single line spectrum in the frequency domain occurring at each integer multiple of the sampling frequency.

Assuming a continuous sinusoidal input signal

$$v(t) = A \sin(w_a t) \quad (14)$$

and a sampler operating at radian frequency $w_s$, the output spectrum is periodic with spurious sidebands located at all multiples of $w_s$. The input spectrum is centered around each of these spurious multiples of the sampling frequency. This is shown in Figure 3.

### The Z-Transform

The z-transform is used to describe a sampled data system in much the same way as the Laplace transform is used to describe a continuous time system. The z-transform of a signal describes the signal at the sampling instant and therefore contains information about the corresponding time function at the sampling instants only. The z-transform is obtained by making the substitution

$$z = e^{sT} \quad (15)$$

or

$$s = \frac{1}{T}\ln(z) \quad (16)$$

where z is interpreted as a complex transform variable. Thus, every continuous signal that has a Laplace transform also has a z-transform by a simple substitution.

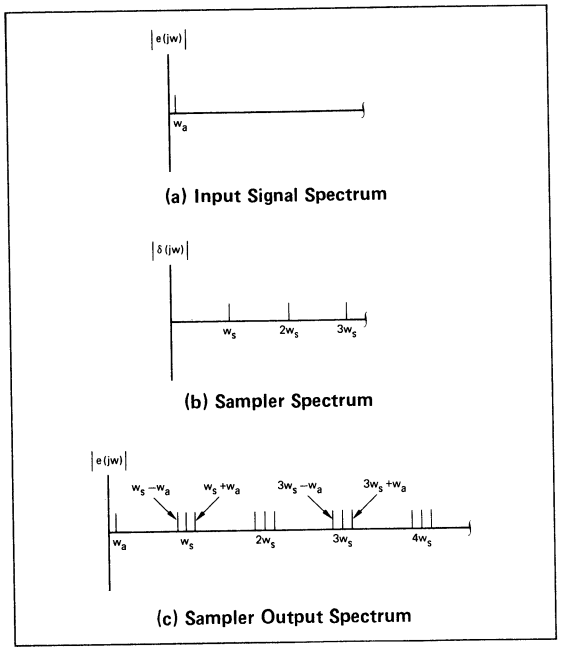



**Figure 3. Frequency Domain Sampling.**

Since the Laplace transform of a sampler is periodic, the z-transform performs a change of variable which retains the s-plane pole-zero configuration while stripping the function of its repetitive character. Thus, the z-transform allows simple algebraic manipulation of the polynomials in the z-plane just as the Laplace transform does for the polynomials in the s-plane.

The above substitution maps the periodic strip from $-w_s/2$ to $+w_s/2$ of the jw-axis of the s-plane onto the unit circle of the z-plane where $w_s$ is the sampling frequency. The remainder of this strip in the left-hand, s-plane is mapped inside the unit circle in the z-plane. This is shown in Figure 4.

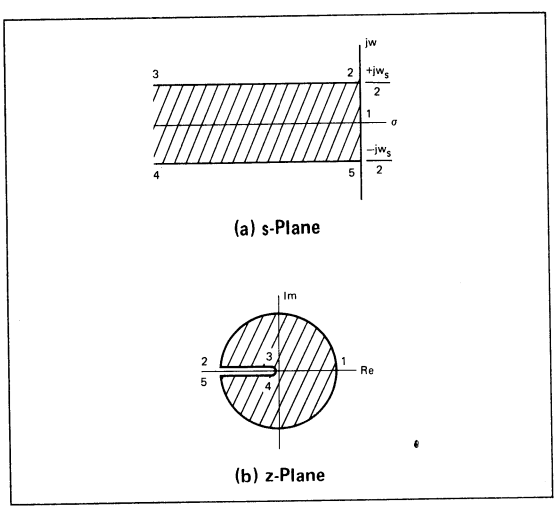



**Figure 4. S-Plane to z-Plane Transformation.**

Successive $w_s = 2\pi/T$ strips of the left hand side of the s-plane are mapped into the same unit circle of the z-plane. Likewise, the corresponding right-half strip is mapped as the exterior of the unit circle in the z-plane. If a transfer function is to be stable, its poles are in the left half of the s-plane; thus, the poles of the transformed function must lie within the unit circle in the z-plane. It follows that the z-plane poles and zeros occur on the real axis or in complex conjugate pairs.

The interval from $-w_s/2$ to $+w_s/2$ is known as the Nyquist interval. This interval places a bound on the bandwidth of the input signal to the sampler such that if the input signal is not bandlimited to below the radian frequency $w_s/2$, it cannot be recovered exactly at the output. Figure 5a shows the aliasing problems on the input spectrum after sampling if the input signal is not bandlimited while Figure 5b shows the spectrum of a bandlimited signal before and after sampling.

Using the substitution $z = e^{sT}$ on equation 3, the z-transform output for a sampled input signal is found as

$$V^*(z) = \sum_{n=0}^{\infty} v(nT)z^{-n} \qquad (17)$$

where $z^{-n}$ is a delay operator and n is an integer representing the number of past unit delays.

## THE DIFFERENCE EQUATION

In linear continuous (analog) filter theory, linear differential equations is one mathematical tool available to describe the transfer function. Similarly, in linear digital (sampled) filter theory, the linear difference equation is available as a mathematical tool for analysis and synthesis.

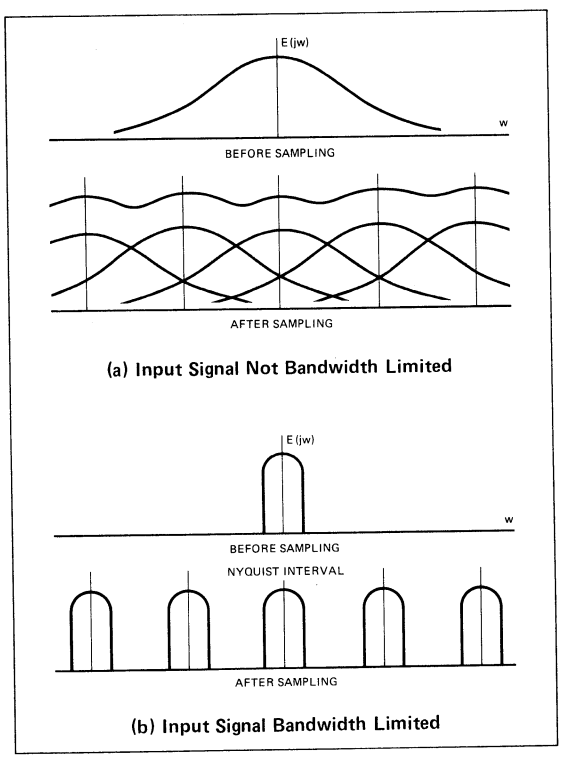



**Figure 5. Effect of Bandlimiting Before Sampling.**

The linear difference equation is used to define the sampled output pulse amplitude y(t) as a function of the present input pulse and any number of past input and output pulses. A general form of the difference equation[13] is

$$y(nT) = \sum_{i=0}^{N} A_i\, x(nT-iT) + \sum_{i=1}^{M} B_i\, y(nT-iT) \qquad (18)$$

where the notation x(nT) represents the present input sample and the x(iT) are past input samples. Similarly, y(nT) is the present output sample and the y(iT) are past output samples. The $A_i$ and $B_i$ coefficients are a set of constants which determine the response of the filter.

The z-transform of the general difference equation 18 is derived by using equation 17 and is given as

$$y(z) = x(z) \sum_{i=0}^{N} A_i z^{-i} + y(z) \sum_{i=1}^{M} B_i z^{-i} \qquad (19)$$

This equation is interpreted as: the present output is equal to the present and past inputs each multiplied by the respective coefficient $A_i$ plus the past outputs each multiplied by the respective coefficient $B_i$. Equation 19 is rewritten in the normal transfer function form as

$$H(z) = \frac{y(z)}{x(z)} = \frac{\sum_{i=0}^{N} A_i z^{-i}}{1 - \sum_{i=1}^{M} B_i z^{-i}} \qquad (20)$$

This is the general form of a transfer function in the z-plane that can be made equal to a transfer function in the s-plane to realize the sampled equivalent of a linear continuous filter.

### First Order Equation

A first order difference equation is written as

$$y(nT) = A_0\, x(nT) + A_1\, x(nT\text{-}T) + B_1\, y(nT\text{-}T) \qquad (21)$$

The z-transform of this difference equation is

$$E_o(z) = A_0 E_i(z) + A_1 z^{-1} E_i(z) + B_1 z^{-1} E_o(z) \qquad (22)$$

where $E_o$ is used to represent the output signal and $E_i$ is used to represent the input signal. The transfer function is obtained by rewriting this equation as

$$\frac{E_o(z)}{E_i(z)} = H(z) = \frac{A_0 + A_1 z^{-1}}{1 - B_1 z^{-1}} = \frac{A_0 z + A_1}{z - B_1} \qquad (23)$$

This transfer function can be implemented as shown in Figure 6.

### Second Order Equation

A second order difference equation is written as

$$y(nT) = A_0\, x(nT) + A_1\, x(nT\text{-}T) + A_2\, x\,(nT\text{-}2T) + B_1\, y(nT\text{-}T) + B_2\, y(nT\text{-}2T)$$

The z-transform of this difference equation is

$$E_o(z) = A_0 E_i(z) + A_1 z^{-1} E_i(z) + A_2 z^{-2} E_i(z) + B_1 z^{-1} E_o(z) + B_2 z^{-2} E_o(z) \qquad (25)$$

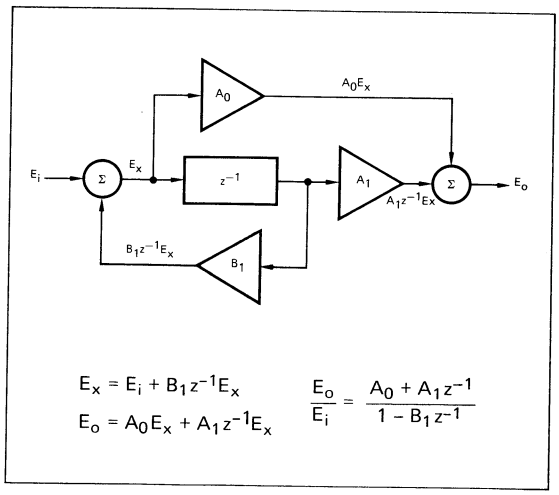



**Figure 6. Implementation of First Order Difference Equation.**

The transfer function is obtained by rewriting this equation as

$$\frac{E_o(z)}{E_i(z)} = H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 - B_1 z^{-1} - B_2 z^{-2}} = \frac{A_0 z^2 + A_1 z + A_2}{z^2 - B_1 z - B_2} \qquad (26)$$

This transfer function can be implemented as shown in Figure 7.

### Difference Equation Summary

The first and second order difference equations, their z-transform functions, and their circuit implementations serve as illustrative examples of the equivalence of the mathematical description and the hardware associated with digital filters. Since the z-transform is equal to the Laplace transform by means of the substitution $z = e^{sT}$, the first and second order implementations are mathematically related to s-plane transfer functions. A great wealth of information for design and synthesis of analog filters using Laplace transforms is available in the literature. It is therefore possible to use these procedures to design an equivalent analog transfer function, then transform this function to the z-plane and implement an equivalent digital filter using an appropriate configuration.

## DIGITAL FILTER CONFIGURATIONS

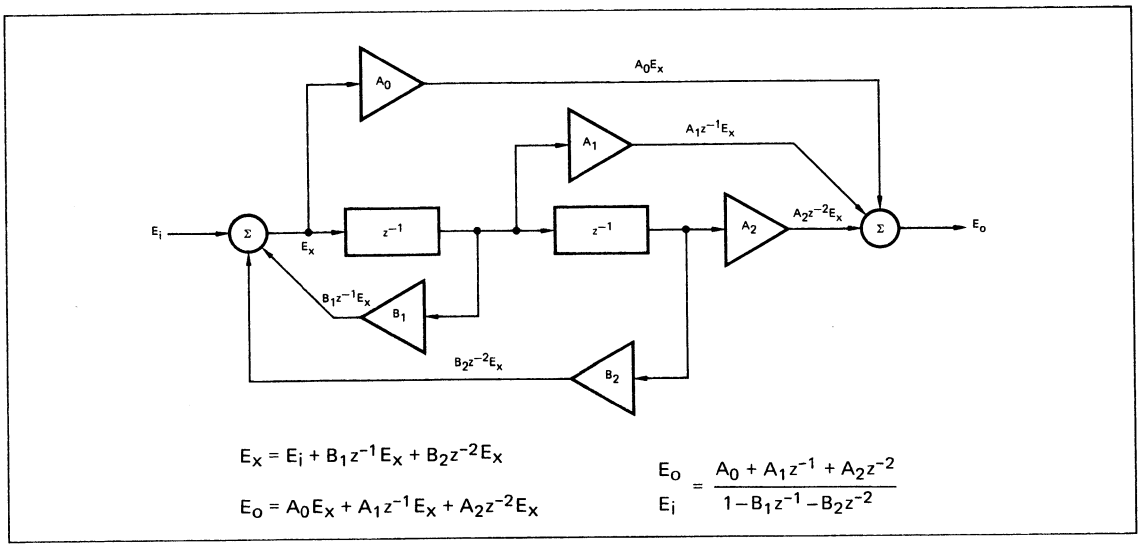
If the output y(nT) of a digital filter is a function of the present and past input samples, the filter is termed nonrecursive. That is, all $B_i$ of the general difference equation and zero. (Reference equation 27). If the past output samples are included in the algorithm, then the digital filter is termed recursive.

### Canonical Forms

There are three canonical forms of realizing a general recursive digital filter. These are the direct form, the cascade form and the parallel form.

In the direct form the output sequence is calculated by implementing the difference equation directly. Since the general equation is

$$y(nT) = \sum_{i=0}^{N} A_i\, x(nT-iT) + \sum_{i=1}^{M} B_i\, y(nT-iT) \qquad (27)$$




$$E_x = E_i + B_1z^{-1}E_x + B_2z^{-2}E_x$$

$$E_o = A_0E_x + A_1z^{-1}E_x + A_2z^{-2}E_x$$

$$\frac{E_o}{E_i} = \frac{A_0 + A_1z^{-1} + A_2z^{-2}}{1 - B_1z^{-1} - B_2z^{-2}}$$

**Figure 7. Implementation of Second Order Difference Equation.**

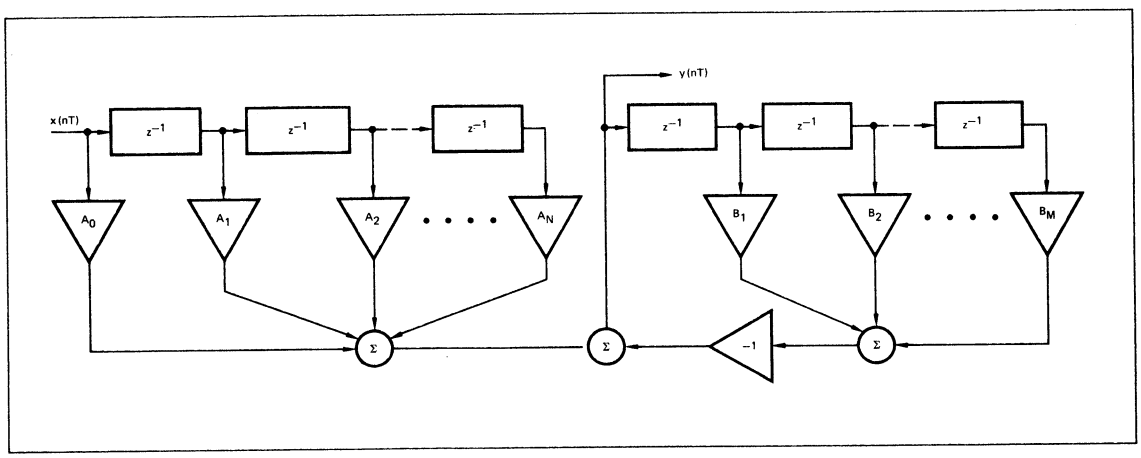



**Figure 8. Direct Canonical Form.**

the direct form digital filter takes the configuration of Figure 8. Figure 9 depicts another configuration of the direct canonic form in which the memory elements ($z^{-1}$) are shared by the feedback and feedforward loops. This direct form suffers from the fact that the pole locations are extremely sensitive functions of the coefficients $B_i$ for higher order filters[7]. This directly affects the precision required for the entire digital filter.

In the cascade form the digital filter is implemented from the transfer function written as a product of factors.

$$H(z) = A \frac{\prod_{i=1}^{K_1} (1 + a_iz^{-1} + b_iz^{-2})}{\prod_{i=1}^{K_2} (1 + c_iz^{-1} + d_iz^{-2})} \qquad (28)$$

This configuration consists of a series of lower order filters connected in cascade as shown in Figure 10. The pole coefficients $c_i$ and $d_i$ are not nearly as sensitive as the direct figuration[4]. Therefore, this form is especially practical for higher order filters.

The parallel canonical form is implemented by writing the transfer function as a sum of partial fractions.

$$H(z) = A_0 + \sum_{i=1}^{K} \left[ B_i \frac{a_i + b_iz^{-1}}{1 + c_iz^{-1} + d_iz^{-2}} \right] \qquad (29)$$

This configuration consists of a group of lower order filters each operating on the input signal with the output of the parallel bank of filters summed together as in Figure 11.

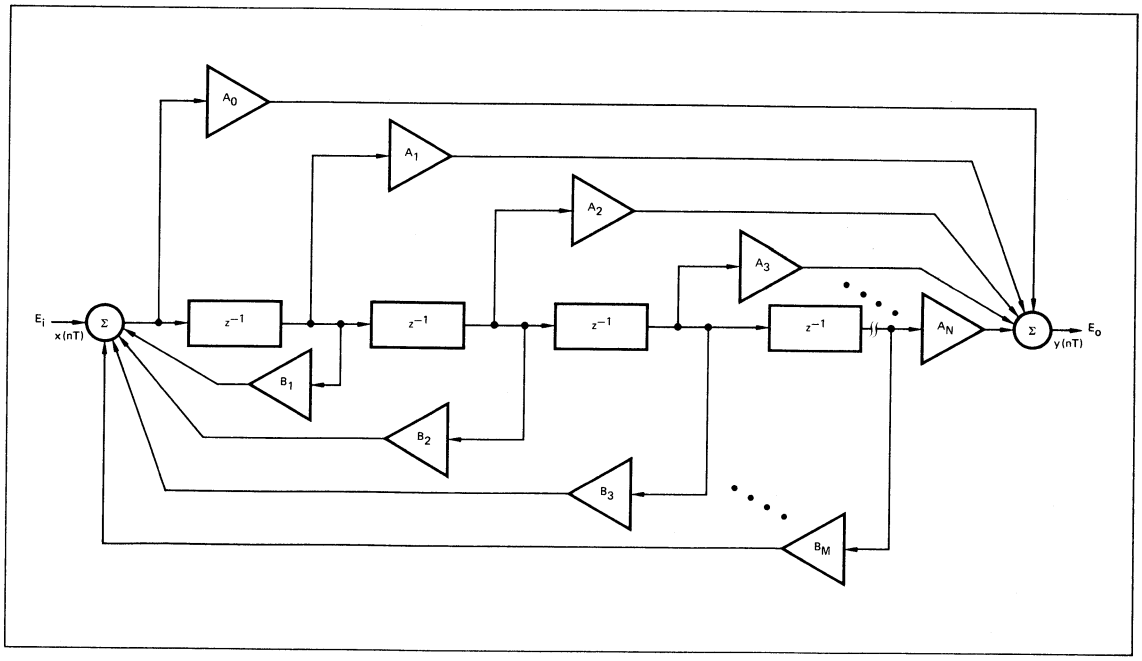



**Figure 9. Direct Canonical Form With Feedback and Feedforward Loops Sharing the Same Memory.**

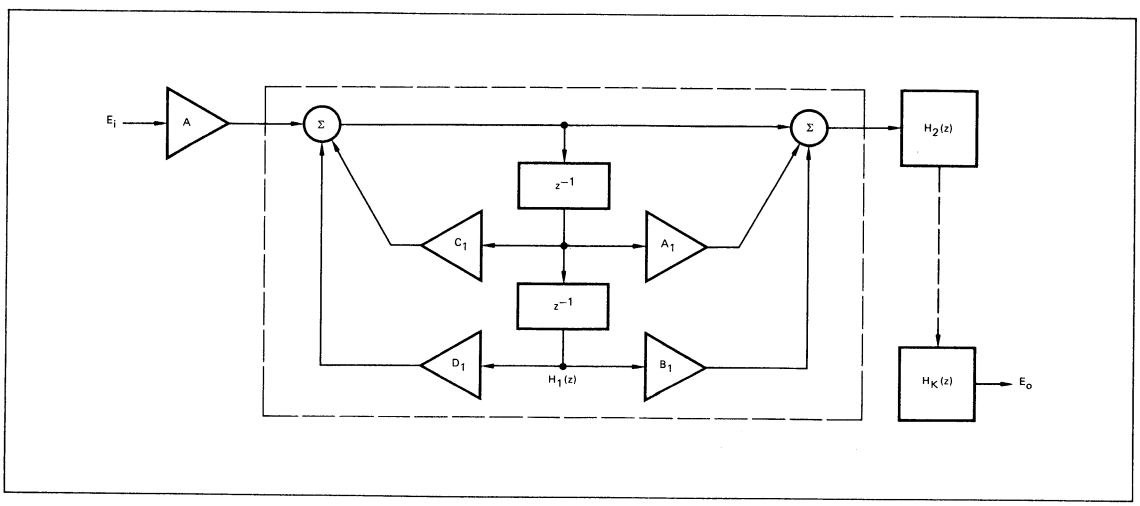



**Figure 10. Cascade Canonical Form.**

### Other Configurations

Figure 12 illustrates a recursive one-pole, one-zero building block while Figure 13 represents a recursive two-pole, two-zero building block. In these structures, the $B_i$ determine the pole locations in the z-plane while the $A_i$ determine the zero locations in the z-plane.

A general recursive two-pole building block with the z-plane transfer function is shown in Figure 14.

It is apparent that many digital filter configurations can be designed. Each configuration has properties that may or may not be desirable depending on the particular application. Thus, each application must be treated individually and it is difficult to generalize that one configuration is always superior.

## SYNTHESIS TECHNIQUES

There are three transform techniques that find the greatest application in the design of digital filters from continuous transfer functions. These are the standard z-transform, the bilinear z-transform and the matched z-transform.

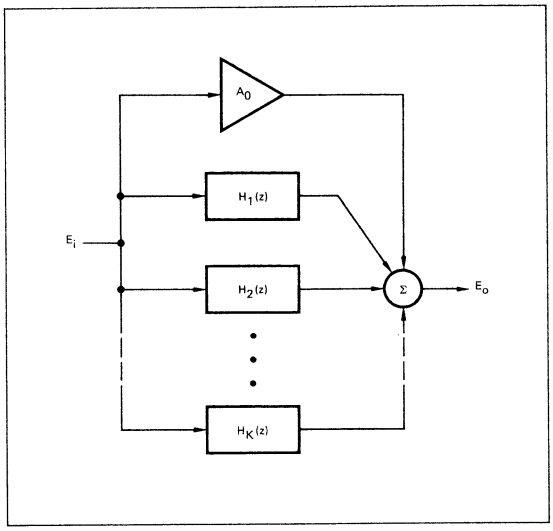



Figure 11. Parallel Canonical Form.

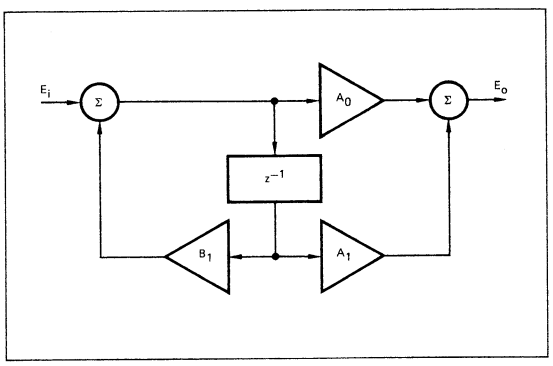



Figure 12. Recursive One-Pole Structure.

### Standard Z-Transform Method

The standard z-transform, also known as the impulse invariant technique, utilizes the partial fraction expansion of the continuous filter transfer function. This transformation preserves the impulse response of the sampled continuous filter and is best suited for low-pass and band-pass applications.

In using this technique the Laplace transform partial fraction expansion terms are replaced by the appropriate z-transform terms. The substitutions used are shown in Table 1.

From this it is seen that the standard z-transform technique gives a transfer function of the form

$$H(z) = A_0 + \sum_{i=1}^{K} \frac{a_i}{1-b_i z^{-1}} + \sum_{j=1}^{L} \frac{a_j + b_j z^{-1}}{1+c_j z^{-1} + d_j z^{-2}} \qquad (30)$$

where any of the above coefficients may be zero.

Thus, the coefficients are defined uniquely and the digital filter can be implemented directly using one-pole and two-pole building blocks in the parallel canonical form as described in the previous section.

### Bilinear Transformation Method

The bilinear z-transform is an algebraic mapping transformation utilizing the substitution

$$s = \frac{2(1-z^{-1})}{T(1+z^{-1})} \qquad (31)$$

This transform maps a sampling interval from $-jw_s/2$ to $+jw_s/2$ in the s-plane onto the unit circle in the z-plane. It should be noted however, that this transform does not yield a linear map as does the substitution $z = e^{st}$; that is, a non-linear warping of the frequency scale in the z-plane results. The magnitude of this warping is given by

$$W_A = \frac{2}{T} \operatorname{Tan}\left(\frac{w_D T}{2}\right) \qquad (32)$$

where $w_A$ = s-plane frequency
$w_D$ = z-plane warped frequency

In searching the literature on the bilinear z-transform,[3,4,5] another substitution is presented that is very similar to equation 31; that is

$$s \rightarrow \frac{z-1}{z+1} \qquad (33)$$

with the warping function given as

$$w_A \rightarrow \operatorname{Tan}\left(\frac{w_D T}{2}\right) \qquad (34)$$

Occasionally this causes confusion since the units are not the same. In practice, however, both substitutions yield the same pole-zero configuration since the w/T terms will factor and cancel. This is best understood by making the respective substitutions in a general transfer function for a complex pole-pair such as

$$H(s) = \frac{w^2}{s^2 + 2\delta w s + w^2} \qquad (35)$$

and comparing the z-plane pole positions that result.

When using the bilinear z-transform care must be taken when the break frequencies are near the half sampling frequency. An illustration of this fact and an appreciation of the warping required is best illustrated by an example. Table 2 shows various digital filter break frequencies and the required warped analog frequencies for a 1000 Hz sampling rate. Figure 15 shows graphically the non-linear frequency scale mapping of the bilinear z-transform.

Thus the bilinear z-transform is a powerful tool in digital filtering and may be utilized with either the partial fraction expansion or the rational fraction form of the Laplace transfer function. It is especially useful in MTI radar filters since the break frequencies of the high-pass and band-pass filters used are normally very low compared with the sampling frequency. This means that the warping is very small and the digital design very closely approximates the analog design.

### Matched Z-Transform

The matched z-transform is somewhat of a compromise between the standard and bilinear z-transforms. It is an exponential mapping transform which gives a z-plane transfer function with poles and zeros matched to those of the continuous function.

Real poles or zeros are mapped using the substitution

$$s - a \rightarrow 1 - z^{-1} e^{aT} \qquad (36)$$

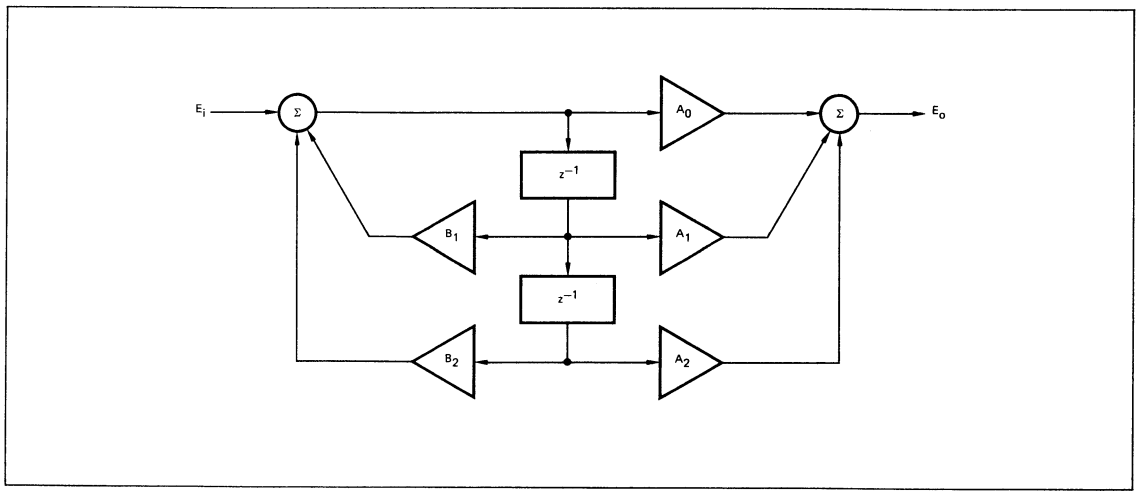
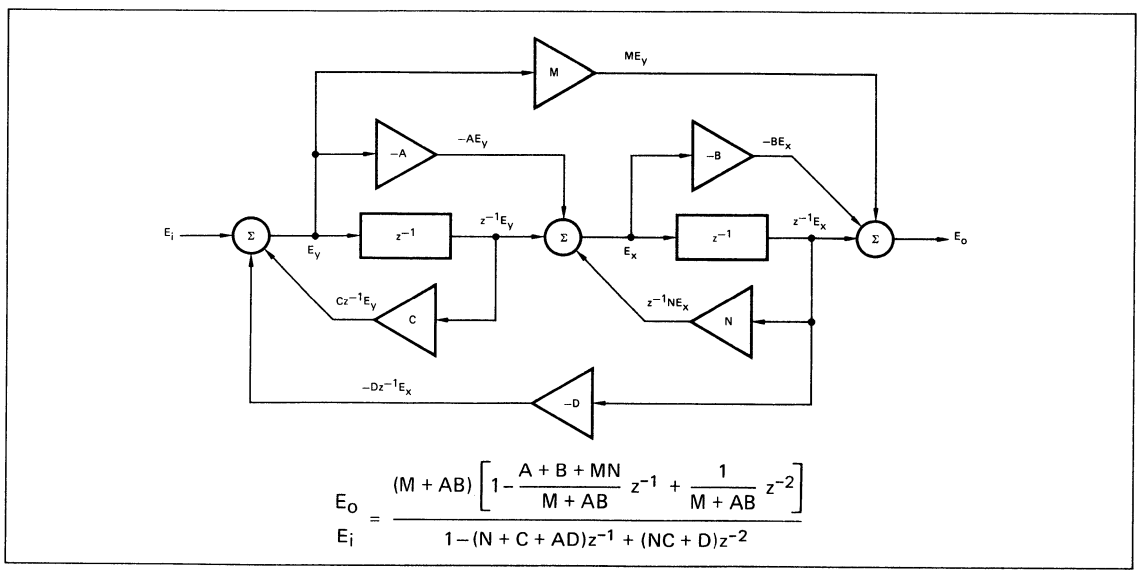



**Figure 13. Recursive Two-Pole Structure.**




$$\frac{E_o}{E_i} = \frac{(M+AB)\left[1-\frac{A+B+MN}{M+AB}z^{-1}+\frac{1}{M+AB}z^{-2}\right]}{1-(N+C+AD)z^{-1}+(NC+D)z^{-2}}$$

**Figure 14. General Two-Pole Building Block.**

while complex poles or zeros are mapped using the substitution

$$(s-a)^2+b^2 \rightarrow 1-2z^{-1}e^{aT}\,\mathrm{Cos}(bT)+z^{-2}e^{2aT} \qquad (37)$$

The resulting z-plane transfer function is normally factored into numerator and denominator polynomials that are easily implemented using one and two-pole building blocks in the cascade canonical form.

The matched z-transform yields the same pole configuration as the standard z-transform; however, the zero configuration may require some modification to give satisfactory results. This usually entails the addition of zeros at the half sampling frequency (z= −1) to give the desired result.[8]

**TABLE I. Standard z-Transform Substitutions.**

| f(t) | F(s) | F(z) |
|---|---|---|
| $e^{-aT}$ | $\frac{1}{s+a}$ | $\frac{z}{z-e^{-aT}}$ |
| $\sin(w_0t)$ | $\frac{w_0}{s^2+w_0^2}$ | $\frac{z\sin(w_0T)}{z^2-2z\cos(w_0T)+1}$ |
| $\cos(w_0t)$ | $\frac{s}{s^2+w_0^2}$ | $\frac{z(z-\cos(w_0T))}{z^2-2z\cos(w_0T)+1}$ |

**TABLE II. Digital Filter Warping Relation.**

$$f_A = \frac{1}{\pi T} \tan(\pi f_D T) \qquad T = 10^{-3} \text{ seconds}$$

| Desired Digital Filter Break Frequency $f_D$ Hz | Prewarped Analog Frequency $f_A$ Hz | $\tan(\pi f_D T)$ |
|---|---|---|
| 50 | 50.5 | .15838 |
| 100 | 103.2 | .32492 |
| 200 | 231 | .72654 |
| 250 | 318 | 1.0000 |
| 300 | 438 | 1.3764 |
| 400 | 978 | 3.0777 |
| 450 | 2010 | 6.3138 |
| 475 | 4050 | 12.706 |
| 500 | ? | $\infty$ |

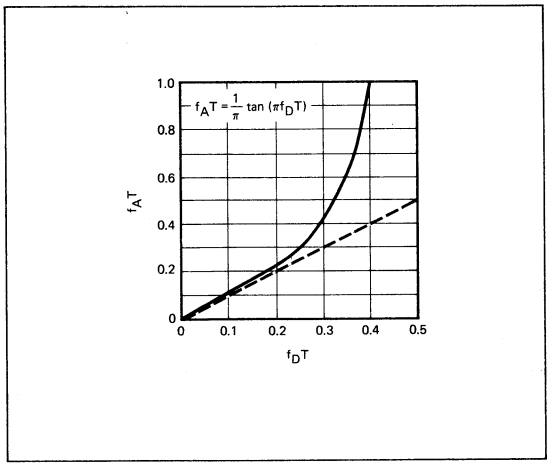



**Figure 15. Bilinear z-Transform Frequency Scale Warping.**

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# DIGITAL FILTER DESIGN

**By John R. Mick**

There are several important considerations in determining parameters for the design of a digital filter. Many trade-offs exist in the selection of configuration, arithmetic, memory type, A/D converters, D/A converters etc. Some of the key parameters are examined here.

The most important single item in the digital filter design is the selection of the configuration. Because of this, an analysis of both a two-pole filter section and a single-pole filter section are presented here. The analysis concentrates primarily on the high-pass filter characteristics; however, it can also be performed on band-pass or low-pass recursive digital filters.

## COMPLEX POLE ANALYSIS

Since the implementation of many digital filters is typically a cascaded combination of two-pole sections composed of complex conjugate pairs of poles, it is important to examine this case in detail. The z-transform analysis of a normalized complex conjugate pair of poles in the s-plane follows and reveals several important equations for the design of digital filters.

Assume a general two-pole transfer function of

$$H(s) = \frac{K}{(s-s_1)(s-s_2)} \tag{1}$$

where $s_1 = (-x + jy)w_a$

$s_2 = (-x - jy)w_a$

such that these poles lie on a normalized unit circle in the s-plane and are scaled to their actual analog radian frequency by a multiplier $w_a$ as shown in Figure 1.

Substituting $s_1$ and $s_2$ into H(s), the transfer function is

$$H(s) = \frac{K}{(s + xw_a)^2 + (yw_a)^2} \tag{2}$$

Expanding the denominator of this transfer function and remembering that $x^2 + y^2 = 1$, the resultant transfer function becomes

$$H(s) = \frac{K}{s^2 + 2xw_a s + w_a{}^2} \tag{3}$$

This is similar to the usual textbook equation of

$$G(s) = \frac{K_0 w_n{}^2}{s^2 + 2\zeta w_n s + w_n{}^2} \tag{4}$$

Clearly, x is equivalent to $\zeta$ (zeta), the damping ratio, and $w_a$ is equivalent to $w_n$, the resonant break frequency.

Since equation 3 describes a continuous analog function and since a digital filter usually is operating as a sampling system with a zero-order hold in the video channel before the filter, this continuous function is transformed to the z-plane for easier algebraic manipulation. Since high-pass filtering is to be described, the equivalent form of the bilinear z-transform is

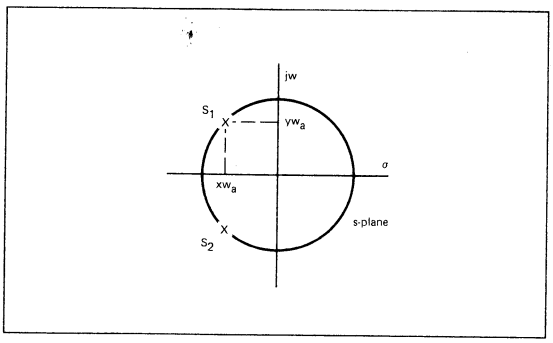


**Figure 1. General Two-Pole s-Plane Plot.**

used. Note that in a low-pass filter section, the zero locations do not affect the pole locations. This form uses the substitution, $s = (z-1)/(z+1)$. The z-plane transfer function becomes

$$H(z) = \left[\frac{K}{1+2xw_a+w_a{}^2}\right]\left[\frac{(z+1)^2}{z^2 - 2\left(\frac{1-w_a{}^2}{1+2xw_a+w_a{}^2}\right)z + \frac{1-2xw_a+w_a{}^2}{1+2xw_a+w_a{}^2}}\right] \tag{5}$$

where a gain multiplier factors from the transfer function when it is put in standard form. The poles in the z-plane are

$$z_1, z_2 = \frac{1-w_a{}^2 \pm j2w_a\sqrt{1-x^2}}{1+2xw_a+w_a{}^2} \tag{6}$$

Also, it is important to recognize that when using the bilinear z-transform, the analog radian break frequency $w_a$ must be prewarped by the relation

$$w_a = \tan\left(\frac{w_D T}{2}\right) = \tan(\pi f_D T) \tag{7}$$

where $f_D$ is the desired break frequency of the digital filter and T is the sampling interval. The prewarping is a function of the sampling rate which means that as the sampling rate is changed, the pole locations of the transfer function change. The transfer function derived in equation 5 is equivalent to the z-transform of a second order difference equation. This difference equation is

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 - B_1 z^{-1} - B_2 z^{-2}} \tag{8}$$

which can be rearranged to eliminate $A_2$ and the variables renamed for convenience as

$$H(z) = G\left[\frac{B + Az^{-1} + z^{-2}}{1 - Cz^{-1} + Dz^{-2}}\right] = G\left[\frac{Bz^2 + Az + 1}{z^2 - Cz + D}\right] \tag{9}$$

The DC gain (z = 1) of this transfer function is

$$\text{DC Gain} = G\left[\frac{B + A + 1}{1 - C + D}\right] \tag{10}$$

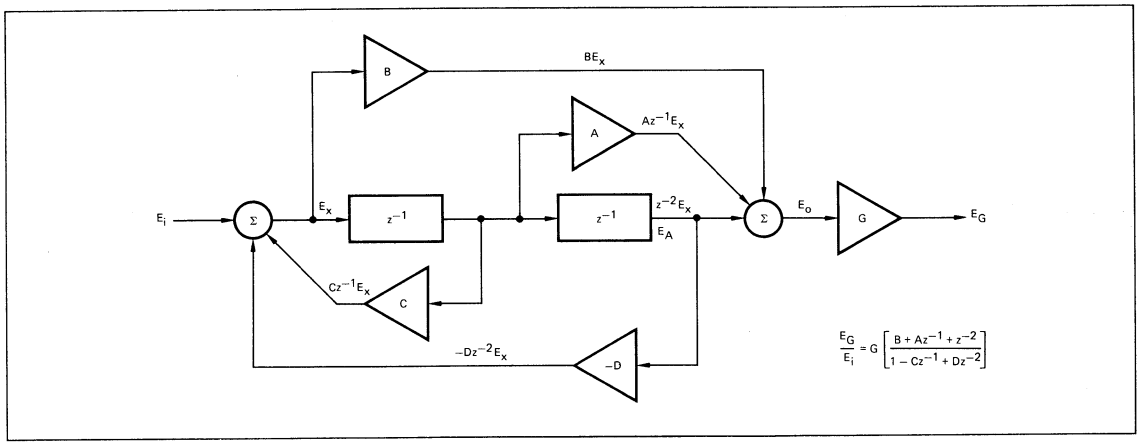


**Figure 2. Canonical Two-Pole Digital Filter Implementation.**

Implementation of this transfer function is shown in Figure 2.

This analysis results in the general z-plane transfer function of equation 5 that is equivalent to the general s-plane transfer function for a complex conjugate pair. The transfer function of equation 5 determines the numerical values for the multipliers in the digital design and yields a digital filter that is equivalent to its analog counterpart.

## INTERNAL MAGNIFICATION – CANONICAL FORM

The internal magnification within the digital filter building block is analyzed to determine the number of additional storage bits that must be provided in memory over and above the input quantization number of bits. This is accomplished by deriving the internal transfer function at each memory input (or output) and computing the peak magnification expected. Also, by setting z = 1, the DC magnification is determined.

The internal transfer function at the memory output within the filter of Figure 2 is

$$\frac{E_A}{E_i} = \frac{z^{-2}}{1 - Cz^{-1} + Dz^{-2}} = \frac{1}{z^2 - Cz + D} \qquad (11)$$

The magnitude squared of this internal transfer function is computed by multiplying the denominator polynomial by its complex conjugate. That is

$$\left|\frac{E_A}{E_i}\right|^2 = \frac{1}{(z^2 - Cz + D)\,(z^{*2} - Cz^* + D)} \qquad (12)$$

which results in

$$\left|\frac{E_A}{E_i}\right|^2 = \frac{1}{1 + C^2 + D^2 + 2D\cos(2wT) - 2C(D+1)\cos(wT)} \qquad (13)$$

Differentiating the denominator with respect to w and setting the result equal to zero yields

$$\frac{d(DENOM)}{dw} = 0 = +2TC(D+1)\sin(wT) - 4DT\sin(2wT) \qquad (14)$$

Thus, the frequency at which the peak internal magnification is reached is

$$\cos(wT) = \frac{C(D+1)}{4D} \leq 1.0 \qquad (15)$$

$$f = \frac{1}{2\pi T}\cos^{-1}\left(\frac{C(D+1)}{4D}\right) \qquad (16)$$

Computing the peak magnitude at this frequency using the squared magnitude function yields

$$M_A = \left|\frac{E_A}{E_i}\right| = \frac{1}{\sqrt{\left(1 - \frac{C^2}{4D}\right)\,(1-D)^2}} \qquad (17)$$

which is the maximum magnification within this two-pole building block. One extra bit must be provided in both memories of this filter for each factor of two or fraction thereof as computed in this magnification for stable operation of the filter. Figure 3 shows the upper right hand quadrant of the z-plane, with contours of constant magnification factor, M, (same as $M_A$) plotted thereon. The lower right hand quadrant is the mirror image of this plot since the poles appear as complex conjugate pairs.

The pole locations as seen from equation 11 for the internal transfer function of this filter are

$$z_1, z_2 = \frac{C}{2} \pm j\frac{\sqrt{|C^2 - 4D|}}{2} \qquad (18)$$

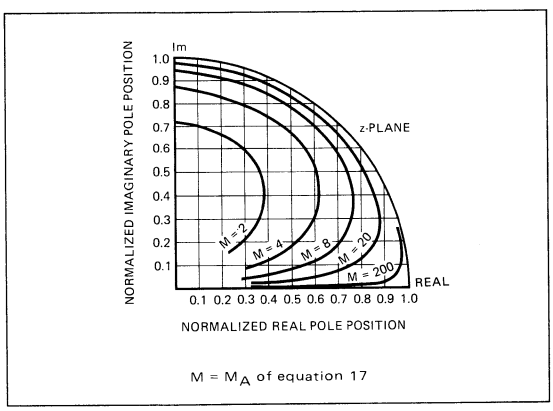


**Figure 3. Peak Gain of Canonical Two-Pole Digital Filter for Pole Position in the z-Plane.**

where $|4D| > |C^2|$

A typical plot of these poles is shown in Figure 4. As these poles are moved toward the point z = 1 in Figure 4, the break frequency of the filter is lowered with respect to the sampling rate. From this, it can be seen that the real part of the pole is approaching 1.0; thus, the value of C is approaching 2.0. Likewise, the imaginary part of the pole is approaching 0.0; thus, the absolute value of $C^2 - 4D$ is approaching zero. Since C is near 2.0, D is approaching 1.0 for this condition. When these values of C = 2 and D = 1 are inserted into the maximum magnification equation, it is found that the peak value goes to infinity. This is easily checked by looking at the DC gain of the internal transfer function by substituting z = 1; it is

$$M_D = \left.\frac{E_A}{E_i}\right|_{z=1} = \frac{1}{1-C+D} \qquad (19)$$

and for C = 2.0 and D = 1.0 is found to be infinite. The internal DC magnification for this two-pole building block is plotted as a function of pole position in Figure 5 for the upper right hand quadrant of the z-plane. The lower right hand quadrant is the mirror image since the poles occur in complex conjugate pairs.

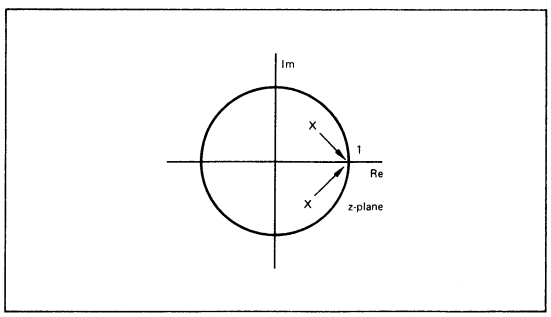


**Figure 4. Internal z-Plane Pole Location of Two-Pole Section.**

## INTERNAL MAGNIFICATION—IMPROVED FORM

The canonical form two-pole, two-zero building block yields an internal transfer function that requires an increasing number of extra storage bits as the cut-off frequency is lowered with constant sampling rate. As the cut-off frequency is designed nearer to zero, the required extra bits can easily be five or ten times the total input quantization number of bits. This has an almost direct effect on the cost of the processor. Therefore, it is essential that a configuration is found that minimizes the internal magnification. The digital filter shown in Figure 6 has this characteristic. The improvement is provided by the zero that is in the internal transfer function. This tends to cancel the effect of the poles and greatly reduces the internal magnification.

The analysis of the filter configuration of Figure 6 demonstrates the improvement realized. The overall filter transfer function is

$$H(z) = \frac{(z-1)^2}{z^2 - Cz + D} \qquad (20)$$

The internal transfer function at the output of the first memory is

$$\frac{E_B}{E_i} = \frac{D + z(1-C)}{z^2 - Cz + D} \qquad (21)$$

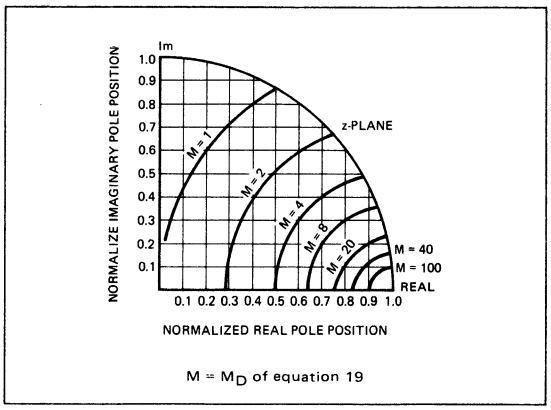


**Figure 5. DC Gain of Canonical Two-Pole Digital Filter for Pole Position in the z-Plane.**

Notice the DC gain of this memory element is not a function of the coefficient values but is

$$\left.\frac{E_B}{E_i}\right|_{z=1} = \frac{D+1-C}{1-C+D} = 1 \qquad (22)$$

The frequency at which the peak magnitude within this part of the filter occurs is

$$\cos(wT) = \alpha = \frac{-(D^2 + (1-C)^2)}{2D(1-C)} \pm \frac{\sqrt{(D^2+(1-C)^2)^2 - (1-C)\left[CD(C-3D) - C(1-C)^2 - D(1-D)^2\right]}}{2D(1-C)} \qquad (23)$$

$$f = \frac{1}{2\pi T}\cos^{-1}(\alpha) \qquad (24)$$

The peak magnitude reached at this frequency is (25)

$$M_B = \left|\frac{E_B}{E_i}\right| = \sqrt{\frac{(1-C)^2 + D^2 + 2D(1-C)\cos(wT)}{(1-D)^2 + C^2 - 2(C+CD)\cos(wT) + 4D\cos^2(wT)}}$$

Examining the transfer function $E_B/E_i$ shows that a discontinuity exists at C = 1. Here the internal transfer function reduces to

$$H(z) = \frac{D}{z^2 - Cz + D} \qquad (26)$$

The peak frequency of H(z) for this condition can be determined from

$$\cos(wT) = \frac{(1+D)}{4D} \leqslant 1.0 \qquad (27)$$

and the peak magnitude at this frequency is

$$M_B\,|_{C=1} = \left|\frac{E_B}{E_i}\right| = \frac{D}{\sqrt{(1-D)^2\left(1-\frac{1}{4D}\right)}} \qquad (28)$$

The internal transfer function at the output of the second memory word of the filter in Figure 6 is

$$\frac{E_F}{E_i} = H(z) = \frac{1-z}{z^2 - Cz + D} \qquad (29)$$

| Filter Coefficients | | z-Plane | | Canonical Magnification | | Improved Form Memory #1 | | Improved Form Memory #2 | |
|---|---|---|---|---|---|---|---|---|---|
| C | D | Real | Imag. | DC | Peak | DC | Peak | DC | Peak |
| 62/32 | 31/32 | .97 | .17 | 32.0 | 181.0 | 1.0 | 31.2 | 0.0 | 32.3 |
| 61/32 | 31/32 | .95 | .17 | 32.0 | 90.9 | 1.0 | 15.1 | 0.0 | 16.1 |
| 60/32 | 29/32 | .94 | .17 | 32.0 | 61.4 | 1.0 | 9.7 | 0.0 | 10.7 |
| 58/32 | 27/32 | .91 | .15 | 32.0 | 39.0 | 1.0 | 5.4 | 0.0 | 6.4 |
| 54/32 | 23/32 | .84 | .08 | 32.0 | 32.0 | 1.0 | 2.6 | 0.0 | 3.6 |
| 50/32 | 20/32 | .78 | .12 | 32.0 | 16.0 | 1.0 | 1.7 | 0.0 | 2.7 |

**Table 1. Magnification Examples**

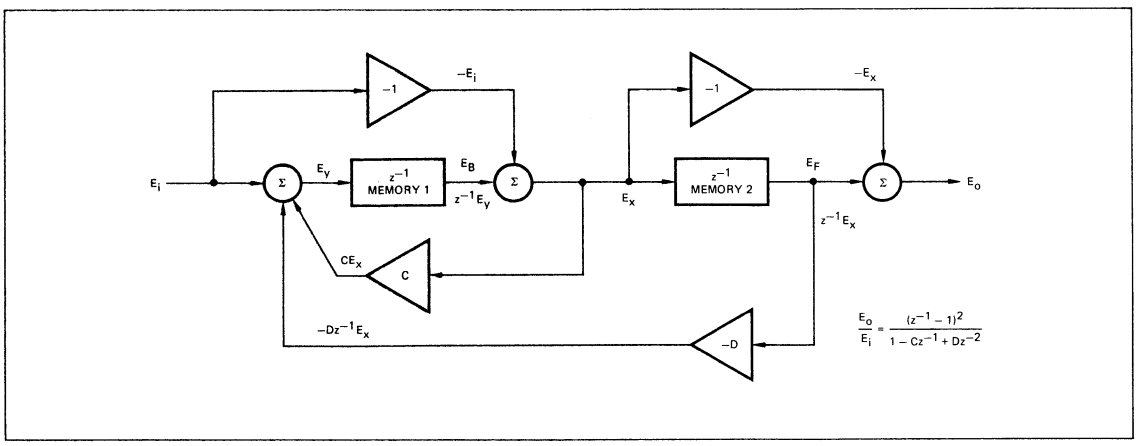


**Figure 6. Improved Two-Pole Digital Filter.**

The DC gain (z = 1) of this memory element is zero—a marked improvement from the canonical form. The frequency at which the peak magnitude occurs in this memory can be computed from

$$\cos(wT) = 1 \pm \frac{C-1+D}{2\sqrt{D}} \leqslant 1.0 \qquad (30)$$

the peak magnitude reached at this frequency is (31)

$$M_F = \left|\frac{E_F}{E_i}\right| = \sqrt{\frac{2-2\cos(wT)}{(1-D)^2+C^2-2(C+CD)\cos(wT)+4D\cos^2(wT)}}$$

An example of the improvement offered by the filter in Figure 6 is shown in Table 1 where the results of several examples using these equations are tabulated. As a result of this analysis it is obvious that an improved form of filter configuration exists. The equations are readily programmed on a general purpose digital computer to assist in the design phase by carrying out the computations for various arithmetic coefficients.

## SINGLE POLE ANALYSIS

For systems where an odd number of poles in the digital processor provides acceptable performance, at least one real pole is required in the digital filter transfer function. To analyze this condition consider the s-plane plot for a single high-pass section. A "zero" is located at zero and a "pole" is located at –a on the real axis in the s-plane as shown in Figure 7a. The resultant s-plane transfer function for the high-pass section is

$$H(s) = \frac{s}{s+a} \qquad (32)$$

Using the equivalent bilinear form of the z-transform, the z-plane transfer function is

$$H(z) = \left(\frac{1}{1+a}\right)\left[\frac{z-1}{z+\frac{(a-1)}{(a+1)}}\right] \qquad (33)$$

and the pole and zero are plotted in Figure 7b. As in the two-pole analysis, the frequency scale must be prewarped due to the non-linear transformation to achieve the desired digital filter implementation

$$a = \tan\left(\frac{w_D T}{2}\right) \qquad (34)$$

where a = design s-plane radian frequency
$w_D$ = desired digital filter cut-off radian frequency

Figure 8 shows a one-pole, one-zero digital filter implementation where the z-plane transfer function is

$$H(z) = \frac{z-1}{z-C} \qquad (35)$$

The coefficient C is determined from

$$C = \frac{1-a}{1+a} \tag{36}$$

If the overall transfer function gain of the digital filter is critical, a gain multiplier equal to 1/(1+a) must be placed after the single-pole section. The internal transfer function of this single-pole cell at the memory output $E_A$ is

$$\frac{E_A(z)}{E_i(z)} = \frac{z^{-1}(1-C)}{1-Cz^{-1}} = \frac{1-C}{z-C} \tag{37}$$

The peak gain occurs at DC for this filter and is computed by setting z = 1. For this filter configuration the DC gain is unity.

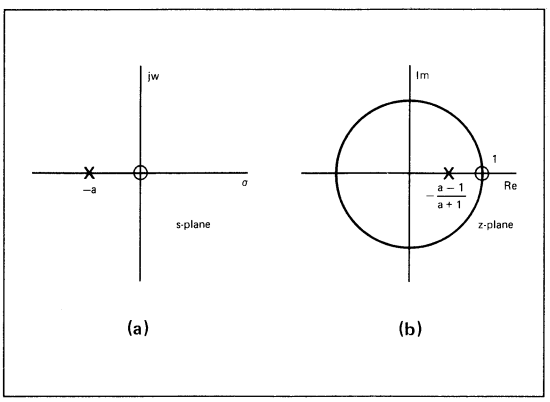


**Figure 7. Single-Pole s-Plane and z-Plane Plot.**

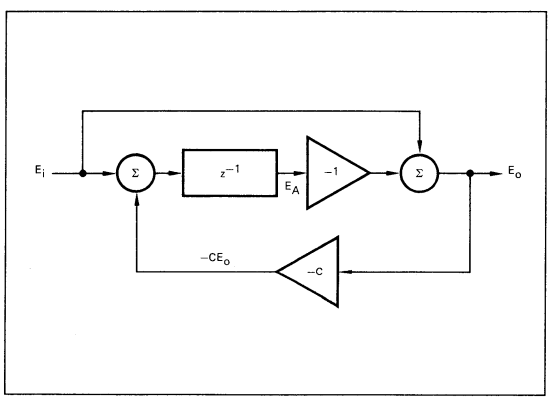


**Figure 8. Single-Pole, Single-Zero Digital Filter.**

## ARITHMETIC

Once the digital filter configuration is selected, several other decisions must be made concerning the actual operations within this configuration. These decisions regarding the numbering system, arithmetic, multipliers etc. influence each other; however, throughout this discussion they are considered independently.

The first of these decisions is the binary number system used. Since the arithmetic to be performed by the digital processor includes addition, subtraction, and multiplication of both positive and negative numbers, the two's complement numbering system is the best binary representation system for real-time digital processors. The two's complement representation is utilized throughout the digital filter as long as a bipolar numbering quantization scheme is required.

The coefficient multipliers C, D and G of Figure 2 can be easily implemented using the Am25LS14 serial/parallel multiplier. Likewise, the additions and subtractions required can be performed using the Am25LS15 quad serial adder/subtractor. The basic signal flow is shown in Figure 9. This figure is an oversimplification since it does not show all the timing and control as well as the delays required in the data path to enable the serial data to arrive at the appropriate adder inputs at the necessary sequence time. The figure does show the basic architecture required to implement the canonical two-pole, two-zero building block using the Am25LS14 and Am25LS15. Also the figure does demonstrate a key point. That is, the entire arithmetic section (assuming 8-bit coefficients) can be implemented using five Am25LS14's and one Am25LS15; a significant hardware reduction compared to any other implementation scheme. The delays, timing and control can be designed as required for each application.

The hardware required to implement the improved two-pole, high-pass filter depicted in Figure 6 is demonstrated in Figure 10. Here the required single flip-flop delay in the serial data path is shown. Thus all memories, multipliers, adder/subtractors and the D-type flip-flop can be clocked in unison and the LSB's reach the data path inputs in synchronism throughout the algorithm.

This two-pole, high-pass filter arithmetic section is implemented using only one Am25LS15 and two Am25LS14's for 8-bit C and D coefficients. The memory length can be as required for the design accuracy of the application. This example assumes that the digital number range has the required dynamic range to handle the maximum expected magnification within the filter. Round-off, truncation, overflow etc. can be handled in other ways as required by the design. If round-off is required an additional adder section can be placed in front of the memory and plus one added at the appropriate bit to perform the rounding. A microprogrammed state-machine approach is recommended as the control means to provide the required input signals and timing. Likewise one section of an Am25LS15 adder can be used to detect overflow if required.

The single-pole, single-zero digital filter section as shown in Figure 8 can also be easily implemented using the Am25LS14, Am25LS15 and the serial memory as required.

From these examples it is seen that the Am25LS14 and Am25LS15 can be used to perform all multiplication, addition and subtraction required in a digital filter algorithm implemented in serial/parallel hardware. While not specifically discussed in these examples, it should be recognized that the Am25LS22 and Am25LS299 are also applicable to the memory portions of the filters. However care must be exercised when using the sign extend feature of the Am25LS22 so that data for the next cycle is not lost.

For example the first memory (left hand side) of Figure 10 can be implemented using a single Am25LS22 (8-bit truncated word).

The second memory (right hand side), however, requires an Am25LS22 preceded by an Am25LS299 (or another Am25LS22) so that the data out of the first adder can be retained while the sign extend function is being performed in this memory.

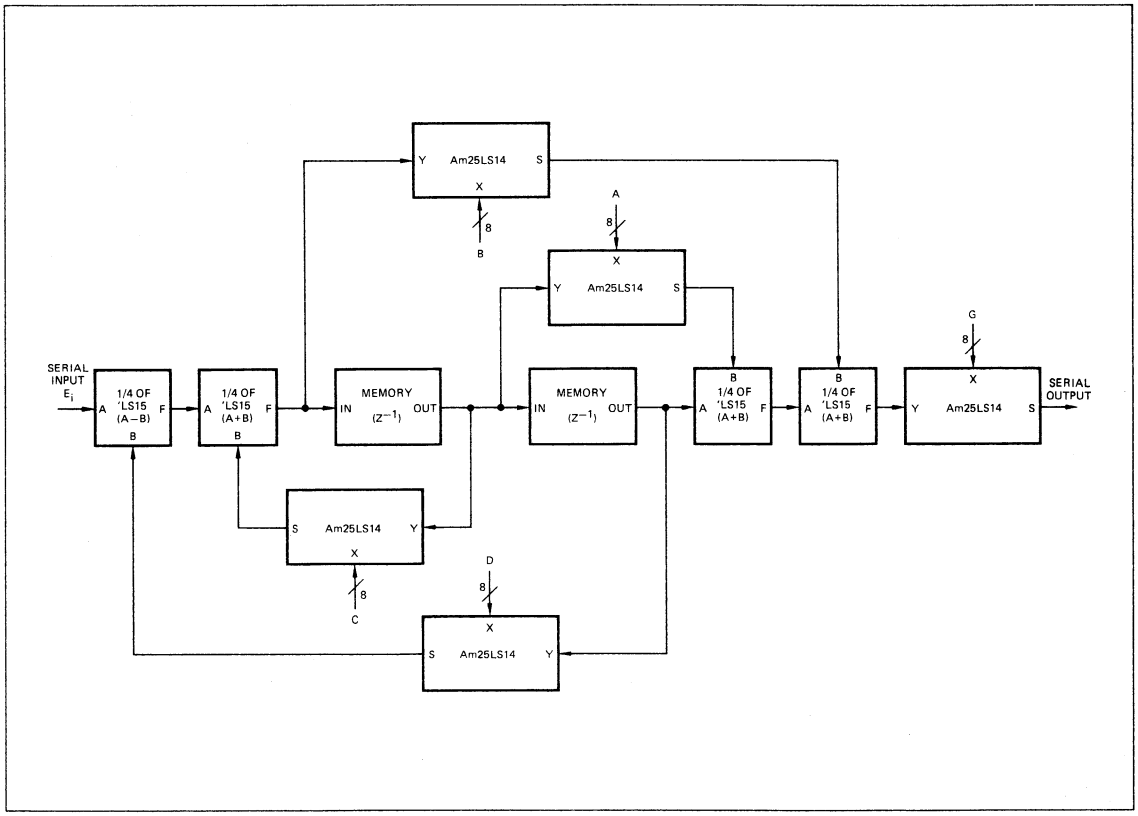


**Figure 9. Canonical Two-Pole, Two-Zero Recursive Digital Filter Using the Am25LS14 and Am25LS15.**

## FILTER GAIN

The s-plane transfer function for a complex pair of poles yields a z-plane transfer function from which a gain multiplier is factored as shown in equation 5 and is

$$\frac{K}{1+2 \times w_a + w_a{}^2} \tag{38}$$

While the K is in the initial s-plane transfer function assumption, the quantity $1/(1 + 2 \times w_a + w_a{}^2)$ is a constant that must be recognized as it is usually greater than 1.0. This means that in the cascade two-pole, building-block approach, the maximum input dynamic range to each section is increasing by this quantity. Therefore a gain coefficient multiplier may be required between each two-pole building block to reduce the input dynamic range to the original A/D converter output equivalent. Likewise the gain at any point throughout the filter can be modified if the designer desires using the gain multiplier approach.

Another form of gain that must be considered in the cascade implementation is the order in which the two-pole sections are placed. It is desirable to place the over-damped poles first in the cascade configuration followed by the under-damped poles. The reason for this requirement is that the under-damped pole pair transfer function has gain at or near the pole pair cut off frequency and thus the input dynamic range to the next cascaded section is magnified.

## OTHER CONSIDERATIONS

In addition, there are other areas the designer can investigate in detail while designing digital filters. The most notable of these is the response of the filter to internal and external noise. It is not the intent of this application note to develop the general theory of noise in digital filters since to some extent that already exists in the literature[1,2,3,4,5].

Another consideration regards the A/D converter. The dynamic range of the A/D converter is selected as required where each bit provides six db dynamic range. The variance of the quantization steps (noise) associated with the A/D converter can be shown[5] to be

$$\sigma^2 = \frac{E^2}{12} \tag{4-1}$$

where E is the quantization step. If the A/D converter is selected as having eight bits, $E^2$ has 48 db range and the quantization noise power is a factor of 12 (11 db) below this level.

Also of importance is the noise due to the multiplication truncation effect, sometimes called the "deadband" effect. Basically this noise causes the internal values within the filter to terminate prematurely. That is, the same steady-state value is not reached as could be reached if infinite-precision arithmetic is used. The easiest demonstration of this effect is to examine the actual hardware response (or computer simula-

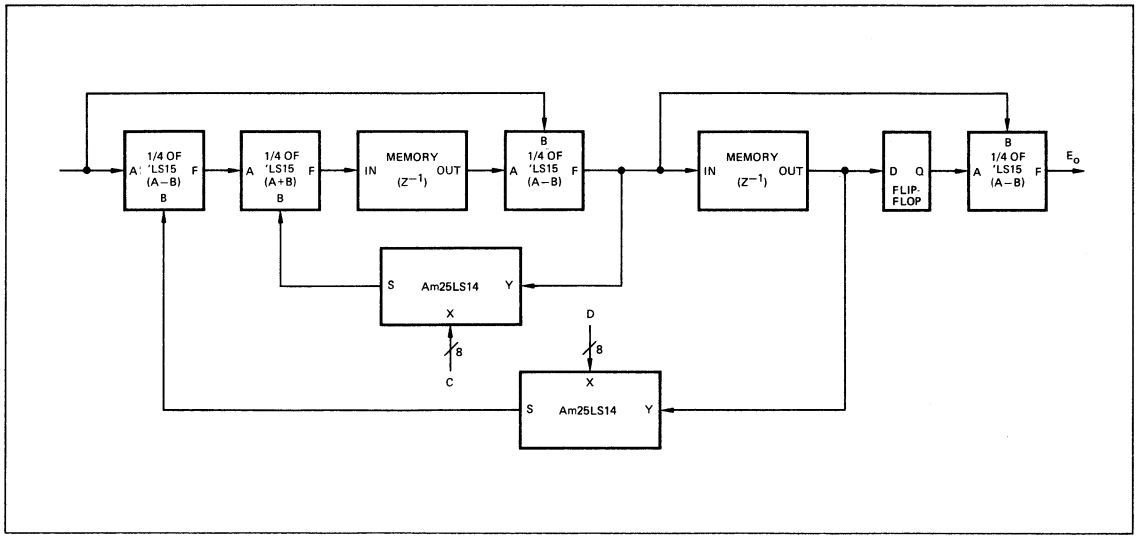


**Figure 10. Two-Pole, High-Pass Recursive Digital Filter.**

tion) of a high-pass filter to an impulse input. After several iterations the filter will "hang up" as the edge of the deadband is reached. Thus it will not decay to zero as might be expected.

Another effect which can sometimes result with a constant input is that a small steady-state oscillation can occur. Typically this behavior occurs as a low amplitude square wave with frequency of PRF/2. The cause of this oscillation is due to noise components which are introduced at the various multipliers within the filter each time the algorithm is iterated; the filter then magnifies the component at PRF/2.

These intricacies demonstrate the need for exhaustive computer simulation of the filter, once designed, to insure operation as desired. Simple Fortran math model programs that allow multiplier and memory truncation as well as A/D quantization effects to occur can quickly demonstrate the various characteristics of the filter.

## TEST EQUIPMENT

One of the most important areas the digital designer must make provision for in the design of a digital filter is the ability to test the various components of the filter (adders, multipliers etc.) after the hardware is constructed. Two techniques can be applied in this application where each gives a partial testing capability. These two techniques are static testing and dynamic testing using special purpose test equipment.

The digital filter should be designed to provide easy access to test points that contain data lines to all of the bits in a complete word. In this manner the complete word including sign is available to the special test set which contains both static readout capability and dynamic readout capability.

Provision should be made in the design to allow any dynamic memories to be replaced by static memories. Thus the digital filter can be "single stepped" such that the outputs of the multipliers and adders can be monitored on readout devices such as lamps or octal display tubes. These readouts can be checked against a computer printout of an exact simulation of the digital filter and the test set. This gives the capability of tracing any defective components or wiring errors in the equipment. Manual switches are used to enter data into the filter and then the filter "stepped along." The corresponding output states are observed to demonstrate that no deviation occurs from the computer tabulation. This is equivalent to checking either the step response or the impulse response of the filter in slow motion depending on the input switch manipulation.

In dynamic testing, digital-to-analog (D/A) converters within the test set can be plugged into the same test points as used in the static mode. The output from the D/A converter is an analog signal viewable on an oscilloscope. Thus, the operation of the filter at various points can be checked at normal operating frequencies and the results observed to determine compliance to the desired performance. In the dynamic mode, the step response, impulse response or Bode response can be determined.

It is important in working with digital filter designs to have a comprehensive test plan included as part of the design. If this is not done, it is almost impossible to "trouble-shoot" such a complex piece of equipment and the desired operation may never be completely verified.

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[1]Rader, C. M., and B. Gold, "Effects of Quantization Noise in Digital Filters," (*1966 Spring Joint Computer Conference, AFIPS Proceedings*, Vol. 28, 1966), pp. 213-219.

[2]Jackson, L. B., "On the Interaction of Roundoff Noise and Dynamic Range in Digital Filters," (*Bell System Technical Journal*, Vol. 49, No. 2, February, 1970), pp. 159-184.

[3]Knowles, J. B., and E. M. Olcayto, "Coefficient Accuracy and Digital Filter Response," (*IEEE Transactions on Circuit Theory*, Vol. CT-15, March, 1969), pp. 31-41.

[4]Koivo, A. J., "Quantization Error and Design of Digital Control Systems," (*IEEE Transactions on Automatic Control*, Vol. 1, February, 1964), pp. 55-58.

[5]Gold, B., and C. M. Rader, *Digital Processing of Signals*, (McGraw-Hill, Inc., New York, 1969), Ch. 4.

# AIRBORNE MTI RADAR- A Digital Filter Application Example

By John R. Mick

A typical non-coherent airborne MTI radar system is shown in Figure 1. This system transmits an RF pulse of width $\tau$ at a carrier frequency of $f_0$ that has a wave length $\lambda$. The receiver output is a video signal representing the echo return power of the ground patch that is defined by the antenna beam width, transmitter pulse width, and depression angle from the aircraft. This received signal contains both the fixed-target and moving-target information from each range cell. The fixed-target return is termed "clutter" since it represents the unwanted signal. The moving-target echo causes a doppler frequency envelope on the received signal and this doppler frequency is

$$f_d = \frac{2 V_r}{\lambda} \cos(\theta)$$

where

$f_d$ = doppler frequency in Hz
$V_r$ = velocity of target in m/sec
$\lambda$ = wave length of transmitted frequency in m
$\theta$ = angle between radar antenna boresight and target velocity vector

The MTI processor detects the moving-target doppler in the received video signal while rejecting the fixed-target clutter return by using a range-gated, high-pass filter. The term "range-gating" refers to the technique of applying individual segments of ground patch echo to corresponding individual high-pass filter elements. The range-gated processor can extract moving-target echos from the clutter return even if the clutter echo is 20 or 30 db greater than the moving-target echo signal.[7] The output of the MTI processor is displayed on an appropriate display such as a cathode ray tube or solid state display.

"Clutter is distinguished from receiver noise by its relatively narrow, low-frequency spectrum, which implies that these echoes are correlated from one sample to the next. Because of this property it is possible to reduce the effects of clutter with filters that reject energy at the clutter frequencies but that pass the doppler-shifted echoes from targets having higher velocities than the clutter. A processor that distinguishes moving targets from clutter by virtue of differences in their spectra is called a moving target indicator or simply MTI!"[6] The clutter spectral spread is effected by aircraft motion, antenna scanning, and radar imperfections. Radar imperfections include transmitted frequency change, amplitude modulation of the transmitted pulse, pulse width jitter, and time jitter between the trigger pulse and transmitted pulse. Also, the clutter is effected by wind effects on the surface terrain foliage such as trees and bushes.

The presence of a moving target within a range resolution cell causes an amplitude modulation of consecutive returns in that cell. A resolution cell has the width of the ground surface illuminated by the antenna azimuth beam width, and the length determined by the range resolution of the radar. After many returns, the resolution cell has an output waveform envelope defined by the moving-target doppler frequency $f_d$ described by equation 1. The output spectrum after the envelope detector in the receiver is shown in Figure 2. Here, the video spectrum for a single cell consists of a large clutter return along with a moving target return.

Because of the spurious sidebands produced by the sampling process, the clutter spectrum is imaged at all integer multiples of the sampling rate, also known as the pulse repetition frequency (PRF). Due to the envelope detection process of the intermediate frequency (IF) signal, all doppler frequencies are found to be "folded" into the positive frequency range from DC to one-half the sampling rate (PRF/2). In addition the moving-target spectrum is found on each side of the clutter spectrum at all integer multiples of the PRF.

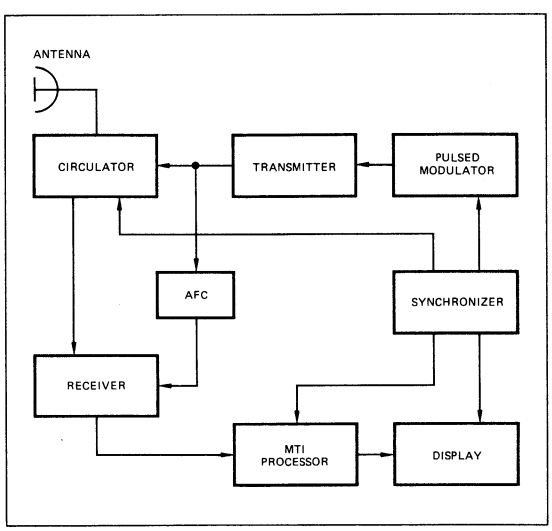


Figure 1. Typical Non-Coherent Airborne MTI Radar System.

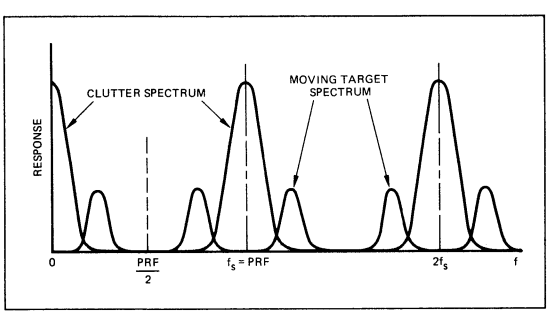


Figure 2. Receiver Output Spectrum.

## DELAY LINE CANCELLERS

Historically, the first MTI detection device used to extract the moving-target doppler echo in the presence of clutter was the delay line canceller. Usually, it consisted of an analog delay line length T = 1.0/PRF seconds and a subtractor as shown in Figure 3.

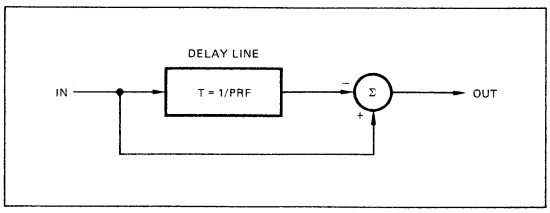


**Figure 3. Single Delay Line Canceller.**

Here, successive returns of the radar from the same range cell are subtracted resulting in an output that is equal to the pulse-to-pulse fluctuations of the radar return. Since fixed targets have a constant amplitude return, the output is zero in the ideal system. When a moving target is added, there is a variation of return amplitude from pulse to pulse as defined by the doppler frequency envelope; thus, an output related to this variation results from the delay line canceller for this range cell.

The amplitude response H(f) for the single delay line canceller is

$$|H(f)| = K|\sin(\pi Tf)|$$

where T is the sampling interval, f is the input frequency, and K is a gain constant. Thus the delay line canceller has a transfer response that is a function of the inter-pulse period and is zero at DC and integer multiples of the PRF as shown in Figure 4.

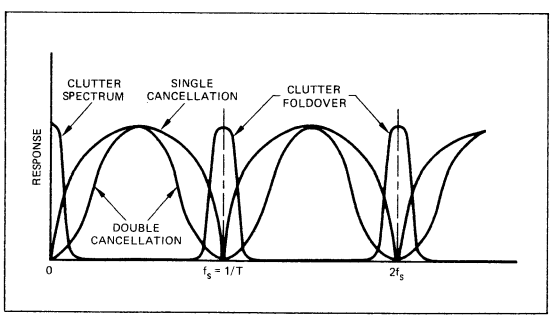


**Figure 4. Frequency Response of Single-Delay-Line Canceller and Double-Delay-Line Canceller.**

A double delay line canceller can be used to increase the clutter rejection of an MTI system. Figure 5 shows two equivalent forms of a double delay line canceller. The $z^{-1}$ notation is the unit delay operator and refers to a delay equal to one interpulse period of the radar. Each canceller has the transfer function

$$\frac{E_o}{E_i} = (z^{-1}-1)^2 = \frac{(z-1)^2}{z^2}$$

The amplitude response for these cancellers is

$$|H(f)| = K_1 |\sin^2(\pi fT)|$$

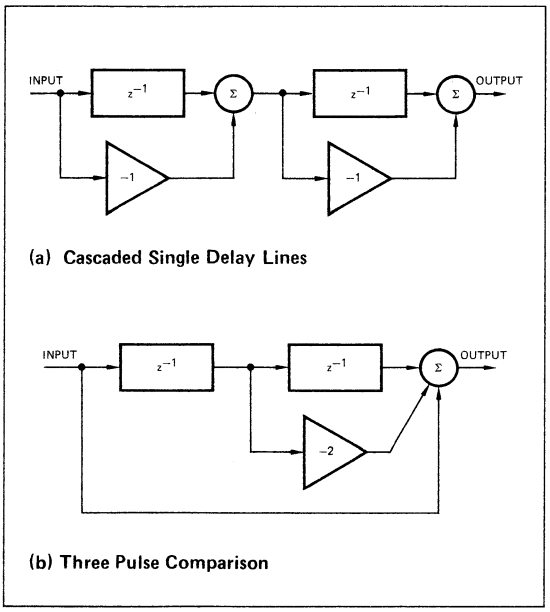


**Figure 5. Double Delay Line Canceller.**

As is seen, the double delay line canceller has a sine-squared response rather than the sine response of a single delay line canceller as shown in Figure 4. As a result, a greater attenuation of the clutter spectrum is realized. It is possible in theory to combine three, four or more delay lines in various configurations to give multiple zeros at the origin in the s-plane. However, these become very difficult to implement since very slight changes in delay time cause significant reductions in cancellation. Even the double delay line canceller is difficult to implement reliably.

## ANALOG RANGE-GATE FILTER

The analog range-gated filter represents a more sophisticated radar technique for separating moving target returns from fixed target returns by detection of the doppler shift in frequency due to the target motion. The combinations of a moving target or targets with a larger fixed target within a resolution cell causes an amplitude modulation of consecutive returns from that cell.[7]

A block diagram of a simple analog range-gated filter is shown in Figure 6. Here input switch $S_1$ and output switch $S_1$ are closed simultaneously for a period equal to the radar pulse width $\tau$.

This causes the radar echo return for the range cell to be stored on capacitor $C_1$. The final voltage on $C_1$ each time switch $S_1$ closes, is equal to the instantaneous value of the radar video input at the end of each sampling interval $\tau$. Therefore, the input switch and capacitor form a zero order hold circuit. After input switch $S_1$ is opened, the analog voltage equal to the return echo will remain as an input to filter number one. At the same time, the output switch $S_1$ applies the present output of the filter to the output line.

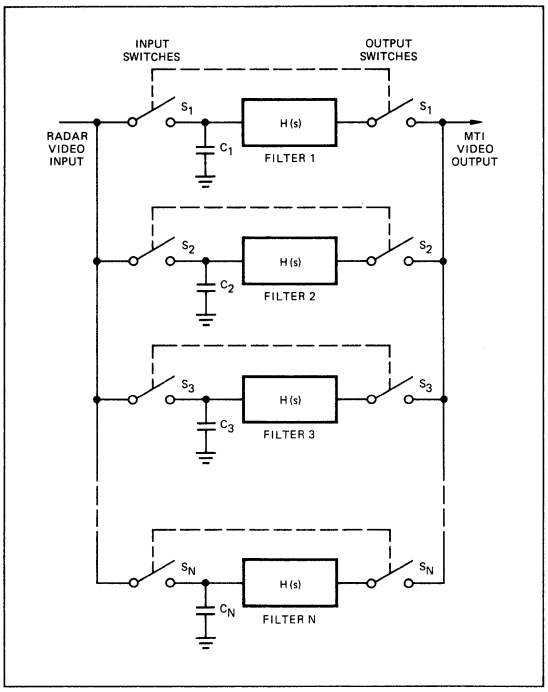


**Figure 6. Simple Analog Range-Gated Filter.**

At the instant switches $S_1$ are opened, switches $S_2$ are closed for $\tau$ seconds and action similar to that described above takes place. Likewise, when switches $S_2$ are opened, switches $S_3$ are closed and this continues sequentially until switches $S_N$ are activated.

As is seen, each filter element receives radar echo return from successive range cells approximately equivalent of $c\tau/2$ in range since a two-way trip is required for the radar energy and where c equals the speed of light. Thus each analog filter is gated to receive a small range patch of radar echo return; thereby, the name analog range-gated filter is derived.

One important aspect of this type of MTI system is that since the filters are time multiplexed, the resolution cells are essentially independent. However successive returns are highly correlated since they represent echoes from essentially the same ground patch. The filter element used to extract the moving target doppler is designed to provide a very sharp rejection of the clutter spectrum while providing near uniform gain to the widest possible band of frequencies containing moving target echoes. This is accomplished with a sharp cut-off high-pass filter, usually with at least 24 db per octave attenuation. The amplitude response of the filter in one element of a range-gated filter is shown in Figure 7 and is compared with the response of a single delay line canceller.

There are many variations that can be derived from the basic analog range-gated filter shown in Figure 6. These include input and output multiplexing schemes to reduce switching speed requirements, various analog filter cut-off frequency control techniques to allow the widest possible acceptance band for moving target frequencies as determined by the spectral spread of the clutter return, etc. Each configuration is still basically a device to separate the moving-target signal spectrum from the fixed-target signal spectrum.

## DIGITAL RANGE-GATED PROCESSOR

A digital range-gated processor is a highly sophisticated radar technique for extracting moving target echoes. The digital range-gated filter performs the identical function as the analog range-gated filter; however, the hardware implementation of the two types of filters is notably different.

A block diagram of a simple digital range-gated processor is shown in Figure 8. Here input switch $S_1$ is closed for $\tau$ seconds to store the final instantaneous value of the radar return echo voltage for the first range cell on capacitor $C_1$. When switch $S_1$ is opened switches $S_2$ and $S_3$ are closed. The second range cell video return is stored on capacitor $C_2$. Thus, switches $S_1$ and $S_3$ along with capacitors $C_1$ and $C_2$ provide two first order hold circuits. Meanwhile switch $S_2$ applies the voltage on $C_1$ to the analog-to-digital (A/D) converter. In the A/D converter the analog voltage is quantitized to a binary number representation. After $\tau$ seconds, $S_2$ and $S_3$ are opened and $S_1$ and $S_4$ are closed resulting in similar action. This process of alternating the $S_1$, $S_4$ pair and the $S_2$, $S_3$ pair continues until the desired range is covered by the processor and each resolution cell echo return in quantized.

The binary output from the A/D converter is applied to the digital filter which, in effect, consists of N individual filters as in the previous analog example. Here, however, the arithmetic circuitry is implemented only once and is time shared among all filter elements in the processor. This is easily achieved since the individual filters operate sequentially. The output of each individual filter element is applied sequentially to the digital-to-analog (D/A) converter resulting in a continuous video MTI output synchronous in range with the radar video input.

One of the key advantages of the digital filter is that the arithmetic operations are all handled by the same hardware for each filter cell. This means each individual filter element has exactly the same transfer function. That is, each has exactly the same mid-band gain, cut-off frequency, and attenuation. In the case of individual analog filters, amplifier gains tend to differ and component values vary initially as well as with temperature and age.

A digital memory word is required for each pole of each cell in the range-gated processor and no sharing is possible. The analog equivalent of this is the storage supplied by capacitors and inductors, since these are the components that provide the terms (sL and 1/sC) associated with the poles in the Laplace transfer function. Many additional advantages of the digital filter approach to MTI radar exist. These will become apparent as the design criteria are examined in more detail.

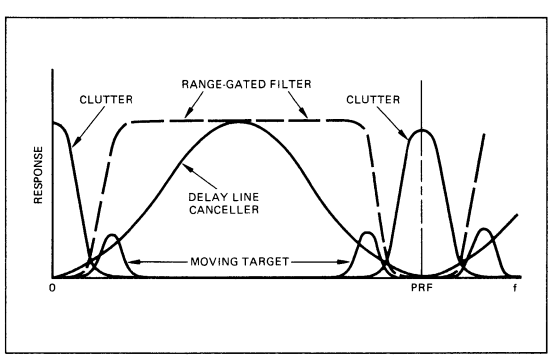


**Figure 7. Spectral Response of Filter Element.**

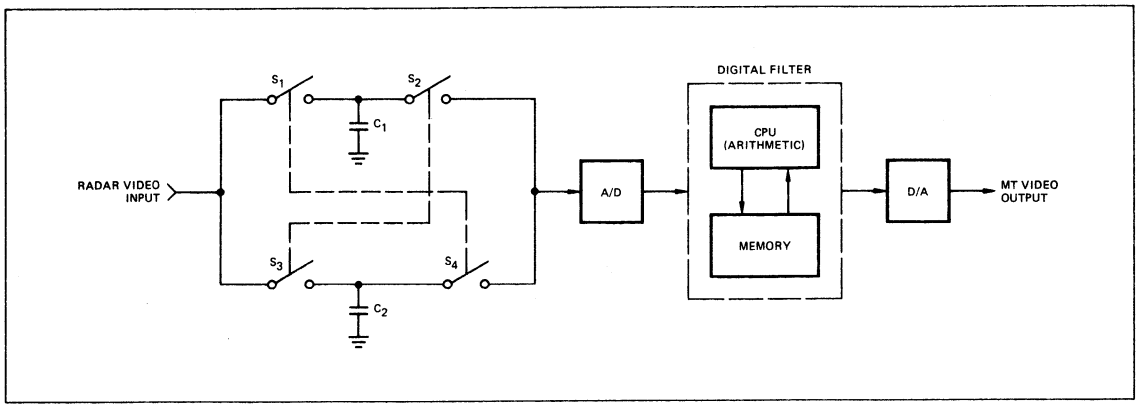


**Figure 8. Simple Digital Range-Gated Processor.**

## SUMMARY

Chronologically the delay line cancellers were the first MTI detection devices for pulse-doppler radar systems. An improvement in detectability was added to the system by the use of the analog range-gated filter. This improvement is related to the sharper filter cut-off characteristic which increases the rejection to clutter. Likewise, additional canceller gain is supplied to the doppler signal from slower moving targets. The most recent improvement in MTI radar processors is a result of the digital implementation of the range-gated processor. The improvement is provided by several features inherent in the digital filter design. These include: the uniform gain provided by all cells of the processor, the ability to move the cut-off frequency to various points near the clutter spectrum, the freedom from variations due to parts aging, and the reduced size and power afforded by arithmetic time sharing.

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# Understanding Booth's Algorithm in 2's Complement Digital Multiplication

By John R. Mick

## INTRODUCTION

At the present time, digital machines perform multiplication using either serial techniques, serial-parallel techniques, or all-parallel techniques. The multiplication speeds can be very slow to very fast depending on the exact hardware implementation used and the hardware constraints imposed.

The Am25LS14 can be used to perform multiplication of 2's complement numbers with a minimum of hardware. The The new Am25LS14 provides the capability to perform very high speed direct hardware multiplications and is especially suited for real-time digital processing applications. This device will find applications in minicomputers, recursive or non-recursive digital filters, Fast Fourier Transform processors, adaptive digital integrators and many other digital implementations of special arithmetic algorithms.

## MULTIPLICATION DEFINITION

According to Webster's Dictionary, multiplication is "a mathematical operation that at its simplest is an abbreviated process of adding an integer to itself a specified number of times and that is extended to other numbers in accordance with laws that are valid for integers." This definition is particularly appropriate for binary numbers in that all hardware binary multiplication schemes make an "add" or "no-add" decision and maintain the "weighting" rules of binary numbers. The two numbers involved in the operation are usually called the multiplicand (the number to be multiplied) and the multiplier (the number that multiplies) with the result being called the product (later in this application note the partial products or partial sums will be important).

Binary multiplication is performed as in the following four digit example. The terms X and Y are:

$$X = x_0(2^0) + x_1(2^1) + x_2(2^2) + x_3(2^3)$$
$$X = x_0(1) + x_1(2) + x_2(4) + x_3(8)$$
$$Y = y_0(1) + y_1(2) + y_2(4) + y_3(8)$$

where $x_i$ and $y_i$ can assume a "0" or "1" value for i = 0, 1, 2 or 3.

If X is the multiplicand and Y is the multiplier, the product S of X·Y is

$$\begin{aligned} S = X \cdot Y = {} & y_0(1)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_1(2)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_2(4)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_3(8)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \end{aligned}$$

In the above example, it can be seen that three additions are required to generate the product S of X·Y; the first two of these are usually called partial products or partial sums. In order to examine the weighting of the binary numbers in the above example, the complete partial product solution is shown in Figure 1 and the weights of the x terms and y terms have been combined.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Multiplicand | $x_3$ (8) + | $x_2$ (4) + | $x_1$ (2) + | $x_0$ (1) |
| | | | | Multiplier | $y_3$ (8) + | $y_2$ (4) + | $y_1$ (2) + | $y_0$ (1) |
| | | | | | $x_3y_0$ (8) + | $x_2y_0$ (4) + | $x_1y_0$ (2) + | $x_0y_0$ (1) |
| | | | | $x_3y_1$ (16) + | $x_2y_1$ (8) + | $x_1y_1$ (4) + | $x_0y_1$ (2) | |
| | | Carry (32) + | $Ps_4$ (16) + | $Ps_3$ (8) + | $Ps_2$ (4) + | $Ps_1$ (2) + | $Ps_0$ (1) | |
| | | $x_3y_2$ (32) + | $x_2y_2$ (16) + | $x_1y_2$ (8) + | $x_0y_2$ (4) | | | |
| Carry (64) + | $Ps_5$ (32) + | $Ps_4$ (16) + | $Ps_3$ (8) + | $Ps_2$ (4) + | $Ps_1$ (2) + | $Ps_0$ (1) | | |
| $x_3y_3$ (64) + | $x_2y_3$ (32) + | $x_1y_3$ (16) + | $x_0y_3$ (8) | | | | | |
| $s_7$(128) + $s_6$(64) + | $s_5$(32) + | $s_4$(16) + | $s_3$(8) + | $s_2$(4) + | $s_1$(2) + | $s_0$(1) | | |

Figure 1. Multiplication of Two Unsigned 4-bit Numbers X and Y.

5

The $s_7$(128) term represents the carry out of the final summation. As is seen, the multiplication of two 4-bit unsigned words results in an 8-bit product. This can be extended to a general statement; that is, the multiplication of a m-bit unsigned number with a n-bit unsigned number gives a m + n bit resultant unsigned product. This number may be truncated of course and rules will be given later for determining the resulting accuracy when the hardware is being reduced.

It should be recognized that the product terms associated with $y_0$ and $y_1$ can be added in one adder and the product terms associated with $y_2$ and $y_3$ can be added in a second adder at the same time; thereby giving two partial products after one adder propagation delay time. These two partial sums can then be added in a third adder to give the resultant product of the multiplication.

One technique for reducing multiplication time that is presently being used in serial and serial-parallel multipliers is to ignore addition when the multiplier bit is a logic "0." When this is done the number of terms to be added is equal to the number of 1's in the multiplier word. This method can be extended in such a way that strings of 1's can also be ignored—this leads to an important new technique for performing high speed multiplication. This technique will be discussed in greater detail later.

| Two's Complement | | | | Decimal Number |
|---|---|---|---|---|
| Sign bit $-2^3$ | $2^2$ | $2^1$ | $2^0$ | |
| −8 | 4 | 2 | 1 | |
| 0 | 1 | 1 | 1 | +7 |
| 0 | 1 | 1 | 0 | +6 |
| 0 | 1 | 0 | 1 | +5 |
| 0 | 1 | 0 | 0 | +4 |
| 0 | 0 | 1 | 1 | +3 |
| 0 | 0 | 1 | 0 | +2 |
| 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | −1 |
| 1 | 1 | 1 | 0 | −2 |
| 1 | 1 | 0 | 1 | −3 |
| 1 | 1 | 0 | 0 | −4 |
| 1 | 0 | 1 | 1 | −5 |
| 1 | 0 | 1 | 0 | −6 |
| 1 | 0 | 0 | 1 | −7 |
| 1 | 0 | 0 | 0 | −8 |

Figure 2. Full Definition of a 4-bit Two's Complement Binary Number.

## TWO'S COMPLEMENT NOTATION

This section is presented as a quick review of the two's complement numbering system and is intended to give insight for the designer not familiar with two's complement notation. The two's complement numbering system is a technique for describing positive and negative numbers in a convenient notation. When contrasted with other numbering systems such as sign-magnitude and one's complement, it has the advantage of only having one representation for the number "zero." Also, two's complement numbers can be added or subtracted without concern for the sign of each number as the result will be correct in two's complement notation.

In 2's complement notation, the sign bit is a logical "0" for positive numbers and a logical "1" for negative numbers. Four bits may be used to represent the numbers +7 to −8 as shown in Figure 2. Notice that the sign bit does carry magnitude information that has a negative value.

From this example, it is readily apparent that the magnitude of the negative numbers is not represented by its associated magnitude bits if the sign bit is ignored as is the case for the positive numbers. One way to find the absolute magnitude of a negative 2's complement number is to invert all bits and add plus binary one as in the example below:

| | |
|---|---|
| 1011 | Negative 2's complement number |
| 0100 | Inverted |
| + 0001 | One Added |
| 0101 | Result |

From this example, it is seen that the magnitude of this negative numbers is five.

Likewise, to form a negative 2's complement number, the positive representation is taken, inverted, and plus binary one is added as shown.

| | |
|---|---|
| Positive number +3 | |
| Binary representation | 0011 |
| Inverted | 1100 |
| One added | + 0001 |
| Minus three in two's complement | 1101 |

The advantage of two's complement in many computers and digital processors is that addition and subtraction can be performed without regard to whether the numbers being added or subtracted are positive or negative. Examples of addition are shown in Figure 3. Note that overflows are discarded.

| | | | | | |
|---|---|---|---|---|---|
| 0001 | +1 | 0001 | +1 | 1110 | −2 |
| 0101 | +5 | 1111 | −1 | 0110 | +6 |
| 0110 | +6 | (1) 0000 | 0 | (1) 0100 | +4 |
| 0110 | +6 | 1010 | −6 | 1110 | −2 |
| 1110 | −2 | 0011 | +3 | 1101 | −3 |
| (1) 0100 | +4 | 1101 | −3 | (1) 1011 | −5 |

Figure 3. Examples of Two's Complement Addition.

Subtraction is much like addition except that the number being subtracted (subtrahend) must be inverted and have one added to its value. It is then added to the minuend. This addition of +1 represents no problem in the hardware because the carry in ($c_n$) of the least significant adder can be used for this purpose — not an additional adder. Figure 4 shows examples of subtraction.

| | | | | |
|---|---|---|---|---|
| Minuend | 0001 +1 | 1110 −2 | 1110 −2 | 1010 −6 |
| Subtrahend | 0101 +5 | 0110 +6 | 1101 −3 | 1101 −3 |
| Minuend | 0001 | 1110 | 1110 | 1010 |
| Inverted Subtrahend | 1010 | 1001 | 0010 | 0010 |
| Add | 1011 | 0111 | 0000 | 1100 |
| Add One | 0001 | 0001 | 0001 | 0001 |
| Result (Binary) | 1100 | 1000 | 0001 | 1101 |
| Result (Decimal) | −4 | −8 | +1 | −3 |

**Figure 4. Examples of Two's Complement Subtraction.**

From these examples, one might conclude that multiplication is simply the product of one 2's complement number with the other. Unfortunately, this is not correct for negative numbers. One obvious technique for multiplication in which negative numbers are represented by 2's complements is to determine the signs and magnitudes of the operands, multiply the magnitudes, and then if the result is negative, cast the result into 2's complement form. It seems preferable, however, to devise a scheme for multiplying such numbers more simply. Booth's method will be considered for this purpose.

## BOOTH'S ALGORITHM

In the usual methods of digital multiplication, the multiplier digits are examined in turn and when the multiplier digit is a logical "1," the multiplicand is added to the running partial sum in the appropriate weight. For each multiplier digit, there is a relative one-digit shift between the multiplicand and partial sum whether there has been an addition or not. Booth's algorithm provides a tool whereby more than one shift at a time may be made, depending on the grouping of strings of logic 1's or logic 0's. This multiple shifting ability may be used to "speed up" the multiplication process.

Ordinary multiplication (disregarding signed numbers) can be performed by summing a series of partial products, each of which is one bit of the multiplier word, Y, times the entire multiplicand word, X, times the weight of the Y multiplier bit. That is,

$$\pi = \sum_{i=0}^{n-1} y_i \cdot X \cdot 2^i$$

where n = number of bits in Y

This method, usually designated "add and shift", is simply performed by ANDing the i-th multiplier bit, $y_i$, with the X value giving a result of X or 0, and then adding this result (X or 0) to the present partial product to generate a new partial product. The new partial product is then shifted one place toward the LSB. This divides it by 2 or, effectively, multiplies X by 2 relative to the partial product. The process is then repeated for the next more significant bit of Y. This algorithm will work for 2's complement values of Y if for the most significant bit of Y, the sign bit, a subtraction rather than addition is performed. This results because the MSB of a 2's complement number effectively carries a negative rather than positive weight as shown in the following Y definition.

$$Y = -y_{n-1}(2^{n-1}) + y_{n-2}(2^{n-2}) + y_{n-3}(2^{n-3}) + \ldots + y_0(2^0)$$

Booth's algorithm is a multiplication technique which can reduce the number of operations required for multiplication. It operates on the fact that a string of 0's in the multiplier requires no additions but just shifting, and a string of 1's in the multiplier running from bit weight $2^r$ to weight $2^s$ can be treated as $2^{s+1}-2^r$. For example, if Y = 001110 (LSB on right), then r = 1 and s = 3 and $2^4-2^1 = 14$. While the add and shift algorithm for this example requires three additions (if additions are ignored for $Y_i = 0$), Booth's algorithm requires only two operations. These are an addition at weight $2^{s+1}$ and a subtraction at weight $2^r$. The algorithm can be verbally stated as follows:

- Examine the multiplier bit by bit beginning with the least significant bit and shifting the partial product relative to the multiplicand as each bit is examined.
- Subtract the multiplicand from the partial product when you find the first 1 in a string of 1's, add the multiplicand to the partial product when you find the first 0 in a string of 0's and do nothing when the bit is identical to the previous multiplier bit.

The significant features of this algorithm are that:

1. It can require n operations (compare, add/subtract, shift) for an n bit multiplier (of alternating 0's and 1's) but it usually requires fewer of these and the remainder are of the type compare, shift operations.
2. It works for X in 2's complement because addition and subtraction logic are identical for unsigned and 2's complement numbers.
3. It works for Y in 2's complement directly, because if Y ends in a string of 1's, the last operation will be a subtraction at the appropriate weight.

The basic algorithm as developed by Booth is as follows: $y_i$ is the i-th most significant bit of an n-bit multiplier representation. $y_{-1}$ is zero. $y_0$ is the least significant bit. $y_{n-1}$ is the sign bit. X is the multiplicand.

Starting with i = 0, $y_i$ and $y_{i-1}$ are compared:

1.) If $y_i = y_{i-1}$; add 0X.

2.) If $y_i = 1$ and $y_{i-1} = 0$; subtract 1X (the multiplicand) from the partial product. (Add the 2's complement).

3.) If $y_i = 0$ and $y_{i-1} = 1$; add 1X to the partial product.

Two examples of this rules are shown in Figure 5.

**Example 1:**

```
1  0 1 1 1      = −9
0  1 0 1 1 (0)  = +11
-------------------------------------------
0  0 0 0 0 1 0 0 1        y0 = 1   y−1 = 0
0  0 0 0 0 0 0 0          y1 = 1   y0  = 1
1  1 1 0 1 1 1            y2 = 0   y1  = 1
0  0 1 0 0 1              y3 = 1   y2  = 0
1  0 1 1 1                y4 = 0   y3  = 1
-------------------------------------------
(1) 1  1 0 0 1 1 1 0 1    = −99
```

**Example 2:**

```
1  1 0 1 1      = −5
1  1 0 0 1 (0)  = −7
-------------------------------------------
0  0 0 0 0 0 1 0 1        y0 = 1   y−1 = 0
1  1 1 1 1 0 1 1          y1 = 0   y0  = 1
0  0 0 0 0 0 0            y2 = 0   y1  = 0
0  0 0 1 0 1              y3 = 1   y2  = 0
0  0 0 0 0                y4 = 1   y3  = 1
-------------------------------------------
(1) 0  0 0 1 0 0 0 1 1    = +35
```

**Figure 5. Examples of Booth's Algorithm for Two's Complement Multiplication.**

Based on these rules as developed by Booth, it is a straight forward process to make a table of desired action for each of the four possible two-bit combinations under inspection. This is shown below. K is the partial product before this level of the algorithm and is zero initially.

**Table of Operation for Booth's Algorithm**

| $y_{i-1}$ | $y_i$ | Function | Partial Product |
|---|---|---|---|
| 0 | 0 | Do nothing | K + 0 |
| 1 | 0 | Add X | K + X |
| 0 | 1 | Subtract X | K − X |
| 1 | 1 | Do nothing | K + 0 = K − 0 |

Note that when $y_i = 0$ and add is required and when $y_i = 1$ a subtract is used. Also, when $y_i \oplus y_{i-1} = 1$ the multiplicand is added (or subtracted) fromt eh running partial product K and when $y_i \oplus y_{i-1} = 0$, zero is used.

## INTEGER MULTIPLICATION

We can multiply 2's complement numbers in either integer or fractional form. The primary difference is in the thought process of the designer. When the binary patterns are treated as integers, the 2's complement numbers can be represented as

$$X = x - x_s 2^{n-1}$$
$$Y = y - y_s 2^{m-1}$$

where

$x_s$ = sigh bit of X (one or zero)
$y_s$ = sign bit of Y (one or zero)
x = magnitude bits of X (less sign)
y = magnitude bits of Y (less sign)
n = number of bits in X word
m = number of bits in Y word

For example, if six bits are assumed for X, n = 6 and the sign bit has a weight of $-2^{6-1} = -2^5 = -32$. The other magnitude bits have their normal weight and since there are five other magnitude bits, they are $2^0$, $2^1$, $2^2$, $2^3$, and $2^4$. Thus, 2's complement integer numbers for n = 6 bits are as shown below:

| Integer Decimal Number Equivalent | Sign $-2^5$ | Magnitude bits $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|---|---|
| | −32 | 16 | 8 | 4 | 2 | 1 |
| 14 | 0 | 0 | 1 | 1 | 1 | 0 |
| 31 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| −7 | 1 | 1 | 1 | 0 | 0 | 1 |
| −25 | 1 | 0 | 0 | 1 | 1 | 1 |
| −32 | 1 | 0 | 0 | 0 | 0 | 0 |

When the product of X and Y is considered, the following equation results:

$$S = XY = x_s y_s 2^{m+n-2} - x y_s 2^{m-1} - y x_s 2^{n-1} + xy$$

The 2's complement product requires m + n bits in order to represent all possibilities. Note that there is only one condition where the m + n bits are required; that condition being:

$$X = -2^{n-1} \text{ and } Y = -2^{m-1}$$

This condition gives $S = XY = 2^{m+n-2}$ which requires m + n digits in a 2's complement signed integer number.

Consider n = 6 and m = 4, then $x_s$ has weight −32 and $y_s$ has weight −8. For X = −32 and Y = −8, the product XY is +256. The 2's complement representation is 0100000000. Ten bits are required to properly represent the 2's complement number. All other combinations of values for X and Y require only m + n −1 bits to represent the 2's complement number. For n = 6 and m = 4 in this case, the ninth bit represents the product sign. Consider (+7) x (−31) is equal to −217 or 100100111. Notice that 1100100111, the ten bit 2's complement representation is identical in value.

The *general* requirement for the product solution of XY is:

$$S = XY = s - s_s 2^{m+n-1}$$

and all binary operations must be carried through m + n bits in the product soltuion unless a simplification is assumed.

## FRACTIONAL MULTIPLICATION

Fractional multiplication is identical with integer multiplication but the notation is changed. The fractional number range is usually limited to $-1 \leqslant X \leqslant 1-2^{-(n-1)}$.

The fractional 2's complement binary numbers can be represented as:

$$X = x\ 2^{-(n-1)} - x_s$$
$$Y = y\ 2^{-(m-1)} - y_s$$
$$K = k\ 2^{-(p-1)} - k_s$$

where the notation is as with integer arithmetic. The sign bit now has a weight of $-2^0 = -1$ and the other magnitude bits have their normal fractional weight.

Two's complement numbers for n = 6 are as shown below.

| Fractional Equivalent | $-2^0$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ |
|---|---|---|---|---|---|---|
| | −1 | 1/2 | 1/4 | 1/8 | 1/16 | 1/32 |
| 14/32 = 7/16 | 0 | 0 | 1 | 1 | 1 | 0 |
| 31/32 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| −7/32 | 1 | 1 | 1 | 0 | 0 | 1 |
| −25/32 | 1 | 0 | 0 | 1 | 1 | 1 |
| −32/32 = −1 | 1 | 0 | 0 | 0 | 0 | 0 |

The notation difference in the fractional representation is that all the integer representations have been divided by $2^{(n-1)}$.

The fractional product XY is

$$S = XY = x_s y_s - x_s y\ 2^{-(m-1)} - y_s \times 2^{-(n-1)} + xy\ 2^{-(m+n-2)}$$

Again, m+n bits are required to cover all possible combinations. Note that X = −1 and Y = −1 results in XY = +1 which is beyond the normal range. In order to cover this possibility, the sign bit should be given a weight of −2 (instead of −1); the next most significant bit is weight +1, the next is +1/2, and so forth. If the −1 times −1 possibility is excluded only m+n−1 bits are required.

This general equation requires the sign bit to have a weight of −2 and all arithmetic to be carried to m+n bits to represent the two's complement solution.

# A HIGH-SPEED SERIAL/PARALLEL MULTIPLIER THE Am25LS14*

By John Mick, John Springer and Clive Ghest

## INTRODUCTION

The Am25LS14 is a complete 8-bit Serial/Parallel Multiplier fabricated as a single 16-pin LSI chip. The device accepts a parallel two's complement or unsigned multiplicand and multiplies it by any arbitrary length serial two's complement or unsigned multiplier. The resulting product is a correct and complete serial two's complement or unsigned product. The complete product of an 8 x 8 multiplication can be performed in 16 clock cycles. Any number of Am25LS14 devices can be cascaded with no additional logic, so that the parallel multiplicand can be easily expanded to any number of bits. Mixed signed (two's complement) and unsigned multiplication is possible, generating a product in signed two's-complement form.

## MULTIPLIER CHARACTERISTICS

The requirements for a good general purpose IC multiplier for use in a wide range of commercial applications are as follows:

- It should be inexpensive
- It should be fast
- It should be easy to use
- It should be adaptable to any word length
- It should handle signed numbers in two's complement notation without correction.

The first two of these requirements tend to be incompatible and in the past have required two types of circuits: one which was designed to be as fast as possible and another which compromised speed for cost. The last two requirements limit the method used to perform the multiplication to an algorithm which works in two's complement notation and is the same for all bits, so that the "sign bit" is treated identically with the other bits.

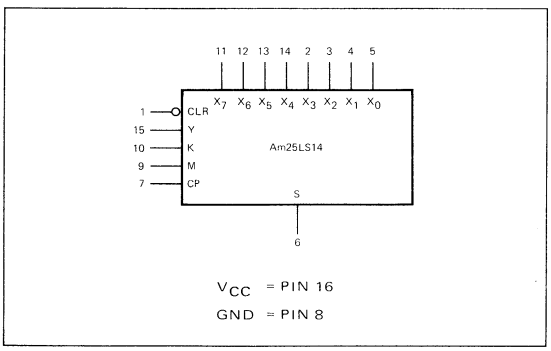



**Figure 2. Logic Symbol for the Am25LS14 (16-Pin Device)**

The Am25LS14 offers an optimum solution to these requirements. It operates by taking the whole multiplicand in parallel and utilizing a single bit at a time of the multiplier word to form partial products in an internal register. The output is a serial bit stream representing the product of the parallel multiplicand word and the serial multiplier word.

## THE LOGIC FUNCTION

A simplified logic diagram of the Am25LS14 Serial/Parallel multiplier is shown in Figure 1 and the 16-pin logic symbol for the device is shown in Figure 2. The multiplier consists of four basic parts; a storage register used to hold the multiplicand word during the multiplication, the adder/subtractor logic containing both a partial product register and a carry/borrow register, a flip-flop and exclusive-NOR gate operating on the serial multiplier string presented at the Y input to provide a

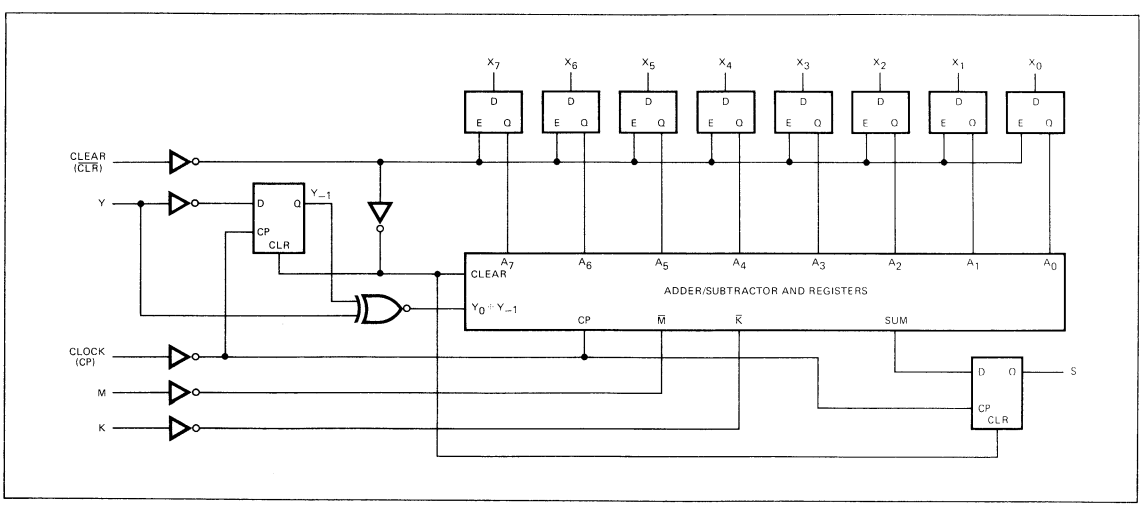



**Figure 1. Functional Logic Diagram for the Am25LS14**

*The Am25LS14 is manufactured under U. S. Patent No. 3,878,985 issued April 22, 1975.

control signal to the adder/subtractor logic, and a logic mode circuit to alter the multiplicand from two's complement to unsigned notation as controlled by the M input. The adder/subtractor logic and product and carry/borrow register is iterative; that is, it consists of eight identical cells with a small change in the eighth cell to efficiently incorporate the multiplicand word sign logic. For a detailed description of the logic design of the Serial/Parallel multiplier, refer to the application note "Mechanization of the Serial/Parallel Multiplier" by John R. Mick.

Prior to a multiplication, the internal multiplier sum and carry registers are reset by applying a LOW to the clear input. The 8-bit multiplicand data is applied to the X inputs and is latched into the multiplicand register as the clear input goes HIGH. This internal multiplicand storage is useful because the multiplicand need not be held constant during the multiplication allowing these inputs to be bus organized. The Serial/Parallel multiplier is now ready to receive the first least significant multiplier bit. The least significant bit of the multiplier word is presented at the Y serial input and when the clock changes from LOW to HIGH, the multiplier produces the first least significant product bit at the serial data output, S. In each succeeding clock period, the next more significant multiplier bit is presented at the Y input and the next more significant product bit is present at the S output. After 8 clock periods, the multiplier serial input string has been exhausted but the most significant half of the product is still in the internal registers of the Am25LS14 Serial/Parallel multiplier and must be clocked out. If the multiplier is an unsigned word, then during the extraction of the most significant half of the product, the multiplier Y input must be held at logic zero. If, however, the multiplier is a two's-complement signed word, then the most significant bit (sign bit) of the multiplier word must be repeated at the Y input until the complete product has been obtained. The multiplicand can be either an unsigned number or a two's-complement number depending upon the logic polarity of the mode input, M. This mode input should be held at a LOW logic level (ground) if the multiplicand is in two's-complement notation and the $X_7$ input is a two's complement sign bit, and it should be held at a HIGH logic level (pulled up through a register to $V_{CC}$) if the 8-bit multiplicand is unsigned (magnitude only number).

The K input is used for expansion purposes. To increase the length of the multiplicand word by using multiple devices, the S output of a higher order device is connected to the K input of the next lower order devices. The clear lines are connected together and the clock lines are connected together. All the mode inputs except the one on the most significant device are held at a HIGH logic level. Whether the multiplicand is signed or unsigned is determined only by the M input of the most significant device. A 24-bit by n-bit multiplier is shown in Figure 3. The K input is held LOW at the most significant device indicating a two's complement multiplicand. The multiplier input can be any length, with n + 24 clock periods required for the multiplication. The resulting product is n + 24 bits long.

If the multiplicand is not an even multiple of 8 bits, then for an unsigned multiplicand the remaining most significant multiplicand inputs are held LOW at logic zero, while for a two's-complement multiplicand, the remaining multiplicand inputs must be connected to the multiplicand sign bit so that the sign is extended and can be interpreted correctly. Figure 4 shows a 12 x n Serial/Parallel multiplier connection for a two's-complement signed multiplicand. The resulting product is n + 12 bits long and only n + 12 clock periods are required to generate the correct product.

The Function Table for the Am25LS14 multiplier operation is given in Figure 5. As shown, the K input is the sum expansion input and allows for the cascading of devices. The mode input, M, is used in conjuction with cascading to determine the most significant bit of the multiplicand and controls the multiplicand sign definition.

## TIMING

Although the Serial/Parallel multiplier requires only m + n clock periods to produce a full length product, (where m is the multiplicand word length and n is the multiplier word length) a practical system may use two additional clock periods. The first additional clock period is used to reset the multiplier at the beginning of a multiplication by using the clear input. This is shown in the timing diagram of Figure 6. This clears the partial product register, the carry/borrow register and the

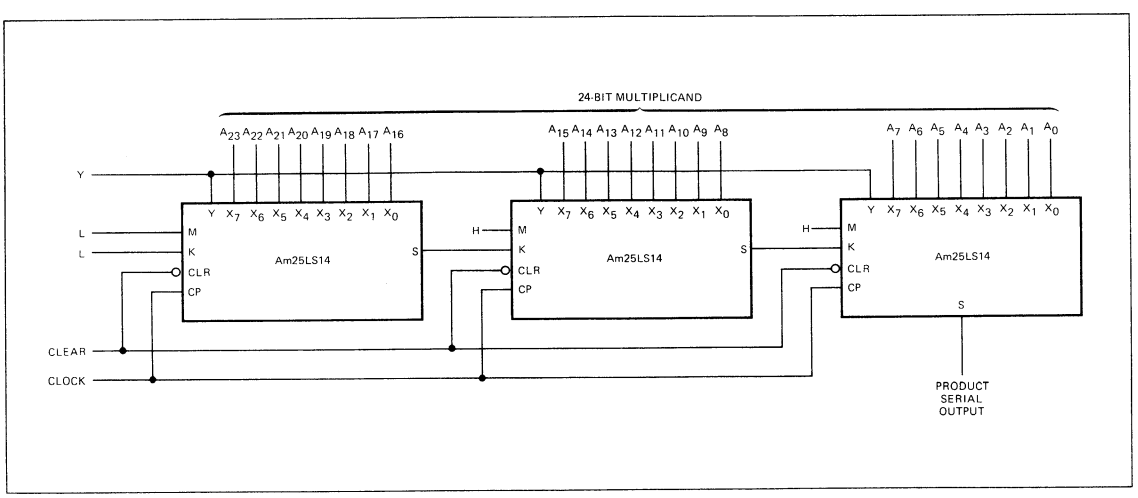



**Figure 3. Three Am25LS14's Cascaded to Make a 1-Bit by 24-Bit Serial-Parallel Multiplier**

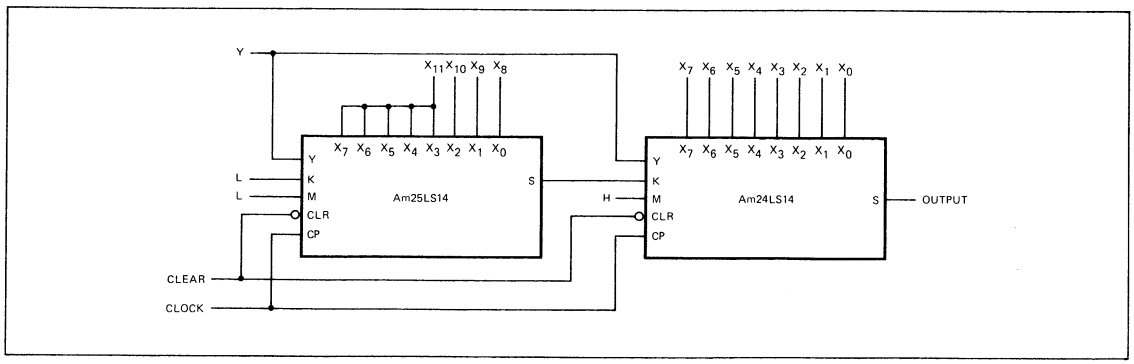



**Figure 4. A 12-Bit by N-Bit Two's Complement Multiplier Using Two Am25LS14's**

| INPUTS | | | | | | INTERNAL | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CP | K | M | $X_i$ | Y | $Y_{-1}$ | S | |
| – | – | L | L | – | – | – | – | Most Significant Multiplier Device |
| – | – | CS | H | – | – | – | – | Devices Cascaded in Multiplier String |
| L | – | – | – | OP | – | L | L | Load New Multiplicand and Clear Internal Sum and Carry Registers |
| H | – | – | – | – | – | – | – | Device Enabled |
| H | ↑ | – | – | – | L | L | AR | Shift Sum Register |
| H | ↑ | – | – | – | L | H | AR | Add Multiplicand to Sum Register and Shift |
| H | ↑ | – | – | – | H | L | AR | Subtract Multiplicand from Sum Register and Shift |
| H | ↑ | – | – | – | H | H | AR | Shift Sum Register |

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = $X_i$ latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

**Figure 5. Function Table Showing the Operation of the Am25LS14**

control flip flop, and loads the new multiplicand into the X holding latch. At this same time, the multiplier word can be loaded into a Parallel-to-Serial converter (such as the Am25LS22) ready for presenting to the Serial/Parallel multiplier Y input. During the first time period after the clear signal, the least significant bit of the multiplier is presented to the Y input of the Am25LS14 and in the next clock period the first bit of the product, $S_0$, is available at the S output of the device. For the next n–1 clock periods, the multiplier bits are presented one at a time to the multiplier Y input and the

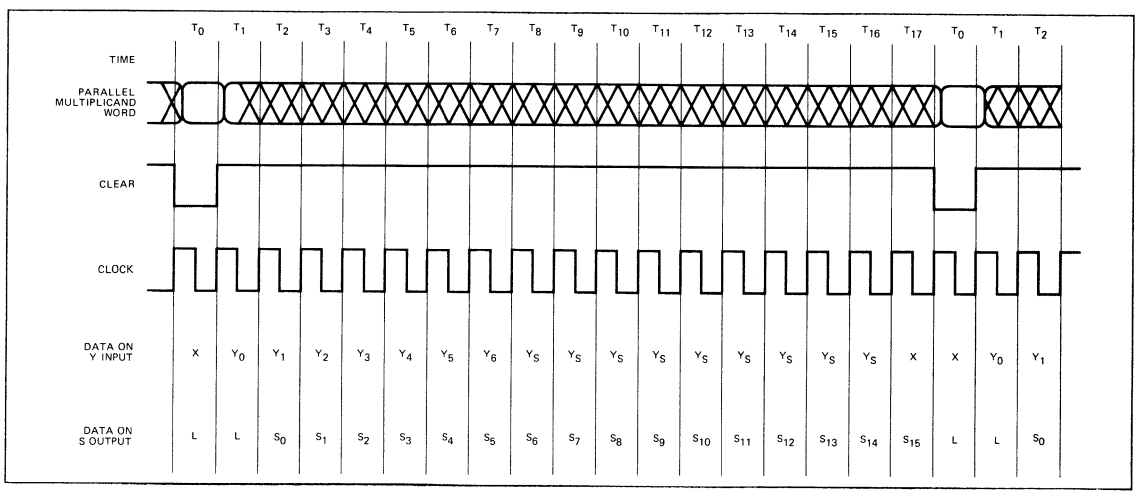



**Figure 6. Timing Diagram Showing 18 Clock Cycle Operation of 8 x 8 Multiplication**

product bits are available one at a time from the S output. For the remaining m clock periods, the Serial/Parallel multiplier requires that either the most significant bit of the multiplier word, Y, be repeated (two's complement operation) or a string of zeroes be applied (if the multiplier is to be treated as an unsigned number) to the Y input.

It is possible to perform an m + n multiplication using only one additional clock cycle. This requires that the clear pulse is presented at the same time as $Y_0$, the least significant Y multiplier bit. Since the minimum clear pulse width is 20ns and the clear recovery time is 18ns, the time duration must be at least 38ns minimum for this clock period. A timing diagram for this mode of operation is shown in Figure 7.

Many applications, especially when using two's complement operands, do not required a full n + m bit product but only an m + n−1 bit product. For example, if fractional operands in the number range of −1 to $1-2^{-(n-1)}$ and −1 to $1-2^{-(m-1)}$ are assumed, only the case of −1 times −1 requires m + n bits to represent the product. All other combinations can be represented correctly in two's complement notation by m + n −1 bits. That is, when dealing with fractions, only one bit to the left of the binary point carrying a weight of −1 is required except for the one special case. This can be used to remove one additional clock cycle from the multiplication process as shown in Figure 8. The same reasoning applies to integer representations where the largest negative numbers are $-2^{(m-1)}$ and $-2^{(n-1)}$. Only m + n bits are required to handle the case of $(-2^{(m-1)})$ $(-2^{(n-1)})$. All other products require only m + n−1 bits for a correct two's complement product. Let's take an example. If m = 4 and n = 3, then seven bits are required to represent (−8)• (−4) = (+32) in two's complement. All other products for a 3-bit and 4-bit multiplicand and multiplier can be represented correctly in two's complement form with a 6-bit representation.

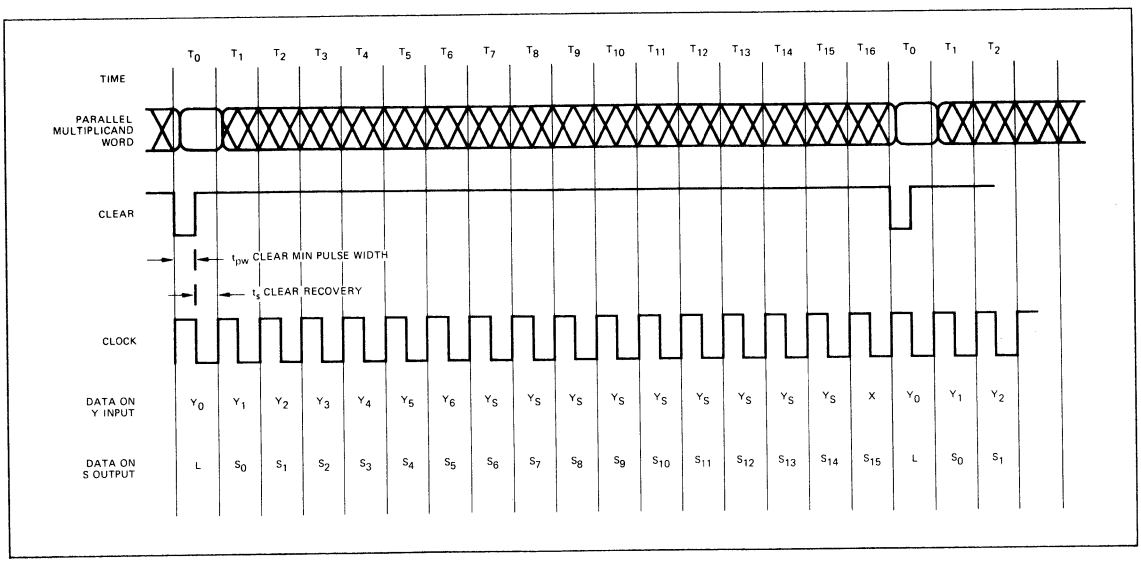



**Figure 7. Timing Diagram Showing 17 Clock Cycle Operation of 8 x 8 Multiplication**

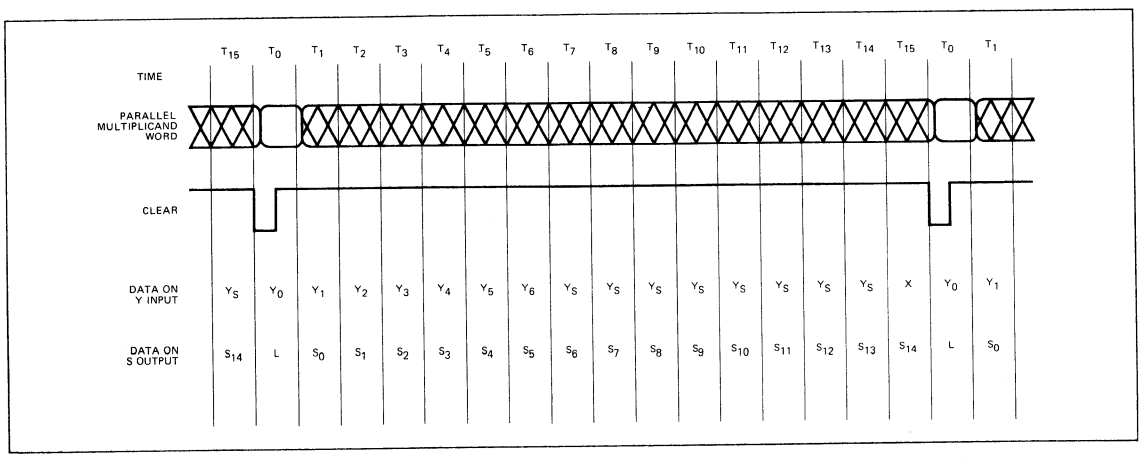



**Figure 8. Timing Diagram Showing 16 Clock Cycle Operation for an 8 x 8 Multiplication (Assumes a 15-Bit Product Representation)**

## ROUNDING AND TRUNCATION

Truncation is performed in the Am25LS14 by ignoring the appropriate number of least significant bits (LSB's). Unfortunately, no clock cycles can be saved when truncating because the product is being developed LSB first. Therefore, the truncated bits are the first bits out of the Am25LS14 multiplier. The subsystem must be clocked the total number of times (m + n) to develop the two's complement product. This does have the advantage of saving register bits to hold the product from the device.

To date, the recommended method of rounding is to use one-fourth of an Am25LS15 to perform rounding. This technique involves adding a one at the bit prior to the LSB of the final product using one input of the Am25LS15. The product from the multiplier is connected to the other input. This does require one extra clock cycle to implement rounding. This technique works for any combination of multiplicand bits, multiplier bits and desired product bits.

## APPLICATIONS

### Eight-Bit by Eight-Bit Multiplier

A circuit which generates a 16-bit product from an 8-bit by 8-bit multiplication is depicted in Figure 9. This sub-system consists of one Am25LS14 serial/parallel multiplier and two Am25LS22 8-bit registers. This configuration accepts an 8-bit multiplicand and an 8-bit multiplier from an 8-bit data bus. It will return a 16-bit product (8-bit upper byte and 8-bit lower byte) using the same 8-bit bus.

The Am25LS22 is an 8-bit register designed for performing various functions with the Am25LS14. It can be used to hold the multiplier word initially, perform the sign-extend function and then hold part of the product. It has separate serial input/output capability as well as shared parallel input/outputs.

The timing sequence for controlling this circuit is shown in Figure 10. Twenty-two clock cycles are used in this example to fully load, multiply and unload the multiplier subsystem. Thus, such an arrangement can be used with any of the popular 8-bit MOS microprocessors such as the 8080, 6800, 2650, F8 and others. This allows the multiplication to be performed outside of the MOS microprocessor with about two to three orders of magnitude improvement in speed.

Referring to the timing sequence of Figure 10, the multiplier word is loaded into the Am25LS22 register at time $T_1$ and the multiplicand word is loaded in the Am25LS14 latches during time $T_1$. The multiplicand and multiplier words must be loaded in this order since there is no hold function on the Am25LS14 multiplier.

During time $T_2$ through $T_{10}$, the least significant product bits are generated and clocked into holding register B. Meanwhile the multiplier sign bit is being extended in Register A. The sign extend is performed only for the eight clock cycles $T_2$ through $T_9$. During time $T_{11}$ through $T_{18}$, the most significant 8-bits of the product are developed in the Am25LS14 multiplier. $T_8$ is used to load the product sign bit from the multiplier into the Am25LS22 B register. During the time $T_1$ through $T_8$, the least significant half of the product is transferred from register B to register A. The remaining two clock cycles, $T_{19}$ and $T_{20}$ are used to unload the product upper and lower byte back onto the 8-bit data bus.

The control signals required for this multiplier are shown in Figures 9 and 10. Notice that the clear input to the Am25LS14 and the Serial/Parallel (S/P) input to the Am25LS22 can be connected together with the appropriate don't cares eliminated. Other control signals to the Am25LS22 include the register enable (RE), sign extend (SE), and the three-state control ($\overline{OE}$). These signals can be generated using a counter and combinatorial logic gates or a counter and small PROM.

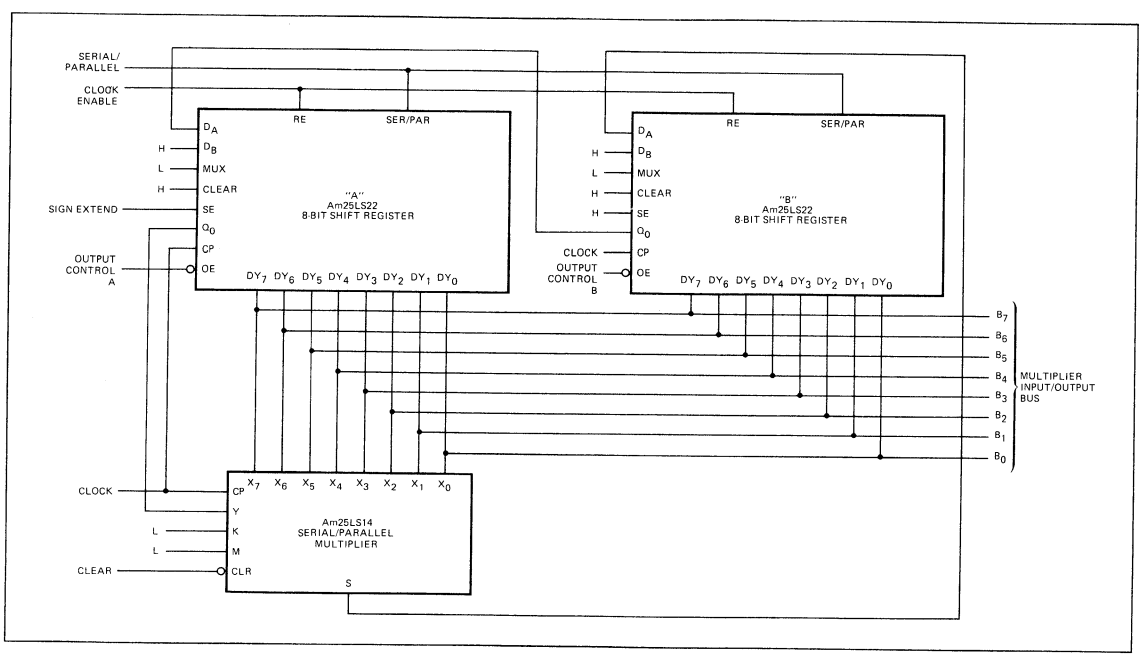



**Figure 9. An 8-Bit by 8-Bit Multiplier with a Full 16-Bit Product Store. The Inputs and Outputs are Bus Organized on an 8-Bit Bus**

| TIME | I/O BUS | Am25LS14 | | | Am25LS22's | | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Y | CLR | S | S/P | RE | SE | $\overline{OE}$ A | $\overline{OE}$ B | |
| $T_0$ | Multiplier | X | X | X | L | L | X | H | H | Load Multiplier (Y) |
| $T_1$ | Multiplicand | X | L | X | X | H | X | H | H | Load Multiplicand (X) |
| $T_2$ | X | $Y_0$ | H | L | H | L | L | H | H | Present $Y_i$ to multiplier. Read $S_i$ into Register B. Extend Y sign. |
| $T_3$ | X | $Y_1$ | H | $S_0$ | H | L | L | H | H | |
| $T_4$ | X | $Y_2$ | H | $S_1$ | H | L | L | H | H | |
| $T_5$ | X | $Y_3$ | H | $S_2$ | H | L | L | H | H | |
| $T_6$ | X | $Y_4$ | H | $S_3$ | H | L | L | H | H | |
| $T_7$ | X | $Y_5$ | H | $S_4$ | H | L | L | H | H | |
| $T_8$ | X | $Y_6$ | H | $S_5$ | H | L | L | H | H | |
| $T_9$ | X | $Y_S$ | H | $S_6$ | H | L | L | H | H | |
| $T_{10}$ | X | $Y_S$ | H | $S_7$ | H | L | H | H | H | Continue Multiplication using $Y_S$ in register. Load least significant part of product into Register A and most significant in Register B. |
| $T_{11}$ | X | $Y_S$ | H | $S_8$ | H | L | H | H | H | |
| $T_{12}$ | X | $Y_S$ | H | $S_9$ | H | L | H | H | H | |
| $T_{13}$ | X | $Y_S$ | H | $S_{10}$ | H | L | H | H | H | |
| $T_{14}$ | X | $Y_S$ | H | $S_{11}$ | H | L | H | H | H | |
| $T_{15}$ | X | $Y_S$ | H | $S_{12}$ | H | L | H | H | H | |
| $T_{16}$ | X | $Y_S$ | H | $S_{13}$ | H | L | H | H | H | |
| $T_{17}$ | X | $Y_S$ | H | $S_{14}$ | H | L | H | H | H | |
| $T_{18}$ | X | X | H | $S_{15}$ | H | L | H | H | H | Load MSB into Register. |
| $T_{19}$ | Product Lower Byte | X | X | X | X | H | X | L | H | Unload product Lower byte onto bus. |
| $T_{20}$ | Product Upper Byte | X | X | X | X | H | X | H | L | Unload product Upper byte onto bus. |

H = HIGH L = LOW X = Don't Care

**Figure 10. Timing Sequence for an 8 x 8 Multiplier with Full 16-Bit Product Register**

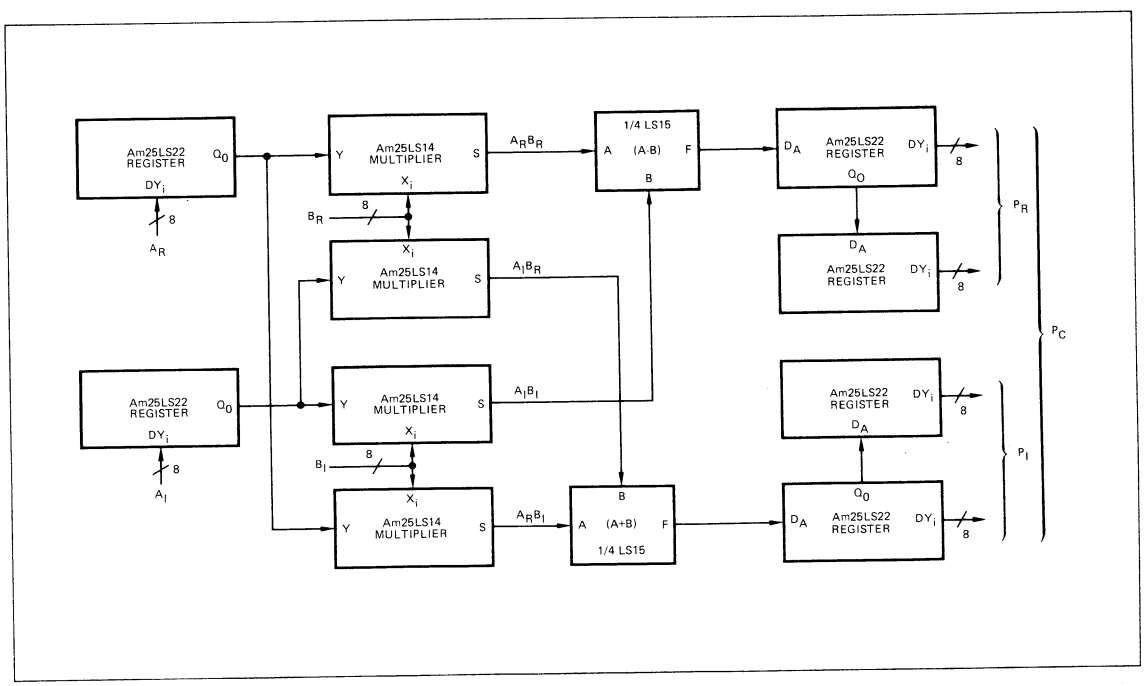



**Figure 11. Complex Arithmetic Multiply $P_C = (A_RB_R - A_IB_I) + j(A_RB_I + A_IB_R)$**

## COMPLEX ARITHMETIC MULTIPLIER

The Am25LS14 serial/parallel multiplier, the Am25LS15 adder/subtractor, and the Am25LS22 eight-bit register can be used to perform rapid multiplication in complex arithmetic processors. In complex arithmetic notation, each variable is assumed to have a real part and an imaginary part. Thus, complex variables $A_C$ and $B_C$ may be represented as:

$$A_C = A_R + jA_I$$
$$B_C = B_R + jB_I$$

The product of $A_C$ and $B_C$ is, of course, complex product $P_C$ where:

$$P_C = P_R + jP_I = A_C B_C$$
$$P_C = (A_R + jA_I)(B_R + jB_I)$$
$$P_C = (A_R B_R - A_I B_I) + j(A_R B_I + A_I B_R)$$

From this discussion, the real and imaginary values of the product $P_C$ are readily identified. These are:

$$P_R = A_R B_R - A_I B_I$$
$$P_I = A_R B_I + A_I B_R$$

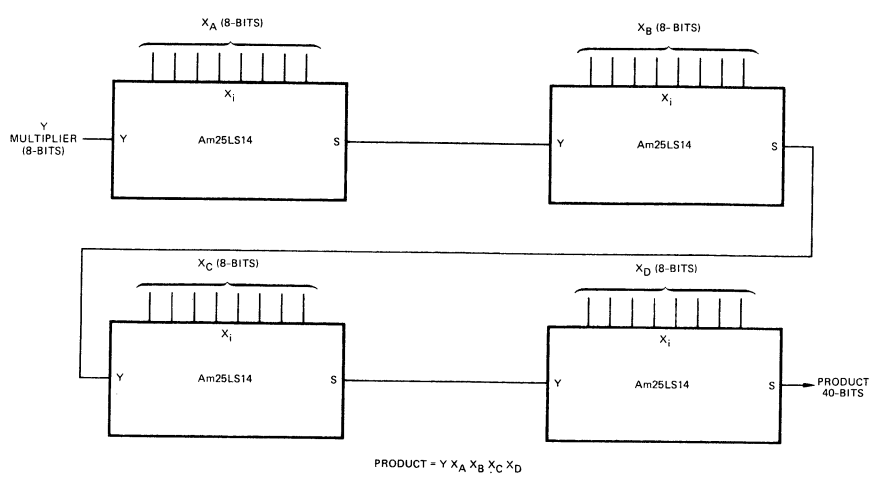
The circuitry required to implement this complex multiplier is shown in Figure 11. In this example, the real and imaginary values of the $A_C$ variable are loaded into the two Am25LS22 registers. The real and imaginary values of the $B_C$ variable are loaded into the latches of the Am25LS14. This loading of the data could be performed simultaneously using all four inputs $A_R$, $A_I$, $B_R$ and $B_I$ or it could be performed sequentially using a pair of inputs or a single input at a time.

Once the incoming $A_C$ and $B_C$ data have been loaded, the devices are clocked such that the four intermediate products are formed as shown in Figure 11. Then, two of the four adder/subtractors in the Am25LS15 are used to complete the generation of real product term $P_R$ and the imaginary product term $P_I$.

These product terms $P_R$ and $P_I$ can be loaded into four additional Am25LS22 registers to hold the double length product terms $P_R$ and $P_I$ (assume least significant bit truncation). After the complex multiplication has been completed, the $P_R$ and $P_I$ variables can be returned to the processor, memory or other destination by using the parallel bus outputs of the Am25LS22.

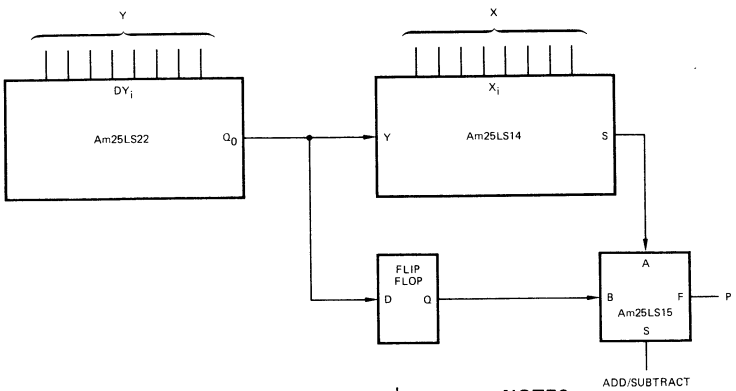
## OTHER APPLICATIONS

Other examples of applications using the Am25LS14 as well as the Am25LS15 and Am25LS22 are shown in Figures 12 through 15. Each of these applications is intended to give the design engineer a new approach to solving numerical problems involving digital multiplication.




Four Am25LS14's can be used to implement the product of five variables Y, $X_A$, $X_B$, $X_C$ and $X_D$. If each input variable is eight bits, a 40-bit product results and the multiplier array must be clocked 40 times. This requires the 8-bit Y variable to be sign extended for 32 additional clock cycles.

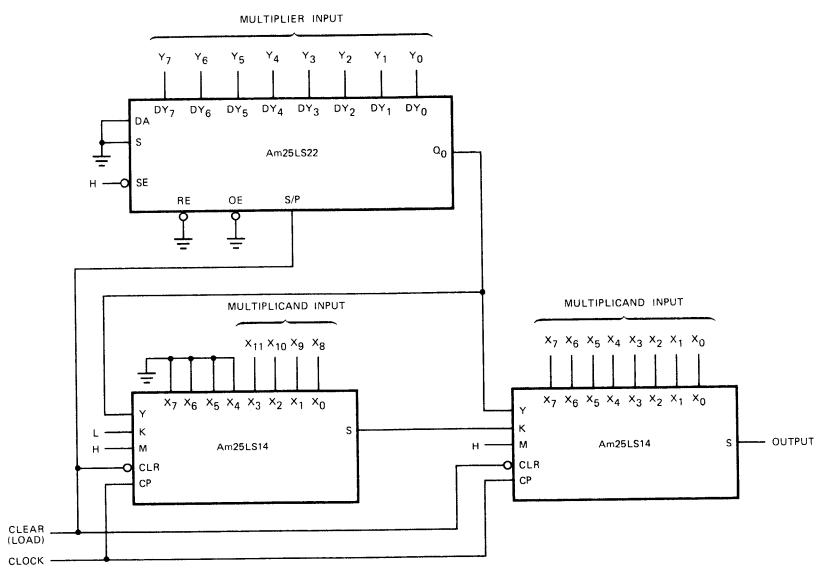
**Figure 12. Multiple Operand Multiplications**




| | FUNCTION | | NOTES |
|---|---|---|---|
| 1 | $P = X \cdot Y + Y$ | $= Y(X + 1)$ | 'LS15 in add mode |
| 2 | $P = X \cdot Y - Y$ | $= Y(X - 1)$ | 'LS15 in subtract mode |
| 3 | $P = X \cdot Y + Y + 1$ | $= Y(X + 1) + 1$ | 'LS15 is subtract mode for clear and add mode for multiply |
| 4 | $P = Y - X \cdot Y$ | $= Y(1 - X)$ | 'LS15 A & B inputs reversed |

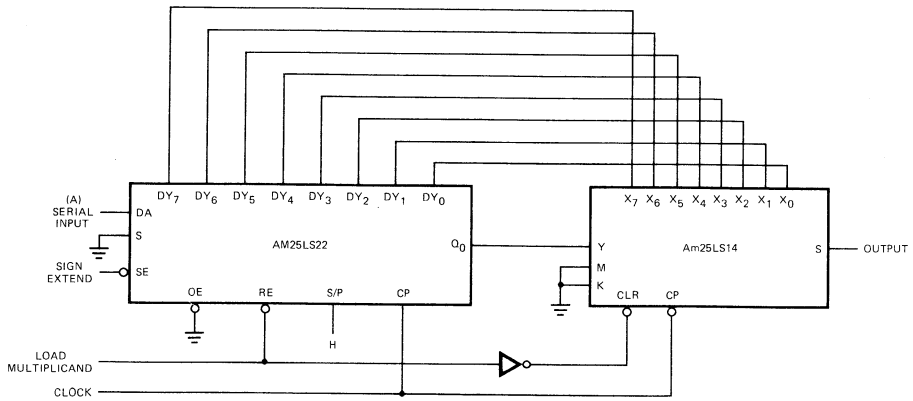
One Am25LS14, Am25LS15 and Am25LS22 can be used to perform several arithmetic functions. Four such functions are shown above. All use a product equal to the multiplicand times the multiplier in combination with a function of the multiplier. Additional combinations are possible, especially if more flip-flops are used to change the relative weight of the multiplier or product function.

**Figure 13.**




A 12-bit by 8-bit unsigned multiplication is performed by tying the four most significant multiplicand bits LOW to logic zero. The Am25LS22 is loaded with the 8-bit unsigned multiplier. As the multiplier is shifted, a "zero-fill" is accomplished using the $D_A$ input on the Am25LS22. Note the MSB M-input is HIGH on the most significant Am25LS14.

**Figure 14.**




One Am25LS14 and Am25LS22 can be used to perform the function $A^2$ on an input variable A. The 8-bit value for A is loaded into the Am25LS22 register in serial form using the $D_A$ input. Once loaded, the A value can be transferred to the Am25LS14 multiplicand latches via the $DY_i$ outputs. Then the product of A·A is formed resulting in $A^2$ at the Am25LS14 output.

**Figure 15.**

# MECHANIZATION OF THE Am25LS14 SERIAL/PARALLEL MULTIPLIER

**By John R. Mick**

The Am25LS14 Serial/Parallel Multiplier uses Booth's algorithm to give the correct two's complement product without the need of post multiplication correction. The algorithm requires that two bits of the multiplier are examined at each time period. These bits are $y_a$, the multiplier bit at the present time $t_a$, and $y_{a-1}$, the multiplier bit at the previous time $t_{a-1}$. The assumption is made that at each time, $t_a$, it is the last multiplier bit in the word and, therefore, it carries a negative weight; if it is a logic one, a subtraction takes place at this weight. If this was not the last bit in the word, a correction takes place during the next time period. The logic, therefore, not only has to examine the multiplier bit $y_a$ in the current time but also the previous $y_{a-1}$ in order to discover whether a correction is necessary.

The algorithm is performing the function:

$$S = \sum_{a=0}^{n-1} X \left\{ y_a (-2^a) + y_{a-1} (2^{a-1}) \right\}$$

where: S = the product X • Y,

X = the multiplicand

$y_a$ = the current multiplier bit

$y_{a-1}$ = the previous multiplier bit

$-2^a$ = two's complement weight of the current multiplier bit

$+2^{a-1}$ = two's complement weight of the previous multiplier bit

n = total number of bits in the multiplier

Obviously, if at $t_a$, $y_a$ is a one and X is positive, then S is negative. If X is negative, then S is positive for $y_a = 1$ at $a = n-1$ which is exactly what is required at the last bit operation during a two's complement multiplication.

The four possibilities of $y_a y_{a-1}$ give the following requirements in order to satisfy Booth's algorithm.

| $y_a y_{a-1}$ | Function |
|---|---|
| 0 0 | No arithmetic operation. Shift partial product relative to multiplier. |
| 0 1 | Add multiplicand to partial product, S, and shift new partial product. |
| 1 0 | Subtract multiplicand from partial product, S, and shift new partial product. |
| 1 1 | No arithmetic operation (perform correction by executing both add and subtract of equation 1). Shift partial product relative to multiplier. |

The last entry with $y_a y_{a-1} = 1, 1$ is made up of an addition and a subtraction of the multiplicand at weights offset by 2. This is used to perform the correction associated with the previous iteration where $y_a$ was also a logic 1 and given negative weight. Since a shift has now taken place, the addition of $(Xy_{a-1}2^{a-1})$ cancels the previous subtraction of $-Xy_a2^a$ before the shift and has the effect of extending the sign of the running partial product.

## IMPLEMENTING THE CARRY

The next consideration in the Am25LS14 Serial/Parallel Multiplier is the carry scheme to be used for the arithmetic section. Since an essential characteristic of the design is a very high processing rate, the carry scheme must have as few a number of gate delays as possible. There are many look-ahead carry schemes but they all suffer from two problems. The carry network becomes increasingly complex as the word length is increased and in any practical scheme, additional delay is incurred for longer word lengths. What is required is a method where the carry delay is short and independent of the word length of the multiplicand.

One method of obtaining this result is called a "stored carry adder" and is particularly suited to serial/parallel arithmetic. The concept is straightforward but is complicated in the Am25LS14 because not only are carries generated but also borrows. (It assists understanding if these borrows are treated as negative carries.) In the stored carry scheme, when an addition (or subtraction) takes place, instead of the carry (borrow) being presented to the next arithmetic stage so as to affect the next sum bit and be used to generate the carry at that stage for the next stage, the carry is stored in a flip-flop at the same stage and incorporated into the arithmetic at the next time iteration of the addition (subtraction).

A combinatorial design of an MSI Serial/Parallel Multiplier is shown in Figure 1. The inputs to the Am25LS181 adder/subtractor are the partial product and the multiplicand. The multiplicand is gated by a function of the $y_a y_{a-1}$ multiplier bits by using the mode control of the Am25LS181. The sum or new partial product out of the 'LS181 adder/subtractor is shifted one place down and stored in the next lower stage partial product register made up of the Am25LS174's. In each adder stage, the generated carry goes to the next higher adder stage internally.

The stored carry concept is shown in Figure 2. Here, the inputs to the full adder are the partial product, the multiplicand gated by the $y_a y_{a-1}$ and the previously stored carry generated at the same stage during the previous cycle. The outputs of the full adder are the sum which is stored in the sum partial product flip-flop at the next lower stage and the carry which is stored in the carry flip-flop at the same stage and is not shifted down. The stored carry concept uses an additional flip-flop per multiplicand bit compared to the standard MSI approach, but the delay between consecutive clock pulses is short and remains the same, independent of the number of stages. In the MSI approach, the total propagation delay is a function of the length of the Am25LS181 adder network. It is possible to have a combination of combinatorial carry

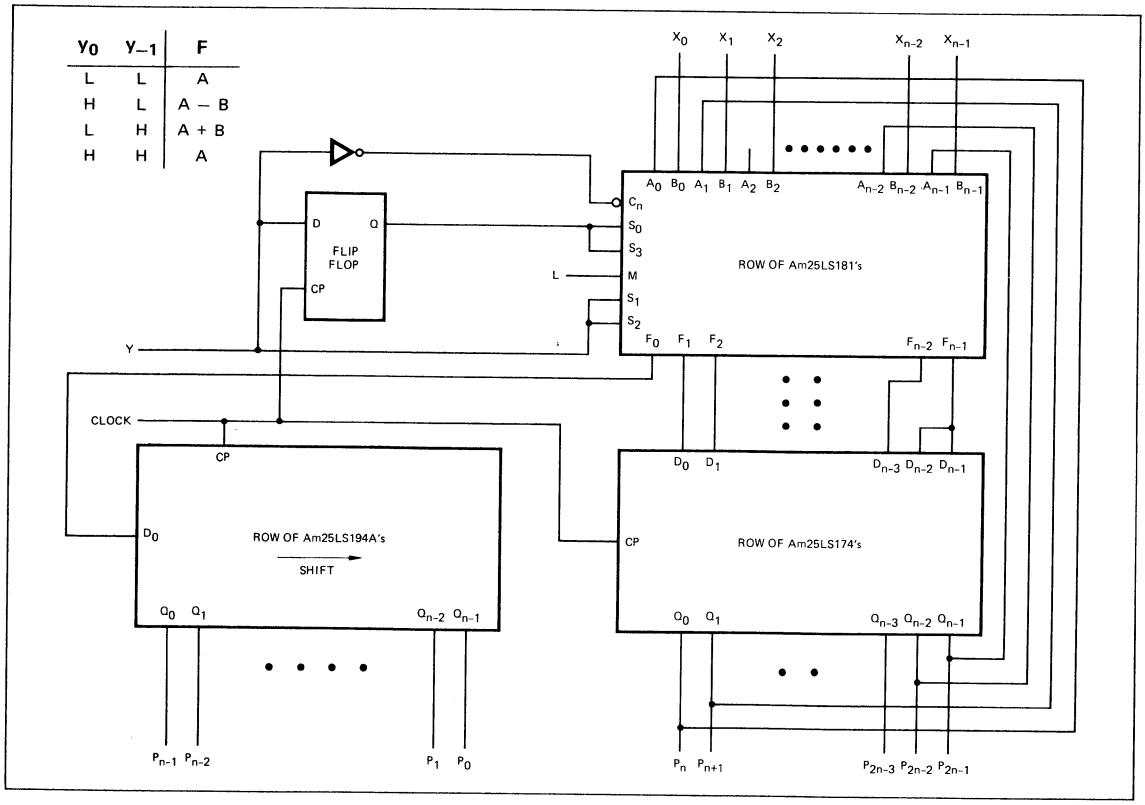



**Figure 1. An MSI Implementation of the Serial/Parallel Multiplier Algorithm**

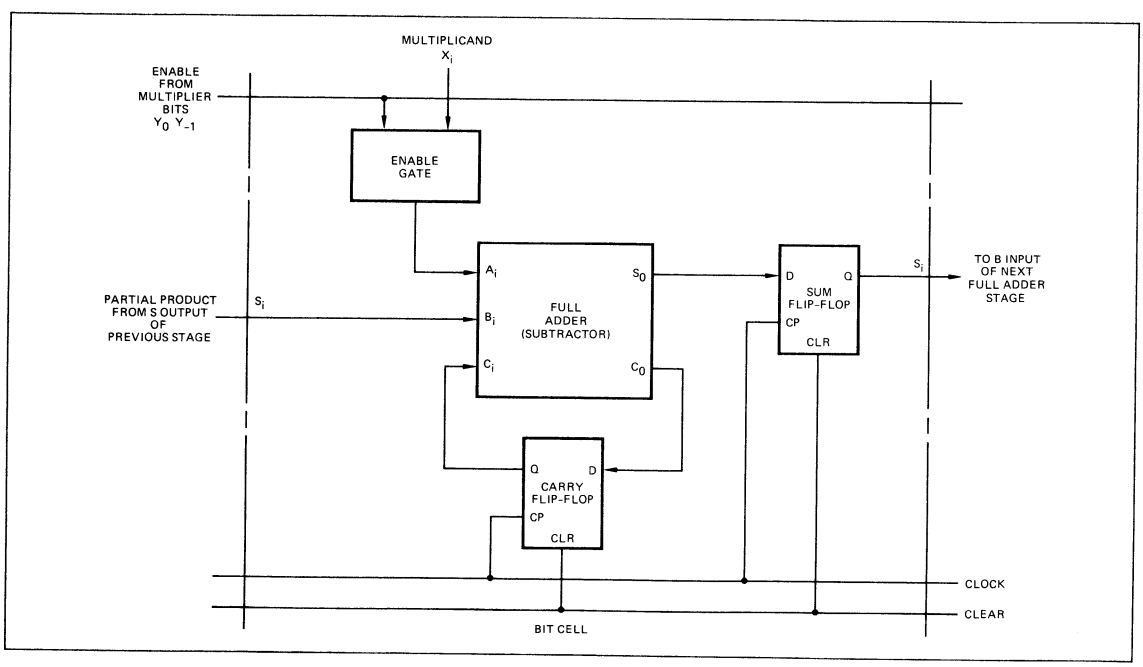



**Figure 2. This Carry Save Cell Could Be Used in a Shift and Add Algorithm for a Serial/Parallel Multiplication**

and stored carry by storing every second or fourth carry generated and so on. However, the best compromise between delay and complexity appears to be satisfied in low-power Schottky technology by incorporating an extra carry flip-flop at each multiplicand stage and storing the carry for each full adder.

## UNDERSTANDING THE ITERATIVE CELL OF THE Am25LS14

In order to fully understand the iterative cell of the Am25LS14, it is necessary to view the cell block diagram of Figure 2. What is desired is to define the logic operation of the multiplicand enable gate and the full adder/subtractor. From the development of Booth's algorithm, it has been shown that $y_0$ and $y_{-1}$ ($y_a$ and $y_{a-1}$ respectively) control the add/subtract function as well as the pass multiplicand/pass zero function. The full adder/subtractor and control gate, therefore, must have $y_0$, $y_{-1}$ and $x_i$ as inputs. Also, the carry saved from the previous iteration is an input, $C_i$, as well as the sum bit, $S_i$, from the previous iteration. The adder/subtractor must generate a new sum bit, $S_0$, and a new carry/borrow bit, $C_0$.

For any multiplication, there is only one value of $x_i$ at each cell. That is, $x_i$ is either a logic 1 or a logic 0. Thus, each case for $x_i$ can be treated separately. Let us assume that $x_i = 0$ as the input to cell shown in Figure 2. It is soon recognized that based on Booth's algorithm, the required operation is add nothing, subtract nothing or do nothing. Thus, if the carry flip-flop is reset initially, the only possible logic 1 into the cell is at the $S_i$ input since $x_i = 0$ and $C_i = 0$ initially. This results because the value at both the B and C inputs to the adder/subtractor are always zero. Therefore, the carry flip-flop can never be set to a one because the carry out is always zero. Thus, $S_0$ is always set equal to the value at B and the cell executes a simple pass function. This is shown in the top 16 states of Table I. Table I shows all the combinatorial output states of the adder/subtractor as a function of the five input variables to the cell; these are $x_i$, $y_0$, $y_{-1}$, $S_i$ and $C_i$.

The more interesting case, obviously, is the condition where the $x_i$ input is a logic 1 for the multiplicand bit at this cell. The easiest way to explain this case is to view the last 16 states of Table I. This should result in considerable misunderstanding not to mention the initial frustration.

Let's try to take this table apart and make some sense out of it. First of all, remember that due to the operation of Booth's algorithm, additions and subtractions must be interleaved. Two additions or two subtractions cannot be sequential. This is an extremely important key in understanding the cell operation.

In Table I, notice that states 16 through 19 execute a do nothing based on Booth's algorithm since $y_0 = 0$ and $y_{-1} = 0$. Likewise, states 20 through 23 execute an add the multiplicand to the running partial product since $y_0 = 0$ and $y_{-1} = 1$. States 24 through 27 requires the multiplicand to be subtracted from the running partial product and states 28 through 31 are also do nothing. It is essential to observe that only one time cycle can be spent in states 20 through 23 or 24 through 27. This is because two additions or subtractions cannot be sequential. Also, certain states result in definite possible state transitions depending on the new $y_0y_1$ value. For example, state 24 can only lead to states 21, 23, 29 or 31. State 23 can only go to states 16, 18, 24 or 26 on the next cycle and so forth. However, once in states 16 through 19, you can remain in states 16 through 19 indefinitely, and once in states 28 through 31 you can remain in states 28 through 31 indefinitely.

So what? After careful scrutinization, it will be realized that the sum, $S_0$, and carry, $C_0$, outputs of the adder/subtractor cell of Figure 2 can only represent the function of the block if the following is true:

- To define the operation of states 16 through 23, the $S_0$ output is weight 1 and $C_0$ is weight 2.
- To define the operation of states 24 through 31, the $S_0$ output is weight 1 and $C_0$ is weight −2.

This results in the carry/borrow definition for the adder/subtractor. Remembering that the running partial product is shifted before the next cycle, the $c_i$ input of the full adder/subtractor is, of course, at weight +1 or −1 after the shift. Once Table I is accepted, all that remains is to generate the required logic for the cell. That is, the logic equations for $S_0$ and $C_0$. Simply stated, the equations for the adder/subtractor cell are as follows:

$$S_0 = S_i \oplus C_i \oplus [X_i\ (y_{-1} \oplus y_0)]$$

$$C_0 = (S_i \oplus y_0)\ [C_i \oplus X_i\ (y_0 \oplus y_{-1})]$$

These are the equations implemented in each cell of the Am25LS14 with a slight modification to the MSB cell.

**Table I**
**Function Table for an Am25LS14 Cell**

| State | $X_i$ | $y_0$ | $y_{-1}$ | $S_i$ | $C_i$ | $S_0$ | $C_0$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | — | — |
| 2 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 | — | — |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 | — | — |
| 6 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 | — | — |
| 8 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 | — | — |
| 10 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 | — | — |
| 12 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 | — | — |
| 14 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 | — | — |
| 16 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 18 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 20 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 22 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 23 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 24 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 25 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 26 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 27 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 28 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 29 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 30 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 31 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

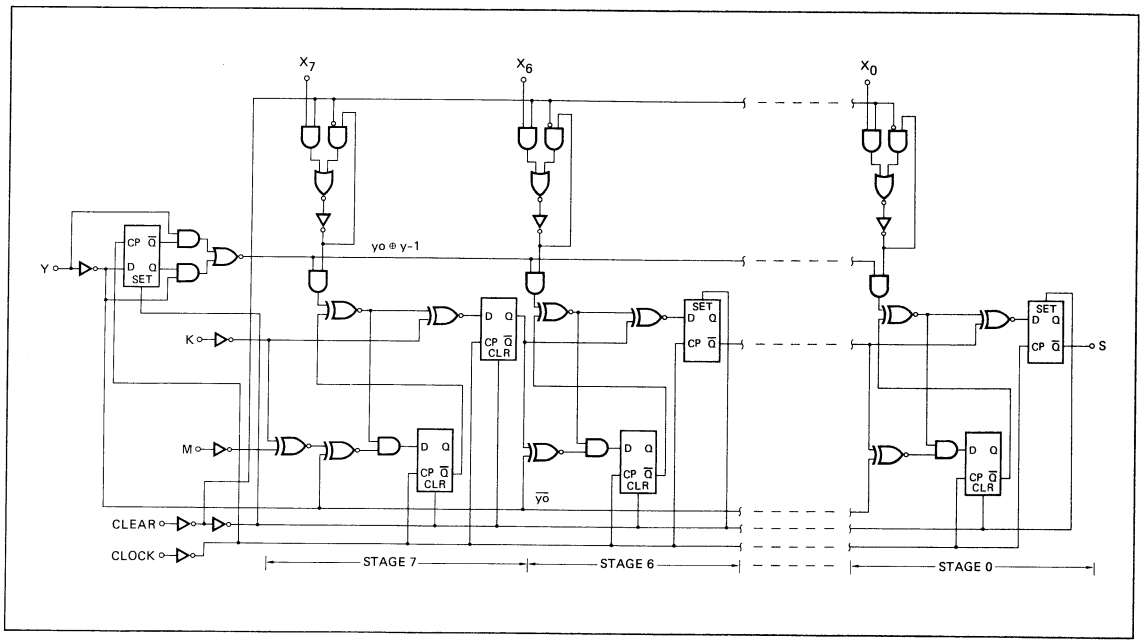



**Figure 3.**

## LOGIC DIAGRAM

A full logic depiction of the Am25LS14 is shown in Figure 3. Each of the seven least significant cells of the device are identical. These are the cells shown as stage 0 through stage 6.

Only the eighth (MSB) cell (stage 7) has a modification to handle the Mode (M) and expansion (K) inputs to allow cascading. Also, the sum flip-flop output is connected to the opposite side compared to the other cells.

# HOW TO MULTIPLY AND/OR DIVIDE IN TWO'S COMPLEMENT HARDWARE

By Roy Levy

A question that is asked of our application group almost daily is "How do I multiply and divide in two's complement hardware". AMD has designed a family of integrated circuits to aid systems' and subsystems' designers in solving some of the complicated arithmetic problems. These circuits are:

- Am25S05 – Schottky Four-Bit by Two-Bit Two's Complement Multiplier.*
- Am2505 – TTL Four-Bit by Two-Bit Two's Complement Multiplier.
- Am25L05 – Low-Power Four-Bit by Two-Bit Two's Complement Multiplier.
- Am2503 – Successive Approximation Register.
- Am25L03 – Low-Power Successive Approximation Register.
- Am25LS22 – Eight-Bit Serial/Parallel Register with Sign Extend.
- Am25LS14 – Eight-Bit Serial/Parallel Two's Complement Multiplier.
- Am25LS15 – Quad Serial Adder/Subtractor.

The problem of two's complement multiply can be solved using AMD devices in either of two ways dependent on speed requirements. One is by using the Am25LS14 and performing a serial by parallel multiply and iterating the algorithm through all "Y" bits of the serial multiplier word (see Figure 1). This particular solution assumes the use of an eight-bit data bus and loads an eight-bit multiplicand into Am25LS14 in two's complement notation and an eight-bit multiplier into the first Am25LS22. After 17 clock cycles, the 16-bit product will be forced into the two 8-bit Am25LS22 registers.

The second and faster method of two's complement multiplication is that of Figure 2. This method employs the use of the Am25S05. The connection symbology will be seen in Figure 3. This implementation can be modified for speed or power by substituting the Am2505 or Am25L05 for the Am25S05; Table A shows a comparison of power and speed for these devices. Table B shows the trade-off when applied to a multiplier array. Rearranging the inputs allows for multiply in a modified number system; i.e., Sign-magnitude or two's complement by one's complement (see Figures 3 and 4).

Division can be accomplished by using the recursion algorithm (or trial and error). In this method (Figure 5), a trial quotient is formed and the product of the trial quotient and division is tested against the actual dividend and the result (sign) noted. If the sign is positive, the MSB quotient is set to a one; if not, a zero is stored. This procedure is repeated for all bits of the desired quotient–MSB first, LSB last. The output of this divide is available in serial or in parallel form. Specifically, the divisor, dividend and trial quotient are all treated as two's complement numbers. Note that the first trial vlaue is integer –1. The operations performed are:

For $Q_S$, the sign digit of the quotient:

If $D_7 = 0$ and $-\frac{D}{2} < P$, Set $Q_S = 0$ Otherwise $Q_S = 1$

If $D_7 = 1$ and $-\frac{D}{2} < P$, Set $Q_S = 1$ Otherwise $Q_S = 0$

For the remaining quotient digits:

If $D_7 = 0$ and $T_{i-1}D + \frac{D}{2} < P$, Set $Q_i$ = I otherwise $Q_i = 0$

If $D_7 = 1$ and $T_{i-1}D + \frac{D}{2} < P$, Set $Q_i = 0$ otherwise $Q_i = 1$

where $T_i$ is the i th trial value held in the SAR.

Since the complement of the most significant bit of the register is used rather than the true output so that resetting the register presents –1 to the multiplier array, the change in

*Further applications of the Am25S05 are shown in "The Am25S05, Am2505 and Am25L05 2's Complement Digital Multipliers" application note contained in the Advanced Micro Devices' Schottky and Low-Power Data Book.

## APPLICATIONS

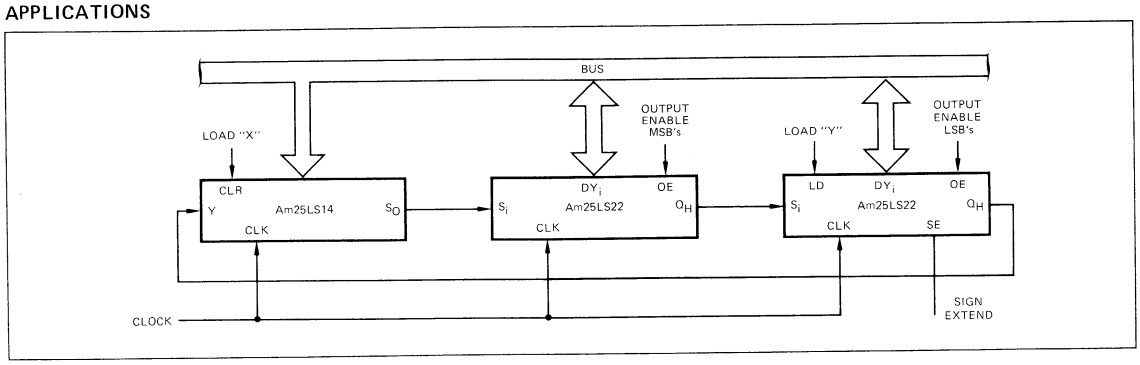



Figure 1. Bus Oriented 8-Bit x 8-Bit Multiplier with 16-Bit Product.

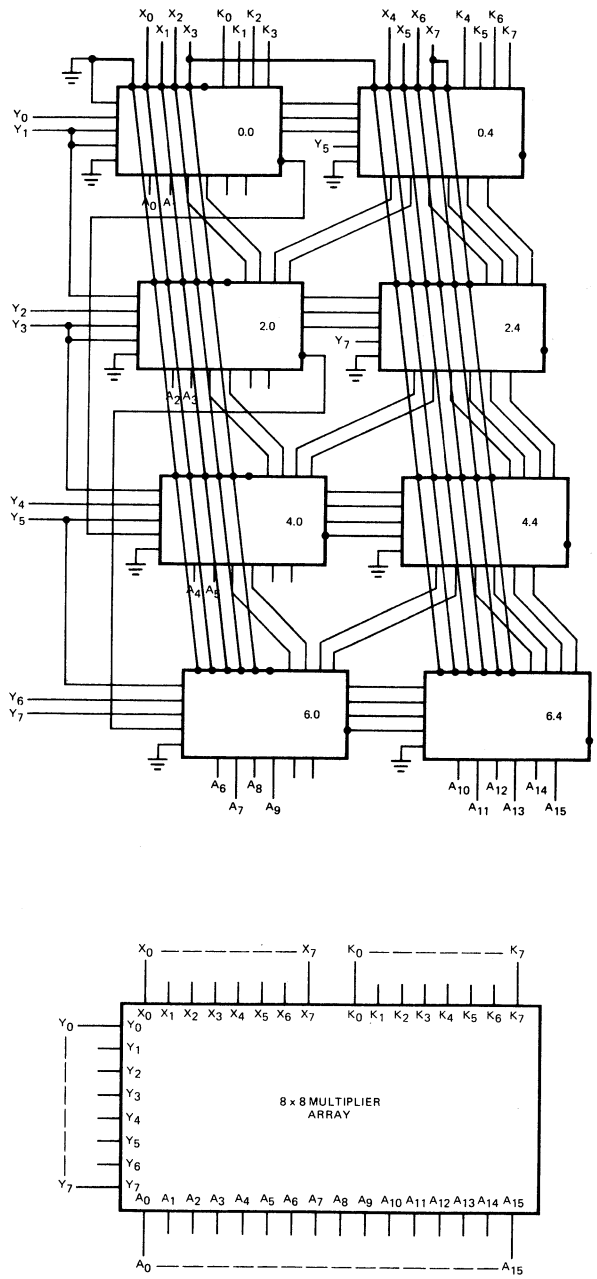
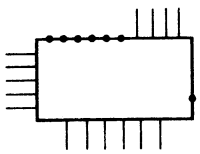



Figure 2. 8 x 8 Multiplication Array for 2's Complement Numbers. Both the Actual Connection Diagram and System Block Diagram are Shown.

Figure 3.

CONNECTION DIAGRAMS

Within this Appendix, the symbol shown at left below is used to represent the Am25S05, Am2505, or Am25L05. The symbol at left should be interpreted as equivalent to the symbol at right.



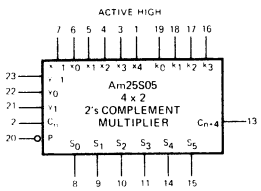



Table A-1 is a summary of the typical switching characteristics for each path through the multiplier.

## TABLE A

### TYPICAL SWITCHING CHARACTERISTICS

$$\left(\frac{t_{PHL} + t_{PLH}}{2}\right)$$

| PATH | Am25S05 | Am2505 | Am25L05 | UNIT |
|---|---|---|---|---|
| $C_n$ to $C_{n+4}$ | 8.5 | 13.5 | 32.5 | ns |
| $C_n$ to $S_{03}$ | 11.0 | 16.5 | 36.0 | ns |
| $C_n$ to $S_{45}$ | 14.0 | 19.5 | 44.0 | ns |
| k to $C_{n+4}$ | 8.25 | 13.5 | 31.0 | ns |
| k to $S_{03}$ | 11.5 | 16.5 | 36.5 | ns |
| k to $S_{45}$ | 14.0 | 21.5 | 51.5 | ns |
| X to $C_{n+4}$ | 17.5 | 21.0 | 63.5 | ns |
| X to $S_{03}$ | 21.0 | 25.0 | 70.0 | ns |
| X to $S_{45}$ | 22.5 | 29.5 | 85.0 | ns |
| Y to $C_{n+4}$ | 21.5 | 33.0 | 75.0 | ns |
| Y to $S_{03}$ | 23.0 | 35.0 | 83.5 | ns |
| Y to $S_{45}$ | 25.0 | 38.5 | 93.5 | ns |
| $I_{CC}$(TYP.) | 120 | 90 | 30 | mA |

## TABLE B

### TYPICAL SPEED & POWER FOR TWO'S COMPLEMENT MULTIPLICATION

| ARRAY SIZE | | Am25S05 | | Am2505 | | Am25L05 | |
|---|---|---|---|---|---|---|---|
| Y • X | # DEVICES | SPEED ns | POWER WATTS | SPEED ns | POWER WATTS | SPEED ns | POWER WATTS |
| 4x4 | 2 | 39 | 1.2 | 60 | 0.9 | 145 | 0.3 |
| 4x8 | 4 | 55 | 2.4 | 83 | 1.8 | 186 | 0.6 |
| 4x12 | 8 | 64 | 4.8 | 96 | 3.6 | 219 | 1.2 |
| 8x8 | 8 | 76 | 4.8 | 115 | 3.6 | 262 | 1.2 |
| 8x12 | 12 | 94 | 7.2 | 143 | 5.4 | 320 | 1.8 |
| 8x16 | 16 | 102 | 9.6 | 156 | 7.2 | 353 | 2.4 |
| 12x12 | 18 | 115 | 10.8 | 175 | 8.1 | 396 | 2.7 |
| 12x16 | 24 | 132 | 14.4 | 203 | 10.8 | 454 | 3.6 |
| 12x20 | 30 | 141 | 18.0 | 216 | 13.5 | 487 | 4.5 |
| 16x16 | 32 | 153 | 19.2 | 235 | 14.4 | 530 | 4.8 |
| 16x20 | 40 | 171 | 24.0 | 263 | 18.0 | 588 | 6.0 |
| 16x24 | 48 | 179 | 28.0 | 276 | 21.6 | 621 | 7.2 |
| 20x20 | 50 | 192 | 30.0 | 295 | 22.5 | 664 | 7.5 |
| 20x24 | 60 | 209 | 36.0 | 323 | 27.0 | 722 | 9.0 |
| 20x28 | 70 | 218 | 42.0 | 336 | 31.5 | 755 | 10.5 |
| 24x24 | 72 | 230 | 43.2 | 355 | 32.4 | 798 | 10.8 |
| 24x28 | 84 | 248 | 48.0 | 383 | 36.0 | 856 | 12.0 |
| 24x32 | 96 | 256 | 52.8 | 396 | 39.6 | 889 | 13.2 |
| 28x28 | 98 | 269 | 54.0 | 415 | 40.5 | 932 | 13.5 |
| 28x32 | 112 | 286 | 62.4 | 443 | 46.8 | 990 | 15.6 |
| 32x32 | 128 | 307 | 72.0 | 475 | 54.0 | 1066 | 18.0 |

NOTE: With Curry's Interchanged to Reverse Speed.

algorithm between the sign bit and the rest of the bits is automatically taken care of.

The D/2 factor in the equations is used to round off the quotient. A double length dividend is assumed. The Am9324 comparator array is wired for a two's complement comparison with the sign digit of the product and dividend crossed over, the divident sign bit forming part of the multiplier word and the product sign bit forming part of the dividend word.

It is evident that the divider can be used as either a divider or a multiplier (Figure 6) by substituting the inputs, outputs and providing buffering. The required control function is subject to the specific usage. Figure 7 indicated the application with bus-oriented computers such as Am9080A, 8080A, 6800, etc. To achieve this configuration, it will be necessary to add storage registers and three-state drivers. As most machines are clocked, the Divisor/Multiplier and dividend registers must be provided to retain this data for the period of operation. In order to avoid interference with the bus structure, all replies must be isolated from the data bus until requested by the machine (CPU). Certain exceptions can be made if the system will tolerate a temporary clock, stoppage while the multiplier/divider is operating. Although the operation is fast, timing consideration must be factored. The slowest operation (divide) will produce results in 16 clock pulses after completion of the loading and statusing operations. The typical sequence is as follows:

Multiply Sequence

1. Load status
2. Load multiplicand
3. Load multiplier
4. Sequence ≈ four clocks
5. Read LSB product
6. Read MSB product

Divide Sequence

1. Load status
2. Load LSB dividend
3. Load MSB dividend
4. Load divisor
5. Sequence ≈ 12 clocks
6. Read quotient

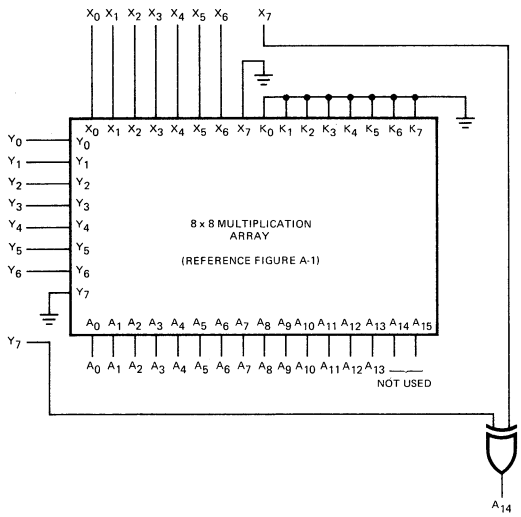
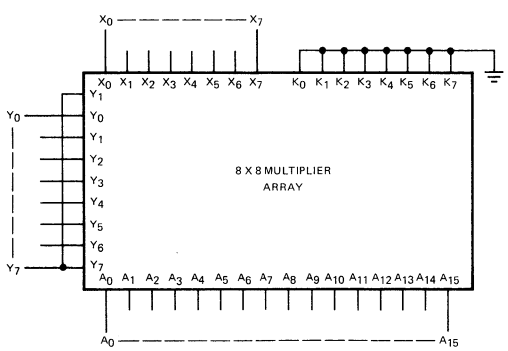



Figure 3. 8 x 8 Multiplication Array for Sign-magnitude Numbers.




$X = x - x_s(2^{n-1})$ (2's Complement Number)

$Y_1 = y - y_s(2^{m-1}-1)$ (1's Complement Number)

$XY_1 = XY + y_sX$ (2's Complement Product

Figure 4. 2's Complement Multiplicand, 1's Complement Multiplier and 2's Complement Product.

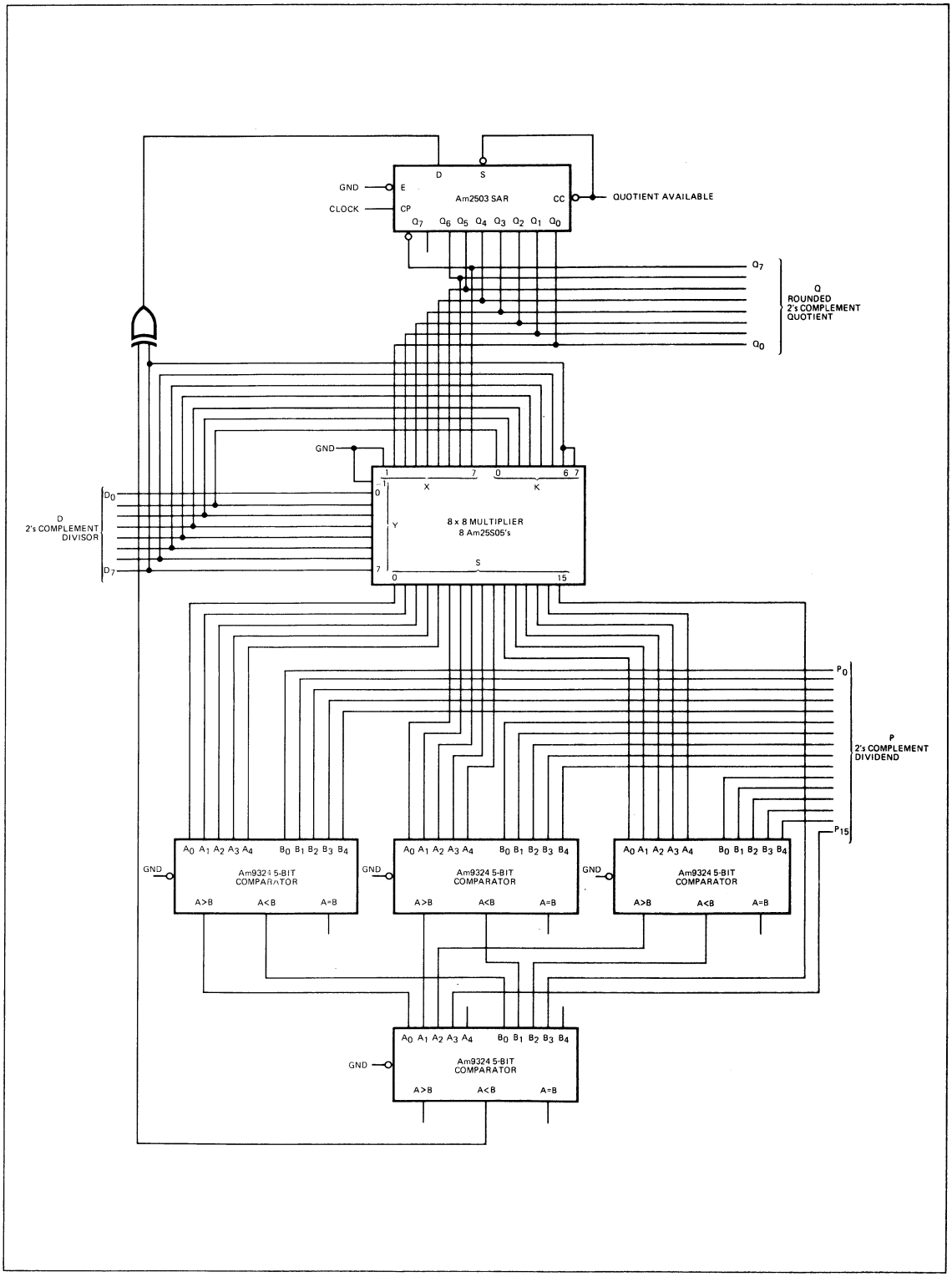



Figure 5. 2's Complement Rounded Division.

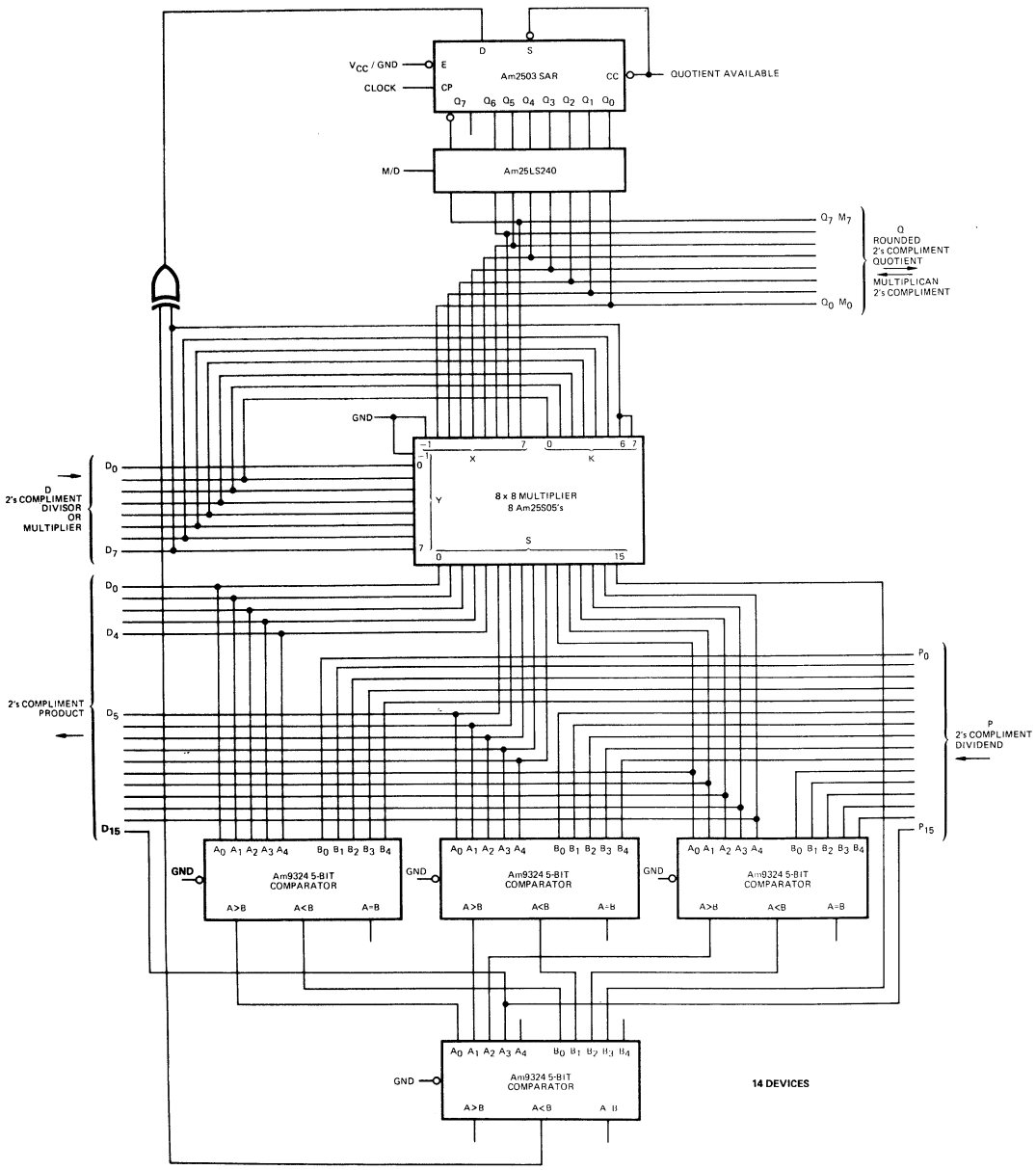
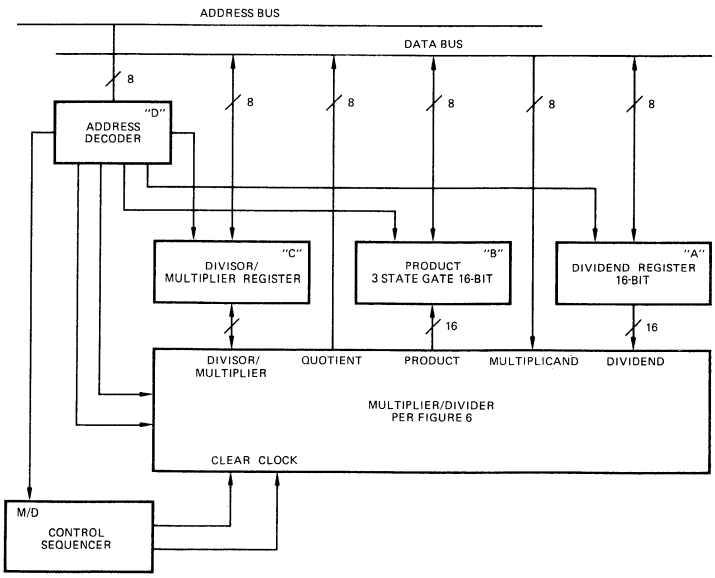



**Figure 6. 2's Complement Multiplier/Divider.**




**SUGGESTED PARTS**

A – 2 ea. Am25LS374
B – 2 ea. Am25LS240
C – 1 ea. Am25LS374
D – 1 ea. Am25LS138

**Figure 7. 8-bit by 8-bit Multiplier/Divider.**

# The Am25S05, Am2505 and Am25L05 Schottky, Standard and Low Power TTL 2's Complement Digital Multipliers

By John R. Mick

## INTRODUCTION

This application note is an updated and expanded version of the "A 2's complement Digital Multiplier — the Am2505" application note by R.C. Ghest, published in November, 1971. The device is now available in three technologies. The Am25S05 is a very high speed 2's complement multiplier built using advanced Schottky technology. The Am2505 is a standard power MSI element for medium speed applications. The Am25L05 is a low-power MSI circuit for slower speed applications.

The Am25S05, Am2505, and Am25L05 can be used in iterative arrays to perform multiplication of 2's complement numbers with a minimum of hardware. The new Am25S05 provides the capability to perform very high speed direct hardware multiplications and is especially suited for real-time digital processing applications. These devices will find applications in minicomputers, recursive or non-recursive digital filters, Fast Fourier Transform processors, adaptive digital integrators and many other digital implementations of special arithmetic algorithms.

At the present time, digital machines perform multiplication using either serial techniques, serial-parallel techniques, or all-parallel techniques. The multiplication speeds can be very slow to very fast depending on the exact hardware implementation used and the hardware constraints imposed. The Am25S05, Am2505, and Am25L05 are particularly suited for either all parallel multiplication or serial-parallel multiplication.

## MULTIPLICATION DEFINITION

According to Webster's Dictionary, multiplication is "a mathematical operation that at its simplest is an abbreviated process of adding an integer to itself a specified number of times and that is extended to other numbers in accordance with laws that are valid for integers." This definition is particularly appropriate for binary numbers in that all hardware binary multiplication schemes make an "add" or "no-add" decision and maintain the "weighting" rules of binary numbers. The two numbers involved in the operation are usually called the multiplicand (the number to be multiplied) and the multiplier (the number that multiplies) with the result being called the product (later in this application note the partial products or partial sums will be important).

Binary multiplication is performed as in the following four digit example. The terms X and Y are:

$$X = x_0(2^0) + x_1(2^1) + x_2(2^2) + x_3(2^3)$$
$$X = x_0(1) + x_1(2) + x_2(4) + x_3(8)$$
$$Y = y_0(1) + y_1(2) + y_2(4) + y_3(8)$$

where $x_i$ and $y_i$ can assume a "0" or "1" value for i = 0, 1, 2 or 3.

If X is the multiplicand and Y is the multiplier, the product S of X·Y is

$$\begin{aligned} S = X \cdot Y = {} & y_0(1)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_1(2)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_2(4)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_3(8)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \end{aligned}$$

In the above example, it can be seen that three additions are required to generate the product S of X·Y; the first two of these are usually called partial products or partial sums. In order to examine the weighting of the binary numbers in the above example, the complete partial product solution is shown in Figure 1 and the weights of the x terms and y terms have been combined.

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Multiplicand | $x_3$ (8) | + | $x_2$ (4) | + | $x_1$ (2) | + | $x_0$ (1) | | | |
| | | | | | | | | Multiplier | $y_3$ (8) | + | $y_2$ (4) | + | $y_1$ (2) | + | $y_0$ (1) | | | |
| | | | | | | | | $x_3y_0$ (8) | + | $x_2y_0$ (4) | + | $x_1y_0$ (2) | + | $x_0y_0$ (1) | | | |
| | | | | | | $x_3y_1$ (16) | + | $x_2y_1$ (8) | + | $x_1y_1$ (4) | + | $x_0y_1$ (2) | | | | | | |
| | | | Carry (32) | + | $Ps_4$ (16) | + | $Ps_3$ (8) | + | $Ps_2$ (4) | + | $Ps_1$ (2) | + | $Ps_0$ (1) | | | | | |
| | | | $x_3y_2$ (32) | + | $x_2y_2$ (16) | + | $x_1y_2$ (8) | + | $x_0y_2$ (4) | | | | | | | | | |
| | Carry (64) | + | $Ps_5$ (32) | + | $Ps_4$ (16) | + | $Ps_3$ (8) | + | $Ps_2$ (4) | + | $Ps_1$ (2) | + | $Ps_0$ (1) | | | | | |
| | $x_3y_3$ (64) | + | $x_2y_3$ (32) | + | $x_1y_3$ (16) | + | $x_0y_3$ (8) | | | | | | | | | | | |
| $s_7$(128) | + $s_6$(64) | + | $s_5$(32) | + | $s_4$(16) | + | $s_3$(8) | + | $s_2$(4) | + | $s_1$(2) | + | $s_0$(1) | | | | | |

Figure 1. Multiplication of Two Unsigned 4-bit Numbers X and Y

The $s_7(128)$ term represents the carry out of the final summation. As is seen, the multiplication of two 4-bit unsigned words results in an 8-bit product. This can be extended to a general statement; that is, the multiplication of a m-bit unsigned number with a n-bit unsigned number gives a m + n bit resultant unsigned product. This number may be truncated of course and rules will be given later for determining the resulting accuracy when the hardware is being reduced.

It should be recognized that the product terms associated with $y_0$ and $y_1$ can be added in one adder and the product terms associated with $y_2$ and $y_3$ can be added in a second adder at the same time; thereby giving two partial products after one adder propagation delay time. These two partial sums can then be added in a third adder to give the resultant product of the multiplication.

One technique for reducing multiplication time that is presently being used in serial and serial-parallel multipliers is to ignore addition when the multiplier bit is a logic "0." When this is done the number of terms to be added is equal to the number of 1's in the multiplier word. This method can be extended in such a way that strings of 1's can also be ignored—this leads to an important new technique for performing high speed multiplication. This technique will be discussed in greater detail later.

| Two's Complement | | | | Decimal Number |
|---|---|---|---|---|
| Sign bit | | | | |
| $-2^3$ | $2^2$ | $2^1$ | $2^0$ | |
| −8 | 4 | 2 | 1 | |
| 0 | 1 | 1 | 1 | +7 |
| 0 | 1 | 1 | 0 | +6 |
| 0 | 1 | 0 | 1 | +5 |
| 0 | 1 | 0 | 0 | +4 |
| 0 | 0 | 1 | 1 | +3 |
| 0 | 0 | 1 | 0 | +2 |
| 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | −1 |
| 1 | 1 | 1 | 0 | −2 |
| 1 | 1 | 0 | 1 | −3 |
| 1 | 1 | 0 | 0 | −4 |
| 1 | 0 | 1 | 1 | −5 |
| 1 | 0 | 1 | 0 | −6 |
| 1 | 0 | 0 | 1 | −7 |
| 1 | 0 | 0 | 0 | −8 |

**Figure 2. Full Definition of a 4-bit Two's Complement Binary Number**

## TWO'S COMPLEMENT NOTATION

This section is presented as a quick review of the two's complement numbering system and is intended to give insight for the designer not familiar with two's complement notation. The two's complement numbering system is a technique for describing positive and negative numbers in a convenient notation. When contrasted with other numbering systems such as sign-magnitude and one's complement, it has the advantage of only having one representation for the number "zero." Also, two's complement numbers can be added or subtracted without concern for the sign of each number as the result will be correct in two's complement notation.

In 2's complement notation, the sign bit is a logical "0" for positive numbers and a logical "1" for negative numbers. Four bits may be used to represent the numbers +7 to −8 as shown in Figure 2. Notice that the sign bit does carry magnitude information that has a negative value.

From this example, it is readily apparent that the magnitude of the negative numbers is not represented by its associated magnitude bits if the sign bit is ignored as is the case for the positive numbers. One way to find the absolute magnitude of a negative 2's complement number is to invert all bits and add plus binary one as in the example below:

| | |
|---|---|
| 1011 | Negative 2's complement number |
| 0100 | Inverted |
| + 0001 | One Added |
| 0101 | Result |

From this example, it is seen that the magnitude of this negative numbers is five.

Likewise, to form a negative 2's complement number, the positive representation is taken, inverted, and plus binary one is added as shown.

| | |
|---|---|
| Positive number +3 | |
| Binary representation | 0011 |
| Inverted | 1100 |
| One added | + 0001 |
| Minus three in two's complement | 1101 |

The advantage of two's complement in many computers and digital processors is that addition and subtraction can be performed without regard to whether the numbers being added or subtracted are positive or negative. Examples of addition are shown in Figure 3. Note that overflows are discarded.

| | | | | | |
|---|---|---|---|---|---|
| 0001 | +1 | 0001 | +1 | 1110 | −2 |
| 0101 | +5 | 1111 | −1 | 0110 | +6 |
| 0110 | +6 | (1) 0000 | 0 | (1) 0100 | +4 |
| 0110 | +6 | 1010 | −6 | 1110 | −2 |
| 1110 | −2 | 0011 | +3 | 1101 | −3 |
| (1) 0100 | +4 | 1101 | −3 | (1) 1011 | −5 |

**Figure 3. Examples of Two's Complement Addition**

Subtraction is much like addition except that the number being subtracted (subtrahend) must be inverted and have one added to its value. It is then added to the minuend. This addition of +1 represents no problem in the hardware because the carry in ($c_n$) of the least significant adder can be used for this purpose — not an additional adder. Figure 4 shows examples of subtraction.

| | | | | |
|---|---|---|---|---|
| Minuend | 0001 +1 | 1110 −2 | 1110 −2 | 1010 −6 |
| Subtrahend | 0101 +5 | 0110 +6 | 1101 −3 | 1101 −3 |
| Minuend | 0001 | 1110 | 1110 | 1010 |
| Inverted Subtrahend | 1010 | 1001 | 0010 | 0010 |
| Add | 1011 | 0111 | 0000 | 1100 |
| Add One | 0001 | 0001 | 0001 | 0001 |
| Result (Binary) | 1100 | 1000 | 0001 | 1101 |
| Result (Decimal) | −4 | −8 | +1 | −3 |

**Figure 4. Examples of Two's Complement Subtraction.**

From these examples, one might conclude that multiplication is simply the product of one 2's complement number with the other. Unfortunately, this is not correct for negative numbers. One obvious technique for multiplication in which negative numbers are represented by 2's complements is to determine the signs and magnitudes of the operands, multiply the magnitudes, and then if the result is negative, cast the result into 2's complement form. It seems preferable, however, to devise a scheme for multiplying such numbers more simply. Booth's method will be considered for this purpose.

## BOOTH'S ALGORITHM

In the usual methods of digital multiplication, the multiplier digits are examined in turn and when the multiplier digit is a logical "1," the multiplicand is added to the running partial sum in the appropriate weight. For each multiplier digit, there is a relative one-digit shift between the multiplicand and partial sum whether there has been an addition or not. Booth's algorithm provides a tool whereby more than one shift at a time may be made, depending on the grouping of strings of logic 1's or logic 0's. This multiple shifting ability may be used to "speed up" the multiplication process.

The basic algorithm as developed by Booth is as follows: $y_i$ is the i-th most significant bit of an n-bit multiplier representation. $y_{-1}$ is zero. $y_0$ is the least significant bit. $y_{n-1}$ is the sign bit. X is the multiplicand.

Starting with i = 0, $y_i$ and $y_{i-1}$ are compared:

1.) If $y_i = y_{i-1}$; add 0X.

2.) If $y_i = 1$ and $y_{i-1} = 0$; subtract 1X (the multiplicand) from the partial product. (Add the 2's complement).

3.) If $y_i = 0$ and $y_{i-1} = 1$; add 1X to the partial product.

Two examples of these rules are shown in Figure 5.

**Example 1:**

```
1 0 1 1 1      = −9
0 1 0 1 1 (0)  = +11
-----------------------------------------
0 0 0 0 0 1 0 0 1      y0 = 1   y−1 = 0
0 0 0 0 0 0 0 0        y1 = 1   y0 = 1
1 1 1 0 1 1 1          y2 = 0   y1 = 1
0 0 1 0 0 1            y3 = 1   y2 = 0
1 0 1 1 1              y4 = 0   y3 = 1
-----------------------------------------
(1) 1 1 0 0 1 1 1 0 1      = −99
```

**Example 2:**

```
1 1 0 1 1      = −5
1 1 0 0 1 (0)  = −7
-----------------------------------------
0 0 0 0 0 0 1 0 1      y0 = 1   y−1 = 0
1 1 1 1 1 0 1 1        y1 = 0   y0 = 1
0 0 0 0 0 0 0          y2 = 0   y1 = 0
0 0 0 1 0 1            y3 = 1   y2 = 0
0 0 0 0 0              y4 = 1   y3 = 1
-----------------------------------------
(1) 0 0 0 1 0 0 0 1 1      = +35
```

**Figure 5. Examples of Booth's algorithm for two's complement multiplication**

Based on these rules as developed by Booth, it is a straight forward process to make a table of desired action for each of the four possible two-bit combinations under inspection. This is shown below. K is the partial product before this level of the algorithm and is zero initially.

**Table of Operation for Booth's Algorithm**

| $y_{i-1}$ | $y_i$ | Function | Partial Product |
|---|---|---|---|
| 0 | 0 | Do nothing | K + 0 |
| 1 | 0 | Add X | K + X |
| 0 | 1 | Subtract X | K − X |
| 1 | 1 | Do nothing | K + 0 = K − 0 |

As stated earlier, one of the initial goals is to develop an algorithm that provides the ability to look ahead more than one bit at a time. Therefore, the above table for one multiplier bit $y_i$ is expanded to Table I for two multiplier bits, $y_i$ and $y_{i+1}$.

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**TABLE I – BOOTH'S ALGORITHM FOR TWO MULTIPLIER BITS TAKEN SIMULTANEOUSLY.**

| Input | | | For | For | Net Result |
|---|---|---|---|---|---|
| $y_{i-1}$ | $y_i$ | $y_{i+1}$ | $y_{i-1}, y_i$ | $y_i, y_{i+1}$ | $y_{i-1}, y_i, y_{i+1}$ |
| 0 | 0 | 0 | K+0 | K+0 | K+0 |
| 1 | 0 | 0 | K+X | K+0 | K+X |
| 0 | 1 | 0 | K−X | K+2X | K+X |
| 1 | 1 | 0 | K−0 | K+2X | K+2X |
| 0 | 0 | 1 | K+0 | K−2X | K−2X |
| 1 | 0 | 1 | K+X | K−2X | K−X |
| 0 | 1 | 1 | K−X | K−0 | K−X |
| 1 | 1 | 1 | K−0 | K−0 | K−0 |

From Table I for two multiplier bits, the following conclusions can be drawn:

1.) The $y_{i+1}$ bit can be used as an add/subtract control where logic "0" is add and logic "1" is subtract.

2.) The function $y_{i-1} \oplus y_i$ can be used as a X weight control indicating the addition or subtraction of X to the partial product K.

3.) The function $y_{i-1}\, y_i\, \overline{y}_{i+1} + \overline{y}_{i-1}\, \overline{y}_i\, y_{i+1}$ can be used as a 2X weight control indicating the addition or subtraction of 2X to the partial product K.

4.) When in the subtract mode, the 2's complement of X ($\overline{X}$ plus one) is added. Thus the $x_i$ bits are exclusive OR'ed with the add/subtract control $y_{i+1}$. The plus one is generated in the partial product LSB by connecting the $y_{i+1}$ to the first $c_n$ of the adder used to add X and K.

5.) When 2X is being subtracted, the carry into the second LSB of the partial product is generated by connecting the first $c_n$ to $y_{i+1}$ and $x_{-1}$ to logic 0.

Thus, all required functions of Table I can be implemented using combinatorial logic elements. The resultant output is a "partial product" of the total multiplication product. Remember that if $y_{i+1}$ is 1, then y has been treated as a negative number up to that point so the partial product may not really be correct yet.

Both $y_{i-1} \oplus y_i$ and $y_{i-1}\, y_i\, \overline{y}_{i+1} + \overline{y}_{i-1}\, \overline{y}_i\, y_{i+1}$ are symmetric functions. This provides the ability to change from positive logic to negative logic ($X = \overline{X}$, $Y = \overline{Y}$) with the combinatorial functions remaining unchanged.

## THE AM25S05

The Am25S05 is an advanced Schottky MSI circuit that implements the algorithm previously developed in this application note. It can be used to multiply signed or unsigned numbers in various number representations and performs multiplications in either positive or negative logic. This discussion applies to the Am2505 and Am25L05 as well; but the Am25S05 has been assumed to provide a single device for discussion purposes.

The logic diagram of the Am25S05 is shown in Figure 6. The logic symbols and connection diagram are shown in Figure 7. The Am25S05 consists of five parts: a multiplier decoder, a shifting array, a complementer, a high speed adder, and a overflow and sign control.

### 1.) Multiplier Decoder

The multiplier decoder generates the required control signals for the shifting array and complementer. First, it decodes whether 0X, 1X or 2X of the X multiplicand is to be added to the incoming partial product. Second, the multiplier decoder generates the add/subtract command. The decoder generates the functions.

$A = y_{i-1} \oplus y_i$ 1X used

$B = y_{i-1}\, y_i\, \overline{y}_{i+1} + \overline{y}_{i-1}\, \overline{y}_i\, y_{i+1}$ 2X used

$C = \overline{P}\, \overline{y}_{i+1} + P(y_{i+1}A + \overline{y}_{i-1}\, y_i)$ add/subtract

(P input LOW = positive logic; P input HIGH = negative logic; P defined true for negative logic).

The "zero" times the multiplicand is obtained by $\overline{A}\overline{B}$. The P input controls the add/subtract sequence so that the multiplier can work in either the positive or negative logic representation. The function includes terms to handle logic "0 X" independent of the positive or negative logic representation when the decoding functions A and B are both false.

### 2.) Shifting Array

The shifting array generates 0, 1 or 2 times the multiplicand and applies this to the complementer. X is inverted through the shifting array and "0" is implemented as all HIGH's out of the array. The $x_{-1}$ input is used to shift up the next lower order bit for the 2X function.

### 3.) Complementer

The complementer consists of a set of exclusive-NOR circuits controlled by the add/subtract function. The add command applies a "0" to each exclusive-NOR while a subtract applies a "1" to each exclusive-NOR. The add command thereby causes each output of the shifting array to be inverted. Thus, the $x_i$ inputs are applied non-inverted to the high speed adder in the add mode and applied inverted in the subtract mode.

### 4.) High-Speed Adder

The high-speed adder is a 4-bit high-speed parallel carry look-ahead adder that adds the selected function of the multiplicand, X, to the partial product presented at the K inputs. The adder also has a carry input, $C_n$; a carry output $C_{n+4}$; and four sum outputs, $S_0$ to $S_3$.

### 5.) Overflow and Sign Control

At the most significant end of the array, i.e. where the sign bits are processed, a problem arises when an overflow occurs as a result of (a) an addition or subtraction or (b) the need to use 2X in the adder. To overcome these overflow situations, the sign digits of the multiplicand and partial product must be repeated twice. Luckily some logic minimization is possible and the $S_4$ and $S_5$ outputs, which are the most significant bits of the 6-bit signed product, can be generated quite easily. These two outputs are required only at the most significant end of each iterative step of a multiplication. In order to re-

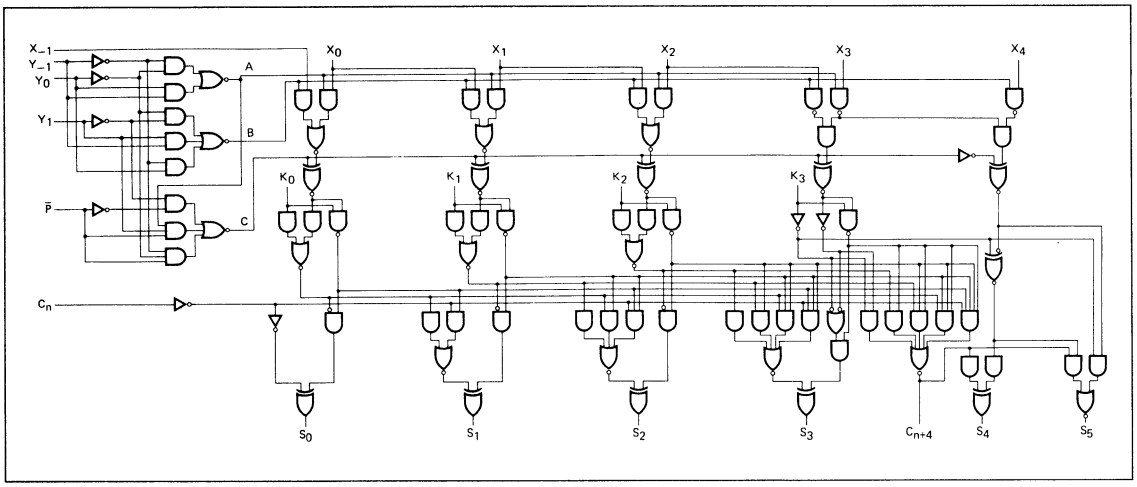


**Figure 6. Logic Diagram for the Am25S05**

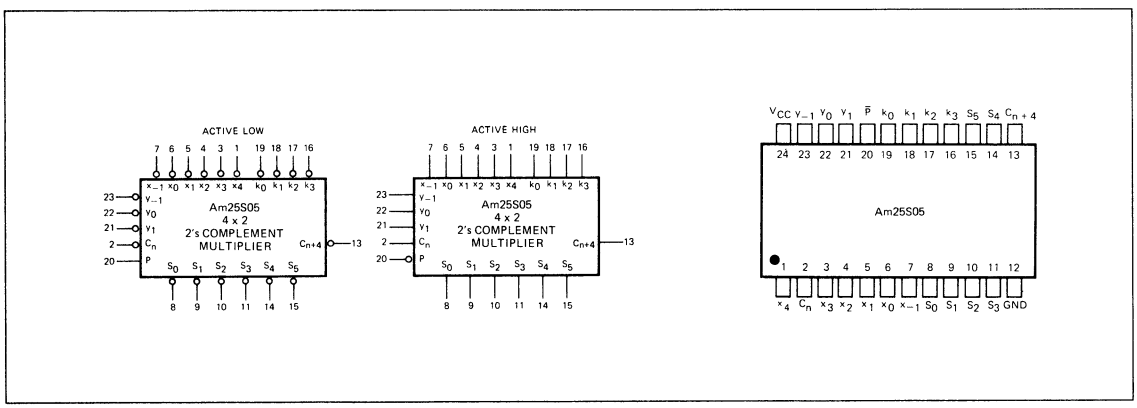


**Figure 7. Logic Symbol and Connection Diagram for the Am25S05**

duce input loading on $x_3$, an additional $x_4$ input is provided which is a part of this overflow circuitry. The $x_4$ input must be connected to $x_3$ at the most significant end of the array only and can be left unconnected elsewhere.

## ITERATIVE ARRAYS USING THE Am25S05

Since the Am25S05 is a 2 x 4 multiplier and performs the arithmetic function S = XY + K, it can be used as an iterative cell in multiplication schemes. The number of multiplier devices required for the multiplication of a n-bit X by an m-bit Y is given by

$$\text{Number of devices} = \left(\frac{n}{4}\right)\left(\frac{m}{2}\right)$$

where X and Y are the multiplicand and multiplier, respectively. (Note – fractions must be rounded up).

When the array is extended, only the $S_0$ through $S_3$ outputs are used in the partial product until the most significant end of the array is reached. Then, the $S_4$ and $S_5$ outputs are used for the most significant bits. Thus, a 4 x 2 multiplication gives a 6-bit output; an 8 x 2 multiplication gives a 10-bit output; a 12 x 2 multiplication gives a 14-bit output and so forth. For the 12 x 2 multiplication case, $S_0$ through $S_3$ are the outputs of the two least significant multipliers and $S_0$ through $S_5$ are the outputs of the most significant multiplier to provide the 14-bit result. When the multiplier array is expanded in the Y direction, it is expanded on a row by row basis. The S outputs of one row are connected to the K inputs of the following row that are shifted up by two bits in the X direction (A weight of $2^2 = 4$). The two least significant output bits not connected ($S_0$ and $S_1$) provide two of the array outputs.

Figure 8 shows four Am25S05's connected to form a 4 x 8 array that produces a 2's complement product from a 4-bit 2's complement multiplier and an 8-bit 2's complement multiplicand. The scheme is shown for the positive logic representation; for the negative logic representation, P must be held high rather than LOW, and '1's and '0's must be reinterpreted. Since the first iteration is treated as if the previous operation were an addition, the $x_{-1}$ and $y_{-1}$ inputs are held at logic '0'. The $S_4$ and $S_5$ outputs are ignored except at the most significant edge of the array. The K inputs allow the accumulation

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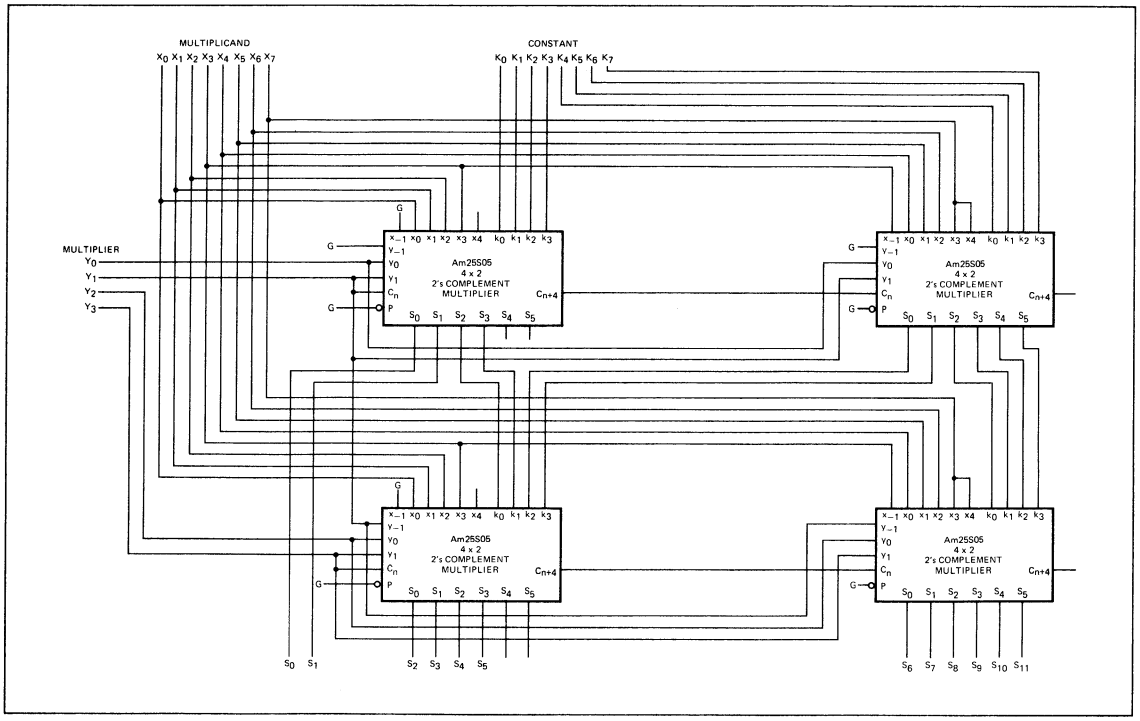



**Figure 8. 2's Complement 8 x 4 Multiplication. Active High Levels**

of partial products as information passes through the array.

Since at the first stage the partial product does not exist, the K inputs can be used to add in a number at the least significant end of the product. Otherwise the K inputs should be held at logic '0'. This feature is very useful as many arithmetic processes consist of a series of multiplication and additions, and these K inputs may save additional devices. For multiplication with longer word lengths, the array can be extended in both the X and Y directions.

Figure 10 shows the straightforward method of stacking multipliers so as to accumulate partial products and generate a resultant product.

Figure 9 diagrammatically shows the connection scheme for the 12 x 12 multiplier of Figure 10, the straightforward parallelogram structure. The longest propagation delay path is shown by the arrow. The typical propagation delay of this path is computed as shown in Table II. Note that this is not the maximum speed connection.

In the diagram of Figure 9, the shorthand notation inside the individual multiplier notation represents the "system" bit numbers connected to the $y_0$ and $x_0$ bits respectively. Thus, if the system words are A and B, 4·8 represent $A_4$ is connected to $y_0$ of that multiplier element and $B_8$ is connected to $x_0$ of that multiplier element. Remember, each individual Am25S05 is labeled $y_{-1}$, $y_0$, $y_1$, $x_{-1}$, $x_0$, $x_1$, $x_2$, $x_3$ and $x_4$. When connected in an iterative system, these inputs should be relabeled to $y_{i-1}$, $y_i$, $y_{i+1}$, $x_{j-1}$, $x_j$, $x_{j+1}$, $x_{j+2}$, $x_{j+3}$ and $x_{j+3}$ (not $x_{j+4}$). Then the ij nomenclature inside the element is for the subscript of the system bit numbers.

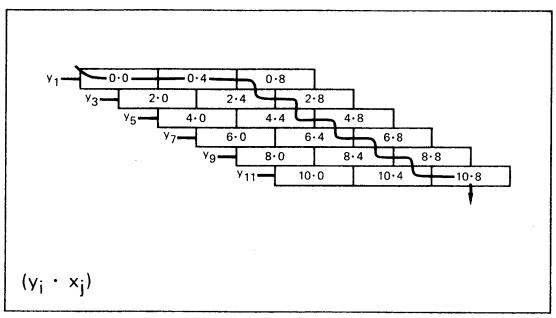



**Figure 9. Diagrammatical Representation of Standard 12 x 12 Parallelogram Structure and Longest Propagation Path**

**TABLE II — CALCULATION OF TYPICAL PROPAGATION DELAY FOR PARALLELOGRAM 12 x 12 MULTIPLIER**

| | $t_{PLH}$ Typical | $t_{PHL}$ Typical | $\frac{t_{PLH} + t_{PHL}}{2}$ |
|---|---|---|---|
| $y_i$ to $C_{n+4}$ | 23 ns | 20 ns | 21.5 ns |
| $C_n$ to $C_{n+4}$ | 8 ns | 9 ns | 8.5 ns |
| $C_n$ to $S_{03}$ | 12 ns | 10 ns | 11.0 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10 ns | 8.25 ns |
| 4 Additional $C_n$ to $S_{03}$ and $k_i$ to $C_{n+4}$ paths | | | 77.0 ns |
| $C_n$ to $S_{45}$ | 15 ns | 13 ns | 14.0 ns |
| | | Total | 140.25 ns |

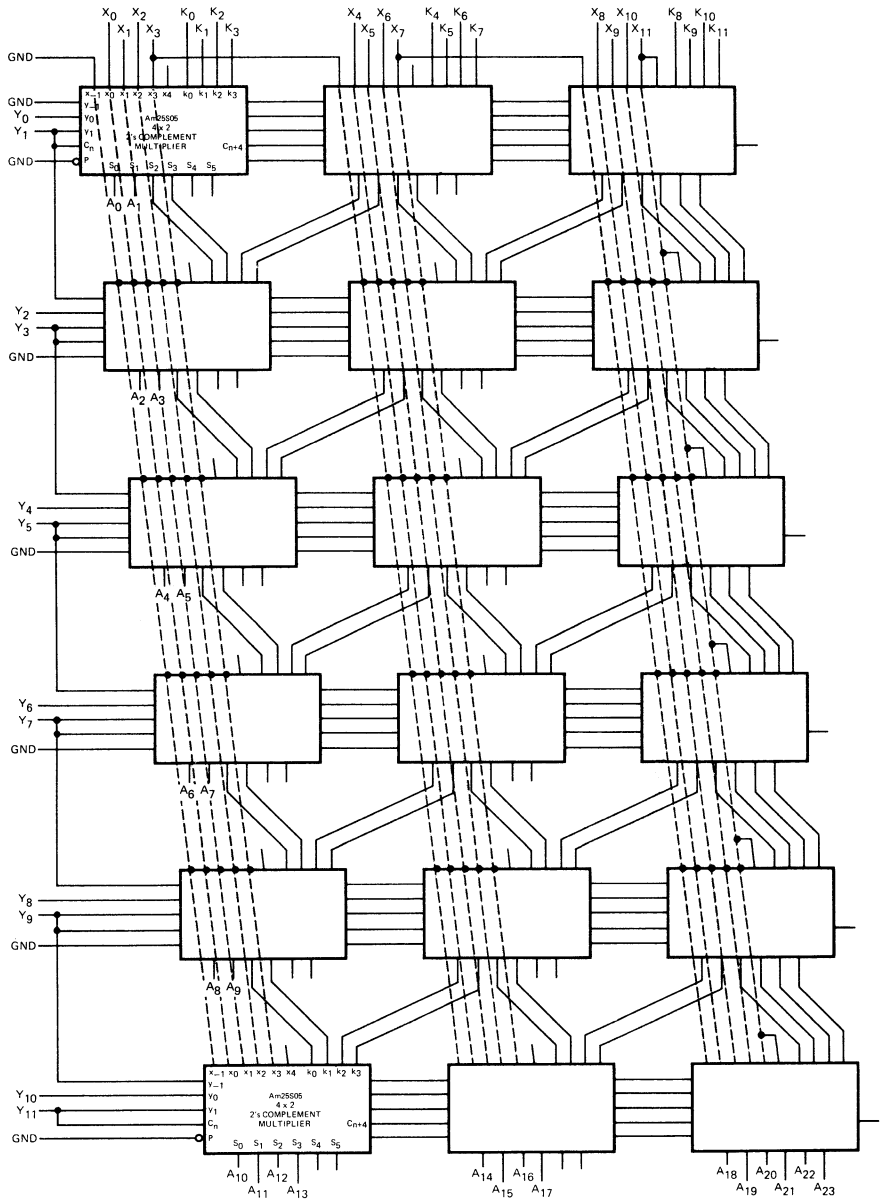



**Figure 10. 12 x 12 Multiplier in Parallelogram Structure**

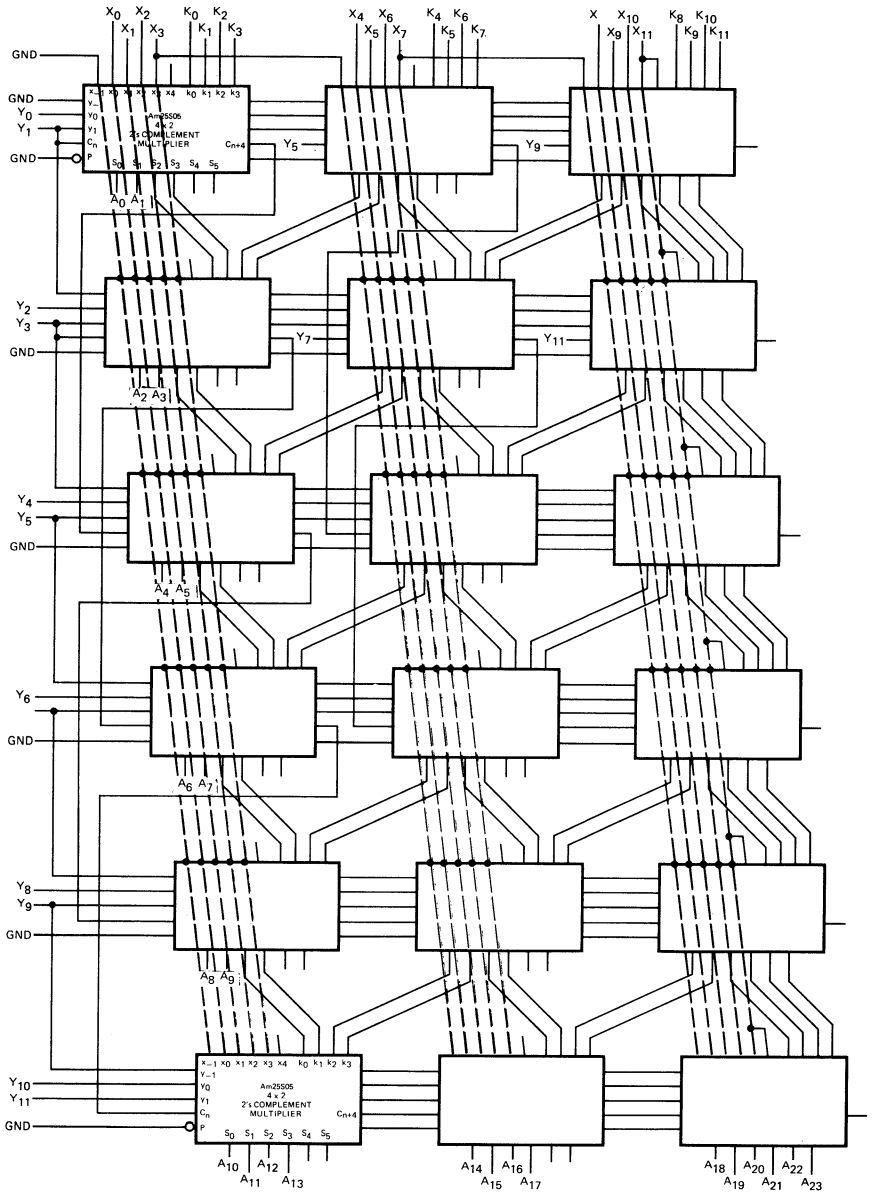



**Figure 11. High Speed 12 x 12 2's Complement Multiplication**

A second, faster configuration for the connection of a 12 x 12 multiplier in a parallelogram-type structure is shown in the connection diagram of Figure 11 and diagramatically in Figure 12. The significant difference between the connection in Figure 11 and the connection in Figure 10 involves the y inputs connected to the carry inputs. Notice in Figure 10 that there are y inputs going into carry inputs down the left edge of the array to add "1" at the LSB of the partial product during subtraction. Every odd $y_{i+1}$ goes into a carry of weight i. However, within the array there are carry signals lying in the critical speed path with the same weight as these y inputs. By interchanging some of these y inputs with carries higher up in the array, it is possible to shorten the critical speed path. For example, the carry out of the first Am25S05 has a weight of $2^4$ as does the $y_5$ input in the third row carry in. By interchanging these two signals as shown in Figure 11, the first Am25S05 is removed from the critical speed path. The carry between the first and second devices in the second row has a weight of $2^6$ and may be interchanged with the $y_7$ signal. This interchanging may be continued across and down the array wherever applicable. The general philosophy of this method is to equalize the delays through the array from the top to all parts of the output rather than having some output bits available very rapidly and others more slowly. The result is that the longest propagation delay path will also be decreased. Table III shows the computation for the typical propagation delay of the longest path for this connection.

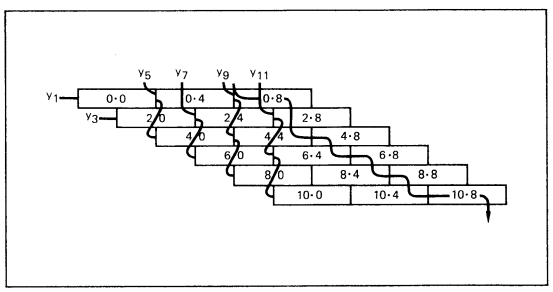



**Figure 12. Diagrammatical Representation of High-Speed 12 x 12 Parallelogram Structure and Longest Propagation Path**

**TABLE III – CALCULATION OF TYPICAL PROPAGATION DELAY FOR 12x12 MULTIPLIER WITH CARRIES MOVED**

| | $t_{PLH}$ Typical | $t_{PHL}$ Typical | $\frac{t_{PLH} + t_{PHL}}{2}$ |
|---|---|---|---|
| $y_i$ to $S_{03}$ | 23 ns | 23 ns | 23 ns |
| $k_i$ to $S_{03}$ | 13.5 ns | 9.5 ns | 11.5 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10 ns | 8.25 ns |
| $C_n$ to $S_{03}$ | 12 ns | 10 ns | 11.0 ns |
| 2 Additional $k_i$ to $C_{n+4}$ and $C_n$ to $S_{03}$ paths | 2(8.25 +11.0)ns | | 38.5 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10 ns | 8.25 ns |
| $C_n$ to $S_{45}$ | 15 ns | 13 ns | 14.0 ns |
| | | Total | 114.5 ns |

A third configuration for a 12 x 12 multiplier is shown diagrammatically in Figure 13. In this structure, four of the Am25S05's have been moved vertically while maintaining the relative partial sum weights. This results in an increase in speed over the standard parallelogram structure by decreasing the maximum propagation path length. The speed of this triangular structure, Figures 13 and 15, is the same as that of the parallelogram structure with carries moved, Figures 11 and 12.

Figure 14 diagrammatically illustrates the connection scheme for 16 x 16 arrays connected in the three types of structures previously described. In each method the carry-in connection

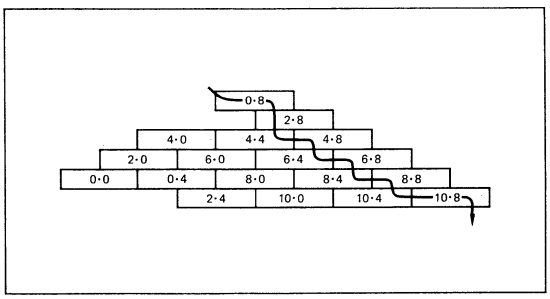



**Figure 13. Diagrammatical Representation of 12 x 12 Multiplier in Triangular Array**

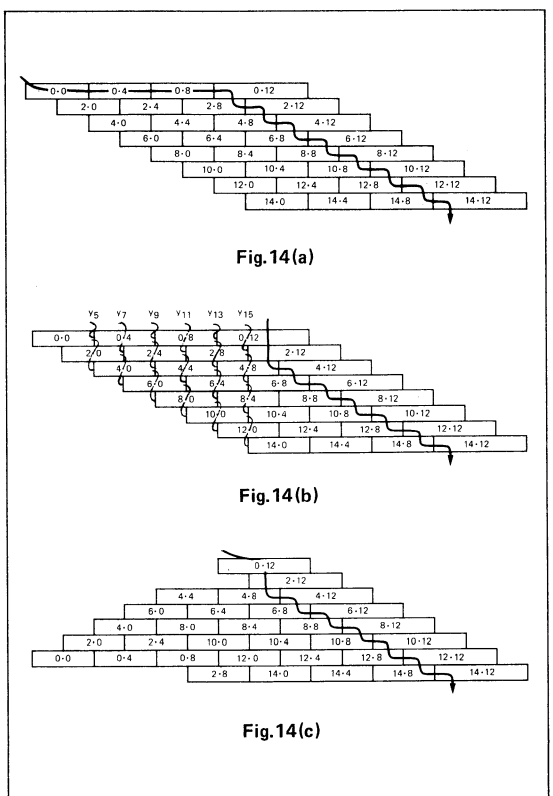



**Figure 14. 16 x 16 Multiplier Connection Schemes**

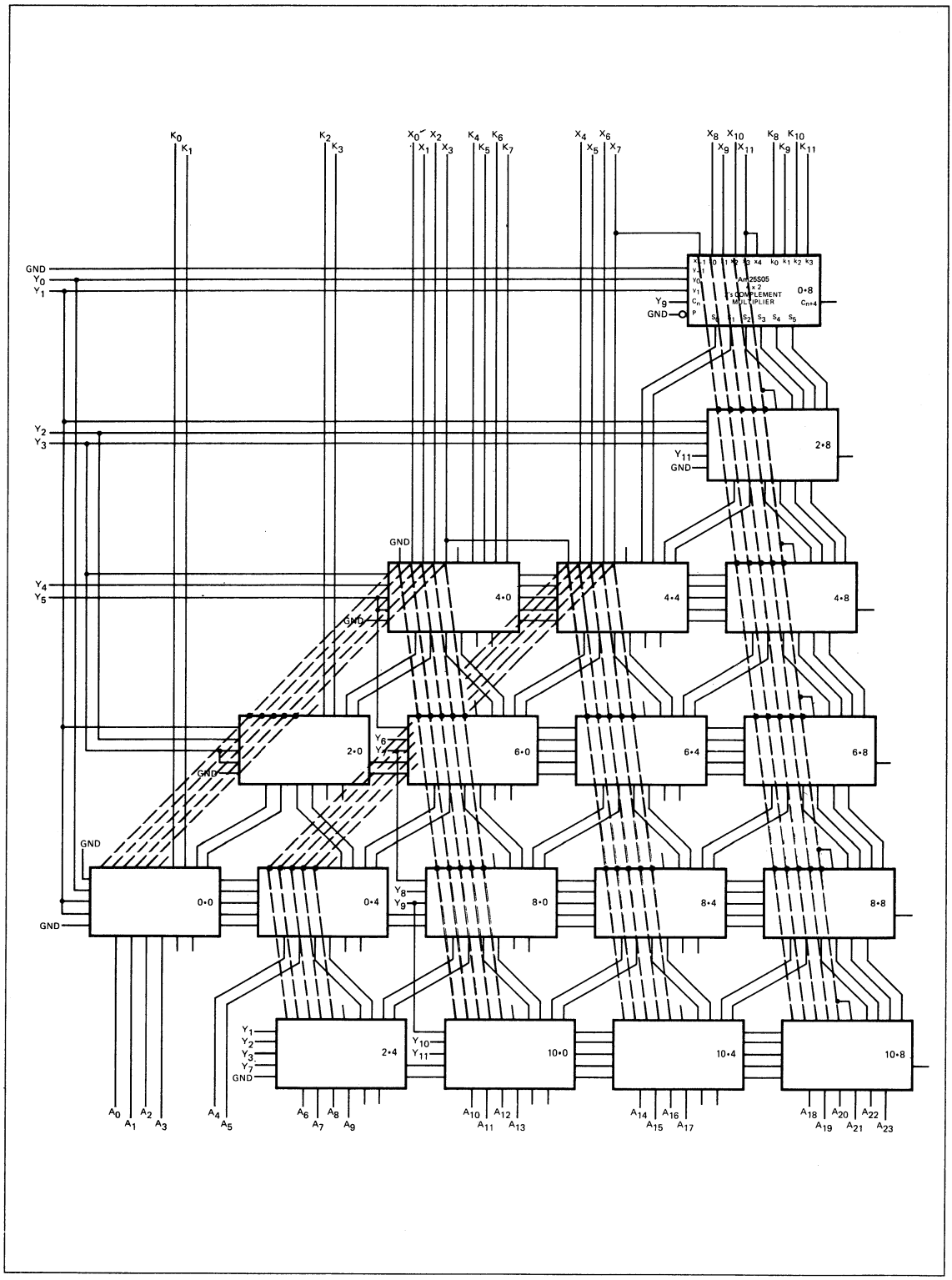



**Figure 15. Connection for 12 x 12 Configuration in the Triangular Array.**

**TABLE IV – TYPICAL MULTIPLICATION TIME IN NANOSECONDS.**

| Array Size Y x X | Number of Am25S05's | Time (ns) Method 1 | Time (ns) Method 2 Method 3 |
|---|---|---|---|
| 4 x 4 | 2 | 39 | – |
| 4 x 8 | 4 | 55 | – |
| 4 x 12 | 6 | 64 | – |
| 8 x 8 | 8 | 94 | 76 |
| 8 x 12 | 12 | 102 | 94 |
| 8 x 16 | 16 | 111 | 102 |
| 12 x 12 | 18 | 141 | 115 |
| 12 x 16 | 24 | 149 | 132 |
| 12 x 20 | 30 | 157 | 141 |
| 16 x 16 | 32 | 188 | 153 |
| 16 x 20 | 40 | 196 | 171 |
| 16 x 24 | 48 | 205 | 179 |
| 20 x 20 | 50 | 235 | 192 |
| 20 x 24 | 60 | 243 | 209 |
| 20 x 28 | 70 | 251 | 218 |
| 24 x 24 | 72 | 282 | 230 |
| 24 x 28 | 84 | 290 | 248 |
| 24 x 32 | 96 | 299 | 256 |
| 28 x 28 | 98 | 329 | 269 |
| 28 x 32 | 112 | 337 | 286 |
| 32 x 32 | 128 | 376 | 307 |

to the $C_n$ level is shown. If no connection is shown, it is assumed that $C_{n+4}$ is connected to the next $C_n$. Table IV shows the delays and package count for various size multiplier arrays using these three connection methods.

## FASTER MULTIPLICATION USING ADDITIONAL ADDERS

If faster multipliers are required, the multiplication array can be split into several parts and the partial products from these parts added using high-speed carry look-ahead adders. This method results in a substantial increase in speed – especially for larger multipliers – with relatively few additional packages. One connection for a 16 x 16 multiplier using one level of additional partial product adders is shown diagrammatically in Figure 16.

This method involves breaking the array into two 8 x 16 indirectly structured arrays. The first contains all X connections and the Y connections to the 0, 1, 4, 5, 8, 9, 12 and 13 bits. The second array contains all X connections and the Y connections to the 2, 3, 6, 7, 10, 11, 14 and 15 bits. In all cases, the $Y_{i-1}$ bit is connected to the correct weight bit. For example, $Y_{i-1}$ is connected to bit 5 for $Y_0 = 6$ and $Y_1 = 7$. Notice that for both 8 x 16 structures, the $Y_{i-1}$ bits are cross coupled to the other array. The typical speed computation for this connection is shown in Table V.

Another connection scheme for a 16 x 16 multiplier using three additional partial product adders (two levels) is shown in Figure 17. Here, the multiplier is broken into four 4 x 16 arrays. Then the outputs of two of the arrays are combined in one high-speed adder and at the same time the outputs of the other two arrays are combined in another high speed adder.

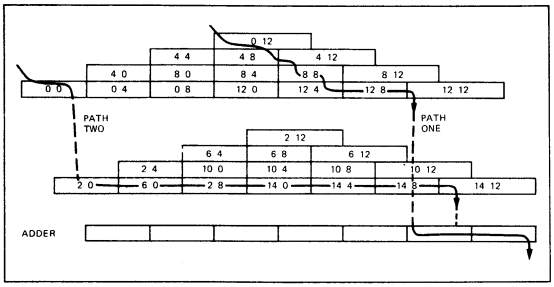



**Figure 16. Multiplier Connection with One Level of Additional Adders**

**TABLE V – CRITICAL PROPAGATION DELAY PATH FOR 16 x 16 MILTIPLIER WITH ONE LEVEL OF ADDERS.**

| Path One | $t_{PLH}$ Typical | $t_{PHL}$ Typical | $\frac{t_{PLH} + t_{PHL}}{2}$ |
|---|---|---|---|
| $Y_i$ to $S_{03}$ | 23.0 ns | 23.0 ns | 23.0 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10.0 ns | 8.25 ns |
| $C_n$ to $S_{03}$ | 12.0 ns | 10.0 ns | 11.0 ns |
| $k_i$ to $S_{03}$ | 13.5 ns | 9.5 ns | 11.5 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10.0 ns | 8.25 ns |
| $C_n$ to $C_{n+4}$ | 8.0 ns | 9.0 ns | 8.5 ns |
| $C_n$ to $S_{03}$ | 12.0 ns | 10.0 ns | 11.0 ns |
| A to $C_{n+4}$ | Am54S/74S181 | Assumed | 12.5 ns |
| $C_n$ to F | Am54S/74S181 | Assumed | 7.0 ns |
| | | | Total 101.0 ns |
| **Path Two** | | | |
| $Y_i$ to $S_{03}$ | 23.0 ns | 23.0 ns | 23.0 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10.0 ns | 8.25 ns |
| $C_n$ to $C_{n+4}$ | 8.0 ns | 9.0 ns | 8.5 ns |
| 4 Additional $C_n$ to $C_{n+4}$ | 4(8.5 ns) | | 34.0 ns |
| $C_n$ to $S_{03}$ | 12.0 ns | 10.0 ns | 11.0 ns |
| B to $C_{n+4}$ | Am54S/74S181 | Assumed | 12.5 ns |
| $C_n$ to F | Am54S/74S181 | Assumed | 7.0 ns |
| | | | Total 104.25 ns |
| | | | ~105 ns |

The resultant sums of the two high speed adders are combined in a third high speed adder which gives the total multiplication result. The typical speed computation for the longest path of this connection is shown in Table VI.

The advantage of the scheme shown in Figure 17 is that about one-half of the total delay is in the external adder. A further decrease in the average multiplication time can be achieved by storing the partial sums in registers or latches, then adding the stored parts in the high speed adders. This results in a two-step time sequenced mode of operation.

## TIME-SEQUENCED MULTIPLIERS

The Am25S05 can be used as the main element in a time-sequenced multiplier. This is illustrated in Figure 18. The multiplier and partial product are shifted two places after each

iteration. Three single-length registers are required: one holds the multiplicand; the other two hold the double-length product. The least significant part of this double-length register originally holds the multiplier, which is sequentially shifted out during the computation. A shift of two places is obtained by splitting the multiplier and partial product into odd and even parts and placing the odd bits in one shift register and the even bits in the other. A shift of one place of both registers then effectively acts as a shift of two places.

The scheme can be extended to use any number of even multiplier bits. As the number of bits increases, the multiplication time increases, and the amount of ancillary hardware increases. When Am25S05's are used in a combinational array, the array does not require any additional devices. Time-sequenced multipliers are worthwhile mainly if the word lengths are long or if the auxiliary registers can be shared with other arithmetic operations. This is one example of a serial-parallel multiplier.

## INTEGER MULTIPLICATION

The Am25S05 can multiply 2's complement numbers in either integer or fractional form. The primary difference is in the thought process of the designer. When the binary patterns are treated as integers, the 2's complement numbers can be represented as

$$X = x - x_s\,2^{n-1}$$
$$Y = y - y_s\,2^{m-1}$$
$$K = k - k_s\,2^{p-1}$$

where

$x_s$ = sign bit of X (one or zero)
$y_s$ = sign bit of Y (one or zero)
$k_s$ = sign bit of K (one or zero)
x = magnitude bits of X (less sign)
y = magnitude bits of Y (less sign)
k = magnitude bits of K (less sign)
n = number of bits in X word
m = number of bits in Y word
p = number of bits in K word

For example, if six bits are assumed for X, n = 6 and the sign bit has a weight of $-2^{6-1} = -2^5 = -32$. The other magnitude bits have their normal weight and since there are five other magnitude bits, they are $2^0$, $2^1$, $2^2$, $2^3$, and $2^4$. Thus, 2's complement integer numbers for n = 6 bits are as shown below:

| Integer Decimal Number Equivalent | Magnitude bits | | | | | |
|---|---|---|---|---|---|---|
| | $-2^5$ Sign | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | −32 | 16 | 8 | 4 | 2 | 1 |
| 14 | 0 | 0 | 1 | 1 | 1 | 0 |
| 31 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| −7 | 1 | 1 | 1 | 0 | 0 | 1 |
| −25 | 1 | 0 | 0 | 1 | 1 | 1 |
| −32 | 1 | 0 | 0 | 0 | 0 | 0 |

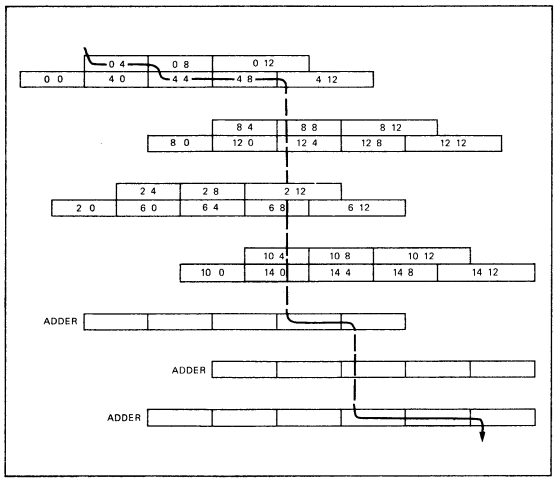



**Figure 17. Multiplier Connection with Two Levels of Additional Adders**

**TABLE VI – CRITICAL PROPAGATION DELAY PATH FOR 16 x 16 MULTIPLIER WITH TWO LEVELS OF ADDERS**

| | $t_{PLH}$ Typical | $t_{PHL}$ Typical | $\frac{t_{PLH} + t_{PHL}}{2}$ |
|---|---|---|---|
| $y_i$ to $C_{n+4}$ | 23.0 ns | 20.0 ns | 21.5 ns |
| $C_n$ to $S_{03}$ | 12.0 ns | 10.0 ns | 11.0 ns |
| $k_i$ to $C_{n+4}$ | 6.5 ns | 10.0 ns | 8.25 ns |
| $C_n$ to $C_{n+4}$ | 8.0 ns | 9.0 ns | 8.5 ns |
| $C_n$ to $S_{03}$ | 12.0 ns | 10.0 ns | 11.0 ns |
| A to $C_{n+4}$ | Am54S/74S181 Assumed | | 12.5 ns |
| $C_n$ to F | Am54S/74S181 Assumed | | 7.0 ns |
| A to $C_{n+4}$ | Am54S/74S181 Assumed | | 12.5 ns |
| $C_n$ to $C_{n+4}$ | Am54S/74S181 Assumed | | 7.0 ns |
| $C_n$ to F | Am54S/74S181 Assumed | | 7.0 ns |
| | | Total | 106.75 ns |

When the product of X and Y is considered, the following equation results:

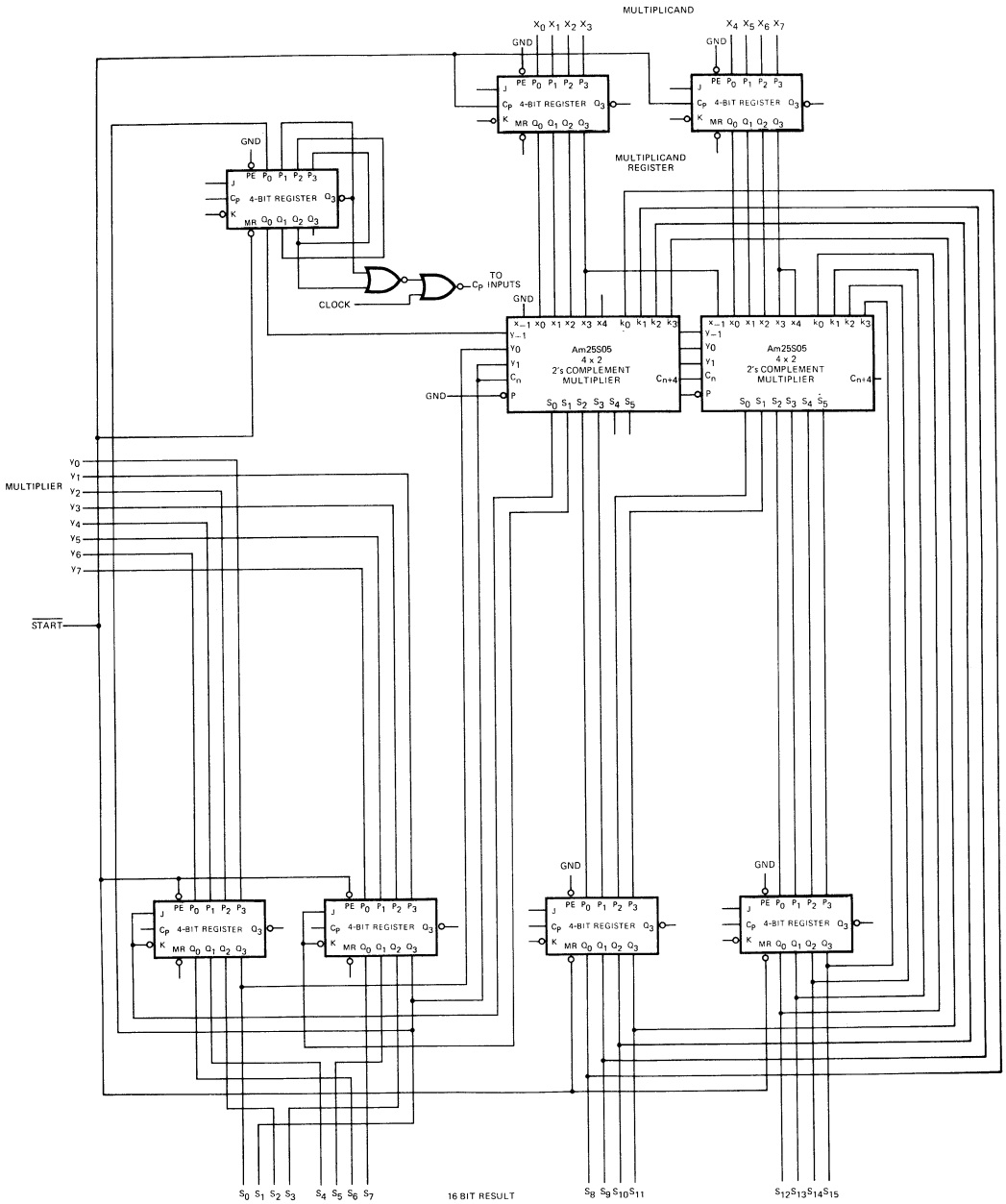
$$S = XY = x_s y_s\,2^{m+n-2} - xy_s\,2^{m-1} - yx_s\,2^{n-1} + xy$$

The 2's complement product requires m + n bits in order to represent all possibilities. Note that there is only one condition where the m + n bits are required; that condition being:

$$X = -2^{n-1} \text{ and } Y = -2^{m-1}$$

This condition gives $S = XY = 2^{m+n-2}$ which requires m + n digits in a 2's complement signed integer number.

Consider n = 6 and m = 4, then $x_s$ has weight −32 and $y_s$ has weight −8. For X = −32 and Y = −8, the product XY is +256. The 2's complement representation is 0100000000. Ten bits are required to properly represent the 2's complement number. All other combinations of values for X and Y require only m + n −1 bits to represent the 2's complement number. For n = 6 and m = 4 in this case, the ninth bit represents the product sign. Consider (+7) x (−31) is equal to −217 or




Note: 4-bit register is Am54S/74S195

**Figure 18. 8 x 8 Time Sequenced Multiplier**

100100111. Notice that 1100100111, the ten bit 2's complement representation is identical in value.

The *general* requirement for the product solution of XY is:

$$S = XY = s - s_s\, 2^{m+n-1}$$

and all binary operations must be carried through m + n bits in the product soltuion unless a simplification is assumed.

In the Am25S05 (as well as the Am2505 and Am25L05), the sum output, S, of the device is:

$$S = XY + K.$$

This can be seen in Figure 6.

The devices are designed such that in an iterative array, the K inputs to the adder are available only at the initial least significant partial product input. Thus in an iterative system, the sum is defined as:

$$S = x_s y_s\, 2^{m+n-2} - xy_s\, 2^{m-1} - (yx_s + k_s)\, 2^{n-1} + xy + k$$

The $k_s$ term can contribute at weight $2^{n-1}$ and the k term at weight $2^0 = 1$. Thus, m + n bits are sufficient to contain all possible values of S = XY + K.

## FRACTIONAL MULTIPLICATION

Fractional multiplication using the Am25S05 is identical with integer multiplication but the notation is changed. The fractional number range is usually limited to $-1 \leqslant X \leqslant 1-2^{-(n-1)}$.

The fractional 2's complement binary numbers can be represented as:

$$X = x\, 2^{-(n-1)} - x_s$$
$$Y = y\, 2^{-(m-1)} - y_s$$
$$K = k\, 2^{-(p-1)} - k_s$$

where the notation is as with integer arithmetic. The sign bit now has a weight of $-2^0 = -1$ and the other magnitude bits have their normal fractional weight.

Two's complement numbers for n = 6 are as shown below.

| Fractional Equivalent | $-2^0$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ |
|---|---|---|---|---|---|---|
| | −1 | 1/2 | 1/4 | 1/8 | 1/16 | 1/32 |
| 14/32 = 7/16 | 0 | 0 | 1 | 1 | 1 | 0 |
| 31/32 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| −7/32 | 1 | 1 | 1 | 0 | 0 | 1 |
| −25/32 | 1 | 0 | 0 | 1 | 1 | 1 |
| −32/32 = −1 | 1 | 0 | 0 | 0 | 0 | 0 |

The notation difference in the fractional representation is that all the integer representations have been divided by $2^{(n-1)}$.

The fractional product XY is

$$S = XY = x_s y_s - x_s y\, 2^{-(m-1)} - y_s\, x\, 2^{-(n-1)} + xy\, 2^{-(m+n-2)}$$

Again, m+n bits are required to cover all possible combinations. Note that X = −1 and Y = −1 results in XY = +1 which is beyond the normal range. In order to cover this possibility, the sign bit should be given a weight of −2 (instead of −1); the next most significant bit is weight +1, the next is +1/2, and so forth. If the −1 times −1 possibility is excluded only m+n−1 bits are required.

The Am25S05 used in an iterative structure produces a fractional sum S = XY + K, but the K inputs are now at the same weight as the least significant partial product inputs. Thus $K = k\, 2^{-(m+n-2)} - k_s\, 2^{-(m-1)}$. The sum is:

$$S = XY + K = x_s y_x - (x_s y + k_s)\, 2^{-(m-1)} - y_s\, x\, 2^{-(n-1)} + (xy + k)\, 2^{-(m+n-2)}$$

This general equation requires the sign bit to have a weight of −2 and all arithmetic to be carried to m+n bits to represent the two's complement solution.

In conventional minicomputer 2's complement multiplication of fractional numbers, the product, S, has only m+n−1 bits and is constrained in the range of $-1 \leqslant S \leqslant 1-2^{-(m+n-2)}$ with the most significant bit (sign bit) having a weight of −1. Outside of this range, an overflow indication is given. The Am25S05 produces a product of m+n digits so that all product results XY+K are correctly represented and the sign bit has weight −2. Notice that if K = 0 (the condition in conventional machine multiplication), m+n digits are required only for X = Y = −1. Thus if S is used with m+n−1 bits, the most significant bit of the Am25S05 array can be ignored, and an overflow indication can be generated by $S_{-2} \oplus S_{+1}$ ($S_5 \oplus S_4$ on the most significant Am25S05 output).

In fractional notation, the K inputs add to the least significant end of the adder. If K is negative, the $k_s$ bit is in effect repeated completely across the most significant part of the product via the $x_4$ input and $S_4$ and $S_5$ outputs. If a double length K addition is required, an adder can be appended to the most significant part of the product with the carry-in terminal connected to $k_s$ so that the "1"s across the most significant part of the product are removed and the desired most significant bits added. Figure 19 shows a 4 x 4 multiplication with double length addition while Figure 20 shows numeric examples of 4 x 4 multiplications.

In the connection scheme of Figure 19, an Am25S05 has been used as an adder to provide the desired overflow operation at the most significant end of the word. With the y input connection shown, the adder performs S = X plus K with the $S_4$ output correct for this 2's complement number range. The $S_5$ output is not used. If K is limited to the range of $-1\text{-}1/8 \leqslant K \leqslant \frac{63}{64}$, an adder such as the Am54S/74S181 or Am54S/74S283 can be used to perform the addition of the most significant K bits. In this case only 8 bits will be required to represent the product and it will be in the range of $-2 \leqslant S \leqslant 1\ \frac{63}{64}$.

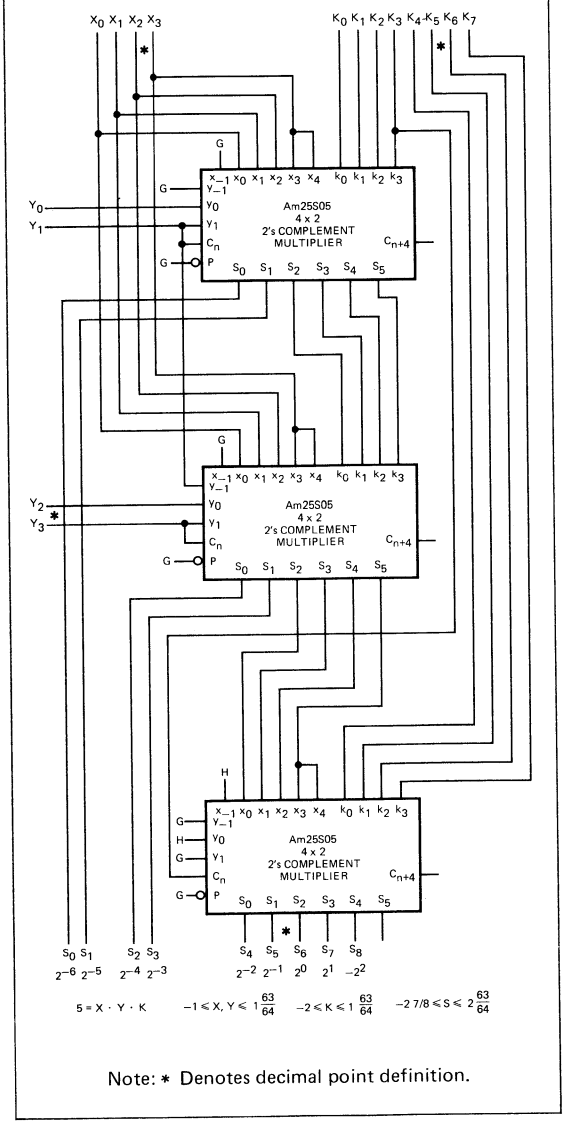



**Figure 19. 4 x 4 Fractional Double Length Multiplication and Addition.**

| | OVER-FLOW | −1 | 1/2 | 1/4 | 1/8 | 1/16 | 1/32 | 1/64 | Fractional value |
|---|---|---|---|---|---|---|---|---|---|
| Example #1 | | | | | | | | | |
| X | | 0 | 1 | 0 | 1 | | | | 5/8 |
| Y | | 0 | 0 | 1 | 1 | | | | 3/8 |
| XY | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 15/64 |
| +K | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3/64 |
| | Sign extended via $k_s$ | | | | | | | | |
| XY+K | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 18/64 |
| Example #2 | | | | | | | | | |
| X | | 1 | 0 | 0 | 0 | | | | -7/8 |
| Y | | 0 | 1 | 0 | 0 | | | | 1/2 |
| XY | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | -28/64 |
| +K | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -1/64 |
| | Sign extended via $k_s$ | | | | | | | | |
| XY+K | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | -29/64 |
| Example #3 | | | | | | | | | |
| X | | 1 | 1 | 0 | 1 | | | | -3/8 |
| Y | | 1 | 0 | 0 | 1 | | | | -7/8 |
| XY | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | |
| +K | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Sign extended via $k_s$ | | | | | | | | |
| XY+K | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 21/64 |

**Figure 20. Three Examples of Two's Complement 4 x 4 Multiplications**

## ROUND-OFF

It is often convenient to use only the most significant half of a product. This product should be rounded off; that is, it should approximate the best n-bit answer possible. This can be done by examining the least significant half of the product, and if it is greater than or equal to a certain value, (normally 1/2 that of the least significant digit of the truncated product) adding a '1' to its most significant position.

Forming a rounded t-bit product from a conventional product constrained within the range $-1 \leqslant S \leqslant 1-2^{-(m+n-2)}$ can be accomplished by adding a '1' to the K input at weight $2^{-t}$. For the case where t = m = n, this is one k position lower than the K sign digit. An example of rounding for t = m = n = 4 is shown below.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| X | = | 0. | 0 | 1 | 1 | | | = 3/8 |
| Y | = | 0. | 1 | 0 | 1 | | | = 5/8 |
| XY | = | 00. | 0 | 0 | 1 | 1 | 1 | = 15/64 |
| +K | = | 00. | 0 | 0 | 0 | 1 | 0 | 0 |
| S | = | 00. | 0 | 1 | 0 | 0 | 1 | 1 |

Rounded t-bit product from the 2t-bit product is

| | | | | | | |
|---|---|---|---|---|---|---|
| S | = | 0. | 0 | 1 | 0 | = 1/4 |

For the case m = 4 and n = 8, the sum of n+m is 12. If a six bit rounded product is desired, a "1" is added at weight $2^{-6}$. If an eight bit rounded product is desired, a one is added at weight $2^{-8}$.

If the sum output is not constrained as before but covers the range $-2 \leqslant S \leqslant 2-2^{-(m+n-2)}$, care must be taken when rounding. For the case where m = n is rounded to m(or n) bits the "1" is to be added at the $k_s$ (sign) weight. The multiplier would treat this as a negative $k_s$ sign bit and it would be extended up through the array most significant bit. Therefore, this connection cannot be made. It is recommended that for this case, the $k_s$ sign bit be connected to logic "0" and all lower order k bits be connected to logic "1". This comes very near the desired rounding criteria; otherwise an additional adder is required at the output to add a one at the $k_s$ weight only.

## TABLE VII – WORST CASE EFFECT OF TRUNCATION BY REMOVING MULTIPLIERS

| 12 bit LSB | | Truncated Bits | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ | Multiplier |
| 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | removed |
| | | | | | | | | | (1) | 1 | 1 | 1 | 1 | 0·0 removed |
| | | | | | | | (1) | 1 | 1 | 1 | 1 | | | 2·0 removed |
| | | | | | | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | effect |
| | | | | | 1 | 1 | 1 | 1 | ⊗ | | | | | 0·4 removed |
| | | | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | effect |
| | | | | | 1 | 1 | 1 | 1 | 1 | | | | | 4·0 removed |
| | | | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | effect |
| | | | 1 | 1 | 1 | 1 | ⊗ | | | | | | | 2·4 removed |
| | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | effect |
| | | | 1 | 1 | 1 | 1 | 1 | | | | | | | 6·0 removed |
| | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | effect |

### TRUNCATION

If the user is prepared to accept a truncated product where the product is incorrect by some fraction of a least significant digit, the number of IC's required for the multiplication can be reduced. The designer can determine the accuracy required for his application and remove packages as long as the error does not exceed the desired accuracy.

A simple procedure for examining the effects of removing each Am25S05 is as follows. Each 4 x 2 multiplier can effect 5 bits of the output partial product by its $S_0$, $S_1$, $S_2$, $S_3$, and $C_{n+4}$ output. As each package is removed, the effect on each bit level can be evaluated by summing the total bits involved.

This is best shown by an example. Assume a 12 x 12 multiplier with a 24-bit result (Reference Figure 12). When the 0·0 multiplier (yx) is removed, the 5 LSB's are effected. If the 2·0 multiplier is removed, then the first eight LSB's are effected as shown in Table VII. If the 0·4 multiplier is also removed, then two multipliers have been removed from row one and one multiplier from row two. Only the first nine bits of row one can be effected by the removal of two multipliers. Since $C_{n+4}$ of 0·0 was considered before, the $S_0$ bit of 0·4 cannot be added a second time. Therefore, when the 0·4 multiplier is removed, only the $S_1$, $S_2$, $S_3$ and $C_{n+4}$ bits effect the result. This is shown in Table VII by cancelling the $S_0$ bit of "0·4 removed". When the 4·0 multiplier is removed from row 3 the $S_0$, $S_1$, $S_2$, $S_3$ and $C_{n+4}$ bits effect the result. When the 2·4 multiplier is removed from row 2, the $S_0$ bit cannot be considered.

Thus, from Table VII it can be seen that when 0·0, 2·0, 0·4, 4·0 and 2·4 are removed, the first 12 LSB's are effected and the 12 bit sum output will be accurate to about 3/4 LSB at this point. Thus, 5 multiplier packages can be removed from a 12 x 12 multiplier and maintain a 3/4 LSB accuracy. Note that 18 devices are required for full accuracy. If the 6·0 multiplier is removed from row 4, the 12-bit result will be accurate to about 1 LSB, but only 12 devices are required rather than 18.

One further note on truncation; when a binary word is truncated, the accuracy is not ±1 LSB or ±1/2 LSB, etc. The truncated result can never increase the magnitude of the LSB because this would include rounding. Thus, a truncated result is always the sum, S, plus zero magnitude of the LSB and minus 1, 1/2 or 1/4 (or any other number) LSB. The magnitude always becomes more negative for either positive or negative numbers.

From this discussion, it should be apparent that the designer can remove packages and truncate the product to any desired bit length and accuracy. When the product is truncated, no speed increase usually occurs, since the removed multipliers are not in the longest critical speed path. This assumes that the highest speed connection is being used.

### MULTIPLICATION IN OTHER NUMBER REPRESENTATIONS

Although 2's complement multiplication is the one most widely used, multiplication in other number representations often must be performed. The Am25S05 can be used to perform these multiplications if appropriate care is used and the proper connections are made.

### UNSIGNED (Magnitude-only) MULTIPLICATION

The most straightforward technique to perform magnitude-only multiplication is to generate two "always positive" two's complement numbers. This is accomplished by adding a logic "0" as the most significant bit of each word, thereby generating a positive sign bit. This increases both the X and Y word lengths by one bit. The Am25S05 can be used "as is" to perform this multiplication and the two most significant multiplier

sum bits are ignored. Thus, if m = 4 and n = 6 in a magnitude-only representation, a 5 x 7 multiplier configuration is required. The two MSB's of the 12-bit sum are ignored which result in a 10-bit product solution in a magnitude-only representation. Note that the multiplier still performs XY + K and m + n bits are sufficient to contain all possibilities. (A 6 x 8 connection is actually used).

A second technique for unsigned multiplication also requires extending the word length one bit, but need not require a larger array. A logic "0" is appended to each word as a positive sign bit; then the LSB of each word is considered separately.

$$X_e = x_0 + 2x - x_s 2^n$$
$$Y_e = y_0 + 2y - y_s 2^m$$

Since $x_s = y_s = 0$, the extended product is

$$X_e Y_e = 4xy + 2xy_0 + 2yx_0 + x_0 y_0$$

A n-bit by m-bit multiplier array can be used to generate 4xy and a conditional adder can be used to generate $2xy_0 + 2yx_0$. The term from this adder can be added to the multiplier array at the K input. The 1, 2 and 4 show the proper weighting for each term. The term $x_0 y_0$ is just an AND function and cannot produce a carry output. The first stage of the conditional adder produces the first bit of the product. The remaining product digits are produced at the output of the multiplier array. The sign digits $x_s$, $y_s$ and $k_s$ are held at logic 0 and the two most significant multiplier sum bits are ignored. The advantage of this connection is that the conditional adder is connected to the K inputs and in some cases the total multiplication time may be faster than if the above method is used.

It should also be noted that depending on the word lengths being used, it may only be necessary to extend one of the input words (X or Y) beyond the iterative array convenient length. Then it may be possible to use the K inputs as most of the conditional adder.

## SIGN-MAGNITUDE MULTIPLICATION

The most straightforward technique for performing sign magnitude multiplication is to split the sign from the magnitude and perform the magnitude multiplication as described in the magnitude-only section. The sum sign bit is $s_s = x_s\overline{y}_s + \overline{x}_s y_s = x_s \oplus y_s$, which can be performed in an external exclusive-OR circuit. Note that for a sign magnitude notation, m = 5 and n = 7 only m+n−1 = 11 bits are needed for the sign-magnitude XY product. **Caution** — care must be taken when using the K inputs because a negative product plus K may be positive and no provision is made for this in the sign bit representation.

The notation used for a sign-magnitude word is:

$$X_{sm} = x(1-2x_s)$$
$$Y_{sm} = y(1-2y_s)$$

The $X_{sm}Y_{sm}$ product is $S_{sm} = X_{sm}Y_{sm} = xy(1-2x_s)(1-2y_s) = xy(1-2x_s-2y_s+4x_sy_s)$

The Am25S05 2's complement multiplier produces the product: $S = XY = x_s y_s 2^{m+n-2} - xy_s 2^{m-1} - yx_s 2^{n-1} + xy$

The resulting solution for the sign magnitude multiplication if the signs are included in the Am25S05 connection is

$$S_{sm} = (XY - x_s y_s 2^{m+n-2} + xy_s 2^{m-1} + yx_s 2^{n-1})$$
$$(1-2x_s-2y_s + 4x_s y_s)$$

There are four conditions for $x_s y_s$ and the correction required in each case is as shown below:

| $x_s y_s$ | $XY_{sm}$ | |
|---|---|---|
| 00 | XY | (no correction) |
| 10 | $-XY - y2^{n-1}$ | |
| 01 | $-XY - x2^{m-1}$ | |
| 11 | $XY - 2^{m+n-2} + x2^{m-1} + y2^{n-1}$ | |

Since the terms to be added begin at weight $2^{m-1}$, $2^{n-1}$ or $2^{m+n-2}$, they must operate on the most significant part of the product. Therefore, additional adders are required at the output to make the proper connection. The technique of keeping the sign bits separate from the multiplier array and setting K = 0 is recommended.

## ONE'S COMPLEMENT MULTIPLICATION

One's complement multiplication does not have a straightforward method as do unsigned or sign-magnitude multiplication schemes. The notation used to represent a 1's complement number is

$$X_1 = x - x_s(2^{n-1} - 1)$$
$$Y_1 = y - y_s(2^{m-1} - 1)$$
$$S_1 = X_1Y_1 = xy + xy_s(1-2^{m-1}) + yx_s(1-2^{n-1}) + x_sy_s(1-2^{n-1} - 2^{m-1} + 2^{m+n-2})$$

If the X and Y word length are the same, then m = n and the product reduces to:

$$S_1 = X_1Y_1 = xy + (xy_s + yx_s)(1-2^{n-1}) + x_sy_s(1-2^n + 2^{2n-2})$$

The Am25S05 product for m = n is

$$XY = x_sy_s 2^{2n-2} - (xy_s + yx_s) 2^{n-1} + xy$$

Remembering the definitions for X and Y in 2's complement, the solution for the one's complement multiplication sum for m = n is

$$S_1 = XY + xy_s + yx_s + x_sy_s(1-2\cdot 2^{n-1})$$
$$S_1 = XY + x_sY + y_sX + x_sy_s$$

Note that the one's complement word relates to the two's complement word as

$$X_1 = X + x_s$$
$$Y_1 = Y + y_s$$

Therefore, the one's complement solution can also be given as

$$S_1 = XY + x_sY_1 + y_sX_1 - x_sy_s$$

The four conditions for $x_s y_s$ with m = n are:

5

| $x_s y_s$ | $X_1Y_1$ Result Correction Requires 2's Complement Inputs and 2's Complement Addition | $X_1Y_1$ Result Correction Requires 1's Complement Inputs and 1's Complement Addition | $X_1Y_1$ Result Correction Requires 1's Complement Inputs and 2's Complement Addition |
|---|---|---|---|
| 00 | XY | XY | XY |
| 10 | XY + Y | XY + $Y_1$ | XY + $Y_1$−1 |
| 01 | XY + X | XY + $X_1$ | XY + $X_1$−1 |
| 11 | XY + X + Y + 1 | XY + $X_1$ + $Y_1$−1 | XY + $X_1$ + $Y_1$ + 1 |

Since the correction to be added is at weight $2^0 = 1$, the K inputs can conveniently be used for this purpose. Note that two designs have been described. The first requires having both one's complement numbers $X_1$ and $Y_1$ available converted to 2's complement numbers X and Y. The second requires only one's complement numbers but requires an addition of −1 (in one's complement notation). Thus, a conditional adder can be used to produce $x_sY_1 + y_sX_1 - x_sy_s$, and the sum can be added to the multiplier at the K inputs.

If m is not equal to n, then the product $X_1Y_1$, using the Am25S05 is $S_1 = X_1Y_1 = XY + xy_s + yx_s + x_sy_s(1 - 2^{n-1} - 2^{m-1})$. Note that the same type of solution is possible as with m = n. $S_1 = X_1Y_1 = XY + y_sX_1 + x_sY, - x_sy_s$.

Thus, a conditional adder can be used and the solution is identical with the four conditions shown for $x_sy_s$ when m = n. The only difference is that the adder will use the m and n word lengths which must be extended sufficiently to cause repetition of the sign bit across the multipliers array.

### THE $y_{-1}$ BIT

It has been stated repeatedly that the multiplier array performs the function S = XY + K. This result assumes that the $y_{-1}$ system bit is held at zero. If $y_{-1}$ is held at logic "1", the array function becomes S = XY + K + X = X (Y+1) + K which may be expanded to include $y_{-1}$ as S = XY + K + $y_{-1}$ X = X ($Y+_{y-1}$) + K where $y_{-1}$ is either logic 1 or 0. There are some applications of the multiplier array that can take advantage of this ability to add X to the product XY.

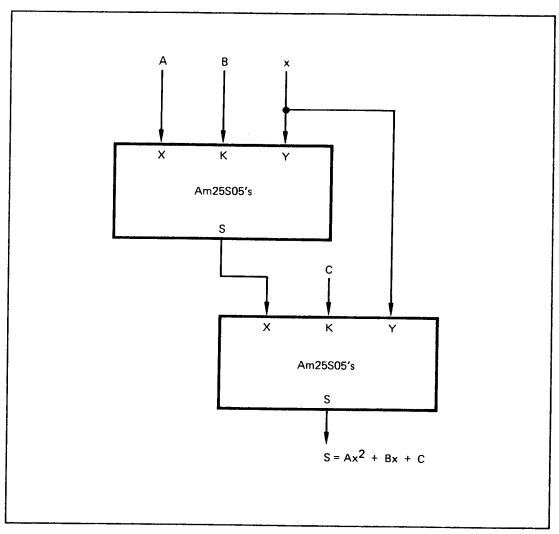



Figure 21. Polynomial Evaluation

## APPLICATIONS

The multiplier is ideal for hardware multiplication in general and special purpose computers, digital filter circuits, Fast Fourier Transform (FFT) processors, and special purpose digital machines. In the applications described in the following figures, the multiplier array is shown as a box which performs the function S = XY + K. Care must be exercised in scaling the numbers appropriately. Likewise, various other registers and adders are assumed to have a word length sufficient to handle the accuracy and magnification required. Figure 21 shows two multiplier arrays connected to generate a quadratic in x. This can be extended to form polynomials with higher powers of x.

A multiplier array connected to perform higher order polynomial evaluation in a time sequenced mode is shown in Figure 22. Note that the output register is initialized to 0 and the constants sequentially applied to the K input.

Figure 23 shows a single-pole, low-pass, recursive digital filter. The z-plane pole location is at z = C where C is a constant. The register is used as the unit time delay operator $z^{-1}$. The K inputs can be used for the least significant bits of the data

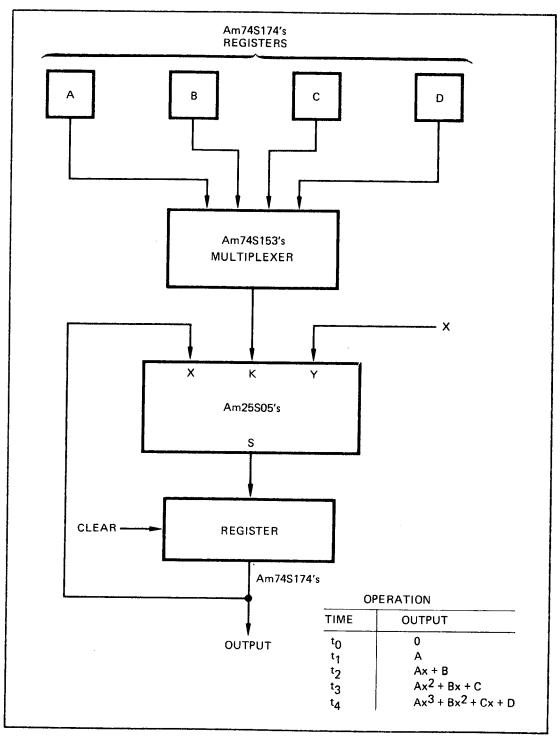



Figure 22. Time Sequenced Polynomial Evaluation

input $E_i$. In some designs, only the K input bits are required for the entire $E_i$ input word. The DC gain at z = +1 is 1/(1–C).

A single pole, high-pass recursive digital filter is shown in Figure 24. The z-plane pole location is at z = C. Note the z-plane zero at z = 1 which results in a DC gain of 0, i.e., a high-pass filter.

A two-pole, low-pass recursive digital filter of canonical form is shown in Figure 25. This block produces a complex conjugate pair of poles in the z-plane when $|4D| > |C^2|$. The pole locations are $z_1, z_2 = \frac{C}{2} \pm j\frac{\sqrt{|C^2-4D|}}{2}$. This configuration can be used as a two-pole building block in more complex Butterworth or Chebychef filters. The DC gain is 1/(1–C+D). This value is usually very close to the peak internal build up which occurs at a frequency just below the filter break frequency. Also shown is the case in which the input word length has been extended to full length.

Figure 26 shows a general two-pole, two-zero recursive canonical structure. By appropriately selecting the A, B, C, and D constants in this configuration, the building block can be used as a high-pass, low-pass, or band-pass digital filter. The DC gain is (1+A+B)/(1–C+D). The pole locations are the same as for Figure 24. The zero pair will be complex if A is negative and $|4B| > |A^2|$. If A = –2 and B = 1, then the zeros are at $(z-1)^2$ and a two-pole, high-pass filter results.

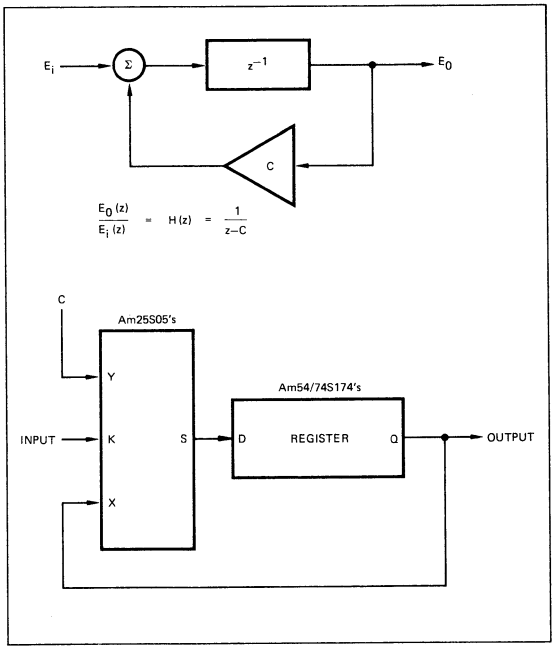



**Figure 23. Single-Pole, Low Pass Recursive Digital Filter**

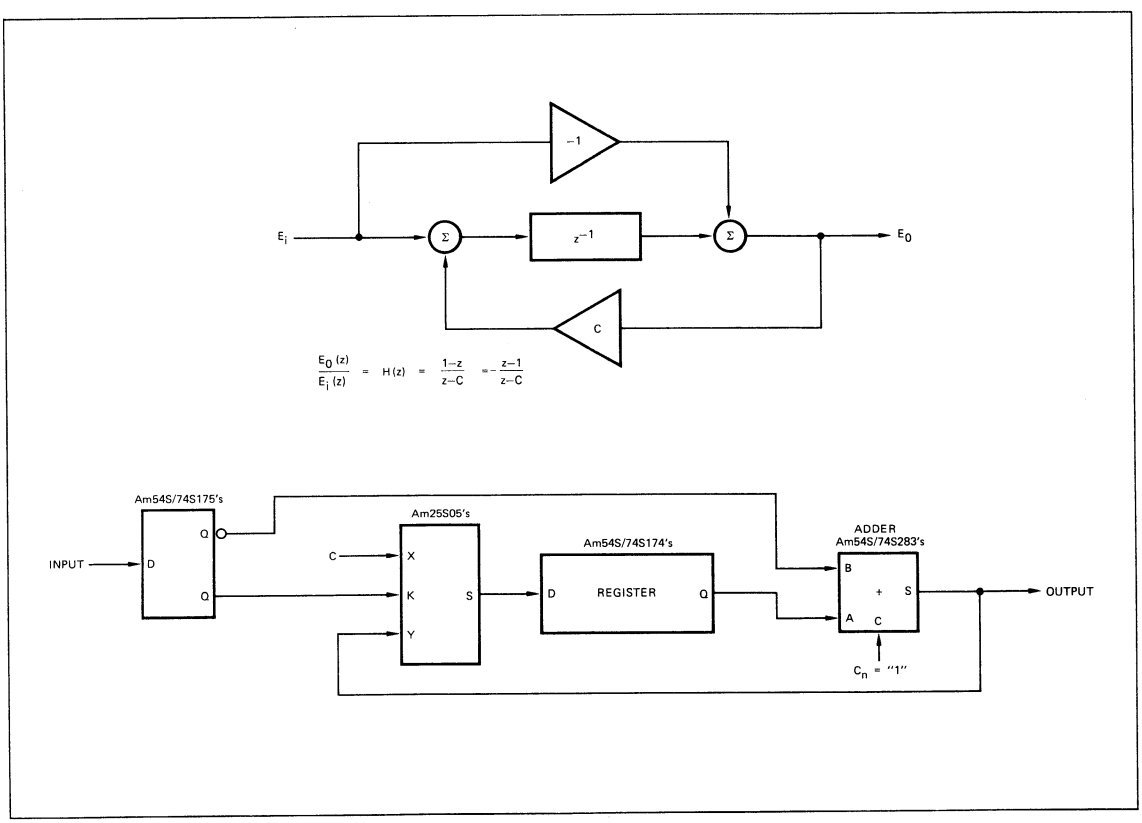



**Figure 24. Single-pole, High-pass Recursive Digital Filter.**

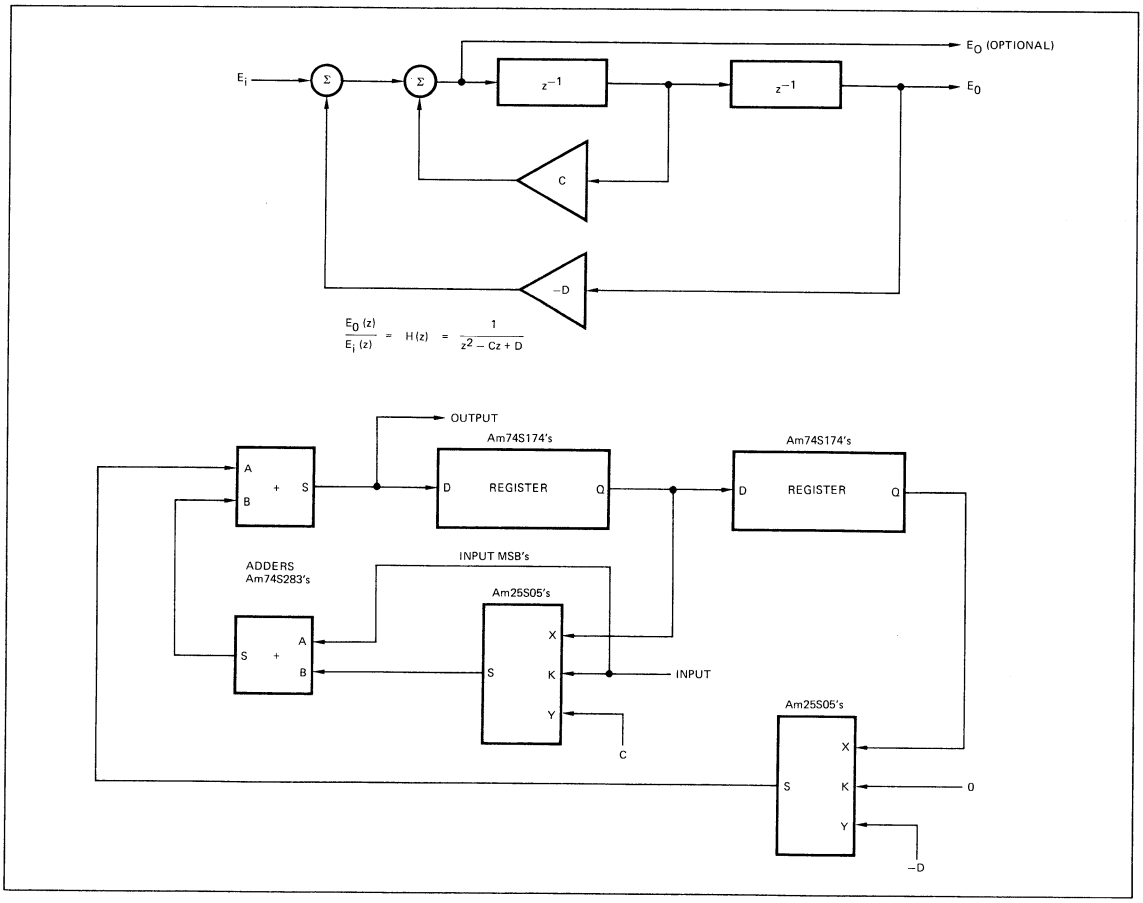



**Figure 25. Two-pole, Low-pass Recursive Digital Filter**

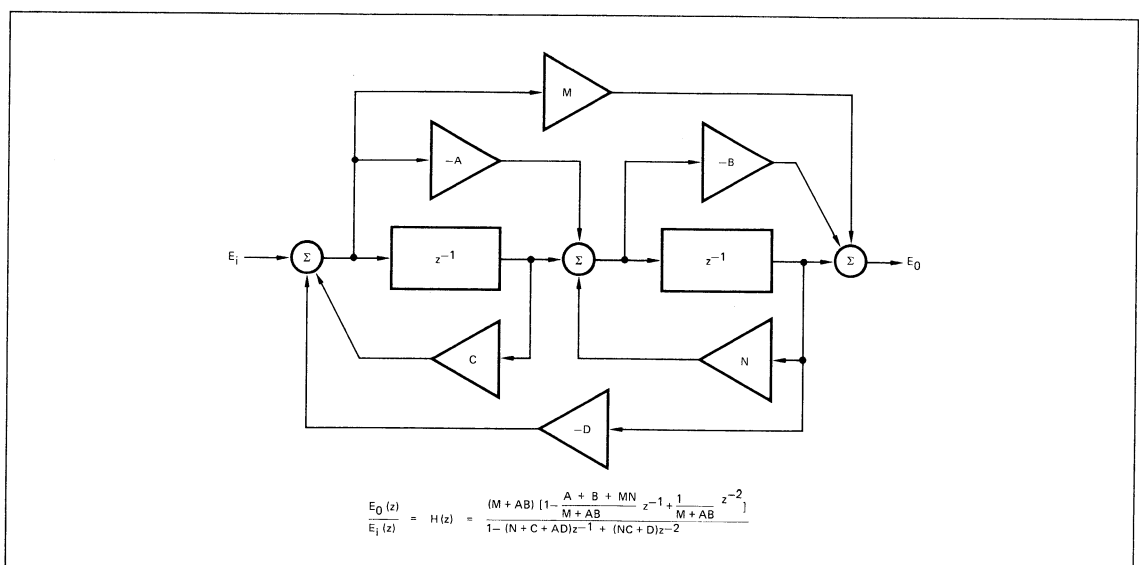
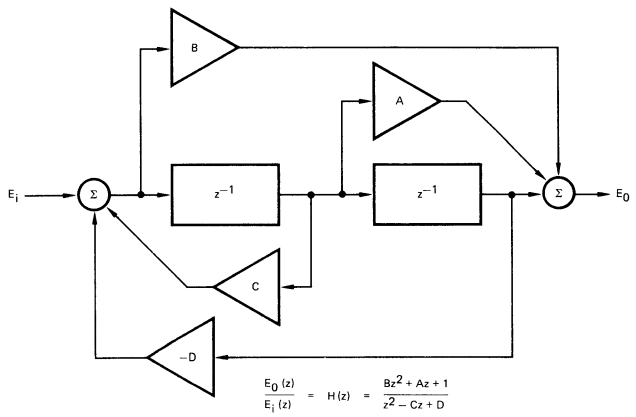



**Figure 27. General Two-pole, Two-zero Recursive Digital Filter Building Block**



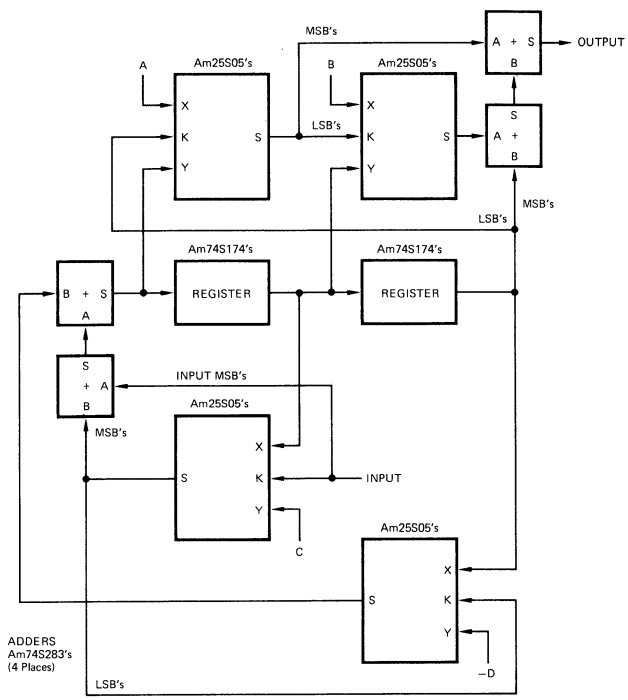



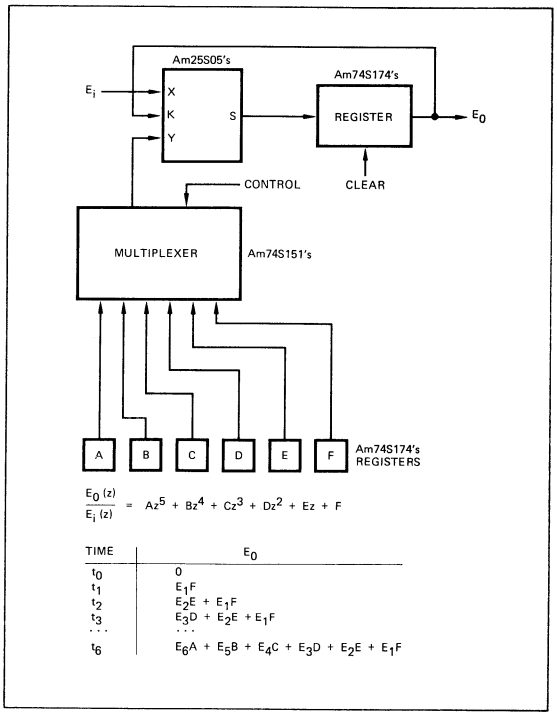

**Figure 26. Canonical Two-pole, Two-zero Recursive Digital Filter.**

A general two-pole building block is shown in Figure 27. There are several options for arranging the multipliers and adders depending on the application. The z-plane transfer function is also shown in Figure 27. The multiplier constants locate the poles and zeros of the filter. Also, the internal characteristics of the filter can be adjusted using the constants.

In all of the digital filter examples shown, the single unit delay register, $z^{-1}$, can be replaced with multi-word resisters. Thus, the arithmetic structure can be time shared by sequentially changing the multiplier constants. Also, such things as comb filters or range-gated filters can be designed using long word length registers. Remember, however, that each pole implemented requires one memory word and no sharing is possible.

A non-recursive digital filter is shown in Figure 28. These structures are useful as equalizers and for certain filter applications. These structures have a finite transient response whereas the recursive filter transient response tends to be infinite.

This same non-recursive structure can be implemented as shown in Figure 29. Here one multiplier and one register are used in a time-sequenced mode. Thus, with the non-recursive structure, both the multipliers and memory may be time shared. The coefficients A, B, C, etc., are evaluated by determining the transient response of the filter desired and implementing the z-transform constants as the multiplier constants. As shown, each constant is stored in a separate register and then multiplexed to the multiplier. This may be more convenient for adaptive filters. Otherwise, the constants can be stored in a shift register that is connected to the Y input of the multiplier.




| TIME | $E_0$ |
|---|---|
| $t_0$ | 0 |
| $t_1$ | $E_1F$ |
| $t_2$ | $E_2E + E_1F$ |
| $t_3$ | $E_3D + E_2E + E_1F$ |
| ... | ... |
| $t_6$ | $E_6A + E_5B + E_4C + E_3D + E_2E + E_1F$ |

**Figure 29. Time Sequenced Non Recursive Digital Filter**

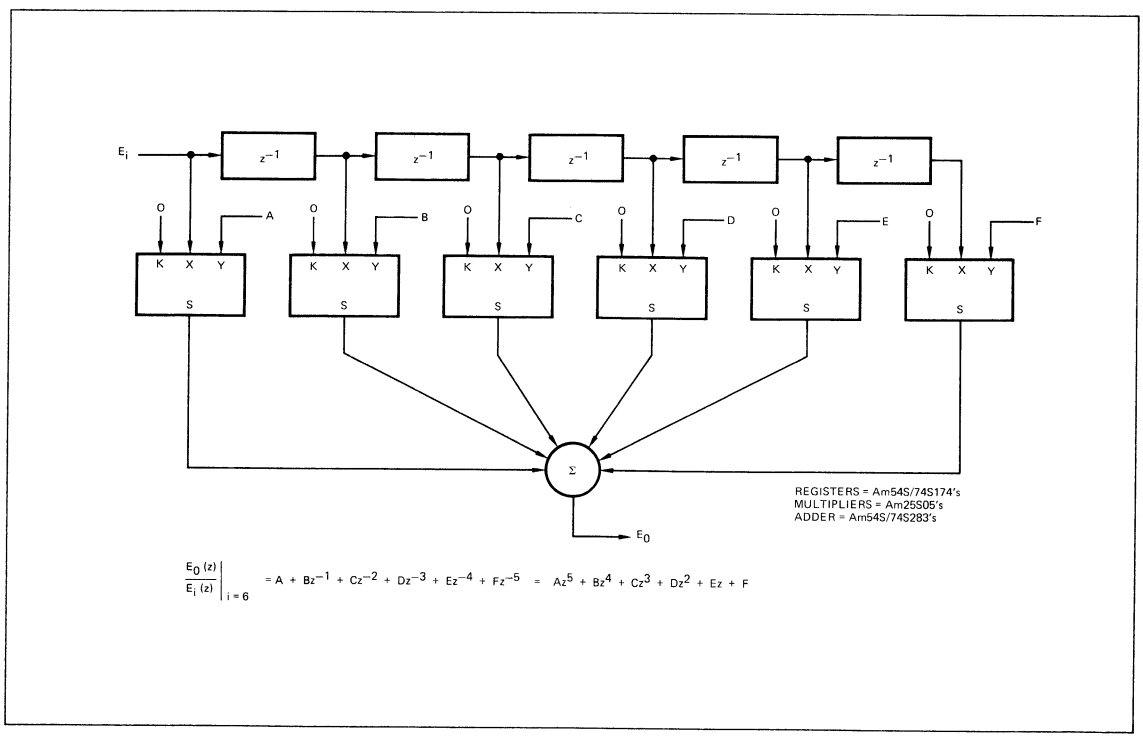



**Figure 28. Non-recursive Digital Filter**

Figure 30 shows how the square root of a number is formed using a multiplier array built with Am25S05 digital multipliers as the function generator. The successive approximation registers provide the estimate that is then squared and compared with the number whose root is required. If the square of the trial value is less than the number whose root is desired, then a "1" is fed back to change the register bit under consideration. The time to achieve a square root is essentially n+1 multiply times. The network can easily be modified to perform operations of the type $r = (X^2 + Y^2 + Z^2)^{1/2}$. The multiplier array can be used to generate the various squares, add the products and then compare the result against a trial value derived from the same multiplier array. The time required would then be n+4 multiplication times.

Another application frequently used is the division operation. This can be performed by multiplying the trial value, n, by the divisor and comparing the result against the dividend. If the dividend is larger then the trial value has to be increased; if the dividend is smaller then the trial value has to be reduced. The operation is fairly straightforward for unsigned division; with signed division a few problems occur.

For 2's complement integer division the logic is shown in Figure 31.

The divisor, dividend and trial quotient are all treated as 2's complement numbers. The first trial value is all ones (−1).

The operations performed are:

For $Q_S$, the sign digit of the quotient:

If $D_7 = 0$ and $-\frac{D}{2} < P$ Set $Q_S = 0$ Otherwise $Q_S = 1$

If $D_7 = 1$ and $-\frac{D}{2} < P$ Set $Q_S = 1$ Otherwise $Q_S = 0$

For the remaining quotient digits:

If $D_7 = 0$ and $T_{i-1}\, D + \frac{D}{2} < P$ Set $Q_i = 1$ Otherwise $Q_i = 0$

If $D_7 = 1$ and $T_{i-1}\, D + \frac{D}{2} < P$ Set $Q_i = 0$ Otherwise $Q_i = 1$

where $T_i$ is the i th trial value held in the SAR.

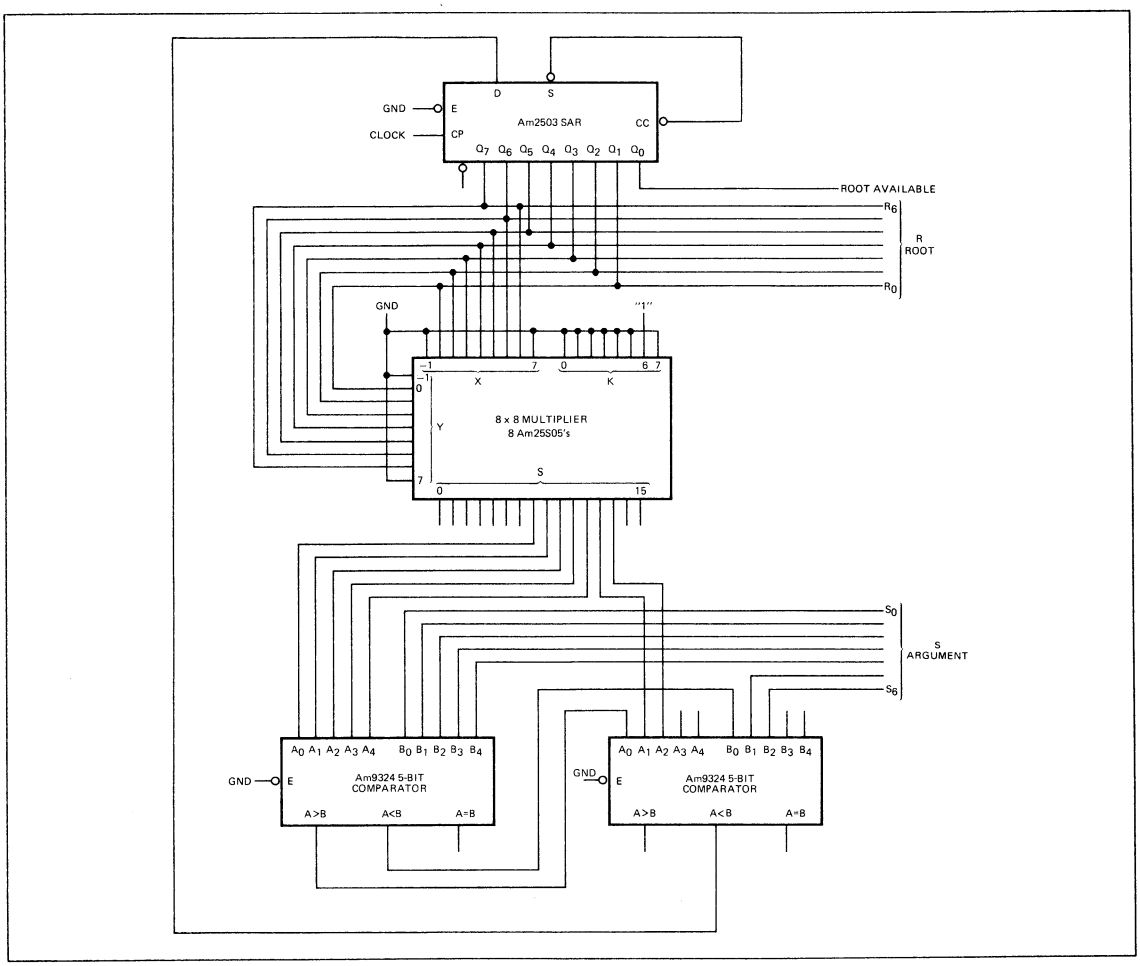



**Figure 30. Square Root Evaluation by Recursion**

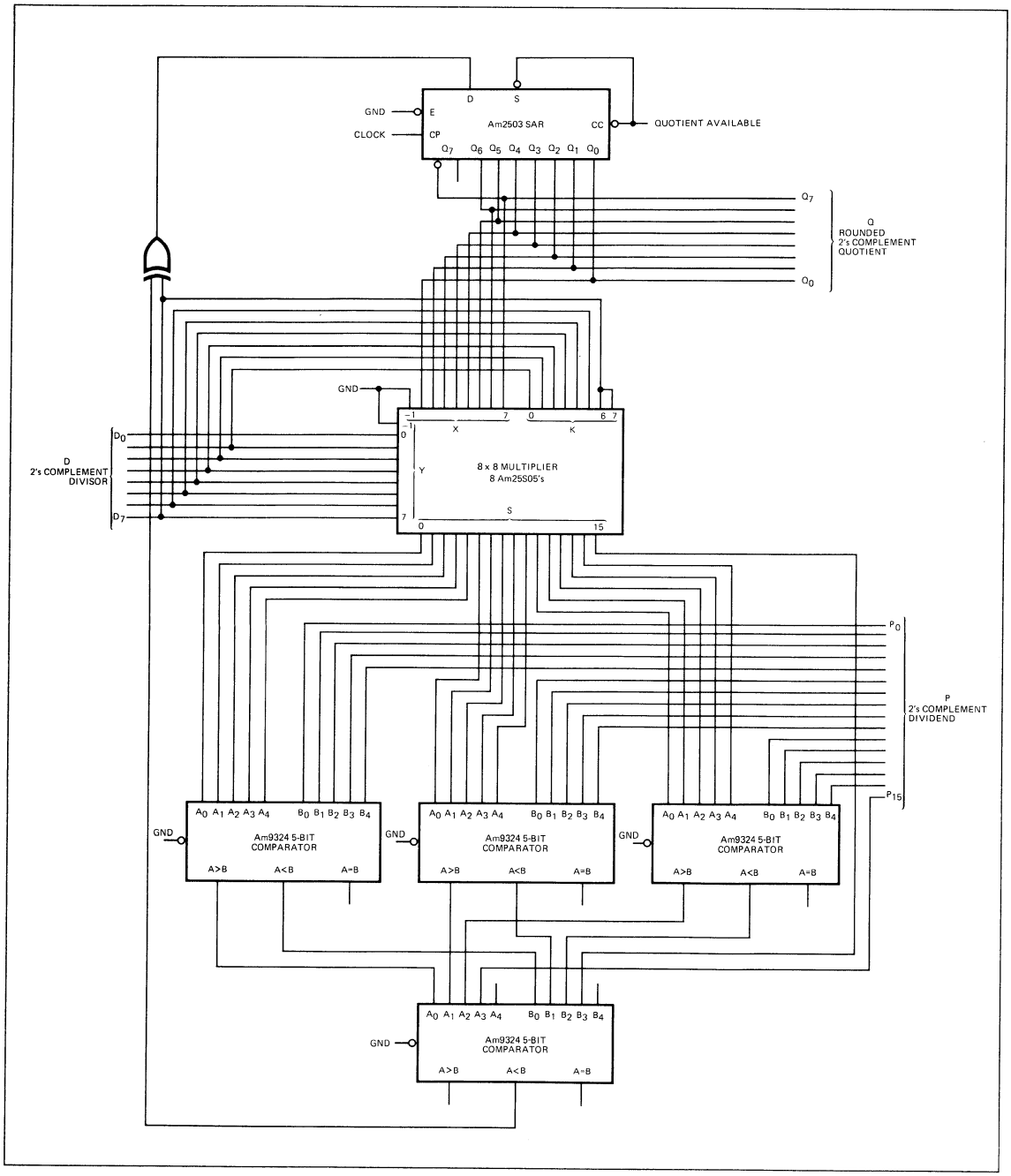



**Figure 31. 2's Complement Rounded Division**

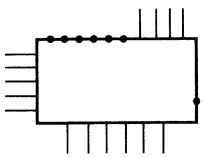
Since the complement of the most significant bit of the register is used rather than the true output so that resetting the register presents −1 to the multiplier array, the change in algorithm between the sign bit and the rest of the bits is automatically taken care of.

The D/2 factor in the equations is used to round off the quotient. A double length dividend is assumed. The comparator is wired for a 2's complement comparison with the sign digit of the product and dividend crossed over, the dividend sign bit forming part of the multiplier word and the product sign bit forming part of the dividend word.

# APPENDIX A

## CONNECTION DIAGRAMS

Within this Appendix, the symbol shown at left below is used to represent the Am25S05, Am2505, or Am25L05. The symbol at left should be interpreted as equivalent to the symbol at right.



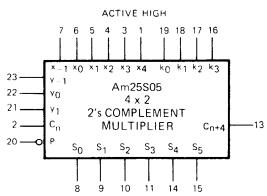



Table A-1 is a summary of the typical switching characteristics for each path through the multiplier. Table A-2 is a summary of speed and power for various size multiplier arrays using the parellelogram connection with carries interchanged (Reference Fig. A-1 and A-2).

## TABLE A-1

### TYPICAL SWITCHING CHARACTERISTICS

$$\left(\frac{t_{PHL} + t_{PLH}}{2}\right)$$

| PATH | Am25S05 | Am2505 | Am25L05 | UNIT |
|---|---|---|---|---|
| $C_n$ to $C_{n+4}$ | 8.5 | 13.5 | 32.5 | ns |
| $C_n$ to $S_{03}$ | 11.0 | 16.5 | 36.0 | ns |
| $C_n$ to $S_{45}$ | 14.0 | 19.5 | 44.0 | ns |
| k to $C_{n+4}$ | 8.25 | 13.5 | 31.0 | ns |
| k to $S_{03}$ | 11.5 | 16.5 | 36.5 | ns |
| k to $S_{45}$ | 14.0 | 21.5 | 51.5 | ns |
| X to $C_{n+4}$ | 17.5 | 21.0 | 63.5 | ns |
| X to $S_{03}$ | 21.0 | 25.0 | 70.0 | ns |
| X to $S_{45}$ | 22.5 | 29.5 | 85.0 | ns |
| Y to $C_{n+4}$ | 21.5 | 33.0 | 75.0 | ns |
| Y to $S_{03}$ | 23.0 | 35.0 | 83.5 | ns |
| Y to $S_{45}$ | 25.0 | 38.5 | 93.5 | ns |

## TABLE A-2

### TYPICAL SPEED & POWER FOR TWO'S COMPLEMENT MULTIPLICATION

| ARRAY SIZE | | Am25S05 | | Am2505 | | Am25L05 | |
|---|---|---|---|---|---|---|---|
| Y • X | # DEVICES | SPEED ns | POWER WATTS | SPEED ns | POWER WATTS | SPEED ns | POWER WATTS |
| 4x4 | 2 | 39 | 1.2 | 60 | 0.9 | 145 | 0.3 |
| 4x8 | 4 | 55 | 2.4 | 83 | 1.8 | 186 | 0.6 |
| 4x12 | 8 | 64 | 4.8 | 96 | 3.6 | 219 | 1.2 |
| 8x8 | 8 | 76 | 4.8 | 115 | 3.6 | 262 | 1.2 |
| 8x12 | 12 | 94 | 7.2 | 143 | 5.4 | 320 | 1.8 |
| 8x16 | 16 | 102 | 9.6 | 156 | 7.2 | 353 | 2.4 |
| 12x12 | 18 | 115 | 10.8 | 175 | 8.1 | 396 | 2.7 |
| 12x16 | 24 | 132 | 14.4 | 203 | 10.8 | 454 | 3.6 |
| 12x20 | 30 | 141 | 18.0 | 216 | 13.5 | 487 | 4.5 |
| 16x16 | 32 | 153 | 19.2 | 235 | 14.4 | 530 | 4.8 |
| 16x20 | 40 | 171 | 24.0 | 263 | 18.0 | 588 | 6.0 |
| 16x24 | 48 | 179 | 28.0 | 276 | 21.6 | 621 | 7.2 |
| 20x20 | 50 | 192 | 30.0 | 295 | 22.5 | 664 | 7.5 |
| 20x24 | 60 | 209 | 36.0 | 323 | 27.0 | 722 | 9.0 |
| 20x28 | 70 | 218 | 42.0 | 336 | 31.5 | 755 | 10.5 |
| 24x24 | 72 | 230 | 43.2 | 355 | 32.4 | 798 | 10.8 |
| 24x28 | 84 | 248 | 48.0 | 383 | 36.0 | 856 | 12.0 |
| 24x32 | 96 | 256 | 52.8 | 396 | 39.6 | 889 | 13.2 |
| 28x28 | 98 | 269 | 54.0 | 415 | 40.5 | 932 | 13.5 |
| 28x32 | 112 | 286 | 62.4 | 443 | 46.8 | 990 | 15.6 |
| 32x32 | 128 | 307 | 72.0 | 475 | 54.0 | 1066 | 18.0 |

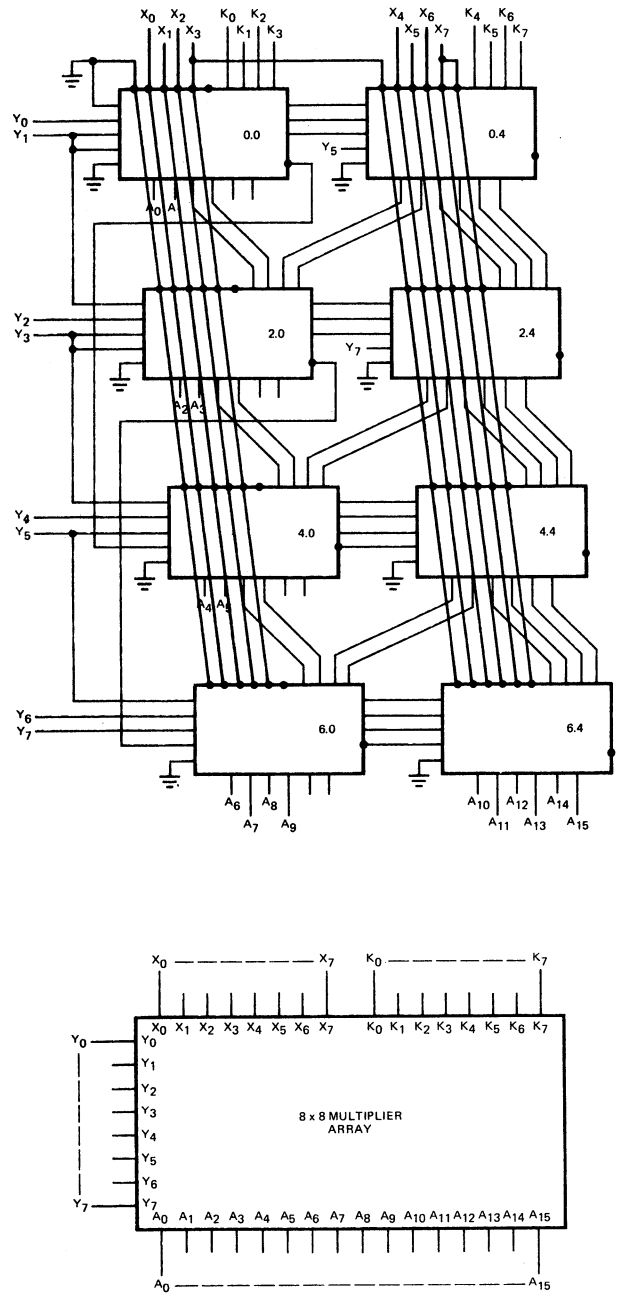



**Figure A-1. 8 x 8 Multiplication Array for 2's Complement Numbers. Both the Actual Connection Diagram and System Block Diagram are Shown.**

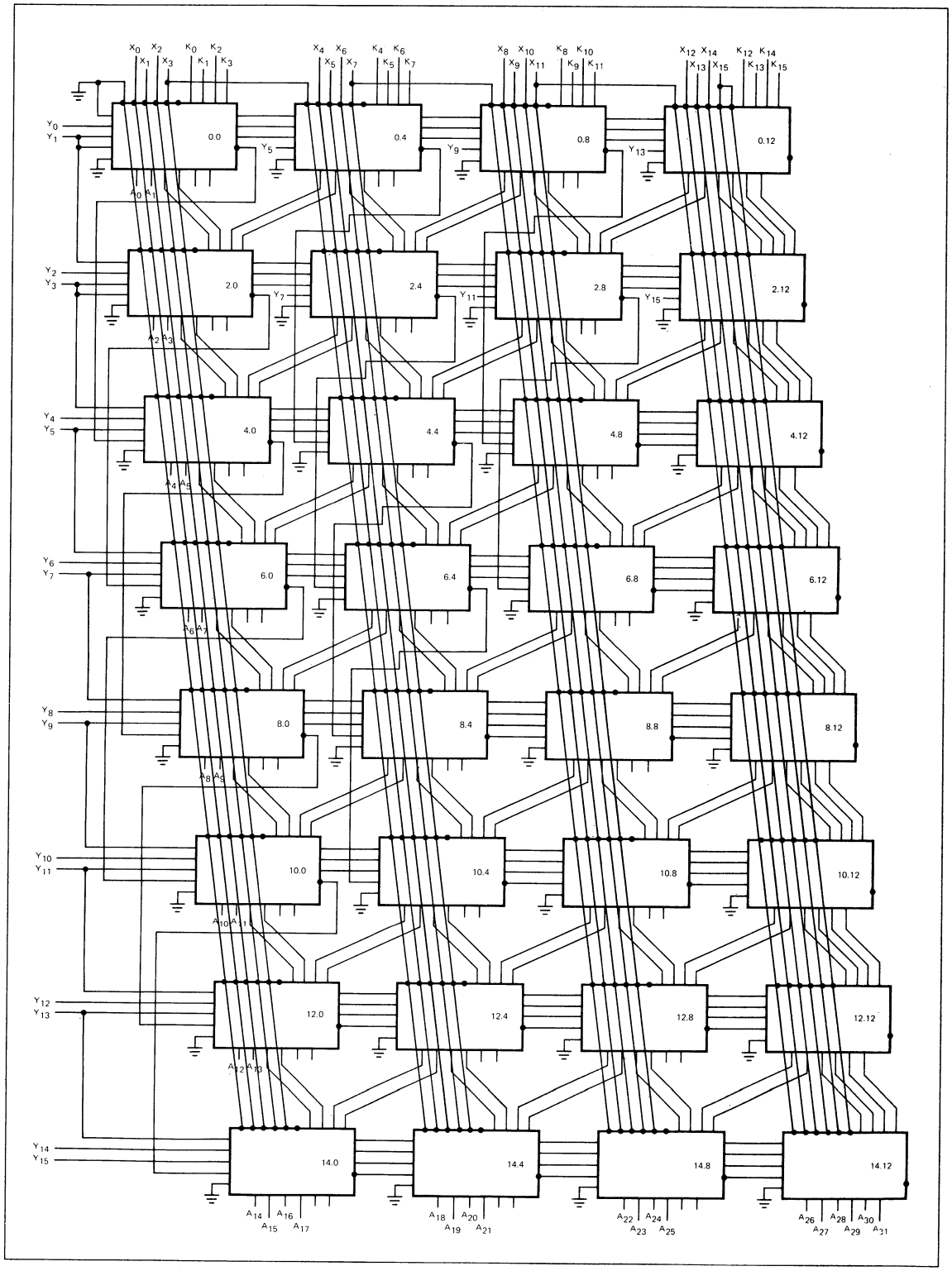



**Figure A-2. 16 x 16 2's Complement Multiplication Array.**

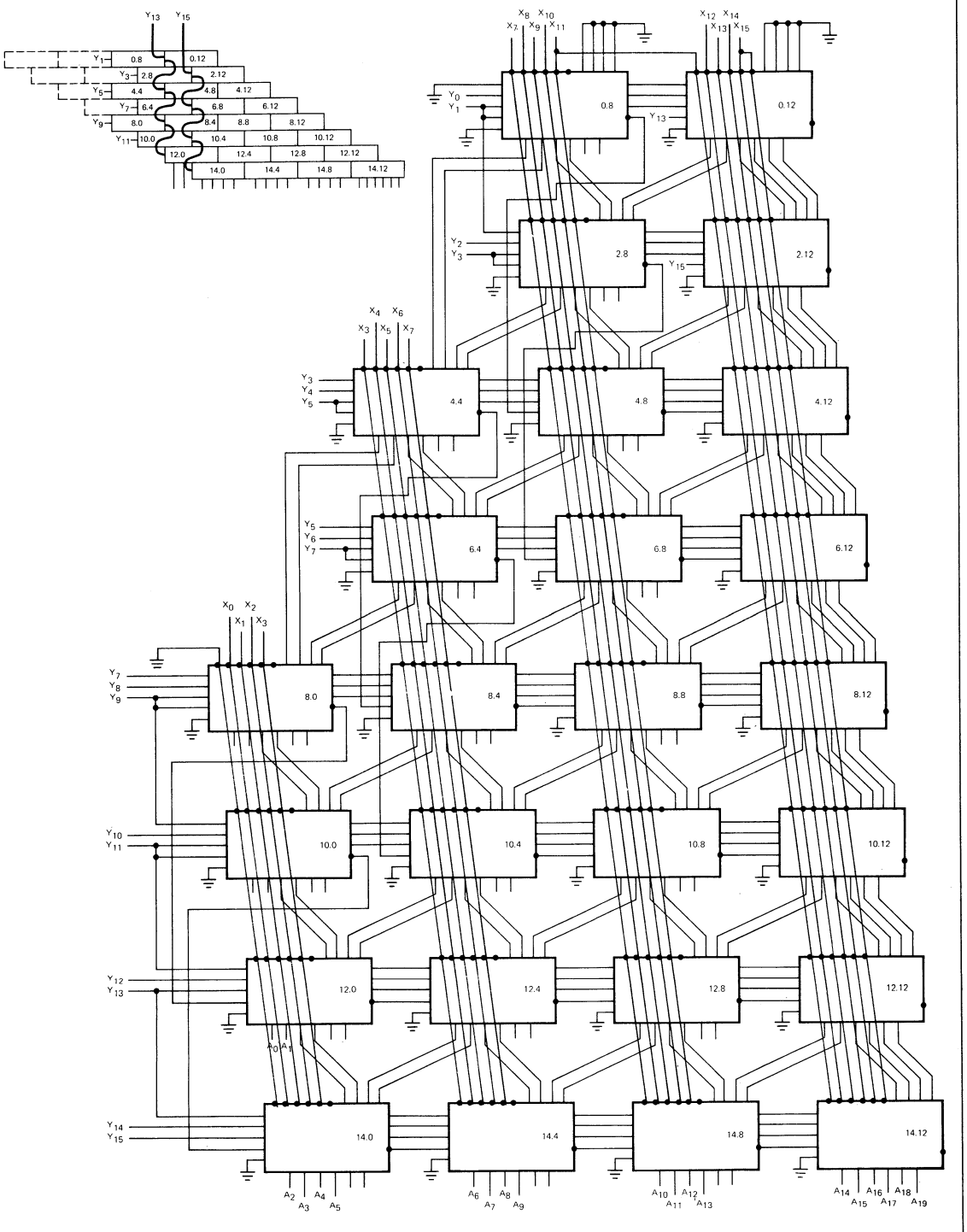



**Figure A-3. 16 x 16 2's Complement Multiplication Array Truncated to a 20-bit Product with ~ 1 LSB Accuracy.**

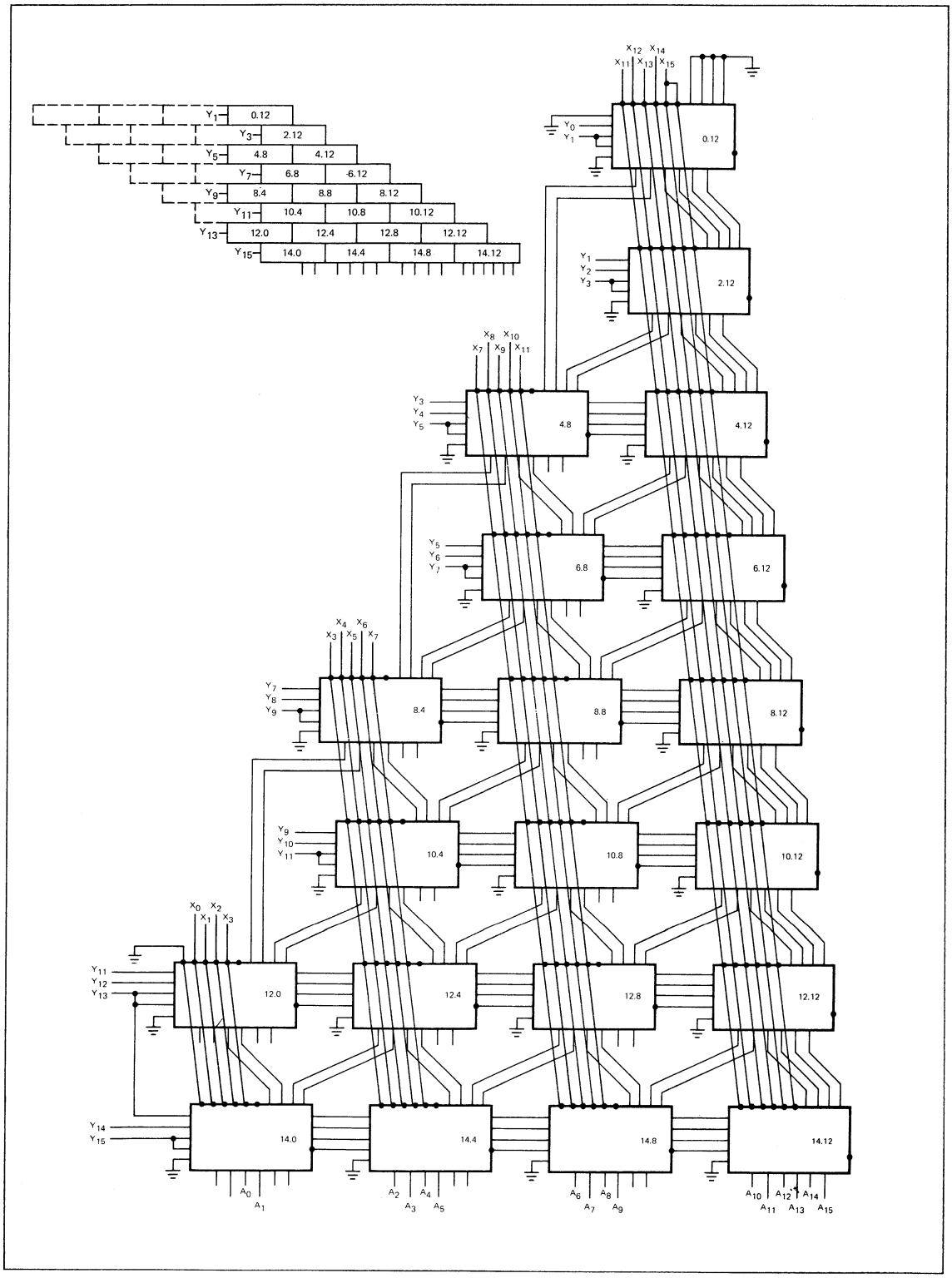
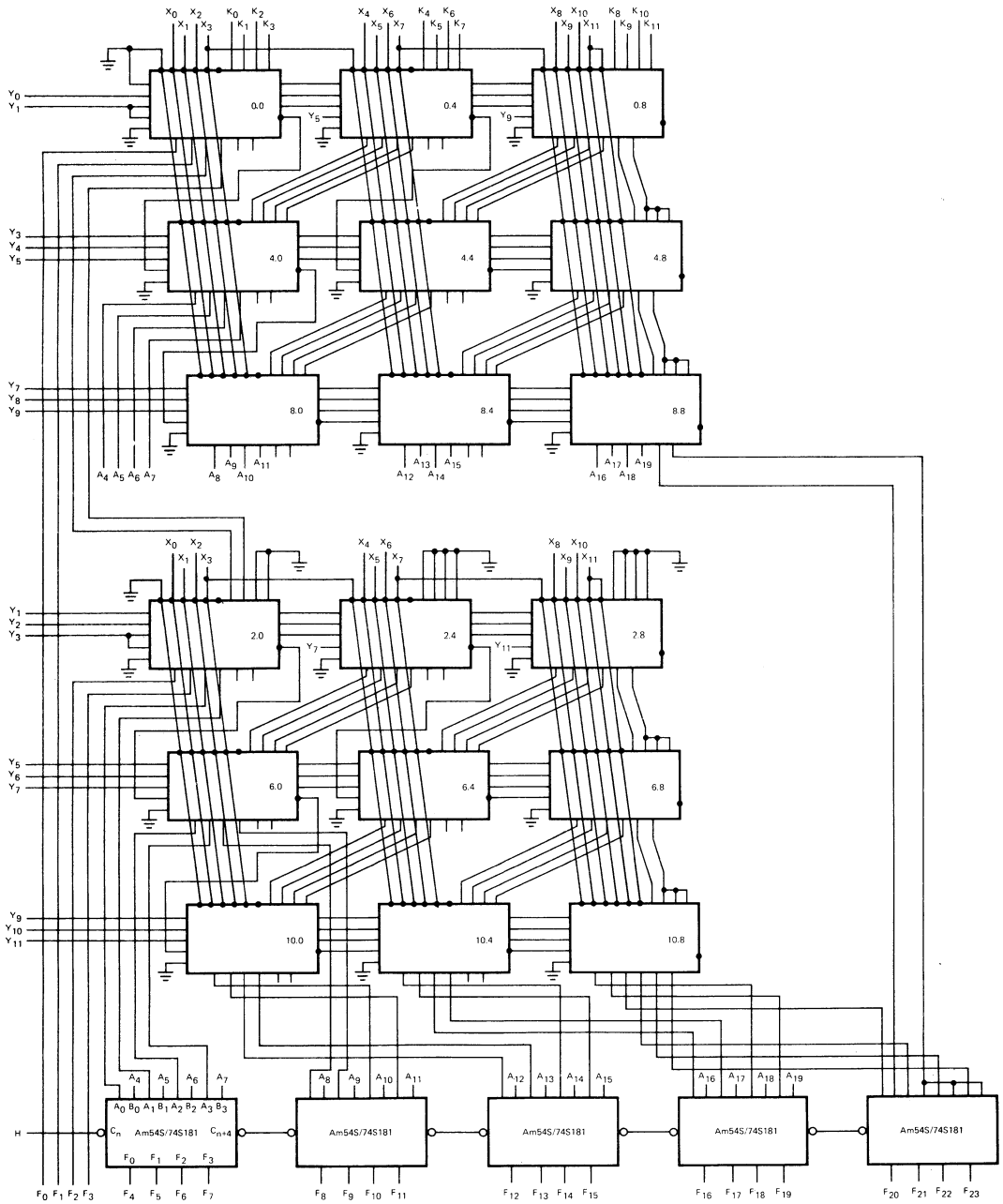
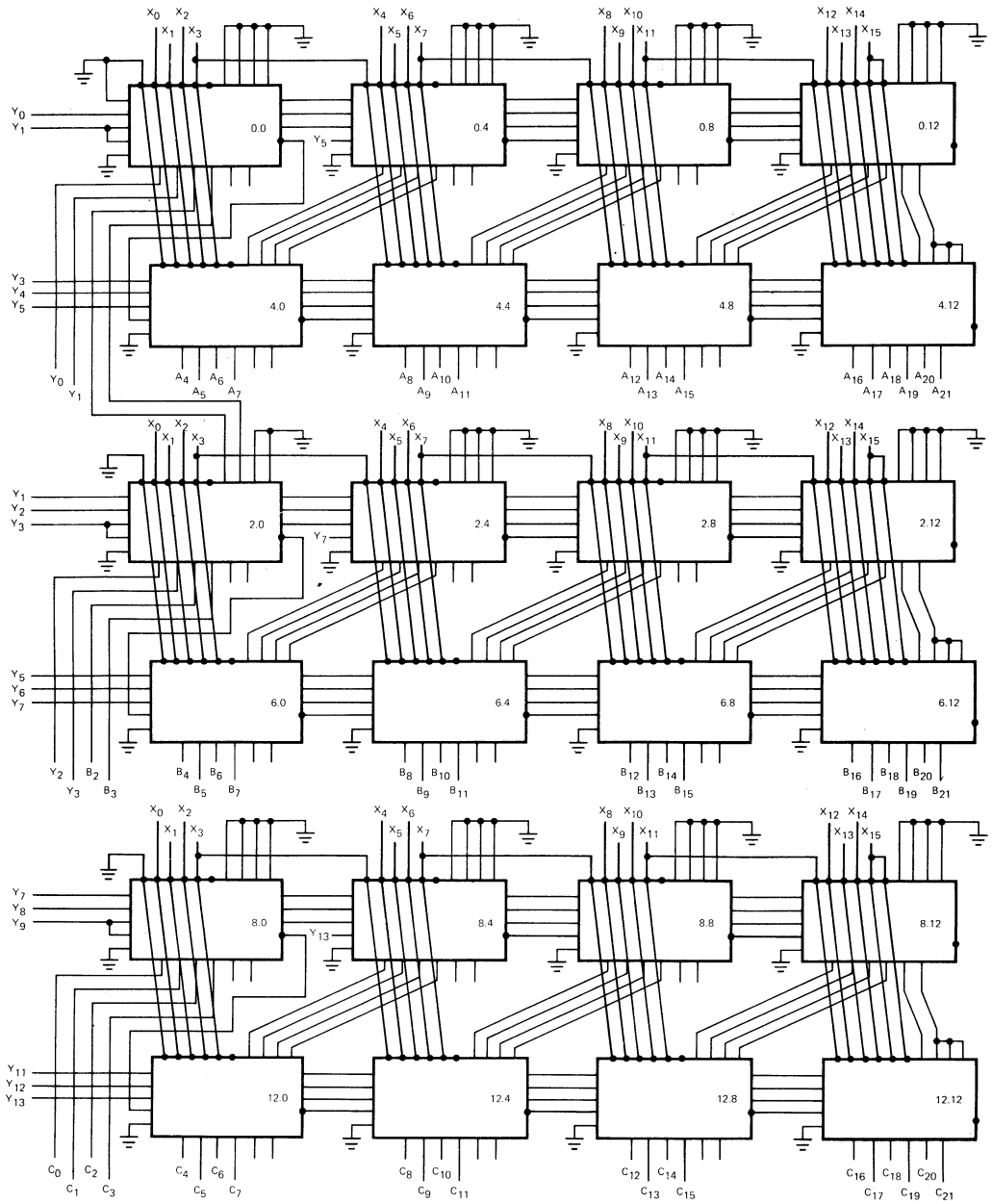



**Figure A-4. 16 x 16 2's Complement Multiplication Array Truncated to a 16-bit Product with ~ 1½ LSB Accuracy.**



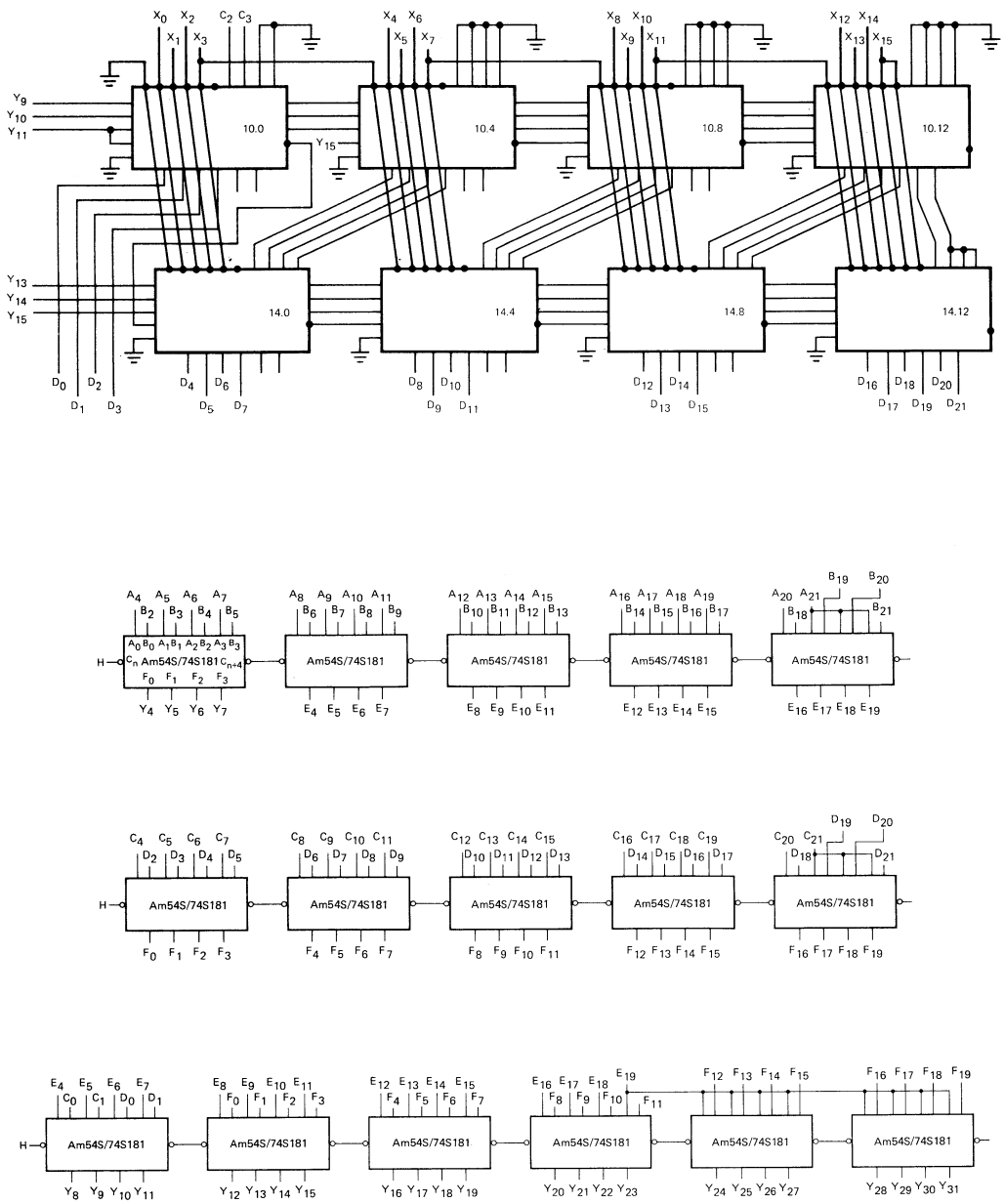

**Am54S/74S181 in ADD mode.**

**Figure A-5. 12 x 12 Multiplication Array Using one Level of Adders. (Similar to Figure 16 on 12 x 12 Array.)**




(Continued next page)

Figure A-6. 16 x 16 Multiplier Using Two Levels of Adders, (Reference Fig. 17).




H = HIGH

**Am54S/74S181 in ADD mode.**

**Figure A-6. (Con't) 16 x 16 Multiplier Using Two Levels of Adders, (Reference Fig. 17).**

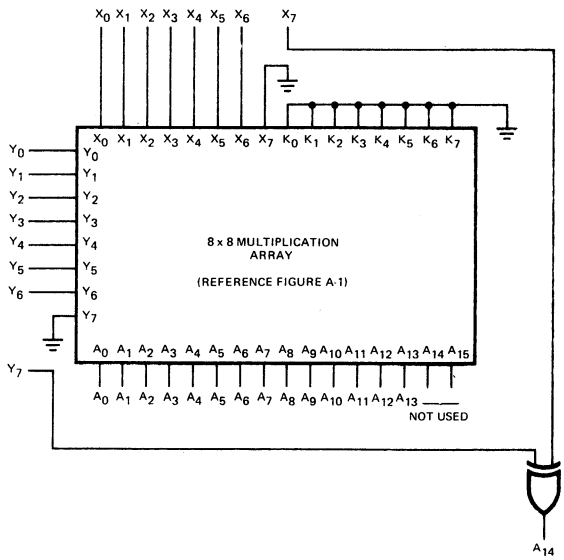
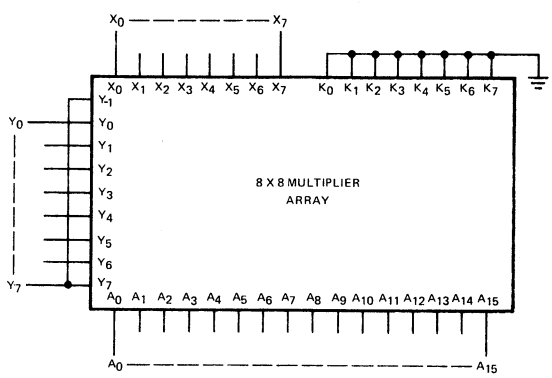



**Figure A-7. 8 x 8 Multiplication Array for Sign-magnitude Numbers.**

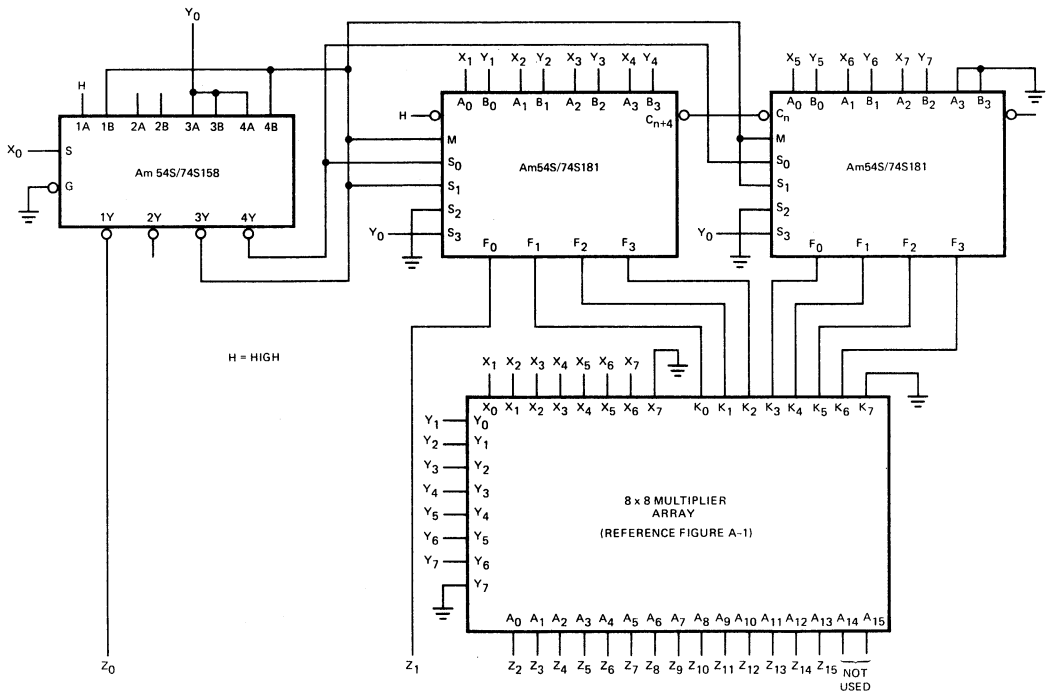



$X = x - x_s(2^{n-1})$ (2's Complement Number)

$Y_1 = y - y_s(2^{m-1} - 1)$ (1's Complement Number)

$XY_1 = XY + y_sX$ (2's Complement Product)

**Figure A-8. 2's Complement Multiplicand, 1's Complement Multiplier and 2's Complement Product.**

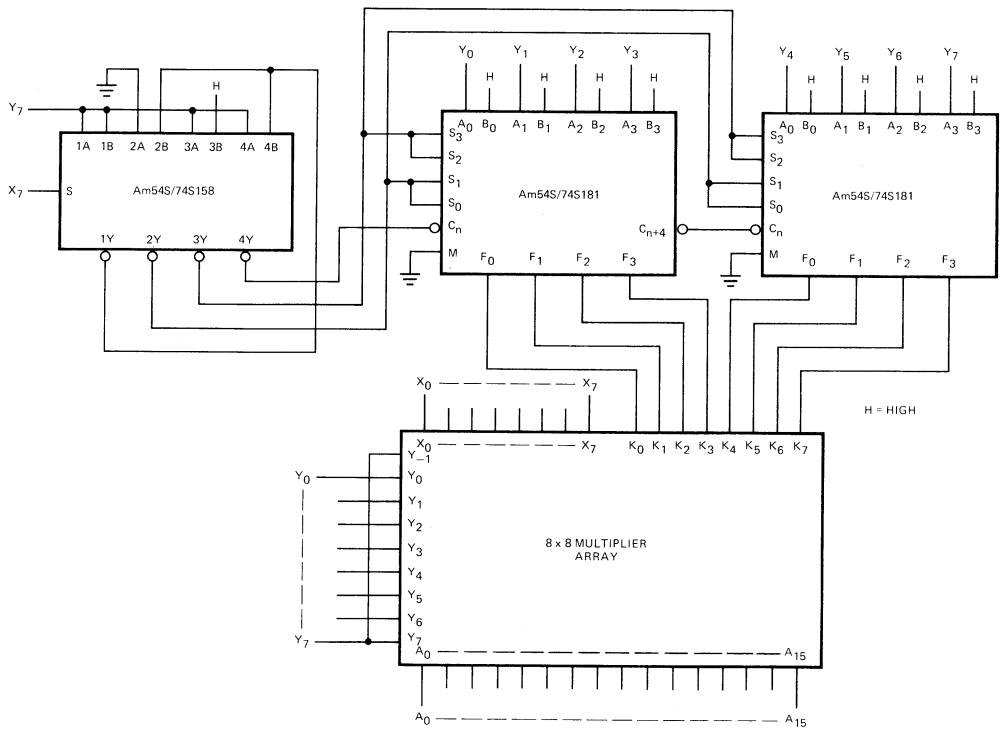



## FUNCTION TABLE FOR DECODE

| $Y_0$ | $X_0$ | $C_n$ | M | $S_3$ | $S_2$ | $S_1$ | $S_0$ | S181 Function | Algorithm Function |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | H | L | L | H | H | 0 | Add 0 |
| 0 | 1 | X | H | H | L | H | L | B | Add Y to XY |
| 1 | 0 | H | L | L | L | L | L | A | Add X to XY |
| 1 | 1 | H | L | H | L | L | H | A Plus B | Add X Plus Y to XY |

0 = Logic "0" = L = LOW
1 = Logic "1" = H = HIGH
X = Don't Care

**Figure A-9. 8 x 8 Multiplier for Unsigned Numbers Using the Product $X_eY_e = 4xy + 2xy_o + 2yx_o + x_oy_o$.**




## FUNCTION TABLE

| Xs | Ys | Function | M | $S_3$ | $S_2$ | $S_1$ | $S_0$ | $C_n$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | L | L | L | H | H | L |
| 0 | 1 | Y−1 | L | H | H | H | H | H |
| 1 | 0 | −1 | L | L | L | H | H | H |
| 1 | 1 | Y+1 | L | L | L | L | L | L |

**Figure A-10. Multiplication of Two 8-bit 1's Complement Numbers Resulting in a 16-bit 1's Complement Product.**

# General Information

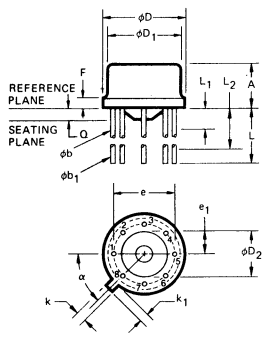


6

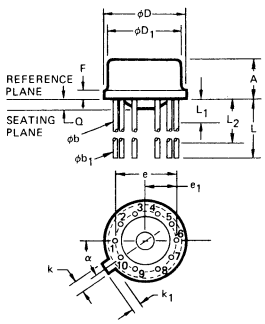
# PACKAGE OUTLINES

## METAL CAN PACKAGES

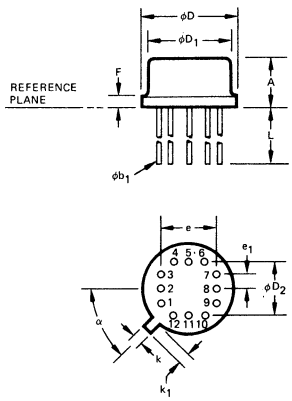
H-8-1




H-10-1




G-12-1



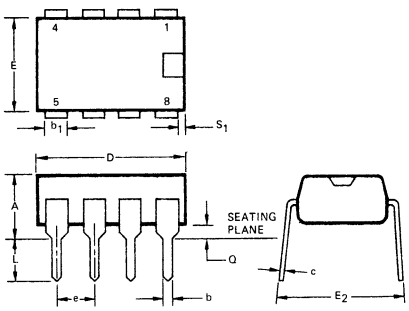

| AMD Pkg. | H-8-1 | | H-10-1 | | G-12-1 | |
|---|---|---|---|---|---|---|
| Common Name | TO-99 Metal Can | | TO-100 Metal Can | | TO-8 Metal Can | |
| 38510 Appendix C | A-1 | | A-2 | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .165 | .185 | .165 | .185 | .155 | .180 |
| e | .185 | .215 | .215 | .245 | .390 | .410 |
| $e_1$ | .090 | .110 | .105 | .125 | .090 | .110 |
| F | .013 | .033 | .013 | .033 | .020 | .030 |
| k | .027 | .034 | .027 | .034 | .024 | .034 |
| $k_1$ | .027 | .045 | .027 | .045 | .024 | .038 |
| L | .500 | .570 | .500 | .610 | .500 | .600 |
| $L_1$ | | .050 | | .050 | | |
| $L_2$ | .250 | | .250 | | | |
| α | 45° BSC | | 36° BSC | | 45° | |
| øb | .016 | .019 | .016 | .019 | | |
| $øb_1$ | .016 | .021 | .016 | .021 | .016 | .021 |
| øD | .350 | .370 | .350 | .370 | .590 | .610 |
| $øD_1$ | .305 | .335 | .305 | .335 | .540 | .560 |
| $øD_2$ | .120 | .160 | .120 | .160 | .390 | .410 |
| Q | .015 | .045 | .015 | .045 | | |

Notes: 1. Standard lead finish is bright acid tin plate or gold plate.
2. øb applies between $L_1$ and $L_2$. $øb_1$ applies between $L_1$ and 0.500" beyond reference plane.

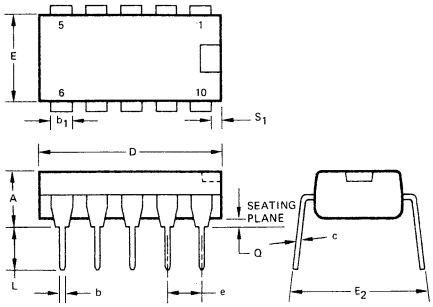
## PACKAGE OUTLINES (Cont.)

### MOLDED DUAL IN-LINE PACKAGES

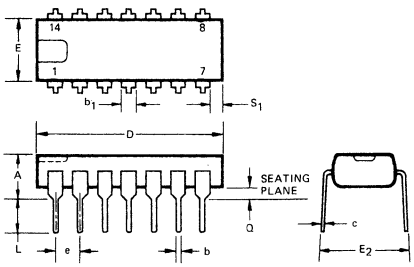
P-8-1



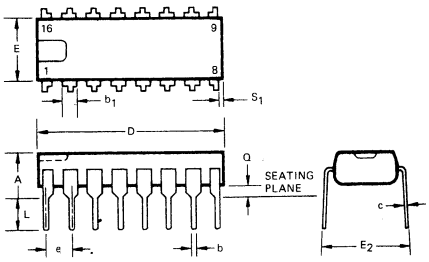

P-10-1



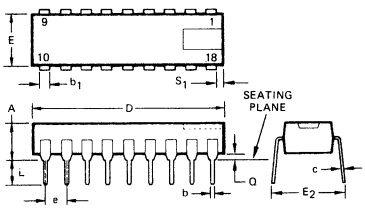

P-14-1



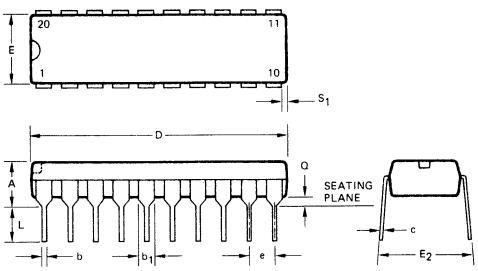

P-16-1



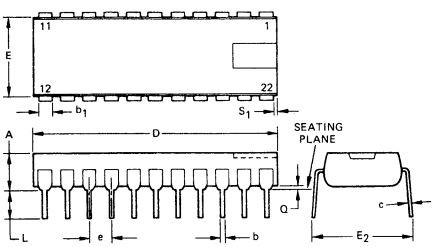

P-18-1




P-20-1




P-22-1

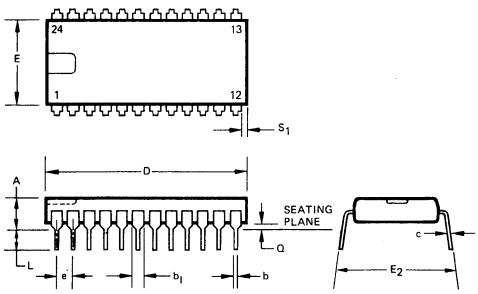



6

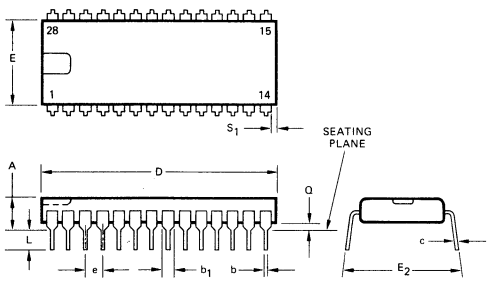
## PACKAGE OUTLINES (Cont.)

### MOLDED DUAL IN-LINE PACKAGES (Cont.)

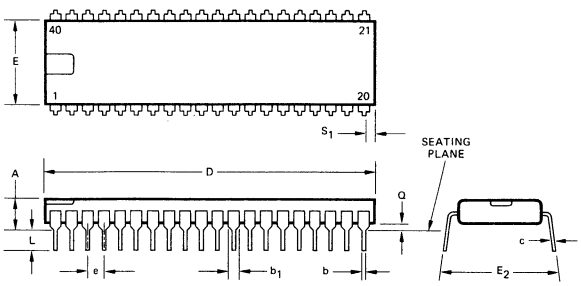
P-24-1




P-28-1




P-40-1



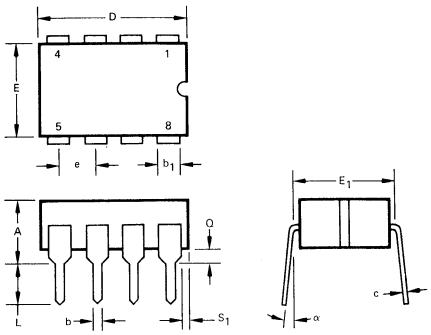

| AMD Pkg. | P-8-1 | | P-10-1 | | P-14-1 | | P-16-1 | | P-18-1 | | P-20-1 | | P-22-1 | | P-24-1 | | P-28-1 | | P-40-1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameters** | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| **A** | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .170 | .215 | .150 | .200 | .150 | .200 |
| **b** | .015 | .022 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 |
| **$b_1$** | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 |
| **c** | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 |
| **D** | .375 | .395 | .505 | .550 | .745 | .775 | .745 | .775 | .895 | .925 | 1.010 | 1.050 | 1.080 | 1.120 | 1.240 | 1.270 | 1.450 | 1.480 | 2.050 | 2.080 |
| **E** | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .250 | .290 | .330 | .370 | .515 | .540 | .530 | .550 | .530 | .550 |
| **$E_2$** | .310 | .385 | .310 | .385 | .310 | .385 | .310 | .385 | .310 | .385 | .310 | .385 | .410 | .480 | .585 | .700 | .585 | .700 | .585 | .700 |
| **e** | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| **L** | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .160 | .125 | .160 | .125 | .160 | .125 | .160 |
| **Q** | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 |
| **$S_1$** | .010 | .030 | .040 | .070 | .040 | .065 | .010 | .040 | .030 | .040 | .025 | .055 | .015 | .045 | .035 | .065 | .040 | .070 | .040 | .070 |

Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension $E_2$ is an outside measurement.

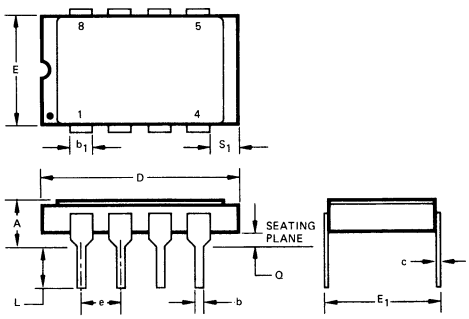
## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES

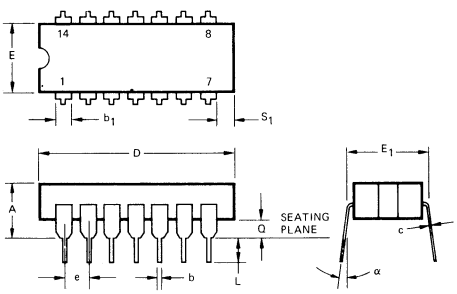
D-8-1



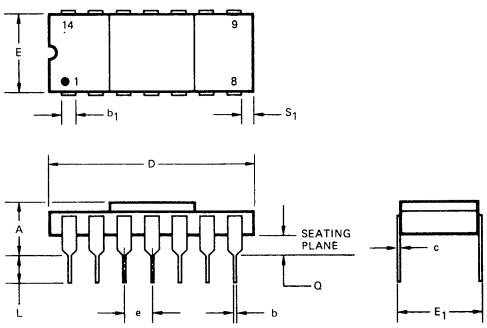

D-8-2



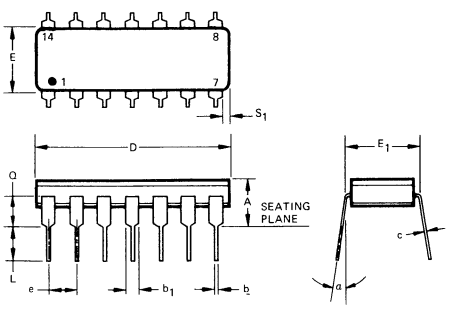

D-14-1



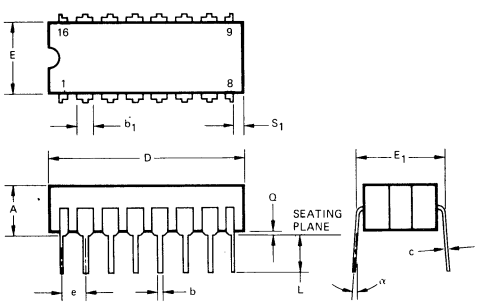

D-14-2



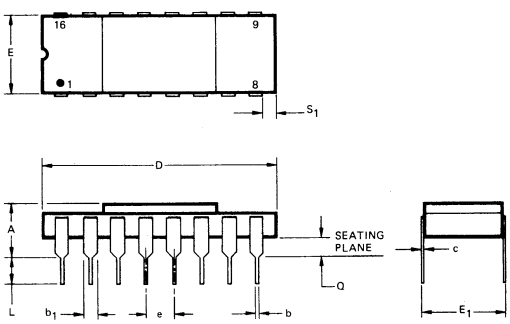

D-14-3




D-16-1




D-16-2

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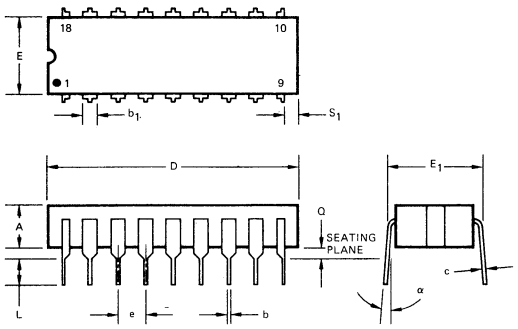
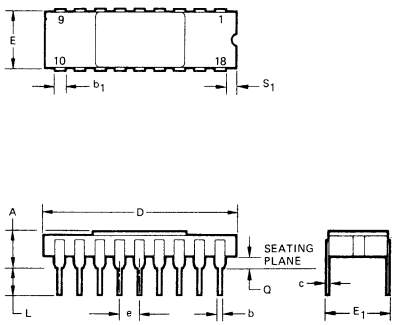
## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

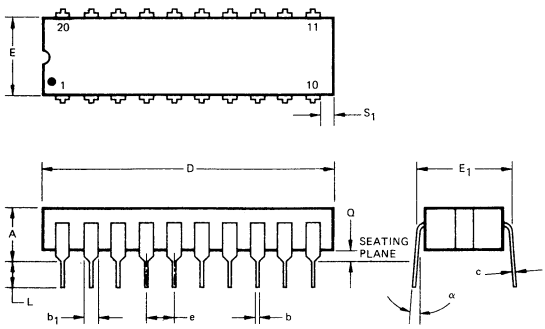
D-18-1



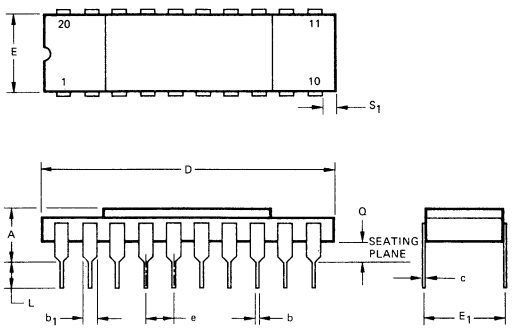

D-18-2



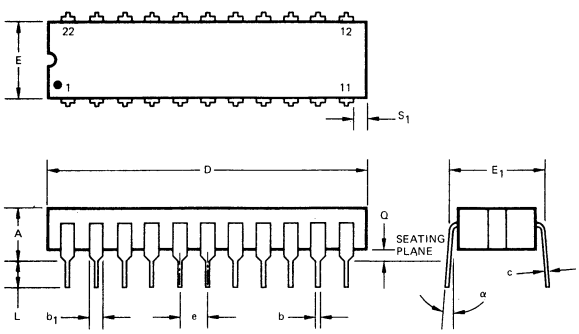

D-20-1



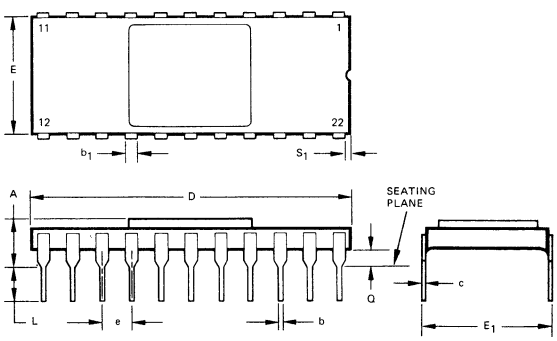

D-20-2



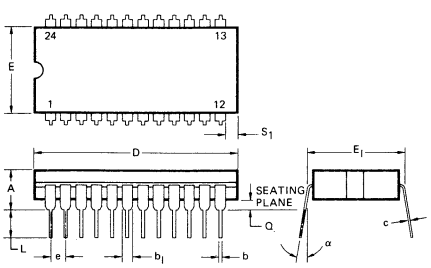

D-22-1



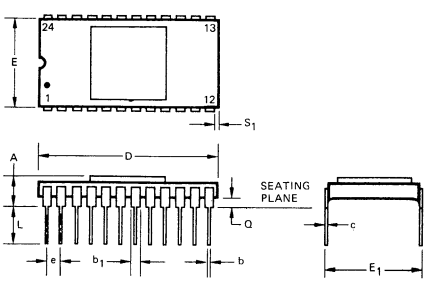

D-22-2




D-24-1 and D-24-4



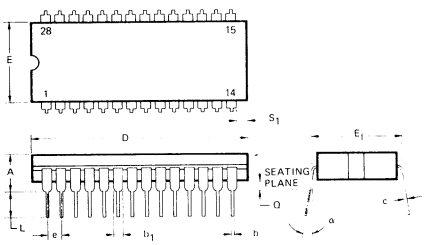

D-24-2



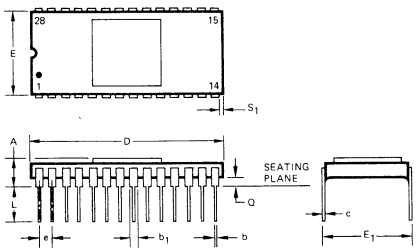
## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

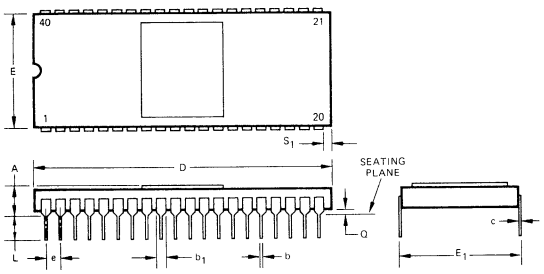
D-28-1



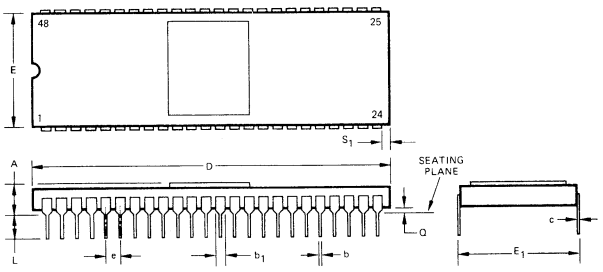

D-28-2




D-40-2




D-48-2




| AMD Pkg. | D-8-1 | | D-8-2 | | D-14-1 | | D-14-2 | | D-14-3 (Note 2) | | D-16-1 | | D-16-2 | | D-18-1 | | D-18-2 | | D-20-1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | METAL DIP | | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | CERDIP | |
| 38510 Appendix C | – | | – | | D-1(1) | | D-1(3) | | D-1(1) | | D-2(1) | | D-2(3) | | – | | – | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .130 | .200 | .100 | .200 | .130 | .200 | .100 | .200 | .100 | .200 | .130 | .200 | .100 | .200 | .130 | .200 | .100 | .200 | .140 | .220 |
| b | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .015 | .023 | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .016 | .020 |
| $b_1$ | .050 | .070 | .040 | .065 | .050 | .070 | .040 | .065 | .030 | .070 | .050 | .070 | .040 | .065 | .050 | .070 | .040 | .065 | .050 | .070 |
| c | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .008 | .011 | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .009 | .011 |
| D | .370 | .400 | .500 | .540 | .745 | .785 | .690 | .730 | .660 | .785 | .745 | .785 | .780 | .820 | .870 | .920 | .850 | .930 | .935 | .970 |
| E | .240 | .285 | .260 | .310 | .240 | .285 | .260 | .310 | .230 | .265 | .240 | .310 | .260 | .310 | .280 | .310 | .260 | .310 | .245 | .285 |
| $E_1$ | .300 | .320 | .290 | .320 | .290 | .320 | .290 | .320 | .290 | .310 | .290 | .320 | .290 | .320 | .290 | .320 | .290 | .320 | .290 | .320 |
| e | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| L | .125 | .150 | .125 | .160 | .125 | .150 | .125 | .160 | .100 | .150 | .125 | .150 | .125 | .160 | .125 | .150 | .125 | .160 | .125 | .150 |
| Q | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .020 | .080 | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .015 | .060 |
| $S_1$ | .004 | | .005 | | .010 | | .005 | | .020 | | .005 | | .005 | | .005 | | .005 | | .005 | |
| α | 3° | 13° | | | 3° | 13° | | | 3° | 13° | 3° | 13° | | | 3° | 13° | | | 3° | 13° |
| Standard Lead Finish | b | | b or c | | b | | b or c | | c | | b | | b or c | | b | | b or c | | b | |

| AMD Pkg. | D-20-2 | | D-22-1 | | D-22-2 | | D-24-1 | | D-24-2 | | D-24-4 | | D-28-1 | | D-28-2 | | D-40-2 | | D-48-2 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | CERVIEW | | CERDIP | | SIDE-BRAZED | | SIDE-BRAZED | | SIDE-BRAZED | |
| 38510 Appendix C | – | | – | | – | | D-3(1) | | D-3(3) | | – | | – | | – | | – | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .100 | .200 | .140 | .220 | .100 | .200 | .150 | .225 | .100 | .200 | .150 | .225 | .150 | .225 | .100 | .200 | .100 | .200 | .100 | .200 |
| b | .015 | .022 | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .016 | .020 | .016 | .020 | .015 | .022 | .015 | .022 | .015 | .022 |
| $b_1$ | .040 | .065 | .045 | .065 | .030 | .060 | .045 | .065 | .030 | .060 | .045 | .065 | .045 | .065 | .030 | .060 | .030 | .060 | .030 | .060 |
| c | .008 | .013 | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .009 | .011 | .009 | .012 | .008 | .013 | .008 | .013 | .008 | .013 |
| D | .950 | 1.010 | 1.045 | 1.110 | 1.050 | 1.110 | 1.230 | 1.285 | 1.170 | 1.200 | 1.235 | 1.280 | 1.440 | 1.490 | 1.380 | 1.420 | 1.960 | 2.040 | 2.370 | 2.430 |
| E | .260 | .310 | .360 | .405 | .360 | .410 | .510 | .545 | .550 | .610 | .510 | .550 | .510 | .545 | .560 | .600 | .550 | .610 | .570 | .610 |
| $E_1$ | .290 | .320 | .390 | .420 | .390 | .420 | .600 | .620 | .590 | .620 | .600 | .630 | .600 | .620 | .590 | .620 | .590 | .620 | .590 | .620 |
| e | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| L | .125 | .160 | .125 | .150 | .125 | .160 | .120 | .150 | .120 | .160 | .120 | .150 | .125 | .150 | .120 | .160 | .120 | .160 | .125 | .160 |
| Q | .020 | .060 | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .015 | .060 | .015 | .060 | .020 | .060 | .020 | .060 | .020 | .060 |
| $S_1$ | .005 | | .005 | | .005 | | .010 | | .005 | | .010 | | .010 | | .005 | | .005 | | .005 | |
| α | | | 3° | 13° | | | 3° | 13° | | | 3° | 13° | 3° | 13° | | | | | | |
| Standard Lead Finish | b or c | | b | | b or c | | b | | b or c | | | | b | | b | | b or c | | b or c | |

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

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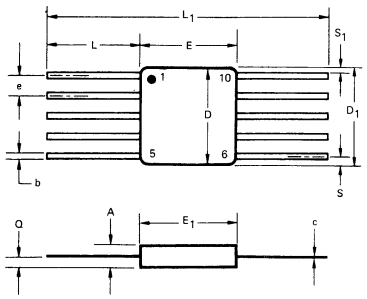
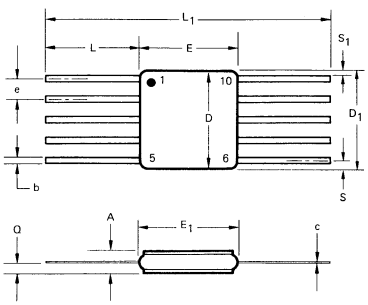
## PACKAGE OUTLINES (Cont.)

### FLAT PACKAGES

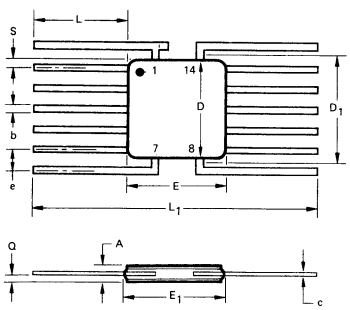
F-10-1



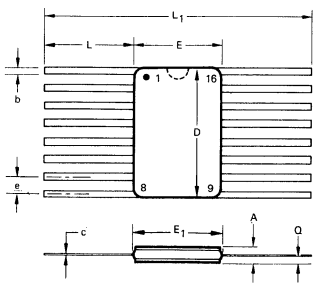

F-10-2




F-14-1 and F-14-2

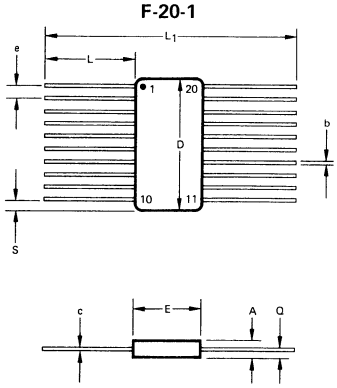



F-16-1 and F-16-2

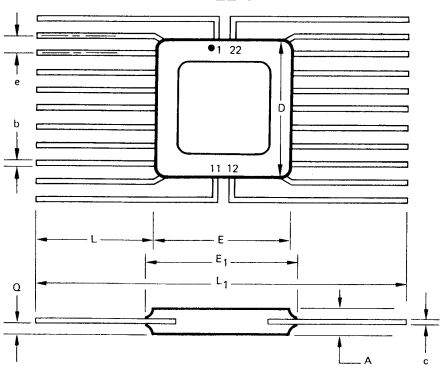



Note: Notch is pin 1 index on cerpack.

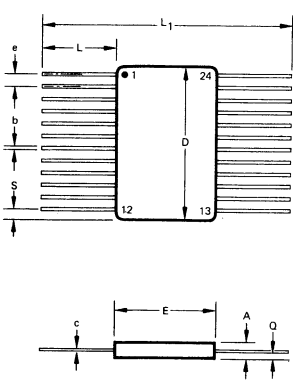
F-20-1



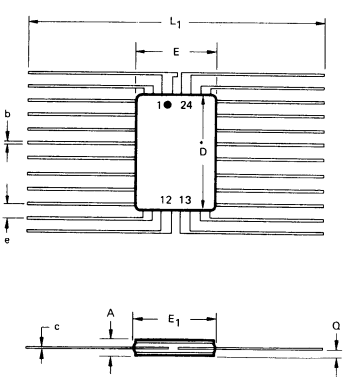

F-22-1



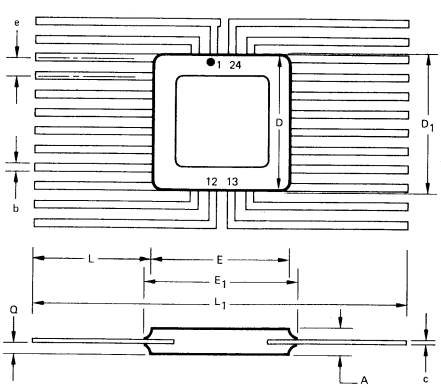

F-24-1




F-24-2



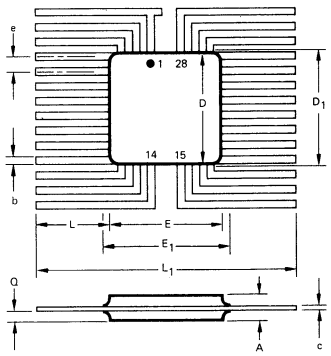

F-24-3



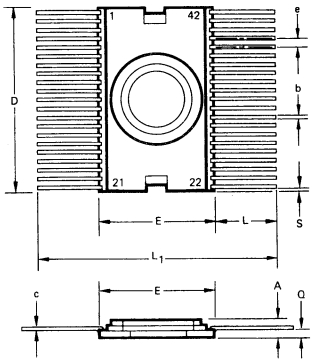
## PACKAGE OUTLINES (Cont.)

### FLAT PACKAGES (Cont.)

F-28-1




F-42-1




| AMD Pkg. | F-10-1 | | F-10-2 | | F-14-1 | | F-14-2 | | F-16-1 | | F-16-2 | | F-20-1 | | F-22-1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common NAME | CERPACK | | METAL FLAT PAK | | CERPACK | | METAL FLAT PAK | | CERPACK | | METAL FLAT PAK | | CERPACK | | METAL FLAT PAK | |
| 38510 Appendix C | F-4 | | F-4 | | .F-1 | | F-1 | | F-5 | | – | | – | | – | |
| **Parameters** | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| **A** | .045 | .080 | .045 | .080 | .045 | .080 | .045 | .085 | .045 | .085 | .045 | .085 | .045 | .085 | .045 | .090 |
| **b** | .015 | .019 | .012 | .019 | .015 | .019 | .012 | .019 | .015 | .019 | .015 | .019 | .015 | .019 | .015 | .019 |
| **c** | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 |
| **D** | .230 | .255 | .235 | .275 | .230 | .255 | .230 | .270 | .370 | .425 | .370 | .400 | .490 | .520 | .380 | .420 |
| **$D_1$** | | | | .275 | | | | .280 | | | | .410 | | | | .440 |
| **E** | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .245 | .285 | .245 | .285 | .245 | .285 | .380 | .420 |
| **$E_1$** | | .275 | | .280 | | .275 | | .280 | | .290 | | .305 | | .290 | | .440 |
| **e** | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 |
| **L** | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .250 | .320 |
| **$L_1$** | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 |
| **Q** | .010 | .040 | .010 | .040 | .010 | .040 | .010 | .040 | .020 | .040 | .010 | .040 | .020 | .040 | .010 | .040 |
| **$S_1$** | .005 | | .005 | | .005 | | .005 | | .005 | | .005 | | .005 | | | |
| **Standard Lead Finish** | b | | c | | b | | c | | b | | c | | b | | c | |

| AMD Pkg. | F-24-1 | | F-24-2 | | F-24-3 | | F-28-1 | | F-42-1 | |
|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | CERPACK | | METAL FLAT PAK | | METAL FLAT PAK | | METAL FLAT PAK | | CERAMIC FLAT PAK | |
| 38510 Appendix C | F-6 | | F-8 | | – | | – | | – | |
| **Parameters** | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| **A** | .050 | .090 | .045 | .090 | .045 | .090 | .045 | .080 | .070 | .115 |
| **b** | .015 | .019 | .015 | .019 | .015 | .019 | .015 | .019 | .017 | .023 |
| **c** | .004 | .006 | .003 | .006 | .003 | .006 | .003 | .006 | .006 | .012 |
| **D** | .580 | .620 | .360 | .410 | .380 | .420 | .360 | .410 | 1.030 | 1.090 |
| **$D_1$** | | | | .420 | | .440 | | .410 | | 1.090 |
| **E** | .360 | .385 | .245 | .285 | .380 | .420 | .360 | .410 | .620 | .660 |
| **$E_1$** | | .410 | | .305 | | .440 | | .410 | | .660 |
| **e** | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 |
| **L** | .265 | .320 | .300 | .370 | .250 | .320 | .270 | .320 | .320 | .370 |
| **$L_1$** | .920 | .980 | .920 | .980 | .920 | .980 | .955 | 1.000 | 1.300 | 1.370 |
| **Q** | .020 | .040 | .010 | .040 | .010 | .040 | .010 | .040 | .020 | .060 |
| **$S_1$** | .005 | | .005 | | 0 | | 0 | | .005 | |
| **Standard Lead Finish** | b | | c | | c | | c | | c | |

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions $E_1$ and $D_1$ allow for off-center lid, meniscus, and glass overrun.

## ORDERING INFORMATION

All Advanced Micro Devices' products listed are stocked locally and distributed nationally by Franchised Distributors. See back of this book for the location nearest you. Please consult them for the latest price revisions. For direct factory orders, call Advanced Micro Devices, 901 Thompson Place, Sunnyvale, California 94086, (408) 732-2400, TWX: 910-339-9280, TELEX: 34-6306.

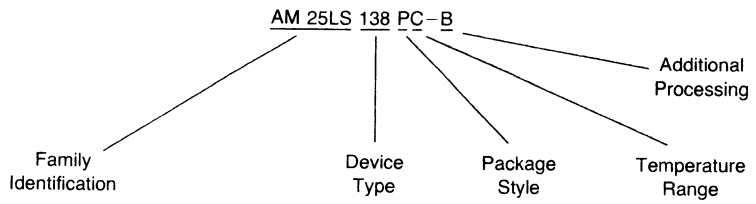
**Minimum Order**

The minimum direct factory order is $100.00 for a standard product.

The minimum direct factory order for Class B, burned-in, product is $250.00.

**Proprietary Product Ordering, Package and Temperature Range Codes**

The following scheme is used to identify Advanced Micro Devices' proprietary products.




**Package Style**

D = Hermetic DIP
F = Flat Package
P = Molded DIP
X = Dice

**Temperature Range**

C = Commercial
0°C to +70°C
M = Military
−55°C to +125°C

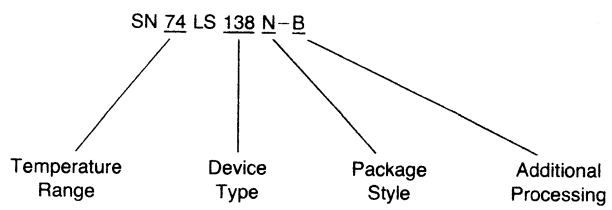
**Additional Processing**

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)
T = Additional high temperature testing

**Second Source Product Ordering, Package and Temperature Range Codes**

An order number and marking system identical to the original manufacturer's is used for the Advanced Micro Devices' pin-for-pin and electrically equivalent circuit.

The following example is the ordering scheme for Advanced Micro Devices' second source to Texas Instruments' products.




**Package Style**

J = Hermetic DIP
N = Molded DIP
W = Flat Package
X = Dice

**Temperature Range**

74 = Commercial
0°C to +70°C
54 = Military
−55°C to +125°C

**Additional Processing**

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)
T = Additional high temperature testing

## STANDARD PRODUCT PROCESSING AND OPTIONS

### 1. AMD STANDARD PRODUCT – CLASS C PROCESSING

All products manufactured by Advanced Micro Devices, including Bipolar Logic and Interface, Memory and Microprocessors, Linear and MOS/LSI meet the quality requirements of MIL-M-38510. In addition all products, both commercial and military temperature range receive the 100% screening procedures defined in the current revision of MIL-STD-883, Method 5004, Class C. This processing is described in Advanced Micro Devices' Product Assurance Document 15-010.

a) **Internal visual inspection:** Method 2010. Condition B.
b) **High temperature storage:** Method 1008, Condition C; 150°C, 24 hours.
c) **Temperature cycling:** Method 1010, Condition C; −65°C, 150°C , 10 cycles.
d) **Constant acceleration:** Method 2001, Condition E; 30,000 g., $Y_1$ plane. (Hermetic packages only.)
e) **Fine leak:** Method 1014, Condition A; $5 \times 10^{-8}$ atm cc per second. (Hermetic packages only.)
f) **Gross leak:** Method 1014, Condition C,, Step 2. (Hermetic packages only.)
g) **Continuity test** at 100°C to 0.01% AQL. (Molded packages only.)
h) **Final electrical test:** 100% D.C. and functional testing at 25°C and Group A sample per Method 5005.

To order this product, use the order number shown for the product desired. Example: AM2501DM for full military temperature range part in dual-in-line package, AM2501DC for commercial temperature range in dual-in-line package.

As noted, all material is processed to Class C and no additional price adders are imposed to deliver this level of reliability.

### 2. CLASS B PROCESSING

#### Military Temperature Range

Standard product is upgraded to Class B with a 160-hour burn-in at 125°C followed by 100% electrical testing of D.C. parameters at 25°C, 125°C, −55°C and A.C. parameters at 25°C.

Burn-in conditions are steady state power (MIL-STD-883, Method 1015.1, Condition B) for linear circuits, and steady state power and reverse bias (Condition C) for all others. Standard burn-in circuit specifications for any device are available upon request. Condition D burn-in is available to special order. Consult your local AMD sales office for price and delivery.

To order this product, use the order number shown for the product desired and add the suffix "B". Example: AM2501DM-B for military temperature product in dual-in-line package with burn-in as described, SN54LS174W-B for military temperature range product in flat pack with burn-in. This processing meets all of the requirements of MIL-STD-883, Class B product.

#### Commercial Temperature Range

Standard AMD Class C commercial temperature range product is burned-in for use in non-military systems to a modified Class B program. A 160 hour burn-in, to a method meeting the requirements of Method 1015.1, Conditions A and B, is followed by the standard Class C electrical test procedures.

To order this level of screening, use the order number shown for the commercial device and add the suffix "B". Examples: AM25LS175DC-B and SN74LS153N-B.

### 3. CLASS S PROCESSING (FORMERLY CLASS A)

Class S processing is recommended only for applications where replacement is extremely difficult and reliability is imperative. This material is only produced to special order. Consult AMD for further details.

### 4. DICE

To assist hybrid manufacturers on prototype products, all AMD dice are available in quantities of 10 pieces or more. All dice are supplied in carriers, are glass scratch protected, and except for some LSI devices, are subjected to complete functional and parametric testing. Advanced Micro Devices' dice are 100% optically inspected to meet MIL-STD-883, Method 2010 Cond. B quality levels. Detailed information on additional extended dice testing and processing is available by contacting Advanced Micro Devices.

# PRODUCT ASSURANCE
# MIL-M-38510 • MIL-STD-883
## AMD Document 15-010 Rev. D

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Two military documents provide the foundation for this program. They are:

**MIL-M-38510** – General Specification for Microcircuits
**MIL-STD-883** – Test Methods and Procedures for Microelectronics

**MIL-M-38510** describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. All circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.

**MIL-STD-883** defines detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

**Test Method 2010** defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of the latest revision of Method 2010, condition B.

**Test Method 5004** defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

**Class C** – Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

**Class B** – Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C followed by more extensive electrical measurements. All other screening requirements are the same.

**Class A** – Used where replacement is extremely difficult and reliability is imperative. Class A screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number, except that linear 100, 200 or 300 series are marked"/883B".

All molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted for solid-package parts.

**Test Method 5005** defines qualification and quality conformance procedures. Subgroups, tests and quality levels for each class are given for Group A (electrical), Group B (mechanical quality measurements related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user. Tables I, II, III and IV give standard test groupings and quality levels for Class B screened devices. These quality levels are used as a minimum for all tests for either Class B or Class C parts.

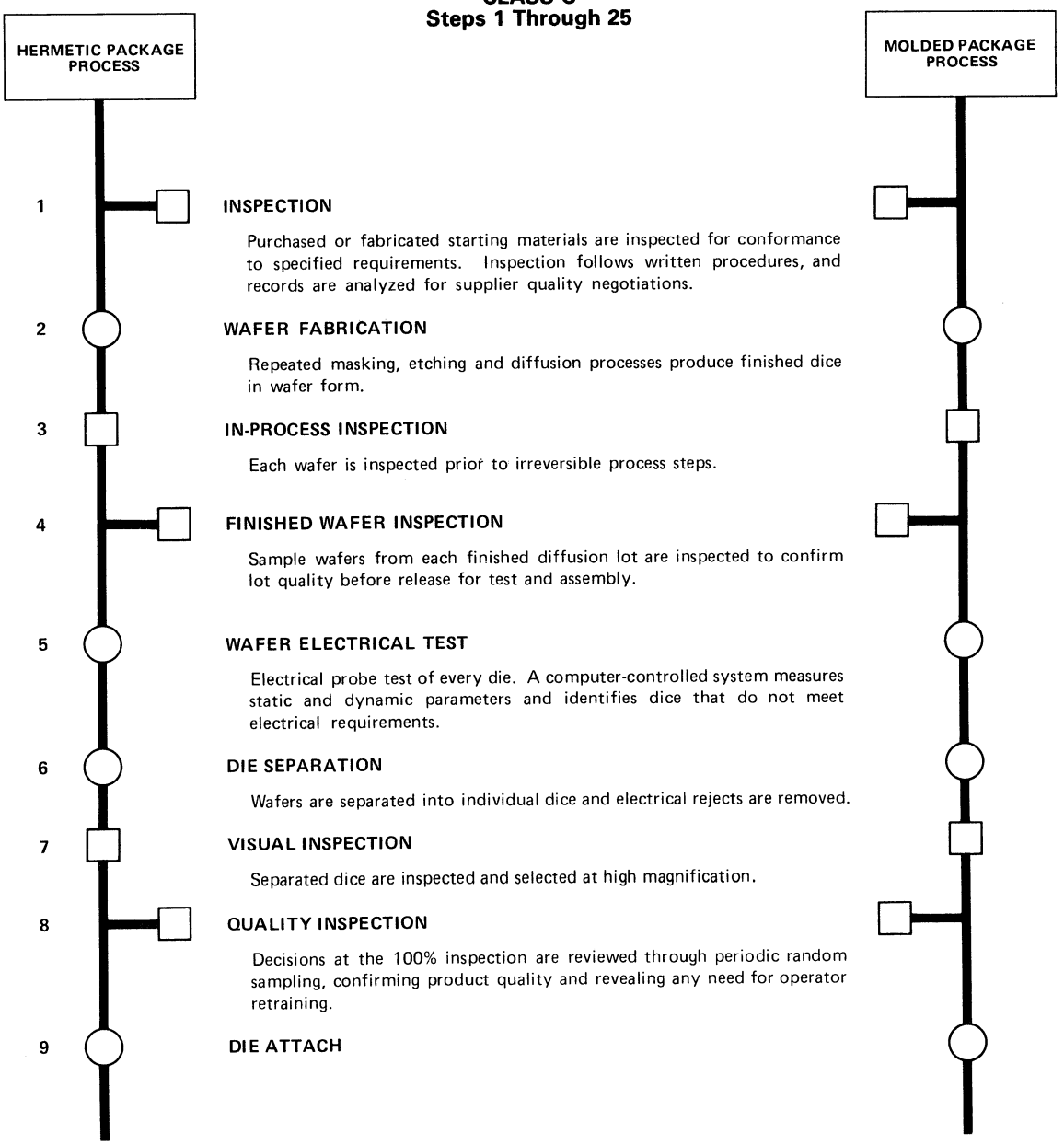
## MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B quality levels on either Class B or Class C product.

All full-temperature-range (−55°C to +125°C) circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.

### STANDARD PROCESSING CLASS C Steps 1 Through 25



10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

**QUALITY STANDARDS:**

All devices – MIL-STD-883, Method 2010, Condition B (latest revision). Full temperature devices – MIL-M-38510, Para. 3.7 for workmanship (re-bonding limits).

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

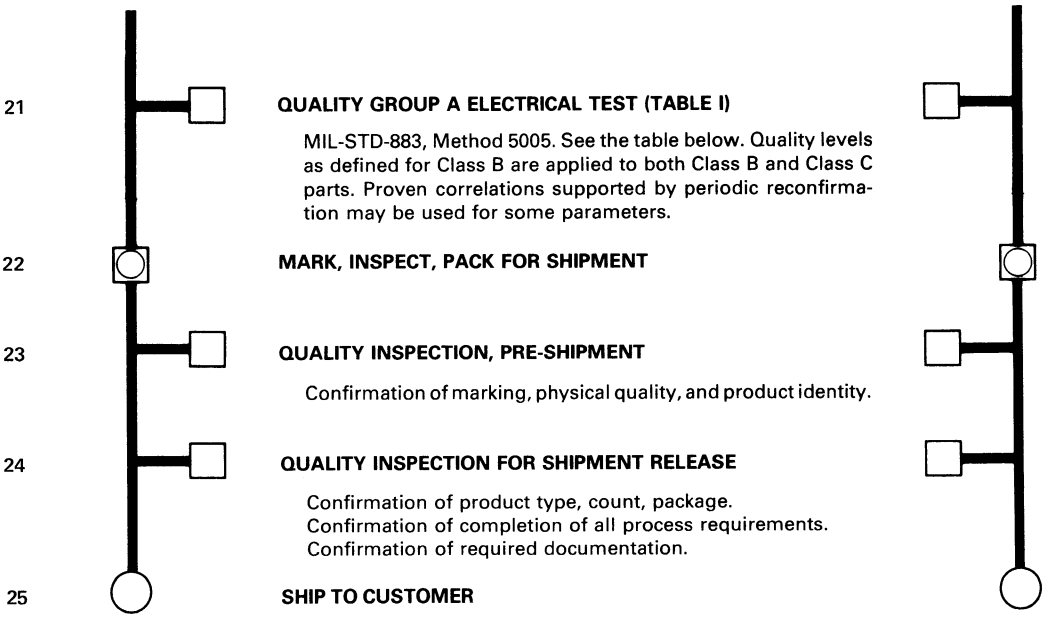
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C or in certain products at the most critical extreme temperature to assure accuracy of device selection.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

MIL-STD-883, Method 5005. See the table below. Quality levels as defined for Class B are applied to both Class B and Class C parts. Proven correlations supported by periodic reconfirmation may be used for some parameters.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

This AMD standard product meets screening requirements of MIL-STD-883, Class C.

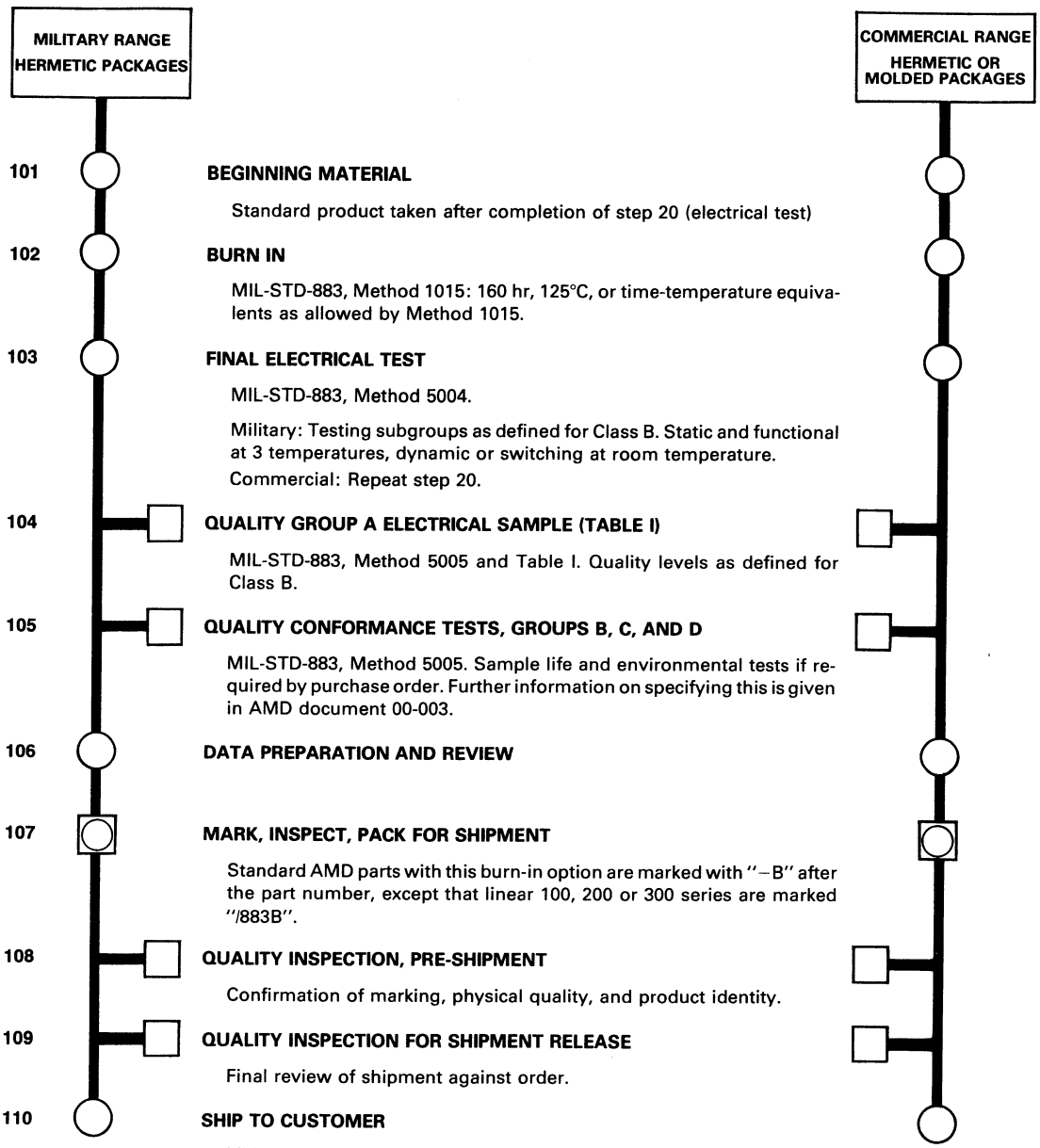
**GROUP A ELECTRICAL TESTS**
**From MIL-STD-883, Method 5005, Table I**

| Subgroups | LTPD (Note 1) | Initial Sample Size |
|---|---|---|
| **Subgroup 1** — Static tests at 25°C | 5 | 45 |
| **Subgroup 2** — Static tests at maximum rated operating temperature | 7 | 32 |
| **Subgroup 3** — Static tests at minimum rated operating temperature | 7 | 32 |
| **Subgroup 4** — Dynamic tests at 25°C — Linear devices | 5 | 45 |
| **Subgroup 5** — Dynamic tests at maximum rated operating temperature — Linear devices | 7 | 32 |
| **Subgroup 6** — Dynamic tests at minimum rated operating temperature — Linear devices | 7 | 32 |
| **Subgroup 7** — Functional tests at 25°C | 5 | 45 |
| **Subgroup 8** — Functional tests at maximum and minimum rated operating temperatures | 10 | 22 |
| **Subgroup 9** — Switching tests at 25°C — Digital devices | 7 | 32 |
| **Subgroup 10** — Switching tests at maximum rated operating temperature — Digital devices (Note 2) | 10 | 10 |
| **Subgroup 11** — Switching tests at minimum rated operating temperature — Digital devices (Note 2) | 10 | 10 |

1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. These subgroups are usually performed during initial device characterization only.

## OPTIONAL EXTENDED PROCESSING
## CLASS B
## Steps 101 Through 110

Advanced Micro Devices offers several extended processing options to meet customer high-reliability requirements. These are defined in AMD document 00-003. The flow chart below outlines Option B, a 160-hr. burn in. Military temperature range devices processed to this flow (in the left column) meet the screening requirements of MIL-STD-883, Class B.




**101** **BEGINNING MATERIAL**

Standard product taken after completion of step 20 (electrical test)

**102** **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C, or time-temperature equivalents as allowed by Method 1015.

**103** **FINAL ELECTRICAL TEST**

MIL-STD-883, Method 5004.

Military: Testing subgroups as defined for Class B. Static and functional at 3 temperatures, dynamic or switching at room temperature.

Commercial: Repeat step 20.

**104** **QUALITY GROUP A ELECTRICAL SAMPLE (TABLE I)**

MIL-STD-883, Method 5005 and Table I. Quality levels as defined for Class B.

**105** **QUALITY CONFORMANCE TESTS, GROUPS B, C, AND D**

MIL-STD-883, Method 5005. Sample life and environmental tests if required by purchase order. Further information on specifying this is given in AMD document 00-003.

**106** **DATA PREPARATION AND REVIEW**

**107** **MARK, INSPECT, PACK FOR SHIPMENT**

Standard AMD parts with this burn-in option are marked with "–B" after the part number, except that linear 100, 200 or 300 series are marked "/883B".

**108** **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

**109** **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Final review of shipment against order.

**110** **SHIP TO CUSTOMER**

Military temperature range parts meet screening requirements of MIL-STD-883, Class B.

## OTHER OPTIONS

Document 00-003, "Extended Processing Options", further defines Option B as well as other screening or sampling options available or special order. Available options are listed here for reference.

| Option | Description | Effect |
|---|---|---|
| A | Modified Class A screen (The AMD-A program) | Provides space-grade product, following most Class A requirements of MIL-STD-883, Method 5004. |
| B | 160-hr operating burn in | Upgrades a part from Class C to Class B. |
| X | Radiographic inspection (X-ray) | Related to Option A. Provides limited internal inspection of sealed parts. |
| S | Scanning Electron Microscope (SEM) metal inspection | Sample inspection of metal coverage of die. |
| V | Preseal visual inspection to MIL-STD-883, Method 2010, Cond. A | More stringent visual inspection of assemblies and die surfaces prior to seal. |
| P | Particle impact noise (PIN) screen with ultrasonic detection. | Detects loose particles of approximately 0.5 mil size or larger, which could affect reliability in zero-G or high vibration applications. |
| Q | Quality conformance inspection (Group B, C and D life and environmental tests) | Samples from the lot are stressed and tested per Method 5005. The customer's order must state which groups are required. Group B destroys 16 devices; Group C, 92 devices; Group D, 60 devices. |



Document 15-010 Rev. D, July 1, 1977 (editorial changes to clarify options)

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