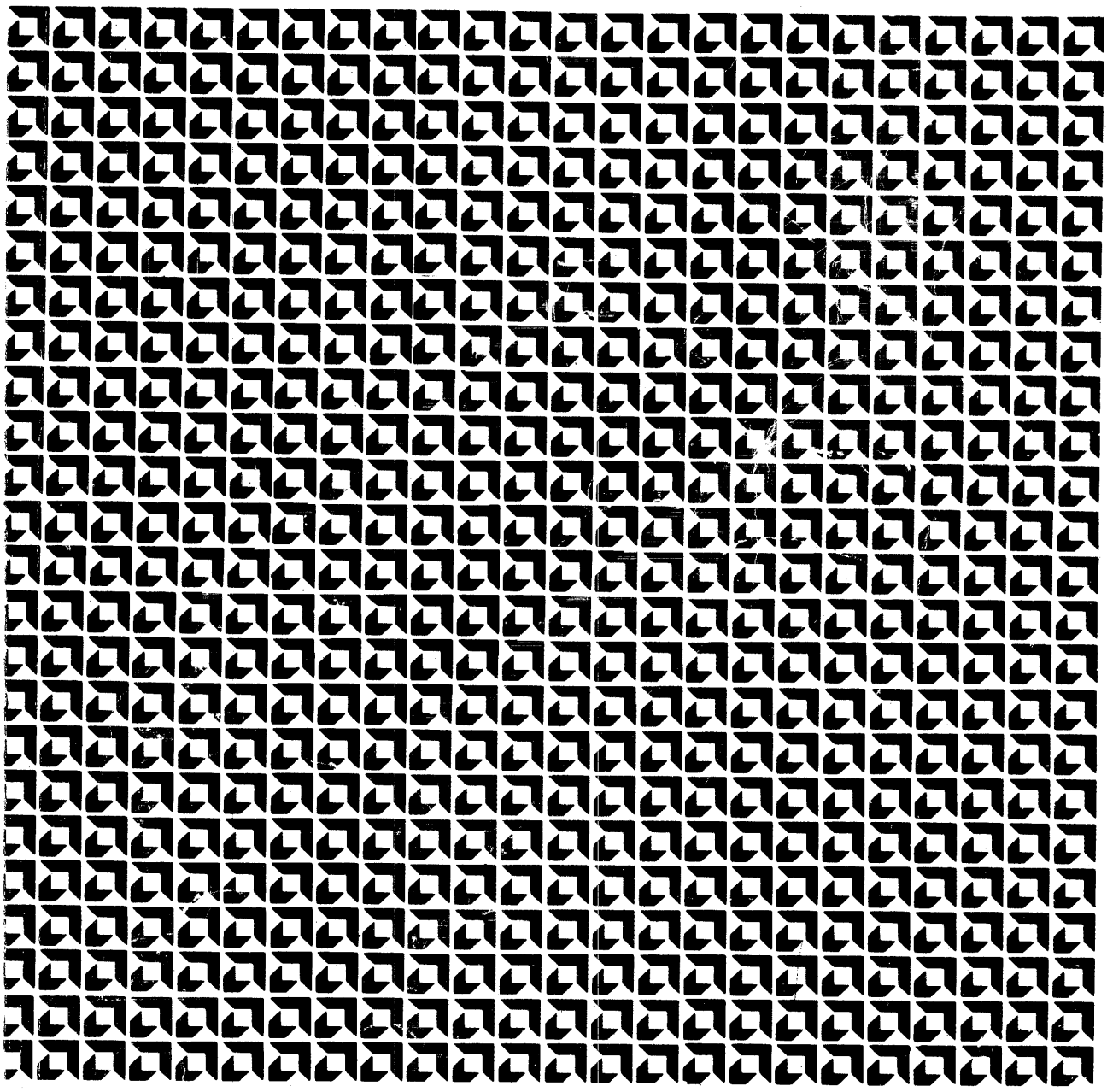
Advanced Micro Devices

The Am2900 Family Data Book



Advanced Micro Devices

The Am2900 Family Data Book With Related Support Circuits

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AM-PUB003

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Am2900 COMPONENTS CONTINUOUSLY BECOME FASTER AND FASTER

MORE SPEED: NO MORE POWER

There's a good old tried and proven way to make faster IC's – burn more power. (That's the only real difference between "LS" and "S" devices). But that solution isn't satisfactory for LSI devices like the Am2900 family. Power is constrained to existing levels for reliability reasons.

Am2900 parts are always designed to obtain the maximum speed at a power level which is safe for the package types and operating environment of the part. To increase speeds, new technologies must be used to build faster components at no increase in power.

NEW CIRCUIT DESIGN TECHNIQUES MAKE FASTER GATES

One way to make faster components is to use new circuit design techniques. The most obvious is internal ECL, which provides very fast gates at similar power levels to LS TTL. Other design techniques, such as low-level logic (with very small logic swings on-chip), can also provide higher speeds without introducing the time penalty of ECL to TTL conversion.

Finally, very low power gates used in non-critical speed paths make more power available for use in critical speed paths. As the 2900 family develops, all these technologies will be used within a single component to achieve the highest speeds without increasing power. Among the first products to take advantage of mixed-circuit technology will be the Am2903A.

IMPROVED PROCESS CONTROL ALLOWS TIGHTER SPECS

Today's 2900 parts are carefully characterized over a wide range of voltages, temperatures, and process parameters before an AC specification is published. As manufacturing technology improves, the process is subject to smaller run-to-run variations, so that all of the product is closer to design nominal. This makes it possible to specify parameters more closely to typical without incurring large yield losses. The first product reflecting this is the Am2903.

WHAT'S GOOD FOR THE GOOSE IS GOOD FOR THE GANDER

Many new tools in production technology are emerging, primarily spurred by the emphasis on high-speed MOS memories. The same tools, such as projection masking, also provide for smaller geometries in bipolar circuits. As MOS gets faster, so does bipolar. The Am2901B obtains its speed improvement over the Am2901A through these tools.

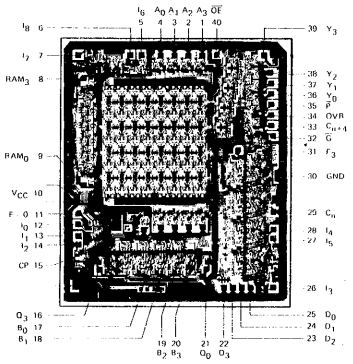
DESIGN FOR THE FUTURE

Every Am2900 part will undergo an evolution as new technologies become practical for production. Every part type will continuously become faster. Within a few short years, 2900-based designs will compete favorably with Schottky MSI on a speed basis at a fraction of the component count.

Most existing 2900 designs can be offered in higher performance versions simply by substitution of the 2901B for the 2901A, the 2909A for the 2909, the 2903A for the 2903, and so forth. Your 2900 design won't run out of speed in a few years. Advanced Micro Devices' 2900 Family will serve tomorrow's needs as well as today's.

SMALLER DIE SIZES MAKE FASTER PARTS

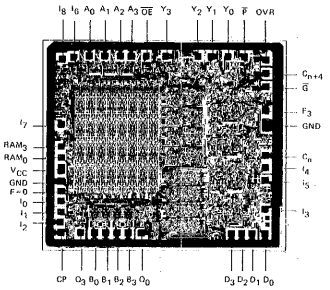
Am2901



DIE SIZE 0.167" X 0.198"

Speed A,B → $\overline{G},\overline{P}$ 80ns

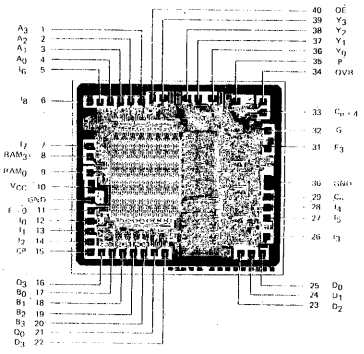
Am2901A



DIE SIZE 0.132" X 0.149"

Speed A,B → $\overline{G},\overline{P}$ 65ns

Am2901B



DIE SIZE 0.117" X 0.128"

Speed A,B → $\overline{G},\overline{P}$ 50ns

INTRODUCTION

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems – circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

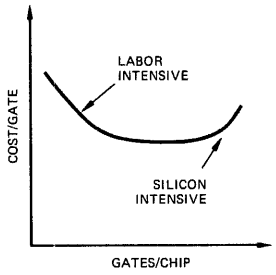


Figure 1. MPR-001

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product – it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

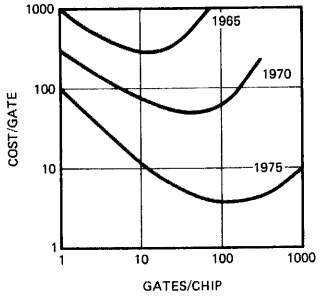


Figure 2. MPR-002

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10-20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20-50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic is around 500 gates/chip.

GENERATION III – The Am2900 Family, 1976

At a 500-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions is needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

The Am2900 Family consists of circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast – utilizing Low-Power Schottky TTL technology; they are expandable; they are flexible – useful in emulation; and they are driven under microprogram control.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am9080A.

While an Am9080A can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am9080A design will, therefore, almost always be cheaper. But the Am9080A, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, usually eight bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10–100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform – reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 3 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901 array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901's), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901 registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901's and sent out to the memory address register (MAR). The four status bits from the 2901's ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909, 2910, or 2911 is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901 instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901 array (Figure 19 on 2901 data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or a 9080A instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 3 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located – the μPC, the stack, or the direct inputs – and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the block labeled "control logic". Frequently this is a PROM or PLA. In the case of the Am2910, it is built into the chip. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two. The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 3.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901's are executing one instruction, the next instruction is being fetched from ROM. Note that there is no sequential logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901's. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

Introduction

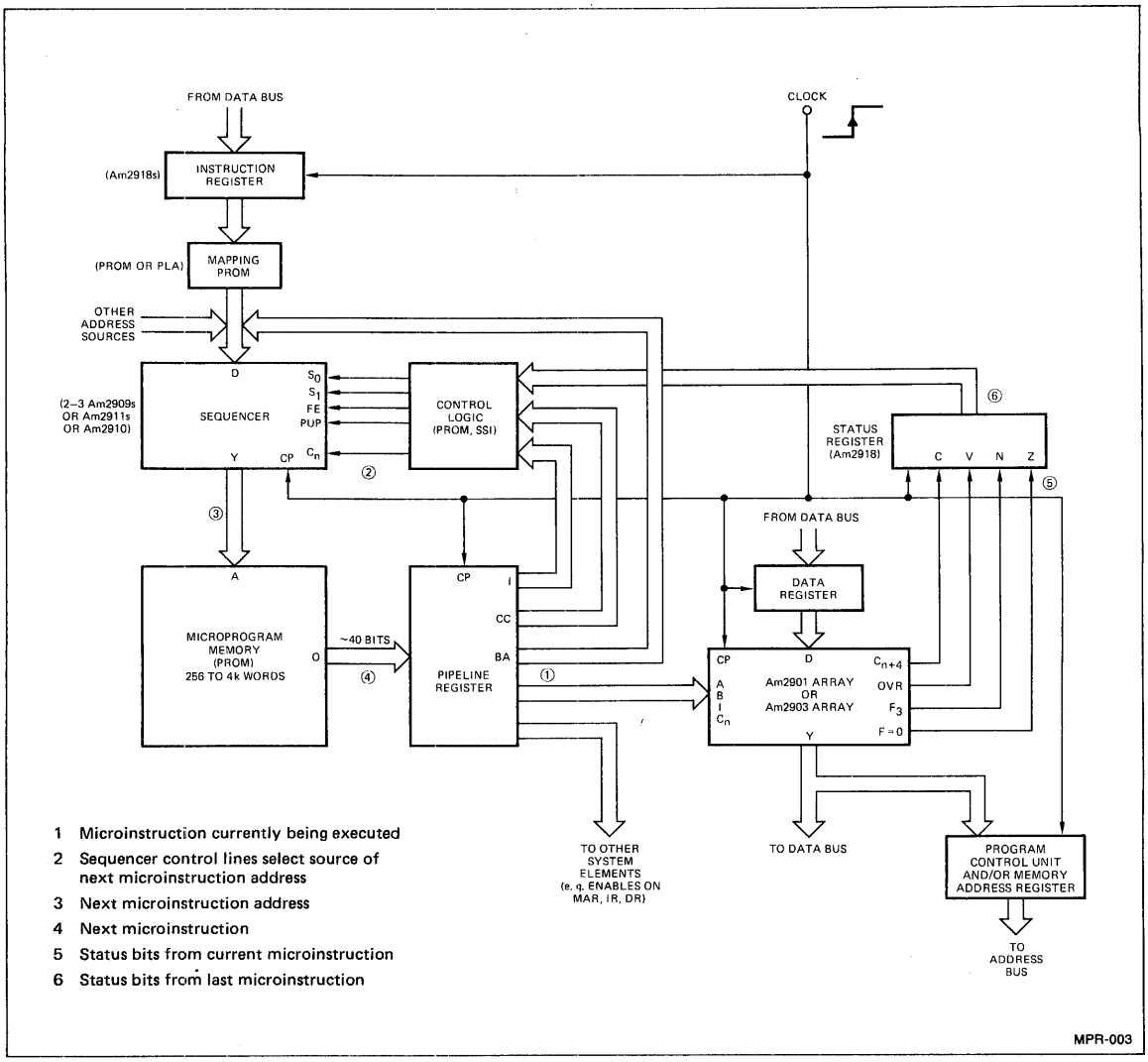


Figure 3.

The system shown in Figure 3 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901 working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-8450. Ask for Am2900 Family Applications.

Am2901 • Am2901A • Am2901B

Four-Bit Bipolar Microprocessor Slice

2

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.
- Fast –
  Am2901B is up to 27% faster than Am2901A, up to 50% faster than Am2901. The Am2901B meets or exceeds all of the specifications for the Am2901 and Am2901A.

TABLE OF CONTENTS

For applications information see the last part of this data sheet and chapters III and IV of "Build a Microcomputer", AMD's application note series on the Am2900 Family.

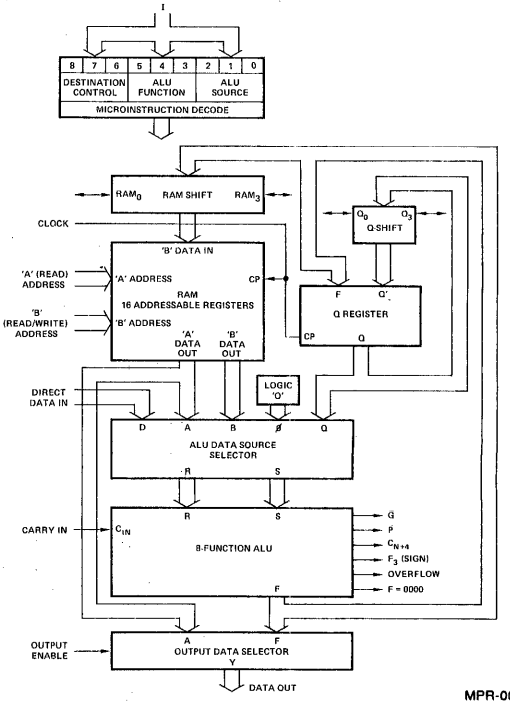
GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

The Am2901B is a plug-in replacement for the Am2901 or Am2901A, but is 25% faster than the Am2901A and 50% faster than the Am2901.

MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-004

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

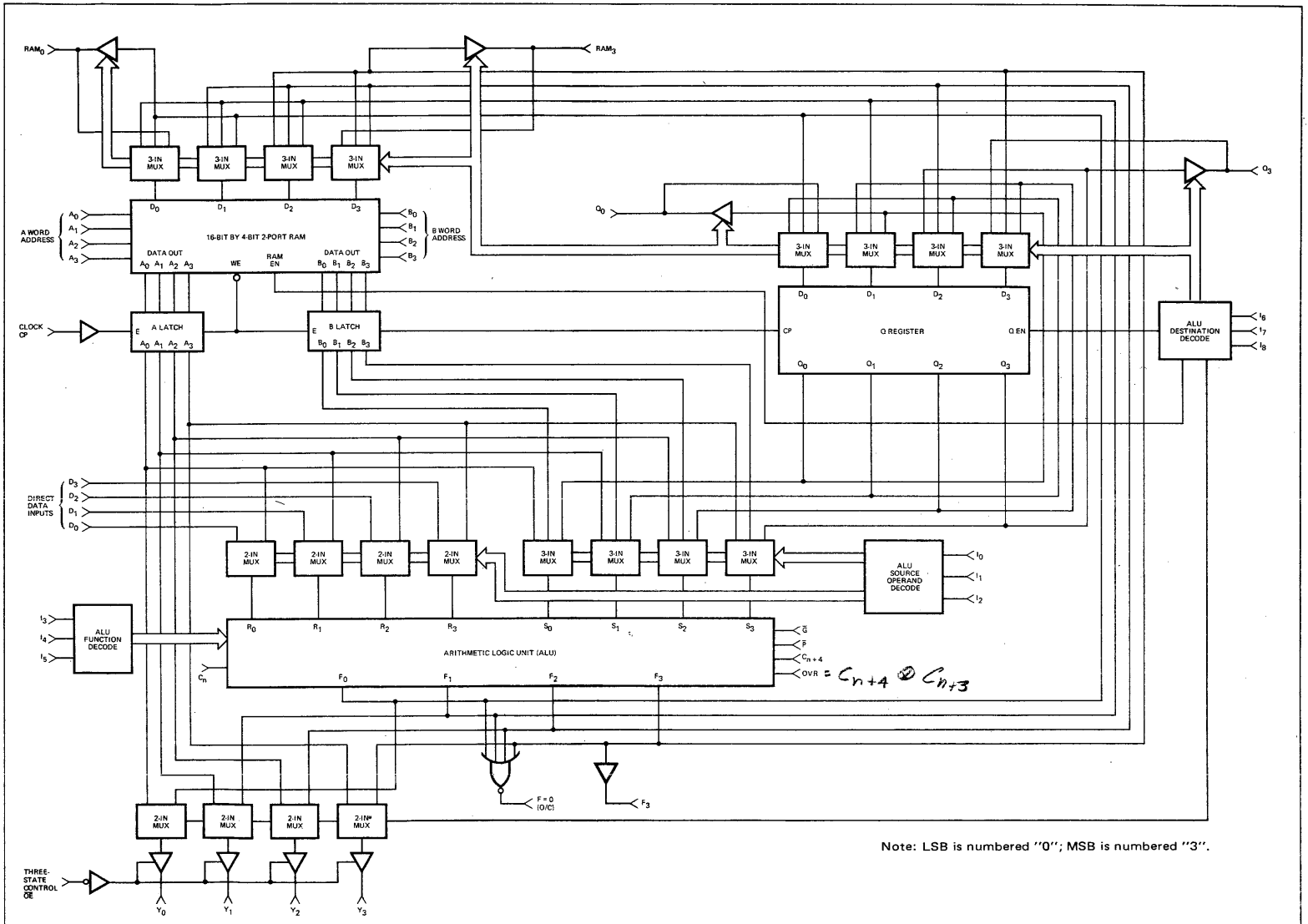


Figure 1. Detailed Am2901B Microprocessor Block Diagram.

MPR-005

	MICRO CODE				ALU SOURCE OPERANDS	
Mnemonic	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 2. ALU Source Operand Control.

	MICRO CODE				ALU	
Mnemonic	I_5	I_4	I_3	Octal Code	Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
Mnemonic	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

✕ DON'T USE □ DISABLE $\overline{FEN}$ △ ENABLE $\overline{FEN}$

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210}	OCTAL	0	1	2	3	4	5	6	7
OCTAL I_{543}	ALU Source / ALU Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

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Octal I_{543}, I_{210}	Group	Function
40	AND	A∧Q
41		A∧B
45		D∧A
46		D∧Q
30	OR	A∨Q
31		A∨B
35		D∨A
36		D∨Q
60	EX-OR	A∀Q
61		A∀B
65		D∀A
66		D∀Q
70	EX-NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A}$∧Q
51		$\overline{A}$∧B
55		$\overline{D}$∧A
56		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
00	ADD	A+Q	ADD plus one	A+Q+1
01		A+B		A+B+1
05		D+A		D+A+1
06		D+Q		D+Q+1
02	PASS	Q	Increment	Q+1
03		B		B+1
04		A		A+1
07		D		D+1
12	Decrement	Q–1	PASS	Q
13		B–1		B
14		A–1		A
27		D–1		D
22	1's Comp. (INV)	–Q–1	2's Comp. (Negate)	–Q
23		–B–1		–B
24		–A–1		–A
17		–D–1		–D
10	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
11		B–A–1		B–A
15		A–D–1		A–D
16		Q–D–1		Q–D
20		A–Q–1		A–Q
21		A–B–1		A–B
25		D–A–1		D–A
26		D–Q–1		D–Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})}$	Seenote

Note: $[\overline{P}_2+\overline{G}_2\overline{P}_1+\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3+\overline{G}_3\overline{P}_2+\overline{G}_3\overline{G}_2\overline{P}_1+\overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

ORDERING INFORMATION

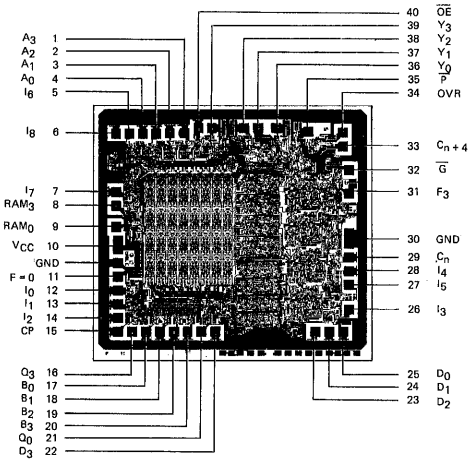
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2901 Order Number	Am2901A Order Number	Am2901B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2901PC	AM2901APC	AM2901BPC	P-40	C	C-1
AM2901DC	AM2901ADC	AM2901BDC	D-40	C	C-1
AM2901DC-B	AM2901ADC-B	AM2901BDC-B	D-40	C	B-2 (Note 4)
	AM2901ADM	AM2901BDM	D-40	M	C-3
	AM2901ADM-B	AM2901BDM-B	D-40	M	B-3
	AM2901AFM	AM2901BFM	F-42	M	C-3
	AM2901AFM-B	AM2901BFM-B	F-42	M	B-3
	AM2901AXC	AM2901BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
	AM2901AXM	AM2901BXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Figure 9.

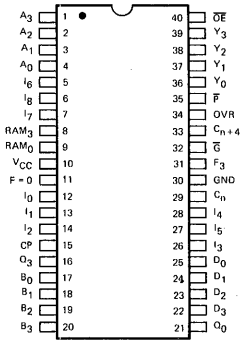
METALLIZATION AND PAD LAYOUT



Am2901B
DIE SIZE 0.117" X 0.128"

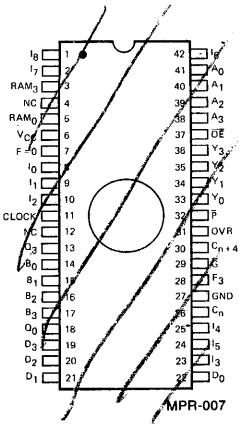
CONNECTION DIAGRAM
Top View

DIP



MPR-006

FLAT PACK CONNECTIONS
Top View



MPR-007

Note: Pin 1 is marked for orientation.

Figure 10.

2

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Part Number Suffix	V_{CC}	Temperature
PC, PCB, DC, DCB XC	4.75V to 5.25V	T_A = 0°C to +70°C
DM, DMB FM, FMB XM	4.50V to 5.50V	T_C = −55°C to +125°C

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq$ 0.4V and $V_{IH} \geq$ 2.4V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3	V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
			$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4V (Note 4)			100	
				V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX. (See Fig. 11)	COM'L and MIL	T_A = 25°C		160	250	mA
			COM'L Only	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			MIL Only	T_C = −55°C to +125°C			280	
				T_C = +125°C			198	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901XM, DM, FM. "COM'L" = Am2901XC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

I. Am2901B Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BPC
Am2901BDC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↓	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. Am2901B Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BDM
Am2901BFM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.	88ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	82	84	80	70	90	86	94	–
D	44	38	40	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	46	65	55	58	–
I345	58	58	58	48	64	56	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ↓	53	50	49	41	63	58	61	31

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	30	0 (Note 3)	88 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	55	0
Cn	–	–	42	0
I012	–	–	58	0
I345	–	–	62	0
I678	14	Do Not Change		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	40	25

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

III. Am2901A Guaranteed Commercial Range Performance

The Am2901B meets or exceeds all of the specifications for the earlier Am2901A. Parts may still be ordered and marked as Am2901A.

IV. Am2901A Guaranteed Military Range Performance

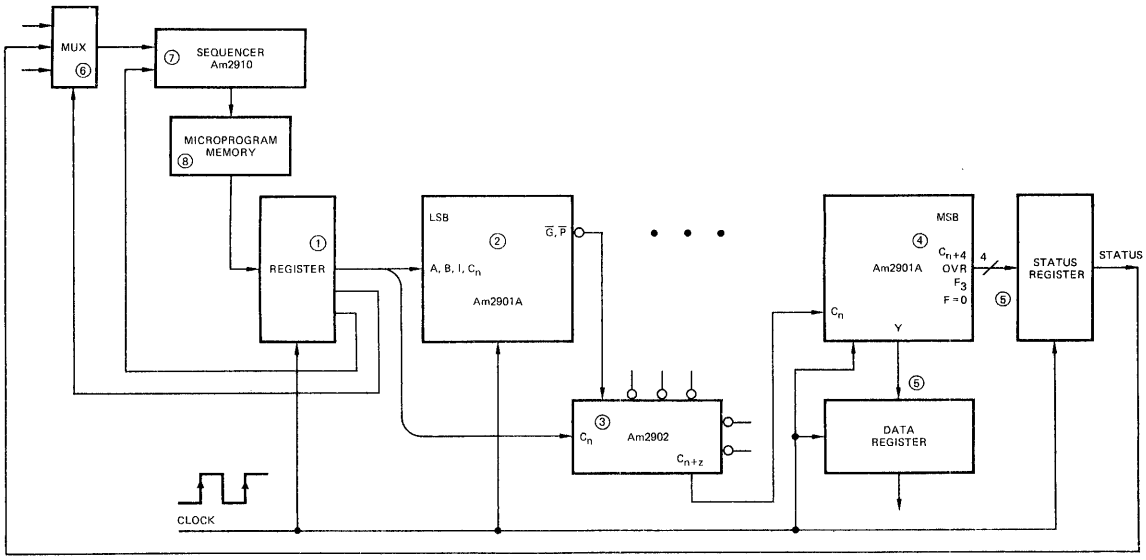
The Am2901B meets or exceeds all of the specifications for the earlier Am2901A. Parts may still be ordered and marked as Am2901A.

V. Am2901 Guaranteed Commercial Range Performance

The Am2901B meets or exceeds all of the specifications of the Am2901. Parts may still be ordered and marked as Am2901.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



MPR-010

Pipelined System. Add without Simultaneous Shift.

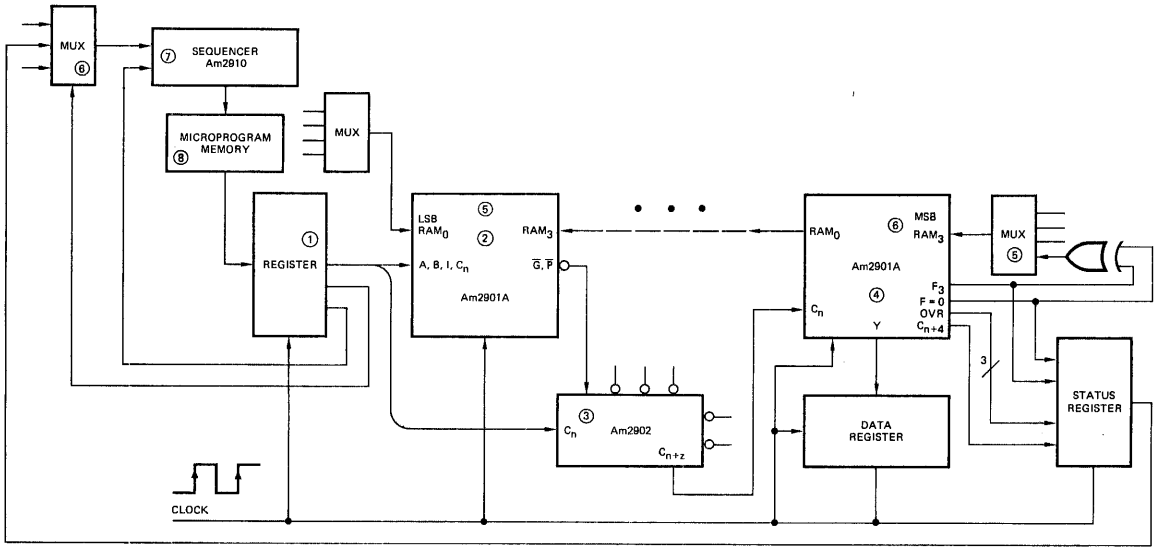
DATA LOOP			CONTROL LOOP		
① Register	Clock to Output	15	① Register	Clock to Output	15
+ ② 2901B	A, B to $\overline{G}$, $\overline{P}$	50	+ ⑥ MUX	Select to Output	20
+ ③ 2902	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10	+ ⑦ 2910	CC to Output	45
+ ④ 2901B	C_n to C_{n+4}, OVR, F_3, F = 0, Y	37	+ ⑧ PROM	Access Time	55
+ ⑤ Register	Set-up Time	5	+ ① Register	Set-up Time	5
		117ns			140ns

Minimum clock period = 140ns

Figure 12.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS (Cont.)

Speeds used in calculations for parts other than Am2901B are representative for available MSI parts.



MPR-011

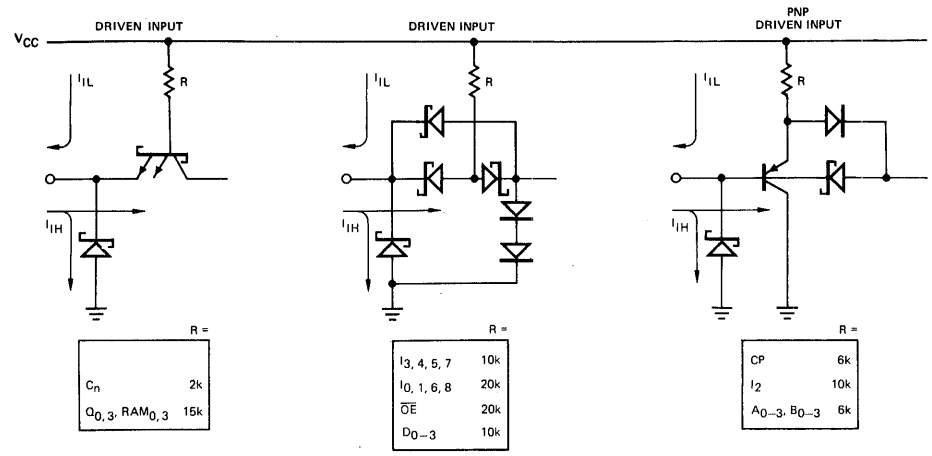
Pipelined System. Simultaneous Add and Shift Down.

DATA LOOP		
① Register	Clock to Output	15
+ ② 2901B	A, B to $\overline{G}$, $\overline{P}$	50
+ ③ 2902	$\overline{G}_0\overline{P}_0$ to C_{n+z}	10
+ ④ 2901B	C_n to F_3, OVR	29
+ ⑤ XOR and MUX		21
+ ⑥ 2901B	RAM_3 Set-up	16
		141ns

CONTROL LOOP		
① Register	Clock to Output	15
+ ⑥ MUX	Select to Output	20
+ ⑦ 2910	CC to Output	45
+ ⑧ PROM	Access Time	55
+ ① Register	Set-up Time	5
		140ns

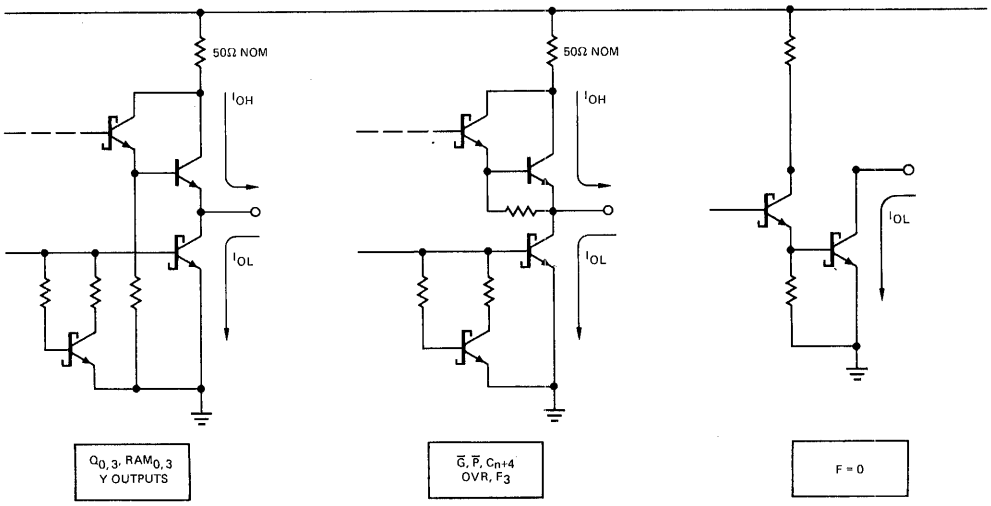
Minimum clock period = 141ns

Figure 12 (Cont).



MPR-013

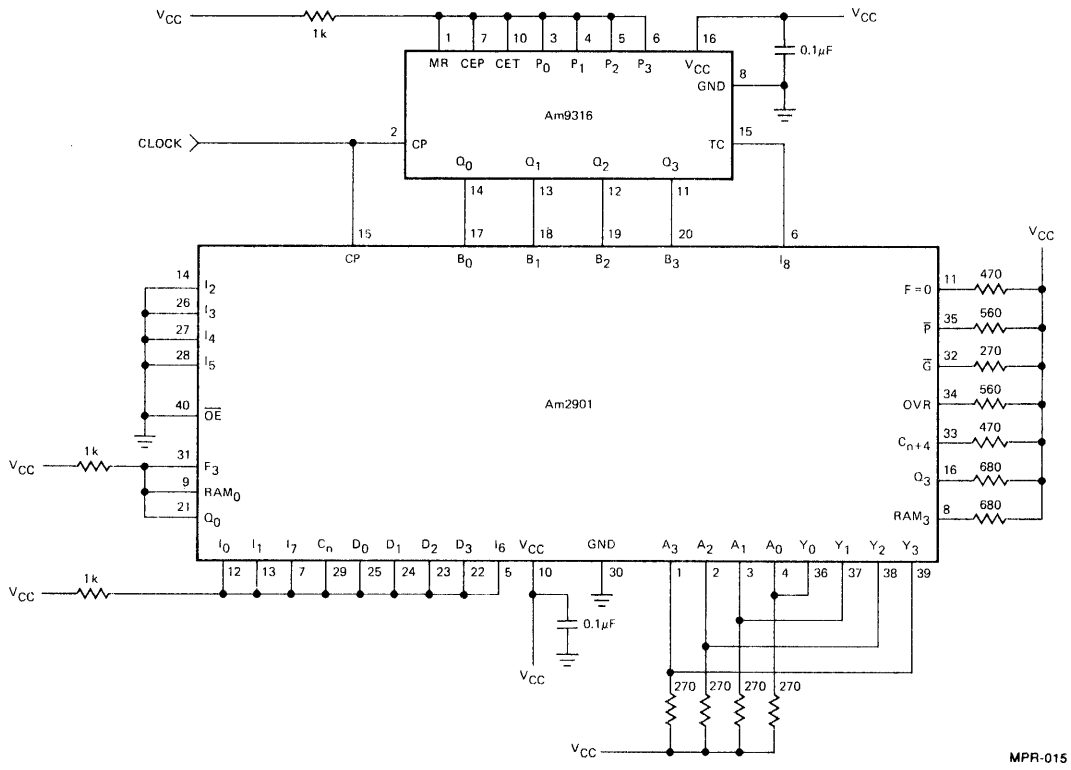
$C_I \approx 5.0$pF, all inputs



MPR-014

$C_O \approx 5.0$pF, all outputs

Figure 13. Input/Output Current Interface Conditions.



V_{CC} = 5.0 V
Frequency = 100 KHz
T_A = 125°C

This circuit conforms to MIL-STD-883, method 1015, condition D.

Figure 14. Life Test and Burn-in Circuit for Military Class B Parts.
(Contact Factory for Commercial Burn-in Conditions)

USING THE Am2901

BASIC SYSTEM ARCHITECTURE

The Am2901 is designed to be used in microprogrammed systems. Figure 15 illustrates such an architecture. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the Am2901. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the Am2901's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the Am2901's, an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2901's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

EXPANSION OF THE Am2901

The Am2901 is a four-bit CPU slice. Any number of Am2901's can be interconnected to form CPU's of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 16 illustrates the interconnection of three Am2901's to form a 12-bit CPU, using ripple carry. Figure 17 illustrates a 16-bit CPU using carry lookahead, and Figure 18 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 16. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all Am2901's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 19)

The open collector F = 0 outputs of all the Am2901's are connected together and to a pull-up resistor. This line will go HIGH if and only if the output of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic

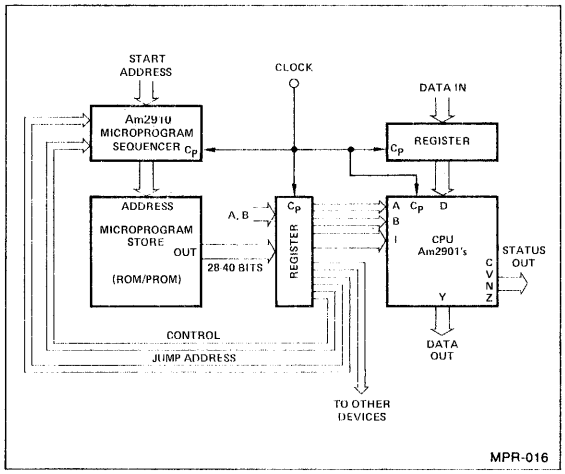


Figure 15. Microprogrammed Architecture Around Am2901's.

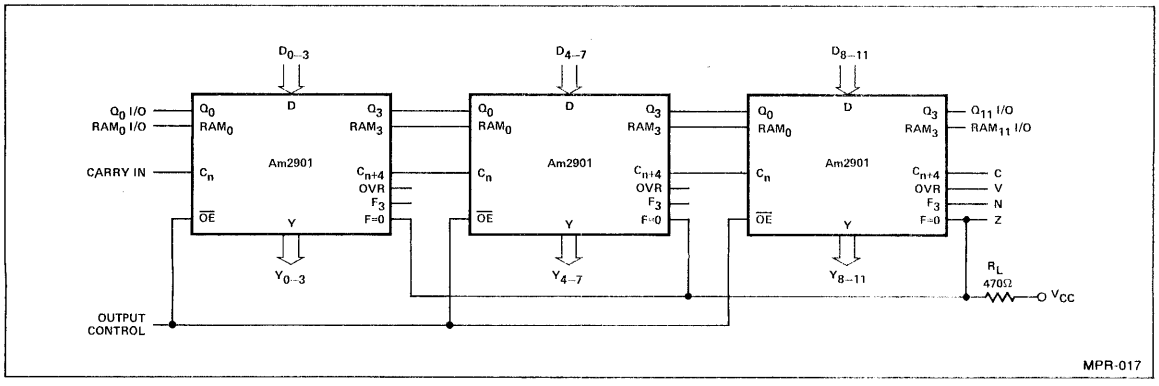


Figure 16. Three Am2901's used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected Together.

operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.

The carry-out from the most significant Am2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the Am2902 lookahead carry generator. The scheme is identical to that used with the 74181/74182. Users unfamiliar with this technique should refer to AMD's application note on Arithmetic Logic Units. Figures 17 and 18 illustrate single and multiple level lookahead.

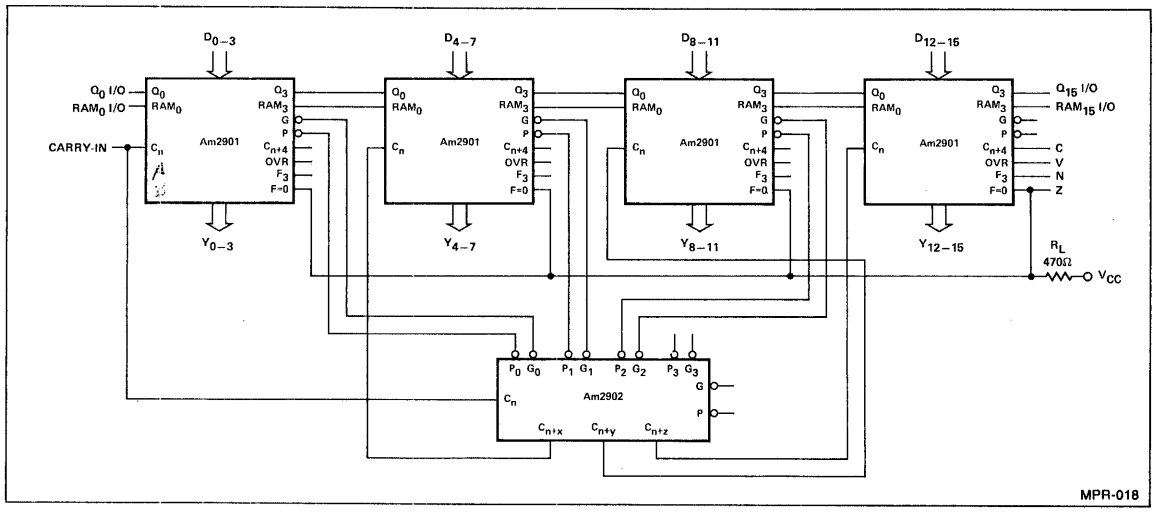


Figure 17. Four Am2901s in a 16-Bit CPU Using the Am2902 for Carry Lookahead.

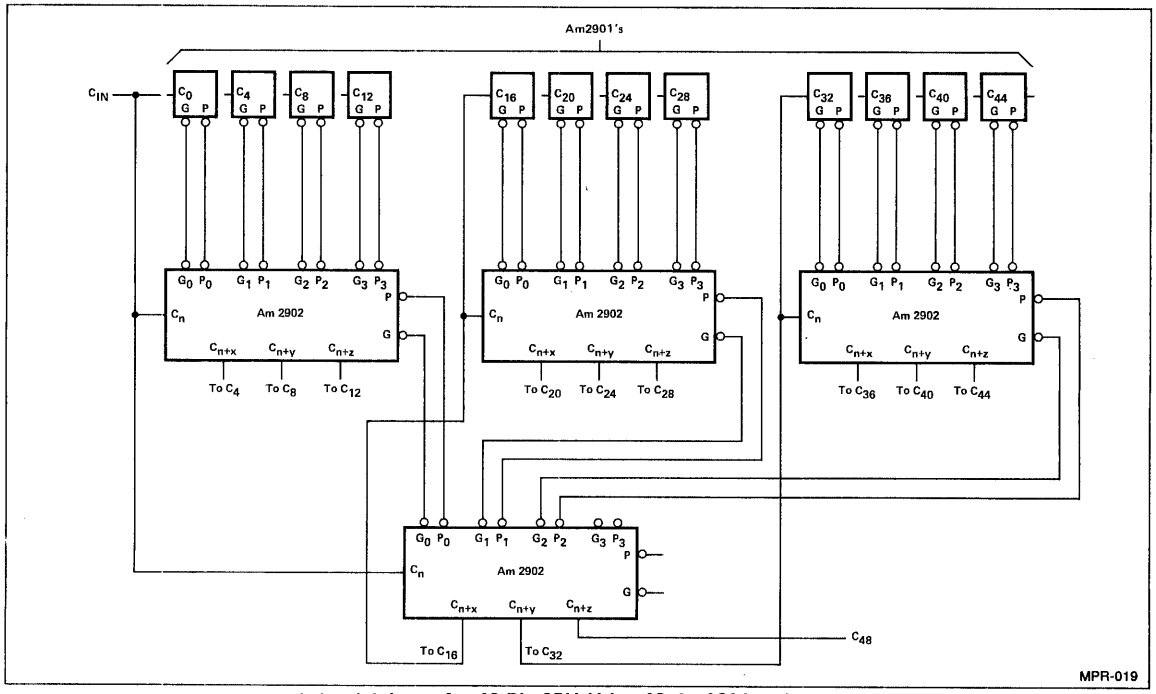


Figure 18. Carry Lookahead Scheme for 48-Bit CPU Using 12 Am2901s. The Carry-Out Flag (C_{48}) Should be Taken From the Lower Am2902 Rather Than the Right-Most Am2901 for Higher Speed.

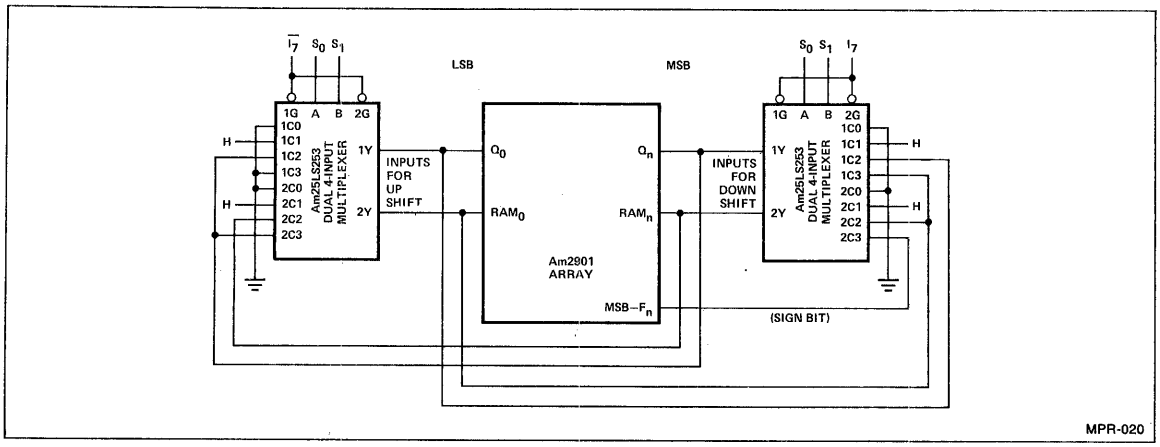


Figure 19. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. The Am2904 includes these multiplexers in a single LSI chip. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the Am2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}		One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1		One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 20 illustrates the interconnections for a hardware multiplication using the Am2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple — the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the Am2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output, and both Q and the ALU output are shifted down one place. The instruction lines to the Am2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 20 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) Am2901s shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

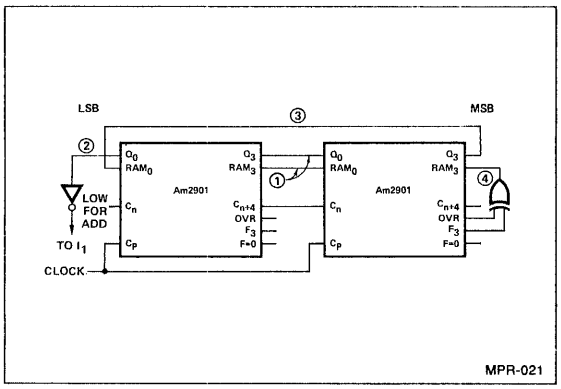


Figure 20. Interconnection for Dedicated Multiplication (8 by 8 Bit) (Corresponding A, B and I Connected Together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F_3}$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight.

$$Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 21 is a table showing the input states of the Am2901 for each step of a signed, two's complement multiplication. The Am2904 LSI chip conveniently implements the required shift linkages and the EX-OR function for this algorithm.

Initial Register States

R	
0	Multiplier
1	Multiplicand
2	X
3	X

Am2901 Microcode

Program 2's Comp. Multiply
Date 8/5/75 By J. S.

Final Register States

R	
0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O ∨ A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O ∧ B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = \overline{Q_0}$ LO	0	–	RAM$_0$	–	$F_3 \forall$ OVR		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = \overline{Q_0}$ LO	1	–	RAM$_0$	–	$F_3 \forall$ OVR		
O ∨ Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 21.

Hardware Division

Division, unlike multiplication, is much more difficult to realize. One of these difficulties can be easily understood by visualizing a 2n-bit Dividend (X) and an n-bit Divisor (Y). The Quotient (Q) can range from 1 bit (when $X \leq Y$) to 2 n bits (when $Y = 1$), discarding the attempt to divide by 0. In most of the divide functions, the Remainder (R) is as important to find as is the Quotient – there is no equivalent to it in multiplication. Division becomes even more complicated when negative numbers are represented in the 2's complement notation. In the "everyday" decimal system, using Sign-and-Magnitude notation, dealing with negative numbers is relatively easy: The sign of the quotient is determined first and then a normal division is performed. Note that in this "normal" division we first "guess" the first digit of the quotient by comparing the most significant part of the dividend to the divisor. Then verify our guess by a multiplication (no "direct" division method is known), and continue to do so for all of the other digits, shifting the divisor to the right one place at a time.

The most straightforward division scheme (for unsigned numbers) is Subsequent Subtraction. The algorithm is as follows: Subtract divisor from dividend and increment a counter (initially reset to zero). Continue to do so as long as the Remainder is positive. When the Remainder becomes negative, cancel the last step; i.e., add back divisor and decrement counter. The counter will contain the Quotient and the Remainder will be correct. The main drawback of this scheme is, of course, the great number of arithmetic operations needed. Again, when dealing with signed numbers, the subtraction should be substituted by addition and vice versa.

A more rapid division can be realized by calculating the Quotient digits instead of counting them. In this algorithm, the divisor is first subtracted from the most significant part of the dividend. If the remainder is positive, the quotient digit is "1", otherwise the subtraction is cancelled (by adding the divisor to the remainder) and the quotient digit will be "0". Now shift the remainder one place to the right (much like you do in a "paper and pencil" division) and repeat until all the quotient digits have been calculated. This algorithm is called "Restoring Division". When signed numbers are involved, inversion of the operations and the quotient digits will be necessary and correction should be performed in some cases. Some time is wasted in the Restoring Division because for every "0" digit in the quotient, two arithmetic operations are needed. This can be saved in the "Non-Restoring Division".

The basis of Non-Restoring Division is the same as in Restoring Division. Consider first unsigned (positive) numbers only. At the beginning, the divisor is subtracted from the most significant part of the dividend. If the result (first remainder) is positive (or zero), the first quotient digit is "1". Otherwise, the quotient digit is "0", but do not restore! Shift divisor one place to the right (or remainder to the left) and add if last quotient digit was "0"; otherwise subtract. Determine quotient digit as before and continue until all quotient digits have been computed. The remainder will be correct if it is non-negative, otherwise correction is needed by a restoring operation (on the remainder only). Extreme care should be taken of the number of bits and the value of the divisor. Assuming the divisor has n bits and the dividend as 2n bits, the above process develops n+1 bits of the quotient. This will not be sufficient if the MSB of the divisor is "0" (which means that the divisor is a small number and more digits are needed in the quotient). Although this condition can be easily detected as overflow will occur in the first subtraction, it can be avoided by aligning the first "1" of the divisor to the MSB of the dividend (by shifting the divisor left until all leading zeros are discarded) before performing the first subtraction. Ample space should be provided for the additional bits of the quotient. Note that leading zeros in the dividend do not disturb the normal operation. The flow chart for unsigned non-restoring division is shown in Figure 22.

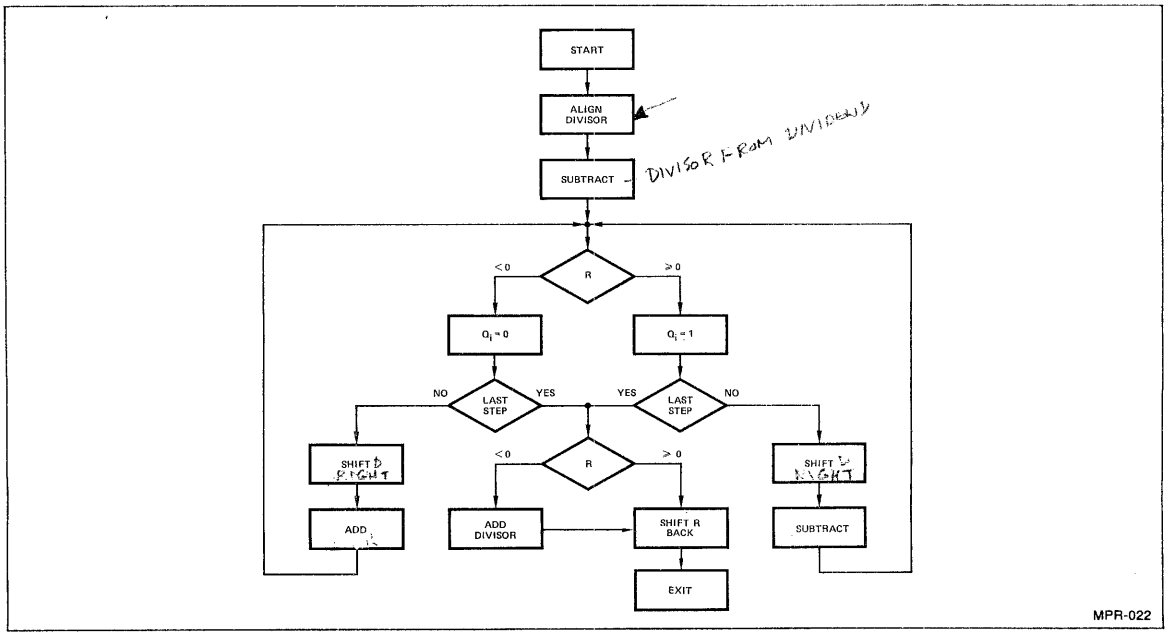


Figure 22. Flowchart for Non-Restoring Division (Unsigned Numbers).

The unsigned division scheme can be applied to signed positive numbers without any change. When negative numbers are encountered, however, changes in the algorithm are necessary. The straightforward method of signed division seems to be "Division in the first quadrant." In that scheme, negative numbers are 2's complemented to obtain positive numbers, remembering the changes done. The division is performed on positive numbers, and finally again 2's complementing occurs wherever necessary. Figure 23 is the flowchart for this algorithm.

Figure 24 is the Interconnection Diagram for both the alignment procedure and the Division Algorithm. It is assumed that the Dividend is in Register R_X (it will be lost during the division and replaced by the Remainder), the Divisor is in Register R_Y. The Quotient will be in the Q register, which should be cleared beforehand.

After checking the signs of the Dividend and Divisor, setting the flags and negating (using 23 or 24 octal as I_5 through I_0 ALU control bits) when necessary, the Divisor should be aligned. This can be done by ORing R_X with 0 (I_{5-0} = 33 octal). The most significant bit is deposited in the Status Register, and can be shifted out by setting $I_8 = I_6$ = HIGH and I_7 to the Exclusive NOR of the previous and present MSB of the Divisor. If these are both "0", I_7 will be HIGH, and an up shift will occur, filling in trailing zeros. When the checked bits are different, I_7 will go LOW, causing a down shift. At the same time the Y output of the Status Register is enabled the leftmost "0" (the sign bit) will be restored.

The first step in the Division routine is a subtract, then shift the R_X and Q registers up. I_{876} will be 6 in octal while I_{210} = 1 in octal and $I_5 = I_4$ = LOW. Pulling the CL bit in the microcode to HIGH, both I_3 and C_n will be HIGH and the ALU is performing a 2's complement subtract. The sign of the Remainder will be latched in the Status Register and the complement of it will be stored in the LSB of the Q register during the shift up operation, which also discards the sign bit of the Remainder.

Now repeating the same operation for all of the other bits of the Remainder with the CL bit in the microcode LOW will leave the control of I_3 to the (complemented) previous sign bit. If it was "0" ($R \geq 0$), I_3 and C_n will be HIGH and the ALU will subtract; if it was 1 ($R < 0$), I_3 and C_n will be LOW and the ALU will ADD, as required. In each up shift, the complement of the present sign bit will be placed at the right of the Quotient, again, as required.

At the end of the division, the sign of the Remainder should be examined and if it is HIGH, the Divisor should be added to it. This can be easily implemented (not depicted on Figure 24) by performing an unconditional ADD (with C_n LOW), letting I_2 LOW, I_0 HIGH and controlling I_1 by the complement of the sign of the Remainder, thus adding to RX either RY (if R_S = 1) or zero (if R_S = 0). If an alignment was performed, the remainder should be shifted down the same number of places.

Finally, the Quotient and/or the Remainder should be 2's complemented again according to the flags.

Figure 25 is a table showing the input states of the Am2901s for each phase of the Alignment and Division.

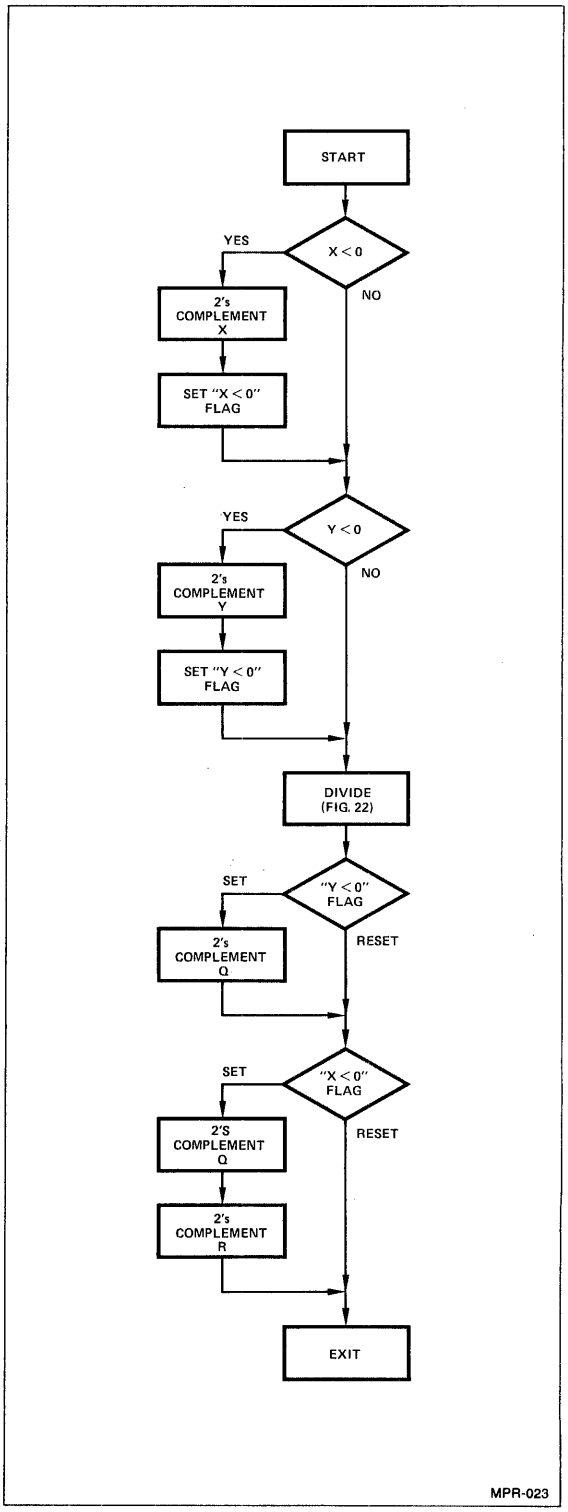


Figure 23. Flowchart for First Quadrant Division with Signed Numbers.

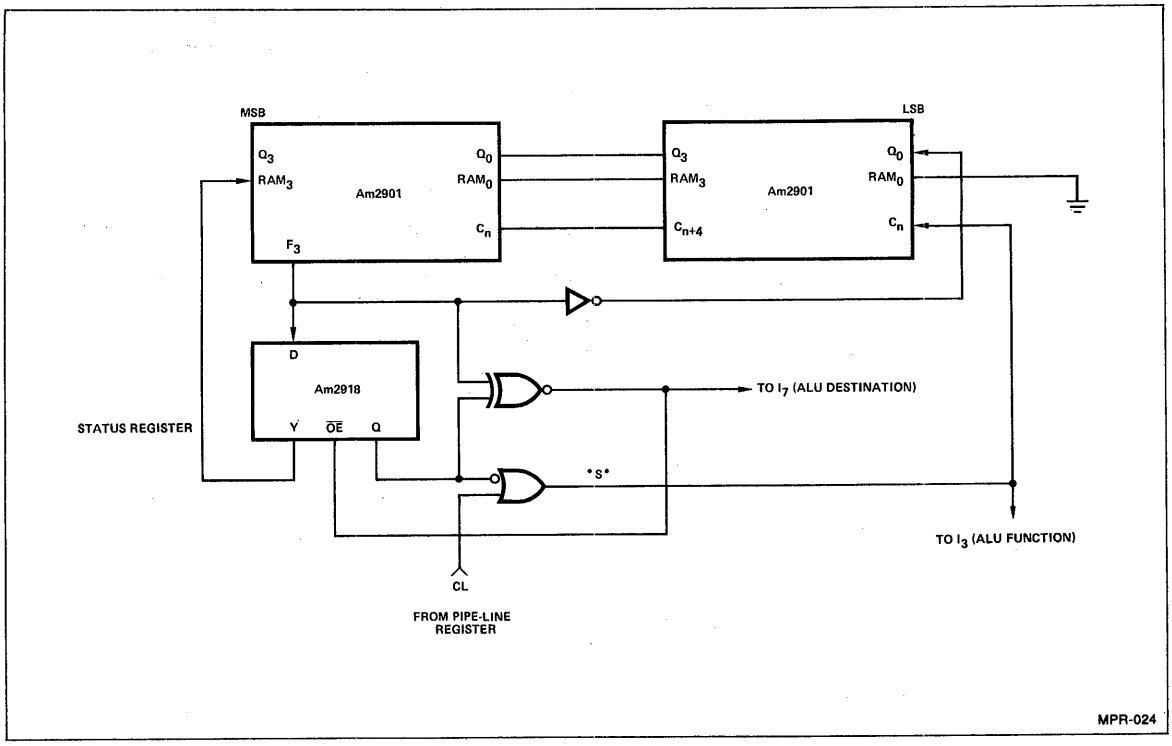


Figure 24. Interconnections for Dedicated Division.

Initial Register Status

R

0	Dividend
1	Divisor
Q	(Cleared)

Am2901 Microcode

Program: 2's Complement Division
Date: 9/24/76 By: M.S.

Final Register Status

R

0	Remainder
1	Divisor
Q	Quotient

S, F	D	Description	CL	Repeat	Pin Status (Octal) A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	Jump to	If
OVB	B	Align Divisor	X	k	X	1	5/7	3	3	X	X	X	0	X or Sign		
(B−A)*2	B	First Subtract & Shift	1	–	1	0	6	1	1	1	$\overline{F_3}$	X	0	X		
(B±A)*2	B	Loop Subtract/Add & Shift	0	k	1	0	6	1/0	1	1/0	$\overline{F_3}$	X	0	X		
B+A or	B	Correct Remainder	X	–	1	0	3	0	1/3	0	X	X	X	X		
B+0	B	Shift Remainder	1	k	X	1	5	1	3	1	X	X	X	Sign		

k = Number of leading zeros of the Divisor

Figure 25. Am2901 Microcode for Dedicated Division.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

Byte Swap of R_0

$A = B = 0$ $I = 701$ $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times.

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the Am2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

$A = B = 15$, $I = 203$, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the instruction register. The fetch operation requires only two microcycles.

ADDITIONAL READING

For more detailed information on applications of the Am2901, the following application notes are available from AMD.

Title	Publication Number
A 16-Bit Microprogrammed Computer	AM-PUB030
An Emulation of the Am9080A	AM-PUB064
A High Performance Disc Controller	AM-PUB065
Build a Microcomputer	
Chapter III	AM-PUB073-3
Chapter IV	AM-PUB073-4

Am2901C

Four-Bit Bipolar Microprocessor Slice

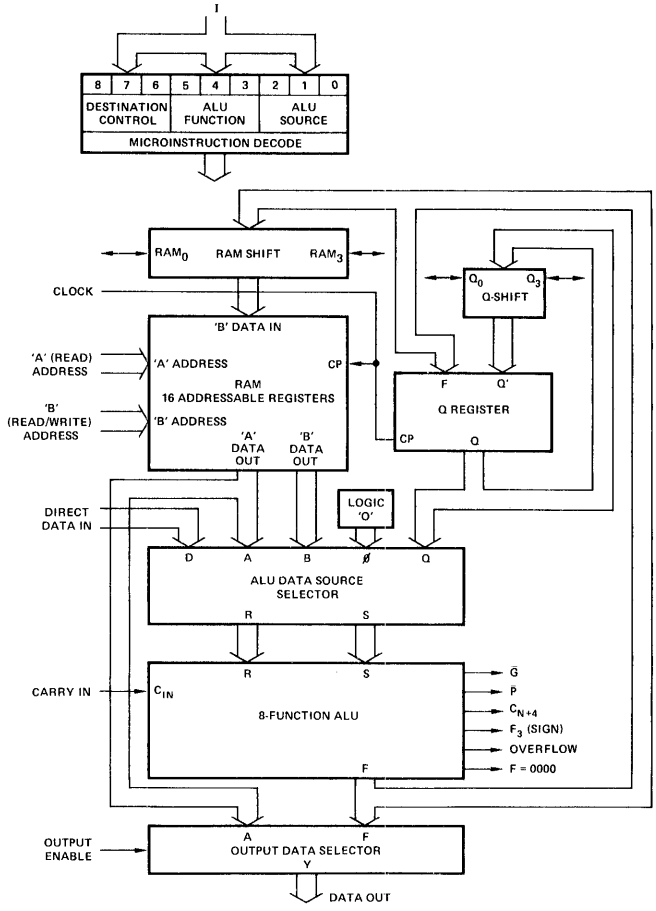
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Third generation of Am2901 four-bit slice**
  Internal ECL circuitry and state-of-the-art process technology combined to provide fastest version of popular Am2901.
- **Plug-in replacement for Am2901, Am2901A, Am2901B**
  The Am2901C is a pin-for-pin replacement for earlier versions of the device. Only the switching speeds are changed.
- **Improved speed**
  25-30% speed improvement on the critical paths versus the Am2901B

2

MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-044

Am2902A

High-Speed Look-Ahead Carry Generator

DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries across a group of four Am2901 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 4.5 ns
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

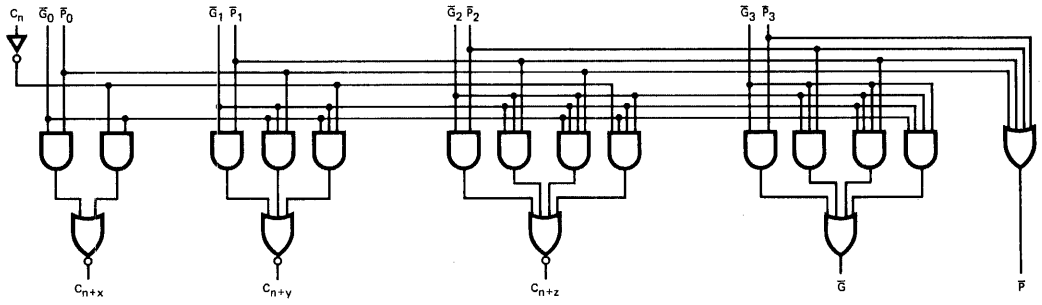
The Am2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902A is generally used with the Am2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

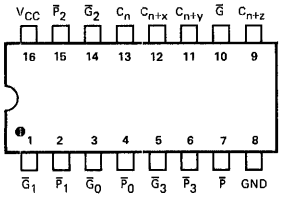
$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC DIAGRAM



MPR-026

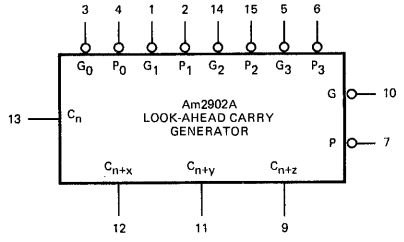
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-027

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-025

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902AXC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2902AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	C_n			−2	mA
			$\overline{P}_3$			−4	
			$\overline{P}_2$			−6	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8	
			$\overline{G}_0, \overline{G}_2$			−14	
			$\overline{G}_1$			−16	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n			50	µA
			$\overline{P}_3$			100	
			$\overline{P}_2$			150	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			350	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 3)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		69	99	mA
			COM'L		69	109	
		V_{CC} = MAX. All Ouputs HIGH	MIL		35		mA
			COM'L		35		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		6.5	10	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		4.5	7	ns	
t_{PHL}			4.5	7		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		5	7.5	ns	
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		4.5	6.5	ns	
t_{PHL}			6.5	10		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Max.	T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		13		15	ns	C_L = 50pF, R_L = 280Ω
t_{PHL}			14		16.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		8		9.5	ns	
t_{PHL}			9		11.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		12		16.5	ns	
t_{PHL}			12		13.5	ns	
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		9.5		11.5	ns	
t_{PHL}			11		12	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901A microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

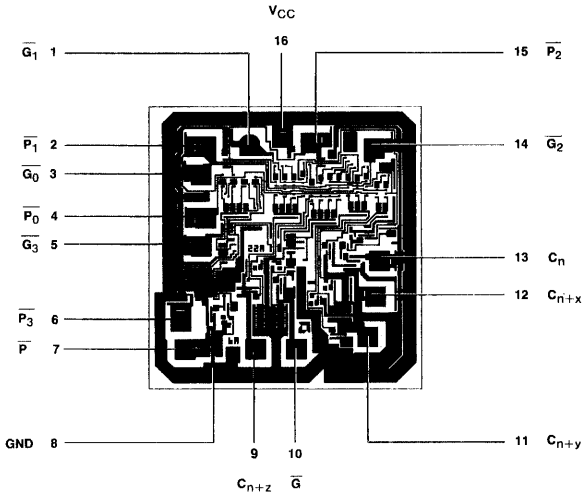
G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X			X	X	X	X	H	H				H	
X			X	X	H	H	H	X				H	
X			H	H	H	X	H	X				H	
H			H	X	H	X	H	X				H	
X			X	X	X	X	L	X				L	
X			X	X	L	X	X	L				L	
X			L	X	X	L	X	L				L	
L			X	L	X	L	X	L				L	
	H			X		X		X					H
	X			H		X		X					H
	X			X		H		X					H
	X			X		X		H					H
	L			L		L		L					L

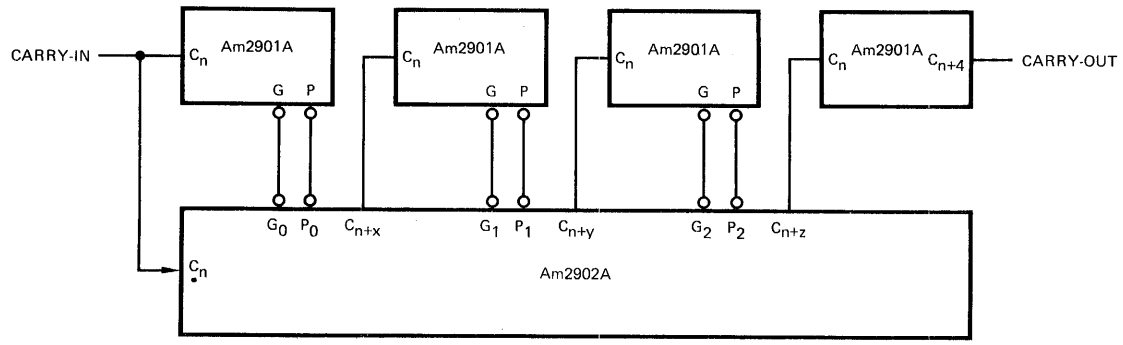
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Metallization and Pad Layout



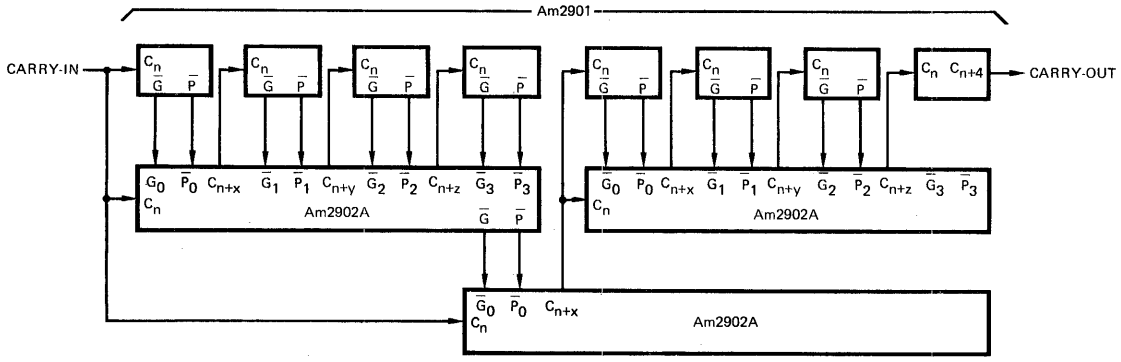
DIE SIZE 0.062" X 0.067"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.

MPR-028



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

MPR-029

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2902APC	P-16	C	C-1
AM2902ADC	D-16	C	C-1
AM2902ADC-B	D-16	C	B-1
AM2902ADM	D-16	M	C-3
AM2902ADM-B	D-16	M	B-3
AM2902AFM	F-16	M	C-3
AM2902AFM-B	F-16	M	B-3
Am2902AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2902AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

If You Liked Our 2901, You'll Love Our 2903!

Same Powerful Architecture:

- 16 Working Registers in 2-address architecture
- Left-Right shift of Data after ALU
- Auxiliary Register for multiple-length operations
- Expandable to any word length in multiples of four bits
- Carry, Overflow, Zero, and Negative Status Flags

Plus These Added Features:

- Two's Complement and Unsigned Multiply
  The Am2903 performs both signed and unsigned multiplication without requiring any additional hardware. For unsigned n x n-bit multiply, a single microinstruction is repeated n times. For a two's complement multiply, a single microinstruction is executed n-1 times, and a second microinstruction is executed once. Both kinds of multiplies produce 2n bit products.
- Two's Complement Divide
  The Am2903 performs a signed division using a non-restoring algorithm. A 2n bit dividend is divided by an n-bit divisor in n cycles (after justification). An n-bit signed quotient and n-bit signed remainder are produced. Extension to multiple length division is simple. No extra hardware is needed.
- Single and Double Length Normalization
  Both single length words and double length words can be normalized; i.e., shifted up to remove leading zeros or ones. During the normalize instructions, the Am2903 provides special flags signaling the completion of normalization.
- Conversion Between Sign-Magnitude and Two's Complement Notations
  On a single cycle, the Am2903 will switch a word from one notation to the other.
- Increment by One or Two
  On a single cycle, the Am2903 can add either 1 or 2 to a word, depending on carry-in.

If You Didn't Like Our 2901, You'll Love Our 2903!

- Two Data Input Ports
  The Am2903 can operate between any two internal registers, any internal register and an external data bus, or two external data buses.
- Expandable Register File
  The Am29705 hooks directly onto the Am2903 to provide *any number* of working registers, without losing the two-address architecture. You can even go to a three-address system, where on one cycle you operate on two registers and place the result in a third.
- Arithmetic *and* Logical Shifts
  Arithmetic shifts hold the MSB (sign bit) in place and shift the rest of the word *around* the MSB. Logical shifts shift all the bits in the word. The 2903 provides both types of shift.
- Sixteen-Function ALU
  Provides 9 Logic Functions and 7 Arithmetic Functions, twice as many functions as the 2901.
- Parity Generated Internally
  A Parity Generator operates on the ALU output and is cascaded between devices, so that a single pin contains parity across the entire ALU output.

And If You Don't Quite Like Our 2903, You'll Definitely Love Our Am29203!

- BCD Arithmetic
  The Am29203 includes special functions for BCD add and subtract, as well as conversion between binary and BCD notations.
- A Byte Better
  The Am29203 is designed to efficiently handle byte operations with a minimum of external logic.
- Both Data Lines Bidirectional
- Decrement by 1 or 2 Instruction
- RAM is enabled only if instruction execution is enabled.

Am2903 • Am29203

The Superslice®

2

DISTINCTIVE CHARACTERISTICS

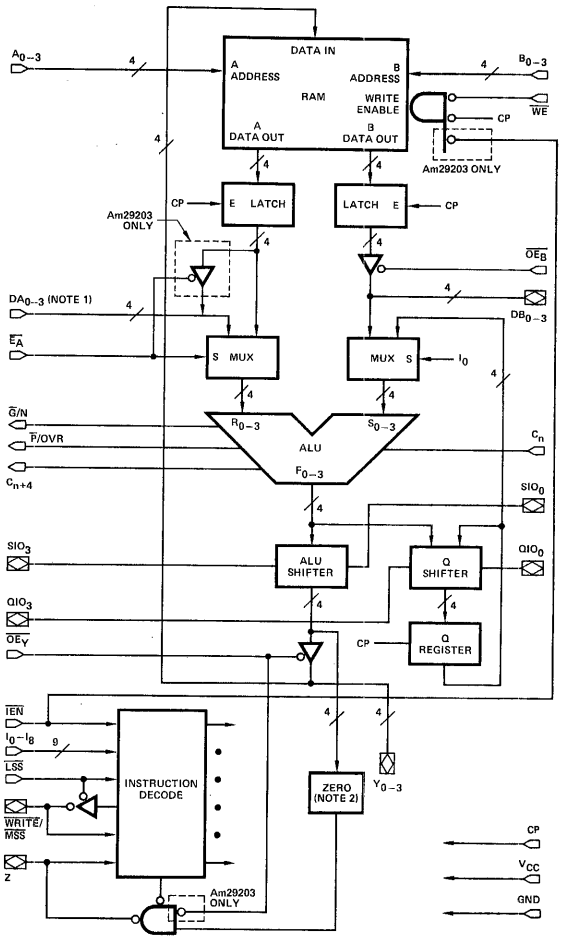
- Expandable Register File –
  Like the Am2901, the Am2903/29203 contains 16 internal working registers arranged in a two-address architecture. But the Am2903/29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- Built-in Multiplication Logic –
  Performing multiplication with the Am2901A requires a few external gates – these gates are contained on-chip in the Am2903/29203. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- Built-in Division Logic –
  The Am2903/29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- Built-in Normalization Logic –
  The Am2903/29203 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- Built-in Parity Generation Circuitry –
  The Am2903/29203 can supply parity across the entire ALU output for use in error detection.
- Built-in Sign Extension Circuitry –
  To facilitate operation on different length two's complement numbers, the Am2903/29203 provides the capability to extend the sign at any slice boundary.
- BCD Arithmetic (Am29203 only) –
  Automatic BCD add and subtract and conversion between binary and BCD.
- Improved Byte Handling (Am29203 only) –
  Zero detection and register writing can be performed on a single byte rather than the whole word.
- Two Bidirectional Data Lines (Am29203 only) –

TABLE OF CONTENTS

GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am29203 is a similar device, but has additional I/O capability, more special instructions and will be at least 30% faster.

BLOCK DIAGRAM



Notes: 1. DA_{0-3} is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the $\overline{OE}_Y$ buffer.

MPR-030

ARCHITECTURE OF THE Am2903 AND Am29203

The Am2903/29203 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPUs, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903/29203 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am2903/29203 is cascadable with full lookahead or ripple carry, has 3-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port. On the Am29203, E_A provides the same feature at the DA port.

External data at the Am2903/29203 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E_A}$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table I shows all possible pairs of ALU source operands as a function of the $\overline{E_A}$, $\overline{OE}_B$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits. The Am29203 ALU is identical, but executes 16 special instructions.

Am2903/29203s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903/29203s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the Am2903/29203 and are available as outputs of the least significant and intermediate slices.

TABLE 1. ALU OPERAND SOURCES

$\overline{E_A}$	I_0	$\overline{OE}_B$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

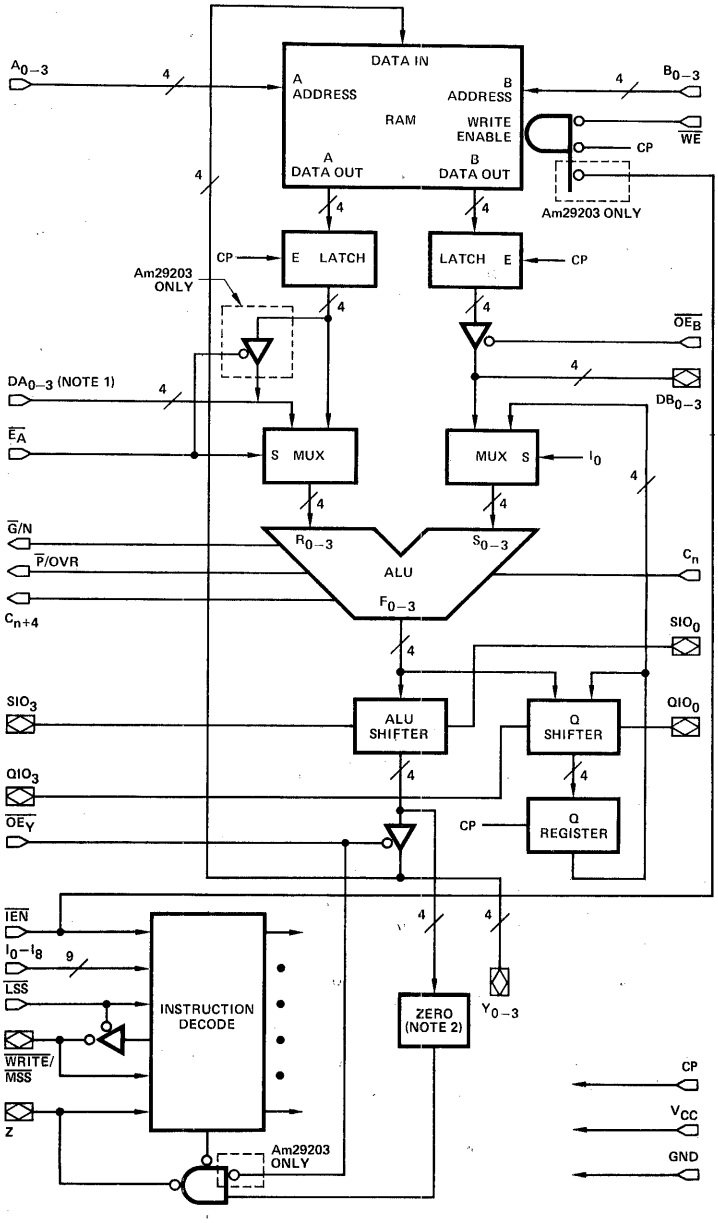
TABLE 2. ALU FUNCTIONS

I_4	I_3	I_2	I_1	I_0	ALU Functions
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	F = S Minus R Minus 1 Plus C_n
L	L	H	L	X	F = R Minus S Minus 1 Plus C_n
L	L	H	H	X	F = R Plus S Plus C_n
L	H	L	L	X	F = S Plus C_n
L	H	L	H	X	F = S Plus C_n
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	F = R Plus C_n
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	F = R Plus C_n
H	L	L	L	L	Reserved Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i = R_i$ AND S_i
H	L	H	L	X	$F_i = R_i$ EXCLUSIVE NOR S_i
H	L	H	H	X	$F_i = R_i$ EXCLUSIVE OR S_i
H	H	L	L	X	$F_i = R_i$ AND S_i
H	H	L	H	X	$F_i = R_i$ NOR S_i
H	H	H	L	X	$F_i = R_i$ NAND S_i
H	H	H	H	X	$F_i = R_i$ OR S_i

L = LOW H = HIGH i = 0 to 3
X = LOW or HIGH

The Am2903/29203 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903/29203 instruction.

BLOCK DIAGRAM



Notes: 1. DA_{0-3} is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the $\overline{OE}_Y$ buffer.

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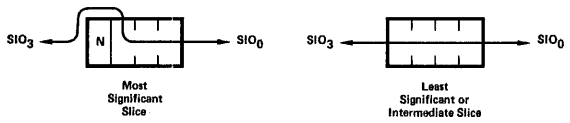
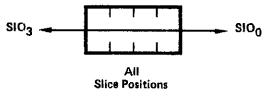
ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.



Am2903/29203 Arithmetic Shift Path



Am2903/29203 Logical Shift Path

Figure A. MPR-031

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am2903/29203 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am2903/29203 applications section for a more detailed description of the Am2903/29203 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903/29203 executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits $I_8I_7I_6I_5$. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am2903/29203. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903/29203 special functions and the operations which the Q Register and shifter perform for each. When the Am2903/29203 executes instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits $I_8I_7I_6I_5$. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. On the Am29203, the DA port is also bidirectional. The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high impedance state when $\overline{OE_Y}$ is HIGH. The DB output buffers are enabled when the $\overline{OE_B}$ input is LOW and the DA buffers are enabled when $\overline{E_A}$ is LOW. (On the Am2903 DA is input only; the pins are never outputs.)

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903 and Am29203 instructions. On the Am29203, the Z pin will be HIGH if $\overline{OE_Y}$ is HIGH, allowing zero detection on less than the full word.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 OR I_4 = HIGH, $\overline{IEN}$ = LOW.

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$
$\forall$ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS: $I_0 = I_1 = I_2 = I_3 = I_4$ = LOW, $\overline{IEN}$ = LOW

I_8	I_7	I_6	I_5	Hex Code	Available On	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig. Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
L	L	L	L	0	Am2903 Am29203	Unsigned Multiply	F= S+C_n if Z=L F=R+S+C_n if Z=H	Log. F/2→Y (Note 1)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	L	L	H	1	Am29203										
L	L	H	L	2	Am2903 Am29203	Two's Complement Multiply	F=S+C_n if Z=L F=R+S+C_n if Z=H	Log. F/2→Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	L	H	H	3	Am29203										
L	H	L	L	4	Am2903 Am29203	Increment by One or Two	F=S+1+C_n	F→Y	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	L	H	5	Am2903 Am29203	Sign/Magnitude-Two's Complement	F=S+C_n if Z=L F=$\overline{S}$+C_n if Z=H	F→Y (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	H	L	6	Am2903 Am29203	Two's Complement Multiply, Last Cycle	F=S+C_n if Z=L F=S−R−1+C_n if Z=H	Log. F/2→Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	H	H	H	7	Am29203										
H	L	L	L	8	Am2903 Am29203	Single Length Normalize	F=S+C_n	F→Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L
H	L	L	H	9	Am29203										
H	L	H	L	A	Am2903 Am29203	Double Length Normalize and First Divide Op.	F=S+C_n	Log 2F→Y	$R_3 \forall F_3$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	L	H	H	B	Am29203										
H	H	L	L	C	Am2903 Am29203	Two's Complement Divide	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	Log. 2F→Y	$R_3 \forall F_3$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	L	H	D	Am29203										
H	H	H	L	E	Am2903 Am29203	Two's Complement Divide, Correction and Remainder	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	F→Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	
H	H	H	H	F	Am29203										

NOTES: 1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated at the Y_3 output.

L = LOW
H = HIGH
X = Don't Care

Hi-Z = High Impedance
$\forall$ = Exclusive OR
Parity = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

Instruction Decoder

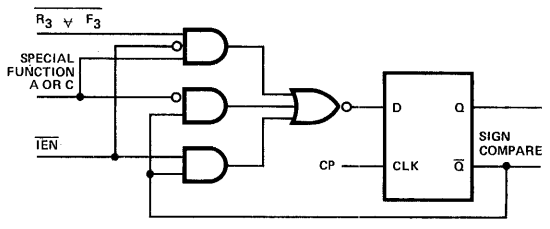
The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am2903 instruction inputs.

On the Am2903, when $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903 divide operation (see Figure B). On the Am29203, $\overline{IEN}$ controls internal writing, but does not affect $\overline{WRITE}$. The $\overline{IEN}$ signal can then be controlled separately at each chip to facilitate byte operations.

Programming the Am2903/29203 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}/\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{W}/\overline{MSS}$ pin must be tied HIGH through a resistor. $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ should not be connected together. See Figure 2 of applications.



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Figure B. Sign Compare Flip-Flop.

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TABLE 5. Am2903/29203 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Gi (i=0 to 3)	Pi (i=0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OE}_Y$ = LOW)		
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Intermediate Slice	Least Sig Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
2	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
4	0	L	See Note 1	See Note 2	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	$\overline{S}_i$ if Z=L S_i if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \forall S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z=L $\overline{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
8	0	L	0	S_i	See Note 3	$Q_2 \forall Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	0	S_i	See Note 4	$F_2 \forall F_1$	$\overline{P}$	F_3	$\overline{G}$	See Note 5	See Note 5	See Note 5
C	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
E	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input

L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
$\forall$ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_pP_1P_2$

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$
   If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$
   If $\overline{LSS}$ is HIGH, $P_i = S_i$
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$
   At other slices, $C_{n+4} = G \vee PC_n$
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$
   At other slices, $C_{n+4} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Am2903 SPECIAL FUNCTIONS

The Am2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903 applications section for a more detailed description of these Special Functions.

PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the Am2903 ALU operand sources; DA_0 is the least significant bit. On the Am29203, the DA path is bidirectional, operating as either an ALU source operand or as an external output for the RAM A-port.

$\overline{EA}$ A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am2903/29203 ALU.

I_{0-8} The nine instruction inputs used to select the Am2903/29203 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am2903, $\overline{IEN}$ also controls $\overline{WRITE}$. On the Am29203, $\overline{WRITE}$ is not affected by $\overline{IEN}$, but internally disables the RAM write enable.

C_{n+4} This output generally indicates the carry-out of the Am2903/29203 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903/29203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

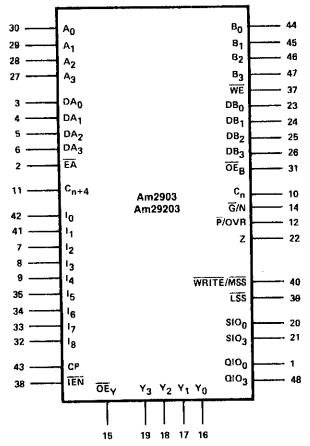
$\overline{WRITE}/\overline{MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the Am2903/29203. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.

CP The clock input to the Am2903/29203. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

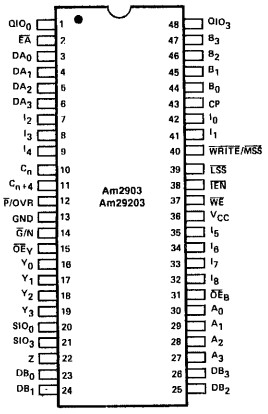
LOGIC SYMBOL



V_{CC} = Pin 36
GND = Pin 13

MPR-033

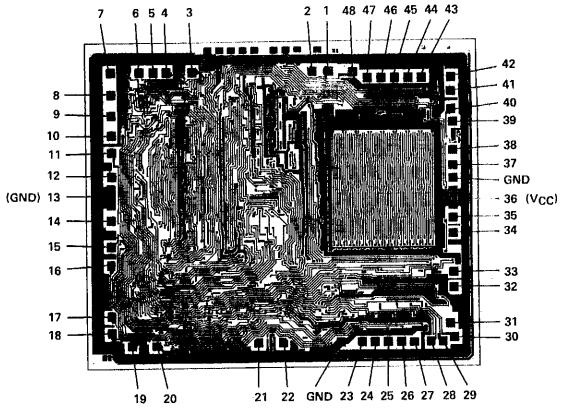
CONNECTION DIAGRAM
Top View



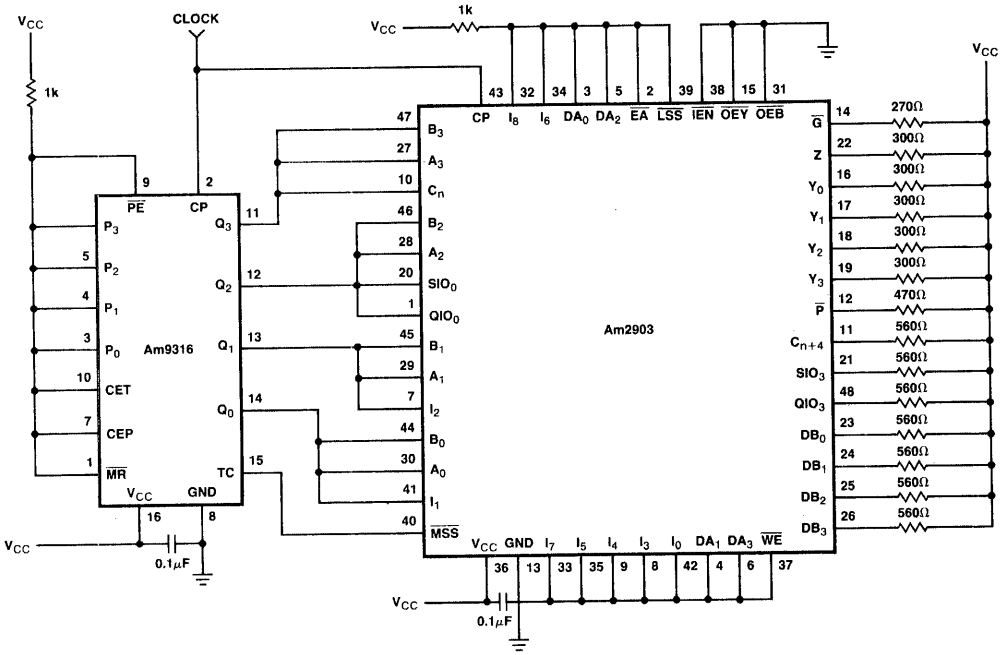
Note: Pin 1 is marked for orientation.

MPR-034

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163" X 0.197"
Note: Pin numbers correspond to DIP package.



MPR-582

V_{CC} = 5.0V
Frequency = 100kHz
T_A = +125°C
All registers are 1/4 watt ±5%
This circuit conforms to MIL-STD-883, Methods 1005 and 1015, Condition D.
One Am9316 Can Drive Maximum of Five Am2903s.

Am2903 Burn-in and Life Test Circuit

Am2903 • Am29203
OPERATING RANGES (over which DC, switching, and functional specifications apply)

Range	Part Number Suffix	Temperature	V_{CC}	V_{IH}	V_{IL}
COM'L	PC, PCB, DC, DCB, XC	T_A = 0 to 70°C	4.75 to 5.25V	2.0V	0.8V
MIL	DM, DMB, FM, FMB, XM	T_C = −55 to +125°C	4.50 to 5.50V	2.0V	0.3V

2

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am29203 Order Number	Am2903 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29203DC	AM2903DC	D-48	C	C-1
AM29203DC-B	AM2903DC-B	D-48	C	B-2 (Note 4)
AM29203DM	AM2903DM	D-48	M	C-3
AM29203DMB	AM2903DM-B	D-48	M	B-3
AM29203FM	AM2903FM	F-48	M	C-3
AM29203FMB	AM2903FM-B	F-48	M	B-3
Am29203XC	Am2903XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am29203XM	Am2903XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N		2.4			Volts
			I_{OH} = −800μA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}		2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} = or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V (Note 4)	C_n				−3.6	mA
			Y_0, Y_1, Y_2, Y_3				−1.13	
			I_0, I_1, I_2, I_3, I_4 DA_0, DA_1, DA_2, DA_3				−0.72	
			SIO_0, SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1, DB_2, DB_3				−0.77	
			All other inputs				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Note 4)	C_n				200	μA
			Y_0, Y_1, Y_2, Y_3				110	
			I_0-I_4, DA_0-DA_3				40	
			SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$				90	
			All other inputs				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX., (Note 4)	Y_0-Y_3	V_O = 2.4V			110	μA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_0, SIO_0, SIO_3, $\overline{MSS}$/IS	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Am2903 SWITCHING CHARACTERISTICS

Am2903 switching characteristics are dependent on temperature, voltage, and the operating mode of the device. The detailed data for the part is given in the 24 tables comprising Appendix A of this data sheet. For reference, one set of these tables is reproduced on this page and the next. For switching data for special functions and military devices, refer to Appendix A.

TABLE III A
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	86	81	69	110	86	108	–	–	–	84	94	115
B Address	99	88	81	123	99	112	49	–	–	94	104	140
A Address (Logic Mode)	87	–	68	111	89	–	–	–	–	79	94	115
B Address	84	–	73	108	84	–	49	–	–	84	90	120
DA Inputs (Arith. Mode)	63	60	49	87	64	89	–	–	–	60	70	101
DB Inputs	61	59	47	85	62	84	–	–	–	62	68	98
DA Inputs (Logic Mode)	64	–	48	88	66	–	–	–	–	61	72	101
DB Inputs	55	–	32	79	57	–	–	–	–	52	61	93
$\overline{EA}$	59	53	42	83	59	83	–	–	–	57	64	98
C_n	40	30	–	64	40	58	–	–	–	38	46	67
I_0	52	48	36	76	52	63	–	49	*	50*	58*	93*
I_{4321}	71	65	72	95	69	84	–	49	*	66*	73*	105*
I_{8765}	42	–	–	66	–	–	–	50	60*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	26	–	–	50	–	–	–	–	–	–	29	36
Clock	87	87	71	111	88	108	37	–	40	84	92	105
Y	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE III B
Guaranteed Set-up and Hold Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

To Output / From Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	20	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A, B as Sources	Clock	27	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	21	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	68	0	See Note 6

Notes:
1. For set-up times from all inputs not specified in Table B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

TABLE III C
Guaranteed Enable/Disable Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE III D
Guaranteed Clock and Write Pulse Characteristics
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE both LOW to Write	30	ns

CYCLE TIMES FOR 16-BIT SYSTEM FOR COMMON OPERATIONS

The illustration below shows a typical configuration using 4 Am2903 Superslices, an Am2902A carry lookahead chip, and the Am2904 for shift multiplexers, status registers, and carry-in control. For the system enclosed within the dashed lines, there are four major switching paths whose values for various kinds of cycles are summarized below, and shown on the timing waveform.

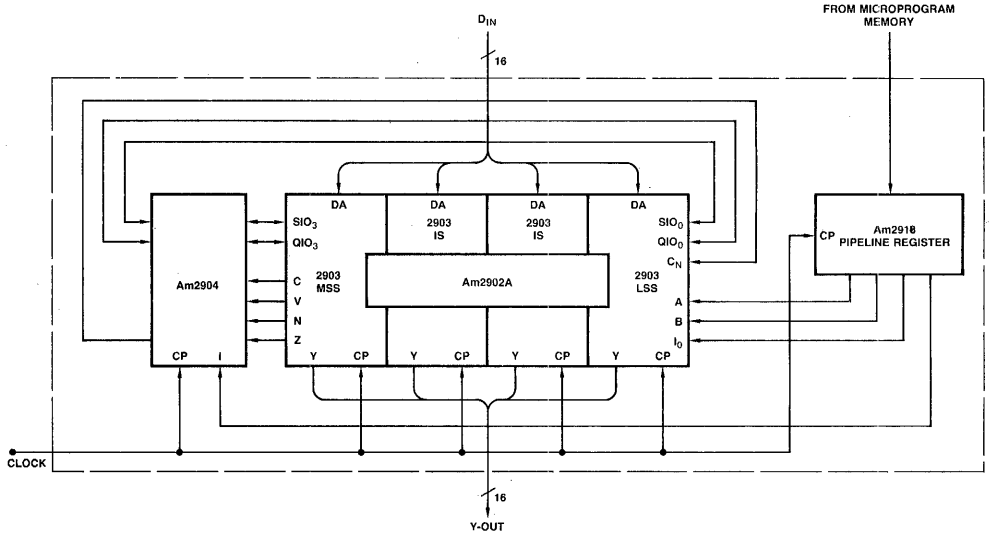
1. MICROCYCLE TIME (TCHCH).
   The minimum time which must elapse between a LOW-TO-HIGH clock transition and the next LOW-TO-HIGH clock transition.
2. DATA SET-UP TIME (TDVCH).
   The minimum time which must be allowed between valid, stable data on the D inputs and the clock LOW-TO-HIGH transition.
3. D TO Y (TDVYV).
   The maximum time required to obtain valid Y output data after the D inputs are valid. This is the combinational delay through the parts from D to Y.
4. CP TO Y (TCHYV).
   The maximum time required to obtain valid Y outputs after a clock LOW-TO-HIGH transition.

The types of cycles for which data is summarized are as follows:

1. Logic – Any logical operation without a shift.
2. Logic Rotate – Any logic operation with a rotate or shift.
3. Arithmetic – An add or subtract with no shift.
4. Multiply – The first cycle of a 2's complement multiply instruction. Subsequent cycles require less time.
5. Divide – The iterative divide cycle. The first divide instruction and the last divide (correction) instruction require less time.

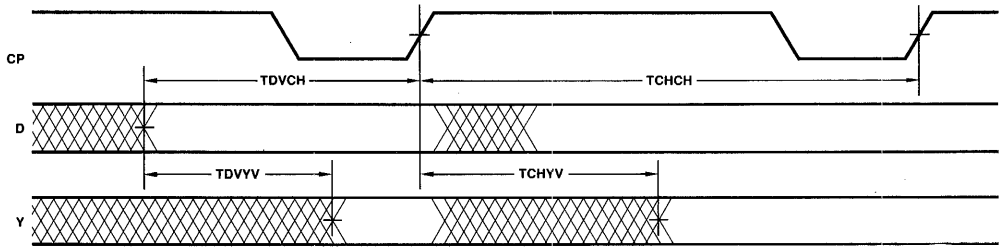
Time in ns Over Commercial Operating Range

CYCLE	TCHCH	TDVCH	TDVYV	TCHYV
LOGIC	143	105	64	102
LOGIC ROTATE	180	143	123	160
ARITHMETIC	184	137	96	143
MULTIPLY	200	140	120	180
DIVIDE	228	167	128	189



16-Bit System with Am2903, Am2902A, Am2904

MPR-583



Timing Waveforms for Data In, Clock, and Y Out

MPR-584

USING THE Am2903 AND Am29203

Except Where Otherwise Noted, All References to the Am2903 Also Apply to the Am29203.

Am2903 APPLICATIONS

The Am2903 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am2903 normally will all come from registers clocked at the same time as the Am2903. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the Am2903's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

One Level Pipeline Based System

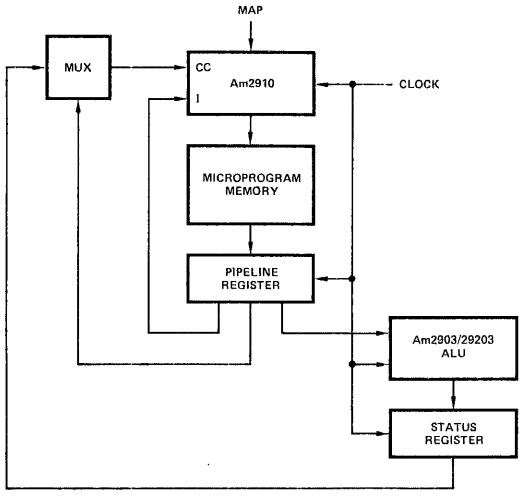


Figure 1. Typical Microprogram Architecture.

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Note that with the microprogram register in between the microprogram memory store and the Am2903's, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2903's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

Expansion of the Am2903

The Am2903 is a four-bit CPU slice. Any number of Am2903's can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am2903's to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all Am2903's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied HIGH. Caution: $\overline{W}/\overline{MSS}$ must be tied to V_{CC} through a resistor; $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ may not be shorted directly together. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE}/\overline{MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x}, C_{n+y}, and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}$/N and $\overline{P}$/OVR pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

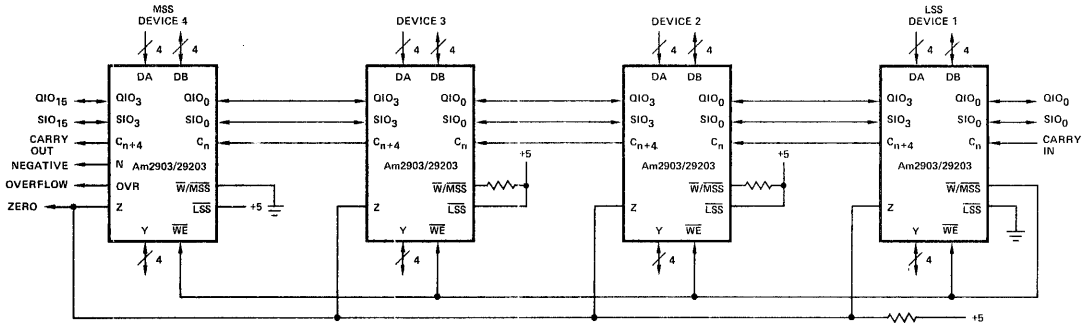


Figure 2. 16-Bit CPU with Ripple Carry.

MPR-036

The $\overline{IEN}$ pin of the Am2903 allows the option of conditional instruction execution. If $\overline{IEN}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the Am2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B→B while the three-address mode makes possibleA+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \forall F_{14} \forall F_{13} \forall \ldots \forall F_1 \forall F_0 \forall SIO_{15}$.

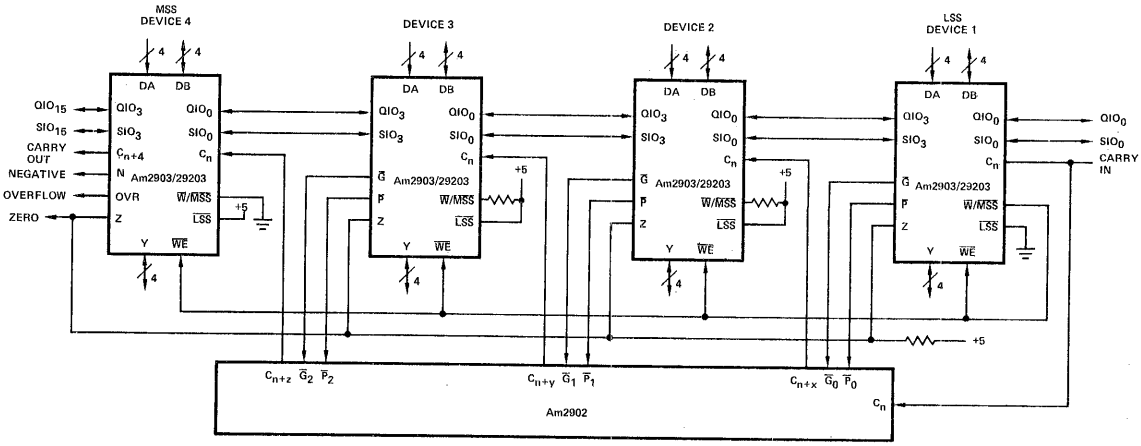


Figure 3. 16-Bit CPU with Carry Look Ahead.

MPR-037

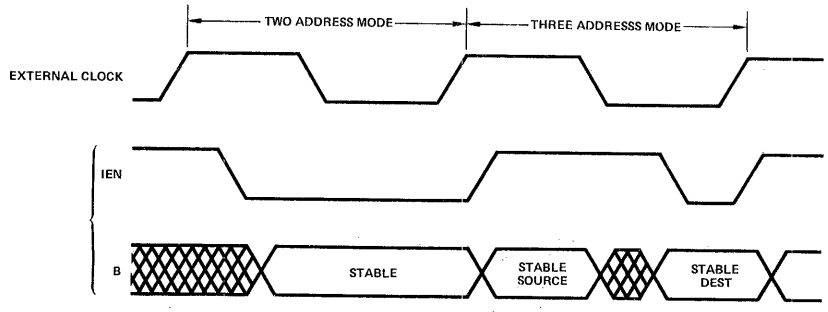


Figure 4. Relationship of $\overline{IEN}$ and Clock During Two Address and Three Address Modes.

MPR-038

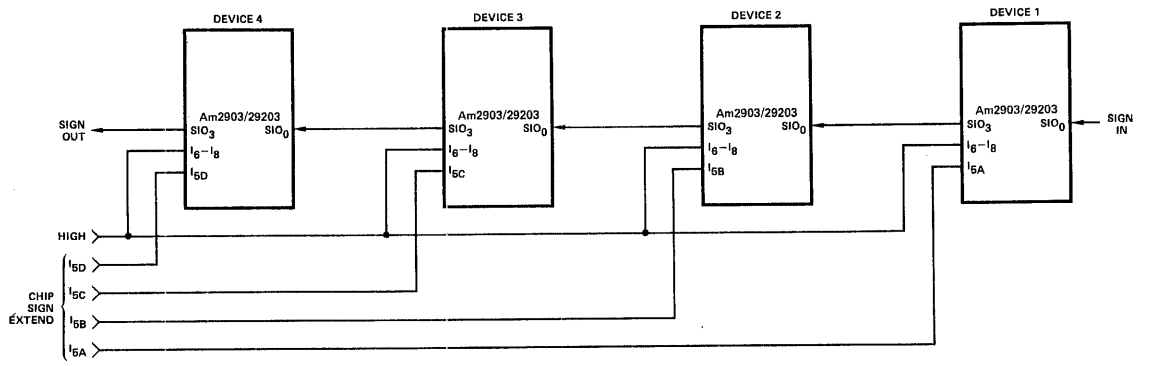


Figure 5. Sign Extend. MPR-039

Sign Extend

Sign extension across any number of Am2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am2903 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by I_{5A-D}. If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

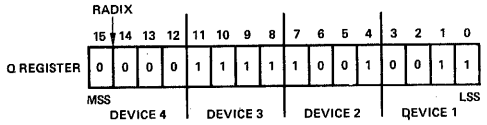
SPECIAL FUNCTIONS

When $I_{0-4} = 0$, the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8}. The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am2903.

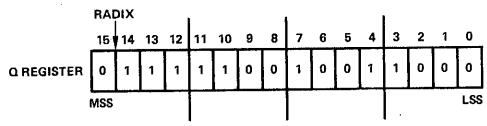
Normalization, Single- and Double-Length

Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice (C_{n+4} MSS = Q_3 MSS $\forall$ Q_2 MSS).



a) Unnormalized Positive Number.



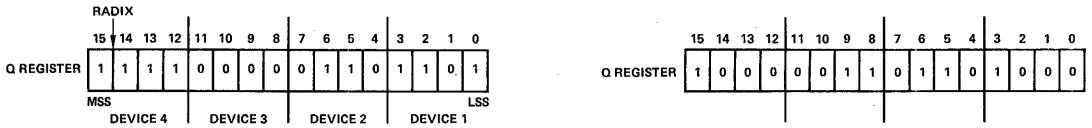
b) Normalized Positive Number.

Figure 6. MPR-040

There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin (OVR = Q_2 MSS $\forall$ Q_1 MSS). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am2903 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, Q_3 MSS. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function $[B] + C_n$ and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4}, OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4}, OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant



a) Unnormalized Negative Single Length Number.

b) Normalized Negative Single Length Number.

Figure 7.

MPR-041

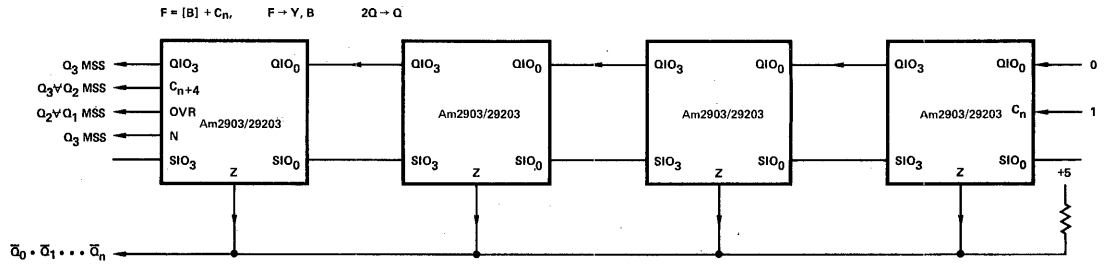


Figure 8. Single Length Normalize.

MPR-042

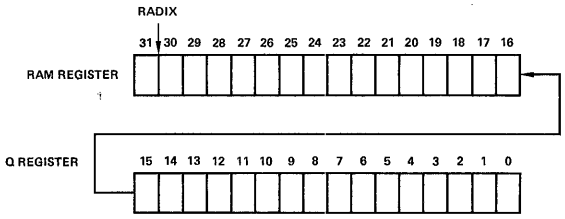


Figure 9. Double Length Word.

MPR-043

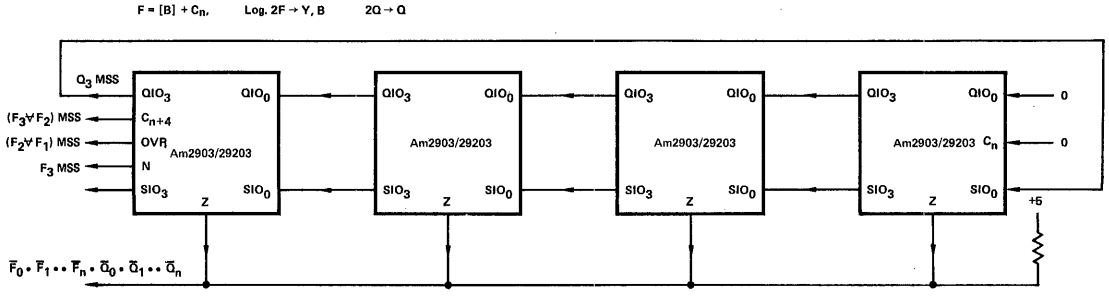


Figure 10. Double Length Normalize.

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slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

Sign Magnitude, Two's Complement Conversion

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., 100 . . . 00 (-2^n)], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation (100 . . . 0) is converted to two's complement notation, the correct result is obtained (0 . . .0).

Increment by One or Two

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

Unsigned Multiply

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1; and 3) the multiplier be in R_2. The first operation transfers the multiplier, R_2, to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

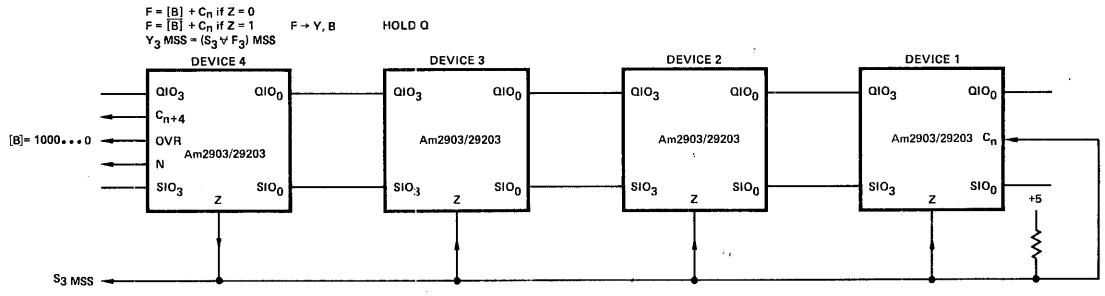


Figure 11. 2's Complement←→Sign/Magnitude.

MPR-045

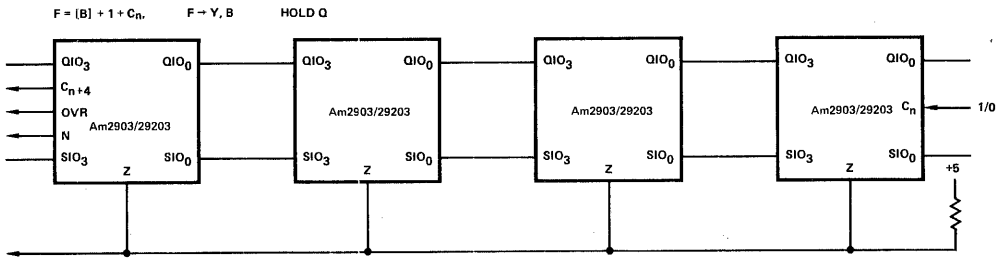


Figure 12. Increment by 2/1.

MPR-046

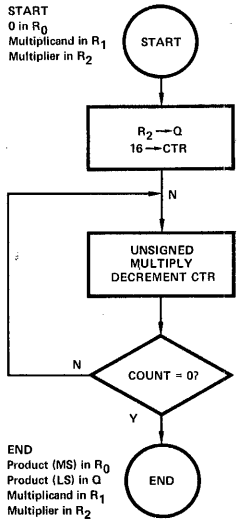


Figure 13. Unsigned 16 X 16 Multiply Flowchart.

tiplicand (referenced by the A address port) if Z = 1. If Z = 0, the output of the ALU is simply the partial product (referenced by the B address port). Since C_n is held LOW, it is not a factor in the computation. Each positive-going edge of the clock will internally shift the ALU outputs toward the least significant bit and simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y_3 position of device 4. At this time, one bit of the multiplier will down shift out of the QIO_0 ports of each device into the QIO_3 port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO_0 and SIO_3 ports, with SIO_0 of device 1 being connected to QIO_3 of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

Two's Complement Multiplication

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term N∀OVR generated in device 4 is internally shifted into the Y_3 position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. The interconnection for this instruction is shown in Figure 18. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

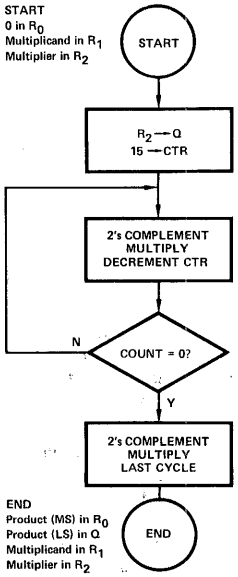
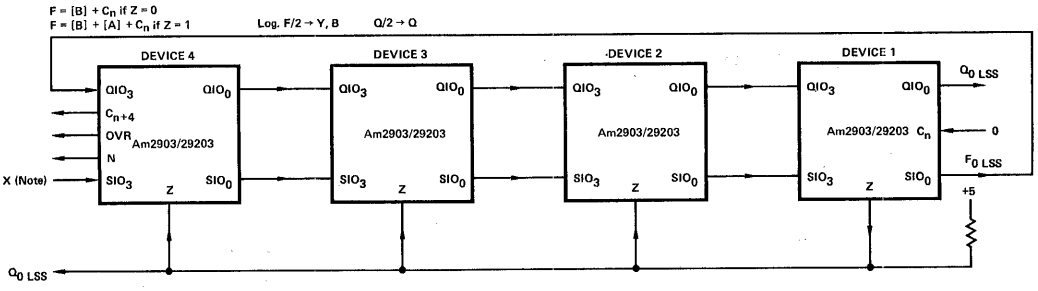


Figure 14. 2's Complement 16 X 16 Multiply.



Note: For unsigned multiply, C_{n+4} MSS is internally shifted into position Y_3 MSS; 2's complement multiply N∀OVR is internally shifted into position Y_3 MSS.

Figure 15. Multiply.

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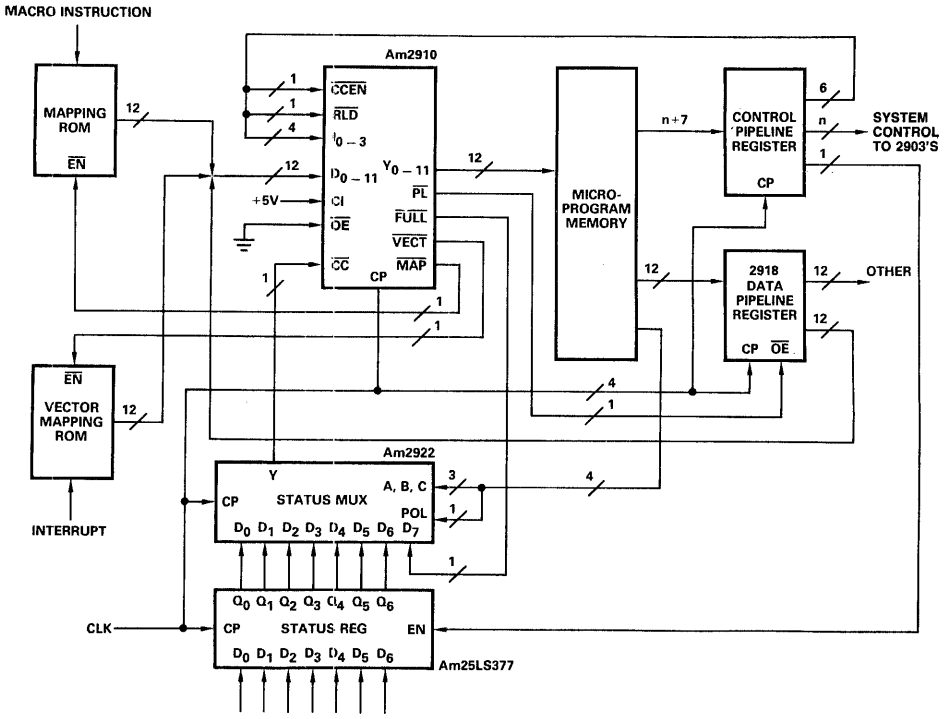

Figure 16. Typical Computer Control Unit (CCU).

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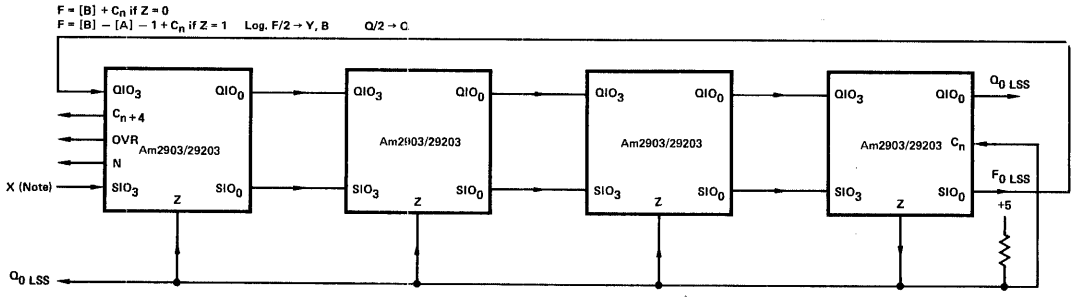
Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00F_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	0	0	0	R_1	R_0	0	Unsigned Multiply

Figure 17. Micro Code for Unsigned 16 X 16 Multiply.



Note: N ∀ OVR is internally shifted into position Y_3 MSS.

Figure 18. 2's Complement Multiply, Last Cycle.

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Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	$I_4 - I_1$	$I_8 - I_5$	$\overline{OEB}$	$\overline{OEY}$	$A_3 - A_0$	$B_3 - B_0$	C_n	Comment
n	LDCT	$00E_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	2	0	0	R_1	R_0	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R_1	R_0	Z	2's Complement Multiply (Last Cycle)

Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

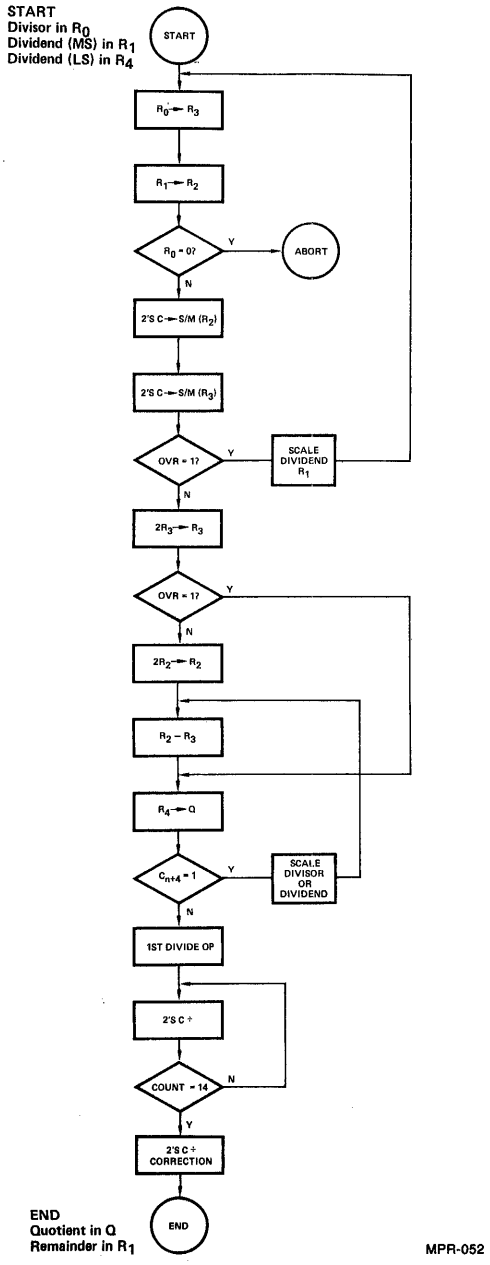

Figure 20. Division Flow Chart – Double Precision Divide.

TWO'S COMPLEMENT DIVISION

The division process is accomplished using a four quadrant non-restoring algorithm which yields an algebraically correct answer such that the divisor times the quotient plus the remainder equals the dividend. The algorithm works for both single precision and multi-precision divide operations. The only condition that needs to be met is that the absolute magnitude of the divisor be greater than the absolute magnitude of the dividend. For multi-precision divide operations the least significant bit of the dividend is truncated. This is necessary if the answer is to be algebraically correct. Bias correction is automatically provided by forcing the least significant bit of the quotient to a one, yet an algebraically correct answer is still maintained. Once the algorithm is completed, the answer may be modified to meet the user's format requirements, such as rounding off or converting the remainder so that its sign is the same as the dividend. These format modifications are accomplished using the standard Am2903 instructions.

The true value of the remainder is equal to the value stored in the working register times 2^{n-1} when n is the number of quotient digits.

The following paragraphs describe a double precision divide operation. The double precision flow chart is based upon the use of the architecture detailed in Figure 16.

Referring to the flow chart outlined in Figure 20, we begin the algorithm with the assumption that the divisor is contained in R_0, while the most significant and least significant halves of the dividend reside in R_1 and R_4 respectively. The first step is to duplicate the divisor by copying the contents of R_0 into R_3. Next the most significant half of the dividend is copied by transferring the contents of R_1 into R_2 while simultaneously checking to ascertain if the divisor (R_0) is zero. If the divisor is zero then division is aborted. If the divisor is not zero, the copy of the most significant half of the dividend in R_2 is converted from its two's complement to its sign magnitude representation. The divisor in R_3 is converted in like manner in the next step, while testing to see if the results of the dividend conversion yielded an indication on the overflow pin of the Am2903. If the output of the overflow pin is a 'one' then the dividend is -2^n and hence is the largest possible number, meaning that it cannot be less than the divisor. What must be done in this case is to scale the dividend by down shifting the upper and lower halves stored in R_1 and R_4 respectively. After scaling, the routine requires that the algorithm be reinitiated at the beginning.

Conversely, if the output of the overflow pin is not a one, the sign magnitude representation of the divisor (R_3) is shifted up in the Am2903, removing the sign while at the same time testing the results of two's complement to sign magnitude conversion of the divisor in the Am2910. If the results of the test indicate that the divisor is -2^n i.e., overflow equals one, then the lower half of the dividend is placed in the Q register

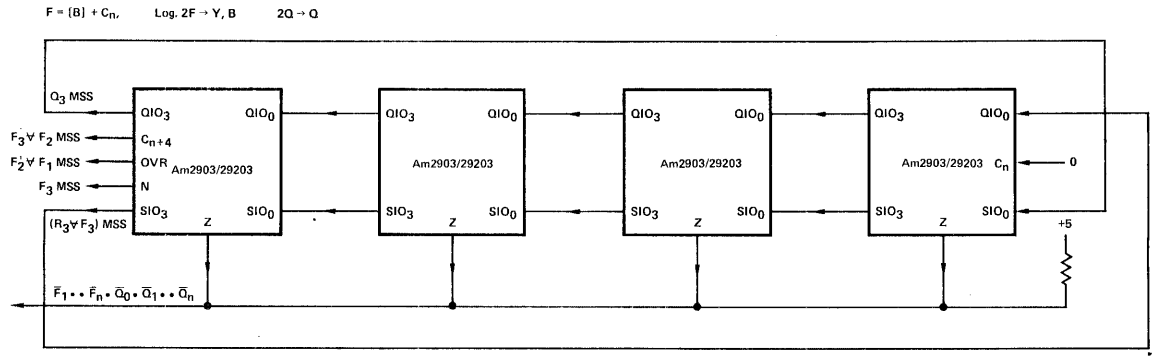

Figure 21. Double Length Normalize/First Divide Operation.

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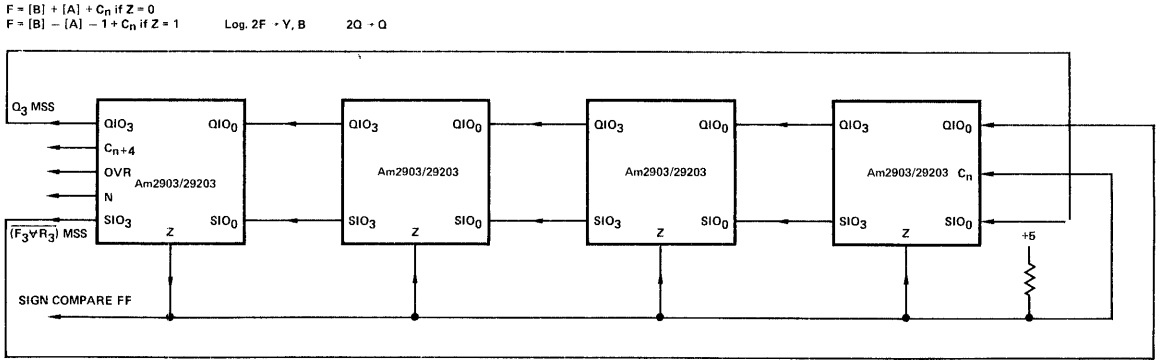

Figure 22. 2's Complement Divide.

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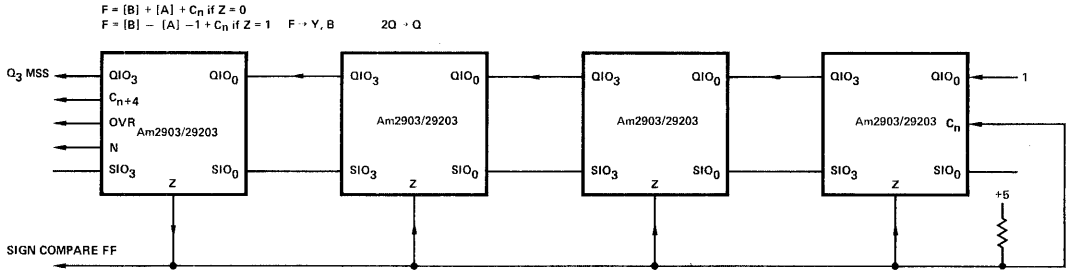

Figure 23. 2's Complement Divide Correction.

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and division may proceed. This is possible because the divisor is now guaranteed to be greater than the dividend. If overflow is not a one then we must proceed by shifting out the sign of the sign magnitude representation of the dividend stored in R_2. At this point we are able to check if the divisor is greater than the dividend by subtracting the absolute value of the divisor (R_3) from the absolute value of the upper half of the dividend (R_2) and storing the results in R_3. Next, the least significant half of the dividend is transferred from R_4 to the Q register while simultaneously testing the carry from the result of the divisor/dividend subtraction. If the carry (C_{n+4}) is one, indicating the divisor is not greater than the dividend then a scaling operation must occur. This involves either shifting up the divisor or shifting down the dividend. If the carry is not one then the divisor is greater than the dividend and division may now begin.

Micro Memory Address	Am2910 Inst.	Data Pipeline Reg.	Am2903/29203 I_0	I_4-I_1	I_8-I_5	$\overline{EA}$	A_3-A_0	B_3-B_0	C_n	Am2922 SEL	POL	Comments
n	CONT	X	0	6	4	0	R_0	R_3	0	X	X	$R_0 \rightarrow R_3$
n+1	CJP	Abort	0	6	4	0	R_1	R_2	0	Z	1	$R_1 \rightarrow R_2$, if $R_0 = 0$ Abort
n+2	CONT	X	0	0	5	X	X	R_2	Z	X	X	2's C to S/M (R_2)
n+3	CJP	Scale Dividend	0	0	5	X	X	R_3	Z	OVR	1	2's C to S/M (R_3), if OVR ≥ 1, scale
n+4	CJP	n+7	0	4	9	X	X	R_2	0	OVR	1	Shift out sign of divisor
n+5	CONT	X	0	4	9	X	X	R_3	0	X	X	Shift out sign of divisor
n+6	CONT	X	0	2	F	0	R_2	R_3	1	X	X	Dividend - Divisor
n+7	CJP	Scale Dividend or Divisor	0	6	6	0	R_4	X	0	C_{n+4}	1	$R_4 \rightarrow Q$, if Carry = 1, scale
n+8	PUSH	$00D_{16}$	0	0	A	0	R_0	R_1	0	0	1	Loop set up and First Divide Operation
n+9	RFCT	X	0	0	C	0	R_0	R_1	Z	X	X	Test Loop Count and 2's C Divide
n+A	CONT	X	0	0	E	0	R_0	R_1	Z	X	X	2's C Divide Correction

Figure 24. Microcode for Double Precision Divide.

The first divide operation is used to ascertain the sign bit of the quotient. The two's complement divide instruction is then executed repetitively, fourteen times in the case of a sixteen bit divisor and a thirty-two bit dividend. The final step is the two's complement correction command which adjusts the quotient by allowing the least significant bit of the quotient to be set to one. At the end of the division algorithm the sixteen bit quotient is found in the Q register while the remainder now replaces the most significant half of the dividend in R_1. It should be noted that the remainder must be shifted down fifteen places to represent its true value. The interconnections for these instructions are shown in Figures 21, 22, 23. Using a typical CCU as shown in Figure 16, the double precision divide operation requires only eleven lines of microcode, as shown in Figure 24.

For those applications that require truncation instead of bias correction, the same algorithm as above should be implemented except one additional Two's Complement Divide instruction should be used in lieu of the Two's Complement Divide Correction and Remainder instruction. However, this technique results in an invalid remainder.

It is possible to do multiple-precision divide operations beyond the double precision divide shown above. For example, to do a triple precision divide for a 16-bit CPU, the upper two thirds of the dividend are stored in R_1 and Q as in the case for double precision divide. The lower third of the dividend is stored in a scratch register, R_5. After checking that the magnitude of the divisor is greater than the magnitude of the dividend, using the same tests as defined in Figure 20, the procedure is as follows:

1. Execute a Double Length Normalize/First Divide Operation instruction.
2. Execute the Two's Complement Divide instruction fifteen times.
3. Transfer the contents of Q, the most significant half of the quotient, to R_2.
4. Transfer R_5 to Q.
5. Execute the Two's Complement Divide instruction fifteen times.
6. Execute the Two's Complement Divide Correction and Remainder instruction.

The upper half of the quotient is then in R_2, the lower half of the quotient is in Q and the remainder is in R_1. The flow chart for this is shown in Figure 25. This technique can be expanded for any precision which is required.

BYTE SWAP

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am2958/2959 Three-state Buffers. The outputs of the three-

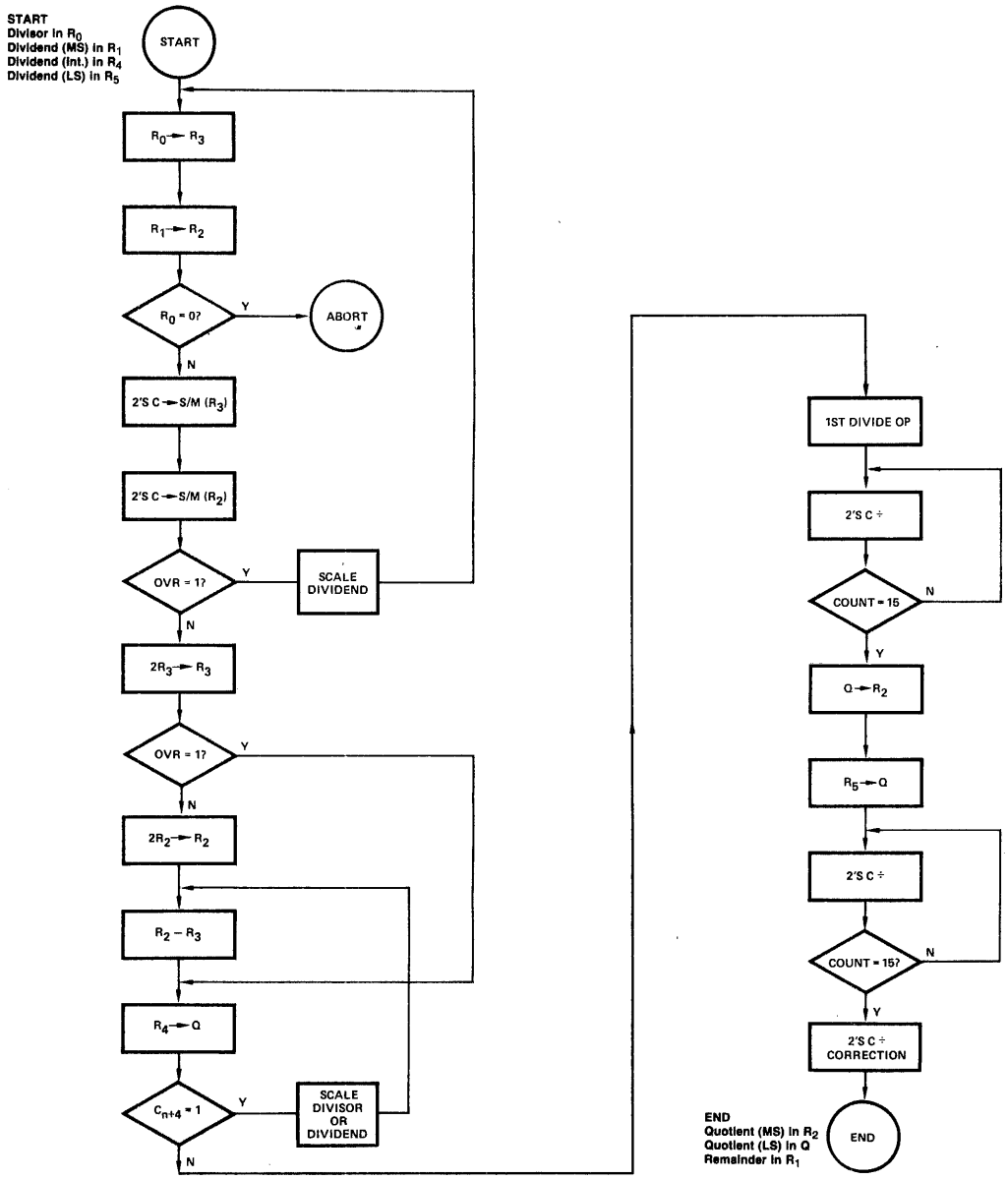

Figure 25. Division Flow Chart – Triple Precision Divide.

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state buffers are permuted such that the byte swap is achieved. The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of F = A plus C_n (C_n = 0) for the Am2958 or F = A plus C_n (C_n = 0) for the Am2959 and the destination command F Y, B.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27 Instead of inputting the permuted data via the DA ports, the permuted data is entered via the Y input/output ports with $\overline{OE_Y}$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command F → Y, B should be used.

WORD/BYTE OPERATIONS

The Am29203 allows for Word/Byte Operations. Figure 28 pictures a 16-bit system which is capable of doing word or byte (lower half of word) operations.

In the Byte mode the BYTE/$\overline{\text{WORD}}$ line is HIGH which in turn asserts a LOW on the $\overline{\text{W}}$/$\overline{\text{MSS}}$ input of Device 2 making it the MSS device. At the same time the multiplexer selects the status flags of Device 2. The $\overline{\text{IEN}}$ and $\overline{\text{OE}}_Y$ of Devices 4 and 3 are forced HIGH which disables them from writing into RAM or onto the Y bus.

In the word mode Device 4 is the $\overline{\text{MSS}}$ device and the multiplexer selects its status flags. The $\overline{\text{IEN}}$ inputs are brought low which enables writing in to RAM. The $\overline{\text{OE}}_Y$ is also allowed to go low.

MEMORY EXPANSION

Both the Am2903 and Am29203 allow for a theoretically infinite memory expansion, but the technique is slightly different. (The Am29203 allows writing less than a full word, e.g., a byte.) Figure 29, *Am2903 and Am29705*, pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am2903 and the Am29705s. The Am29705 RAM is functionally identical to the Am2903 RAM. The Am27S19 is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29705s or the Am2903. The memory addressing scheme specifies the data source for the R input of the ALU eminating from the register locations specified by address field A. A_{0-3} addresses 16 memory locations in each chip while address bits A_{4-6} are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

Bits B_{0-3} are for source register addressing in each chip. Bits B_4 and B_5 are used for chip output enable selection. C_{0-3} access the 16 destination addresses on each chip while bits C_4 and C_5 control the Write Enable of the desired chip. The source and destination register address are multiplexed such that when the clock is HIGH, the source register address is presented to the B address ports of the RAM's. The Instruction Enable ($\overline{\text{IEN}}$) is HIGH at this time. The data flows from the Y port or the internal B port as selected by the decoder whose inputs are B_4 and B_5. When the clock goes LOW, the data eminating from the selected Y outputs of the Am29705's and the RAM outputs of the Am2903 are latched and the destination address is now selected for use by the RAM address lines. When the destination address stabilizes on the address lines, the $\overline{\text{IEN}}$ pin is brought LOW. The $\overline{\text{WRITE}}$ output of the Am2903 will now go LOW, enabling the decoder sourced by address bits C_4 and C_5. The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$ and $B_{4-5} = C_{4-5}$. For two-address architecture, the MUX is removed from the circuit.

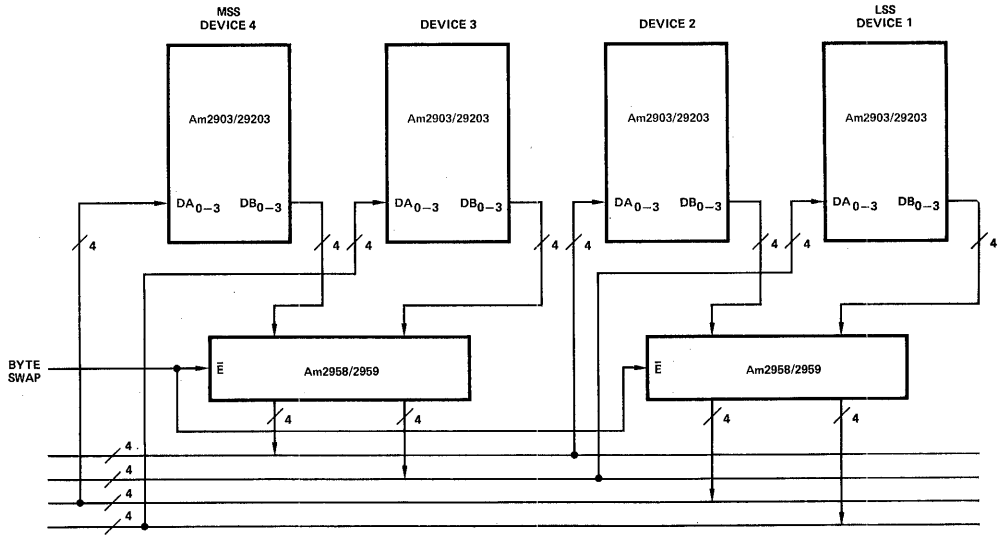

Figure 26. Byte Swap.

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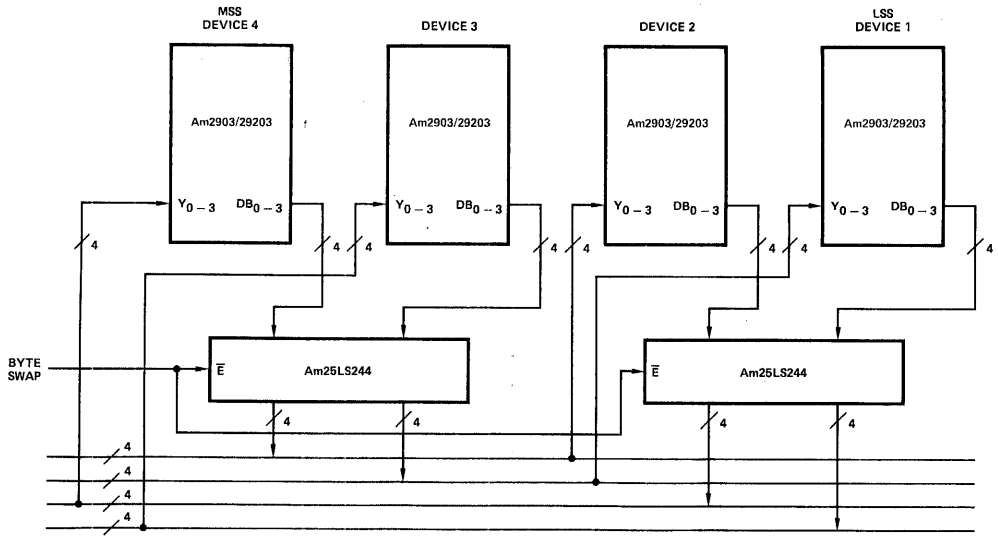

Figure 27. High Speed Byte Swap.

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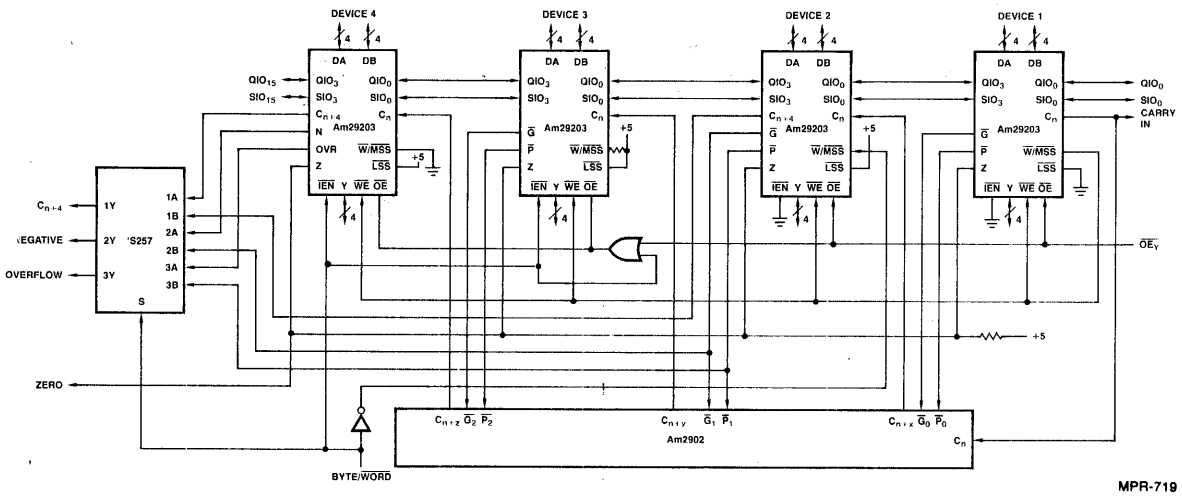

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Figure 28. Connections for Word/Byte Operations (Am29203 Only).

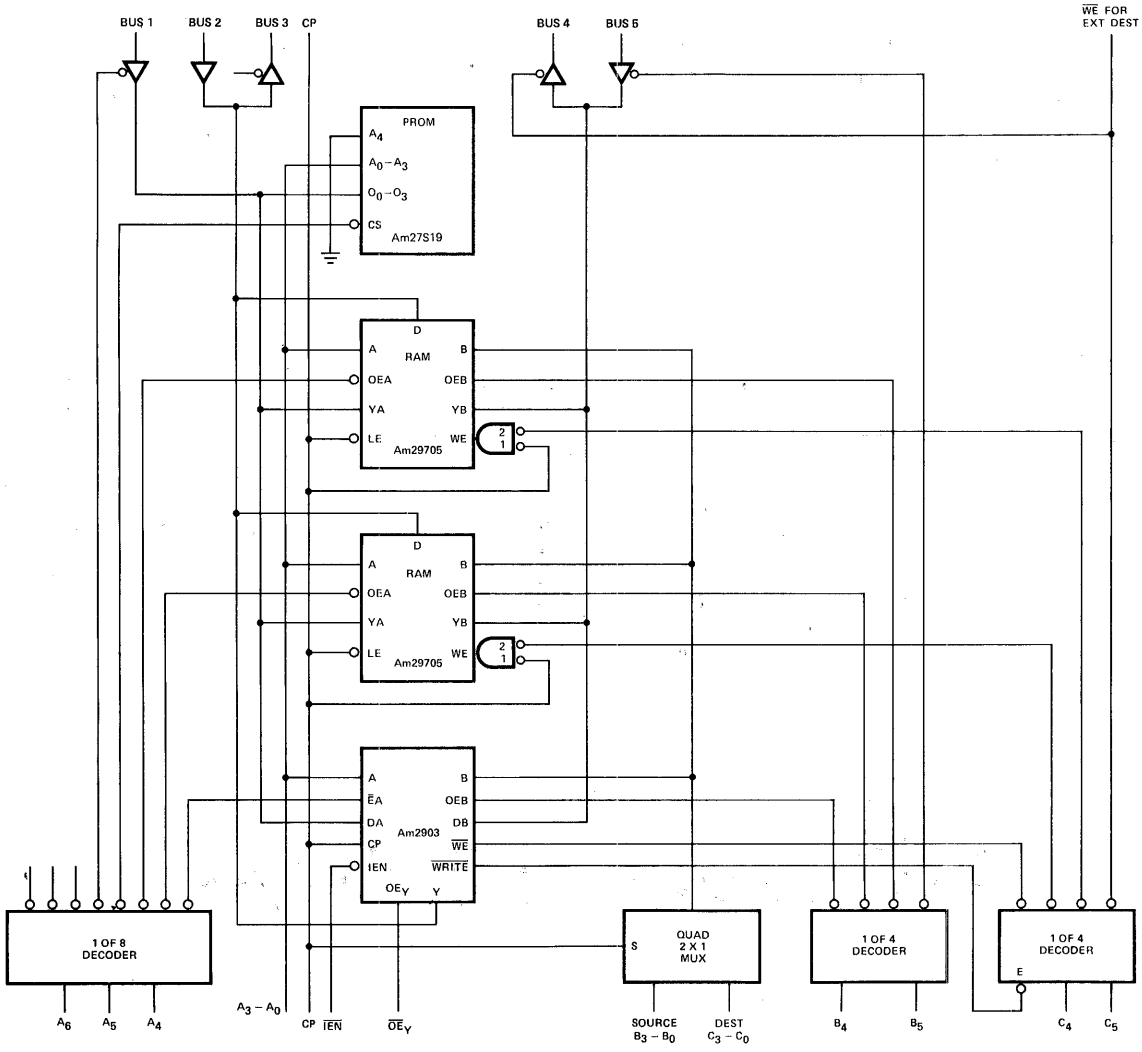

Figure 29. Expanded Memory on Am2903.

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Memory Expansion with the Am29203

The expansion scheme using the Am29203 and Am29705 is only slightly different from that for the Am2903, and is illustrated in Figure 30. The difference is due to the fact that the $\overline{\text{WRITE}}$ signal from the Am29203 is not internally gated by $\overline{\text{IEN}}$. This gating is performed external to the Am29203, either in a gate or, as shown in Figure 30, by using the enable on the chip select decoder. The advantage of separating the write signal from the $\overline{\text{IEN}}$ signal is that writing can be controlled over less than the full word length. For example, in a 16-bit system, the lower two devices can have one $\overline{\text{IEN}}$ signal and the upper two devices a second $\overline{\text{IEN}}$ signal. Controlling these two signals separately allows data to be written in either byte without disturbing the other byte. The 2- and 3-address architecture is handled in the same way as with the Am2903.

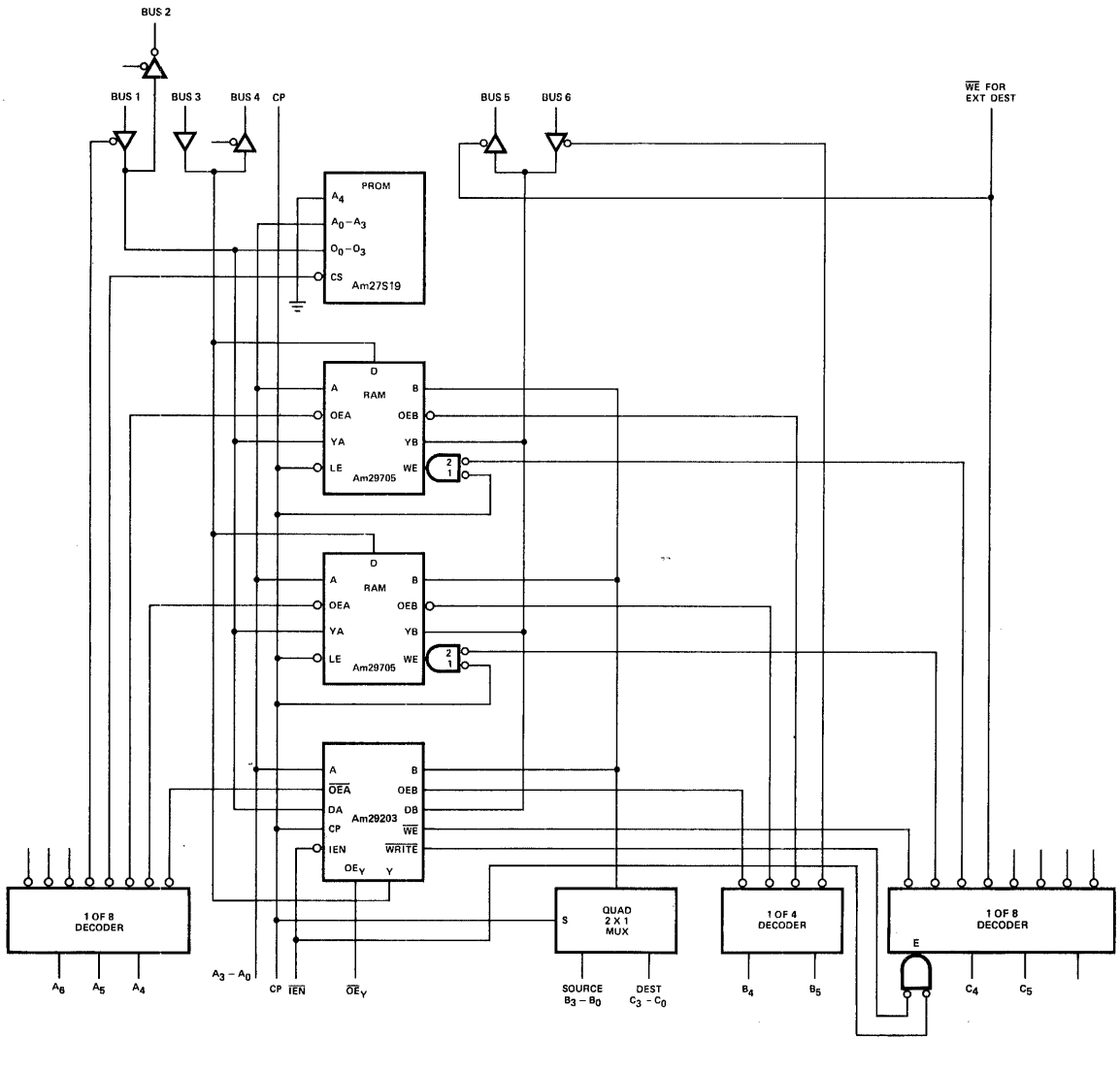


Figure 30. Expanded Memory for Am29203.

APPENDIX A

Am2903 SWITCHING CHARACTERISTICS

The switching characteristics of the Am2903 are a function of the power supply voltage, the temperature, and the operating mode of the device. The data has been condensed onto the tables on the following 24 pages. The first sets of tables define the speeds of the device for all operations except the special functions (where I_{43210} = 00000). The remaining tables define the speeds of the combinational paths for each of the special functions. Set-up and hold times do not change for the special functions. An index to the AC tables is shown below. The roman numeral identifies the conditions:

I = room temperature typical
II = room temperature guaranteed
III = guaranteed commercial operating range
IV = guaranteed military operating range

The letter designates the type of data:

A = standard function combinational delays
B = set-up and hold times
C = Enable/Disable times
D = clock and write pulses
E = special function combinational delays

2

Data is shown in Tables E in bold face where different from the data given in Tables A. Except where otherwise noted, data is taken with inputs switching between 0V and 3.0V at 1V/ns, with the measurement point at 1.5V. Outputs are measured at 1.5V and are loaded with C_L = 50pF and maximum DC load.

INDEX TO SWITCHING TABLES

Table	Data Type	Typical/ Guaranteed	Conditions	Applicable to
I A	Combinational Delays	Typical	5.0V, 25°C	Standard functions
II A	Combinational Delays	Guaranteed	5.0V, 25°C	Standard functions
III A	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Standard functions
III B	Set-up and Hold Times	Guaranteed	4.75 to 5.25V, 0°C to +70°C	All functions
III C	Enable/Disable Times	Guaranteed	4.75 to 5.25V, 0°C to +70°C	All functions
III D	Write Pulse and Clock	Guaranteed	4.75 to 5.25V, 0°C to +70°C	All functions
III E-0	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Unsigned multiply instruction
III E-2	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement multiply instruction
III E-4	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Increment by one or two instruction
III E-5	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Sign magnitude/two's complement conversion
III E-6	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement multiply, last cycle
III E-8	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Single-length normalize
III E-A	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	First divide operation (dbl. length norm.)
III E-C	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement divide
III E-E	Combinational Delays	Guaranteed	4.75 to 5.25V, 0°C to +70°C	Two's complement divide, correction
IV A	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Standard functions
IV B	Set-up and Hold Times	Guaranteed	4.5 to 5.5V, −55°C to +125°C	All functions
IV C	Enable/Disable Times	Guaranteed	4.5 to 5.5V, −55°C to +125°C	All functions
IV D	Write Pulse and Clock	Guaranteed	4.5 to 5.5V, −55°C to +125°C	All functions
IV E-0	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Unsigned multiply instruction
IV E-2	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement multiply instruction
IV E-4	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Increment by one or two instruction
IV E-5	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Sign magnitude/two's complement conversion
IV E-6	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement multiply, last cycle
IV E-8	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Single-length normalize
IV E-A	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	First divide operation (dbl. length norm.)
IV E-C	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement divide
IV E-E	Combinational Delays	Guaranteed	4.5 to 5.5V, −55°C to +125°C	Two's complement divide, correction

TABLE I A
Typical Combinational Delays
T_A = 25°C, V_{CC} = 5.0V
Standard Functions

To Output / From Input	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	54	48	43	66	54	67	–	–	–	52	58	74
B Address	63	56	52	75	62	71	31	–	–	61	66	90
A Address (Logic Mode)	54	–	42	66	55	–	–	–	–	49	59	74
B Address	53	–	45	63	53	–	31	–	–	53	56	76
DA Inputs (Arith. Mode)	40	36	30	52	40	55	–	–	–	37	43	62
DB Inputs	38	35	28	50	38	52	–	–	–	38	41	61
DA Inputs (Logic Mode)	40	–	29	52	40	–	–	–	–	38	43	62
DB Inputs	34	–	20	46	35	–	–	–	–	34	38	57
$\overline{EA}$	39	32	26	51	39	52	–	–	–	36	42	61
C_n	25	18	–	37	25	35	–	–	–	22	28	41
I_0	33	29	22	43	33	38	–	33	*	33 *	36 *	59 *
I_{4321}	46	42	44	57	44	52	–	33	*	42 *	47 *	68 *
I_{8765}	28	–	–	40	–	–	–	32	36 *	27 *	28 *	27 *
$\overline{IEN}$	–	–	–	–	–	–	–	12	–	–	–	–
SIO_3, SIO_0	15	–	–	–	–	–	–	–	–	–	17	20
Clock	55	53	44	67	57	67	23	–	25	53	60	66
Y	–	–	–	12	–	–	–	–	–	–	–	–
$\overline{MSS}$	28	–	28	40	28	28	–	–	–	28	30	28

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE III A
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	86	81	69	110	86	108	–	–	–	84	94	115
B Address	99	88	81	123	99	112	49	–	–	94	104	140
A Address (Logic Mode)	87	–	68	111	89	–	–	–	–	79	94	115
B Address	84	–	73	108	84	–	49	–	–	84	90	120
DA Inputs (Arith. Mode)	63	60	49	87	64	89	–	–	–	60	70	101
DB Inputs	61	59	47	85	62	84	–	–	–	62	68	98
DA Inputs (Logic Mode)	64	–	48	88	66	–	–	–	–	61	72	101
DB Inputs	55	–	32	79	57	–	–	–	–	52	61	93
$\overline{EA}$	59	53	42	83	59	83	–	–	–	57	64	98
C_n	40	30	–	64	40	58	–	–	–	38	46	67
I_0	52	48	36	76	52	63	–	49	*	50*	58*	93*
I_{4321}	71	65	72	95	69	84	–	49	*	66*	73*	105*
I_{8765}	42	–	–	66	–	–	–	50	60*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	26	–	–	50	–	–	–	–	–	–	29	36
Clock	87	87	71	111	88	108	37	–	40	84	92	105
Y	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay tc correct data is determined by something else.

TABLE III B
Guaranteed Set-up and Hold Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

To Output / From Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	20	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A, B as Sources	Clock	27	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	21	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	68	0	See Note 6

Notes:
1. For set-up times from all inputs not specified in Table B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

TABLE III C
Guaranteed Enable/Disable Times
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE III D
Guaranteed Clock and Write Pulse Characteristics
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE both LOW to Write	30	ns

TABLE III E-0
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Unsigned Multiply Instruction
(I_{8765} = 0_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**102**	88	–	–	99	112	49	–	–	94	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	94	–	–
DA, DB Inputs	MSS	**65**	60	–	–	64	89	–	–	–	62	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	62	–	–
$\overline{EA}$	MSS	**73**	53	–	–	59	83	–	–	–	57	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	57	–	–
C_n	MSS	**45**	30	–	–	40	58	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**94**	**95**	–	–	**87**	**102**	–	–	*	**70***	*	–
	IS	**94**	**95**	**80**	–	–	–	–	–	*	**70***	*	–
	LSS	**94**	**95**	**80**	**42**	–	–	–	49	*	**70***	*	–
I_{4321}	MSS	**102**	**96**	–	–	**92**	**110**	–	–	*	**72***	*	–
	IS	**102**	**96**	**81**	–	–	–	–	–	*	**72***	*	–
	LSS	**102**	**96**	**81**	**43**	–	–	–	49	*	**72***	*	–
I_{8765}	MSS	**102**	**90**	–	–	**77**	**84**	–	–	*	**72***	*	–
	IS	**102**	**90**	**84**	–	–	–	–	–	*	**72***	*	–
	LSS	**102**	**90**	**84**	**46**	–	–	–	50	*	**72***	*	–
Clock	MSS	**91**	87	–	–	88	108	37	–	40	84	–	–
	IS, LSS	87	87	71	**53**	–	–	37	–	40	84	–	–
Z	MSS	**74**	**62**	–	–	**70**	**78**	–	–	–	**71**	–	–
	IS	**74**	**62**	**48**	–	–	–	–	–	–	**71**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S + R + C_n$ if $Z = 1$
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-2
Guaranteed Combinational Delays
T_A = 0° to +70°C, V_{CC} = 4.75 to 5.25V
Two's Complement Multiply Instruction
(I_{8765} = 2_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**106**	88	–	–	99	112	49	–	–	94	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	94	–	–
DA, DB Inputs	MSS	**78**	60	–	–	64	89	–	–	–	62	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	62	–	–
$\overline{EA}$	MSS	**85**	53	–	–	59	83	–	–	–	57	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	57	–	–
C_n	MSS	**58**	30	–	–	40	58	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**104**	**95**	–	–	**89**	**102**	–	–	*	**68***	*	–
	IS	**104**	**95**	**78**	–	–	–	–	–	*	**68***	*	–
	LSS	**104**	**95**	**78**	**42**	–	–	–	49	*	**68***	*	–
I_{4321}	MSS	**112**	**95**	–	–	**94**	**108**	–	–	*	**71***	*	–
	IS	**112**	**95**	**78**	–	–	–	–	–	*	**71***	*	–
	LSS	**112**	**95**	**78**	**43**	–	–	–	49	*	**71***	*	–
I_{8765}	MSS	**98**	**84**	–	–	**76**	**100**	–	–	*	**71***	*	–
	IS	**98**	**84**	**82**	–	–	–	–	–	*	**71***	*	–
	LSS	**98**	**84**	**82**	**46**	–	–	–	50	*	**71***	*	–
Clock	MSS	**100**	87	–	–	88	108	37	–	40	84	–	–
	IS, LSS	87	87	71	**53**	–	–	37	–	40	84	–	–
Z	MSS	**90**	**62**	–	–	**69**	**78**	–	–	–	**71**	–	–
	IS	**90**	**62**	**48**	–	–	–	–	–	–	**71**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$R + S + C_n$ if $Z = 1$
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-4
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Increment by One or Two Instruction
(I_{8765} = 4_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mod	MSS	99	88	–	123	99	112	49	–	–	–	–	140
	IS, LSS	99	88	81	123	–	–	49	–	–	–	–	140
DA, DB Inputs	MSS	63	60	–	87	64	89	–	–	–	–	–	101
	IS, LSS	63	60	49	87	–	–	–	–	–	–	–	101
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	64	40	58	–	–	–	–	–	67
	IS, LSS	40	30	–	64	40	58	–	–	–	–	–	67
I_0	MSS	**66**	**60**	–	**90**	**71**	**82**	–	–	*	*	*	**103***
	IS	**66**	**60**	**58**	**90**	–	–	–	–	*	*	*	**103***
	LSS	**66**	**60**	**58**	**90**	–	–	–	49	*	*	*	**103***
I_{4321}	MSS	**71**	**60**	–	**95**	**72**	**80**	–	–	*	*	*	**102***
	IS	**71**	**60**	**58**	**95**	–	–	–	–	*	*	*	**102***
	LSS	**71**	**60**	**58**	**95**	–	–	–	49	*	*	*	**102***
I_{8765}	MSS	**71**	**60**	–	**95**	**72**	**82**	–	–	*	*	*	**102***
	IS	**71**	**60**	**58**	**95**	–	–	–	–	*	*	*	**102***
	LSS	**71**	**60**	**58**	**95**	–	–	–	50	*	*	*	**102***
Clock	MSS	87	87	71	111	88	108	37	–	40	–	–	105
	IS, LSS	87	87	71	111	88	108	37	–	40	–	–	105
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
Y	Any	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + 1 + C_n$.

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-5
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Sign Magnitude/Two's Complement Conversion
(I_{8765} = 5_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**138**	88	–	**70**	**138**	112	49	–	–	–	–	140
	IS, LSS	99	88	81	–	–	–	49	–	–	–	–	140
DA, DB Inputs	MSS	**98**	60	–	**40**	**98**	89	–	–	–	–	–	101
	IS, LSS	63	60	49	–	–	–	–	–	–	–	–	101
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	**79**	30	–	–	**79**	58	–	–	–	–	–	67
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	67
I_0	MSS	**102**	**78**	–	**46**	**100**	**112**	–	–	*	*	*	**131***
	IS	**102**	**78**	**70**	–	–	–	–	–	*	*	*	**131***
	LSS	**102**	**78**	**70**	–	–	–	–	49	*	*	*	**131***
I_{4321}	MSS	**102**	**78**	–	**46**	**100**	**103**	–	–	*	*	*	**131***
	IS	**102**	**78**	**72**	–	–	–	–	–	*	*	*	**131***
	LSS	**102**	**78**	**72**	–	–	–	–	49	*	*	*	**131***
I_{8765}	MSS	**100**	**78**	–	**46**	**97**	**105**	–	–	*	*	*	**138***
	IS	**100**	**78**	**65**	–	–	–	–	–	*	*	*	**138***
	LSS	**100**	**78**	**65**	–	–	–	–	50	*	*	*	**138***
Clock	MSS	**118**	87	71	**58**	**118**	108	37	–	–	–	–	105
	IS, LSS	87	87	71	–	–	–	37	–	–	–	–	105
Z	MSS	Z is an output											
	IS, LSS	**72**	**60**	**48**	–	–	–	–	–	–	–	–	**114**
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$\overline{S} + C_n$ if $Z = 1$
$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-6
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Two's Complement Multiply, Last Cycle
(I_{8765} = 6_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**120**	88	–	–	99	112	49	–	–	94	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	94	–	–
DA, DB Inputs	MSS	**85**	60	–	–	64	89	–	–	–	62	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	62	–	–
$\overline{EA}$	MSS	**93**	53	–	–	59	83	–	–	–	57	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	57	–	–
C_n	MSS	**64**	30	–	–	40	58	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**112**	**99**	–	–	**91**	**120**	–	–	*	**98***	*	–
	IS	**112**	**99**	**86**	–	–	–	–	–	*	**98***	*	–
	LSS	**112**	**99**	**86**	**42**	–	–	–	49	*	**98***	*	–
I_{4321}	MSS	**115**	**93**	–	–	**94**	**124**	–	–	*	**97***	*	–
	IS	**115**	**93**	**85**	–	–	–	–	–	*	**97***	*	–
	LSS	**115**	**93**	**85**	**43**	–	–	–	49	*	**97***	*	–
I_{8765}	MSS	**105**	**93**	–	–	**88**	**114**	–	–	*	**96***	*	–
	IS	**105**	**93**	**78**	–	–	–	–	–	*	**96***	*	–
	LSS	**105**	**93**	**78**	**50**	–	–	–	50	*	**96***	*	–
Clock	MSS	**110**	87	–	–	88	108	37	–	40	84	–	–
	IS, LSS	87	87	71	**53**	–	–	37	–	40	84	–	–
Z	MSS	**91**	**64**	–	–	**74**	**98**	–	–	–	**70**	–	–
	IS	**91**	**64**	**50**	–	–	–	–	–	–	**70**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$Y_3 = OVR \oplus F_3$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-8
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Single-Length Normalize Instruction
(I_{8765} = 8_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	88	–	–	99	112	49	–	–	–	–	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	–	–
DA, DB Inputs	MSS	63	60	–	–	64	89	–	–	–	–	–	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	–	–
$\overline{EA}$	MSS	59	53	–	–	59	83	–	–	–	–	–	–
	IS, LSS	59	53	42	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	–	40	58	–	–	–	–	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	–
I_0	MSS	**67**	**52**	–	**33**	**45**	**42**	–	–	*	*	**72***	–
	IS	**67**	**52**	**58**	**33**	–	–	–	–	*	*	**72***	–
	LSS	**67**	**52**	**58**	**33**	–	–	–	49	*	*	**72***	–
I_{4321}	MSS	**68**	**58**	–	**34**	**45**	**47**	–	–	*	*	**72***	–
	IS	**68**	**58**	**58**	**36**	–	–	–	–	*	*	**72***	–
	LSS	**68**	**58**	**58**	**36**	–	–	–	49	*	*	**72***	–
I_{8765}	MSS	**66**	**70**	–	**44**	**50**	**47**	–	–	*	*	**72***	–
	IS	**66**	**70**	**41**	**44**	–	–	–	–	*	*	**72***	–
	LSS	**66**	**70**	**41**	**44**	–	–	–	50	*	*	**72***	–
Clock	MSS	87	**49**	–	**46**	**49**	**47**	37	–	40	–	92	–
	IS, LSS	87	87	71	**48**	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$OVR = Q_2 \oplus Q_1$ (MSS)
$N = Q_3$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-A
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
First Divide Operation (Double Length Normalize)
($I_{8765} = A_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	**113**	–	**94**	**94**	**102**	49	–	–	–	**120**	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	104	–
DA, DB Inputs	MSS	63	**75**	–	**54**	**54**	**62**	–	–	–	–	**80**	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	70	–
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	**76**	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	64	–
C_n	MSS	40	**54**	–	**45**	**45**	**50**	–	–	–	–	**68**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**69**	**95**	–	**68**	**72**	**86**	–	–	*	*	**96** *	–
	IS	**69**	**95**	**56**	**68**	–	–	–	–	*	*	**96** *	–
	LSS	**69**	**95**	**56**	**68**	–	–	–	49	*	*	**96** *	–
I_{4321}	MSS	**69**	**94**	–	**68**	**72**	**86**	–	–	*	*	**96** *	–
	IS	**69**	**94**	**57**	**68**	–	–	–	–	*	*	**96** *	–
	LSS	**69**	**94**	**57**	**68**	–	–	–	49	*	*	**96** *	–
I_{8765}	MSS	**69**	**95**	–	**68**	**72**	**86**	–	–	*	*	**96** *	–
	IS	**69**	**95**	**57**	**68**	–	–	–	–	*	*	**96** *	–
	LSS	**69**	**95**	**57**	**68**	–	–	–	50	*	*	**96** *	–
Clock	MSS	87	**101**	–	**80**	**84**	**89**	37	–	40	–	**106**	–
	IS, LSS	87	87	71	**80**	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$N = F_3$ (MSS)
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-C
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Two's Complement Divide Operation
(I_{8765} = C_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	88	–	–	99	112	49	–	–	–	**107**	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	104	–
DA, DB Inputs	MSS	63	60	–	–	64	89	–	–	–	–	**84**	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	70	–
$\overline{EA}$	MSS	59	53	–	–	59	83	–	–	–	–	**91**	–
	IS, LSS	59	53	42	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	58	–	–	–	–	**64**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**94**	**93**	–	**39**	**94**	**120**	–	–	*	*	**108***	–
	IS	**94**	**93**	**74**	–	–	–	–	–	*	*	**108***	–
	LSS	**94**	**93**	**74**	–	–	–	–	49	*	*	**108***	–
I_{4321}	MSS	**94**	**84**	–	**42**	**93**	**120**	–	–	*	*	**108***	–
	IS	**94**	**84**	**74**	–	–	–	–	–	*	*	**108***	–
	LSS	**94**	**84**	**74**	–	–	–	–	49	*	*	**108***	–
I_{8765}	MSS	**93**	**89**	–	**43**	**93**	**120**	–		*	*	**108***	–
	IS	**93**	**89**	**64**	–	–	–	–	–	*	*	**108***	–
	LSS	**93**	**89**	**64**	–	–	–	–	50	*	*	**108***	–
Clock	MSS	87	87	–	**53**	88	108	37	–	40	–	**130**	–
	IS, LSS	87	87	71	–	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS, LSS	**68**	**65**	**52**	–	–	–	–	–	–	–	**77**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = R + S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE III E-E
Guaranteed Combinational Delays
T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Two's Complement Divide, Correction
(I_{8765} = E_H, I_{4321} = 0_H, I_0 = 0)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	99	88	–	–	99	112	49	–	–	–	104	–
	IS, LSS	99	88	81	–	–	–	49	–	–	–	104	–
DA, DB Inputs	MSS	63	60	–	–	64	89	–	–	–	–	70	–
	IS, LSS	63	60	49	–	–	–	–	–	–	–	70	–
$\overline{EA}$	MSS	59	53	–	–	59	83	–	–	–	–	64	–
	IS, LSS	59	53	42	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	58	–	–	–	–	46	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**95**	**91**	–	**42**	**94**	**120**	–	–	*	*	**98***	–
	IS	**95**	**91**	**72**	–	–	–	–	–	*	*	**98***	–
	LSS	**95**	**91**	**72**	–	–	–	–	49	*	*	**98***	–
I_{4321}	MSS	**96**	**91**	–	**42**	**94**	**118**	–	–	*	*	**98***	–
	IS	**96**	**91**	**78**	–	–	–	–	–	*	*	**98***	–
	LSS	**96**	**91**	**78**	–	–	–	–	49	*	*	**98***	–
I_{8765}	MSS	**85**	**78**	–	**43**	**74**	**89**	–	–	*	*	**88***	–
	IS	**85**	**78**	**62**	–	–	–	–	–	*	*	**88***	–
	LSS	**85**	**78**	**62**	–	–	–	–	50	*	*	**88***	–
Clock	MSS	87	87	–	**53**	88	108	37	–	40	–	92	–
	IS, LSS	87	87	71	–	–	–	37	–	40	–	92	–
Z	MSS	Z is an output											
	IS, LSS	**73**	**66**	**54**	–	–	–	–	–	–	–	**79**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = R + S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$Z = \overline{F_3} \oplus \overline{R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

Table IV A
Guaranteed Combinational Delays
T_C = −55° to +125°C, V_{CC} = 4.5V to 5.5V
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	91	85	72	116	92	115	–	–	–	89	98	120
B Address	101	93	84	126	102	118	52	–	–	97	106	148
A Address (Logic Mode)	92	–	72	117	93	–	–	–	–	84	98	120
B Address	86	–	73	111	89	–	52	–	–	86	92	125
DA Inputs (Arith. Mode)	64	62	51	89	66	94	–	–	–	62	71	107
DB Inputs	63	60	48	88	63	89	–	–	–	64	68	100
DA Inputs (Logic Mode)	65	–	51	90	67	–	–	–	–	62	72	108
DB Inputs	56	–	32	81	57	–	–	–	–	52	63	100
$\overline{EA}$	60	56	43	85	60	87	–	–	–	58	64	103
C_n	40	30	–	65	40	59	–	–	–	38	46	69
I_0	52	50	36	77	52	66	–	53	*	51 *	58 *	96 *
I_{4321}	72	69	73	97	71	88	–	53	*	66 *	75 *	111 *
I_{8765}	44	–	–	69	–	–	–	50	65 *	42 *	45 *	42 *
$\overline{IEN}$	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	26	–	–	51	–	–	–	–	–	–	29	36
Clock	89	90	74	114	89	116	39	–	42	91	96	110
Y	–	–	–	25	–	–	–	–	–	–	–	–
$\overline{MSS}$	45	–	44	70	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

TABLE IV B
Guaranteed Set-up and Hold Times
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions
CAUTION: READ NOTES TO TABLE B. NA = Not Applicable; no timing constraint.

Input	With Respect to this Signal	HIGH-to-LOW		LOW-to-HIGH		Comment
		Set-up	Hold	Set-up	Hold	
Y	Clock	NA	NA	23	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	35	0	To Write into RAM
A, B as Sources	Clock	38	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	23	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	74	0	See Note 6

Notes:
1. For set-up times from all inputs not specified in Table IV B, the set-up time is computed by calculating the delay to stable Y outputs and then allowing the Y set-up time. Even if the RAM is not being loaded, the Y set-up time is necessary to set-up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

TABLE IV C
Guaranteed Enable/Disable Times
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	34	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	70	60	ns
$\overline{LSS}$	$\overline{WRITE}$	34	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE IV D
Guaranteed Clock and Write Pulse Characteristics
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
All Functions

Minimum Clock LOW Time	40	ns
Minimum Clock HIGH Time	40	ns
Minimum Time CP and WE both LOW to Write	40	ns

TABLE IV E-0
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Unsigned Multiply Instruction
(I_{8765} = 0_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**103**	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	**66**	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	**74**	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	**45**	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**97**	**97**	–	–	**87**	**106**	–	–	*	**71***	*	–
	IS	**97**	**97**	**85**	–	–	–	–	–	*	**71***	*	–
	LSS	**97**	**97**	**85**	**42**	–	–	–	53	*	**71***	*	–
I_{4321}	MSS	**103**	**100**	–	–	**94**	**111**	–	–	*	**73***	*	–
	IS	**103**	**100**	**86**	–	–	–	–	–	*	**73***	*	–
	LSS	**103**	**100**	**86**	**43**	–	–	–	53	*	**73***	*	–
I_{8765}	MSS	**102**	**93**	–	–	**76**	**89**	–	–	*	**75***	*	–
	IS	**102**	**93**	**92**	–	–	–	–	–	*	**75***	*	–
	LSS	**102**	**93**	**92**	**51**	–	–	–	50	*	**75**	*	–
Clock	MSS	**94**	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	**57**	–	–	39	–	42	91	–	–
Z	MSS	**76**	**65**	–	–	**70**	**81**	–	–	–	**72**	–	–
	IS	**76**	**65**	**49**	–	–	–	–	–	–	**72**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S + R + C_n$ if $Z = 1$
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-2
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Multiply Instruction
($I_{8765} = 2_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**113**	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	**78**	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	**85**	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	**58**	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**105**	**97**	–	–	**89**	**102**	–	–	*	**71***	*	–
	IS	**105**	**97**	**81**	–	–	–	–	–	*	**71***	*	–
	LSS	**105**	**97**	**81**	**42**	–	–	–	53	*	**71***	*	–
I_{4321}	MSS	**112**	**98**	–	–	**94**	**111**	–	–	*	**75***	*	–
	IS	**112**	**98**	**85**	–	–	–	–	–	*	**75***	*	–
	LSS	**112**	**98**	**85**	**43**	–	–	–	53	*	**75***	*	–
I_{8765}	MSS	**99**	**86**	–	–	**78**	**100**	–	–	*	**74***	*	–
	IS	**99**	**86**	**84**	–	–	–	–	–	*	**74***	*	–
	LSS	**99**	**86**	**84**	**48**	–	–	–	50	*	**74***	*	–
Clock	MSS	**107**	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	**57**	–	–	39	–	42	91	–	–
Z	MSS	**90**	**65**	–	–	**70**	**81**	–	–	–	**72**	–	–
	IS	**90**	**65**	**48**	–	–	–	–	–	–	**72**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S + R + C_n$ is $Z = 1$
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-4
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Increment by One or Two Instruction
(I_{8765} = 4_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	126	102	118	52	–	–	–	–	148
	IS, LSS	101	93	84	126	–	–	52	–	–	–	–	148
DA, DB Inputs	MSS	64	62	–	89	66	94	–	–	–	–	–	107
	IS, LSS	64	62	51	89	–	–	–	–	–	–	–	107
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	65	40	59	–	–	–	–	–	69
	IS, LSS	40	30	–	65	40	59	–	–	–	–	–	69
I_0	MSS	**73**	**61**	–	**98**	**72**	**87**	–	–	*	*	*	**110***
	IS	**73**	**61**	**62**	**98**	–	–	–	–	*	*	*	**110***
	LSS	**73**	**61**	**62**	**98**	–	–	–	53	*	*	*	**110***
I_{4321}	MSS	**72**	**61**	–	**97**	**74**	**87**	–	–	*	*	*	**110***
	IS	**72**	**61**	**62**	**97**	–	–	–	–	*	*	*	**110***
	LSS	**72**	**61**	**62**	**97**	–	–	–	53	*	*	*	**110***
I_{8765}	MSS	**72**	**61**	–	**97**	**74**	**87**	–	–	*	*	*	**110***
	IS	**72**	**61**	**62**	**97**	–	–	–	–	*	*	*	**110***
	LSS	**72**	**61**	**62**	**97**	–	–	–	50	*	*	*	**110***
Clock	MSS	89	90	74	114	89	116	39	–	42	–	–	110
	IS, LSS	89	90	74	114	89	116	39	–	42	–	–	110
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
Y	Any	–	–	–	25	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + 1 + C_n$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-5
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Sign Magnitude/Two's Complement Conversion
(I_{8765} = 5_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**143**	93	–	**78**	**143**	118	52	–	–	–	–	148
	IS, LSS	101	93	84	–	–	–	52	–	–	–	–	148
DA, DB Inputs	MSS	**103**	62	–	**40**	**103**	94	–	–	–	–	–	107
	IS, LSS	64	62	51	–	–	–	–	–	–	–	–	107
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	**83**	30	–	–	**83**	59	–	–	–	–	–	69
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	69
I_0	MSS	**102**	**80**	–	**50**	**100**	**115**	–	–	*	*	*	**132***
	IS	**102**	**80**	**70**	–	–	–	–	–	*	*	*	**132***
	LSS	**102**	**80**	**70**	–	–	–	–	53	*	*	*	**132***
I_{4321}	MSS	**102**	**80**	–	**50**	**102**	**110**	–	–	*	*	*	**132***
	IS	**102**	**80**	**75**	–	–	–	–	–	*	*	*	**132***
	LSS	**102**	**80**	**75**	–	–	–	–	53	*	*	*	**132***
I_{8765}	MSS	**103**	**80**	–	**50**	**100**	**112**	–	–	*	*	*	**142***
	IS	**103**	**80**	**65**	–	–	–	–	–	*	*	*	**142***
	LSS	**103**	**80**	**65**	–	–	–	–	50	*	*	*	**142***
Clock	MSS	**120**	90	–	**61**	**120**	116	39	–	–	–	–	110
	IS, LSS	89	90	74	–	–	–	39	–	–	–	–	110
Z	MSS	Z is an output											
	IS, LSS	**76**	**61**	**51**	–	–	–	–	–	–	–	–	**118**
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = \overline{S} + C_n$ if Z = 0
$\overline{S} + C_n$ if Z = 1
$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-6
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Multiply, Last Cycle
(I_{8765} = 6_H, I_{4321} = 0_H, I_0 = 0)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	**121**	93	–	–	102	118	52	–	–	97	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	97	–	–
DA, DB Inputs	MSS	**88**	62	–	–	66	94	–	–	–	64	–	–
	IS, LSS	64	62	51	–	–	–	–	–	–	64	–	–
$\overline{EA}$	MSS	**96**	56	–	–	60	87	–	–	–	58	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	58	–	–
C_n	MSS	**64**	30	–	–	40	59	–	–	–	38	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	38	–	–
I_0	MSS	**118**	**102**	–	–	**97**	**126**	–	–	*	**102***	*	–
	IS	**118**	**102**	**87**	–	–	–	–	–	*	**102***	*	–
	LSS	**118**	**102**	**87**	**42**	–	–	–	53	*	**102***	*	–
I_{4321}	MSS	**120**	**101**	–	–	**97**	**127**	–	–	*	**101***	*	–
	IS	**120**	**101**	**86**	–	–	–	–	–	*	**101***	*	–
	LSS	**120**	**101**	**86**	**43**	–	–	–	53	*	**101***	*	–
I_{8765}	MSS	**105**	**98**	–	–	**88**	**115**	–	–	*	**102***	*	–
	IS	**105**	**98**	**86**	–	–	–	–	–	*	**102***	*	–
	LSS	**105**	**98**	**86**	**51**	–	–	–	50	*	**102***	*	–
Clock	MSS	**110**	90	–	–	89	116	39	–	42	91	–	–
	IS, LSS	89	90	74	**58**	–	–	39	–	42	91	–	–
Z	MSS	**92**	**67**	–	–	**80**	**103**	–	–	–	**72**	–	–
	IS	**92**	**67**	**53**	–	–	–	–	–	–	**72**	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ is $Z = 1$
$Y_3 = (OVR \oplus F_3)$ MSS
$Z = Q_0$ (LSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-8
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Single-Length Normalize Instruction
(I_{8765} = 8_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	–	102	118	52	–	–	–	–	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	–	–
DA, DB Inputs	MSS	63	60	–	–	66	94	–	–	–	–	–	–
	IS, LSS	63	60	51	–	–	–	–	–	–	–	–	–
$\overline{EA}$	MSS	60	56	–	–	60	87	–	–	–	–	–	–
	IS, LSS	60	56	43	–	–	–	–	–	–	–	–	–
C_n	MSS	40	30	–	–	40	59	–	–	–	–	–	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	–	–
I_0	MSS	**72**	**60**	–	**34**	**43**	**42**	–	–	*	*	**78***	–
	IS	**72**	**60**	**59**	**34**	–	–	–	–	*	*	**78***	–
	LSS	**72**	**60**	**59**	**34**	–	–	–	53	*	*	**78***	–
I_{4321}	MSS	**72**	**60**	–	**38**	**48**	**47**	–	–	*	*	**78***	–
	IS	**72**	**60**	**60**	**38**	–	–	–	–	*	*	**78***	–
	LSS	**72**	**60**	**60**	**38**	–	–	–	53	*	*	**78***	–
I_{8765}	MSS	**67**	**58**	–	**50**	**53**	**47**	–	–	*	*	**72***	–
	IS	**67**	**58**	**42**	**50**	–	–	–	–	*	*	**72***	–
	LSS	**67**	**58**	**42**	**50**	–	–	–	50	*	*	**72***	–
Clock	MSS	89	**53**	–	**53**	**49**	**49**	39	–	42	–	96	–
	IS, LSS	89	90	74	**53**	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS, LSS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$OVR = Q_2 \oplus Q_1$ (MSS)
$N = Q_3$ (MSS)
$Z = \overline{Q_0 Q_1 Q_2 Q_3}$

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-A
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
First Divide Operation (Double Length Normalize)
(I_{8765} = A_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	**122**	–	**96**	**100**	**112**	52	–	–	–	**130**	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	106	–
DA, DB Inputs	MSS	64	**80**	–	**63**	**65**	**72**	–	–	–	–	**84**	–
	IS, LSS	64	62	51	–	–	–	–	–	–	–	71	–
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	**80**	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	46	–
C_n	MSS	40	**57**	–	**48**	**48**	**55**	–	–	–	–	**68**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**71**	**98**	–	**85**	**72**	**91**	–	–	*	*	**101***	–
	IS	**71**	**98**	**61**	**85**	–	–	–	–	*	*	**101***	–
	LSS	**71**	**98**	**61**	**85**	–	–	–	53	*	*	**101***	–
I_{4321}	MSS	**71**	**98**	–	**85**	**76**	**91**	–	–	*	*	**101***	–
	IS	**71**	**98**	**61**	**85**	–	–	–	–	*	*	**101***	–
	LSS	**71**	**98**	**61**	**85**	–	–	–	53	*	*	**101***	–
I_{8765}	MSS	**71**	**98**	–	**85**	**76**	**91**	–	–	*	*	**101***	–
	IS	**71**	**98**	**61**	**85**	–	–	–	–	*	*	**101***	–
	LSS	**71**	**98**	**61**	**85**	–	–	–	50	*	*	**101***	–
Clock	MSS	89	**113**	–	**90**	**87**	**98**	39	–	42	–	**114**	–
	IS, LSS	89	90	74	**90**	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS	Z is an output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + C_n$
$N = F_3$ (MSS)
$SIO_3 = F_3 \oplus R_3$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-C
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Divide Operation
(I_{8765} = C_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	–	102	118	52	–	–	–	**112**	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	106	–
DA, DB Inputs	MSS	64	62	–	–	66	94	–	–	–	–	**88**	–
	IS, LSS	64	62	51	–	–	–	–	–	–	–	71	–
$\overline{EA}$	MSS	60	56	–	–	60	87	–	–	–	–	**96**	–
	IS, LSS	60	56	43	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	59	–	–	–	–	**64**	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**95**	**96**	–	**42**	**98**	**127**	–	–	*	*	**113***	–
	IS	**95**	**96**	**77**	–	–	–	–	–	*	*	**113***	–
	LSS	**95**	**96**	**77**	–	–	–	–	53	*	*	**113***	–
I_{4321}	MSS	**96**	**96**	–	**42**	**97**	**124**	–	–	*	*	**114***	–
	IS	**96**	**97**	**82**	–	–	–	–	–	*	*	**114***	–
	LSS	**96**	**97**	**82**	–	–	–	–	53	*	*	**114***	–
I_{8765}	MSS	**98**	**97**	–	**44**	**102**	**112**	–	–	*	*	**119***	–
	IS	**98**	**97**	**64**	–	–	–	–	–	*	*	**119***	–
	LSS	**98**	**97**	**64**	–	–	–	–	50	*	*	**119***	–
Clock	MSS	89	90	–	**58**	89	116	39	–	42	–	**136**	–
	IS, LSS	89	90	74	–	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS, LSS	**71**	**68**	**56**	–	–	–	–	–	–	–	**81**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = S + R + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

TABLE IV E-E
Guaranteed Combinational Delays
T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V
Two's Complement Divide, Correction
(I_{8765} = E_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith. Mode)	MSS	101	93	–	–	102	118	52	–	–	–	106	–
	IS, LSS	101	93	84	–	–	–	52	–	–	–	106	–
DA, DB Inputs	MSS	64	62	–	–	66	94	–	–	–	–	71	–
	IS, LSS	64	62	51	–	–	–	–	–	–	–	71	–
$\overline{EA}$	MSS	60	56	–	–	60	87	–	–	–	–	64	–
	IS, LSS	60	56	43	–	–	–	–	–	–	–	64	–
C_n	MSS	40	30	–	–	40	59	–	–	–	–	46	–
	IS, LSS	40	30	–	–	–	–	–	–	–	–	46	–
I_0	MSS	**98**	**96**	–	**42**	**96**	**127**	–	–	*	*	**105***	–
	IS	**98**	**96**	**78**	–	–	–	–	–	*	*	**105***	–
	LSS	**98**	**96**	**78**	–	–	–	–	53	*	*	**105***	–
I_{4321}	MSS	**100**	**96**	–	**43**	**97**	**123**	–	–	*	*	**104***	–
	IS	**100**	**96**	**84**	–	–	–	–	–	*	*	**104***	–
	LSS	**100**	**96**	**84**	–	–	–	–	53	*	*	**104***	–
I_{8765}	MSS	**85**	**78**	–	**44**	**78**	**95**	–	–	*	*	**89***	–
	IS	**85**	**78**	**62**	–	–	–	–	–	*	*	**89***	–
	LSS	**85**	**78**	**62**	–	–	–	–	50	*	*	**89***	–
Clock	MSS	89	90	–	**58**	89	116	39	–	42	–	96	–
	IS, LSS	89	90	74	–	–	–	39	–	42	–	96	–
Z	MSS	Z is an output											
	IS, LSS	**76**	**70**	**54**	–	–	–	–	–	–	–	**79**	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	Any	26	–	–	–	–	–	–	–	–	–	–	–

$F = R + S + C_n$ if $Z = 0$
$S - R - 1 + C_n$ if $Z = 1$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Notes: 1. A "*" means the output is enabled or disabled by the input. See Tables C for enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in bold face is different from Table A; other data is the same.

Am2903A

The Superslice®

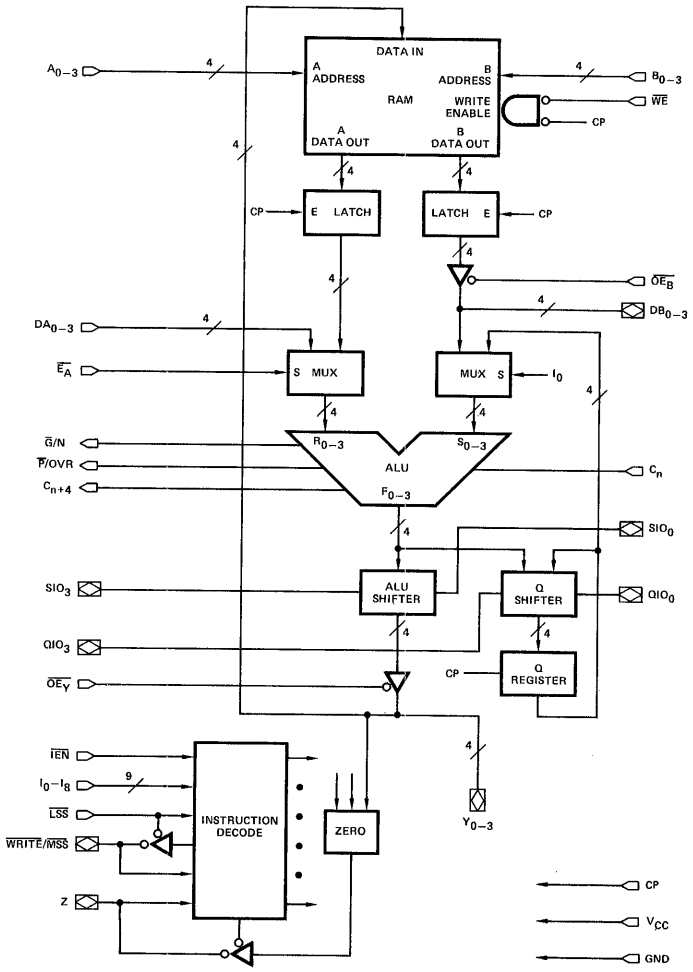
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Second generation of Am2903 Superslice® –**
  Improved design/process results in fastest version of the Am2903.
- **Plug-in replacement for Am2903 –**
  The Am2903A is a pin-for-pin replacement for the original version of the Am2903. Only the switching speeds have changed.
- **At least 30% faster –**
  The design objective is for the Am2903A to be at least 30% faster than the original Am2903 on critical paths.

2

BLOCK DIAGRAM



Am2904
Status and Shift Control Unit

DISTINCTIVE CHARACTERISTICS

- **Replaces most MSI used around any ALU** including the Am2901, Am2903 and MSI ALUs.
- **Generates Carry-In to the ALU**
  Carry signal is selectable from 7 different sources.
- **Contains shift linkage multiplexers**
  Connects to shift lines at the ends of an Am2901 or Am2903 array to implement single and double length arithmetic and logical shifts and rotates – 32 different modes in all.
- **Contains two edge-triggered status registers**
  Use for foreground/background registers in controllers or as microlevel and machine level status registers. Bit manipulating instructions are provided.
- **Condition Code Multiplexer on chip**
  Single cycle tests for any of 16 different conditions. Tests can be performed on either of the two status registers or directly on the ALU output.

DESCRIPTION

The Am2904 is designed to perform all the miscellaneous functions which are usually performed in MSI around an ALU. These include the generation of the carry-in signal to the ALU and carry lookahead unit; the interconnection of the data path, auxiliary register, and carry flip-flop during shift operations; and the storage and testing of ALU status flags. These tasks are accomplished in the Am2904 by three nearly independent blocks of logic. The carry-in is generated by a multiplexer. The shift linkages are established by four three-state multiplexers. There are two registers for storing the carry, overflow, zero, and negative status flags. The condition code multiplexer on the Am2904 can look at true or complement of any of the four status bits and certain combinations of status bits from either of the storage registers or directly from the ALU.

For additional applications refer to Chapter 4 of "Build A Microcomputer," the AMD application book on bipolar microprocessors.

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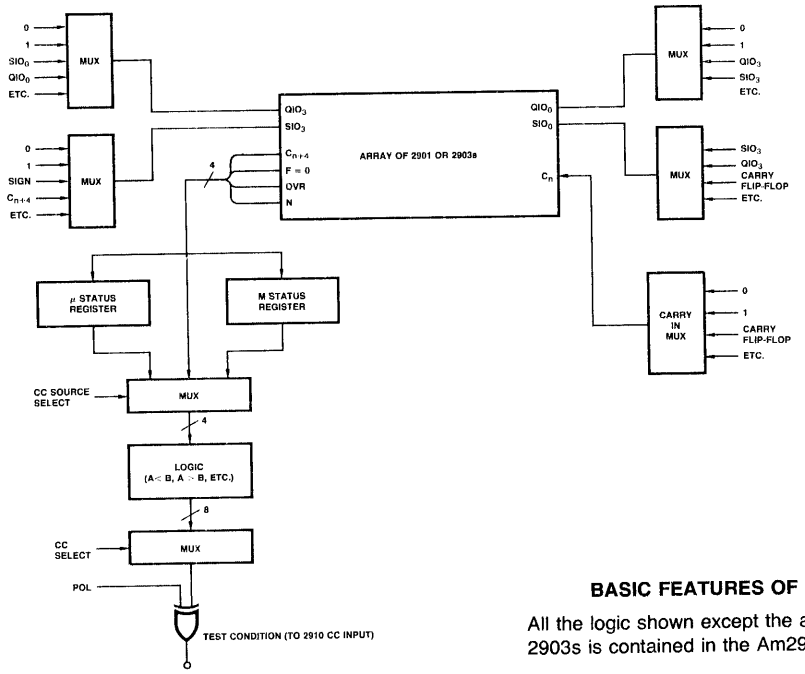
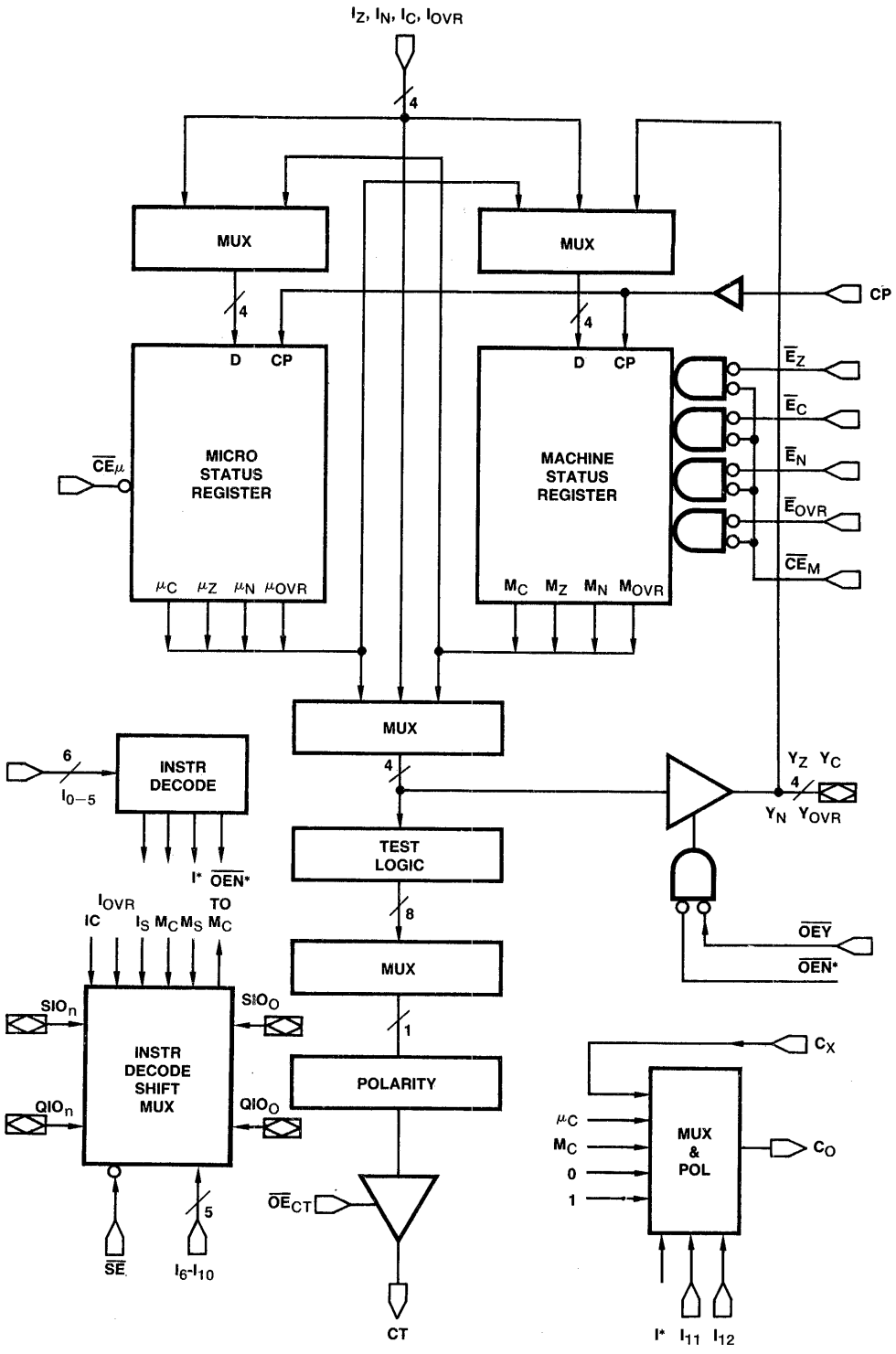


MPR-722

BASIC FEATURES OF Am2904

All the logic shown except the array of 2901s or 2903s is contained in the Am2904.

BLOCK DIAGRAM



*INTERNAL

MPR-060

Am2904 ARCHITECTURE

The Am2904 Status and Shift Control Unit provides four functions which are included in all processors. These are: a) Status Register, b) Condition Code Multiplexer, c) Shift Linkages and d) Carry-in Control. The architecture and instruction codes have been designed to complement the flexibility of the 2900 Family.

Status Register

The Am2904 contains two four-bit registers which can store the status outputs of an ALU: Carry (C), Negative (N), Zero (Z), and Overflow (OVR). They are designated Micro Status Register (μSR) and Machine Status Register (MSR). Each register can be independently controlled. The registers use edge-triggered D-type flip-flops which change state on the LOW to HIGH transition of the Clock Input.

The μSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}) or from the MSR under instruction control (I_{0-5}). The bits in the μSR can also be individually set or reset under instruction control (I_{0-5}). When the $\overline{CE\mu}$ input is HIGH, the μSR is inhibited from changing, independent of the I_{0-5} inputs.

The MSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}), from the μSR, and from the four parallel input/output pins (Y_C, Y_N, Y_Z, Y_{OVR}) under instruction control (I_{0-5}) .The MSR can also be set, reset or complemented under instruction control (I_{0-5}). The bits in the MSR can be selectively updated by controlling the four bit-enable inputs ($\overline{E_Z}$, $\overline{E_N}$, $\overline{E_C}$, $\overline{E_{OVR}}$) and the $\overline{CE_M}$ input. A LOW on both the $\overline{CE_M}$ input and the bit enable input for a specific bit enables updating that bit. A HIGH on a given bit enable input prevents the corresponding bit changing in the MSR. A HIGH on $\overline{CE_M}$ prevents any bits changing in the MSR.

The four parallel bidirectional input/output pins (Y_Z, Y_N, Y_C, Y_{OVR}) allow the contents of both the μSR and the MSR to be transferred to the system data bus and also allows the MSR to be loaded from the system data bus. This capability is used to save and restore the status registers during certain subroutines and when servicing interrupts.

Condition Code Multiplexer

The Condition Code Multiplexer output, CT, can be selected from 16 different functions. These include the true and complemented state of each of the status bits and combinations of these bits to detect such conditions as "greater than", "greater than or equal to", "less than" or "less than or equal to" for unsigned or two's complement numbers.

The Am2904 can perform these tests on the contents of the μSR, the MSR or the direct status inputs, (I_Z, I_N, I_C, I_{OVR}). The CT output is used as the test ($\overline{CC}$) input of the Am2910 and is provided with an output enable, $\overline{OE_{CT}}$ to make the addition of other condition inputs to this point easy.

Shift Linkage Multiplexer

The Shift Linkage Multiplexer generates the necessary linkages to allow the ALU to perform 32 different shift and rotate functions. Both single length and double length shifts and rotates, with and without carry (M_C), are provided. When the $\overline{SE}$ input is HIGH, the four input/output pins (SIO_0, SIO_n, QIO_0, QIO_n) are disabled. The SIO_0, SIO_n, QIO_0, QIO_n pins of the Am2904 are intended to be directly connected to the RAM_0, RAM_3, Q_0 and Q_3 pins of the Am2901 or the SIO_0, SIO_3, QIO_0, QIO_3 pins of the Am2903.

Carry-In Control Multiplexer

The Carry-In Control Multiplexer generates the C_0 output which can be selected from 7 functions (0, 1, C_X, μ_C, M_C, $\overline{\mu_C}$, $\overline{M_C}$). These functions allow easy implementation of both single length and double length addition and subtraction. The C_X input is intended to be connected to the Z output of the Am2903 to facilitate execution of some of the Am2903 special instructions. The C_0 pin is to be connected to the C_n pin of the least significant Am2901 or Am2903 and the C_n pin of the Am2902A.

Am2904 INSTRUCTION SET

The Am2904 is controlled by manipulating the 13 instruction lines, I_{0-12}, together with the nine enable lines, $\overline{CE_M}$, $\overline{CE\mu}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, $\overline{SE}$. Most systems will save on microword bits by tying some of these lines to a fixed level or by connecting certain lines together, or by decoding microinstructions to generate appropriate Am2904 controls.

Status Registers

Instruction lines I_5, I_4, I_3, I_2, I_1, I_0 control the Status Registers. Below, these lines are referred to as two octal digits.

Micro Status Register (μSR)

The instruction codes for the Micro Status Register fall into three groups: Bit Operations, Register Operations and Load Operations (See Table 1 and Map 1). All operations require

TABLE 1. MICRO STATUS REGISTER INSTRUCTION CODES.

Bit Operations

I_{543210} Octal	μSR Operation	Comments
10	0 → μ_Z	RESET ZERO BIT
11	1 → μ_Z	SET ZERO BIT
12	0 → μ_C	RESET CARRY BIT
13	1 → μ_C	SET CARRY BIT
14	0 → μ_N	RESET SIGN BIT
15	1 → μ_N	SET SIGN BIT
16	0 → μ_{OVR}	RESET OVERFLOW BIT
17	1 → μ_{OVR}	SET OVERFLOW BIT

Register Operations

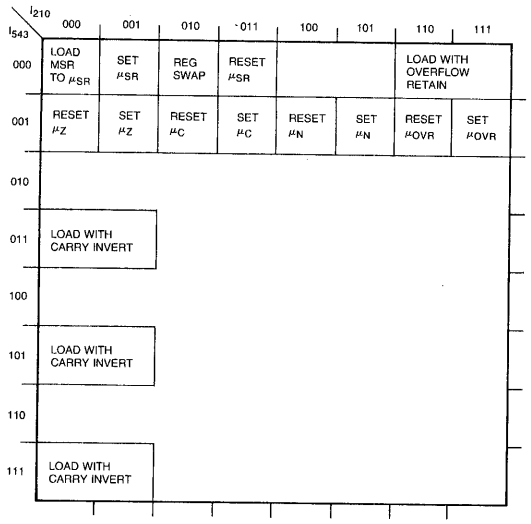
I_{543210} Octal	μSR Operation	Comments
00	M_X → μ_X	LOAD MSR TO μSR
01	1 → μ_X	SET μSR
02	M_X → μ_X	REGISTER SWAP
03	0 → μ_X	RESET μSR

Load Operations

I_{543210} Octal	μSR Operation	Comments
06, 07	I_Z → μ_Z I_C → μ_C I_N → μ_N I_{OVR} + μ_{OVR} → μ_{OVR}	LOAD WITH OVERFLOW RETAIN
30, 31 50, 51 70, 71	I_Z → μ_Z $\overline{I_C}$ → μ_C I_N → μ_N I_{OVR} → μ_{OVR}	LOAD WITH CARRY INVERT
04, 05 20-27 32-47 52-67 72-77	I_Z → μ_Z I_C → μ_C I_N → μ_N I_{OVR} → μ_{OVR}	LOAD DIRECTLY FROM I_Z, I_C, I_N, I_{OVR}

Note: The above tables assume $\overline{CE}$ μ is LOW.

MAP 1. MICRO STATUS REGISTER INSTRUCTION CODES.



Notes: 1. All unmarked locations are a load direct from I_Z, I_C, I_N, I_{OVR}.

that $\overline{CE}_\mu$ be LOW to operate.

Instruction Codes 10_8 to 17_8 are BIT operations. These operations set or reset the individual bits in the μSR.

Instruction Codes 00_8 to 03_8 are REGISTER operations. These operations affect all bits in the μSR.

00_8 This instruction loads the μSR with the contents of the MSR while loading the MSR from the Y inputs and is further explained under "INTERRUPTS".

01_8 This instruction SETS all μSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all μSR bits.

All instruction codes except those mentioned in the above two sections cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

06_8, 07_8 When a series of arithmetic operations are being executed sometimes it is not necessary to test for an overflow condition after *each* operation, but rather it is sufficient simply to know that an overflow occured during any one of the operations. Use of these instructions captures the overflow condition by loading the μSR overflow bit with the LOGICAL OR of its present state and I_{OVR}. Thus, once an overflow occurs, μOVR will remain set throughout the remaining operations.

30_8, 31_8, 50_8, 51_8, 70_8, 71_8 These instructions cause a load from the I inputs, but invert the carry bit. The reason for this is explained more fully under the "BORROW SAVE" section.

All others The remaining instructions load the μSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

Machine Status Register (MSR)

The instruction codes for the MSR fall into two groups; REGISTER Operations and LOAD Operations. All operations require that CE_M be LOW to operate (See Table 2 and Map 2).

BIT operations are accomplished by the use of Register or Load Operations with the $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ inputs selectively set LOW.

Instruction codes 00_8-03_8 and 05_8 are REGISTER operations. They affect only those bits enabled by $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

00_8 This instruction loads the MSR from the Y inputs while transferring the present contents to the μSR. The use of this instruction is further explained under "INTERRUPTS".

01_8 This instruction SETS all enabled MSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all enabled MSR bits.

05_8 This instruction COMPLEMENTS all enabled MSR bits.

All instruction codes except those mentioned in the above section cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

04_8 The Am2904 Shift Linkage Multiplexer allows for shifts and rotates through the MSR CARRY bit. Some machines require a shift or rotate through the OVERFLOW bit. By using this code, which swaps the contents of the MSR CARRY bit (M_C) and OVERFLOW bit (M_{OVR}), the shift or rotate can be made to appear to take place through the OVERFLOW bit. The procedure is to swap the bits, shift or rotate (any number or positions) then swap the bits again.

TABLE 2. MACHINE STATUS REGISTER INSTRUCTION CODES.

Register Operations

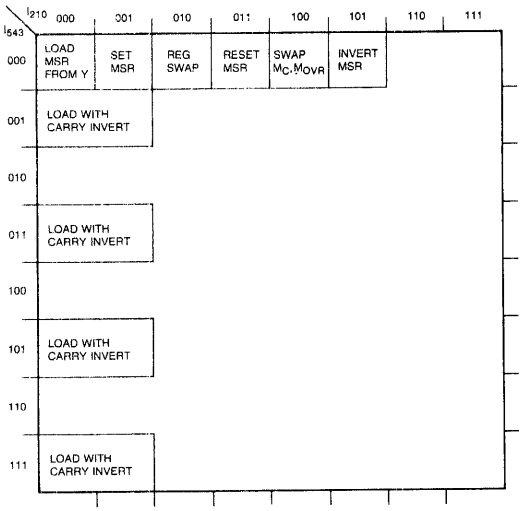
I_{543210} Octal	MSR Operation	Comments
00	$Y_X \rightarrow M_X$	LOAD Y_Z, Y_C, Y_N, Y_{OVR} TO MSR
01	$1 \rightarrow M_X$	SET MSR
02	$\mu_X \rightarrow M_X$	REGISTER SWAP
03	$0 \rightarrow M_X$	RESET MSR
05	$\overline{M_X} \rightarrow M_X$	INVERT MSR

Load Operations

I_{543210} Octal	MSR Operation	Comments
04	$I_Z \rightarrow M_Z$ $M_{OVR} \rightarrow M_C$ $I_N \rightarrow M_N$ $M_C \rightarrow M_{OVR}$	LOAD FOR SHIFT THROUGH OVERFLOW OPERATION
10, 11 30, 31 50, 51 70, 71	$I_Z \rightarrow M_Z$ $\overline{I_C} \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD WITH CARRY INVERT
06, 07 12-17 20-27 32-37 40-47 52-67 72-77	$I_Z \rightarrow M_Z$ $I_C \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C I_N, I_{OVR}

Notes: 1. The above tables assume $\overline{CE_M}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ are LOW.
2. A shift-through-carry instruction loads M_C irrespective of I_5-I_0.

MAP 2. MACHINE STATUS REGISTER INSTRUCTION CODES.



Note 1. All unmarked locations are a load direct from I_Z, I_C, I_{OVR}, I_N.

06_8, 07_8
12_8-27_8
32_8-47_8
52_8-67_8
72_8-77_8

These instructions load the MSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

10_8, 11_8
30_8, 31_8
50_8, 51_8
70_8, 71_8

These instructions cause a load from the I inputs but invert the CARRY bit. The reason for this is explained more fully under the "BORROW SAVE" section

Condition Code Multiplexer

The four instruction lines I_3, I_2, I_1, I_0 will select one of 16 possible operations to be carried out on the input bits, the result being routed to the Conditional Test Output (CT). Eight of the operations supply an individual status bit or its complement to the CT output. Another four do more complex operations while the remaining four are the complemented results of these (See Table 4).

TABLE 3. Y OUTPUT INSTRUCTION CODES.

$\overline{OE_Y}$	I_5	I_4	Y Output	Comment
1	X	X	Z	Output Off High Impedance
O	O	X	$\mu_i \rightarrow Y_i$	See Note 1
O	1	O	$M_i \rightarrow Y_i$	
O	1	1	$I_i \rightarrow Y_i$	

Notes: 1. For the conditions:
I_5, I_4, I_3, I_2, I_1, I_0 are LOW, Y is an input.
$\overline{OE_Y}$ is "Don't Care" for this condition.
2. X is "Don't Care" condition.

TABLE 4. CONDITION CODE OUTPUT (CT) INSTRUCTION CODES.

$I_3 - 0$ HEX	I_3	I_2	I_1	I_0	$I_5 = I_4 = 0$	$I_5 = 0, I_4 = 1$	$I_5 = 1, I_4 = 0$	$I_5 = I_4 = 1$
0	0	0	0	0	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(M_N \oplus M_{OVR}) + M_Z$	$(I_N \oplus I_{OVR}) + I_Z$
1	0	0	0	1	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(\mu_N \odot \mu_{OVR}) \cdot \overline{\mu}_Z$	$(M_N \odot M_{OVR}) \cdot \overline{M}_Z$	$(I_N \odot I_{OVR}) \cdot \overline{I}_Z$
2	0	0	1	0	$\mu_N \oplus \mu_{OVR}$	$\mu_N \oplus \mu_{OVR}$	$M_N \oplus M_{OVR}$	$I_N \oplus I_{OVR}$
3	0	0	1	1	$\mu_N \odot \mu_{OVR}$	$\mu_N \odot \mu_{OVR}$	$M_N \odot M_{OVR}$	$I_N \odot I_{OVR}$
4	0	1	0	0	μ_Z	μ_Z	M_Z	I_Z
5	0	1	0	1	$\overline{\mu}_Z$	$\overline{\mu}_Z$	$\overline{M}_Z$	$\overline{I}_Z$
6	0	1	1	0	μ_{OVR}	μ_{OVR}	M_{OVR}	I_{OVR}
7	0	1	1	1	$\overline{\mu}_{OVR}$	$\overline{\mu}_{OVR}$	$\overline{M}_{OVR}$	$\overline{I}_{OVR}$
8	1	0	0	0	$\mu_C + \mu_Z$	$\mu_C + \mu_Z$	$M_C + M_Z$	$\overline{I}_C + I_Z$
9	1	0	0	1	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{\mu}_C \cdot \overline{\mu}_Z$	$\overline{M}_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z$
A	1	0	1	0	μ_C	μ_C	M_C	I_C
B	1	0	1	1	$\overline{\mu}_C$	$\overline{\mu}_C$	$\overline{M}_C$	$\overline{I}_C$
C	1	1	0	0	$\overline{\mu}_C + \mu_Z$	$\overline{\mu}_C + \mu_Z$	$\overline{M}_C + M_Z$	$\overline{I}_C + I_Z$
D	1	1	0	1	$\mu_C \cdot \overline{\mu}_Z$	$\mu_C \cdot \overline{\mu}_Z$	$M_C \cdot \overline{M}_Z$	$I_C \cdot \overline{I}_Z$
E	1	1	1	0	$I_N \oplus M_N$	μ_N	M_N	I_N
F	1	1	1	1	$I_N \odot M_N$	$\overline{\mu}_N$	$\overline{M}_N$	$\overline{I}_N$

Notes: 1. $\oplus$ Represents EXCLUSIVE-OR
$\odot$ Represents EXCLUSIVE-NOR or coincidence.

TABLE 5. CRITERIA FOR COMPARING TWO NUMBERS FOLLOWING "A MINUS B" OPERATION.

	For Unsigned Numbers			For 2's Complement Numbers		
		I_{3-0}			I_{3-0}	
Relation	Status	CT = H	CT = L	Status	CT = H	CT = L
A = B	Z = 1	4	5	Z = 1	4	5
A ≠ B	Z = 0	5	4	Z = 0	5	4
A ≥ B	C = 1	A	B	N ⊙ OVR = 1	3	2
A < B	C = 0	B	A	N ⊕ OVR = 1	2	3
A > B	$C \cdot \overline{Z} = 1$	D	C	$(N \odot OVR) \cdot \overline{Z} = 1$	1	0
A ≤ B	$\overline{C} + Z = 1$	C	D	(N ⊕ OVR) + Z = 1	0	1

⊕ = Exclusive OR H = HIGH
⊙ = Exclusive NOR L = LOW

Note: For Am2910, the CC input is active LOW, so use I_{3-0} code to produce CT = L for the desired test.

The more complex operations are intended to follow the calculation A-B to give an indication of which is the larger (A, B unsigned) or more positive (A, B in 2's complement form). See Table 5.

The two instruction lines I_4, I_5 select whether the μSR, the MSR or the direct inputs I_Z, I_C, I_N, I_{OVR} are used as the inputs to the Y output buffer and the CT output (see Tables 3 and 4).

Instruction codes 16_8 and 17_8 form the EXCLUSIVE – OR and the EXCLUSIVE – NOR functions of M_N and I_N. The use of these instructions is explained under "NORMALIZING"

Shift Linkage Multiplexer

The five instruction lines I_{10}, I_9, I_8, I_7, I_6 control the SHIFT LINKAGE multiplexer. All instructions set up the linkages for both the ALU shifter (RAM shifter on the Am2901A) and the Q register.

UP and DOWN shifts are decided by I_{10} which should be connected to I_8 of the Am2903's instruction lines or I_7 of the Am2901's instruction lines. A wide range of input and output connections are provided, allowing for single or double length shifting or rotating with or without the use of the MSR CARRY or SIGN bits (See Table 7).

In the following discussion of some of the shifts the instruction codes are given as two octal digits AB; A represents I_{10}, I_9, B represents I_8, I_7, I_6.

When adding and down shifting on the same microcycle, (i.e. when doing multiplication or averaging) the shifter input must be the present CARRY, I_C, rather than the carry resulting from the last cycle (M_C). Instruction Code 13_8 accomplishes this for unsigned arithmetic. For 2's complement arithmetic, the required shifter input is: $I_N \oplus I_{OVR}$. This is provided by Instruction Code 16_8.

Instruction Codes 14_8, 15_8, 17_8 provide the RIGHT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

Instruction Codes 34_8, 35_8, 37_8 provide the LEFT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

The shift outputs are in the high impedance state unless $\overline{SE}$ is LOW.

Loading of the M_C bit by a shift operation overrides any loading or holding of the M_C bit by MSR Instructions (I_{0-5}, $\overline{CE_M}$ and $\overline{E_C}$).

"CARRY-IN" Control Multiplexer

The two instruction lines I_{12}, I_{11} control the source of the CARRY output (C_0).

When $I_{12} = 0$ $C_0 = I_{11}$

When $I_{12} = 1$ and $I_{11} = 0$, the external carry input C_X is presented to the carry output.

When $I_{12} = I_{11} = 1$ the carry output is selected from μ_C, $\overline{\mu_C}$, M_C or $\overline{M_C}$ as defined by I_5, I_3, I_2, I_1 (See Table 6).

TABLE 6. CARRY-IN CONTROL MULTIPLEXER INSTRUCTION CODES.

I_{12}	I_{11}	I_5	I_3	I_2	I_1	C_0
0	0	X	X	X	X	0
0	1	X	X	X	X	1
1	0	X	X	X	X	C_X
1	1	0	0	X	X	μ_C
1	1	0	X	1	X	μ_C
1	1	0	X	X	1	μ_C
1	1	0	1	0	0	$\overline{\mu_C}$
1	1	1	0	X	X	M_C
1	1	1	X	1	X	M_C
1	1	1	X	X	1	M_C
1	1	1	1	0	0	$\overline{M_C}$

APPLICATIONS INFORMATION

Borrow – Save

One of the capabilities of the Am2900 Family is the complete emulation of other processing machines. One requirement of an emulator is that, when a calculation is being performed, not only must the answer obtained from the Am2900 chips be the same as that from the machine being emulated, but after each machine level instruction, the status bits must be indentical.

There are alternative methods for subtracting in a digital machine and the state of the CARRY after the calculation depends on the method. For instance, the subtraction of 0100 from 1010 by the 2's complement add method generates a result of 0110 with a CARRY. Direct subtraction however, yields an answer of 0110 with no BORROW.

Many machines store the state of the CARRY for subtract operations, and this is the recommended method for maximum effective use of the Am2904, but, to allow those machines which store the BORROW to be efficiently emulated, the Am2904 has allocated special instructions. Using these codes causes the CARRY bit to be inverted before storage in the status registers and also re-inverts these status bits before using them as carry inputs. These codes are 10_8, 11_8, 30_8, 31_8, 50_8, 51_8, 70_8, 71_8 (I_{5-0}).

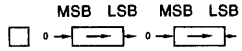
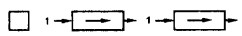
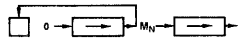
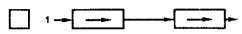
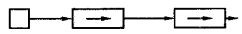
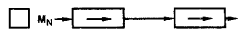
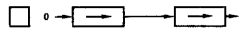
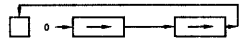
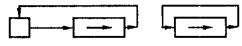
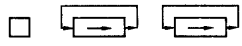
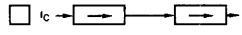
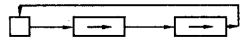
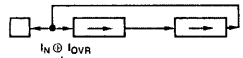
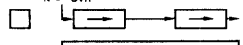
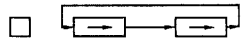
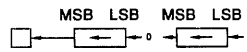
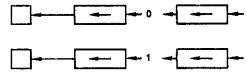
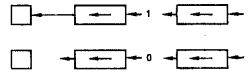
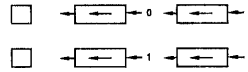
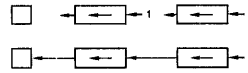
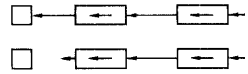
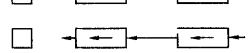
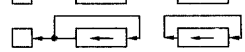
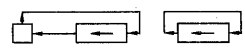
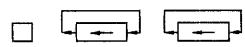
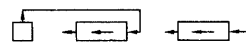
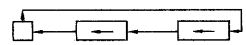
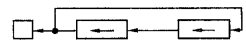
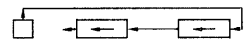
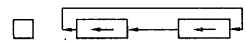
Notice that when these codes are used to load the inverted CARRY to either of the status registers, the CT output selected by the Condition Code Multiplexer assumes the CARRY is inverted and still defines whether $A > B$ or $A \leq B$ (See Table 4).

Similarly, when doing a compare on a machine which saves the borrow, testing for $A > B$, $A \leq B$ forces the complement of the CARRY to be stored in the status registers (See Tables 1 and 2).

Normalizing

Normalizing is the process of stripping off all leading sign bits until the two most significant bits are complementary. The Am2904 facilitates both single and double length normalization in the Am2901 and the Am2903. When using the NORMALIZE special instructions with the Am2903, the EXCLUSIVE – OR of the most significant two bits is generated at the C_{n+4} pin of the most significant Am2903. The EXCLUSIVE – OR of the two bits next to the most significant bit is also generated at the OVR pin. The procedure for normalizing then is to loop on the normalize instruction with a branch condition on the C_{n+4} state or the OVR state, depending on the architecture employed. The C_{n+4} or OVR output is routed to the Am2910 CC input through the Am2904 Condition Code multiplexer. As the contents of the status registers always refers to the last cycle, not the present one, the last operation in Normalizing is to downshift, bringing the sign bit (M_N) back into the most significant bit position. This is achieved using the shift operations 05_8 (I_{10-6}) for double length normalizing,

TABLE 7. SHIFT LINKAGE MULTIPLEXER INSTRUCTION CODES.

I_{10}	I_9	I_8	I_7	I_6	M_C RAM Q	SIO_0	SIO_n	QIO_0	QIO_n	Loaded Into M_C
					MSB LSB MSB LSB					
0	0	0	0	0		Z	0	Z	0	
0	0	0	0	1		Z	1	Z	1	
0	0	0	1	0		Z	0	Z	M_N	SIO_0
0	0	0	1	1		Z	1	Z	SIO_0	
0	0	1	0	0		Z	M_C	Z	SIO_0	
0	0	1	0	1		Z	M_N	Z	SIO_0	
0	0	1	1	0		Z	0	Z	SIO_0	
0	0	1	1	1		Z	0	Z	SIO_0	QIO_0
0	1	0	0	0		Z	SIO_0	Z	QIO_0	SIO_0
0	1	0	0	1		Z	M_C	Z	QIO_0	SIO_0
0	1	0	1	0		Z	SIO_0	Z	QIO_0	
0	1	0	1	1		Z	I_C	Z	SIO_0	
0	1	1	0	0		Z	M_C	Z	SIO_0	QIO_0
0	1	1	0	1		Z	QIO_0	Z	SIO_0	QIO_0
0	1	1	1	0		Z	$I_N \oplus I_{OVR}$	Z	SIO_0	
0	1	1	1	1		Z	QIO_0	Z	SIO_0	
					MSB LSB MSB LSB					
1	0	0	0	0		0	Z	0	Z	SIO_n
1	0	0	0	1		1	Z	1	Z	SIO_n
1	0	0	1	0		0	Z	0	Z	
1	0	0	1	1		1	Z	1	Z	
1	0	1	0	0		QIO_n	Z	0	Z	SIO_n
1	0	1	0	1		QIO_n	Z	1	Z	SIO_n
1	0	1	1	0		QIO_n	Z	0	Z	
1	0	1	1	1		QIO_n	Z	1	Z	
1	1	0	0	0		SIO_n	Z	QIO_n	Z	SIO_n
1	1	0	0	1		M_C	Z	QIO_n	Z	SIO_n
1	1	0	1	0		SIO_n	Z	QIO_n	Z	
1	1	0	1	1		M_C	Z	0	Z	
1	1	1	0	0		QIO_n	Z	M_C	Z	SIO_n
1	1	1	0	1		QIO_n	Z	SIO_n	Z	SIO_n
1	1	1	1	0		QIO_n	Z	M_C	Z	
1	1	1	1	1		QIO_n	Z	SIO_n	Z	

Notes: 1. Z = High impedance (outputs off) state.
2. Outputs enabled and M_C loaded only if $\overline{SE}$ is LOW.
3. Loading of M_C from I_{10-6} overrides control from I_{5-0}, $\overline{CE}_M$, $\overline{E}_C$.

and 02_8 for single length normalizing. For more details regarding normalizing with the Am2903 see the Am2903 data sheet.

The Am2901 does not have the EXCLUSIVE – OR gates to help with normalizing, so the Am2904 includes in the Condition Code multiplexer the EXCLUSIVE – OR and EXCLUSIVE – NOR functions of M_N (the sign bit resulting from the last operation) and I_N (the sign bit resulting from the present operation).

Interrupts

Some machines allow interrupts only at the machine instruction level while others allow them at the microinstruction level. The Am2904 is designed to handle both cases.

When the machine is interrupted, it is necessary to store the contents of either the MSR (machine instruction level interrupts) or both the status registers (micro instruction level interrupts) into an external store. This transfer is intended to take place over the Y input/output pins (See Table 3).

After the interrupt has been serviced the registers must be restored to their pre-interrupt state. This is accomplished by two operations of instruction 00_8 (I_{5-0}) which loads the MSR from the Y inputs while loading the μSR from the MSR. Thus, the pre-interrupt contents of the μSR are first loaded to the MSR (first instruction 00_8), then this data is transferred to the μSR while the MSR is restored to its pre-interrupt state (second instruction 00_8).

In controllers and some other microprogrammed machines the applications program itself is often in the microprogram memory; that is, there is no macroinstruction set. These machines require only a microstatus register since there is no separate machine status. The MSR in the Am2904 can be used as a one-level stack on the microstatus register. When an interrupt occurs, the μSR and the MSR are simply swapped ($I_{5-0} = 02_8$).

PIN DEFINITIONS

I_Z Zero status input pin, intended for connection to the Z outputs of the Am2903 or the F = 0 ouputs of the Am2901.

I_C Carry status input pin, intended for connection to the C_{n+4} output of the most significant ALU slice.

I_N Sign status input pin, intended for connection to the most significant ALU slice. The connection is to the N pin on the Am2903, and the F_3 pin on the Am2901.

I_{OVR} Overflow status input pin, intended for connection to the OVR pin on the most significant ALU slice.

I_{0-12} The thirteen instruction pins which select the operation the Am2904 is to perform.

$\overline{CE_M}$ This pin, used in conjunction with $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ acts as the overall enable for the machine status register. When the pin is LOW, MSR bits may be modified, according to the states of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$. When HIGH, the MSR will retain the present state, regardless of the state of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

$\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ These pins, when LOW, enable the corresponding bits in the Machine Status Register. When HIGH, they will prevent the corresponding bits from changing state. By using these pins together with the $\overline{CE_M}$ pin, MSR bits can be selectively modified.

$\overline{CE_\mu}$ This pin, when LOW, enables all four bits of the Micro Status Register. When this pin is HIGH, the μSR will not change state.

Y_Z, Y_C, Y_N, Y_{OVR} These pins form a three-state bidirectional bus over which MSR and μSR status can be read out or the MSR can be loaded in parallel.

$\overline{OE_Y}$ When LOW, this pin enables the Y pins as outputs. When HIGH, the Y outputs are in the high impedance state.

CT The conditional test output. The output of the Condition Code multiplexer appears here.

$\overline{OE_{CT}}$ When this pin is LOW, the CT pin is active. When HIGH the CT pin is in the high impedance state.

SIO_0, SIO_n, QIO_0, QIO_n These pins complete the linking for the various shift and rotate conditions. SIO_0 is intended for connection to the SIO_0 pin of the least significant Am2903 slice (RAM_0 for Am2901). SIO_n connects to the SIO_3 pin of the most significant Am2903 slice, (RAM_3 for Am2901). QIO_0 connects to the QIO_0 pin of the least significant Am2903 slice (QIO_0 for Am2901) and QIO_n connects to the QIO_3 pin of the most significant Am2903 slice (Q_3 for Am2901).

$\overline{SE}$ This pin controls the state of the shift outputs. When LOW, the shift outputs are enabled. When HIGH, the shift outputs are in the high impedance state.

C_0 This pin is the output of the Carry In control multiplexer. It connects to the C_n input of the least significant ALU slice, and the C_n input of the Am2902A.

C_X This pin is used as an input to the Carry In Control multiplexer which can route it to the C_0 pin. The C_X pin is intended for connection to the Z output of the Am2903 to facilitate some of the Am2903 special instructions.

CP The clock input to the device. The μSR and MSR are modified on the LOW to HIGH transition of the clock input. All other portions of the Am2904 are combinational and are unaffected by CP.

ORDERING INFORMATION

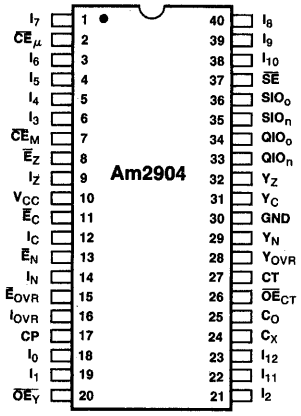
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2904PC	P-40	C	C-1
AM2904DC	D-40	C	C-1
AM2904DC-B	D-40	C	B-2 (Note 4)
AM2904DM	D-40	M	C-3
AM2904DM-B	D-40	M	B-3
AM2904FM	F-42	M	C-3
AM2904FM-B	F-42	M	B-3
AM2904XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2904XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

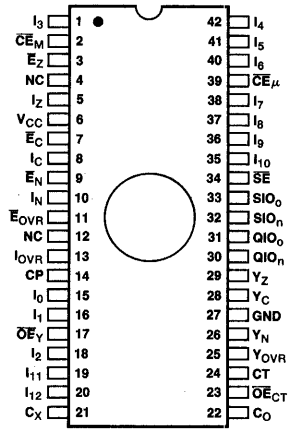
CONNECTION DIAGRAMS
Top Views

DIP



MPR-723

Flat Package



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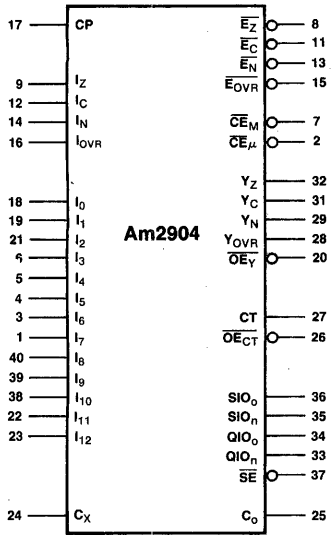
Note: Pin 1 is marked for orientation.
NC = No Connection.

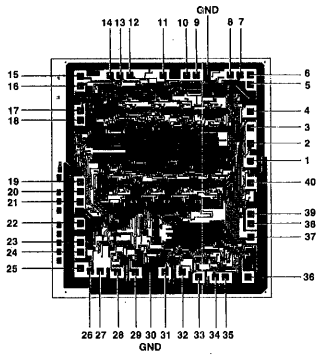
LOGIC SYMBOL
(DIP)



MPR-725

V_{CC} = Pin 10
GND = Pin 30

Am2904 Metallization and Pad Layout



DIE SIZE 0.140" X 0.161"
Pad Numbers correspond to DIP pinout

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2904PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V, MAX. = 5.25V)
Am2904DM, FM	MIL	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V, MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_Z, Y_C, Y_N, Y_{OVR}		2.4			Volts
			I_{OH} = −0.8mA SIO_o, SIO_n, QIO_o QIO_n, CT, CO		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_Z, Y_C Y_N, Y_{OVR}	I_{OL} = 24mA (Com'l)			0.5	
				I_{OL} = 16mA (MIL)			0.5	Volts
			SIO_o, QIO_o, CT, SIO_n, QIO_n, CO	I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	CP				−0.7	mA
			$\overline{CE_m}$, $\overline{CE_\mu}$				−1.8	
			I_Z, I_C, I_N, I_{OVR}				−1.2	
			I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$ $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X, Y_Z, Y_C, Y_N, Y_{OVR}				−0.45	
			$\overline{SE}$, SIO_o, SIO_n, QIO_o, QIO_n				−1.35	
I_{IH}	Input HIGH Current	V_{CC} = MAX. V_{IN} = 2.7V	CP, I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X				20	μA
			$\overline{CE_m}$, $\overline{CE_\mu}$				80	
			I_Z, I_C, I_N, I_{OVR}, $\overline{SE}$				60	
			SIO_o, SIO_n, QIO_o, QIO_n				110	
			Y_Z, Y_C, Y_N, Y_{OVR}				70	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	CT	V_O = 2.4			50	μA
				V_O = 0.5			−50	
			SIO_o, SIO_n, SIO_o, QIO_n (Note 4)	V_O = 2.4			110	
				V_O = 0.5			−1350	
			Y_Z, Y_C, Y_N, Y_{OVR} (Note 4)	V_O = 2.4			70	
				V_O = 0.5			−450	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V, V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX.		T_A = 25°C		180	296	mA
			Am2904PC, DC	T_A = 0°C to +70°C			318	
				T_A = +70°C			262	
			Am2904DM, FM	T_C = −55°C to +125°C			346	
				T_C = +125°C			220	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2904 XM, DM, FM. "COM'L" = Am2904 XC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

SWITCHING CHARACTERISTICS

The tables below define the Am2904 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	8	2
I_C (I_1 I_2 I_3 ≠ 001)	20	1
I_C (I_1 I_2 I_3 = 001)	8	1
$\overline{CE_\mu}$	12	0
$\overline{CE_M}$	16	0
$\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$	14	0
I_0-I_5	29	0
I_6-I_{10}	30	0
$\overline{SE}$	26	0
Y_Z, Y_C, Y_N, Y_{OVR} (I_0-I_5 = LOW)	9	0
SIO_o, SIO_n, QIO_o	10	0

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	27
CP	Y_Z, Y_C, Y_N, Y_{OVR}	38
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	32
I_Z, I_C, I_N, I_{OVR}	CT	35
CP	CT	43
I_0-I_5	CT	38
C_X	C_O	13
CP	C_O	28
$I_{1,2,3,5,11,12}$	C_O	28
SIO_n, QIO_n	SIO_o	17
SIO_o, QIO_o	SIO_n	16
I_C, I_N, I_{OVR}	SIO_n	23
SIO_n, QIO_n	QIO_o	18
SIO_o, QIO_o	QIO_n	16
CP	SIO_o, SIO_n QIO_o, QIO_n	29
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	23

C. Clock Requirements (ns)

Minimum Clock LOW Time	10
Minimum Clock HIGH Time	10

D. Enable/Disable Times (ns)
C_L = 5.0pF for Output Disable Tests

From (Input)	To (Output)	Enable	Disable
$\overline{OE_{CT}}$	CT	13	10
$\overline{SE}$	SIO_o, SIO_n QIO_o, QIO_n	21	8
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	30	20
$\overline{OE_Y}$	Y_Z, Y_C, Y_N, Y_{OVR}	16	12
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	23	25

GUARANTEED ROOM TEMPERATURE CHARACTERISITICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

(Group A, Subgroup 9 Tests)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	15	5
I_C (I_1 I_2 I_3 ≠ 001)	26	5
I_C (I_1 I_2 I_3 = 001)	15	5
$\overline{CE_\mu}$	18	5
$\overline{CE_M}$	22	5
$\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$	20	5
I_0-I_5	37	0
I_6-I_{10}	38	0
$\overline{SE}$	33	0
Y_Z, Y_C, Y_N, Y_{OVR} (I_0-I_5 = LOW)	15	5
SIO_o, SIO_n, QIO_o	17	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	35
CP	Y_Z, Y_C, Y_N, Y_{OVR}	46
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	43
I_Z, I_C, I_N, I_{OVR}	CT	43
CP	CT	54
I_0-I_5	CT	47
C_X	C_O	20
CP	C_O	36
$I_{1,2,3,5,11,12}$	C_O	36
SIO_n, QIO_n	SIO_o	23
SIO_o, QIO_o	SIO_n	23
I_C, I_N, I_{OVR}	SIO_n	30
SIO_n, QIO_n	QIO_o	25
SIO_o, QIO_o	QIO_n	22
CP	SIO_o, SIO_n QIO_o, QIO_n	37
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	30

C. Clock Requirements (ns)

Minimum Clock LOW Time	25
Minimum Clock HIGH Time	25

D. Enable/Disable Times (ns)
C_L = 5.0pF for Output Disable Tests

From (Input)	To (Output)	Enable	Disable
$\overline{OE_{CT}}$	CT	20	16
$\overline{SE}$	SIO_o, SIO_n QIO_o, QIO_n	29	14
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	38	24
$\overline{OE_Y}$	Y_Z, Y_C, Y_N, Y_{OVR}	22	19
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	38	32

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	27	5
I_C (I_1 I_2 I_3 ≠ 001)	28	5
I_C (I_1 I_2 I_3 = 001)	17	5
$\overline{CE}_\mu$	20	5
$\overline{CE}_M$	25	5
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$, $\overline{E}_{OVR}$	23	5
I_0-I_5	41	0
I_6-I_{10}	40	0
$\overline{SE}$	36	0
Y_Z, Y_C, Y_N, Y_{OVR} (I_0-I_5 = LOW)	18	5
SIO_o, SIO_n, QIO_o	19	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	38
CP	Y_Z, Y_C, Y_N, Y_{OVR}	50
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	43
I_Z, I_C, I_N, I_{OVR}	CT	48
CP	CT	58
I_0-I_5	CT	50
C_X	C_O	20
CP	C_O	37
$I_{1,2,3,5,11,12}$	C_O	37
SIO_n, QIO_n	SIO_o	25
SIO_o, QIO_o	SIO_n	24
I_C, I_N, I_{OVR}	SIO_n	32
SIO_n, QIO_n	QIO_o	26
SIO_o, QIO_o	QIO_n	23
CP	SIO_o, SIO_n QIO_o, QIO_n	39
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	32

C. Clock Requirements (ns)

Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30

D. Enable/Disable Times (ns)
C_L = 5.0pF for Output Disable Tests

From (Input)	To (Output)	Enable	Disable
$\overline{OE}_{CT}$	CT	23	18
$\overline{SE}$	SIO_o, SIO_n QIO_o, QIO_n	34	16
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	44	33
$\overline{OE}_Y$	Y_Z, Y_C, Y_N, Y_{OVR}	28	21
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	43	41

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	17	8
I_C (I_1 I_2 I_3 ≠ 001)	28	7
I_C (I_1 I_2 I_3 = 001)	18	6
$\overline{CE}_\mu$	20	4
$\overline{CE}_M$	25	6
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$ $\overline{E}_{OVR}$	23	6
I_0-I_5	48	0
I_6-I_{10}	44	2
$\overline{SE}$	40	0
Y_Z, Y_C, Y_N, Y_{OVR} (I_{0-5} = LOW)	18	6
SIO_o, SIO_n, QIO_o	19	6

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	40
CP	Y_Z, Y_C, Y_N, Y_{OVR}	50
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	43
I_Z, I_C, I_N, I_{OVR}	CT	55
CP	CT	67
I_0-I_5	CT	65
C_X	C_O	24
CP	C_O	38
$I_{1,2,3,5,11,12}$	C_O	43
SIO_n, QIO_n	SIO_o	27
SIO_o, QIO_o	SIO_n	27
I_C, I_N, I_{OVR}	SIO_n	35
SIO_n, QIO_n	QIO_o	28
SIO_o, QIO_o	QIO_n	28
CP	SIO_o, SIO_n QIO_o, QIO_n	39
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	32

C. Clock Requirements (ns)

Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30

D. Enable/Disable Times (ns)
C_L = 5.0pF for Output Disable Tests

From (Input)	To (Output)	Enable	Disable
$\overline{OE}_{CT}$	CT	25	18
$\overline{SE}$	SIO_o, SIO_n QIO_o, QIO_n	34	16
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	44	33
$\overline{OE}_Y$	Y_Z, Y_C, Y_N, Y_{OVR}	28	21
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	43	41

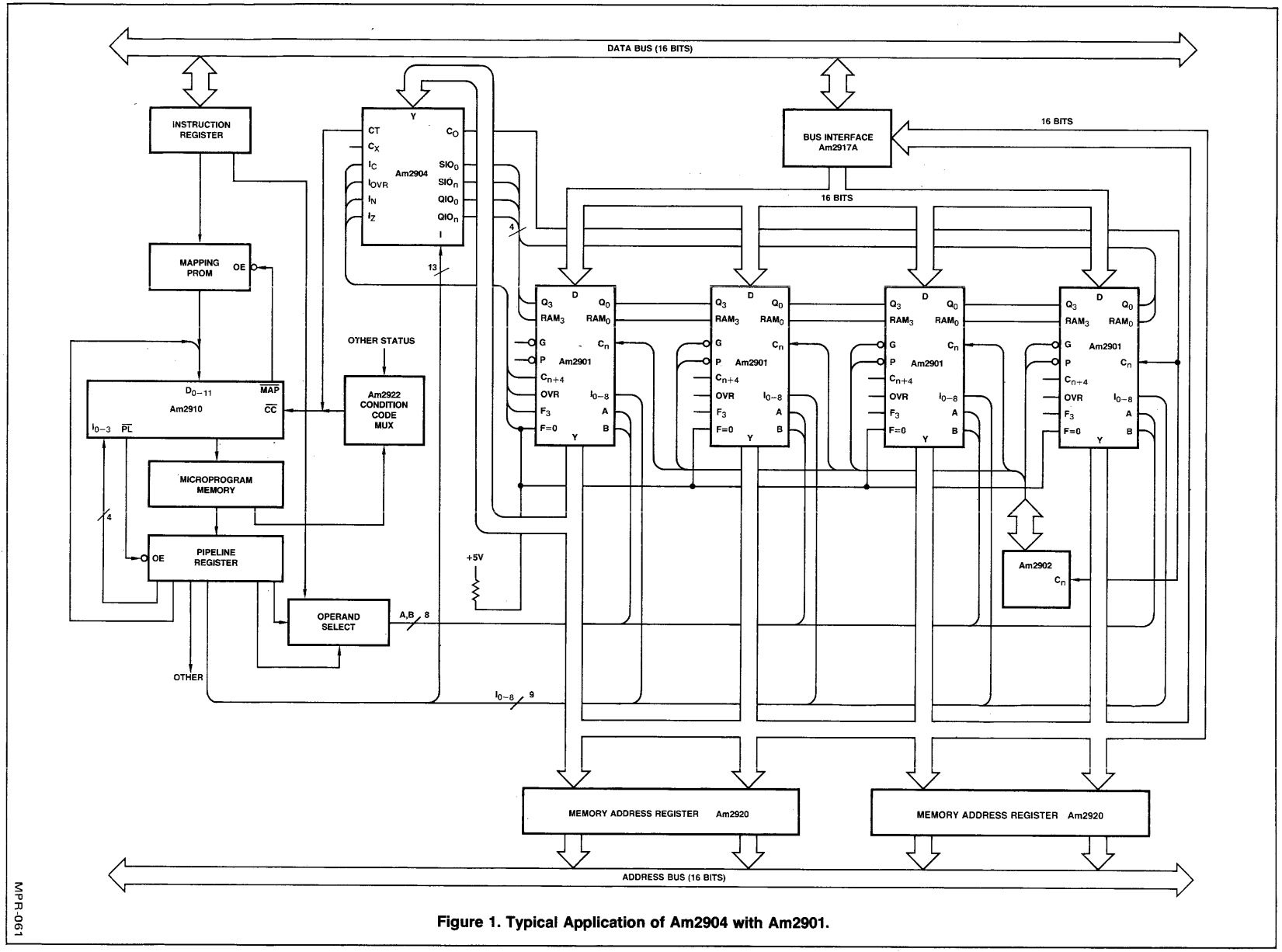


Figure 1. Typical Application of Am2904 with Am2901.

MPR-061

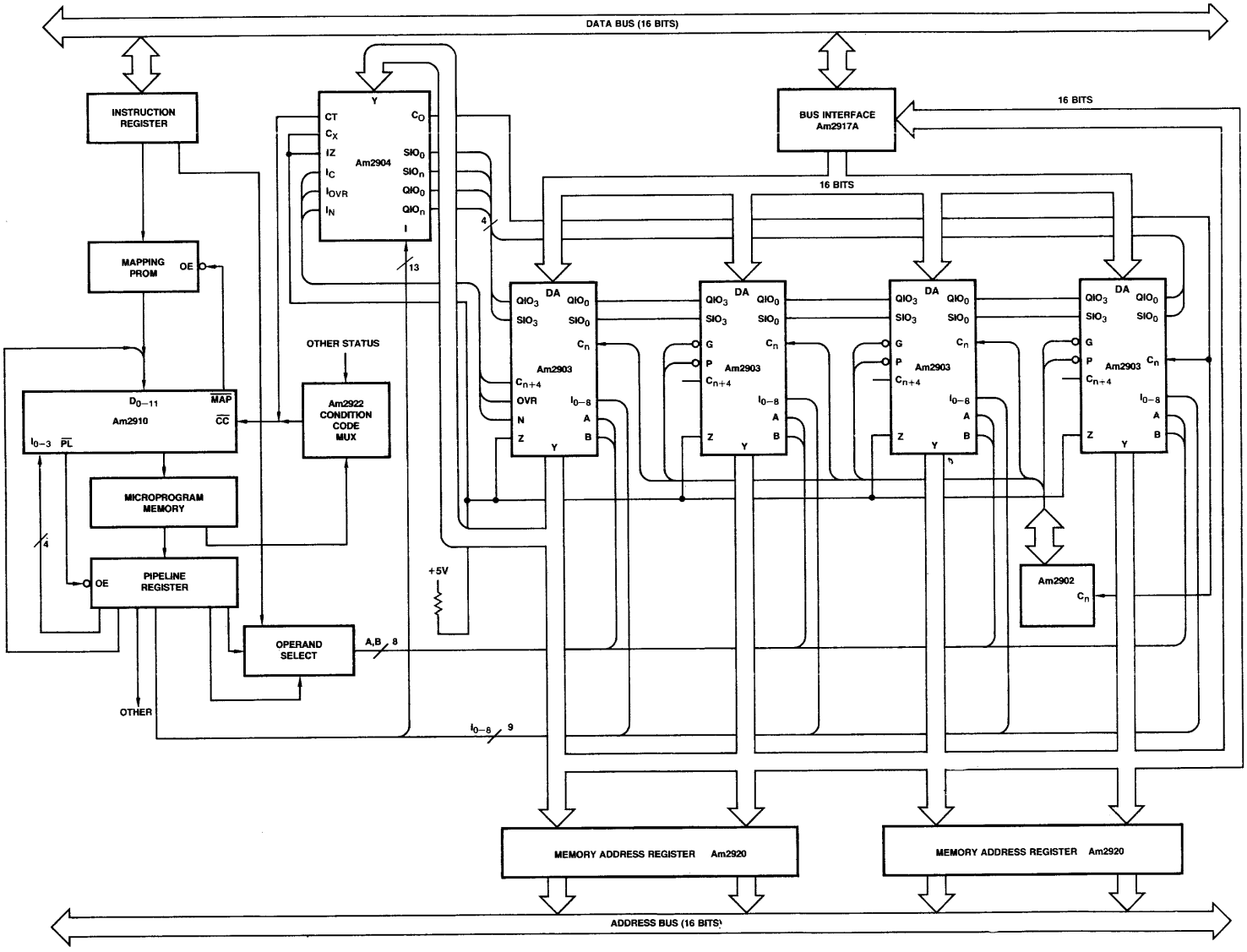


Figure 2. Typical Application of Am2904 with Am2903.

MPR-062

Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

2

FUNCTIONAL DESCRIPTION

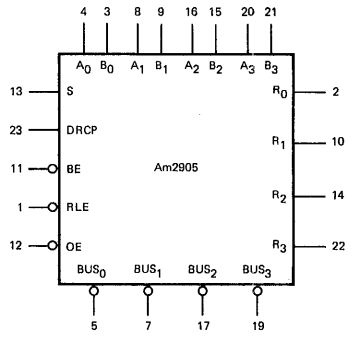
The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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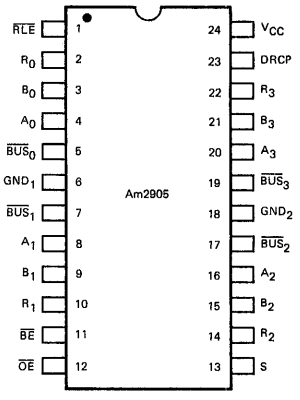
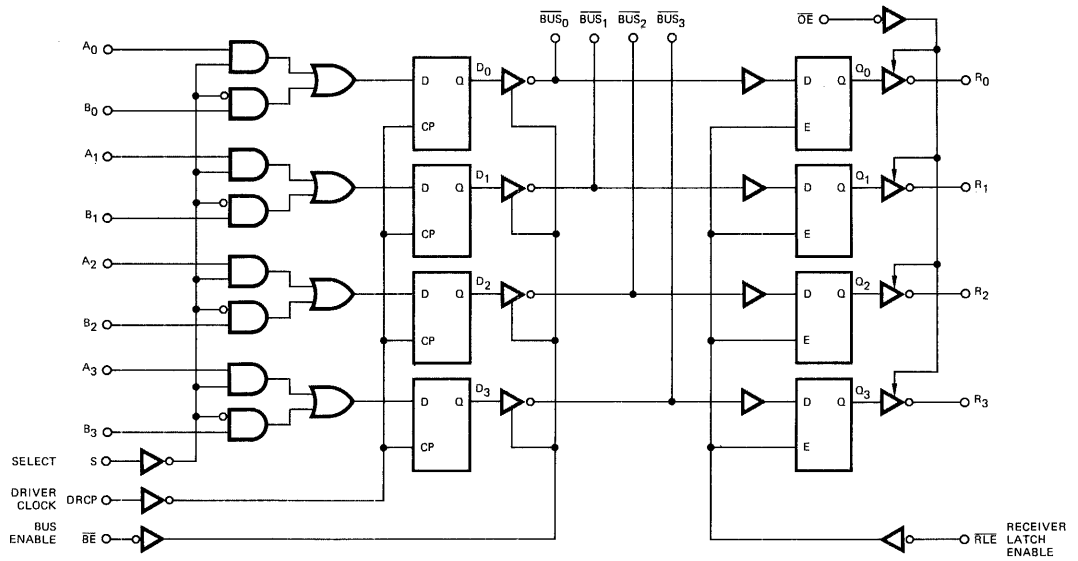
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-064

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2905XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

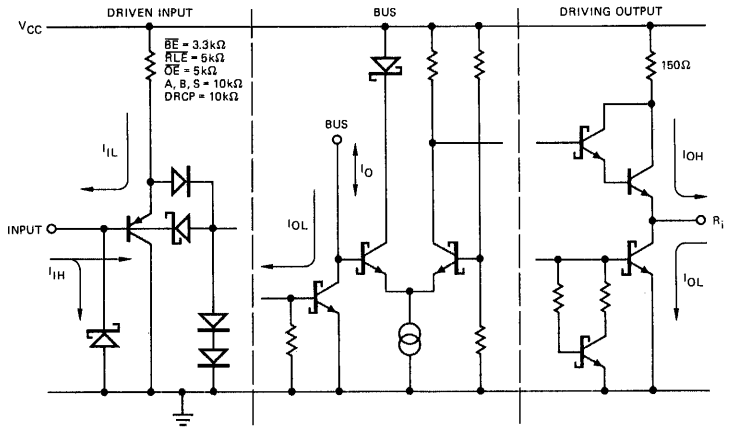
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$V				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	$V_O = 2.4$V			20	μA
			$V_O = 0.4$V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

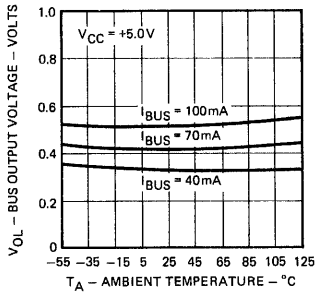


Note: Actual current flow direction shown.

MPR-066

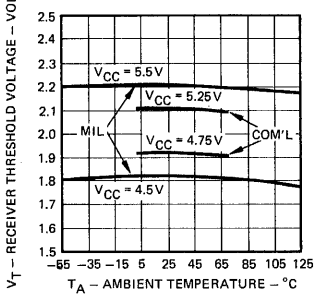
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



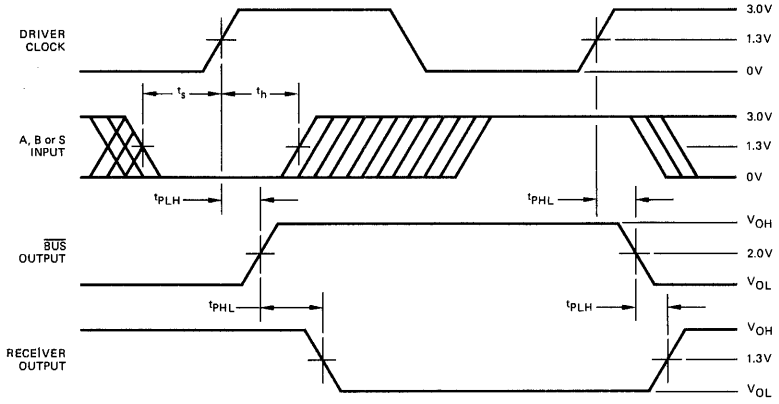
MPR-067

Receiver Threshold Variation Versus Ambient Temperature



MPR-068

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-069

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care I = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2905PC	P-24	C	C-1
AM2905DC	D-24	C	C-1
AM2905DC-B	D-24	C	B-1
AM2905DM	D-24	M	C-3
AM2905DM-B	D-24	M	B-3
AM2905FM	F-24-1	M	C-3
AM2905FM-B	F-24-1	M	B-3
AM2905XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2905XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

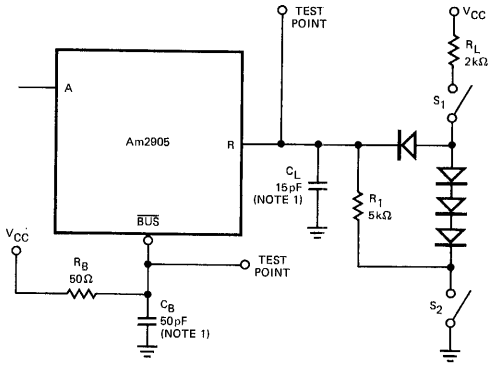
$\overline{BUS_0}$, $\overline{BUS_1}$, $\overline{BUS_2}$, $\overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

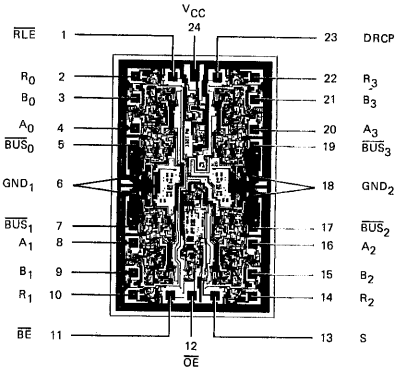
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



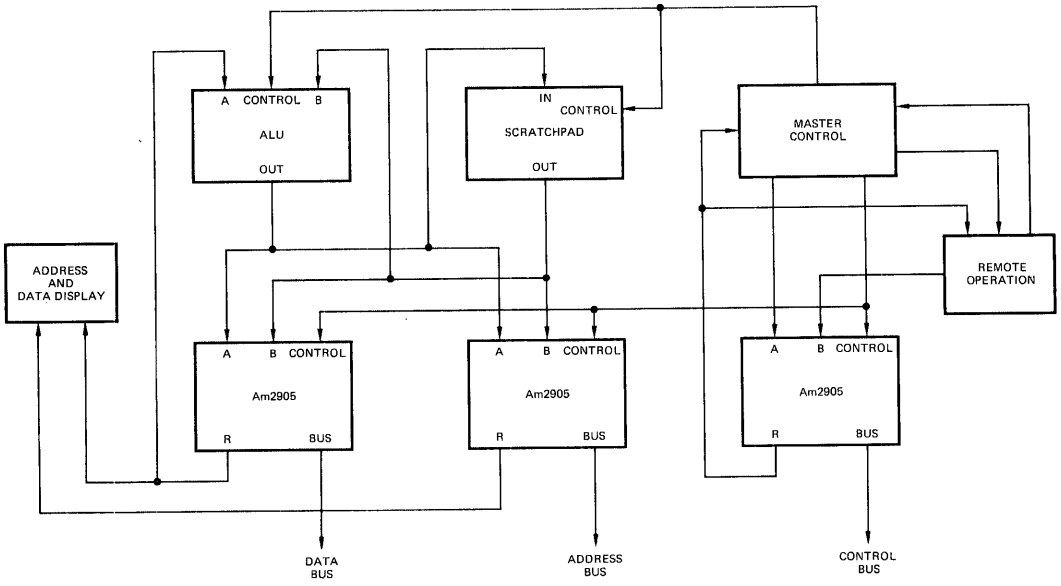
MPR-070

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-071

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

2

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

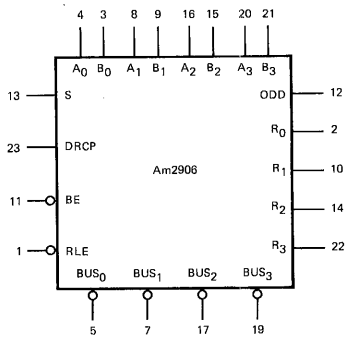
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

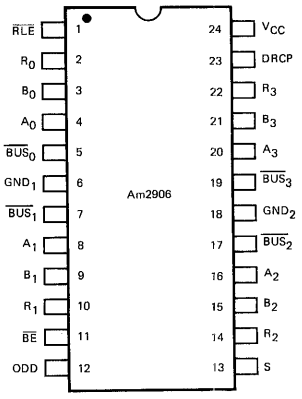
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-073

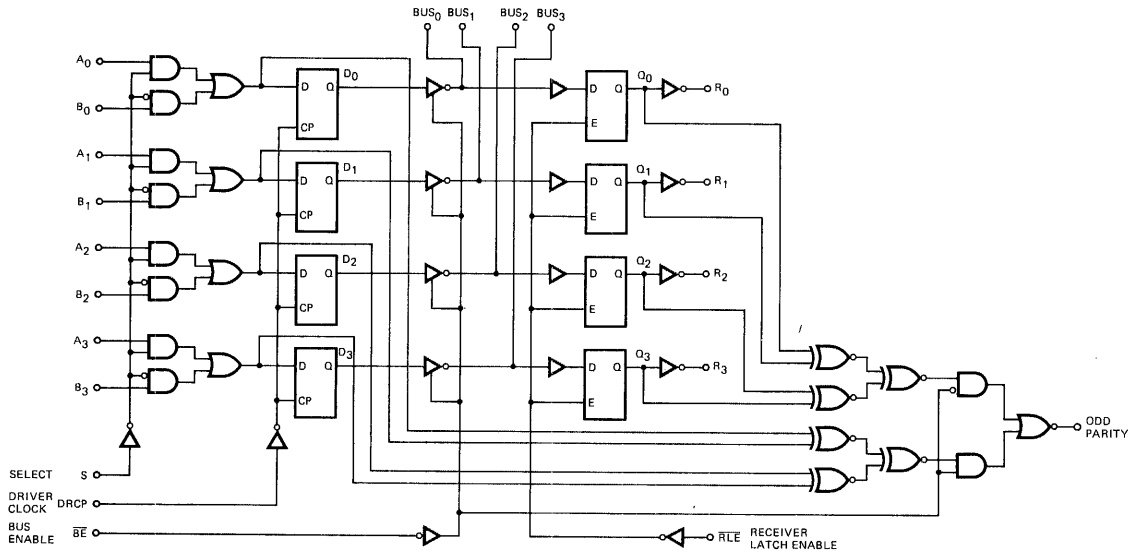
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-074

LOGIC DIAGRAM



MPR-075

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units.
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

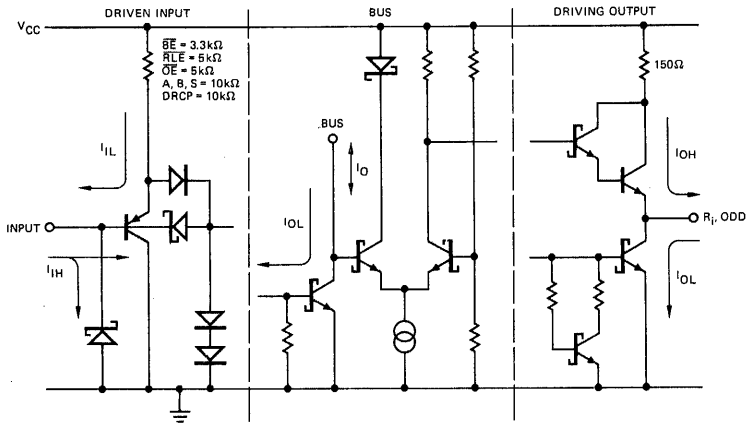
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}		$I_{OL} = 4mA$		0.27	0.4	Volts
				$I_{OL} = 8mA$		0.32	0.45	
				$I_{OL} = 12mA$		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	$C_L = 15pF$, $R_L = 2.0k\Omega$	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

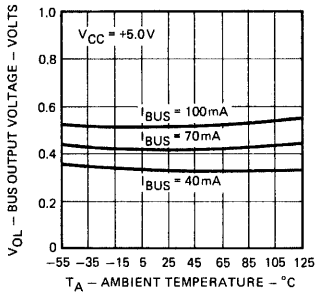


Note: Actual current flow direction shown.

MPR-076

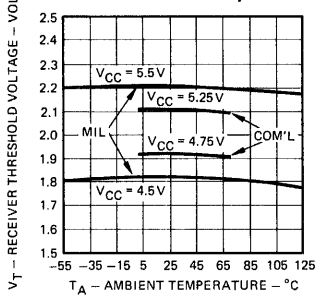
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



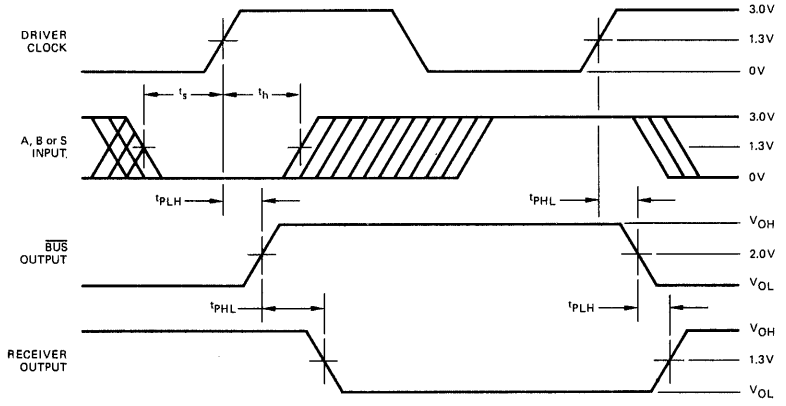
MPR-077

Receiver Threshold Variation Versus Ambient Temperature



MPR-078

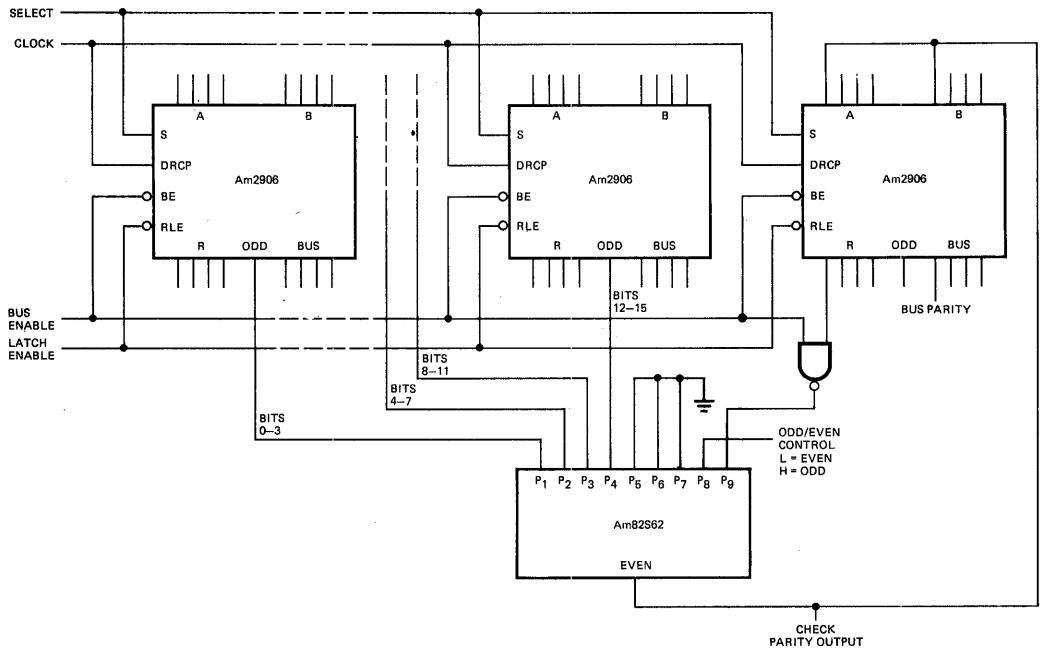
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-079

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-081

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	H	X	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2906PC	P-24	C	C-1
AM2906DC	D-24	C	C-1
AM2906DC-B	D-24	C	B-1
AM2906DM	D-24	M	C-3
AM2906DM-B	D-24	M	B-3
AM2906FM	F-24-1	M	C-3
AM2906FM-B	F-24-1	M	B-3
AM2906XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2906XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

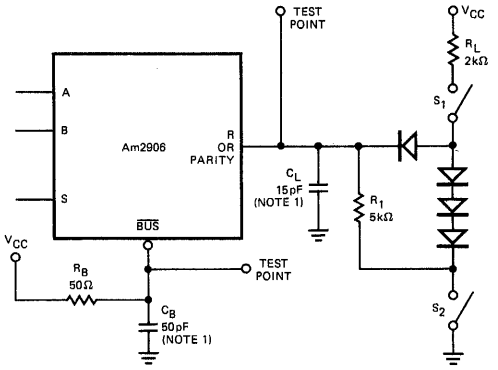
$\overline{BUS_0}$, $\overline{BUS_1}$, $\overline{BUS_2}$, $\overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

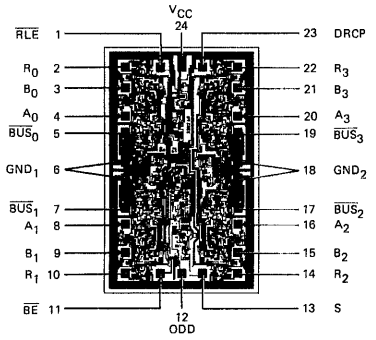
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



MPR-080

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

Am2907 • Am2908

Quad Bus Transceivers with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100mA at 0.8V max.
- Internal odd 4-bit parity checker/generator
- Am2907 has 2.0V input receiver threshold; Am2908 is "DEC Q or LSI-II bus compatible" with 1.5V receiver threshold
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced Low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

2

FUNCTIONAL DESCRIPTION

The Am2907 and Am2908 are high-performance bus transceivers intended for bipolar or MOS microprocessor system applications. The Am2908 is Digital Equipment Corporation "Q or LSI-II bus compatible" while the Am2907 features a 2.0V receiver threshold. These devices consist of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The devices also contain a four-bit odd parity checker/generator.

These LSI bus transceivers are fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

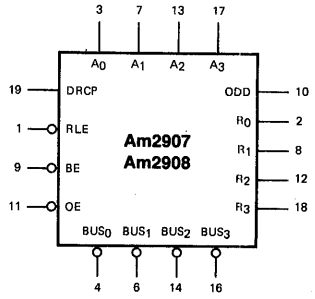
The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted form driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 and Am2908 feature a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

The Am2907 has receiver threshold typically of 2.0V while the Am2908 threshold is typically 1.5V.

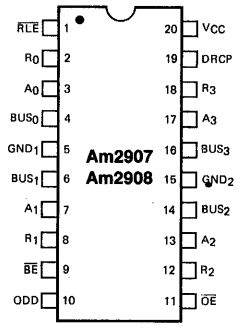
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

MPR-083

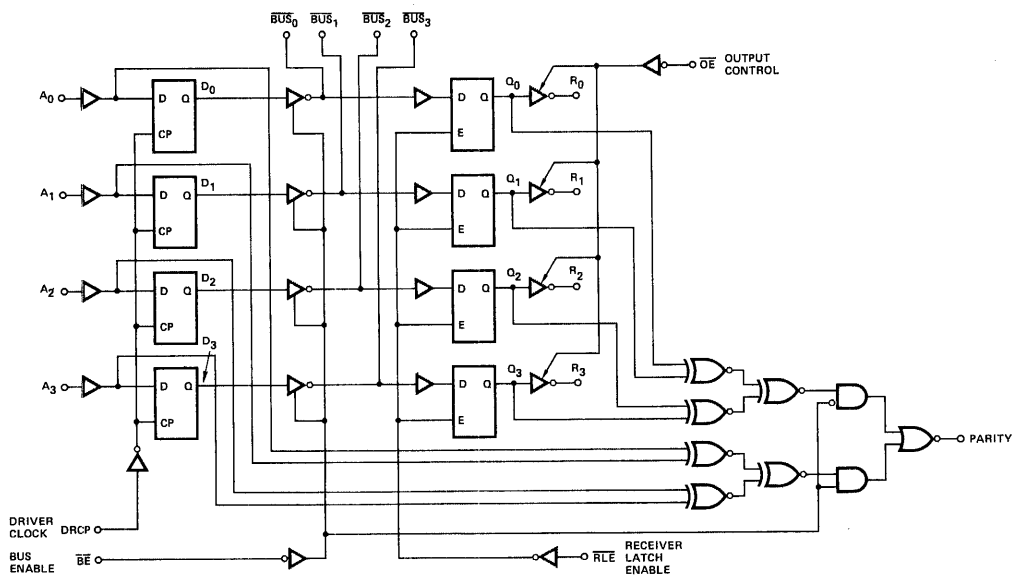
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-084

LOGIC DIAGRAM



MPR-085

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM, Am2908XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V	Am2907	MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
			Am2908	MIL	1.9	1.5		
				COM'L	1.7	1.5		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V	Am2907	MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	
			Am2908	MIL		1.5	1.1	
				COM'L		1.5	1.3	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

Am2907XM, Am2908XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1mA		2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA, V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND				75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	

Am2907 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs	C_L = 15pF, R_L = 2.0kΩ	18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2908 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2908XM Min.	Am2908XM Typ. (Note 2)	Am2908XM Max.	Am2908XC Min.	Am2908XC Typ. (Note 2)	Am2908XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF R_L(BUS): 91Ω to V_{CC} 200Ω to GND		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_r	Bus Output Rise Time		5	10		7	10		ns
t_f	Bus Output Fall Time		3	6		4	6		
t_s	Data Inputs		18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 50pF R_L = 2.0kΩ		18	38		18	35	ns
t_{PHL}				18	38		18	35	
t_{PLH}	Latch Enable to Receiver Output			21	38		21	35	ns
t_{PHL}				21	38		21	35	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)	C_L = 15pF R_L = 2.0kΩ		21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics fo the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

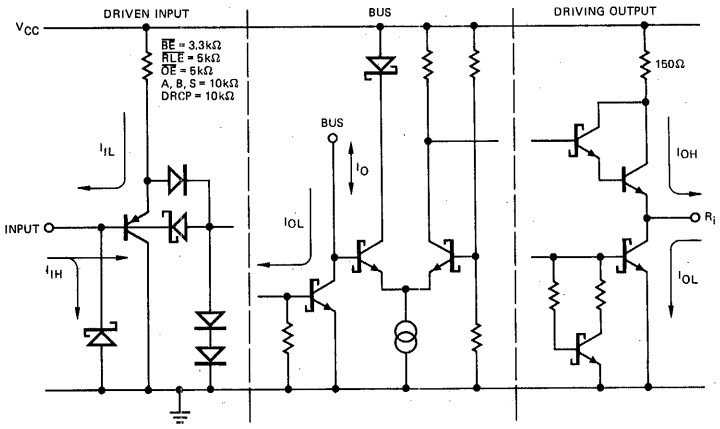
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2907 Order Number	Am2908 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2907PC	AM2908PC	P-20	C	C-1
AM2907DC	AM2908DC	D-20	C	C-1
AM2907DC-B	AM2908DC-B	D-20	C	B-1
AM2907DM	AM2908DM	D-20	M	C-3
AM2907DM-B	AM2908DM-B	D-20	M	B-3
AM2907FM	AM2908FM	F-20	M	C-3
AM2907FM-B	AM2908FM-B	F-20	M	B-3
AM2907XC	AM2908XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2907XM	AM2908XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C, Level B-3 conforms to MIL-STD-883, Class B.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

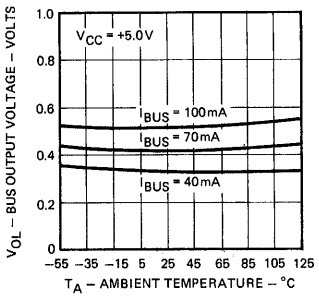


Note: Actual current flow direction shown.

MPR-086

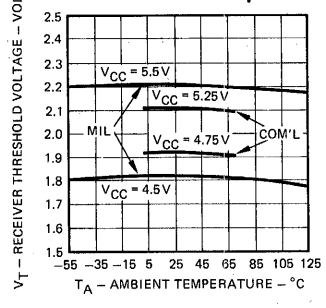
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



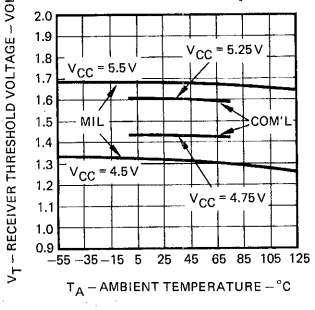
MPR-087

Am2907 Receiver Threshold Variation Versus Ambient Temperature



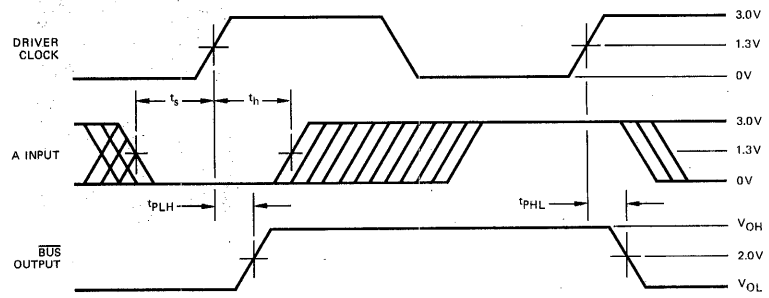
MPR-088

Am2908 Receiver Threshold Variation Versus Ambient Temperature



MPR-508

Am2907/08 SWITCHING WAVEFORMS



1. INPUT SET-UP AND HOLD TIMES.

MPR-089

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

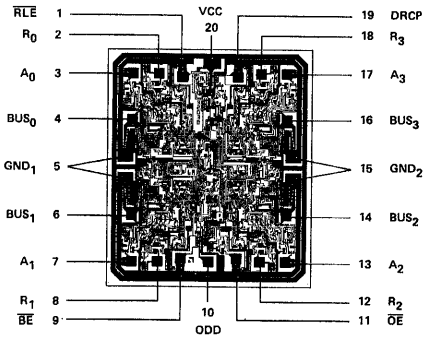
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

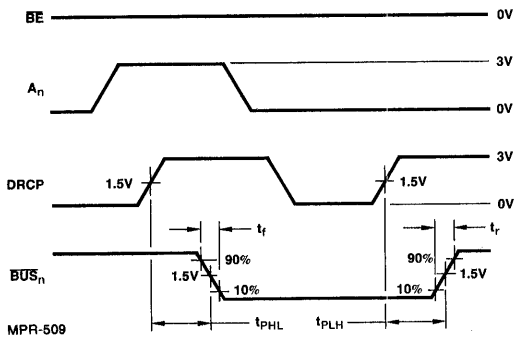
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Metallization and Pad Layout

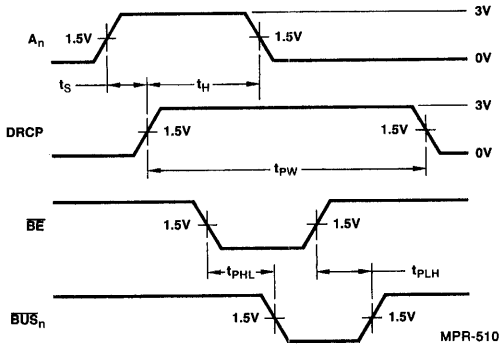


DIE SIZE 0.088" X 0.103"

Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS

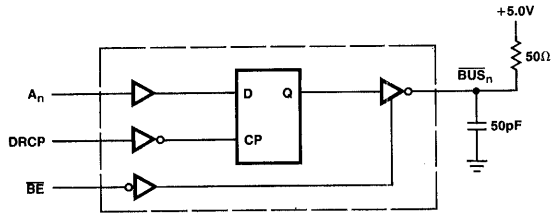


2. DRIVER CLOCK (DRCP) TO BUS

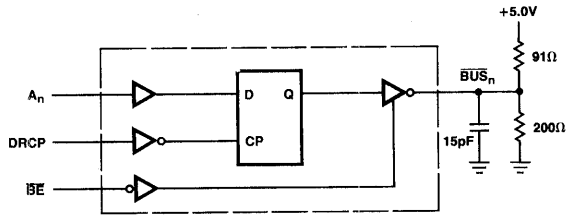


3. BUS ENABLE ($\overline{BE}$) TO BUS

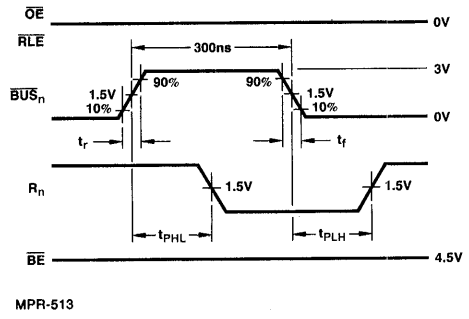
DRIVER SWITCHING WAVEFORMS



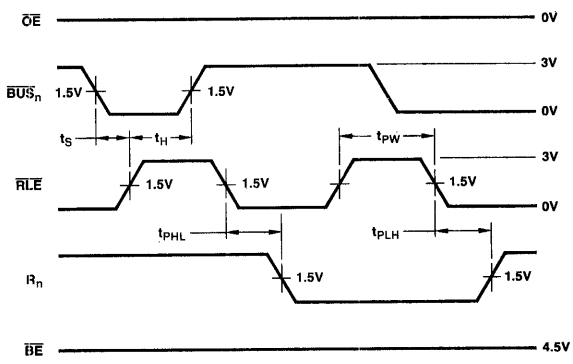
Am2907
DRIVER LOAD TEST CIRCUIT



Am2908
DRIVER LOAD TEST CIRCUIT

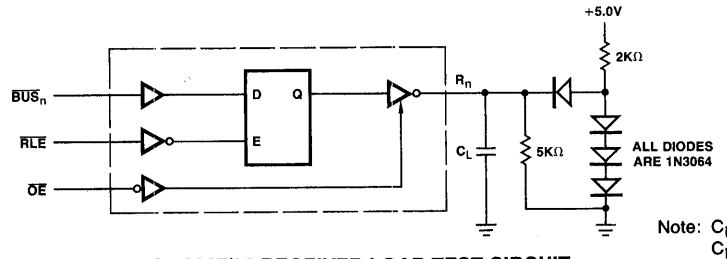


4. BUS TO RECEIVER OUTPUT (LATCH ENABLED)



5. LATCH ENABLE TO OUTPUT

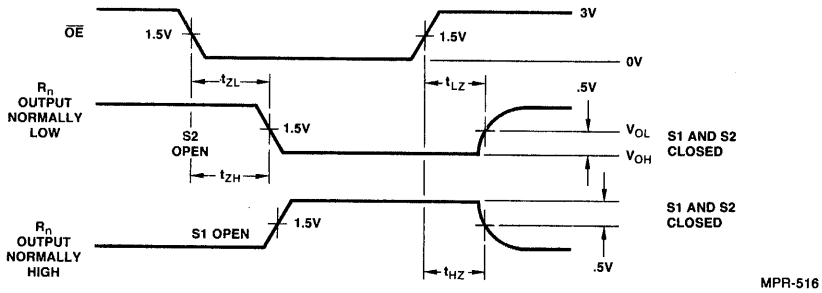
RECEIVER SWITCHING WAVEFORMS



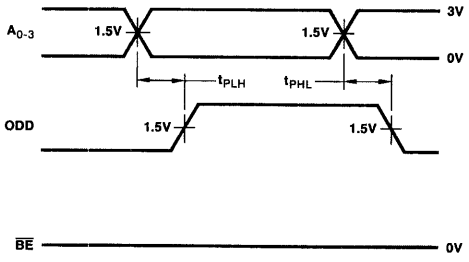
Note: C_L = 15pF for Am2907
C_L = 50pF for Am2908

Am2907/08 RECEIVER LOAD TEST CIRCUIT.

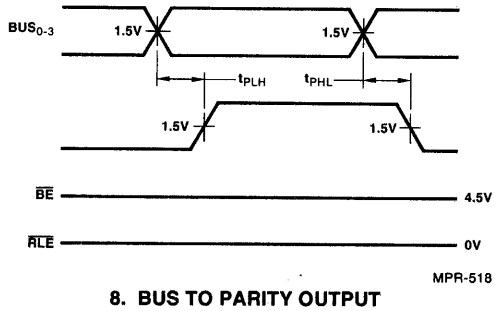
Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS (Cont.)



6. RECEIVER TRI-STATE WAVEFORMS

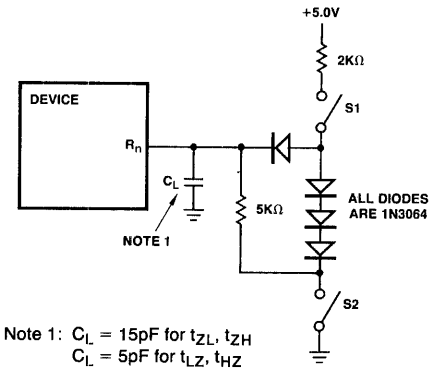


7. A INPUT TO PARITY OUTPUT

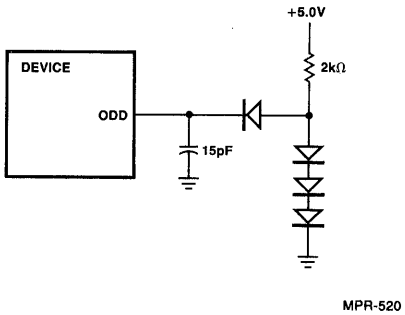


8. BUS TO PARITY OUTPUT

ODD PARITY OUTPUT WAVEFORMS

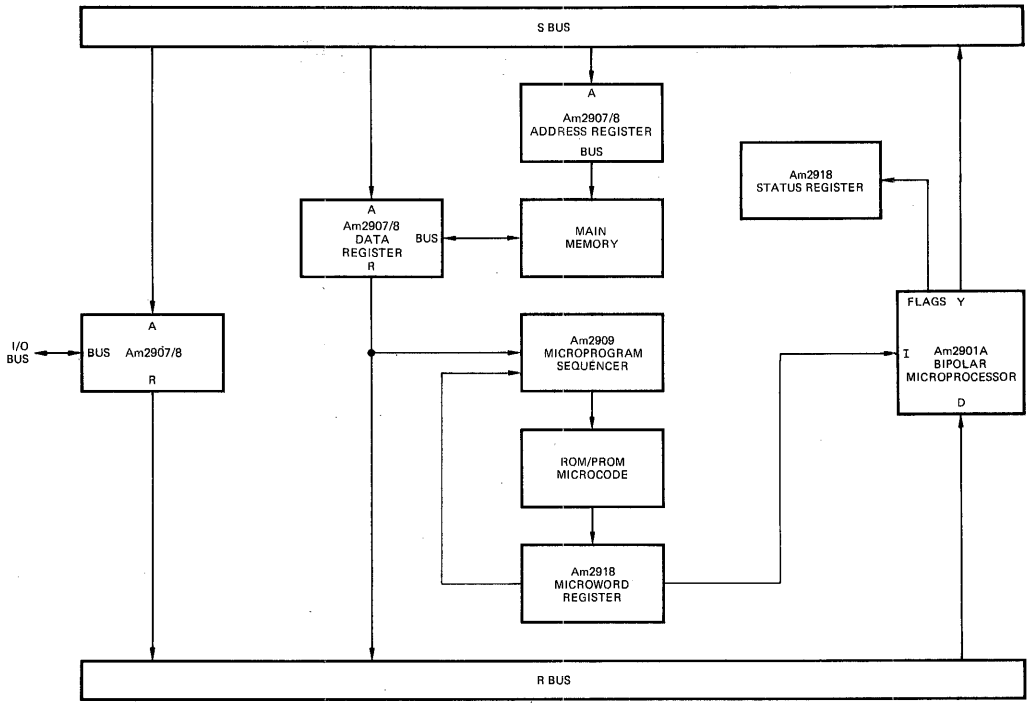


LOAD FOR RECEIVER TRI-STATE TEST



LOAD FOR PARITY OUTPUT

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

MPR-091

Am2909 • Am2911
Am2909A • Am2911A
Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only)
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package
- New high-speed versions (Am2909A and Am2911A) are plug-in replacements for original Am2909 and Am2911
- Critical path speeds will be improved by about 25%

GENERAL DESCRIPTION

The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

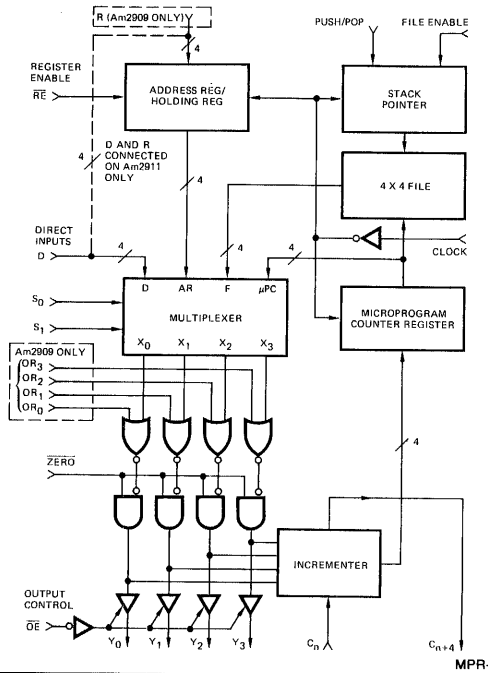
The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package. The Am2909A and Am2911A are direct plug-in replacements for the Am2909 and Am2911, but are about 25% faster.

TABLE OF CONTENTS

For applications information, see Chapter II of "Build a Microcomputer".

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



MPR-093

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

2

OPERATING RANGE

Operating Range	Part Number Suffix	Power Supply	Temperature Range
Commercial	PC, DC	5.0V ±5%	T_A = 0°C to +70°C
Military	DM, FM	5.0V ±10%	T_C = −55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Notes)

(For Am2909, Am2911, Am2909A, Am2911A)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA, 2909/11				0.4	Volts
			I_{OL} = 8.0mA, 2909/11				0.45	
			I_{OL} = 12mA, 2909/11 (Note 5)				0.5	
			I_{OL} = 16mA, 2909A/11A				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL, 2909/11				0.7	Volts
			All others				0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	μA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		$Y_0 - Y_3$	−30		−100	mA
				$C_n + 4$	−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)				80	130	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7V	V_{OUT} = 0.4V				−20	μA
I_{OZH}			V_{OUT} = 2.7V				20	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911 and Am2911A, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

Am2909 and Am2911 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II, and III below define the timing characteristics of the Am2909 and Am2911 over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e. clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	Am2909APC, DC Am2911APC, DC	5.0V ±5%	T_A = 0°C to +70°C
Mil	Am2909ADM, FM Am2911ADM	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

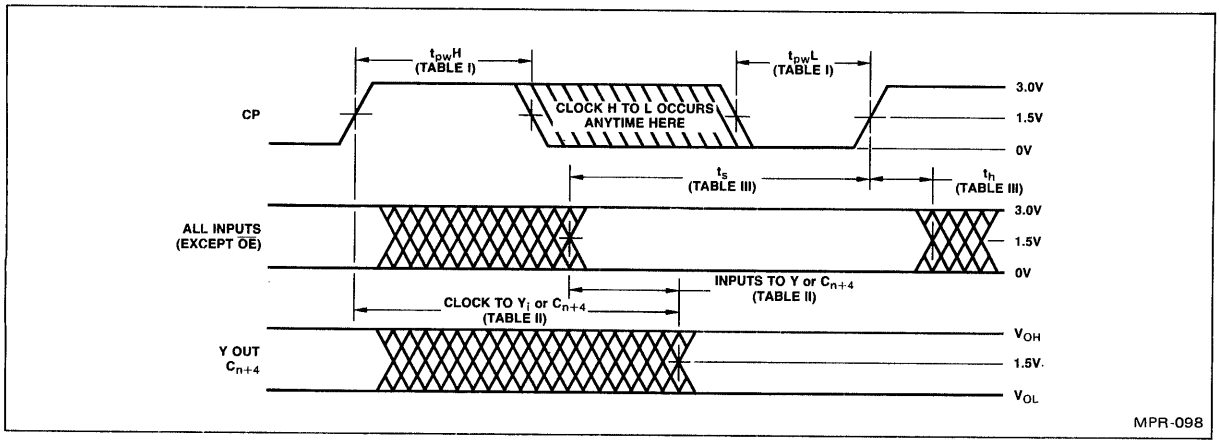
TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

From Input	COMMERCIAL		MILITARY	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	30	20	32
S_0, S_1	30	48	40	50
OR_i	17	30	20	32
C_n	–	14	–	16
$\overline{ZERO}$	30	48	40	50
$\overline{OE}$ LOW (enable)	25	–	25	–
$\overline{OE}$ HIGH (disable)	25	–	25	–
Clock ↑ S_1S_0 = LH	43	55	50	62
Clock ↑ S_1S_0 = LL	43	55	50	62
Clock ↑ S_1S_0 = HL	80	95	90	102

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
PUSH/POP		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		28	5	30	5
D_i	2	30	0	35	3
OR_i		30	0	35	3
S_0, S_1		45	0	50	0
$\overline{ZERO}$		45	0	50	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911A, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



Am2909A and Am2911A SWITCHING CHARACTERISTICS TYPICAL ROOM TEMPERATURE

Tables I, II and III below give typical timing characteristics of the Am2909A and Am2911A at room temperature. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	Am2909PC, DC Am2911PC, DC	5.0V ±5%	T_A = 0°C to +70°C
Mil	Am2909DM, FM Am2911DM	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

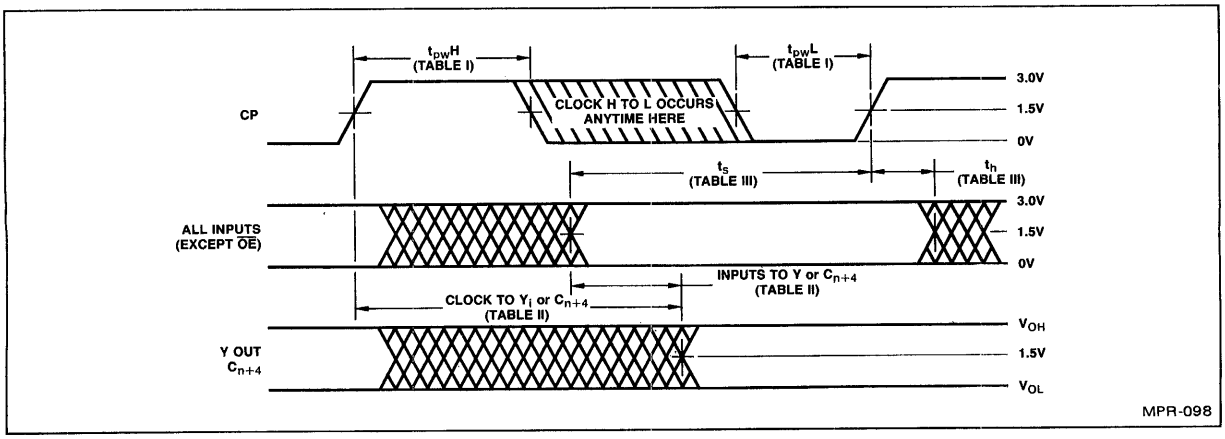
TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

From Input	TYPICAL ROOM TEMPERATURE Y	TYPICAL ROOM TEMPERATURE C_{n+4}	Y	C_{n+4}
D_i	10	10		
S_0, S_1	18	18		
OR_i	14	14		
C_n	–	9		
$\overline{ZERO}$	18	18		
$\overline{OE}$ LOW (enable)	13	–		–
$\overline{OE}$ HIGH (disable)	13	–		–
Clock ↑ S_1S_0 = LH	26	24		
Clock ↑ S_1S_0 = LL	26	24		
Clock ↑ S_1S_0 = HL	36	35		

TABLE III
SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	TYPICAL ROOM TEMPERATURE Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		9	0		
R_i	2	4	0		
PUSH/POP		11	0		
$\overline{FE}$		12	0		
C_n		8	0		
D_i	2	11	0		
OR_i		11	0		
S_0, S_1		15	0		
$\overline{ZERO}$		15	0		

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of Am2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

Y_i	Address outputs from Am2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
AR	Contents of the address/holding register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is perfc med. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

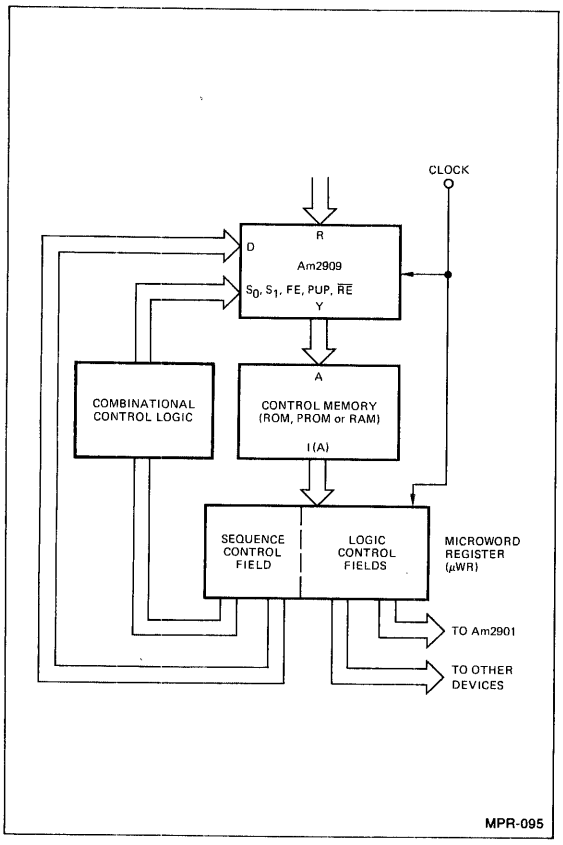


Figure 3. Microprogram Sequencer Control.

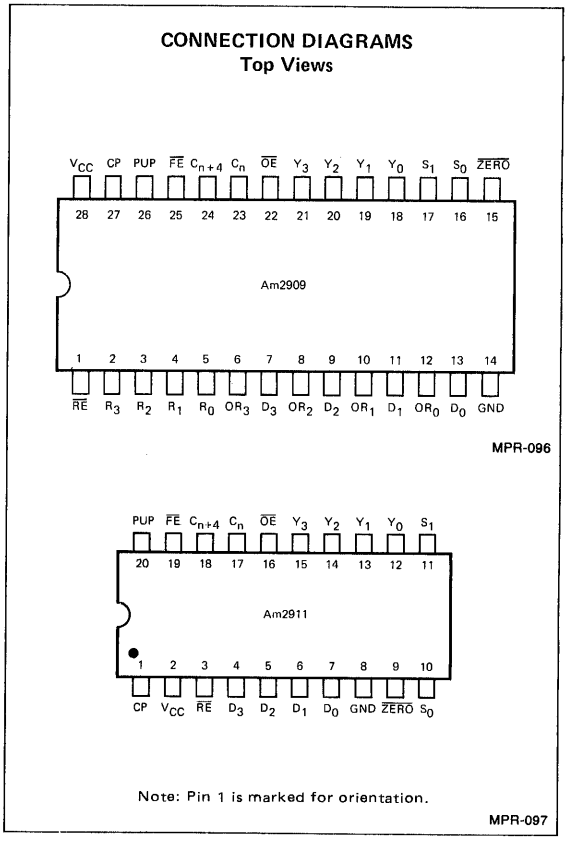


Figure 4.

OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Address/Holding Register	AR
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	0 0 0 0	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End Loop
N+1	–	J+1	K	Rb	Rc	Rd	Ra	–		
N	0 0 0 1	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up Loop
N+1	–	J+1	K	J	Ra	Rb	Rc	–		
N	0 0 1 X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N+1	–	J+1	K	Ra	Rb	Rc	Rd	–		
N	0 1 0 0	J	K	Ra	Rb	Rc	Rd	K	Pop Stack; Use AR for Address	End Loop
N+1	–	K+1	K	Rb	Rc	Rd	Ra	–		
N	0 1 0 1	J	K	Ra	Rb	Rc	Rd	K	Push μPC; Jump to Address in AR	JSR AR
N+1	–	K+1	K	J	Ra	Rb	Rc	–		
N	0 1 1 X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N+1	–	K+1	K	Ra	Rb	Rc	Rd	–		
N	1 0 0 0	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Pop Stack	RTS
N+1	–	Ra+1	K	Rb	Rc	Rd	Ra	–		
N	1 0 0 1	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Push μPC	
N+1	–	Ra+1	K	J	Ra	Rb	Rc	–		
N	1 0 1 X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref (Loop)
N+1	–	Ra+1	K	Ra	Rb	Rc	Rd	–		
N	1 1 0 0	J	K	Ra	Rb	Rc	Rd	D	Pop Stack; Jump to Address on D	End Loop
N+1	–	D+1	K	Rb	Rc	Rd	Ra	–		
N	1 1 0 1	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D; Push μPC	JSR D
N+1	–	D+1	K	J	Ra	Rb	Rc	–		
N	1 1 1 X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N+1	–	D+1	K	Ra	Rb	Rc	Rd	–		

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

Figure 7 illustrates the execution of a subroutine using the Am2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_6	J+3	–
T_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A+1	–
T_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution. C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_9	J+3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A+1	–
T_5	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
	–	–
	•	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH

USING THE Am2909 AND Am2911

The Am2909 and Am2911 are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909 and Am2911 apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909 or Am2911 should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on Am2910

Architecture of the Control Unit

The recommended architecture using the Am2909 or Am2911 is shown in Figure 1. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909 or Am2911. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.

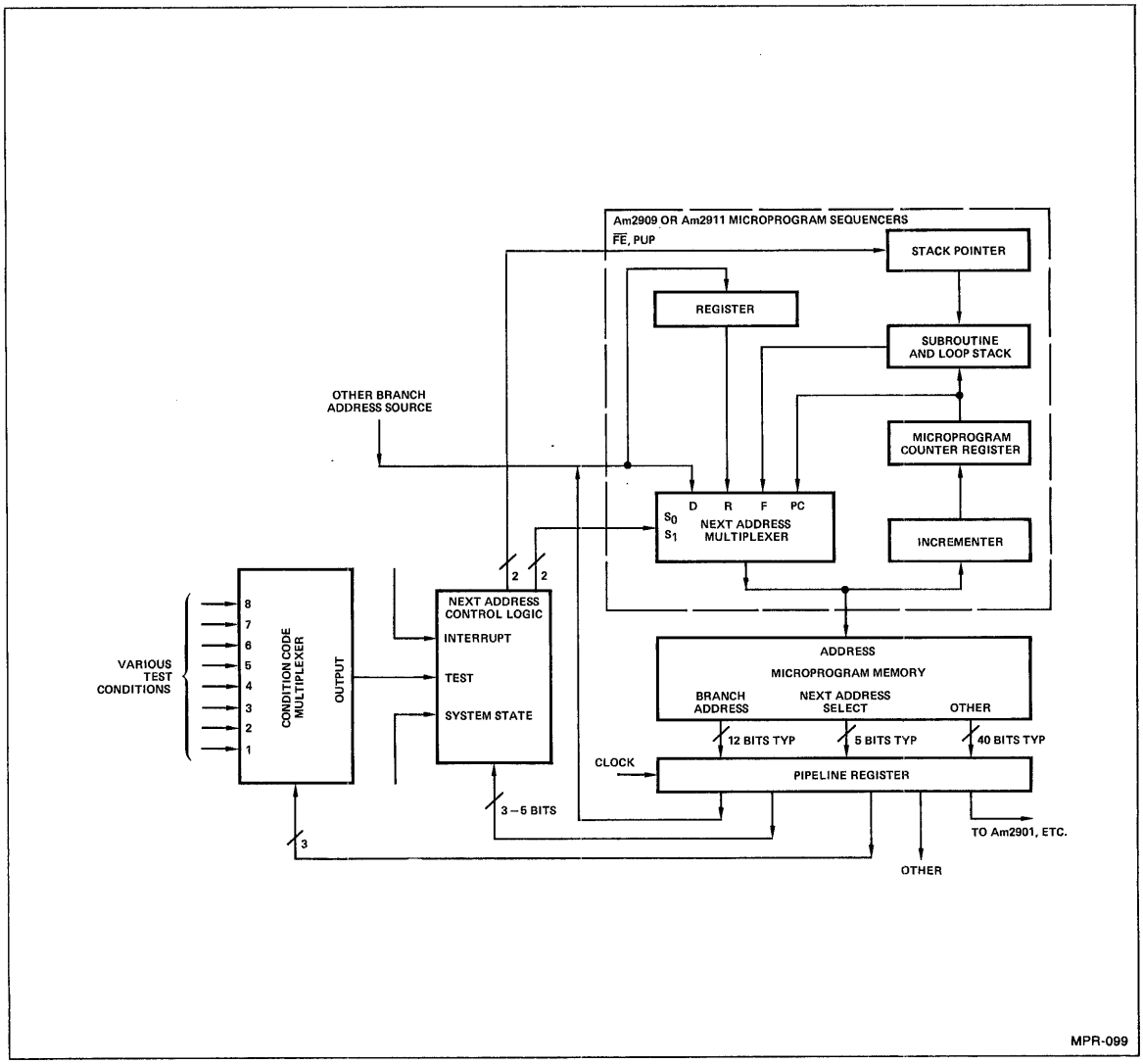


Figure 1. Recommended Computer Control Unit Architecture Using the Am2911 or Am2909.

The Am29811A is a combinational circuit which implements 16 sequence control instructions; it may be used with either an Am2909 or an Am2911. The set of instructions is nearly identical to that implemented internally in the Am2910.

Figure 2 shows the CCU of Figure 1 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911, also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 3, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

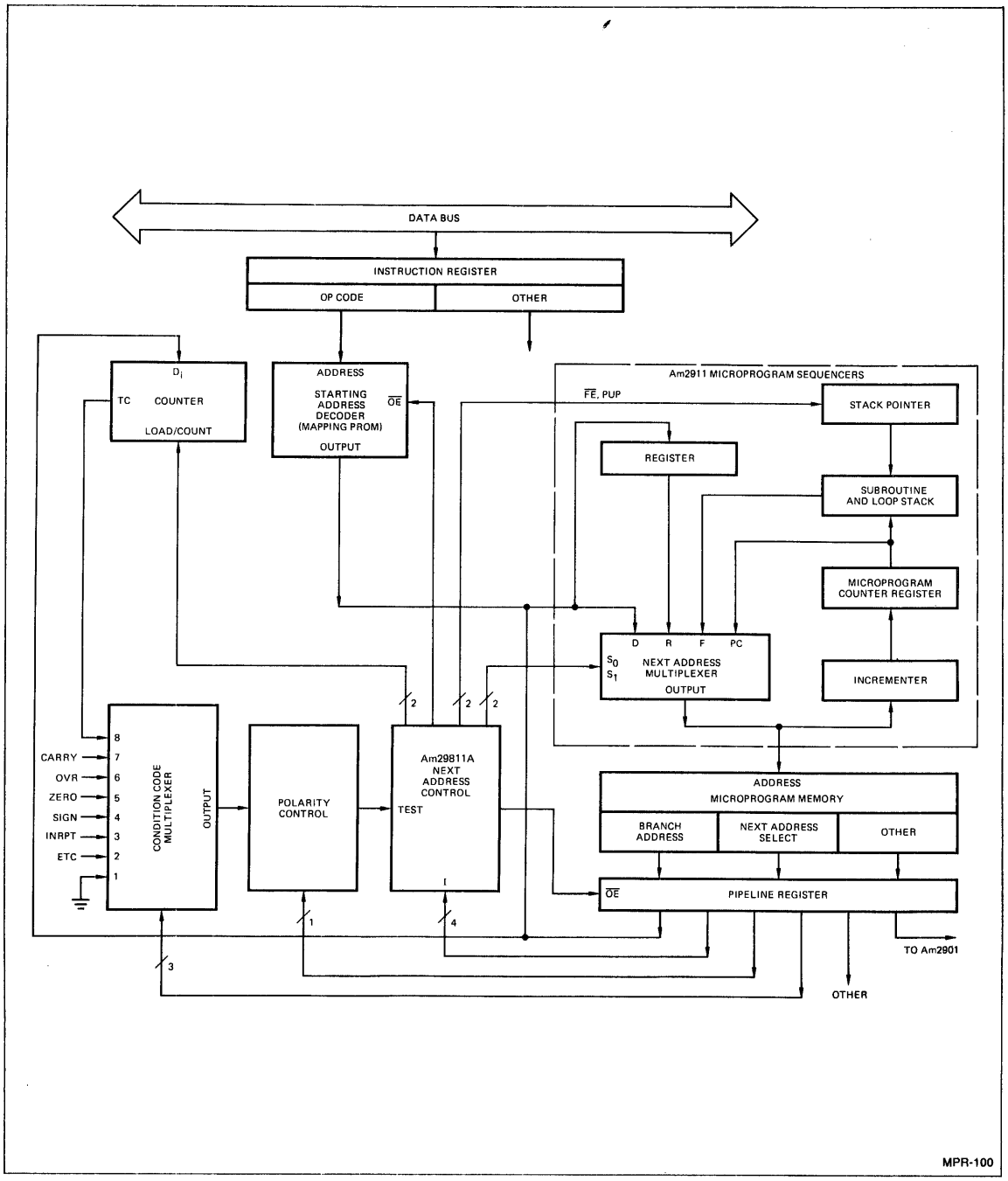


Figure 2. A Typical Computer Control Unit Using the Am2911 and Am29811A.

Am29811A FUNCTION TABLE

MNEMONIC	INPUTS: INSTRUCTION I_3 I_2 I_1 I_0	INPUTS: FUNCTION	INPUTS: TEST INPUT	OUTPUTS: NEXT ADDR SOURCE	OUTPUTS: FILE	OUTPUTS: COUNTER	OUTPUTS: MAP-E	OUTPUTS: PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	LL*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW
H = HIGH
X = Don't Care

DEC = Decrement
*LL = Special Case

Am29811A TRUTH TABLE

MNEMONIC	FUNCTION	INPUTS: I_3	I_2	I_1	I_0	TEST	OUTPUTS: NEXT ADDR SOURCE S_1	S_0	FILE $\overline{FE}$	PUP	COUNTER $\overline{LOAD}$	$\overline{EN}$	$\overline{MAP\ E}$	$\overline{PL\ E}$
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

Figure 3.

Expansion of the Am2909 or Am2911

Figure 4 shows the interconnection of three Am2911's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the Am2911 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911 output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the Am2909 and Am2911

The difference between the Am2909 and the Am2911 involves two signals: the data inputs to the holding register and the "OR" inputs. In the Am2909, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 5. Using the Am2909, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911, it is more common to connect the Am2911's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 5 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

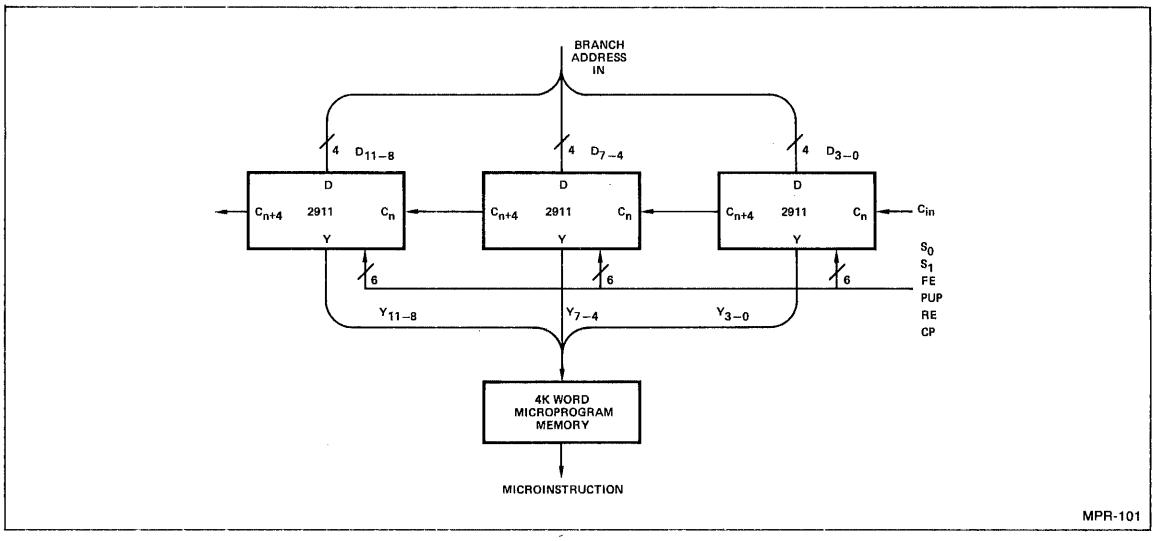


Figure 4. Twelve Bit Sequencer.

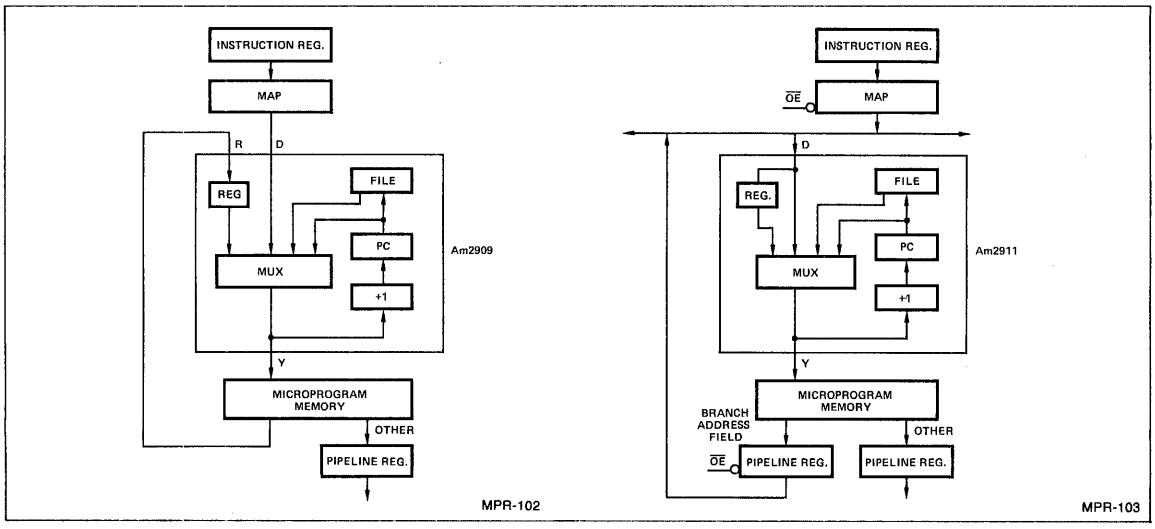


Figure 5. Branch Address Structures.

The second difference between the Am2909 and Am2911 is that the Am2909 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 6. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 6, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.

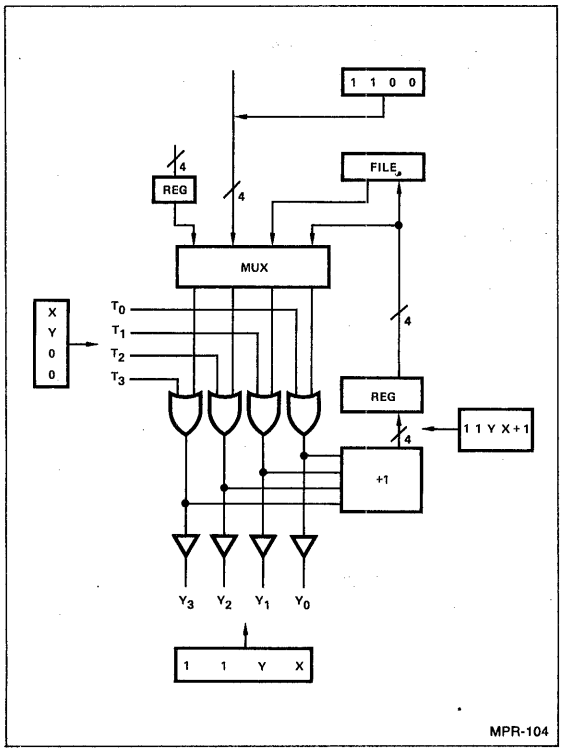


Figure 6. Use of OR Inputs to Obtain 4 - Way Branch.

The Am29803A has been designed to selectively apply any or all of four different test conditions to an Am2909. Figure 7 shows the truth table for this device. A nice trade off between flexibility and board space is achieved by using a single 28-pin Am2909 for the least significant four bits of a sequencer, and using the space-saving 20-pin Am2911's for the remainder of the bits. A detailed logic design for such a system is contained in The Microprogramming Handbook.

How to Perform Some Common Functions with the Am2909 or Am2911

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	1	0	0	1	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	1	1	1	1	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	1	1	1	0	1

Sub-routine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	1	1	0	0	0

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Am29803A FUNCTION TABLE

	BRANCH ON	I_3	I_2	I_1	I_0	OR_3	OR_2	OR_1	OR_0
NONE	NONE	L	L	L	L	L	L	L	L
Two-Way Branches	T_0	L	L	L	H	L	L	L	T_0
	T_1	L	L	H	L	L	L	L	T_1
	T_2	L	H	L	L	L	L	L	T_2
	T_3	H	L	L	L	L	L	L	T_3
Four-Way Branches	T_1 & T_0	L	L	H	H	L	L	T_1	T_0
	T_2 & T_0	L	H	L	H	L	L	T_2	T_0
	T_3 & T_0	H	L	L	H	L	L	T_3	T_0
	T_2 & T_1	L	H	H	L	L	L	T_2	T_1
	T_3 & T_1	H	L	H	L	L	L	T_3	T_1
	T_3 & T_2	H	H	L	L	L	L	T_3	T_2
Eight-Way Branches	T_2, T_1, T_0	L	H	H	H	L	T_2	T_1	T_0
	T_3, T_1, T_0	H	L	H	H	L	T_3	T_1	T_0
	T_3, T_2, T_0	H	H	L	H	L	T_3	T_2	T_0
	T_3, T_2, T_1,	H	H	H	L	L	T_3	T_2	T_1
Sixteen-Way Branch	T_3, T_2, T_1, T_0	H	H	H	H	T_3	T_2	T_1	T_0

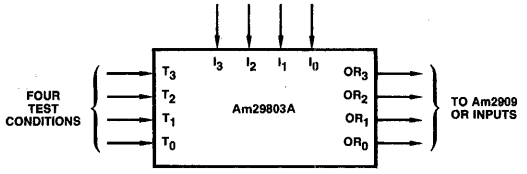
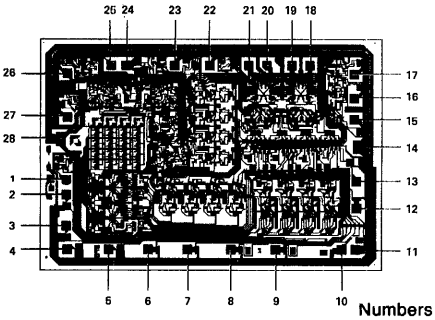


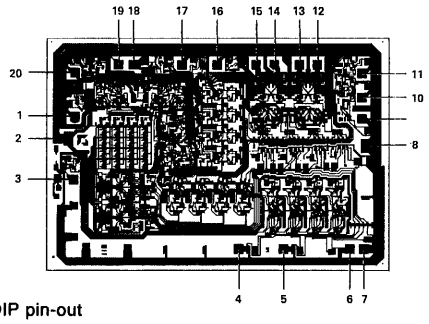
Figure 7.

Metallization and Pad Layouts

Am2909



Am2911



Numbers correspond to DIP pin-out

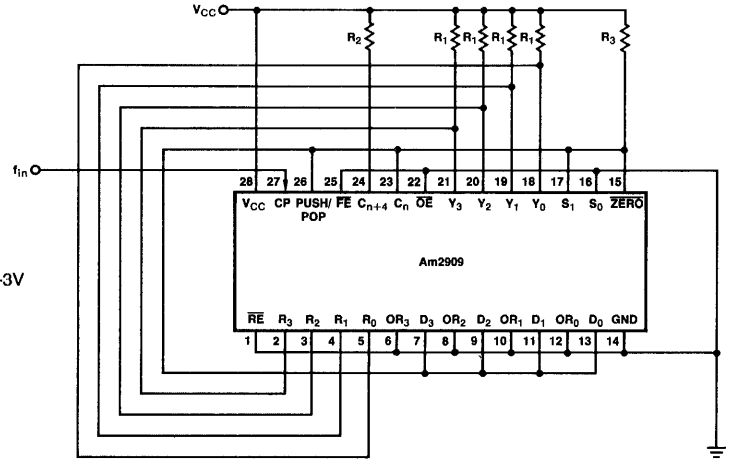
DIE SIZE 0.110" X 0.160"

Burn-in Circuit for Am2909 (Flatpack and Hermetic DIP)

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

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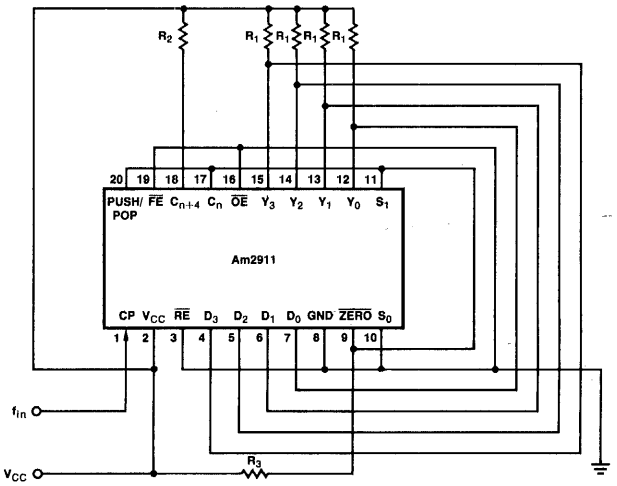
Burn-in Circuit for Am2911

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

From clock buffer on each board:
V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

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ARCHITECTURE OF THE Am2909/Am2911

The Am2909/Am2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage – the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

ORDERING INFORMATION

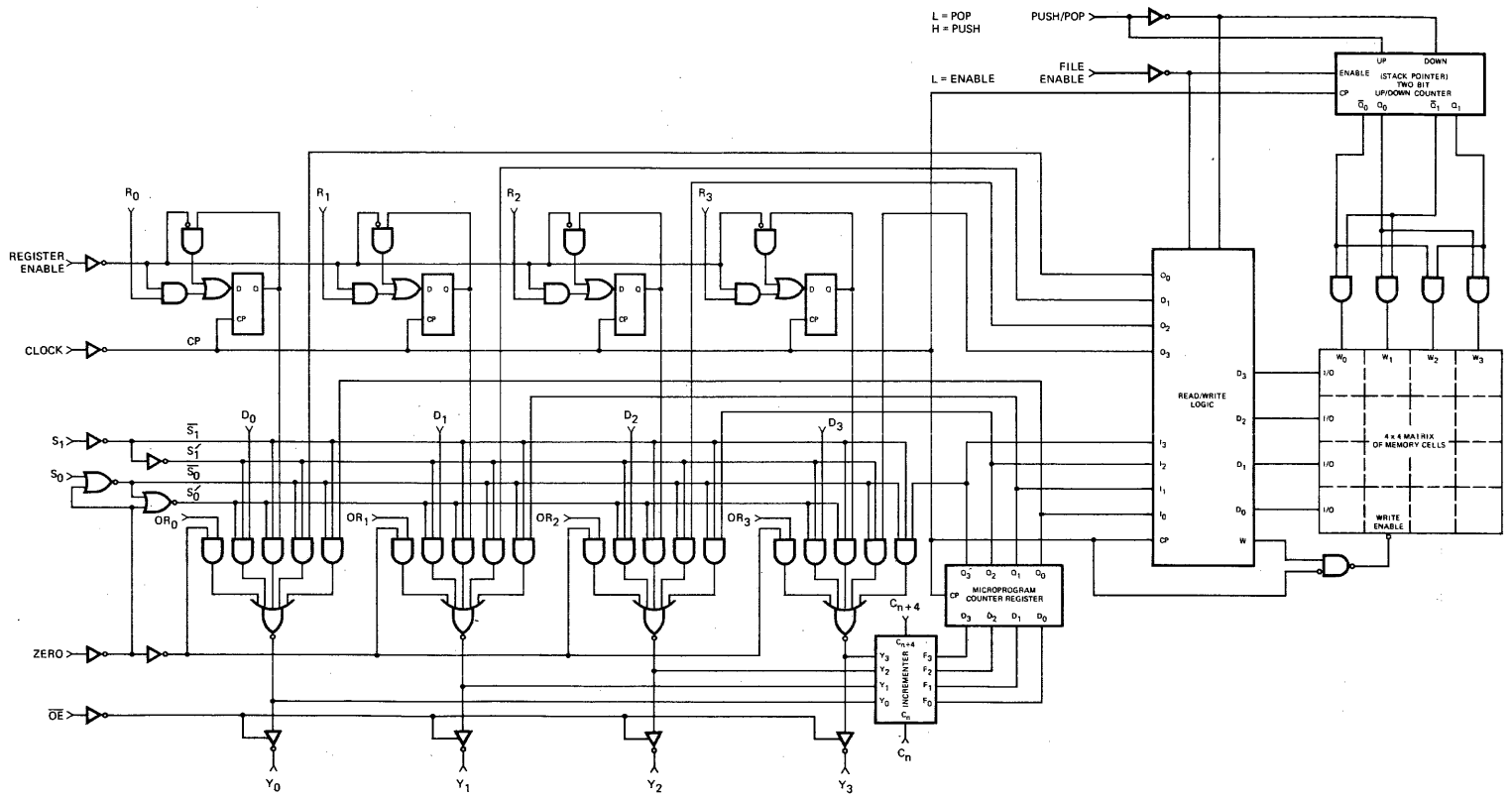
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2911 Order Number	Am2911A Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2911PC	AM2911APC	P-20	C	C-1
AM2911DC	AM2911ADC	D-20	C	C-1
AM2911DC-B	AM2911ADC-B	D-20	C	B-2 (Note 4)
AM2911DM	AM2911ADM	D-20	M	C-3
AM2911DM-B	AM2911ADM-B	D-20	M	B-3
AM2911XC	AM2911AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2911XM	AM2911AXM	Dice	M	

Am2909 Order Number	Am2909A Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2909PC	AM2909APC	P-28	C	C-1
AM2909DC	AM2909ADC	D-28	C	C-1
AM2909DC-B	AM2909ADC-B	D-28	C	B-2 (Note 4)
AM2909DM	AM2909ADM	D-28	M	C-3
AM2909DM-B	AM2909ADM-B	D-28	M	B-3
AM2909FM	AM2909AFM	F-28-1	M	C-3
AM2909FM-B	AM2909AFM-B	F-28-1	M	B-3
AM2909XC	AM2909AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2909XM	AM2909AXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hours of burn-in.

Figure 1.



Note: R_i and D_i connected together on Am2911 and OR_i removed.

Figure 2. Microprogram Sequencer Block Diagram.

MPR-094

Am2910
Microprogram Controller

DISTINCTIVE CHARACTERISTICS

- Twelve Bits Wide
  Address up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.
- Internal Loop Counter
  Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- Four Address Sources
  Microprogram Address may be selected from microprogram counter, branch address bus, 5-level push/pop stack, or internal holding register.
- Sixteen Powerful Microinstructions
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- Output Enable Controls for Three Branch Address Sources
  Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- All Registers Positive Edge-triggered
  Simplifies timing problems. Eliminates long set-up times.
- Fast Control from Condition Input
  Delay from condition code input to address output only 21ns typical.

GENERAL DESCRIPTION

The Am2910 Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

During each microinstruction, the Microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a five-deep last-in, first-out stack (F).

For a detailed discussion of this architectural approach to microprogram control units, refer to "The Microprogramming Handbook", an AMD applications publication.

Am2910 BLOCK DIAGRAM

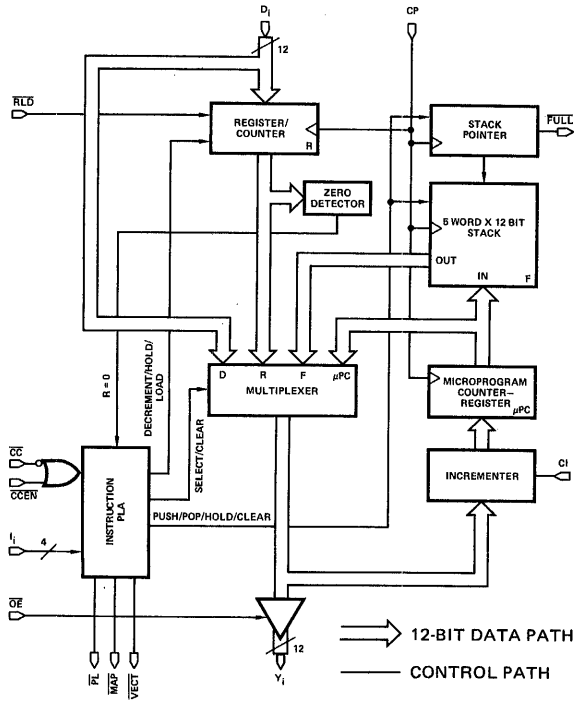


Figure 1.

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For applications information, see Chapter II of "Build a Microcomputer".

ARCHITECTURE OF THE Am2910

The Am2910 is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in Figure 1.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is LOW, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The Am2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 1, 4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes LOW. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8, 9, 15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N+1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table I shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$ is LOW. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic

Several inputs, as shown in Table II, can modify instruction execution. The combination $\overline{CC}$ HIGH and $\overline{CCEN}$ LOW is used as a test in 9 of the 16 instructions. $\overline{RLD}$, when LOW, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally LOW, may be forced HIGH to remove the Am2910 Y outputs from a three-state bus.

The stack, a five-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

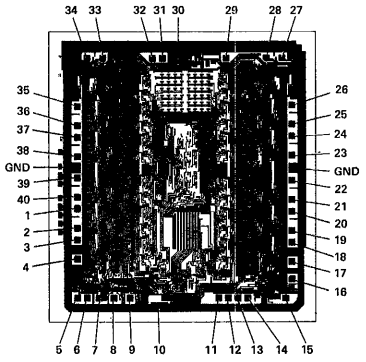
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2910PC	P-40	C	C-1
AM2910DC	D-40	C	C-1
AM2910DC-B	D-40	C	B-2 (Note 4)
AM2910DM	D-40	M	C-3
AM2910DM-B	D-40	M	B-3
AM2910FM	F-42	M	C-3
AM2910FM-B	F-42	M	B-3
AM2910XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2910XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

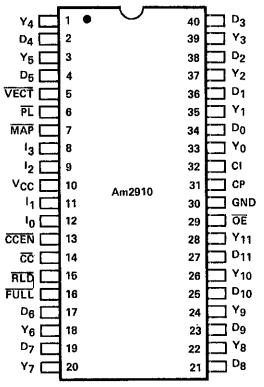
Metallization and Pad Layout



Die Size 0.170" x 0.194"
(Note: Numbers refer to DIP connections)

CONNECTION DIAGRAMS — Top Views

DIP



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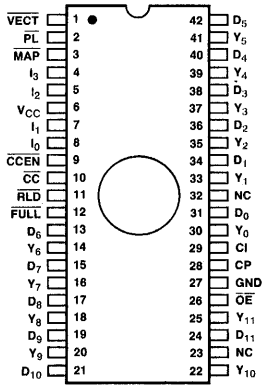
Flat Package



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Pin 1 is marked for orientation.

TABLE I. INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CONTENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠0	F	HOLD	F	HOLD	DEC	PL
			=0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠0	D	HOLD	D	HOLD	DEC	PL
			=0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠0	F	HOLD	PC	POP	DEC	PL
			=0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

TABLE II. PIN FUNCTIONS

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB
I_i	Instruction Bit i	Selects one-of-sixteen instructions for the Am2910
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge
V_{CC}	+5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB
$\overline{FULL}$	Full	Indicates that five items are on the stack
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.6mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12mA			0.5	Volts
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-11}			−0.87	mA
			CI, $\overline{CCEN}$			−0.54	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			−0.72	
			$\overline{CC}$			−1.31	
			CP			−2.14	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-11}			80	µA
			CI, $\overline{CCEN}$			30	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			40	
			$\overline{CC}$			50	
			CP			100	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V			−50	µA
I_{OZH}			V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current	V_{CC} = MAX.	T_A = 25°C		195	320	mA
		Am2910PC, DC	T_A = 0°C to +70°C			344	
			T_A = +70°C			280	
		Am2910DM, FM	T_C = −55°C to +125°C			340	
			T_C = +125°C			227	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.

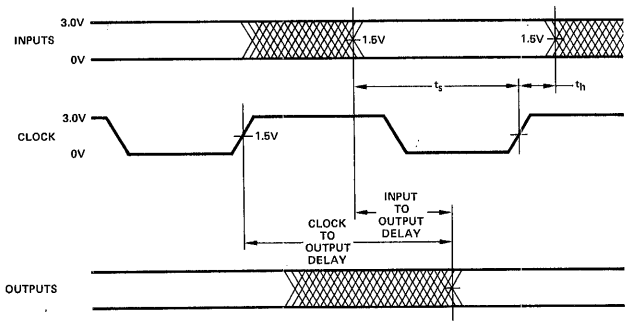

Figure 2. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs. See Figure 5 for timing of a typical CCU cycle.

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Am2910 SWITCHING CHARACTERISTICS

The tables below define the Am2910 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$	9	4
$D_i \rightarrow PC$	34	3
I_0-I_3	64	0
$\overline{CC}$	46	0
$\overline{CCEN}$	49	0
CI	26	2
$\overline{RLD}$	18	2

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	14	–	–
I_0-I_3	40	27	–
$\overline{CC}$	21	–	–
$\overline{CCEN}$	23	–	–
CP (Note 2) I = 8, 9, 15	54	–	29
	79	–	29
CP All other I	26	–	29
$\overline{OE}$ (Note 3)	25/24	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	74	ns
	99	
Minimum Clock Period, I=14	60	ns

II. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2910PC,DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$	24	6
$D_i \rightarrow PC$	58	4
I_0-I_3	104	0
$\overline{CC}$	80	0
$\overline{CCEN}$	80	0
CI	46	5
$\overline{RLD}$	36	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	20	–	–
I_0-I_3	70	51	–
$\overline{CC}$	43	–	–
$\overline{CCEN}$	45	–	–
CP (Note 2) I = 8, 9, 15	100	–	60
	125	–	60
CP All other I	55	–	60
$\overline{OE}$ (Note 3)	35/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	50	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	138	ns
	163	
Minimum Clock Period, I=14	93	ns

III. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2910DM,FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$	28	6
$D_i \rightarrow PC$	62	4
I_0-I_3	110	0
$\overline{CC}$	86	0
$\overline{CCEN}$	86	0
CI	58	5
$\overline{RLD}$	42	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	25	–	–
I_0-I_3	75	58	–
$\overline{CC}$	48	–	–
$\overline{CCEN}$	50	–	–
CP (Note 2) I = 8, 9, 15	106	–	67
	130	–	67
CP All other I	61	–	67
$\overline{OE}$ (Note 3)	40/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	58	ns
Minimum Clock HIGH Time	42	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	143	ns
	167	
Minimum Clock Period, I=14	100	ns

NOTES:
1. Clock periods for instructions not specified are determined by external conditions.
2. These instructions are conditional on the counter. Use the shorter specified delay times if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.
3. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF.

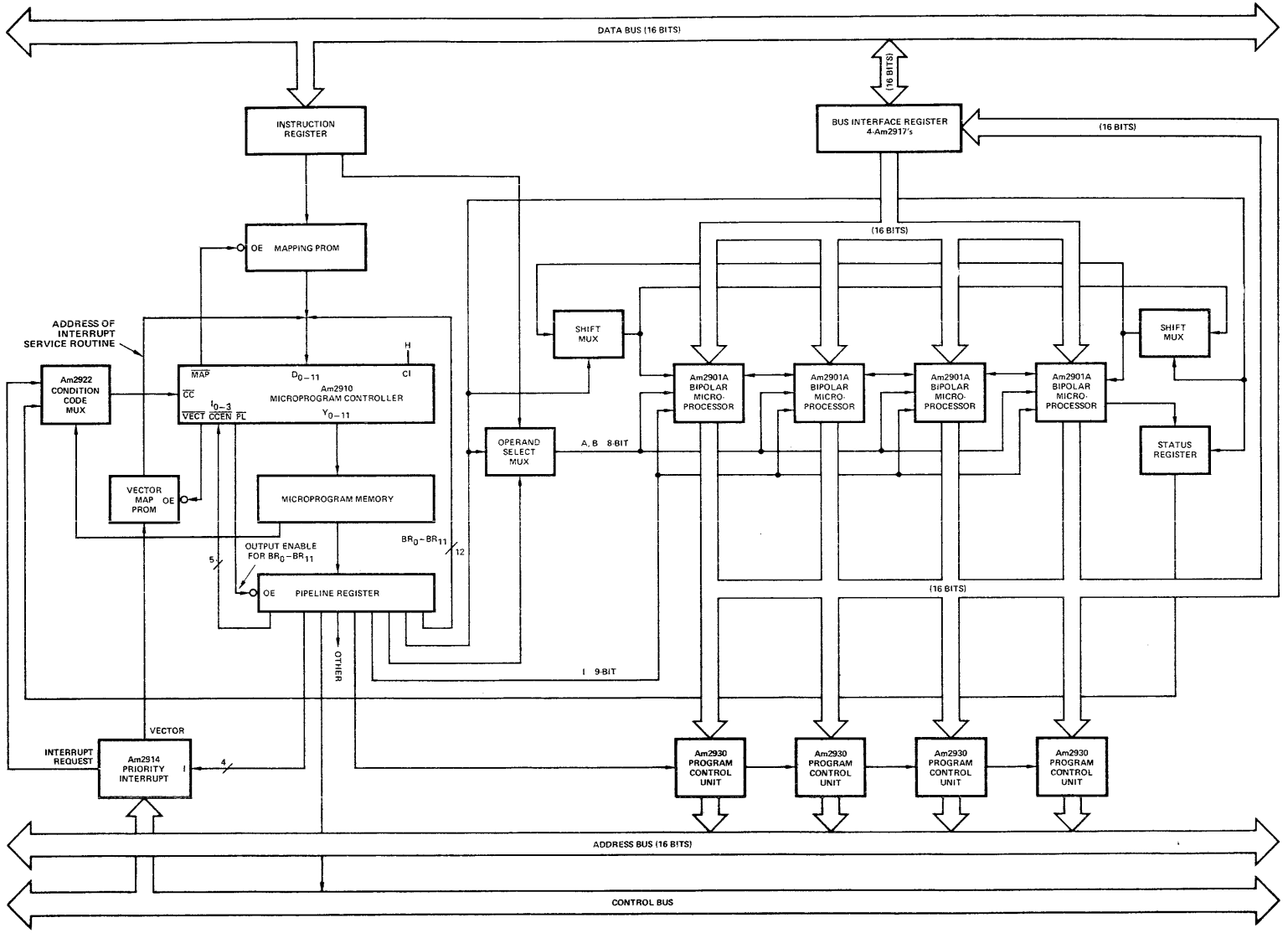

Figure 3. Typical Bipolar Microcomputer Using Am2910.

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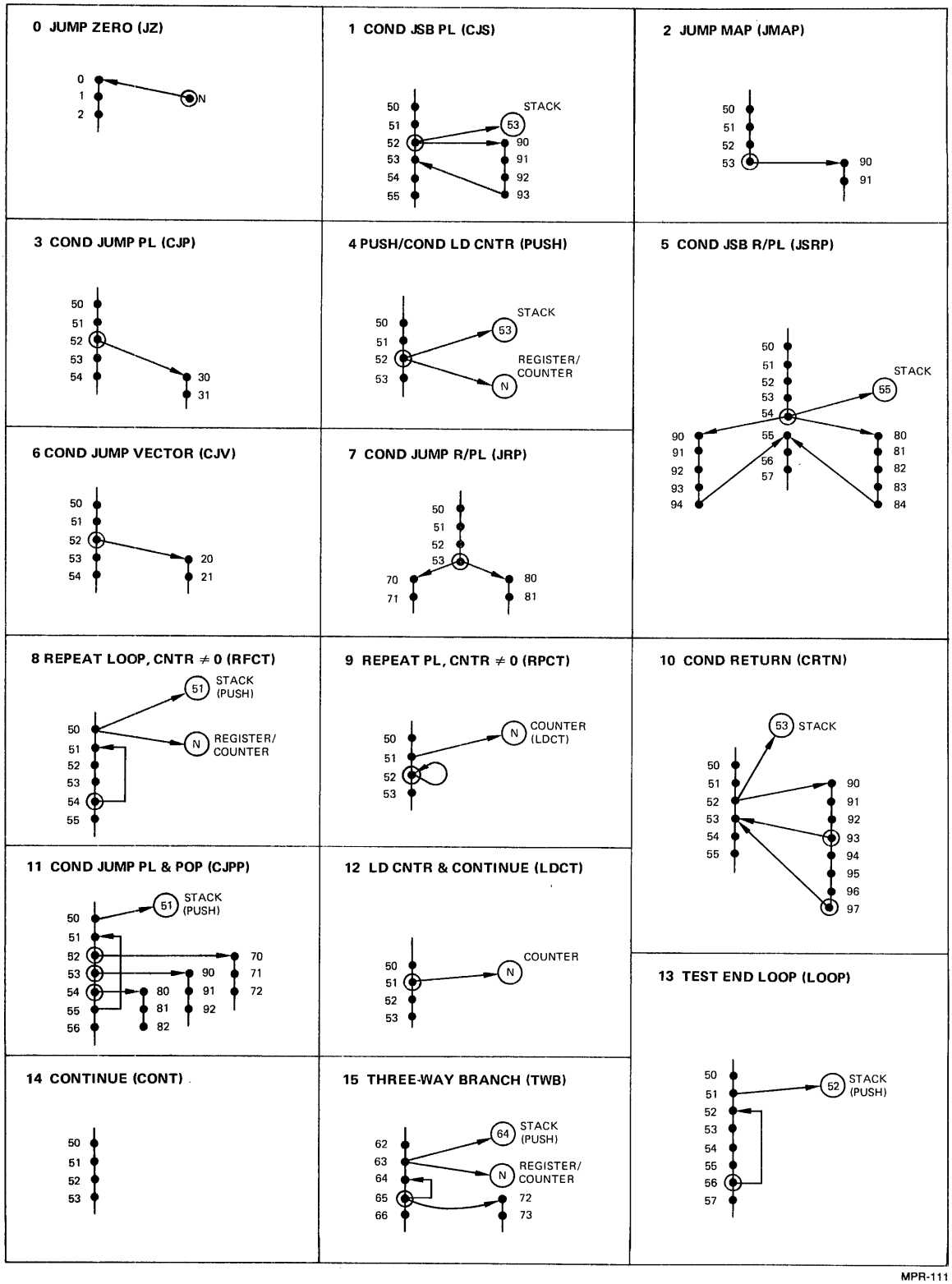

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Figure 4. Am2910 Execution Examples.

THE Am2910 INSTRUCTION SET

The Am2910 provides 16 instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional – their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table I. In this discussion it is assumed that C_n is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of Am2910 instruction bit I_0, which leaves instructions 4, 6, and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the Am2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, Figure 4 is included and depicts examples of all 16 instructions.

The examples given in Figure 4 should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, as shown in Figure 4, simply means that the contents of microprogram memory word 50 is executed, then the contents of word 51 is executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the text to follow will explain what the conditional choices are in each example.

It might be appropriate at this time to mention that AMD has a microprogram assembler called AMDASM, which has the capability of using the Am2910 instructions in symbolic representation. AMDASM's Am2910 instruction symbolics (or mnemonics) are given in Figure 4 for each instruction and are also shown in Table I.

Instruction 0, JZ (JUMP and ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. As shown in Figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure 4, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value (BR_0 – BR_{11} in Figure 2). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. Figure 4 shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (3) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In Figure 4, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will

THE Am2910 INSTRUCTION SET (Cont.)

describe how to use the pushed value and the register/counter for looping.

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown in Figure 4, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the Am2910 register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the Am2910 output, $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example of Figure 4, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

Instruction 7 is a CONDITIONAL JUMP via the contents of the Am2910 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the conditional jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7. Figure 4 depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the Am2910. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

An example of the REPEAT LOOP, COUNTER ≠ ZERO instruction is shown in Figure 4. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In the example of Figure 4, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multiinstruction loops can be performed in this manner for a fixed number of times as determined by the counter.

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example in Figure 4 depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force

THE Am2910 INSTRUCTION SET (Cont.)

$\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example in Figure 4 shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter – the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of the $\overline{RLD}$ input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example in Figure 4 shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POP'd; thus, accomplishing the required stack maintenance.

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

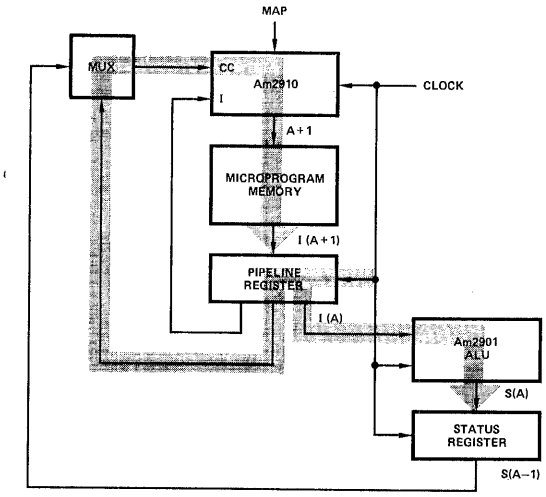
As one example, consider the case of a memory search instruction. As shown in Figure 4, the instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once, removing the value 64 from the top of the stack.

ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

Figure 5.

One Level Pipeline Based
(Recommended)



One level pipeline provides better speed than most other architectures. The μProgram Memory and the Am2901 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs.

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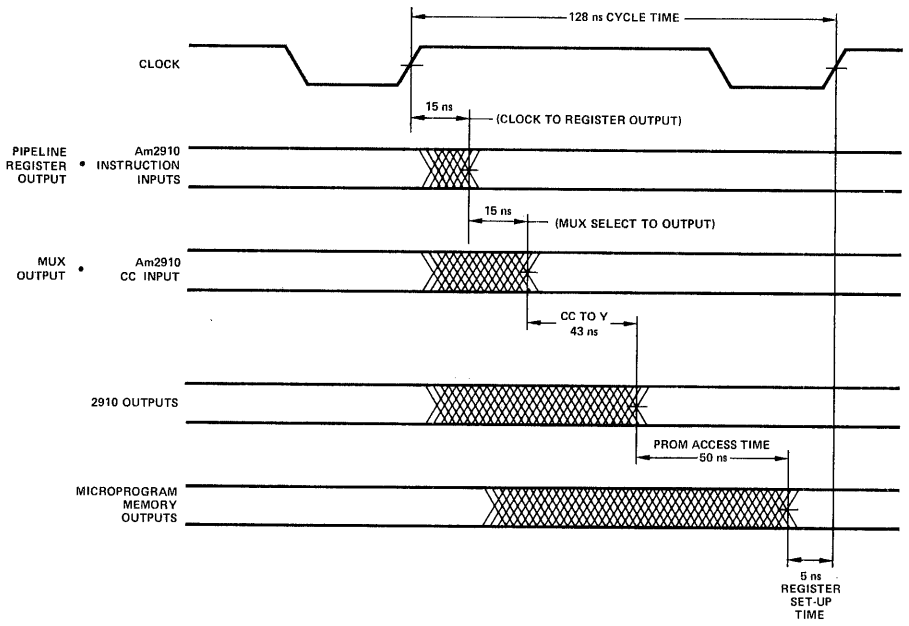

Typical CCU Cycle Timing Waveforms.

This drawing shows the timing relationships in the CCU illustrated above.

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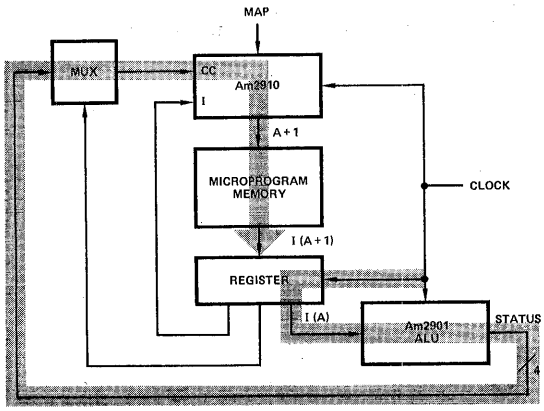
OTHER ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

Figure 6.

A. Instruction Based



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2901 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

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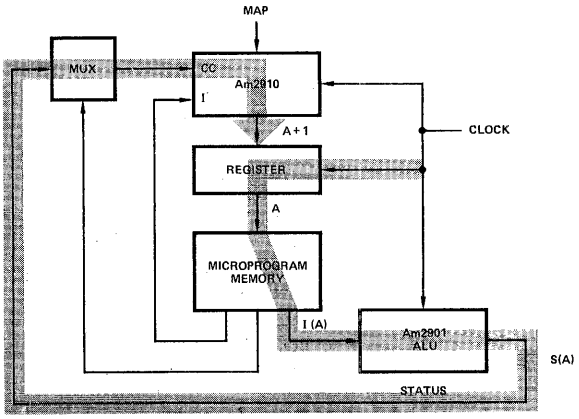
B. Addressed Based



The Register at the Am2910 output contains the address of the microinstruction being executed. The Microprogram Memory and Am2901 are in series in the critical path. This architecture provides about the same speed as the Instruction based architecture, but requires fewer register bits, since only the address (typically 10-12 bits) is stored instead of the instruction (typically 40-60 bits).

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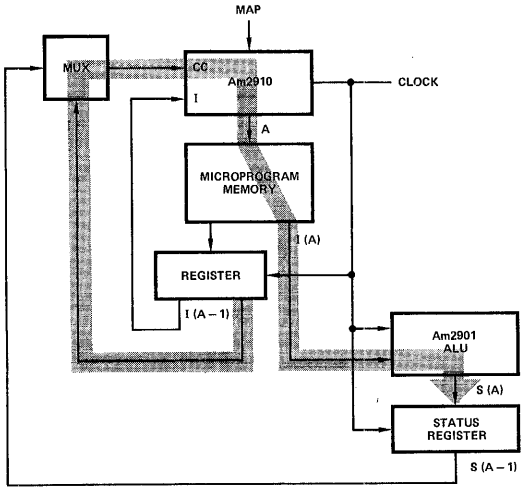
C. Data Based



The Status Register provides conditional Branch control based on results of previous ALU cycle. The Microprogram Memory and Am2901 are in series in the critical paths.

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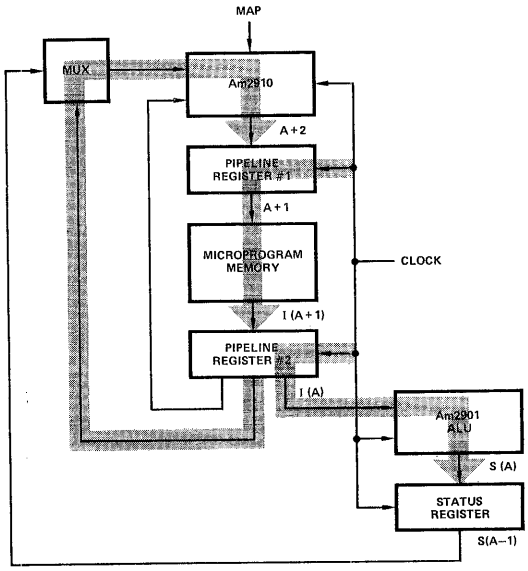
D. Two Level Pipeline Based



Two level pipeline provides highest possible speed. It is more difficult to program because the selection of a microinstruction occurs two instructions ahead of its execution.

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Am2912
Quad Bus Transceiver

Distinctive Characteristics

- Input to bus is inverting
- Quad high-speed open collector bus transceiver
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

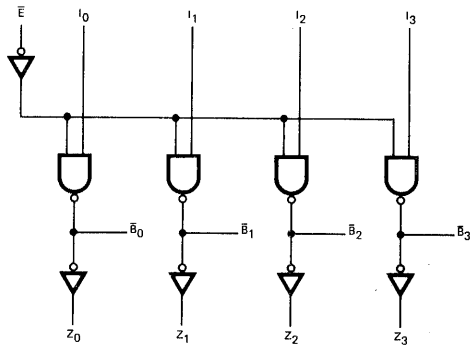
The Am2912 is a quad Bus Transceiver consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

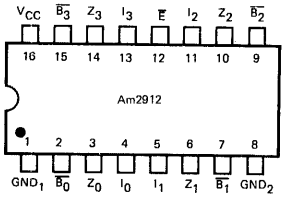
The Am2912 features advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

LOGIC DIAGRAM



BLI-061

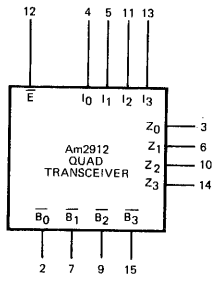
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-062

LOGIC SYMBOL



V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

BLI-063

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7V
DC Voltage Applied to Outputs for High Output State	–0.5V to +V_{CC} max.
DC Input Voltage	–0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	–30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

2

Am2912PC, DC, XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2912DM, FM, XM T_A = –55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OH} = –1.0mA, V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = –18mA				–1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			–0.36	mA
			Data			–0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	µA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	–20		–55	mA
			COM'L	–18		–60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX., Enable = GND			45	70	mA

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			–50	µA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50pF (Note 1)		10	15	ns
t_{PHL}				10	15	
t_{PLH}	Enable Input to Bus			14	18	ns
t_{PHL}				13	18	
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}				10	15	
t_r	Bus	R_B = 50Ω, C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus		2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLE

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

ORDERING INFORMATION

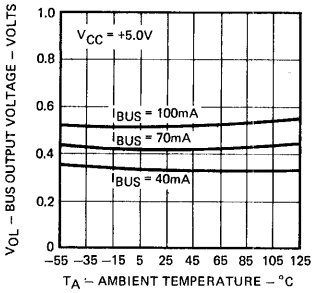
Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2912PC	P-16-1	C	C-1
AM2912DC	D-16-1	C	C-1
AM2912DC-B	D-16-1	C	B-1
AM2912DM	D-16-1	M	C-3
AM2912DM-B	D-16-1	M	B-3
AM2912FM	F-16-1	M	C-3
AM2912FM-B	F-16-1	M	B-3
AM2912XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2912XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

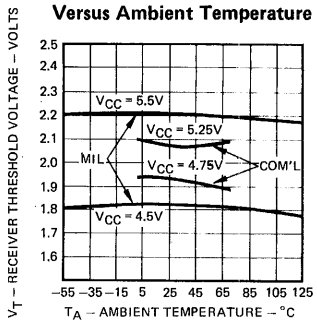
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



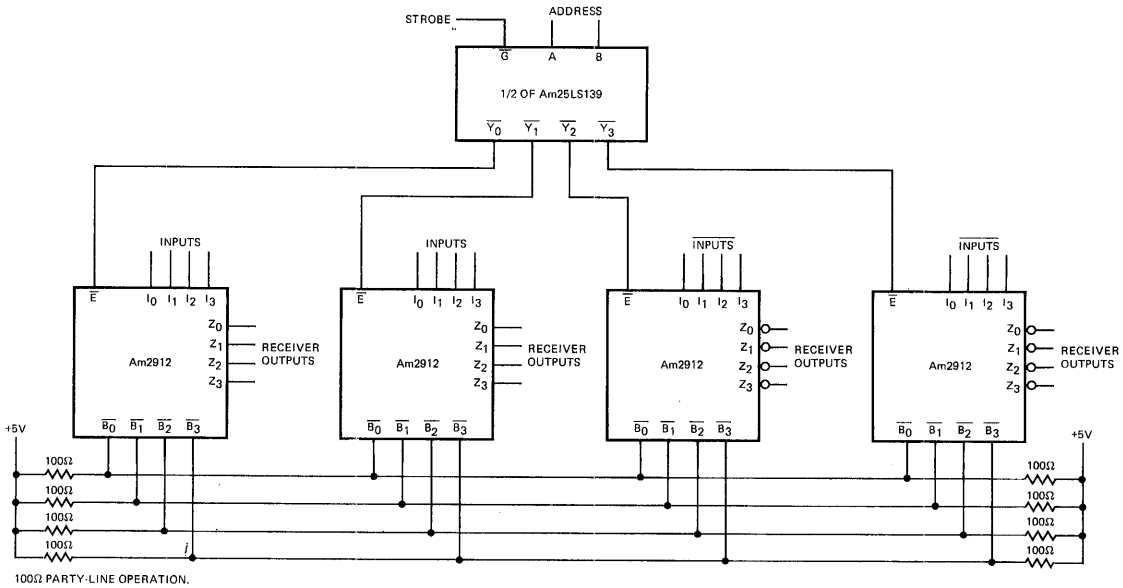
BLI-064

Receiver Threshold Variation Versus Ambient Temperature



BLI-065

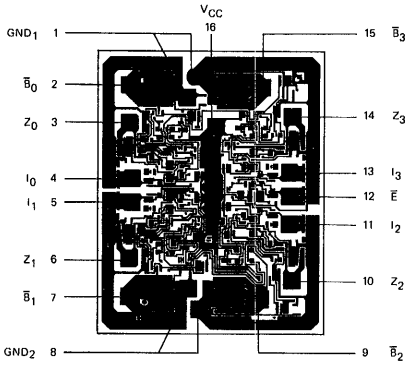
TYPICAL APPLICATION



100Ω PARTY-LINE OPERATION.

BLI-066

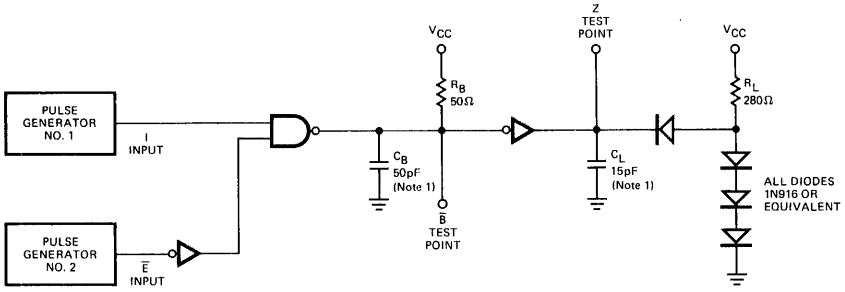
Metallization and Pad Layout



DIE SIZE 0.059" X 0.075"

SWITCHING CHARACTERISTICS

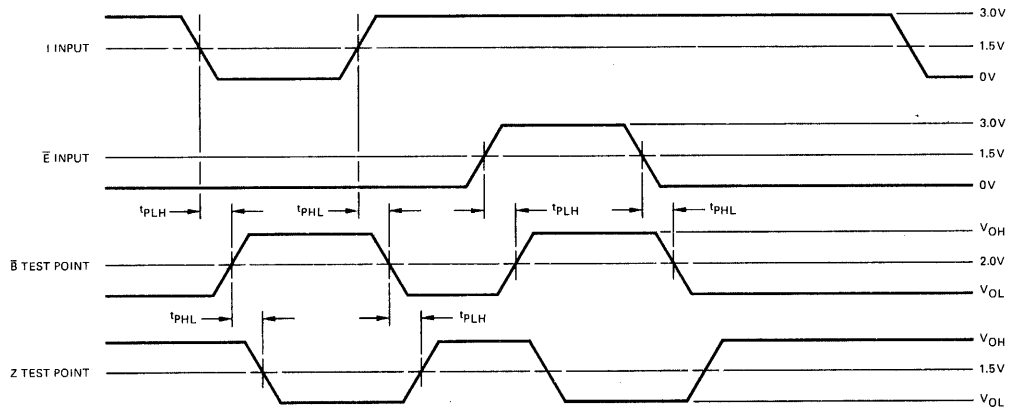
TEST CIRCUIT



BLI-067

Note 1. Includes Probe and Jig Capacitance.

WAVEFORMS



BLI-068

Am2913

Priority Interrupt Expander

Distinctive Characteristics

- Encodes eight lines to three-line binary
- Expands use of Am2914
- Cascadable
- Similar in function to Am54LS/74LS/25LS148/2513
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

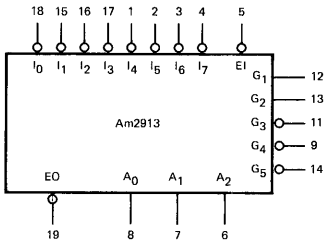
2

FUNCTIONAL DESCRIPTION

The Low-Power Schottky Priority Interrupt Expander is an extention of the Am2900 series of Bipolar Processor family and is used to expand and prioritize the output of the Am2914 Priority Interrupt circuit. Affording an increase of vectored priority interrupt in groups of eight, this unit accepts active LOW inputs and produces a three-state active HIGH output prioritized from active $\overline{I}_7$ to $\overline{I}_0$. The output is gated by five control signals, three active LOW and two active HIGH. Also provided is a cascade input ($\overline{EI}$) and Enable Output ($\overline{EO}$).

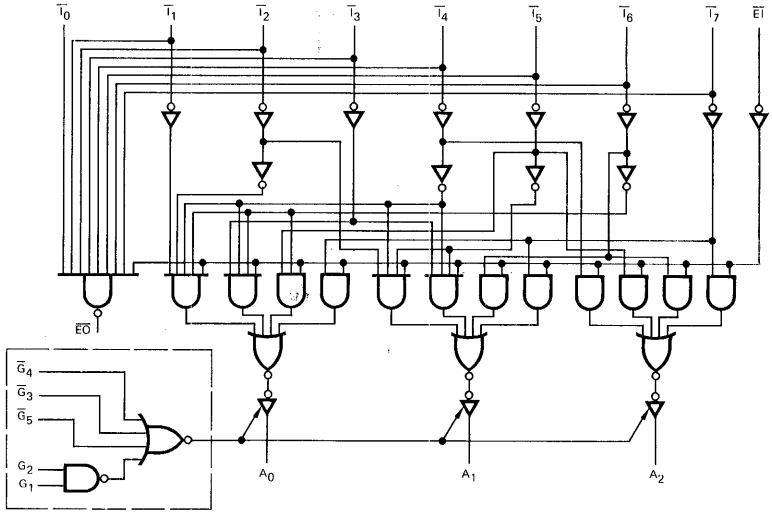
One Am2913 will accept and encode group signal lines from up to 8 Am2914's (64 levels of interrupt). Additional Am2913's may be used to encode more interrupt levels.

LOGIC SYMBOL



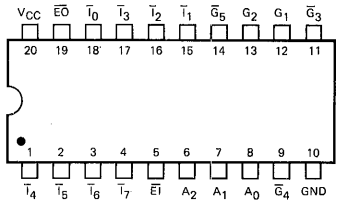
MPR-118

LOGIC DIAGRAM



MPR-119

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-120

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.2		
			$\overline{EO}$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA (A_n$ Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{EI}, G_1, G_2, \overline{G}_3, \overline{G}_4, \overline{G}_5, \overline{I}_0$				0.4	mA
			All others				0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{EI}, G_1, G_2, \overline{G}_3, \overline{G}_4, \overline{G}_5, \overline{I}_0$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	$\overline{EI}, G_1, G_2, \overline{G}_3, \overline{G}_4, \overline{G}_5, \overline{I}_0$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2913PC	P-20	C	C-1
AM2913DC	D-20	C	C-1
AM2913DC-B	D-20	C	B-1
AM2913DM	D-20	M	C-3
AM2913DM-B	D-20	M	B-3
AM2913FM	F-20	M	C-3
AM2913FM-B	F-20	M	B-3
AM2913XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2913XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential Continuous	–0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	–0.5V to +V_{CC} max.
DC Input Voltage	–0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	–30mA to +5.0mA

2

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		17	25	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		11	17	ns	
t_{PHL}			12	18		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		7.0	11	ns	
t_{PHL}			24	36		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		11	17	ns	
t_{PHL}			23	34		
t_{PLH}	$\overline{EI}$ to A_n		12	18	ns	
t_{PHL}			14	21		
t_{ZH}	G_1 or G_2 to A_n		23	40	ns	
t_{ZL}			20	37		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		20	30	ns	
t_{ZL}			18	27		
t_{HZ}	G_1 or G_2 to A_n		17	27	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			19	28		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		16	24	ns	
t_{LZ}			18	27		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2913 COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2913 COM'L Max.	Am2913 MIL T_A = –55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2913 MIL Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		31		37	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			30		34		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		22		27	ns	
t_{PHL}			22		25		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		15		18	ns	
t_{PHL}			48		60		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		19		21	ns	
t_{PHL}			46		57		
t_{PLH}	$\overline{EI}$ to A_n		22		25	ns	
t_{PHL}			27		32		
t_{ZH}	G_1 or G_2 to A_n		42		49	ns	
t_{ZL}			43		49		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		36		43	ns	
t_{ZL}			35		43		
t_{HZ}	G_1 or G_2 to A_n		34		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			34		40		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		30		35	ns	
t_{LZ}			31		35		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

DEFINITIONS OF FUNCTIONAL TERMS

$A0, A1, A2$	Three-state, active high encoder outputs
$\overline{EI}$	Enable input provided to allow cascaded operation
$\overline{EO}$	Enable output provided to enable the next lower order priority chip
G_1, G_2	Active high three-state output controls
$\overline{G}_3, \overline{G}_4, \overline{G}_5$	Active low three-state output controls
$\overline{I}_{0-7}$	Active low encoder inputs

TRUTH TABLE

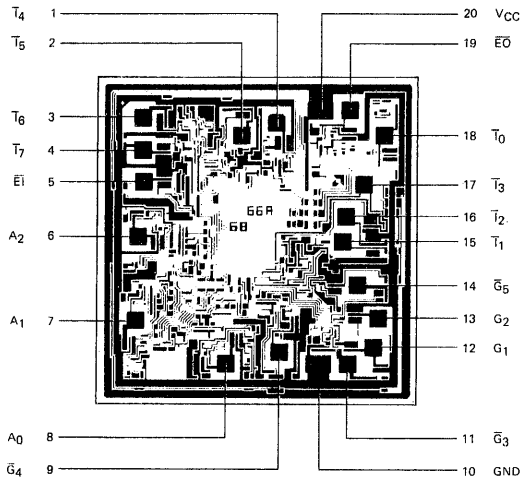
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

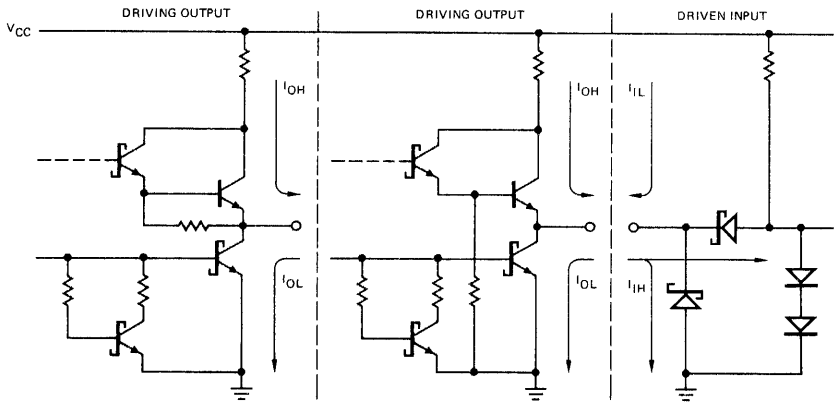
Z = HIGH Impedance

Metallization and Pad Layout



DIE SIZE 0.082" X 0.085"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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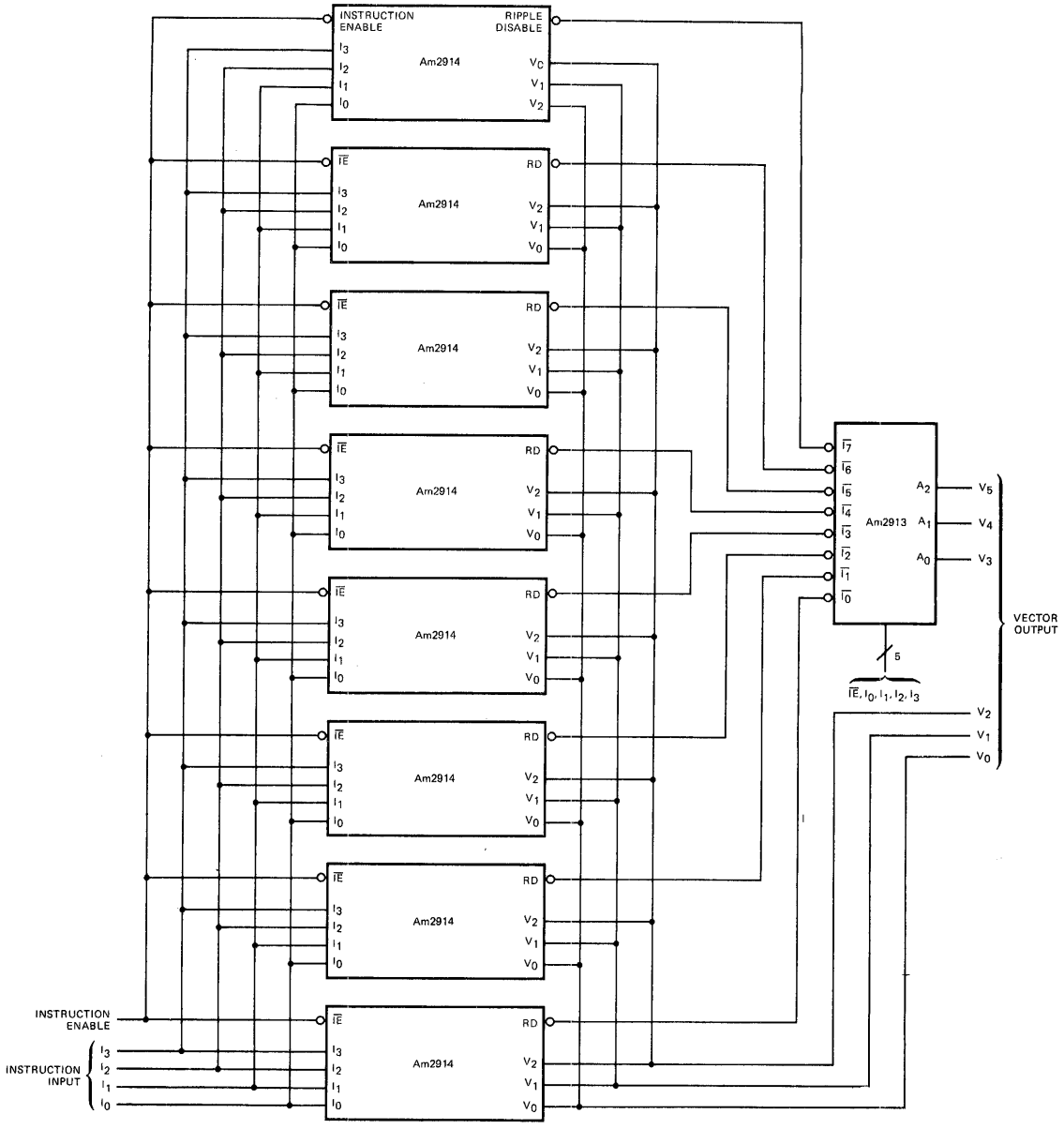

Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

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Am2914

Vectored Priority Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register
  Six different operations can be performed on mask register
- Built-in status register
  Status register holds code for lowest allowed interrupt
- Vectored output
  Output is binary code for highest priority un-masked interrupt
- Expandable
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming
- High-speed operation
  Delay from an interrupt clocked into the interrupt register to interrupt request output is typically 60 ns

TABLE OF CONTENTS

For applications information,
see Chapter VI of "Build a Microcomputer".

FUNCTIONAL DESCRIPTION

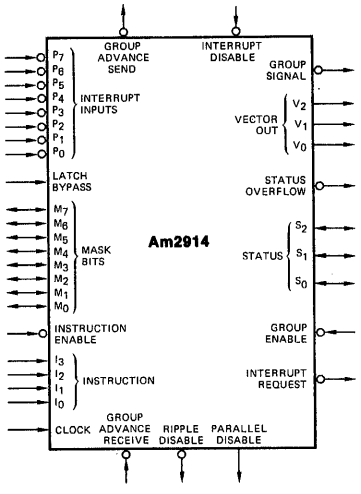
The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

LOGIC SYMBOL



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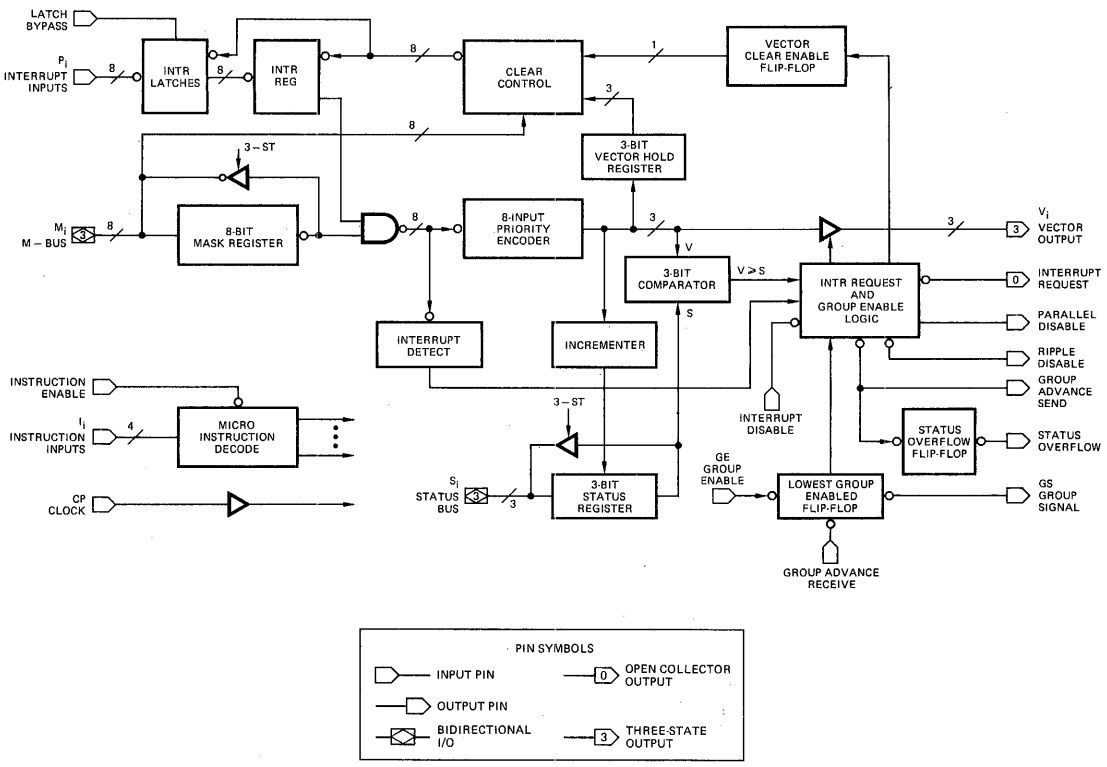
BLOCK DIAGRAM



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BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

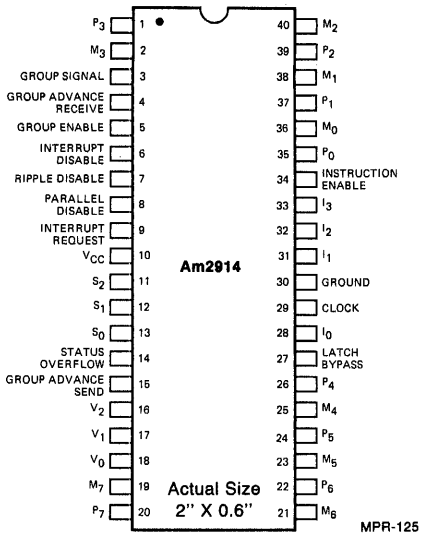
The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

CONNECTION DIAGRAMS – Top Views

DIP



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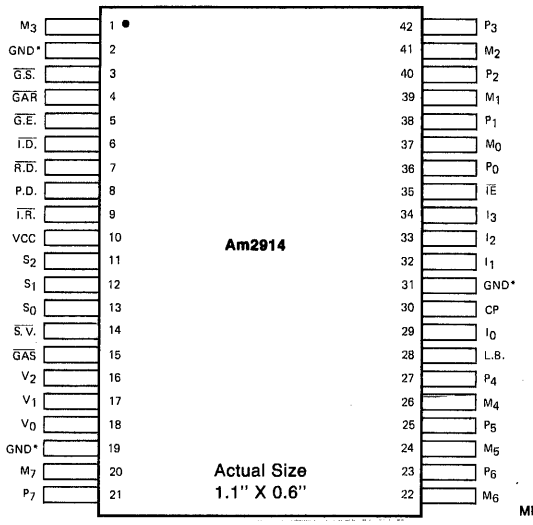
Flat Package



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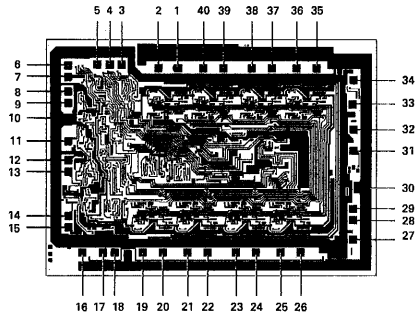
*Note: GND's and pins 2, 19, 31 must all be tied together externally.

Note: Pin 1 is marked for orientation.

Metallization and Pad Layout



DIE SIZE
0.133" X 0.187"
Numbers correspond to DIP pin-out.

TABLE I
MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions
14	LDM	Load mask register from M bus
7	RDM	Read mask register to M bus
12	CLRM	Clear mask register (enables all priorities)
8	SETM	Set mask register (inhibits all interrupts)
10	BCLRM	Bit clear mask register from M bus
11	BSETM	Bit set mask register from M bus
		Status Register Functions
9	LDSTA	Load status register from S bus and LGE flip-flop from GE input
6	RDSTA	Read status register to S bus
		Interrupt Request Control
15	ENIN	Enable interrupt request
13	DISIN	Disable interrupt request
		Vectored Output
5	RDVC	Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.
		Priority Interrupt Register Clear
1	CLRIN	Clear all interrupts
3	CLRMR	Clear interrupts from mask register data (uses the M bus)
2	CLRMB	Clear interrupts from M bus data
4	CLRVC	Clear the individual interrupt associated with the last vector read
		Master Clear
0	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2914PC, DC	Am2914DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/sec	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups. Maximum accept number is 3		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2914PC.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2914PC	P-40	C	C-1
AM2914DC	D-40	C	C-1
AM2914DC-B	D-40	C	B-2 (Note 4)
AM2914DM	D-40	M	C-3
AM2914DM-B	D-40	M	B-3
AM2914FM	F-42	M	C-3
AM2914FM-B	F-42	M	B-3
AM2914XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2914XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Temperature	V_{CC}
Am2914PC, DC	0°C to +70°C	4.75V to 5.25V
Am2914DM, FM	−55°C to +125°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Am2914XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V

Am2914XM T_C = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN., V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	M_{0-7}				−0.15	mA
			S_{0-2}				−0.1	
			L. B.				−0.4	
			$\overline{I. D.}$				−2.0	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	M_{0-7}				150	µA
			S_{0-2}				100	
			$\overline{IE}$, $\overline{GE}$, $\overline{GAR}$				40	
			$\overline{I. D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Off-State Output Current	V_{CC} = MAX.	V_{OUT} = 0.5V	M_{0-7}			−150	µA
				S_{0-2}			−100	
				V_{0-2}			−50	
			V_{OUT} = 2.4V	M_{0-7}			150	
				S_{0-2}			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = 5.0V, 25°C				170	–	mA
		V_{CC} = MAX.	COM'L	0°C			305	
				70°C			250	
			MIL	−55°C			310	
				125°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS AT 25°C AND 5.0 VOLTS

Note: Guaranteed limits at 25°C and 5.0V are group A, subgroup 9 tests
All outputs fully loaded. C_L = 50pF. Measurements made at 1.5V with
input levels of 0V and 3.0V. All numbers are in ns.
For interrupt request output, $R_L = 470\Omega$

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	GUARANTEED
Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	25
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	10

2

TABLE II. COMBINATIONAL PROPAGATION DELAYS (ns)

From Input \ To Output	TYPICAL						GUARANTEED					
	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	36	40	40	–	–	30	48	55	55	–	–	47
I_{0123}	36	40	40	–	–	30	48	55	55	–	–	47
Irpt. Disable	–	–	25	35	8	19	–	–	37	42	18	25

TABLE III. DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	TYPICAL							GUARANTEED						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Mask Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Status Register	45	55	28	31	37	–	–	59	74	57	57	58	–	–
Lowest Group Enabled Flip-Flop	–	–	22	25	–	–	17	–	–	42	45	–	–	32
Irpt Request Enable Flip-Flop	–	40	–	–	–	–	–	–	56	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	17	–	–	–	–	–	–	30	–

TABLE IV. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	GUARANTEED	
	Set-up Time	Hold Time
S-Bus	11	8
M-Bus	11	8
$\overline{P_0}$-$\overline{P_7}$	11	6
Latch Bypass	16	0
$\overline{IE}$ I_{0123} (See Note)	46 t_{pwL} + 29	0
$\overline{GE}$	11	11
$\overline{GAR}$	11	11
$\overline{Irpt\ Disable}$	35	0
P_0-P_7 Hold Time Relative to LB	–	21

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

(Group A, subgroup 10 and 11 tests and limits)

All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0V and 3.0V. For Interrupt Request Output, R_L = 470Ω.

TABLE V. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%	Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE VI. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

From Input \ To Output	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%						Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%					
	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	65	–	–	56	60	68	70	–	–	62
I_{0123}	52	60	65	–	–	56	60	68	70	–	–	62
Irpt. Disable	–	–	45	52	20	30	–	–	48	60	22	33

TABLE VII. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

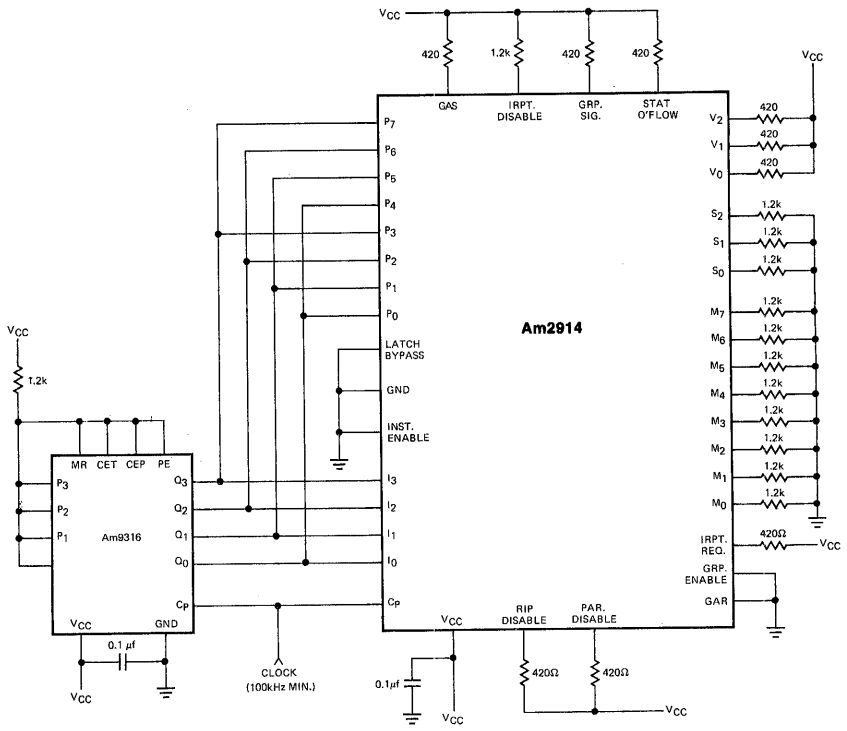
Clock Path	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%							Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip-Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip-Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

TABLE VIII. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%		Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%	
	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	10	15	10
M-Bus	15	10	15	10
$\overline{P_0}$-$\overline{P_7}$	15	8	15	8
Latch Bypass	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	13	15	13
$\overline{Irpt\ Disable}$	42	0	42	0
P_0-P_7 Hold Time Relative to LB	—	25	—	25

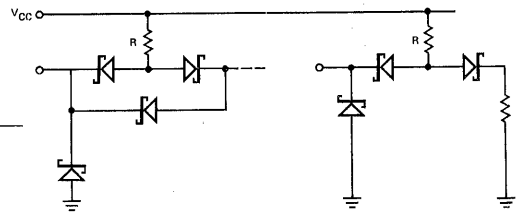
Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.



Am2914 Burn-in Circuit

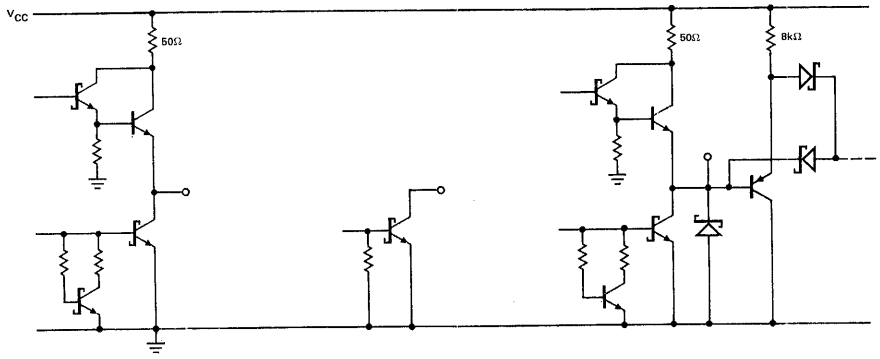
MPR-127

INPUT/OUTPUT CIRCUITS



INPUT	R
I_0-I_3, CP, $\overline{GE}$, $\overline{GAR}$	10K
LB	20K
$\overline{IE}$	6.7K
$\overline{ID}$	4K

INPUT	R
$\overline{P_7}$-$\overline{P_0}$	10K



OUTPUTS	
V_0-V_3	$\overline{SO}$
$\overline{GAS}$	PD
$\overline{GS}$	$\overline{RD}$

OUTPUT
$\overline{IR}$

OUTPUTS
M_0-M_7
S_0-S_3

MPR-128

A MICROPROGRAMMABLE, BIPOLAR, LSI INTERRUPT STRUCTURE USING THE Am2914

INTRODUCTION

Advanced Micro Devices' introduction of the Am2914 Vectored Priority Interrupt Controller now makes possible the structuring of a microprogrammable bipolar LSI interrupt system. The design engineer may use the Am2914 to simplify his design process, dramatically reduce the system cost, size and package count, and increase the speed, capability and reliability of his interrupt system.

The Am2914 is a modular, low cost, standard LSI component that may be microprogrammed to meet the requirements of specific applications. Today's engineer may utilize the Am2914 microprogrammability to provide functional flexibility and ease of engineering change, while taking advantage of its modularity to provide hardware regularity and future expansion capability.

THE INTERRUPT CONCEPT

In any state machine, a requirement exists for the efficient synchronization and response to asynchronous events such as power failure, machine malfunctions, control panel service requests, external timer signals, supervisory calls, program errors, and input/output device service requests. The merit of such an "asynchronous event handler" may be measured in terms of response time, system throughput, real time overhead, hardware cost and memory space required.

The simplest approach to asynchronous event handling is the poll approach. A status indicator is associated with each possible asynchronous event. The processor tests each indicator in sequence and, in effect, "asks" if service is required. This program-driven method is inefficient for a number of reasons. Much time is consumed polling when no service is required; programs must have frequent test points to poll indicators, and since indicators are polled in sequence, considerable time may elapse before the processor responds to an event. Thus, system throughput is low; real time overhead and response time are high, and a large memory space is required.

The interrupt method is a much more efficient way of servicing asynchronous requests. An asynchronous event requiring service generates an interrupt request signal to the processor. When the processor receives the interrupt request, it may suspend the program it is currently executing, execute an interrupt service routine which services the asynchronous request, then resume the execution of the suspended program. In this system, the execution of the service routine is initiated by an interrupt request; thus, the system is interrupt driven and service routines are executed only when service is requested. Although hardware cost may be higher in this type of system, it is more efficient since system throughput is higher, response time is faster, real time overhead is lower and less memory space is required.

INTERRUPT SYSTEM FUNCTIONAL DEFINITION

A complete and clear functional definition is key to the design of a good interrupt system. The following features are useful.

Multiple Interrupt Request Handling: Since interrupt requests are generated from a number of different sources, the interrupt system's ability to handle interrupt requests from several sources is important.

Interrupt Request Prioritization: Since the processor can service only one interrupt request at a time, it is important that the interrupt system has the ability to prioritize the requests and determine which has the highest priority.

Interrupt Service Routine "Nesting": This feature allows an interrupt service routine for a given priority request to be interrupted in turn, but only by a higher priority interrupt request. The service routine for the higher priority request is executed, then the execution of the interrupted service routine is resumed. If there are "n" interrupt requests, an "n" deep "nest" is possible.

Dynamic Interrupt Enabling/Disabling: The ability to enable/disable all interrupts "on the fly" under microprogram control can be used to prevent interruption of certain processes.

Dynamic Interrupt Request Masking: The ability to selectively inhibit or "mask" individual interrupt requests under microprogram control is useful.

Interrupt Request Vectoring: Many times, a particular interrupt request requires the execution of a unique interrupt service routine. For this reason, the generation of a unique binary coded vector for each interrupt request is very helpful. This vector can be used as a pointer to the start of a unique service routine.

Interrupt Request Priority Threshold: The ability to establish a priority threshold is valuable. In this type of operation, only those interrupt requests which have higher priority than a specified threshold priority are accepted. The threshold priority can be defined by microprogram or can be automatically established by hardware at the interrupt currently being serviced plus one. This automatic threshold prevents multiple interrupts from the same source. Also useful is the ability to read the threshold priority under microprogram control. Thus, the interrupt request being serviced may be determined by the microprogram.

Interrupt Request Clearing Flexibility: Flexibility in the method of clearing interrupt requests allows different modes of interrupt system operation. Of particular value are the abilities to clear the interrupt currently being serviced, clear all interrupts, or clear interrupts via a programmable mask register or bus.

Microprogrammability: Microprogrammability permits the construction of a general purpose or "universal" interrupt structure which can be microprogrammed to meet a specific application's requirements. The universality of the structure allows standardization of the hardware and amortization of the hardware development costs across a much broader user base. The end result is a flexible, low cost interrupt structure.

Hardware Modularity: Modular interrupt system hardware is beneficial in two ways. First, hardware modularity provides expansion capability. Additional modules may be added as the need to service additional requests arises. Secondly, hardware modularity provides a structural regularity which simplifies the system structure and also reduces the number of hardware part numbers.

Fast Interrupt System Response Time: Quick interrupt system response provides more efficient system operation. Fast response reduces real time overhead and increases overall system throughput.

INTERRUPT SYSTEM IMPLEMENTATION USING THE Am2914

The Am2914 provides all of the foregoing features on a single LSI chip. The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The Am2914's high speed is ideal for use in Am2900 Family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on eight Interrupt Input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses (HIGH-LOW-HIGH) on these lines, or the latch may be bypassed so that the request lines drive the D-inputs to the edge-triggered Interrupt Register directly. An eight-bit Mask Register is used to mask individual interrupts. Considerable flexibility is provided for controlling the Mask Register. Requests in the Interrupt Register (P_0-P_7) are ANDed with the corresponding bits in the mask register (M_0-M_7) and the results are sent to an eight-input priority encoder, which produces a three-bit encoded vector representing the highest priority input which is not masked.

An internal Status Register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the Status Register are compared with the output of the priority encoder, and an Interrupt Request output will occur if the vector is greater than or equal to the contents of the Status Register. Whenever a vector is read from the Am2914, the Status Register is automatically updated to point to one level higher than the vector read. (The Status Register can be loaded externally or read out at any time using the S-Bus.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A Status Overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a four-bit microinstruction field I_0-I_3. The microinstruction is executed if $\overline{IE}$ (Instruction Enable) is LOW and is ignored if $\overline{IE}$ is HIGH, allowing the four I bits to be shared with other functions. Sixteen different microinstructions are executed. Figure 2 shows the microinstructions and the microinstruction codes.

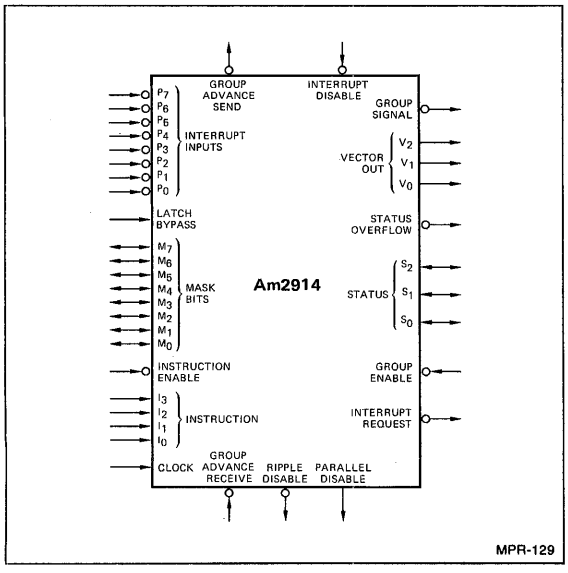


Figure 1. Am2914 Logic Symbol.

MICROINSTRUCTION DESCRIPTION	MICROINSTRUCTION CODE $I_3I_2I_1I_0$
MASTER CLEAR	0000
CLEAR ALL INTERRUPTS	0001
CLEAR INTERRUPTS FROM M-BUS	0010
CLEAR INTERRUPTS FROM MASK REGISTER	0011
CLEAR INTERRUPT, LAST VECTOR READ	0100
READ VECTOR	0101
READ STATUS REGISTER	0110
READ MASK REGISTER	0111
SET MASK REGISTER	1000
LOAD STATUS REGISTER	1001
BIT CLEAR MASK REGISTER	1010
BIT SET MASK REGISTER	1011
CLEAR MASK REGISTER	1100
DISABLE INTERRUPT REQUEST	1101
LOAD MASK REGISTER	1110
ENABLE INTERRUPT REQUEST	1111

Figure 2. Am2914 Microinstruction Set.

In this microinstruction set, the *Master Clear* microinstruction is selected as binary zero so that during a power up sequence, the microinstruction register in the microprogram control unit of the central processor can be cleared to all zeros. Thus, on the next clock cycle, the Am2914 will execute the *Master Clear* function. This includes clearing the Interrupt Latches and Register as well as the Mask Register and Status Register. The LGE flip-flop of the least significant group is set LOW because the Group Advance Receive input is tied LOW. All other Group Advance Receive inputs are tied to Group Advance Send outputs and these are forced HIGH during this instruction. This clear instruction also sets the Interrupt Request Enable flip-flop so that a fully interrupt driven system can be easily initiated from any interrupt.

The *Clear All Interrupts* microinstruction clears the Interrupt Latches and Register.

The *Clear Interrupts from Mask Register* microinstruction clears those Interrupt Latches and Register bits which have corresponding Mask Register bits set equal to one. The M-Bus is used by the Am2914 during the execution of this microinstruction and must be floating.

The *Clear Interrupts from M-Bus* microinstruction clears those Interrupt Latches and Register bits which have corresponding M-Bus bits set equal to one.

The *Clear Interrupt, Last Vector Read* microinstruction clears the Interrupt Latch and Register bit associated with the last vector read.

The *Read Vector* microinstruction is used to read the vector value of the highest priority request causing the interrupt. The vector outputs are three-state drivers that are enabled onto the $V_0V_1V_2$ bus during this instruction. This microinstruction also automatically loads the value "vector plus one" into the Status Register. In addition, this instruction sets the Vector Clear Enable flip-flop and loads the current vector value into the Vector Hold Register so that this value can be used by the *Clear Interrupt, Last Vector Read* microinstruction. This allows the user to read the vector associated with the interrupt, and at some later time clear the Interrupt Latch and Register bit associated with the vector read.

The *Load Status Register* microinstruction loads S-Bus data into the Status Register and also loads the LGE flip-flop from the Group Enable input.

During the *Read Status Register* microinstruction, the Status Register outputs are enabled onto the Status Bus (S_0-S_2). The Status Bus is a three-bit, bi-directional, three-state bus.

The *Load Mask Register* microinstruction loads data from the three-state, bi-directional M-Bus into the Mask Register.

The *Read Mask Register* microinstruction enables the Mask Register outputs onto the bi-directional, three-state M-Bus.

The *Set Mask Register* microinstruction sets all the bits in the Mask Register to one. This results in all interrupts being inhibited.

The entire Mask Register is cleared by the *Clear Mask Register* microinstruction. This enables all interrupts subject to the Interrupt Enable flip-flop and the Status Register.

The *Bit Clear Mask Register* microinstruction may be used to selectively clear individual Mask Register bits. This microinstruction clears those Mask Register bits which have corresponding M-Bus bits equal to one. Mask Register bits with corresponding M-Bus bits equal to zero are not affected.

The *Bit Set Mask Register* microinstruction sets those Mask Register bits which have corresponding M-Bus bits equal to one. Other Mask Register bits are not affected.

All Interrupt Requests may be disabled by execution of the *Disable Interrupt Request* microinstruction. This microinstruction resets an Interrupt Request Enable flip-flop on the chip.

The *Enable Interrupt Request* microinstruction sets the Interrupt Enable flip-flop. Thus, Interrupt Requests are enabled subject to the contents of the Mask and Status Registers.

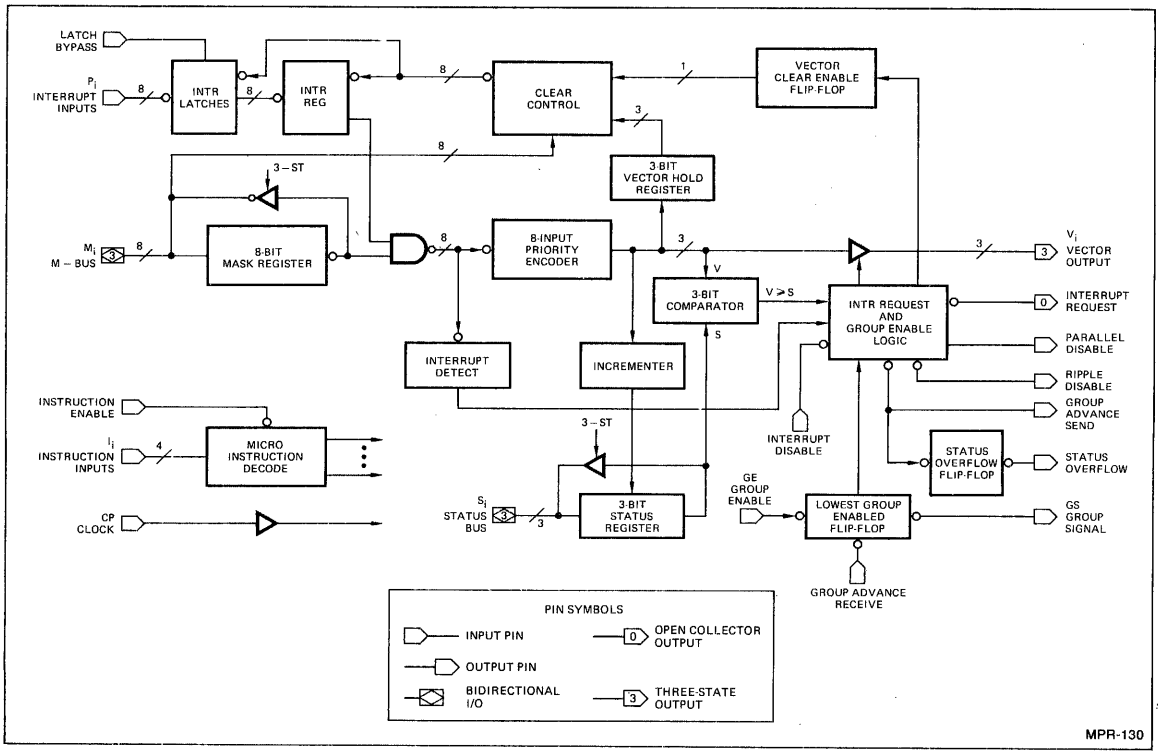


Figure 3. Am2914 Block Diagram.

Am2914 BLOCK DIAGRAM DESCRIPTION

The Am2914 block diagram is shown in Figure 3. The Micro-instruction Decode circuitry decodes the Interrupt Micro-instructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal if the Interrupt Input is LOW.

The Interrupt latches are set/reset latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M-Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector can be used later for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S-Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus, the Status Register points to a level one greater than the vector just read.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this chip. When it is set it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

The Am2914 can be microprogrammed in many different ways. Figure 4 shows an example interrupt sequence. The *Read Vector* microinstruction is necessary in order to read the interrupt priority level. Since vector plus one is automatically loaded into the Status Register when a *Read Vector* microinstruction is executed, the Status Register possibly will overflow and disable all interrupts. For this reason, the Status Register must be reloaded periodically. The other Am2914 microinstructions are optional.

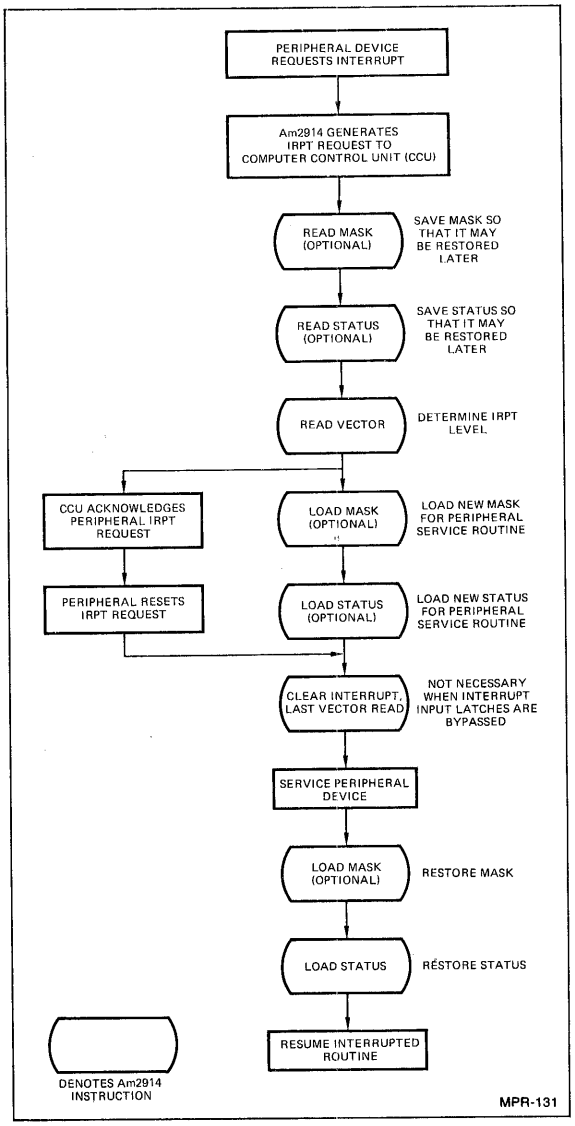


Figure 4. Example Interrupt Sequence.

CASCADING THE Am2914

A number of input/output signals are provided for cascading the Am2914 Vectored Priority Interrupt Encoder. A definition of these I/O signals and their required connections follows:

Group Signal ($\overline{GS}$) – This signal is the output of the Lowest Group Enabled flip-flop and during a Read Status microinstruction is used to generate the high order bits of the Status word.

Group Enable ($\overline{GE}$) – This signal is one of the inputs to the Lowest Group Enable flip-flop and is used to load the flip-flop during the Load Status microinstruction.

Group Advance Send ($\overline{GAS}$) – During a Read Vector microinstruction, this output signal is LOW when the highest priority vector (vector seven) of the group is being read. In a cascaded system Group Advance Send must be tied to the Group Advance Receive input of the next higher group in order to transfer status information.

Group Advance Receive ($\overline{GAR}$) – During a Master Clear or Read Vector microinstruction, this input signal is used with other internal signals to load the Lowest Group Enabled flip-flop. The Group Advance Receive input of the lowest priority group must be tied to ground.

Status Overflow ($\overline{SV}$) – This output signal becomes LOW after the highest priority vector (vector seven) of the group has been read and indicates the Status Register has overflowed. It stays LOW until a Master Clear or Load Status microinstruction is executed. The Status Overflow output of the highest priority group should be connected to the Interrupt Disable input of the same group and serves to disable all interrupts until new status is loaded or the system is master cleared. The Status Overflow outputs of lower priority groups should be left open (see Figure 7).

Interrupt Disable ($\overline{ID}$) – When LOW, this input signal inhibits the Interrupt Request output from the chip and also generates a Ripple Disable output.

Ripple Disable ($\overline{RD}$) – This output signal is used only in the Ripple Cascade Mode (see below). The Ripple Disable output is LOW when the Interrupt Disable input is LOW, the Lowest Group Enabled flip-flop is LOW, or an Interrupt Request is generated in the group. In the ripple cascade mode, the

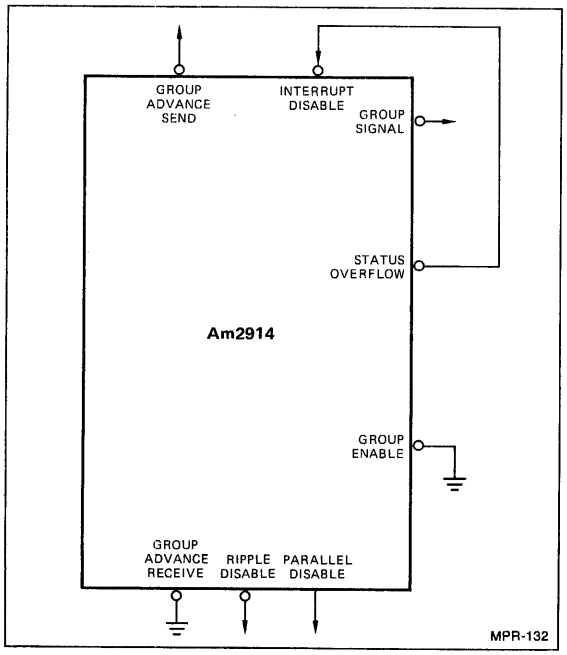


Figure 5. Cascade Lines Connection for Single Chip System.

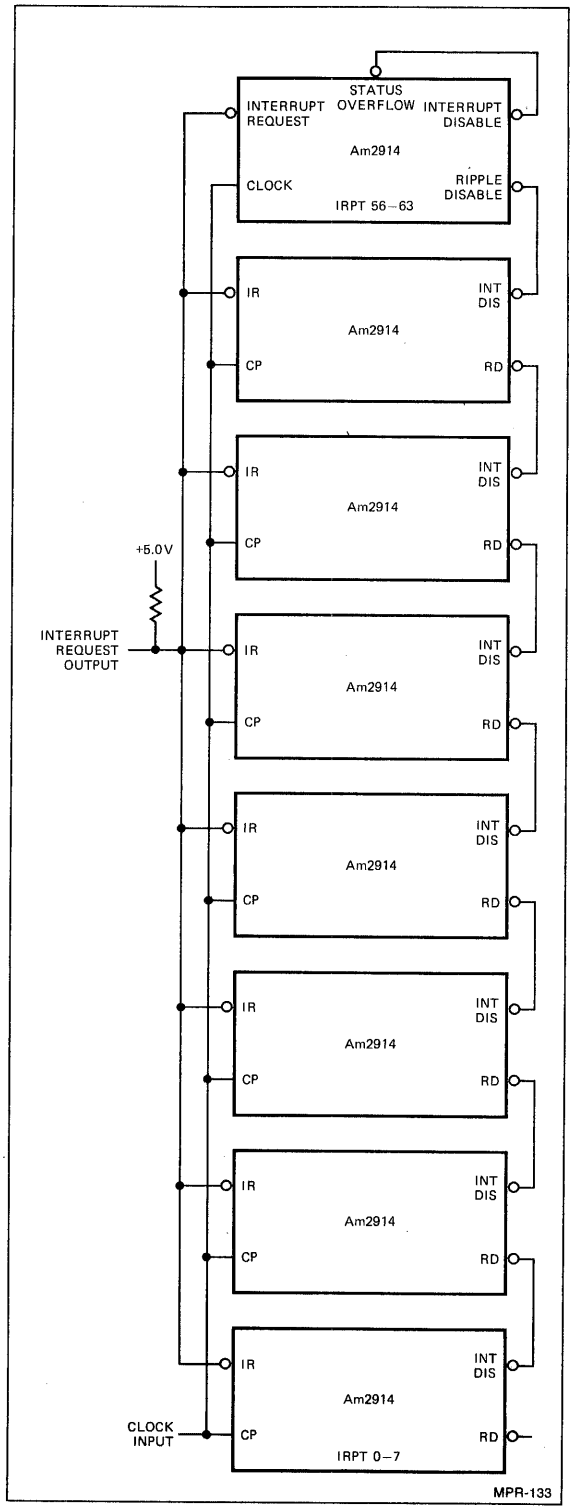


Figure 6. Interrupt Disable Connections for Ripple Cascade Mode.

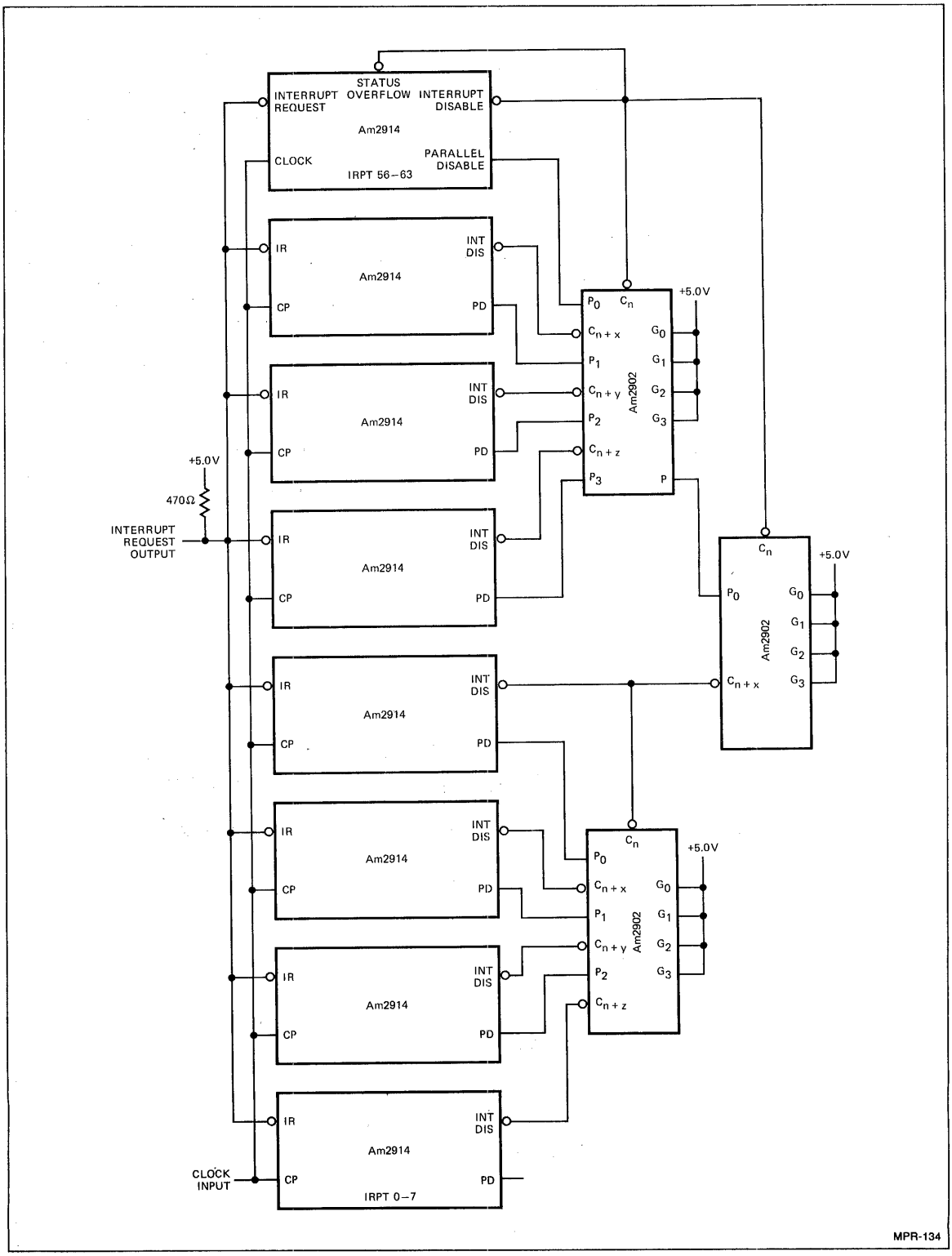


Figure 7. Interrupt Disable Connections for Parallel Cascade Mode.

Ripple Disable output is tied to the Interrupt Disable input of the next lower priority group (see Figure 6).

Parallel Disable (PD) – This output is used only in the parallel cascade mode (see below). It is HIGH when the Lowest Group Enabled flip-flop is LOW or an Interrupt Request is generated in the group. It is not affected by the Interrupt Disable input.

A single Am2914 chip may be used to prioritize and encode up to eight interrupt inputs. Figure 5 shows how the above cascade lines should be connected in such a single chip system.

The Group Advance Receive and Group Enable inputs should be connected to ground so that the Lowest Group Enabled flip-flop is forced LOW during a *Master Clear* or *Load Status* microinstruction. Status Overflow should be connected to Interrupt Disable in order to disable interrupts when vector seven is read. The Group Advance Send, Ripple Disable, Group Signal and Parallel Disable pins should be left open.

The Am2914 may be cascaded in either a Ripple Cascade Mode or a Parallel Cascade Mode. In the Ripple Cascade Mode, the Interrupt Disable signal, which disables lower priority interrupts, is allowed to ripple through lower priority groups. Figures 6, 9 and 11 show the cascade connections required for a ripple cascade 64 input interrupt system.

In the parallel cascade mode, a parallel lookahead scheme is employed using the high-speed Am2902 Lookahead Carry Generator. Figures 7, 9 and 10 show the cascade connections required for a parallel cascade 64-input interrupt system. For this application, the Am2902 is used as a lookahead interrupt disable generator. A Parallel Disable output from any group results in the disabling of all lower priority groups in parallel. Figure 8 shows the Am2902 logic diagram and equations.

In Figures 9 and 10, the Am2913 Priority Interrupt Expander is shown forming the high order bits of the vector and status, respectively. The Am2913 is an eight-line to three-line priority encoder with three-state outputs which are enabled by the five output control signals G1, G2, $\overline{G3}$, $\overline{G4}$, and $\overline{G5}$. In Figure 9, the Am2913 is connected so that its outputs are enabled during a Read Vector instruction, and in Figure 10 the Am2913 is connected so that its outputs are enabled during a Read Status instruction. The Am2913 logic diagram and truth table are shown in Figure 11.

The Am25LS138 three-line to eight-line Decoder also is shown in Figure 10. It is used to decode the three high order status bits during a Load Status instruction. The Am25LS138 logic diagram and truth table are shown in Figure 12.

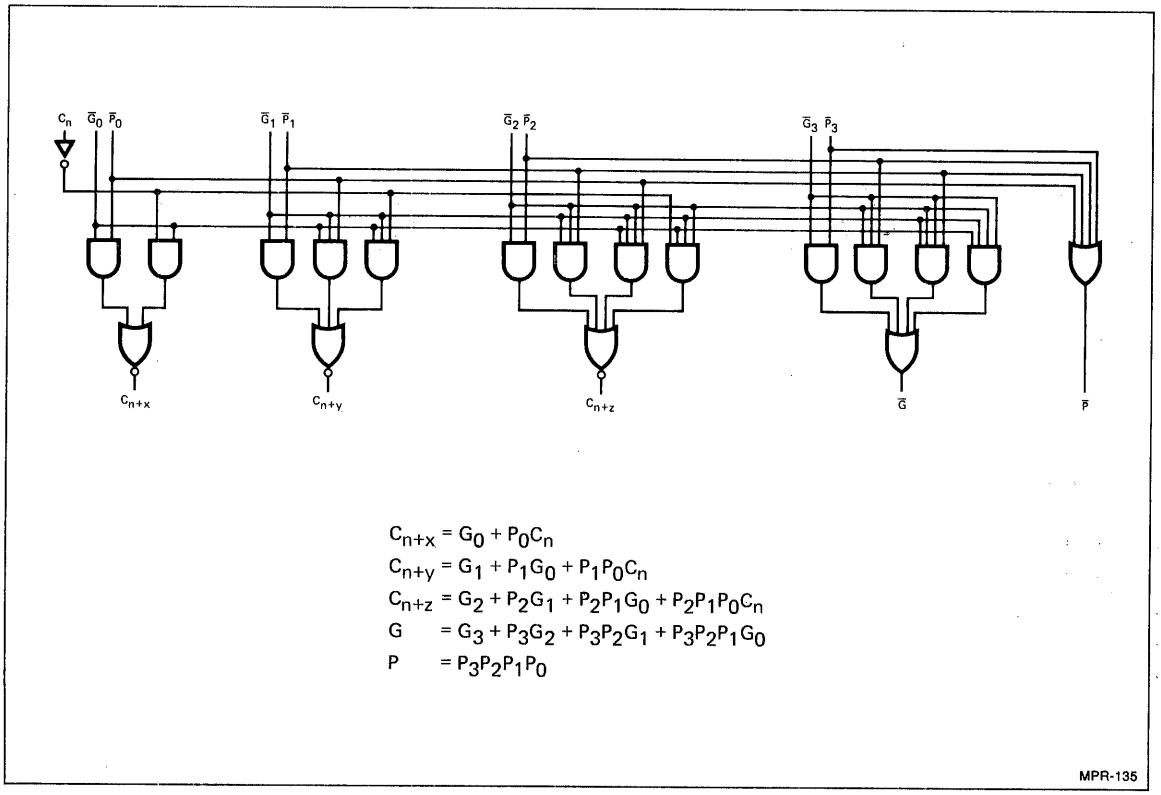


Figure 8. Am2902 Carry Look-Ahead Generator Logic Diagram and Equations.

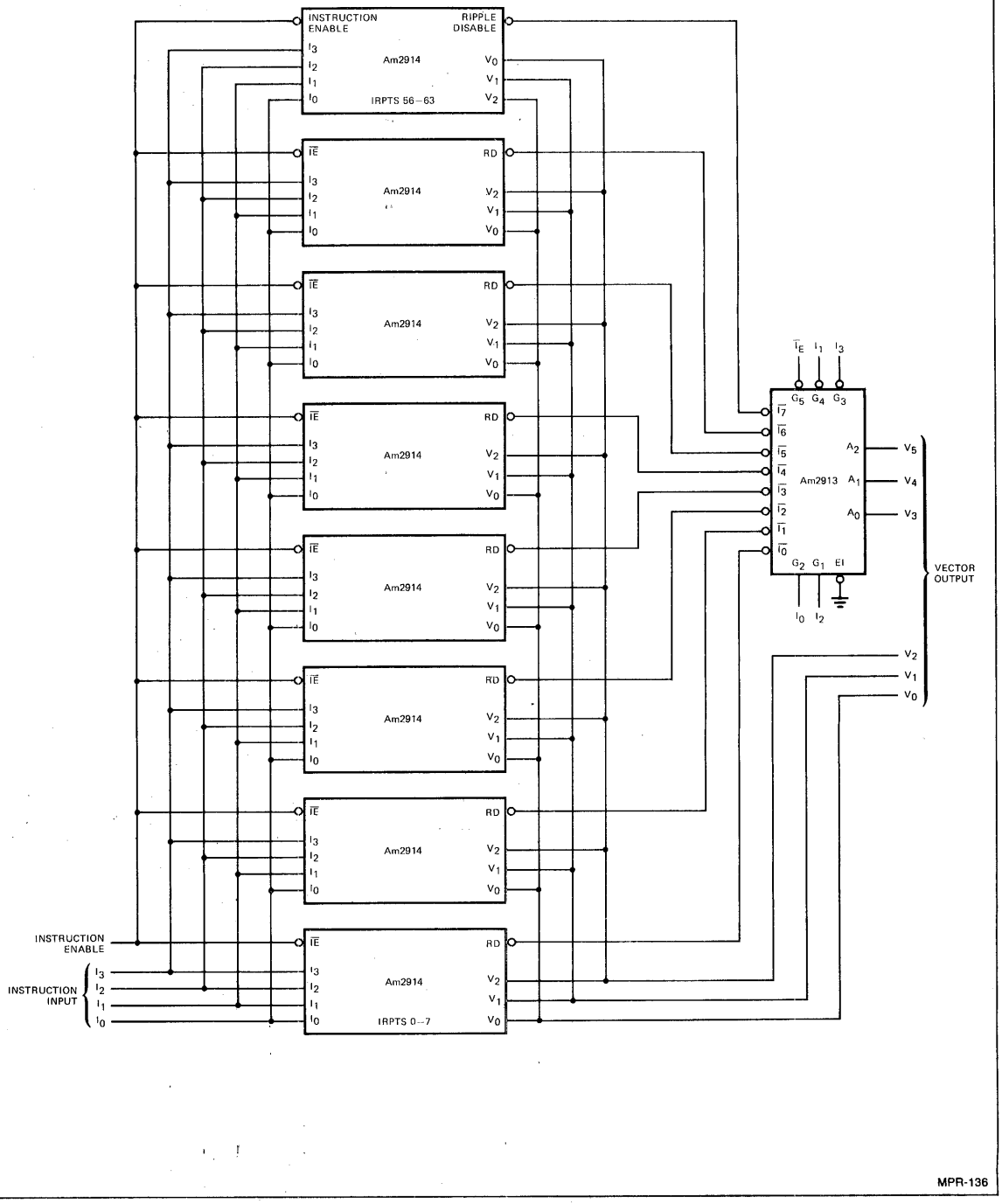


Figure 9. Vector Connections for both the Parallel and Ripple Cascade Modes.

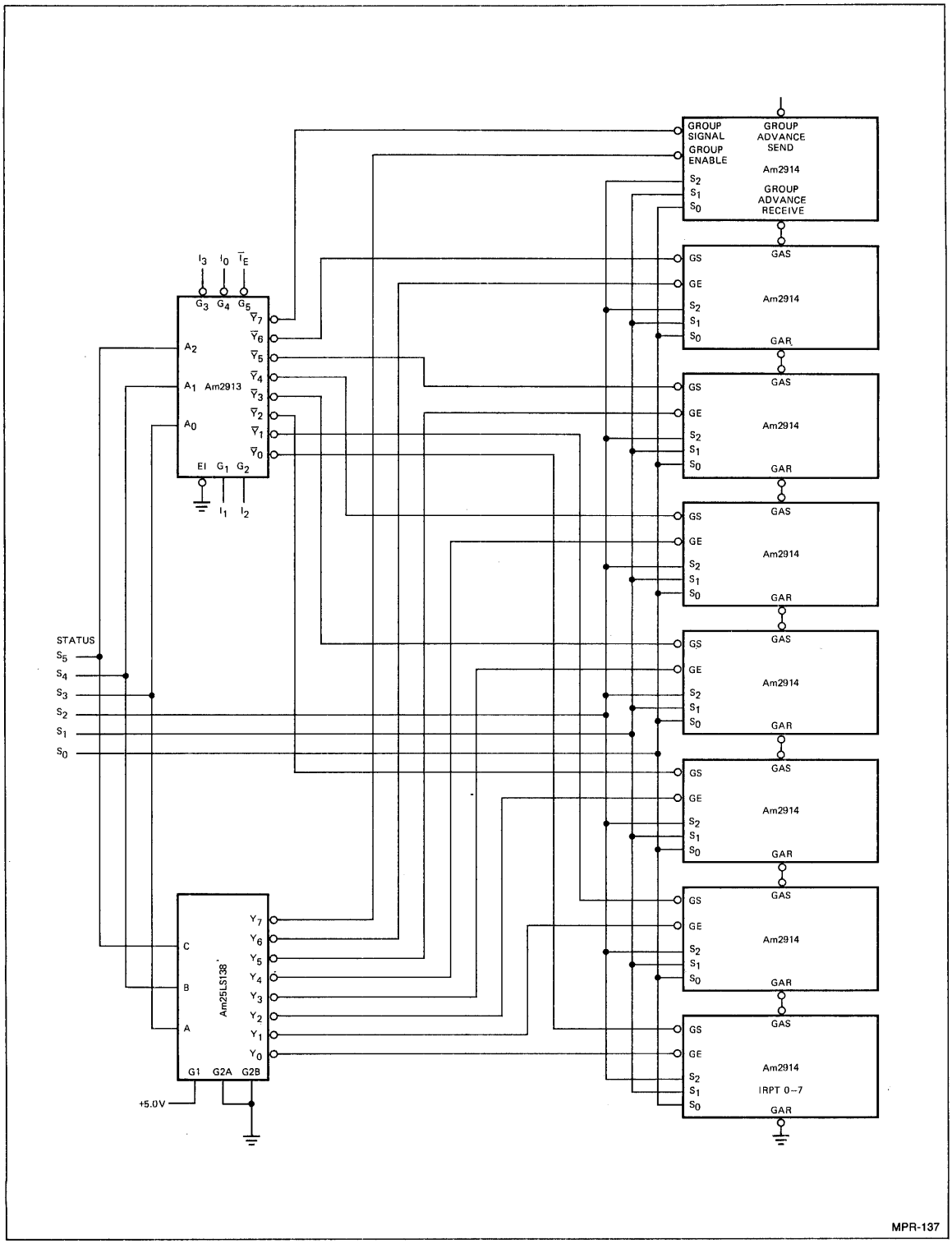
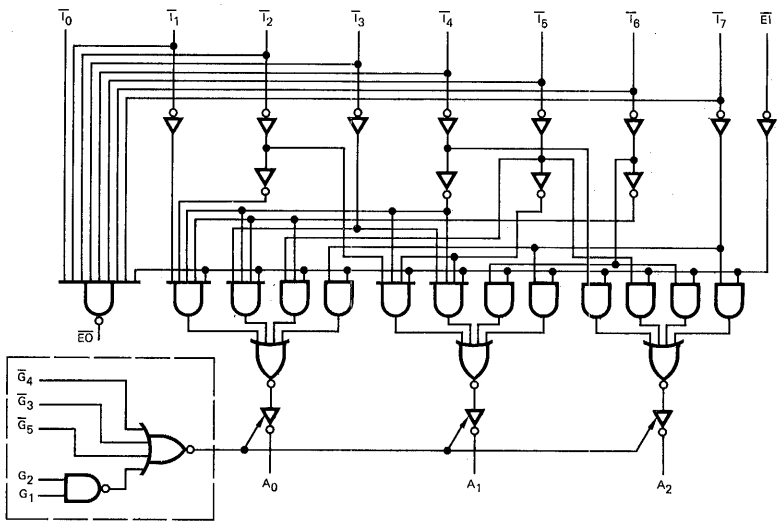


Figure 10. Group Signal, Group Enable, Group Advance Send, Group Advance Receive and Status Connections for Both the Parallel and Ripple Cascade Modes.



Inputs								Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G1 = H, G2 = H,
G3 = L, G4 = L, G5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH Impedance

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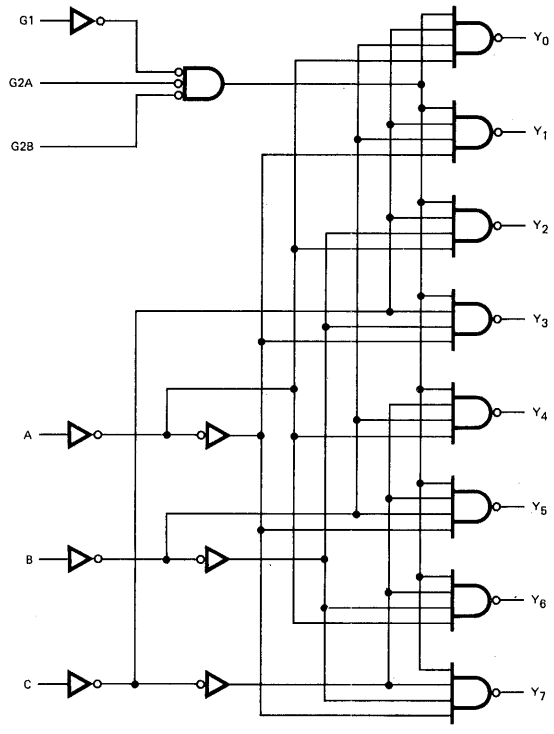
Figure 11. Am2913 Priority Interrupt Expander Logic Diagram and Truth Table.



Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't Care

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Figure 12. Am25LS138 3 to 8 Line Decoder Logic Diagram and Truth Table.

EXAMPLE INTERRUPT SYSTEMS DESIGNS FOR AN Am2900 SYSTEM

A classical computer architecture is shown in Figure 13. The Computer Control Unit controls the internal busses and subsystems of the processor, synchronizes internal and external events and grants or denies permission to external systems. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination(s) of the data. The Address Bus is typically used to select a word in memory for an internal computer function or to select an input/output port for an external subsystem or peripheral function. The source of the data for the address bus, also selected by microprogram commands, may be the program counter, the memory address register, a direct memory address controller, an interface controller, etc.

The arithmetic/logic unit (ALU) is that portion of the processor that computes. Under control of the microprogram, the ALU performs a number of different arithmetic and logic functions on data in the working registers or from the data bus. The ALU also provides a set of condition codes as a result of the current arithmetic or logic operation. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands which are necessary to fetch the data required for the execution of the current instruction.

A subroutine address stack is provided to allow the return address linkage to be handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the CCU microinstruction word.

The next microprogram address control (NMAC) circuitry controls the generation of microinstruction addresses. Based on microprogram control, interrupt requests, test conditions and commands from a control panel or other processor, the NMAC determines the address of the next microinstruction to be executed.

For a more detailed description of the above portions of the computer, refer to Advanced Micro Devices' Application Note *A Microprogrammed 16 Bit Computer* by James R.W. Clymer.

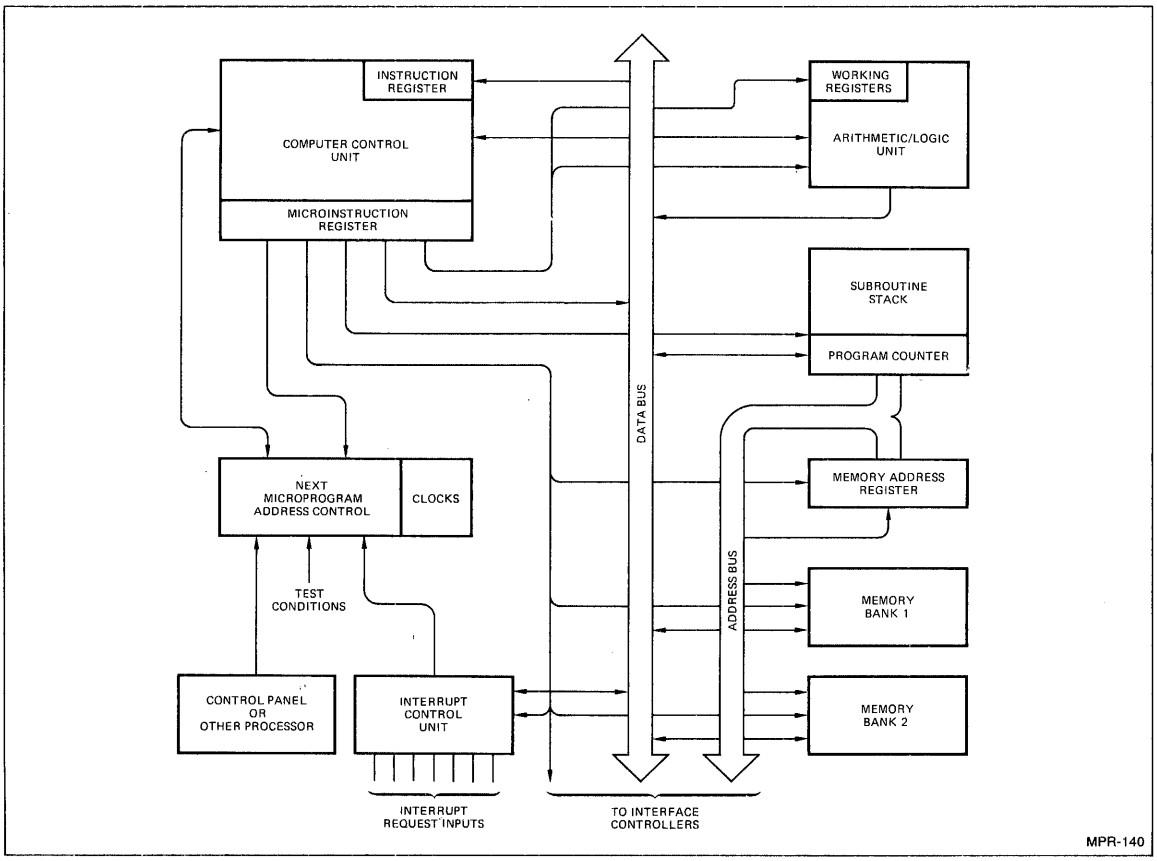


Figure 13. Generalized Computer Architecture.

Am2914 PRIORITY INTERRUPT ENCODER DETAILED LOGIC DESCRIPTION

INTRODUCTION

A clear understanding of the Am2914 Priority Interrupt controller's operation facilitates its efficient use. With that idea in mind, a detailed logic description of the Am2914 is presented here. A detailed logic diagram and control signal truth table are shown, and significant aspects of the Am2914 design are described verbally.

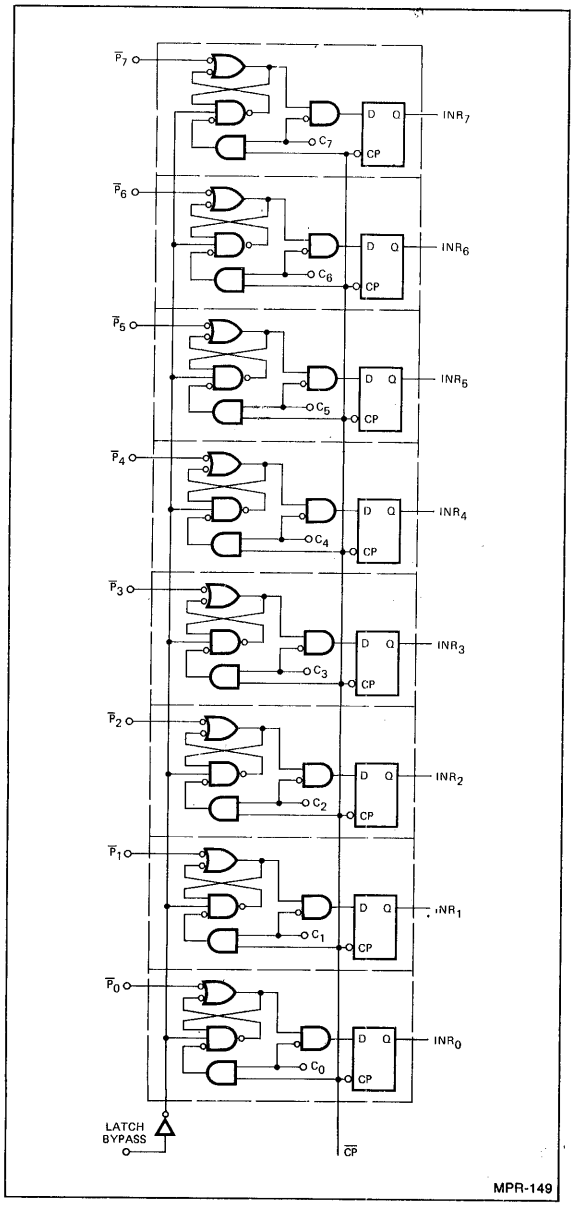


Figure 1. Interrupt Latches and Register.

LOGIC DIAGRAM DESCRIPTION

The Interrupt Latches and Register are shown in Figure 1. The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent. The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register. It is updated on the LOW-to-HIGH transition of the clock pulse (HIGH-to-LOW transition of the $\overline{CP}$ signal) as are all of the flip-flops on the chip.

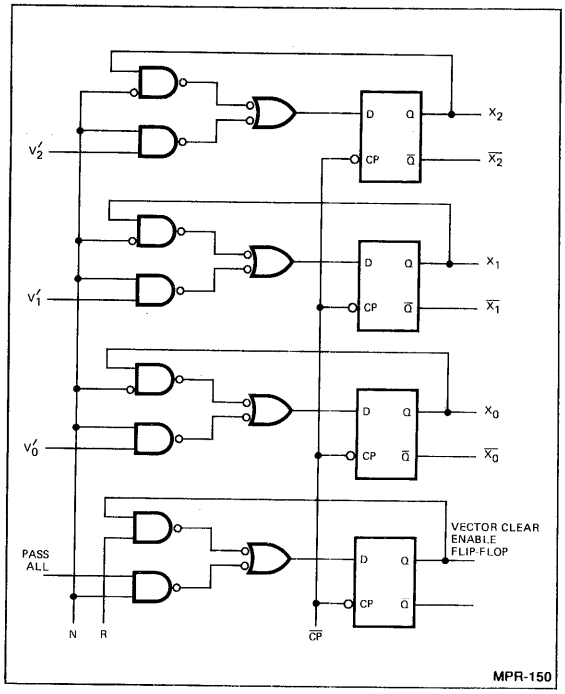


Figure 2. Vector Hold Register

When a Read Vector instruction is executed, the binary coded vector is loaded into the Vector Hold Register of Figure 2. This stored vector can be used later for clearing the interrupt associated with the last vector that was read. The Vector Clear Enable Flip-Flop of Figure 2 is set when a Read Vector instruction is executed and the PASS ALL signal is HIGH. A HIGH PASS ALL signal level indicates that this group is enabled and that an interrupt request in this group was detected and passed priority. The Vector Hold Register and the Vector Clear Enable Flip-Flop are cleared when a Master Clear, Clear All Interrupts, or Clear Interrupt Last Vector Read is executed. Table 1 shows the generation of the "N and R" control signals for each of these operations.

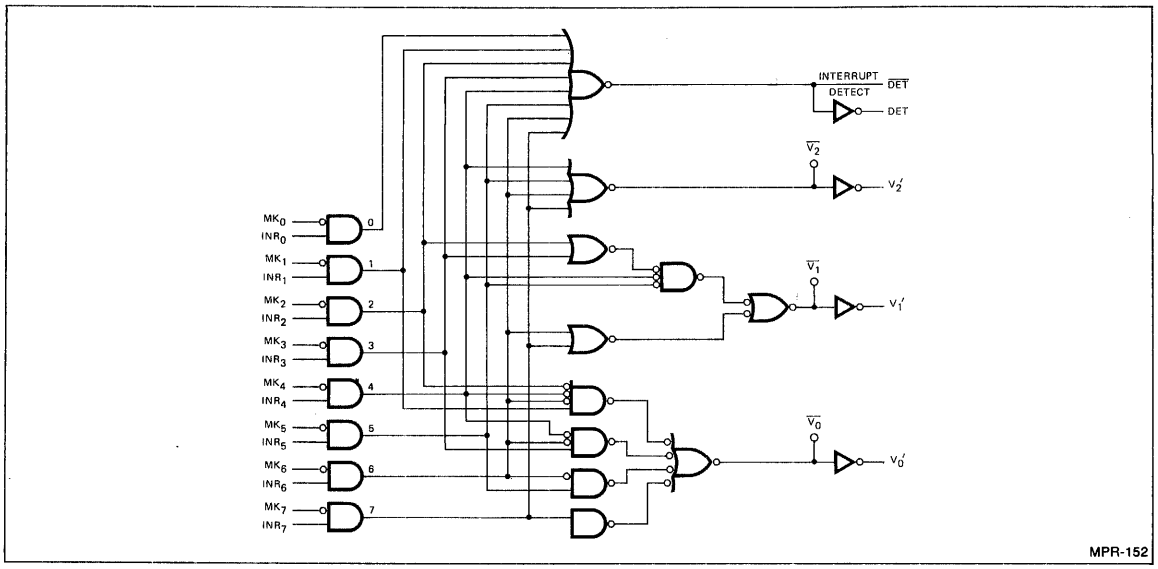


Figure 4. Interrupt Request Detect and Priority Decoder.

The Interrupt Request Detect and Priority Encode circuitry are shown in Figure 4. The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector, V_0-V_2.

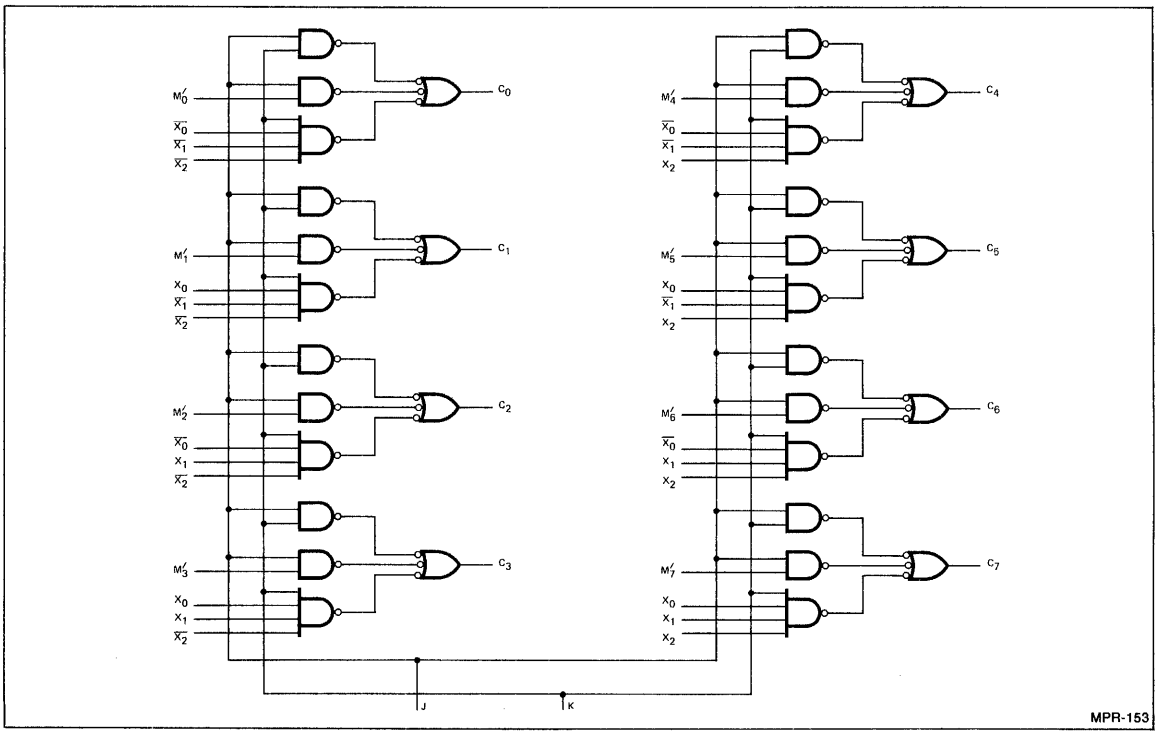


Figure 5. Clear Control.

The Clear Control logic of Figure 5 generates the eight individual clear signals for the eight Interrupt Register bits. Under microinstruction control, all interrupts, interrupts with corresponding mask register bits set, interrupts with corresponding mask bus bits equal to one, or the interrupt associated with the last vector read may be cleared. Table 1 shows the generation of the "J" and "K" control signals for each of these operations.

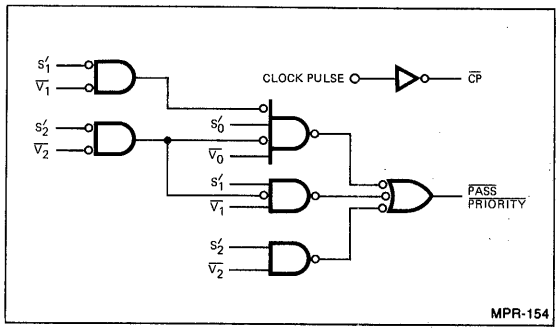


Figure 6. Three-Bit comparator.

The three-bit Comparator of Figure 6 compares the interrupt vector with the contents of the Status Register. A LOW signal level at the PASS PRIORITY output indicates that the interrupt vector is greater than or equal to the contents of the Status Register.

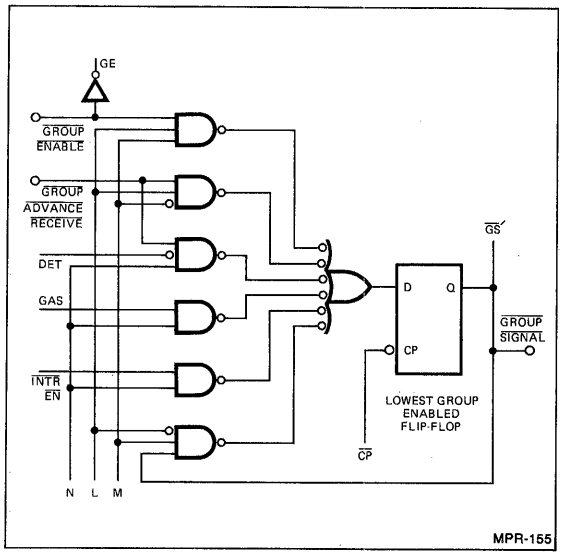


Figure 7. Group Enable Logic.

The Lowest Group Enabled Flip-Flop, Figure 7, is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the group which contains the lowest priority interrupt which will be accepted and is used to form the high order status bits. When a Load Status instruction is executed, the flip-flop is loaded from the GROUP ENABLE input. When a Master Clear instruction is executed, it is loaded from the GROUP ADVANCE RECEIVE input. The flip-flop is set HIGH when a Read Vector instruction is executed if a Group Advance is not received and no interrupt in this group is detected, if a Group Advance is sent from this group, or if interrupts from this group are disabled. For all other instructions, the flip-flop remains the same. Table 1 shows the generation of the "N", "L" and "M" control signals for these operations.

The Status Register holds the status bits and may be loaded from or read to the "S" bus as shown in Figure 8. Note that when a Load Status instruction is executed, status from the "S" bus is loaded into the Status Register only if the GROUP ENABLE input is LOW; if the GROUP ENABLE input is HIGH, the Status Register is cleared. Also note that during a Read Status instruction, the Status Register outputs are enabled onto the "S" bus only if the Lowest Group Enabled Flip-Flop of this group is LOW. When a Read Vector instruction is executed, the incrementer increases the vector by one and the result is loaded into the Status Register. Thus, the Status Register always points to the lowest level at which an interrupt will be accepted. Table 1 shows the generation of the "F", "G" and "OE-S" control signals for Status Register operations.

The Interrupt Request Logic, shown in Figure 9, generates the RIPPLE DISABLE, PARALLEL DISABLE, INTERRUPT REQUEST, GROUP ADVANCE SEND, and STATUS OVERFLOW output signals. The PARALLEL DISABLE signal is generated when the Lowest Group Enabled signal is LOW or an interrupt request in this group is detected and passes priority. The RIPPLE DISABLE signal is generated when the PARALLEL DISABLE signal is generated and also when the INTERRUPT DISABLE input signal is LOW. The INTERRUPT REQUEST output signal is generated when interrupt requests in this group are enabled and a request is detected and passes priority. The GROUP ADVANCE SEND output signal is generated when a vector of value seven is being read. The Status Overflow Flip-Flop is set LOW when a vector of value seven is read and indicates the Status Register has overflowed. The Interrupt Request Enable Flip-Flop is either set or reset by the Enable Request or Disable Request microinstructions respectively, and is used to enable or disable the INTERRUPT REQUEST output. Table 1 shows the generation of control signals "D", "E", "S" and "H".

Note that the vector outputs are enabled only when a Read Vector is being executed. Also note that when a Read Vector instruction is executed, the vector outputs will be disabled after the execution of the instruction since the Status Register is loaded with V+1, and the INTERRUPT REQUEST will no longer be generated.

The Microinstruction Decode circuitry, Figure 10, decodes the Am2914 microinstructions and generates the required internal control signals. Table 1 shows the truth table for these functions and Figure 11 shows the function tables.

Table 1. Am2914 Control Signal Truth Table.
0 = LOW, 1 = HIGH

Microinstruction						Function	Mask Register				Status Register			Group Enable		Clear Control		Irpt Request Enable		Vector Hold Register		Other	
Decimal	$\overline{I_E}$	I_3	I_2	I_1	I_0	Description	A	B	C	OE-M	F	G	$\overline{OE\text{-}S}$	L	M	J	K	D	E	N	R	S	H
0	0	0	0	0	0	Master Clear	0	0	1	0	0	0	1	1	0	1	1	0	1	0	0	1	1
1	0	0	0	0	1	Clear All Interrupts	1	0	1	0	0	1	1	0	1	1	1	1	X	0	0	1	0
2	0	0	0	1	0	Clear Intr Via M Bus	1	0	1	0	0	1	1	0	1	1	0	1	X	0	1	1	0
3	0	0	0	1	1	Clear Intr Via M Reg	1	0	1	1	0	1	1	0	1	1	0	1	X	0	1	1	0
4	0	0	1	0	0	Clear Intr, Last Vector	1	0	1	0	0	1	1	0	1	0	1/0	1	X	0	0	1	0
5	0	0	1	0	1	Read Vector	1	0	1	0	0/1	0	1	0	0	0	0	1	X	1	0	0	1
6	0	0	1	1	0	Read Status Reg	1	0	1	0	0	1	0	0	1	0	0	1	X	0	1	1	0
7	0	0	1	1	1	Read Mask Reg	1	0	1	1	0	1	1	0	1	0	0	1	X	0	1	1	0
8	0	1	0	0	0	Set Mask Reg	0	0	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
9	0	1	0	0	1	Load Status Reg	1	0	1	0	1	1	1	1	1	0	0	1	X	0	1	1	1
10	0	1	0	1	0	Bit Clear Mask Reg	0	1	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
11	0	1	0	1	1	Bit Set Mask Reg	1	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
12	0	1	1	0	0	Clear Mask Reg	0	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
13	0	1	1	0	1	Disable Request	1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0
14	0	1	1	1	0	Load Mask Reg	0	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
15	0	1	1	1	1	Enable Request	1	0	1	0	0	1	1	0	1	0	0	0	1	0	1	1	0
X	1	X	X	X	X	Instruction Disable	1	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0

Notes: 1. Control line "F" during "READ VECTOR" instruction is 0 when "PASS ALL" is LOW and 1 when "PASS ALL" is HIGH.
2. Control line "K" during "Clear Intr, Last Vector" instruction is 0 when "Vector Clear Enable" is LOW and 1 when "Vector Clear Enable" is HIGH.

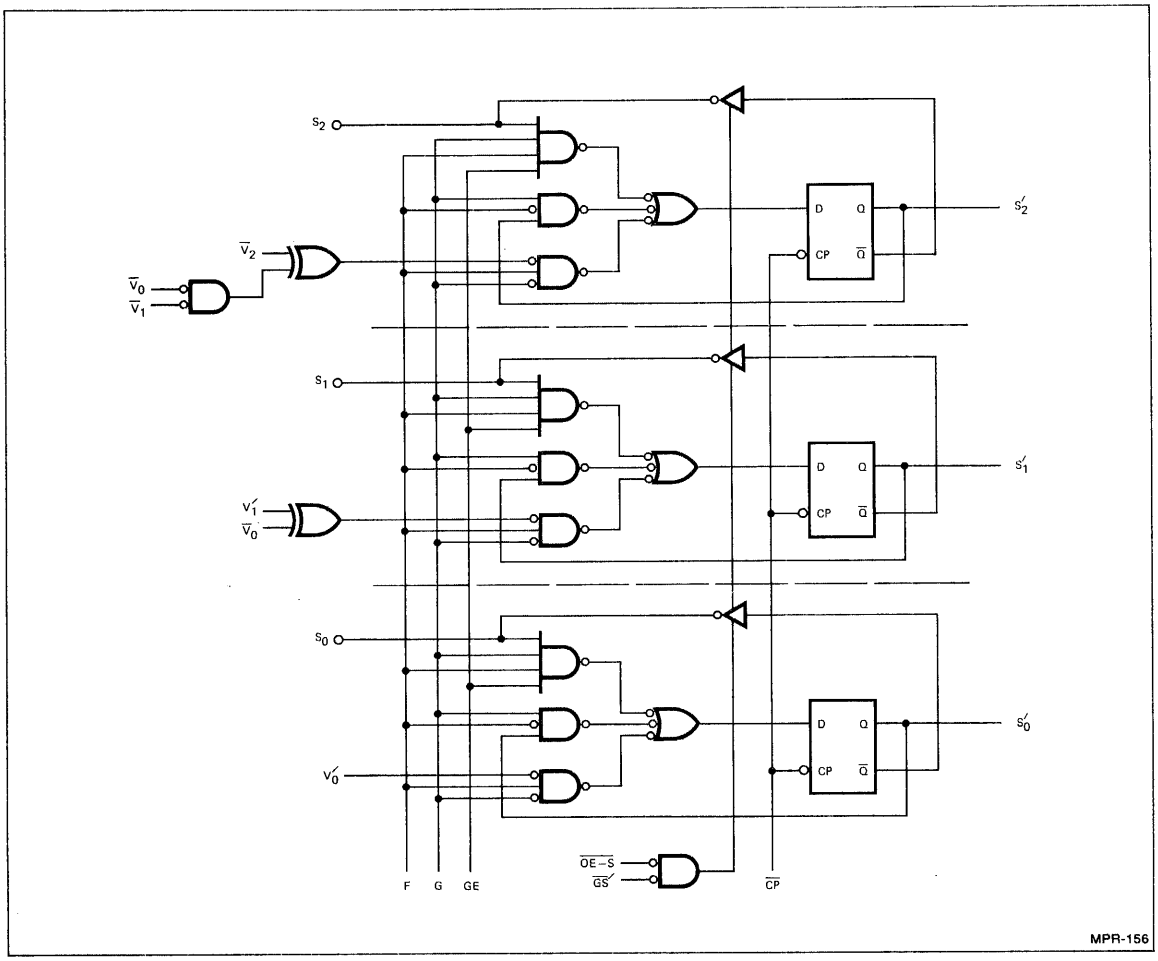


Figure 8. Incrementer and Status Register.

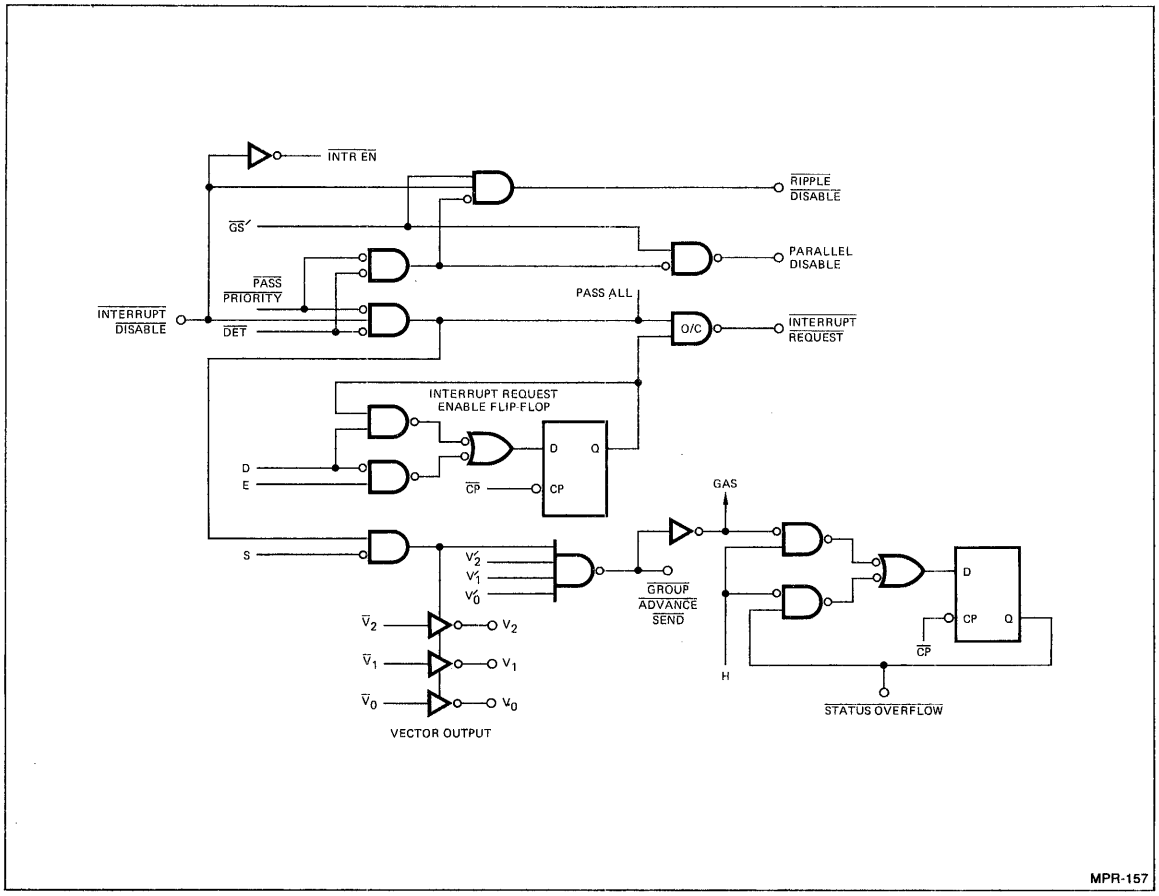


Figure 9. Interrupt Request Logic.

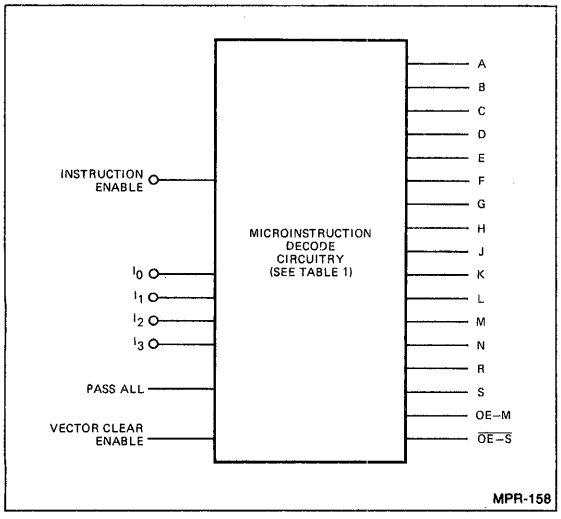


Figure 10.

MASK REGISTER

A	B	C	FUNCTION
0	0	0	SET
0	0	1	CLEAR
0	1	0	BIT CLEAR
0	1	1	LOAD
1	0	1	HOLD
1	1	1	BIT SET

CLEAR CONTROL

J	K	FUNCTION
0	0	NO CLEAR
0	1	CLEAR IRPT, VECTOR
1	0	CLEAR IRPTS VIA M
1	1	CLEAR ALL IRPTS

VECTOR HOLD REGISTER

N	FUNCTION
0	HOLD
1	LOAD

LOWEST GROUP ENABLED FLIP-FLOP

L	M	FUNCTION
0	0	UPDATE
0	1	HOLD
1	0	LOAD VIA GROUP ADVANCE RECEIVE
1	1	LOAD VIA GROUP ENABLE

STATUS REGISTER

F	G	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD VECTOR + 1
1	1	LOAD VIA "S" BUS

INTERRUPT REQUEST ENABLE FLIP-FLOP

D	E	FUNCTION
0	0	DISABLE IRPTS
0	1	ENABLE IRPTS
1	X	HOLD

VECTOR CLEAR ENABLE FLIP-FLOP

N	R	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD

STATUS OVERFLOW FLIP-FLOP

H	FUNCTION
0	HOLD
1	LOAD

Figure 11. Control Function Tables.

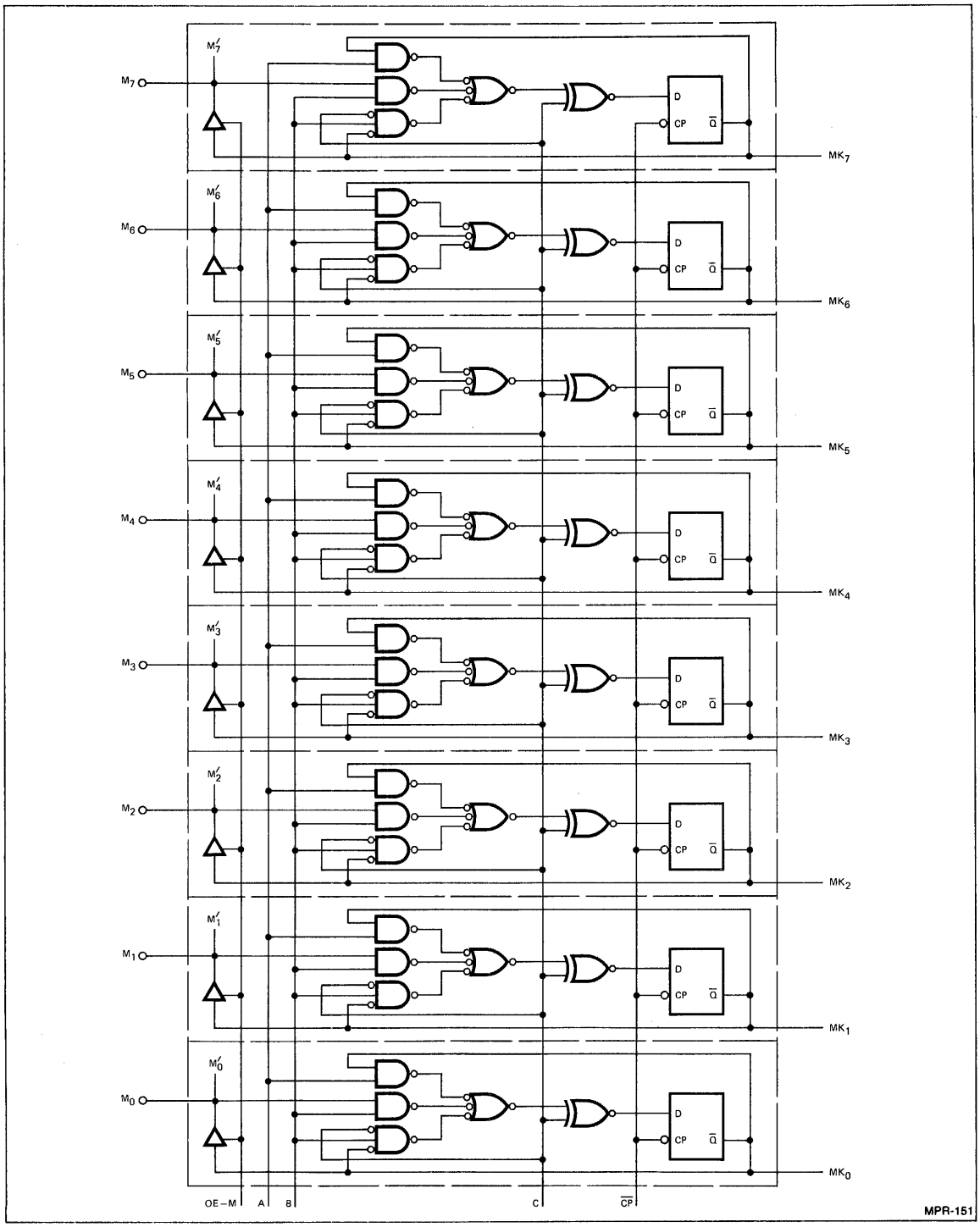


Figure 3. Mask Register.

The Mask Register shown in Figure 3 holds the eight mask bits associated with the eight interrupt levels. The register may be set or cleared, bit set or bit cleared from the "M" bus, or loaded or read to the "M" bus. Table 1 shows the generation of the "A", "B", "C" and "OE-M" control signals for each of these operations.

Am2915A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

2

FUNCTIONAL DESCRIPTION

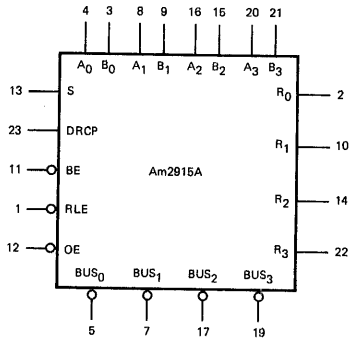
The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

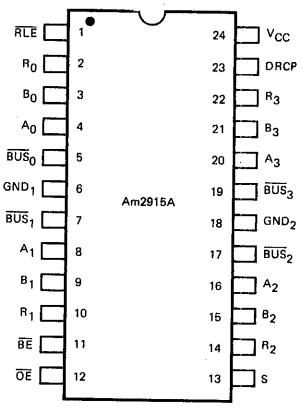
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-159

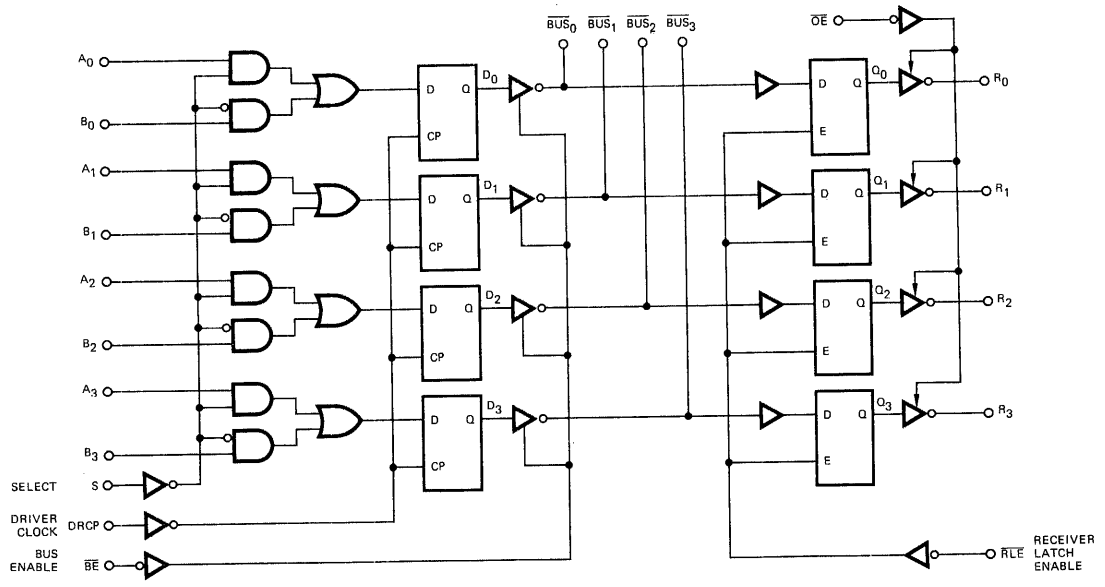
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-160

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2915AXM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	µA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	µA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$V			50	μA
			$V_O = 0.4$V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915AXM Min.	Am2915AXM Typ. (Note 2)	Am2915AXM Max.	Am2915AXC Min.	Am2915AXC Typ. (Note 2)	Am2915AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	$C_L = 15$pF, $R_L = 2.0$kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		$C_L = 5$pF, $R_L = 2.0$kΩ		14	26		14	23	

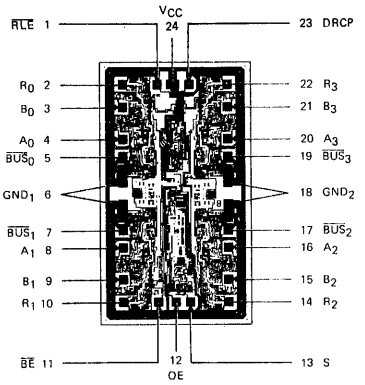
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

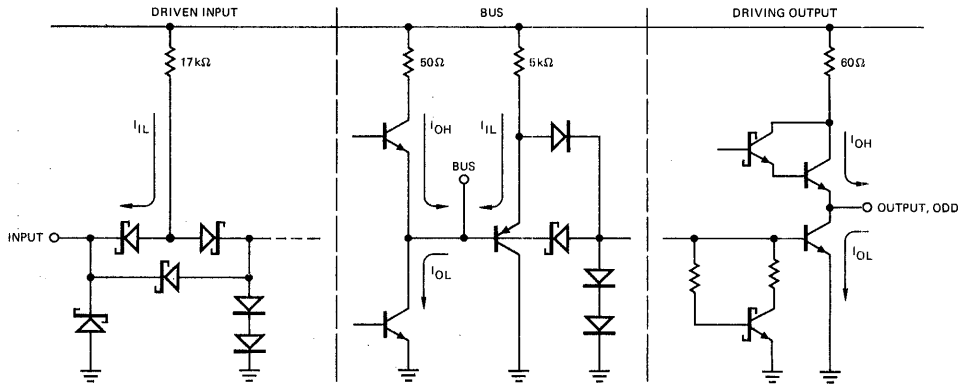
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2915APC	P-24	C	C-1
AM2915ADC	D-24	C	C-1
AM2915ADC-B	D-24	C	B-1
AM2915ADM	D-24	M	C-3
AM2915ADM-B	D-24	M	B-3
AM2915AFM	F-24-1	M	C-3
AM2915AFM-B	F-24-1	M	B-3
AM2915AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2915AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

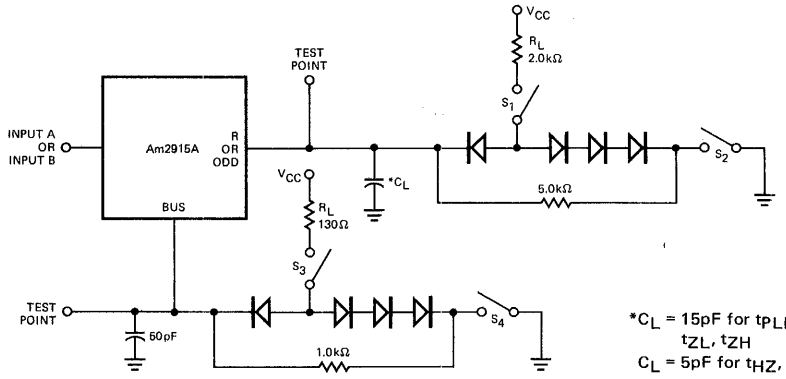
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-162

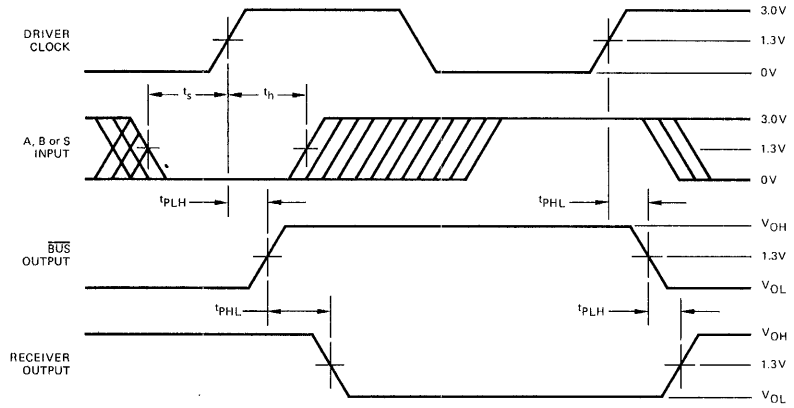
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

MPR-163

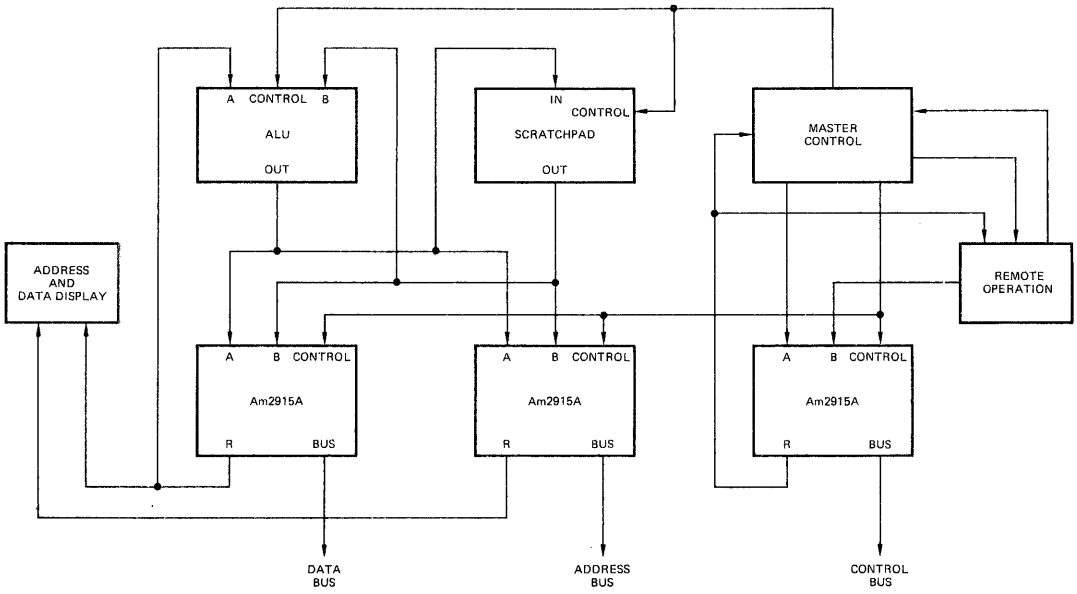
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-164

APPLICATIONS



The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-165

Am2916A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

2

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

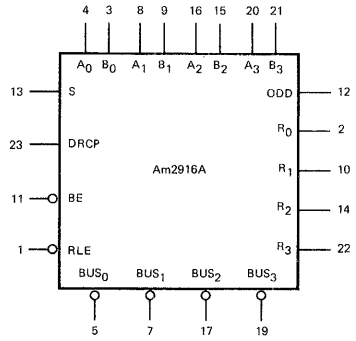
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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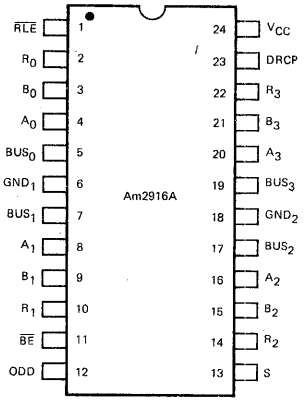
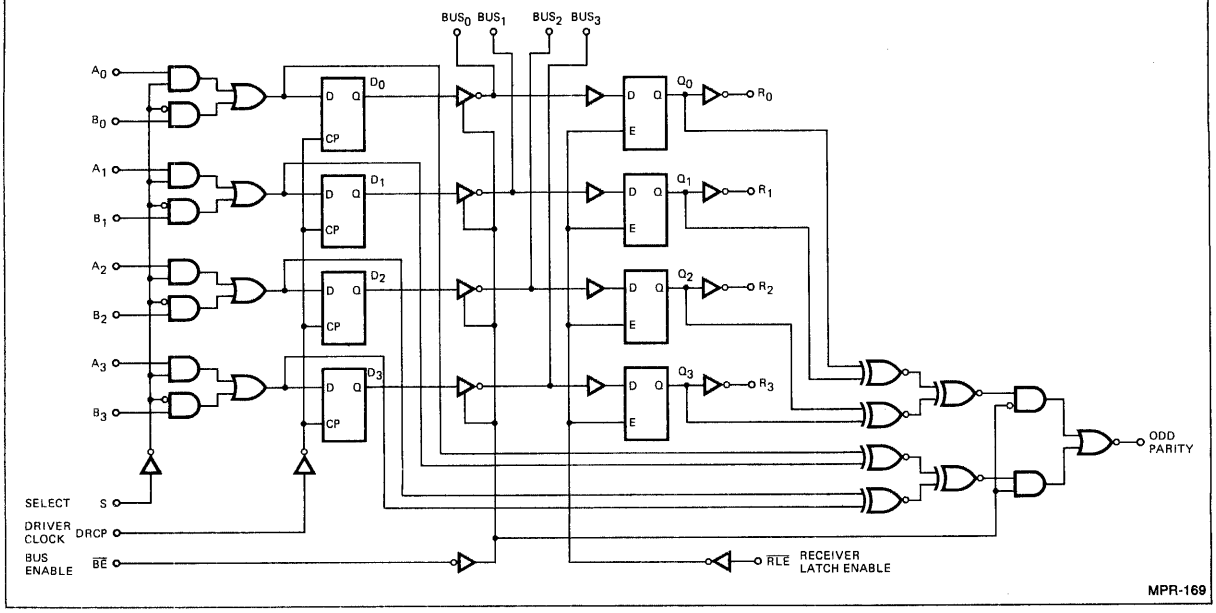
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-168

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75 V	V_{CC} MAX. = 5.25 V
Am2916AXM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. = 4.50 V	V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

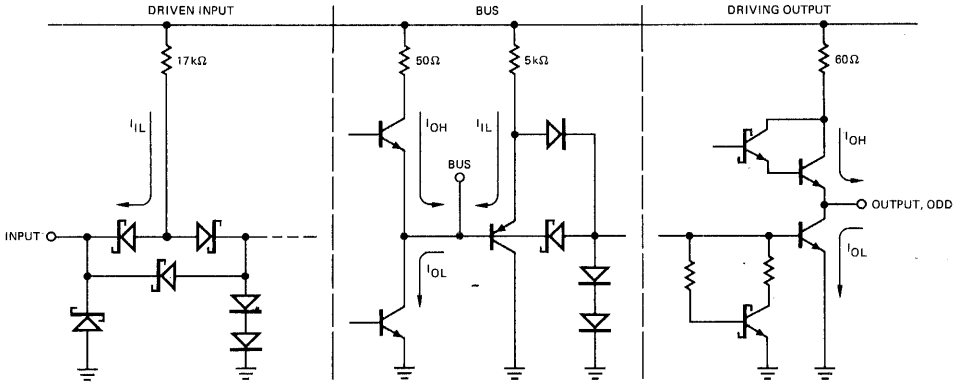
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM Min.	Am2916AXM Typ. (Note 2)	Am2916AXM Max.	Am2916AXC Min.	Am2916AXC Typ. (Note 2)	Am2916AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 130 Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)		15			12			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 15 pF, R_L = 2.0 kΩ		18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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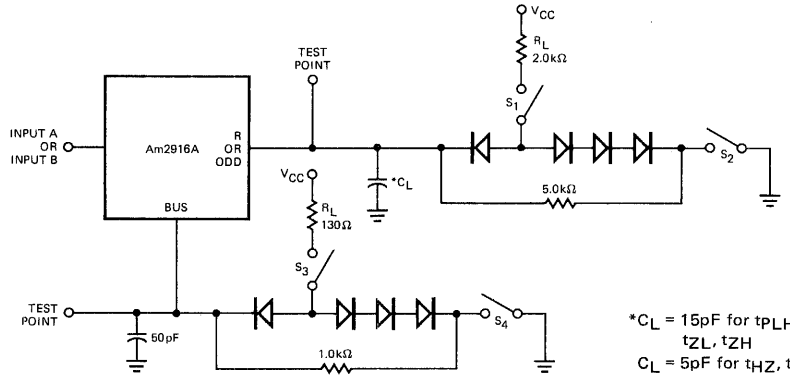
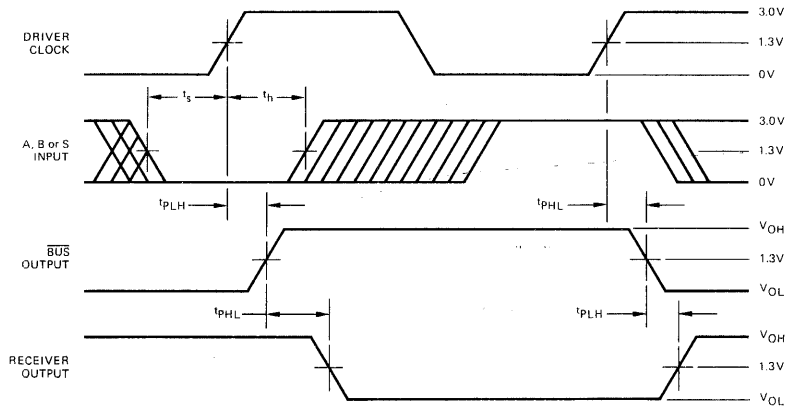
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

MPR-171

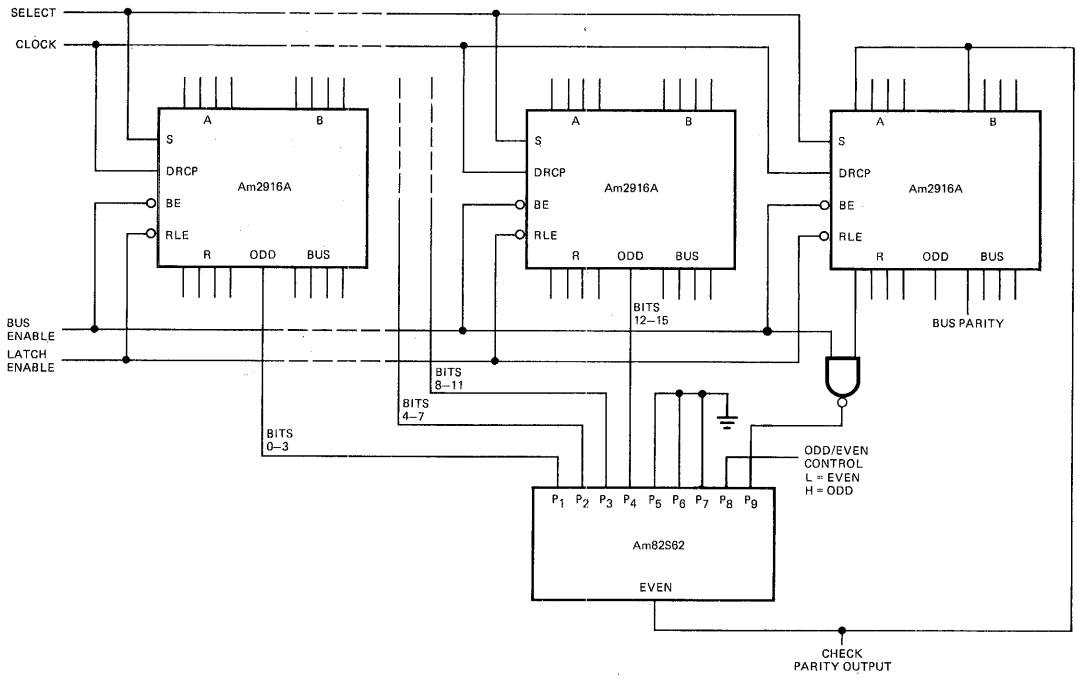
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-172

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-173

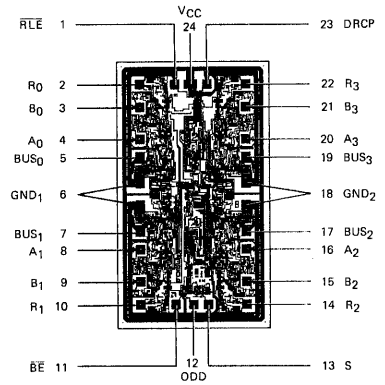
2

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care I = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



'DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2916APC	P-24	C	C-1
AM2916ADC	D-24	C	C-1
AM2916ADC-B	D-24	C	B-1
AM2916ADM	D-24	M	C-3
AM2916ADM-B	D-24	M	B-3
AM2916AFM	F-24-1	M	C-3
AM2916AFM-B	F-24-1	M	B-3
AM2916AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2916AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2917A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

2

FUNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

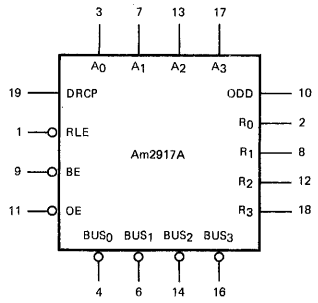
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

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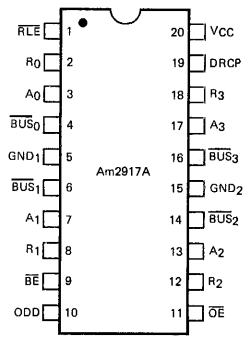
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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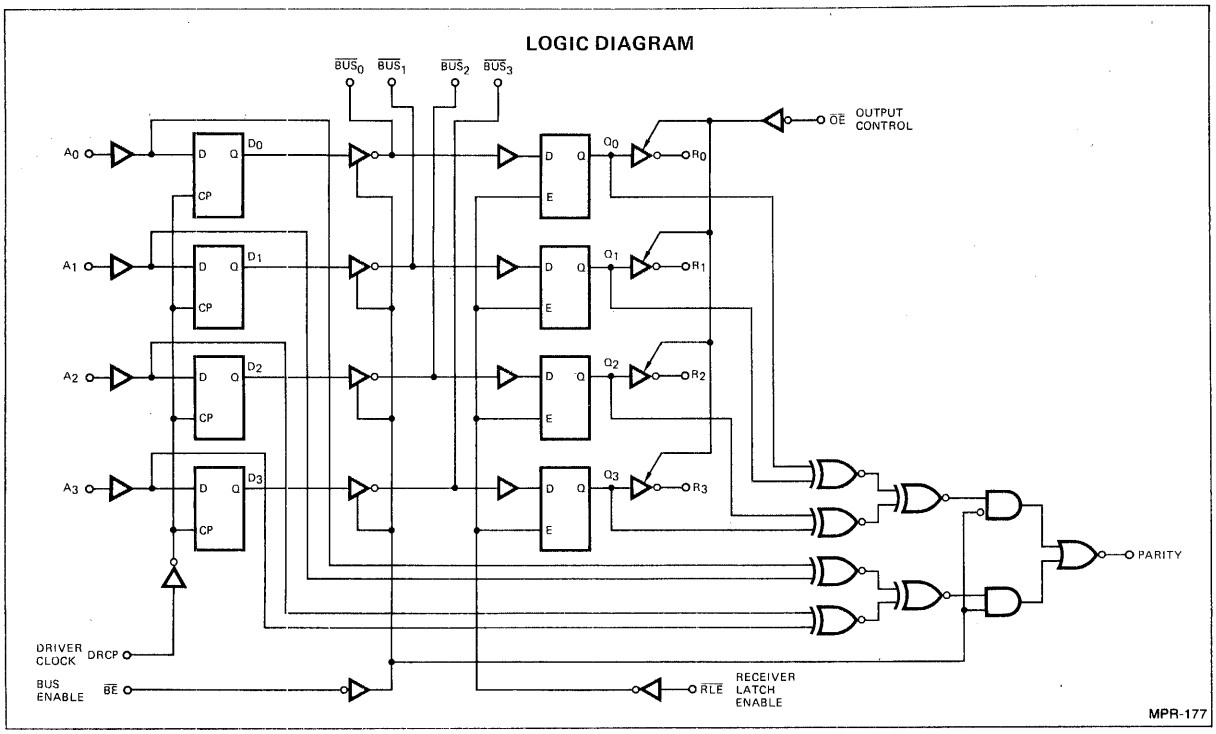
LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20 mA	2.4			Volts
			MIL, I_{OH} = −15 mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

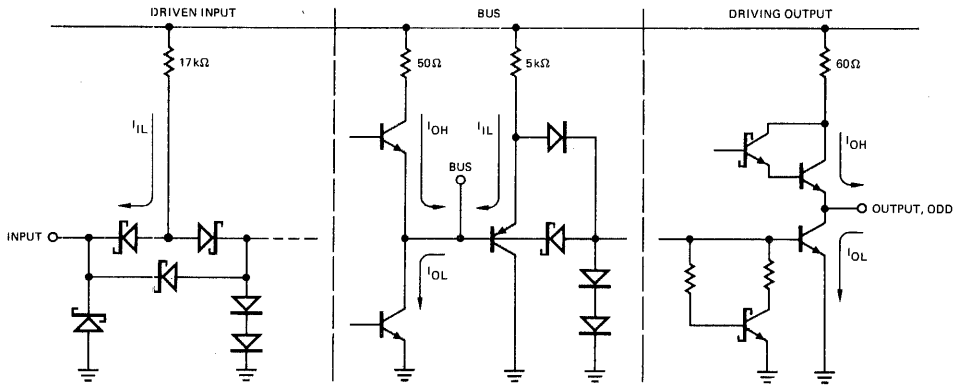
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$V			50	μA
			$V_O = 0.4$V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917AXM Min.	Am2917AXM Typ. (Note 2)	Am2917AXM Max.	Am2917AXC Min.	Am2917AXC Typ. (Note 2)	Am2917AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_LBUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs		15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)	C_L = 15pF, R_L = 2.0kΩ	15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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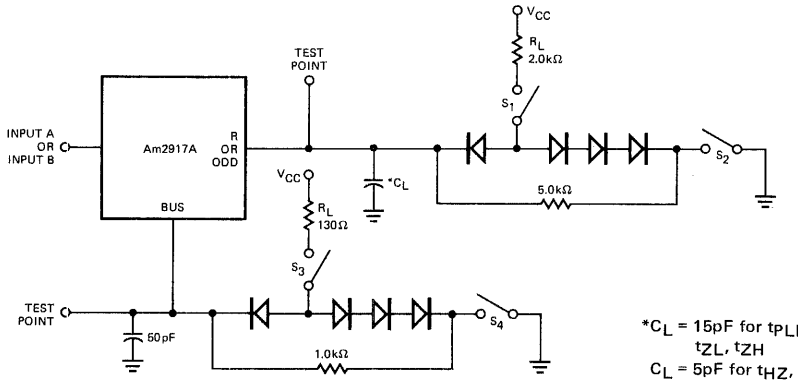
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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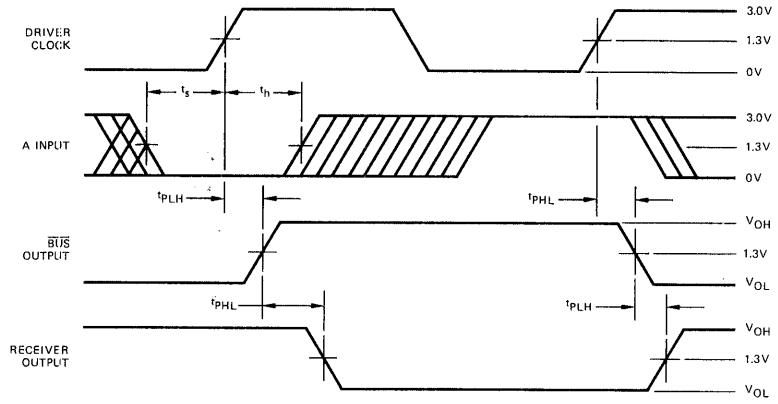
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

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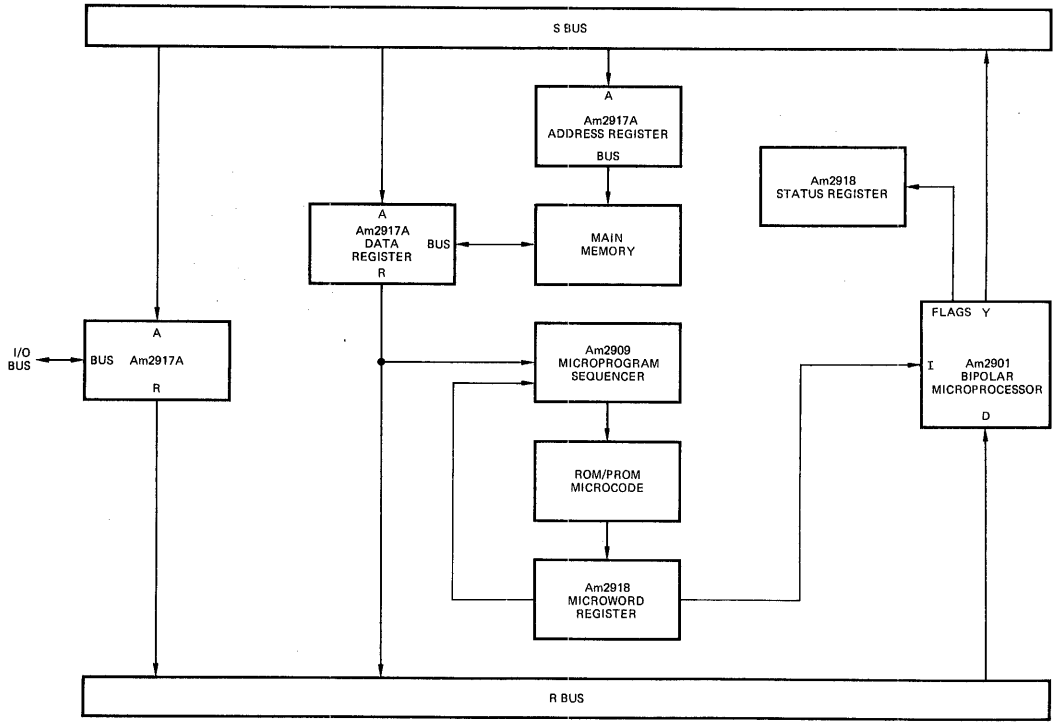
APPLICATIONS



The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

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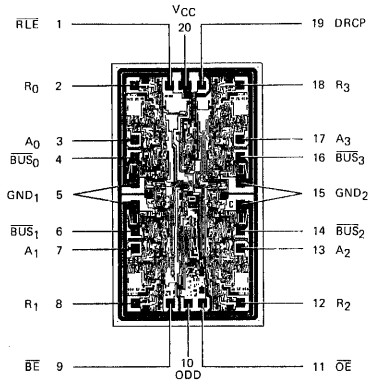
FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	Z	X	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care I = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2917APC	P-20	C	C-1
AM2917ADC	D-20	C	C-1
AM2917ADC-B	D-20	C	B-1
AM2917ADM	D-20	M	C-3
AM2917ADM-B	D-20	M	B-3
AM2917AFM	F-20	M	C-3
AM2917AFM-B	F-20	M	B-3
AM2917AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2917AXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

Am2918

Quad D Register With Standard And Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

2

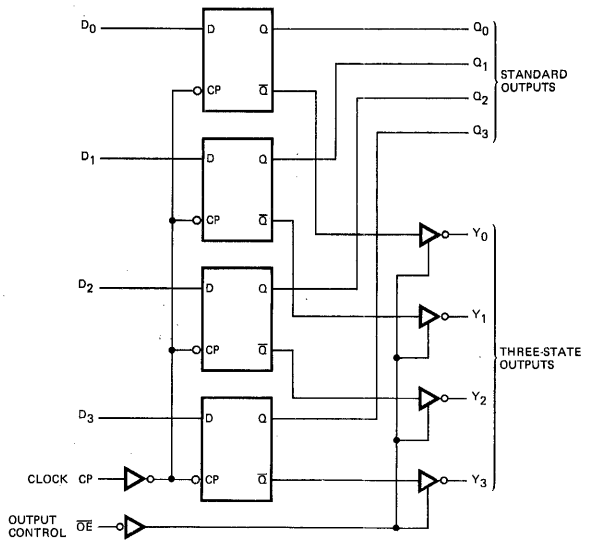
FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration – especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

LOGIC DIAGRAM



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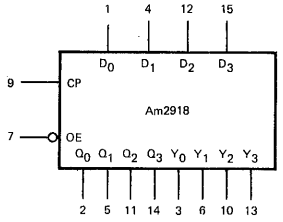
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2918PC	P-16	C	C-1
AM2918DC	D-16	C	C-1
AM2918DC-B	D-16	C	B-1
AM2918DM	D-16	M	C-3
AM2918DM-B	D-16	M	B-3
AM2918FM	F-16	M	C-3
AM2918FM-B	F-16	M	B-3
AM2918XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2918XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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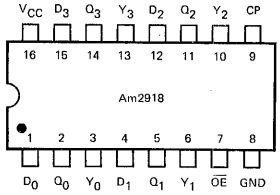
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2918XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2918XM T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA; V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15 pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0 pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

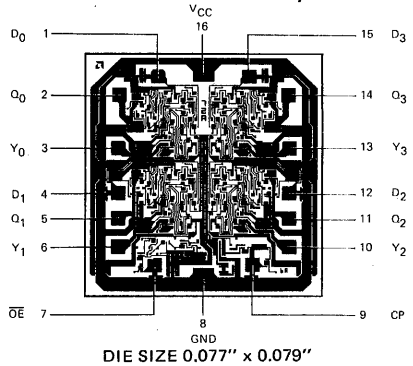
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

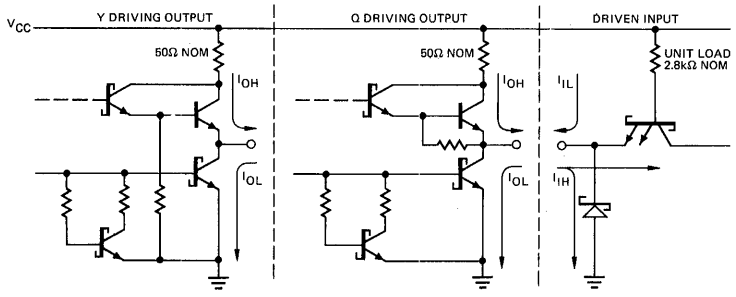
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

Metallization and Pad Layout



DIE SIZE 0.077" x 0.079"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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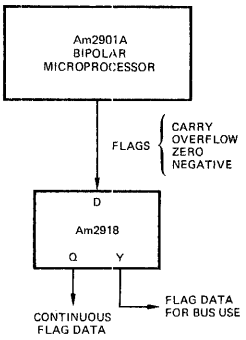
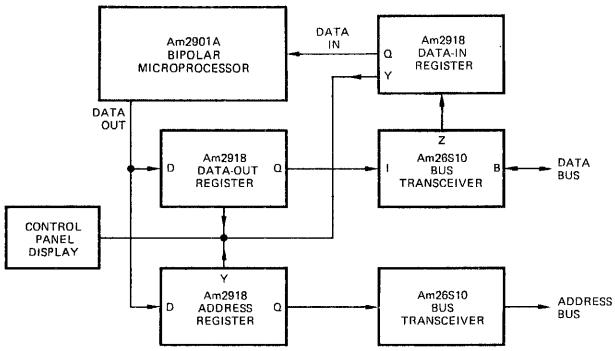
APPLICATIONS



The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.

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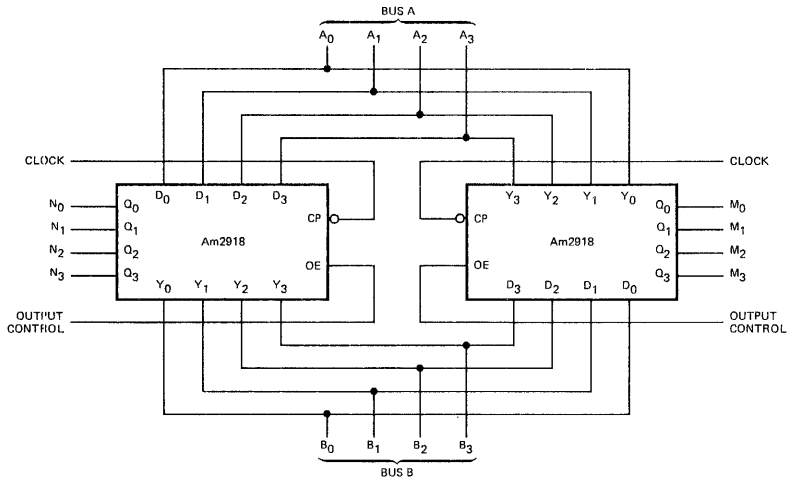

The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.

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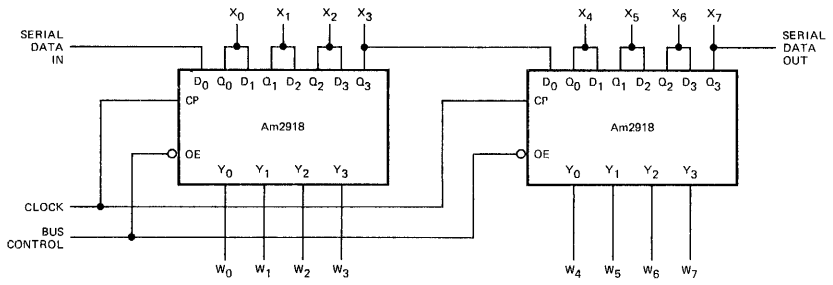


8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

MPR-189

Am29LS18

Quad D Register With Standard And Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

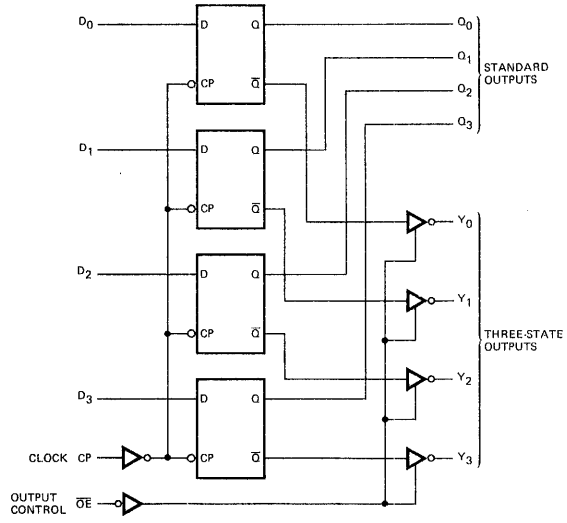
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

LOGIC DIAGRAM



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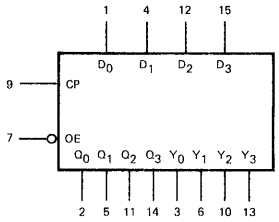
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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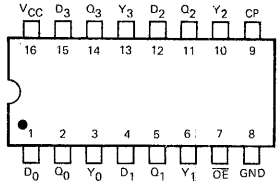
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75 V MAX. = 5.25 V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50 V MAX. = 5.50 V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q, $I_{OH} = -660\mu A$	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, $I_{OH} = -1.0mA$	2.4	3.4		
				COM'L, $I_{OH} = 2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					-1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					-0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				-20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			-15		-85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +V_{CC} max.
DC Input Voltage	-0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width	LOW	18			ns	
		HIGH	15				
t_s	Data		15			ns	
t_h	Data		5.0			ns	
t_{ZH}	$\overline{OE}$ to Y_i			7.0	11	ns	
t_{ZL}				8	12		
t_{HZ}	$\overline{OE}$ to Y_i			14	21	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz	

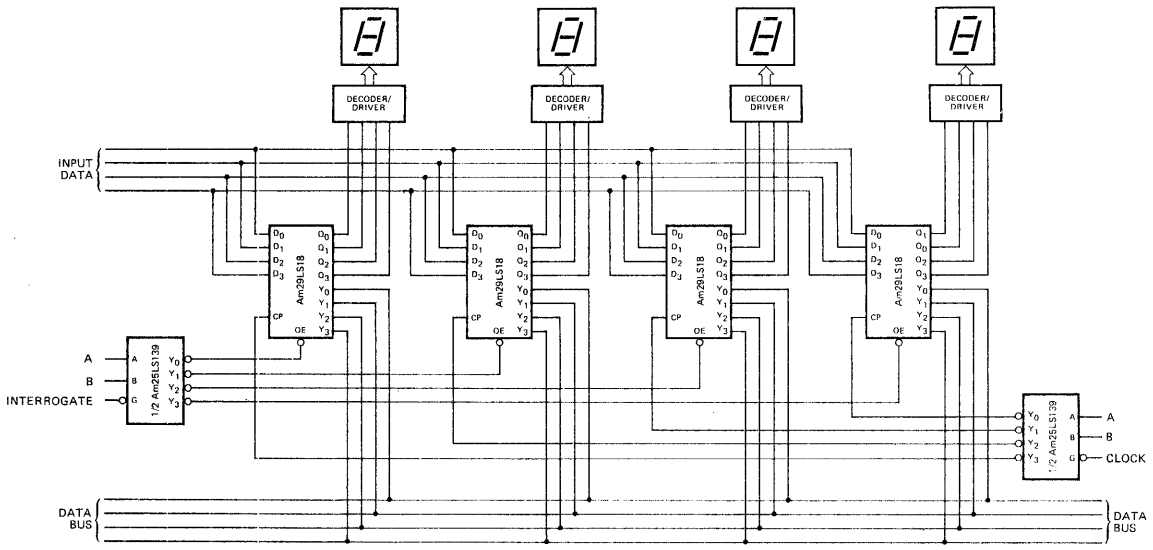
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am29LS18PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am29LS18PC, DC Max.	Am29LS18DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am29LS18DM, FM Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			38		45	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		5.0		5.0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			15		17	ns	
t_{ZL}				16		17		
t_{HZ}	$\overline{OE}$ to Y_i			27		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency (Note 1)		30				MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

APPLICATIONS



The Am29LS18 used as a display register with bus interrogate capability.

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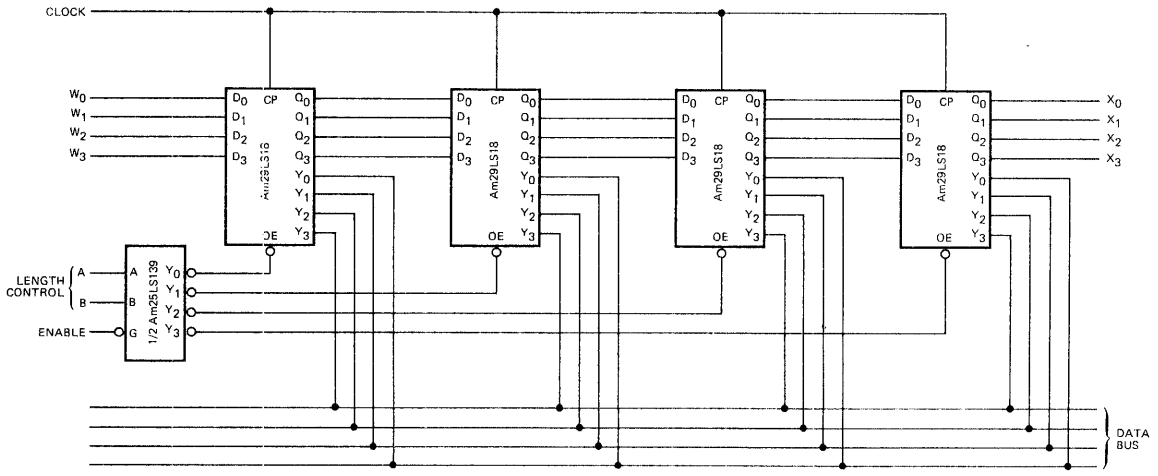
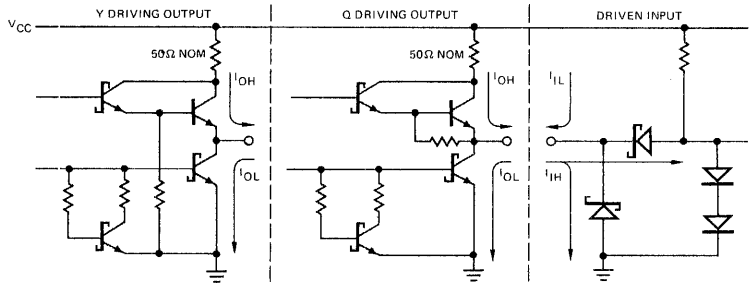


The Am29LS18 as a variable length (1, 2, 3 or 4 word) shift register.

MPR-194

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

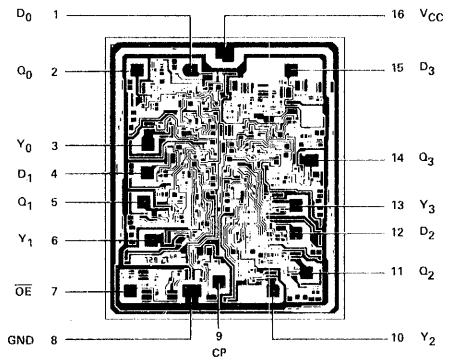
L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

2

Metallization and Pad Layout



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29LS18PC	P-16	C	C-1
AM29LS18DC	D-16	C	C-1
AM29LS18DC-B	D-16	C	B-1
AM29LS18DM	D-16	M	C-3
AM29LS18DM-B	D-16	M	B-3
AM29LS18FM	F-16	M	C-3
AM29LS18FM-B	F-16	M	B-3
AM29LS18XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29LS18XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2919

Quad Register With Dual Three-State Outputs

DISTINCTIVE CHARACTERISTICS

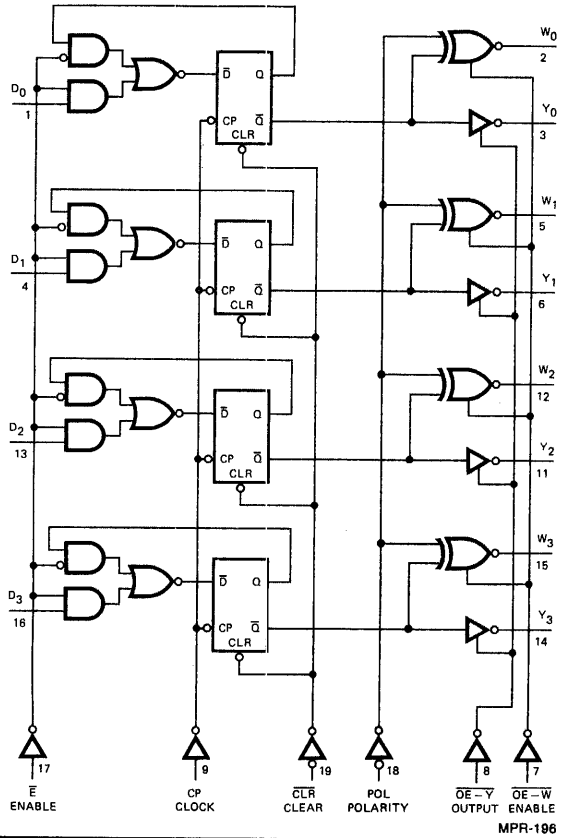
- Two sets of three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs
- 100% reliability assurance testing in compliance with MIL STD-883

FUNCTIONAL DESCRIPTION

The Am2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am2919 is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM



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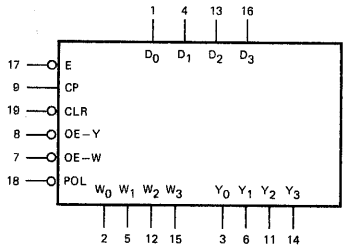
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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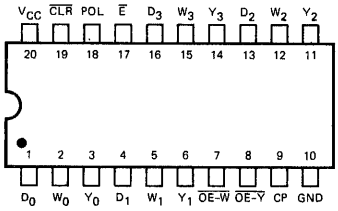
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				-1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				-0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			-20	µA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		-15		-85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	MIL		24	36	mA
			COM'L		24	39	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +V_{CC} max.
DC Input Voltage	-0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW H = HIGH Z = High Impedance NC = No Change X = Don't Care ↑ = LOW-to-HIGH Transition

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i (Either Polarity)			24	36	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2919PC, DC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am2919DM, FM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i (Either Polarity)			41		43	ns	
t_{PHL}				44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF R_L = 2.0kΩ

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

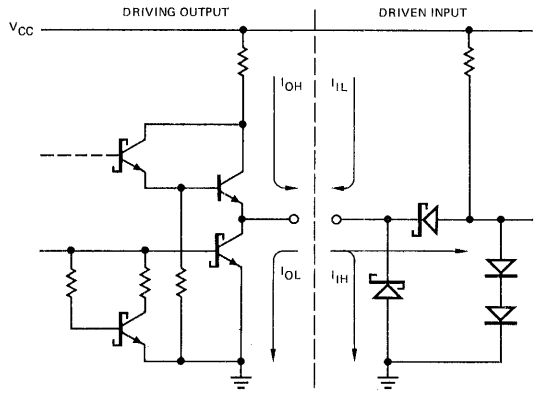
D_i	Any of the four D flip-flop data lines.
$\overline{E}$	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
CP	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
$\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$	Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.
Y_i	Any of the four non-inverting three-state output lines.
W_i	Any of the four three-state outputs with polarity control.
POL	Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
$\overline{CLR}$	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE\text{-}W}$	1.0	–	–	–	–
8	$\overline{OE\text{-}Y}$	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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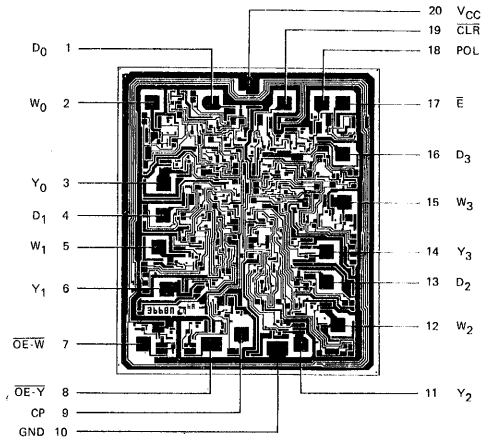
Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

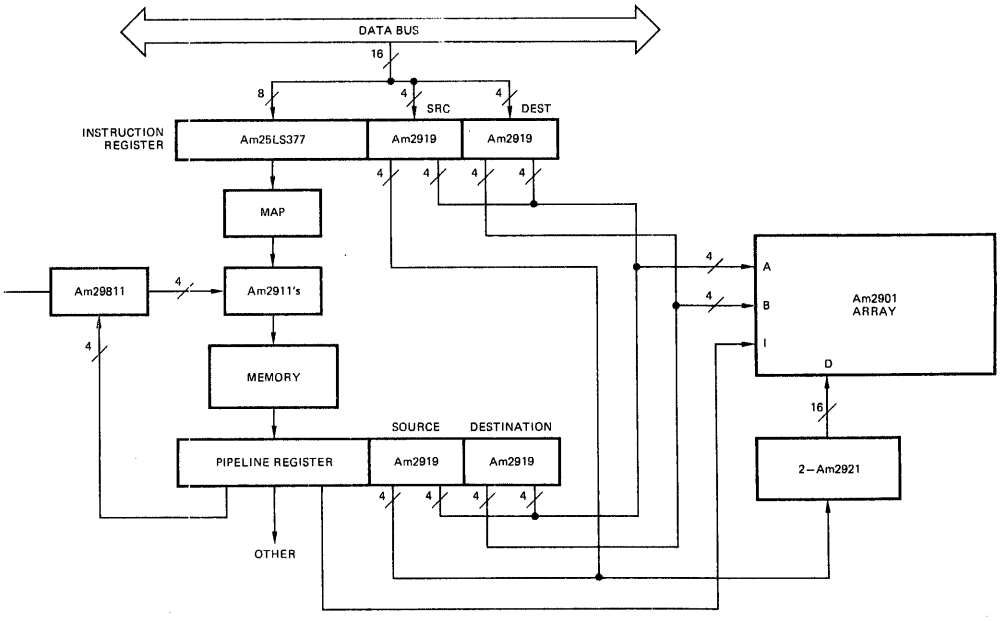
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2919PC	P-20	C	C-1
AM2919DC	D-20	C	C-1
AM2919DC-B	D-20	C	B-1
AM2919DM	D-20	M	C-3
AM2919DM-B	D-20	M	B-3
AM2919FM	F-20	M	C-3
AM2919FM-B	F-20	M	B-3
AM2919XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2919XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



The Am2919 provides for easy control of the selection of source and destination register addresses for the Am2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the Am2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the Am2901. Two registers can be selected for the Am2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the Am2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

MPR-200

Am2920

Octal D-Type Flip-Flop With Clear, Clock Enable And Three-State Control

2

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2920 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

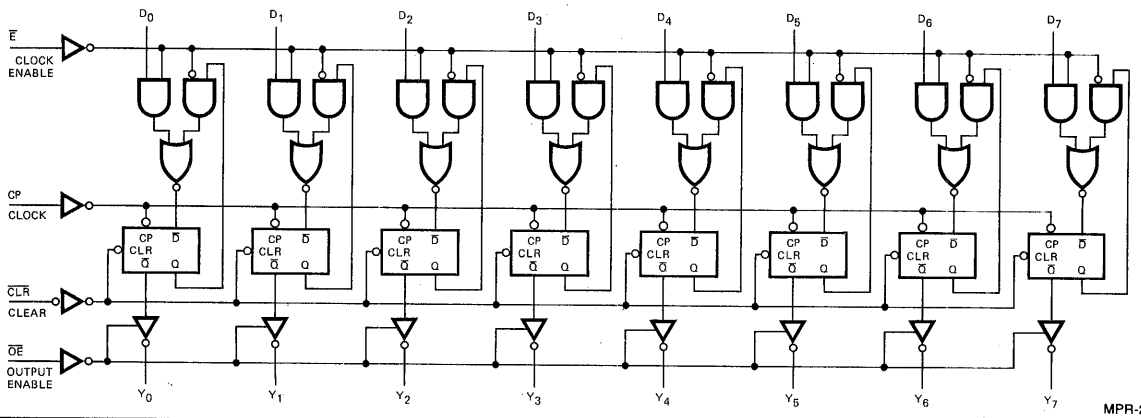
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package.

LOGIC DIAGRAM



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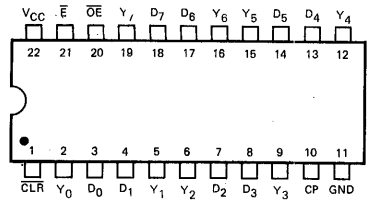
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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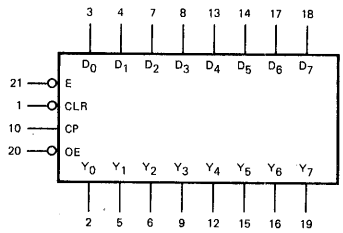
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2920PC	P-22	C	C-1
AM2920DC	D-22	C	C-1
AM2920DC-B	D-22	C	B-1
AM2920DM	D-22	M	C-3
AM2920DM-B	D-22	M	B-3
AM2920FM	F-22	M	C-3
AM2920FM-B	F-22	M	B-3
AM2920XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2920XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2920PC,DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am2920PC,DC Max.	Am2920DM,FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am2920DM,FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0 pF, R_L = 2.0 kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A; Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i — The D flip-flop data inputs.

$\overline{CLR}$ — When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP — Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i — The register three-state outputs.

$\overline{E}$ — Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ — Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

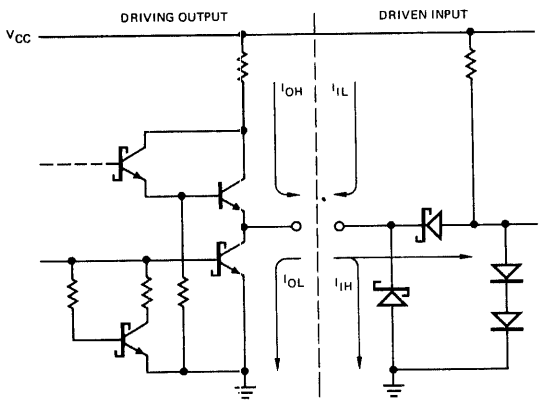
H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Am2920				
		Input	Output HIGH		Output LOW	
Pin No.'s	Input/Output	Load	MIL	COM'L	MIL	COM'L
1	$\overline{CLR}$	1	–	–	–	–
2	Y_0	–	50	130	22	22
3	D_0	1	–	–	–	–
4	D_1	1	–	–	–	–
5	Y_1	–	50	130	22	22
6	Y_2	–	50	130	22	22
7	D_2	1	–	–	–	–
8	D_3	1	–	–	–	–
9	Y_3	–	50	130	22	22
10	CP	1	–	–	–	–
11	GND	–	–	–	–	–
12	Y_4	–	50	130	22	22
13	D_4	1	–	–	–	–
14	D_5	1	–	–	–	–
15	Y_5	–	50	130	22	22
16	Y_6	–	50	130	22	22
17	D_6	1	–	–	–	–
18	D_7	1	–	–	–	–
19	Y_7	–	50	130	22	22
20	$\overline{OE}$	1	–	–	–	–
21	$\overline{E}$	1	–	–	–	–
22	V_{CC}	–	–	–	–	–

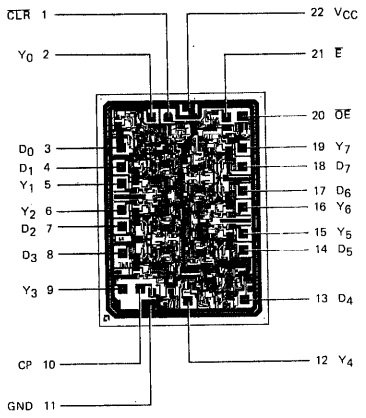
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

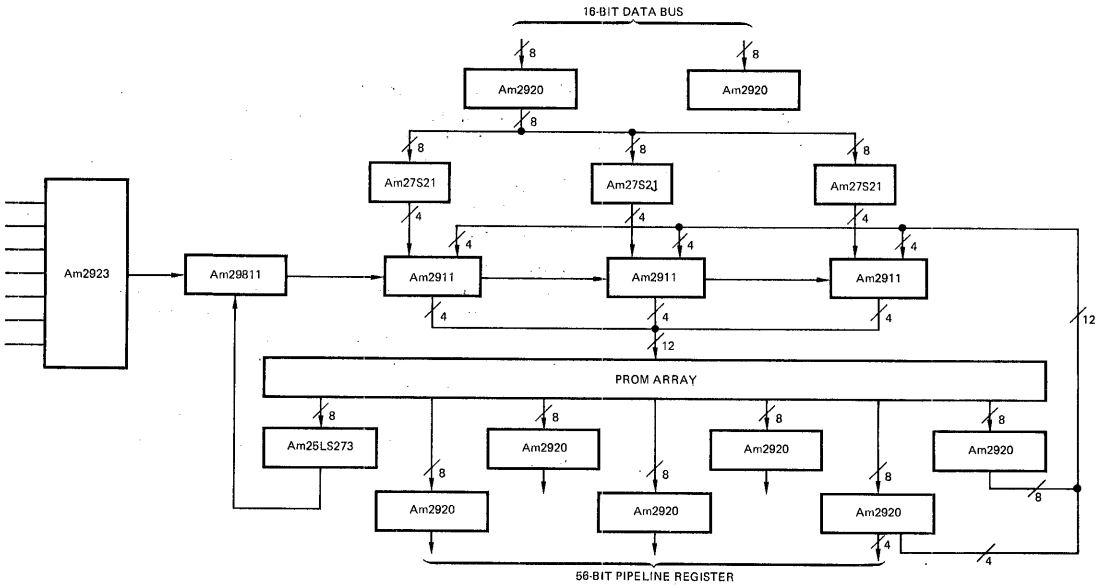
MPR-204

Metallization and Pad Layout



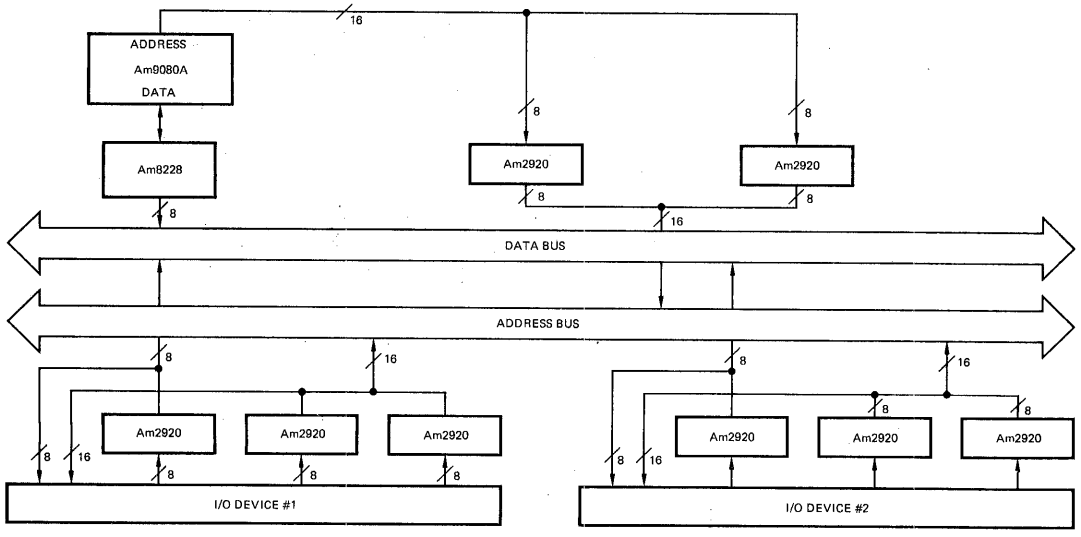
DIE SIZE 0.080" X 0.111"

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.

MPR-205



The Am2920 is a useful device in interfacing with the Am9080A system buses.

MPR-206

Am2921

One-of-Eight Decoder
With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- AC parameters specified over operating temperature and power supply ranges.
- 100% reliability assurance testing in compliance with MIL-STD-883

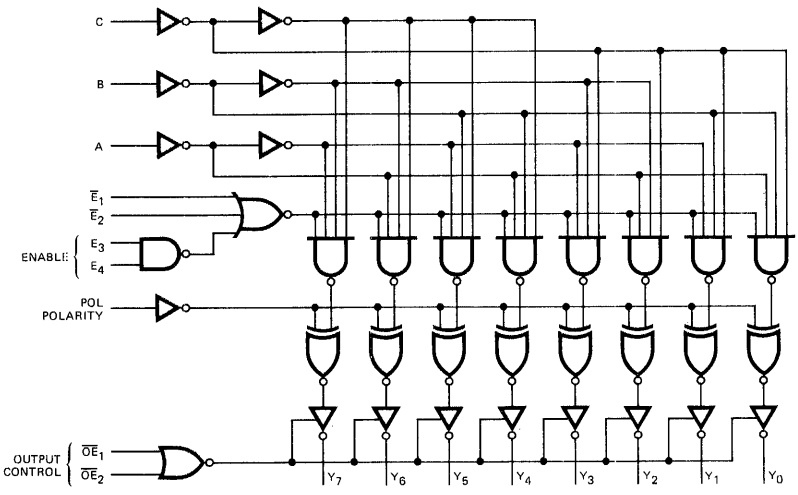
FUNCTIONAL DESCRIPTION

The Am2921 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B, and C, which are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM
One-of-Eight Decoder



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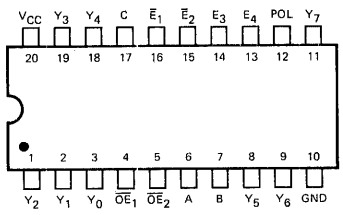
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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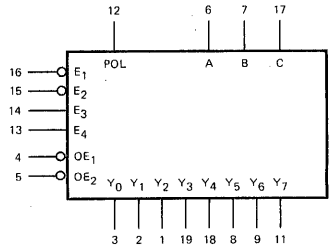
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-209

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = 1.0mA$ (MIL)	2.4	3.4		Volts
			$I_{OH} = -2.6mA$ (COM'L)	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				-1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				-0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			-20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		-15		-85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND ; $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2 = 4.5V$.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +V_{CC} max.
DC Input Voltage	-0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

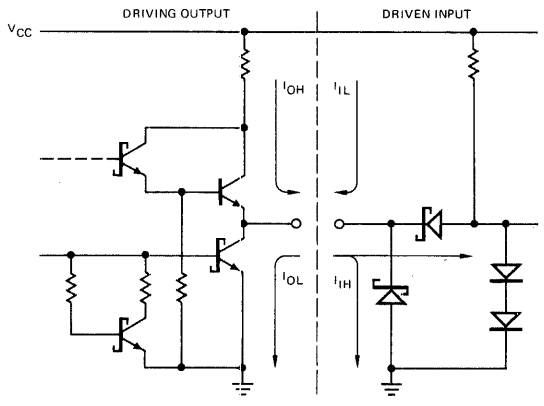
Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		20	30	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	22		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		19	28	ns	
t_{PHL}			20	30		
t_{PLH}	E_3, E_4 to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			20	30		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			20	30		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2921PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		Am2921DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	A, B, C to Y_i		36		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			29		37		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		34		39	ns	
t_{PHL}			38		45		
t_{PLH}	E_3, E_4 to Y_i		38		45	ns	
t_{PHL}			43		52		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		38		45	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		29		33	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			33		36		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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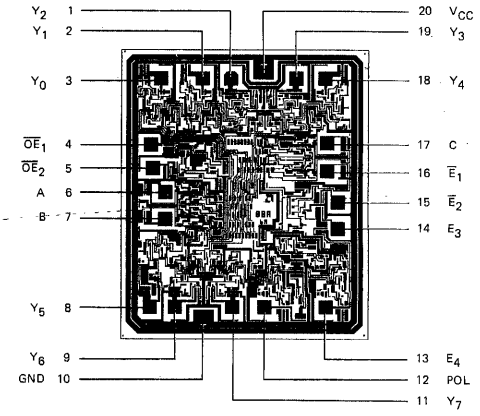
Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D — The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ — The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 — The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL — Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ — Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

Y_i — The eight outputs for the decoder/demultiplexer.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	Y_2	—	50	130	33	33
2	Y_1	—	50	130	33	33
3	Y_0	—	50	130	33	33
4	$\overline{OE}_1$	1.0	—	—	—	—
5	$\overline{OE}_2$	1.0	—	—	—	—
6	A	1.0	—	—	—	—
7	B	1.0	—	—	—	—
8	Y_5	—	50	130	33	33
9	Y_6	—	50	130	33	33
10	GND	—	—	—	—	—
11	Y_7	—	50	130	33	33
12	POL	1.0	—	—	—	—
13	E_4	1.0	—	—	—	—
14	E_3	1.0	—	—	—	—
15	$\overline{E}_2$	1.0	—	—	—	—
16	$\overline{E}_1$	1.0	—	—	—	—
17	C	1.0	—	—	—	—
18	Y_4	—	50	130	33	33
19	Y_3	—	50	130	33	33
20	V_{CC}	—	—	—	—	—

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

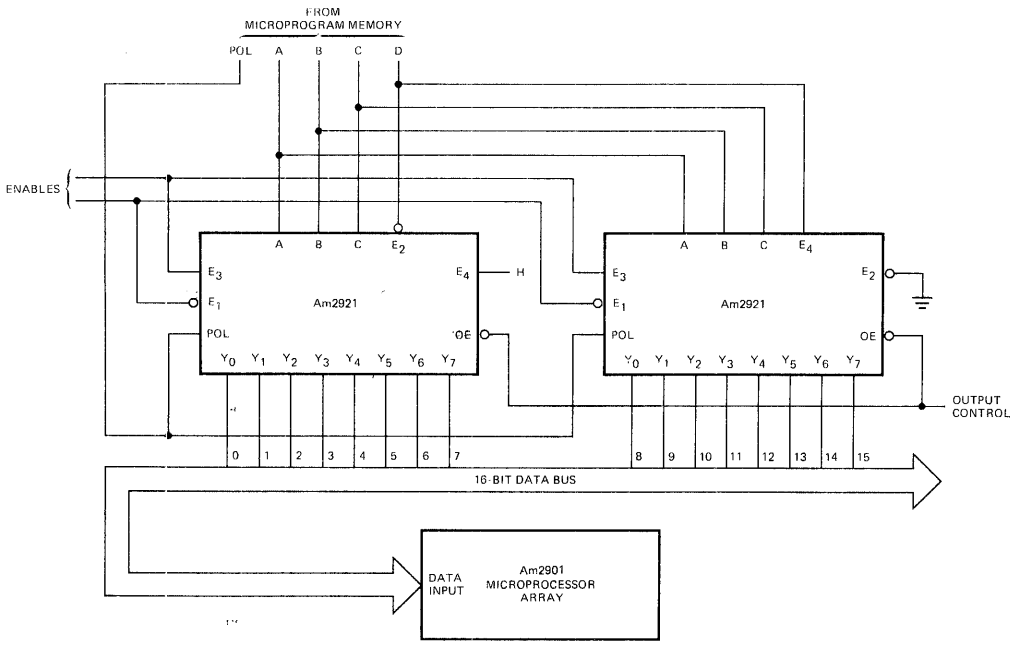
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2921PC	P-20	C	C-1
AM2921DC	D-20	C	C-1
AM2921DC-B	D-20	C	B-1
AM2921DM	D-20	M	C-3
AM2921DM-B	D-20	M	B-3
AM2921FM	F-20	M	C-3
AM2921FM-B	F-20	M	B-3
AM2921XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2921XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



MPR-211

Two Am2921's can be used to perform a bit set, bit clear, bit toggle or bit test on any of sixteen bits in a microprocessor system. Examples of the operations performed are as follows:

Microprogram Control					16-Bit Field From Am2921															Am2901 ALU Function	Bit Function Performed On Selected Register
D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	OR	BIT SET
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	AND	BIT TEST
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	AND	BIT CLEAR
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	EX NOR	BIT TOGGLE
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	EX OR	BIT TOGGLE

Note: Bit test is performed using F = 0 output of Am2901A.

Am2922

Eight Input Multiplexer With Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- AC parameters specified over operating temperature and power supply ranges.
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am2922 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

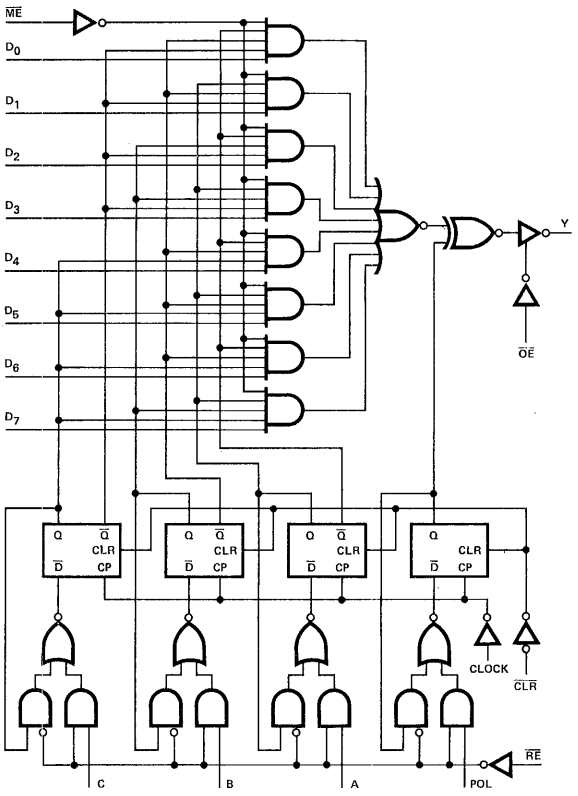
The Am2922 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (Polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am2922 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

LOGIC DIAGRAM



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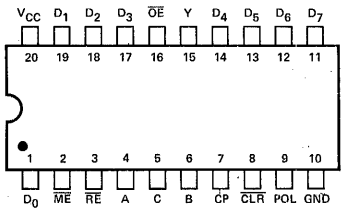
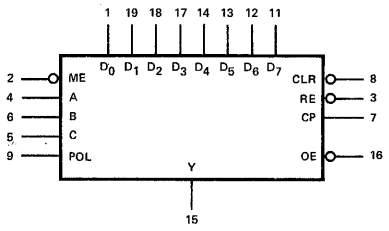
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-212

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -2.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -6.5mA$	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 20mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			50	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−50	μA
			$V_O = 2.4V$			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			97	148	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. D_N, A, B, C, POL, $\overline{ME}$ at Gnd. All other inputs and outputs open. Measured after a momentary ground then 4.5V applied to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y POL – LOW		21	32	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			19	29		
t_{PLH}	Clock to Y POL – HIGH		16	24	ns	
t_{PHL}			19	29		
t_{PLH}	D_n to Y		10	16	ns	
t_{PHL}			13	19		
t_{PLH}	CLR to Y		22	33	ns	
t_{PHL}			22	33		
t_{PLH}	ME to Y		12	18	ns	
t_{PHL}			12	18		
t_{ZL}	OE to Y		8	14	ns	
t_{ZH}			8	14		
t_{LZ}			10	17	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			10	17		
t_s	A, B, C, POL	10			ns	C_L = 15pF, R_L = 2.0kΩ
	CE	15				
t_s	CLR Recovery	5			ns	
t_{pw}	Clock	10			ns	
	Clear (LOW)	10				
t_h	A, B, C, POL, CE	0			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2922PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2922PC, DC Max.	Am2922DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2922DM, FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y, POL-L		40		47	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		38		
t_{PLH}	Clock to Y, POL-H		29		33	ns	
t_{PHL}			35		41		
t_{PLH}	D_N to Y		19		21	ns	
t_{PHL}			22		24		
t_{PLH}	CLR to Y		39		45	ns	
t_{PHL}			39		45		
t_{PLH}	ME to Y		22		26	ns	
t_{PHL}			19		20		
t_{ZL}	OE to Y		19		24	ns	
t_{ZH}			22		29		
t_{LZ}	OE to Y		24		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			24		30		
t_s	A, B, C POL	11		12		ns	C_L = 50pF, R_L = 2.0kΩ
	CE	18		20			
t_s	CLR Recovery	6		7		ns	
t_{pw}	Clock	11		12		ns	
	Clear (LOW)	11		12			
t_H	A, B, C, POL, CE	3		3		ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

A, B, C Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

POL Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

$\overline{ME}$ Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

$\overline{RE}$ Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

$\overline{CLR}$ Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

D_1-D_8 Data Inputs to the 8-input multiplexer.

CP Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

$\overline{OE}$ Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

Y The chip output.

FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	$\overline{D}_i/D_i$ (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L	↓	↓	↓	↓	L	H	L	↓	↓	↓	$\overline{D}_2/D_2$
	L	H	H	↓	↓	↓	↓	L	H	H	↓	↓	↓	$\overline{D}_3/D_3$
	H	L	L	↓	↓	↓	↓	H	L	L	↓	↓	↓	$\overline{D}_4/D_4$
	H	L	H	↓	↓	↓	↓	H	L	H	↓	↓	↓	$\overline{D}_5/D_5$
	H	H	L	↓	↓	↓	↓	H	H	L	↓	↓	↓	$\overline{D}_6/D_6$
	H	H	H	↓	↓	↓	↓	H	H	H	↓	↓	↓	$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

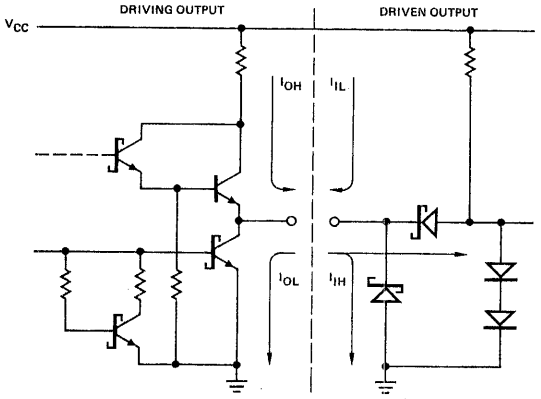
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2922PC	P-20	C	C-1
AM2922DC	D-20	C	C-1
AM2922DC-B	D-20	C	B-1
AM2922DM	D-20	M	C-3
AM2922DM-B	D-20	M	B-3
AM2922FM	F-20	M	C-3
AM2922FM-B	F-20	M	B-3
AM2922XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2922XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

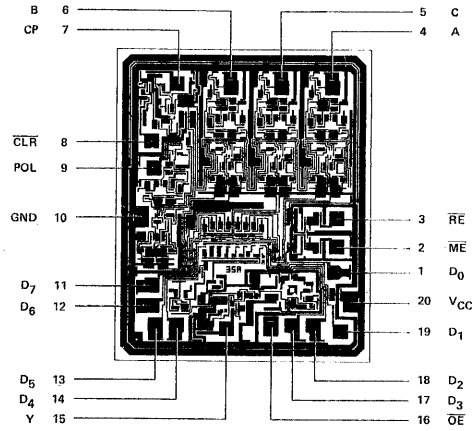
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

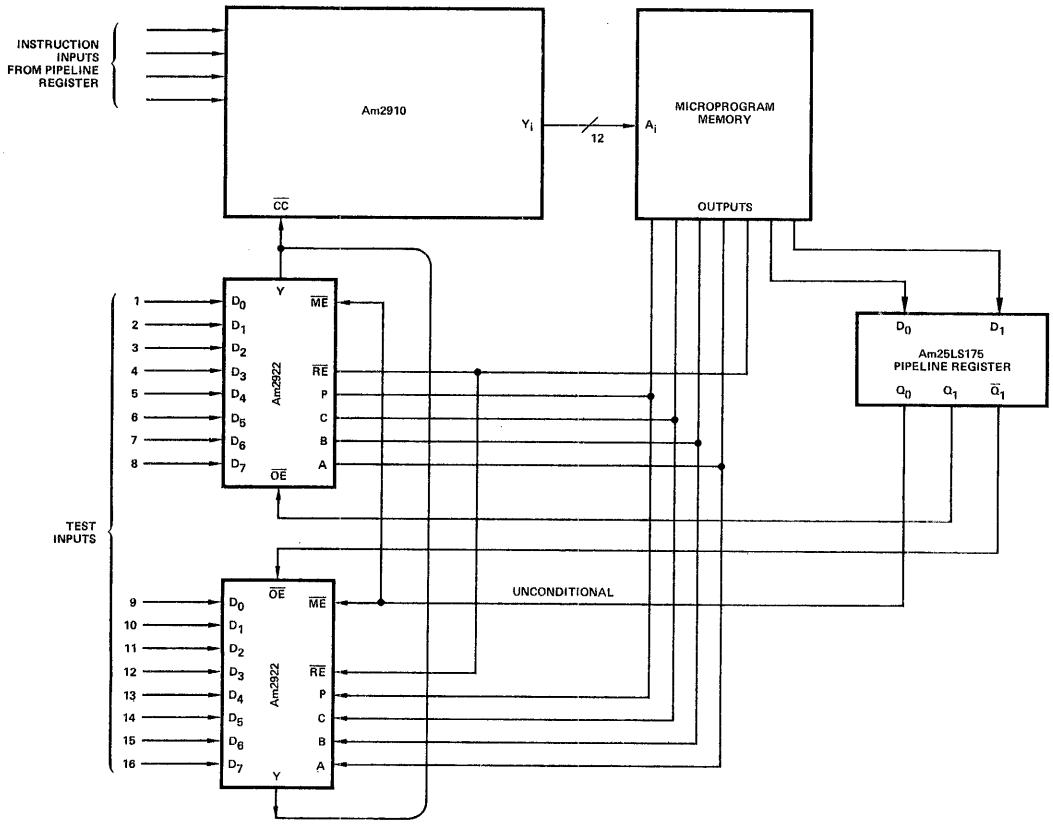
MPR-215

Metallization and Pad Layout



DIE SIZE 0.080" X 0.099"

APPLICATION



A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

MPR-216

Am2923
Eight-Input Multiplexer

Distinctive Characteristics

- Advanced Schottky technology
- Switches one of eight inputs to two complementary outputs
- 3-state output for bus organized systems
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2923 is an 8-input multiplexer that switches one of eight inputs onto the inverting and non-inverting outputs under the control of a 3-bit select code. The inverting output is one gate delay faster than the non-inverting output.

The Am2923 features a 3-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

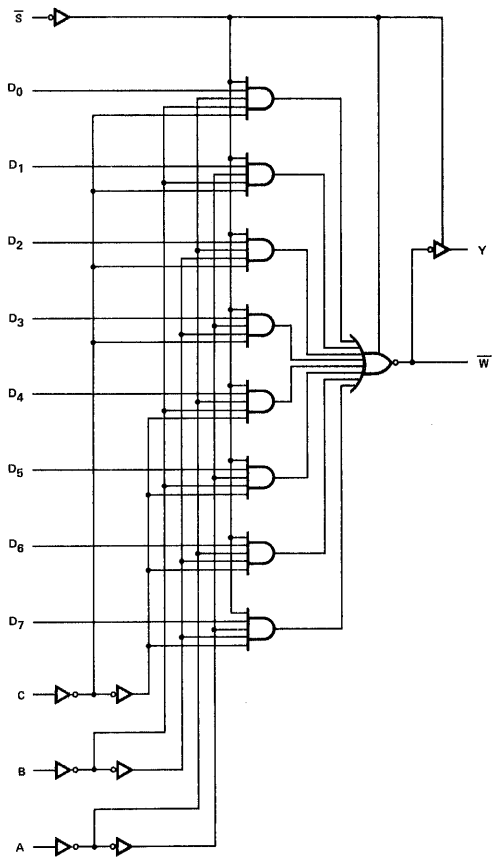
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2923PC	P-16-1	C	C-1
AM2923DC	D-16-1	C	C-1
AM2923DC-B	D-16-1	C	B-1
AM2923DM	D-16-1	M	C-3
AM2923DM-B	D-16-1	M	B-3
AM2923FM	F-16-1	M	C-3
AM2923FM-B	F-16-1	M	B-3
AM2923XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2923XM	Dice	M	

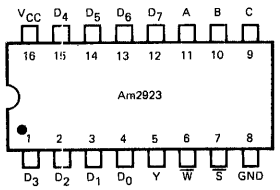
Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

LOGIC DIAGRAM



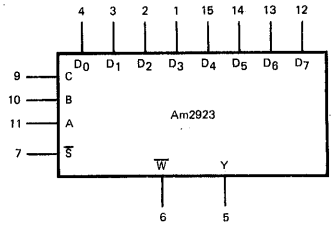
BLI-069

CONNECTION DIAGRAM
Top View



BLI-070

LOGIC SYMBOL



BLI-071

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to + V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Output	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2923PC, DC, XC T_A =0 to 70°C V_{CC} = 5.0V ±5% (COM'L) MIN = 4.75V MAX = 5.25V
Am2923DM, FM, XM T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIL) MIN = 4.5V MAX = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	MIL	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2mA	2.4	3.4		Volts
		COM'L		I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1	mA
$I_{O(off)}$	Off-State (High-Impedance) Output Current		V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL}	V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX, V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX (Note 5)			55	85	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs at 4.5V.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, or C to Y; 4 Levels of Delay	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		12	18	ns
t_{PHL}				13	19.5	
t_{PLH}	A, B, or C to $\overline{W}$; 3 Levels of Delay			10	15	ns
t_{PHL}				9	13.5	
t_{PLH}	Any D to Y			8	12	ns
t_{PHL}				8	12	
t_{PLH}	Any D to $\overline{W}$			4.5	7	ns
t_{PHL}				4.5	7	
t_{ZH}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		13	19.5	ns
t_{ZL}				14	21	
t_{ZH}	Output Enable to $\overline{W}$			13	19.5	ns
t_{ZL}				14	21	
t_{HZ}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 5pF		5.5	8.5	ns
t_{LZ}				9	14	
t_{HZ}	Output Enable to $\overline{W}$			5.5	8.5	ns
t_{LZ}				9	14	

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			Output Control		
C	B	A	$\overline{S}$	Y	$\overline{W}$
X	X	X	H	Z	Z
L	L	L	L	D_0	D_0
L	L	H	L	D_1	D_1
L	H	L	L	D_2	D_2
L	H	H	L	D_3	D_3
H	L	L	L	D_4	D_4
H	L	H	L	D_5	D_5
H	H	L	L	D_6	D_6
H	H	H	L	D_7	D_7

H = HIGH X = Don't Care
L = LOW Z = High Impedance

D_0–D_7 = The output will follow the HIGH-level or LOW-level of the selected input.

$\overline{D}_0$–$\overline{D}_7$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

DEFINITION OF FUNCTIONAL TERMS

A, B, C The three select inputs of the multiplexer.

D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7 The eight data inputs of the multiplexer.

Y The true multiplexer output.

$\overline{W}$ The complement multiplexer output.

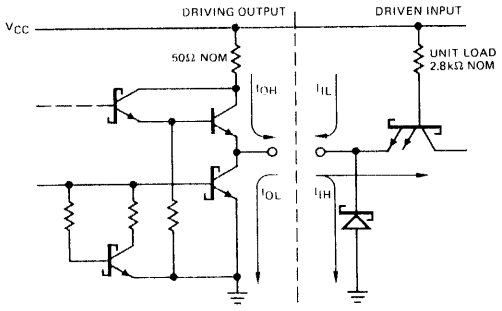
$\overline{S}$ Output Control. HIGH on the output control (or strobe) forces both the $\overline{W}$ and Y outputs to the high-impedance (off) state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_3	1	1	–	–
D_2	2	1	–	–
D_1	3	1	–	–
D_0	4	1	–	–
Y	5	–	20	10
$\overline{W}$	6	–	20	10
$\overline{S}$	7	1	–	–
GND	8	–	–	–
C	9	1	–	–
B	10	1	–	–
A	11	1	–	–
D_7	12	1	–	–
D_6	13	1	–	–
D_5	14	1	–	–
D_4	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

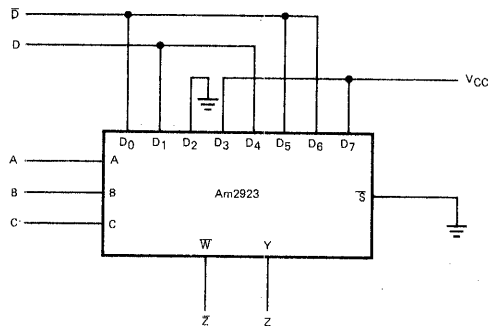


Note: Actual current flow direction shown.

BLI-072

APPLICATIONS

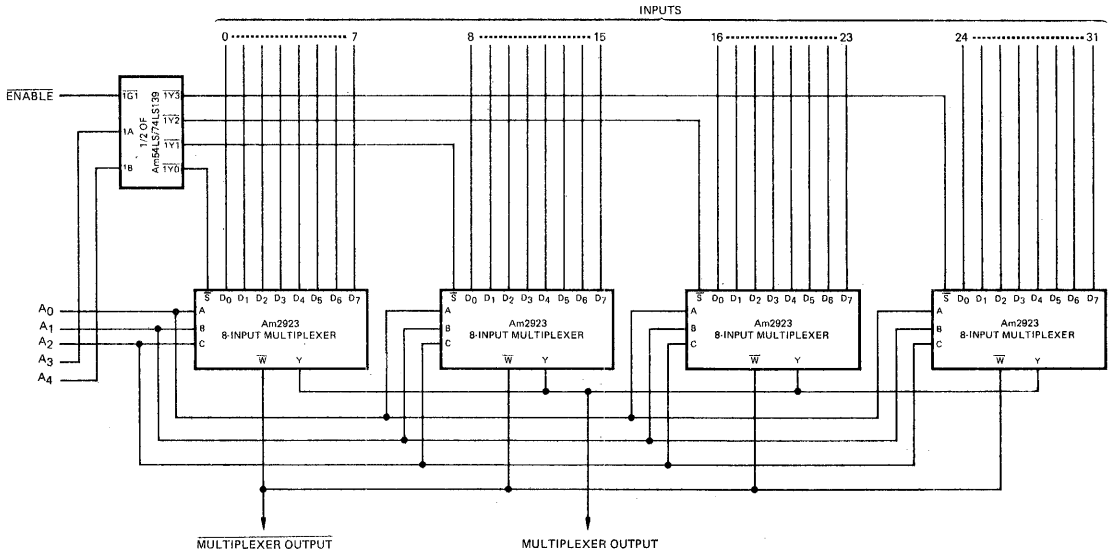
LOGIC FUNCTION GENERATION



$$Z = \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{C}D + AB + AC\bar{D} + BC\bar{D}$$

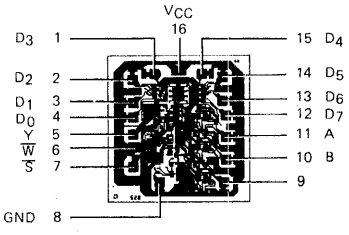
BLI-073

32-INPUT MULTIPLEXER



BLI-074

Metallization and Pad Layout



DIE SIZE: 0.064" X 0.067"

Am2924

3-Line to 8-Line Decoder/Demultiplexer

Distinctive Characteristics

- Advanced Schottky technology
- Inverting and non-inverting enable inputs
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2924 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight $\overline{Y}$ outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight $\overline{Y}$ outputs are HIGH regardless of the A, B and C select inputs.

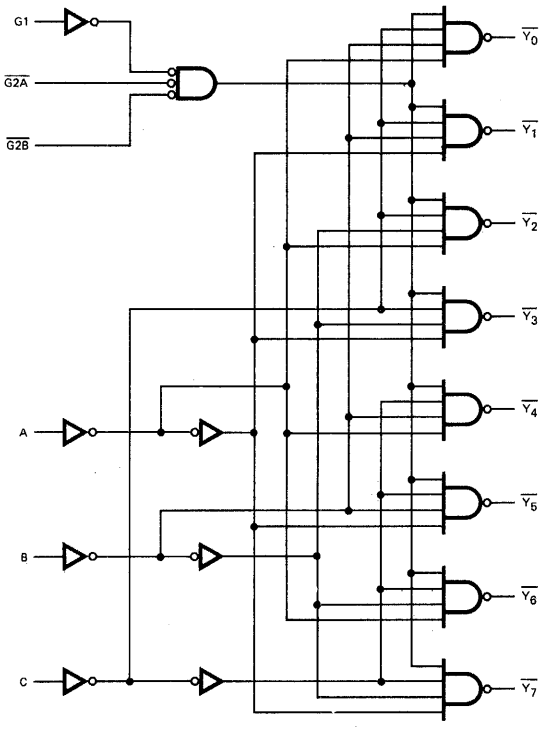
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2924PC	P-16-1	C	C-1
AM2924DC	D-16-1	C	C-1
AM2924DC-B	D-16-1	C	B-1
AM2924DM	D-16-1	M	C-3
AM2924DM-B	D-16-1	M	B-3
AM2924FM	F-16-1	M	C-3
AM2924FM-B	F-16-1	M	B-3
AM2924XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2924XM	Dice	M	

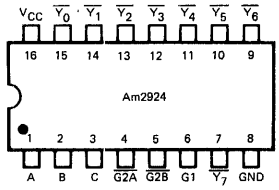
Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883 Class B.

LOGIC DIAGRAM



BLI-075

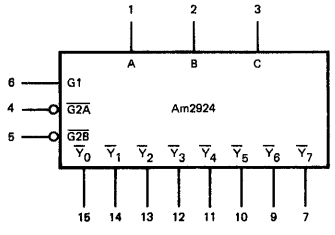
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-076

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BLI-077

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +Vcc max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

2

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2924PC, DC, XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2924DM, FM, XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			49	74	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs enabled and open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Two Level Delay Select to Output	V_{CC} = 5V, C_L = 15pF, R_L = 280Ω		4.5	7	ns
t_{PHL}				7	10.5	
t_{PLH}	Three Level Delay Select to Output			7.5	12	ns
t_{PHL}				8	12	
t_{PLH}	$\overline{G2A}$ or $\overline{G2B}$ to Output			5	8	ns
t_{PHL}				7	11	
t_{PLH}	G1 to Output			7	11	ns
t_{PHL}				7	11	

FUNCTION TABLE

Inputs						Outputs							
Enable			Select										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A	1	1	–	–
B	2	1	–	–
C	3	1	–	–
$\overline{G2A}$	4	1	–	–
$\overline{G2B}$	5	1	–	–
G1	6	1	–	–
$\overline{Y_7}$	7	–	20	10
GND	8	–	–	–
$\overline{Y_6}$	9	–	20	10
$\overline{Y_5}$	10	–	20	10
$\overline{Y_4}$	11	–	20	10
$\overline{Y_3}$	12	–	20	10
$\overline{Y_2}$	13	–	20	10
$\overline{Y_1}$	14	–	20	10
$\overline{Y_0}$	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS:

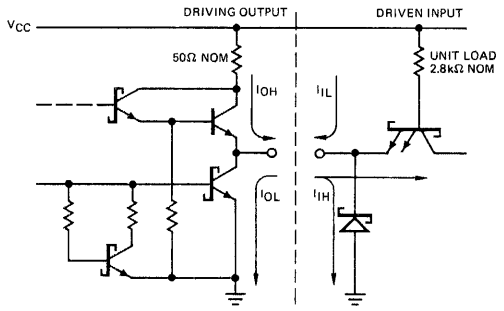
A, B, C Select. The three select inputs to the decoder.

G1 The active-HIGH enable input. A LOW on the G1 input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.

$\overline{G2A}$, $\overline{G2B}$ The active-LOW enable input. A HIGH on either the $\overline{G2A}$ or $\overline{G2B}$ input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.

$\overline{Y_0}$, $\overline{Y_1}$, $\overline{Y_2}$, $\overline{Y_3}$, $\overline{Y_4}$, $\overline{Y_5}$, $\overline{Y_6}$, $\overline{Y_7}$ The eight decoder outputs.

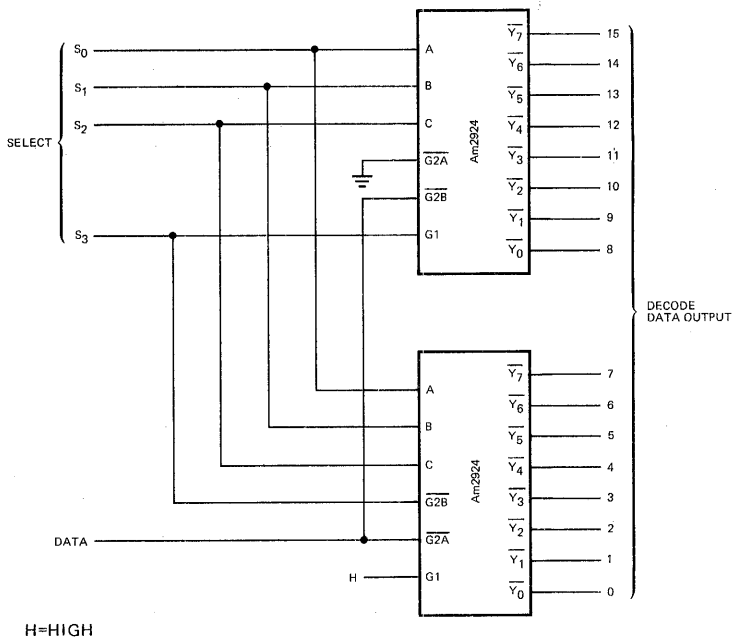
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-078

APPLICATION

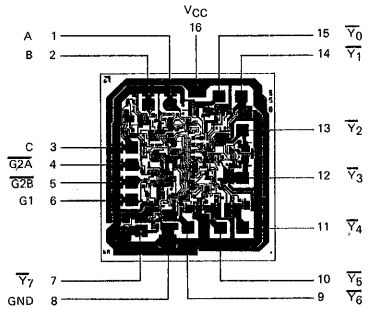


H=HIGH

ONE-OF-SIXTEEN DEMULTIPLEXER

BLI-079

Metallization and Pad Layout



DIE SIZE 0.065"X0.070"

Am2925

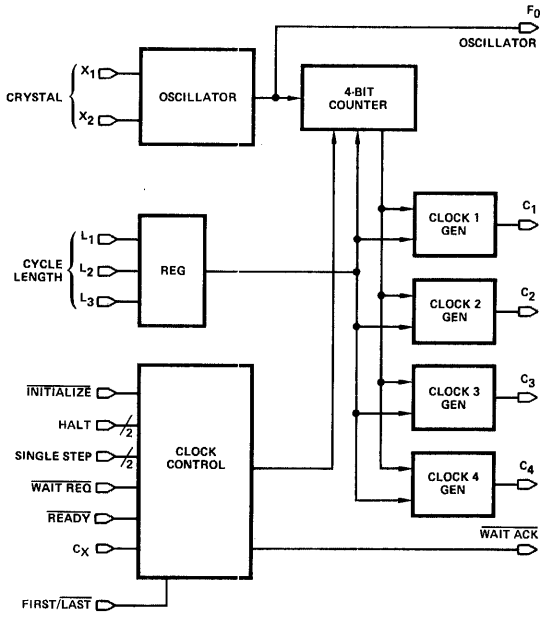
System Clock Generator and Driver

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Single chip clock generator and driver
- Four different clock output waveforms for Am2900 and other bipolar and MOS systems
- Crystal controlled for stable system operation
- Oscillator to 31MHz – oscillator output for external system timing
- Clock halt, single-step and wait controls
- Variable cycle lengths – 1 of 8 different cycle lengths may be programmed
- Slim 0.3" 24-pin package
- 100% product assurance screening to MIL-STD-883 requirements

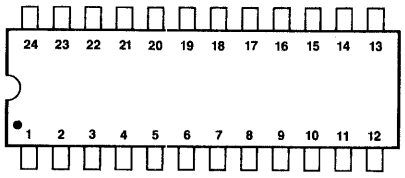
LOGIC DIAGRAM



MPR-217

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MPR-219

FUNCTIONAL DESCRIPTION

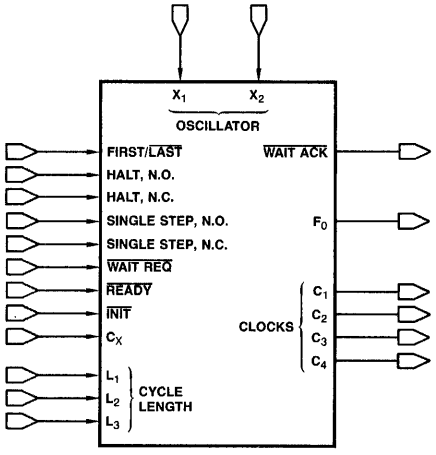
The Am2925 is a single-chip general purpose clock generator/driver. It is controlled by a crystal, selected by the designer, and is microprogrammable to meet a variety of system speed requirements. The Am2925 generates four different clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. Also, variable cycle lengths may be generated under microprogram control. One of eight different cycle lengths may be microprogrammed using the Cycle Length inputs L_1, L_2, and L_3.

The Am2925 oscillator runs at frequencies up to 31MHz. A buffered oscillator output is provided for external system timing.

Clock halt, single-step and wait controls are provided for the Am2925. The HALT REQ input halts the clocks; the clocks resume when the HALT REQ input is deactivated. The SINGLE-STEP input, which operates only when the clocks are halted, generates the clocks for a single cycle. The WAIT REQ input stops the clocks and puts the Am2925 in a "wait" state. In this state, the clocks remain stopped until an asynchronous READY input signal is received. The WAIT ACK output indicates when the Am2925 is in the "wait" state. The WAIT REQ and READY inputs are pulse sensitive and are overridden by the HALT REQ input.

One of eight cycle lengths may be microprogrammed using the L_1, L_2, and L_3 inputs. There are four clock output waveforms for each of the 8 possible cycle lengths.

LOGIC SYMBOL



MPR-218

The Am2925 is scheduled for introduction in 2Q '80.

Am2926 • Am2929

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- 3-state outputs on driver and receiver
- PNP inputs
- Am2926 has inverting outputs
- Am2929 has non-inverting outputs
- Driver propagation delay – 14ns max for Am2926; 17ns max for Am2929
- Receiver propagation delay – 14ns max for Am2926; 17ns max for Am2929
- 100% reliability assurance testing in compliance with MIL-STD-883

2

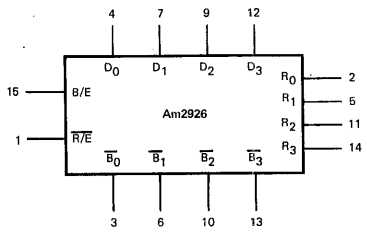
FUNCTIONAL DESCRIPTION

The Am2926 and Am2929 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable ($\overline{R/E}$) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

LOGIC SYMBOL

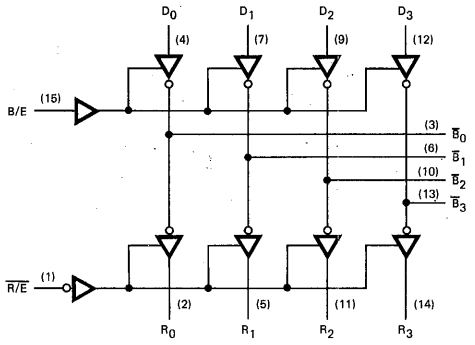


VCC = Pin 16
GND = Pin 8

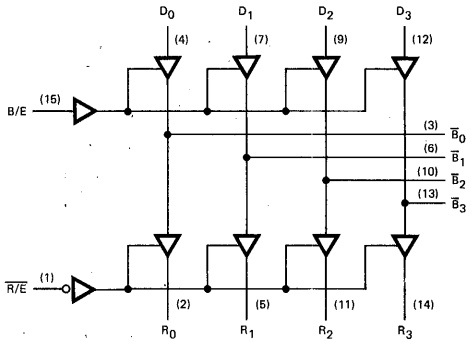
BLI-136

LOGIC DIAGRAMS

Am2926
Inverting Output (3-State)

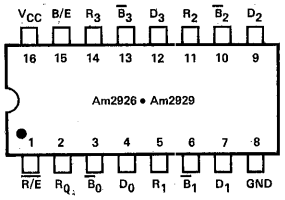


Am2929
Non-Inverting Output (3-State)



BLI-080

CONNECTION DIAGRAM
Top View



BLI-081

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Receiver)	30mA
DC Output Current, Into Outputs (BUS)	80mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am2926PC, DC, XC Am2929PC, DC, XC T_A = 0°C to +75°C (COM'L) MIN. = 4.75 V MAX. = 5.25 V

Am2929DM, XM Am2926DM, XM T_A = −55°C to +125°C (MIL) MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
Driver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4 V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 48 mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −10 mA, V_{CC} = V_{CC} MIN. (Note 6)	2.4			Volts
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC} MAX. (Note 4)	−50		−150	mA
Receiver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20 mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −100 μA, V_{CC} = 5.0 V	3.5			Volts
		I_{OUT} = −2.0 mA (Note 6)	2.4			
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC} MAX.	−30		−75	mA
Both Driver and Receiver						
V_{TL}	Low Level Input Threshold Voltage		0.85			Volts
V_{TH}	High Level Input Threshold Voltage				2.0	Volts
I_O	Low Level Output Off Leakage Current	V_{OUT} = 0.5 V			−100	μA
	High Level Output Off Leakage Current	V_{OUT} = 2.4 V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA			−1.0	Volts
P_{WR}/I_{CC}	Power/Current Consumption (Am2926)	V_{CC} = V_{CC} MAX.			457/87	mW/mA
	Power/Current Consumption (Am2929)	V_{CC} = V_{CC} MAX.			578/110	mW/mA

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Am2926 Min.	Am2926 Typ.	Am2926 Max.	Am2929 Min.	Am2929 Typ.	Am2929 Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		10	14		13	17	ns
t_{PHL}				10	14		13	17	
t_{PLH}	Bus to Receiver Output	Figure 2		9.0	14		12	17	ns
t_{PHL}				6.0	14		9.0	17	
t_{ZL}	Driver Enable to Bus	Figure 3		19	25		21	28	ns
t_{LZ}				15	20		18	23	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		15	20		18	23	ns
t_{LZ}				10	15		13	18	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Measurements apply to each output and the associated data input independently.

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

$\overline{B_0}, \overline{B_1}, \overline{B_2}, \overline{B_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

$\overline{R/E}$ Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{R/E}$	1	1/8	–	–
R_0	2	–	50	10
$\overline{B_0}$	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
$\overline{B_1}$	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
$\overline{B_2}$	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
$\overline{B_3}$	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

DRIVER FUNCTION TABLE

INPUTS		Am2926 OUTPUT	Am2929 OUTPUT
B/E	D_i	$\overline{B_i}$	$\overline{B_i}$
L	X	Z	Z
H	L	H	L
H	H	L	H

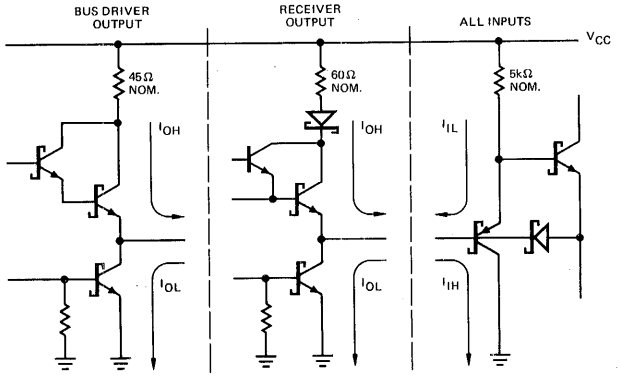
L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		Am2926 OUTPUT	Am2929 OUTPUT
$\overline{R/E}$	$\overline{B_i}$	R_i	R_i
H	X	Z	Z
L	L	H	L
L	H	L	H

L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-082

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)

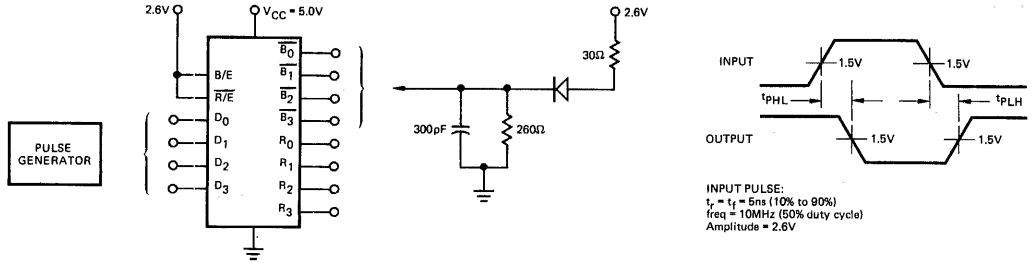


Figure 1

BLI-083

PROPAGATION DELAY (Bus to Receiver Out)

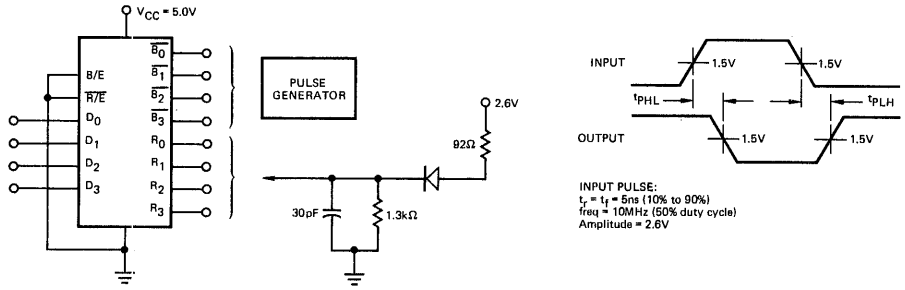


Figure 2

BLI-084

PROPAGATION DELAY (Bus Enable to Bus Output)

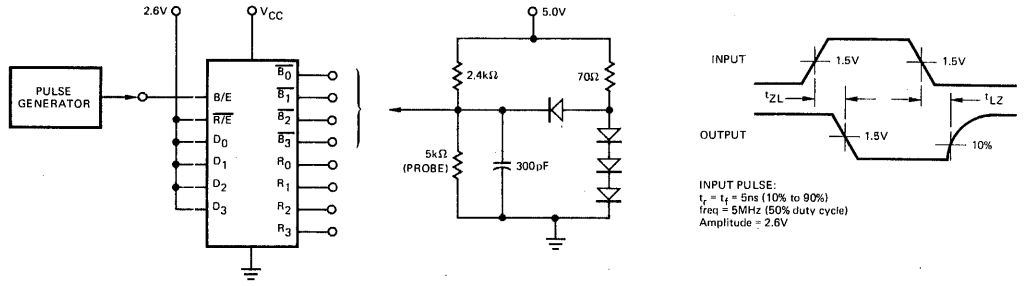


Figure 3

BLI-085

PROPAGATION DELAY (Receive Enable to Receive Output)

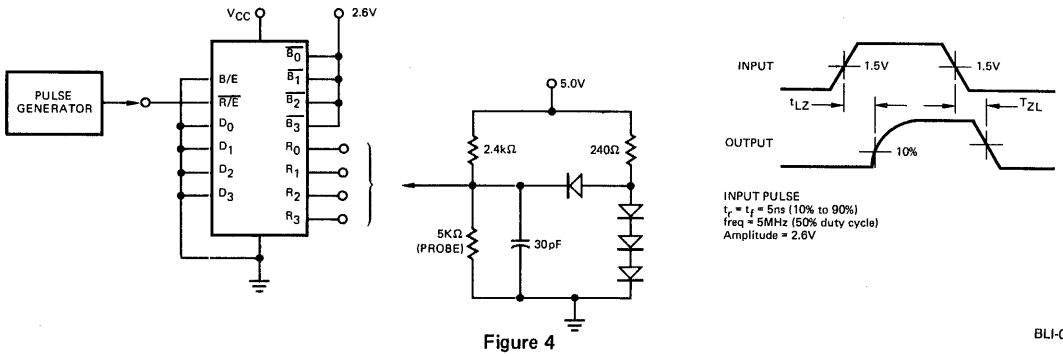
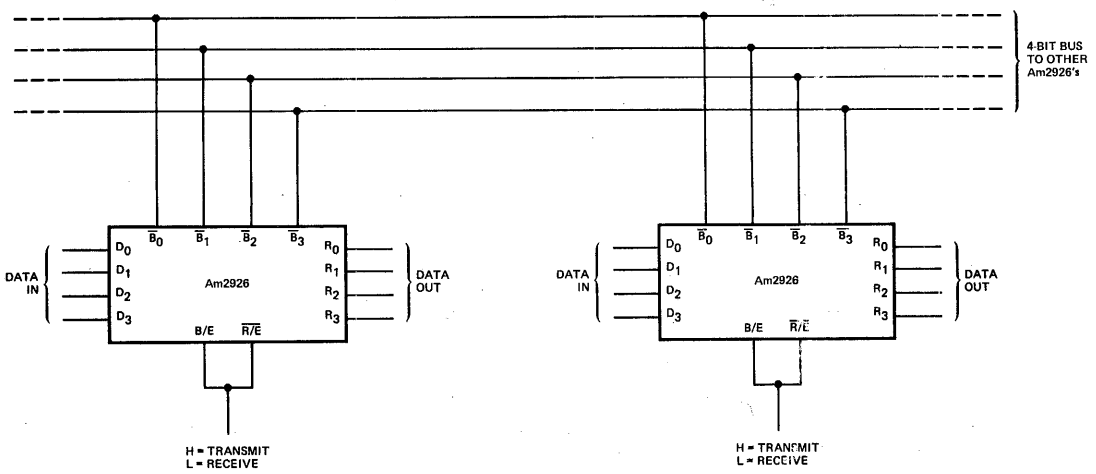


Figure 4

BLI-086

APPLICATION



ORDERING INFORMATION

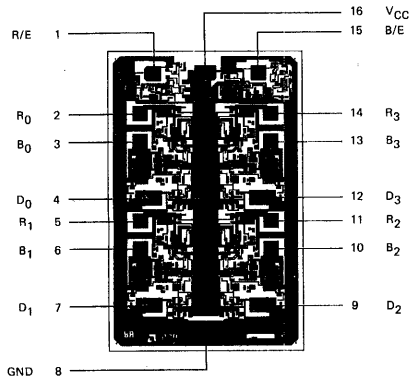
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2926 Order Number	Am2929 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2929PC	AM2929PC	P-16-1	C	C-1
AM2929DC	AM2929DC	D-16-1	C	C-1
AM2929DC-B	AM2929DC-B	D-16-1	C	B-1
AM2926DM		D-16-1	M	C-3
AM2926DM-B		D-16-1	M	B-3
AM2926XC	AM2929XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010 B.
AM2926XM		Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

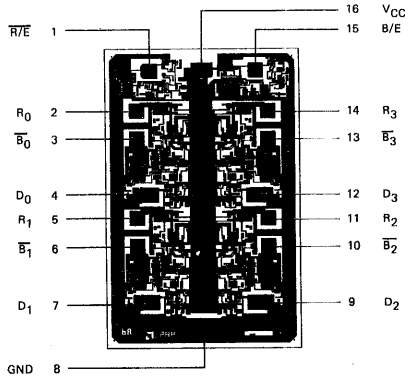
Metallization and Pad Layouts

Am2926



DIE SIZE 0.058" X 0.091"

Am2929



DIE SIZE 0.058" X 0.091"

Am2927 • Am2928

Quad Three-State Bus Transceivers With Clock Enable

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceivers
- Three-state bus driver and receiver outputs
- D-type register on drivers
- Latch output on Am2927
- Registered output on Am2928
- Output data to input wrap around gating
- Input register to output transfer gating with or without driving data bus
- Clock enabled registers
- Bus driver outputs can sink 48mA at 0.5V max.
- Three-state receiver outputs sink 20mA at 0.5V max.
- 3.5V minimum V_{OH} for direct interface to MOS microprocessors
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2927 and Am2928 are high-performance, low-power Schottky, quad bus transceivers intended for use in bipolar or MOS microprocessor system applications.

Both devices feature register enable lines which function as clock enables without introducing gate delay in the clock inputs. The four transceivers share common enables, clock, select and three-state control lines.

The Am2927 consists of four D-type edge-triggered flip-flops. Each flip-flop output is connected to a three-state data bus driver and separately to the input of a corresponding receiver latch input. The receiver latch can select input from the driver or the data bus. The select line determines the source of input data for the bus driver choosing between input data or data recirculated from the receiver output. The receiver output also has a three-state output buffer.

The combination of the select input, S, the driver input enable, $\overline{ENDR}$, and the receiver latch enable, $\overline{RLE}$, provide seven different data path operating modes not available in other transceivers. For example, transmitted data can be stored in the receiver for subsequent retransmission. Also, received data can be output to the system and simultaneously fed back to the driver input.

The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, $\overline{ENREC}$, which functions as a common clock enable.

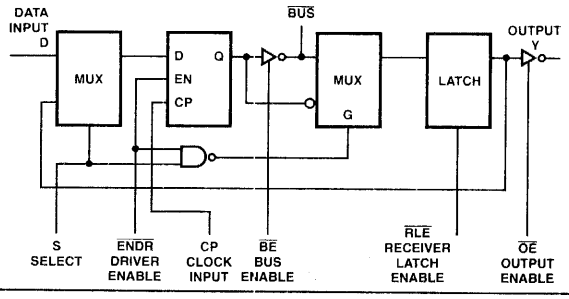
Data from each D input is inverted at the bus output. Likewise, data at the bus input is inverted at the receiver output.

All three-state controls and enable lines are active low (the Am2927 receiver latch is transparent when $\overline{RLE}$ is LOW). The select input, S, determines whether the enabled driver input accepts data from the data input, D, or from the corresponding receiver output, Y. Similarly, the select line determines whether the receiver accepts input data from the data bus, or the driver output.

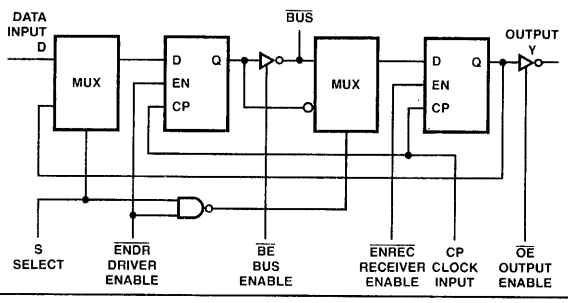
BLI-088

SIMPLIFIED LOGIC DIAGRAMS

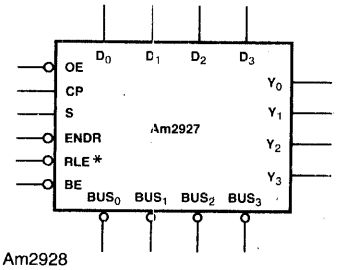
Am2927



Am2928



LOGIC SYMBOL



*ENREC for Am2928

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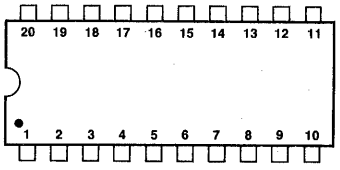
CONNECTION DIAGRAM
Top View

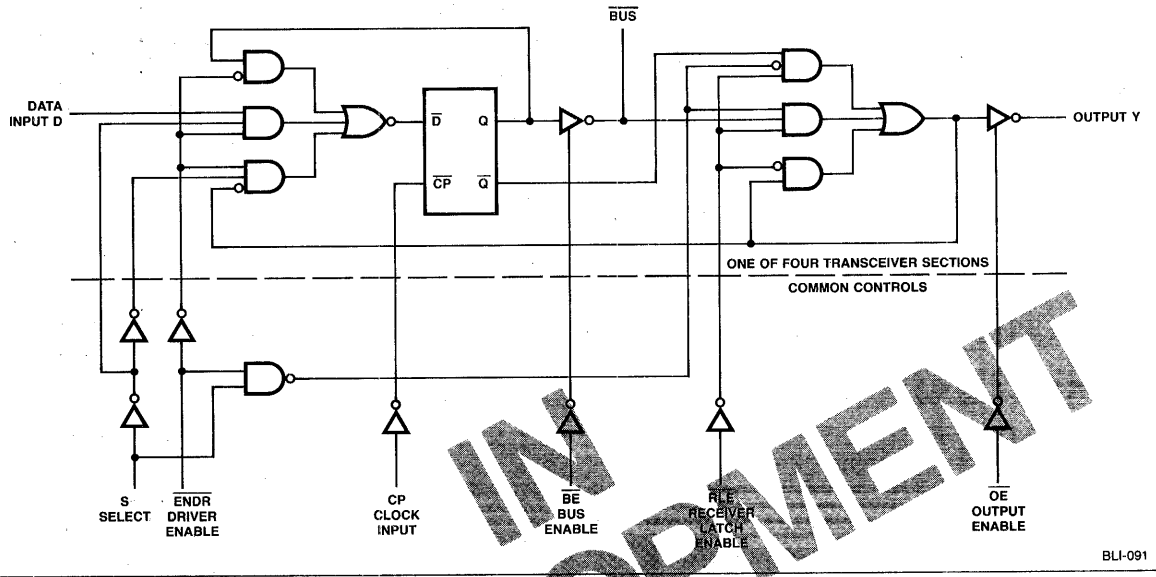


Note: Pin 1 is marked for orientation.

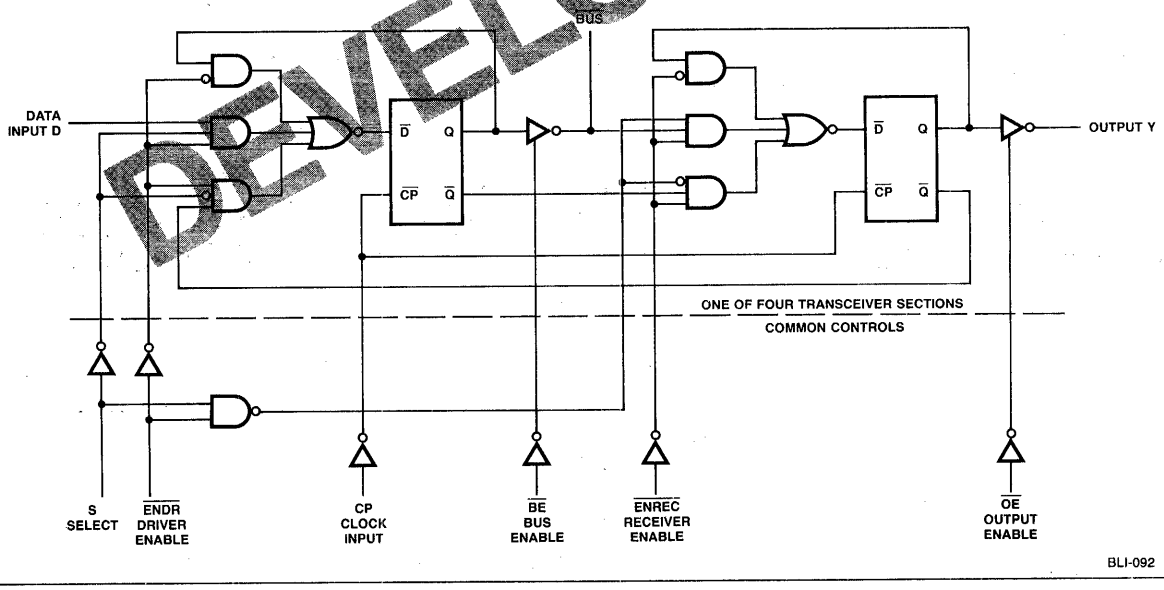
BLI-090

DETAILED LOGIC DIAGRAMS

Am2927



Am2928



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA	2.4			
V_{IH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus Enable = 2.4V				0.8	Volts
I_{OFF}	Bus Leakage Current (Power Off)	V_{CC} = 0V, V_O = 4.5V				100	μA
I_O	Bus Leakage Current (HIGH Impedance)	V_{CC} = MAX Bus Enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX, V_O = 0V		−50		−255	mA
C_B	Bus Capacitance (Note 4)	V_{CC} = 0V			8		pF

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.4		
		V_{CC} = 5.0V	I_{OH} = −100μA	3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH}	I_{OL} = 20mA			0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	S, ENDR			100	μA
			All other inputs			50	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0V	S, ENDR			2.0	mA
			All other inputs			1.0	
I_O	Off-State Output Current (Receiver Output)	V_{CC} = MAX.	V_O = 2.4V			50	μA
			V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	Receiver	−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					mA

Am2927
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2927XM Min	Am2927XM Typ	Am2927XM Max	Am2927XC Min	Am2927XC Typ	Am2927XC Max	Units
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L (BUS) = 130Ω					18		ns
t_{PHL}							18		
$t_{ZH} \bullet t_{ZL}$	Bus Enable, $\overline{BE}$, to $\overline{BUS}$						14		ns
$t_{HZ} \bullet t_{LZ}$		C_L = 5pF					12		
t_{PW}	Min. Clock Pulse Width (HIGH or LOW)					10			ns
t_{PLH}	$\overline{BUS}$ to Receiver Output (Latch Enabled)						16		ns
t_{PHL}							16		
t_{PLH}	Latch Enable, $\overline{RLE}$, to Receiver Output						18		ns
t_{PHL}							18		
$t_{ZH} \bullet t_{ZL}$	Output Enable, $\overline{OE}$, to Output	C_L = 15pF, R_L = 2.0kΩ					16		ns
$t_{HZ} \bullet t_{LZ}$		C_L = 5pF, R_L = 2.0kΩ					14		
t_s	Driver Enable, $\overline{ENDR}$, to Clock					8			ns
t_h						2			
t_s	Select, S, to Clock ($\overline{RLE}$ = HIGH)					10			ns
t_h						0			
t_s	Select, S, to Clock ($\overline{RLE}$ = LOW)					13			ns
t_h						0			
t_s	Data Inputs, D, to Clock					7			ns
t_h						2			
t_s	$\overline{BUS}$ to Latch Enable, $\overline{RLE}$					10			ns
t_h						1			

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2928
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2928XM Min	Am2928XM Typ	Am2928XM Max	Am2928XC Min	Am2928XC Typ	Am2928XC Max	Units
t_{PLH}	Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L (BUS) = 130Ω					18		ns
t_{PHL}							18		
$t_{ZH} \bullet t_{ZL}$	Bus Enable, $\overline{BE}$, to $\overline{BUS}$						14		ns
$t_{HZ} \bullet t_{LZ}$		C_L = 5pF					12		
t_{PLH}	Clock, CP, to Output, Y	C_L = 15pF, R_L = 2.0kΩ					18		ns
t_{PHL}							18		
t_{PW}	Min. Clock Pulse Width (HIGH or LOW)					10			ns
$t_{ZH} \bullet t_{ZL}$	Output Enable, $\overline{OE}$, to Output, Y	C_L = 15pF, R_L = 2.0kΩ					16		ns
$t_{HZ} \bullet t_{LZ}$		C_L = 5pF, R_L = 2.0kΩ					14		
t_s	Driver Enable, $\overline{ENDR}$, to Clock					8			ns
t_h						2			
t_s	$\overline{BUS}$ to Clock (Receiver Register)					7			ns
t_h						2			
t_s	Receiver Enable, $\overline{ENREC}$, to Clock					8			ns
t_h						2			
t_s	S to Clock					10			ns
t_h						0			
t_s	Data Inputs, D, to Clock (Driver Register)					7			ns
t_h						2			

Notes: 1. For conditions shown an MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DEFINITION OF FUNCTIONAL TERMS

CP — Clock Pulse to internal registers enters data on the LOW-to-HIGH transition.

$\overline{BE}$ — Bus Enable. When Bus Enable is LOW the four drivers drive the $\overline{BUS}$ outputs.

$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ — The four driver outputs and receiver inputs.

D_0, D_1, D_2, D_3 — The four driver data inputs inverting from D to $\overline{BUS}$.

Y_0, Y_1, Y_2, Y_3 — The four receiver data outputs inverting from $\overline{BUS}$ to Y.

S — Select input controls data path modes in conjunction with $\overline{ENDR}$ and $\overline{RLE}$ (or $\overline{ENREC}$).

$\overline{OE}$ — Output Enable. When Output Enable is LOW the four receiver outputs Y are active.

$\overline{ENDR}$ — Driver Enable. Common clock enable for the input register. Allows the data on the D inputs to be loaded into the driver register on the clock LOW-to-HIGH transition.

$\overline{RLE}$ — Receiver Latch Enable (Am2927 only). When Receiver Latch Enable is LOW, the four receiver latches are transparent. The latches hold received data when $\overline{RLE}$ is HIGH.

$\overline{ENREC}$ — Receiver Enable (Am2928 only). Common clock enable for the receiver register. Allows the $\overline{BUS}$ driver or previous receiver data to enter the receiver register on the rising edge of the clock.

Am2927 FUNCTION TABLES

Driver Register Control

$\overline{ENDR}$	S	$\overline{RLE}$	Driver Register
H	X	X	Hold Previous Data
L	L	X	Load from D Input
L	H	L	Load from $\overline{BUS}$
L	H	H	Load Latched Receiver Data

Receiver Latch Control

$\overline{ENDR}$	S	$\overline{RLE}$	Receiver Output
X	X	H	Data Latched
H	H	L	Driver Register Output at Y Output (Latch Transparent)
X	L	L	Bus Data at Y Output (Latch Transparent)
L	X	L	

Am2928 FUNCTION TABLES

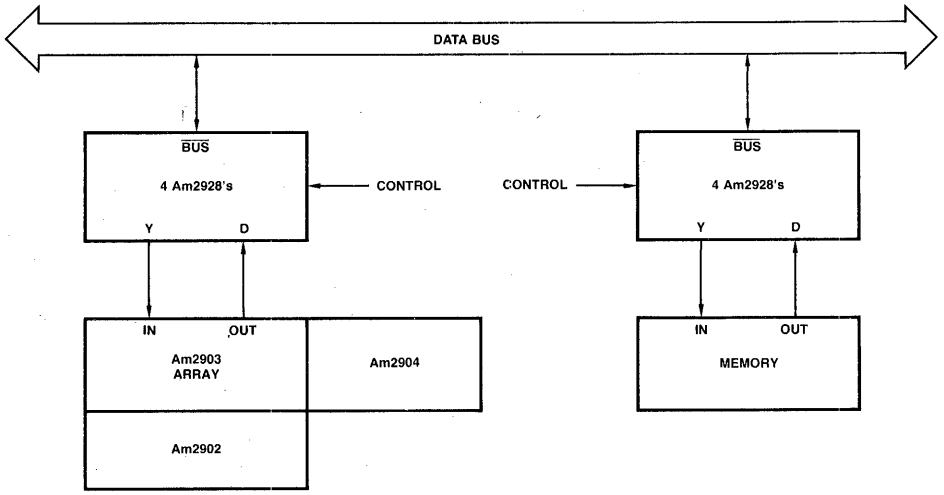
Driver Register Control

$\overline{ENDR}$	S	Driver Register
H	X	Hold Previous Data
L	L	Load from D Input
L	H	Load from Receiver Register

Receiver Register Control

$\overline{ENDR}$	S	$\overline{ENREC}$	Receiver Output
X	X	H	Hold Previous Data
H	H	L	Load from Driver Register
X	L	L	Load from $\overline{BUS}$
L	X	L	

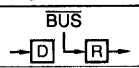
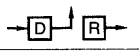
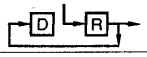
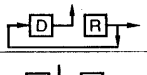
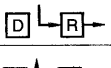
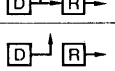
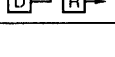
APPLICATION



The Am2927 and Am2928 can be used to provide Data Bus, Address Bus and Control Bus Interface in a high-speed bipolar microprocessor system.

BLI-093

Am2927 AND Am2928 FUNCTION TABLE

Driver Input From	Receiver Input From	Control Input Condition			Signal Flow	$\overline{BE}$
		S	$\overline{ENDR}$	*		
D Input	BUS	L	L	L		H
	(No Load)	L	L	H		L
Receiver	BUS	H	L	L		H
	(No Load)	H	L	H		L
(No Load)	BUS	L	H	L		H
	Driver	H	H	L		X
	(No Load)	X	H	H		L

*$\overline{RLE}$ for Am2927 (asynchronous) or $\overline{ENREC}$ for Am2928 (⌐).

Am2930

Program Control Unit

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 32 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Twelve different relative address instructions are provided; including jump-to-subroutine relative and return-from-subroutine relative
- Built-in condition code input
  Sixteen instructions are dependent on external condition control
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

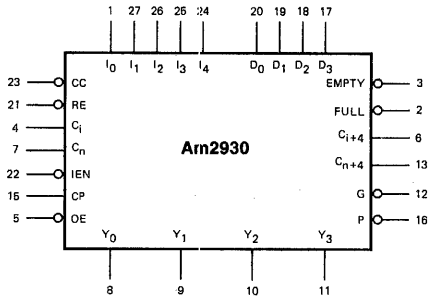
GENERAL DESCRIPTION

The Am2930 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2930's may be interconnected to generate a 16-bit address (64K words). The Am2930 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2930 performs five types of instructions. These are: 1) Unconditional Fetch; 2) Conditional Jump; 3) Conditional Jump-to-Subroutine; 4) Conditional Return-from-Subroutine; and 5) miscellaneous instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter (PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_4), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register. A condition code input is provided for conditional instructions.

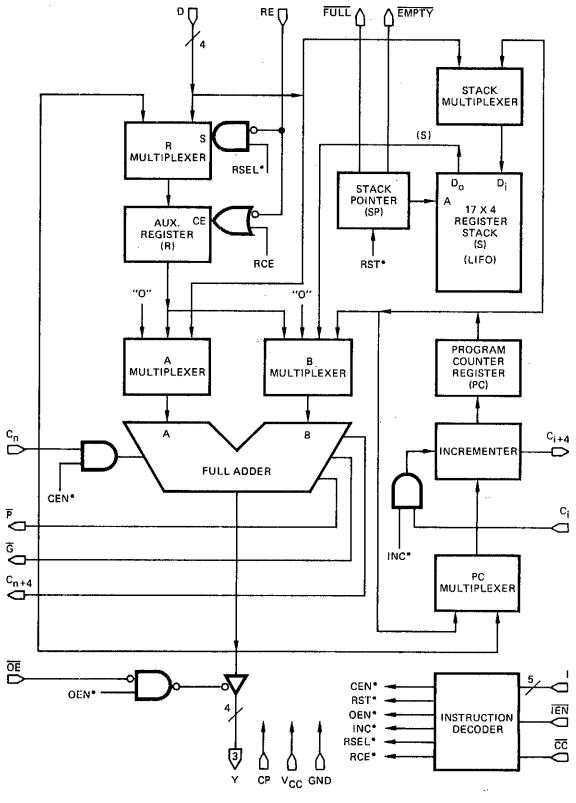
LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

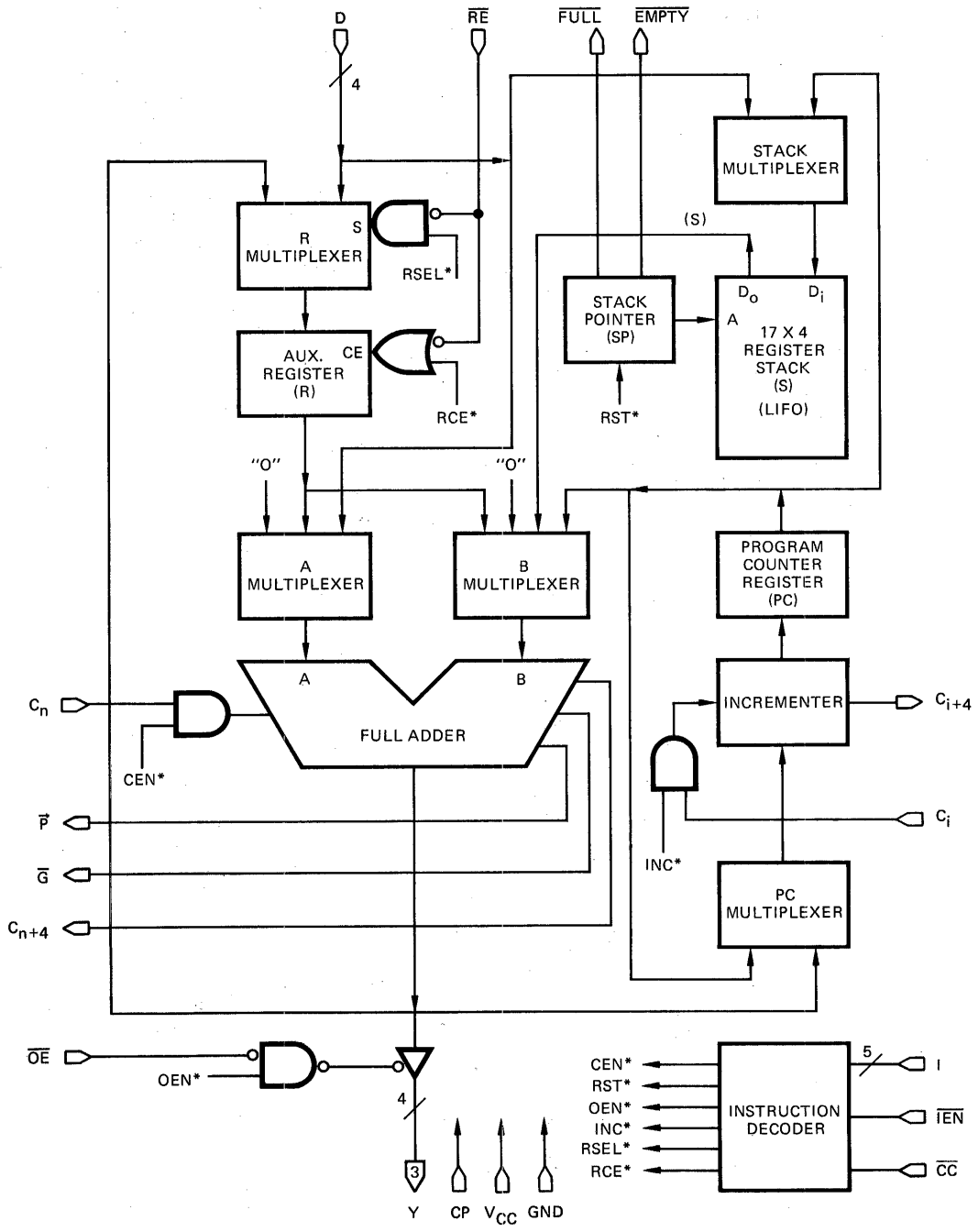
MPR-220

BLOCK DIAGRAM



MPR-221

BLOCK DIAGRAM



MPR-221

ARCHITECTURE OF THE Am2930

The Am2930 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition and provision is made for further lookahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. In slower systems, the carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceeded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During three instructions (unconditional Hold and conditional Hold and Suspend when the $\overline{CC}$ input is LOW), the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer if the $\overline{CC}$ input is LOW. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Empty output ($\overline{EMPTY}$) is LOW when the stack is empty (after the Reset instruction and after the last word has been Popped from the stack); the active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Register Enable input ($\overline{RE}$) is LOW or if the Instruction inputs call for it to be loaded. When $\overline{RE}$ is LOW, R is loaded from the D inputs unless the Instruction dictates that R be loaded from the output of the Full Adder.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

For unconditional instructions, the $\overline{CC}$ input is not utilized; it may be either HIGH or LOW. For conditional instructions, if $\overline{CC}$ is LOW, the condition is met and the conditional operation is performed; if $\overline{CC}$ is HIGH, a Fetch PC is performed.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled either under Instruction control or by a HIGH on the Output Enable input ($\overline{OE}$). Disabling the Y outputs does not affect the execution of instructions inside the Am2930.

Instruction Enable

When HIGH, the Instruction Enable input ($\overline{IEN}$) forces PC and SP into the hold mode and disables the write circuitry to the RAM. The auxiliary register (R) is under control of the $\overline{RE}$ input when $\overline{IEN}$ is HIGH, independent of the state of the Instruction inputs. The $\overline{IEN}$ input does not affect the combinatorial data paths or Y outputs in the Am2930. The data paths are selected by the Instruction and $\overline{CC}$ inputs and are not affected by $\overline{IEN}$.

Am2930 INSTRUCTION SET

The Am2930 Instruction set can be divided into five types of instructions. These are:

- Unconditional Fetches
- Conditional Jumps
- Conditional Jumps-to-Subroutine
- Conditional Returns-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Unconditional Fetches

As can be seen from Table 1, there are nine unconditional Fetch instructions (Instructions 1-9). Under control of the Instruction inputs, the desired function is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instructions 1 through 7, the auxiliary register is under control of the RE input. For Instructions 8 and 9, R is loaded with PC and R + D, respectively. The RAM and Stack Pointer are not changed during a Fetch instruction.

Conditional Jumps

There are six conditional Jump instructions (Instructions 16 through 21). Under control of the Instruction inputs, the desired function is placed at the Y outputs. Additionally, the desired function is incremented if C_i of the least significant device is HIGH and loaded into PC. During these instructions, R is controlled by $\overline{RE}$. The RAM and Stack Pointer are not changed during these instructions. The above operations are performed if the $\overline{CC}$ input is LOW; if $\overline{CC}$ is HIGH, a Fetch PC operation is performed.

Conditional Jumps-to-Subroutine

There are six conditional Jump-to-Subroutine instructions (Instructions 22 through 27). Under control of the Instruction inputs, the desired function is placed on the Y outputs. On the rising edge of the clock the data on the Y outputs is incremented and loaded into PC, PC is loaded into the RAM at location SP+1; and SP is incremented.

As with Conditional Jump Instructions, R is controlled by $\overline{RE}$ and whether the Jump-to-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Conditional Returns-from-Subroutine

There are two conditional Return-from-Subroutine instructions (Instructions 28 and 29). Under control of the instruction inputs, either S or S+D is placed at the Y outputs. Additionally, the selected function is incremented and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

As with the Condition Jump and Jump-to-Subroutine Instructions, R is controlled by $\overline{RE}$ and whether the Return-from-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM is unchanged and R is controlled by $\overline{RE}$.

Load R (Instruction 10)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 11)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 12)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 13)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is controlled by $\overline{RE}$.

Pop PC (Instruction 14)

This instruction is the same as Fetch PC except SP is decremented at the end of the cycle, causing the data at the top of the stack to be lost.

Hold (Instruction 15)

This instruction places PC at the Y outputs and inhibits any change in PC, SP, and RAM. R is controlled by $\overline{RE}$.

Conditional Hold (Instruction 30)

This instruction is the same as Hold except $\overline{CC}$ must be LOW. If $\overline{CC}$ is HIGH, the Fetch PC instruction is performed.

Suspend (Instruction 31)

The Suspend instruction is the same as th Conditional Hold instruction except the Y outputs are forced into the high-impedance state if $\overline{CC}$ is LOW.

TABLE I – Am2930 INSTRUCTION SET

Mnemonic	Instruction Number	I_4	I_3	I_2	I_1	I_0	$\overline{CC}$	$\overline{IEN}$	Instruction	Y_0-Y_3	Next State (after CP ↓) (Note 3) PC	R $\overline{RE}$ = L	R $\overline{RE}$ = H	RAM	SP
		X	X	X	X	X	X	H	Instruction Disable	Note 1	–	D	–	–	–
PRST	0	L	L	L	L	L	X	L	RESET	"0"	"0"+C_i	D	–	–	Reset
FPC	1	L	L	L	L	H	X	L	FETCH PC	PC	PC+C_i	D	–	–	–
FR	2	L	L	L	H	L	X	L	FETCH R	R	PC+C_i	D	–	–	–
FD	3	L	L	L	H	H	X	L	FETCH D	D	PC+C_i	D	–	–	–
FRD	4	L	L	H	L	L	X	L	FETCH R+D	R+D+C_n	PC+C_i	D	–	–	–
FPD	5	L	L	H	L	H	X	L	FETCH PC+D	PC+D+C_n	PC+C_i	D	–	–	–
FPR	6	L	L	H	H	L	X	L	FETCH PC+R	PC+R+C_n	PC+C_i	D	–	–	–
FSD	7	L	L	H	H	H	X	L	FETCH S+D	S+D+C_n	PC+C_i	D	–	–	–
FPLR	8	L	H	L	L	L	X	L	FETCH PC → R	PC	PC+C_i	PC	PC	–	–
FRDR	9	L	H	L	L	H	X	L	FETCH R+D → R	R+D+C_n	PC+C_i	R+D+C_n	R+D+C_n	–	–
PLDR	10	L	H	L	H	L	X	L	LOAD R	PC	PC+C_i	D	D	–	–
PSHP	11	L	H	L	H	H	X	L	PUSH PC	PC	PC+C_i	D	–	PC → Loc SP+1	SP+1
PSHD	12	L	H	H	L	L	X	L	PUSH D	PC	PC+C_i	D	–	D → Loc SP+1	SP+1
POPS	13	L	H	H	L	H	X	L	POP S	S	PC+C_i	D	–	–	SP–1
POPP	14	L	H	H	H	L	X	L	POP PC	PC	PC+C_i	D	–	–	SP–1
PHLD	15	L	H	H	H	H	X	L	HOLD	PC	–	D	–	–	
	16-31	H	X	X	X	X	H	L	FAIL COND'L TEST (FETCH PC)	PC	PC+C_i	D	–	–	–
JMPR	16	H	L	L	L	L	L	L	JUMP R	R	R+C_i	D	–	–	–
JMPD	17	H	L	L	L	H	L	L	JUMP D	D	D+C_i	D	–	–	–
JMPZ	18	H	L	L	H	L	L	L	JUMP "0"	"0"	"0"+C_i	D	–	–	–
JPRD	19	H	L	L	H	H	L	L	JUMP R+D	R+D+C_n	R+D+C_n+C_i	D	–	–	–
JPPD	20	H	L	H	L	L	L	L	JUMP PC+D	PC+D+C_n	PC+D+C_n+C_i	D	–	–	–
JPPR	21	H	L	H	L	H	L	L	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	D	–	–	–
JSBR	22	H	L	H	H	L	L	L	JSB R	R	R+C_i	D	–	PC → Loc SP+1	SP+1
JSBD	23	H	L	H	H	H	L	L	JSB D	D	D+C_i	D	–	PC → Loc SP+1	SP+1
JSBZ	24	H	H	L	L	L	L	L	JSB "0"	"0"	"0"+C_i	D	–	PC → Loc SP+1	SP+1
JSRD	25	H	H	L	L	H	L	L	JSB R+D	R+D+C_n	R+D+C_n+C_i	D	–	PC → Loc SP+1	SP+1
JSPD	26	H	H	L	H	L	L	L	JSB PC+D	PC+D+C_n	PC+D+C_n+C_i	D	–	PC → Loc SP+1	SP+1
JSPR	27	H	H	L	H	H	L	L	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	D	–	PC → Loc SP+1	SP+1
RTS	28	H	H	H	L	L	L	L	RETURN S	S	S+C_i	D	–	–	SP–1
RTSD	29	H	H	H	L	H	L	L	RETURN S+D	S+D+C_n	S+D+C_n+C_i	D	–	–	SP–1
CHLD	30	H	H	H	H	L	L	L	HOLD	PC	–	D	–	–	–
PSUS	31	H	H	H	H	H	L	L	SUSPEND	Z (Note 2)	–	D	–	–	–

PC – Program Counter SP – Stack Pointer
R – Auxiliary Register D – Direct Inputs

Notes: 1. When $\overline{IEN}$ is HIGH, the Y_0-Y_3 outputs contain the same data as when $\overline{IEN}$ is LOW, as determined by I_0-I_4 and $\overline{CC}$.
2. Z = High impedance state (outputs "OFF").
3. – = No change

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2930PC, DC	T_A = 0 to 70°C	4.75V to 5.25V
Am2930DM, FM	T_C = −55 to +125°C	4.50V to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 $\overline{G}$, C_{n+4}, C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, C_{n+4} C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				−.702	
			$\overline{CC}$				−.657	
			C_i				−2.31	
			C_n				−3.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				40	
			$\overline{CC}$				50	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V		V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = 5.0V		T_A = 25°C		150	205	mA
		V_{CC} = MAX.		T_C = −55 to +125°C			239	
				T_C = +125°C			170	
				T_A = 0 to 70°C			220	
				T_A = 70°C			185	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

Am2930 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2930. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. Typical Room Temperature Performance.

V_{CC} = 5.0V, T_A = 25°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	18ns
Minimum Clock HIGH Time	20ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	18	17
$\overline{CC}$ (Note 1)	Y	39	27
I_{4-0} (Note 1)	Y	57	41

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	61	50	57	61	69	52	–
$\overline{CC}$	46	32	39	–	53	29	–
C_n	25	–	17	–	32	–	–
C_i	–	–	–	14	14	–	–
CP	52	40	46	33	58	40	40
D	37	23	30	–	43	–	–
$\overline{IEN}$	–	–	–	–	–	27	–

Note 1: "Suspend" instruction.

TABLE ID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	68	0
$\overline{CC}$	53	0
$\overline{IEN}$	39	0
C_n	28	0
C_i	18	3
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	14	0
D (All other conditions)	44	0
$\overline{RE}$	13	2

II. Guaranteed Performance Over Commercial Operating Range.

V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	27	26
$\overline{CC}$ (Note 1)	Y	55	37
I_{4-0} (Note 1)	Y	80	55

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	81	67	77	80	91	69	–
$\overline{CC}$	63	45	55	–	72	42	–
C_n	32	–	25	–	45	–	–
C_i	–	–	–	22	22	–	–
CP	69	53	61	43	78	55	55
D	49	33	40	–	59	–	–
$\overline{IEN}$	–	–	–	–	–	40	–

Note 1: "Suspend" instruction.

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	114	0
$\overline{CC}$	75	0
$\overline{IEN}$	55	0
C_n	43	0
C_i	32	5
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	25	2
D (All other conditions)	66	2
$\overline{RE}$	24	4

III. Guaranteed Performance Over Military Operating Range.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	32	31
$\overline{CC}$ (Note 1)	Y	60	42
I_{4-0} (Note 1)	Y	85	60

TABLE IIIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	88	74	82	87	97	78	–
$\overline{CC}$	68	52	60	–	78	47	–
C_n	37	–	30	–	46	–	–
C_i	–	–	–	23	23	–	–
CP	74	58	66	48	84	60	60
D	55	38	45	–	65	–	–
$\overline{IEN}$	–	–	–	–	–	45	–

Note 1: "Suspend" instruction.

TABLE IIID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	124	0
$\overline{CC}$	80	0
$\overline{IEN}$	69	0
C_n	52	0
C_i	37	5
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	30	2
D (All other conditions)	72	2
$\overline{RE}$	29	4

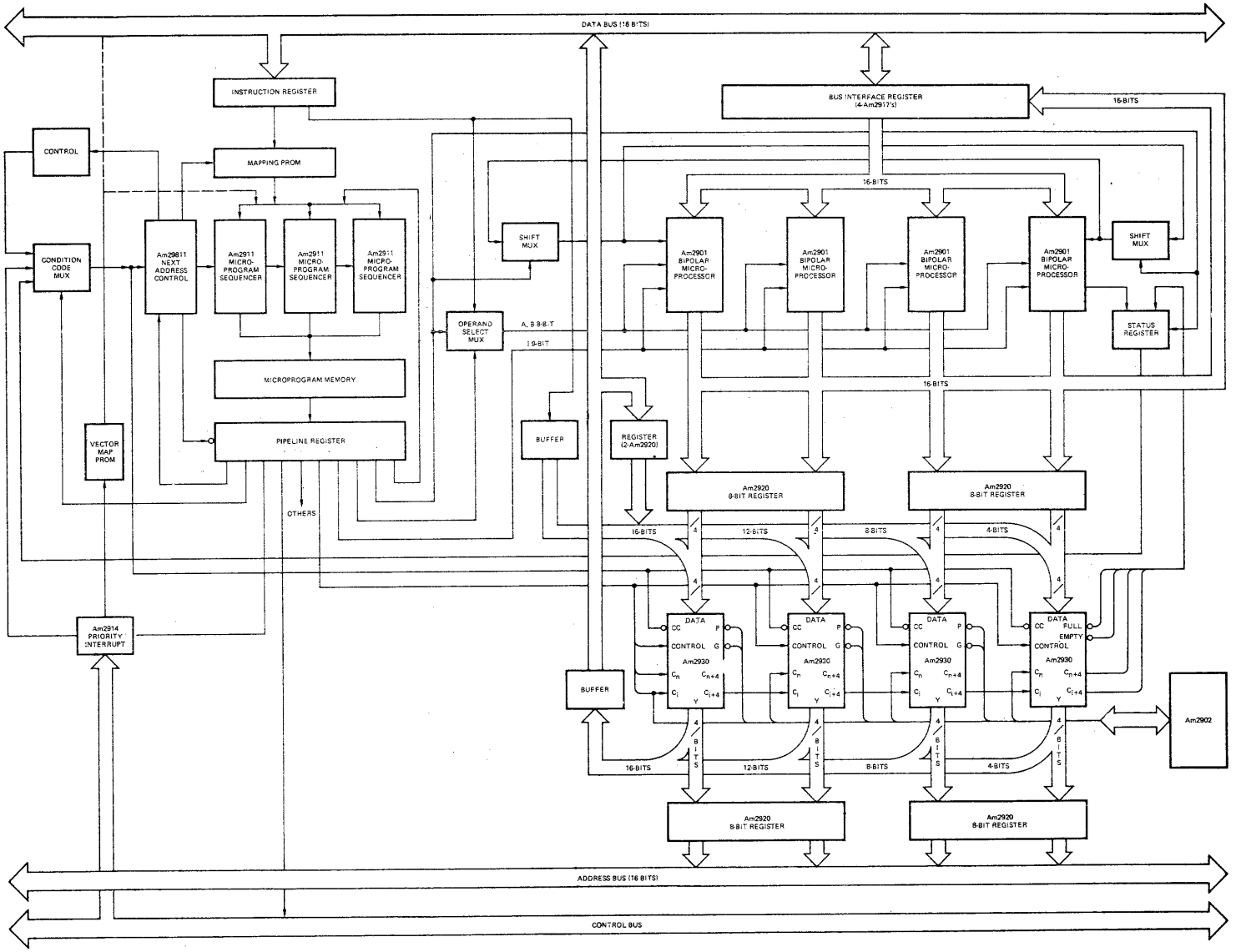


Figure 1. Typical 16-Bit Microcomputer Design.

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APPLICATIONS

The Am2930 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2930 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901's via a 16-bit register.

The Address outputs (Y) of the Am2930 are loaded into a 16-bit Memory Address Register (MAR). Although the MAR is shown as part of the CPU, in some applications it may be part of the memory.

An Am2902 High-Speed Lookahead Carry Generator is utilized to provide high-speed relative and indexed addressing. In slower systems, the C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The Condition Code input ($\overline{CC}$) is derived from the same condition code multiplexer which generates the condition code input for the microprogram sequencer.

The control inputs of the Am2930 (I_{0-4}, $\overline{IEN}$, $\overline{RE}$, $\overline{OE}$, and C_i and C_n of the least significant device) are shown originating at the Pipeline Register. Although it is not shown in Figure 1, it is possible to share the Pipeline Register outputs which go to these pins with another device. This can be accomplished if both the Am2930 and the other device do not operate on the same microcycle. Forcing the $\overline{IEN}$ input HIGH inhibits any changes in the Am2930 internal registers, independent of the state of these seven inputs. This allows the Am2930 to be placed in a hold mode while the other device is using the same Pipeline Register outputs as control signals.

PIN DEFINITIONS

I_{0-4} The five Instruction control lines to the Am2930, used to establish data paths and enable internal registers.

$\overline{IEN}$ The Instruction Enable Input, used to enable and disable internal registers. When $\overline{IEN}$ is LOW, all internal registers are under control of the Instruction inputs. When $\overline{IEN}$ is HIGH, all internal registers except R are inhibited from changing state. R is controlled by the $\overline{RE}$ input. The $\overline{IEN}$ input does not affect the combinatorial data paths and the outputs established by the Instruction inputs.

$\overline{CC}$ The Condition Code input determines whether or not a conditional instruction (Instructions 16-31) is performed. If $\overline{CC}$ is LOW, the conditional instruction is executed. If $\overline{CC}$ is HIGH, Fetch PC (Instruction 1) is executed. The $\overline{CC}$ input may be either HIGH or LOW for unconditional instructions (Instructions 0-15).

$\overline{RE}$ The Register Enable input for the Auxiliary Register (R). A LOW on $\overline{RE}$ causes the Auxiliary Register (R) to be loaded from the D inputs unless Instruction 8 or 9 is being executed and $\overline{IEN}$ is LOW.

C_n The carry-in to the Full Adder.

C_{n+4} The carry-out of the Full Adder.

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Full Adder.

C_i The carry-in to the program counter incrementer.

C_{i+4} The carry-out of the program counter incrementer.

Y_{0-3} The four address outputs of the Am2930. These are three-state output lines. When enabled, they display the outputs of the Full Adder.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high-impedance); when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

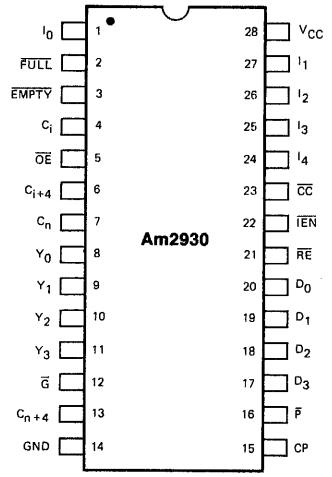
D_{0-3} The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.

$\overline{Empty}$ The Empty output is LOW when the Stack is empty.

$\overline{Full}$ The Full output is LOW when the LIFO stack is full — during and after the 17th push operation.

CP The clock input to the Am2930. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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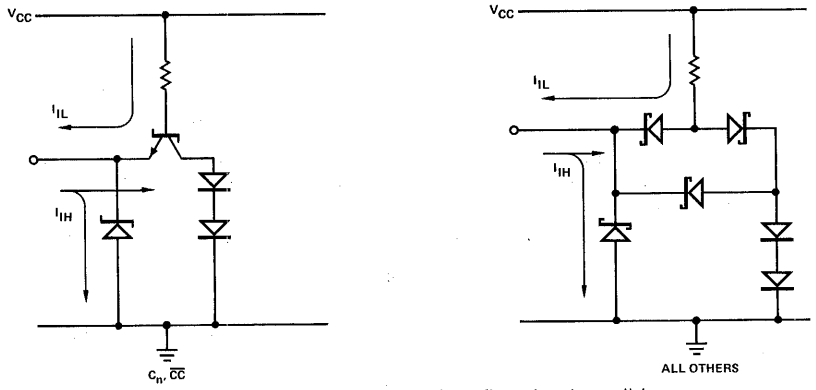
INPUT/OUTPUT CIRCUIT CURRENT INTERFACE

DRIVEN INPUTS



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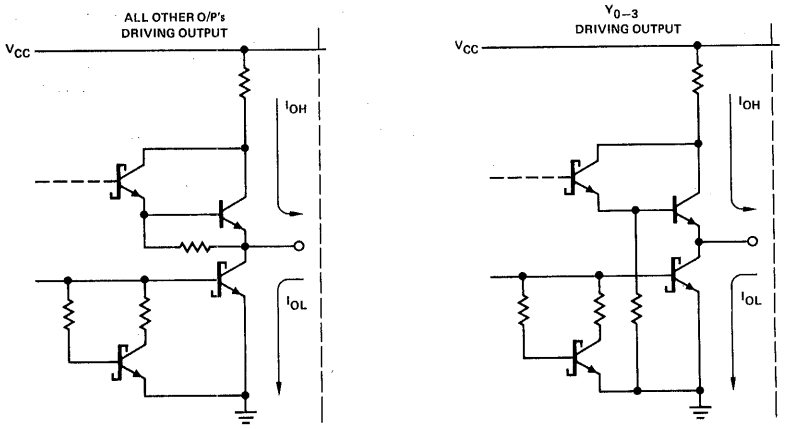
Note; C_i input is connected to both configurations in parallel.

DRIVING OUTPUTS



Note; Actual current flow direction shown.

MPR-224

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2930PC	P-28	C	C-1
AM2930DC	D-28	C	C-1
AM2930DC-B	D-28	C	B-2 (Note 4)
AM2930DM	D-28	M	C-3
AM2930DM-B	D-28	M	B-3
AM2930FM	F-28-2	M	C-3
AM2930FM-B	F-28-2	M	B-3
AM2930XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2930XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V; M = −55 to +125°C, V_{CC} = 4.50 to 5.50V
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2932

Program Control Unit/Push-Pop Stack

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 16 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Eight relative address instructions are provided, including jump relative and jump-to-subroutine relative
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

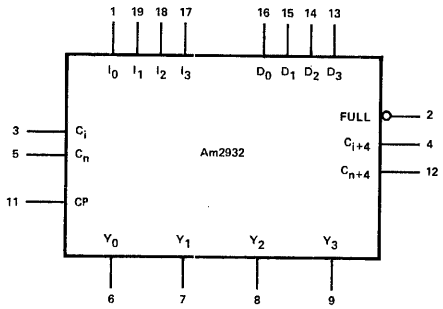
GENERAL DESCRIPTION

The Am2932 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2932s may be interconnected to generate a 16-bit address (64K words). The Am2932 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2932 performs five types of instructions. These are: 1) Fetch; 2) Jump; 3) Jump-to-Subroutine; 4) Return-from-Subroutine; and 5) miscellaneous instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter(PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_3), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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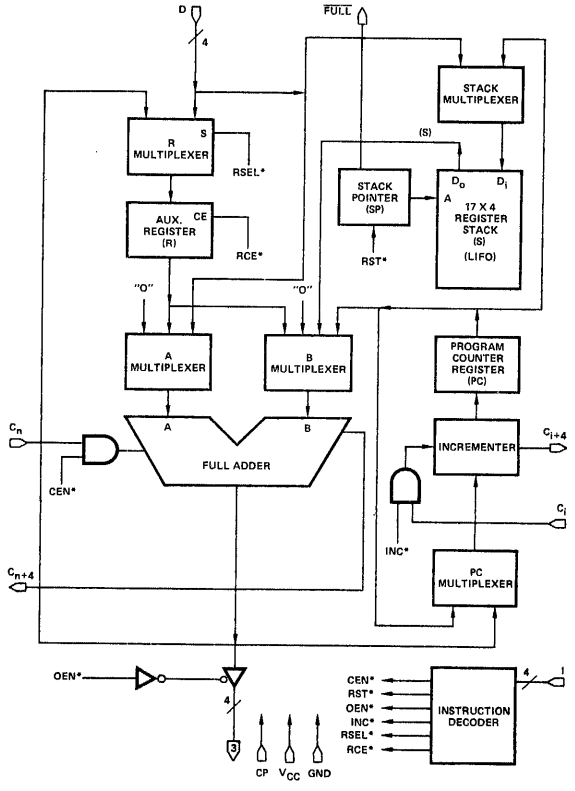
BLOCK DIAGRAM



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ARCHITECTURE OF THE Am2931/32

The Am2932 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition. The carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During the suspend instruction the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Instruction inputs call for it to be loaded.

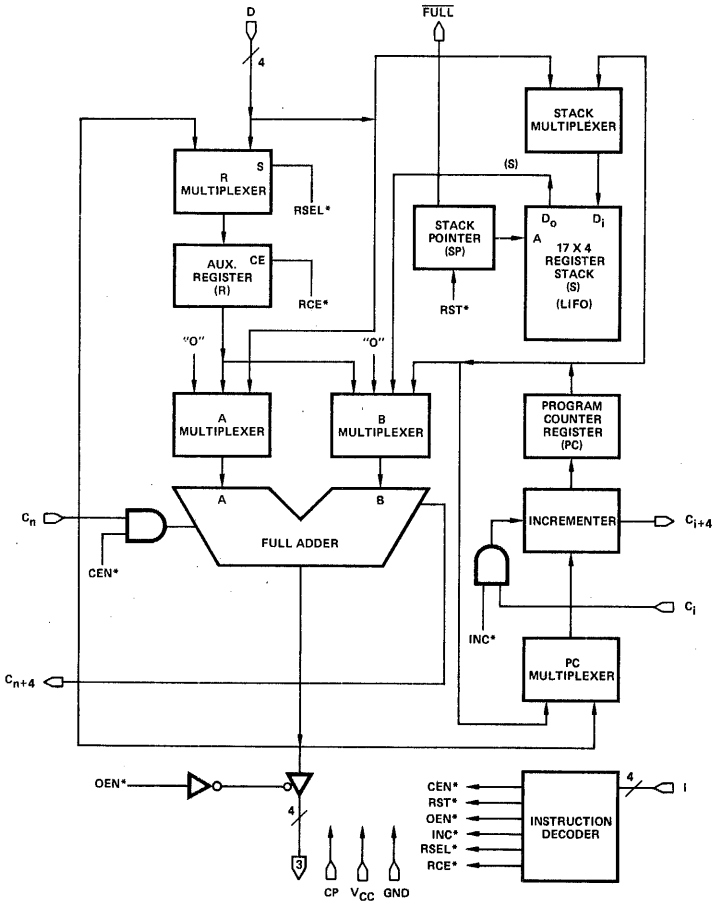
Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

Output Buffers

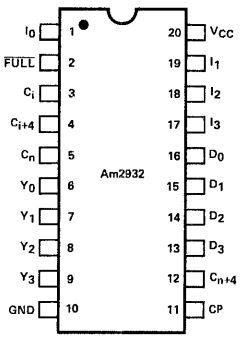
The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled under Instruction control.

BLOCK DIAGRAM



BLI-096

CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation.

TABLE I — Am2932 INSTRUCTION SET

Instruction Number	I_3	I_2	I_1	I_0	Mnemonic	Instruction	Y_0-Y_3	Next State (after CP↑) — Note 2			
								PC	R	RAM	SP
0	L	L	L	L	PRST	RESET	"0"	"0"+C_i	—	—	Reset
1	L	L	L	H	PSUS	SUSPEND	Z (Note 1)	—	—	—	—
2	L	L	H	L	PSHD	PUSH D	PC	PC+C_i	—	D→Loc SP+1	SP+1
3	L	L	H	H	POPS	POP S	S	PC+C_i	—	—	SP—1
4	L	H	L	L	FPC	FETCH PC	PC	PC+C_i	—	—	—
5	L	H	L	H	JMPD	JUMP D	D	D+C_i	—	—	—
6	L	H	H	L	PSHP	PUSH PC	PC	PC+C_i	—	PC→Loc SP+1	SP+1
7	L	H	H	H	RTS	RETURN S	S	S+C_i	—	—	SP—1
8	H	L	L	L	FR	FETCH R	R	PC+C_i	—	—	—
9	H	L	L	H	FPR	FETCH PC+R	PC+R+C_n	PC+C_i	—	—	—
10	H	L	H	L	FPLR	FETCH PC→R	PC	PC+C_i	PC	—	—
11	H	L	H	H	JMPR	JUMP R	R	R+C_i	—	—	—
12	H	H	L	L	JPPR	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	—	—	—
13	H	H	L	H	JSBR	JSB R	R	R+C_i	—	PC→Loc SP+1	SP+1
14	H	H	H	L	JSPR	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	—	PC→Loc SP+1	SP+1
15	H	H	H	H	PLDR	LOAD R	PC	PC+C_i	D	—	—

Notes: 1. Z = High impedance state (outputs "OFF")
2. — = No change

PC — Program Counter
R — Auxiliary Register
SP — Stack Pointer
D — Direct Inputs

2

Am2932 INSTRUCTION SET

The Am2932 Instruction set can be divided into five types of instructions. These are:

- Fetches
- Jumps
- Jumps-to-Subroutine
- Return-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Fetches

As can be seen from Table I, there are four Fetch instructions (Instructions 4, 8, 9, 10). Under control of the Instructions inputs, the desired function is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instruction 10 R is loaded with PC. The RAM and Stack Pointer are not changed during a Fetch instruction.

Jumps

There are three Jump instructions (Instructions 5, 11, 12). Under control of the Instruction inputs, the desired function is placed at the Y outputs. Additionally, the desired function is incremented if C_i of the least significant device is HIGH and loaded into PC. The RAM, Stack Pointer and R are not changed during these instructions.

Jumps-to-Subroutine

There are two Jump-to-Subroutine instructions (Instructions 13 and 14). Under control of the Instruction inputs, the desired function is placed on the Y outputs. On the rising edge of the clock the data on the Y outputs is incremented and loaded into PC, PC is loaded into the RAM at location SP+1; and SP is incremented.

During these instructions, R is not changed.

Return-from-Subroutine (Instruction 7)

Under control of the instruction inputs, S is placed at the Y outputs. Additionally, S is incremented and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

During this instruction, R is not changed.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM and R are unchanged.

Load R (Instruction 15)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 6)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 2)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 3)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is not changed.

Suspend (Instruction 1)

The Suspend instruction inhibits any change in PC, SP, R and RAM and forces the Y outputs into the high impedance state.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2932PC, DC	T_A = 0 to 70°C	4.75V to 5.25V
Am2932DM	T_C = −55 to +125°C	4.50V to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 G, C_{n+4}, C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{FULL}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			C_{n+4}, C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{FULL}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-3}, CP				−.702	
			C_i				−2.0	
			C_n				−3.69	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-3}, CP				40	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V				−50	μA
I_{OZH}			V_{OUT} = 2.4V				50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = 5.0V	T_A = 25°C			128	176	mA
		V_{CC} = MAX.	T_C = −55 to +125°C				210	
			T_C = +125°C				145	
			T_A = 0 to 70°C				190	
			T_A = 70°C				160	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

Am2932 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2932. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. Typical Room Temperature Performance.

V_{CC} = 5.0V, T_A = 25°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	18ns
Minimum Clock HIGH Time	20ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	57	41

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	61	57	69	61	52
C_n	25	17	32	–	–
C_i	–	–	14	14	–
CP	52	46	58	33	40
D	29	–	37	–	–

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

TABLE ID
Set-up and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: Set-up Time	Hold Time
C_n	28	0
C_i	18	3
D	35	0
I_{3-0}	68	0

II. Guaranteed Performance Over Commercial Operating Range.

V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	80	55

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	81	77	91	80	69
C_n	32	25	45	–	–
C_i	–	–	22	22	–
CP	69	61	78	43	55
D	39	–	50	–	–

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: Set-up Time	Hold Time
C_n	43	0
C_i	32	5
D	52	2
I_{3-0}	114	0

III. Guaranteed Performance Over Military Operating Range.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	85	60

TABLE IIIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	88	82	97	87	78
C_n	37	30	46	–	–
C_i	–	–	23	23	–
CP	74	66	84	45	60
D	44	–	55	–	–

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

TABLE IIID
Set-up and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: Set-up Time	Hold Time
C_n	52	0
C_i	37	5
D	60	2
I_{3-0}	124	0

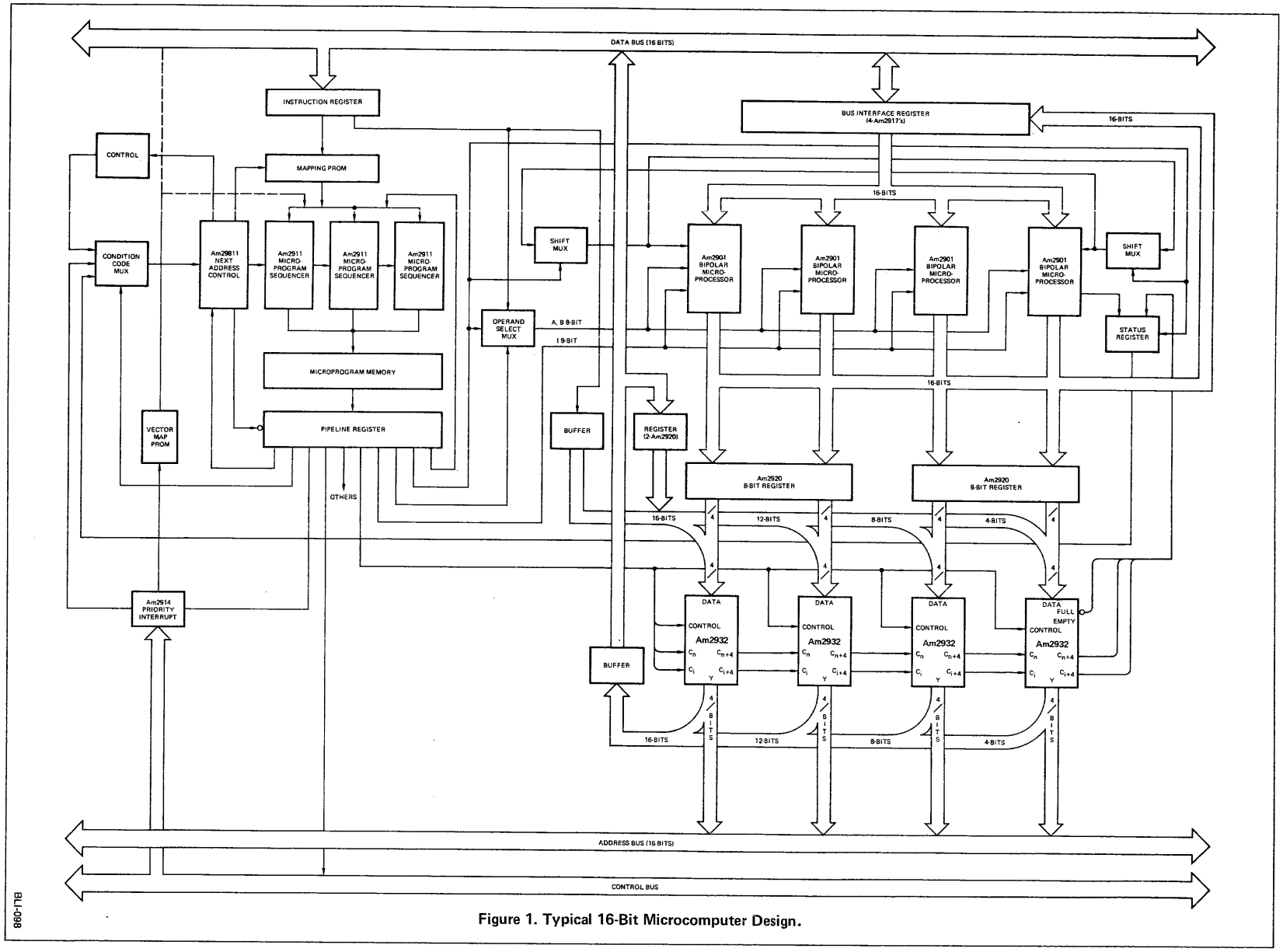

Figure 1. Typical 16-Bit Microcomputer Design.

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APPLICATIONS

The Am2932 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2932 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901s via a 16-bit register.

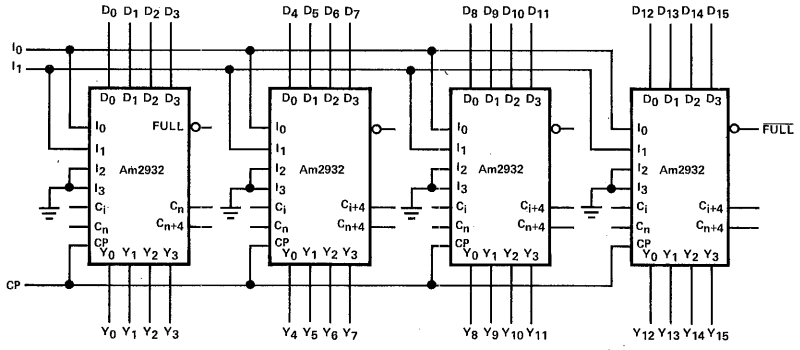
The Address outputs (Y) of the Am2932 are passed to the address bus.

The C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

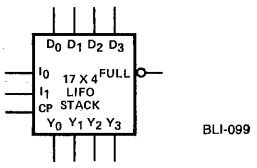
The control inputs of the Am2932 (I_{0-3}, C_i and C_n of the least significant device) are shown originating at the Pipeline Register.

PIN DEFINITIONS

I_{0-3}	The four Instruction control lines to the Am2932, used to establish data paths and enable internal registers.
C_n	The carry-in to the Full Adder.
C_{n+4}	The carry-out of the Full Adder.
C_i	The carry-in to the program counter incrementer.
C_{i+4}	The carry-out of the program counter incrementer.
Y_{0-3}	The four address outputs of the Am2932. These are three-state output lines. When enabled, they display the outputs of the Full Adder.
D_{0-3}	The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.
$\overline{Full}$	The Full output is LOW when the LIFO stack is full – during and after the 17th push operation.
CP	The clock input to the Am2932. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.



I_1	I_0	INSTRUCTION	Y OUTPUTS
L	L	RESET	"0"
L	H	SUSPEND	Z (HIGH IMPEDANCE)
H	L	PUSH D	SEE NOTE 1
H	H	POP S	TOP OF STACK

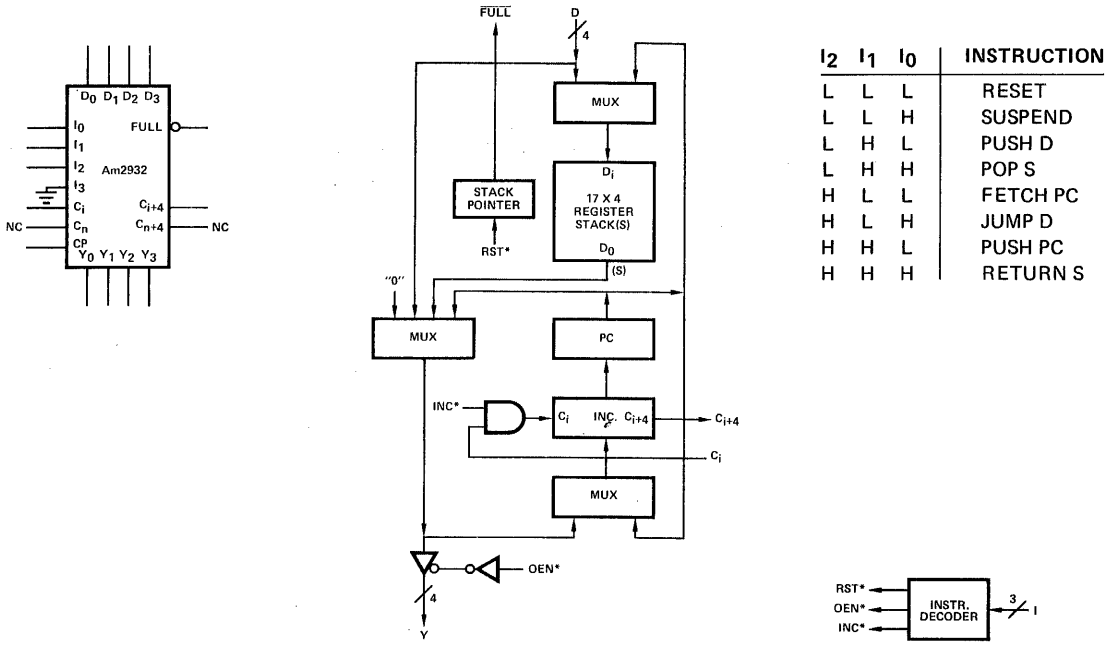


Equivalent Logic Symbol for Am2932 with I_2, I_3 Grounded

Figure shows the use of four Am2932s as a 17-word by 16-bit LIFO stack by grounding I_2 and I_3. The effect of grounding I_3 is shown in Figure 3.

Note 1. During this instruction, PC is placed on the Y outputs. If C_i is held LOW, the Y outputs will be LOW for this instruction after the device is initialized with a Reset instruction.

Figure 2. Application of Four Am2932s as a 17-Word by 16-Bit LIFO Stack.



I_2	I_1	I_0	INSTRUCTION
L	L	L	RESET
L	L	H	SUSPEND
L	H	L	PUSH D
L	H	H	POP S
H	L	L	FETCH PC
H	L	H	JUMP D
H	H	L	PUSH PC
H	H	H	RETURN S

Figure 3. Equivalent Circuit of Am2932 with I_3 Grounded.

BLI-100

ORDERING INFORMATION

Am2932 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2932PC	P-20	C	C-1
AM2932DC	D-20	C	C-1
AM2932DC-B	D-20	C	B-2 (Note 4)
AM2932DM	D-20	M	C-3
AM2932DMB	D-20	M	B-3
AM2932FM	F-20	M	C-3
AM2932FMB	F-20	M	B-3
AM2932XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2932XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V
   M = −55 to +125°C, V_{CC} = 4.50 to 5.50V
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2940
DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- DMA Address Generation
  Generates memory address, word count and DONE signal for DMA transfer operation.
- Expandable Eight-bit Slice
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- Repeat Data Transfer Capability
  Initial memory address and word count are saved so that the data transfer can be repeated.
- Programmable Control Modes
  Provides four types of DMA transfer control plus memory address increment/decrement.
- High Speed, Bipolar LSI
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 50ns and 24mA output current sink capability.
- Microprogrammable
  Executes 8 different instructions.

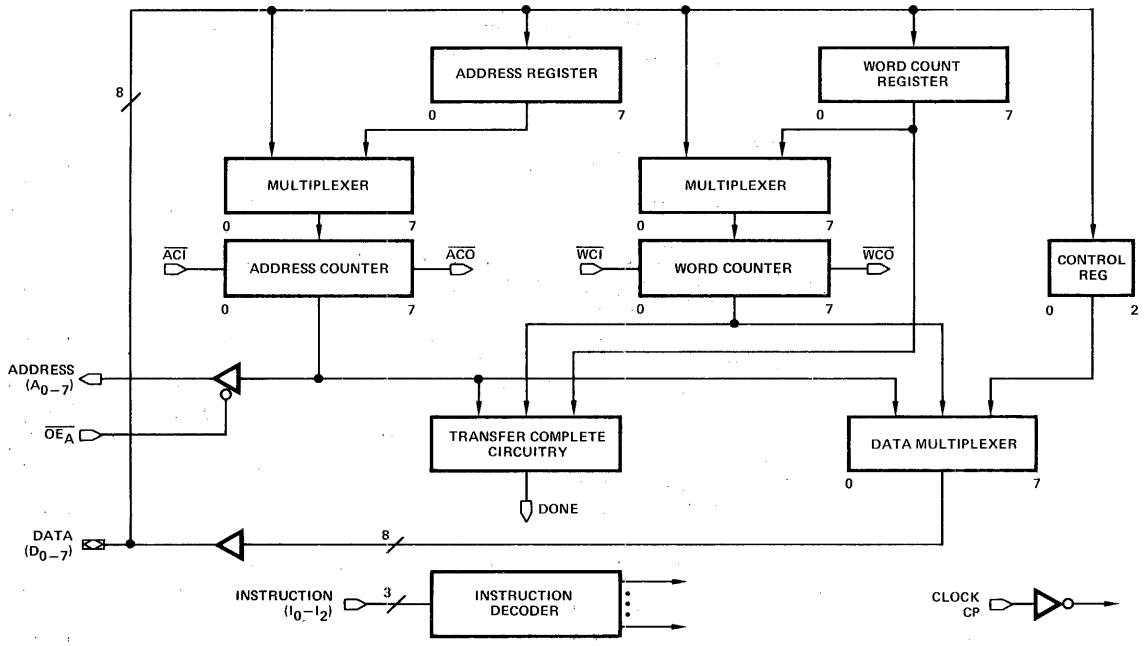
GENERAL DESCRIPTION

The Am2940, a 28-pin member of Advanced Micro Devices Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

BLOCK DIAGRAM



Am2940 DMA Address Generator

MPR-226

Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits 0 and 1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

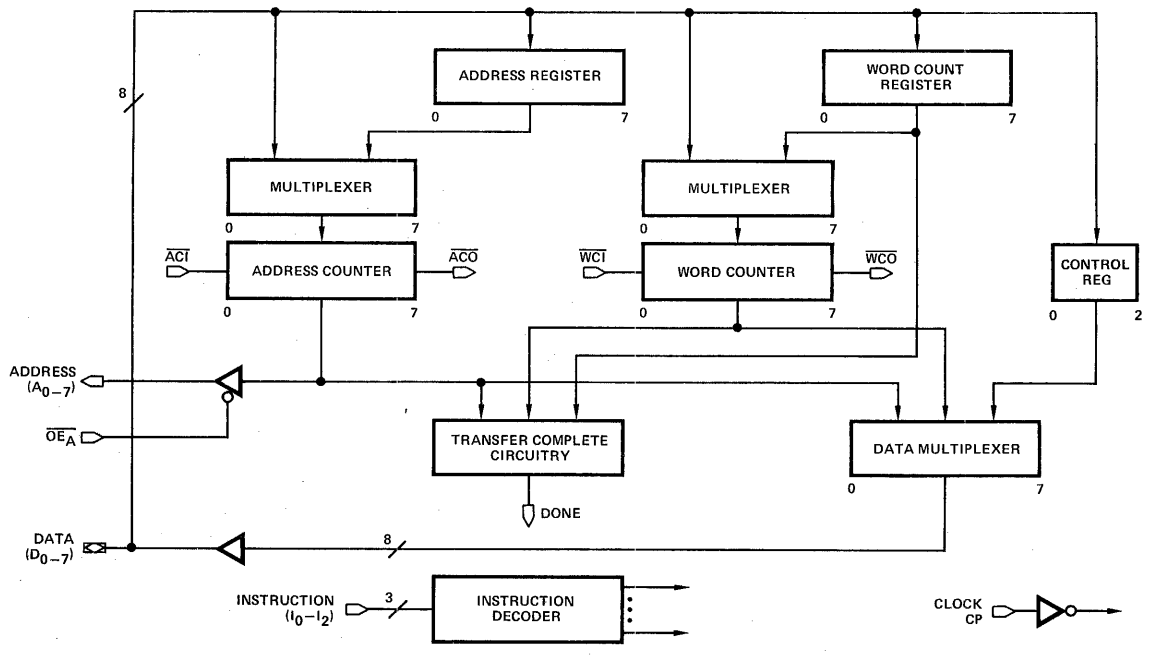
CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

Figure 1. Control Register Format Definition.

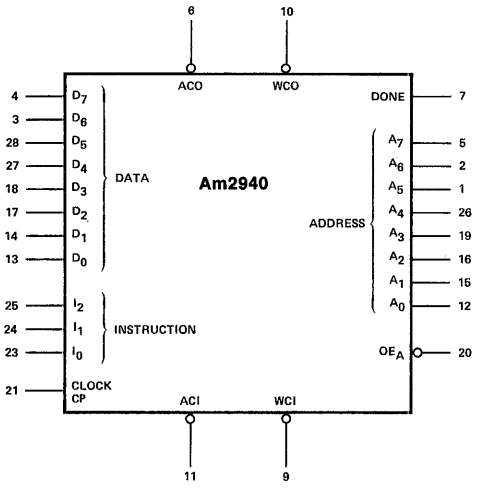
BLOCK DIAGRAM



Am2940 DMA Address Generator

MPR-226

LOGIC SYMBOL



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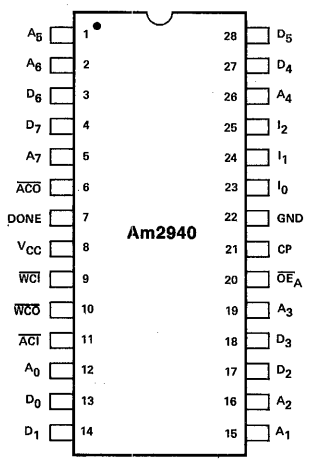
CONNECTION DIAGRAMS
Top Views

DIP



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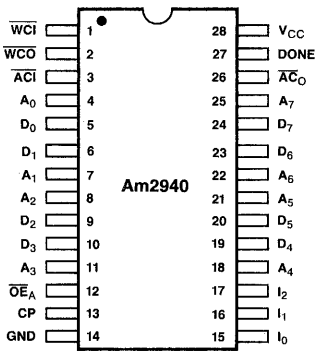
Flat Pack



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Note: Pin 1 is marked for orientation

Am2940 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register, one instruction enables the Address and Word counters, and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

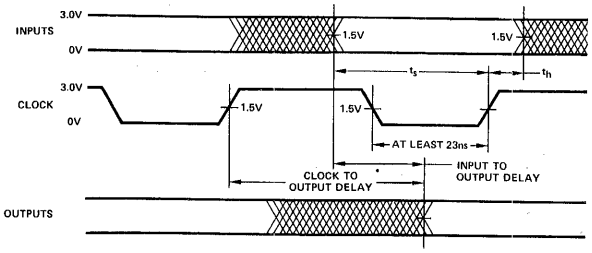
P/N	Range	Temperature	V_{CC}	
Am2940PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2940DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

2

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA	2.4			Volts
				COM'L I_{OH} = −2.6mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL} (Note 5)	WCO, ACO	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			A_{0-7}, D_{0-7} DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7}			−0.15	mA
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7}			150	µA
				All Others			40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_O = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	A_{0-7}			−50	µA
				D_{0-7}			−150	
I_{OZH}			V_{OUT} = 2.4V	A_{0-7}			50	
				D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		170	275	mA
			Am2940PC, DC	T_A = 0°C to +70°C			290	
				T_A = +70°C			235	
			Am2940DM, FM	T_C = −55°C to +125°C			315	
				T_C = +125°C			225	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 2. Switching Waveforms.

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SWITCHING CHARACTERISTICS

The tables below define the Am2940 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times ($\overline{OE}$ to A and I to D) which are specified for a 5pF load. All times are in ns.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	13	3
I_{012}	33	2
$\overline{ACI}$	15	2
$\overline{WCI}$ (Note 1)	15	1

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	12	–	–	–	–
$\overline{WCI}$ (Note 2)	–	12	–	27	–
I_{0-2}	–	–	–	–	21
CP (Note 3)	35	35	35	50	–

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	25	ns
Maximum Clock Frequency	22	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	25	19	ns
$\overline{OE}$	A_{0-7}	19	13	ns

II. GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	21	4
I_{012}	41	3
$\overline{ACI}$	27	3
$\overline{WCI}$ (Note 1)	27	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	18	–	–	–	–
$\overline{WCI}$ (Note 2)	–	18	–	41	–
I_{0-2}	–	–	–	–	34
CP (Note 3)	50	50	48	77	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	18	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	30	30	ns
$\overline{OE}$	A_{0-7}	23	23	ns

III. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE
Am2940PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	5
I_{012}	46	4
$\overline{ACI}$	30	4
$\overline{WCI}$ (Note 1)	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–	–
$\overline{WCI}$ (Note 2)	–	20	–	46	–
I_{0-2}	–	–	–	–	37
CP (Note 3)	58	58	54	85	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	35	35	ns
$\overline{OE}$	A_{0-7}	25	25	ns

IV. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE
Am2940DM, FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	6
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$ (Note 1)	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–	–
$\overline{WCI}$ (Note 2)	–	21	–	54	–
I_0-I_2	–	–	–	–	41
CP (Note 3)	64	64	62	88	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	16	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	42	42	ns
$\overline{OE}$	A_{0-7}	30	30	ns

Notes: 1. Control modes 0, 1, and 3 only.
2. WCI to Done occurs only in control modes 0 and 1.
3. CP to Done occurs only in control modes 0, 1, and 2.

APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller. The Am2910 Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Transceivers, the Am2940, the Am2901A Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 4. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910 Microprogram Sequencer.

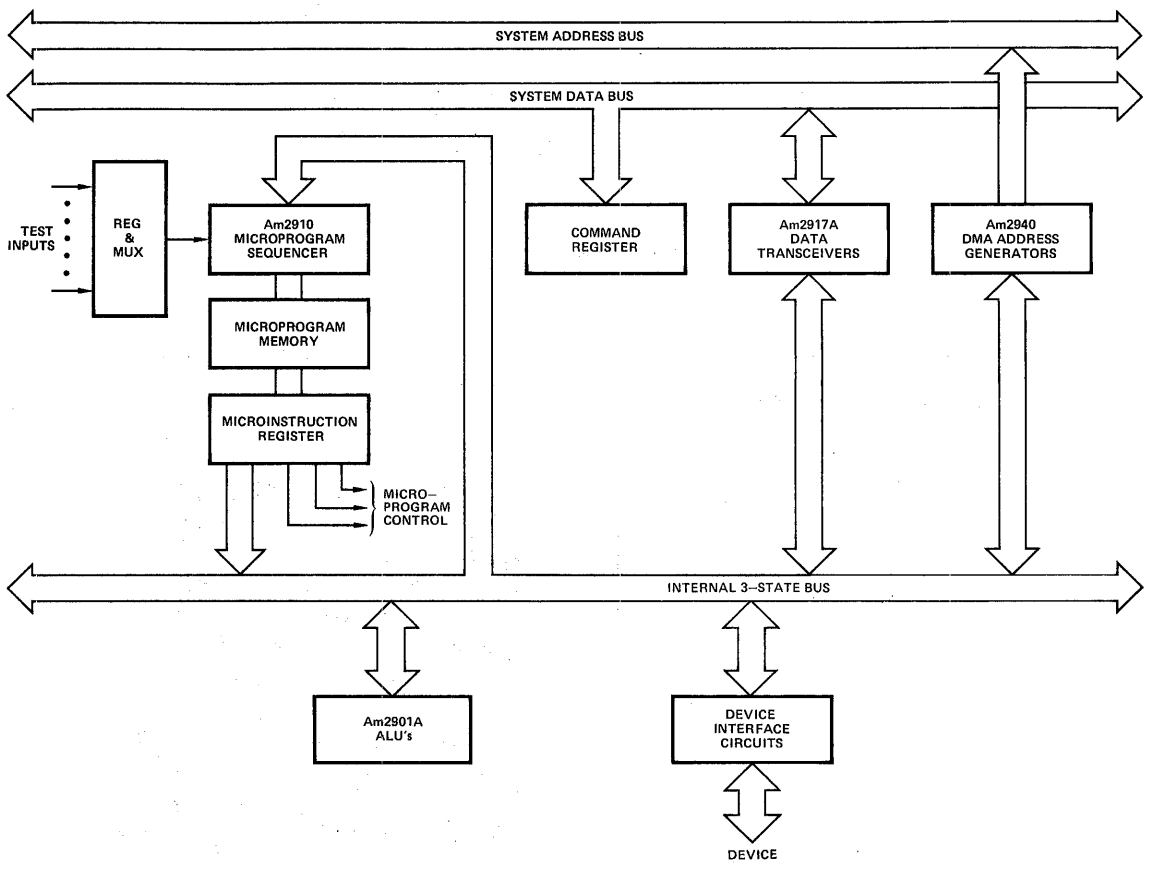

Figure 3. DMA Peripheral Controller Block Diagram.

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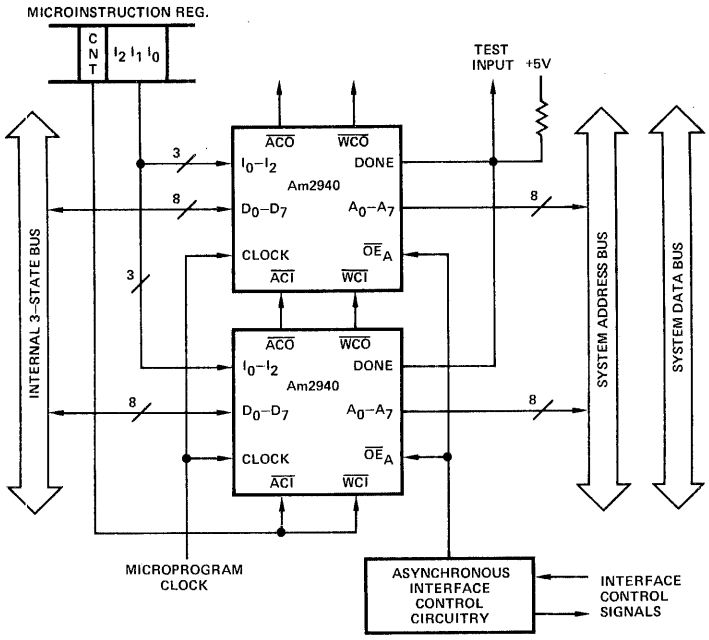

Figure 4. Am2940 Interconnections.

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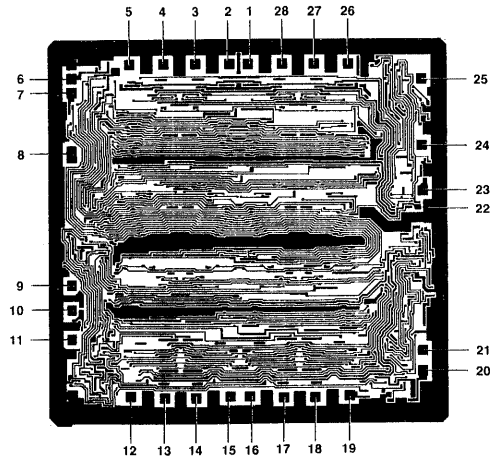
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2940PC	P-28	C	C-1
AM2940DC	D-28	C	C-1
AM2940DC-B	D-28	C	B-2 (Note 4)
AM2940DM	D-28	M	C-3
AM2940DM-B	D-28	M	B-3
AM2940FM	F-28-2	M	C-3
AM2940FM-B	F-28-2	M	B-3
AM2940XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2940XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in

METALLIZATION AND PAD LAYOUT



Note: Numbers refer to DIP pin connections.

DIE SIZE: 0.178" X 0.181"

Am2942

Programmable Timer/Counter
DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- 22-pin version of Am2940 –
  Provides multiplexed Address and Data lines plus additional Instruction Input and Instruction Enable pins.
- Can be used as either DMA Address Generator or Programmable Timer Counter.
- Executes 16 instructions –
  Eight DMA instructions plus eight Timer/Counter instructions
- Provides two independent programmable 8-bit up/down counters in a 22-pin package –
  Counters can be cascaded to form single-chip 16-bit up/down counter.
- Reinitialize capability –
  Counters can be reinitialized from on-chip registers.
- Expandable eight-bit slice –
  Any number of Am2942s can be cascaded. Three devices provide a 48 bit counter.
- Programmable control modes –
  Provide four types of control.
- High speed bipolar LSI –
  Advanced Low-Power Schottky TTL technology provides typical count frequency of 25MHz and 24mA output current sink capability.

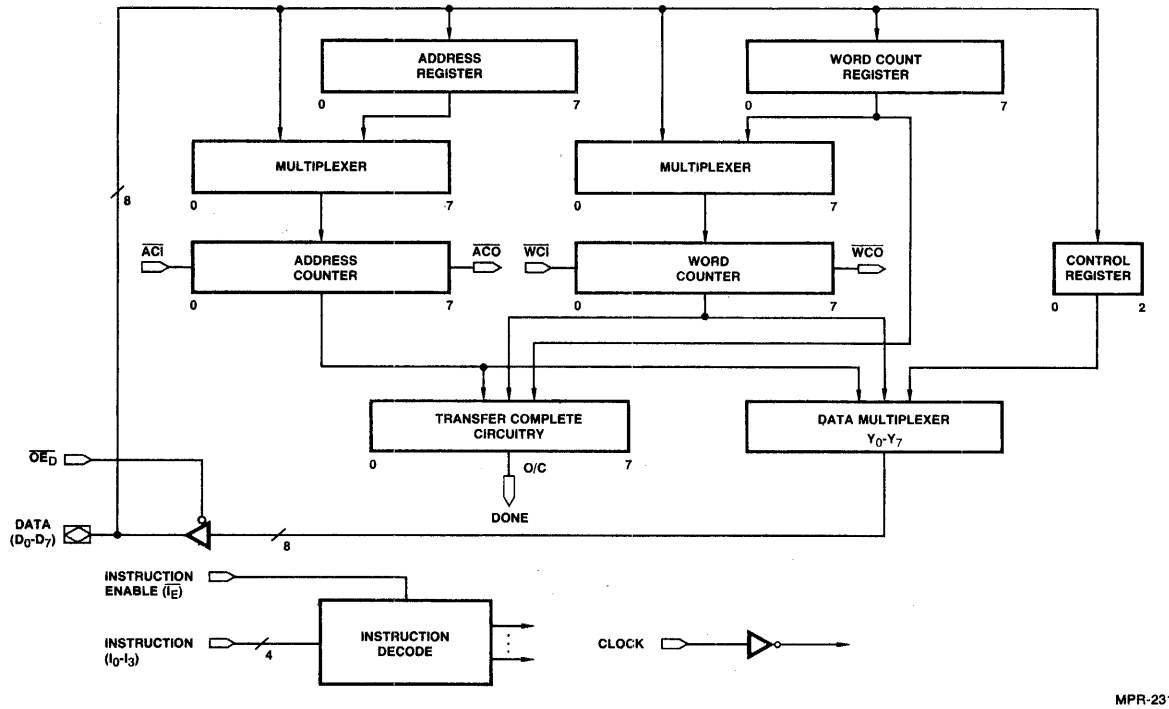
GENERAL DESCRIPTION

The Am2942, a 22-pin version of the Am2940, can be used as a high-speed DMA Address Generator or Programmable Timer/Counter. It provides multiplexed Address and Data lines, for use with a common bus, and additional Instruction Input and Instruction Enable pins. The Am2942 executes 16 instructions; eight are the same as the Am2940 instructions, and eight instructions facilitate the use of the Am2942 as a Programmable Timer/Counter. The Instruction Enable input allows the sharing of the Am2942 instruction field with other devices.

When used as a Timer/Counter, the Am2942 provides two independent, programmable, eight-bit, up-down counters in a 22-pin package. The two on-chip counters can be cascaded to form a single chip, 16-bit counter. Also, any number of chips can be cascaded – for example three cascaded Am2942s form a 48-bit timer/counter.

Reinitialization instructions provide the capability to reinitialize the counters from on-chip registers. Am2942 Programmable Control Modes, identical to those of the Am2940, offer four different types of programmable control.

BLOCK DIAGRAM



Am2942 ARCHITECTURE

As shown in the Block Diagram, the Am2942 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2942 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, and decrements in Control Modes 0 and 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, three-input multiplexer which allows the Address Counter, Word Counter and Control Register to be read at DATA lines D_0-D_7. The Data Multiplexer output, Y_0-Y_7, is enabled onto DATA lines D_{0-7} if and only if the Output Enable input, $\overline{OE}_D$, is LOW. (Refer to Figure 2.)

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_3 Control Register bits 0 and 1, and the INSTRUCTION ENABLE input, $\overline{I}_E$.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Decrement	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

H = HIGH
L = LOW

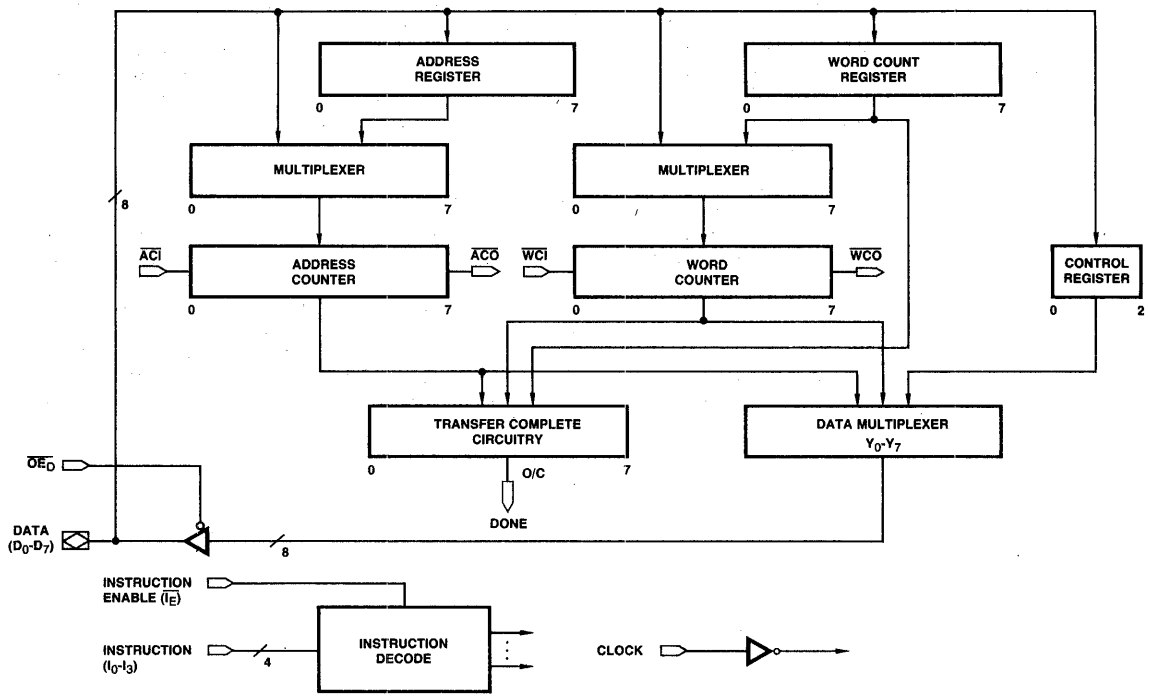
CR_2	Address Counter
L	Increment
H	Decrement

Figure 1. Control Register Format Definition.

$\overline{OE}_D$	D_0-D_7
L	DATA MULTIPLEXER OUTPUT, Y_0-Y_7
H	HIGH Z

Figure 2. Data Bus Output Enable Function.

BLOCK DIAGRAM



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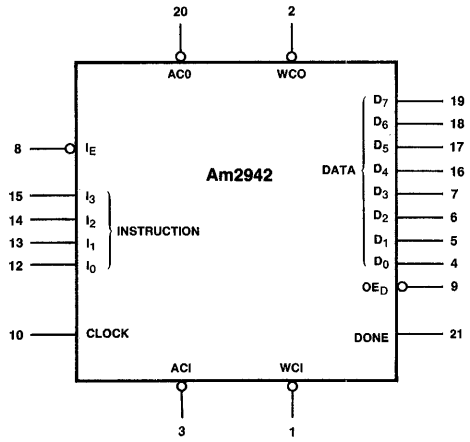
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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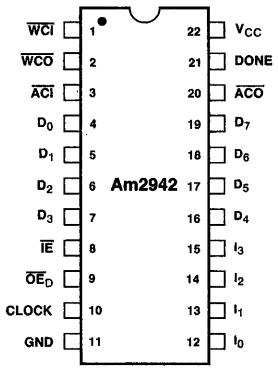
CONNECTION DIAGRAM
Top View

DIP



Note: Pin 1 is marked for orientation.

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Am2942 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. Figure 1 specifies when the DONE signal is generated in this mode.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2942 INSTRUCTIONS

The Am2942 instruction set consists of sixteen instructions. Eight are DMA Instructions and are similar to the Am2940 instructions. The remaining eight instructions are designed to facilitate the use of the Am2942 as a Programmable Timer/Counter. Figures 3 and 4 define the Am2942 Instructions.

Instructions 0-7 are DMA instructions. The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register to Data Multiplexer outputs Y_0-Y_2 Outputs Y_3-Y_7 are HIGH during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter to Data Multiplexer outputs, Y_0-Y_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter to Data Multiplexer outputs, Y_0-Y_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

$\overline{I_E}$	I_3	I_2	I_1	I_0	HEX CODE		
0	0	0	0	0	0	WRITE CONTROL REGISTER	DMA INSTRUCTIONS
0	0	0	0	1	1	READ CONTROL REGISTER	
0	0	0	1	0	2	READ WORD COUNTER	
0	0	0	1	1	3	READ ADDRESS COUNTER	
0	0	1	0	0	4	REINITIALIZE COUNTERS	
0	0	1	0	1	5	LOAD ADDRESS	
0	0	1	1	0	6	LOAD WORD COUNT	
0	0	1	1	1	7	ENABLE COUNTERS	
1	0	X	X	X	0-7	INSTRUCTION DISABLE	
0	1	0	0	0	8	WRITE CONTROL REGISTER, T/C	TIMER/COUNTER INSTRUCTIONS
0	1	0	0	1	9	REINITIALIZE ADDRESS COUNTER	
0	1	0	1	0	A	READ WORD COUNTER, T/C	
0	1	0	1	1	B	READ ADDRESS COUNTER, T/C	
0	1	1	0	0	C	REINITIALIZE ADDRESS & WORD COUNTERS	
0	1	1	0	1	D	LOAD ADDRESS, T/C	
0	1	1	1	0	E	LOAD WORD COUNT, T/C	
0	1	1	1	1	F	REINITIALIZE WORD COUNTER	
1	1	X	X	X	8-F	INSTRUCTION DISABLE, T/C	

0 = LOW 1 = HIGH X = DON'T CARE

Notes: 1. When I_3 is tied LOW, the Am2942 acts as a DMA circuit: When I_3 is tied HIGH, the Am2942 acts as a Timer/Counter circuit.
2. Am2942 instructions 0 through 7 are the same as Am2940 instructions.

Figure 3. Am2942 Instructions.

When $\overline{I_E}$ is HIGH, Instruction inputs, I_0-I_2, are disabled. If I_3 is LOW, the function performed is identical to that of the ENABLE COUNTERS instruction. Thus, counting can be controlled by the carry inputs with the ENABLE COUNTERS instruction applied or with Instruction Inputs I_0-I_2 disabled.

Instructions 8-F facilitate the use of the Am2942 as a Programmable Timer/Counter. They differ from instructions 0-7 in that they provide independent control of the Address Counter, Word Counter and Control Register.

The WRITE CONTROL REGISTER, T/C instruction writes DATA input D_0-D_2 into the Control Register. DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The Address and Word Counters are enabled, and the Control Register contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS COUNTER instruction allows the independent reinitialization of the Address Counter. The Word Counter is enabled and the contents of the Address Counter appear at the Data Multiplexer output.

The Word Counter can be read, using the READ WORD COUNTER, T/C instruction. Both counters are enabled when this instruction is executed.

When the READ ADDRESS COUNTER, T/C instruction is executed, both counters are enabled and the address counter contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS and WORD COUNTERS instruction provides the capability to reinitialize both counters at the same time. The Address Counter contents appear at the Data Multiplexer output.

DATA inputs D_0-D_7 are loaded into both the Address Register and Counter when the LOAD ADDRESS, T/C instruction is executed. The Word Counter is enabled and its contents appear at the Data Multiplexer output.

The LOAD WORD COUNT, T/C instruction is identical to the LOAD WORD COUNT instruction with the exception that Address Counter is enabled.

The Word Counter can be independently reinitialized using the REINITIALIZE WORD COUNTER instruction. The Address Counter is enabled and the Word Counter contents appear at the Data Multiplexer output.

When the $\overline{I_E}$ input is HIGH, Instruction inputs, I_0-I_2, are disabled. The function performed when I_3 is HIGH is identical to that performed when I_3 is LOW, with the exception that the Word Counter contents appear at the Data Multiplexer output.

$\overline{I_E}$	$I_3I_2I_1I_0$ (Hex)	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Adr. Reg.	Adr. Counter	Control Reg.	Data Multiplexer Output
L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	$D_{0\text{-}2} \rightarrow$ CR	FORCED HIGH
L	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CONTROL REG.
L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WORD COUNTER
L	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	ADR. COUNTER
L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D → AR	D → AC	HOLD	WORD COUNTER
L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D → WR	D → WC	HOLD	HOLD	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	FORCED HIGH
L	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
H	0-7	INSTRUCTION DISABLE	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
L	8	WRITE CONTROL REGISTER, T/C	WCRT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	$D_{0\text{-}2} \rightarrow$ CR	CONTROL REG.
L	9	REINITIALIZE ADR. COUNTER	REAC	0, 1, 2, 3	HOLD	ENABLE	HOLD	AR → AC	HOLD	ADR. COUNTER
L	A	READ WORD COUNTER, TC	RWCT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
L	B	READ ADDRESS COUNTER, T/C	RACT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. COUNTER
L	C	REINITIALIZE ADDRESS AND WORD COUNTERS	RAWC	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	D	LOAD ADDRESS, T/C	LDAT	0, 1, 2, 3	HOLD	ENABLE	D → AR	D → AC	HOLD	WORD COUNTER
L	E	LOAD WORD COUNT, T/C	LWCT	0, 2, 3	D → WR	D → WC	HOLD	ENABLE	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	ENABLE	HOLD	FORCED HIGH
L	F	REINITIALIZE WORD COUNTER	REWC	0, 2, 3	HOLD	WR → WC	HOLD	ENABLE	HOLD	WD. CNTR.
				1	HOLD	ZERO → WC	HOLD	ENABLE	HOLD	WD. CNTR.
H	8-F	INSTRUCTION DISABLE, T/C	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WD. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	WD. CNTR.

WR = WORD REGISTER
WC = WORD COUNTER
AR = ADDRESS REGISTER
AC = ADDRESS COUNTER
CR = CONTROL REGISTER
D = DATA

Figure 4. Am2942 Function Table.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

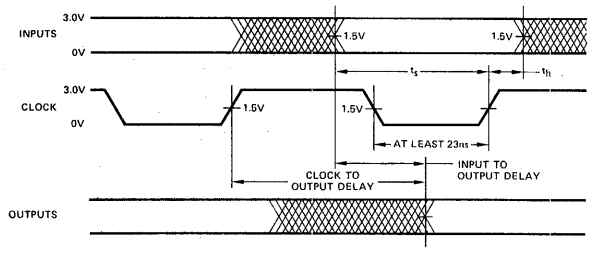
P/N	Range	Temperature	V_{CC}	
Am2942PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2942DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

2

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA	2.4			Volts
				COM'L I_{OH} = −2.6mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	WCO, ACO	MIL I_{OL} = 8.0mA			0.5	Volts
				COM'L I_{OL} = 12mA				
			D_{0-7}, DONE	MIL I_{OL} = 16mA				
				COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-7}				−0.15	mA
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-7}				150	μA
			All Others				40	
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_O = 5.5V					250	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	D_{0-7}			−150	μA
I_{OZH}			V_{OUT} = 2.4V	D_{0-7}			150	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		155	250	mA
			Am2942PC, DC	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			Am2942DM, FM	T_C = −55°C to +125°C			285	
				T_C = +125°C			205	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 5. Switching Waveforms.

MPR-728

SWITCHING CHARACTERISTICS

The tables below define the Am2942 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times (I to D) which are specified for a 5pF load. All times are in ns.

I. TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	13	3
I_{012}	33	2
$\overline{ACI}$	15	2
$\overline{WCI}$	15	1

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	12	–	–	–
$\overline{WCI}$ (Note 1)	–	12	27	–
I_{0-2}	–	–	–	21
CP (Note 2)	35	35	50	37

C. Clock Requirements

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	28	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	19	13	ns

II. GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	21	4
I_{012}	41	3
$\overline{ACI}$	27	3
$\overline{WCI}$	27	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	18	–	–	–
$\overline{WCI}$ (Note 1)	–	18	41	–
I_{0-2}	–	–	–	34
CP (Note 2)	50	50	77	53

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Maximum Clock Frequency	22	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	23	23	ns

III. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2942PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	6
I_{012}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–
$\overline{WCI}$ (Note 1)	–	20	46	–
I_{0-2}	–	–	–	37
CP (Note 2)	58	58	85	59

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	20	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	25	25	ns

IV. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2942DM, FM (T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	7
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–
$\overline{WCI}$ (Note 1)	–	21	54	–
I_{0-2}	–	–	–	41
CP (Note 2)	64	64	88	68

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	15	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	30	30	ns

Notes: 1. $\overline{WCI}$ to Done occurs only in control modes 0 and 1.
2. CP to Done occurs only in control modes 0, 1, and 2.

APPLICATIONS

Figure 6 shows an Am2942 used as two independent, programmable eight-bit timer/counters. In this example, an Am2910 Microprogram Sequencer provides an address to Am27S27 512 x 8 Registered PROMs. The on-chip PROM output register is used as the Microinstruction Register.

The Am2942 Instruction input, I_3, is tied HIGH to select the eight Timer/Counter instructions. The $\overline{I_E}$, I_0-I_2, and $\overline{OE_D}$ inputs are provided by the microinstruction, and the D_0-D_7 data lines are connected to a common Data Bus. GATE WC and GATE AC are separate enable controls for the respective Word Counter and Address Counter. The DONE, $\overline{ACO}$ and $\overline{WCO}$ output signals indicate that a pre-programmed time or count has been reached.

Figure 7 shows an Am2942 used as a single 16-bit programmable timer/counter. In this example, the Word Counter carry-out, $\overline{WCO}$, is connected to the Address Counter carry-in, $\overline{ACI}$, to form a single 16-bit counter which is enabled by the GATE signal.

Figure 8 shows two Am2942s cascaded to form a 32-bit programmable timer/counter. The two Word Counters form the low order 16 bits, and the two Address Counters form the high order bits. This allows the timer/counter to be loaded and read 16 bits at a time.

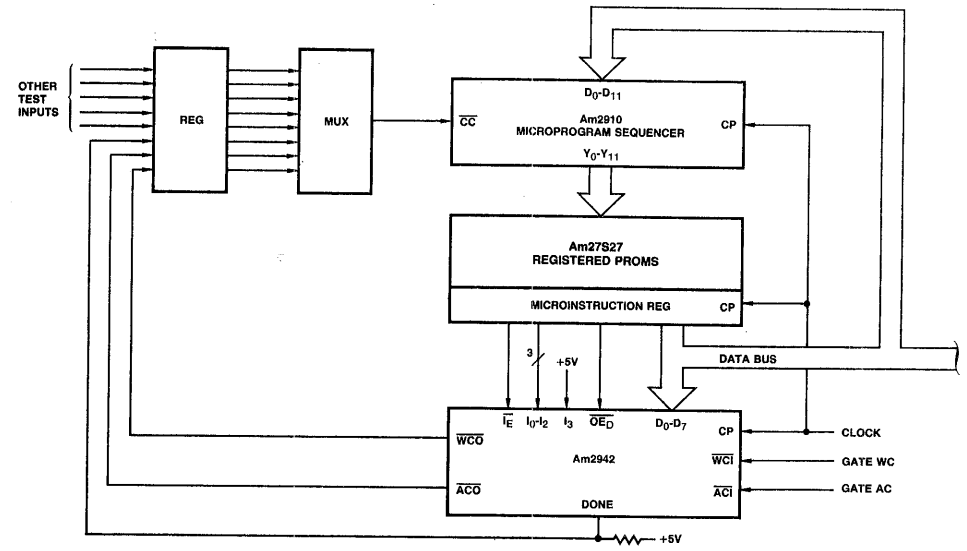


Figure 6. Two 8-Bit Programmable Counters/Timers in a 22-Pin Package.

MPR-234

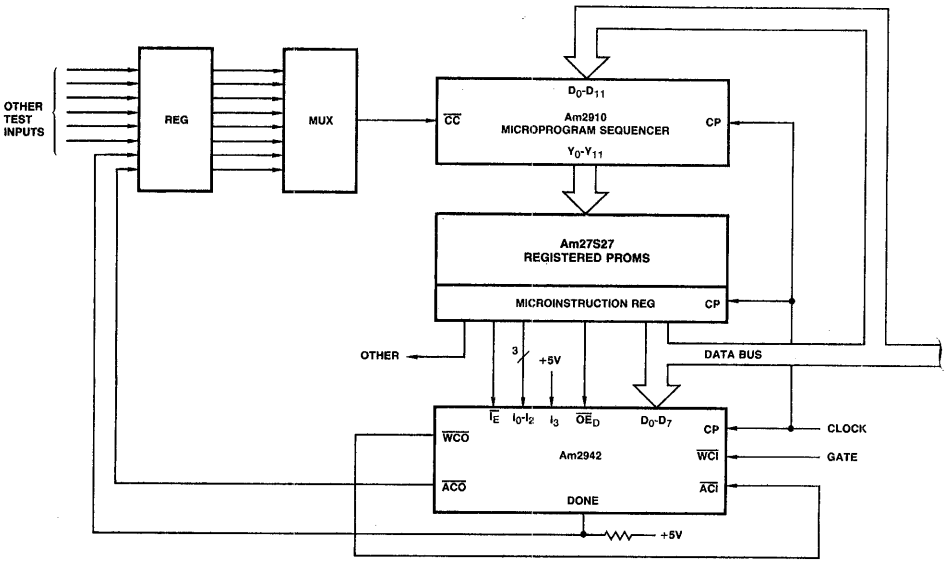


Figure 7. 16-Bit Programmable Counter/Timer Using a Single Am2942.

MPR-235

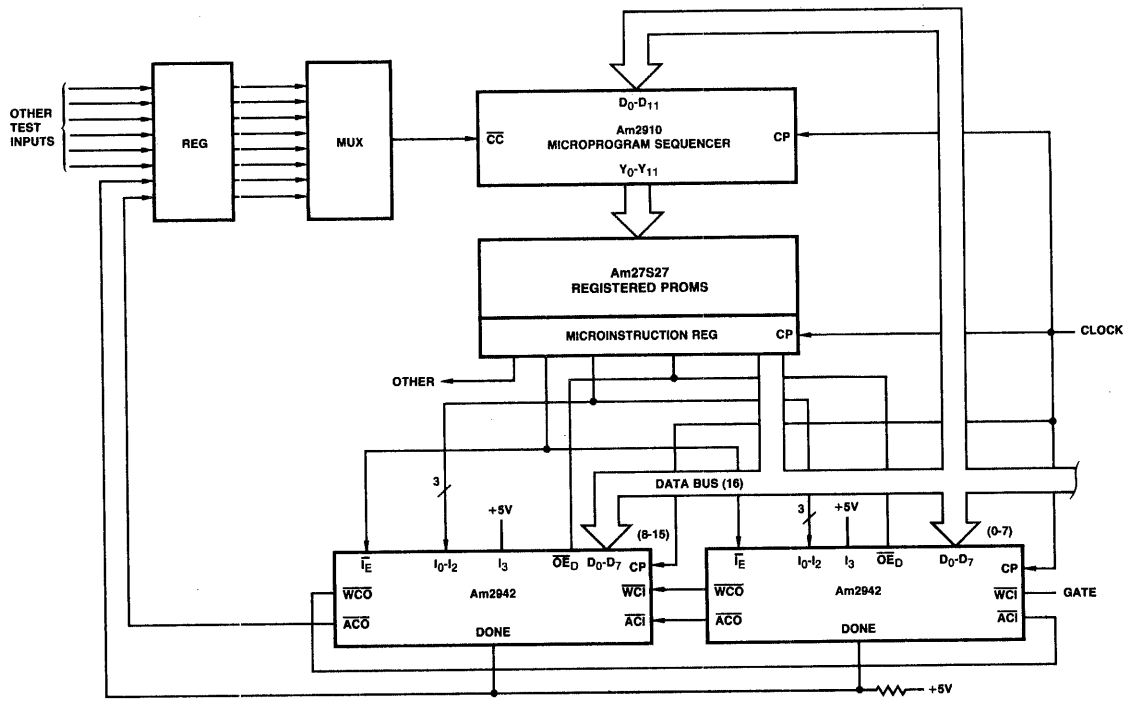


Figure 8. 32-Bit Programmable Counter/Timer Using Two Am2942s.

MPR-236

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2942PC	P-22	C	C-1
AM2942DC	D-22	C	C-1
AM2942DCTB	D-22	C	B-2 (Note 4)
AM2942DM	D-22	M	C-3
AM2942DM-B	D-22	M	B-3
AM2942FM	F-22	M	C-3
AM2942FM-B	F-22	M	B-3
AM2942XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2942XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2946 • Am2947

Octal 3-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- $V_{CC}-1.15V$ V_{OH} interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am2946 has inverting transceivers
- Am2947 has non-inverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

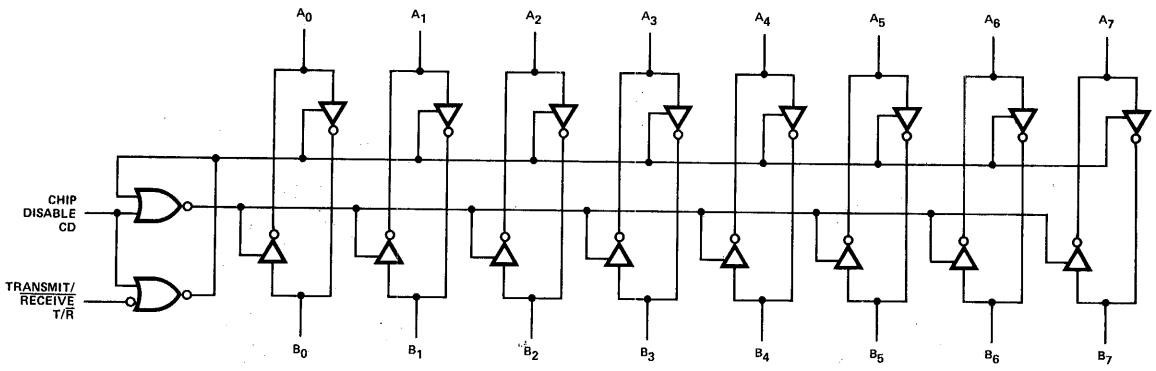
The Am2946 and Am2947 are 8-bit 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (V_{OH}) is specified at $V_{CC}-1.15V$ minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM or microprocessors.

LOGIC DIAGRAM

Am2946

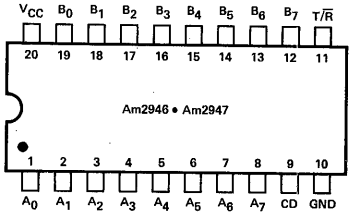


Am2947 has non-inverting transceivers.

BLI-101

CONNECTION DIAGRAM

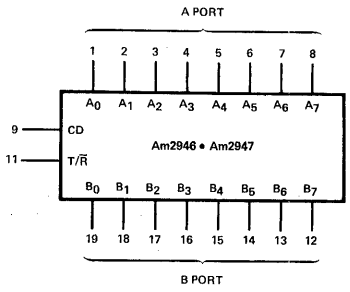
Top View



Note: Pin 1 is marked for orientation.

BLI-102

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

BLI-103

ORDERING INFORMATION

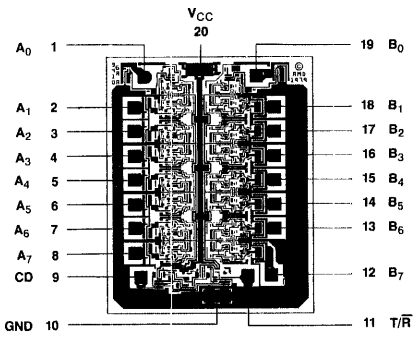
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2946 Order Number	Am2947 Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
AM2946PC	AM2947PC	P-20-1	C	C-1
AM2946DC	AM2947DC	D-20-1	C	C-1
AM2946DC-B	AM2947DC-B	D-20-1	C	B-1
AM2946DM	AM2947DM	D-20-1	M	C-3
AM2946DM-B	AM2947DM-B	D-20-1	M	B-3
AM2946XC	AM2947XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

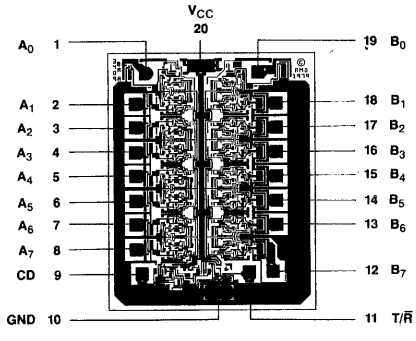
Metallization and Pad Layouts

Am2946



DIE SIZE 0.069" X 0.089"

Am2947



DIE SIZE 0.069" X 0.089"

Am2946 • Am2947
ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL T_A = −55 to +125°C V_{CC}MIN = 4.5V V_{CC}MAX = 5.5V
COM'L T_A = 0 to 70°C V_{CC}MIN = 4.75V V_{CC}MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description		Test Conditions		Min	Typ (Note 1)	Max	Units
			A PORT (A_0-A_7)					
V_{IH}	Logical "1" Input Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	COM'L			0.8	Volts
				MIL			0.7	
V_{OH}	Logical "1" Output Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = 0.8 V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
				I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = 0.8 V	I_{OL} = 12mA		0.3	0.4	Volts
				COM'L, I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current		CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage		CD = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage		CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		CD = 2.0V	V_O = 0.4V			−200	μA
				V_O = 4.0V			80	
			B PORT (B_0-B_7)					
V_{IH}	Logical "1" Input Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX		2.0			Volts
V_{IL}	Logical "0" Input Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX	COM'L			0.8	Volts
				MIL			0.7	
V_{OH}	Logical "1" Output Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
				I_{OH} = −5mA	2.7	3.9		
				I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
				I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current		CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current		CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage		CD = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current		CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage		CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		CD = 2.0V	V_O = 0.4V			−200	μA
				V_O = 4.0V			200	
			CONTROL INPUTS CD, T/$\overline{R}$					
V_{IH}	Logical "1" Input Voltage				2.0			Volts
V_{IL}	Logical "0" Input Voltage			COM'L			0.8	Volts
				MIL			0.7	
I_{IH}	Logical "1" Input Current		V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current		V_I = 0.4V	T/$\overline{R}$		−0.1	−.25	mA
				CD		−0.1	−.25	
V_C	Input Clamp Voltage		I_{IN} = −12mA			−0.8	−1.5	Volts
			POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current	Am2946	CD = V_I = 2.0V, V_{CC} = MAX			70	100	mA
			CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2V, V_{CC} = MAX			100	150	
		Am2947	CD = 2.0V, V_I = 0.4V, V_{CC} = MAX			70	100	
			CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = MAX			90	140	

Am2946

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF		20	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF		19	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		7	12	
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 4 45pF		9	14	
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		13	18	ns
t_{PHZB}	Propagation Delay from A Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF		25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF		16	25	
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF		22	35	ns
		S_3 = 0, R_5 = 5kΩ, C_4 = 45pF		14	25	
TRANSMIT/RECEIVE MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF		22	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF		26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF		27	35	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTIONAL TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

Am2947
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
tPDHLA	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD =0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF		27	35	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		11	18	
t_{PDLHB}	Propagation Delay to Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		11	18	
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF		32	40	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF		16	22	
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF		26	35	ns
		S_3 = 0, R_5 = 5kΩ, C_4 = 45pF		14	22	
TRANSMIT/RECEIVE MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 =5pF S_2 = 0, R_3 = 5k, C_2 = 30pF		28	40	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF		31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF		28	40	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

DEFINITION OF FUNCTIONAL TERMS

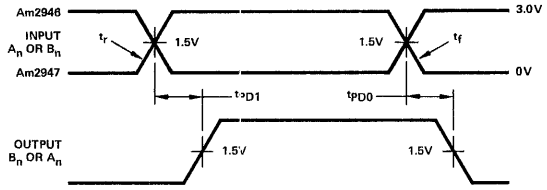
A_0-A_7 A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

B_0-B_7 B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

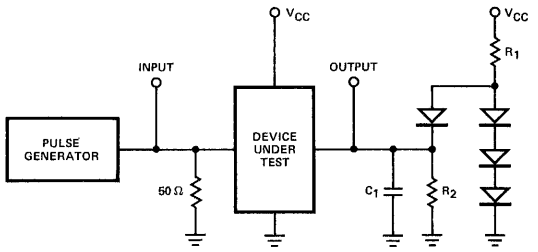
CD Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

T/$\overline{R}$ Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH, A port is the input and B port is the output. With T/$\overline{R}$ LOW, A port is the output and B port is the input.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



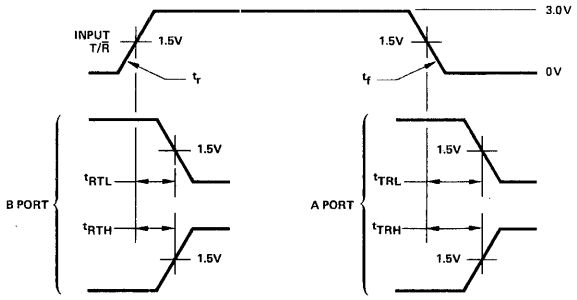
$t_r = t_f < 10ns$
10% to 90%



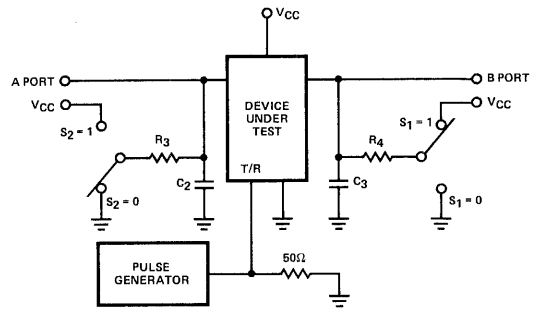
Note: C_1 includes test fixture capacitance.

Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.

BLI-104



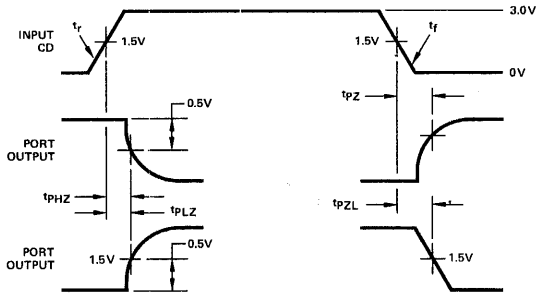
$t_r = t_f < 10ns$
10% to 90%



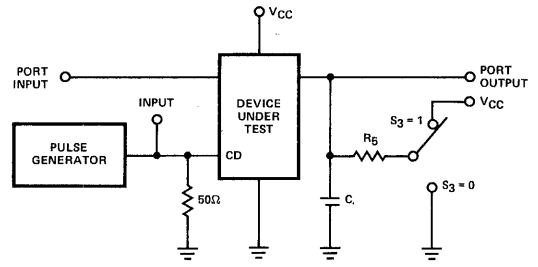
Note: C_2 and C_3 include test fixture capacitance.

Figure 2. Propagation Delay from T/R to A Port or B Port.

BLI-105



$t_r = t_f < 10ns$
10% to 90%



Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

Figure 3. Propagation Delay from CD to A Port or B Port.

BLI-106

Am2948 • Am2949

Octal 3-State Bidirectional Bus Transceivers

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am2948 has inverting transceivers
- Am2949 has non-inverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ enables
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

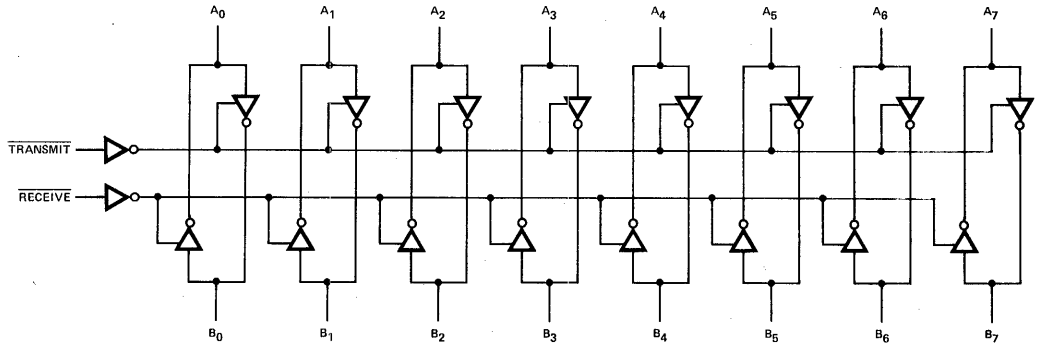
FUNCTIONAL DESCRIPTION

The Am2948 and Am2949 are 8-bit 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ enables are provided for microprocessor systems with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at $V_{CC}-1.15V$ minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM or microprocessors.

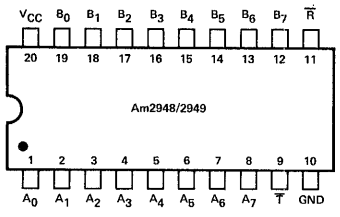
Am2949
LOGIC DIAGRAM



Am2948 has inverting transceivers.

BLI-107

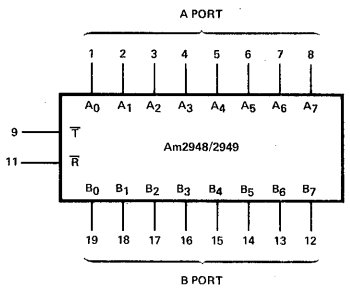
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-108

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

BLI-109

Am2950 • Am2951

Eight-Bit Bidirectional I/O Ports

DISTINCTIVE CHARACTERISTICS

- Eight-Bit, Bidirectional I/O Port with Handshake – Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- Register Full/Empty Flags – On-chip flag flip-flops provide data transfer handshaking signals.
- Separate Clock, Clock Enable and Three-State Output Enable for Each Register.
- Separate, Edge-Sensitive Clear Control for Each Flag Flip-Flop.
- Inverting and Non-Inverting Versions – The Am2950 provides non-inverting data outputs. The Am2951 provides inverting data outputs.
- 24mA Output Current Sink Capability.
- 100% Reliability Assurance Testing in Compliance with MIL-STD-883.

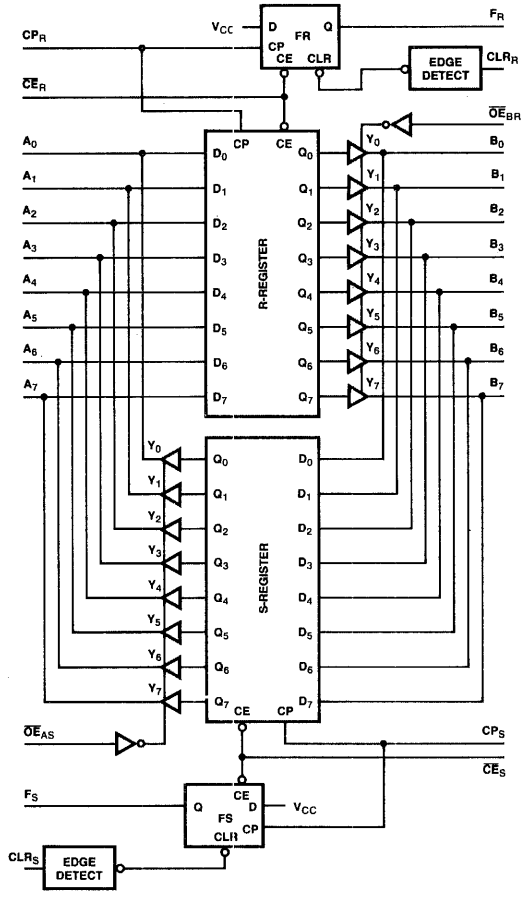
GENERAL DESCRIPTION

The Am2950 and Am2951, members of Advanced Micro Devices Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back to back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

Considerable flexibility is designed into the Am2950 • Am2951. Separate clock, clock enable and three-state output enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

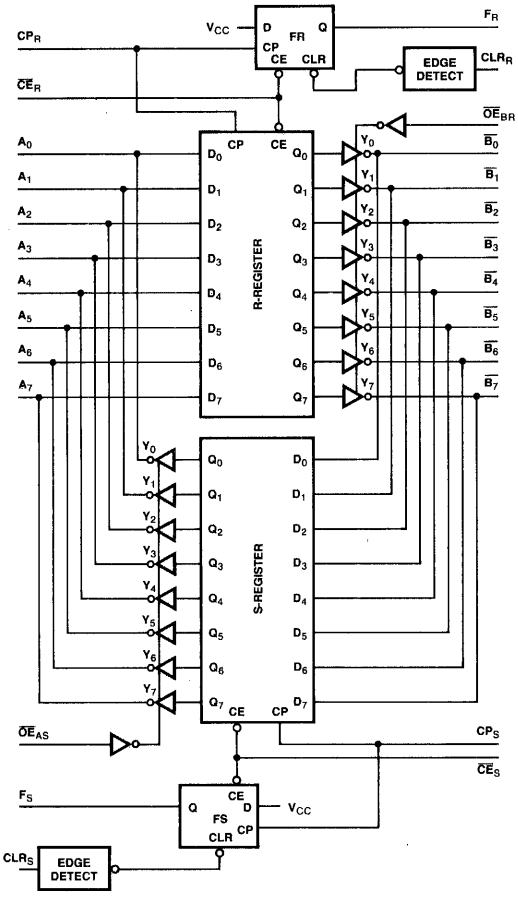
Twenty-four mA output current sink capability, sufficient for most three-state busses, is provided by the Am2950 • Am2951.

Am2950 BLOCK DIAGRAM



MPR-573

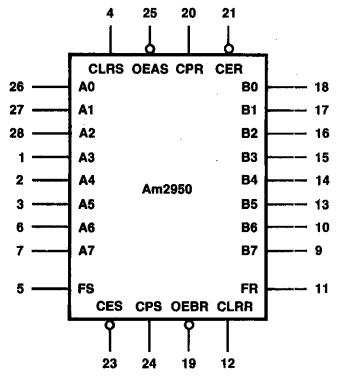
Am2951 BLOCK DIAGRAM



MPR-574

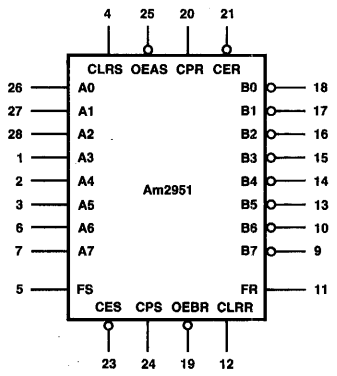
LOGIC SYMBOLS

Am2950



MPR-575

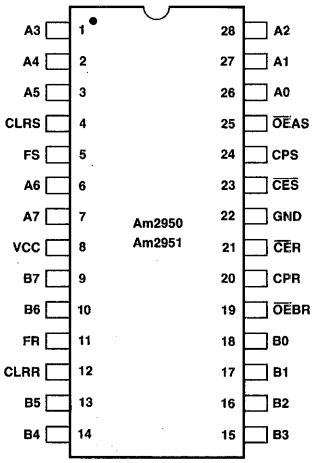
Am2951



MPR-576

CONNECTION DIAGRAMS
Top Views

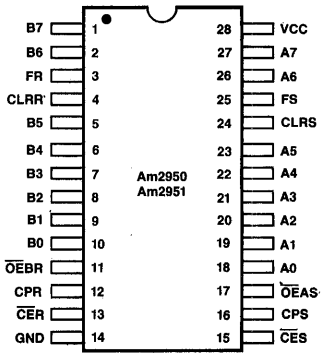
DIP



Note: Pin 1 is marked for orientation.
Bi is inverted on Am2951.

MPR-577

FLAT PACK



MPR-585

DEFINITION OF FUNCTIONAL TERMS

A0-7 Eight bidirectional lines carrying the R Register inputs or S Register outputs.

B0-7 Eight bidirectional lines carrying the S Register inputs or R Register outputs.

CPR The clock for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW to HIGH transition of the CPR signal.

$\overline{CER}$ The Clock Enable for the R Register and FR Flip-Flop. When $\overline{CER}$ is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW to HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, The R Register and FR Flip-Flop hold their contents, regardless of CPR signal transitions.

$\overline{OEBR}$ The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, The R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state.

FR The FR Flip-Flop output.

CLRR The clear control for the FR Flip-Flop. The FR Flip-Flop is cleared on the LOW to HIGH transition of CLRR signal.

CPS The clock for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW to HIGH transtion of the CPS signal.

$\overline{CES}$ The clock enable for the S Register and FS Flip-Flop. When $\overline{CES}$ is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW to HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register and FS Flip-Flop hold their contents, regardless of CPS signal transitions.

$\overline{OEAS}$ The output enable for the S Register. When $\overline{OEAS}$ is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When OEAS is HIGH, the S Register outputs are in the high-impedance state.

FS The FS Flip-Flop output.

CLRS The clear control for the FS Flip-Flop. The FS Flip-Flop is cleared on the LOW to HIGH transition of CLRS signal.

REGISTER FUNCTION TABLE
(Applies to R or S Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

	Internal	Y-Outputs		
$\overline{OE}$	Q	Am2950	Am2951	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

FLAG FLIP-FLOP FUNCTION TABLE
(Applies to R or S Flag Flip-Flop)

Inputs				
$\overline{CE}$	CP	CLR	F-Output	Function
H	X	↑̸	NC	Hold Flag
X	X	↑	L	Clear Flag
L	↑	↑̸	H	Set Flag

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance

NC = NO CHANGE
↑ = LOW-to-HIGH Transition
↑̸ = NO LOW-to-HIGH Transition

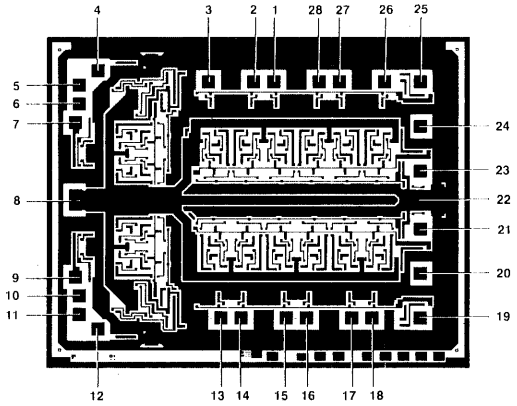
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2950 Order Number	Am2951 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2950PC	AM2951PC	P-28	C	C-1
AM2950DC	AM2951DC	D-28	C	C-1
AM2950DC-B	AM2951DC-B	D-28	C	B-2 (Note 4)
AM2950DM	AM2951DM	D-28	M	C-3
AM2950DM-B	AM2951DM-B	D-28	M	B-3
AM2950FM	AM2951FM	F-28-2	M	C-3
AM2950FM-B	AM2951FM-B	F-28-2	M	B-3
AM2950XC	AM2951XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2950XM	AM2951XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

METALLIZATION AND PAD LAYOUT



Numbers refer to DIP pin connection
DIE SIZE 0.107" X 0.138"

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +VCC max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

2

OPERATING RANGE

Part Number	Range	Temperature	VCC
Am2950/51PC, DC	COM'L	T_A = 0°C to +70°C	VCC = 5.0V ±5% (MIN. = 4.75V, MAX. =5.25V)
Am2950/51DM, FM	MIL	TC = −55°C to +125°C	VCC = 5.0V ±10% (MIN. = 4.50V, MAX. = 5.50V)

Am2950, Am2951
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
VOH	Output HIGH Voltage	VCC = MIN. VIN = VIH or VIL	FR, FS	IOH = −1mA	2.4	3.4		Volts
			A0-7, B0-7	MIL, IOH = −2mA	2.4	3.4		
				COM'L, IOH = −6.5mA	2.4	3.4		
VOL	Output LOW Voltage (Note 5)	VCC = MIN. VIN = VIH or VIL	FR, FS	IOL = 12mA			0.5	Volts
			A0-7, B0-7	MIL IOL = 16mA			0.5	
				COM'L IOL = 24mA			0.5	
VIH	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
VIL	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
VI	Input Clamp Voltage	VCC = MIN., IIN = −18mA					−1.5	Volts
IIL	Input LOW Current	VCC = MAX., VIN = 0.5V		A0-7, B0-7			−250	μA
				CLRR, CLRS			−2.0	mA
				Others			−360	μA
IIH	Input HIGH Current	VCC = MAX., VIN = 2.7V		A0-7, B0-7			70	μA
				CLRR, CLRS			100	
				Others			20	
II	Input HIGH Current	VCC = MAX., VIN = 5.5V					1.0	mA
IO	Output Off-state Leakage Current	VCC = MAX.	A0-7, B0-7	V0 = 2.4V			70	μA
				V0 = 0.4V			−250	
ISC	Output Short Circuit Current (Note 3)	VCC =MAX.			−30		−85	mA
ICC	Power Supply Current (Notes 4, 6)	VCC = MAX.		T_A = 25°C		156	263	mA
			COM'L	T_A = 0°C to +70°C			275	
				T_A = +70°C			228	
			MIL	T_C = −55°C to +125°C			309	
				T_C = +125°C			202	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at VCC = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. ICC is measured with all inputs at 4.5V and all outputs open.
5. The sum of IOL into Ai and Bi for each i must not exceed 32mA COM'L, 24mA MIL at a given point in time.
6. Worst case ICC is at minimum temperature.

SWITCHING CHARACTERISTICS

The tables below define the Am 2950 • Am2951 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagation delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, VCC = 5.0V)

A. Set-up and Hold Times (With respect to clock LOW-to-HIGH transition.)

Input	With Respect To	ts	th
A0-7	CPS ↑	2	0
B0-7	CPR ↑	2	0
$\overline{CE}$S	CPS ↑	9	0
$\overline{CE}$R	CPR ↑	9	0

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↑	15	–	13	–
CPR ↑	–	15	–	13
CLRS ↑	–	–	11	–
CLRR ↑	–	–	–	11

C. Recovery Times

From	To	tREC
CLRS ↑	CPS ↑	17
CLRR ↑	CPR ↑	17

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	15	15
CPR	15	15
CLRS	15	15
CLRR	15	15

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	15	16
$\overline{OE}$BR	B0-7	15	16

GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, VCC = 5.0V)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPS ↑		
B0-7	CPR ↑		
$\overline{CE}$S	CPS ↑		
$\overline{CE}$R	CPR ↑		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↑		–		–
CPR ↑	–		–	
CLRS ↑	–	–		–
CLRR ↑	–	–	–	

C. Recovery Times

From	To	tREC
CLRS ↑	CPS ↑	
CLRR ↑	CPR ↑	

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7		
$\overline{OE}$BR	B0-7		

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0°C to +70°C, VCC = 4.75 to 5.25V)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPS ↓	7	5
B0-7	CPR ↓	7	5
$\overline{CE}$S	CPS ↓	15	4
$\overline{CE}$R	CPR ↓	15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓	26	–	20	–
CPR ↓	–	26	–	20
CLRS ↓	–	–	22	–
CLRR ↓	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	31
CLRR ↓	CPR ↓	31

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	22	27
$\overline{OE}$BR	B0-7	22	27

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55°C to +125°C, VCC = 4.5 to 5.5V)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPS ↓	11	8
B0-7	CPR ↓	11	8
$\overline{CE}$S	CPS ↓	15	4
$\overline{CE}$R	CPR ↓	15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓	28	–	20	–
CPR ↓	–	28	–	20
CLRS ↓	–	–	22	–
CLRR ↓	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	34
CLRR ↓	CPR ↓	34

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	24	28
$\overline{OE}$BR	B0-7	24	28

APPLICATIONS

The Am2950 • Am2951 provides data transfer handshaking signals as well as eight-bit, bidirectional data storage. Its flexibility allows it to be used in any type of computer system, including Am2900, 8080, 8085, 8086, Z80, and Z8000 systems.

Figure 1 shows an Am2950 used to store data moving in both directions between a bidirectional system data bus and a bidirectional peripheral data bus. The on-chip Flag flip-flops provide the data in, data out handshaking signals required for data transfer and interrupt request generation.

Figure 2 shows a multiple I/O port system using Am2950's. Two Am2950's are used at each port to interface the 16-bit system data bus. The Am2950 flags are used to generate I/O interrupt requests.

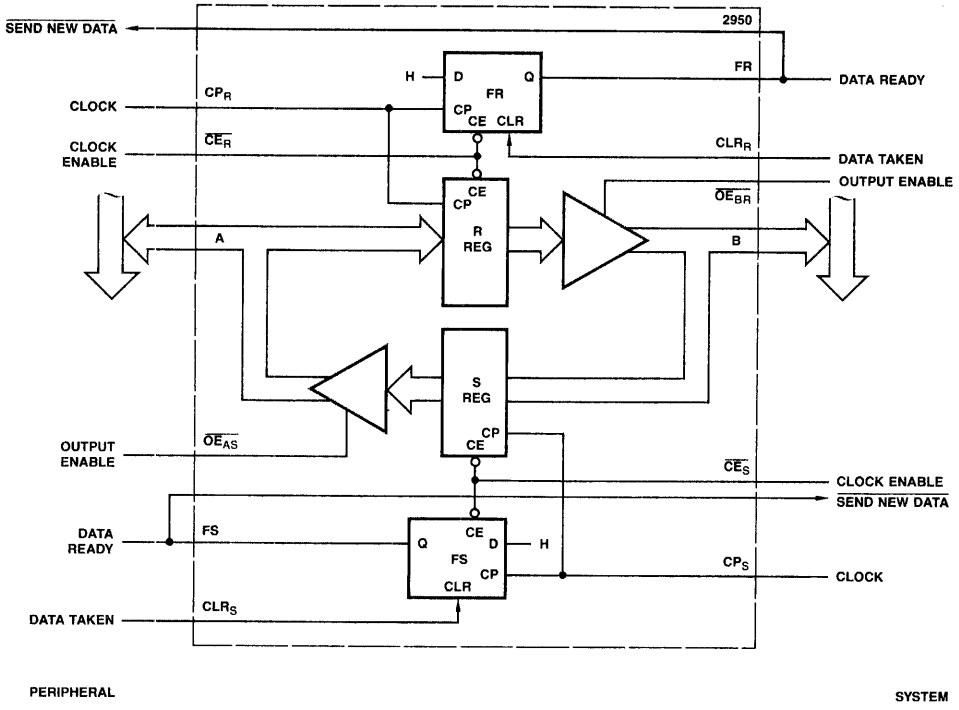


Figure 1. A Bidirectional I/O Port with Handshaking Using the Am2950.

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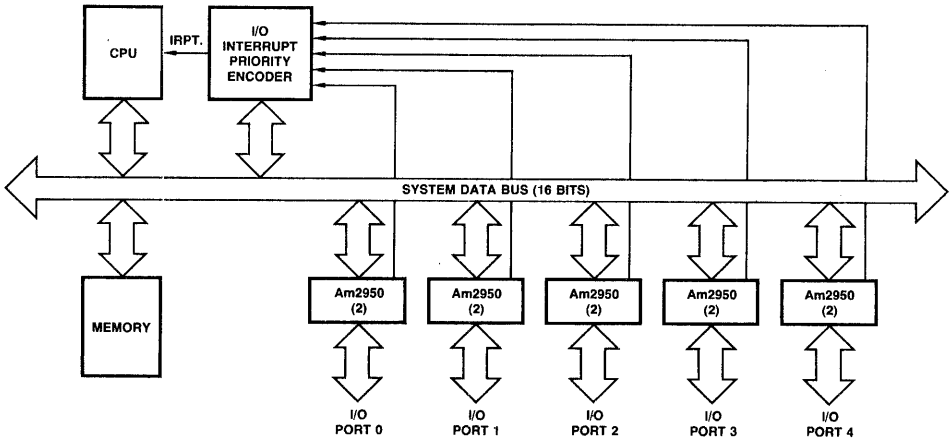


Figure 2. Multiple I/O Port System.

MPR-579

Am2954 • Am2955

Octal Registers with Three-State Outputs

2

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Am2954 has non-inverting inputs
- Am2955 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- High-speed – Clock to output 11ns typical
- 100% product assurance screening to MIL-STD-883 requirements

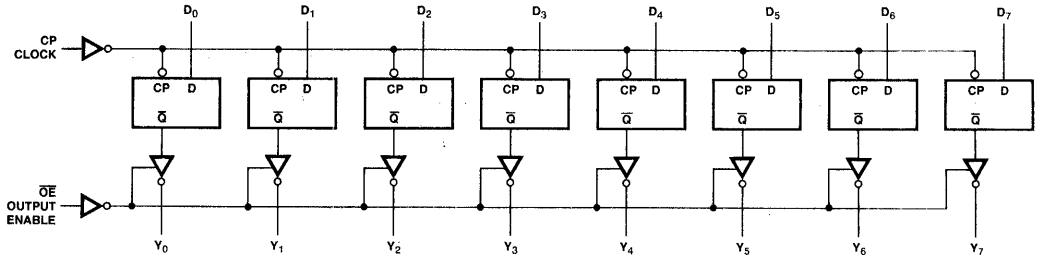
FUNCTIONAL DESCRIPTION

The Am2954 and Am2955 are 8-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the 3-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM
Am2954



Inputs D_0 through D_7 are inverted on the Am2955.

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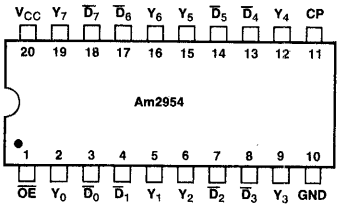
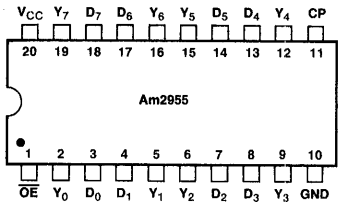
CONNECTION DIAGRAMS – Top Views

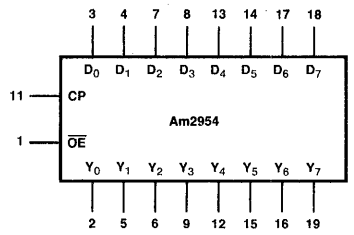


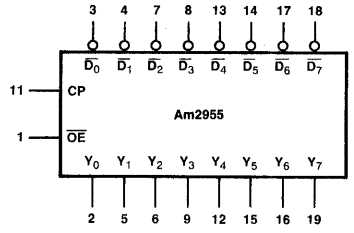


Note: Pin 1 is marked for orientation.

BLI-111

LOGIC SYMBOLS





V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2954XC, DC, PC	Am2955XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am2954XM, DM, FM	Am2955XM, DM, FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
			I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0,5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			90	140	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Am2954 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.
   Am2955 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0 5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2954 Order Number	Am2955 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2954PC	AM2955PC	P-20-1	C	C-1
AM2954DC	AM2955DC	D-20-1	C	C-1
AM2954DC-B	AM2955DC-B	D-20-1	C	B-1
AM2954DM	AM2955DM	D-20-1	M	C-3
AM2954DM-B	AM2955DM-B	D-20-1	M	B-3
AM2954FM	AM2955FM	F-20	M	C-3
AM2954FM-B	AM2955FM-B	F-20	M	B-3
AM2954XC	AM2955XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2954XM	AM2955XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs (Am2954, non-inverting).

$\overline{D_i}$ The D flip-flop data inputs (Am2955, inverting).

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Y_i The register three-state outputs (Am2954, non-inverting).

$\overline{OE}$ Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

FUNCTION TABLE

	Inputs				Internal	Outputs
Function	$\overline{OE}$	Clock	Am2954 D_i	Am2955 $\overline{D_i}$	Q_i	Y_i
Hi-Z	H	L	X	X	NC	Z
	H	H	X	X	NC	Z
LOAD REGISTER	L	↑	L	H	L	L
	L	↑	H	L	H	H
	H	↑	L	H	L	Z
	H	↑	H	L	H	Z

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

SWITCHING CHARACTERISTICS

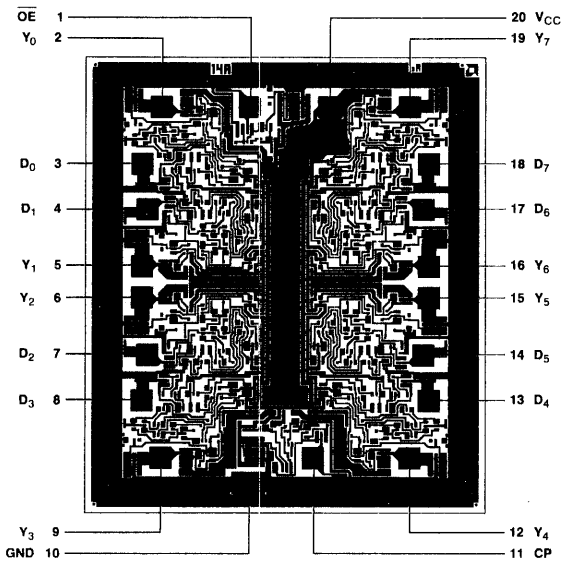
(T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description		Am2954 • Am2955 Min	Typ	Max	Units	Test Conditions
t_{PLH}	Clock to Output, Y_i			8	15	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}				11	17	ns	
t_{ZH}	$\overline{OE}$ to Y_i			8	15	ns	
t_{ZL}				11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i			5	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}				7	12	ns	
t_{PW}	Clock Pulse Width	HIGH	6			ns	C_L = 15pF, R_L = 280Ω
		LOW	7.3			ns	
t_S	Data to Clock		5			ns	
t_H			2			ns	
f_{max}	Maximum Clock Frequency (Note 1)		75	100		MHz	

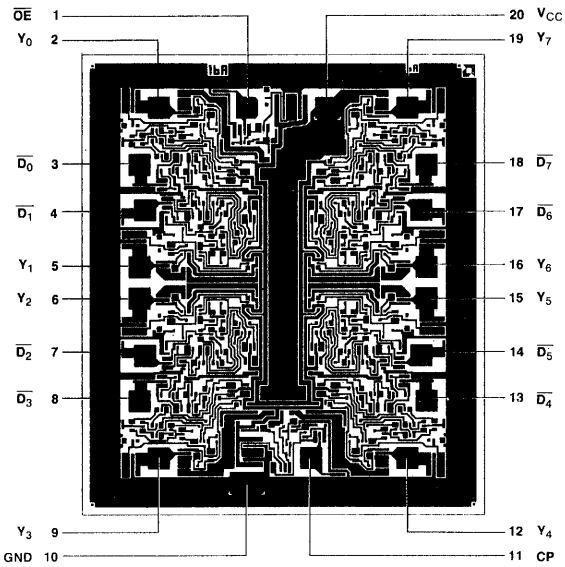
Note: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Metallization and Pad Layouts

Am2954

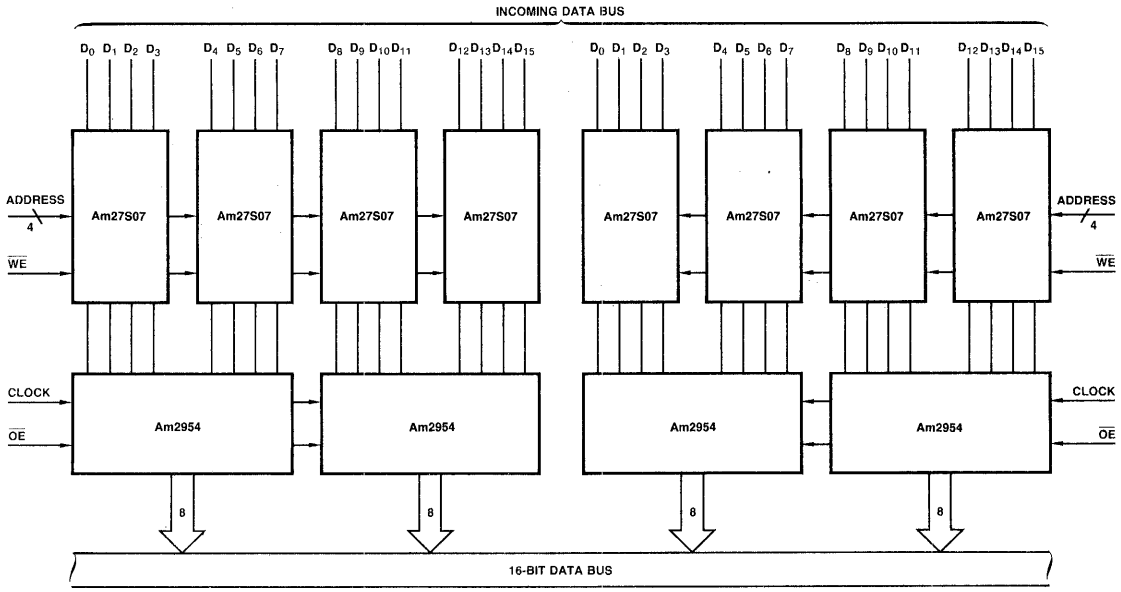


Am2955



DIE SIZE 0.096" X 0.083"

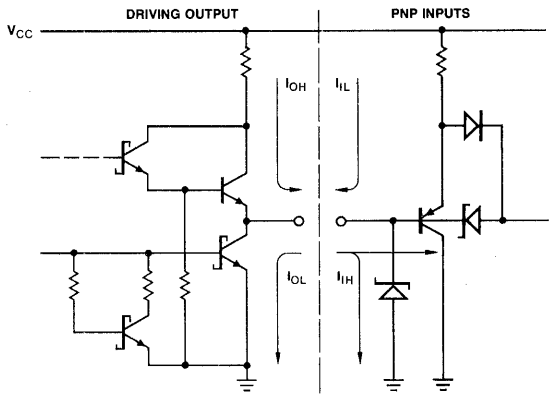
APPLICATION



Dual 16-word by 16-bit non-inverting high-speed data buffer.

BLI-113

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI- 14

Am2956 • Am2957

Octal Latches with Three-State Outputs

ADVANCED DATA

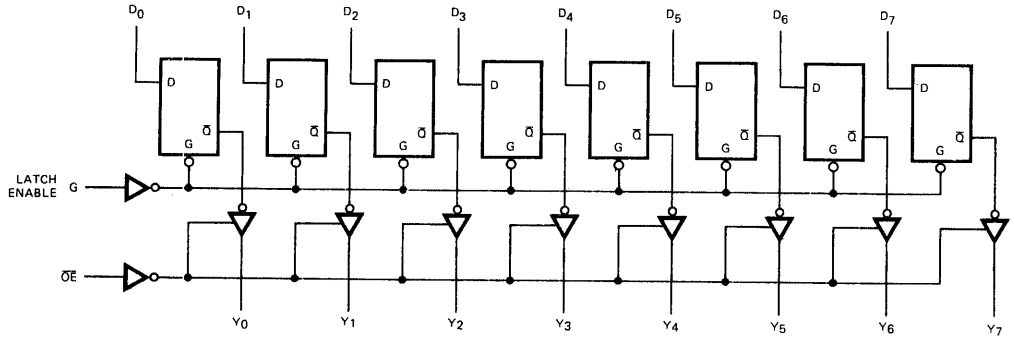
DISTINCTIVE CHARACTERISTICS

- 8 latches in a single package
- Am2956 has non-inverting outputs
- Am2957 has inverting outputs
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- High speed – Clock to output 12ns typical
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am2956 is an octal latch with 3-state outputs for bus organized system applications. The latching flip-flops appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, OE, is LOW. When OE is HIGH the bus output is in the high-impedance state.

LOGIC DIAGRAM
Am2956



Inputs D_0 through D_7 are inverted on the Am2957.

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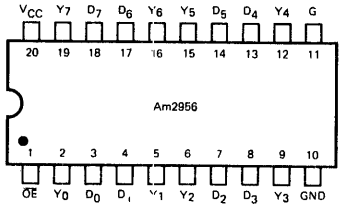
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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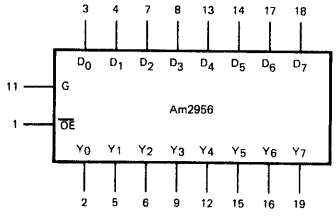
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-362

Am2958 • Am2959

Octal Buffers/Line Drivers/Line Receivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 65mA for commercial-range product; 48mA for military-range product
- Data-to-output propagation delay times:
  Inverting – 7.0ns MAX
  Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20-pin hermetic and molded DIP packages

FUNCTIONAL DESCRIPTION

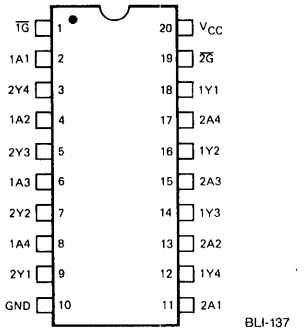
These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

The Am2958 and Am2959 have four buffers enabled from one common line, and the other four buffers enabled from another common line. The Am2958 is inverting, while the Am2959 presents true data at the outputs.

CONNECTION DIAGRAMS
Top Views

Am2958



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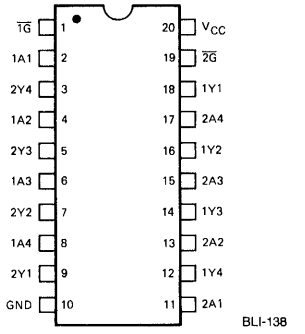
Am2959



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ORDERING INFORMATION

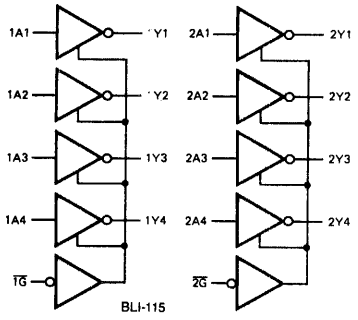
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2958 Order Number	Am2959 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2958PC	AM2959PC	P-20-1	C	C-1
AM2958DC	AM2959DC	D-20-1	C	C-1
AM2958DC-B	AM2959DC-B	D-20-1	C	B-1
AM2958DM	AM2959DM	D-20-1	M	C-3
AM2958DM-B	AM2959DM-B	D-20-1	M	B-3
Am2958XC	Am2959XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2958XM	Am2959XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883.

LOGIC DIAGRAMS

Am2958



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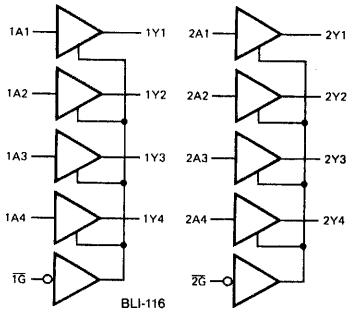
Am2959



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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am2958 (MIL) $T_A = -55°C$ to $+125°C$ V_{CC}(MIN.) = 4.50V V_{CC}(MAX.) = 5.50V
Am2959 (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC}(MIN.) = 4.75V V_{CC}(MAX.) = 5.25V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

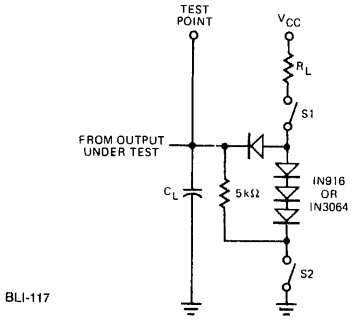
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{IH}	High-Level Input Voltage				2.0			Volts
V_{IL}	Low-Level Input Voltage						0.8	Volts
V_{IK}	Input Clamp Voltage	V_{CC} = MIN., I_I = −18mA					−1.2	Volts
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN.			0.2	0.4		Volts
V_{OH}	High-Level Output Voltage	V_{CC} = MIN., V_{IL} = 0.8V	COM'L, I_{OH} = −1mA		2.7			Volts
			I_{OH} = −3mA		2.4	3.4		
		V_{CC} = MIN., V_{IL} = 0.5V	MIL, I_{OH} = −12mA		2.0			
			COM'L, I_{OH} = −15mA		2.0			
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN., V_{IL} = 0.8V	MIL, I_{OL} = 48mA				0.55	Volts
			COM'L, I_{OL} = 64mA				0.55	
I_{OZH}	Off-State Output Current, High-Level Voltage Applied	V_{CC} = MAX., V_{IH} = 2.0V, V_{IL} = 0.8V	V_O = 2.4V				50	µA
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied		V_O = 0.5V				−50	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	High-Level Input Current, Any Input	V_{CC} = MAX., V_{IH} = 2.7V					50	µA
I_{IL}	Low-Level Input Current	Any A	V_{CC} = MAX., V_{IL} = 0.5V				−400	µA
		Any G					−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)	V_{CC} = MAX.			−50		−225	mA
I_{CC}	Supply Current	Am2958, All Outputs HIGH	V_{CC} = MAX., Outputs open	MIL		80	123	mA
				COM'L		80	135	
		Am2958, All Outputs LOW		MIL		100	145	
				COM'L		100	150	
		Am2958, Outputs at Hi-Z		MIL		100	145	
				COM'L		100	150	
		Am2959, All Outputs HIGH		MIL		95	147	
				COM'L		95	160	
		Am2959, All Outputs LOW		MIL		120	170	
				COM'L		120	180	
		Am2959, Outputs at Hi-Z		MIL		120	170	
				COM'L		120	180	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25° C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

Parameter	Description	Test Conditions	Am2958 Min.	Am2958 Typ.	Am2958 Max.	Am2959 Min.	Am2959 Typ.	Am2959 Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0pF, R_L = 90Ω (Note 3)		10	15		10	15	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



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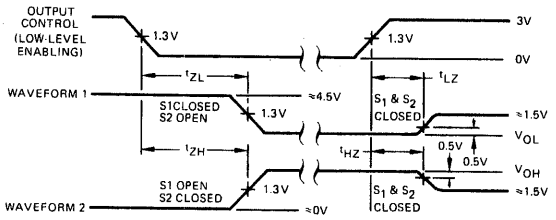
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



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Notes:
1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

FUNCTION TABLES

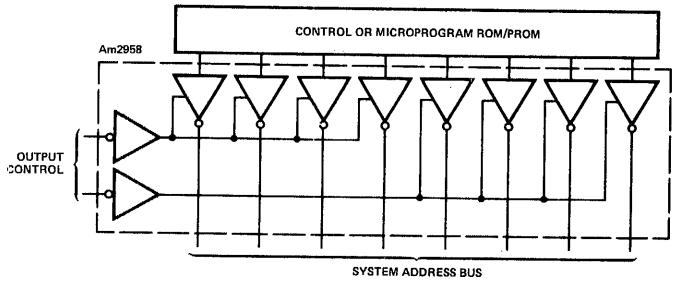
Am2958

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2959

INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

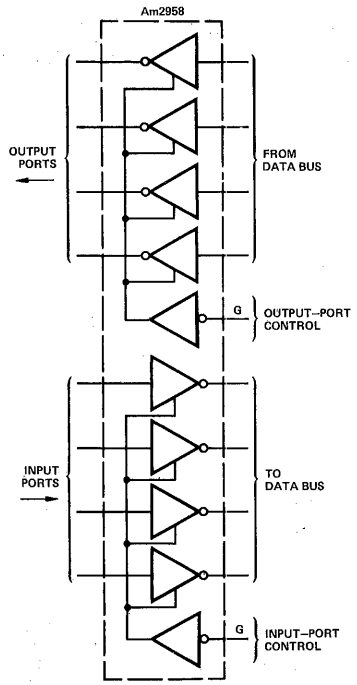
Am2958 USED AS SYSTEM BUS DRIVER – 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



BLI-119

APPLICATIONS (Cont.)

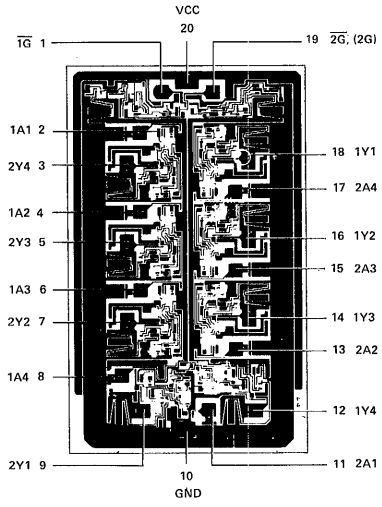
INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



BLI-120

Metallization and Pad Layout

Am2958 • Am2959



DIE SIZE 0.077" X 0.124"

Am2960
Fast Error Detection and Correction for Memories

Corrects All Single-Bit Errors

Corrects all single bit errors. Detects all double and some triple bit errors.

Expandable

One Am2960 provides Error Detection and Correction for 16-bits. Two Am2960s handle 32 bits; four Am2960s handle 64 bits.

Fast

Design objective of 30ns typical to detect errors, and 50ns to correct for 16-bits.

Flexible

Can be used with Am2900-based designs, the AmZ8000 or other CPUs.

Diagnostics Built-In

Logic on-chip for device test and software-controlled diagnostics.

Allows for Increased Memory Reliability

And can significantly reduce field servicing costs.

Am2960

Cascadable 16-Bit Error Detection and Correction Unit

ADVANCED DATA

DISTINCTIVE CHARACTERISTICS

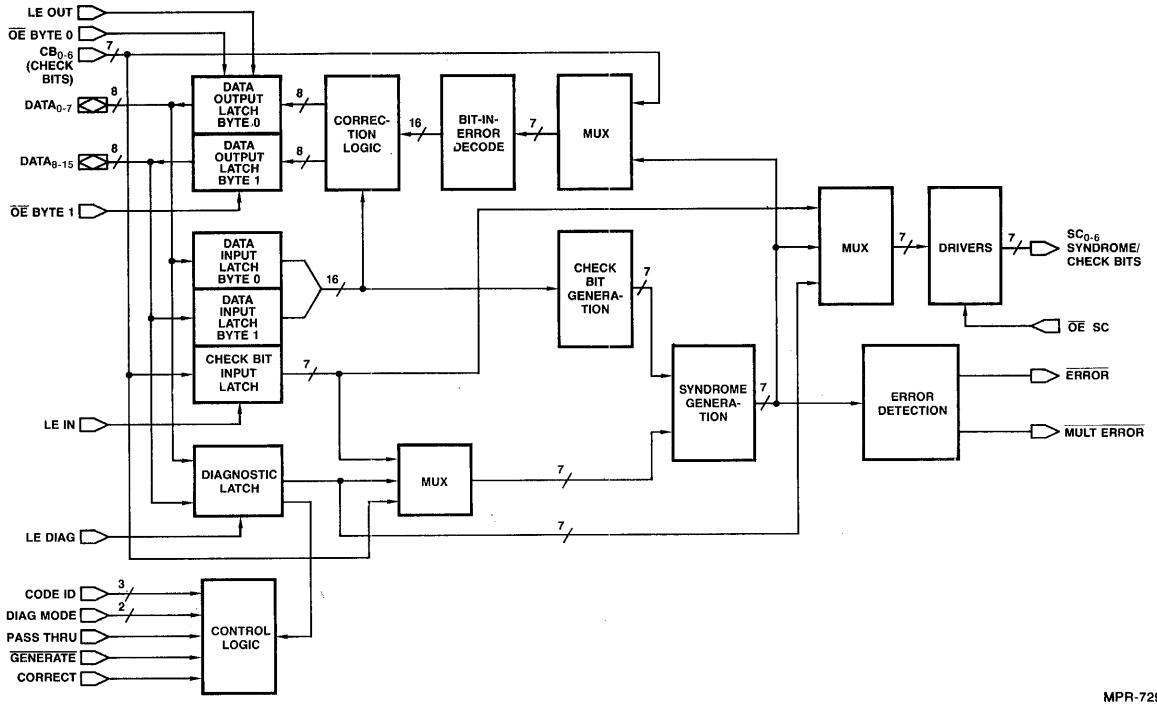
- Modified Hamming Code
  Detects multiple errors and corrects single bit errors in a parallel data word. Ideal for use in dynamic memory systems.
- Expandable
  One Am2960 provides EDC on 16-bit data words.
  Two Am2960s provide EDC on 32-bit data words.
  Four Am2960s provide EDC on 64-bit data words.
- Syndromes provided.
  The Am2960 makes available the syndrome bits when an error occurs, so the location of memory faults can be logged.
- Microprocessor compatible
  The Am2960 is designed to work with Z8000 microprocessor systems as well as high performance 2900 designs.
- Advanced circuit and process technologies
  Newest 2900 LSI techniques provide very high performance.
  Data-in to error detection typically 30ns
  Data-in to correct data out typically 50ns
- Built-in Diagnostics
  Extra logic on the chip provides diagnostic functions to be used during device test and for system diagnostics.

GENERAL DESCRIPTION

The Am2960 Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am2960 will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

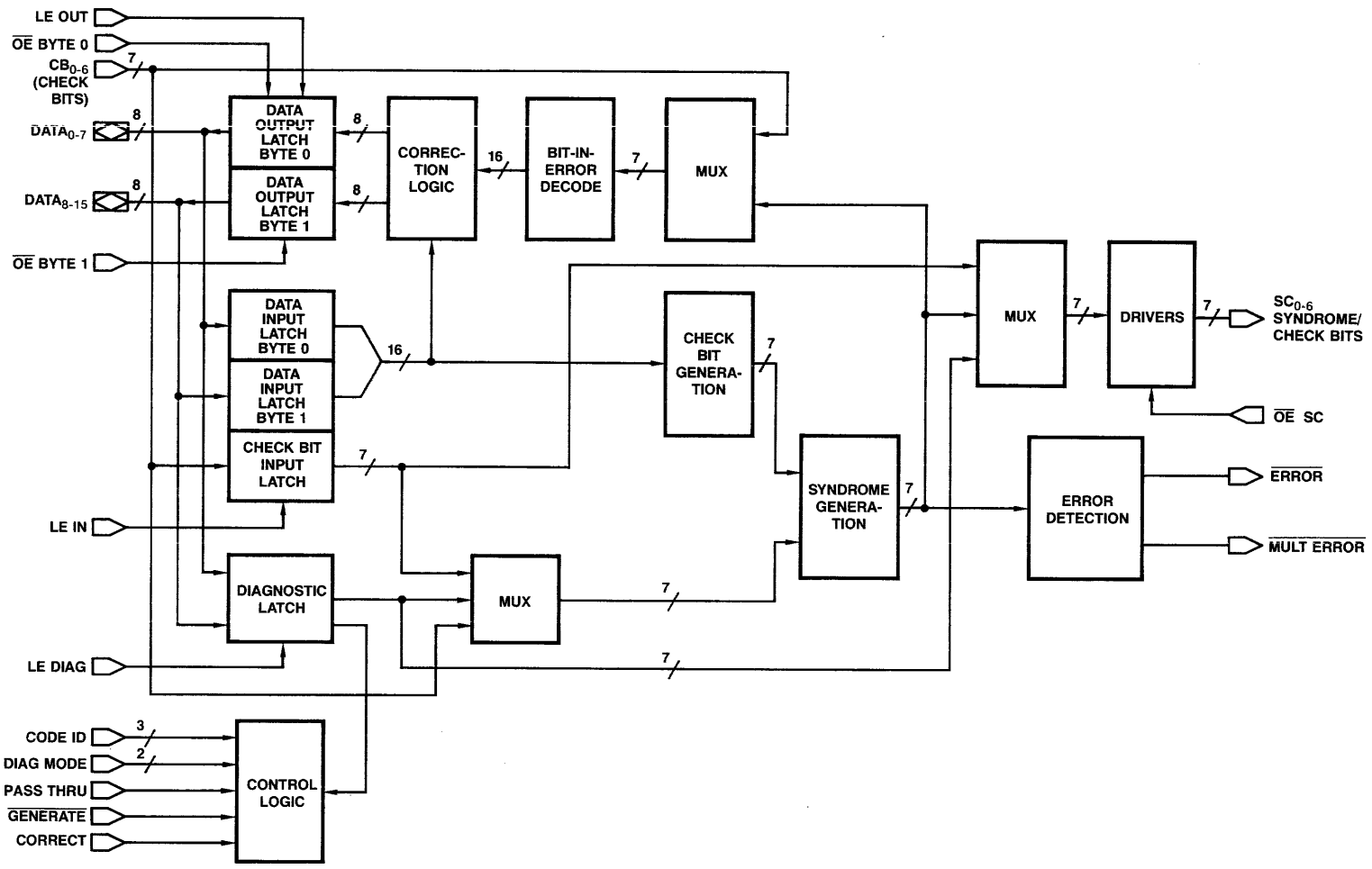
The Am2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

BLOCK DIAGRAM



MPR-729

BLOCK DIAGRAM



MPR-729

EDC Architecture

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

Check Bit Generation Logic

This block generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULTI ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULTI ERROR}}$ go LOW.

Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

PIN DEFINITIONS

$DATA_{0-15}$ 16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

CB_{0-6} Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

$\overline{\text{GENERATE}}$ Generate Check Bits input. When this input is LOW the EDC is in the Check Bit Generate Mode. When HIGH the EDC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC_{0-6} Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

$\overline{\text{OE SC}}$ Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.

$\overline{\text{ERROR}}$ Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

$\overline{\text{MULTI ERROR}}$ Multiple Errors Detected output. When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate Mode, $\overline{\text{MULTI ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULTI ERROR}}$ must be externally implemented.)

CORRECT Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

LE OUT Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.

$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1 Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

DIAG $MODE_{0-1}$ Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.

CODE ID_{0-2} Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG Latch Enable – Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

FUNCTIONAL DESCRIPTION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. The Am2960 may be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE ID_{0-2}, as shown in Table I. The three modified Hamming codes referred to in Table I are:

- 16/22 code – 16 data bits
  – 6 check bits
  – 22 bits in total.
- 32/39 code – 32 data bits
  – 7 check bits
  – 39 bits in total.
- 64/72 code – 64 data bits
  – 8 check bits
  – 72 bits in total.

CODE ID input 001 (ID_2, ID_1, ID_0) is a special code used to operate the device in Internal Control Mode (described later in this section).

TABLE I. HAMMING CODE AND SLICE IDENTIFICATION.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

Control Mode Selection

The device control lines are $\overline{\text{GENERATE}}$, CORRECT , PASS THRU, DIAG $MODE_{0-1}$ and CODE ID_{0-2}. Table II indicates the control modes selected by various combinations of the control line inputs.

Diagnostics

Table III shows specifically how DIAG $MODE_{0-1}$ select between normal operation, initialization and one of two diagnostic modes.

The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

Check and Syndrome Bit Labeling

The check bits generated in the EDC are designated as follows:

- 16-bit configuration – CX C0, C1, C2, C4, C8;
- 32-bit configuration – CX, C0, C1, C2, C4, C8, C16;
- 64-bit configuration – CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits and 8 syndrome bits in the 64-bit configuration.

FUNCTIONAL DESCRIPTION – 16-BIT DATA WORD CONFIGURATION

The 16-bit format consists of 16 data bits, 6 check bits and is referred to as 16/22 code (see Figure 1).

The 16-bit configuration is shown in Figure 2.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC_{0-5} (SC_6 is unspecified for 16-bit operation).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table IV. Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR is an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULTI ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs SC_{0-5} are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table V gives the chart for decoding the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001 this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

Pass Thru Mode

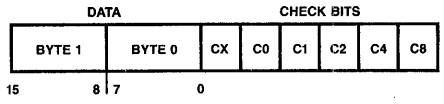
In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC_{0-5}.

TABLE II. EDC CONTROL MODE SELECTION.

$\overline{\text{GENERATE}}$	CORRECT	PASS THRU	DIAG $\text{MODE}_{0\text{-}1}$ (DM_1, DM_0)	CODE $\text{ID}_{0\text{-}2}$ (ID_2, ID_1, ID_0)	Control Mode Selected
LOW	LOW	LOW	00	Not 001	Generate
LOW	LOW	LOW	01	Not 001	Generate Using Diagnostic Latch
LOW	LOW	LOW	10	Not 001	Generate
LOW	LOW	LOW	11	Not 001	Initialize
LOW	LOW	HIGH	00	Not 001	Pass Thru
LOW	LOW	HIGH	01	Not 001	Pass Thru
LOW	LOW	HIGH	10	Not 001	Pass Thru
LOW	LOW	HIGH	11	Not 001	Undefined
LOW	HIGH	LOW	00	Not 001	Generate
LOW	HIGH	LOW	01	Not 001	Generate Using Diagnostic Latch
LOW	HIGH	LOW	10	Not 001	Generate
LOW	HIGH	LOW	11	Not 001	Initialize
LOW	HIGH	HIGH	00	Not 001	Pass Thru
LOW	HIGH	HIGH	01	Not 001	Pass Thru
LOW	HIGH	HIGH	10	Not 001	Pass Thru
LOW	HIGH	HIGH	11	Not 001	Undefined
HIGH	LOW	LOW	00	Not 001	Detect
HIGH	LOW	LOW	01	Not 001	Detect
HIGH	LOW	LOW	10	Not 001	Detect Using Diagnostic Latch
HIGH	LOW	LOW	11	Not 001	Initialize
HIGH	LOW	HIGH	00	Not 001	Pass Thru
HIGH	LOW	HIGH	01	Not 001	Pass Thru
HIGH	LOW	HIGH	10	Not 001	Pass Thru
HIGH	LOW	HIGH	11	Not 001	Undefined
HIGH	HIGH	LOW	00	Not 001	Correct
HIGH	HIGH	LOW	01	Not 001	Correct
HIGH	HIGH	LOW	10	Not 001	Correct Using Diagnostic Latch
HIGH	HIGH	LOW	11	Not 001	Initialize
HIGH	HIGH	HIGH	00	Not 001	Pass Thru
HIGH	HIGH	HIGH	01	Not 001	Pass Thru
HIGH	HIGH	HIGH	10	Not 001	Pass Thru
HIGH	HIGH	HIGH	11	Not 001	Undefined
Any	Any	Any	Any	001	Internal Control Using Diagnostic Latch

TABLE III. DIAGNOSTIC MODE CONTROL.

DIAG MODE_1	DIAG MODE_0	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Mode A.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Mode B.** In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	**Initialize.** The inputs of the Data Output Latch are forced to zeroes and the check bits generated correspond to the all-zero data.



Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

Figure 1. 16 Bit Data Format.

MPR-730

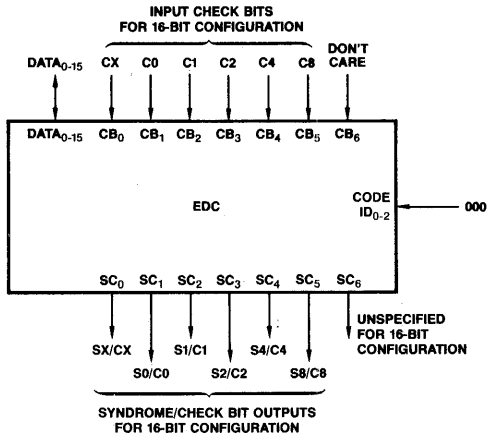


Figure 2. 16 Bit Configuration.

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TABLE IV. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

TABLE V. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits SX	S0	S1	S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

* – no errors detected
Number – the location of the single bit-in-error
T – two errors detected
M – three or more errors detected

TABLE VI. DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table VI shows the loading definitions for the DATA lines.

Generate Using Diagnostic Latch (Diagnostic Mode A)

Detect Using Diagnostic Latch (Diagnostic Mode B)

Correct Using Diagnostic Latch (Diagnostic Mode B)

These are special diagnostic modes selected by DIAG $MODE_{0-1}$ where either normal check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch. See Table III for details.

Internal Control Mode

This mode is selected by CODE ID_{0-2} input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode, the EDC takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table VI gives the format for loading the Diagnostic Latch.

FUNCTIONAL DESCRIPTION – 32-BIT DATA WORD CONFIGURATION

The 32-bit format consists of 32 data bits, 7 check bits and is referred to as 32/39 code (see Figure 3).

The 32-bit configuration is shown in Figure 4.

The upper EDC (Slice 0/1) handles the least significant bytes 0 and 1 – the external DATA lines 0 to 15 are connected to the same numbered inputs of the upper device. The lower EDC (Slice 2/3) handles the most significant bytes 2 and 3 – the external DATA lines for bits 16 to 31 are connected to inputs $DATA_0$ through $DATA_{15}$ respectively.

The valid syndrome and check bit outputs are those of Slice 2/3 as shown in the diagram. In Correct Mode these must be read into Slice 0/1 via the CB inputs, thus requiring external buffering and output enabling of the check bit lines as shown. The $\overline{OE}$ SC signal can be used to control enabling of check bit inputs – when syndrome outputs are enabled, the external check bit inputs will be disabled.

The valid $\overline{ERROR}$ and $\overline{MULTI\ ERROR}$ outputs are those of the Slice 2/3. The $\overline{ERROR}$ and $\overline{MULTI\ ERROR}$ outputs of Slice 0/1 are unspecified. All of the latch enables and control signals must be input to both of the devices.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC_{0-6} of Slice 2/3.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table VII. Check bits are generated as either an XOR or XNOR of 16 of the 32 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If two or more errors are detected, $\overline{MULTI\ ERROR}$ goes LOW. Both error indicators are HIGH if there are no errors. The valid ERROR and MULTI ERROR signals are those of Slice 2/3 – those of Slice 0/1 are undefined.

Also available on Slice 2/3 outputs SC_{0-6} are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table VIII gives the chart for decoding the syndrome bits generated for the 32-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16 were 0010011 this would be decoded to indicate that there is a single-bit error at data bit 25). If no error is detected the syndrome bits will be all zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction – if desired this would be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

For data correction, both Slices 0/1 and 2/3 require access to the syndrome bits on Slice 2/3's outputs SC_{0-6}. Slice 2/3 has access to these syndrome bits through internal data paths, but for Slice 0/1 they must be read through the inputs CB_{0-6}. The device connections for this are shown in Figure 4. When in Correct Mode the SC outputs must be enabled so that they are available for reading in through the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC_{0-6} of Slice 2/3.

Uses Modified Hamming Code 32/39
- 32 data bits
- 7 check bits
- 39 bits in total

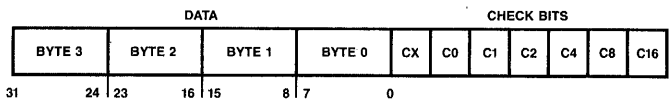

Figure 3. 32 Bit Data Format.

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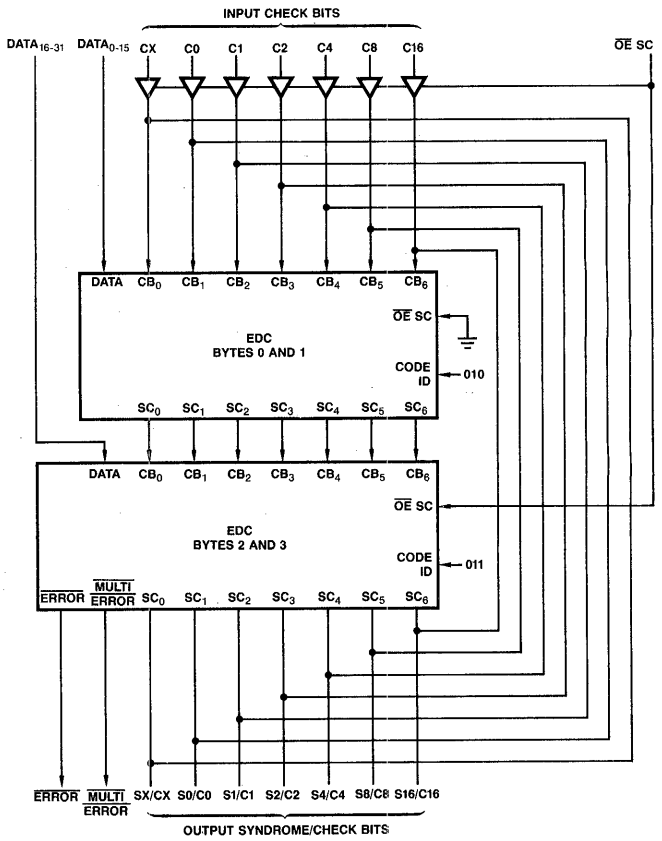

Figure 4. 32 Bit Configuration.

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TABLE VII. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

TABLE VIII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* – no errors detected
Numbers – number of the single bit-in-error
T – two errors detected
M – three or more errors detected

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table IX shows the loading definitions for the DATA lines.

Generate Using Diagnostic Latch (Diagnostic Mode A)

Detect Using Diagnostic Latch (Diagnostic Mode B)

Correct Using Diagnostic Latch (Diagnostic Mode B)

These are special diagnostic modes selected by DIAG $MODE_{0-1}$ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch. See Table III for details.

Internal Control Mode

This mode is selected by CODE ID_{0-2}, input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode the device takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines.

Table IX gives the format for loading the Diagnostic Latch.

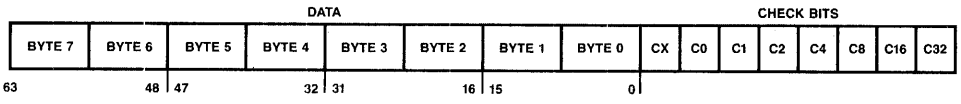
FUNCTIONAL DESCRIPTION – 64-BIT DATA WORD CONFIGURATION

The 64-bit format consists of 64 data bits, 8 check bits and is referred to as 64/72 code (see Figure 5).

The configuration to process 64-bit format is shown in Figure 6. In this configuration a portion of the syndrome generation and error detection is implemented externally of the EDCs in MSI. For error correction the syndrome bits generated must be read back into all four EDCs through the CB inputs. This necessitates the check bit buffering shown in the connection diagram of Figure 6. The $\overline{OE}$ SC signal can control the check bit enabling – when syndrome bit outputs are enabled the external check bit lines will be disabled so that the syndrome bits may be read onto the CB inputs.

TABLE IX. DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care



Uses Modified Hamming Code 64/72
– 64 data bits
– 8 check bits
– 72 bits in total

Figure 5. 64 Bit Data Format.

MPR-734

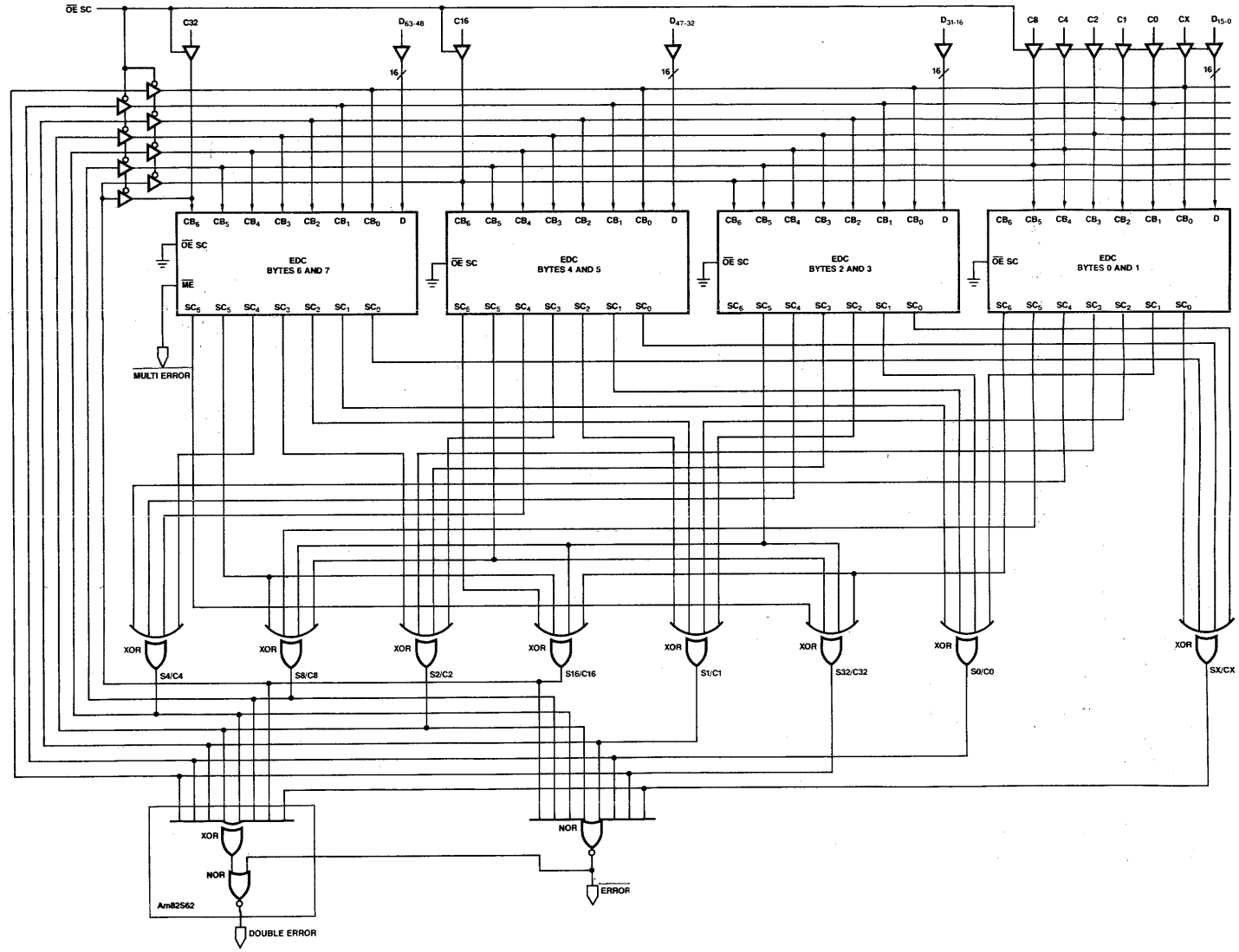


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Figure 6. Am2960 – 64 Bit Data Configuration.

Input CB_6 of Slice 0/1 is unused and need not be connected. Output SC_6 of Slice 2/3 is unspecified for the 64-bit configuration.

The error detection signals for the 64-bit configuration differ from the 16 and 32-bit configurations. The $\overline{\text{ERROR}}$ signal functions the same: it is LOW if one or more errors are detected, and HIGH if no errors are detected. The DOUBLE ERROR signal is HIGH if and only if a double-bit error is detected – it is LOW otherwise. All of the $\overline{\text{MULTI ERROR}}$ outputs of the four devices are valid. $\overline{\text{MULTI ERROR}}$ is LOW when three or more errors are detected; it is HIGH if either zero, one or two errors are detected. This is a different meaning for $\overline{\text{MULTI ERROR}}$ than in other configurations.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated appear at the outputs of the XOR gates as indicated in Figure 6.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table X. Check bits are generated as either an XOR or XNOR

TABLE X. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

of 32 of the 64 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If exactly two errors are detected, DOUBLE ERROR goes HIGH. If three or more errors are detected, $\overline{\text{MULTI ERROR}}$ goes LOW – the $\overline{\text{MULTI ERROR}}$ output of any of the four EDCs may be used.

Available as XOR gate outputs are the generated syndrome bits (see Figure 6). The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table XI gives the chart for encoding the syndrome bits generated for the 64-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16/S32 were 00100101 this would be decoded to indicate that there is a single-bit error at data bit 41). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single bit error is a check bit there is no automatic correction. Check bit correction can be done by placing the device in generate mode to produce a correct check bit sequence for the data in the Data Input Latch.

To perform the correction step, all four slices require access to the syndrome bits which are generated externally of the devices. This access is provided by reading the syndrome bits in through the CB inputs. The device connections for this are shown in Figure 6. When in Correct Mode the SC outputs must be enabled so that the syndrome bits are available at the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check Bit Input Latch are passed through the external XOR network and appear unmodified at the XOR gate outputs labeled CX to C32 (see Figure 6).

TABLE XI. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits																		
				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* – no errors detected
Number – the number of the single bit-in-error
T – two errors detected
M – more than two errors detected

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table XII shows the loading definitions for the DATA lines.

Generate Using Diagnostic Latch (Diagnostic Mode A)

Detect Using Diagnostic Latch (Diagnostic Mode B)

Correct Using Diagnostic Latch (Diagnostic Mode B)

These are special diagnostic modes selected by DIAG $MODE_{0\text{-}1}$ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch. See Table III for details.

Internal Control Mode

This mode is selected by CODE $ID_{0\text{-}2}$, input 001 (ID_2, ID_1, ID_0).

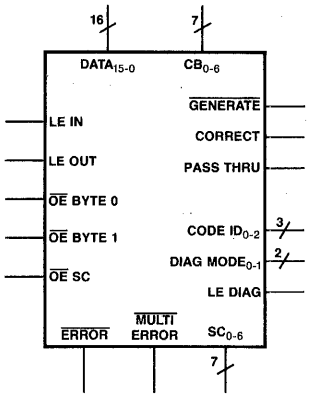
When in Internal Control Mode the EDC takes the CODE $ID_{0\text{-}2}$, DIAG $MODE_{0\text{-}1}$, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines. Table XII gives format for loading the Diagnostic Latch.

TABLE XII. DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU

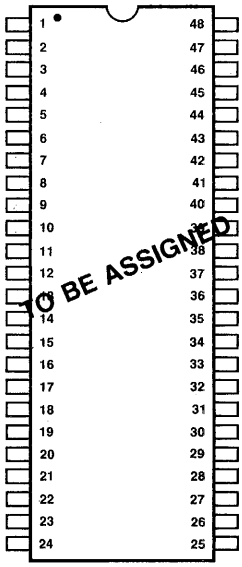
Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 – CODE ID 0
41	Slice 4/5 – CODE ID 1
42	Slice 4/5 – CODE ID 2
43	Slice 4/5 – DIAG MODE 0
44	Slice 4/5 – DIAG MODE 1
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 – CODE ID 0
57	Slice 6/7 – CODE ID 1
58	Slice 6/7 – CODE ID 2
59	Slice 6/7 – DIAG MODE 0
60	Slice 6/7 – DIAG MODE 1
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASS THRU
63	Don't Care

LOGIC SYMBOL



MPR-736

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-737

2

APPLICATIONS

The EDC unit may be used in two different ways depending upon whether the design objective is to minimize the total time for memory operations or to minimize system complexity.

Check-Only Configuration

Figure 7 shows the EDC unit in a Check-Only configuration. This method minimizes the delay needed on memory operations for EDC.

On writes to memory the EDC unit generates check-bits. On reads from memory, the EDC unit monitors the data and check bits. If an error is detected, the CPU is interrupted – the CPU then issues the appropriate control signals to the EDC unit to correct the data, write back into memory and/or perform diagnostics and error logging.

Correct-Always Configuration

Figure 8 illustrates the use of EDC unit in a Correct-Always configuration. This method has the advantage of being less complex than the Check-Only configuration. Memory operations are slower in this configuration since on reads from memory, data is always passed through the EDC unit for correction. This method does not necessarily slow down total system speed if the CPU cycle-time is the constraint on system speed.

In the Correct-Always configuration, check bits are generated by the EDC on writes into memory. On reads from memory, the check and data bits are loaded into the EDC unit – after a delay, corrected data is available at the EDC unit's outputs and is placed on the system bus. If the data was not correctable, then the $\overline{\text{MULTI ERROR}}$ output will go active and may be used to interrupt the CPU.

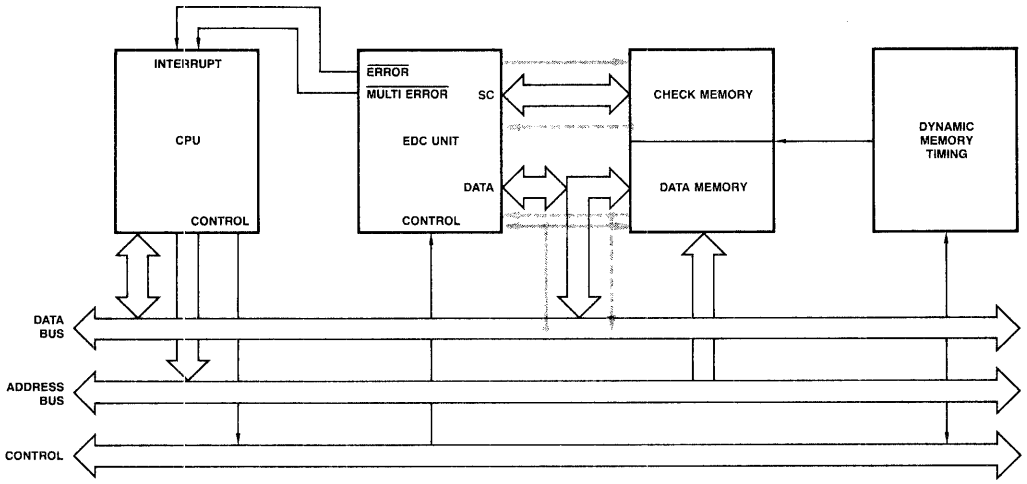


Figure 7. Check-Only Configuration. MPR-738

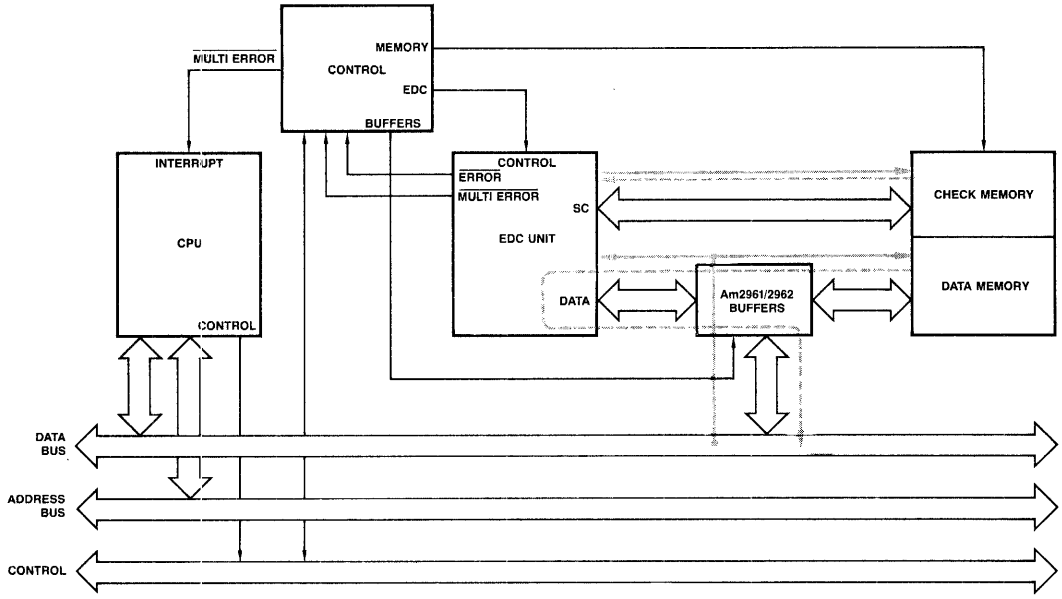


Figure 8. Correct-Always Configuration. MPR-739

Am2961 • Am2962

4-Bit Error Correction Multiple Bus Buffers

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Provides complete data path interface between the Am2960 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- Three-state 24mA output to data bus
- Three-state data output to memory
- Inverting data bus for Am2961 and non-inverting for Am2962
- Data bus latches allow operation with multiplexed buses
- Advanced low-power Schottky processing
- Space saving 24-pin 0.3" package
- 100% product assurance screening to MIL-STD-883 requirements

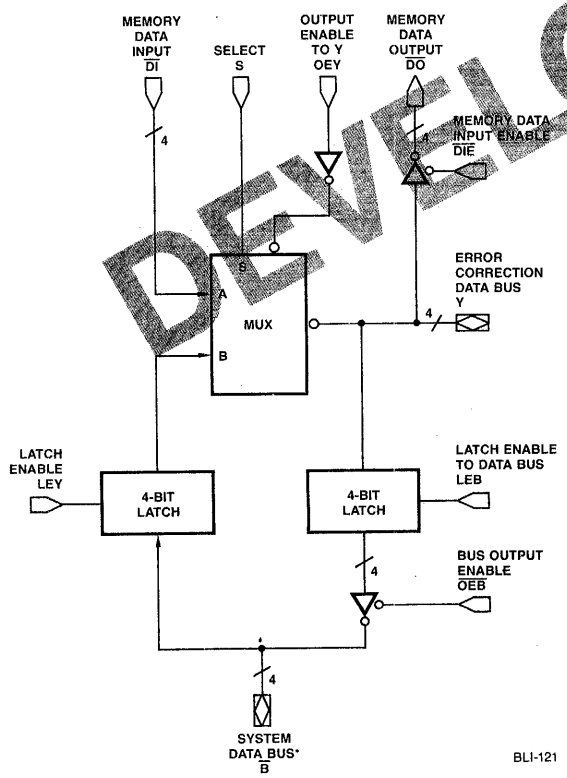
FUNCTIONAL DESCRIPTION

The Am2961 and Am2962 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the Am2960 Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The Am2961 provides an inverting data path between the data bus (B_i) and the Am2960 error correction data input (Y_i) and the Am2962 provides a non-inverting configuration (B_i to Y_i). Both devices provide inverting data paths between the Am2960 and memory data bus thereby optimizing internal data path speeds.

The Am2961 and Am2962 are 4-bit devices. Four devices are used to interface each 16-bit Am2960 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

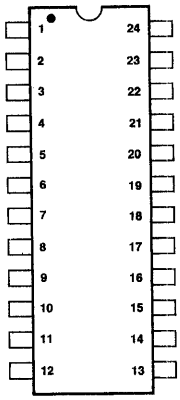
Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

LOGIC DIAGRAM



*Am2962 is the same function but non-inverting to the system data bus, B.

CONNECTION DIAGRAM
Top View



24 pin slim (0.3")

BLI-122

Note: Pin 1 is marked for orientation.

Am2964

Dynamic Memory Controller

IN DEVELOPMENT

DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter terminal count selectable at 256 or 128
- Latch Input $\overline{RAS}$ Decoder provides 4 $\overline{RAS}$ outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Grouping functions on a common chip minimizes speed differential/skew between address, $\overline{RAS}$ and $\overline{CAS}$ outputs
- 3-Port, 8-Bit Address Multiplexer with Schottky speed
- Burst mode, distributed refresh or transparent refresh mode determined by user
- Non-inverting address, $\overline{RAS}$ and $\overline{CAS}$ paths
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

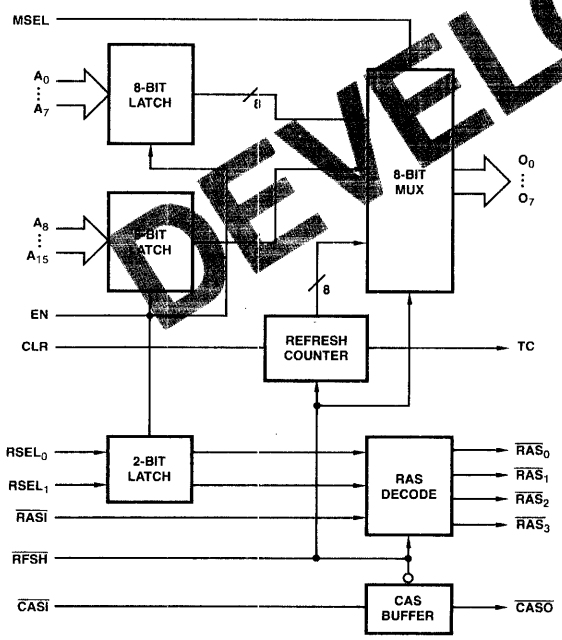
The Am2964 Dynamic Memory Controller replaces several MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the dynamic RAM address lines.

The same silicon chip also includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

Pulsing the active LOW refresh line $\overline{RFSH}$, switches the MUX to the counter output, inhibits $\overline{CAS}$, and forces all four $\overline{RAS}$ decoder outputs active simultaneously. The counter is advanced at the end of the refresh cycle – the LOW-to-HIGH transition of $\overline{RFSH}$. Various refresh modes can be accommodated – for 16K or 64K RAMs and for a wide variety of processor configurations.

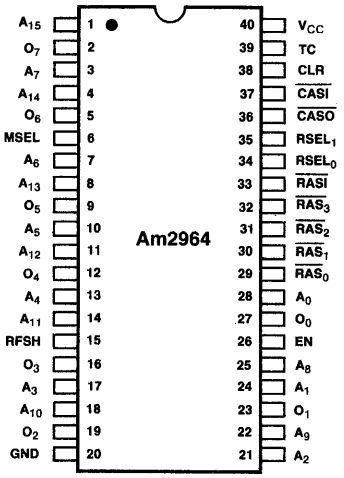
A_{15} is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1KΩ to terminate the refresh count at 128 instead of 256.

LOGIC DIAGRAM



BLI-123

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-124

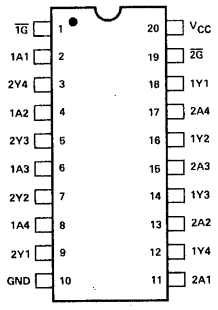
Am2965 • Am2966

Octal Dynamic Memory Drivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Octal drivers for 16K and 64K Dynamic RAMs
- Maximum performance with −0.5V max undershoot
- No external resistors required
- Improved performance over 'S240/'S244
- t_{PD} specified for 50pF and 500pF
- Specified for V_{CC} = 5.0V ±10% for COM'L and MIL versions
- V_{OH} guaranteed at V_{CC} −1.15V min
- I_{OH} and I_{OL} specified at +2.0V
- Low-power Schottky input characteristics
- Inverting Am2965 and non-inverting Am2966
- Glitch-free 3-state outputs during power-up/down
- Pin compatible replacements for designs using 'S240 and 'S244 plus external resistors
- Symmetrical controlled rise and fall time
- 100% product assurance screening per MIL-STD-883

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-125

FUNCTIONAL DESCRIPTION

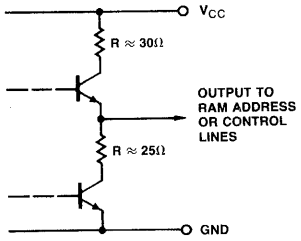
The Am2965 and Am2966 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to V_{CC} − 1.15V to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

The Am2965 and Am2966 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The Am2965 has inverting drivers and the Am2966 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the Am2964 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{PD} difference of unspecified devices.

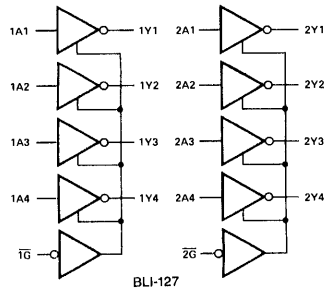
TYPICAL OUTPUT DRIVER



BLI-126

LOGIC DIAGRAMS

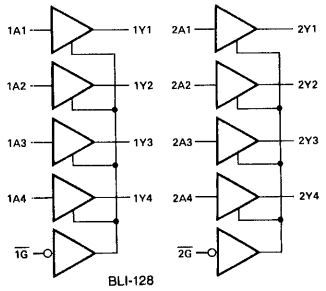
Am2965



BLI-127

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2966



BLI-128

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +7.0V
DC Output Current, into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2965/66XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)
Am2965/66XM, DM	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)
Am2965/66FM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	V_{CC}−1.15	V_{CC}−0.7V		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
				I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.4V				−200	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZH}	Off-State Current		V_O = 2.7V				100	μA
I_{OZL}	Off-State Current		V_O = 0.4V				−200	μA
I_{OL}	Output Sink Current		V_{OL} = 2.0V		35			mA
I_{OH}	Output Source Current		V_{OH} = 2.0V		−35			mA
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−60 (see I_{OH})		−200	mA
I_{CC}	Supply Current	Am2965	All Outputs HIGH	V_{CC} = MAX Outputs Open		24	50	mA
			All Outputs LOW			86	125	
			All Outputs Hi-Z			86	125	
		Am2966	All Outputs HIGH	V_{CC} = MAX Outputs Open		53	75	
			All Outputs LOW			92	130	
			All Outputs Hi-Z			116	150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2965 • Am2966
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

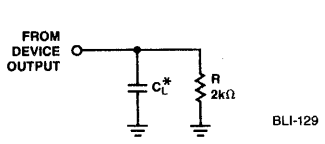
Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Output	Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms	C_L = 0pF		6	(Note 4)	ns
			C_L = 50pF	6	9	15	
			C_L = 500pF	15	22	35	
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Output		C_L = 0pF		4	(Note 4)	ns
			C_L = 50pF	6	12	20	
			C_L = 500pF	20	30	45	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4, S = 1			13	20	ns
t_{PHZ}		Figures 2 and 4, S = 2			8	12	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4, S = 1			13	20	ns
t_{PZH}		Figures 2 and 4, S = 2			13	20	
t_{SKEW}	Output-to-Output Skew	Figures 1 and 3, C_L = 50pF			±0.5	±3.0 (Note 5)	ns
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			0	−0.5	Volts

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 6)

				COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±10%		MIL (Note 7) T_A = −55 to +125°C V_{CC} = 5.0V ±10%		
Parameters	Description	Test Conditions		Min	Max	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	Figures 1 and 3	C_L = 50pF	4	20	4	20	ns
			C_L = 500pF	13	40	13	40	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Figures 1 and 3	C_L = 50pF	4	24	4	24	ns
			C_L = 500pF	17	50	17	50	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4	S = 1		24		24	ns
t_{PHZ}			S = 2		16		16	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4	S = 1		28		28	ns
t_{PZH}			S = 2		28		28	
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			−0.5		−0.5	Volts

Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
7. T_C = −55 to +125°C for Flatpak versions.

SWITCHING TEST CIRCUITS



*t_{pd} specified at C = 50 and 500pF.

Figure 1. Capacitive Load Switching.

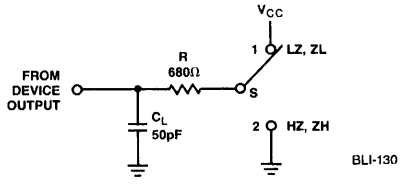
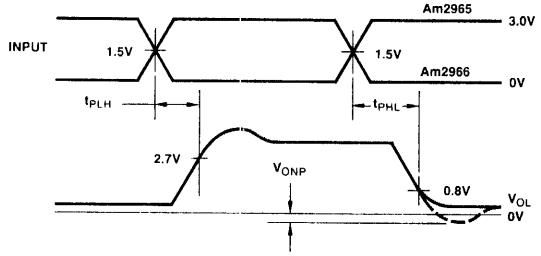


Figure 2. Three-State Enable/Disable.

TYPICAL SWITCHING CHARACTERISTICS

VOLTAGE WAVEFORMS



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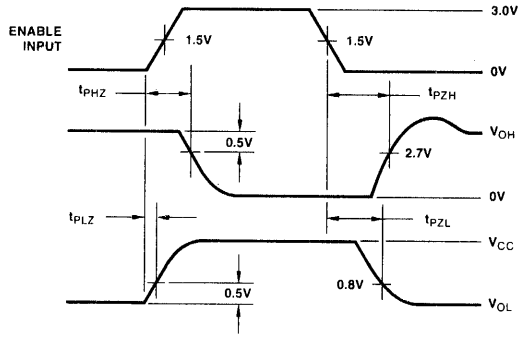
$t_r = t_f = 2.5ns$
f = 2.5MHz
t_{pw} = 200ns

Figure 3. Output Drive Levels.



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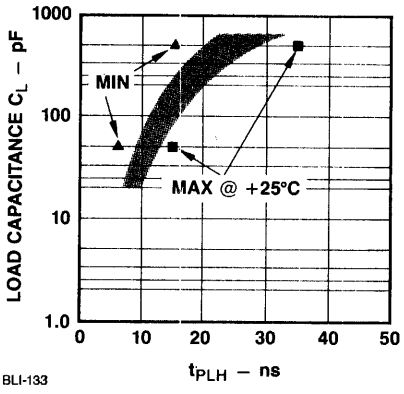
$t_r = t_f = 2.5ns$
f = 1MHz
t_{pw} = 800ns

Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈33Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} – 1.15V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

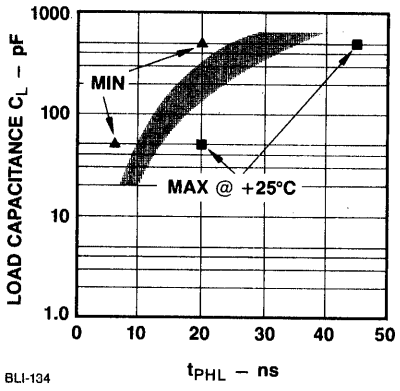
The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (Am2965) and non-inverting (Am2966) RAM Drivers.



BLI-133

Figure 5. t_{PLH} for V_{OH} = 2.7 Volts vs. C_L.

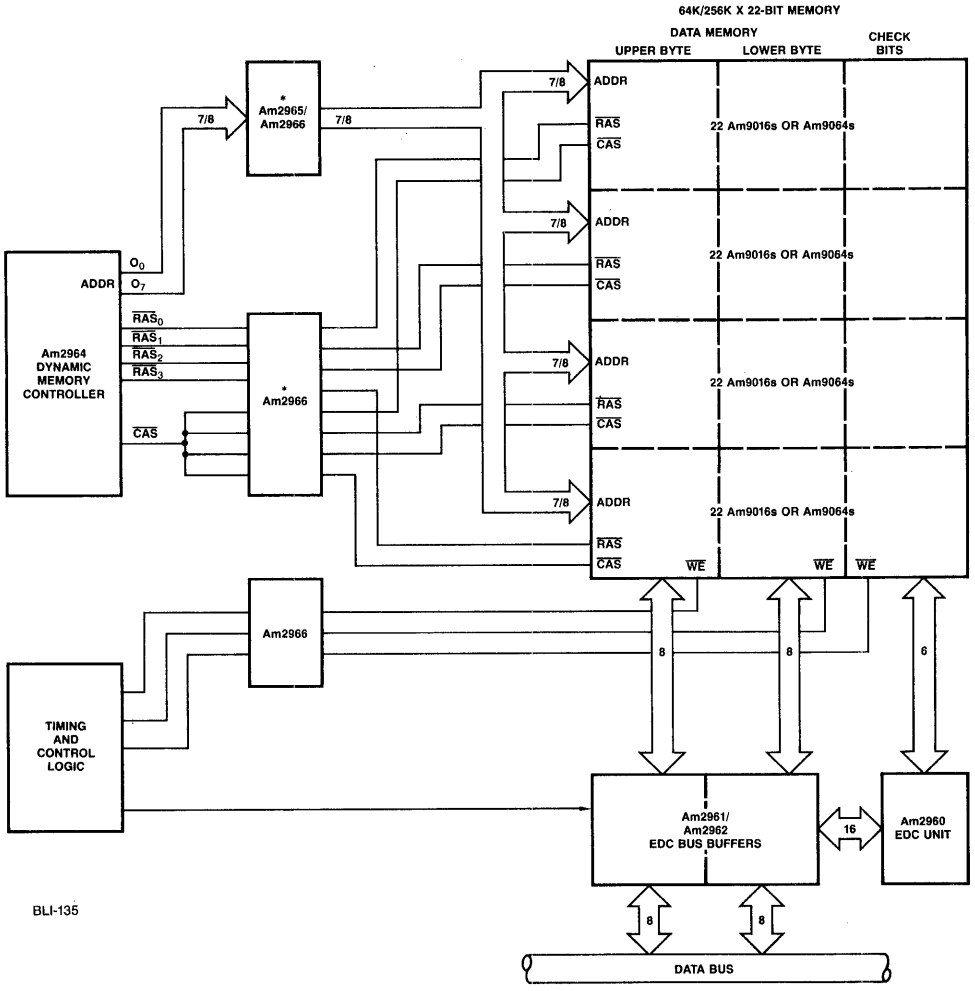


BLI-134

Figure 6. t_{PHL} for V_{OL} = 0.8 Volts vs. C_L.

The curves above depict the typical tPLH and tPHL for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

APPLICATION

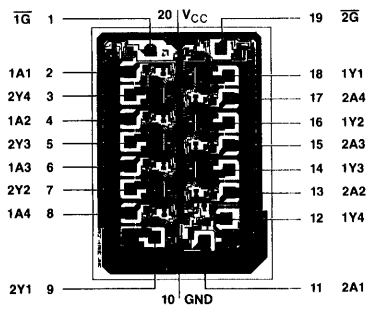


*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION

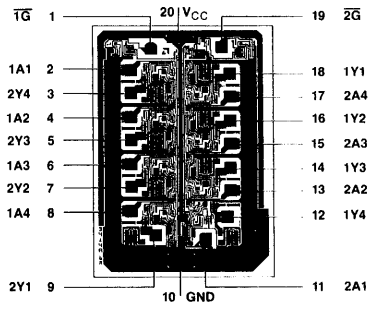
Metallization and Pad Layouts

Am2965



DIE SIZE 0.094" X 0.060"

Am2966



DIE SIZE 0.094" X 0.066"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2965 Order Number	Am2966 Order Number	Package Type	Temperature Range	Screening Level
AM2965PC	AM2966PC	P-20	C	C-1
AM2965DC	AM2966DC	D-20	C	C-1
AM2965DC-B	AM2966DC-B	D-20	C	B-1
AM2965DM	AM2966DM	D-20	M	C-3
AM2965DMB	AM2966DMB	D-20	M	B-3
AM2965FM	AM2966FM	F-20	M	C-3
AM2965FMB	AM2966FMB	F-20	M	B-3
AM2965XC	AM2966XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2965XM	AM2966XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless othewise specified.
2. C = 0 to 70°C, V_{CC} = 4.50V to 5.50V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29112

Interruptable 8-Bit Microprogram Sequencer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **FAST**
  Designed to operate in 10MHz microprogrammed systems.
- **Expandable**
  One Am29112 directly addresses up to 256 words of microcode. Two Am29112's can directly address up to 64K words of microcode.
- **Interruptable**
  The Am29112 may be interrupted at the completion of a microcycle. Internal states are saved on the stack and the Am29112 branches automatically to the interrupt service routine.
- **Many Addressing Modes**
  Immediate, relative, and N-Way addressing are all possible with the Am29112.
- **31-Level Stack**
  On-chip 31-level stack is used for subroutines, interrupts and loops.
- **Single or Double Pipeline**
  The Am29112 may be configured for either single-level pipeline or double-level pipeline operation.
- **40-Pin Dual-in-Line Package**

Note: Am2900 High Performance Controller Products Family.

For information on using the Am29112 with other Am2900 High Performance Controller Products, refer to page 2-339.

BLOCK DIAGRAM

Am29116

16-Bit Bipolar Microprocessor

ADVANCE INFORMATION

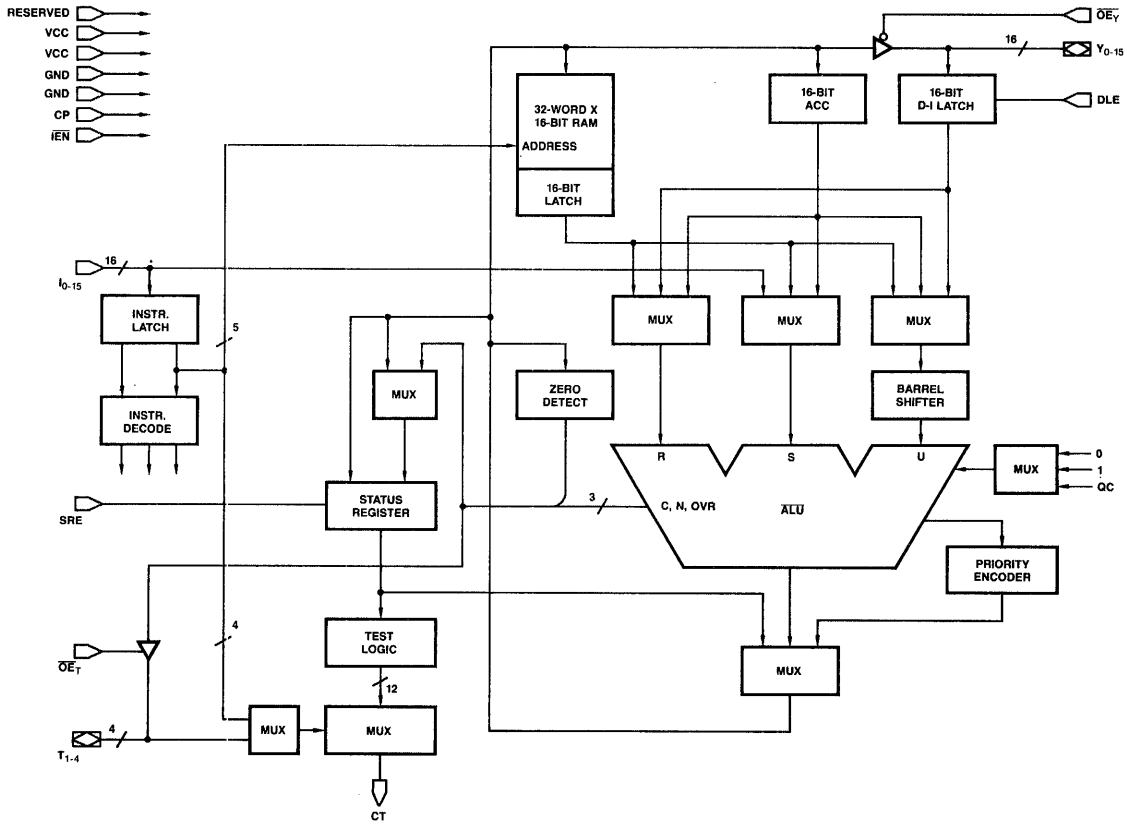
DISTINCTIVE CHARACTERISTICS

- **Designed for Controller Applications**
  Instruction set designed for high performance peripheral controllers, communications controllers, industrial controllers and digital modems . . . but general purpose, too. Excellent solution for applications requiring speed and bit-manipulation power.
- **FAST**
  Design objective of 100ns maximum microcycle time for all instructions. Allows a 10MHz clock rate.
- **Powerful Instruction Set**
  All instructions executable in single cycle on full 16-bit word or on 8-bit byte:
  - Add, Subtract
  - N-bit Rotate
  - Shift-Up/Shift-Down
  - Set-Bit/Reset-Bit
  - Add/Subtract 2^N
  - Rotate & Merge
  - Rotate & Compare
  - CRC Generation
  - Priority Encode
- **Powerful Data Manipulation**
  Full 16-bit data path. 32 registers on chip. Direct data input for immediate mode instructions.

Note: Am2900 High Performance Controller Products Family.

Refer to the following page for more information on the Am2900 High Performance Controller Products Family.

BLOCK DIAGRAM



MPR-740

Am2900 HIGH PERFORMANCE CONTROLLER PRODUCTS

A Better Way is Coming

A new family of products coming from Advanced Micro Devices makes high-performance controller design a snap.

Microprogramming: Best for Computers, Best for Controllers

Microprogramming, long the preferred approach for computer design, offers lots of advantages in controllers as well. The ease with which the functions of a microprogrammed controller can be enhanced and modified made the original 2900 Family popular for many disk, printer and communications controllers. The high speed operation of these microprogrammed systems makes it possible to handle higher data rates from newer peripheral devices and to build intelligence into the controller.

But the original 2900 products are architecturally oriented toward computers, with design features optimized for arithmetic functions and short sequences of microinstructions. MOS processors are good choices for many low speed applications, but when the demand for speed and intelligence goes up, they cannot keep pace. Controllers need something better.

Something better has been added to our 2900 Family: New products especially for controllers. Through 1980 and 1981, we'll be bringing you new products whose architectural features are optimized for bit manipulation, character handling, data communication and long, sophisticated microprograms. (Continued on next page)

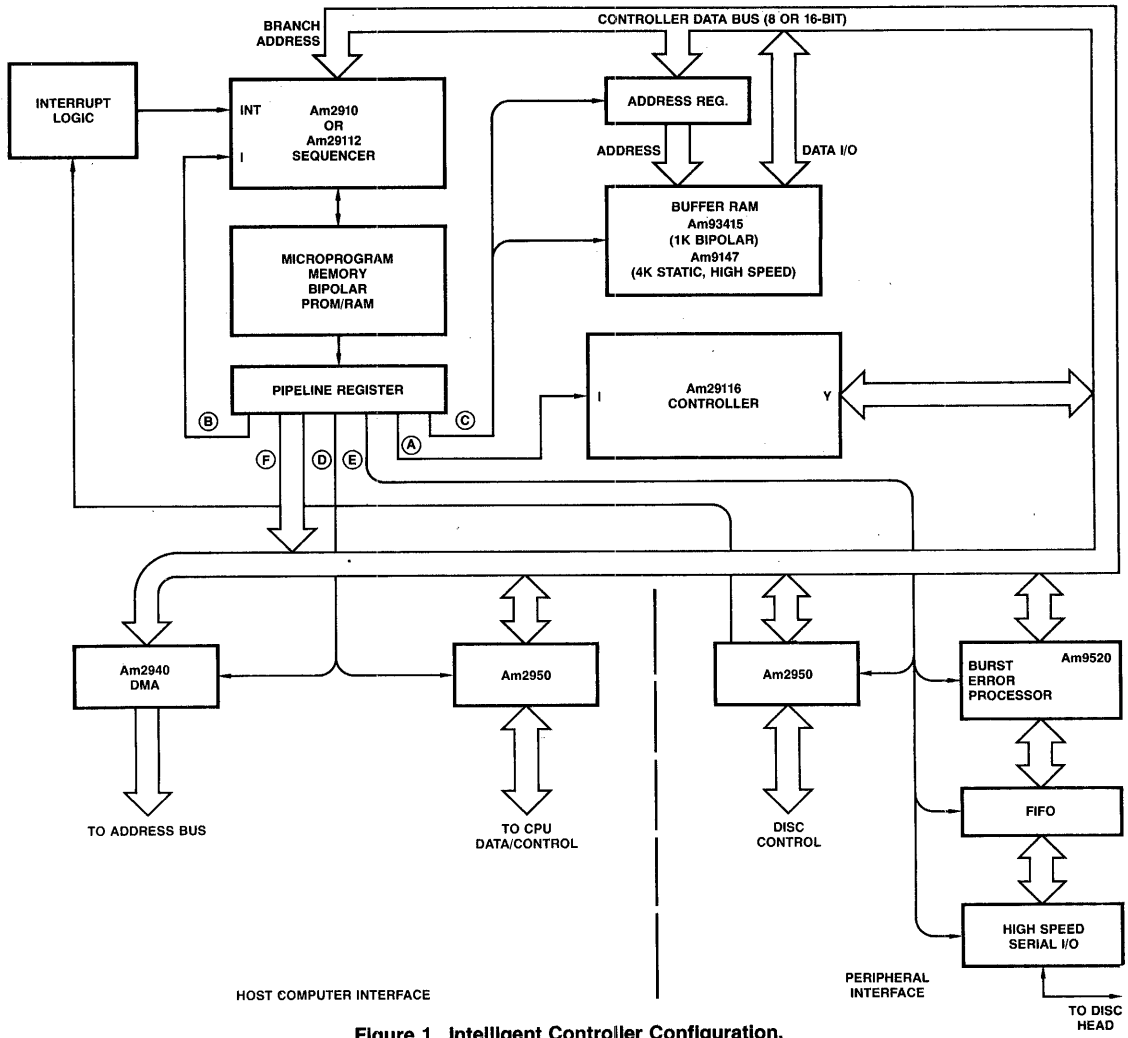


Figure 1. Intelligent Controller Configuration.

MPR-741

Fast Like You've Never Had

The central element of our new high speed controller family is the Am29116 – a 16-bit bipolar microprocessor. It's not a "bit slice" – it's a complete 16-bit processor, with ALU, working registers and status register. It can do computer instructions like add and subtract, but it's more than a computer. The Am29116 has instructions just for controllers – instructions not available in any other microprocessor. And it's fast – designed to run at 10MHz clock rate, to keep up with the needs of today's high performance peripherals and tomorrow's high speed communication channels.

A Whole Family of Fast LSI Controller Parts

There's more to our controller family than just the Am29116. A new sequencer, the Am29112, has been expressly designed for 10MHz microprogram control, with features like real-time interrupt servicing and deep subroutining. Rapid internal data transfer is handled by the Am2940 DMA Address Generator and by the Am2950 handshaking I/O port. The Am9520 Burst Error Processor will provide a solution for error correction on disk reads. And special I/O devices are in development for disk interfaces, fiber optics links and more. Now, more than ever, the 2900 Family is the better solution for high data rate and highly intelligent control problems.

Typical Configuration Using the 2900 Controller Family

A typical intelligent controller configuration is shown in Figure 1. The basic controller consists of the Am29116, a microprogram control unit and a high speed buffer memory. Each microinstruction includes: A) a 16-bit instruction field to the Am29116, B) next-microinstruction selection bits, C) control for the buffer memory, D and E) control for the interface circuits and F) possibly an 8 or 16-bit data field.

Interface circuits like the Am2940 and Am2950 are used to provide DMA and to pass data between the controller and the host computer. Other circuits are used to interface to the peripheral. In this example, a disk interface is shown with a serial-parallel converter, a FIFO and a burst error processor. Controllers for other peripherals use identical hardware except for the peripheral interface itself.

Am29700 • Am29701

Non-Inverting Schottky 64-Bit Random Access Memories

Refer to

Am27S06 • Am27S07

in the Bipolar Memory Section

2

The Am29700 is replaced by the Am27S06 (open collector).

The Am29701 is replaced by the Am27S07 (3-state).

Am29702 • Am29703

Schottky 64-Bit Random Access Memories

Refer to

Am27S02 • Am27S03

in the Bipolar Memory Section

The Am29702 is replaced by the Am27S02 (open collector).

The Am29703 is replaced by the Am27S03 (3-state).

Am29705

16-Word by 4-Bit 2-Port RAM

Distinctive Characteristics

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port
- Data output is non-inverting with respect to data input
- Chip Select and Write Enable inputs for ease in cascading
- Advanced Low-Power Schottky processing
- 100% reliability testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

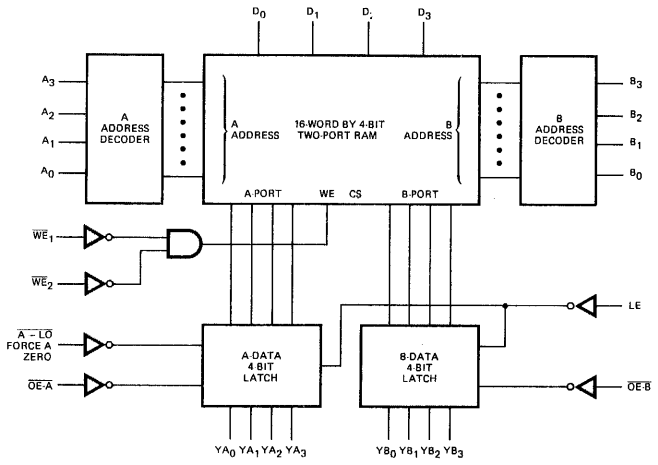
The Am29705 is a 16-word by 4-bit, two-port RAM built using advanced Low-Power Schottky processing. This RAM features two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29705 features three-state outputs so that several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE\text{-}A}$ input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE\text{-}B}$ input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM.

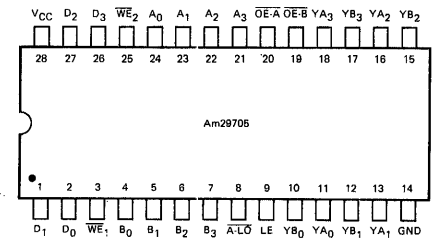
LOGIC DIAGRAM



MPR-251

CONNECTION DIAGRAM

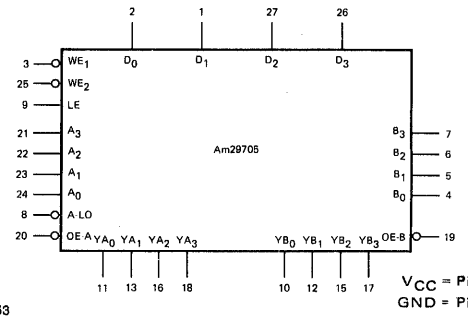
Top View



Note: Pin 1 is marked for orientation.

MPR-252

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

MPR-253

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

2

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am29705XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am29705XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4			Volts
			COM'L, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			$\overline{OE\text{-}A}$, $\overline{OE\text{-}B}$			−0.54	
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				0.1	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX., V_{IN} = V_{IH} or V_{IL}	V_O = 2.7V			20	µA
			V_O = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Worst case I_{CC} is at minimum temperature) (Note 4)	T_A = 25°C		121	195	mA
			T_A = 0°C to +70°C			210	
			T_A = 70°C			170	
			T_C = −55°C to +125°C			210	
			T_C = 125°C			150	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded except $\overline{OE\text{-}A}$ and $\overline{OE\text{-}B}$ =2.4V.

SWITCHING CHARACTERISTICS

(Input Levels = 0V and 3.0V, Transitions Measured at 1.5V)

Maximum Combinational Delays (in ns) (R_L = 390Ω, C_L = 50pF)

Parameters	From	To	Conditions	T_A = 0°C to +70°C V_{CC} = 4.75V to 5.25V	T_C = −55°C to +125°C V_{CC} = 4.5V to 5.5V
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	53	58
Turn-On Time	$\overline{OE\text{-}A}$ or $\overline{OE\text{-}B}$ LOW	YA or YB Stable		30	30
Turn-Off Time	$\overline{OE\text{-}A}$ or $\overline{OE\text{-}B}$ HIGH	YA or YB Off	C_L = 5.0pF	20	20
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		35	35
Enable Time	LE HIGH	YA and YB Stable		32	32

SWITCHING CHARACTERISTICS (Cont.)

(Input Levels = 0V and 3.0V, Transitions Measured at 1.5V)

Minimum Set-up and Hold Times (in ns)

Parameters	From	To	Conditions	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max.	$T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max.
Data Set-up Time	D Stable	Either $\overline{WE}$ HIGH		20	25
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		3	5
Address Set-up Time	B Stable	Both $\overline{WE}$ LOW		5	5
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0	0
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0	0
Address Set-up Before Latch Closes	A or B Stable	LE LOW		45	50

Minimum Pulse Widths

Parameters	Input	Pulse	Conditions	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max.	$T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max.
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25	25
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	20	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20	20
Latch Data Capture	LE	LOW-HIGH-LOW		20	25

FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	Function	RAM Outputs at Latch Inputs A-Port	B-Port
L	L	Write D Into B	A data (A ≠ B)	Not Specified
X	H	No write	A data	B data
H	X	No write	A data	B data

H = HIGH
L = LOW
X = Don't care

YA READ

Inputs $\overline{OE-A}$	Inputs $\overline{A-LO}$	Inputs LE	YA Output	Function
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A – Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

YB READ

Inputs $\overline{OE-B}$	Inputs LE	YB Output	Function
H	X	Z	High impedance
L	H	B – Port RAM data	Latches transparent
L	L	NC	Latches retain data

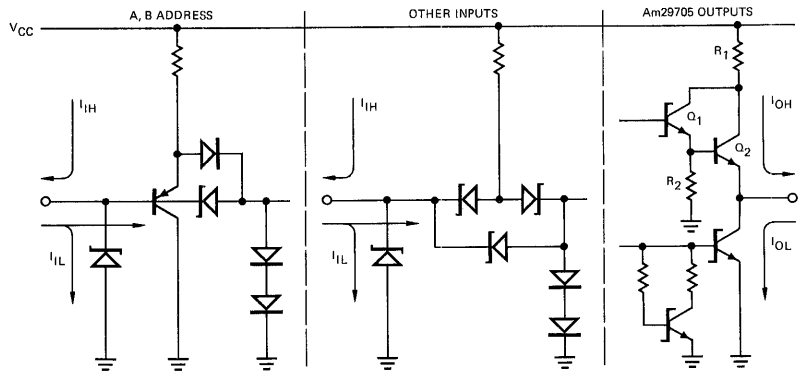
H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_1	1	1	–	–
D_0	2	1	–	–
$\overline{WE}_1$	3	1	–	–
B_0	4	0.55	–	–
B_1	5	0.55	–	–
B_2	6	0.55	–	–
B_3	7	0.55	–	–
$\overline{A-LO}$	8	1	–	–
LE	9	1	–	–
YB_0	10	–	100/200	33
YA_0	11	–	100/200	33
YB_1	12	–	100/200	33
YA_1	13	–	100/200	33
GND	14	–	–	–
YB_2	15	–	100/200	33
YA_2	16	–	100/200	33
YB_3	17	–	100/200	33
YA_3	18	–	100/200	33
$\overline{OE-B}$	19	1	–	–
$\overline{OE-A}$	20	1	–	–
A_3	21	0.55	–	–
A_2	22	0.55	–	–
A_1	23	0.55	–	–
A_0	24	0.55	–	–
$\overline{WE}_2$	25	1	–	–
D_3	26	1	–	–
D_2	27	1	–	–
V_{CC}	28	–	–	–

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



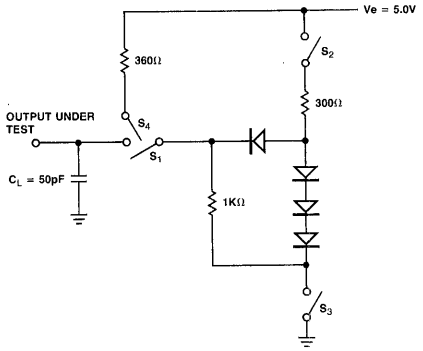
Note: Actual current flow direction shown.

MPR-254

LOAD CIRCUITS FOR AC TESTS

All delays are measured from 1.5V at the input to 1.5V at the output, except the output disable times which are measured from 1.5V at the input to 0.5V below or above the output level.

1. For function and AC tests except output enable tests S_1, S_2 and S_3 are closed while S_4 is open.
2. For output enable tests:
   t_{PZH}: S_1 and S_3 are closed, S_2 and S_4 are open.
   t_{PZL}: S_1 and S_2 are closed, S_3 and S_4 are open.
3. C_L = 5pF for output disable tests.



MPR-581

DEFINITION OF TERMS

D_0, D_1, D_2, D_3 Data Inputs. New data is written into the RAM through these inputs.

A_0, A_1, A_2, A_3 The A-address Inputs. The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

B_0, B_1, B_2, B_3 The B-address inputs. The four-bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

YA_0, YA_1, YA_2, YA_3 The four A-Data Latch Outputs.

YB_0, YB_1, YB_2, YB_3 The four B-Data Latch Outputs.

$\overline{WE}_1, \overline{WE}_2$ Write Enables. When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

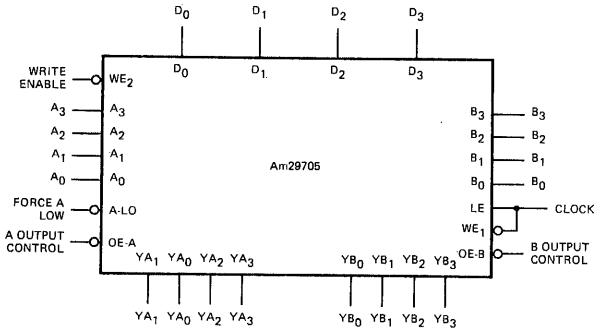
$\overline{OE}$-A A-port Output Enable. When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE}$-A is HIGH, the YA_i outputs are in the high-impedance (off) state.

$\overline{OE}$-B B-port Output Enable. When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE}$-B is HIGH, the YB_i outputs are in the high-impedance (off) state.

LE Latch Enable. The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs.

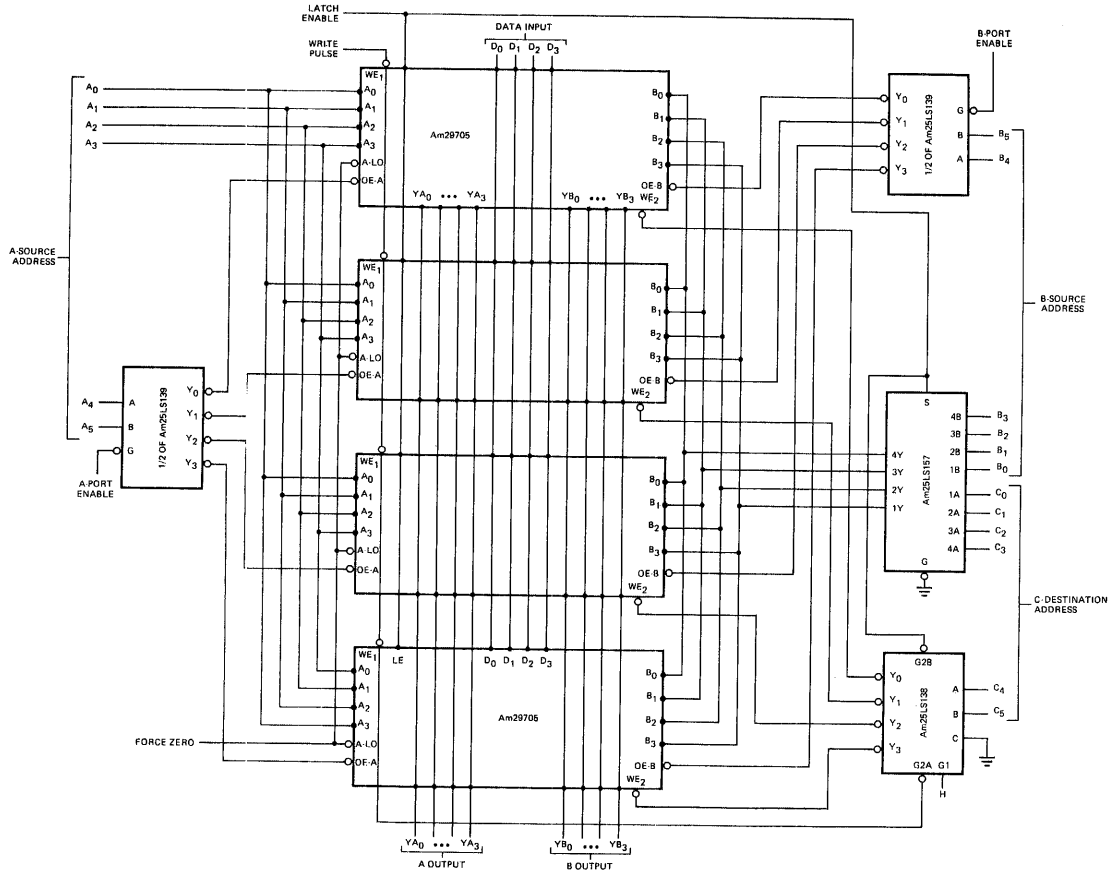
$\overline{A\text{-}LO}$ Force A Zero. This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed.

APPLICATIONS



MPR-257

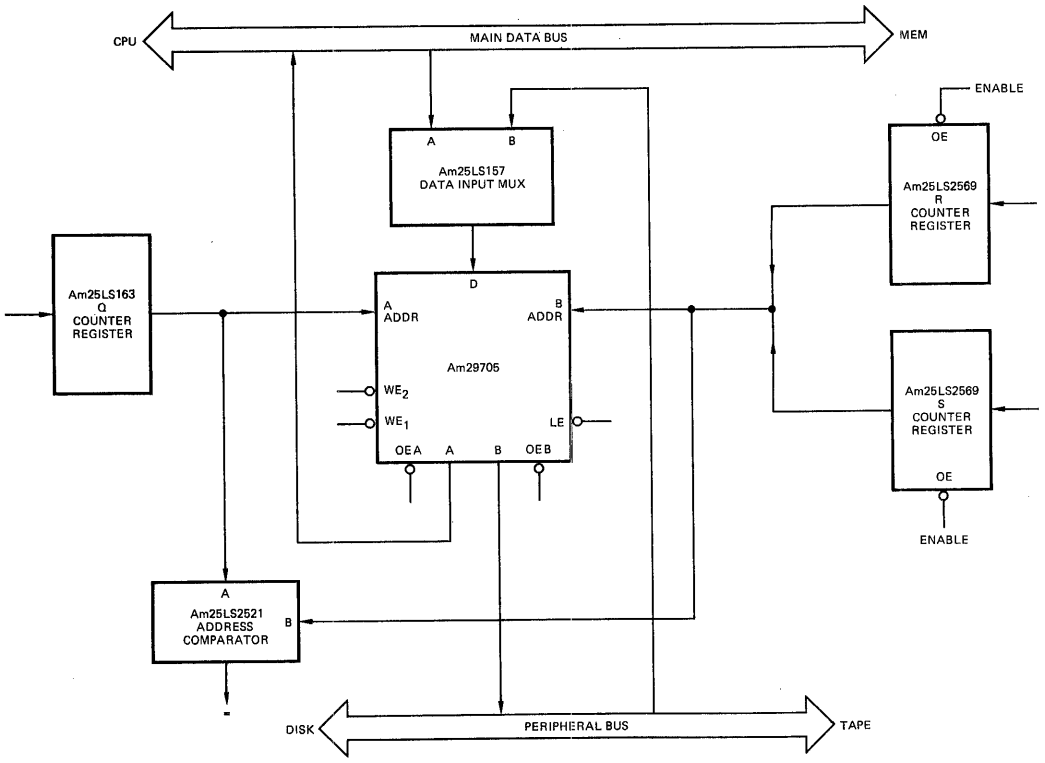
A 16-word by 4-bit two-port RAM with LE and WE_1 connected to make the device appear edge triggered. WE_1 and WE_2 are logically identical but are electrically slightly different. For synchronous operation without possibility of race, WE_1 should be connected to LE.



MPR-258

A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

APPLICATIONS (Cont'd)



The Am29705 as a two-way interface buffer. Data may be passed between the main data bus and the peripheral data bus under I/O control. The two-port RAM allows data to be written into buffer storage from a peripheral device, using the B address port and the S counter register, while it is being read into main memory, using the A address port and the Q counter register. This simultaneous read/write capability facilitates DMA transfers because the CPU can ignore write requests from the peripheral device. Data output from CPU to the peripheral device is handled by sequential write and read operations. Data is written into buffer storage from the CPU, using the B address port and the R counter register. It is read onto the peripheral device using the B address port and either the R register, for single word transfers, or the S register, for block transfers.

MPR-259

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29705PC	P-28	C	C-1
AM29705DC	D-28	C	C-1
AM29705DCTB	D-28	C	B-2 (Note 4)
AM29705DM	D-28	M	C-3
AM29705DM-B	D-28	M	B-3
AM29705FM	F-28-1	M	C-3
AM29705FM-B	F-28-1	M	B-3
AM29705XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29705XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am29705A

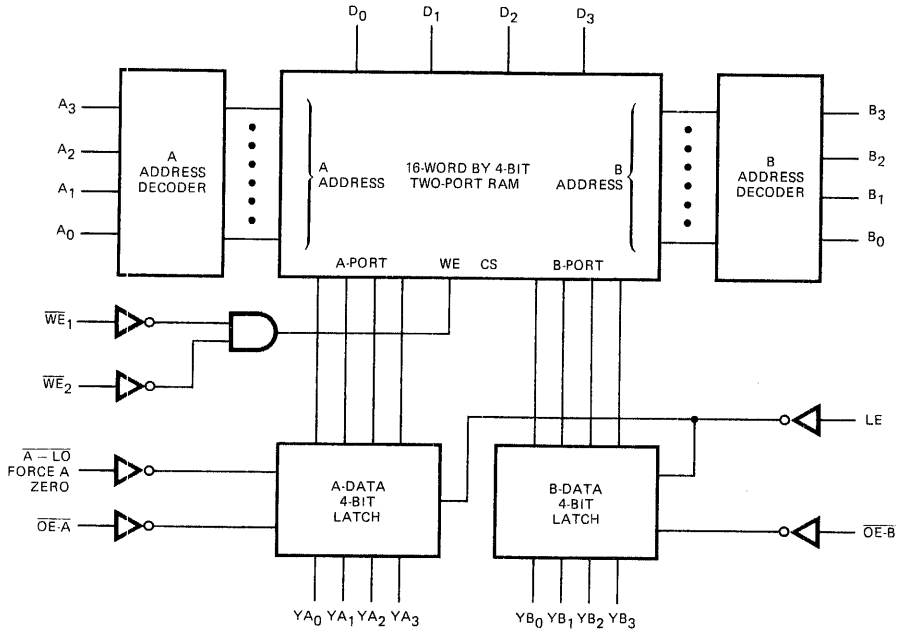
16-Word by 4-Bit 2-Port RAM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Faster Version of the Am29705**
  The Am29705A has a design objective of a 30-40% speed improvement on the critical paths versus the Am29705.
- **Plug-in Replacement for the Am29705**
  The Am29705A is a pin-for-pin replacement for the Am29705. Systems using the Am29705 will be able to use the Am29705A instead with no design changes.

LOGIC DIAGRAM



Am29720 • Am29721

Low-Power Schottky 256-Bit Random Access Memories

Refer to

Am27LS00 • Am27LS01

in the Bipolar Memory Section

2

The Am29720 is replaced by the Am27LS01 (open collector).

The Am29721 is replaced by the Am27LS00 (3-state).

Am29750A • Am29751A

256-Bit Generic Series Bipolar PROM

Refer to

Am27S18 • Am27S19

in the Bipolar Memory Section

The Am29750A is replaced by the Am27S18 (open collector).

The Am29751A is replaced by the Am27S19 (3-state).

Am29760A • Am29761A

1024-Bit Generic Series Bipolar PROM

Refer to

Am27S20 • Am27S21

in the Bipolar Memory Section

The Am29760A is replaced by the Am27S20 (open collector).

The Am29761A is replaced by the Am27S21 (3-state).

Am29770 • Am29771

2048-Bit Generic Series Bipolar PROM

Refer to

Am27S12 • Am27S13

in the Bipolar Memory Section

The Am29770 is replaced by the Am27S12 (open collector).

The Am29771 is replaced by the Am27S13 (3-state).

Am29774 • Am29775

4096-Bit Generic Series Bipolar PROM with Register

Refer to
Am27S26 • Am27S27
in the Bipolar Memory Section

The Am29774 is replaced by the Am27S26 (open collector).

The Am29775 is replaced by the Am27S27 (3-state).

Am29803A

16-Way Branch Control Unit

DISTINCTIVE CHARACTERISTICS

- 16 separate instructions -- 2 , 4 , 8 , or 16-way branch in one microprogram execution cycle
- Four individual test inputs
- Four individual outputs for driving the four OR inputs on the Am2909 Microprogram Sequencer
- Provides maximum branch capability in a microprogram control unit using the Am2909
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

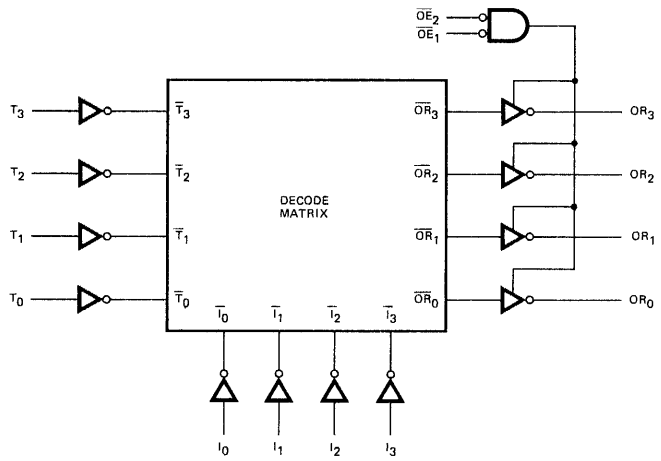
FUNCTIONAL DESCRIPTION

The Am29803A is a Low-Power Schottky processed device that provides 16-way branch control when used in conjunction with the Am2909 Microprogram Sequencer.

The device features 16 instructions that provide all combinations of simultaneous testing of four different inputs. The device has four outputs that are used to drive the four OR inputs of the Am2909 Microprogram Sequencer.

The "zero" instruction inhibits the testing of any of the four test (T) inputs. The remaining 15 instructions are used to test combinations of 1, 2, 3, or 4 of the T inputs simultaneously. If one T input is being tested, the Am29803A will select one of two possible addresses. If two T inputs are being tested, the device will select one of four possible addresses. If three T inputs are being tested, the device will select one of eight possible addresses. If all four T inputs are being tested, the device will select one of sixteen addresses as the field used to drive the OR inputs of the Am2909.

LOGIC DIAGRAM



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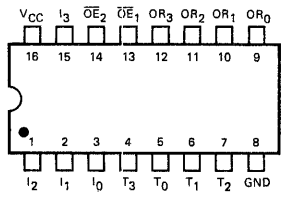
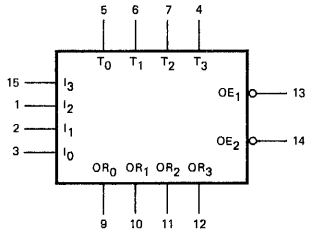
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-310

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-311

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

2

OPERATING RANGE

COM'L	Am29803ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29803ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		25	35	ns
t_{PLH} / t_{PHL}	Γ_i to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		25	35	ns
t_{ZH} / t_{ZL}	$\overline{OE}_i$ to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		15	18	ns
t_{HZ} / t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 5.0 pF, R_L = 2.0 kΩ		15	18	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	COM'L T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% Min.	MIL Max.	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		45		60	ns
t_{PLH} / t_{PHL}	T_i to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		45		60	ns
t_{ZH} / t_{ZL}	$\overline{OE}_i$ to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		30		30	ns
t_{HZ} / t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		20		20	ns

DEFINITION OF FUNCTIONAL TERMS

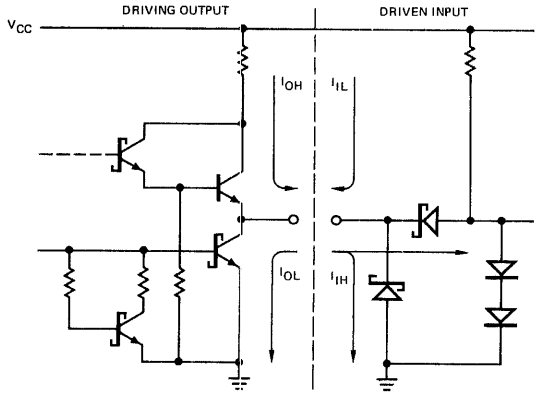
I_0, I_1, I_2, I_3 — The four instruction inputs to the device

T_0, T_1, T_2, T_3 — The four test inputs for the device

OR_0, OR_1, OR_2, OR_3 — The four outputs of the device that are connected to the four OR inputs of the Am2909

$\overline{OE}_1, \overline{OE}_2$ — Output Enable. When either $\overline{OE}$ input is HIGH, the OR_i outputs are in the high impedance state. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the OR outputs are enabled and the selected data will be present.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	I_2	0.5	–	–	–
2	I_1	0.5	–	–	–
3	I_0	0.5	–	–	–
4	T_3	0.5	–	–	–
5	T_0	0.5	–	–	–
6	T_1	0.5	–	–	–
7	T_2	0.5	–	–	–
8	GND	–	–	–	–
9	OR_0	–	100	44	44
10	OR_1	–	100	44	44
11	OR_2	–	100	44	44
12	OR_3	–	100	44	44
13	$\overline{OE}_1$	0.5	–	–	–
14	$\overline{OE}_2$	0.5	–	–	–
15	I_3	0.5	–	–	–
16	V_{CC}	–	–	–	–

FUNCTION TABLE

Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X X	X X	X X	L H	L L	L L	L L	L H
Test T_1	L	L	H	L	X X	X X	L H	X X	L L	L L	L L	L H
Test T_0 & T_1	L	L	H	H	X X X X	X X X X	L L H H	L H L H	L L L L	L L L L	L L H H	L H L H
Test T_2	L	H	L	L	X X	L H	X X	X X	L L	L L	L L	L H
Test T_0 & T_2	L	H	L	H	X X X X	L L H H	X X X X	L H L H	L L L L	L L L L	L L H H	L H L H
Test T_1 & T_2	L	H	H	L	X X X X	L L H H	L H L H	X X X X	L L L L	L L L L	L L H H	L H L H
Test T_0, T_1 & T_2	L	H	H	H	X X X X X X X X	L L L L H H H H	L L H H L L H H	L H L H L H L H	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_3	H	L	L	L	L H	X X	X X	X X	L L	L L	L L	L H
Test T_0 & T_3	H	L	L	H	L L H H	X X X X	X X X X	L H L H	L L L L	L L L L	L L H H	L H L H
Test T_1 & T_3	H	L	H	L	L L H H	X X X X	L H L H	X X X X	L L L L	L L L L	L L H H	L H L H
Test T_0, T_1 & T_3	H	L	H	H	L L L L H H H H	X X X X X X X X	L L H H L L H H	L H L H L H L H	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_2 & T_3	H	H	L	L	L L H H	L H L H	X X X X	X X X X	L L L L	L L L L	L L H H	L H L H
Test T_0, T_2 & T_3	H	H	L	H	L L L L H H H H	L L H H L L H H	X X X X X X X X	L H L H L H L H	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_1, T_2 & T_3	H	H	H	L	L L L L H H H H	L L H H L L H H	L H L H L H L H	X X X X X X X X	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_0, T_1, T_2 & T_3	H	H	H	H	L L L L L L H H H H H H H H	L L L L H H L L L L H H H H	L L H H L L H H L L H H L L	L H L H L H L H L H L H L H	L L L L L L H H H H H H H H	L L L L H H L L L L H H H H	L L H H L L H H L L H H L L	L H L H L H L H L H L H L H

L = LOW, H = HIGH, X = Don't care

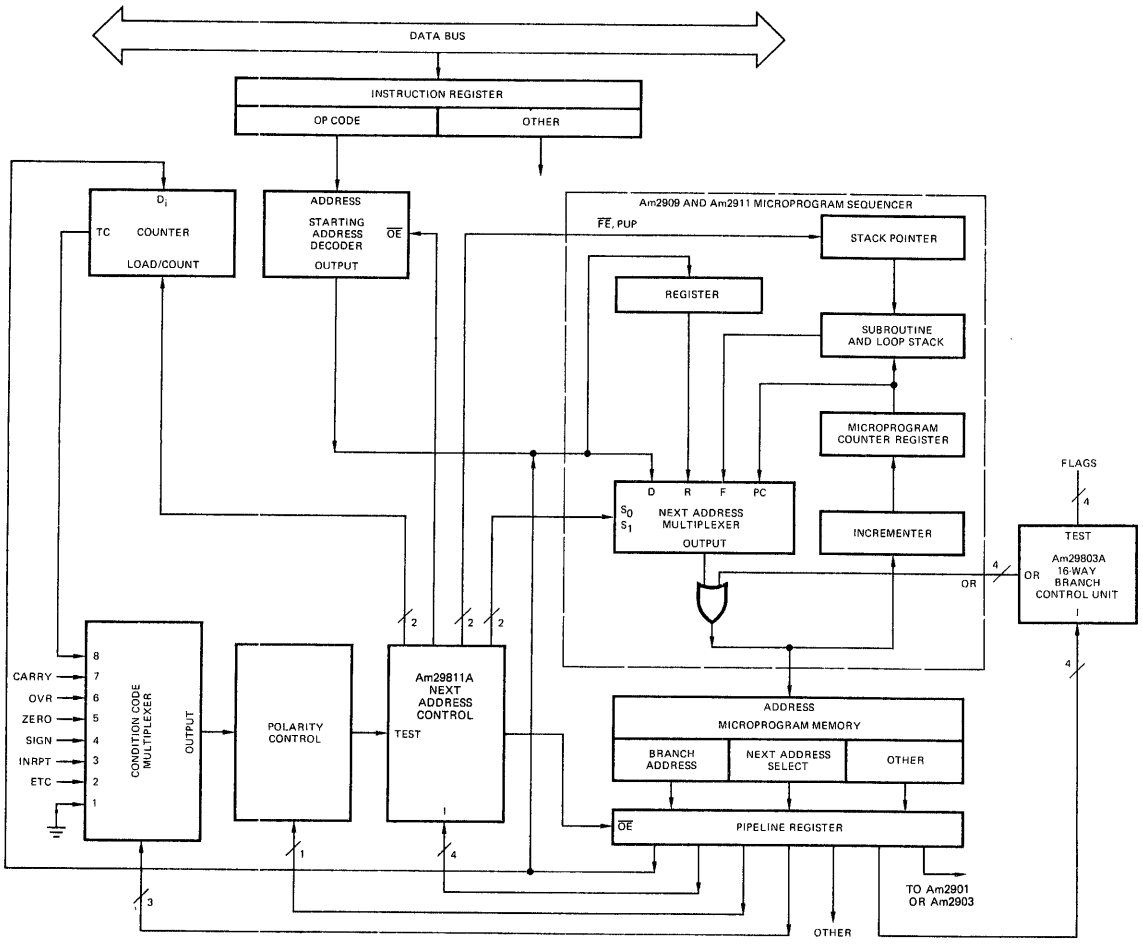
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29803APC	P-16	C	C-1
AM29803ADC	D-16	C	C-1
AM29803ADC-B	D-16	C	B-1
AM29803ADM	D-16	M	C-3
AM29803ADM-B	D-16	M	B-3
AM29803AFM	F-16	M	C-3
AM29803AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A typical computer control unit using the Am2909, Am2911, Am29803A and Am29811A. Note that the least significant microprogram sequencer is an Am2909 and the more significant sequencers are Am2911's.

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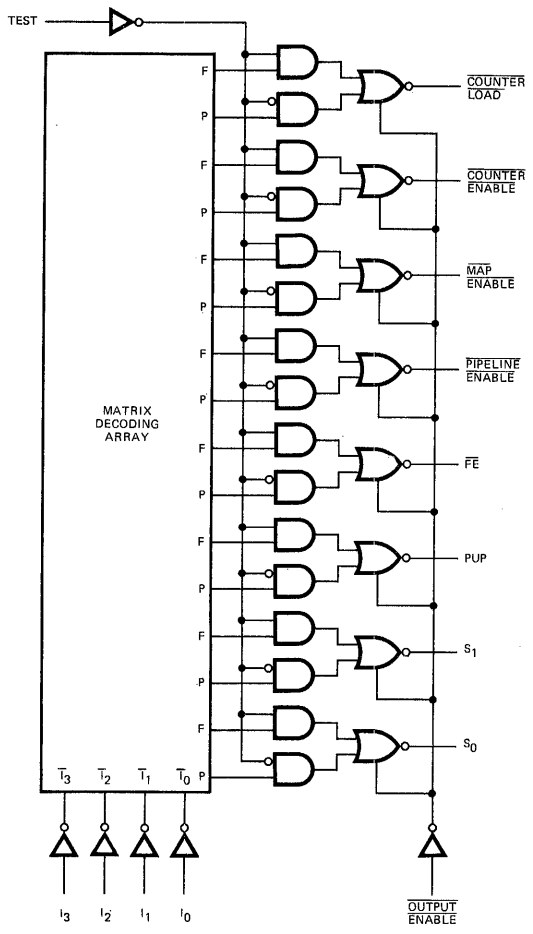
Am29811A
Next Address Control Unit

DISTINCTIVE CHARACTERISTICS

- Next address control unit for the Am2911 Microprogram Sequencer
- 16 next address instructions
- Test input for conditional instructions
- Separate outputs to control the Am2911, an independent event counter, and a mapping PROM/branch address interface
- Advanced Low-Power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

LOGIC DIAGRAM



P = Pass
F = Fail

MPR-314

FUNCTIONAL CHARACTERISTICS

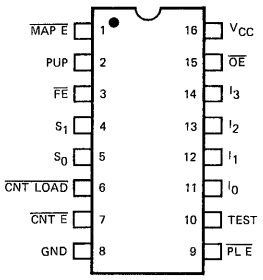
The Am29811A is a Low-Power Schottky device designed specifically for next address control of the Am2911 Microprogram Sequencer. The device contains all outputs required to control a high-performance computer control unit or a structured state machine design using microprogramming techniques.

Sixteen instructions are available by using a four-bit instruction field $I_{0\text{-}3}$. In addition, a test input is available such that conditional instructions can be performed based on a condition code test input.

The full instruction set consists of such functions as conditional jumps, conditional jump-to-subroutine, conditional return-from-subroutine, conditional repeat loops, conditional branch to starting address, and so forth.

One Am29811A can be used to control any number of Am2911 Microprogram Sequencers. The Am2911 Sequencer is a four-bit slice itself. Thus, one Am29811A Next Address Control Unit and three Am2911 Microprogram Sequencers can be used to build the most powerful, state-of-the-art, microprogram sequencer capable of controlling 4k words of microprogram memory.

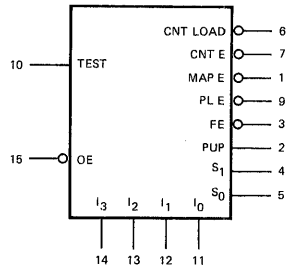
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-315

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)	
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29811ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29811ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 2.4V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} / t_{PHL}	I_i to Any Output	C_L = 15 pF, R_L = 2.0 kΩ		25	35	ns
t_{PLH} / t_{PHL}	Test to Any Output			25	35	ns
t_{ZH} / t_{ZL}	$\overline{OE}$ to Any Output			15	20	ns
t_{HZ} / t_{LZ}	$\overline{OE}$ to Any Output	C_L = 5.0 pF, R_L = 2.0 kΩ		15	20	ns

2

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			COM'L		MIL		
			T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5%		T_A = –55°C to +125°C, V_{CC} = 5.0 V ±10%		
Parameters	Description	Test Conditions	Min.	Max.	Min.	Max.	Units
t_{PLH} / t_{PHL}	I_i to Any Output	C_L = 15 pF, R_L = 2.0 kΩ		40		50	ns
t_{PLH} / t_{PHL}	Test to Any Output			40		50	ns
t_{ZH} / t_{ZL}	$\overline{OE}$ to Any Output			25		30	ns
t_{HZ} / t_{LZ}	$\overline{OE}$ to Any Output			25		30	ns

DEFINITION OF FUNCTIONAL TERMS

I_0, I_1, I_2, I_3 The four instruction inputs to the Am29811A.

TEST The condition code input to the device. When the test input is LOW, the device assumes the test has failed. When the test input is HIGH, the device assumes the condition code required has been met; the test has passed.

$\overline{\text{Counter Load}}$ This output is used to drive the parallel load input of an Am25LS169 up/down counter.

$\overline{\text{Counter Enable}}$ This output is used to drive the counter enable input of an Am25LS169 up/down counter.

$\overline{\text{Map Enable}}$ This output is used to control the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.

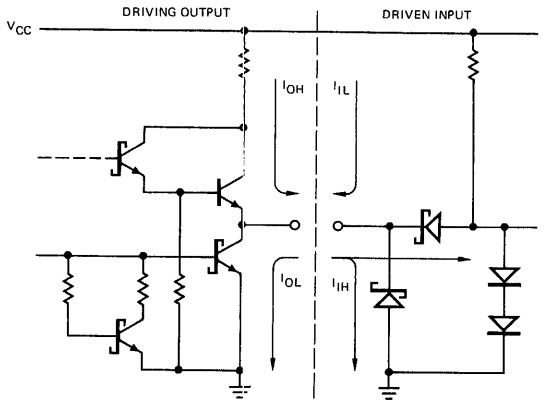
$\overline{\text{Pipeline Enable}}$ This output is used to control the three-state output of the pipeline register (Am2918) containing the branch address for the computer control unit.

$\overline{\text{FE}}$ File Enable This output is used to drive the file enable input of the Am2911. When the file enable output is LOW, a stack operation will take place.

PUP Push/Pop. The PUP output is used to drive the push/pop input of the Am2911 Microprogram Sequencer. When the PUP output is HIGH, a push will take place when the file is enabled. When the PUP output is LOW, a pop will take place when the file is enabled.

S_0, S_1 These two outputs are used to drive the S_0 and S_1 inputs to the Am2911 Microprogram Sequencer. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-317

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	$\overline{MAP\ E}$	–	100	44	44
2	PUP	–	100	44	44
3	$\overline{FE}$	–	100	44	44
4	S_1	–	100	44	44
5	S_0	–	100	44	44
6	$\overline{CNT\ LOAD}$	–	100	44	44
7	$\overline{CNT\ E}$	–	100	44	44
8	GND	–	–	–	–
9	$\overline{PL\ E}$	–	100	44	44
10	TEST	0.5	–	–	–
11	I_0	0.5	–	–	–
12	I_1	0.5	–	–	–
13	I_2	0.5	–	–	–
14	I_3	0.5	–	–	–
15	$\overline{OE}$	–	100	44	44
16	V_{CC}	–	–	–	–

INSTRUCTION TABLE

MNEMONIC	I_3 I_2 I_1 I_0	INSTRUCTION
JZ	L L L L	Jump to Address Zero
CJS	L L L H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L L H L	Jump to Address at Mapping PROM Output.
CJP	L L H H	Conditional Jump to Address in Pipeline Register
PUSH	L H L L	Push Stack and Conditionally Load Counter
JSRP	L H L H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
CJV	L H H L	Conditional Jump to Vector Address.
JRP	L H H H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
RFCT	H L L L	Repeat Loop if Counter is not Equal to Zero.
RPCT	H L L H	Repeat Pipeline Address if Counter is not Equal to Zero.
CRTN	H L H L	Conditional Return-from-Subroutine.
CJPP	H L H H	Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H H L L	Load Counter and Continue.
LOOP	H H L H	Test End of Loop.
CONT	H H H L	Continue to Next Address.
JP	H H H H	Jump to Pipeline Register Address.

FUNCTION TABLE

MNEMONIC	INPUTS			OUTPUTS				
	INSTRUCTION I_3 I_2 I_1 I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	LL*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW
H = HIGH
X = Don't Care

DEC = Decrement
*LL = Special Case

TRUTH TABLE

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER			
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	$\overline{LOAD}$	$\overline{EN}$	$\overline{MAP\ E}$	$\overline{PL\ E}$
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

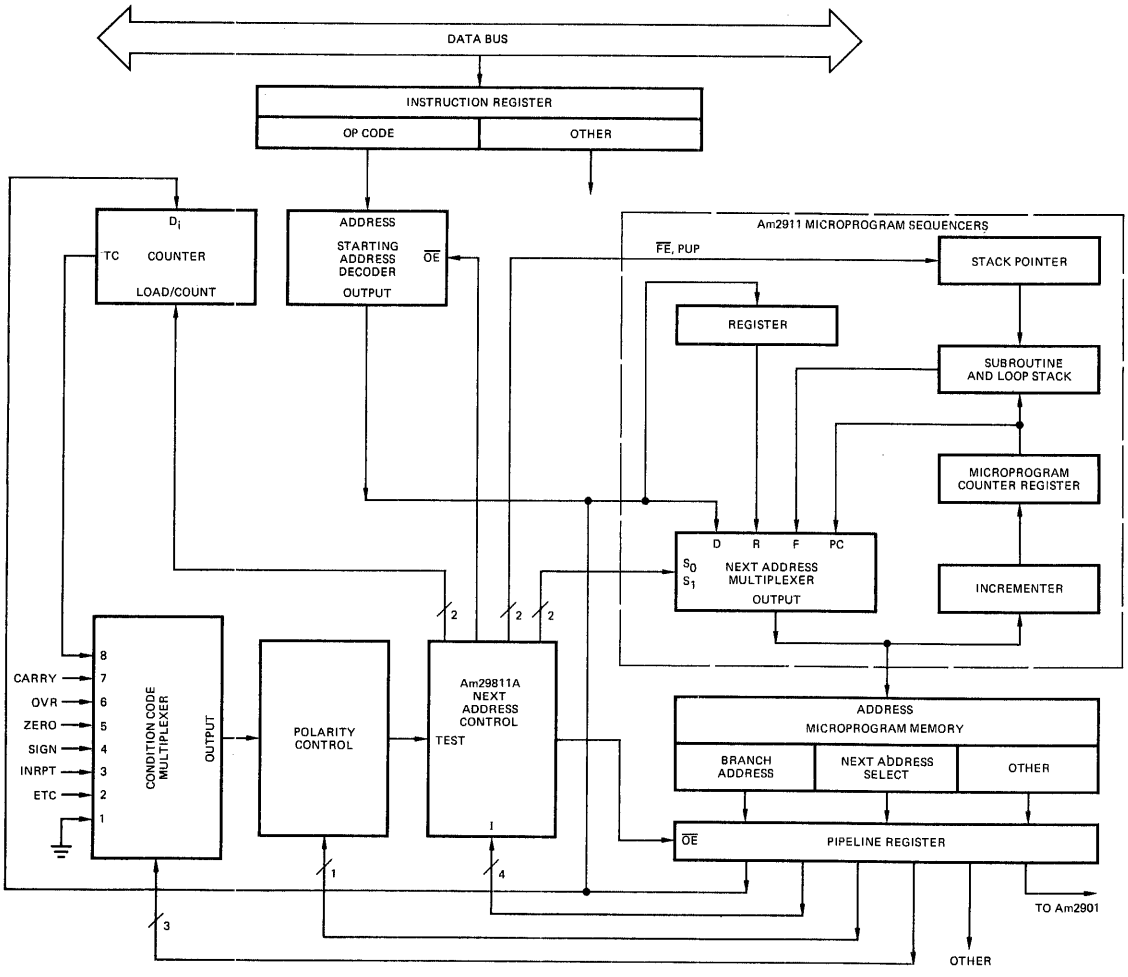
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29811APC	P-16	C	C-1
AM29811ADC	D-16	C	C-1
AM29811ADC-B	D-16	C	B-1
AM29811ADM	D-16	M	C-3
AM29811ADM-B	D-16	M	B-3
AM29811AFM	F-16	M	C-3
AM29811AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A Typical Computer Control Unit Using the Am2911 and Am29811A.

MPR-318

Am2900 Family Applications Literature

Build an Am2900 Microcomputer

This comprehensive book discusses in detail the design of a microprogrammed computer using the 2900 Family. Examples are used extensively. The book's chapters:

I – Computer Architecture
II – Microprogrammed Design
III – The Data Path
IV – The Data Path, Part Two
V – Program Control Unit
VI – Interrupt
VII – Direct Memory Access
VIII – The Hex 29
IX – The Super Sixteen

Order AM-PUB073-X

A High Performance Disc Controller

This book covers the detailed design of a controller. Specifically it is an interface between a Pertec disc and a DEC PDP-11® minicomputer. Most controllers will be architecturally similar. Includes schematics and microcode.

Order AM-PUB065 Price $5.00

An Emulation of the Am9080A

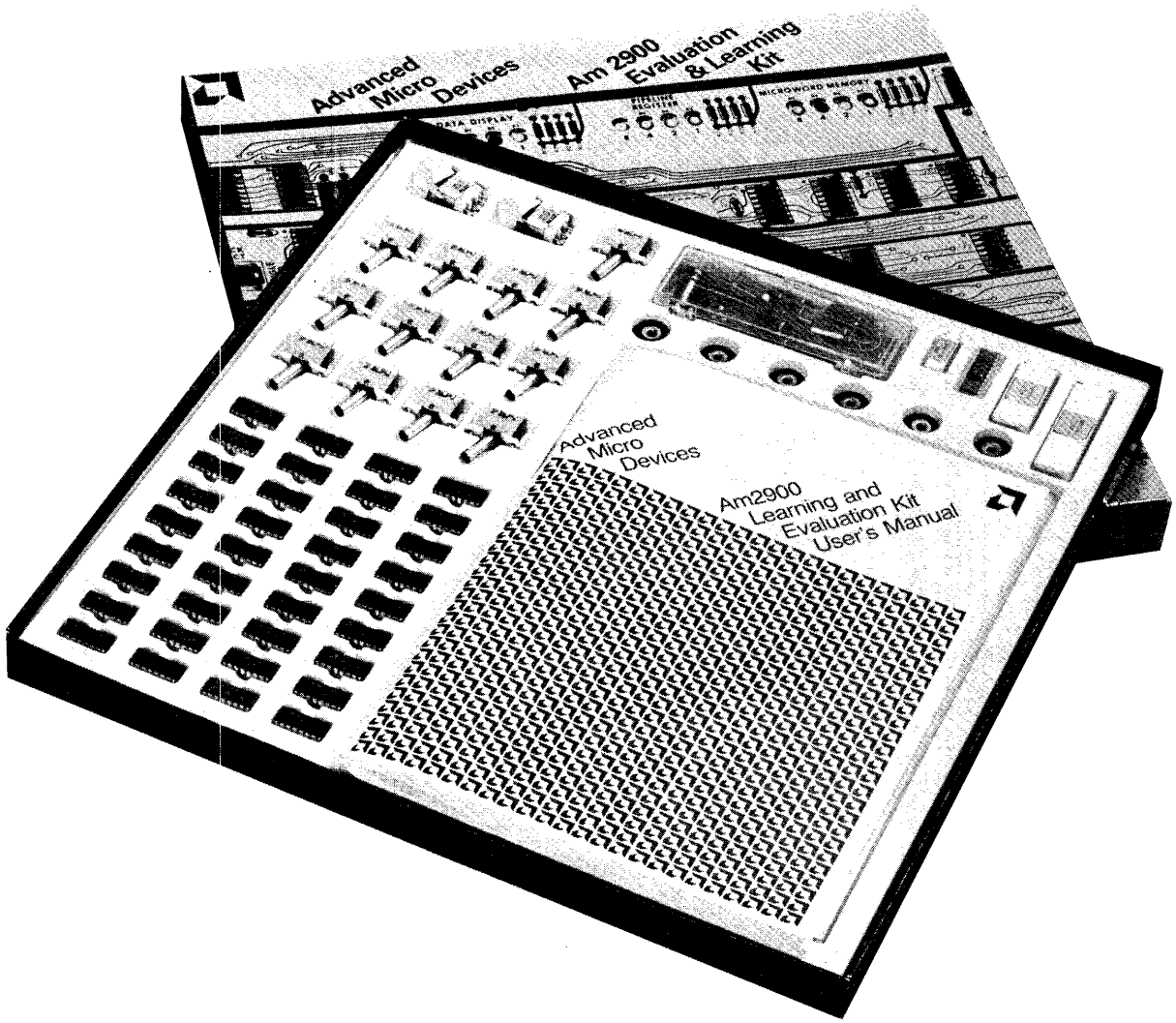
This book describes a 2900 based system which executes instructions of the Am9080A MOS microprocessor. It operates about 4 times faster than the Am9080A and leaves space for user defined instructions in addition to the standard instruction set.

Order AM-PUB064 Price $5.00

Microprogram Design with the Am2900 Family

A discussion of the "instruction-cracking" problem in microprogrammed machines. Discusses ways to translate op codes into microprogram addresses and control lines.

Order AM-PUB069 Free


Advanced
Micro
Devices
Am 2900
Evaluation
& Learning
Kit
Advanced
Micro
Devices
Am2900
Learning and
Evaluation Kit
User's Manual

THE Am2900 EVALUATION AND LEARNING KIT

Pictured at the left is the Am2900 Evaluation Kit. The system consists of a microprogrammed control unit which controls all the inputs to an Am2901 microprocessor slice. Thirty-two bit microinstructions are entered into a RAM in the control unit using the switch register. Each microinstruction contains bits to control the Am2901A's A and B addresses, instruction, carry in, and data input. Additional bits in the microinstruction control an Am2909 sequencer which generates the addresses for the microprogram memory. Once entered, microinstructions may be executed using a single step clock or using a pulse generator. The LED display provides access to nearly every signal path in the system.

Sixteen "sequence control" instructions are available, including execute, branch conditional, jump-to-subroutine, return, and loop. Because the set of sequence instructions is implemented in a PROM, the user can devise his own set of operations by programming a new PROM.

The kit is supplied with 40 IC's, all resistors, capacitors, LED's and switches, the PC board, and a manual containing assembly instructions, theory and a set of exercises. The user need only solder the components in place and attach a 5 V power supply (2.0 ampere rating).

Working with the kit, the user will gain familiarity with a high performance pipelined microprogrammed architecture, and with the operation of the Am2909 and Am2901A. By driving the kit from a pulse generator, the user can observe the operation of the components in real time, executing real instructions.

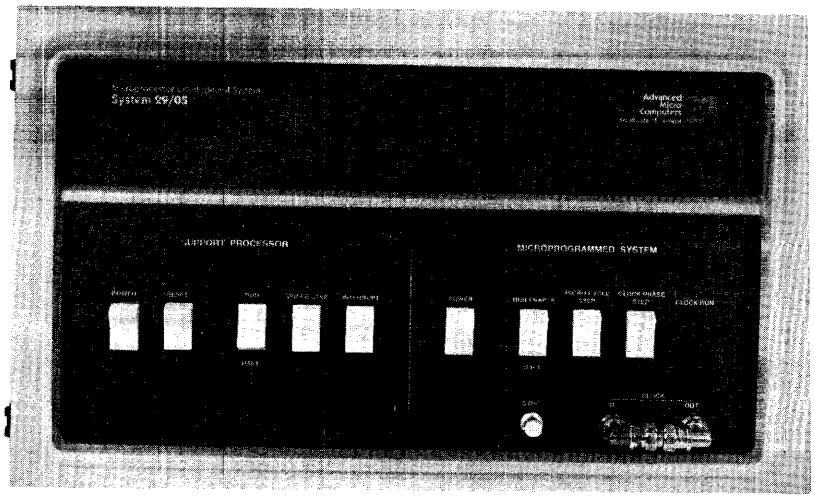
The part number for this kit is Am2900K1.

System 29

The Advanced Microprogram Development System

FEATURES

- **The first universal, complete development system for microprogrammed machines.**
  Use to assemble microcode, debug microcode, check out hardware.
- **AMDASM® 29 microassembler resident on system.**
  Microprograms can be written, assembled, and loaded into the development hardware all on one system. No transferring from one system to another. No messy paper tape.
- **Software to check out microcode.**
  All the tools needed in a useful development system including single step, trap, edit.
- **Writable Control Store up to 4K words.**
  RAM in System 29 serves as control memory for prototype. Expandable up to 4K words, up to 128 bits each. Access time down to 50ns.
- **Application Cards Available.**
  Pre-built prototype systems reduce design time, get products out sooner.
- **Universal Prototyping cards**
  Use popular SBC-80 form factor and hold parts on 0.3", 0.4", and 0.6" centers.
- **Time proven disk operating system.**
  Complete file management including a context editor.
- **8080 software development tools.**



SOFTWARE FEATURES

- The convenience of the AMDOS® 29 Disk Operating System with a full set of file management commands, including and editor.
- Microprogram generation software including the AMDASM® 29 micro-assembler and the AMSCRM® 29 and AMPROM® 29 post-processing programs.
- Microprogram support software to load, save, and debug microcode during the firmware/hardware check-out phase.
- Am9080A software to write special programs to add to the existing software or for separate designs using the Am9080A fixed-instruction-set micro-processor.

HARDWARE FEATURES

- Writable Control Store for microprogram memory and ROM simulation. Its storage capacity can be easily expanded and a high speed option permits real-time testing.
- Microcode check-out functions let the user interact freely with the microcode, i.e., display, modify, move, locate, store, and verify. The user can also single-step through instructions, set trap bits, set comparison values, and force address jumps for easy test and debug of the microcode and its associated hardware. These are combined hardware-software features which are accessible either at the CRT Console or the System Mainframe front panel.
- Universal Prototyping Cards feature high packing density. They accept the user prototype and plug right into System 29.
- The Outboard Interface cable interfaces System 29 to the user design for a form factor that calls for an outboard configuration.
- A number of application cards help the user in his microprogrammed system design.
- Developed microcode can be stored on flexible diskettes, printed out, punched on paper tape or used to drive a PROM programmer.
- Diskette to main memory data transfers are affected by direct memory access (DMA) without I/O port addressing. This results in high-speed data transfers.
- An internal 2.457MHz crystal-controlled clock oscillator is provided. An external connector is available for providing a different clock frequency from a signal generator or an external circuit to meet individual user requirements.

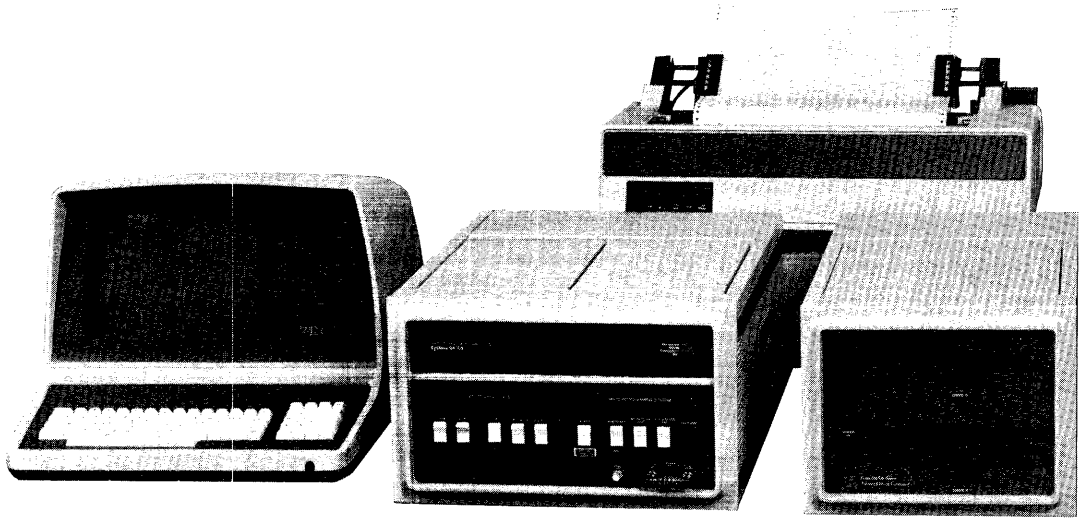
System 29

DESCRIPTION:

System 29 is a complete development system. It encompasses all the tools needed, from microcode/firmware definition, assembly, check-out of the hardware and formatting of the microcode, through programming PROM's.

System 29 includes a System Mainframe, CRT Console, and Dual-Drive Flexible Disk. It comes with a comprehensive software package. It is ready to operate in its basic configuration which includes 2K words by 64 bits Writeable Control Store and a Computer Control Unit (CCU) microprogram controller. A number of peripherals (line printer, paper tape reader-punch, PROM programmer) and cards (high-speed Writeable Control Store, trace analyzer, 8080 emulator application card, 16-bit microcomputer application card) enhance its performance even further.

Because it is controlled by an Am9080A, it can also serve as a software development system for the 8080 fixed-instruction-set microprocessors.



SYSTEM DESCRIPTION

BASIC SYSTEM:

A complete working system including;

Equipment

- System Mainframe:
  - Support Processor:
    - Am9080A CPU Card
    - System Memory Card, 32K bytes, expandable to 64K bytes with an additional card
    - 4 Serial Ports (RS232)
    - 1 Parallel Port
    - Power Supply
  - Microprogrammed System:
    - 1 Writeable Control Store Card, 2K x 64 bits. System is pre-wired for 2.
    - 1 Instrumentation Card
    - 1 Computer Control Unit Application Card
    - 5 Open Slots for Additional User Cards
    - 1 Power Supply, +5V, 25A (50A Optional)
- CRT Console
- Dual Drive Flexible Disk
- Universal Prototyping Card
- Outboard Interface Cable
- Blank Diskettes (2)

Software

- AMDOS 29® Disk Operating System with full set of commands
- Microprogram Generation Software
  - AMDASM 29® Microprogram Assembler
  - AMSCRM 29®, AMPROM 29® Post-Processing Programs
- Microprogram Support Software
- Am9080A Software (Assembler, Loader, Dynamic Debugger including disassembler and trace capability)

Documentation (2 sets)

- User Manual
- Software Manual
- Hardware Manual

Services

- User Training (2 Persons)
- Field Applications Support
- Warranty: 1 Year (90 days on System Mainframe Plug-in Cards)

SYSTEM OPTIONS[1]

CARDS[2]

Option No.

0100 *Universal Prototying card,* additional to one included in the basic system.

0105 *Writable Control Store card.* 2K x 64 bits, additional to one included in the basic system. Field updatable.

0106 *High Speed Writable Control Store card,* 1K x 64 bits; system is pre-wired for 2. Field updatable.

PERIPHERALS

0503 *Character Printer,* 120 CPS.

0510 *Paper Tape Reader-Punch*[3]. 300cps read, 75cps punch.

SERVICES

0800 *Training Course.* System 29, for one additional person. Training for 2 persons included in the basic system.

MISCELLANEOUS

0900 *High Speed Extender card,* multilayer (internal ground plane)

0901 *Power Supply,* 50A Module. Field updatable

0902 *Diskettes.* Package of 10 blanks[4].

0903 *System Manual.* One set of manuals, additional to 2 provided with the basic system.[4]

NOTES:

1. SY29XXXX – When coding orders, replace X's with 4 digit option number, leave blank for basic system. Example: SY290500 is code for the Line Printer option.
2. Warranty 90 days, parts and labor.
3. Warranty 120 days, parts and labor.
4. Quantity 2 minimum when purchased separately.

The Unique Microprocessor Lab For Your Microprogrammed Designs

Why?

The "microprogrammable" microprocessor—like the Am2900 family—offers higher performance and versatility than the "fixed-instruction-set" microprocessor—like the Am9080 family. However, this versatility makes the design of microprogrammed machines more difficult. To start with, the engineer must design his own set of particular instructions before he can write application software. He also customizes the architecture of his special purpose processor. It is this versatility which optimizes performance and, at the same time, complicates the design process—because every design is different.

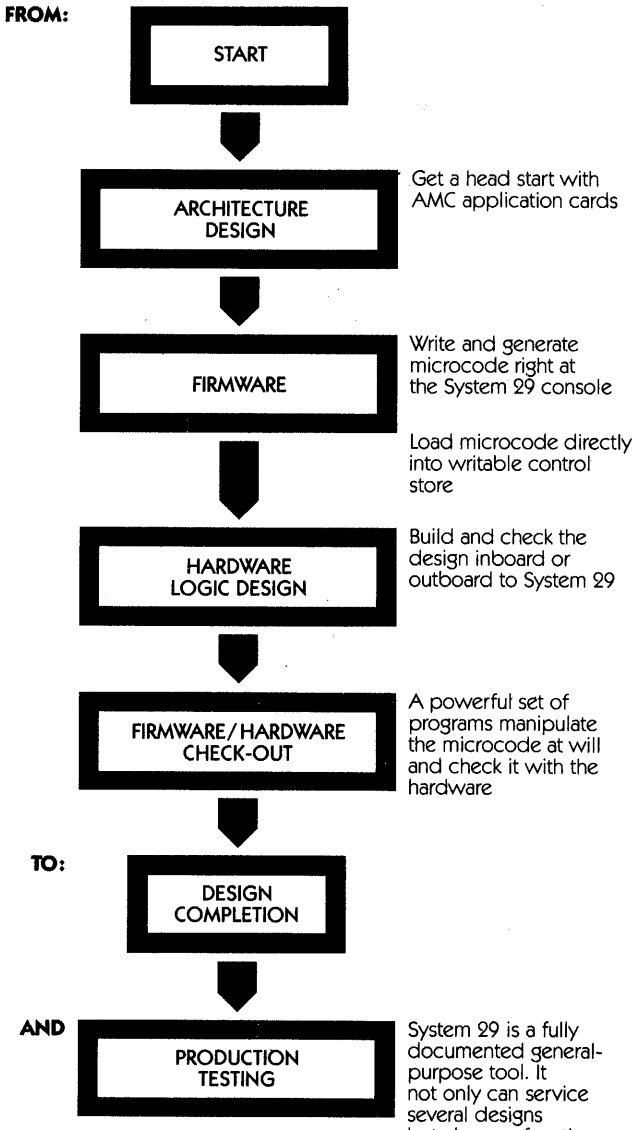
Since each design is different, hardware prototyping and microcode development tend to be an ad hoc process with little of the work expended on one design transferable to the next.

Until now, no single tool had been available to assist in the complete development of microprogrammed machines. Before the engineer could even start with his design, he had to locate a computing facility to assemble the microcode, come up with some type of PROM simulator (i.e., a dedicated mini with writable control store), assemble special test fixtures to control the system parameters of a given architecture, develop special programs to manipulate the microcode in the PROM simulator. Then, he had to generate the microcode with a microprogram assembler that probably required modification. All this meant delay and expense.

Microprogramming had to be made easier.

Advanced Micro Computers now offers a cost effective solution with System 29, the Advanced Microprogramming Development System.

Read about its contribution from the start to finish of your microprogrammed design. Find out how it can significantly reduce your design time and then be used to either follow your new product through production or start immediately on your next design. And how it offers much more than a mere technical solution. Read why it is "an investment that pays for itself."



From firmware generation...

The convenience of a disk operating system...

Once the microprogrammed design architecture is set, the next step is the generation of the microcode. System 29 provides the tools.

- ☐ The AMDOS® 29 Disk Operating System provides complete file management for a Dual Flexible Disk System.
- ☐ Each flexible disk has **ample storage** (240K bytes) for long programs.
- ☐ A powerful **text editor** is used to create and modify microprogram source files.
- ☐ A number of other **utility programs** makes it easy to manipulate the code from one peripheral format to another, process various commands in batch mode, provide information about any file on the disk, etc....
- ☐ A **CRT Console** lets the user interact with the system. An optional high-speed line printer provides permanent hardcopy which is helpful during the firmware development phase.

...And a powerful resident micro-assembler...

Microcode can be written in symbolic language and assembled right on System 29 with AMDASM® 29. AMDASM 29 is a powerful assembler that is easily "personalized" to match the microformat. Its output is readily loadable into the Writable Control Store which is supplied with System 29 to simulate the microprogram PROM's in the user system.

...Provide all the software tools for firmware generation.

By writing individual programs for the Support Processor, the designer can add to System 29's already powerful set of commands and customize System 29 for particular needs.

Get a head start with a number of AMC application cards

They work from day one and provide the general-purpose functions that get microprogrammed designs off the ground and let designers concentrate on their specific application. The Computer Control Unit (CCU) is an example.

You have all the tools for checking your logic design

Sit down and write simple diagnostic programs to verify that prototyping circuits perform the way they are intended to.

...to hardware design

Build your microprogrammed system inboard or outboard to System 29

System 29 is accommodating. It has five card slots dedicated to the user prototype complete with a power supply to drive them. If an outboard configuration is preferred, it allows easy connection to its development functions.

Take advantage of the universal card format

The Universal Prototyping Card is compatible with the SBC-80 format which is rapidly becoming the industry standard. It offers high packing density and easy interface to both System 29 controls and other circuits. System 29 can host enough cards for any design.

...and the integration of both

Versatile microprogram memory is the key to firmware generation and hardware check-out.

- ☐ **Writable Control Store** (WCS) is where it all happens since it serves the vital function of microprogram memory and ROM simulation. Microprograms can easily be loaded into it after assembly and initial debug. Many features (such as automatic assembly of the modified portion of the microprogram) are available to conveniently manipulate the microcode at any time. The storage capacity can be easily expanded and a high-speed option permits real-time operation of your design.
- ☐ **Microcode Check-Out Functions**—Once the microprogram is assembled, System 29 knows the battle is only half over. Firmware and hardware can be integrated right at the CRT Console.

  A powerful set of programs lets the user display, move, locate, store and verify the microcode at will.

  Single-step through instructions, set traps, loop around sections of code, execute microcode until a specific address is reached, then execute some special code (i.e., to display the content of some registers).

  Single Level Trace allows monitoring of 20 test points connected anywhere in the user's prototype.

  A Logic Analyzer option allows monitoring of 64 test points in real-time and displays the last 256 states on the CRT Console.
- ☐ **Microcode Output in a Directly Usable Format**—When the microcode is debugged, the System 29 Reader/Punch option will output a paper tape directly usable on most commercially available PROM programmers. Alternatively, an optional PROM programmer can be driven directly from System 29.

An 8080 software development capability is also included

Because System 29 is controlled by an Am9080A* based Support Processor, a complete software package is available to generate programs for other designs with the widely used Am9080A/8080 fixed-instruction-set microprocessor.

The tools include an assembler, a debugger complete with a disassembler, and a loader.

This capability adds to the universality of System 29 and is another factor to justify its use for microprocessor development.

*The Am9080A is a high-speed, pin-compatible version of the 8080A.

3

The hardware

The **System Mainframe** is divided into a Support Processor section and a Microprogrammed System section. The **Support Processor** is a microcomputer built around the Am9080A MOS fixed-instruction-set microprocessor and a 32K RAM System Memory. It controls all input/output communications with the user via the peripherals. It executes programs called from the CRT Console and provides all the necessary controls to the Microprogrammed System.

The **Microprogrammed System** interfaces to microprogrammed designs. It has the ability to house these circuits on a number of Universal Prototyping Cards. It can also interface to outboard designs, located outside the System Mainframe. The Microprogrammed System section also houses the Writable Control Store (WCS) Card(s), the Instrumentation Card, and the Computer Control Unit (CCU) card.

- **Writable Control Store.** The basic WCS configuration is easily expanded, by the addition of a second pre-wired card, from 2K by 64 bits to 4K by 64 bits or 2K by 128 bits. Additional WCS Cards can be accommodated, if necessary. Two optional high-speed WCS Cards (1K by 64 bits each), make it possible to achieve speeds similar to that of final designs.
- **The Instrumentation Card** includes the functions of clock control as well as microprogram address trap and branch control.

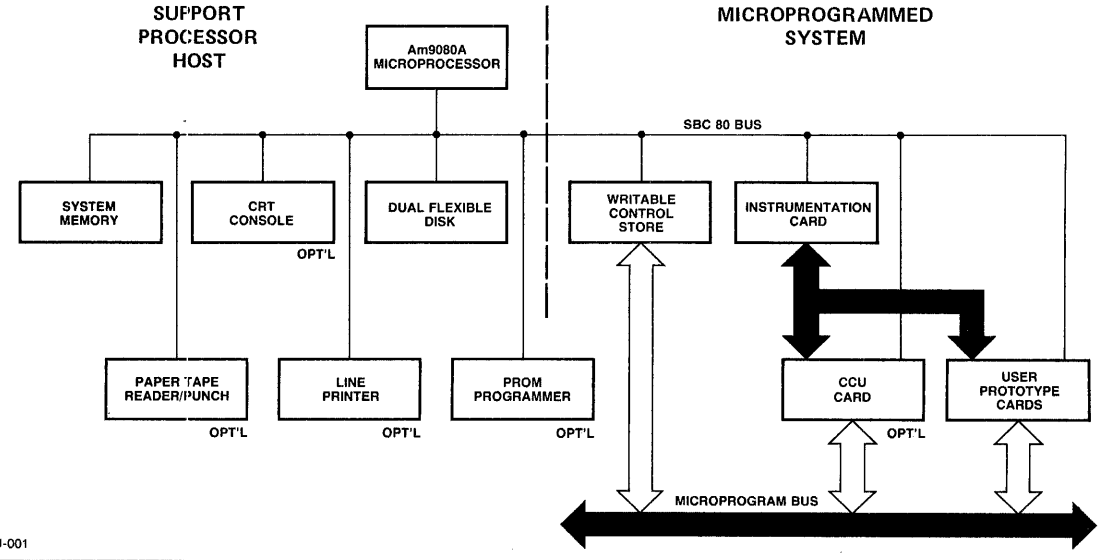
  Stop, single-step, or run can be activated from commands at the CRT console or buttons at the mainframe front panel.

  Stop or breakpoint on an address, or sequence of addresses, input from the keyboard. System 29 will stop the microprogram when the input address matches the microprogram address provided to WCS. Inputing a sequence of addresses, allows isolation of a particular combination of microcode.

  Branch or force a particular address onto the microprogram for one microcycle. For example, this allows branching to a special diagnostic subroutine or an alternate microprogram subroutine you may want to activate.

  Monitor in real-time some 64 test points (an option to System 29). Define these test points, i.e., the microword, the output of the ALU, the CPU-to-memory bus, designators, etc. They are saved at the clock frequency (or some selectable fraction or multiple of it). When the clock is stopped, some 256 steps can be displayed in a convenient format to help trace what actually happened, step-by-step.

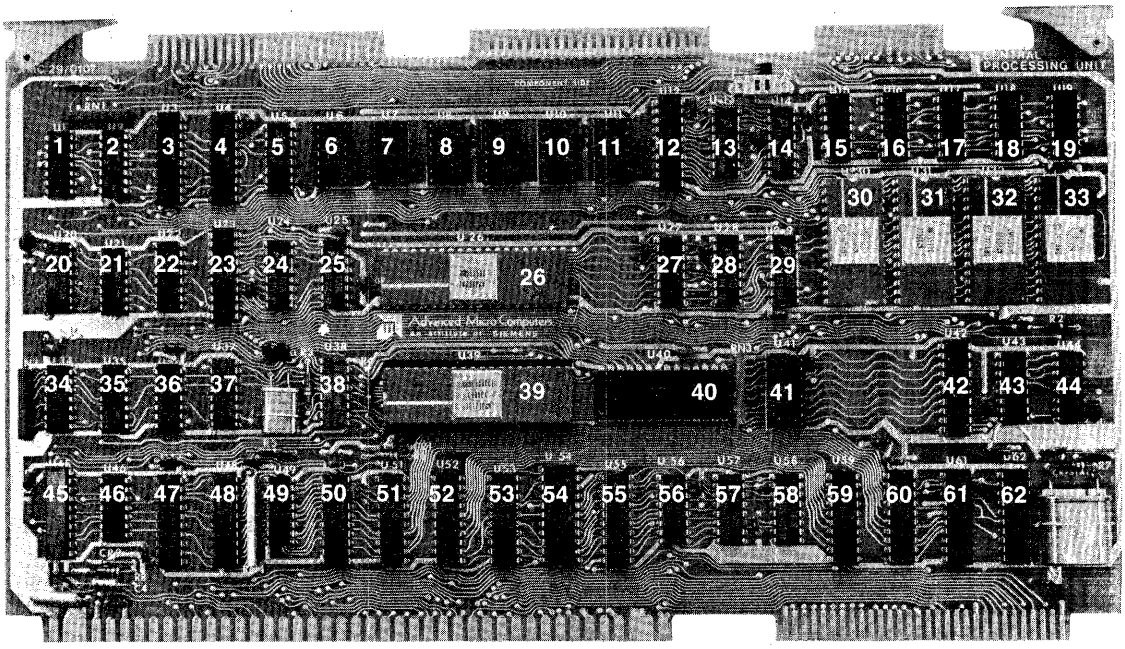
  The standard configuration allows the user to monitor in snapshot fashion (stop the clock and interrogate) some 20 test points and up to 12 microprogram address bits.
- **Application Card.** The CCU Card is an application card available from AMC to expand the capabilities of System 29. It is a pipelined microprogram sequencing unit designed around the Am2911 Microprogram Controller.
- The **Universal Prototyping Card** has space for over 100 16-pin DIP's. It holds wire-wrapped dual-in-line sockets with pin centers of 0.3, 0.4, 0.6, 0.7, and 0.9 inches. It is prewired for Vcc and ground on each side respectively.
- **Power Supply.** The System Mainframe includes a separate +5 volt, 25 amp (50 amp optional) power supply to support any bipolar circuits mounted on inboard Universal Prototyping Cards. Therefore, a totally self-contained microprogrammed system can be designed.
- The **Peripherals** include a CRT Console and a Dual Flexible Disk for the basic configuration. Optional peripherals include a Line Printer, a Paper Tape Reader/Punch, and a PROM programmer.



System 29
LOGIC CARD SET

THE HEART OF SYSTEM 29 IS AMD'S POWERFUL Am9080 MICROCOMPUTER WHICH FEATURES:

- **Am9080 MICROPROCESSOR** — Compatible with Intel 8080
- **FOUR SERIAL I/O CHANNELS** — 9600, 9600, 600, 110 bauds
- **THREE EIGHT-BIT PARALLEL I/O PORTS** — Am9555
- **CRT CONSOLE INTERFACE** — RS232 – 9600 baud
- **PAPER TAPE READER/PUNCH INTERFACE** — RS232 – 600 baud
- **PROM PROGRAMMER INTERFACE** — Data I/O Corp model 17 or 19
- **LINE PRINTER INTERFACE** — For hard copies RS232 – 9600 baud
- **DUAL DRIVE FLEXIBLE DISK INTERFACE** — 500K bytes on-line mass storage
- **32K X 8 MOS SYSTEM RAM** — Expandable up to 64K x 8 for higher level languages

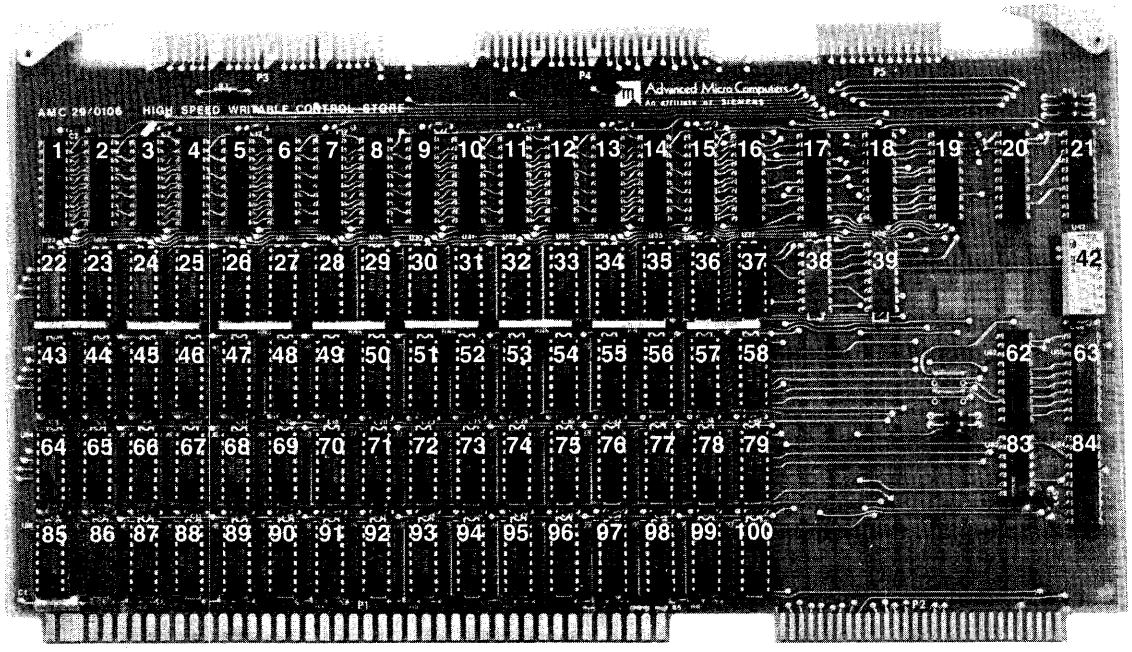


SUPPORT PROCESSOR SECTION

System 29
LOGIC CARD SET

WRITABLE CONTROL STORE – **TO STORE USER MICROCODE UNDER DEVELOPMENT**

			MAX CONFIG.
• HIGH SPEED/BIPOLAR	MAXIMUM SPEED 44nsec TYPICAL 50nsec MAX	1K X 64	4K X 64 2K X 128*
• MEDIUM SPEED	MAXIMUM CAPACITY	2K X 64	4K X 128



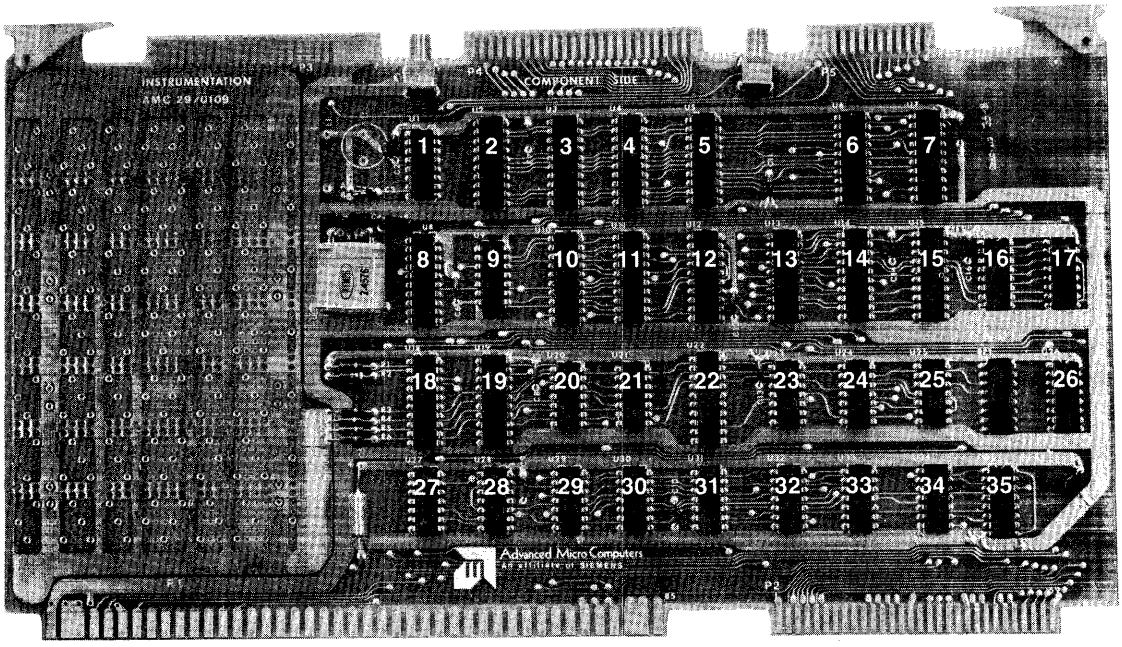
MICROPROGRAMMED SECTION

System 29
LOGIC CARD SET

INSTRUMENTATION CARD

CONTAINS ALL THE CIRCUITS TO IMPLEMENT THE DEBUGGING FEATURES

- **CLOCK GENERATION FROM OSCILLATOR**
- **CLOCK CONTROL** — Control can be entered from front panel or CRT
  HALT, RUN, SINGLE STEP, MICRO STEP, MULTIPLE MICRO STEP
  Single step = one clock cycle
  Micro step = one microinstruction
- **ADDRESS BREAKPOINT/SYNC/INTERRUPT 5**
- **ADDRESS JAMMING** — Initiate program execution at selected locations
- **KEEP TRACK OF LAST MICROPROGRAM ADDRESS**
- **KEEP TRACK OF LAST STATE OF 20 MONITOR BITS** — Can be interactively displayed at CRT
- **TRAP BITS TO CONTROL CLOCK** — Defined by user



MICROPROGRAMMED SECTION

3

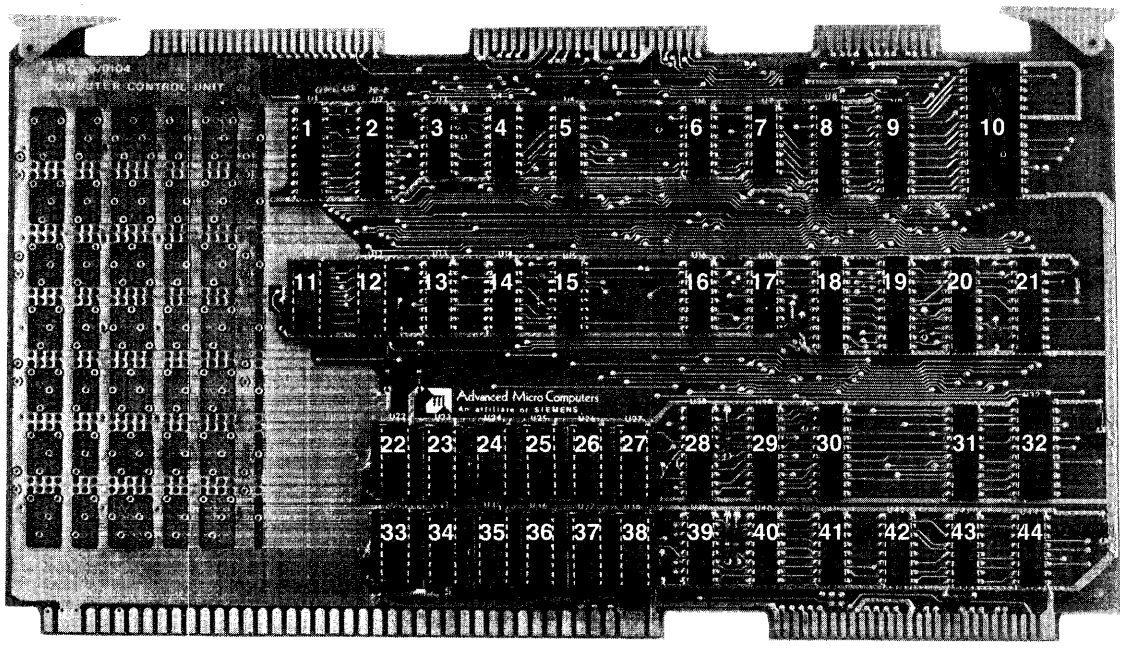
System 29
LOGIC CARD SET

COMPUTER CONTROL UNIT CARD

PROVIDES PIPELINED CONTROL FOR ADDRESS SEQUENCING AS WELL AS AN OPCODE MAP

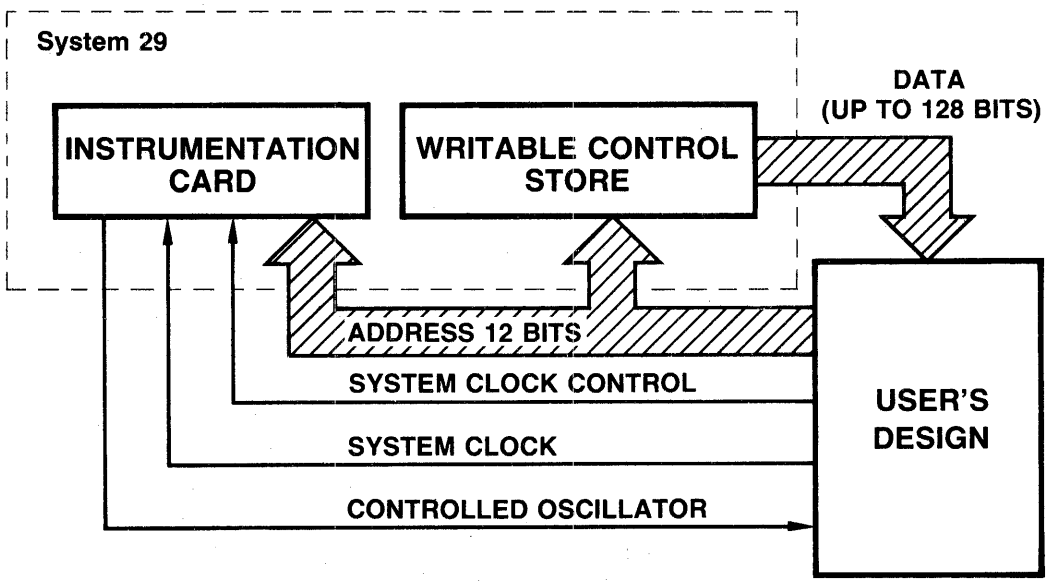
FEATURES:

- **AN EXAMPLE OF GENERAL PURPOSE MICROPROGRAM NEXT ADDRESS CONTROL**
- **SECTIONS OF PIPELINE REGISTER DEDICATED TO PRE-DEFINED MICROCODE FORMAT**
- **INTERFACE DIRECTLY TO WCS**
- **OPTIONAL USE BY USER**
- **SIMILAR TO Am2910**
- **STARTING ADDRESS MAPPING RAM (256 WORDS X 12 BITS)** — RAM can be modified easily interactively at CRT
- **VECTOR ADDRESS PROM**
- **ADDRESSES 4K WORDS OF MICROCODE WITH THREE SEQUENCERS** — For interrupts
- **NEXT ADDRESS CONTROLLER**
- **TEST CONDITION MULTIPLEXER** — One of 16 conditions can be selected for a conditional instruction
- **16-WAY BRANCH CONTROL**
- **LOOP COUNTERS**



MICROPROGRAMMED SECTION

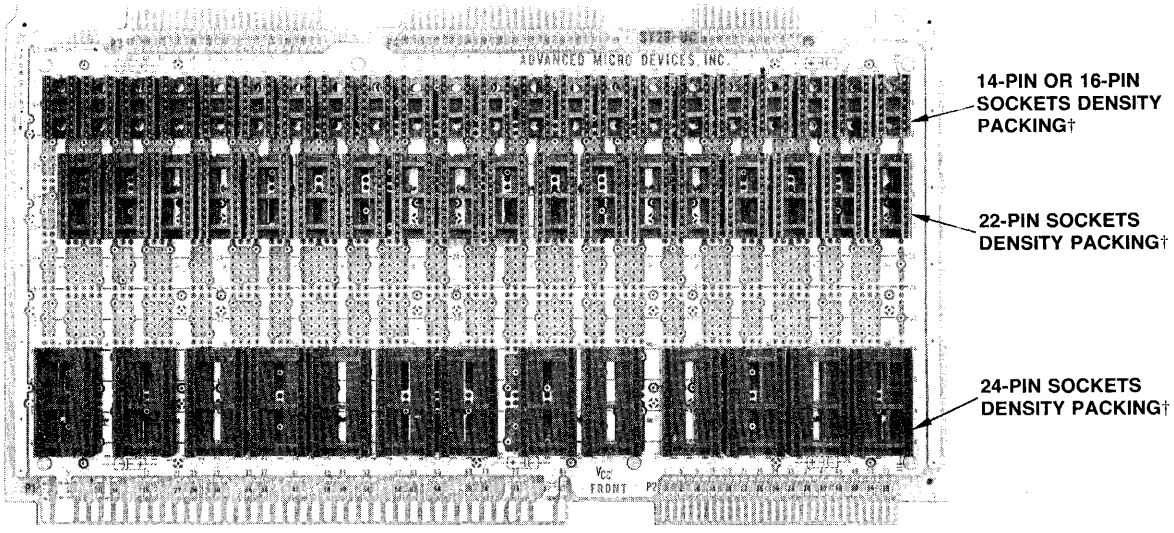
System 29
LOGIC CARD SET



Extremely simple user interface. Address bus, Data bus, and a few control lines and clock signals.

AMC-008

USER INTERFACE



UNIVERSAL PROTOTYPE CARD

†SOCKETS ARE NOT INCLUDED

System 29
SOFTWARE

A COMPLETE SOFTWARE PACKAGE COMES WITH SYSTEM 29, INCLUDING A POWERFUL ASSEMBLER, A COMPREHENSIVE DISK OPERATING SYSTEM, AND MICROCODE DEBUG PROGRAMS.

AMDOS 29, the Disk Operating System, performs file management of programs on the Flexible Disk and all I/O routines required for peripheral communications. It supports a named file system with up to 64 distinct files on each flexible disk. Each file can contain up to 240K bytes. Sequential and random access are provided. A table summary of its commands is shown below.

Built-in Commands

TYPE Displays the contents of a file at the CRT Console.

DIR Directory: Displays file name and file type of all files present on a disk.

REN Rename: Changes a file name.

ERA Erases a given file or set of files from the disk.

SAVE Saves a portion of System Memory (RAM) on the disk as a named file.

Transient Commands

ED The **Editor** allows preparation of programs and text using powerful context editing and display commands.

PIP Peripheral Interchange Program allows transfer of files between various peripherals and disk files.

Examples:
-Copy file from disk drive A to B.
-Output any disk file to the CRT Console or Printer.
-Read a paper tape onto disk.
-Copy and rename a given file.
-Concatenate files.

SUBMIT Allows commands to be batched together and be executed automatically.

SET Sets up system parameters.

DUMP Prints the contents of a file in "hex" and ASCII format at the CRT Console.

SYSGEN Initializes a flexible disk with the operating system.

DISPL Displays source and list files from the disk on the CRT Console.

STAT Statistics: Lists files by name, file space used by each, remaining disk space, device assignments. Allows user to change device assignments.

Microprogram Generation Software

AMDASM® 29 A **microprogram assembler** which can be personalized by defining a particular microcode format. It will then assemble the microcode from source to object code.

AMSCRM® 29 Reorganizes the microprogram for a given PROM organization.

AMPROM® 29 Outputs the microprogram in a form suitable to a given PROM organization.

AMMAP® 29 Generates microprogram entry point addresses that are loaded into the CCU mapping RAM.

Microprogram Support Software

These programs load, save, and debug microcode during the firmware/hardware check-out phase of the design.

LBPM Loads Bipolar Memory (BPM) from disk to Writable Control Store (WCS) or Mapping RAM (MAP).

VBPM Verifies BPM—compares data in WCS or MAP with data on disk.

SBPM Saves BPM—saves on disk, the microprogram stored in WCS or MAP.

RBPM Restores BPM—reloads the saved microprogram.

DDT29 Dynamic Debugging Tool allows dynamic manipulation while running the microprogram. Commands such as TRACE, STEP, HALT, RUN, DISPLAY, MODIFY, and JUMP offer complete control over the microprogrammed processor.

Am9080A Software

This software allows the writing of programs for Am9080A fixed-instruction-set microprocessor design for the customization of System 29 by writing special programs for its Am9080A-based Support Processor.

ASM Am9080A Assembler

DDT Dynamic Debugging Tool is a monitor that allows symbolic program tracing, debugging, and testing. DDT contains a complete Am9080A Disassembler.

LOAD The loader prepares a memory image file from an assembled file, ready for direct execution.

MICROPROGRAMMING SOFTWARE GENERATION

TYPICAL DEFINITION FILE

```
;
;AM2909 NEXT MICROINSTRUCTION ADDRESS SELECT DEFINITIONS
;
CJR:     DEF     4VX,H#Ø,24X  ;JUMP REGISTER IF F Ø
JR:      DEF     4VX,H#1,24X  ;JUMP REGISTER
CONT:    DEF     4VX,H#2,24X  ;CONTINUE
JMAP:    DEF     4VX,H#3,24X  ;JUMP MAP
CJSR:    DEF     4VX,H#4,24X  ;JUMP SUBROUTINE IF F Ø
JSR:     DEF     4VX,H#5,24X  ;JUMP TO SUBROUTINE (CALL)
RTN:     DEF     4VX,H#6,24X  ;RETURN FROM SUBROUTINE
LOOP:    DEF     4VX,H#7,24X  ;FILE REFERENCE
ELPFØ:   DEF     4VX,H#8,24X  ;END LOOP & POP IF F=Ø
PUSH:    DEF     4VX,H#9,24X  ;PUSH PC AND CONTINUE
POP:     DEF     4VX,H#A,24X  ;POP AND CONTINUE
ELPCN4:  DEF     4VX,H#B,24X  ;END LOOP & POP IF CN+4
JRFØ:    DEF     4VX,H#C,24X  ;JUMP REGISTER IF F=Ø
JRF3:    DEF     4VX,H#D,24X  ;JUMP REGISTER IF F3
JROVR:   DEF     4VX,H#E,24X  ;JUMP REGISTER IF OVR
JRCN4:   DEF     4VX,H#F,24X  ;JUMP REGISTER IF CN4
;
;OTHER DEFINITIONS
;
AM2901:  DEF     9X,3VQ#1,1X,3VX,1VX,3VX,4VX,4VX,4X
DATA:    DEF     28X,4VH# ;DEF TO SUPPLY ALU DATA INPUT
```

TYPICAL MICROPROGRAM SOURCE FILE

```
AMD AMDASM MICRO ASSEMBLER, V1.Ø                          PAGE    1
AM2900 KIT EXERCISE #1Ø

      ;AMDASM EXAMPLE, ASSEMBLY PHASE
      ;
 0000          CONT   & AM2901 RAMF,DZ,,OR,,RØ & DATA H#F     ;   1
 0001          CONT   & AM2901 RAMF,DZ,,OR,,R1 & DATA 9       ;   2
 0002          CONT   & AM2901 RAMF,DZ,,OR,,R2 & DATA B#ØØØ1  ;   3
 ØØØ3          CONT   & AM2901 RAMF,DZ,,OR,,R4 & DATA 4       ;   4
 0004          PUSH   & AM2901 RAMF,ZB,,AND,,R3               ;   5
 0005 BEGIN::  CONT   & AM2901 ,DA,,AND,RØ,RØ & DATA 1        ;   6
 ØØØ6          CJSR   INCR3 & AM2901 RAMD,ZB,,OR,,RØ          ;   7
 0007          CONT   & AM2901 ,DA,,AND,R1,R1 & DATA 1        ;   8
 0008          CJSR   INCR3 & AM2901 RAMD,ZB,,OR,,R1          ;   9
 0009          CONT   & AM2901 ,DA,,AND,R2,R2 & DATA 1        ;  1Ø
 ØØØA          CJSR   INCR3 & AM2901 RAMD,ZB,,OR,,R2          ;  11
 ØØØB          CONT   & AM2901 RAMF,ZB,CNØ,SUBR,,R4           ;  12
 ØØØC          ELPFØ  & AM2901                                ;  13
 ØØØD STOP::   JR     STOP & AM2901 ,ZB,,OR,,R3               ;  14
 ØØØF          ORG    15                                      ;  15
 ØØØF INCR3::  RTN    & AM2901 RAMF,ZB,CN1,ADD,,R3            ;  16
      ;
      END
```

TYPICAL MICROPROGRAM OBJECT FILE

```
0000 XXXX0010X011X111 X011XXXX00001111
0001 XXXX0010X011X111 X011XXXX00011001
0002 XXXX0010X011X111 X011XXXX00100001
0003 XXXX0010X011X111 X011XXXX01000100
0004 XXXX1001X011X011 X100XXXX0011XXXX
0005 XXXX0010X001X101 X1000000000000001
0006 11110100X101X011 X011XXXX0000XXXX
0007 XXXX0010X001X101 X1000001000010001
0008 11110100X101X011 X011XXXX0001XXXX
0009 XXXX0010X001X101 X1000010000100001
000A 11110100X101X011 X011XXXX0010XXXX
000B XXXX0010X011X011 0001XXXX0100XXXX
000C XXXX1000X001XXXX XXXXXXXXXXXXXXXX
000D 11010001X001X011 X011XXXX0011XXXX
000F XXXX0110X011X011 1000XXXX0011XXXX
```

MICROPROGRAM CHECK-OUT SOFTWARE

MANIPULATE MICROCODE IN WCS OR MAPPING RAM

- LBPM: LOAD FROM DISK
- VBPM: VERIFY AFTER LOAD
- SBPM: SAVE ON DISK
- RBPM: RESTORE AFTER SAVE

MICROPROGRAM CHECK-OUT SOFTWARE DDT29 – A MICROCODE DEBUGGER

- MANIPULATE MICROCODE IN WCS OR MAPPING RAM
  - DISPLAY, MODIFY
- CLOCK CONTROL
  - HALT, SINGLE STEP, MICROSTEP, RUN
  - BREAKPOINT TRAP
- BRANCH CONTROL
  - ADDRESS JAMMING
- SINGLE LEVEL TRACE
  - DISPLAY 20 MONITOR BITS
- BATCH CAPABILITY

Using the System 29

System 29 is useful to the microprogrammed system designer from initial hardware/firmware design to final interface and debugging. It also provides a production test station after the design has been completed.

- ☐ **System Initialization** is as simple as pressing a front panel button. AMDOS 29 is automatically loaded from disk to RAM System Memory and System 29 is ready to work.
- ☐ **Logic Design.** Mount logic circuits on the Universal Prototyping Card which plugs directly inside the System Mainframe. Alternatively, connect an outboard design via cable interface.
  At any time you can write simple programs that will analyze the logic design, wiring errors, and component failures.
- ☐ **Microcode Generation.** Once the microcode format has been set, the AMDASM 29 assembler can be personalized. This is the Definition Phase. System 29 acts as an interactive CRT Console as the Editor is used to build the Definition File. The next step is to generate the microcode source files, written in mnemonic language, again using the interactive Editor. The assembly process then turns these source files into object files, i.e., a binary representation of the microcode (1's, 0's and "don't cares"). When the assembly is completed, they are routed to disk storage.
- ☐ **Microcode Check-out.** Once the microcode (firmware) has been assembled and the logic design has been checked-out, they are ready to be interfaced, using System 29 as a check-out station. Load the microcode into Writable Control Store (microprogram memory) and begin using the System 29 features available to:
  Verify and edit microcode in WCS.
  Run, halt, and single-step the microprogram.
  Stop or breakpoint an address, or a sequence of addresses, input from the keyboard.
  Branch or force a particular address onto the microprogram for one microcycle.
  Generate and debug sequences of microcode written explicitly for hardware debugging purposes and not a permanent part of the final microcode.
  Monitor some 64 test points in real-time.
- ☐ **Firmware Post-Processing.** When microcode check-out has been completed, AMPROM 29 will output the microcode on the optional Paper Tape Punch in a format appropriate for a given PROM programmer. Alternatively, the output can be sent to an optional PROM programmer connected directly to System 29. AMSCRM 29 allows reorganization of the microinstruction fields for various PROM organizations before outputting the microcode.

Complete support

System 29 comes with complete support:

Training courses for two engineers on microprogramming techniques and the detailed use of the system; a complete documentation package; an extensive warranty and service plan for both hardware and software products after installation at your facilities; the active participation of a team of Field Application Engineers fully trained on the use of the system and the design of microprogrammed systems.

3

EXAMPLE OF System 29 DEVELOPMENT

The capabilities of SYSTEM 29 can be demonstrated by microprogramming one of the exercises from the Am2900 Learning and Evaluation Kit. This kit provides a simple but complete example of a microprogrammed system.

The architecture of the kit is shown in Figure 5-1. The dashed lines outline the two LSI components, the Am2909 microprogram sequencer and the Am2901 four-bit slice microprocessor. Each microinstruction in the microprogram memory consists of 32 bits divided into fields to control the sequencer, branch address, shift multiplexers, and all the inputs to the Am2901. The fields and their functions are defined in Figure 5-2.

The first step in using SYSTEM 29 is the creation of a set of definitions which reflect the hardware on which the microprogram will run. The statements in Figure 5-3 completely define, mnemonically, the fields in the kit. That is, they implement exactly the fields and their functions for the microprocessor architecture defined in Figure 5-1, and so may be used in writing all microprograms that are to operate in this architecture. Figure 5-4 shows a flow chart of the program to be written. Figure 5-5 is the SYSTEM 29 output in Block format.

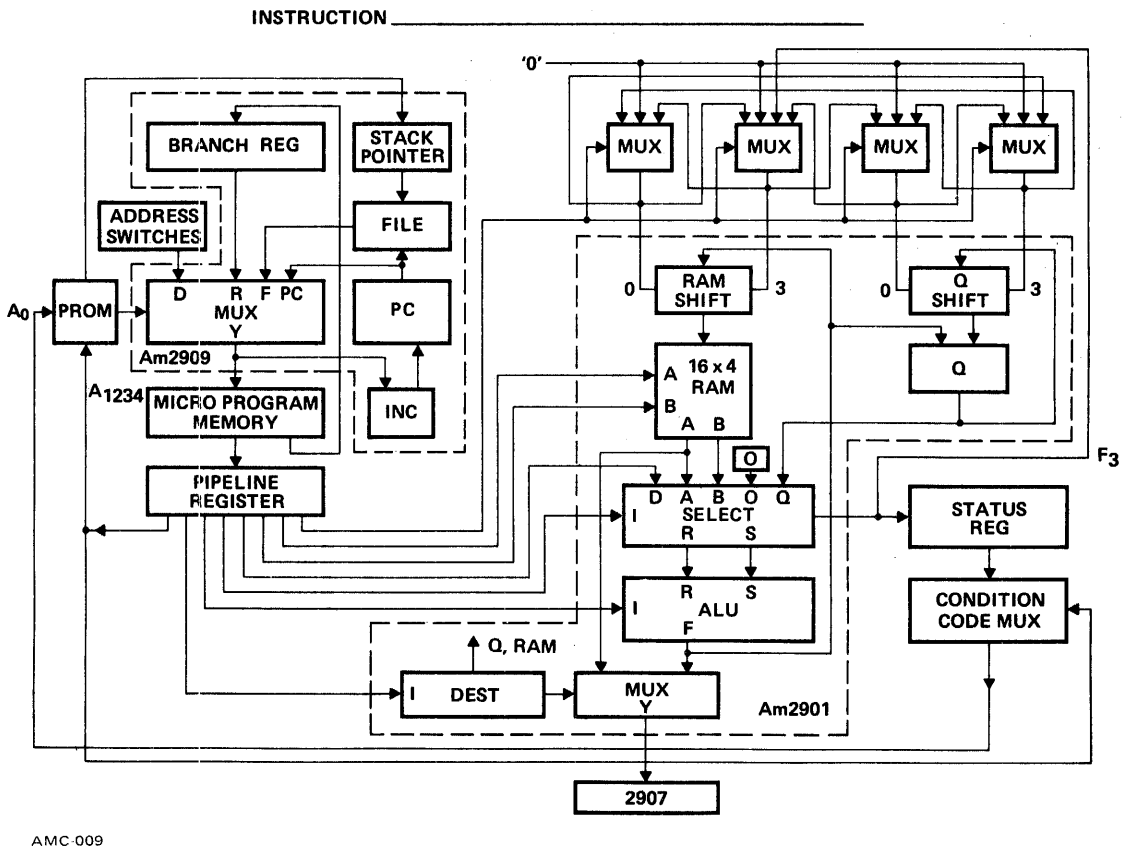


Figure 5-1. Am2900 Learning and Evaluation Kit Architecture.

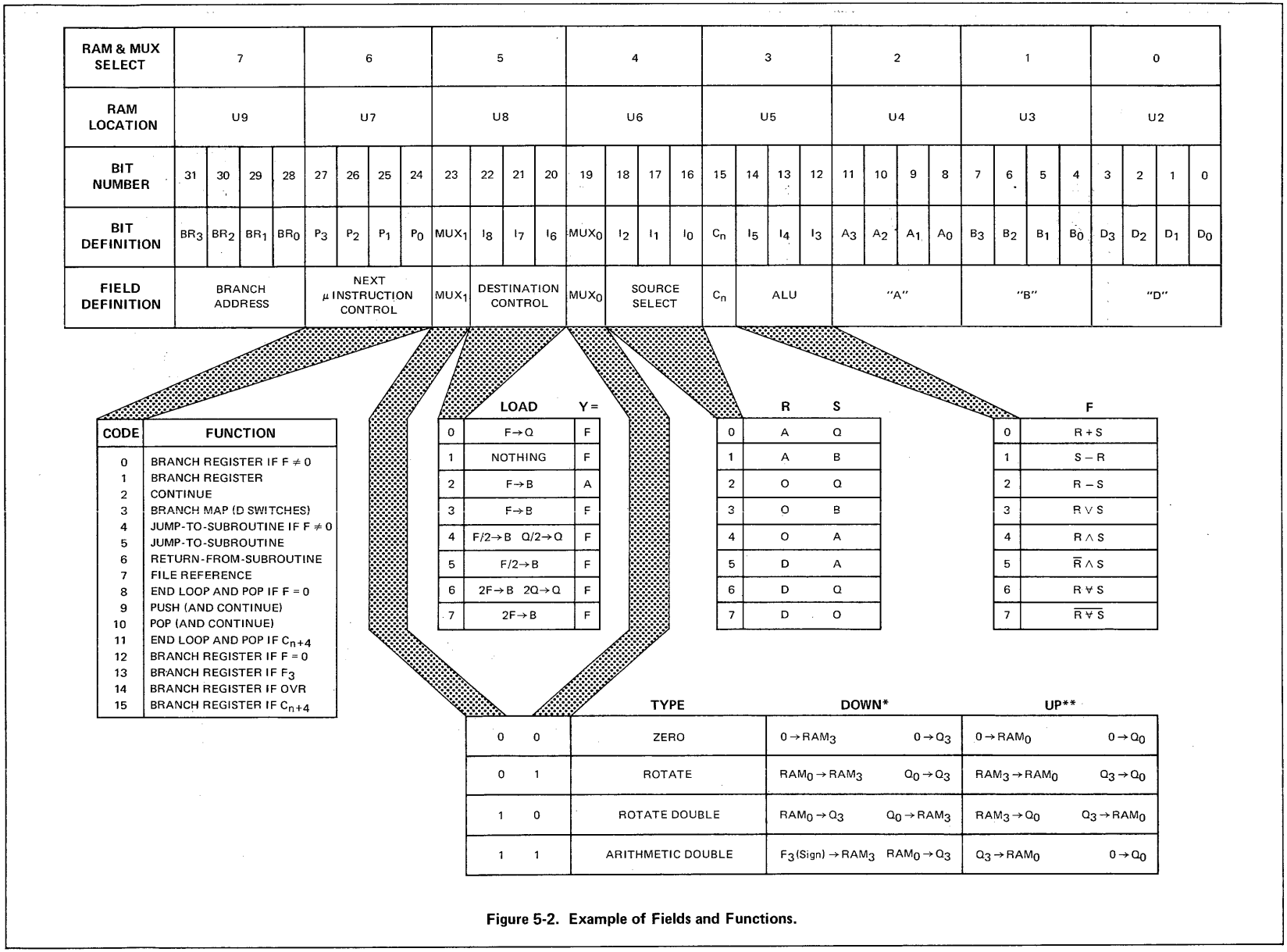


Figure 5-2. Example of Fields and Functions.

```
TITLE AM2900 KIT DEFINITIONS

WORD 32

;REGISTER DEFINITIONS

R0:  EQU H#0
R1:  EQU H#1
R2:  EQU H#2
R3:  EQU H#3
R4:  EQU H#4
R5:  EQU H#5
R6:  EQU H#6
R7:  EQU H#7
R8:  EQU H#8
R9:  EQU H#9
R10: EQU H#A
R11: EQU H#B
R12: EQU H#C
R13: EQU H#D
R14: EQU H#E
R15: EQU H#F

;AM2901 SOURCE OPERANDS (R S)

AQ: EQU Q#0
AB: EQU Q#1
ZQ: EQU Q#2
ZB: EQU Q#3
ZA: EQU Q#4
DA: EQU Q#5
DQ: EQU Q#6
DZ: EQU Q#7

;AM2901 ALU FUNCTIONS (R FUNCTION S)

ADD:   EQU O#0
SUBR:  EQU O#1
SUBS:  EQU O#2
OR:    EQU O#3
AND:   EQU O#4
NOTRS: EQU O#5
EXOR:  EQU O#6
EXNOR: EQU O#7

;AM2901 DESTINATION CONTROL

QREG:  EQU D#0
NOP:   EQU D#1
RAMA:  EQU D#2
RAMF:  EQU D#3
RAMQD: EQU D#4
RAMD:  EQU D#5
RAMQU: EQU D#6
RAMU:  EQU D#7

;SHIFT MATRIX CONTROL

SHIFT:   DEF 8X,B#0,3X,B#0,19X
ROTATE:  DEF 8X,B#0,3X,B#1,19X
DBLROT:  DEF 8X,B#1,3X,B#0,19X
ARITH:   DEF 8X,B#1,3X,B#1,19X

;NEXT MICROINSTRUCTION ADDRESS SELECT

BRFNO:     EQU H#0 ;BRANCH REGISTER IF F NOT EQUAL TO ZERO
BR:        EQU H#1 ;BRANCH REGISTER
CONT:      EQU H#2 ;CONTINUE
BM:        EQU H#3 ;BRANCH MAP
JSRFNO:    EQU H#4 ;JUMP-TO-SUBROUTINE IF F NOT EQUAL TO ZERO
JSR:       EQU H#5 ;JUMP-TO-SUBROUTINE
RTS:       EQU H#6 ;RETURN FROM SUBROUTINE
STKREF:    EQU H#7 ;FILE REFERENCE
LOOPFNO:   EQU H#8 ;END LOOP AND POP IF F=0
PUSH:      EQU H#9 ;PUSH AND CONTINUE
POP:       EQU H#A ;POP AND CONTINUE
LOOPCOUT:  EQU H#B ;END LOOP AND POP IF CN+4
BRFEQ0:    EQU H#C ;BRANCH REGISTER IF F=0
BRF3:      EQU H#D ;BRANCH REGISTER IF F3
BROVR:     EQU H#E ;BRANCH REGISTER IF OVR
BRCOUT:    EQU H#F ;BRANCH REGISTER IF CN+4

;OTHER STUFF

CN0:  EQU B#0
CN1:  EQU B#1
LOW:  EQU B#0
HIGH: EQU B#1
ZERO: EQU B#0
ONE:  EQU B#1

AM2901: DEF 9X,3VQ#1,1X,3VX,1VX,3VX,4VX,4VX,4X
AM2909: DEF 4VX,4VH#2,24X
DIN:    DEF 28X,4VH#

END
```

"R0" to "R15" are set to hex 0 to F using the "equate" statement. The "H#" designator means the numbers following are in hex, and each digit represents 4 bits.

ALU Source operands are assigned octal values using the "equate". The "Q#" designates octal, 3 bits, per digit.

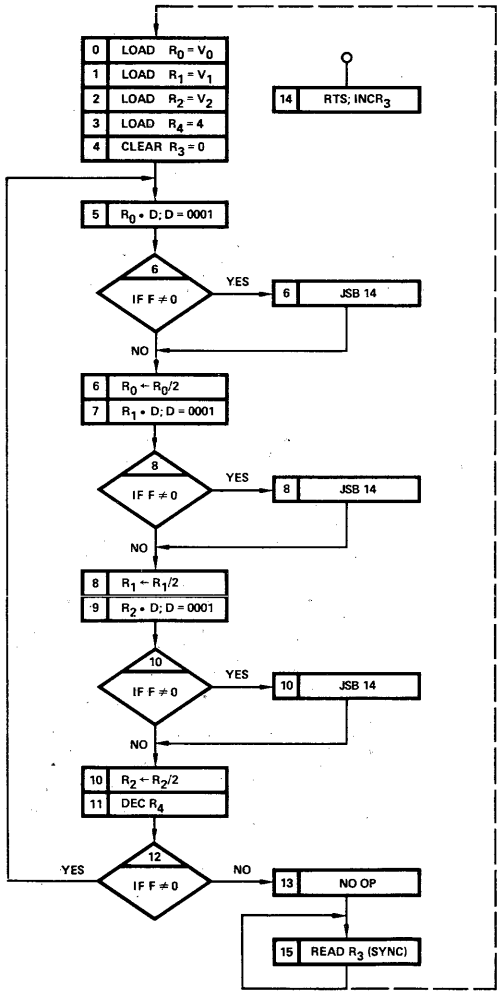
The 8 ALU functions of the AM2901 are given names.

Defines the two separated bits which control the left-right shift multiplexers. The "x's" are "don't-care" bits in between the defined bits.

Definitions for the sequence control instructions used in the second field of the microinstruction.

Format definitions are made for the ALU fields, the sequence control fields, and the data input. Formats contain don't cares (x) and variables (v). Each variable can have a default value. For example, in AM2909, the second four-bit variable defaults to hex 2, and the first four-bit variable defaults to x.

Figure 5-3. Definition File.



AMDASM29-2

Figure 5-4. Flow Chart of Example.

```
0000      AM2909 & AM2901   RAMF, DZ,,OR,,RØ & DIN H#F
0001      AM2909 & AM2901   RAMF, DZ,,OR,,R1 & DIN 9
0002      AM2909 & AM2901   RAMF, DZ,,OR,,R2 & DIN Ø
0003      AM2909 & AM2901   RAMF, DZ,,OR,,R4 & DIN 4
0004      AM2909 & AM2901   RAMF, ZB,,AND,,R3
0005 A5:  AM2909 & AM2901    ,DA,,AND,RØ,RØ & DIN 1
0006      AM2909 A14,JSRFNØ & AM2901  RAMD, ZB,,OR,,RØ
0007      AM2909 & AM2901   ,DA,,AND,R1,R1 & DIN 1
0008      AM2909 A14,JSRFNØ & AM2901  RAMD, ZB,,OR,,R1
0009      AM2909 & AM2901   ,DA,,AND,R2,R2  & DIN 1
000A      AM2909 A14,JSRFNØ & AM2901  RAMD, ZB,,OR,,R2
000B      AM2909 & AM2901  RAMF, ZB, CNØ,SUBR,,R4
000C      AM2909 A5,BRFNØ & AM2901
000D      AM2909 A15,BR & AM2901
000E A14: AM2909 ,RTS & AM2901  RAMF, ZB,CN1,ADD,,R3
000F A15: AM2909 A15,BR & AM2901   ,ZB,,OR,,R3
     END

0000 XXXX0010X011X111 X011XXXX00001111
0001 XXXX0010X011X111 X011XXXX00011001
0002 XXXX0010X011X111 X011XXXX00100000
0003 XXXX0010X011X111 X011XXXX01000100
0004 XXXX0010X011X011 X100XXXX0011XXXX
0005 XXXX0010X001X101 X100000000000001
0006 11100100X101X011 X011XXXX0000XXXX
0007 XXXX0010X001X101 X100000100010001
0008 11100100X101X011 X011XXXX0001XXXX
0009 XXXX0010X001X101 X100001000100001
000A 11100100X101X011 X011XXXX0010XXXX
000B XXXX0010X011X011 0001XXXX0100XXXX
000C 01010000X001XXXX XXXXXXXXXXXXXXXX
000D 11110001X001XXXX XXXXXXXXXXXXXXXX
000E XXXX0110X011X011 1000XXXX0011XXXX
000F 11110001X001X011 X011XXXX0011XXXX
```

Figure 5-5. Assembly Output in Block Diagram.

RESULTANT PROM SET

When a user has completed an assembly, he may wish to output his binary object code in a form which corresponds with his PROMs' organization and/or he may wish to punch the object code from his program onto paper tapes to be used as input to a PROM burner.

PROM ORGANIZATION

The assembler generates binary object code for the executable statements in the file named ASM.

This binary object code is output to a file called PRMOUT.

For our example we shall assume that the microword is 48 bits wide and the number of executable statements is 1024.

This gives us a matrix 48 wide by 1024 deep as shown in Figure 6-1.

Bit No.	1 2 3 4 • 48
Executable Instruction Number	1 2 3 4 • • • 1024

Figure 6-1. Bit Matrix

After PROM width and depth are specified, the Bit Matrix is subdivided to yield a PROM Map where each PROM is n bits wide by m bits deep. If we assume that the program origin is zero for our example, the actual PROM MAP printed might appear as shown in Figure 6-2.

For the example, PROMs shall be organized as shown in Figure 6-3.

Each executable instruction naturally has a program counter associated with it by virtue of its position in the program and/or the origin(s) that were set during the assembly execution.

This breakup of the matrix is now called a PROM map which has associated with it, not only the PROMs shown, but rows and columns as shown in Figure 6-3. Thus, we may now refer to PROM 19 by using the digits 19, or by referencing R3 for Row 3 and C5 for Column 5.

As shown in Figure 6-4, all PROMs in Row 1 are 256 (instructions) deep, but PROMs 1, 3, 5, and 6 are only 4 bits wide, while PROMs 2 and 7 are 8 bits wide and PROM 4 is 16 bits wide.

In Row 2, all PROMs are 512 (instructions) deep and PROMs 8, 10, 12 and 13 are 4 bits wide, PROMs 9 and 14 are 8 bits wide and PROM 11 is 16 bits wide.

Rows 3 and 4 are each 128 (instructions) deep; PROMs 15, 22, 17, 24, 19, 26, 20, and 27 are 4 bits wide; PROMs 16, 23, 21, and 28 are 8 bits wide; and PROMs 18 and 25 are 16 bits wide.

If the user requests printing (or punching) of PROM #1 he will obtain data that is 4 by 256.

If the user requests printing of Row 3, he will obtain data (i.e., the contents of PROMs 15 through 21) in the following form:

4 X 128, 8 X 128, 4 X 128, 16 X 128, 4 X 128, 4 X 128, 8 X 128

If the user requests printing of Column 4 he will obtain data (i.e., the contents of PROMs 4, 11, 18, and 25) that is:

16 X 256, 16 X 512, 16 X 128, 16 X 128

	PC	C1	C2	C3	C4	C5	C6	C7	
R1	0000	1	2	3	4	5	6	7	PROM No.
R2	0100	8	9	10	11	12	13	14	
R3	0300	15	16	17	18	19	20	21	
R4	0380	22	23	24	25	26	27	28	

where

PC represents the initial program counter value for that PROM row. The PC value is given in hexadecimal.

Figure 6-2. Sample PROM MAP.

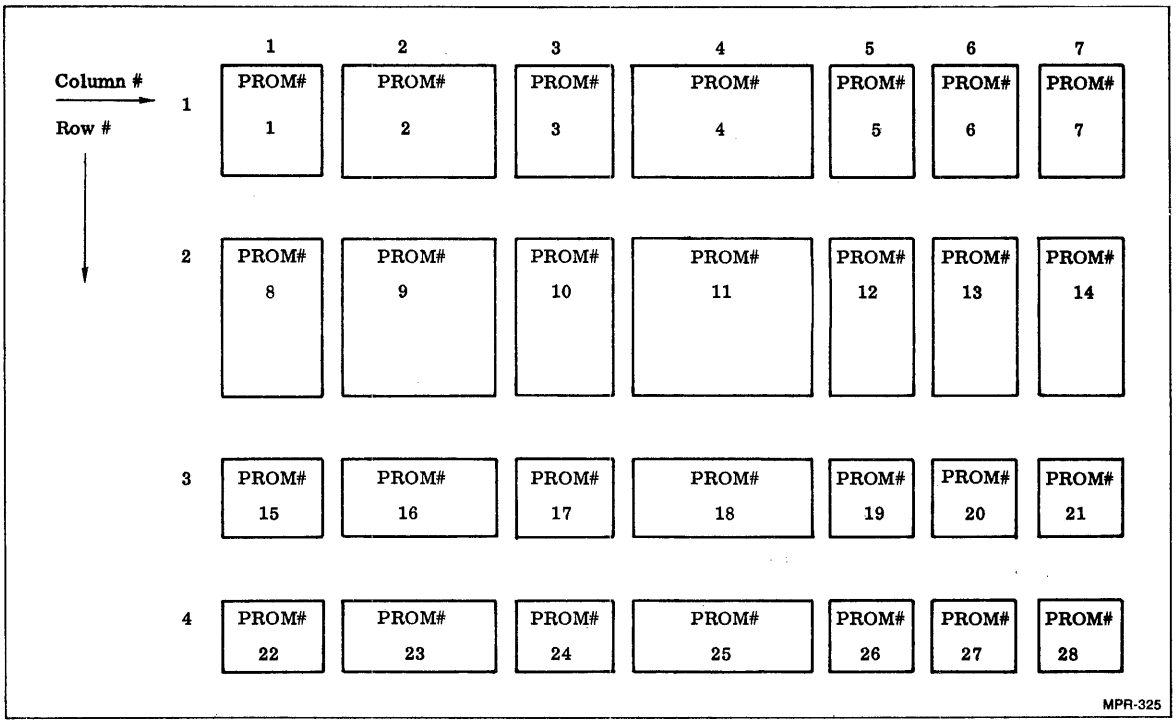


Figure 6-3. PROM MAP

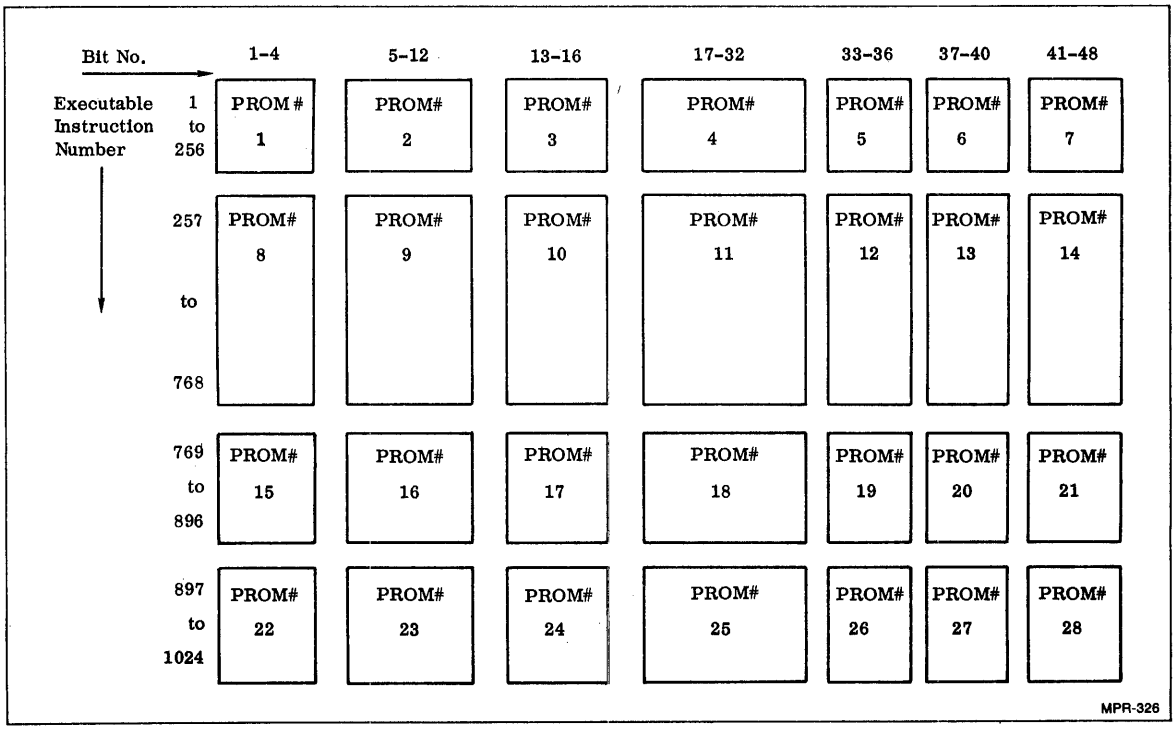


Figure 6-4. Organization of PROMs

Bipolar Logic and Interface

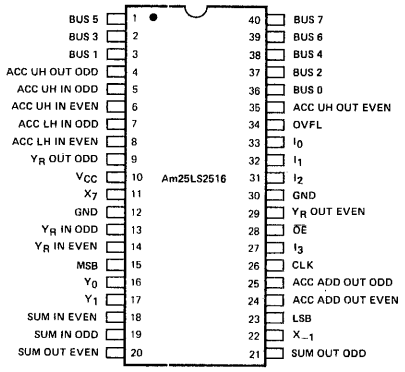
4

MULTIPLIERS

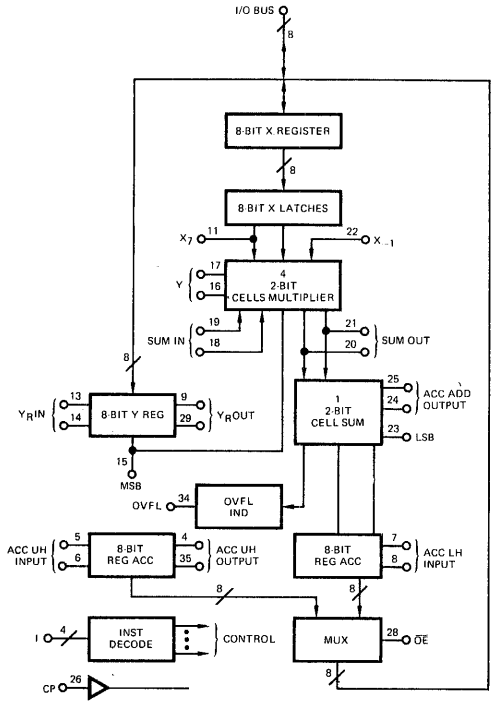
Am25LS2516

- 8-bit by 8-bit serial/parallel multiplier
- Two's complement, two-bit look-ahead carry-save arithmetic
- Microprogrammable – four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- 8-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz typ.

CONNECTION DIAGRAM



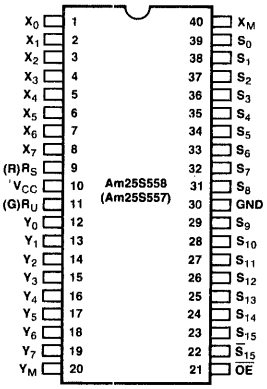
LOGIC DIAGRAM



Am25S557 • Am25S558

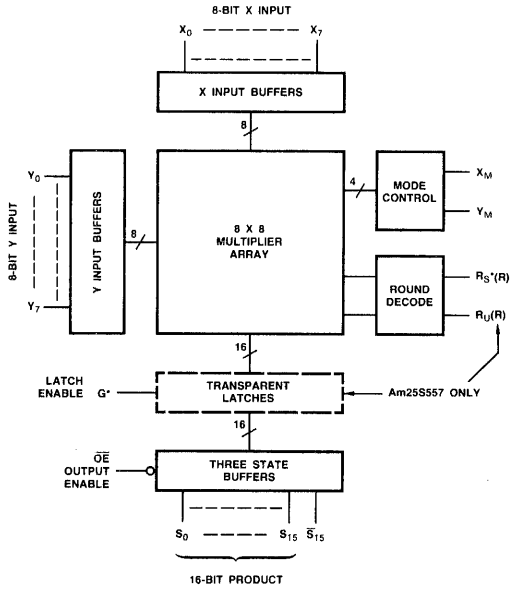
- 8-bit by 8-bit combinatorial multiplier
- Full 8 x 8 multiply in 45ns typ.
- Cascades to 16 x 16 in 110ns typ.
- Unsigned, two's complement or mixed operands
- MSB and MSB outputs for easy expansion
- Implements common rounding algorithms with additional logic
- Three-state outputs
- Transparent 16-bit latch in Am25S557

CONNECTION DIAGRAM



Pin assignments shown are for Am25S558. G and R shown in parentheses are pin assignments for Am25S557.

LOGIC DIAGRAM



*Pin11 is G for Am25S557 and R_U for Am25S558.

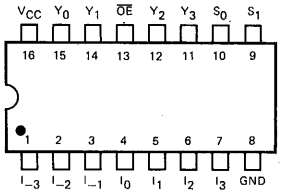
Refer to Schottky and Low-Power Schottky Data Book for complete product data.

SHIFTERS

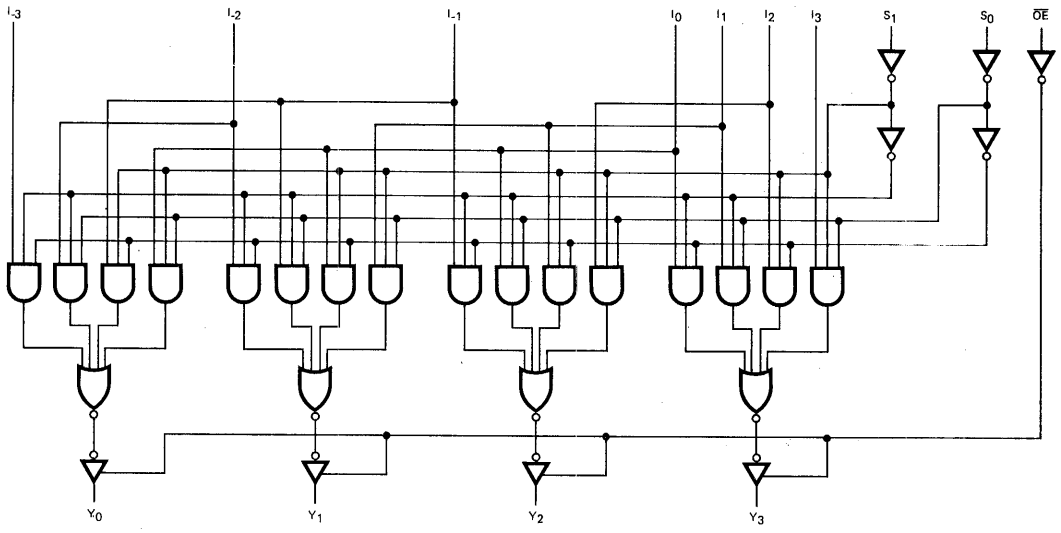
Am25S10

- Shifts 4 bits 0, 1, 2 or 3 places
- Three-state outputs
- t_{PD} 6.5ns typ.
- Easy expansion to any number of bits without propagation delay increase

CONNECTION DIAGRAM



LOGIC DIAGRAM



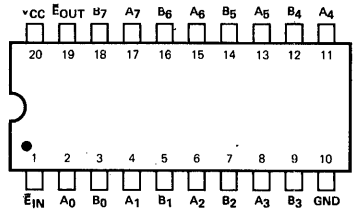
4

COMPARATORS

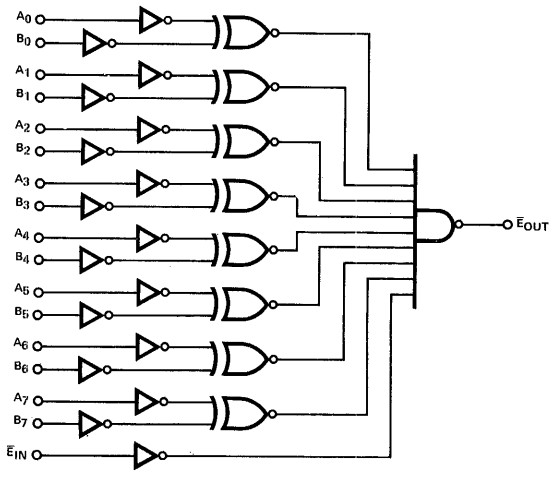
Am25LS2521

- 8-bit byte oriented equal-to comparator
- Easily cascadable using $\overline{E}_{IN}$
- Combinatorial logic with t_{PD} = 9.0ns typ.
- Broad application in conditional gating and microprocessor memory address decoding

CONNECTION DIAGRAM



LOGIC DIAGRAM



Refer to Schottky and Low-Power Schottky Data Book for complete product data.

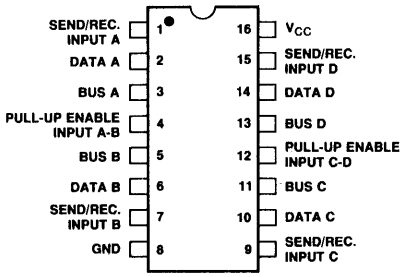
BUS TRANSCEIVERS/DRIVERS

Am3448A

FEATURES

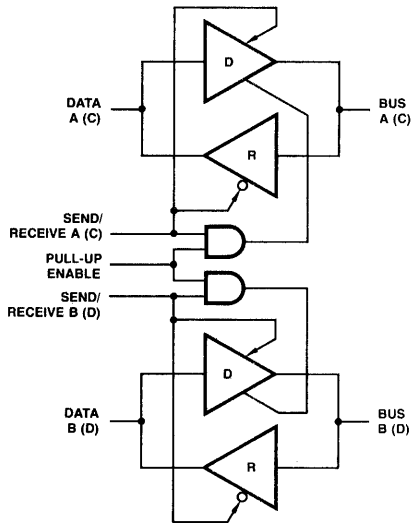
- IEEE-488 quad bidirectional transceiver
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV typ.
- Fast propagation times – 50-20ns typ.
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided

CONNECTION DIAGRAM



LOGIC DIAGRAM

1/2 Am3448A



Refer to Schottky and Low-Power Schottky Data Book for complete product data.

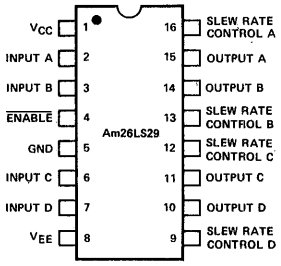
LINE DRIVERS

Am26LS29

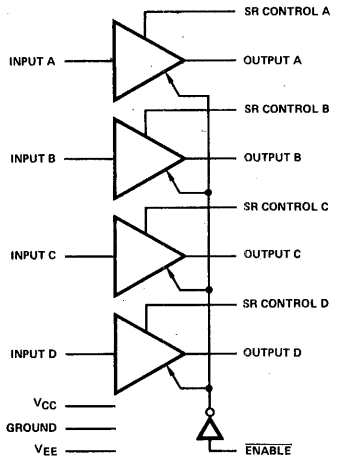
FEATURES

- Four single-ended line drivers in one package
- Meets all requirements of RS-423
- Output short-circuit protection
- Individual rise time control for each output
- 50Ω transmission line drive capability
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in high-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS

CONNECTION DIAGRAM



LOGIC DIAGRAM

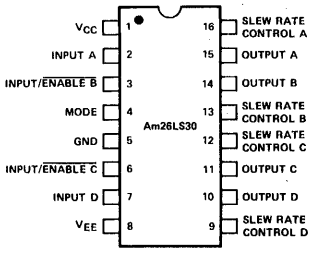


Am26LS30

FEATURES

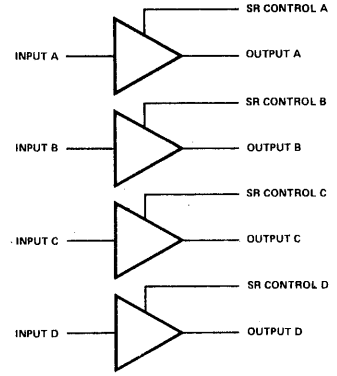
- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in high-impedance state
- Individually three-state drivers when used in differential mode
- Low I_{CC} and I_{EE} power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability

CONNECTION DIAGRAM

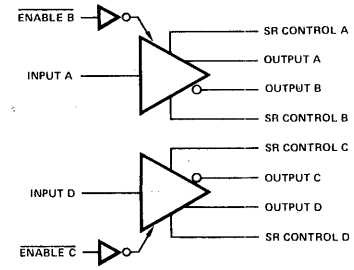


LOGIC DIAGRAMS

Am26LS30 with Mode Control HIGH (RS-423)



Am26LS30 with Mode Control LOW (RS-422)



Refer to Schottky and Low-Power Schottky Data Book for complete product data.

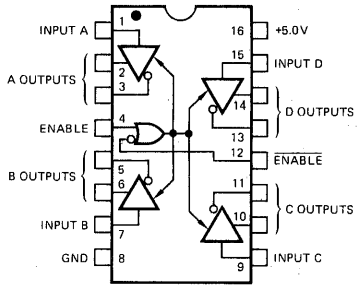
LINE DRIVERS AND RECEIVERS

Am26LS31

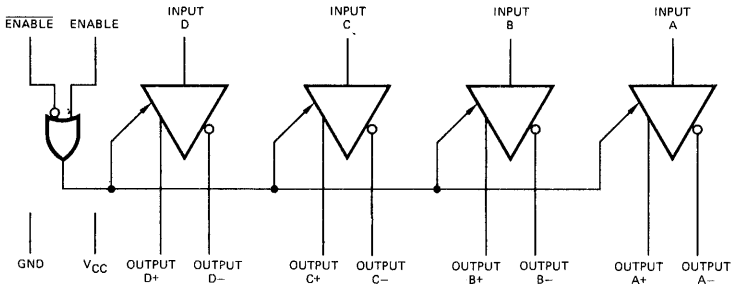
FEATURES

- Four line drivers in one package
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Output short-circuit protection
- Complementary outputs
- Outputs won't load line when V_{CC} = 0
- Output skew – 2.0ns typ.
- Input to output delay – 12ns
- Operation from single +5V supply

CONNECTION DIAGRAM



LOGIC DIAGRAM

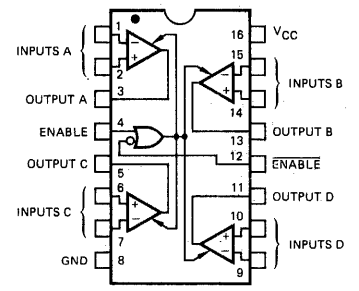


Am26LS32 • Am26LS33

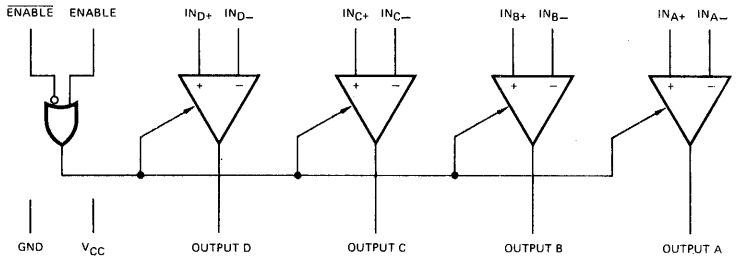
FEATURES

- Quad differential line receivers
- Am26LS32 meets all the requirements of RS-422 and RS-423
- Input voltage range 15V on Am26LS33; 7V on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- Fail safe input/output relationship. Output always high when inputs are open
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply

CONNECTION DIAGRAM



LOGIC DIAGRAM



Refer to Schottky and Low-Power Schottky Data Book for complete product data.

Advanced Bipolar Memory

5

BIPOLAR MEMORY SELECTION GUIDE

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Operating Power – Max. (mW)	Outputs
Am3101	16 x 4	60	C	550	Open Collector
Am3101-1XC†	16 x 4	35	C	525	Open Collector
Am3101-1XM†	16 x 4	50	M	580	Open Collector
Am5489-1†	16 x 4	50	M	580	Open Collector
Am7489	16 x 4	60	C	550	Open Collector
Am7489-1†	16 x 4	35	C	525	Open Collector
Am31L01AXC	16 x 4	55	C	185	Open Collector
Am31L01AXM	16 x 4	65	M	210	Open Collector
Am27S02XC	16 x 4	35	C	550	Open Collector
Am27S02XM	16 x 4	50	M	580	Open Collector
Am27S03XC	16 x 4	35	C	550	3-State
Am27S03XM	16 x 4	50	M	580	3-State
Am27S02AXC	16 x 4	25	C	525	Open Collector
Am27S02AXM	16 x 4	30	M	580	Open Collector
Am27S03AXC	16 x 4	25	C	525	3-State
Am27S03AXM	16 x 4	30	M	580	3-State
Am27LS02XC	16 x 4	55	C	185	Open Collector
Am27LS02XM	16 x 4	65	M	210	Open Collector
Am27LS03XC	16 x 4	55	C	185	3-State
Am27LS03XM	16 x 4	65	M	210	3-State
Am27S06XC††	16 x 4	25	C	525	Open Collector
Am27S06XM††	16 x 4	30	M	580	Open Collector
Am27S07XC††	16 x 4	25	C	525	3-State
Am27S07XM††	16 x 4	30	M	580	3-State
Am27LS06XC††	16 x 4	55	C	185	Open Collector
Am27LS06XM††	16 x 4	65	M	210	Open Collector
Am27LS07XC††	16 x 4	55	C	185	3-State
Am27LS07XM††	16 x 4	65	M	210	3-State
Am27LS00AXC	256 x 1	35	C	525	3-State
Am27LS00AXM	256 x 1	45	M	550	3-State
Am27LS00XC	256 x 1	45	C	370	3-State
Am27LS00XM	256 x 1	55	M	385	3-State
Am27LS01AXC	256 x 1	35	C	525	Open Collector
Am27LS01AXM	256 x 1	45	M	550	Open Collector
Am27LS01XC	256 x 1	45	C	370	Open Collector
Am27LS01XM	256 x 1	55	M	385	Open Collector
Am93415XC	1024 x 1	45	C	815	Open Collector
Am93425XM	1024 x 1	60	M	935	3-State
*Am93412XC	256 x 4	45	C	815	Open Collector
*Am93422XM	256 x 4	60	M	935	3-State

†Option of new improved Am27S02A featuring higher speed and write cycle transparency similar to Am3101 and Am7489
††Same as Am27S02A/03A and Am27LS02/03 respectively with non-inverting outputs
*Available first quarter 1980

READ-ONLY MEMORIES

Part Number	Organization	Access Time	Temp. Range	Power Supplies	Operating Power (mW)	Outputs
Am27S80XC	1024 x 8	175	C	+5V	895	Open Collector
Am27S80XM	1024 x 8	275	M	+5V	935	Open Collector
Am27S81XC	1024 x 8	175	C	+5V	895	3-State
Am27S81XM	1024 x 8	275	M	+5V	935	3-State
Am27S82XC†††	1024 x 8	175	C	+5V	895	Open Collector
Am27S82XM†††	1024 x 8	275	M	+5V	935	Open Collector
Am27S83XC†††	1024 x 8	175	C	+5V	895	3-State
Am27S83XM†††	1024 x 8	275	M	+5V	935	3-State

†††Same as Am27S80 and Am27S81 with OR Enable Chip Select.

BIPOLAR MEMORY SELECTION GUIDE

PROGRAMMABLE READ-ONLY MEMORIES

Part Numbers	Organization	Access Time	Temp. Range	Power Supplies	Operating Power (mW)	Package Pins	Outputs
Am27S18XC	32 x 8	40	C	+5V	605	16	Open Collector
Am27S18XM	32 x 8	50	M	+5V	635	16	Open Collector
Am27S19XC	32 x 8	40	C	+5V	605	16	3-State
Am27S19XM	32 x 8	50	M	+5V	635	16	3-State
Am27LS20XC	256 x 4	45	C	+5V	685	16	Open Collector
Am27LS20XM	256 x 4	60	M	+5V	715	16	Open Collector
Am27LS21XC	256 x 4	45	C	+5V	685	16	3-State
Am27LS21XM	256 x 4	60	M	+5V	715	16	3-State
Am27S12XC	512 x 4	50	C	+5V	685	16	Open Collector
Am27S12XM	512 x 4	60	M	+5V	715	16	Open Collector
Am27S13XC	512 x 4	50	C	+5V	685	16	3-State
Am27S13XM	512 x 4	60	M	+5V	715	16	3-State
Am27S15XC	512 x 8	60	C	+5V	920	24	3-State w/Latches
Am27S15XM	512 x 8	90	M	+5V	1020	24	3-State w/Latches
Am27S25XC	512 x 8	N.A.†	C	+5V	970	24††	3-State w/Registers
Am27S25XM	512 x 8	N.A.†	M	+5V	1020	24††	3-State w/Registers
Am27S26XC	512 x 8	N.A.†	C	+5V	970	22	Open Collector w/Registers
Am27S26XM	512 x 8	N.A.†	M	+5V	1020	22	Open Collector w/Registers
Am27S27XC	512 x 8	N.A.†	C	+5V	970	22	3-State w/Registers
Am27S27XM	512 x 8	N.A.†	M	+5V	1020	22	3-State w/Registers
Am27S28XC	512 x 8	55	C	+5V	920	20	Open Collector
Am27S28XM	512 x 8	70	M	+5V	965	20	Open Collector
Am27S29XC	512 x 8	55	C	+5V	920	20	3-State
Am27S29XM	512 x 8	70	M	+5V	965	20	3-State
Am27S30XC	512 x 8	55	C	+5V	920	24	Open Collector
Am27S30XM	512 x 8	70	M	+5V	965	24	Open Collector
Am27S31XC	512 x 8	55	C	+5V	920	24	3-State
Am27S31XM	512 x 8	70	M	+5V	965	24	3-State
Am27S32XC	1024 x 4	55	C	+5V	735	18	Open Collector
Am27S32XM	1024 x 4	70	M	+5V	800	18	Open Collector
Am27S33XC	1024 x 4	55	C	+5V	735	18	3-State
Am27S33XM	1024 x 4	70	M	+5V	800	18	3-State
Am27S180XC	1024 x 8	60	C	+5V	920	24	Open Collector
Am27S180XM	1024 x 8	80	M	+5V	1020	24	Open Collector
Am27S181XC	1024 x 8	60	C	+5V	920	24	3-State
Am27S181XM	1024 x 8	80	M	+5V	1020	24	3-State
*Am27S184XC	2048 x 4	55	C	+5V	630	18	Open Collector
*Am27S184XM	2048 x 4	70	M	+5V	715	18	Open Collector
*Am27S185XC	2048 x 4	55	C	+5V	630	18	3-State
*Am27S185XM	2048 x 4	70	M	+5V	715	18	3-State

†Normal Access time not applicable – this product contains built-in pipeline registers – nominal address to clock set-up time 40ns, clock to output 15ns.
††Slimline 300 mil pin centers.
*Available second quarter 1980.

Am27LS00/Am27LS01

Low-Power Schottky 256-Bit Random Access Memories

Distinctive Characteristics

- Fully decoded 256-bit TTL RAMs.
  - Plug-in replacements for 74200. IM5503/5523, 93411/21
  - Pin compatible with MM6530/31, 3106/7, 82S06, 74S201
- Open collector (Am27LS01) and three-state (Am27LS00)
- High speed operation:
  - 35ns typical access time
  - 45ns guaranteed (0°C to +75°C)
  - 55ns guaranteed (–55°C to +125°C)
- Very low power dissipation
  - 275mW typical
  - 70mA maximum I_{CC}
- Full military temperature range performance.
  - 100% tested to GALPAT at –55°C and +125°C
  - 10% power supply tolerance
- Internal ECL circuitry
  - Uniform access times over voltage and temperature variations.
- Tested to GALPAT.
  - Functional and switching characteristics are guaranteed for all data and address patterns.

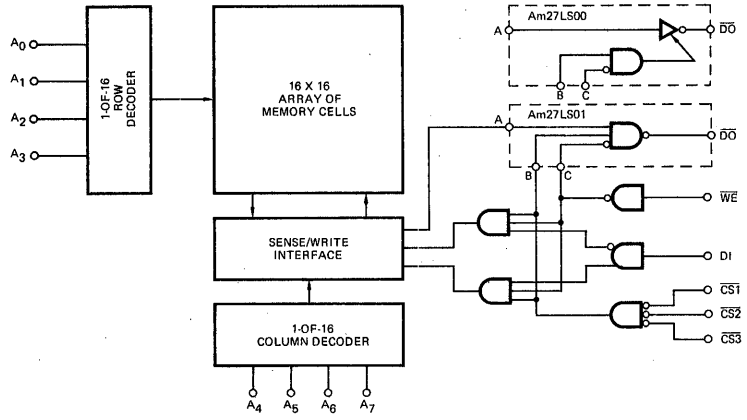
FUNCTIONAL DESCRIPTION

The Am27LS00 and Am27LS01 are fully decoded bipolar random access memories for use in high-speed buffer memories and as a replacement for high-speed core memories in digital systems. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00) or open-collector output (Am27LS01). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or from the memory. These three active LOW chip select inputs permit the Am9301 or Am54LS/74LS138 MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

LOGIC DIAGRAM



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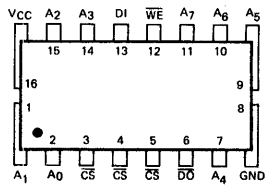
ORDERING INFORMATION

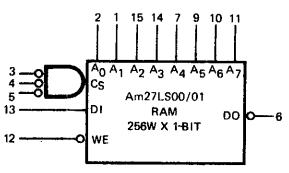
Three-State Output		
Molded DIP	0°C to +75°C	AM27LS00PC
Hermetic DIP	0°C to +75°C	AM27LS00DC
Hermetic DIP	–55°C to +125°C	AM27LS00DM
Flat Pack	–55°C to +125°C	AM27LS00FM
Open Collector Output		
Molded DIP	0°C to +75°C	AM27LS01PC
Hermetic DIP	0°C to +75°C	AM27LS01DC
Hermetic DIP	–55°C to +125°C	AM27LS01DM
Flat Pack	–55°C to +125°C	AM27LS01FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +V_{CC}
Output Current, Into Outputs	30 mA
DC Input Current	−30mA to +50mA

OPERATING RANGE

Part No.	Ambient Operating Temperature	Power Supply Voltage
Am27LS00DC, PC Am27LS01DC, PC	0°C to +75°C	4.75 V to 5.25 V
Am27LS00DM, FM Am27LS01DM, FM	−55°C to +125°C	4.50 V to 5.50 V

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage (Am27LS00 Only)	V_{CC} = MIN., I_{OH} = −2.0 mA (MIL Range) V_{IN} = V_{IH} or V_{IL}, I_{OH} = −2.6 mA (COM'L Range)	2.4	3.1		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA, V_{IN} = V_{IH} or V_{IL}		0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−0.50	−0.80	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V		<1	20	μA
V_{BK}	Input Breakdown Voltage	V_{CC} = MAX., I_{IN} = 100 μA	7.0			V
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 2.4 V		<1	30	μA
		V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 0.4 V		<1	−30	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−20	−30	−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		55	70	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA			−1.5	Volts

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description		T_A = 25°C Typ.	T_A = 0°C to 75°C Min.	T_A = 0°C to 75°C Max.	T_A = −55°C to 125°C Min.	T_A = −55°C to 125°C Max.	Units
t_{PLH}(A) t_{PHL}(A)	Delay from Address to Output	See Fig. 2	35	15	45	10	55	ns
t_{PZH}($\overline{CS}$) t_{PZL}($\overline{CS}$)	Delay from Chip Select to Active Output and Correct Data	See Fig. 2	15	5	25	5	30	ns
t_{PHZ}($\overline{CS}$) t_{PLZ}($\overline{CS}$)	Delay from Chip Select to Inactive Output	See Fig. 2	15	5	25	5	30	ns
t_{rec}($\overline{WE}$)	Delay from Write Enable (HIGH) to Correct Output Data	See Fig. 1	25		45		55	ns
t_{PZH}($\overline{WE}$) t_{PZL}($\overline{WE}$)	Delay from Write Enable (HIGH) to Active Output	See Fig. 1		5		5		ns
t_{PHZ}($\overline{WE}$) t_{PLZ}($\overline{WE}$)	Delay from Write Enable (LOW) to Inactive Output	See Fig. 1	20		30		40	ns
t_s(A)	Set-up Time Address	See Fig. 1	0	0		5		ns
t_h(A)	Hold Time Address		0	0		5		ns
t_s(DI)	Set-up Time Data Input	See Fig. 1	20	30		35		ns
t_h(DI)	Hold Time Data Input	See Fig. 1	0	0		5		ns
t_{pw}($\overline{WE}$)	Write Enable Pulse Width	See Fig. 1	20	30		35		ns

Am27LS00/Am27LS01 LOADING RULES (In TTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A_1	1	0.5	–	–
A_0	2	0.5	–	–
$\overline{CS}$	3	0.5	–	–
$\overline{CS}$	4	0.5	–	–
$\overline{CS}$	5	0.5	–	–
DO (Note)	6	–	50/65	10
A_4	7	0.5	–	–
GND	8	–	–	–
A_5	9	0.5	–	–
A_6	10	0.5	–	–
A_7	11	0.5	–	–
$\overline{WE}$	12	0.5	–	–
DI	13	0.5	–	–
A_3	14	0.5	–	–
A_2	15	0.5	–	–
V_{CC}	16	–	–	–

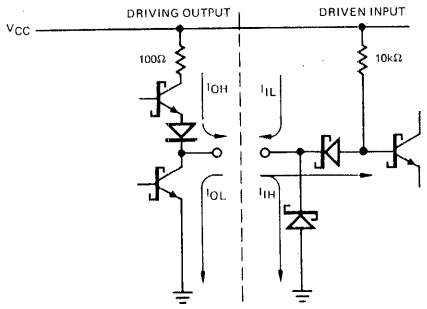
Note: Am27LS01 has open collector output.
A Standard TTL Unit Load is defined as 40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

Am27LS00/Am27LS01 LOADING RULES (In Low Power Schottky Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A_1	1	2.2	–	–
A_0	2	2.2	–	–
$\overline{CS}$	3	2.2	–	–
$\overline{CS}$	4	2.2	–	–
$\overline{CS}$	5	2.2	–	–
DO (Note)	6	–	100/130	44
A_4	7	2.2	–	–
GND	8	–	–	–
A_5	9	2.2	–	–
A_6	10	2.2	–	–
A_7	11	2.2	–	–
$\overline{WE}$	12	2.2	–	–
DI	13	2.2	–	–
A_3	14	2.2	–	–
A_2	15	2.2	–	–
V_{CC}	16	–	–	–

Note: Am27LS01 has open collector output.
A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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TRUTH TABLE

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	DI	$\overline{DO}(t_{n+1})$	
H	X	X	OFF	No Selection
L	L	L	OFF	Write '0'
L	L	H	OFF	Write '1'
L	H	X	$\overline{DI}(t_n)$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
OFF = Floating output level is determined by external circuitry connected to the output.

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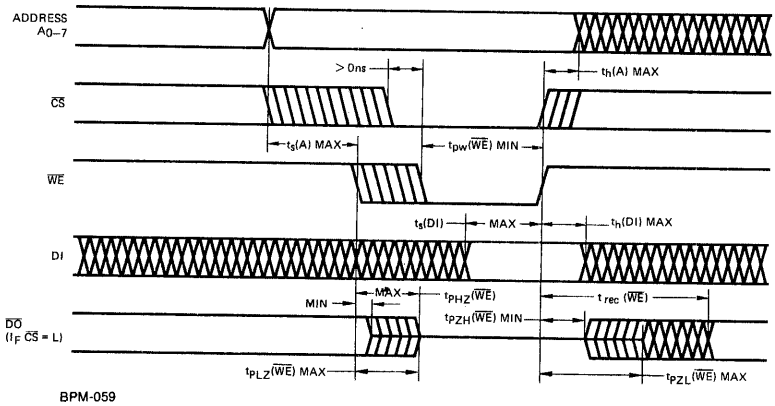
SWITCHING WAVEFORMS



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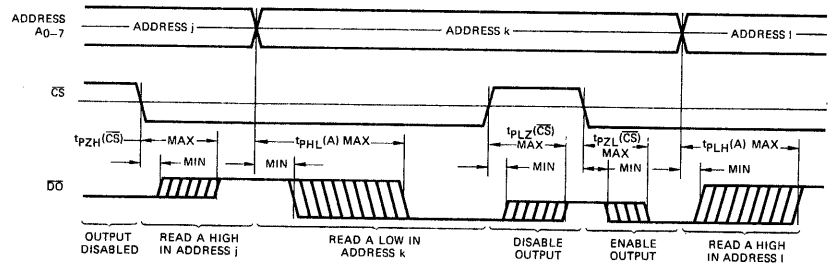
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⟋⟋⟋	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⟋⟋⟋	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s (A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h (A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

Figure 1



Switching delays from address and chip select inputs to the data output. For the Am27LS00 disabled output is "OFF," represented by a single center line. For the Am27LS01, a disabled output is HIGH.

Figure 2

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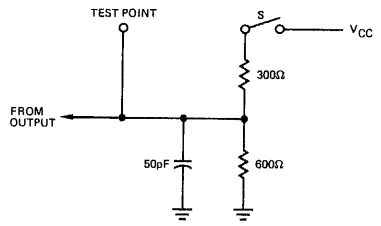
TEST LOAD



Note: All measurements at 1.5V

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S is closed for all tests except for Am27LS00 tests in which the output switches between an active HIGH level and a HIGH impedance state.

OUTPUT LOADING RULES

The Am27LS01 has an open collector output. The outputs of several memories may be tied together and the common line connected through a pull-up resistor to V_{CC}. The common line will go LOW if and only if one of the Am27LS01 outputs connected to it goes LOW, i.e., is enabled and reading a LOW. The HIGH state is established by the pull-up resistor. The value of the resistor is limited by two equations:

$$R(min) = \frac{V_{CC}\ (max) - 0.4}{16 - i\ (1.6)}$$

i = number of TTL inputs driven

$$R(max) = \frac{V_{CC}\ (min) - 2.4}{0.03n + 0.04i}$$

n = number of Am27LS01 outputs connected together

For highest speed, use the minimum R; for lowest power, use the maximum R.

The Am27LS00 has active circuitry to establish both the HIGH and LOW logic levels and requires no pull-up resistor. Up to 64 Am27LS00 outputs can be connected together.

DEFINITIONS OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

X Unknown or don't care state

Z OFF, applying to the third high impedance state of the output.

FUNCTIONAL TERMS:

Three State A three state output can exist in three possible states: output LOW sinking current, output HIGH sourcing current, and output floating where the output level is determined by external circuitry connected to the output. This three state output allows AND tying of memory outputs for memory expansion and still keeps the inherent high speed of active pull-up circuitry.

Fully Decoded In a fully decoded memory every possible address combination of logic HIGH's and LOW's uniquely selects a memory word. This form of decoding requires no additional special purpose decoders for system operation and is the most efficient in terms of address inputs required and overall system speed.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{PXH} The delay from a logic level change at an input to a HIGH level on an output.

t_{PXL} The delay from a logic level change at an input to a LOW level on an output.

t_{PXZ} The delay from a logic level change at an input to a high impedance state on a three state output. Measured with a resistor pull-down or pull-up.

t_{PXX}**(A)** The delay from an address input to the memory output.

t_{PXX}**(**$\overline{\text{CS}}$**)** The delay from a chip select input to the memory output.

t_{PXZ}**(**$\overline{\text{WE}}$**)** The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the memory output.

t_{PZX}**(**$\overline{\text{WE}}$**)** The delay from a LOW-to-HIGH transition on the write enable to an active level on the memory output.

t_{pw}**(**$\overline{\text{WE}}$**)** The shortest LOW pulse on the write enable input which is guaranteed to cause the memory to write. Pulses shorter than $t_{pw}(\overline{WE})$ min. may or may not cause a write to occur.

t_s**(A)** The set-up time of the address inputs relative to the HIGH-to-LOW edge of the write pulse. This is the time required for internal address decoding to settle. To avoid writing in spurious addresses, a stable address should be applied to the address inputs at least $t_s(A)$ max. before the write pulse begins.

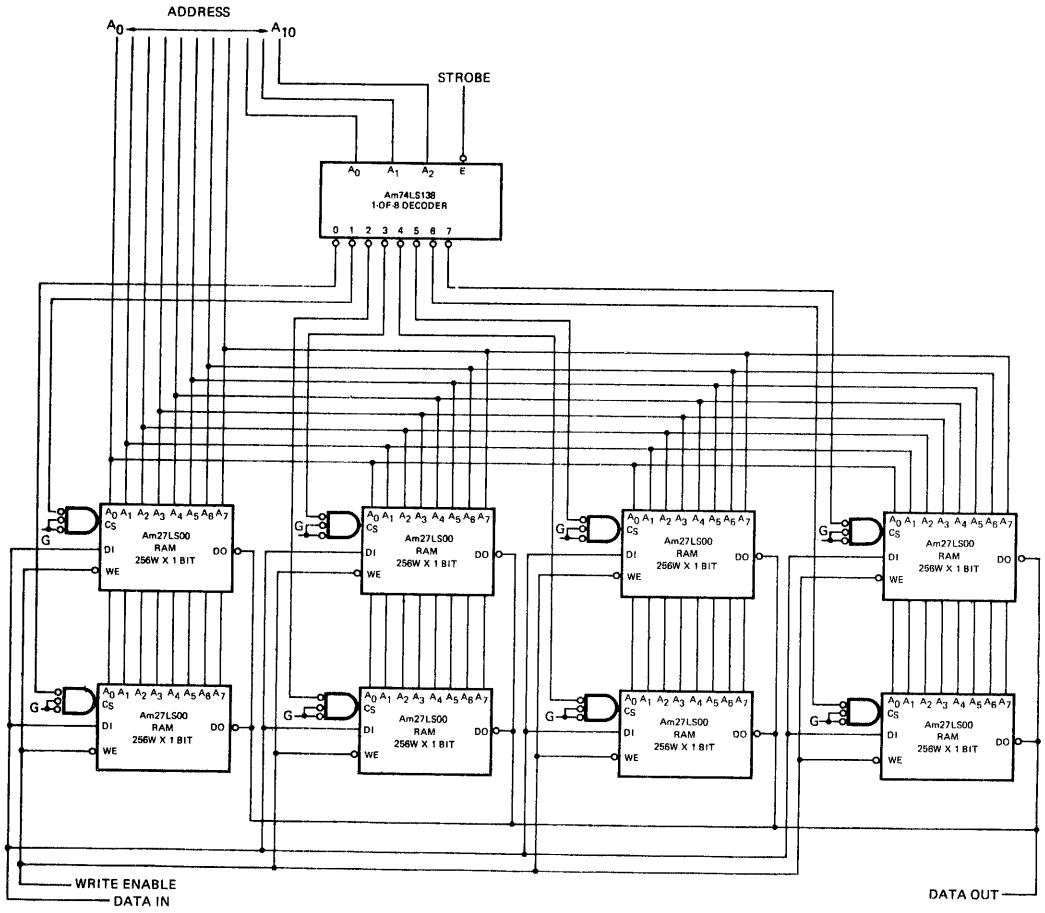
t_h**(A)** The address hold time. This parameter is similar to $t_s(A)$ but is measured relative to the end of the write pulse rather than the beginning. A stable address should be maintained on the address inputs for $t_h(A)$ max. after the write pulse has ended in order to prevent writing in spurious addresses.

t_s**(DI)** Data set-up time. The time prior to the end of the write pulse during which data must be stable to be correctly written into the memory.

t_h**(DI)** Data hold time. The time following the end of the write pulse during which data must not be changed.

5

APPLICATION



G = LOW

2048 WORD x 1-BIT MEMORY

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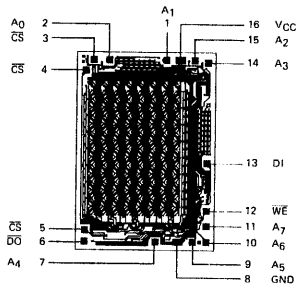
Metallization and Pad Layout



DIE SIZE : 0.084" X 0.121"

Am27S02 • 27S03

64-Bit Random Access Memory

Distinctive Characteristics

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAM.
- Access time typically 22ns.
- Available with three-state outputs (Am27S03) or with open collector outputs (Am27S02).
- Pin compatible high speed replacement for 3101, 93403, and 7489 (use Am27S02) and for DM 75/8599 (use Am27S03).
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

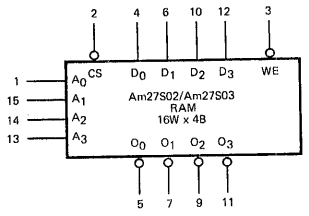
The Am27S02(Am3101A) and Am27S03 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am3101A/Am27S02) or three-state outputs (Am27S03). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am9301 and Am9311.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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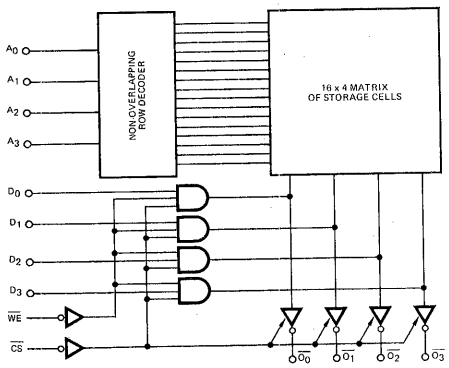
LOGIC BLOCK DIAGRAM



BPM-064

ORDERING INFORMATION

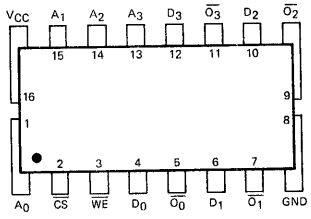
Open Collector Outputs

Package Type	Temperature Range	Order Number
Molded DIP	0°C to 75°C	AM27S02PC or P3101A
Hermetic DIP	0°C to 75°C	AM27S02DC or C3101A
Hermetic DIP	–55°C to +125°C	AM27S02DM
Hermetic Flat Pak	–55°C to +125°C	AM27S02FM

Three-State Outputs

Molded DIP	0°C to +75°C	AM27S03PC
Hermetic DIP	0°C to +75°C	AM27S03DC
Hermetic DIP	–55°C to +125°C	AM27S03DM
Hermetic Flat Pak	–55°C to +125°C	AM27S03FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am27S02XC, Am27S03XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am27S02XM, Am27S03XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S03 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA, V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.3	0.45	Volts
			I_{OL} = 20mA			0.5	
*V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
*V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V	$\overline{WE}$, D_0–D_3, A_{0-3}		.030	0.25	mA
			$\overline{CS}$		.060	0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				10	µA
I_{SC} (Am27S03 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX.	Am27S02		76	105	mA
			Am27S03		87	125	
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −5.0mA				−1.0	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V	Am27S02			100	µA
			Am27S03			40	
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX.	(Am27S03)	−40			µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS

Parameters	Description	Test Conditions		25°C Typ.	T_A = 0° to 75°C Min.	Max.	Units
$t_{pd\pm}(\overline{CS})$	Delay Chip Select to Output HIGH or LOW	V_{CC} = 5.0V, C_L = 30 pF, R_L = 300Ω V_{CC} and 600Ω to GND (16mA Load) measure at 1.5V	Am27S02	12	5	17	ns
			Am27S03	15		25	
$t_{pdz}(\overline{CS})$	Delay Chip Select HIGH to Output OFF			12		20	ns
t_{pd+}(A)	Delay Address to Output HIGH			22	10	35	ns
t_{pd-}(A)	Delay Address to Output LOW			22	10	35	ns
$t_{rec}(\overline{WE})$	Write Recovery Time					35	ns
*$t_{pw}(\overline{WE})$	Write Pulse Width				25		ns
*t_s(D)	Data Set-up Time				25		ns
*t_h(D)	Data Hold Time				0		ns
*t_s(A)	Address Set-up Time				0		ns
*t_h(A)	Address Hold Time				0		ns
$t_{pd\pm}(\overline{WE})$	Delay $\overline{WE}$ HIGH to Output Active			12		25	ns
$t_{pdz}(\overline{WE})$	Delay $\overline{WE}$ LOW to Output OFF			12		25	ns

*System requirement. Parameters preceded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CS}$ Active LOW chip select input. When the chip select is LOW data can be read from or written into the memory.

D_i The data inputs of the memory. i = 1 – 4

O_i The data outputs of the memory, i = 1 – 4

$O_i(t_n)$ The state of output i at time n.

$D_i(t_{n-x})$ The state of the D_i input at time t_{n-x}, where t_{n-x} is the time of the last write operation into a given address.

$\overline{WE}$ Active LOW Write Enable. When the write enable is LOW, data on the data inputs is written into the addressed memory location. When $\overline{WE}$ is HIGH data is read from the addressed location and appears, inverted, at the $\overline{O}$ outputs.

UNIT LOAD A TTL input unit load is defined as −1.6mA at 0.4V (LOW state) and 40μA at 2.4V (HIGH state).

SWITCHING TERMS

$t_{pd\pm}(\overline{CS})$ The delay from the chip select input going LOW to the output going active.

$t_{pdz}(\overline{CS})$ The delay from the chip select going HIGH to the output assuming an inactive high impedance level.

$t_{pd\pm}(A)$ The delay from a change on the address inputs to a correct HIGH (t_{pd+}) or LOW (t_{pd-}) level on the outputs. Access time.

$t_{rec}(\overline{WE})$ Write recovery time. The delay from a LOW-to-HIGH transition on the write enable to the correct data on the outputs of the memory. This is the time required between the end of the write operation and a read operation in the same address.

* $t_{pw}(\overline{WE})$ Minimum write pulse width. The LOW time on the write enable input required to cause a write.

* $t_s(D)$, * $t_h(D)$ Data set-up and hold times. The time, relative to the end of the write pulse (LOW-to-HIGH edge) after which the data on the data inputs will not be written into the memory. To ensure writing the correct data, the data must be present before * $t_s(D)$ min. and must remain until after * $t_h(D)$ min.

* $t_s(A)$ Address set-up time. The time prior to the start of the write pulse (HIGH-to-LOW edge) at which the correct write address must be on the address inputs. An address change later than * $t_s(A)$ max. may cause writing in two addresses.

* $t_h(A)$ Address hold time. The time following the end of the write pulse (LOW-to-HIGH transition) at which a new address may be applied. An address change earlier than * $t_h(A)$ min. may cause writing into two addresses.

$t_{pd\pm}(\overline{WE})$ The delay from a LOW-to-HIGH transition of the write enable to an active (but not necessarily correct) state on the data outputs. The correct state will be present after the write recovery time has elapsed.

$t_{pdo}(\overline{WE})$ The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the data outputs, if the chip is selected.

*System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

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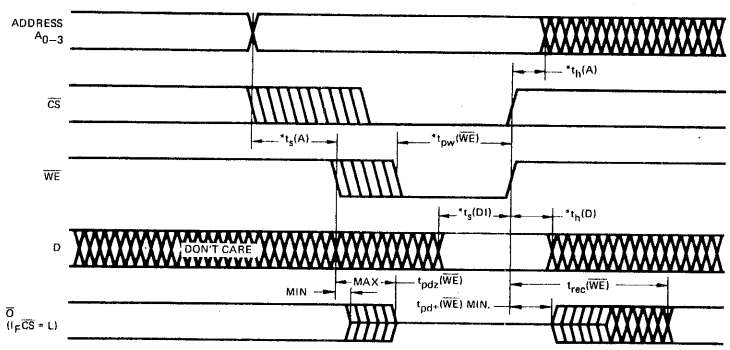
SWITCHING WAVEFORMS



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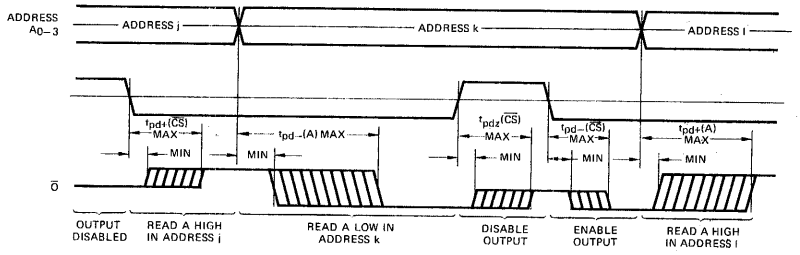
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $*t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $*t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03) while the write enable is LOW. The three parameters $t_s(A)$, $t_h(A)$ and $t_{pw}(WE)$ apply to the condition CS LOW AND WE LOW.

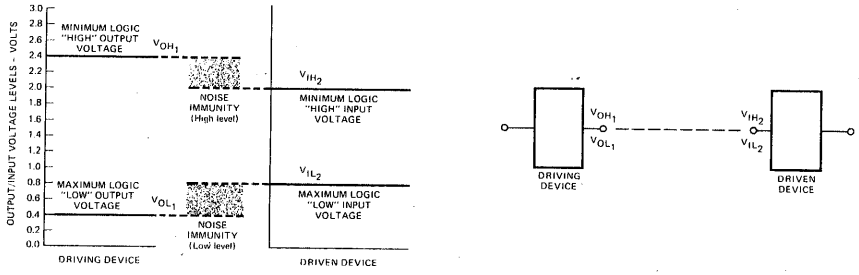


Switching delays from address and chip select inputs to the data output. For the Am27S03 disabled output is "OFF", represented by a single center line. For the Am27S02, a disabled output is HIGH.

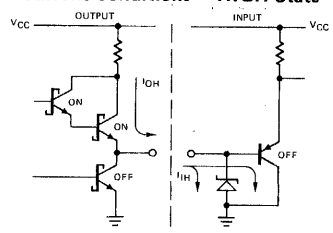
BPM-067

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

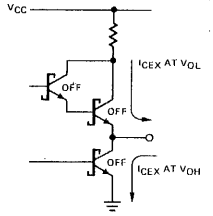


Current Conditions — HIGH State



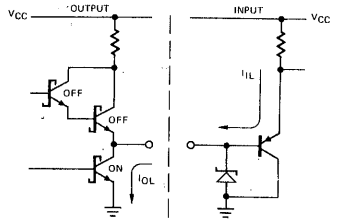
Note: Am27S02 is open collector

Currents Conditions — OFF State



Note: Am27S02 is open collector

Current Conditions — LOW State



BPM-068

USER NOTES

1. The Am27S03 output has active circuitry for both logic levels and requires no external pull-up resistor.
2. For a good DC noise margin with the Am3101A/27S02 a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH}\text{ required}}{nI_{CEX} + NI_{IH}} > R_L > \frac{V_{CC} - V_{OL}\text{ required}}{I_{OL} - NI_{IL}}$$

   Where n is number of OR tied outputs
   N is the number of TTL units loads driven.

3. Address and data lines can be interchanged within their respective groups for ease of P. C. layout without effecting device operation.
4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

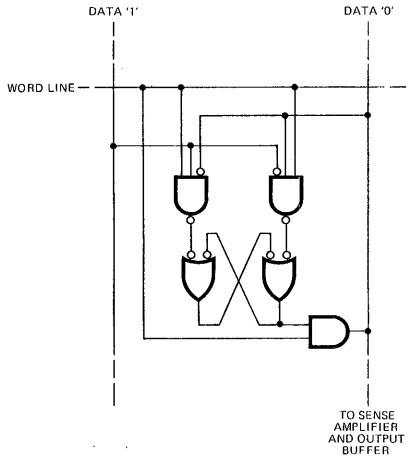
Am3101A LOADING RULES (In TTL Loads)

Input/Output	Pin No.'s	Input Loading	Output Drive (Am27S03) HIGH	LOW
A_0	1	.16	–	–
$\overline{CS}$	2	.16	–	–
$\overline{WE}$	3	.16	–	–
D_0	4	.16	–	–
$\overline{O}_0$	5	–	20	10
D_1	6	.16	–	–
$\overline{O}_1$	7	–	20	10
GND	8	–	–	–
$\overline{O}_2$	9	–	20	10
D_2	10	.16	–	–
$\overline{O}_3$	11	–	20	10
D_3	12	.16	–	–
A_3	13	.16	–	–
A_2	14	.16	–	–
A_1	15	.16	–	–
V_{CC}	16	–	–	–

A TTL unit load is −1.6mA at 0.4V and 40μA at 2.0V.
The Am27S02 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

5

BASIC MEMORY CELL



BPM-069

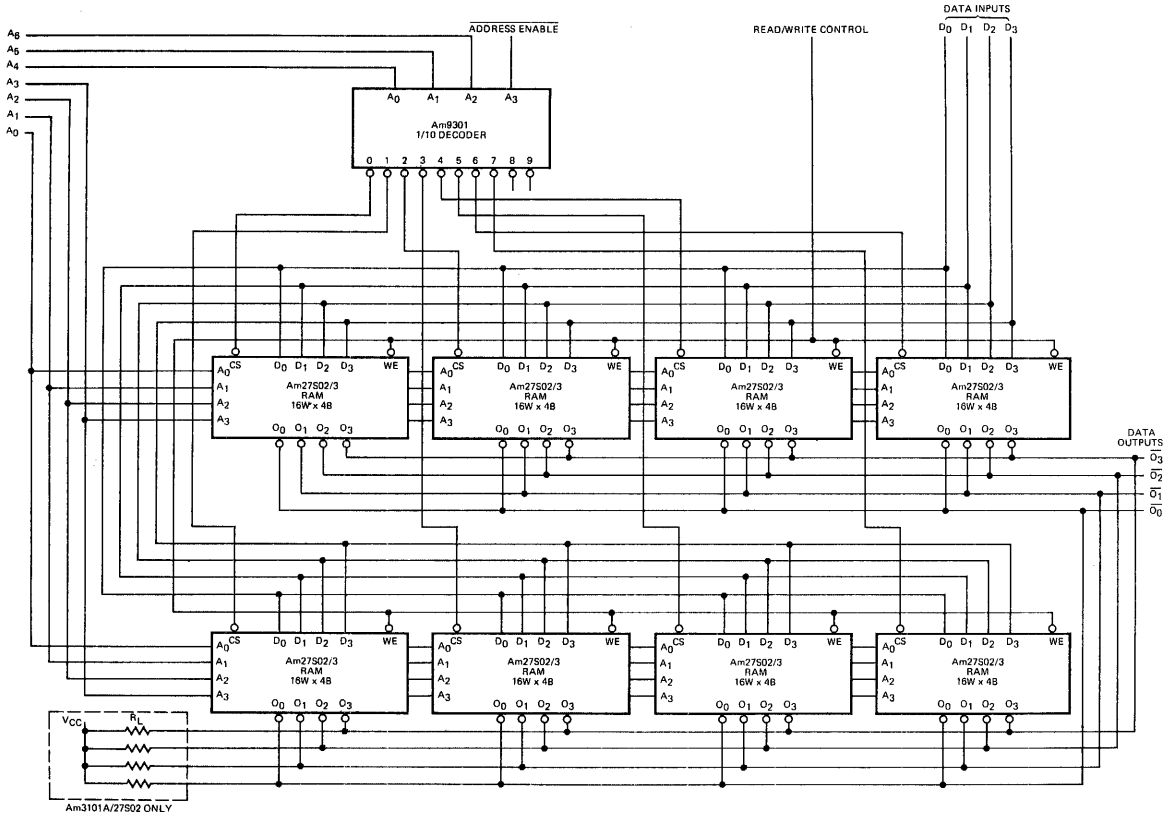
TRUTH TABLE

INPUTS			OUTPUTS	MODE
$\overline{CS}$	$\overline{WE}$	D_i	$\overline{O}_i(t_n)$	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	$D_i(t_{n-x})$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
OFF = HIGH Impedance

Note: The Am27S02 output is at a high impedance level at all times except when reading a LOW.

Am3101A/27S02/27S03 APPLICATION



128 WORD x 4-BIT MEMORY

BPM-070

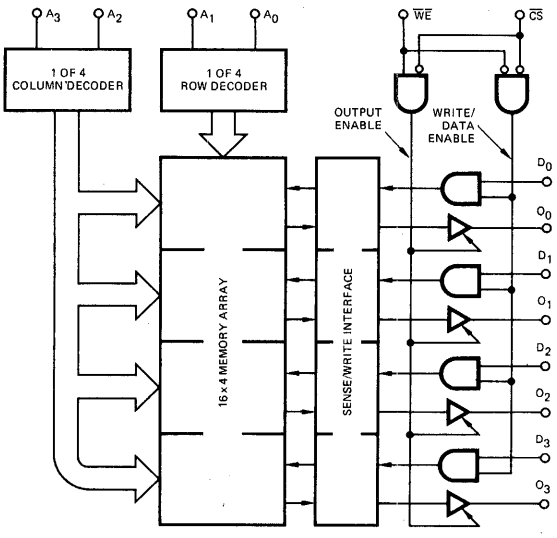
Am27S06 • Am27S07

Non-Inverting Schottky 64-Bit Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power Schottky RAMs
- Ultra-high speed: Address access time typically 15ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am27S07) or with open collector outputs (Am27S06)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

LOGIC BLOCK DIAGRAM



MPR-239

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collector Outputs		
Molded DIP	0°C to +75°C	AM27S06APC
Hermetic DIP	0°C to +75°C	AM27S06ADC
Hermetic DIP	–55°C to +125°C	AM27S06ADM
Hermetic Flat Pak	–55°C to +125°C	AM27S06AFM
Three-State Outputs		
Molded DIP	0°C to +75°C	AM27S07APC
Hermetic DIP	0°C to +75°C	AM27S07ADC
Hermetic DIP	–55°C to +125°C	AM27S07ADM
Hermetic Flat Pak	–55°C to +125°C	AM27S07AFM

FUNCTIONAL DESCRIPTION

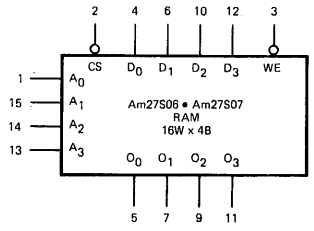
The Am27S06 and Am27S07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27S06) or three-state outputs (Am27S07). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

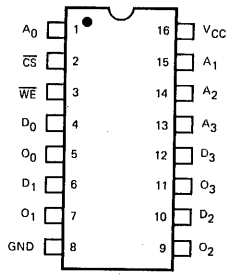
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-240

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-241

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	–0.5V to +7V
DC Voltage Applied to Outputs for High Output State	–0.5V to V_{CC} max.
DC Input Voltage	–0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	–30mA to +5.0mA

OPERATING RANGE

Part No.	V_{CC}	Ambient Temperature
Commercial Grade Am27S06APC, DC Am27S07APC, DC	5.0V ±5%	0°C to +75°C
Military Grade Am27S06ADM, FM Am27S07ADM, FM	5.0V ±10%	–55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	D. C. Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S07 Only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –5.2mA I_{OH} = –2.0mA	COM'L MIL	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA I_{OL} = 20mA			0.350 0.380	0.45 0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3 $\overline{CS}$			–0.015 –0.030	.250 .250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				0.0	10	µA
I_{SC} (Am29701 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			–20	–45	–90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		COM'L MIL		75 75	100 105	mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = –18mA				–0.850	–1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V		Am29700/01		0	40	µA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.		Am29701	–40	0		µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

FUNCTION TABLE

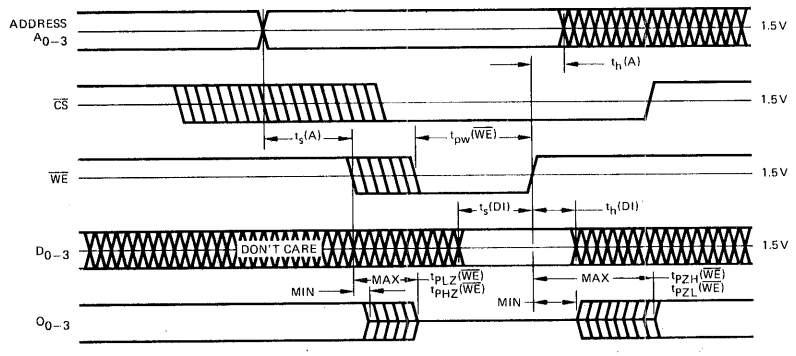
Input		Function	Data Output Status O_{0-3}
$\overline{CE}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word
High	Don't Care	Deselect	Output and Write Disabled

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description		A. C. Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	22		35		50	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		14		17		25	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		19		35		50	ns
$t_s(A)$	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		–6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		–2.5	0		0		ns
$t_s(DI)$	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		18	25		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		–4.0	0		0		ns
$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		18	25		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		13		17		25	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		15		25		35	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S07) while the write enable is LOW.

Figure 1.

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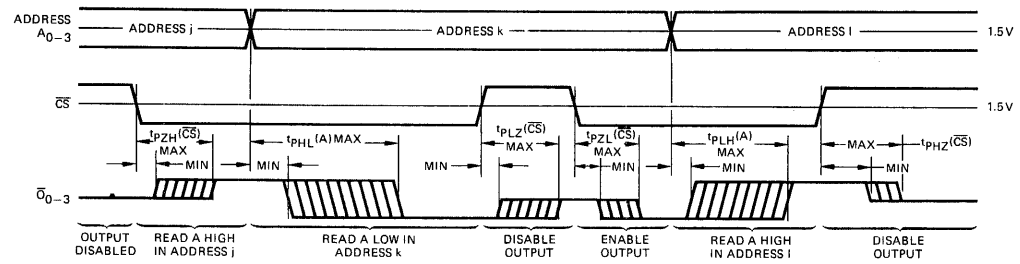
SWITCHING WAVEFORMS (Cont.)



Switching delays from address and chip select inputs to the data output. For the Am27S07 disabled output is "OFF", represented by a single center line. For the Am27S06, a disabled output is HIGH.

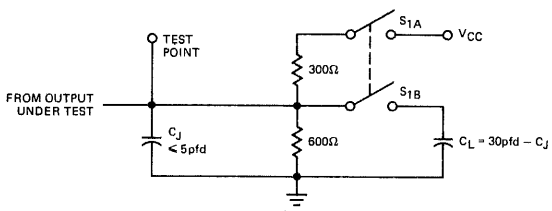
Figure 2.

MPR-243

TEST LOAD

Open Collector Am27S06

S_1 is closed for all A. C. tests. Note that $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ parameters do not apply to 27S06 where disabled output is HIGH.



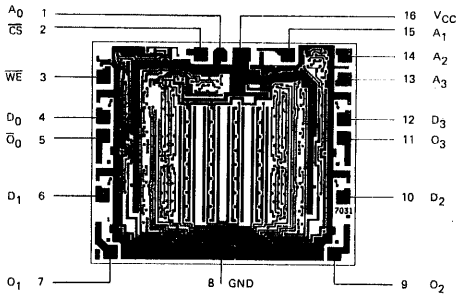
Three-State Am27S07

S_1 is closed for all A. C. tests except $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ where S_1 is open and jig capacitance (C_J) is $\leq$ 5pfd.

Figure 3.

MPR-244

Metallization and Pad Layout



DIE SIZE
0.092" X 0.078"

Am27S12 • Am27S13

2048-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 50ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S12 and Am27S13 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

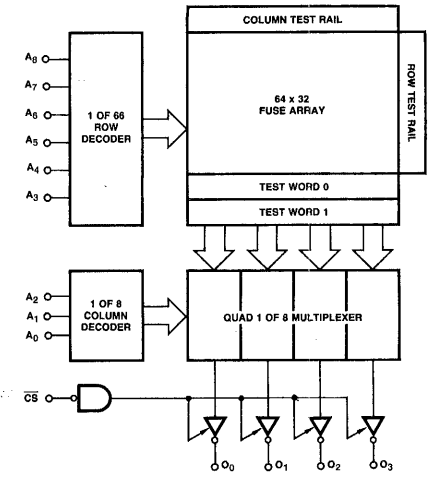
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0°C to +75°C	AM27S12DC
Hermetic DIP	−55°C to +125°C	AM27S12DM
Hermetic Flat Pak	−55°C to +125°C	AM27S12FM
	Three-State Outputs	
Hermetic DIP	0°C to +75°C	AM27S13DC
Hermetic DIP	−55°C to +125°C	AM27S13DM
Hermetic Flat Pak	−55°C to +125°C	AM27S13FM

FUNCTIONAL DESCRIPTION

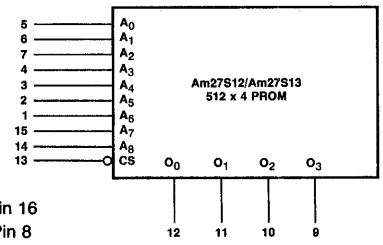
The Am27S12 and Am27S13 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 4 configuration, they are available in both open collector Am27S12 and three-state Am27S13 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-001

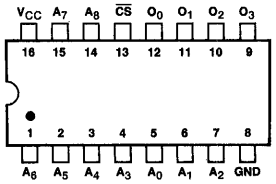
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-002

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming.(Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S12XC, Am27S13XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S12XM, Am27S13XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S13 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S13 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		100	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S13 only; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S13 only; V_O = 2.4V			40	
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S13 only; V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

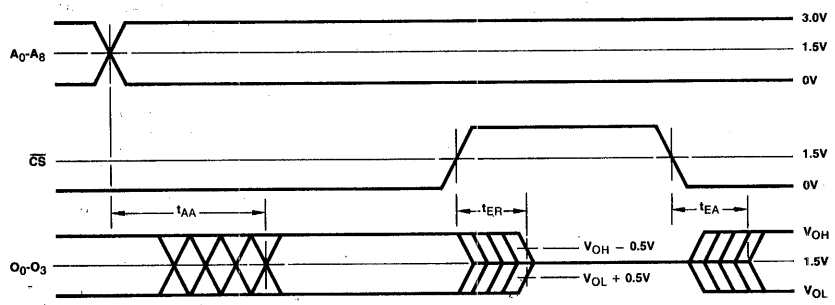
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	50	60	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

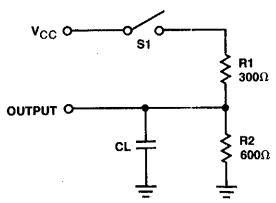
BPM-004

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-005

5

PROGRAMMING

The Am27S12 and Am27S13 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycle. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

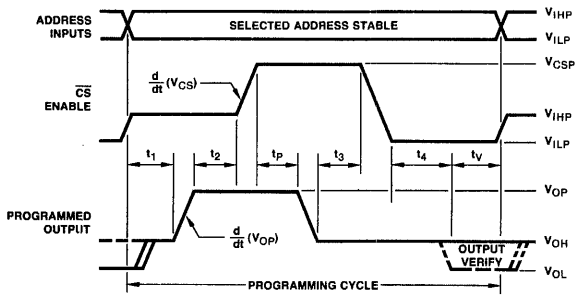
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

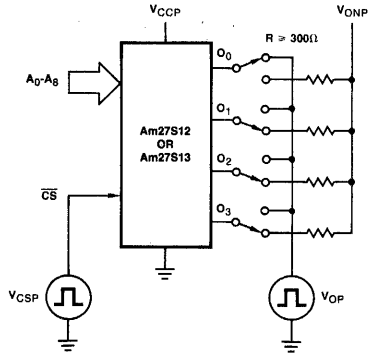
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-006

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-007

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S12 • Am27S13 ADAPTERS AND CONFIGURATOR	715-1408-2	PA16-5 and 512 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

5

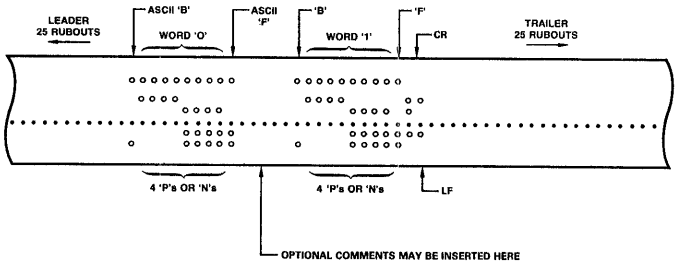
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 :      :        :
511   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	H	H	L	H	H	L	L
					⋮							
H	H	H	H	H	H	H	H	H	H	H	H	L

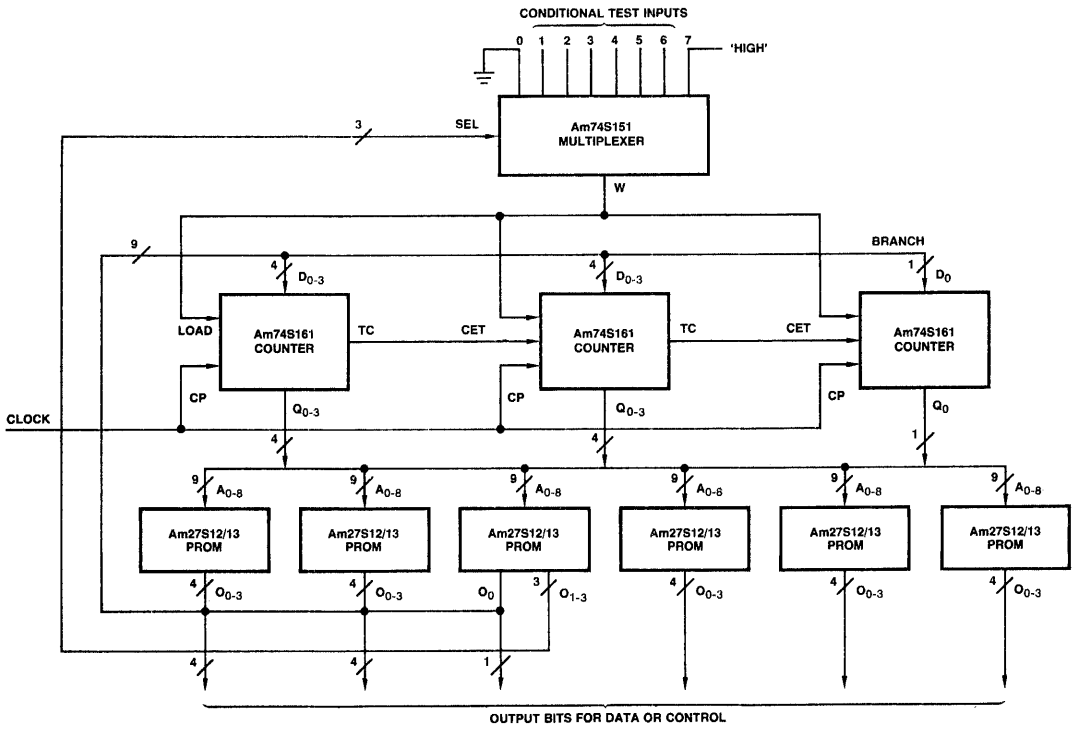
ASCII PAPER TAPE



BPM-008

APPLYING THE Am27S12 AND Am27S13

The Am27S12 and Am27S13 can be used with a high speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12 or Am27S13 PROMs.



BPM-009

Am27S18 • Am27S19

256-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 40ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

FUNCTIONAL DESCRIPTION

The Am27S18 and Am27S19 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am27S18 and three-state Am27S19 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_4 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

GENERIC SERIES CHARACTERISTICS

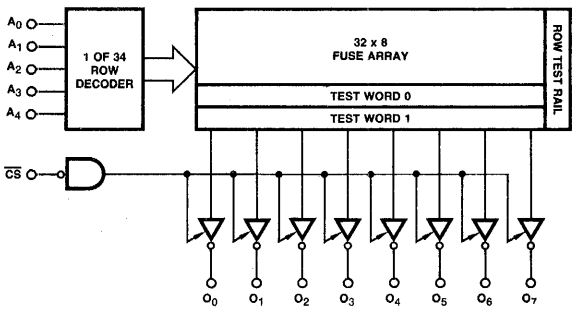
The Am27S18 and Am27S19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

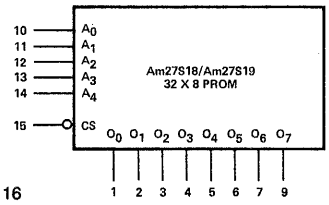
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



BPM-018

LOGIC SYMBOL



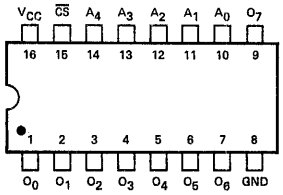
V_{CC} = Pin 16
GND = Pin 8

BPM-019

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S18DC
Hermetic DIP	−55°C to +125°C	AM27S18DM
Hermetic Flat Pak	−55°C to +125°C	AM27S18FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S19DC
Hermetic DIP	−55°C to +125°C	AM27S19DM
Hermetic Flat Pak	−55°C to +125°C	AM27S19FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-020

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to, +5mA

OPERATING RANGE

COM'L	Am27S18XC, Am27S19XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S18XM, Am27S19XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27LS19 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27LS19 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

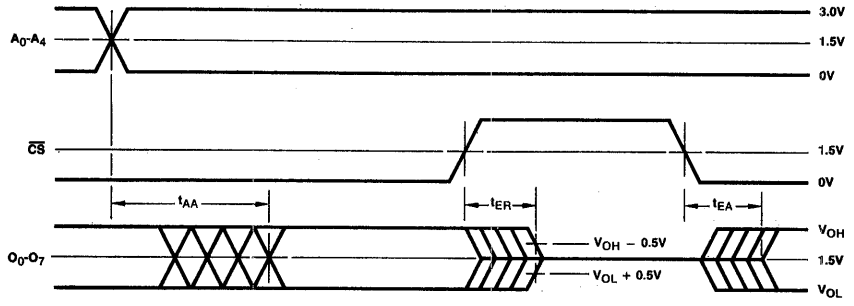
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	25	40	50	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



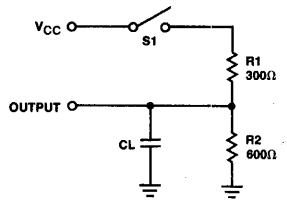
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

BPM-021

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-022

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PROGRAMMING

The Am27S18 and Am27S19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

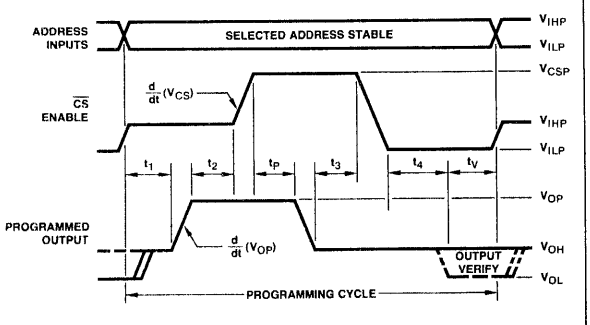
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

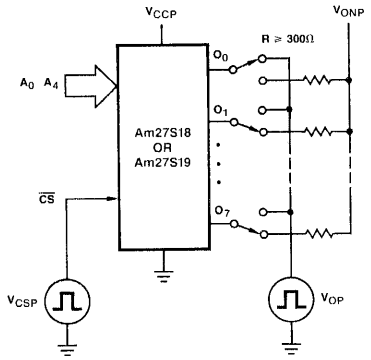
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-023

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-024

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S18 • Am27S19 ADAPTERS AND CONFIGURATOR	715-1407-1	PA16-6 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

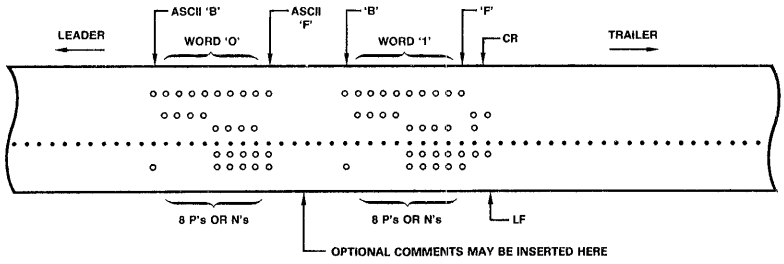
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
Ø02   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
Ø04   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
Ø06   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
Ø31   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
		⋮						⋮				
H	H	H	H	H	L	L	L	L	H	H	H	L

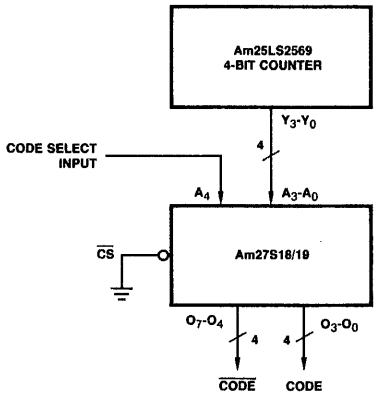
ASCII PAPER TAPE



BPM-025

APPLYING THE Am27S18 AND Am27S19

The Am27S18 and Am27S19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18 or Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



BPM-026

TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

Am27S20 • Am27S21

1024-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 45ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S20 and Am27S21 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

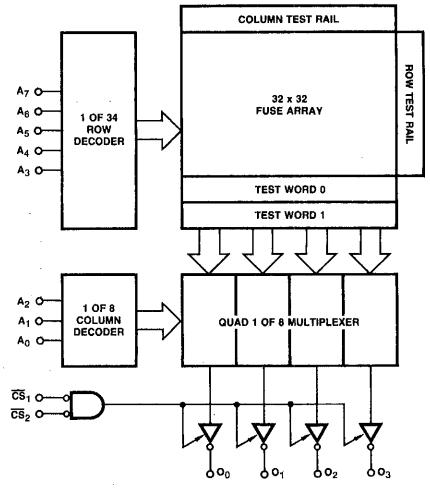
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S20DC
Hermetic DIP	−55°C to +125°C	AM27S20DM
Hermetic Flat Pak	−55°C to +125°C	AM27S20FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S21DC
Hermetic DIP	−55°C to +125°C	AM27S21DM
Hermetic Flat Pak	−55°C to +125°C	AM27S21FM

FUNCTIONAL DESCRIPTION

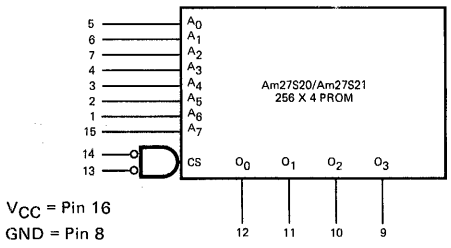
The Am27S20 and Am27S21 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector Am27S20 and three-state Am27S21 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_7 and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, at a logic LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



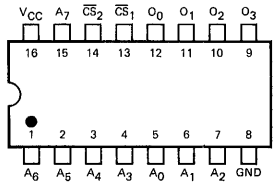
BPM-027

LOGIC SYMBOL



BPM-028

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-029

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S20XC, Am27S21XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S20XM, Am27S21XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S21 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am27S21 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $V_{\overline{CS1}}$ = 2.4V		V_O = 4.5V			40	μA
			Am27S21 only	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)				8		

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

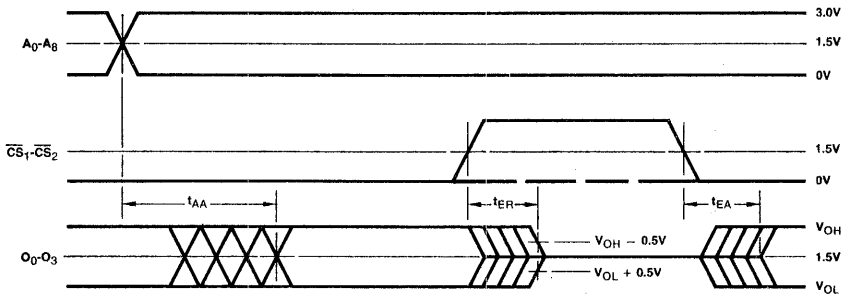
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	25	45	60	ns
t_{EA}	Enable Access Time		15	20	30	ns
t_{ER}	Enable Recovery Time		15	20	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

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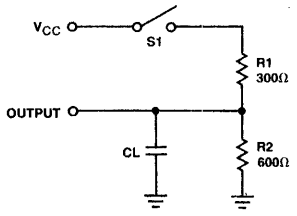
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
——— / ———	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



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5

PROGRAMMING

The Am27S20 and Am27S21 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

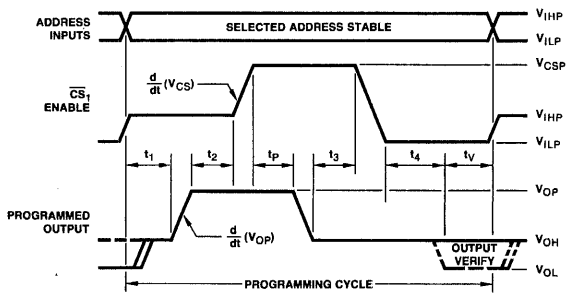
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

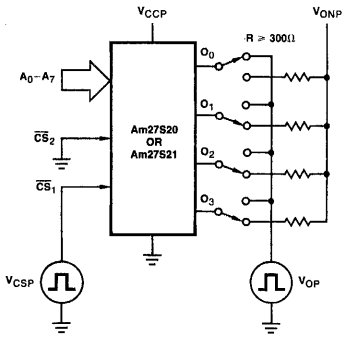
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-032

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-033

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S20 • Am27S21 ADAPTERS AND CONFIGURATOR	715-1408-1	PA16-5 and 256 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 256 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

5

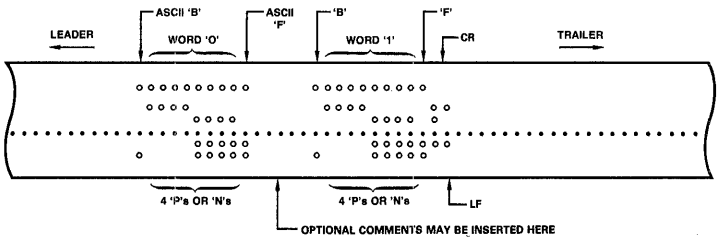
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 :     :::::    :
255   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}_1$ & $\overline{CS}_2$ = LOW)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	H	H	L	H	H	L	L
				⋮					⋮		
H	H	H	H	H	H	H	H	H	H	H	L

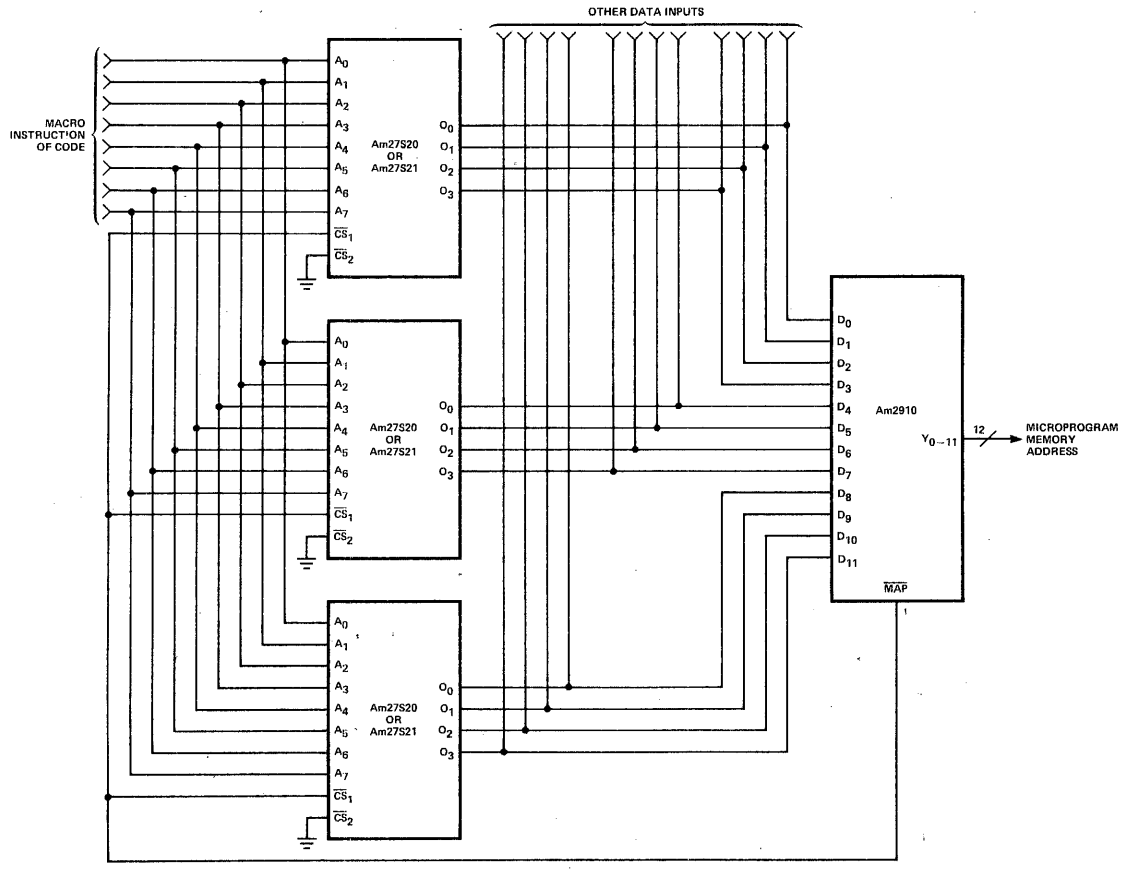
ASCII PAPER TAPE



BPM-034

APPLYING THE Am27S20/21

Typical application of the Am27S20/21 is shown below. The Am27S20/21's are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the A_{0-7} inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{CS}_1$ input of the Am27S20/21 such that when the $\overline{CS}_1$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20 or in the three-state mode in the case of the Am27S21. In both cases the $\overline{CS}_2$ input is grounded, thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.



MICROPROGRAMMING INSTRUCTION MAPPING

BPM-035

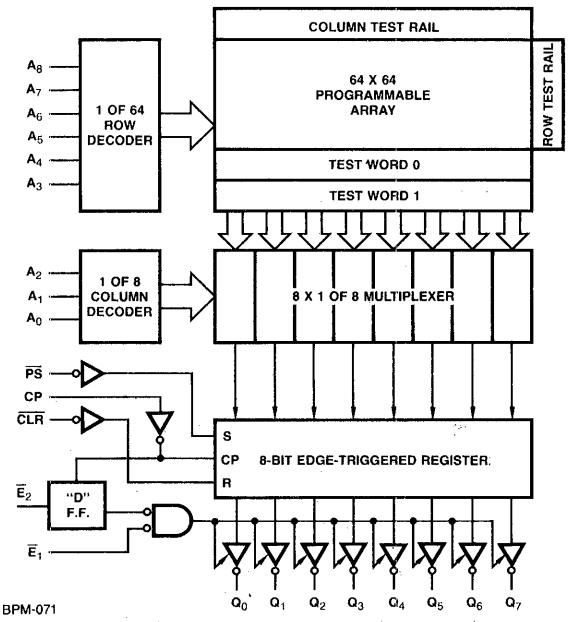
Am27S25

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common asynchronous $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- Space saving 24-pin package with 300 mil lateral centers
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current three-state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



BPM-071

FUNCTIONAL DESCRIPTION

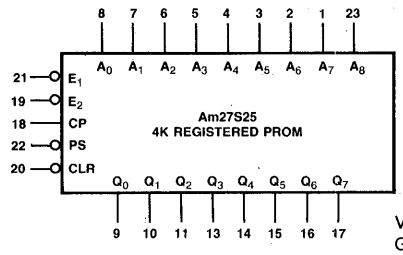
The Am27S25 is an electrically programmable Schottky TTL read only memory incorporating true D-type, master-slave data registers on chip. This device features the versatile 512 word by 8 bit organization and is available in the three-state Am27S25 output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S25 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_2$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_2$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}_1$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_2$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}_1$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered asynchronous $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs. These functions are common to all registers and are useful during power up timeout sequences. With outputs enabled the $\overline{\text{PS}}$ input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the $\overline{\text{CLR}}$ input is LOW, the internal flip-flops of the data register are reset and, a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

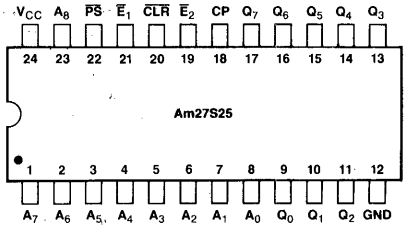
LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

BPM-072

CONNECTION DIAGRAM – Top View



BPM-073

Note: Pin 1 is marked for orientation.

5

GENERIC SERIES CHARACTERISTICS

The Am27S25 is a member of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM27S25XC	T_A = 0 to 75°C	V_{CC} = 5.0V ±5%
MIL	AM27S25XM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.			130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $\overline{VE}_1$ = 2.4V	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			12		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

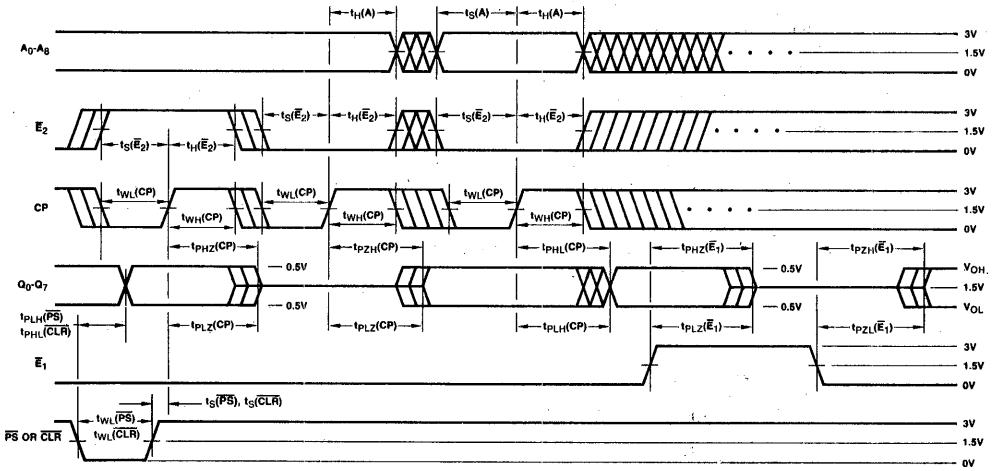
PRELIMINARY DATA

Parameter	Description	Test Conditions	T_A = 25°C, V_{CC} = 5.0V Typ	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF, S_1 closed. (See AC Test Load below)	35					ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15					ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15					ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10					ns
$t_S(\overline{E}_2)$	$\overline{E}_2$ to CP (HIGH) Setup Time		10					ns
$t_H(\overline{E}_2)$	$\overline{E}_2$ to CP (HIGH) Hold Time		10					ns
$t_{PLH}(\overline{PS})$	Delay from $\overline{PS}$ (LOW) to Output (HIGH)		17					ns
$t_{PHL}(\overline{CLR})$	Delay from $\overline{CLR}$ (LOW) to Output (LOW)		17					ns
$t_{WL}(\overline{PS})$	$\overline{PRESET}$ Pulse Width (LOW)		10					ns
$t_{WL}(\overline{CLR})$	$\overline{CLEAR}$ Pulse Width (LOW)		10					ns
$t_S(\overline{PS})$	$\overline{PS}$ Recovery (Inactive) to Clock (HIGH)		12					ns
$t_S(\overline{CLR})$	$\overline{CLR}$ Recovery (Inactive) to Clock (HIGH)		12					ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW)	C_L = 30pF, S_1 is closed for t_{PZL} and open for t_{PZH}	22					ns
$t_{PZL}(\overline{E}_1)$ $t_{PZH}(\overline{E}_1)$	Delay from $\overline{E}_1$ (LOW) to Active Output (HIGH or LOW)		22					ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or high Impedance)	C_L = 5pF (Note 1), S_1 closed for t_{PLZ} and open for t_{PHZ}	22					ns
$t_{PLZ}(\overline{E}_1)$ $t_{PHZ}(\overline{E}_1)$	Delay from $\overline{E}_1$ (HIGH) to Inactive Output (OFF or high Impedance)		22					ns

Notes: 1. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
2. Tests are performed with input 10 to 90% rise and fall times of 5ns or less.

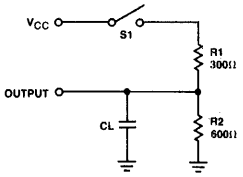
5

SWITCHING WAVEFORMS



BPM-074

AC TEST LOAD



BPM-075

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

PROGRAMMING

The Am27S25 is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

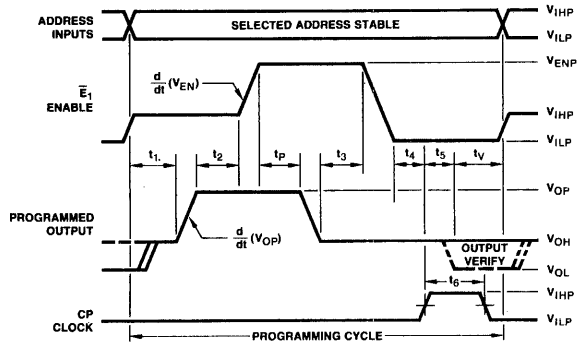
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.
5. $\overline{PS}$ and $\overline{CLR}$ must be connected to V_{IHP} during programming.

PROGRAMMING WAVEFORMS



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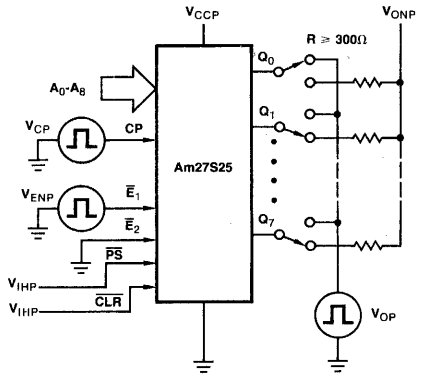
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S25 ADAPTERS AND CONFIGURATOR	715-1617	PA24-16 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

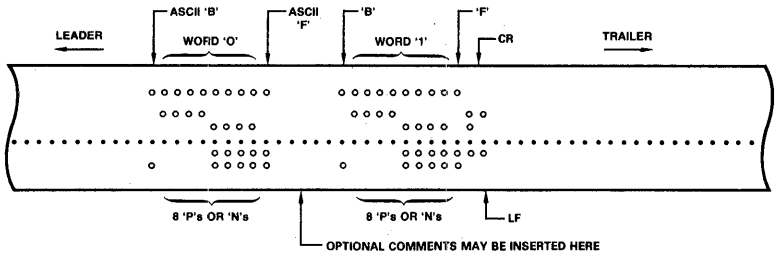
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE
($\overline{E}_1$ AND $\overline{E}_2$ LOW, $\overline{PS}$ AND $\overline{CLR}$ HIGH)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



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APPLYING THE Am27S25 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am27S25 registered PROM, the design engineer can upgrade the performance of existing systems or implement new system taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familar to many design engineers. This technique is called microprogramming.

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

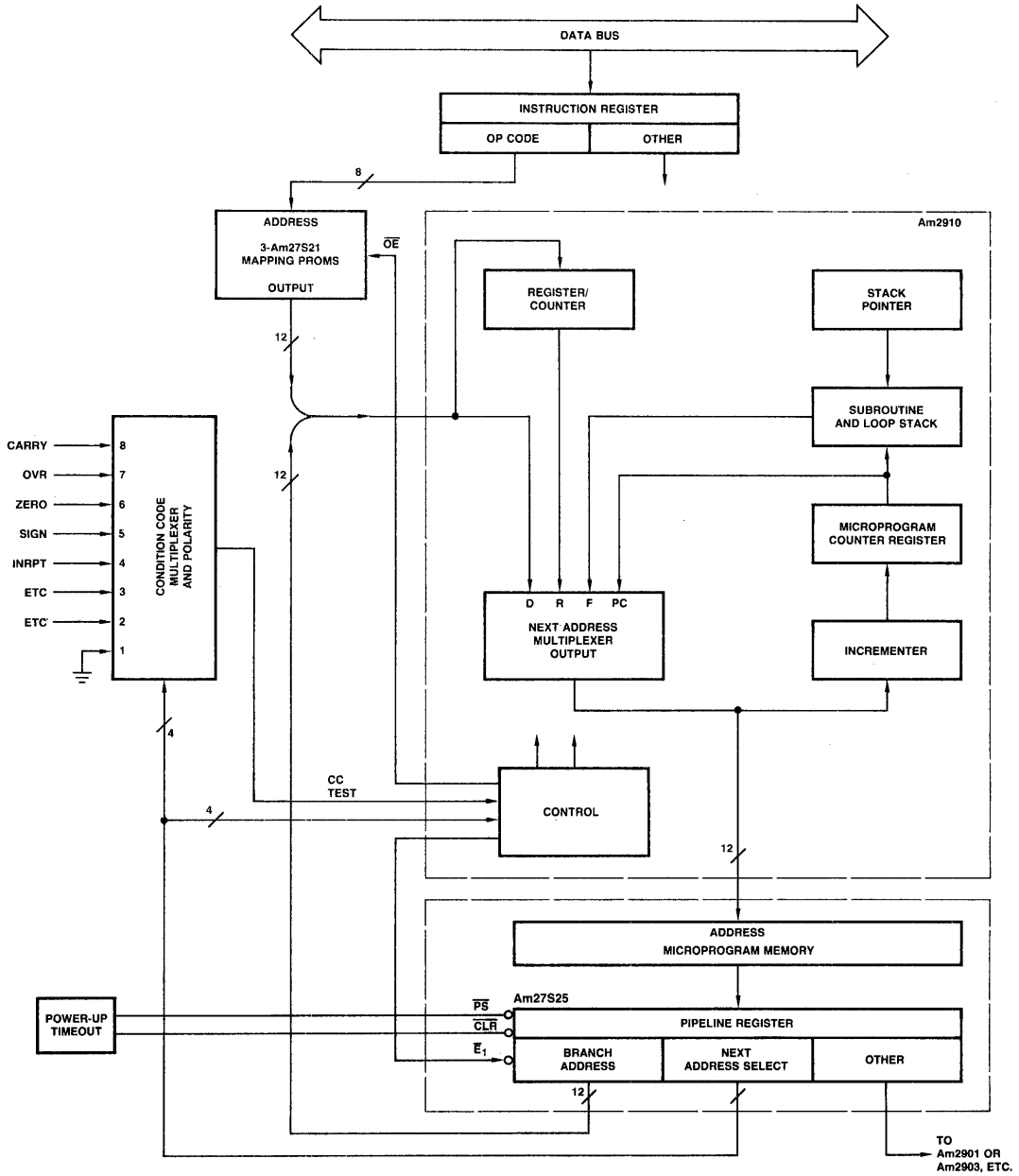

Figure 1. A Typical Computer Control Unit Using the Am27S25.

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APPLYING THE Am27S25 IN BIPOLAR MICROCOMPUTERS (Cont.)

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROM's for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction.

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am27S25 registered PROMs. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and file (F). The starting address decoder (mapping PROM) output and the Am27S25's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcyle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am27S25 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am27S25 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The Am27S25 contains a $\overline{\text{PRESET}}$ ($\overline{\text{PS}}$) and a $\overline{\text{CLEAR}}$ ($\overline{\text{CLR}}$) function that is useful for power-up operations and other initialization functions. These signals can also be used to provide "trap" jumps to the all zeros or ones addresses in microprogram memory.

The expansion scheme for increasing the depth of Am27S25 is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am27S25 registered PROMs is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

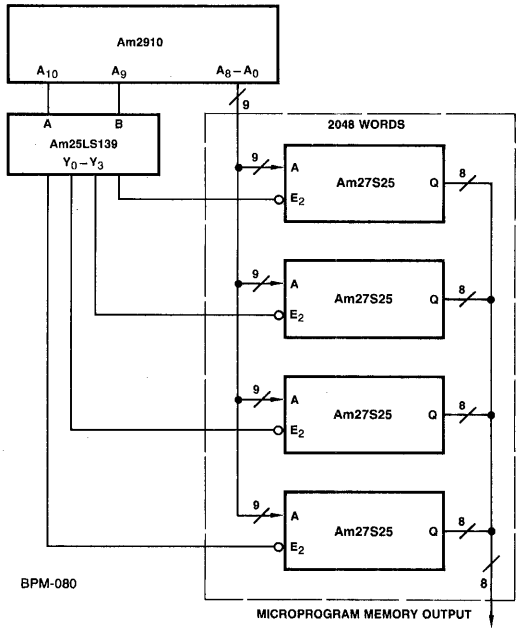

Figure 2. Word Expansion Scheme for the Am27S25.

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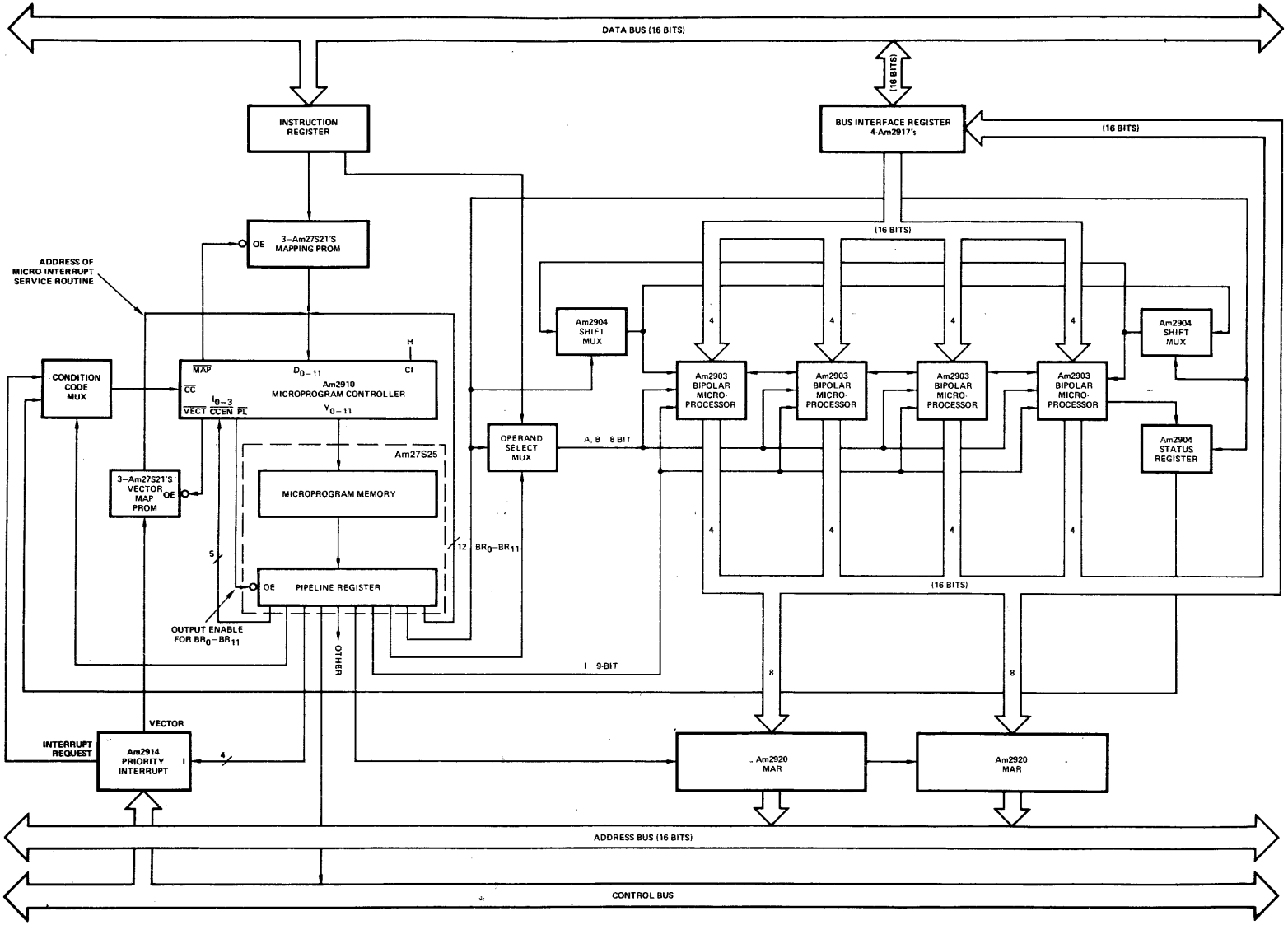
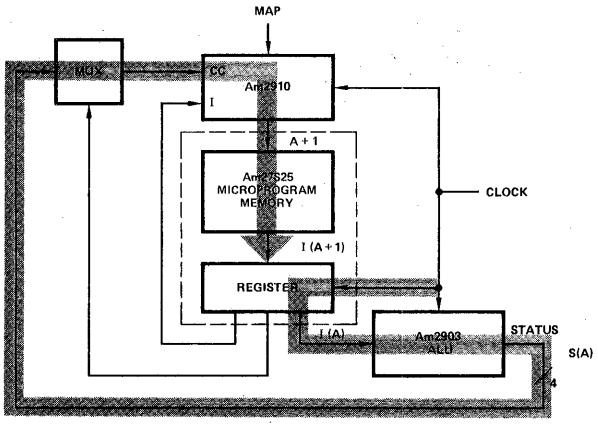
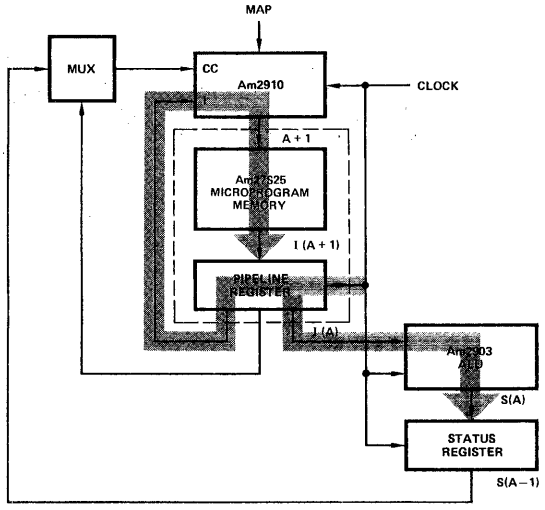


Figure 3. Typical Bipolar Microcomputer Using the Am27S25.

USING THE Am27S25 IN A PIPELINED ARCHITECTURE



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.



One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am27S25 reduces the parts count of the microprogram memory/pipeline by a factor of two.

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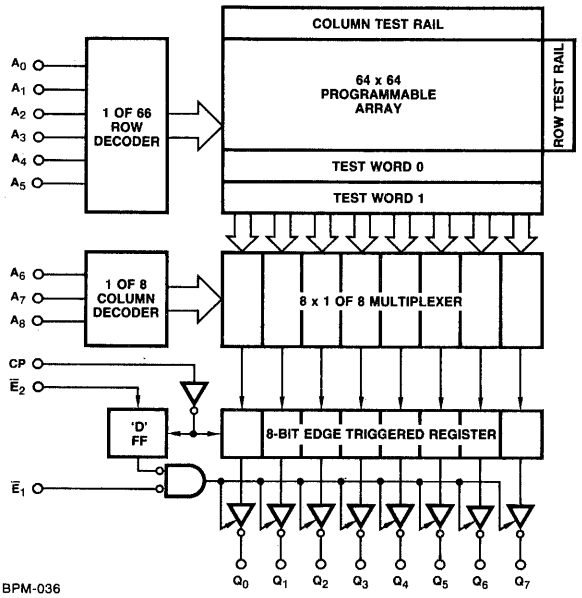
Am27S26 • Am27S27

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Space saving 22 pin package
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



BPM-036

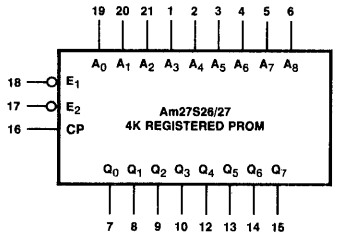
FUNCTIONAL DESCRIPTION

The Am27S26 and Am27S27 are electrically programmable Schottky TTL read only memories incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512 word by 8 bit organization and are available in both the open collector Am27S26 and three-state Am27S27 output versions. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed system and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S26 and Am27S27 also offer maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_2$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_2$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}_1$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_2$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}_1$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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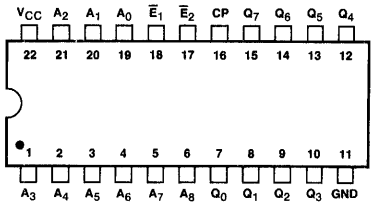
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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GENERIC SERIES CHARACTERISTICS

The Am27S26 and Am27S27 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM27S26XC, AM27S27XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	AM27S26XM, AM27S27XM	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S27 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am27S27 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $V\overline{E}_1$ = 2.4V		V_O = 4.5V			100	μA
			Am27S27 Only	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)				5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)				12		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

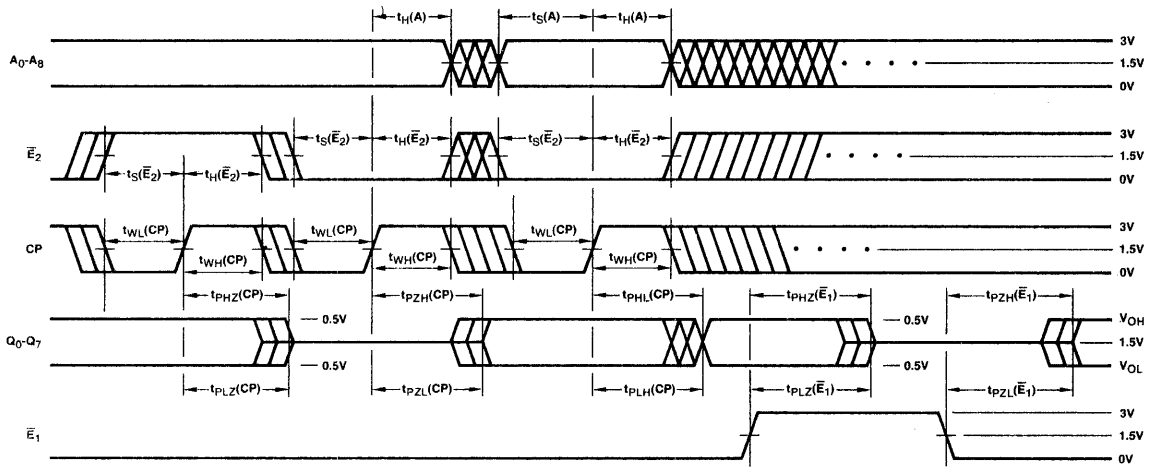
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

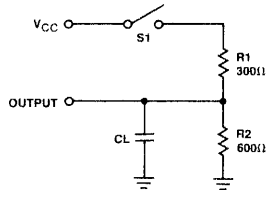
Parameter	Description	Test Conditions	Typ 5V 25°C	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF S_1 closed. (See AC Test Load below)	40	55		65		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0		0		ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		27		30	ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10		30		40	ns
$t_S(E_2)$	E_2 to CP (HIGH) Setup Time		10	25		30		ns
$t_H(E_2)$	E_2 to CP (HIGH) Hold Time		−10	0		0		ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 1)	C_L = 30pF S_1 closed for t_{PZL} and open for t_{PZH}	15		35		45	ns
$t_{PZL}(E_1)$ $t_{PZH}(E_1)$	Delay from E_1 (LOW) to Active Output (HIGH or LOW) (Note 1)		15		40		45	ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or high Impedance) (Note 1)	C_L = 5pF (Note 2) S_1 closed for t_{PLZ} and open for t_{PHZ}	15		35		45	ns
$t_{PLZ}(E_1)$ $t_{PHZ}(E_1)$	Delay from E_1 (HIGH) to Inactive Output (OFF or high Impedance) (Note 1)		10		30		40	ns

Notes: 1. t_{PHZ} and t_{PZH} apply to the three-state Am27S27 only.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input 10 to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS



AC TEST LOAD



BPM-040

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING

The Am27S26 and Am27S27 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

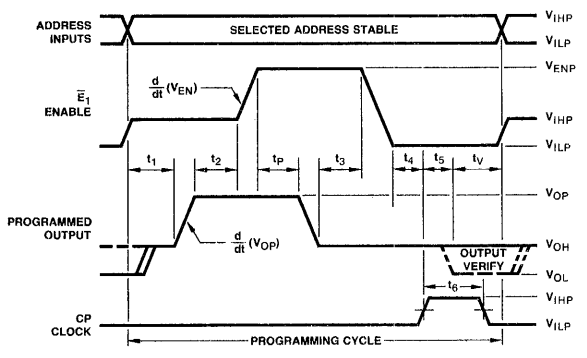
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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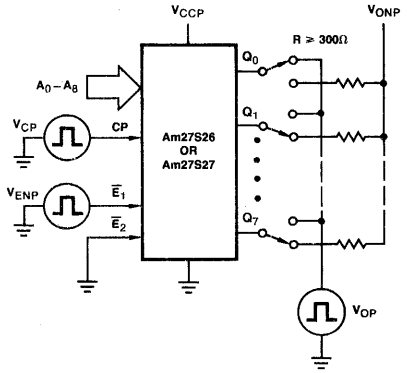
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-042

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S26 • Am27S27 ADAPTERS AND CONFIGURATOR	715-1412-2	PA22-4 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

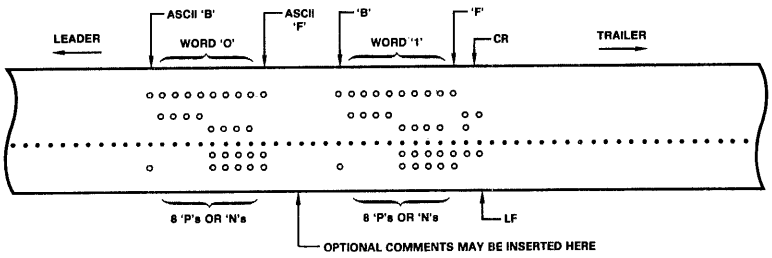
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 •     ••••••••••    •
 •     ••••••••••    •
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{E}_1$ AND $\overline{E}_2$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-043

APPLYING THE Am27S26 AND Am27S27 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am27S26/27 registered PROM, the design engineer can upgrade the performance of existing systems or implement new systems taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familiar to many design engineers. This technique is called microprogramming.

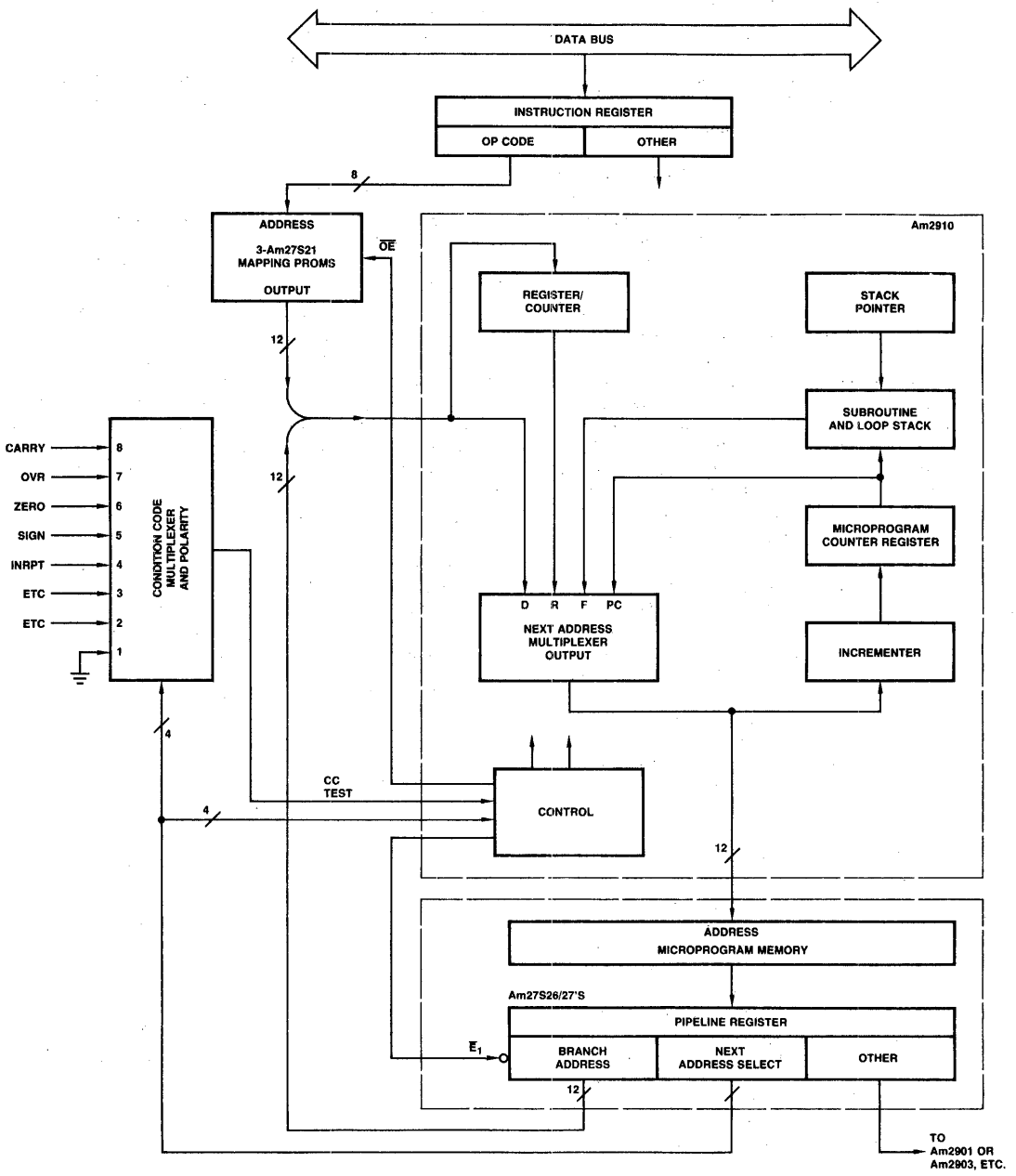


Fig. 1. A Typical Computer Control Unit using the Am27S26/27.

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5

APPLYING THE Am27S26 and Am27S27 IN BIPOLAR MICROCOMPUTERS (Cont.)

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROM's for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am27S26/27 registered PROM's. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and the file (F). The starting address decoder (mapping PROM) output and the Am27S26/27's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcyle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am27S26/27 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am27S26/27 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The expansion scheme for increasing the depth of Am27S26/27's is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am27S26/27 registered PROM's is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

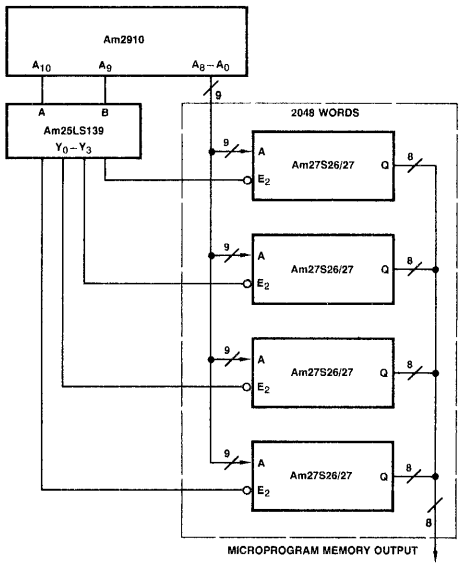

Fig. 2. Word Expansion Scheme for the Am27S26 and Am27S27.

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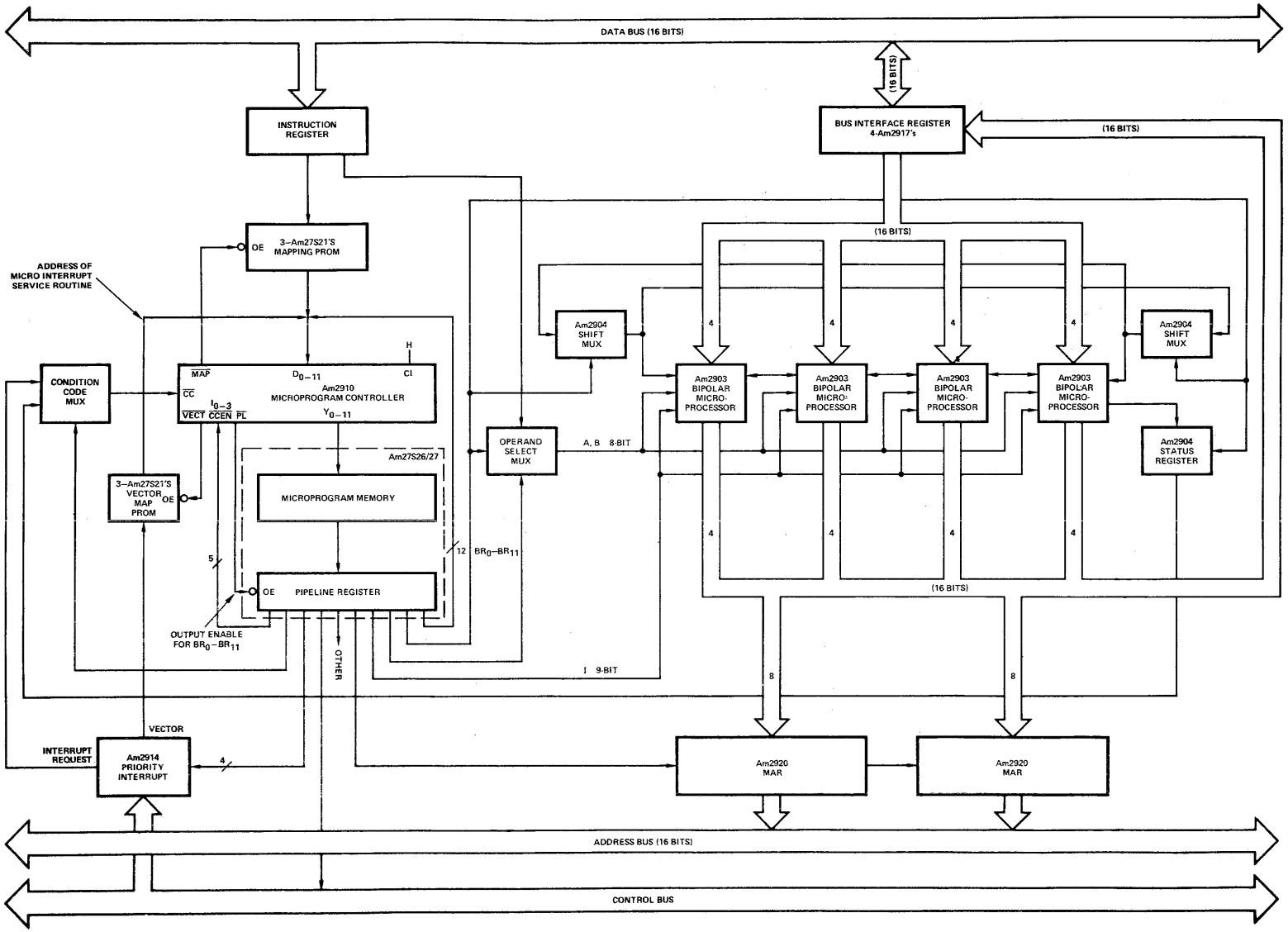
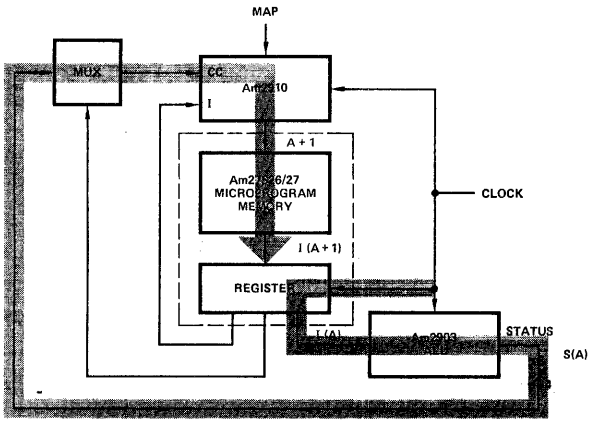


Fig. 3. Typical Bipolar Microcomputer using the Am27S26/27.

BPM-046

USING THE Am27S26/27 IN A PIPELINED ARCHITECTURE



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

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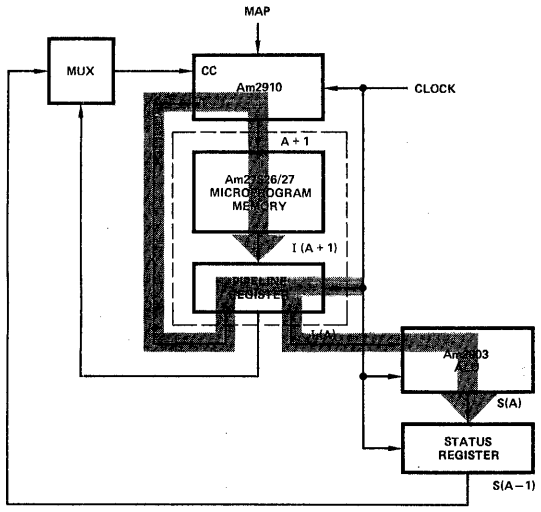

One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am27S26/27 reduces the parts count of the microprogram memory/pipeline by a factor of two.

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ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0°C to +75°C	AM27S26DC
Hermetic DIP	−55°C to +125°C	AM27S26DM
	Three-State Outputs	
Hermetic DIP	0°C to +75°C	AM27S27DC
Hermetic DIP	−55°C to +125°C	AM27S27DM

Am27S28 • Am27S29

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S28 and Am27S29 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test rows are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

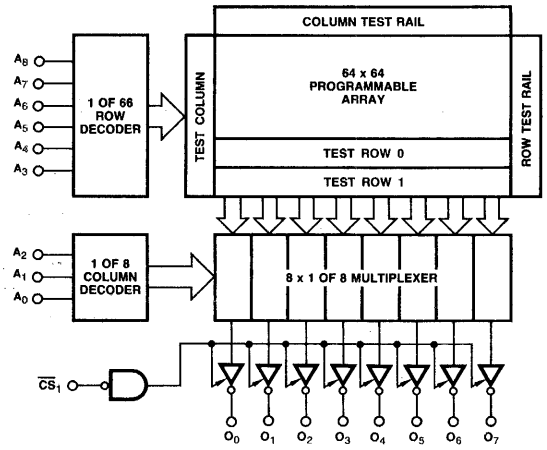
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S28DC
Hermetic DIP	−55°C to +125°C	AM27S28DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S29DC
Hermetic DIP	−55°C to +125°C	AM27S29DM

FUNCTIONAL DESCRIPTION

The Am27S28 and Am27S29 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S28 and three-state Am27S29 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

BLOCK DIAGRAM



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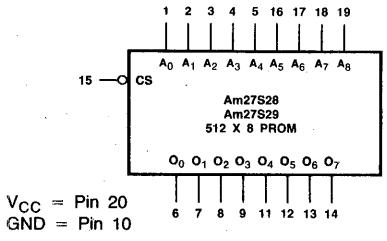
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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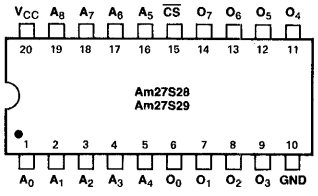
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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5

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S28XC, Am27S29XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S28XM, Am27S29XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S29 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S29 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		105	160	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S29 only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S29 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S29 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

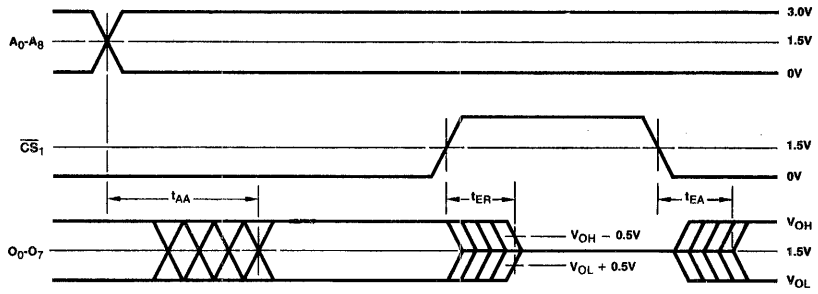
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	35	55	70	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



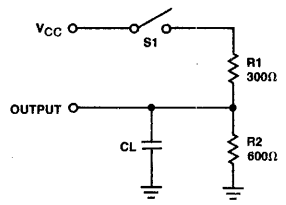
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

BPM-086

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-087

PROGRAMMING

The Am27S28 and Am27S29 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

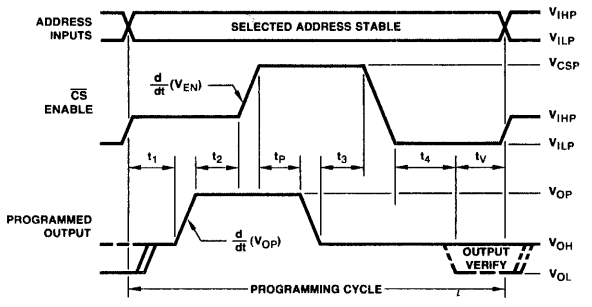
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	v/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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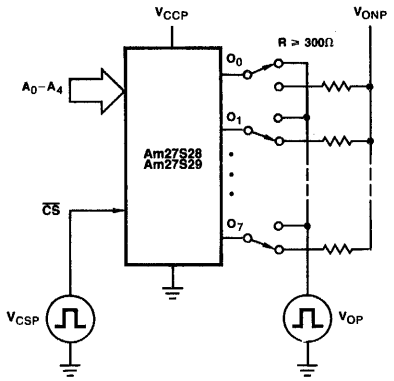
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-089

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S28 • Am27S29 ADAPTERS AND CONFIGURATOR	715-1413	PA20-4 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

5

TYPICAL PAPER TAPE FORMAT

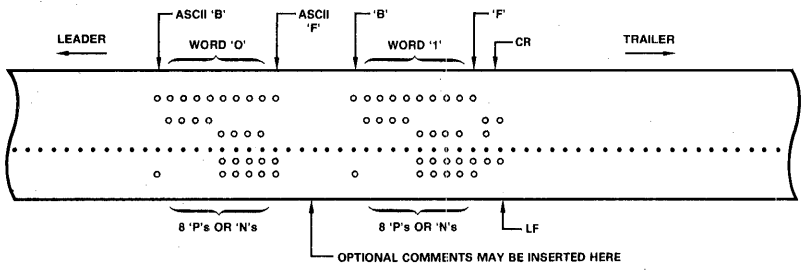
```
øøø   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
øø2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
øø4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
øø6   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-017

Am27S32 • Am27S33

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S32 and Am27S33 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

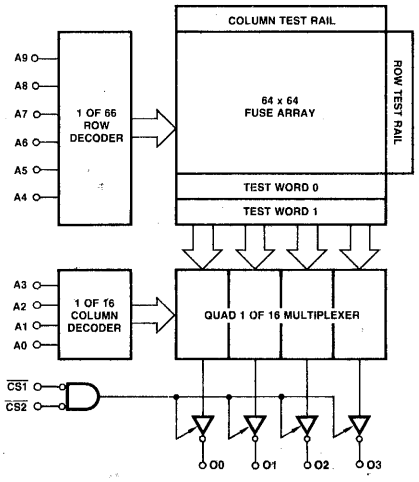
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0°C to +75°C	AM27S32DC
Hermetic DIP	−55°C to +125°C	AM27S32DM
	Three-State Outputs	
Hermetic DIP	0°C to +75°C	AM27S33DC
Hermetic DIP	−55°C to 125°C	AM27S33DM

FUNCTIONAL DESCRIPTION

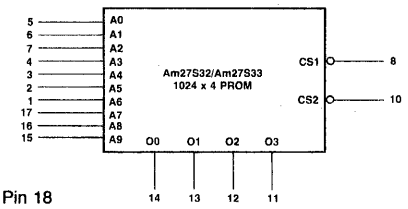
The Am27S32 and Am27S33 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 4 configuration, they are available in both open collector Am27S32 and three-state Am27S33 output versions. After programming, stored information is read on outputs O0–O3 by applying unique binary addresses to A0–A9 and holding the chip select inputs, $\overline{CS1}$ and $\overline{CS2}$, LOW. If either chip select input goes to a logic HIGH, O0–O3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-090

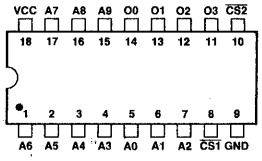
LOGIC SYMBOL



VCC = Pin 18
GND = Pin 9

BPM-091

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-092

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +VCC max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S32XC, Am27S33XC	T_A = 0°C to +75°C	VCC = 5.0V ±5%
MIL	Am27S32XM, Am27S33XM	T_A = −55°C to +125°C	VCC = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
VOH (Am27S33 only)	Output HIGH Voltage	VCC = MIN., IOH = −2.0mA VIN = VIH or VIL			2.4			Volts
VOL	Output LOW Voltage	VCC = MIN., IOL = 16mA VIN = VIH or VIL					0.45	Volts
VIH	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
VIL	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
IIL	Input LOW Current	VCC = MAX., VIN = 0.45V				−0.020	−0.250	mA
IIH	Input HIGH Current	VCC = MAX., VIN = 2.7V					25	μA
II	Input HIGH Current	VCC = MAX., VIN = 5.5V					1.0	mA
ISC (Am27S33 only)	Output Short Circuit Current	VCC = MAX., VOUT = 0.0V (Note 2)			−20	−40	−90	mA
ICC	Power Supply Current	All inputs = GND VCC = MAX.		COM'L		105	140	mA
				MIL		105	145	
VI	Input Clamp Voltage	VCC = MIN., IIN = −18mA					−1.2	Volts
ICEX	Output Leakage Current	VCC = MAX. $\overline{VCS1}$ = 2.4V		VO = 4.5V			40	μA
			Am27S33 only	VO = 2.4V			40	
				VO = 0.4V			−40	
CIN	Input Capacitance	VIN = 2.0V @ f = 1MHz (Note 3)				5		pF
COUT	Output Capacitance	VOUT = 2.0V @ f = 1MHz (Note 3)				12		

Notes: 1. Typical limits are at VCC = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

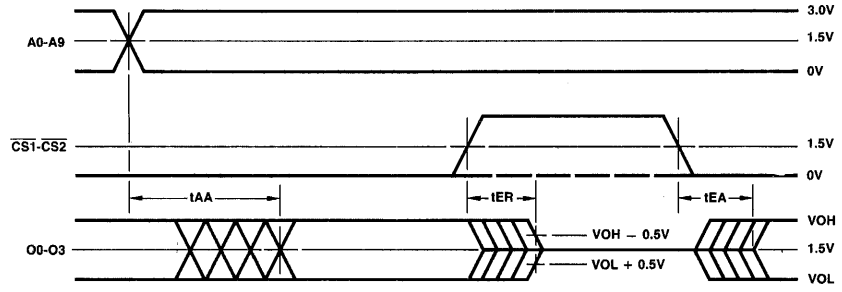
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	38	55	70	ns
t_{EA}	Enable Access Time		10	25	30	ns
t_{ER}	Enable Recovery Time		10	25	30	ns

Notes: 1. tAA is tested with switch S1 closed and CL = 30pF.
2. For open collector outputs, tEA and tER are tested with S1 closed to the 1.5V output level. CL = 30pF.
3. For three state outputs, tEA is tested with CL = 30pF to the 1.5V level; S1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. tER is tested with CL = 5pF. HIGH to high impedance tests are made with S1 open to an output voltage of VOH − 0.5V; LOW to high impedance tests are made with S1 closed to the VOL + 0.5V level.

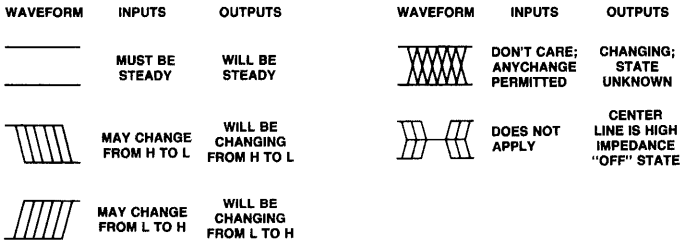
SWITCHING CHARACTERISTICS



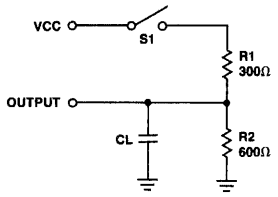
Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

BPM-093

KEY TO TIMING DIAGRAM



AC TEST LOAD



BPM-094

PROGRAMMING

The Am27S32 and Am27S33 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycle. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including VCC should be removed for a period of 5 seconds after which programming may be resumed.

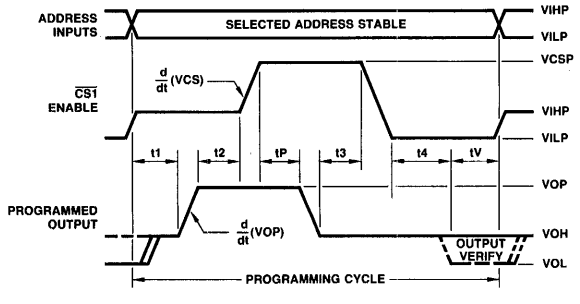
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
VCCP	VCC During Programming	5.0	5.5	Volts
VIHP	Input HIGH Level During Programming	2.4	5.5	Volts
VILP	Input LOW Level During Programming	0.0	0.45	Volts
VCSP	$\overline{CS1}$ Voltage During Programming	14.5	15.5	Volts
VOP	Output Voltage During Programming	19.5	20.5	Volts
VONP	Voltage on Outputs. Not to be Programmed	0	VCCP+0.3	Volts
IONP	Current into Outputs Not to be Programmed		20	mA
d(VOP)/dt	Rate of Output Voltage Change	20	250	V/μsec
d(VCS)/dt	Rate of $\overline{CS1}$ Voltage Change	100	1000	V/μsec
tP	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5	15	msec

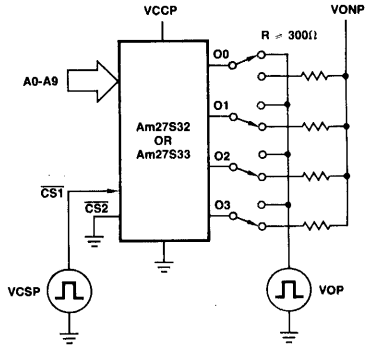
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e. not to the midpoints.
2. Delays t1, t2, t3 and t4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During tv, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to VONP through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-095

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-096

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each base part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S32 • Am27S33 ADAPTERS AND CONFIGURATOR	715-1414	PA 18-6 and 1024 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 1024 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

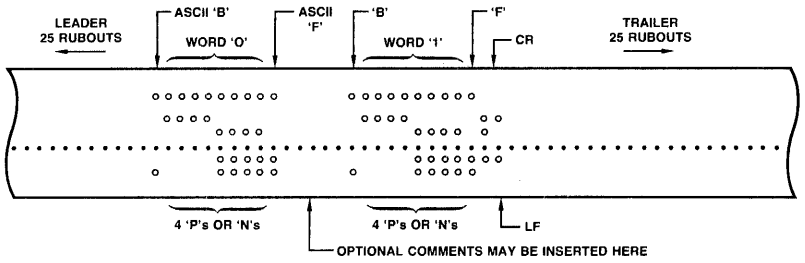
ØØØ	BNNNPF	WORD ZERO (R) (L)
	BPPNNF	COMMENT FIELD (R) (L)
ØØ2	BPPPNF	ANY (R) (L)
	BNNNNF	TEXT (R) (L)
ØØ4	BNNNPF	CAN (R) (L)
	BPPNNF	GO (R) (L)
ØØ6	BPPNNF	HERE (R) (L)
•	•••••••	•
•	•••••••	•
1024	BPPPNF	END (R) (L)

RESULTING DEVICE TRUTH TABLE

($\overline{CS1}$ and $\overline{CS2}$ = LOW)

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O3	O2	O1	O0
L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	L	H	H	L	H	H	L	L
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	H	H	H	H	H	H	H	H	H	H	H	H	L

ASCII PAPER TAPE



BPM-097

Am27S180 • Am27S181

8192-Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- High Speed – 60ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S180 and Am27S181 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

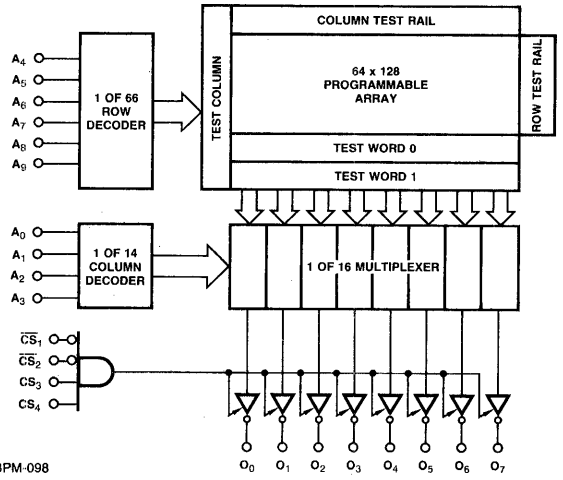
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S180DC
Hermetic DIP	−55°C to +125°C	AM27S180DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S181DC
Hermetic DIP	−55°C to +125°C	AM27S181DM

FUNCTIONAL DESCRIPTION

The Am27S180 and Am27S181 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 8 configuration, they are available in both open collector Am27S180 and three-state Am27S181 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_9 and enabling the chip ($\overline{CS}_1$, $\overline{CS}_2$, low and CS_3, CS_4 high). Changes of chip select input levels disables the outputs causing them to go to the off or high impedance state.

BLOCK DIAGRAM



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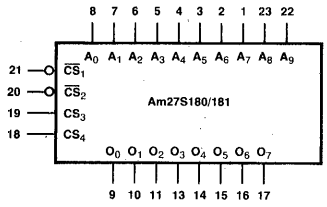
LOGIC DIAGRAM

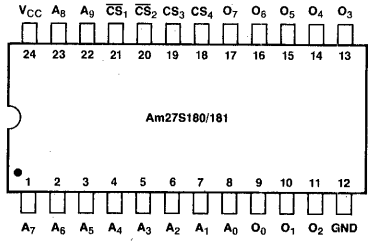


BPM-099

V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM

Top View



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Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

COM'L	Am27S180XC, Am27S181XC	T_A = 0 to 75°C	V_{CC} = 5.0V ±5%
MIL	Am27S180XM, Am27S181XM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S181 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am27S181 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				120	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}1,2}$ = 2.4V $V_{CS3,4}$ = 0.4V		V_O = 4.5V			40	μA
			Am27S181 Only	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)				5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)				12		

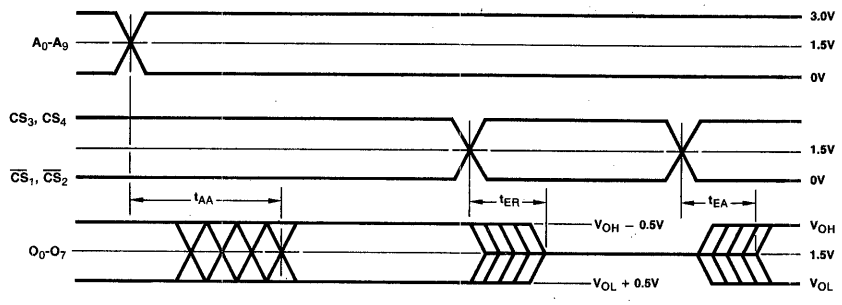
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE
PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	40	60	80	ns
t_{EA}	Enable Access Time		20	40	50	ns
t_{ER}	Enable Recovery Time		20	40	50	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING CHARACTERISTICS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

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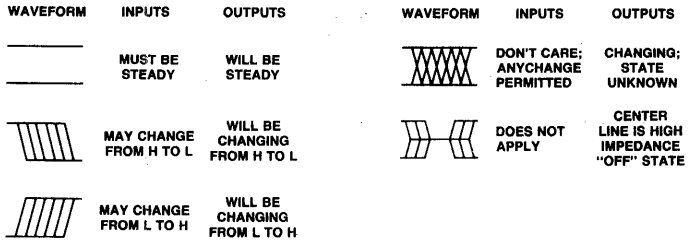
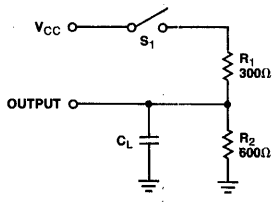
KEY TO TIMING DIAGRAM



AC TEST LOAD



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PROGRAMMING

The Am27S180 and Am27S181 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

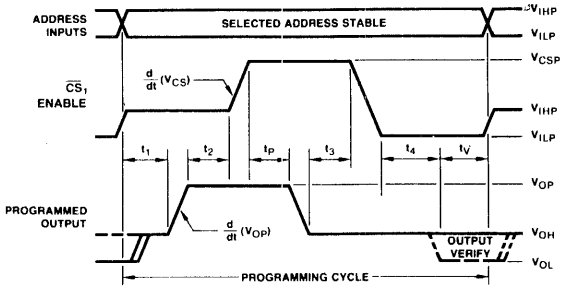
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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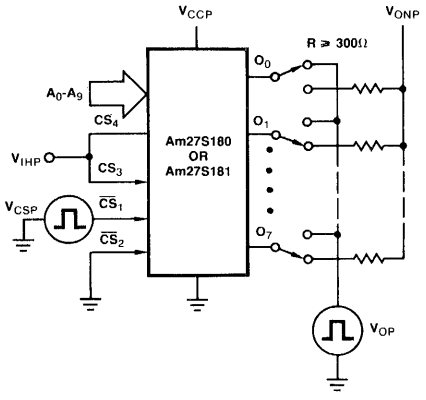
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-104

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S180 • Am27S181 ADAPTERS AND CONFIGURATOR	715-1545-2	PA24-13 and 1024 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 1024 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

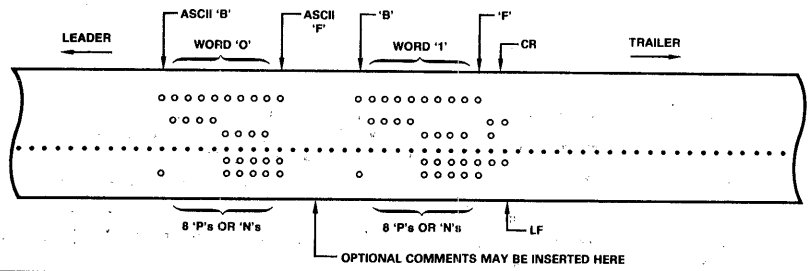
```
ØØØ   BPNPPNNNPF   WORD ZERO Ⓡ Ⓛ
      BPPPPPPNNF   COMMENT FIELD Ⓡ Ⓛ
ØØ2   BNNNPPPPNF   ANY Ⓡ Ⓛ
      BNNNNNNNNF   TEXT Ⓡ Ⓛ
ØØ4   BPNNNNNNPF   CAN Ⓡ Ⓛ
      BNPPNPPNNF   GO Ⓡ Ⓛ
ØØ6   BPNNPPPNNF   HERE Ⓡ Ⓛ
 :    ::::::::::::   :
1023  BNNNNPPPNF   END Ⓡ Ⓛ
```

Ⓡ = CARRIAGE RETURN
Ⓛ = LINE FEED

RESULTING DEVICE TRUTH TABLE
($\overline{CS}_1$ AND $\overline{CS}_2$ LOW, CS_3 AND CS_4 HIGH)

A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮										⋮							
H	H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-105

Am27S184 • Am27S185

8192-Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S184 and Am27S185 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

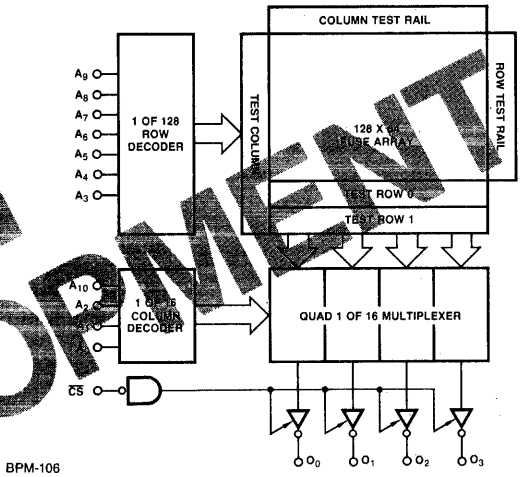
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0 to +75°C	AM27S184DC
Hermetic DIP	−55 to +125°C	AM27S184DM
Three-State Outputs		
Hermetic DIP	0 to +75°C	AM27S185DC
Hermetic DIP	−55 to +125°C	AM27S185DM

FUNCTIONAL DESCRIPTION

The Am27S184 and Am27S185 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 2048 x 4 configuration, they are available in both open collector Am27S184 and three-state Am27S185 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{10} and holding the chip select input $\overline{CS}$ LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high-impedance state.

BLOCK DIAGRAM



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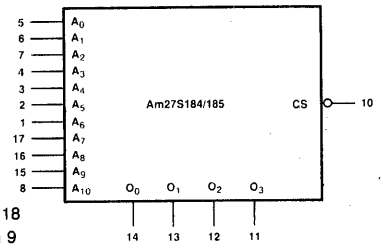
LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

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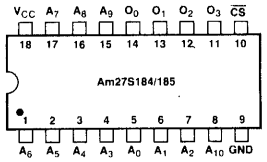
CONNECTION DIAGRAM
Top View



Note 1: Pin 1 is marked for orientation

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

COM'L	Am27S184XC, Am27S185XC	T_A = 0 to 75°C	V_{CC} = 5.0V ±5%
MIL	Am27S184XM, Am27S185XM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH} (Am27S185 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.020	−.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			40	mA
I_{SC} (Am27S185 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		80	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}}$ = 2.4V			40	μA
		Am27S185 only, V_O = V_{CC}			40	
		Am27S185 only, V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)		8		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

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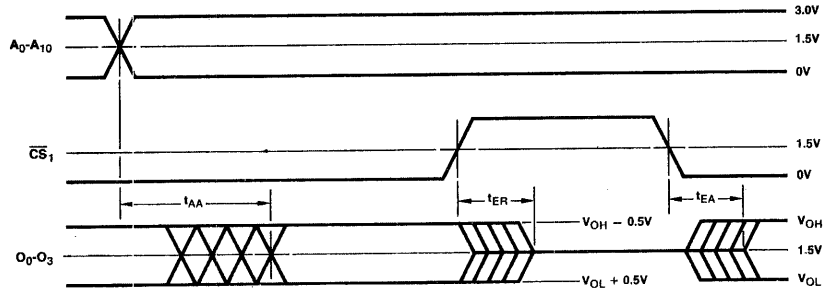
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ	Max		Units
			5V 25°C	COM'L	MIL	
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	40	–	–	ns
t_{EA}	Enable Access Time		10	–	–	ns
t_{ER}	Enable Recovery Time		10	–	–	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING CHARACTERISTICS



Note: Level on output while either $\overline{CS}_1$ is HIGH is determined externally.

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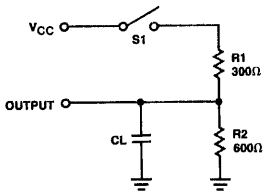
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANYCHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



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PROGRAMMING

The Am27S184 and Am27S185 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

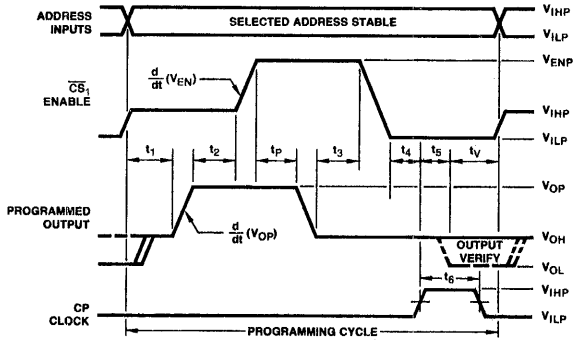
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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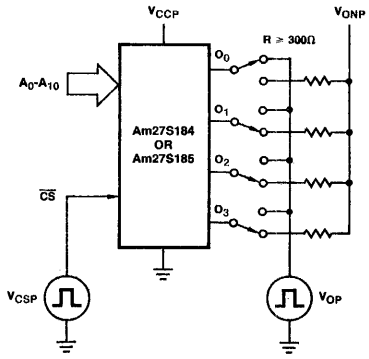
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S184 • Am27S185 ADAPTERS AND CONFIGURATOR	715-1616	PA18-8 and 2048 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 2048 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

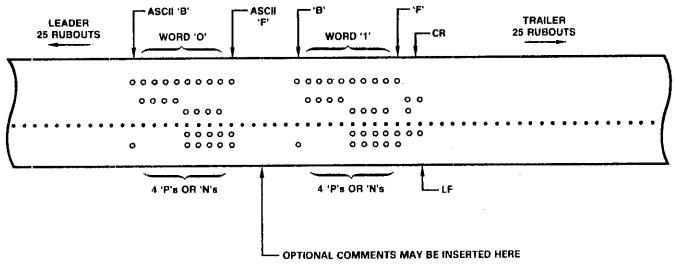
TYPICAL PAPER TAPE FORMAT

ØØØ	BNNNPF	WORD ZERO (R) (L)
	BPPNNF	COMMENT FIELD (R) (L)
ØØ2	BPPPNF	ANY (R) (L)
	BNNNNF	TEXT (R) (L)
ØØ4	BNNNPF	CAN (R) (L)
	BPPNNF	GO (R) (L)
ØØ6	BPPNNF	HERE (R) (L)
•	•	•
2047	BPPPNF	END (R) (L)

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ LOW)

A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	L	L	H	H	L	H	H	L	L
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

ASCII PAPER TAPE



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ADVANCED MOS/LSI

Advanced Micro Devices is an industry leader in the production of high-technology MOS products. The company's n-channel, silicon-gate MOS process is ideally suited for the dense, high-speed memory and microprocessor products required by today's systems.

Although most of the MOS products are oriented toward the Am9080A 8-bit MOS microprocessor, the static RAM's are ideal for use with the Am2900 family. The access times of these devices are often well matched to 2900 system microcycle times and provide significant cost benefits over bipolar memories of the same density.

Of particular interest to users of the Am2900 family are the Am9244/9044 and Am9124/9114 4096-bit RAMs. These devices are organized as 4K x 1 and as 1K x 4 and are available with access times to 200ns. The Am9147 is a 4K x 1 bit with access times as fast as 55ns.

Complete data on these devices is included in the following pages, along with our 16K dynamic RAM, the Am9016. The selection guide on the next few pages lists other Advanced MOS products which may be of interest. Most of these products are available for full military temperature range operation. For complete data on our MOS products, see our MOS/LSI Data Book.

MOS MEMORY SELECTION GUIDE

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltage	Outputs	Data I/O Configuration	Package Pins	Operating Power Max. (mW)	Standby Power Max. (mW)	
Am9101A	256 x 4	500	C, M	+5	3-State	Separate	22	290	46	
Am91L01A	256 x 4	500	C, M	+5	3-State	Separate	22	173	37	
Am9101B	256 x 4	400	C, M	+5	3-State	Separate	22	290	46	
Am91L01B	256 x 4	400	C, M	+5	3-State	Separate	22	173	37	
Am9101C	256 x 4	300	C, M	+5	3-State	Separate	22	315	46	
Am91L01C	256 x 4	300	C, M	+5	3-State	Separate	22	189	37	
Am9101D	256 x 4	250	C	+5	3-State	Separate	22	315	46	
Am9102	1024 x 1	650	C, M	+5	3-State	Separate	16	263	42	
Am91L02	1024 x 1	650	C, M	+5	3-State	Separate	16	158	35	
Am9102A	1024 x 1	500	C, M	+5	3-State	Separate	16	263	42	
Am91L02A	1024 x 1	500	C, M	+5	3-State	Separate	16	158	35	
Am9102B	1024 x 1	400	C, M	+5	3-State	Separate	16	263	42	
Am91L02B	1024 x 1	400	C, M	+5	3-State	Separate	16	158	35	
Am9102C	1024 x 1	300	C, M	+5	3-State	Separate	16	290	42	
Am91L02C	1024 x 1	300	C, M	+5	3-State	Separate	16	173	35	
Am9102D	1024 x 1	250	C	+5	3-State	Separate	16	290	42	
Am9111A	256 x 4	500	C, M	+5	3-State	Bussed	18	290	46	
Am91L11A	256 x 4	500	C, M	+5	3-State	Bussed	18	173	37	
Am9111B	256 x 4	400	C, M	+5	3-State	Bussed	18	290	46	
Am91L11B	256 x 4	400	C, M	+5	3-State	Bussed	18	173	37	
Am9111C	256 x 4	300	C, M	+5	3-State	Bussed	18	315	46	
Am91L11C	256 x 4	300	C, M	+5	3-State	Bussed	18	189	37	
Am9111D	256 x 4	250	C	+5	3-State	Bussed	18	315	46	
Am9112A	256 x 4	500	C, M	+5	3-State	Bussed	16	290	46	
Am91L12A	256 x 4	500	C, M	+5	3-State	Bussed	16	173	37	
Am9112B	256 x 4	400	C, M	+5	3-State	Bussed	16	290	46	
Am91L12B	256 x 4	400	C, M	+5	3-State	Bussed	16	173	37	
Am9112C	256 x 4	300	C, M	+5	3-State	Bussed	16	315	46	
Am91L12C	256 x 4	300	C, M	+5	3-State	Bussed	16	189	37	
Am9112D	256 x 4	250	C	+5	3-State	Bussed	16	315	46	
Am9114B	1024 x 4	450	C, M	+5	3-State	Bussed	18	367		
Am9114C	1024 x 4	300	C, M	+5	3-State	Bussed	18	367		
Am9114E	1024 x 4	200	C	+5	3-State	Bussed	18	367		
Am91L14B	1024 x 4	450	C, M	+5	3-State	Bussed	18	262		
Am91L14C	1024 x 4	300	C, M	+5	3-State	Bussed	18	262		
Am91L14E	1024 x 4	200	C	+5	3-State	Bussed	18	262		
Am9124B	1024 x 4	450	C, M	+5	3-State	Bussed	18	367	157	Δ
Am9124C	1024 x 4	300	C, M	+5	3-State	Bussed	18	367	157	Δ
Am9124E	1024 x 4	200	C	+5	3-State	Bussed	18	367	157	Δ
Am91L24B	1024 x 4	450	C, M	+5	3-State	Bussed	18	262	105	Δ
Am91L24C	1024 x 4	300	C, M	+5	3-State	Bussed	18	262	105	Δ
Am91L24E	1204 x 4	200	C	+5	3-State	Bussed	18	262	105	Δ
Am9130A	1024 x 4	500	C, M	+5	3-State	Bussed	22	578	84	
Am9130B	1024 x 4	400	C, M	+5	3-State	Bussed	22	578	84	
Am9130C	1024 x 4	300	C, M	+5	3-State	Bussed	22	578	84	
Am9130D	1024 x 4	250	C	+5	3-State	Bussed	22	578	84	
Am9130E	1024 x 4	200	C	+5	3-State	Bussed	22	578	84	
Am91L30A	1024 x 4	500	C, M	+5	3-State	Bussed	22	367	72	
Am91L30B	1024 x 4	400	C, M	+5	3-State	Bussed	22	367	72	
Am91L30C	1024 x 4	300	C, M	+5	3-State	Bussed	22	367	72	
Am91L30D	1024 x 4	250	C	+5	3-State	Bussed	22	367	72	
Am9131A	1024 x 4	500	C, M	+5	3-State	Bussed	22	578	84	
Am9131B	1024 x 4	400	C, M	+5	3-State	Bussed	22	578	84	
Am9131C	1024 x 4	300	C, M	+5	3-State	Bussed	22	578	84	
Am9131D	1024 x 4	250	C	+5	3-State	Bussed	22	578	84	
Am9131E	1024 x 4	200	C	+5	3-State	Bussed	22	578	84	
Am91L31A	1024 x 4	500	C, M	+5	3-State	Bussed	22	367	72	
Am91L31B	1024 x 4	400	C, M	+5	3-State	Bussed	22	367	72	
Am91L31C	1024 x 4	300	C, M	+5	3-State	Bussed	22	367	72	
Am91L31D	1024 x 4	250	C	+5	3-State	Bussed	22	367	72	
Am9140A	4096 x 1	500	C, M	+5	3-State	Separate	22	578	84	
Am9140B	4096 x 1	400	C, M	+5	3-State	Separate	22	578	84	
Am9140C	4096 x 1	300	C, M	+5	3-State	Separate	22	578	84	
Am9140D	4096 x 1	250	C	+5	3-State	Separate	22	578	84	
Am9140E	4096 x 1	200	C	+5	3-State	Separate	22	578	84	
Am91L40A	4096 x 1	500	C, M	+5	3-State	Separate	22	367	72	
Am91L40B	4096 x 1	400	C, M	+5	3-State	Separate	22	367	72	
Am91L40C	4096 x 1	300	C, M	+5	3-State	Separate	22	367	72	
Am91L40D	4096 x 1	250	C	+5	3-State	Separate	22	367	72	
Am9141A	4096 x 1	500	C, M	+5	3-State	Separate	22	578	84	
Am9141B	4096 x 1	400	C, M	+5	3-State	Separate	22	578	84	

MOS MEMORY SELECTION GUIDE

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltage	Outputs	Data I/O Configuration	Package Pins	Operating Power Max (mW)	Standby Power Max (mW)
Am9141C	4096 x 1	300	C, M	+5	3-State	Separate	22	578	84
Am9141D	4096 x 1	250	C	+5	3-State	Separate	22	578	84
Am9141E	4096 x 1	200	C	+5	3-State	Separate	22	578	84
Am91L41A	4096 x 1	500	C, M	+5	3-State	Separate	22	367	72
Am91L41B	4096 x 1	400	C, M	+5	3-State	Separate	22	367	72
Am91L41C	4096 x 1	300	C, M	+5	3-State	Separate	22	367	72
Am91L41D	4096 x 1	250	C	+5	3-State	Separate	22	367	72
Am9044B	4096 x 1	450	C, M	+5	3-State	Separate	18	385	
Am9044C	4096 x 1	300	C, M	+5	3-State	Separate	18	385	
Am9044D	4096 x 1	250	C, M	+5	3-State	Separate	18	385	
Am9044E	4096 x 1	200	C	+5	3-State	Separate	18	385	
Am9244B	4096 x 1	450	C, M	+5	3-State	Separate	18	385	165 Δ
Am9244C	4096 x 1	300	C, M	+5	3-State	Separate	18	385	165 Δ
Am9244D	4096 x 1	250	C, M	+5	3-State	Separate	18	385	165 Δ
Am9244E	4096 x 1	200	C	+5	3-State	Separate	18	385	165 Δ
Am90L44B	4096 x 1	450	C, M	+5	3-State	Separate	18	275	
Am90L44C	4096 x 1	300	C, M	+5	3-State	Separate	18	275	
Am90L44D	4096 x 1	250	C	+5	3-State	Separate	18	275	
Am92L44B	4096 x 1	450	C, M	+5	3-State	Separate	18	275	110 Δ
Am92L44C	4096 x 1	300	C, M	+5	3-State	Separate	18	275	110 Δ
Am92L44D	4096 x 1	250	C	+5	3-State	Separate	18	275	110 Δ
Am9147-70	4096 x 1	70	C, M	+5	3-State	Separate	18	990	165 Δ
Am9147-55	4096 x 1	55	C	+5	3-State	Separate	18	990	165 Δ

ΔAutomatic power down with chip select.

DYNAMIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltages	Operating Power (mW)	Outputs	Data I/O Configuration	Package Pins	Refresh Time (ns)	Standby Power-Max. (mW)
Am9050C	4096 x 1	300	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9050D	4096 x 1	250	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9050E	4096 x 1	200	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9060C	4096 x 1	300	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9060D	4096 x 1	250	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9060E	4096 x 1	200	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am90L50C	4096 x 1	300	C	−5, +12	396	Open Drain	Bussed	18	2.0	3.0
Am90L50D	4096 x 1	250	C	−5, +12	396	Open Drain	Bussed	18	2.0	3.0
Am90L50E	4096 x 1	200	C	−5, +12	396	Open Drain	Bussed	18	2.0	3.0
Am90L60C	4096 x 1	300	C	±5, +12	396	3-State	Separate	22	2.0	3.0
Am90L60D	4096 x 1	250	C	±5, +12	396	3-State	Separate	22	2.0	3.0
Am90L60E	4096 x 1	200	C	±5, +12	396	3-State	Separate	22	2.0	3.0
Am9016C	16384 x 1	300	C	±5, +12	480	3-State	Separate	16	2.0	20.0
Am9016D	16384 x 1	250	C	±5, +12	480	3-State	Separate	16	2.0	20.0
Am9016E	16384 x 1	200	C	±5, +12	480	3-State	Separate	16	2.0	20.0
Am9016F	16384 x 1	150	C	±5, +12	480	3-State	Separate	16	2.0	20.0

READ-ONLY MEMORIES

Part Number	Organization	Access Time (ns)	Temp. Range	Supply Voltages	Operating Power – Max. (mW)	Outputs
C8316A	2048 x 8	850	C	+5	514	3-State
C8316E	2048 x 8	450	C	+5	499	3-State
Am9208B	1024 x 8	400	C, M	+5, +12	620	3-State
Am9208C	1024 x 8	300	C, M	+5, +12	620	3-State
Am9208D	1024 x 8	250	C	+5, +12	700	3-State
Am9214	512 x 8	500	C, M	+5	263	3-State
Am9216B	2048 x 8	400	C, M	+5, +12	660	3-State
Am9216C	2048 x 8	300	C	+5, +12	700	3-State
Am9217A	2048 x 8	550	C, M	+5	367	3-State
Am9217B	2048 x 8	450	C, M	+5	367	3-State
Am9218B	2048 x 8	450	C, M	+5	367	3-State
Am9218C	2048 x 8	350	C	+5	367	3-State
Am9232	4096 x 8	350	C, M	+5	500	3-State

MOS MEMORY SELECTION GUIDE

ERASABLE PROGRAMMABLE READ-ONLY MEMORY

Part Number	Organization	Access Time (nsec)	Temp. Range	Supply Voltages	Operating Power – Max. (mW)	Outputs
Am1702A	256 x 8	1000	C, E	−9V, +5V	676	3-State
Am1702A-1	256 x 8	550	C, E	−9V, +5V	676	3-State
Am1702A-2	256 x 8	650	C, E	−9V, +5V	676	3-State
Am1702AL	256 x 8	1000	C, E	−9V, +5V	–	3-State
Am1702AL-1	256 x 8	550	C, E	−9V, +5V	–	3-State
Am1702AL-2	256 x 8	650	C, E	−9V, +5V	–	3-State
Am2708	1024 x 8	450	C, M	+5V, +12V, −5V	800	3-State
**Am2716	2048 x 8	450	C	+5V	–	3-State
****Am2732	4192 x 8	450	C	+5V	–	3-State

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Am9016

16,384 x 1 Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 16k x 1 organization
- Direct replacement for MK4116
- Low maximum power dissipation — 462mW active, 20mW standby
- High speed operation — 150ns access, 320ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

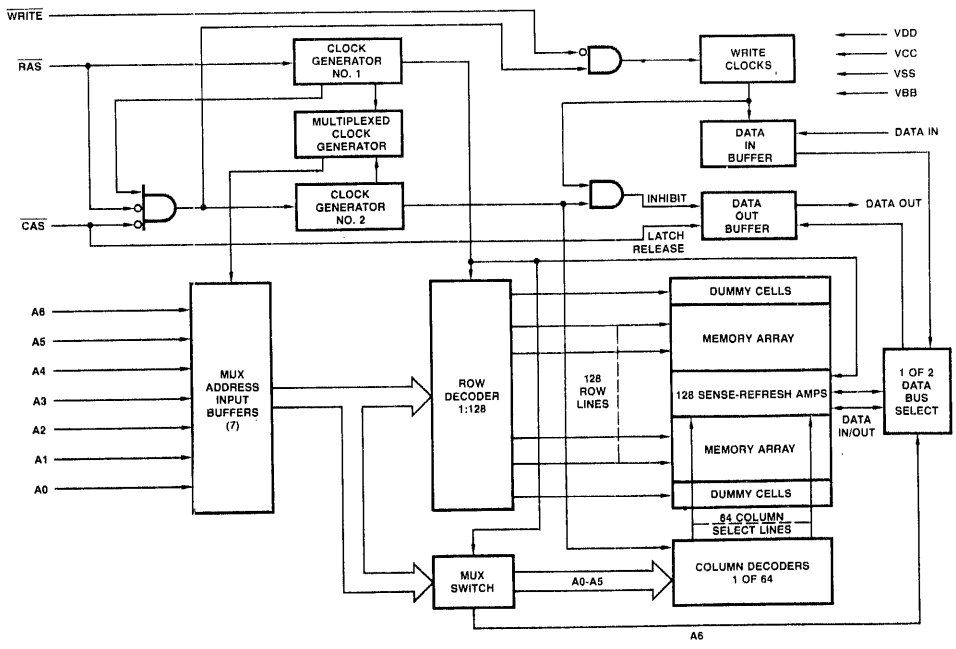
GENERAL DESCRIPTION

The Am9016 is a high speed, 16k-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share 7 input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance, and power dissipation.

The three-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

BLOCK DIAGRAM



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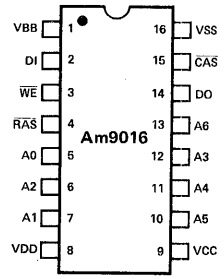
ORDERING INFORMATION

Ambient Temperature	Package Type	Access Time			
		300ns	250ns	200ns	150ns
0°C ≤ T_A ≤ +70°C	Hermetic DIP	AM9016CDC	AM9016DDC	AM9016EDC	AM9016FDC
	Molded DIP	AM9016CPC	AM9016DPC	AM9016EPC	AM9016FPC

CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

A0 – A6	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
RAS	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (–5V)
WE	WRITE ENABLE

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MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	–65°C to +150°C
Ambient Temperature Under Bias	0°C to +70°C
Voltage on Any Pin Relative to VBB	–0.5V to +20V
VDD and VCC Supply Voltages with Respect to VSS	–1.0V to +15.0V
VBB – VSS (VDD – VSS > 0V)	0V
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulation of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VSS	VBB
0°C ≤ T_A ≤ +70°C	+12V ±10%	+5V ±10%	0	–5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

Parameters	Description		Test Conditions	Am9016X Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage		IOH = –5.0mA	2.4		VCC	Volts
VOL	Output LOW Voltage		IOL = 4.2mA	VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In			2.4		7.0	Volts
VIHC	Input HIGH Voltage for CAS, RAS, WE			2.7		7.0	Volts
VIL	Input LOW Voltage			–1.0		0.80	Volts
IIX	Input Load Current		VSS ≤ VI ≤ 7V	–10		10	µA
IOZ	Output Leakage Current		VSS ≤ VO ≤ VCC, Output OFF	–10		10	µA
ICC	VCC Supply Current		Output OFF (Note 4)	–10		10	µA
IBB	VBB Supply Current, Average		Standby, RAS ≥ VIHC			100	µA
			Operating, Minimum Cycle Time			200	
IDD	VDD Supply Current, Average	Operating IDD1	RAS Cycling, CAS Cycling, Minimum Cycle Times			35	mA
		Page Mode IDD4	RAS ≤ VIL, CAS Cycling, Minimum Cycle Times			27	
		RAS Only Refresh IDD3	RAS Cycling, CAS ≥ VIHC, Minimum Cycle Times			27	
		Standby IDD2	RAS ≥ VIHC			1.5	
CI	Input Capacitance	RAS, CAS, WE	Inputs at 0V, f = 1MHz, Nominal Supply Voltages			10	pF
		Address, Data In				5.0	
CO	Output Capacitance		Output OFF			7.0	

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SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

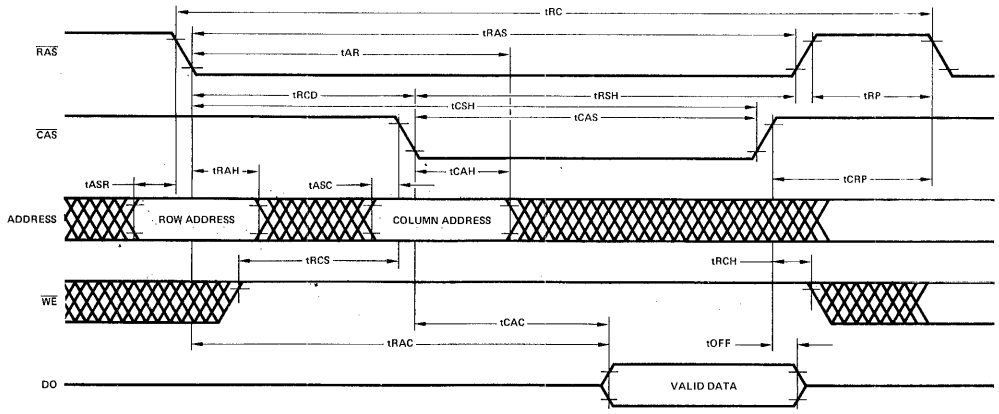
Parameters	Description	Am9016C		Am9016D		Am9016E		Am9016F		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tAR	$\overline{RAS}$ LOW to Column Address Hold Time	200		160		120		95		ns
tASC	Column Address Set-up Time	−10		−10		−10		−10		ns
tASR	Row Address Set-up Time	0		0		0		0		ns
tCAC	Access Time from $\overline{CAS}$ (Note 6)		185		165		135		100	ns
tCAH	$\overline{CAS}$ LOW to Column Address Hold Time	85		75		55		45		ns
tCAS	$\overline{CAS}$ Pulse Width	185	10,000	165	10,000	135	10,000	100	10,000	ns
tCP	Page Mode $\overline{CAS}$ Precharge Time	100		100		80		60		ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		−20		ns
tCSH	$\overline{CAS}$ Hold Time	300		250		200		150		ns
tCWD	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	145		125		95		70		ns
tCWL	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time	100		85		70		50		ns
tDH	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7)	85		75		55		45		ns
tDHR	$\overline{RAS}$ LOW to Data In Valid Hold Time	200		160		120		95		ns
tDS	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7)	0		0		0		0		ns
tOFF	$\overline{CAS}$ HIGH to Output OFF Delay	0	60	0	60	0	50	0	40	ns
tPC	Page Mode Cycle Time	295		275		225		170		ns
tRAC	Access Time from $\overline{RAS}$ (Note 6)		300		250		200		150	ns
tRAH	$\overline{RAS}$ LOW to Row Address Hold Time	45		35		25		20		ns
tRAS	$\overline{RAS}$ Pulse Width	300	10,000	250	10,000	200	10,000	150	10,000	ns
tRC	Random Read or Write Cycle Time	460		410		375		320		ns
tRCD	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6)	35	115	35	85	25	65	20	50	ns
tRCH	Read Hold Time	0		0		0		0		ns
tRCS	Read Set-up Time	0		0		0		0		ns
tREF	Refresh Interval		2		2		2		2	ms
tRMW	Read Modify Write Cycle Time	600		500		405		320		ns
tRP	RAS Precharge Time	150		150		120		100		ns
tRSH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay	185		165		135		100		ns
tRWC	Read/Write Cycle Time	525		425		375		320		ns
tRWD	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)	260		210		160		120		ns
tRWL	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time	100		85		70		50		ns
tT	Transition Time	3	50	3	50	3	50	3	35	ns
tWCH	Write Hold Time	85		75		55		45		ns
tWCR	$\overline{RAS}$ LOW to Write Hold Time	200		160		120		95		ns
tWCS	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9)	−20		−20		−20		−20		ns
tWP	Write Pulse Width	85		75		55		45		ns

NOTES

1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input set-up and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

SWITCHING WAVEFORMS

READ CYCLE



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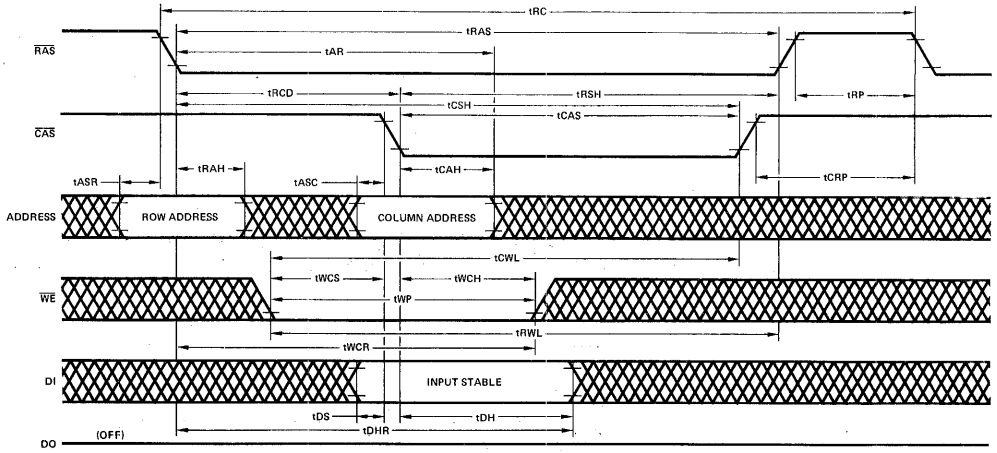
WRITE CYCLE (EARLY WRITE)



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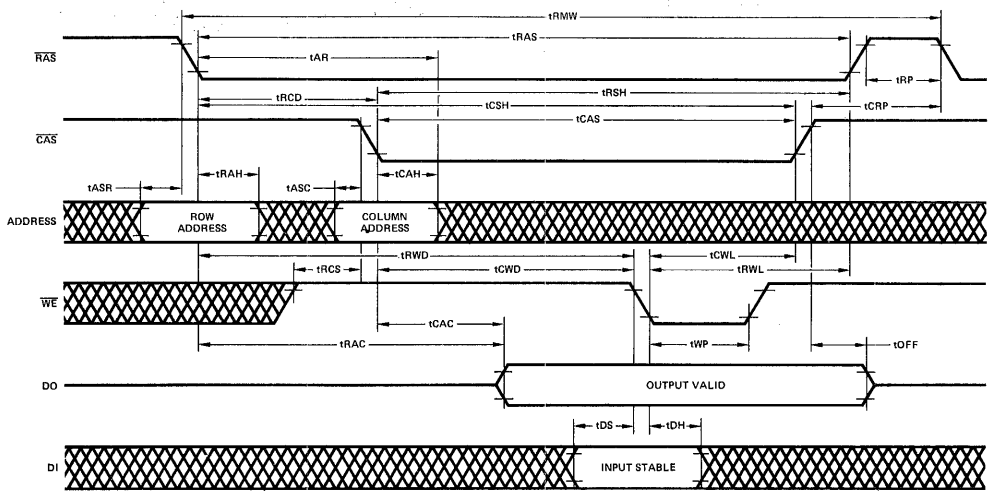
READ-WRITE/READ-MODIFY-WRITE CYCLE



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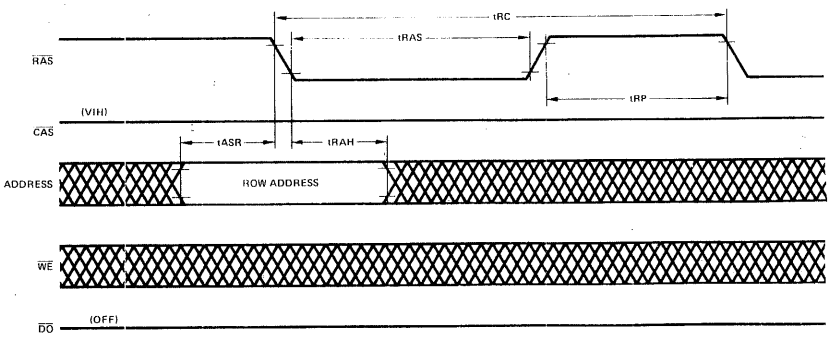
SWITCHING WAVEFORMS (Cont.)

$\overline{RAS}$ ONLY REFRESH CYCLE



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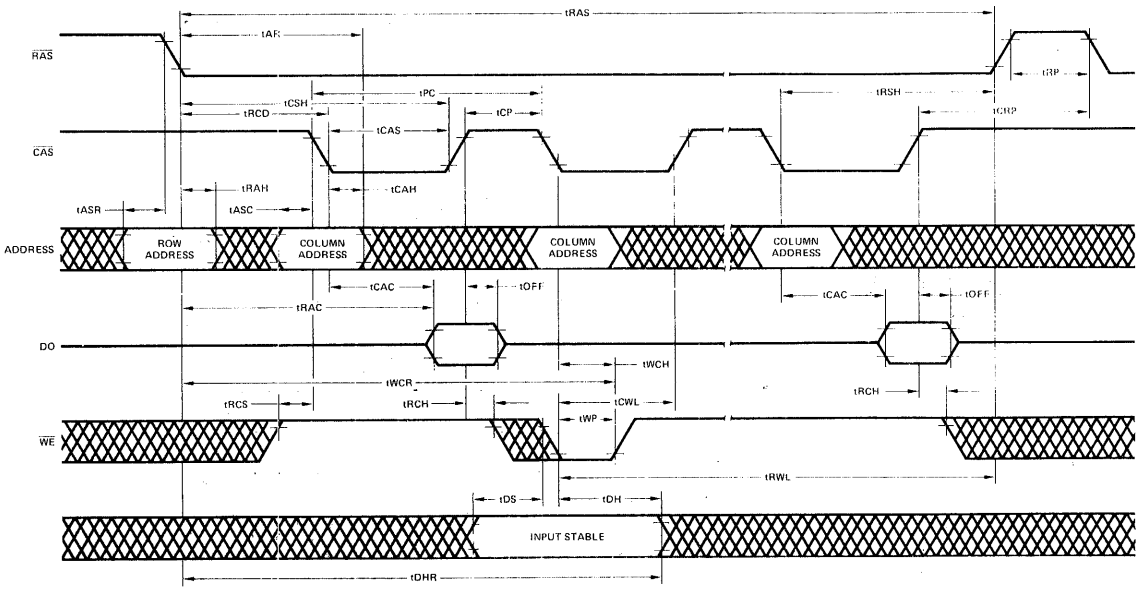
PAGE MODE CYCLE



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APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

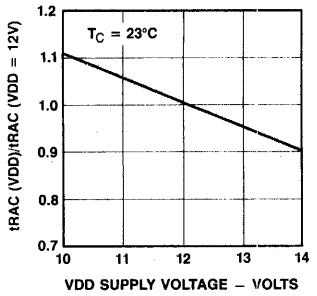
POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

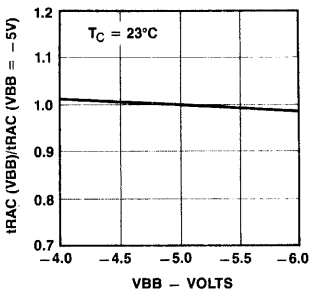
At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

TYPICAL CHARACTERISTICS

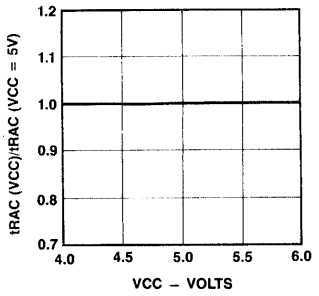
Typical Access Time (Normalized) tRAC Versus VDD



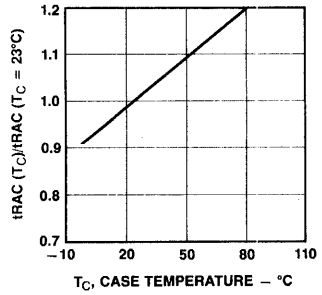
Typical Access Time (Normalized) tRAC Versus VBB



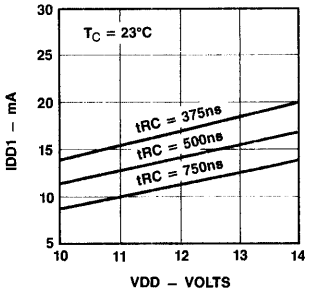
Typical Access Time (Normalized) tRAC Versus VCC



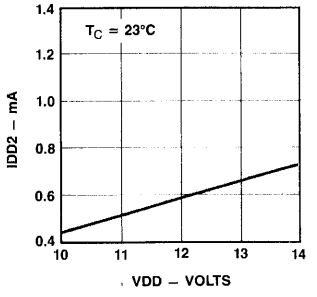
Typical Access Time (Normalized) tRAC Versus Case Temperature



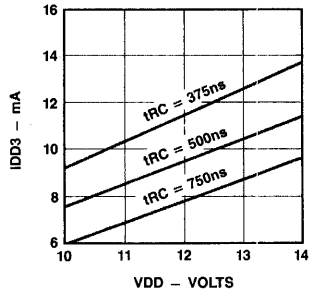
Typical Operating Current IDD1 Versus VDD



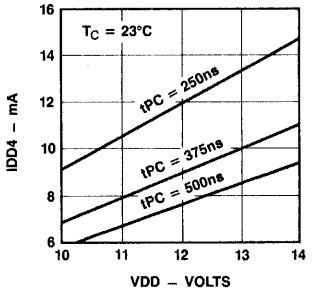
Typical Standby Current IDD2 Versus VDD



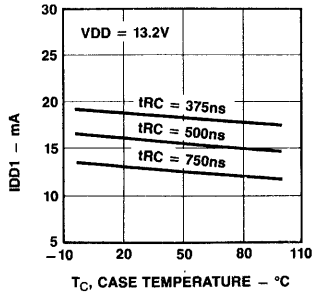
Typical Refresh Current IDD3 Versus VDD



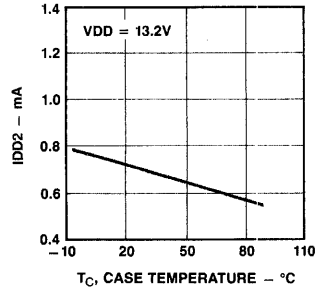
Typical Page Mode Current IDD4 Versus VDD



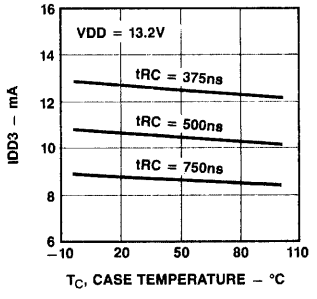
Typical Operating Current IDD1 Versus Case Temperature



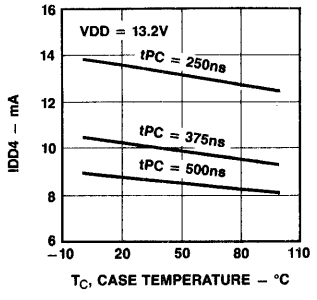
Typical Standby Current IDD2 Versus Case Temperature



Typical Refresh Current IDD3 Versus Case Temperature



Typical Page Mode Current IDD4 Versus Case Temperature



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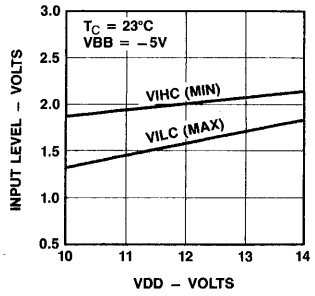
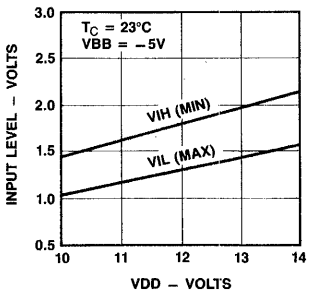
TYPICAL CHARACTERISTICS (Cont.)

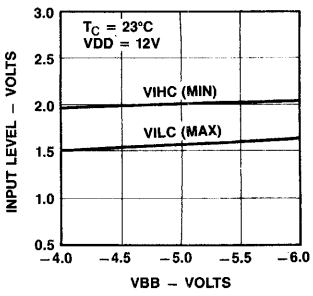
Input Voltage Levels Versus VDD



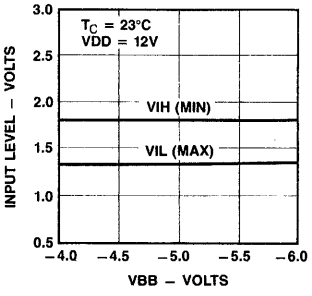
Input Voltage Levels Versus VDD



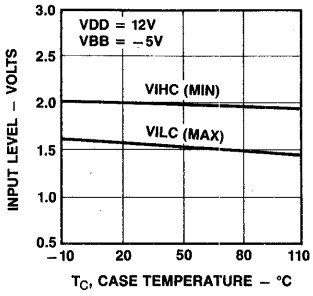
Input Voltage Levels Versus VBB



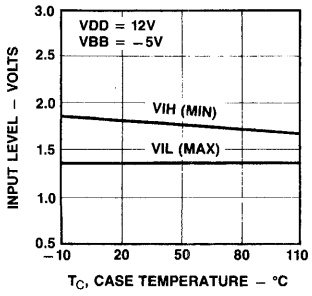
Input Voltages Levels Versus VBB



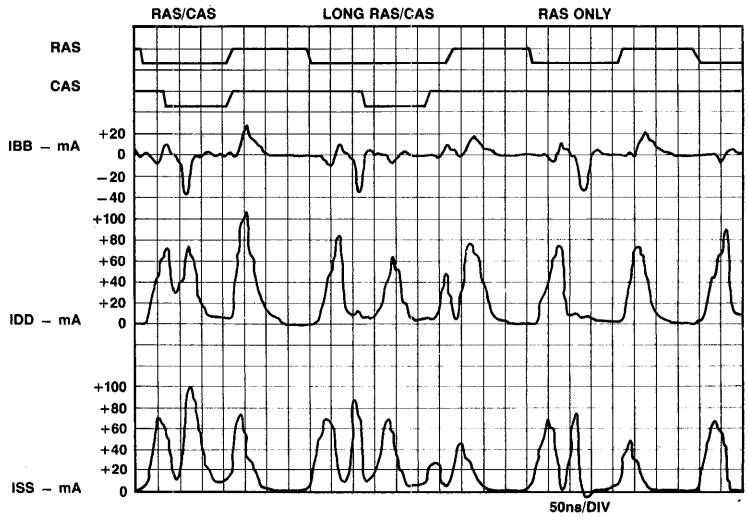
Input Voltage Levels Versus Case Temperature



Input Voltage Levels Versus Case Temperature



TYPICAL CURRENT WAVEFORMS



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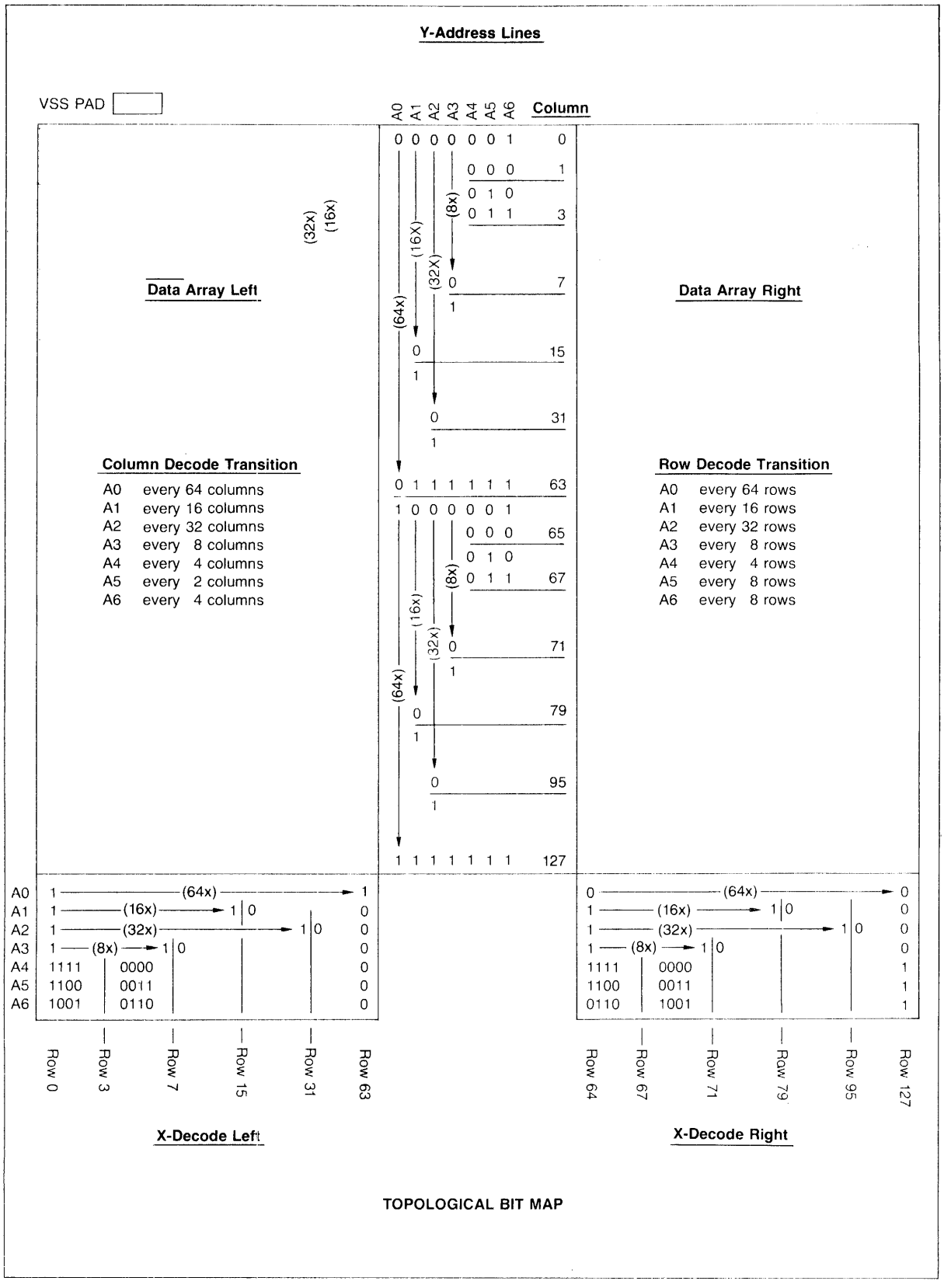
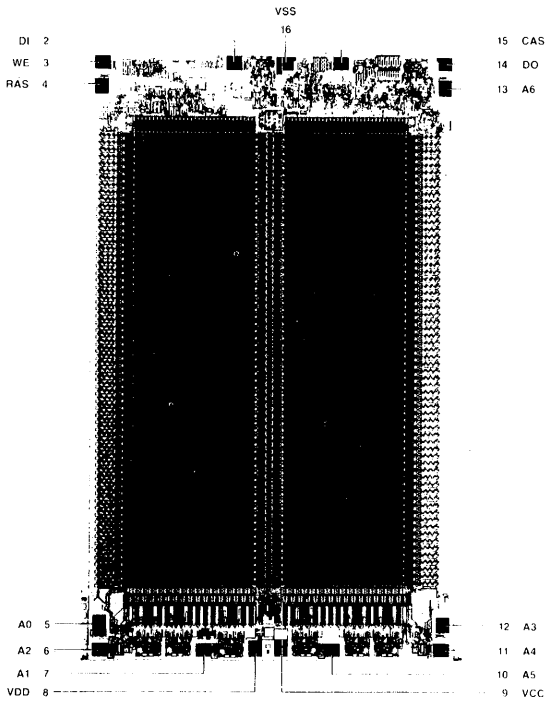

Y-Address Lines
VSS PAD
A0 A1 A2 A3 A4 A5 A6 Column
Data Array Left
Data Array Right
Column Decode Transition
A0 every 64 columns
A1 every 16 columns
A2 every 32 columns
A3 every 8 columns
A4 every 4 columns
A5 every 2 columns
A6 every 4 columns
Row Decode Transition
A0 every 64 rows
A1 every 16 rows
A2 every 32 rows
A3 every 8 rows
A4 every 4 rows
A5 every 8 rows
A6 every 8 rows
(64x)
(32x)
(16x)
(8x)
Row 0
Row 3
Row 7
Row 15
Row 31
Row 63
Row 64
Row 67
Row 71
Row 79
Row 95
Row 127
X-Decode Left
X-Decode Right
TOPOLOGICAL BIT MAP

Metallization and Pad Layout



DIE SIZE 0.106" X 0.205"

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Am9044 • Am9244

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  Am9044/Am9244 385mW (70mA)
  Am90L44/Am92L44 275mW (50mA)
- **LOW STANDBY POWER (MAX)**
  Am92L44 110mW (20mA)
- Access times down to 200ns (max)
- Military temperature range available to 250ns (max)
- Am9044 is a direct plug-in replacement for 4044
- Am9244 pin and function compatible with Am9044 and 4044 plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive – 4.0mA sink current @ 0.4V
- TTL identical interface logic levels
- 100% MIL-STD-883 reliability assurance testing

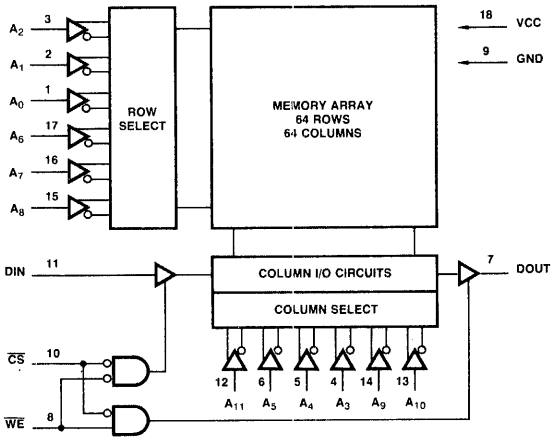
GENERAL DESCRIPTION

The Am9044 and Am9244 are high performance, static, N-Channel, read/write, random access memories organized as 4096 x 1. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of about 30%. The Am9044 and Am9244 are the same except that the Am9244 offers an automatic $\overline{CS}$ power down feature.

The Am9244 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9244 power decreases from 385mW to 165mW in the standby mode, and the Am92L44 from 275mW to 110mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9044.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9244 and Am9044 provide increased short circuit current for improved compacitive drive.

BLOCK DIAGRAM



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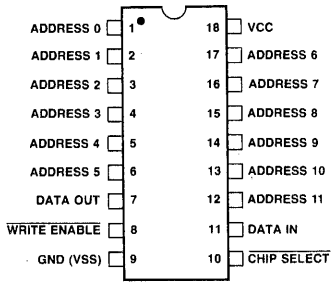
CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

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ORDERING INFORMATION

Ambient Temperature	Package Type	ICC Current Level	Access Times							
			Am9044				Am9244			
			450ns	300ns	250ns	200ns	450ns	300ns	250ns	200ns
0°C ≤ T_A ≤ +70°C	Plastic	70mA	AM9044BPC	AM9044CPC	AM9044DPC	AM9044EPC	AM9244BPC	AM9244CPC	AM9244DPC	AM9244EPC
		50mA	AM90L44BPC	AM90L44CPC	AM90L44DPC		AM92L44BPC	AM92L44CPC	AM92L44DPC	
	Hermetic	70mA	AM9044BDC	AM9044CDC	AM9044DDC	AM9044EDC	AM9244BDC	AM9244CDC	AM9244DDC	AM9244EDC
		50mA	AM90L44BDC	AM90L44CDC	AM90L44DDC		AM92L44BDC	AM92L44CDC	AM92L44DDC	
−55°C ≤ T_A ≤ +125°C	Hermetic	90mA	AM9044BDM	AM9044CDM	AM9044DDM		AM9244BDM	AM9244CDM	AM9244DDM	
		60mA	AM90L44BDM	AM90L44CDM			AM92L44BDM	AM92L44CDM		

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC	Part Number	Ambient Temperature	VSS	VCC
Am9044DC/PC Am90L44DC/PC Am9244DC/PC Am92L44DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ±10%	Am9044DM Am90L44DM Am9244DM Am92L44DM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions			Am9244XX Am92L44XX Min.	Typ.	Max.	Am9044XX Am90L44XX Min.	Typ.	Max.	Units
IOH	Output High Current	VOH = 2.4V	VCC = 4.5V	70°C	−1.0			−1.0			mA
		VOH = 2.4V	VCC = 4.5V	125°C	−.4			−.4			
IOL	Output Low Current	VOL = 0.4V	$T_A = +70°C$		4.0			4.0			mA
			$T_A = +125°C$		3.2			3.2			
VIH	Input High Voltage				2.0		VCC	2.0		VCC	Volts
VIL	Input Low Voltage				−0.5		0.8	−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC					10			10	µA
IOZ	Output Leakage Current	0.4V ≤ VO ≤ VCC Output Disabled	$T_A = +125°C$		−50		50	−50		50	µA
			$T_A = +70°C$		−10		10	−10		10	
CI	Input Capacitance (Note 1)	Test Frequency = 1.0MHz $T_A = 25°C$, All pins at 0V				3.0	5.0		3.0	5.0	pF
CI/O	I/O Capacitance (Note 1)					5.0	6.0		5.0	6.0	

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am92L44 Typ.	Am92L44 Max.	Am9244 Typ.	Am9244 Max.	Am90L44 Typ.	Am90L44 Max.	Am9044 Typ.	Am9044 Max.	Units
ICC	VCC Operating Supply Current	Max. VCC $\overline{CS} \leq$ VIL for Am9244/92L44	$T_A = 0°C$		50		70		50		70	mA
			$T_A = -55°C$		60		80		60		80	
IPD	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC} ($\overline{CS} \geq V_{IH}$)	$T_A = 0°C$		20		30		–		–	mA
			$T_A = -55°C$		22		33		–		–	

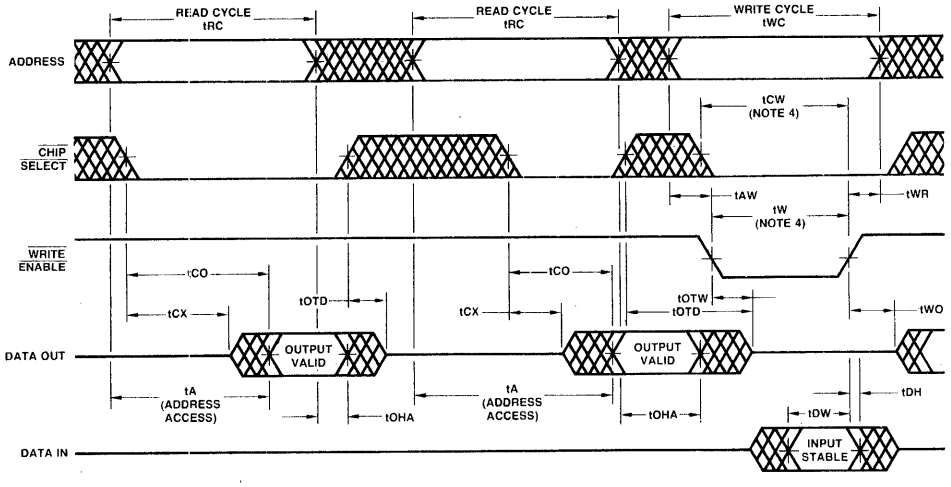
Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9244 than for the Am9044. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.

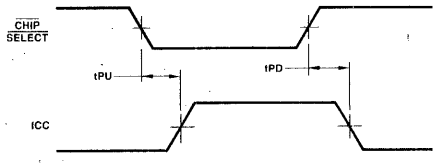
SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am9044B Am9244B Min.	Am9044B Am9244B Max.	Am9044C Am9244C Min.	Am9044C Am9244C Max.	Am9044D Am9244D Min.	Am9044D Am9244D Max.	Am9044E Am9244E Min.	Am9044E Am9244E Max.	Units
Read Cycle											
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		250		200		ns
tA	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		250		200	ns
tCO	Chip Select Low to Data Out Valid (Note 5)	Am9044		100		100		70		70	ns
		Am9244		450		300		250		200	ns
tCX	Chip Select Low to Data Out On		20		20		20		20		ns
tOTD	Chip Select High to Data Out Off			100		80		60		60	ns
tOHA	Address Unknown to Data Out Unknown Time		20		20		20		20		ns
Write Cycle											
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		250		200		ns
tW	Write Enable Low to Write Enable High Time (Note 4)	Am9044	200		150		100		100		ns
		Am9244	250		200		150		150		ns
tWR	Write Enable High to Address Do Not Care Time		0		0		0		0		ns
tOTW	Write Enable Low to Data Out Off Delay			100		80		60		60	ns
tDW	Data In Valid to Write Enable High Time		200		150		100		100		ns
tDH	Write Enable Low to Data In Do Not Care Time		0		0		0		0		ns
tAW	Address Valid to Write Enable Low Time		0		0		0		0		ns
tPD	Chip Select High to Power Low Delay (Am9244 only)			200		150		100		100	ns
tPU	Chip Select Low to Power High Delay (Am9244 only)		0		0		0		0		ns
tCW	Chip Select Low to Write Enable High Time (Note 4)	Am9044	200		150		100		100		ns
		Am9244	250		200		150		150		ns
tWO	Write Enable High To Output Turn On			100		100		70		70	ns

SWITCHING WAVEFORMS



POWER DOWN WAVEFORM (Am9244 ONLY)



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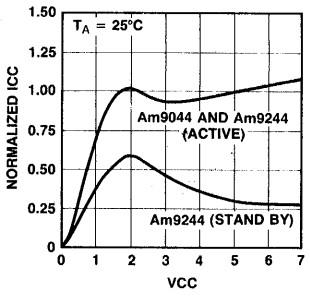
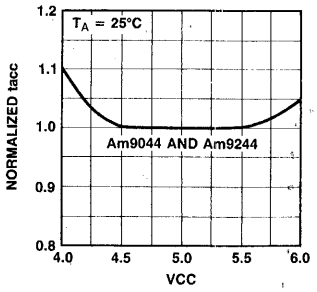
TYPICAL CHARACTERISTICS

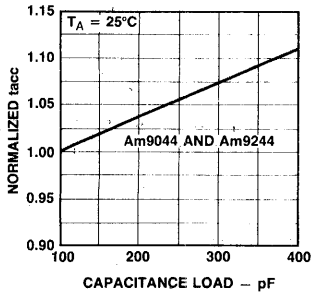
Typical ICC Versus VCC Characteristics



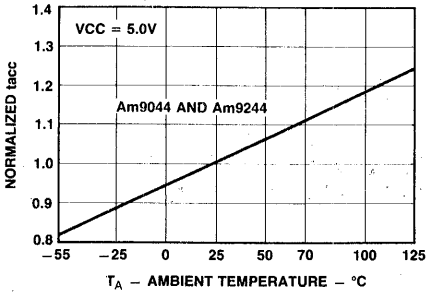
Typical tacc Versus VCC Characteristics



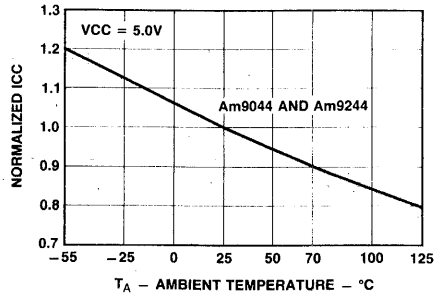
Typical C Load Versus Normalized tacc Characteristics



Normalized tacc Versus Ambient Temperature



Normalized ICC Versus Ambient Temperature



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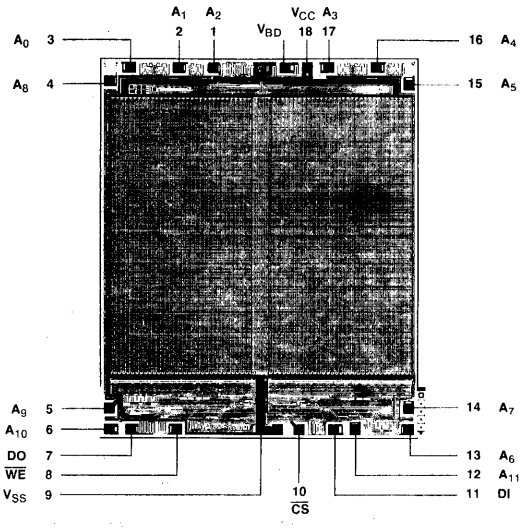
BIT MAP



Address Designators	
External	Internal
A0	A2
A1	A1
A2	A0
A3	A8
A4	A9
A5	A10
A6	A3
A7	A4
A8	A5
A9	A7
A10	A6
A11	A11

Figure 1. Bit Mapping Information.

Am9114

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- Access times down to 200ns (max)
- Military temperature range available to 300ns (max)
- Direct plug-in replacement for 2114
- Low operating power (max)
  Am9114 525mW (100mA I_{CC})
  Am91L14 368mW (70mA I_{CC})
- Identical access and cycle time
- Full 400mV worst-case noise immunity
- TTL identical input/output levels
- Pin compatible with industry standard 4K bipolar PROMs
- Single +5V power supply
- High density 18 pin package
- High output drive
  3.2mA sink current @ 0.4V
  1.0mA source current @ 2.4V
- 100% MIL-STD-883 reliability assurance testing

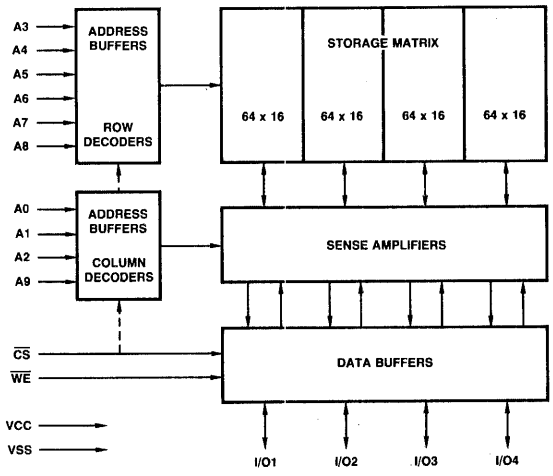
GENERAL DESCRIPTION

The Am9114 is a 4096-bit high performance, static, N-channel, read/write, random access memory organized 1024 words by 4 bits. Operation is from a single +5V power supply, and all interface levels are identical to standard TTL specifications.

Common data input/output pins are provided. Readout is non-destructive and is the same polarity as data input. Chip Select ($\overline{CS}$) provides simplified selection of an individual package when the outputs are OR-tied. The output of 3.2mA provides increased short-circuit current for improved capacitive drive.

A low-power version, the Am91L14, reduces power consumption by 30%. Additional power savings are available from the pin compatible Am9124 which provides lower operating power plus automatic power-down on deselection.

BLOCK DIAGRAM



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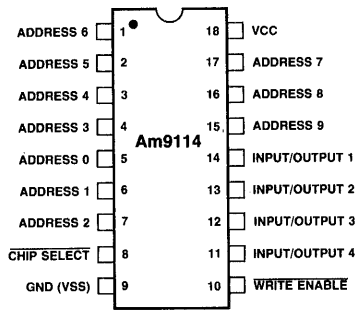
CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

MOS-261

ORDERING INFORMATION

Ambient Temperature	Package Type	Power Level	Access Times		
			450ns	300ns	200ns
0°C ≤ T_A ≤ 70°C	Molded	STD	Am9114BPC	Am9114CPC	Am9114EPC
		LOW	Am91L14BPC	Am91L14CPC	
	Hermetic	STD	Am9114BDC	Am9114CDC	Am9114EDC
		LOW	Am91L14BDC	Am91L14CDC	
−55°C ≤ T_A ≤ +125°C	Hermetic	STD	Am9114BDM	Am9114CDM	
		LOW	Am91L14BDM	Am91L14CDM	

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am9114DC/PC Am91L14DC/PC	0°C ≤ T_A ≤ +70°C	0V	+5.0V ±5%
Am9114DM Am91L14DM	−55°C ≤ T_A ≤ +125°C	0V	+5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range

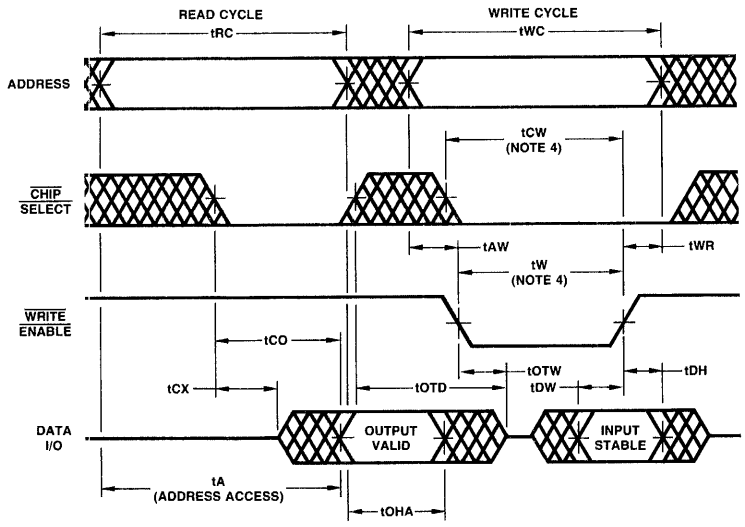
Parameter	Description	Test Conditions		Am9114 Min.	Am9114 Typ.	Am9114 Max.	Am91L14 Min.	Am91L14 Typ.	Am91L14 Max.	Units
V_{OH}	Output High Voltage	T_A = 70°C, I_{OH} = −1.0mA		2.4			2.4			Volts
		T_A = 125°C, I_{OH} = −1.0mA		2.2			2.2			
V_{OL}	Output Low Voltage	T_A = 125°C, I_{OL} = 2.4mA				0.4			0.4	Volts
		T_A = 70°C, I_{OL} = 3.2mA				0.4			0.4	
V_{IH}	Input High Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input Low Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{IX}	Input Load Current	V_{SS} ≤ V_I ≤ V_{CC}				10			10	μA
I_{OZ}	Output Leakage Current	V_{SS} ≤ V_O ≤ V_{CC} Output Disabled	T_A = 125°C	−50		50	−50		50	μA
			T_A = 70°C	−10		10	−10		10	
I_{OHS}	Output High Short Circuit Current	(Note 2)				75			75	mA
I_{CC}	V_{CC} Supply Current	MAX. V_{CC}	T_A = 25°C			95			65	mA
			T_A = 0°C			100			70	
			T_A = −55°C			110			80	
C_I	Input Capacitance (Note 1)	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V			3.0	5.0		3.0	5.0	pF
C_{IO}	I/O Capacitance (Note 1)				5.0	6.0		5.0	6.0	

Notes:
1. Typical values are for T_A = 25°C nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description	Am9114B Min.	Am9114B Max.	Am9114C Min.	Am9114C Max.	Am9114E Min.	Am9114E Max.	Units
Read Cycle								
t_{RC}	Address Valid to Address Do Not Care Time (Red Cycle Time)	450		300		200		ns
t_A	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		200	
t_{CO}	Chip Select Low to Data Out Valid (Note 5)		120		100		70	
t_{CX}	Chip Select Low to Data Out On	20		20		20		
t_{OTD}	Chip Select High to Data Out Off		100		80		60	
t_{OHA}	Address Unknown to Data Out Unknown Time	50		50		50		
Write Cycle								
t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		200		ns
t_W	Write Enable Low to Write Enable High Time (Note 4)	200		150		120		
t_{WR}	Write Enable High to Address Do Not Care Time	0		0		0		
t_{OTW}	Write Enable Low to Data Out Off Delay		100		80		60	
t_{DW}	Data In Valid to Write Enable High Time	200		150		120		
t_{DH}	Write Enable Low to Data In Do Not Care Time	0		0		0		
t_{AW}	Address Valid to Write Enable Low Time	0		0		0		
t_{CW}	Chip Select Low to Write Enable High Time (Note 4)	200		150		120		

SWITCHING WAVEFORMS



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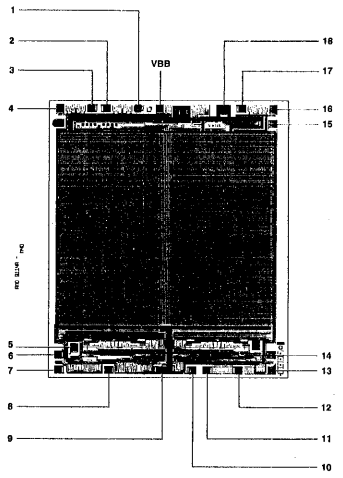
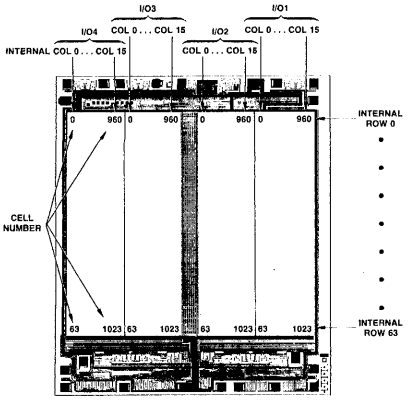
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.137" X 0.168"

BIT MAP

Address Designators	
External	Internal
A0	A9
A1	A8
A2	A7
A3	A0
A4	A1
A5	A2
A6	A3
A7	A4
A8	A5
A9	A6



Am9124

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

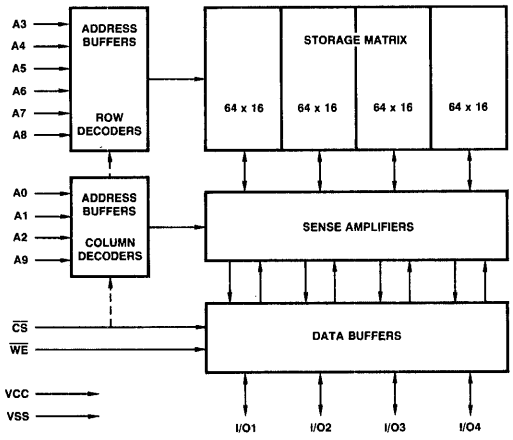
- Access times down to 200ns (max)
- Military temperature range available to 300ns (max)
- Pin and function compatible with Am9114 and Intel 2114, plus automatic power down
- Low operating power (max) –
  Am9124 315mW (60mA I_{CC})
  Am91L24 210mW (40mA I_{CC})
- Automatic standby power (max) –
  Am9124 105mW (20mA I_{CC})
  Am91L24 79mW (15mA I_{CC})
- Identical access and cycle time
- TTL identical input/output levels
- Full 400mV worst-case noise immunity
- Pin compatible with industry standard 4K bipolar PROMs
- Single +5V power supply
- High density 18 pin package
- High output drive –
  4.0mA sink current @ 0.4V
  1.0mA source current @ 2.4V
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am9124 is a 4096-bit, low-power, high performance, static, N-channel, read/write, random access memory organized 1024 words by 4 bits. Operation is from a single +5V power supply, and all interface levels are identical to standard TTL specifications. The device is pin and functional compatible with the Am9114 with the added benefits of 40% less operating power plus automatic Chip Select power-down that reduces power an additional 60%. The supply current advantage of the Am9124 vs. the 2114/ Am9114 are shown in Figure 1.

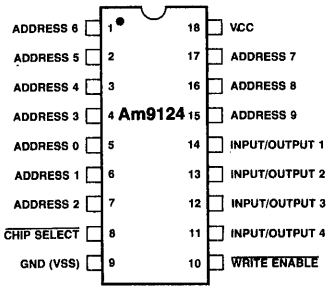
Common data input/output pins are provided. Readout is non-destructive and is the same polarity as data input. Chip Select ($\overline{CS}$) automatically controls power-down and provides simplified selection of an individual package when the outputs are OR-tied. The output of 4.0mA provides increased short-circuit current for improved capacitive drive.

BLOCK DIAGRAM



MOS-263

CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

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ORDERING INFORMATION

Ambient Temperature	Package Type	Power Level	Access Times: Am9124 450ns	Am9124 300ns	Am9124 200ns
0°C ≤ T_A ≤ 70°C	Molded	STD	Am9124BPC	Am9124CPC	Am9124EPC
		LOW	Am91L24BPC	Am91L24CPC	
	Hermetic	STD	Am9124BDC	Am9124CDC	Am9124EDC
		LOW	Am91L24BDC	Am91L24CDC	
−55°C ≤ T_A ≤ +125°C	Hermetic	STD	Am9124BDM	Am9124CDM	
		LOW	Am91L24BDM	Am91L24CDM	

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am9124DC/PC Am91L24DC/PC	0°C ≤ T_A ≤ +70°C	0V	+5.0V ±5%
Am9124DM Am91L24DM	−55°C ≤ T_A ≤ +125°C	0V	+5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am9124 Min.	Am9124 Typ.	Am9124 Max.	Am91L24 Min.	Am91L24 Typ.	Am91L24 Max.	Units
V_{OH}	Output High Voltage	T_A = 70°C, I_{OH} = −1.4mA		2.4			2.4			Volts
		T_A = 125°C, I_{OH} = −1.0mA		2.2			2.2			
V_{OL}	Output Low Voltage	T_A = 125°C, I_{OL} = 3.2mA				0.4			0.4	Volts
		T_A = 70°C, I_{OL} = 4.0mA				0.4			0.4	
V_{IH}	Input High Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input Low Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{IX}	Input Load Current	V_{SS} ≤ V_I ≤ V_{CC}				10			10	µA
I_{OZ}	Output Leakage Current	V_{SS} ≤ V_O ≤ V_{CC} Output Disabled	T_A = 125°C	−50		50	−50		50	µA
			T_A = 70°C	−10		10	−10		10	
I_{OHS}	Output High Short Circuit Current	(Note 2)	T_A = 0°C			95			95	mA
			T_A = −55°C			115			115	
I_{CC}	V_{CC} Operating Supply Current	MAX. V_{CC} ($\overline{CS}$ ≤ V_{IL})	T_A = 25°C			55			37	mA
			T_A = 0°C			60			40	
			T_A = −55°C			70			50	
I_{PD}	V_{CC} Power Down Supply Current	MAX. V_{CC} ($\overline{CS}$ ≤ V_{IH}) (Deselected)	T_A = 25°C			19			14	mA
			T_A = 0°C			20			15	
			T_A = −55°C			22			17	
C_I	Input Capacitance (Note 1)	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V			3.0	5.0		3.0	5.0	pF
C_{IO}	I/O Capacitance (Note 1)				5.0	6.0		5.0	6.0	

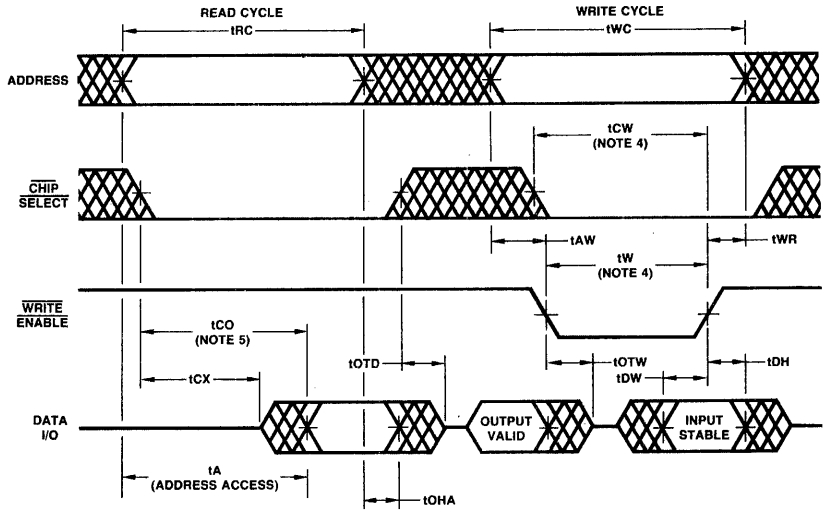
Notes:

1. Typical values are for T_A = 25°C nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9124 than for the Am9114/2114. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.

SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description	Am9124B Min.	Am9124B Max.	Am9124C Min.	Am9124C Max.	Am9124E Min.	Am9124E Max.	Units
Read Cycle								
t_{RC}	Address Valid to Address Do Not Care Time (Red Cycle Time)	450		300		200		ns
t_A	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		200	
t_{CO}	Chip Select Low to Data Out Valid (Note 5)		420		280		185	
t_{CX}	Chip Select Low to Data Out On	20		20		20		
t_{OTD}	Chip Select High to Data Out Off		100		80		60	
t_{OHA}	Address Unknown to Data Out Unknown Time	50		50		50		
Write Cycle								
t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		200		ns
t_W	Write Enable Low to Write Enable High Time (Note 4)	250		200		150		
t_{WR}	Write Enable High to Address Do Not Care Time	0		0		0		
t_{OTW}	Write Enable Low to Data Out Off Delay		100		80		60	
t_{DW}	Data In Valid to Write Enable High Time	200		150		120		
t_{DH}	Write Enable Low to Data In Do Not Care Time	0		0		0		
t_{AW}	Address Valid to Write Enable Low Time	0		0		0		
t_{PD}	Chip Select High to Power Low Delay		200		150		100	
t_{PU}	Chip Select Low to Power High Delay	0		0		0		
t_{CW}	Chip Select Low to Write Enable High Time (Note 4)	250		200		150		

SWITCHING WAVEFORMS



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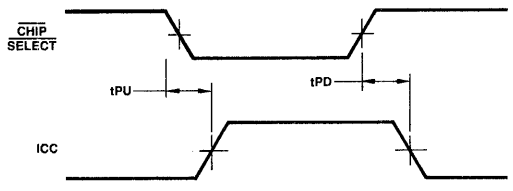
POWER DOWN WAVEFORM



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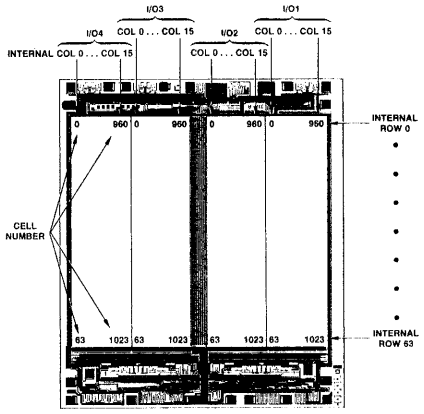
Configuration	Part Number	Average Worst Case Current (mA at 0°C) 100% Duty Cycle	50% Duty Cycle
2K x 8	Am2114 Am2114L	400 280	400 280
	Am9124 Am91L24	160 110	120 85
4K x 12	Am2114 Am2114L	1200 840	1200 840
	Am9124 Am92L24	360 255	300 217
8K x 16	Am2114 Am2114L	3200 2240	3200 2240
	Am9124 Am91L24	800 580	720 530

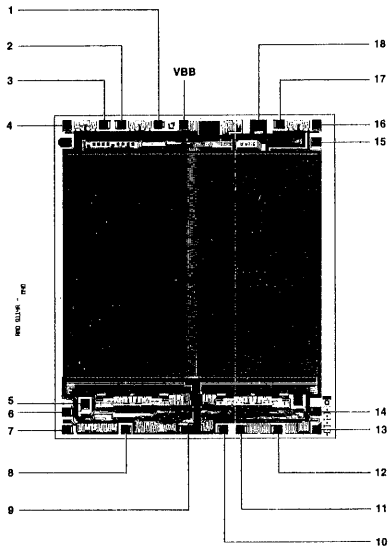
Figure 1. Supply Current Advantages of Am9124 vs. Am2114.

BIT MAP

Address Designators	
External	Internal
A0	A9
A1	A8
A2	A7
A3	A0
A4	A1
A5	A2
A6	A3
A7	A4
A8	A5
A9	A6



Metallization and Pad Layout



DIE SIZE 0.137" X 0.168"

6

Am9147

4096 x 1 Static R/W Random Access Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 55ns maximum
- 4k x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power-down when deselected
- Low power dissipation
  - Am9147: 000mW active, 000mW power down
  - Am91L47: 000mW active, 000mW power down
- Standard 18 pin, .300 inch dual in-line package
- High output drive – up to 00 standard TTL loads or 4 Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing

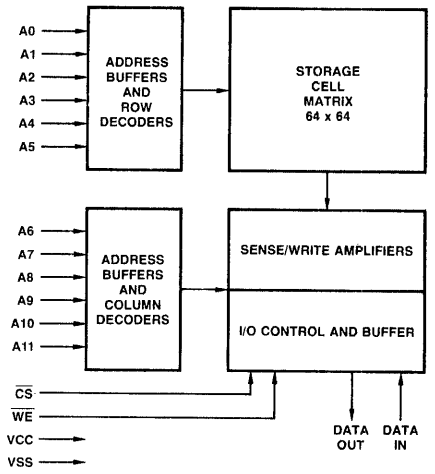
GENERAL DESCRIPTION

The Am9147 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by 1 bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to 4 standard Schottky TTL loads or up to 5 standard TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CS} \geq$ VIH), the Am9147 automatically enters a power-down mode which reduces power dissipation by more than 00%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



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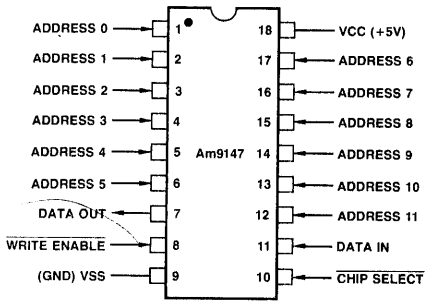
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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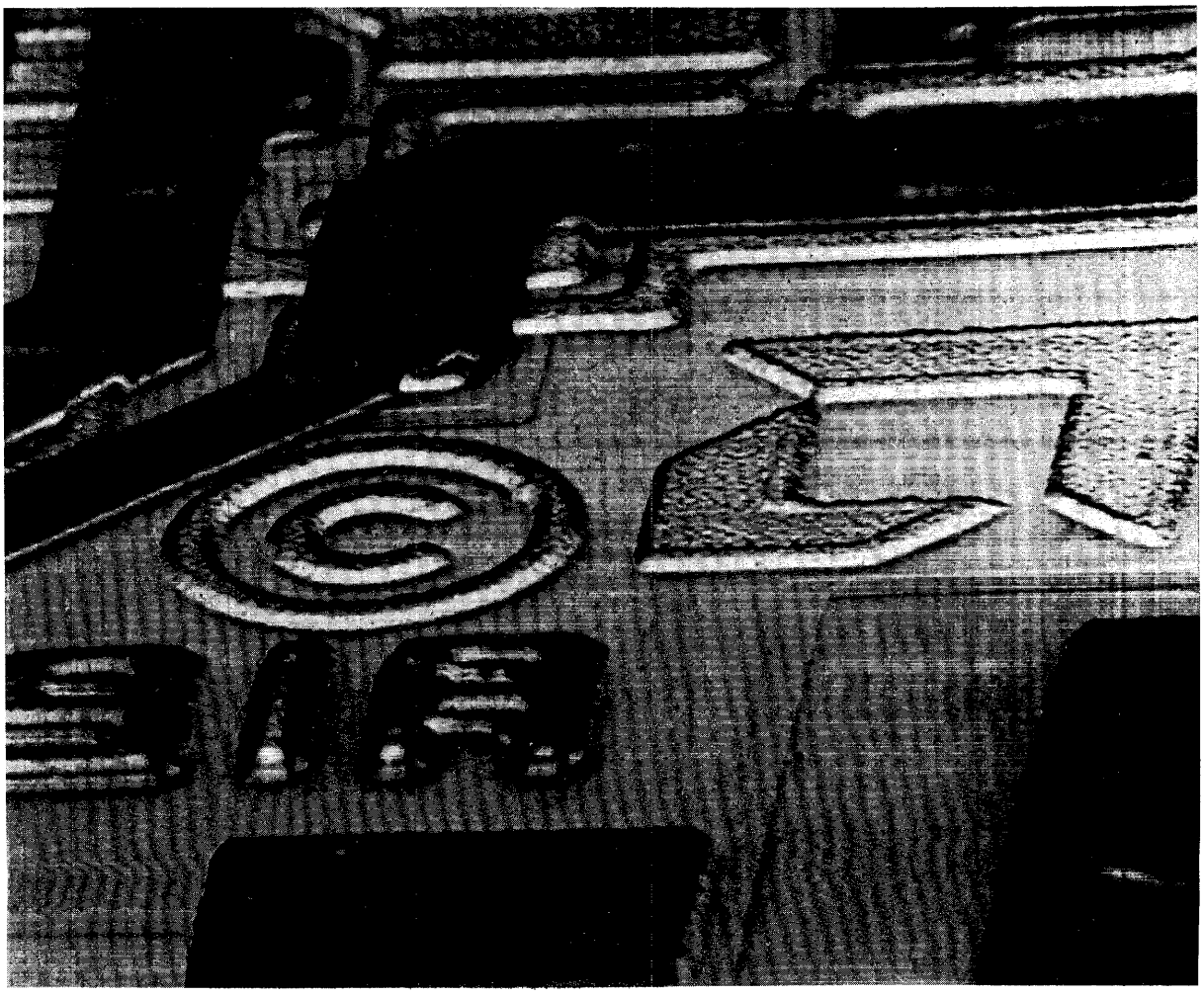
Advanced Micro Devices Commitment to Excellence

Product Assurance Programs for Military and Commercial Integrated Circuits



A

A COMMITMENT TO EXCELLENCE

Advanced Micro Devices was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence.

In product assurance procedures, Advanced Micro Devices is unique. Only Advanced Micro Devices processes all integrated circuits, commercial as well as military, to the demanding requirements of MIL-STD-883. The Rome Air Development Center (RADC), which is the Air Force's principal authority on component reliability, has issued MIL-HDBK-217B which indicates that parts processed to Military Standard 883, Level C (Advanced Micro Devices' standard processing) yield a product nearly ten times better in failure rates than the industry commercial average.

Our Sunnyvale facility has been certified by the Defense Electronics Supply Center (DESC) to produce parts to JAN Class B and C under Military Specification MIL-M-38510. The National Aeronautics and Space Administration (NASA) has certified this production line for the manufacture of Class A products for programs requiring the highest levels of reliability. Advanced Micro Devices is the only integrated circuit company formed within the last ten years to achieve such line certification.

This brochure outlines Advanced Micro Devices' standard programs for Class B, C and A devices for military and commercial operating range applications. These will cover the majority of system requirements today. Alternative screening flows for specific user needs can be performed on request. Check with your local sales office for further information.

ADVANCED MICRO DEVICES' STANDARD PRODUCTS ARE MANUFACTURED TO MIL-STD-883 REQUIREMENTS

Advanced Micro Devices' product assurance programs are based on two key documents.

MIL-M-38510 – General Specification for Microcircuits

MIL-STD-883 – Test Methods and Procedures for Microelectronics

The screening charts in this brochure show that every integrated circuit shipped by Advanced Micro Devices receives the critical screening procedures defined in MIL-STD-883, Method 5004 for Class C product. This includes molded plastic devices.

In addition, documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

Commercial and industrial users receive the quality and reliability benefits of this aerospace-type screening and documentation at no additional cost.

STANDARD PRODUCT TESTING CATEGORIES

Advanced Micro Devices offers integrated circuits to four standard testing categories.

1. Commercial operating range product (typically 0°C to 70°C)
2. Commercial product with 100% temperature testing
3. Military operating range product (typically −55°C to +125°C)
4. JAN qualified product

Categories 1, 2 and 3 are available on most Advanced Micro Devices circuits. Category 4 is offered on a more limited line. Check with your local sales office for details.

STANDARD PRODUCT ASSURANCE CATEGORIES

Devices produced to the above testing categories are available to the three standard classes of product assurance defined by MIL-STD-883. As a minimum, every device shipped by Advanced Micro Devices meets the screening requirements of Class C.

Class C – For commercial and ground-based military systems where replacement can be accomplished without difficulty.

According to MIL-HDBK-217B, this assures relative failure rates 9.4 times better than that of regular industry commercial product.

Class B – For flight applications and commercial systems where maintenance is difficult or expensive and where reliablity is vital.

Devices are upgraded from Class C to Class B by burn-in screening and additional testing.

According to MIL-HDBK-217B, Class B failure rate is improved 30 times over regular industry commercial product. Advanced Micro Devices Class B processing conforms to MIL-STD-883 requirements. MIL-HDBK-217B indicates that this may provide failure rates as much as two times better than some other manufacturers' "equivalent" or "pseudo" Class B programs.

Class S – For space applications where replacement is extremely difficult or impossible and reliability is imperative.

Class S screening includes x-ray and other special inspections tailored to the specific requirements of the user.

The 100% screening and quality conformance testing performed within these Advanced Micro Devices programs is shown in TABLES I, II and III. A full description of the process flow is provided in Product Assurance Document 15-010, available on request.

CLASS C SCREENING FLOW FOR COMMERCIAL SYSTEMS AND GROUND BASED MILITARY SYSTEMS

TABLE I
CLASS C
INTEGRATED CIRCUITS

Screening Procedure per MIL-STD-883 Method 5004, Class C		COMMERCIAL OPERATING RANGE		MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES		HERMETIC PACKAGE ONLY	
Screen	Test Method	C1 Commercial Product	C2 Commercial Product With 100% Temperature Testing	C3 Military Product	C4 Jan Qualified Product
VISUAL AND MECHANICAL					
Internal visual	2010, Condition B	100%	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%	100%
Constant acceleration	2001	100% (1)	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100% (1)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	–	–
Functional	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	–	–
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	(2)	–	–
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample	Sample
Sample Tests	Group B	–	–	–	Sample
	Group C	–	–	–	Sample
	Group D	–	–	–	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%	100%

TABLE II
GROUP A QUALITY CONFORMANCE LEVELS

Advanced Micro Devices employs the military-recommended LTPD sampling system to assure quality. MIL-STD-883, Method 5005, TABLE I, Group A, subgroups 1 through 9 as appropriate to the device family are performed on every lot. Quality levels defined for Class B product are applied by Advanced Micro Devices to both Class B and Class C orders.

	LTPD	INITIAL SAMPLE SIZE
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – LINEAR devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – LINEAR devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – LINEAR devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – DIGITAL devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperatures – DIGITAL devices	*	
Subgroup 11 – Switching tests at minimum rated operating temperatures – DIGITAL devices	*	

*These subgroups, where applicable, are usually performed during initial characterization only for all except JAN Qualified product.

CLASS B SCREENING FLOW
FOR HIGH RELIABILITY COMMERCIAL AND MILITARY SYSTEMS

TABLE III
CLASS B
INTEGRATED CIRCUITS
(Class C plus burn in screening and additional testing.)

Screening Procedure per MIL-STD-883 Method 5004, Class B		COMMERCIAL OPERATING RANGE		MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES		HERMETIC PACKAGE ONLY	
Screen	Test Method	B1 Commercial Product	B2 Commercial Product With 100% Temperature Testing	B3 Military Product	B4 Jan Qualified Product
VISUAL AND MECHANICAL					
Internal visual	2010, Condition B	100%	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%	100%
Constant acceleration	2001	100% (1)	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100% (1)	100%	100%
BURN IN					
Interim (pre burn in) electricals	Per applicable device specification	100%	100%	100%	100%
Burn in	1015, 160 hours at 125°C or equivalent.*	100%	100%	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	100%	100%
Functional	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	100%	100%
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	(2)	100%	100%
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample	Sample
Sample Tests	Group B	–	–	(4)	Sample
	Group C	–	–	(4)	Sample
	Group D	–	–	(4)	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%	100%

Notes: 1. Not applicable to molded packages.
2. All MOS RAMs and many other MOS devices receive a.c. testing and 100% d.c. screening at high temperature and power supply extremes as standard. Other products sampled at Group A (Table III).
3. Tested at high temperature, 100°C, only on commercial range product. Note that this is a full d.c. check of all parameters in addition to the simple "hot-rail" functional sequence performed on most other commercial programs.
4. Available to special order.
5. Without optical aid for commercial devices.

*Unless otherwise specified on the device data sheet.

CLASS S
FOR AEROSPACE SYSTEMS. (FORMERLY CLASS A)

Advanced Micro Devices offers a Class S program.

This program together with other high reliability screening options, such as SEM and x-ray, is described as Option A in Advanced Micro Devices' Extended Processing Options Document 00-003. Contact your local Advanced Micro Devices' sales office for more information.

A

STANDARD PRODUCT
SCREENING SUMMARY AND ORDERING INFORMATION

1. COMMERCIAL PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic and molded packages.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class C and Class B options.

Class C (Flow C1)

- Order standard AMD part number.
- Marked same as order number.

  Example: Am2901ADC

Class B (Flow B1)

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix B (or /883B for 1, 2 and 300 Series Linear devices).
- Marked same as order number.

  Example: Am2901ADC-B

2. COMMERCIAL PRODUCT WITH 100% TEMPERATURE TESTING

- Identical to standard commercial operating range product with the addition of 100% dc and functional testing at 100°C and power supply extremes.

Class C (Flow C2)

- Order standard AMD part number, add suffix T.
- Marked same as order number.

  Example: Am2901ADC-T

Class B (Flow B2)

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix TB.
- Marked same as order number.

  Example: Am2901ADC-TB

3. MILITARY PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic package only.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class B and Class C options.

Class C (Flow C3)

- Order standard AMD part number.
- Marked same as order number.

  Example: Am2901ADM

Class B (Flow B3)

- Burn in performed in AMD circuit condition.
- AC at 25°C, dc and functional testing at 25°C as well as temperature and power supply extremes performed on 100% of every lot.
- Quality conformance testing, Method 5005, Groups B, C and D available to special order.
- Order standard AMD part number, add suffix B.
- Marked same as order number.

  Example: Am2901ADM-B

4. JAN QUALIFIED PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested to JAN detail specification (slash sheet).
- Manufactured in Defense Logistics Agency certified facility.
- Quality conformance testing, Method 5005, Groups A, B, C and D performed as standard and must be completed prior to shipment.
- It is a product for which AMD has gained QPL listing.*

Class C (Flow C4)

- Order per military document.
- Marked per military document.

  Example: JM38510/44001CQB

Class B (Flow B4)

- Burn in performed in circuit condition approved for JAN devices.
- Order per military document.
- Marked per military document.

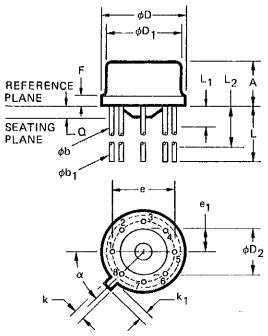
  Example: JM38510/44001BRC

*In certain cases where JAN Qualified product is specified but is not available, Advanced Micro Devices can provide devices to the electrical limits and burn-in criteria of the slash sheet. This class of product has been called JAN Equivalent and marked M38510/ by some manufacturers. This identification is no longer permitted by DESC. Check with your local sales office for availability of specific device types.

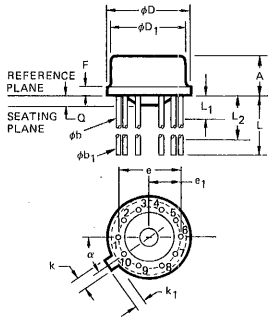
PACKAGE OUTLINES

METAL CAN PACKAGES

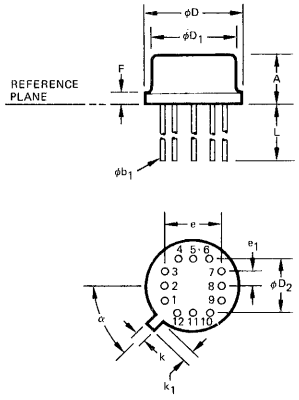
H-8-1



H-10-1



G-12-1



AMD Pkg.	H-8-1		H-10-1		G-12-1	
Common Name	TO-99 Metal Can		TO-100 Metal Can		TO-8 Metal Can	
38510 Appendix C	A-1		A-2		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.
A	.165	.185	.165	.185	.155	.180
e	.185	.215	.215	.245	.390	.410
e_1	.090	.110	.105	.125	.090	.110
F	.013	.033	.013	.033	.020	.030
k	.027	.034	.027	.034	.024	.034
k_1	.027	.045	.027	.045	.024	.038
L	.500	.570	.500	.610	.500	.600
L_1		.050		.050		
L_2	.250		.250			
α	45° BSC		36° BSC		45°	
ϕb	.016	.019	.016	.019		
ϕb_1	.016	.021	.016	.021	.016	.021
ϕD	.350	.370	.350	.370	.590	.610
ϕD_1	.305	.335	.305	.335	.540	.560
ϕD_2	.120	.160	.120	.160	.390	.410
Q	.015	.045	.015	.045		

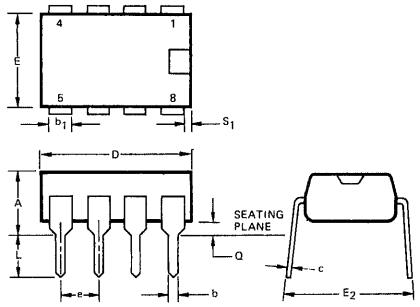
Notes: 1. Standard lead finish is bright acid tin plate or gold plate.
2. ϕb applies between L_1 and L_2. ϕb_1 applies between L_1 and 0.500" beyond reference plane.

B

PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES

P-8-1



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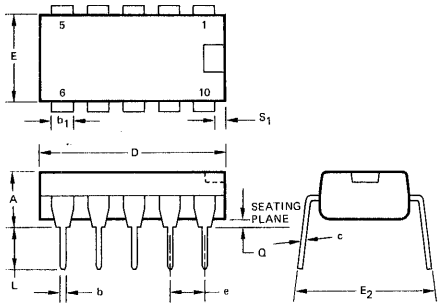
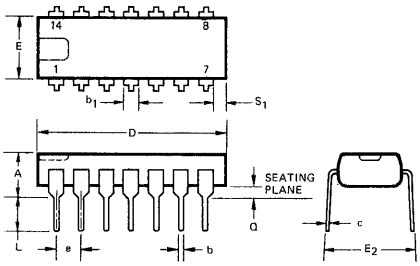
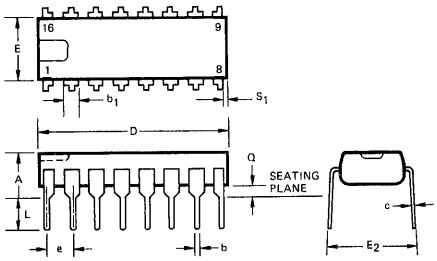


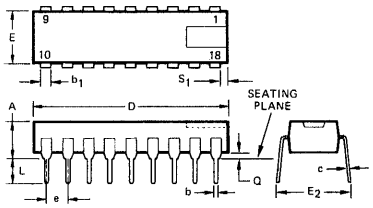
P-14-1



P-16-1



P-18-1



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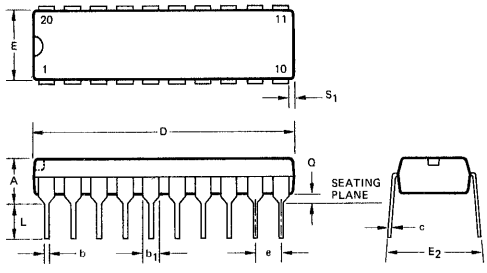

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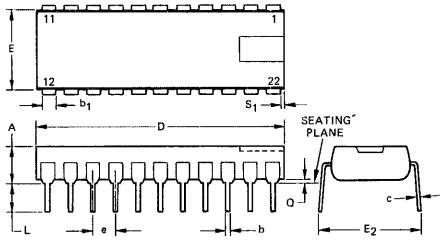
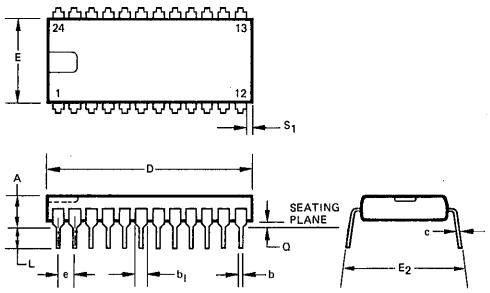


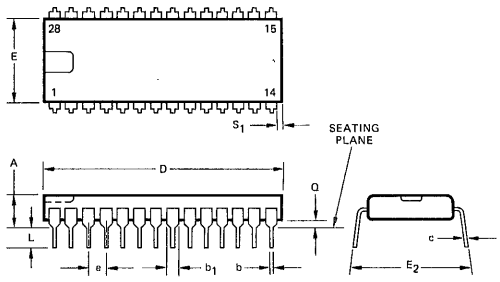
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES (Cont.)

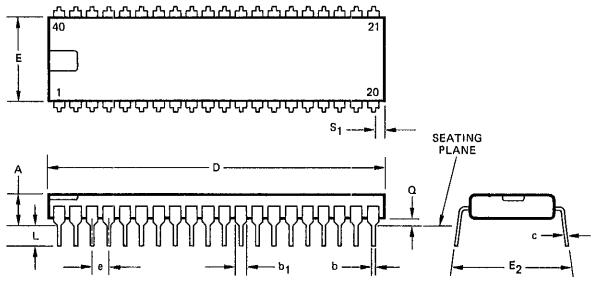
P-24-1



P-28-1



P-40-1



AMD Pkg.	P-8-1		P-10-1		P-14-1		P-16-1		P-18-1		P-20-1		P-22-1		P-24-1		P-28-1		P-40-1	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215	.150	.200	.150	.200
b	.015	.022	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.375	.395	.505	.550	.745	.775	.745	.775	.895	.925	1.010	1.050	1.080	1.120	1.240	1.270	1.450	1.480	2.050	2.080
E	.240	.260	.240	.260	.240	.260	.240	.260	.240	.260	.250	.290	.330	.370	.515	.540	.530	.550	.530	.550
E_2	.310	.385	.310	.385	.310	.385	.310	.385	.310	.385	.310	.385	.410	.480	.585	.700	.585	.700	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.010	.030	.040	.070	.040	.065	.010	.040	.030	.040	.025	.055	.015	.045	.035	.065	.040	.070	.040	.070

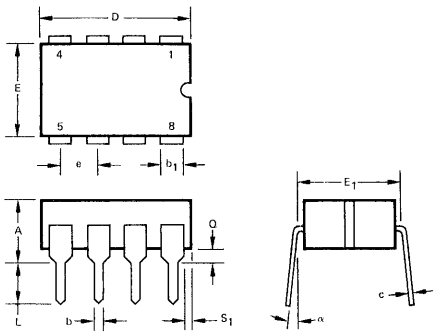
Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension E_2 is an outside measurement.

B

PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

D-8-1



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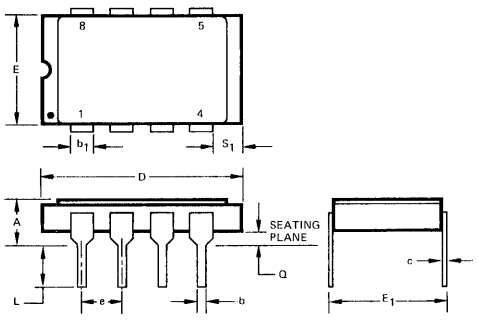

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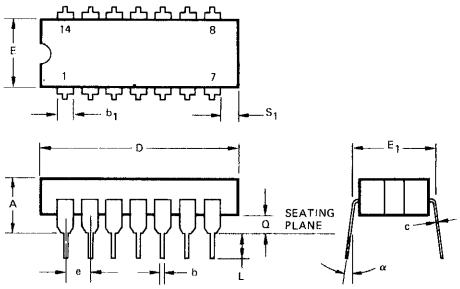
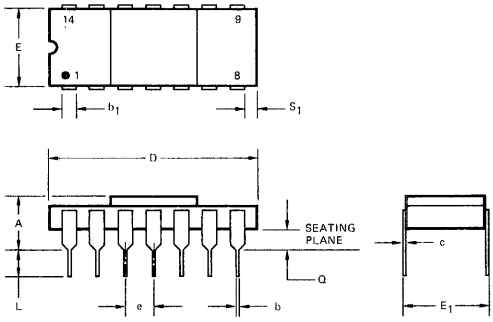
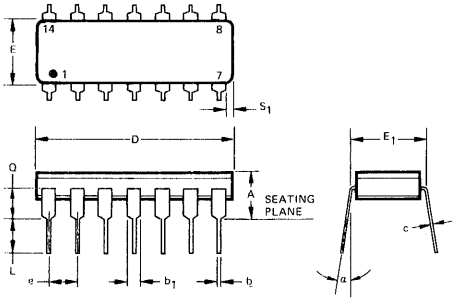


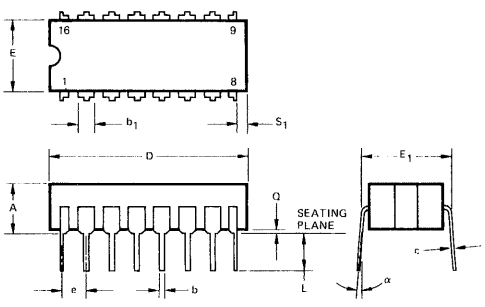
D-14-2



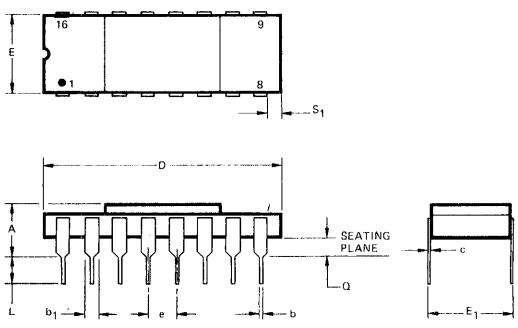
D-14-3



D-16-1



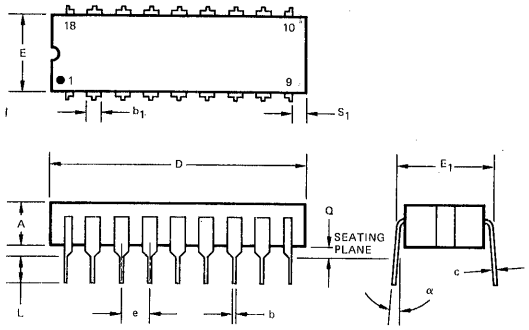
D-16-2



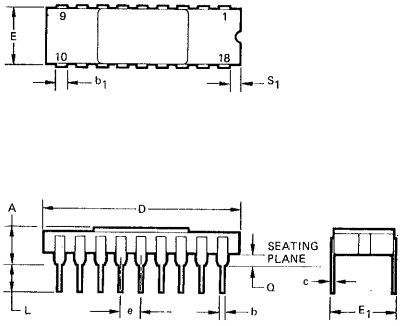
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

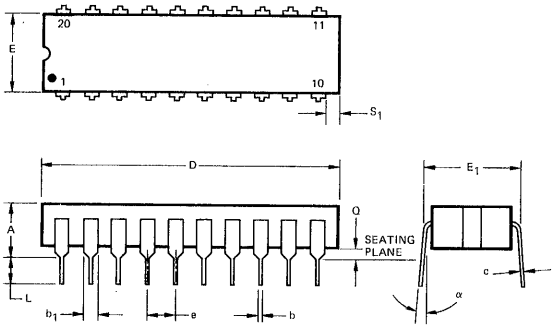
D-18-1



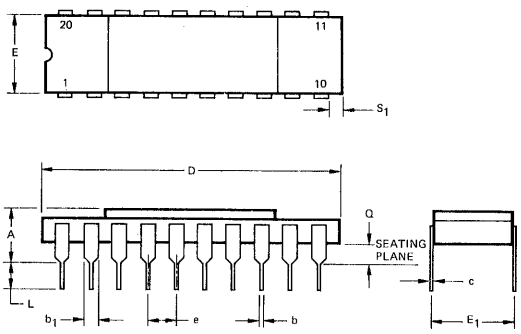
D-18-2



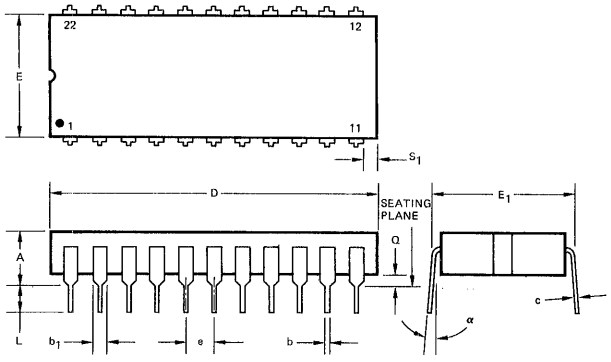
D-20-1



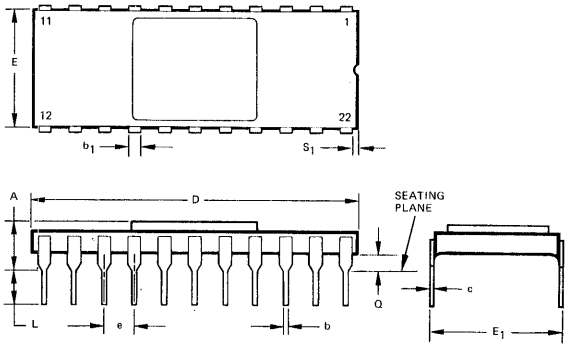
D-20-2



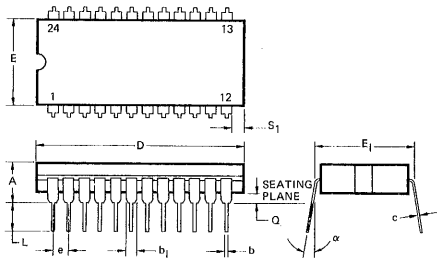
D-22-1



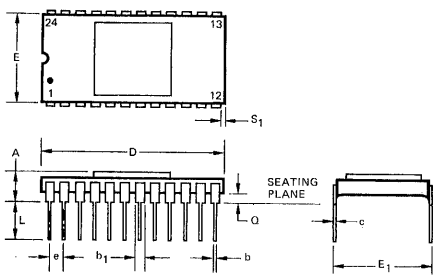
D-22-2



D-24-1 and D-24-4



D-24-2

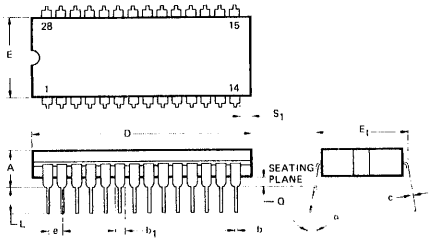


B

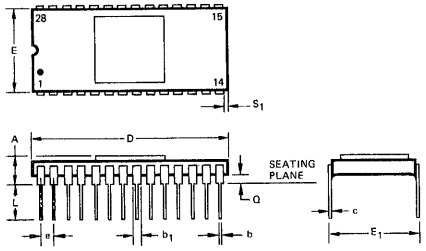
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

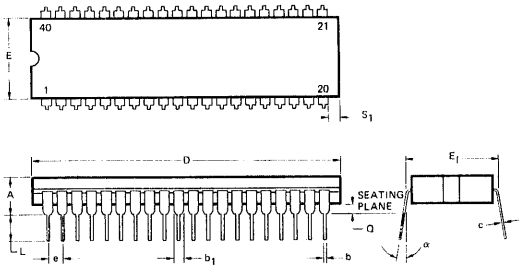
D-28-1



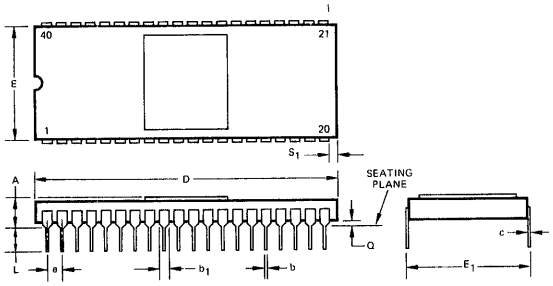
D-28-2



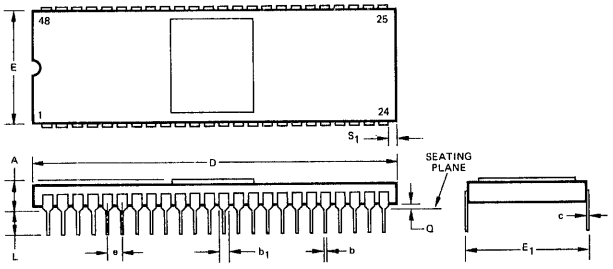
D-40-1



D-40-2



D-48-2



PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

AMD Pkg.	D-8-1		D-8-2		D-14-1		D-14-2		D-14-3 (Note 2)		D-16-1		D-16-2	
Common Name	CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		METAL DIP		CERDIP		SIDE-BRAZED	
38510 Appendix C	–		–		D-1(1)		D-1(3)		D-1(1)		D-2(1)		D-2(3)	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.130	.200	.100	.200	.100	.200	.130	.200	.100	.200
b	.016	.020	.015	.022	.016	.020	.015	.022	.015	.023	.016	.020	.015	.022
b_1	.050	.070	.040	.065	.050	.070	.040	.065	.030	.070	.050	.070	.040	.065
c	.009	.011	.008	.013	.009	.011	.008	.013	.008	.011	.009	.011	.008	.013
D	.370	.400	.500	.540	.745	.785	.690	.730	.660	.785	.745	.785	.780	.820
E	.240	.285	.260	.310	.240	.285	.260	.310	.230	.265	.240	.310	.260	.310
E_1	.300	.320	.290	.320	.290	.320	.290	.320	.290	.310	.290	.320	.290	.320
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150	.125	.160	.100	.150	.125	.150	.125	.160
Q	.015	.060	.020	.060	.015	.060	.020	.060	.020	.080	.015	.060	.020	.060
S_1	.004		.005		.010		.005		.020		.005		.005	
α	3°	13°			3°	13°			3°	13°	3°	13°		
Standard Lead Finish	b		b or c		b		b or c		c		b		b or c	

AMD Pkg.	D-18-1		D-18-2		D-20-1		D-20-2		D-22-1		D-22-2		D-24-1	
Common Name	CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERDIP	
38510 Appendix C	–		–		–		–		–		–		D-3(1)	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.140	.220	.100	.200	.140	.220	.100	.200	.150	.225
b	.016	.020	.015	.022	.016	.020	.015	.022	.016	.020	.015	.022	.016	.020
b_1	.050	.070	.040	.065	.050	.070	.040	.065	.045	.065	.030	.060	.045	.065
c	.009	.011	.008	.013	.009	.011	.008	.013	.009	.011	.008	.013	.009	.011
D	.870	.920	.850	.930	.935	.970	.950	1.010	1.045	1.110	1.050	1.110	1.230	1.285
E	.280	.310	.260	.310	.245	.285	.260	.310	.360	.405	.360	.410	.510	.545
E_1	.290	.320	.290	.320	.290	.320	.290	.320	.390	.420	.390	.420	.600	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150	.125	.160	.125	.150	.125	.160	.120	.150
Q	.015	.060	.020	.060	.015	.060	.020	.060	.015	.060	.020	.060	.015	.060
S_1	.005		.005		.005		.005		.005		.005		.010	
α	3°	13°			3°	13°			3°	13°			3°	13°
Standard Lead Finish	b		b or c		b		b or c		b		b or c		b	

B

PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

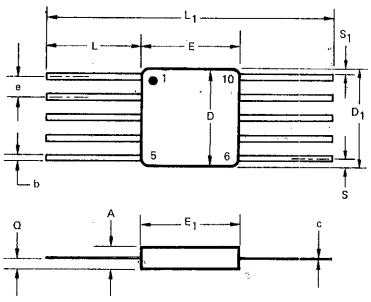
AMD Pkg.	D-24-2		D-24-4		D-28-1		D-28-2		D-40-1		D-40-2		D-48-2	
Common Name	SIDE-BRAZED		CERVIEW		CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		SIDE-BRAZED	
38510 Appendix C	D-3(3)		–		–		–		D-5		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.100	.200	.150	.225	.150	.225	.100	.200	.150	.225	.100	.200	.100	.200
b	.015	.022	.016	.020	.016	.020	.015	.022	.016	.020	.015	.022	.015	.022
b_1	.030	.060	.045	.065	.045	.065	.030	.060	.045	.065	.030	.060	.030	.060
c	.008	.013	.009	.011	.009	.011	.008	.013	.009	.011	.008	.013	.008	.013
D	1.170	1.200	1.235	1.280	1.440	1.500	1.380	1.420	2.020	2.100	1.960	2.040	2.370	2.430
E	.550	.610	.510	.550	.510	.550	.560	.600	.510	.550	.550	.610	.570	.610
E_1	.590	.620	.600	.630	.600	.630	.590	.620	.600	.630	.590	.620	.590	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.120	.160	.120	.150	.120	.150	.120	.160	.120	.150	.120	.160	.125	.160
Q	.020	.060	.015	.060	.015	.060	.020	.060	.015	.060	.020	.060	.020	.060
S_1	.005		.010		.005		.005		.005		.005		.005	
α			3°	13°	3°	13°			3°	13°				
Standard Lead Finish	b or c				b		b		b		b or c		b or c	

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

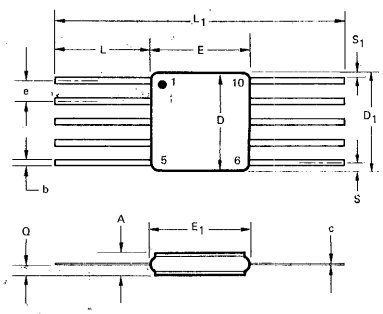
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

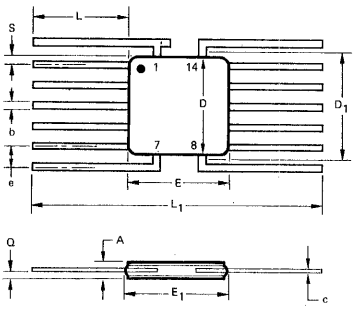
F-10-1



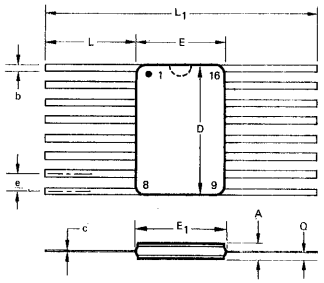
F-10-2



F-14-1 and F-14-2

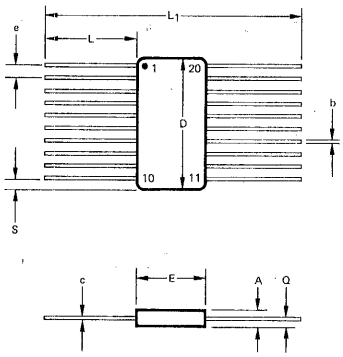


F-16-1 and F-16-2

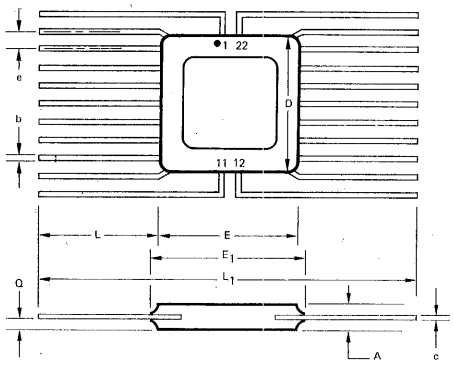


Note: Notch is pin 1 index on cerpack.

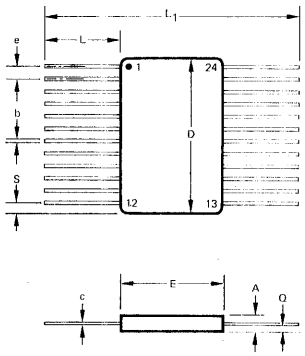
F-20-1



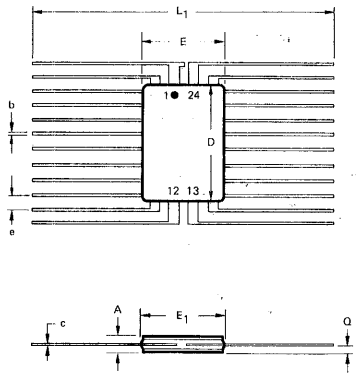
F-22-1



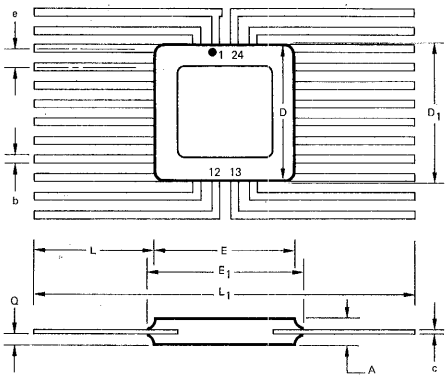
F-24-1



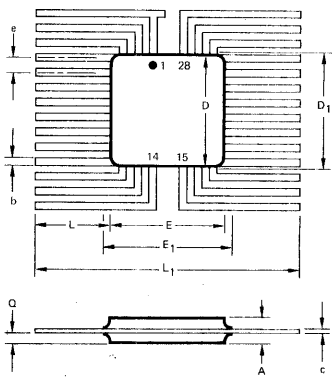
F-24-2



F-24-3



F-28-1

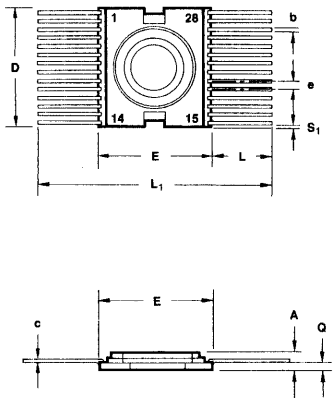


B

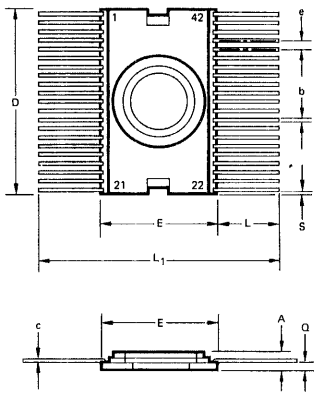
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES (Cont.)

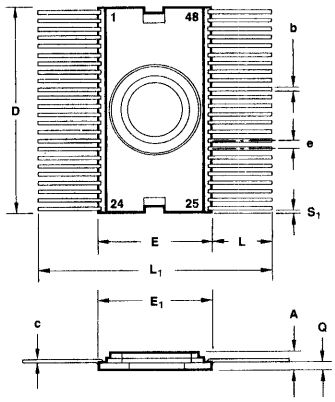
F-28-2



F-42-1



F-48-2



AMD Pkg.	F-10-1		F-10-2		F-14-1		F-14-2		F-16-1		F-16-2		F-20-1		F-22-1	
Common NAME	CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK	
38510 Appendix C	F-4		F-4		.F-1		F-1		F-5		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.045	.080	.045	.080	.045	.080	.045	.085	.045	.085	.045	.085	.045	.085	.045	.090
b	.015	.019	.012	.019	.015	.019	.012	.019	.015	.019	.015	.019	.015	.019	.015	.019
c	.004	.006	.003	.006	.004	.006	.003	.006	.004	.006	.003	.006	.004	.006	.003	.006
D	.230	.255	.235	.275	.230	.255	.230	.270	.370	.425	.370	.400	.490	.520	.380	.420
D_1				.275				.280				.410				.440
E	.240	.260	.240	.260	.240	.260	.240	.260	.245	.285	.245	.285	.245	.285	.380	.420
E_1		.275		.280		.275		.280		.290		.305		.290		.440
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.250	.320
L_1	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980
Q	.010	.040	.010	.040	.010	.040	.010	.040	.020	.040	.010	.040	.020	.040	.010	.040
S_1	.005		.005		.005		.005		.005		.005		.005			
Standard Lead Finish	b		c		b		c		b		c		b		c	

AMD Pkg.	F-24-1		F-24-2		F-24-3		F-28-1		F-28-2		F-42-1		F-48-2	
Common Name	CERPACK		METAL FLAT PAK		METAL FLAT PAK		METAL FLAT PAK		CERAMIC FLAT PAK		CERAMIC FLAT PAK		CERAMIC FLAT PAK	
38510 Appendix C	F-6		F-8		–		–		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.050	.090	.045	.090	.045	.090	.045	.080	.065	.085	.070	.115	.070	.110
b	.015	.019	.015	.019	.015	.019	.015	.019	.016	.025	.017	.023	.018	.022
c	.004	.006	.003	.006	.003	.006	.003	.006	.007	.010	.006	.012	.006	.010
D	.580	.620	.360	.410	.380	.420	.360	.410	.700	.720	1.030	1.090	1.175	1.250
D_1				.420		.440		.410		.720		1.090		1.250
E	.360	.385	.245	.285	.380	.420	.360	.410	.625	.650	.620	.660	.615	.670
E_1		.410		.305		.440		.410		.650		.660		.670
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.265	.320	.300	.370	.250	.320	.270	.320	.415	.435	.320	.370	.320	.370
L_1	.920	.980	.920	.980	.920	.980	.955	1.000	1.475	1.500	1.300	1.370	1.310	1.365
Q	.020	.040	.010	.040	.010	.040	.010	.040	.017	.025	.020	.060	.020	.055
S_1	.005		.005		0		0		.005		.005		.015	
Standard Lead Finish	b		c		c		c		c		c		c	

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions E_1 and D_1 allow for off-center lid, meniscus, and glass overrun.

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