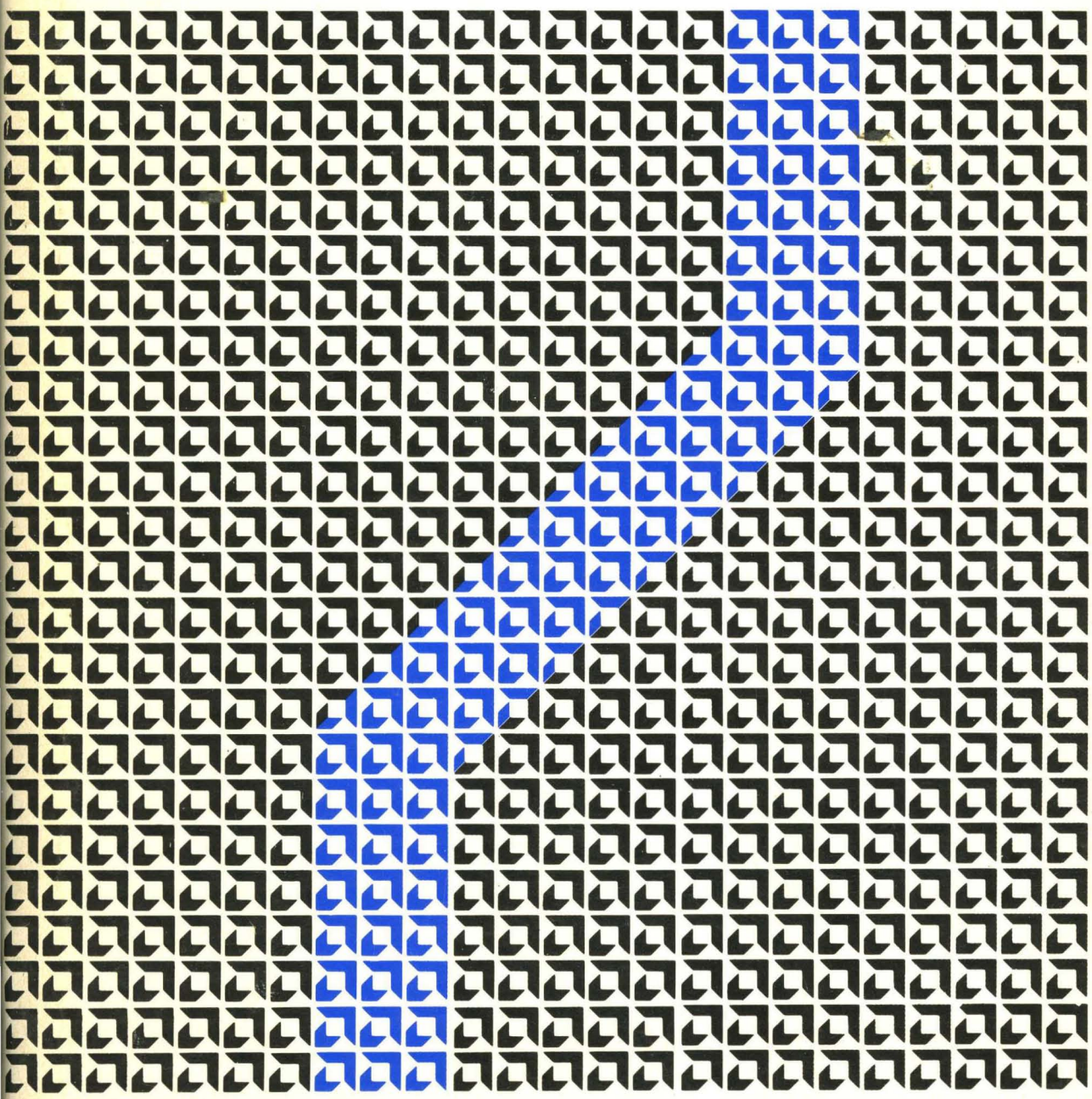
Advanced Micro Devices

Bipolar Generic PROMs



ADVANCED MICRO DEVICES

Bipolar Memory
Generic PROM Series

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INTRODUCTION

GENERIC SERIES CHARACTERISTICS

The devices included in this book are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

TABLE OF CONTENTS

Bipolar PROM Cross Reference Guide

AMD Part No.	Size	Organization	Output	Package Pins	Fairchild	Harris	Intel	Intersil	Monolithic Memories	National	Signetics	TI
Am27LS18 (Low Power)	256	32 x 8	OC	16					53/63LS080		N/S82S23	
Am27LS19 (Low Power)	256	32 x 8	3S	16					53/63LS081		N/S82S123	
Am27S18	256	32 x 8	OC	16		HM7602		IM5600	53/6330-1	DM75/8577 DM54/74S188	N/S82S23	SN54/74188A SN54/74S188
Am27S19	256	32 x 8	3S	16		HM7603		IM5610	53/6331-1	DM75/8578 DM54/74S288	N/S82S123	SN54/74S288
Am27S20	1024	256 x 4	OC	16	93417	HM7610	3601	IM5603A IM56S03	53/6300-1	DM54/74S387	N/S82S126	SN54/74S387
Am27S21	1024	256 x 4	3S	16	93427	HM7611	3621	IM5623 IM56S23	53/6301-1	DM54/74S287	N/S82S129	SN54/74S287
Am27S12	2048	512 x 4	OC	16	93436	HM7620	3602	IM5604 IM56S04	53/6305-1	DM54/74S570	N/S82S130	
Am27S13	2048	512 x 4	3S	16	93446	HM7621	3622	IM5624 IM56S24	53/6306-1	DM54/74S571	N/S82S131	
Am27S15	4096	512 x 8	3S	24		HM7647R					N/S82S115	
Am27S25	4096	512 x 8	3S	24								
Am27S26	4096	512 x 8	OC	22								
Am27S27	4096	512 x 8	3S	22								
Am27S28	4096	512 x 8	OC	20		HM7648			53/6348	DM54/74S473	N/S82S146	SN54/74S473
Am27S29	4096	512 x 8	3S	20		HM7649			53/6349	DM54/74S472	N/S82S147	SN54/74S472
Am27S30	4096	512 x 8	OC	24	93438	HM7640	3604	IM5605	53/6340	DM77/87S475	N/S82S140	SN54/74S475
Am27S31	4096	512 x 8	3S	24	93448	HM7641	3624	IM5625	53/6341	DM77/87S474	N/S82S141	SN54/74S474
Am27S32	4096	1024 x 4	OC	18	93452	HM7642	3605	IM5606	53/6352	DM54/74S572	N/S82S136	SN54/74S477
Am27S33	4096	1024 x 4	3S	18	93453	HM7643	3625	IM5626	53/6353	DM54/74S573	N/S82S137	SN54/74S476
Am27S180	8192	1024 x 8	OC	24	93450	HM7680	3608		53/6380	DM77/87S180	N/S82S180	SN54/74S479
Am27S181	8192	1024 x 8	3S	24	93451	HM7681	3628		53/6381	DM77/87S181	N/S82S181	SN54/74S478
Am27S184*	8192	2048 x 4	OC	18		HM7684			53/63100	DM77/87S184	N/S82S184	
Am27S185*	8192	2048 x 4	3S	18		HM7685			53/63101	DM77/87S185	N/S82S185	

*Available 1st Qtr. 1980

Bipolar PROM Selection Guide

Device	Size	Organization	Output	Package Pins	Max Access Time (ns) COM'L	Max Access Time (ns) MIL	Max I_{CC}(mA)	Other Features
Am27LS18 (Note 2)	256	32 x 8	OC	16	50	65	80	Low Power
Am27LS19 (Note 2)	256	32 x 8	3S	16	50	65	80	Low Power
Am27S18	256	32 x 8	OC	16	40	50	115	
Am27S19	256	32 x 8	3S	16	40	50	115	
Am27S20	1024	256 x 4	OC	16	45	60	130	
Am27S21	1024	256 x 4	3S	16	45	60	130	
Am27S12	2048	512 x 4	OC	16	50	60	130	
Am27S13	2048	512 x 4	3S	16	50	60	130	
Am27S15	4096	512 x 8	3S	24	60	90	175/185 (Note 3)	Output Latches
Am27S25	4096	512 x 8	3S	24	N.A. (Note 4)	N.A. (Note 4)	185	Output Registers Slimline Package
Am27S26	4096	512 x 8	OC	22	N.A. (Note 4)	N.A. (Note 4)	185	Output Registers
Am27S27	4096	512 x 8	3S	22	N.A. (Note 4)	N.A. (Note 4)	185	Output Registers
Am27S28	4096	512 x 8	OC	20	55	70	160	
Am27S29	4096	512 x 8	3S	20	55	70	160	
Am27S30	4096	512 x 8	OC	24	55	70	175	
Am27S31	4096	512 x 8	3S	24	55	70	175	
Am27S32	4096	1024 x 4	OC	18	55	70	140/145 (Note 3)	
Am27S33	4096	1024 x 4	3S	18	55	70	140/145 (Note 3)	
Am27S180	8192	1024 x 8	OC	24	60	80	185	
Am27S181	8192	1024 x 8	3S	24	60	80	185	
Am27S184*	8192	2048 x 4	OC	18	60	70	130	
Am27S185*	8192	2048 x 4	3S	18			130	

*Available 1st Qtr. 1980.

Notes: 1. COM'L = 0 to 75°C, V_{CC} = 5V ±5%
MIL = −55 to +125°C, V_{CC} = 5V ±10%
2. Replaces Am27LS08/09
3. COM'L/MIL
4. Normal access time not applicable – this product contains built-in pipeline registers – nominal address to clock set up time typ 40ns. Clock to output typ 15ns.

TECHNICAL REPORT

RELIABILITY REPORT
BIPOLAR GENERIC PROM SERIES

ABSTRACT

This report is a review of the manufacturing process, the circuit design techniques, the testing, the fuse element, and the reliability of Advanced Micro Devices' Generic Bipolar PROM Series. Results indicate that platinum silicide forms a fuse with excellent reliability characteristics.

The purpose of this report is to present a description of Advanced Micro Devices' Bipolar PROM circuits, their manufacturing process and their reliability. Included is a discussion of the wafer fabrication in which an advanced, highly reliable platinum silicide fuse is utilized, a description of the circuits and their testing, an analysis of the fusing characteristics of platinum silicide and supportive reliability data.

The products evaluated in this report are members of a generic family of field programmable-read-only memories (PROMs) from 256 bits through 8192 bits. All of these devices use the manufacturing process described in this report. The circuit design concepts are similar on each of the PROMs with the result that the products can be programmed using the same hardware. Only the socket adaptor required for the PROM configuration and pin count is different. The same programming algorithm is used for all devices with completely satisfactory results. The PROMs utilize a platinum Schottky diode structure with barrier metal. Dual-layer metallization is also employed to maximize speed and minimize chip size. All Advanced Micro Devices' circuits receive screening per MIL-STD-883, Method 5004 class C. Ongoing reliability monitors confirm the continuing integrity of these products.

Prepared by: Advanced Micro Devices Quality and Reliability Department in Conjunction with Bipolar Memory Engineering.

Advanced Micro Devices cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Advanced Micro Devices' product.

THE PROCESS TECHNOLOGY

Advanced Micro Devices has chosen a platinum silicide Schottky, washed emitter, dual-layer metal process for its bipolar PROMs. Platinum silicide has been chosen as the material to form the fuse for several reasons. First, it has been demonstrated to be an extremely reliable fuse material. It does not have the growback phenomenon common to nichrome technologies; it is not moisture sensitive in freeze-out tests; it is less fragile than nichrome, and it does not have mass transport problems associated with moderate current densities. Second, the manufacturing process is easily controlled with regard to reliability factors and fusing currents. Third, the fuses are quite easy to form during the manufacturing process without a substantial number of additional processing steps.

Figure 2 is a cross section of a transistor and a fuse. A heavily doped buried layer diffusion is first performed to allow for the fabrication of NPN transistors with low saturation resistances. A thin epitaxial layer is grown followed by isolation and base diffusions. The isolation and base are effectively self-aligned using a composite masking approach. A short series of steps results in the definition of polycrystalline silicon in the shape of the fuse.

A second composite mask now defines all the emitter, contact, Schottky diode and ohmic contact areas.

Following the emitter diffusion and the contact mask, platinum is sputtered over the entire wafer. Since all contacts, Schottkies, and fuses are exposed at this point, an alloying operation allows platinum silicide to form. The residual platinum is etched off the wafer leaving the silicide contacts, Schottkies, and fuses. After this step, the semiconductor elements of the circuit have been completely formed, and all that remains is the interconnect metallization.

To form the interconnects, aluminum is used as the primary conducting element. Aluminum has a very strong affinity for silicon, including that in platinum silicide. To retain the advantages of the very stable platinum silicide Schottky devices, it is necessary to sputter an inactive metal, tungsten, with a small amount of titanium as a bonding agent over the surface of the wafers to serve as a barrier to the diffusion or microalloying of the aluminum. Aluminum is now evaporated over the surface of the wafers and conventional masking and etching cycles are used to define the aluminum interconnections. Figure 3 shows the structure of this metal layer.

To complete the dual-layer metallization structure, silicon dioxide is chemically vapor deposited on the wafer and etched with interlayer metal contact openings (vias). A second layer of aluminum is then placed on top of the dielectric. This layer has a thickness substantially greater than the first one and is especially suited for power busses and output lines.

To complete the circuit, a passivation layer is deposited over the top of the wafers and etched at the appropriate locations to allow for bonding pad contact.

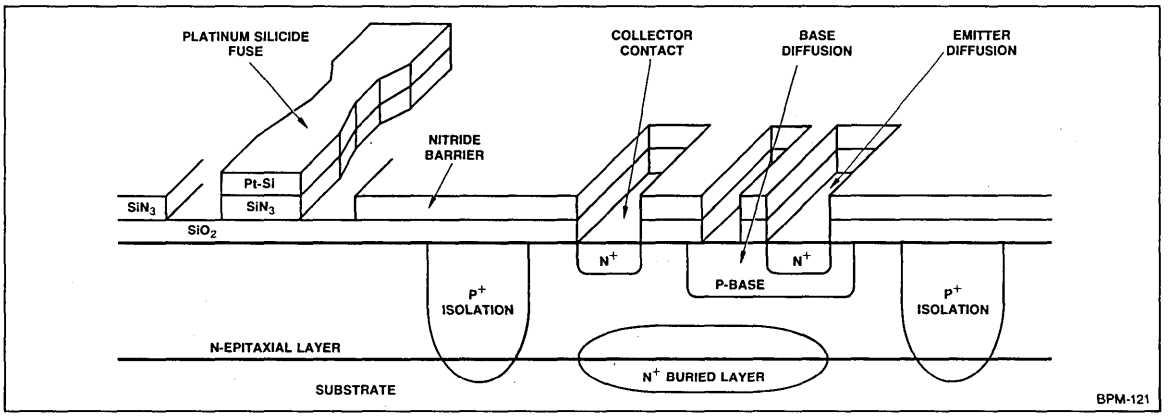


Figure 2. Transistor & Fuse Structures.

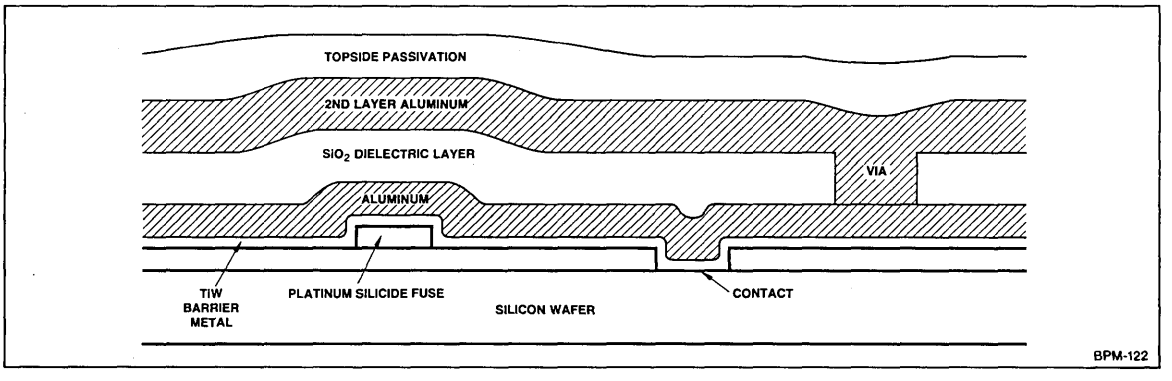


Figure 3. 2 Layer Metallization Structure.

PROGRAMMABLE READ-ONLY MEMORY CIRCUITRY

Advanced Micro Devices' bipolar PROM designs have the general configuration shown in Figure 4. Although the figure is for that of the Am27S20, the circuit techniques are the same for the entire generic family of PROMs.

Input, Memory & Output Circuitry

Two groups of input buffers and decoders called "X" and "Y" are used to drive word lines and columns respectively. The X-decode addresses (A_3-A_7) have Schottky clamp diode protected, PNP inputs for minimum loading. (Figure 5). The X-input buffers (A_3-A_7) provide A and $\overline{A}$ outputs to a Schottky decode matrix which selects one of 64 word drivers. The word line drivers are very fast high current, high voltage, non-saturating buffers providing voltage pull down to the selected word line.

The Y-decode address buffers (A_0-A_2) are also Schottky diode clamped, PNP inputs driving a Schottky diode matrix. However, this diode matrix selects one of eight columns on each of the four output bits. The selected column line drives the sense amplifier input to a high level in the case of a blown fuse, or current is shunted through an unblown fuse through the selected word driver to ground resulting in a "low" input to the sense amplifier.

The sense amplifier is a proprietary fast level shifter-inverter with temperature and voltage threshold sensitivities compensated for the driving circuitry. Each of the four sense amplifiers in this circuit provides active drive to an output buffer.

Each output buffer also contains a disable input, which is driven from the chip-enable buffer. The chip-enable buffer input is a Schottky diode clamped PNP buffered design with an active pull up and pull down to drive the output buffer. Additionally, the chip-enable gate contains circuitry to provide fuse control as described below.

Fusing Circuitry

Platinum silicide fuses as implemented in Advanced Micro Devices' PROMs have extremely high fuse current to sense current ratios. Sensing normally requires that only a few hundred microamps flow through the fuse, whereas absolute minimum requirements for opening the fuse are approximately 100 times that amount. This provides a significant safety margin for transient protection and long-term reliability.

High-yield fusing of platinum silicide fuses requires that a substantial current be delivered to each fuse. This current is sourced from the output terminals through darlingtons which can drive the column lines when enabled. These darlingtons are driven directly from the output and are selected by the Y-decode column select circuitry. Current during fusing flows from the output through the darlington directly to the fuse

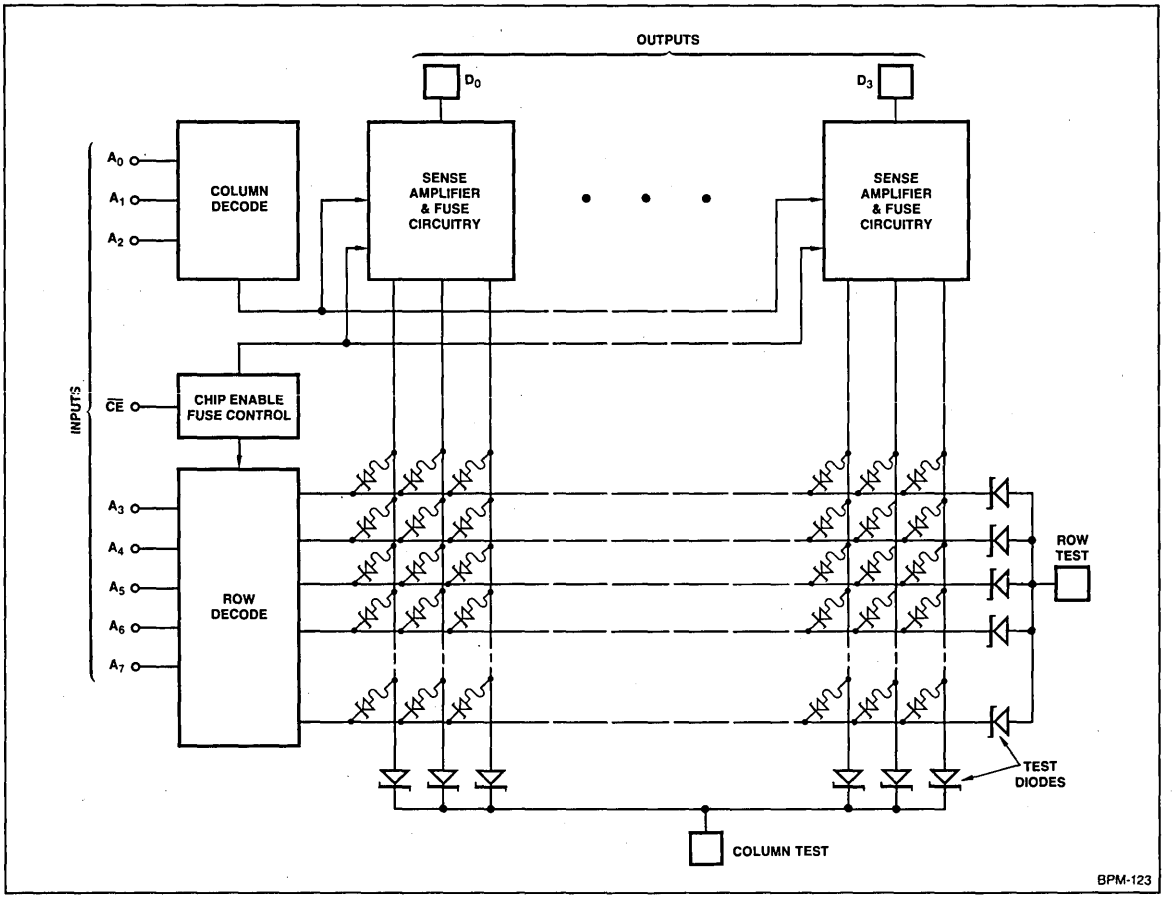


Figure 4. PROM Circuitry Block Diagram.

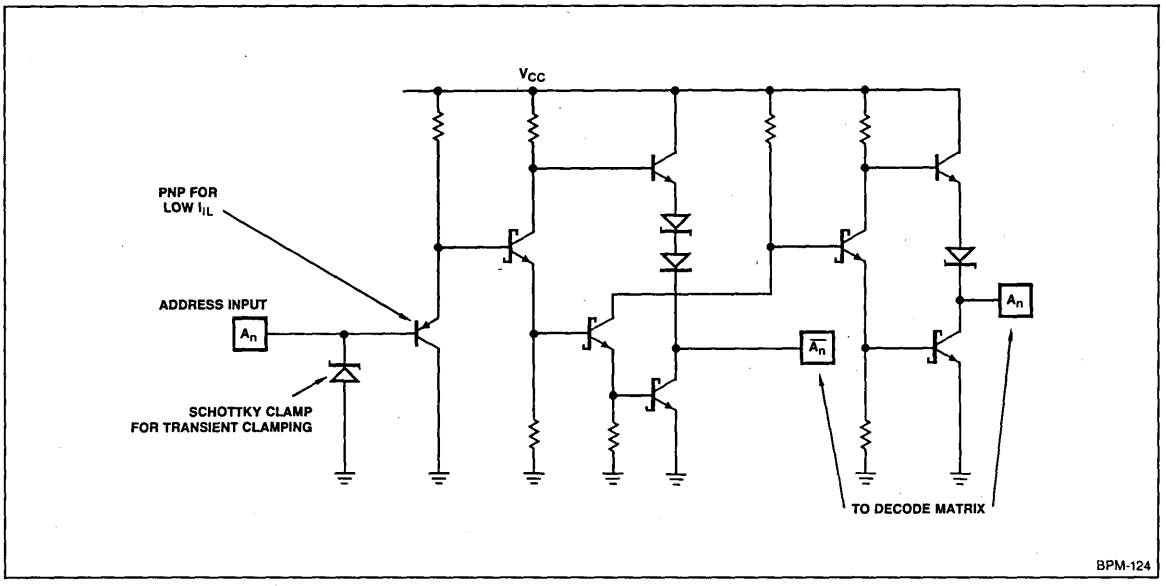


Figure 5. Input Buffer Schematic.

through the selected array Schottky and finally through the word-driver output transistor to ground. This path is designed for a very large fusing current safety margin.

The control circuitry works as follows: After V_{CC} is applied, the appropriate address is selected and the $\overline{CE}$ input is taken to a logic high, the programmer applies 20 volts to the bit output to be programmed. The application of the 20 volts simultaneously deselects the output buffer to prevent destructive current flow, and powers down internal circuitry unneeded during fusing to minimize chip heating.

It also enables the darlington base drive circuitry, makes power available to the darlington from the output and enables the fusing control circuitry. At this point, the PROM is ready for the control line at the chip-select pin to release the selected word driver to allow current flow through the fuse. This technique is particularly advantageous because the control signal does not supply the large fusing currents. They are supplied through the darlington from the output power supply. Some care must be taken to avoid excessive line inductance on the output line. Reasonable and normal amounts of care will reward the user with high-programming yields.

Special Test Circuitry

All Advanced Micro Devices PROMs include high-threshold voltage gates paralleling several address lines to allow the selection of special test words and the deselection of the columns to allow for more complete testing of the devices. Additionally, special test pads accessible prior to assembly allow for testing of some key attributes of the devices. The function of these special circuits will be described in more detail in the section, "Testing", later in this report.

THE PLATINUM SILICIDE FUSE

Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1. V_{CC} power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to one output;
5. The chip enable voltage is raised to enable high-threshold voltage gate. This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The output voltage is lowered; the programming voltage is removed.
7. The device is enabled and the bit is sensed to verify that the fuse is blown. In the unusual event that the fuse does not verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse opens; and,
8. The sequence of 2 through 7 is repeated for each bit which must be fused.

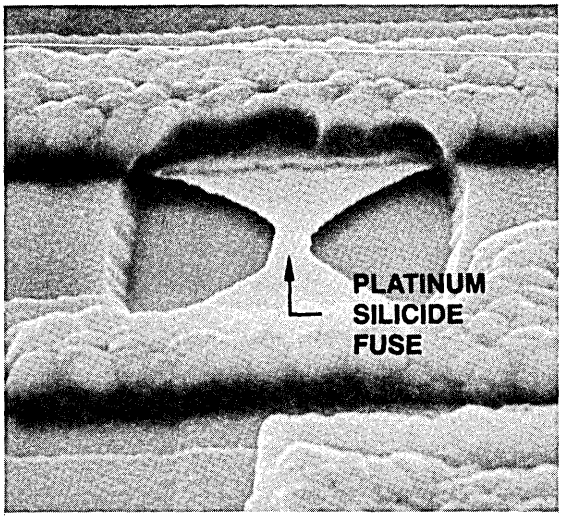
There are several advantages to this technique. First, the two high current power sources, V_{CC} and the voltage applied to the output do not have critical timing requirements. The low current chip select pin gates the fusing current into the circuit. Since it is generally desirable to gate the fusing current into the chip at relatively fast rates, the use of the chip select for this purpose avoids the speed trade-off which would exist using the output voltage as the control. The output voltage must not be raised too quickly to avoid breakdown and latchback conditions which might occur with sub-microsecond rise times on the output.

The second major advantage of this technique is that in the event that the fuse does not open during the first attempt to blow it, a near DC condition may be safely applied to it with no danger of developing a reliability problem such as that which occurs with nichrome fuses. This will be discussed in more detail later. The algorithm can therefore be designed first to minimize the time required to program the PROM, i.e. with a fast first pulse, and second, to maximize the probability that any circuit will program. Most PROMs do, of course, fuse satisfactorily with all short pulses. However, it is impossible for any manufacturer to guarantee absolutely that all fuses in all circuits receive 100 percent of the rated fusing current during programming.

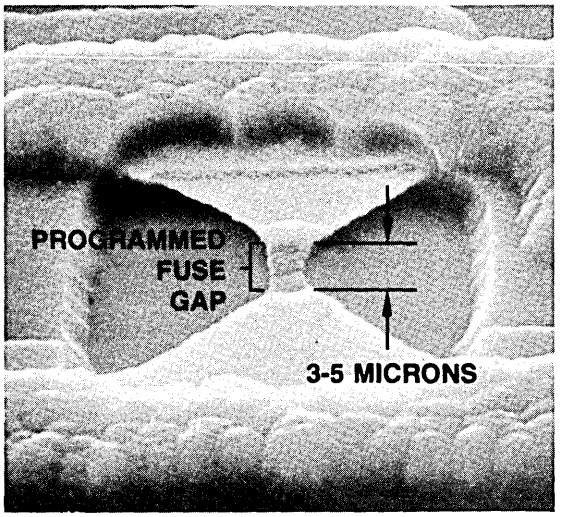
Circuit defects which may be resistant to pre-programming testing prevent such a guarantee. It is, therefore, quite important to have a fuse material insensitive to marginal conditions. Even the application of single, short pulses does not guarantee that no fuse received marginal amounts of current during fusing. The silicide fuse provides this safety margin and allows the programmer to maximize the possibility of fusing by applying near DC condition to the fuses.

Fuse Characteristics

When a fast (less than 500ns rise time) current pulse is applied to a fuse, the fuse voltage rises abruptly to a value approaching the level anticipated from calculations of the room temperature resistance. However, it quickly falls to a value of approximately two volts. This value is nearly independent of the applied current. During this period of time, typically, the fuse is molten. Very abruptly, the fuse current drops to zero indicating the separation of the platinum silicide into two distinct sections. Scanning Electron Microscope photographs of the resulting fuses (see Figure 6) indicate that the typical case is a sharp, clean separation in excess of a micron. This separation occurs in the center of the fuse because the bow-tie structure (see Figure 7) concentrates the energy density in the center away from the aluminum lines. The energy density in the center of the fuse is capable of creating temperatures substantially greater than required to melt the silicide. The very abrupt, high



Unprogrammed Fuse



Programmed Fuse

Figure 6.

power applied to the fuse melts the fuse center and results in a wicking of material on either side due to surface tension.

Reliability of Fuses Programmed Under Non-optimal Conditions

The marginally opened fuse has been studied in some detail even though it rarely occurs in practice. Under conditions where the fuse is purposely blown at much slower rates, it is possible for the fuse to assume a high impedance state which is sensed as an open fuse by the circuit. This occurs because the fuse cools before separation is achieved. Electrical and SEM studies of fuses blown with these characteristics indicate that a small conductive path of silicon remains of sufficiently high resistance to prevent appropriate power transfer required for complete opening on subsequent applications of power. Under these slow-blow conditions, the thermal conductivity of the silicon nitride pedestal on which the fuse rests, the silicon dioxode beneath that, and the silicon chip become factors because sufficient time exists for the heat flow to carry a significant amount of energy away from the fuse. This is extremely unusual in practice since it requires a rather narrow set of conditions. However, a number of PROMs have been specially programmed under these unusual conditions which can cause this type of fuse to occur. These devices have been life tested for over two thousand hours. No failures occurred in any of these circuits. It is clear from this study that partially opened platinum silicide fuses are stable. Although it is very rare to see such a fuse in a circuit which has been programmed under normal conditions, Advanced Micro Devices believes that such fuses do not represent a reliability hazard based on this study and the results of the other studies run on the programmable-read-only memories. It should be noted that most manufacturers carefully specify the conditions under which their devices *must* be programmed in order to avoid reliability problems. Reliability data available on these devices must be assumed to have been generated using optimally programmed devices. Advanced Micro Devices believes that the study described here and four billion fuse hours of data from many production lots of PROMs demonstrate the capability of the platinum slicide fuse under a wide variety of conditions.

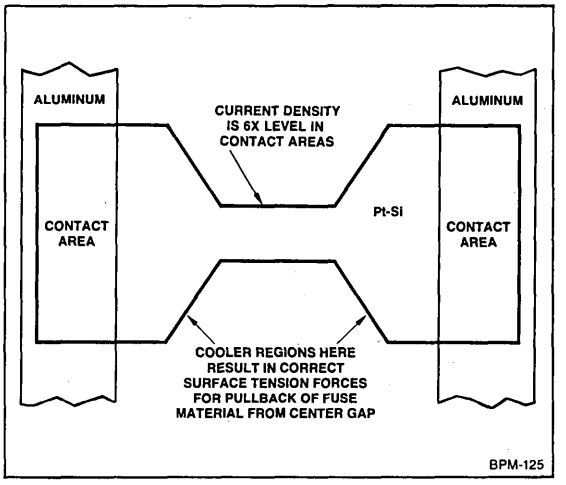


Figure 7. Bowtie Fuse Design.

FINAL TESTING OF ADVANCED MICRO DEVICES' MEMORIES

Wafer Level Tests

In addition to all the standard DC tests, Advanced Micro Devices performs a series of special tests to conform to the screening criteria of MIL-STD-883, Method 5004 3.3; also, AMD performs special tests to increase the confidence level of unique address selection and to demonstrate fusing capability on all columns and word drivers. To accomplish this, diodes are connected from the column lines and the word lines to special test pads which are accessible only during wafer probing. (See Figure 4). Using these diodes, Advanced Micro Devices confirms that each word driver is capable of sinking sufficient current to blow fuses, has appropriate saturation characteristics for AC performance, and has sufficient voltage breakdown to withstand fusing voltages. In addition, using special software, a sequence of tests dramatically increases the confidence of unique address selection on the address decoding. All darlingtons are checked to confirm that sufficient current drive is available to blow fuses from any column. Schottky diode array leakage is also checked to affirm that it is sufficiently low so as not to overload the pull down circuitry during the high-voltage application of fusing. Finally, high voltages are applied to the inputs and outputs to remove potentially weak devices before the PROM's are assembled.

Test Fusing

Each PROM has two additional word drivers connected to special test fuses. These test words are valuable in demonstrating beyond reasonable doubt that the device is capable of opening fuses in all columns. They also increase the confidence level in unique addressing. Furthermore, the test words serve as correlatable measures of the access times that the user can expect from his devices after he has placed his own program in the memory. These test words are not visible to the user unless he applies special voltages to certain address pins. Figure 8 is a diagram of this input circuit. One hundred percent of the PROM devices shipped from Advanced Micro Devices have had AC testing for access and enable times at high-and low-power supply voltages to affirm their AC characteristics.

The result of this extensive testing at both the wafer and finished device level is a product with very high-programming yields and virtually guaranteed AC performance after the user places his program in the parts. Additionally, the high voltage tests provide an additional level of confidence that the oxide and junction integrity is excellent in each circuit and that the devices will be relatively insensitive to small transients common to programming equipment.

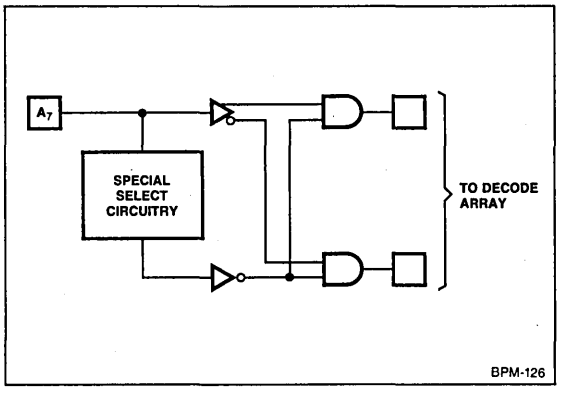


Figure 8. Special Input Circuit Used for Array Deselection and Test Word Check.

THE MANUFACTURING PROCESS

All products bearing the Advanced Micro Devices' logo will have screening meeting the requirements of the MIL-STD-883 Method 5004, for Class C microcircuits. A summary of the standard processing is shown below. The presence of the Advanced Micro Devices' logo on the package is confirmation that the screening has been completed. The only exceptions to this procedure are special products revised by contract for a customer's lesser requirements and distinctly marked for that customer alone. Standard burn-in option B is available on standard product which allows the customer to upgrade to Class B microcircuits.

Assembly and Environmental Standard Processing

1. Die Visual Inspection	Method 2010 Condition B
2. Wire Bond	Method 2010 Condition B rebonds less than 10 percent
3. Internal Visual	Method 2010 Condition B
4. Seal	
5. High Temperature Storage	Method 1008 Condition C
6. Temperature Cycle	Method 1010 Condition C
7. Constant Acceleration	Method 2001 Condition E
8. Visual Inspection	Method 5004
9. Fine Leak	Method 1014 Condition A or B
10. Gross Leak	Method 1014 Condition C Step 2

Note: Steps 7-10 not required for solid packages.

Electrical Test through Shipping Standard Processing

1. Initial Electrical Test	Method 5004 to device specifications.
2. Group A Electrical	Method 5005, Class B quality levels.
3. Mark	Per customer order or Advanced Micro Devices catalog identification.
4. External Visual	Method 2009
5. Sample Quality Inspection	Physical or electrical verification of product identity.

RELIABILITY TESTING

Advanced Micro Devices has an ongoing reliability program to evaluate its bipolar memory products. Reliability testing conforms to MIL-STD-883 Method 1005 Conditions C or D. Examples of the test circuits used are shown in Figure 9. Data has now been accumulated on the process described here in excess of ten thousand hours on some devices. Over four billion fuse hours have been completed with no fuse oriented failures.

Advanced Micro Devices selects samples of its product stratified by product type at periodic intervals for this testing. Thus, the tests are representative of a total cross section of time and product base during the past year and a half. Figure 10 is a tabulation of the results of the lots placed on test during this period of time. The data demonstrates a highly reliable process. The fuse has an immeasurably low contribution to the failure rate at this point in the reliability testing.

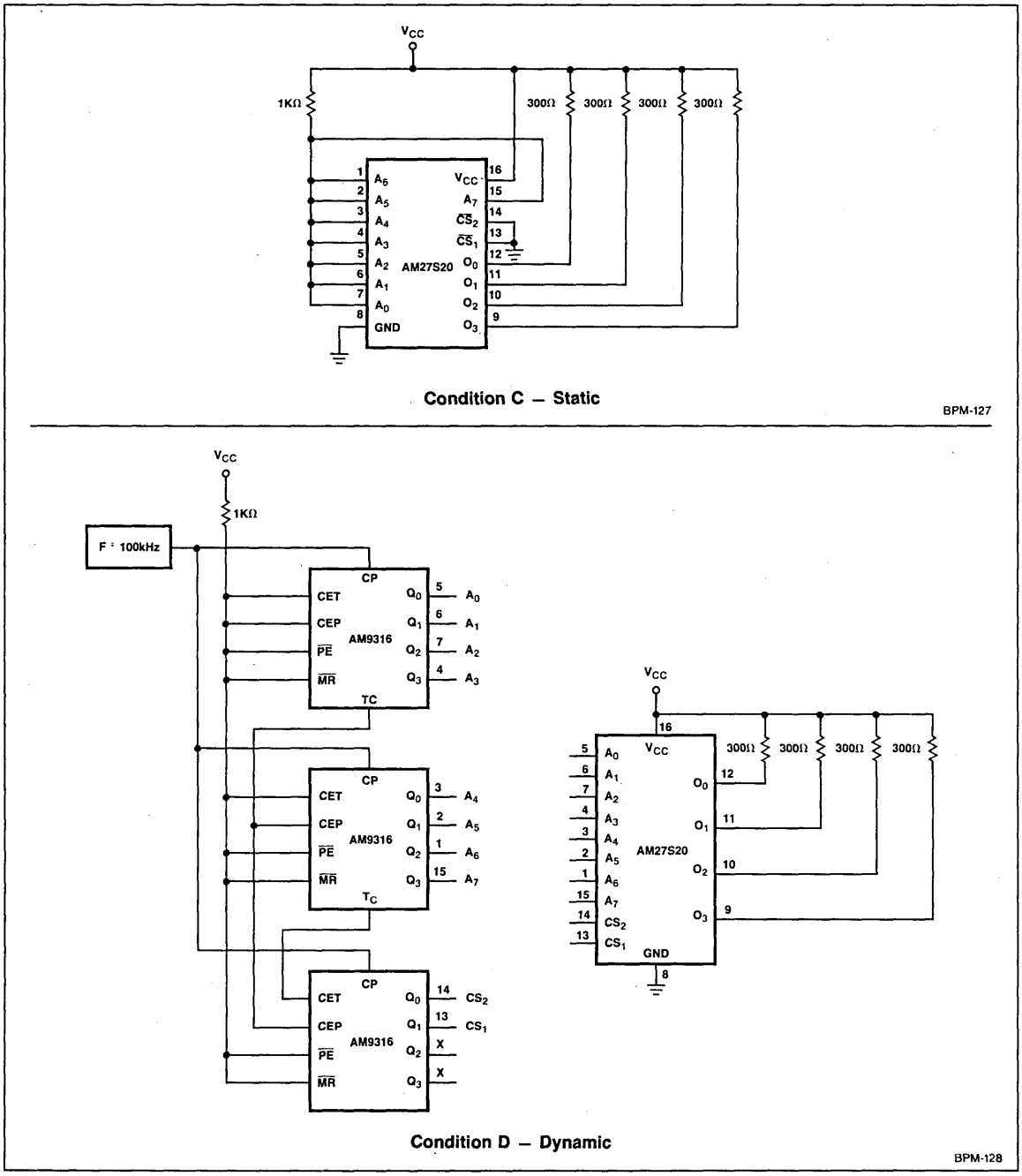


Figure 9. Burn-In Circuits For Conditions C & D-27S20.

BIPOLAR MEMORY RELIABILITY SUMMARY

Product	Production Lots	Units Tested	Total Unit-Hours	Total Fuse Hours (billions)	Unit Failures	Fuse Related Failures	Unit Failure Rate @ 60% Confidence %/1000 hrs. at 125°C	Unit Failure Rate* @ 60% Confidence %/1000 hrs. at 70°C
27S20/21 (1K Bit PROM)	10	731	1,610,000	1.648B	2**	0	0.12	0.0011
27S12/13 (2K Bit PROM)	7	156	1,011,000	2.070B	0	0	0.10	0.0009
27S15 27S26/27 (4K Bit PROM)	7	136	139,000	0.569	0	0	0.72	0.0067
Totals For PROM Products	24	1023	2,760,000	4.287	2**	0	0.072	0.0007

*Assuming an activation energy of 1.0 eV.
**Oxide failures

Figure 10.

SUMMARY

The Advanced Micro Devices' bipolar memory process has been described with particular emphasis on programmable-read-only memories. An advanced form of the low-power Schottky process is used in conjunction with a highly reliable and stable platinum silicide fuse. Extensive testing and screening have been used to assure that the products will meet all specification after the user has placed his program into the device and that the circuit reliability will be outstanding.

Am27LS18 • Am27LS19

Low-Power Schottky 256-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 50ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

FUNCTIONAL DESCRIPTION

The Am27LS18 and Am27LS19 are high speed electrically programmable Schottky read-only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector (Am27LS18) and three-state (Am27LS19) output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_4 and holding the chip select input, CS, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

GENERIC SERIES CHARACTERISTICS

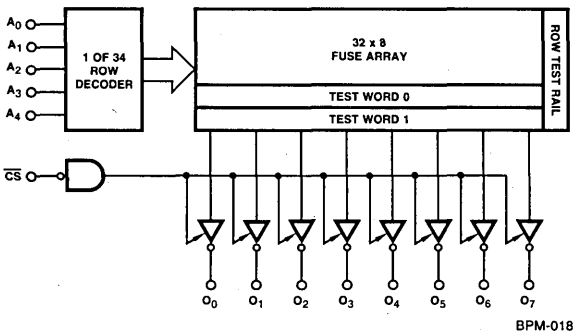
The Am27LS18 and Am27LS19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

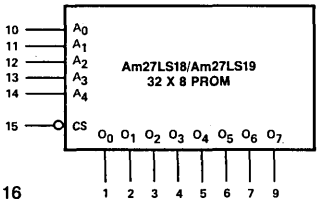
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



BPM-018

LOGIC SYMBOL



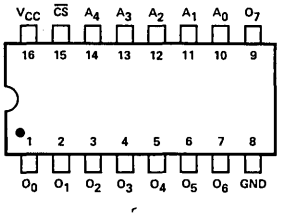
V_{CC} = Pin 16
GND = Pin 8

BPM-019

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27LS18DC
Hermetic DIP	−55°C to +125°C	AM27LS18DM
Hermetic Flat Pak	−55°C to +125°C	AM27LS18FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27LS19DC
Hermetic DIP	−55°C to +125°C	AM27LS19DM
Hermetic Flat Pak	−55°C to +125°C	AM27LS19FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-020

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27LS18XC, Am27LS19XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27LS18XM, Am27LS19XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27LS19 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27LS19 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		60	80	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

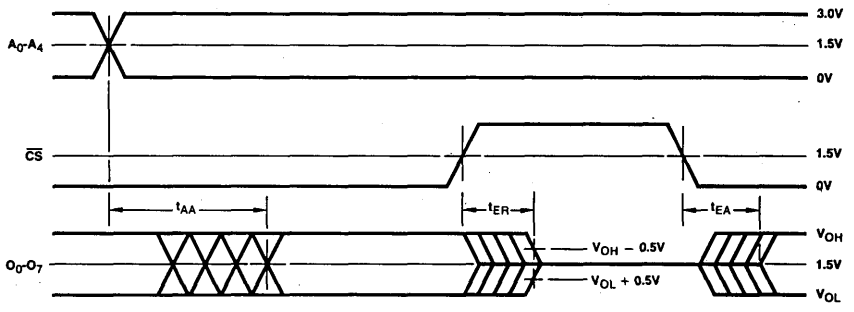
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	55	75	ns
t_{EA}	Enable Access Time		22	40	50	ns
t_{ER}	Enable Recovery Time		18	35	40	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

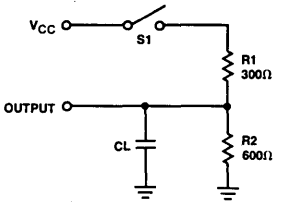
BPM-021

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
⋈⋈⋈	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE. "OFF" STATE

AC TEST LOAD



BPM-022

PROGRAMMING

The Am27LS18 and Am27LS19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

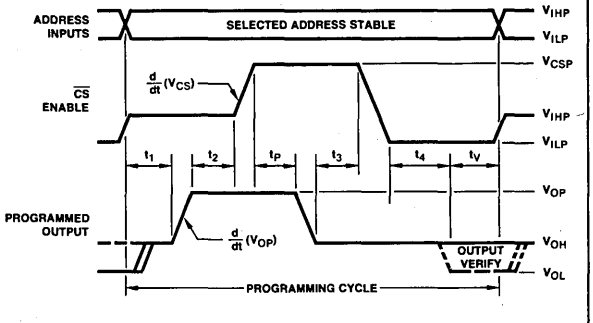
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

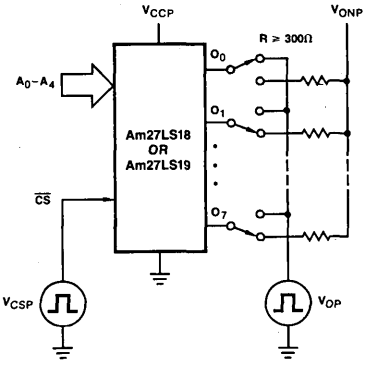
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-023

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-024

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27LS18 • Am27LS19 ADAPTERS AND CONFIGURATORS	715-1407-1	PA16-6 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

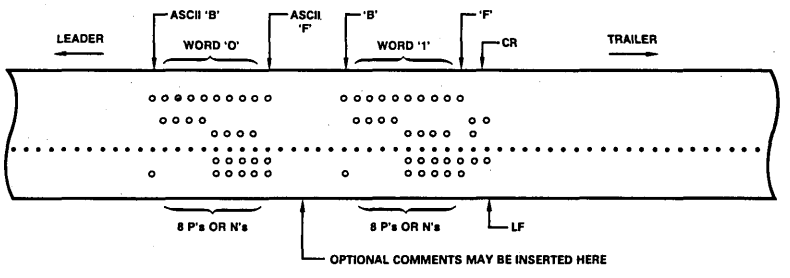
ØØØ	BPNPPNNNPF	WORD ZERO Ⓡ Ⓛ
	BPPPPPPNNF	COMMENT FIELD Ⓡ Ⓛ
Ø02	BNNNPPPPNF	ANY Ⓡ Ⓛ
	BNNNNNNNNF	TEXT Ⓡ Ⓛ
Ø04	BPNNNNNNPF	CAN Ⓡ Ⓛ
	BNPPNPPNNF	GO Ⓡ Ⓛ
Ø06	BPNNPPPNNF	HERE Ⓡ Ⓛ
⋮	⋮	⋮
Ø31	BNNNNPPPNF	END Ⓡ Ⓛ

Ⓡ = CARRIAGE RETURN
Ⓛ = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	L	L	L	L	H	H	H	L

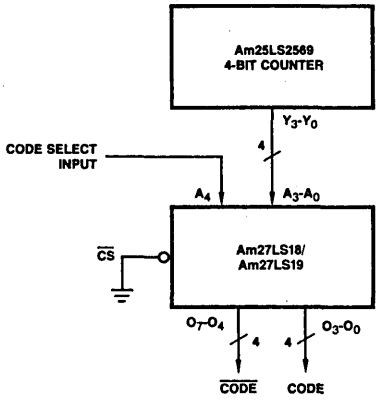
ASCII PAPER TAPE



BPM-025

APPLYING THE Am27LS18 AND Am27LS19

The Am27LS18 and Am27LS19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27LS18 or Am27LS19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.

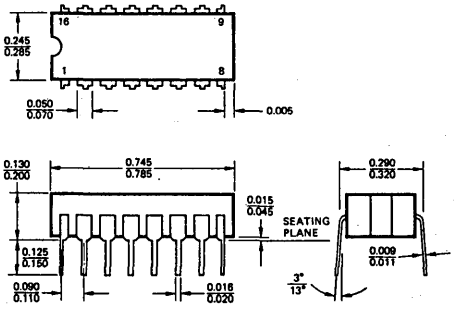


TRUTH TABLE

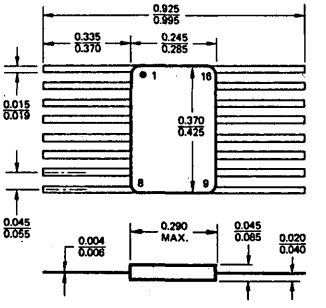
ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



Am27S18 • Am27S19

256-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 40ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

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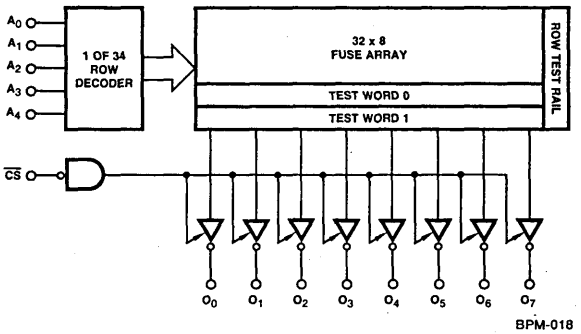
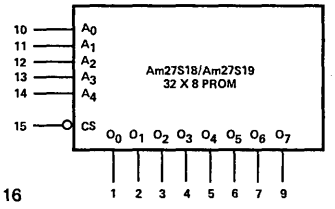


BPM-018

LOGIC SYMBOL



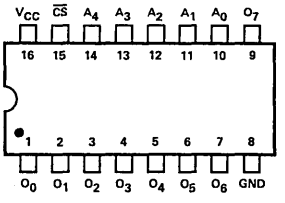
V_{CC} = Pin 16
GND = Pin 8

BPM-019

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S18DC
Hermetic DIP	−55°C to +125°C	AM27S18DM
Hermetic Flat Pak	−55°C to +125°C	AM27S18FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S19DC
Hermetic DIP	−55°C to +125°C	AM27S19DM
Hermetic Flat Pak	−55°C to +125°C	AM27S19FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-020

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S18XC, Am27S19XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S18XM, Am27S19XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27LS19 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27LS19 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

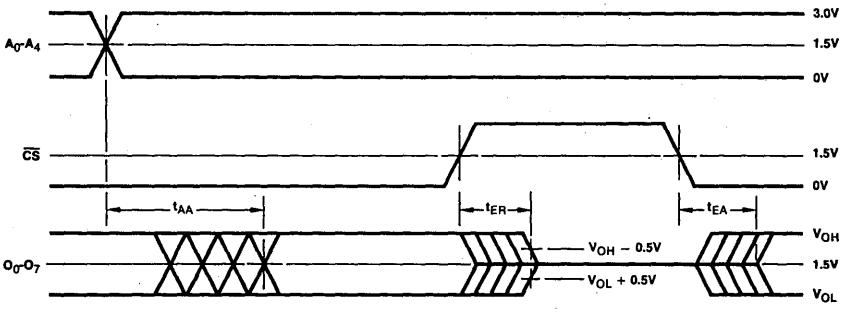
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	25	40	50	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

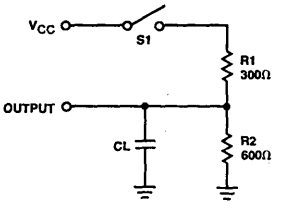
BPM-021

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-022

PROGRAMMING

The Am27S18 and Am27S19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

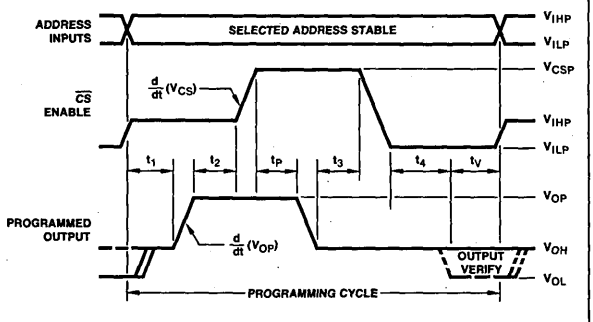
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

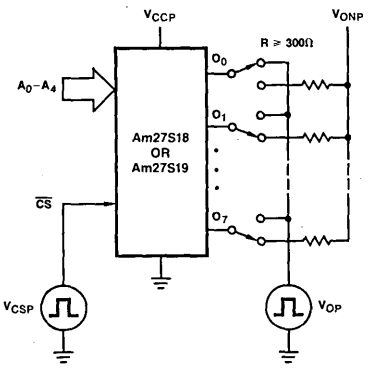
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-023

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-024

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S18 • Am27S19 ADAPTERS AND CONFIGURATOR	715-1407-1	PA16-6 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

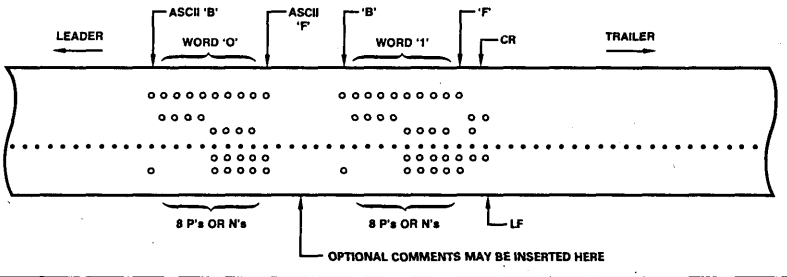
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
Ø02   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
Ø04   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
Ø06   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
Ø31   BNNNNPPPNF   END (R) (L)

(R) = CARRIAGE RETURN
(L) = LINE FEED
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
:	:	:	:	:	:	:	:	:	:	:	:	:
H	H	H	H	H	L	L	L	L	H	H	H	L

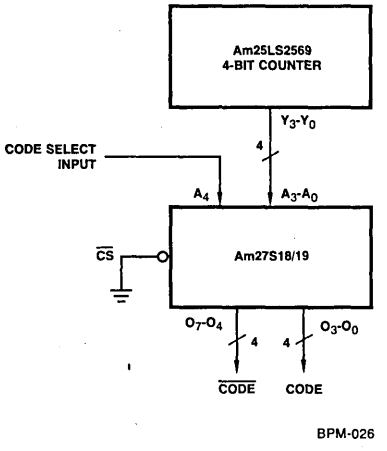
ASCII PAPER TAPE



BPM-025

APPLYING THE Am27S18 AND Am27S19

The Am27S18 and Am27S19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18 or Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



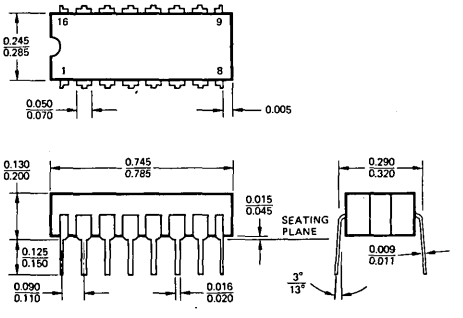
BPM-026

TRUTH TABLE

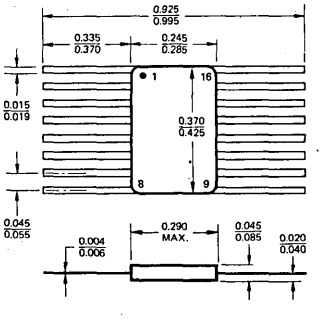
ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	0	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



Am27S20 • Am27S21

1024-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 45ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S20 and Am27S21 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

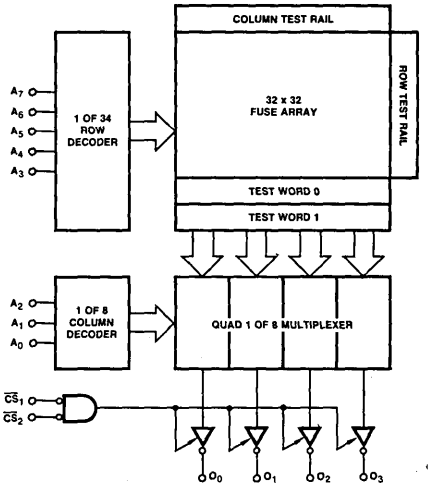
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S20DC
Hermetic DIP	−55°C to +125°C	AM27S20DM
Hermetic Flat Pak	−55°C to +125°C	AM27S20FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S21DC
Hermetic DIP	−55°C to +125°C	AM27S21DM
Hermetic Flat Pak	−55°C to +125°C	AM27S21FM

FUNCTIONAL DESCRIPTION

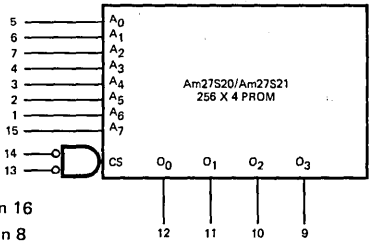
The Am27S20 and Am27S21 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector Am27S20 and three-state Am27S21 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_7 and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, at a logic LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-027

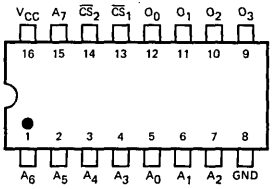
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-028

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-029

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S20XC, Am27S21XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S20XM, Am27S21XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

LECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

RELIMINARY DATA

arameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S21 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am27S21 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $V_{\overline{CS1}}$ = 2.4V	Am27S21 only	V_O = 4.5V			40	µA
				V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)				8		pF

lote 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

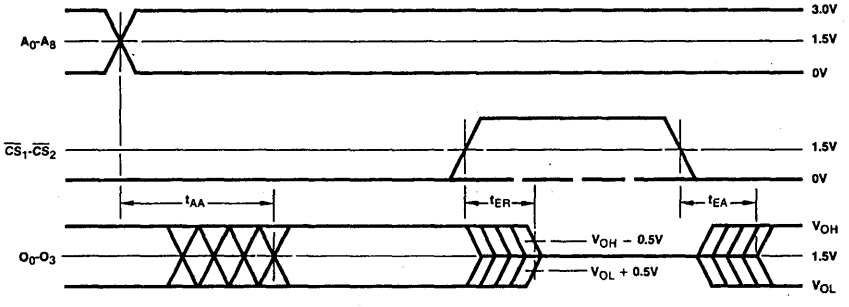
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	25	45	60	ns
t_{EA}	Enable Access Time		15	20	30	ns
t_{ER}	Enable Recovery Time		15	20	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

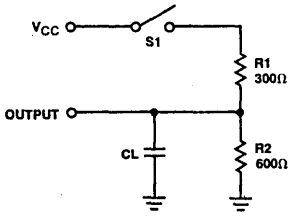
BPM-030

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-031

PROGRAMMING

The Am27S20 and Am27S21 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

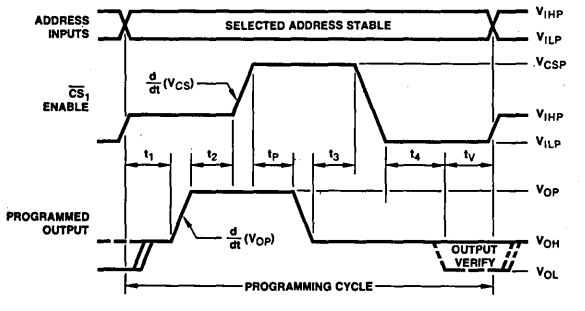
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

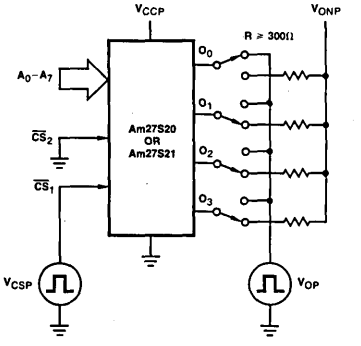
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-032

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-033

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S20 • Am27S21 ADAPTERS AND CONFIGURATOR	715-1408-1	PA16-5 and 256 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 256 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

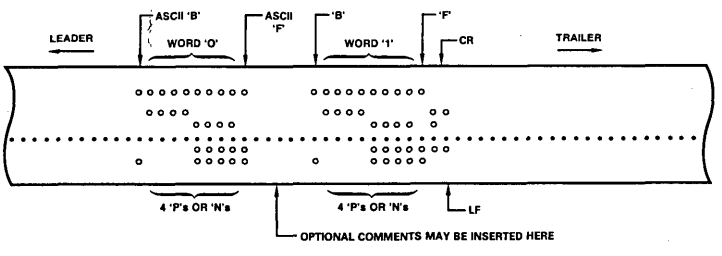
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 :     :::::    :
255   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}_1$ & $\overline{CS}_2$ = LOW)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	H	H	L	H	H	L	L
				⋮					⋮		
H	H	H	H	H	H	H	H	H	H	H	L

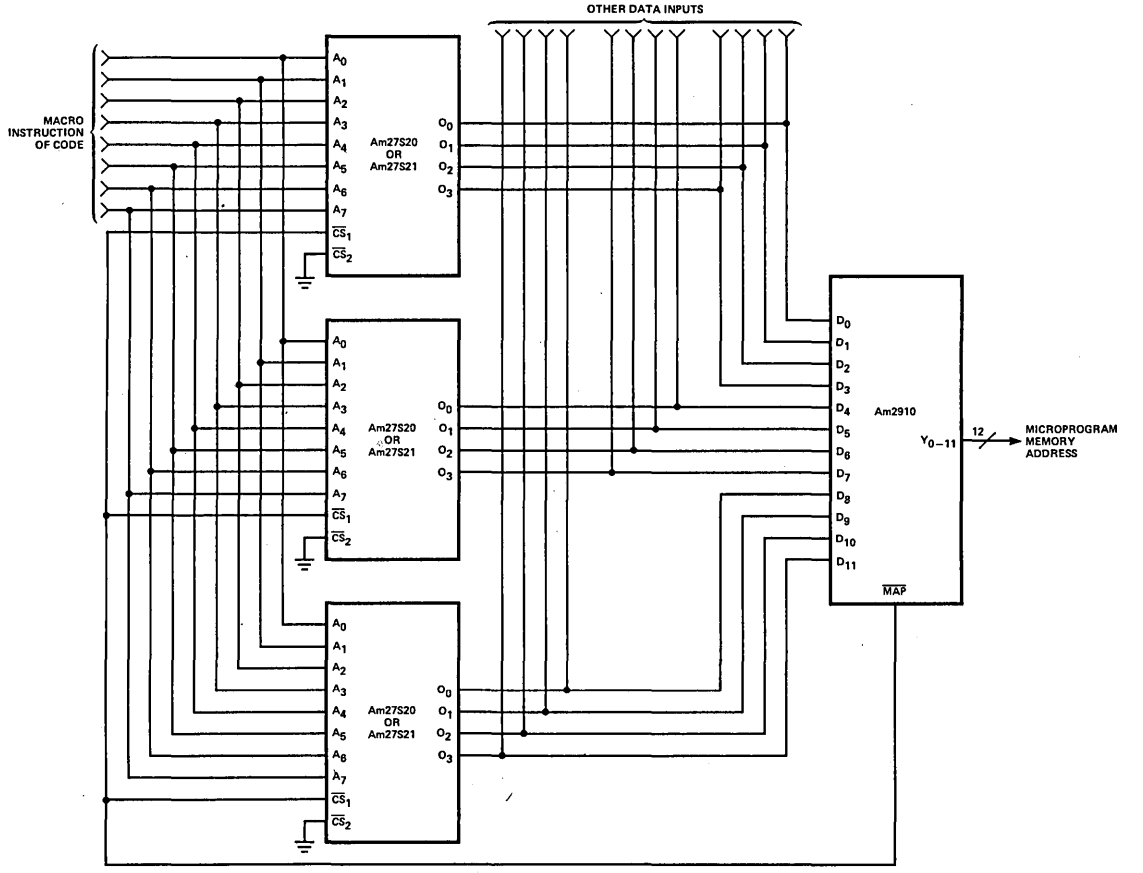
ASCII PAPER TAPE



BPM-034

APPLYING THE Am27S20/21

Typical application of the Am27S20/21 is shown below. The Am27S20/21's are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the A_{0-7} inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{CS}_1$ input of the Am27S20/21 such that when the $\overline{CS}_1$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20 or in the three-state mode in the case of the Am27S21. In both cases the $\overline{CS}_2$ input is grounded, thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.

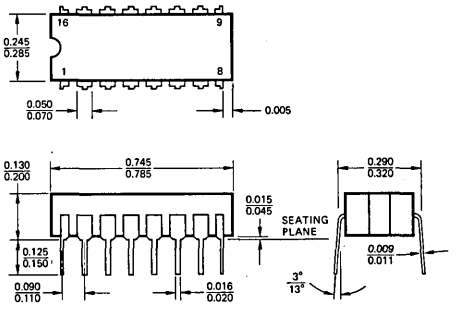


MICROPROGRAMMING INSTRUCTION MAPPING

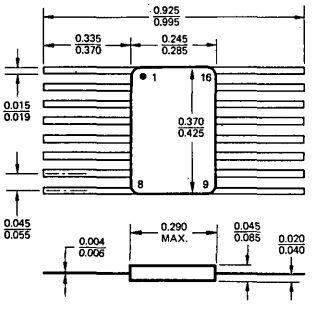
BPM-035

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



Am27S12 • Am27S13

2048-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 50ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S12 and Am27S13 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

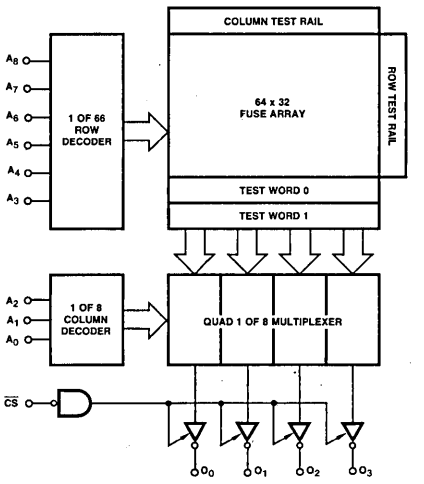
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0°C to +75°C	AM27S12DC
Hermetic DIP	−55°C to +125°C	AM27S12DM
Hermetic Flat Pak	−55°C to +125°C	AM27S12FM
	Three-State Outputs	
Hermetic DIP	0°C to +75°C	AM27S13DC
Hermetic DIP	−55°C to +125°C	AM27S13DM
Hermetic Flat Pak	−55°C to +125°C	AM27S13FM

FUNCTIONAL DESCRIPTION

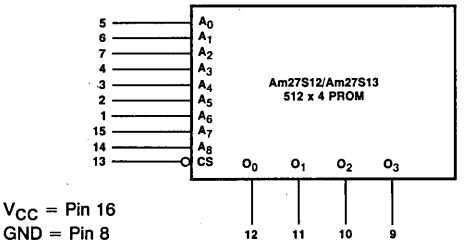
The Am27S12 and Am27S13 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 4 configuration, they are available in both open collector Am27S12 and three-state Am27S13 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-001

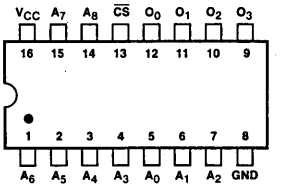
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-002

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-003

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S12XC, Am27S13XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S12XM, Am27S13XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S13 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S13 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		100	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $\overline{CS}$ = 2.4V; Am27S13 only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $\overline{CS}$ = 2.4V; Am27S13 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $\overline{CS}$ = 2.4V; Am27S13 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

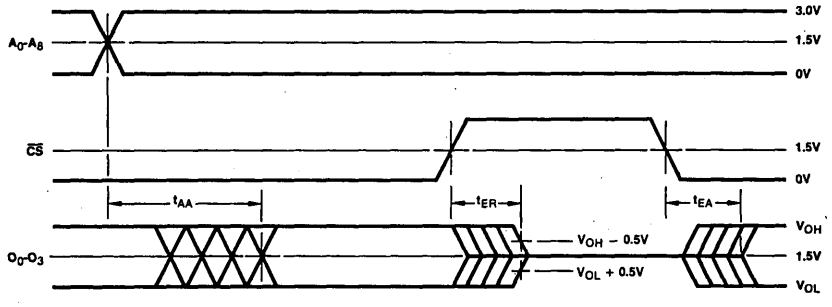
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	50	60	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



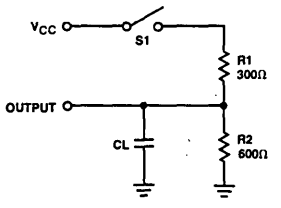
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

BPM-004

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY	▒▒▒	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▒▒▒	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L	⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
▒▒▒	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-005

PROGRAMMING

The Am27S12 and Am27S13 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycle. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

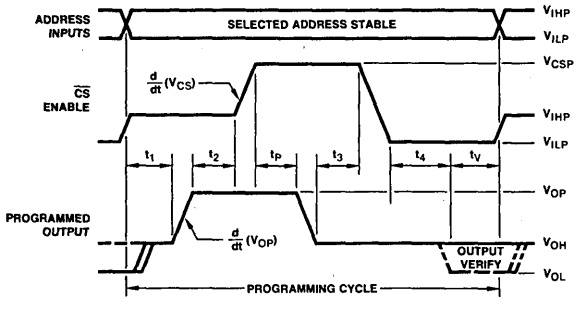
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

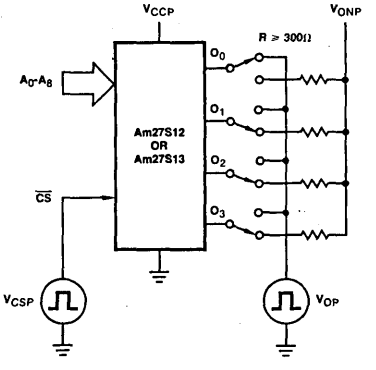
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-006

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-007

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S12 • Am27S13 ADAPTERS AND CONFIGURATOR	715-1408-2	PA16-5 and 512 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

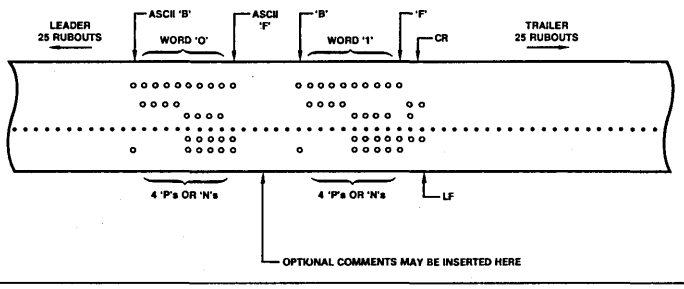
TYPICAL PAPER TAPE FORMAT

ØØØ	BNNNPF	WORD ZERO (R) (L)
	BPPNNF	COMMENT FIELD (R) (L)
Ø02	BPPPNF	ANY (R) (L)
	BNNNNF	TEXT (R) (L)
Ø04	BNNNPF	CAN (R) (L)
	BPPNNF	GO (R) (L)
Ø06	BPPNNF	HERE (R) (L)
⋮	⋮	⋮
511	BPPPNF	END (R) (L)

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	H	H	L	H	H	L	L
					⋮							
H	H	H	H	H	H	H	H	H	H	H	H	L

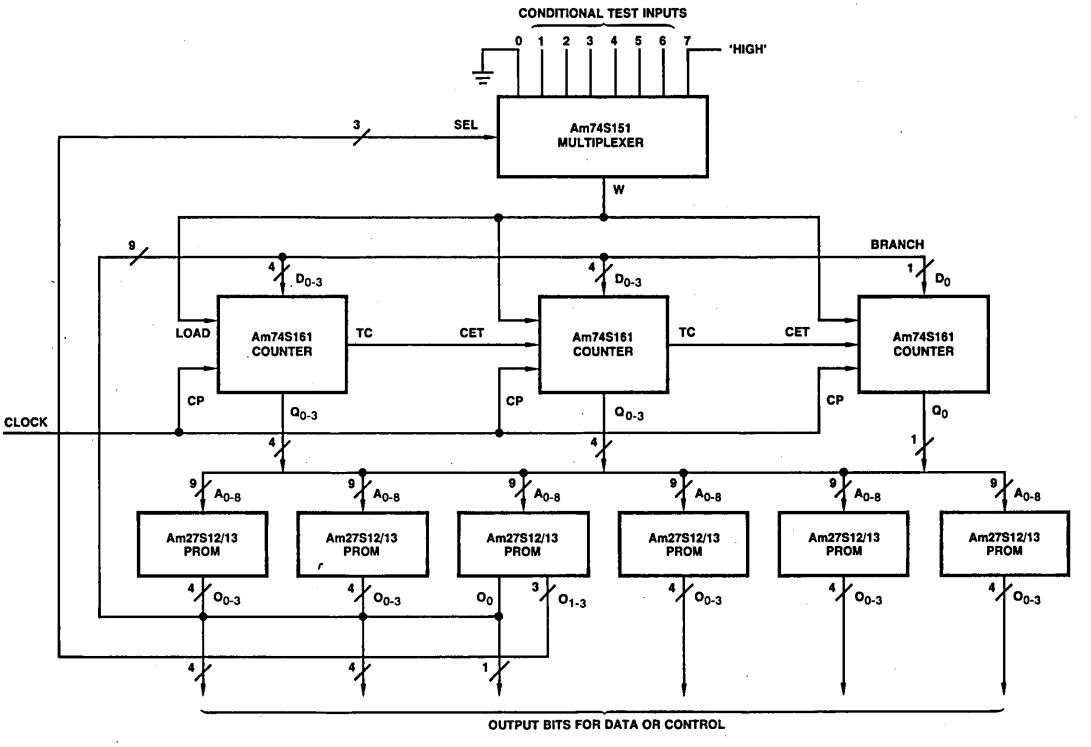
ASCII PAPER TAPE



BPM-008

APPLYING THE Am27S12 AND Am27S13

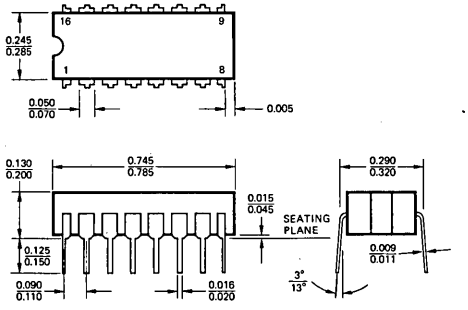
The Am27S12 and Am27S13 can be used with a high speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12 or Am27S13 PROMs.



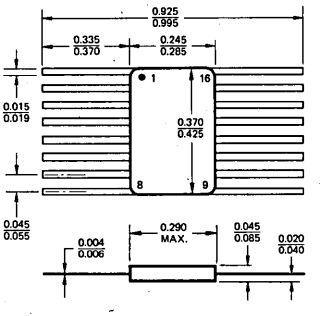
BPM-009

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package



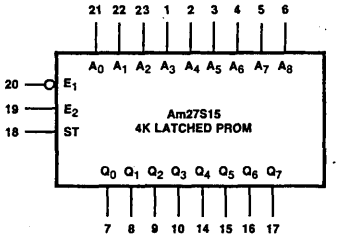
Am27S15

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On-chip data latches
- Latched true and complemented output enables for easy word expansion
- Predetermined OFF outputs on power-up
- Plug-in replacement for the 82S115
- Fast access time – 60ns commercial and 90ns military maximum
- Performance pretested with N^2 patterns
- Highly reliable, ultra-fast programming Platinum-Silicide fuses – High programming yield
- Low current PNP inputs
- High current three-state outputs
- Common Generic PROM Series characteristics and programming procedures

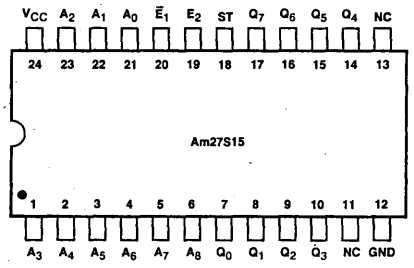
LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12
(Pins 11 and 13 open)

BPM-010

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
NC = No connection.

BPM-011

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	Am27S15DC
Hermetic DIP	−55°C to +125°C	Am27S15DM

FUNCTIONAL DESCRIPTION

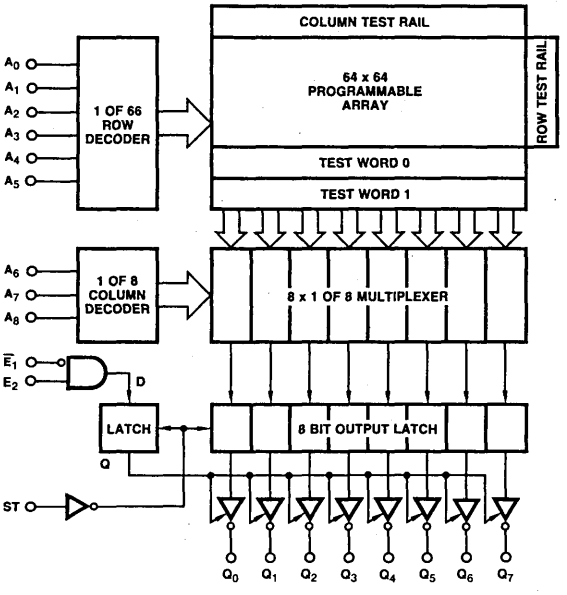
The Am27S15 is an electrically programmable Schottky read only memory incorporating on-chip data and enable latches. The device is organized as 512 words of 8 bits and features three-state outputs with full 16mA drive capability.

When in the transparent mode, with the strobe (ST) input HIGH, reading stored data is accomplished by enabling the chip ($\overline{E}_1$ LOW and E_2 HIGH) and applying the binary word address to the address inputs, A_0-A_8. In this mode, changes of the address inputs cause the outputs, Q_0-Q_7, to read a different stored word; changes of either enable input level disable the outputs, causing them to go to the high impedance state.

Dropping the strobe input to the LOW level places the device in the latched mode of operation. The output condition present (reading a word of stored data or disabled) when the strobe goes LOW remains at the outputs, regardless of further address or enable transitions, until a positive (LOW to HIGH) strobe transition occurs. With the strobe HIGH, Q_0-Q_7 again respond to the address and enable input conditions.

If the strobe is LOW (latched mode) when V_{CC} power is first applied, the outputs will be in the disabled state, eliminating the need for special "power-up" design precautions.

BLOCK DIAGRAM



BPM-012

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC}(max)
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration = 1sec)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S15XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S15XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}	COM'L	2.7			Volts
			MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	COM'L			0.85	Volts
			MIL			0.80	
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V	COM'L			−0.100	mA
			MIL			−0.150	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	COM'L	−20		−70	mA
			MIL	−15		−85	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX.	COM'L		125	175	mA
			MIL		125	185	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $\overline{VE_1}$ = 2.4V, VE_2 = 0.4V	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			12		

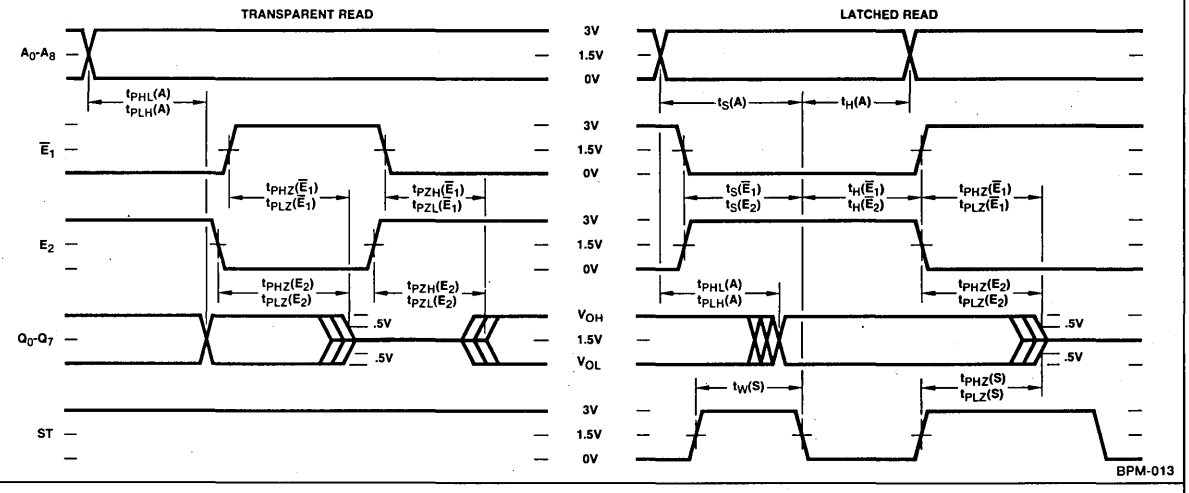
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

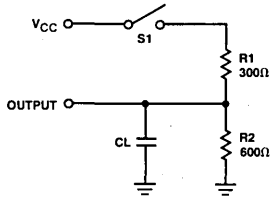
Parameter	Description	Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PHL}(A)$ $t_{PLH}(A)$	Transparent Mode Address to Output Access Time	C_L = 30pF S_1 Closed (See AC Test Load Below)	35		60		90	ns
$t_W(S)$	Strobe Pulse Width (HIGH)		10	30		40		ns
$t_S(A)$	Address to Strobe (LOW) Set-up Time		35	60		90		ns
$t_H(A)$	Address to Strobe (LOW) Hold Time		−10	0		5		ns
$t_S(E_1)$ $t_S(E_2)$	Enable to Strobe (LOW) Set-up Time			40		50		ns
$t_H(E_1)$ $t_H(E_2)$	Enable to Strobe (LOW) Hold Time		0	10		10		ns
$t_{PZH}(\overline{E}_1,E_2)$ $t_{PZL}(\overline{E}_1,E_2)$	Transparent Mode Enable to Output Enabled (HIGH or LOW) Time	C_L = 30pF S_1 Closed for t_{PZL}, & Open for t_{PZH}	20		40		50	ns
$t_{PHZ}(S)$ $t_{PLZ}(S)$	Strobe Delatch (HIGH) to Output Disabled (OFF or HIGH impedance) Time	C_L = 5pF (Note 2) S_1 closed for t_{PLZ} & Open for t_{PHZ}			35		45	ns
$t_{PHZ}(\overline{E}_1,E_2)$ $t_{PLZ}(\overline{E}_1,E_2)$	Transparent Mode Enable to Output Disabled (OFF or high impedance) Time		20		40		50	ns

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input rise and fall times (10% to 90%) of 5ns or less.

SWITCHING WAVEFORMS

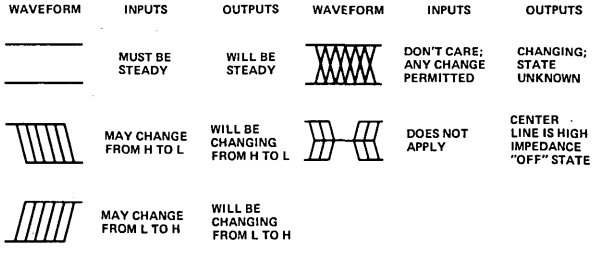


AC TEST LOAD



BPM-014

KEY TO TIMING DIAGRAM



PROGRAMMING

The Am27S15 is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

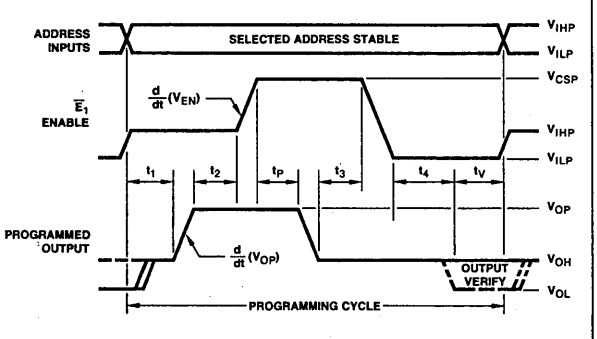
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	v/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

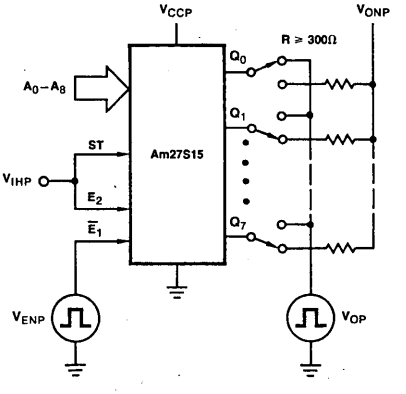
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-015

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-016

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S15 ADAPTERS AND CONFIGURATOR	715-1411-1	PA24-14 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

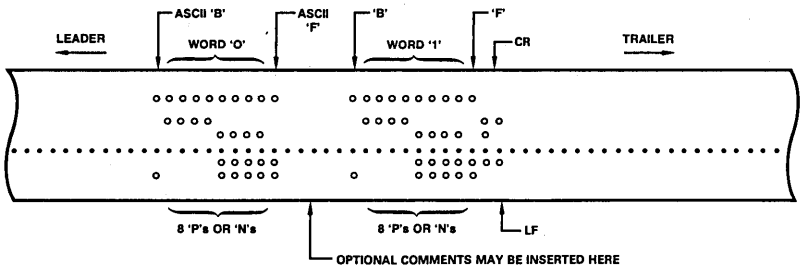
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :         :            :
511   BNNNNPPPNF   END (R) (L)
(R) = CARRIAGE RETURN
(L) = LINE FEED
```

RESULTING DEVICE TRUTH TABLE ($\overline{E}_1$ AND $\overline{E}_2$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-017

GENERIC SERIES CHARACTERISTICS

The Am27S15 is a member of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

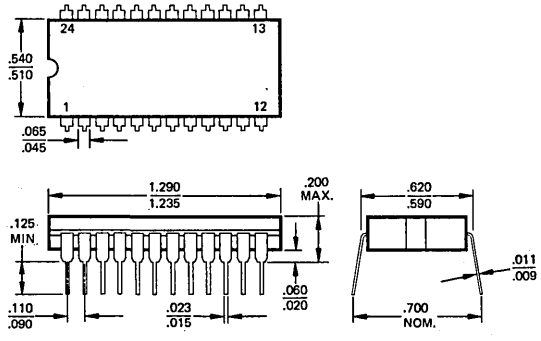
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

PHYSICAL DIMENSIONS
Dual-In-Line

24-Pin Hermetic



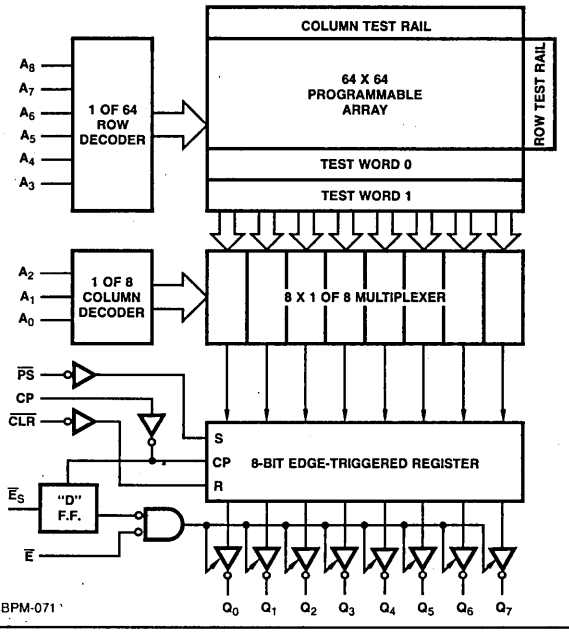
Am27S25

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

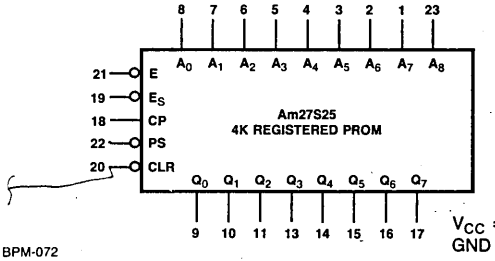
- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common asynchronous $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- Space saving 24-pin package with 300 mil lateral centers
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current three-state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



BPM-071

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

BPM-072

FUNCTIONAL DESCRIPTION

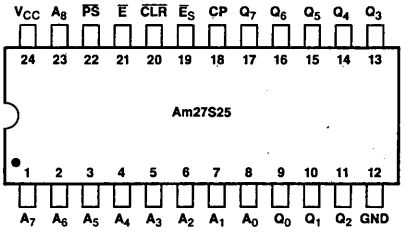
The Am27S25 is an electrically programmable Schottky TTL read only memory incorporating true D-type, master-slave data registers on chip. This device features the versatile 512 word by 8 bit organization and is available in the three-state Am27S25 output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S25 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered asynchronous $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs. These functions are common to all registers and are useful during power up timeout sequences. With outputs enabled the $\overline{\text{PS}}$ input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the $\overline{\text{CLR}}$ input is LOW, the internal flip-flops of the data register are reset and, a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

CONNECTION DIAGRAM – Top View



BPM-073

Note: Pin 1 is marked for orientation.

GENERIC SERIES CHARACTERISTICS

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Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM27S25XC	T_A = 0 to 75°C	V_{CC} = 5.0V ±5%
MIL	AM27S25XM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.			130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $\overline{VE}$ = 2.4V	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			12		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

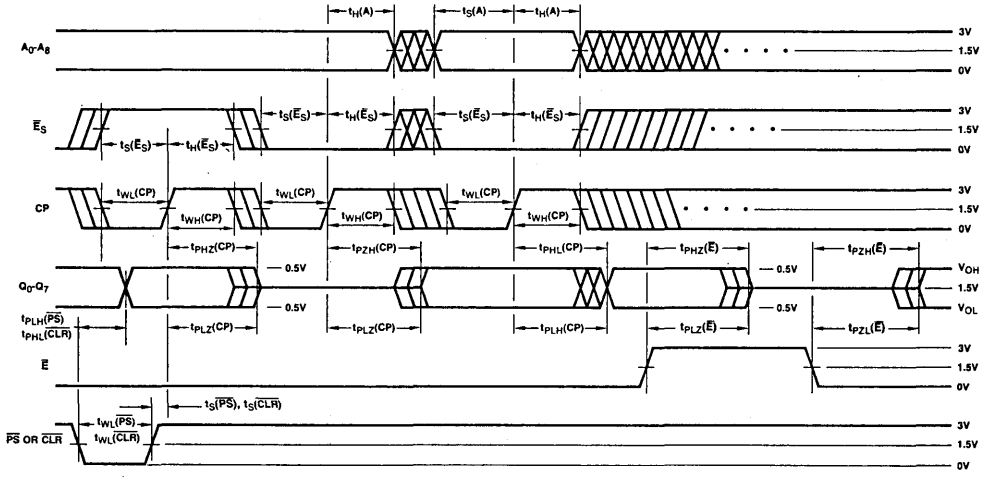
T_A = 25°C, V_{CC} = 5.0V

Parameter	Description	Test Conditions	Typ	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF, S_1 closed (See AC Test Load below)	35		50		60	ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0		0		ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		25		30	ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10					ns
$t_S(\overline{E_S})$	$\overline{E_S}$ to CP (HIGH) Setup Time		10					ns
$t_H(\overline{E_S})$	$\overline{E_S}$ to CP (HIGH) Hold Time		−10					ns
$t_{PLH}(\overline{PS})$	Delay from $\overline{PS}$ (LOW) to Output (HIGH)		17					ns
$t_{PHL}(\overline{CLR})$	Delay from $\overline{CLR}$ (LOW) to Output (LOW)		17					ns
$t_{WL}(\overline{PS})$	$\overline{PRESET}$ Pulse Width (LOW)		10					ns
$t_{WL}(\overline{CLR})$	$\overline{CLEAR}$ Pulse Width (LOW)		10					ns
$t_S(\overline{PS})$	$\overline{PS}$ Recovery (Inactive) to CLock (HIGH)		12					ns
$t_S(\overline{CLR})$	$\overline{CLR}$ Recovery (Inactive) to Clock (HIGH)		12					ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW)	C_L = 30pF, S_1 is closed for t_{PZL} and open for t_{PZH}	22					ns
$t_{PZL}(\overline{E})$ $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW)		22					ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance)	C_L = 5pF (Note 1), S_1 closed for t_{PLZ} and open for t_{PHZ}	22					ns
$t_{PLZ}(\overline{E})$ $t_{PHZ}(\overline{E})$	Delay from $\overline{E}$ (HIGH to Inactive Output (OFF or High Impedance)		22					ns

PRELIMINARY

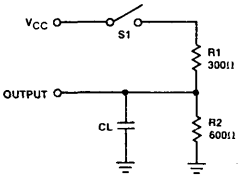
Notes: 1. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
2. Tests are performed with input 10 to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS



BPM-074

AC TEST LOAD



BPM-075

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING

The Am27S25 is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

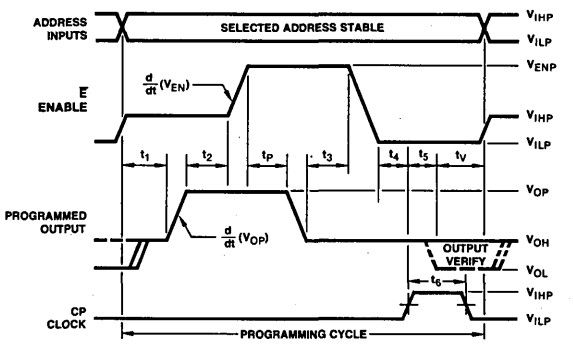
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

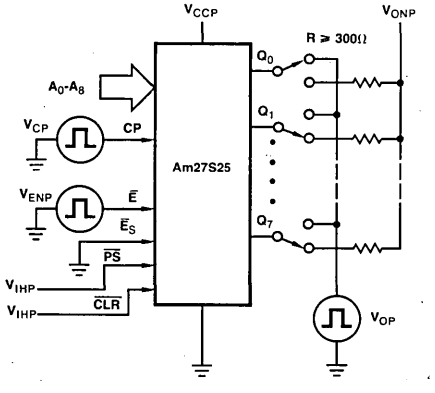
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.
5. $\overline{PS}$ and $\overline{CLR}$ must be connected to V_{IHP} during programming.

PROGRAMMING WAVEFORMS



BPM-076

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-077

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S25 ADAPTERS AND CONFIGURATOR	715-1617	PA24-16 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

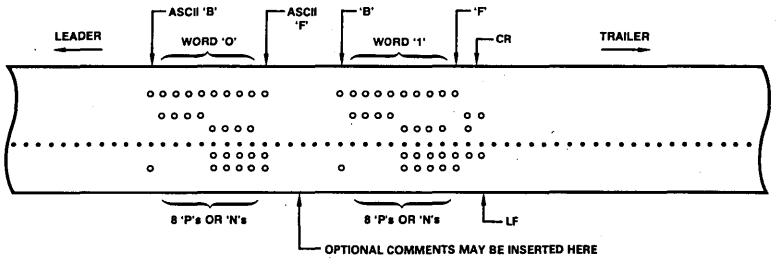
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE
($\overline{E}$ AND $\overline{E}_S$ LOW, $\overline{PS}$ AND $\overline{CLR}$ HIGH)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-078

APPLYING THE Am27S25 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am27S25 registered PROM, the design engineer can upgrade the performance of existing systems or implement new systems taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familiar to many design engineers. This technique is called microprogramming.

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

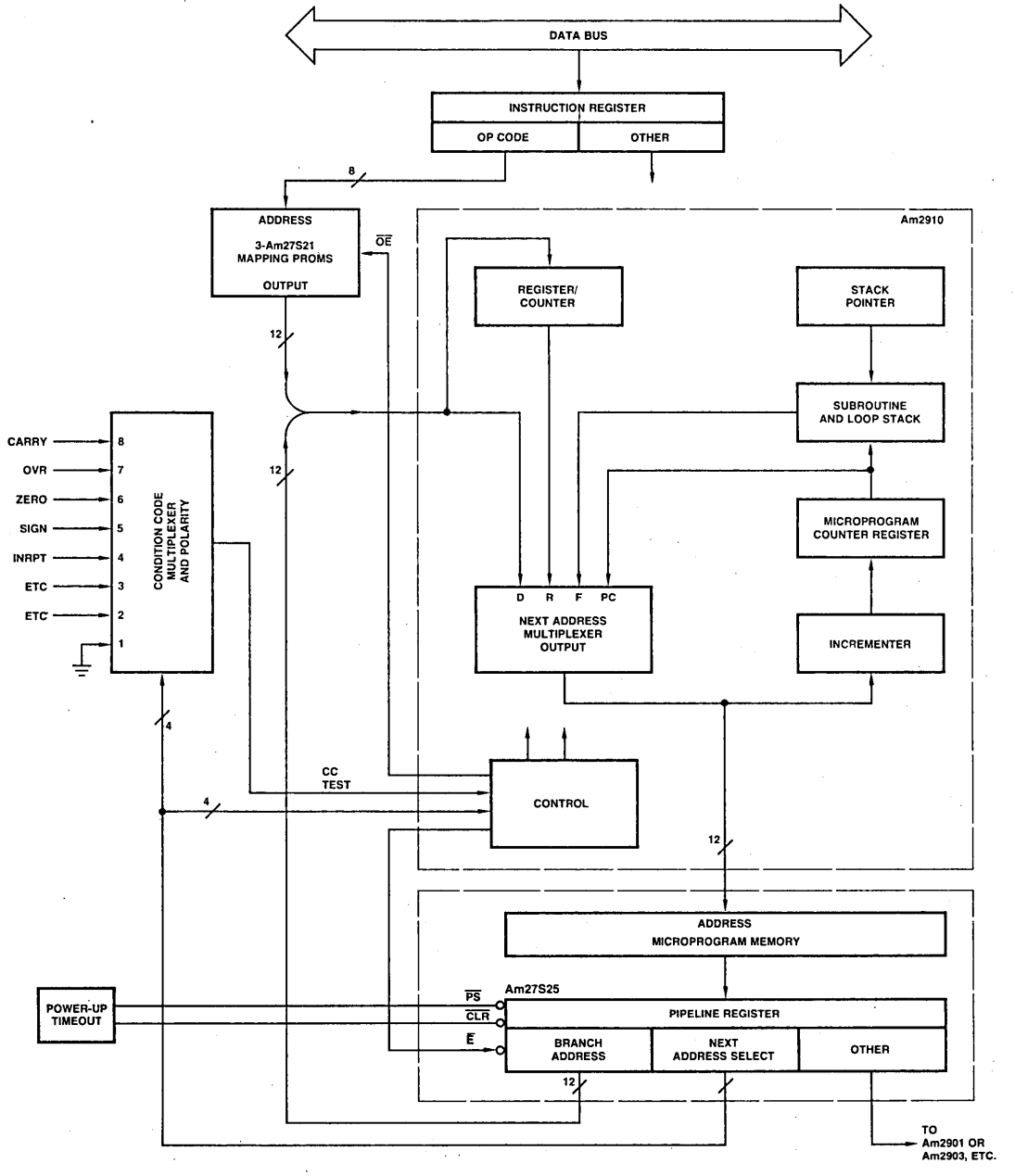


Figure 1. A Typical Computer Control Unit Using the Am27S25.

BPM-079

APPLYING THE Am27S25 IN BIPOLAR MICROCOMPUTERS (Cont.)

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROMs for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction.

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am27S25 registered PROMs. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and file (F). The starting address decoder (mapping PROM) output and the Am27S25's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcycle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am27S25 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am27S25 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The Am27S25 contains a $\overline{\text{PRESET}}$ ($\overline{\text{PS}}$) and a $\overline{\text{CLEAR}}$ ($\overline{\text{CLR}}$) function that is useful for power-up operations and other initialization functions. These signals can also be used to provide "trap" jumps to the all zeros or ones addresses in microprogram memory.

The expansion scheme for increasing the depth of Am27S25 is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am27S25 registered PROMs is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

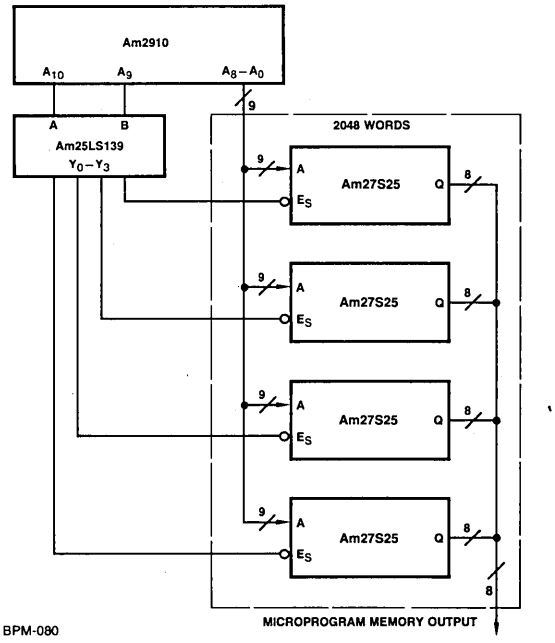


Figure 2. Word Expansion Scheme for the Am27S25.

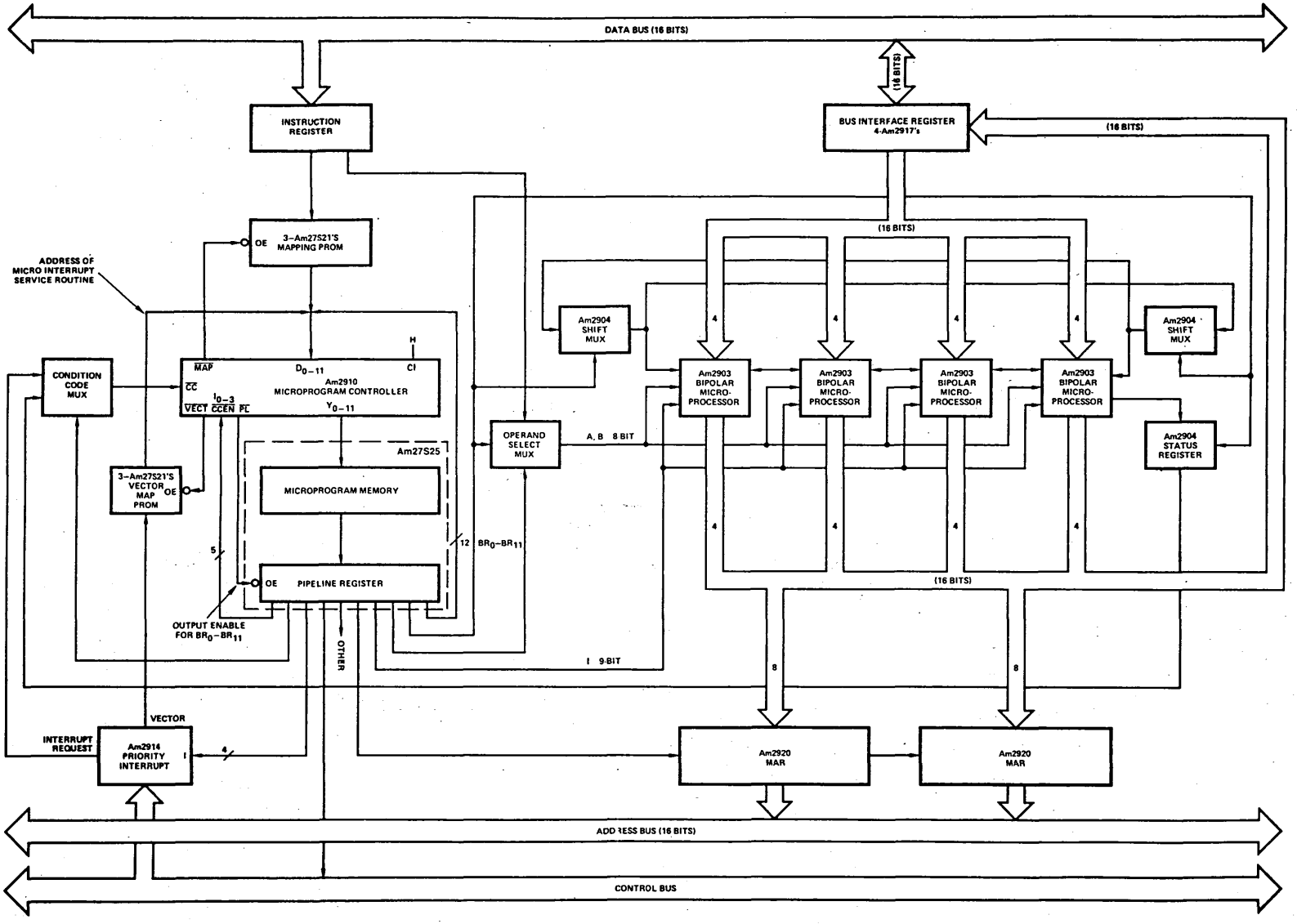
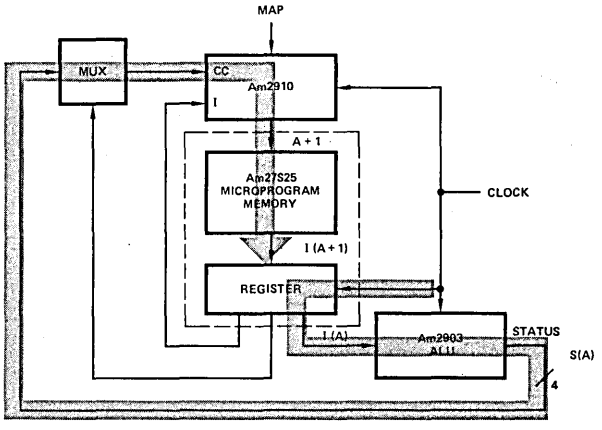


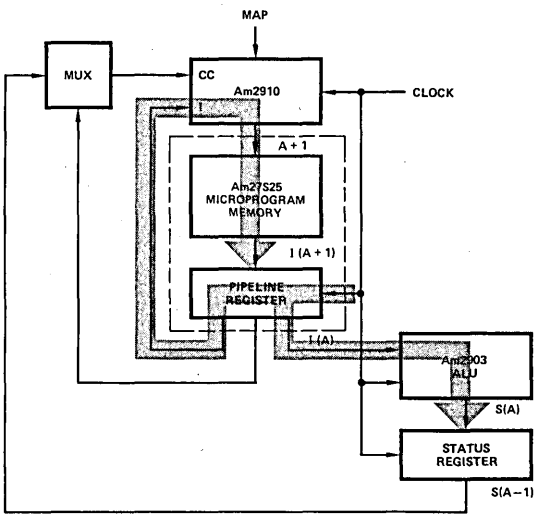
Figure 3. Typical Bipolar Microcomputer Using the Am27S25.

USING THE Am27S25 IN A PIPELINED ARCHITECTURE



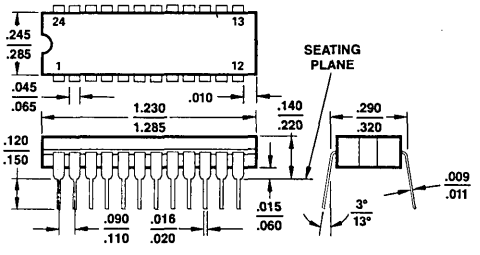
BPM-082

A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.



One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am27S25 reduces the parts count of the microprogram memory/pipeline by a factor of two.

PHYSICAL DIMENSIONS
Dual In-Line
24-Pin Slim Cerdip



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Three-State Outputs	
Hermetic DIP	0 to 75°C	AM27S25DC
Hermetic DIP	−55 to +125°C	AM27S25DM

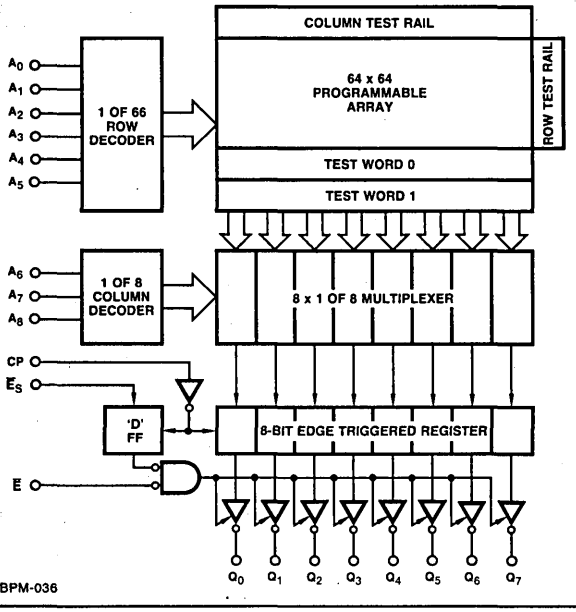
Am27S26 • Am27S27

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Space saving 22 pin package
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



BPM-036

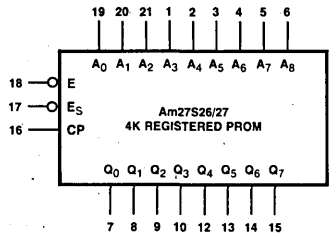
FUNCTIONAL DESCRIPTION

The Am27S26 and Am27S27 are electrically programmable Schottky TTL read only memories incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512 word by 8 bit organization and are available in both the open collector Am27S26 and three-state Am27S27 output versions. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed system and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S26 and Am27S27 also offer maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

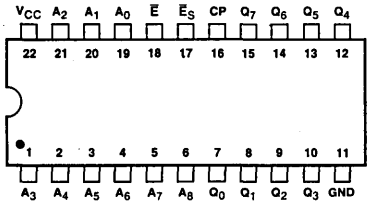
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

BPM-037

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-038

GENERIC SERIES CHARACTERISTICS

The Am27S26 and Am27S27 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 11) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM27S26XC, AM27S27XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	AM27S26XM, AM27S27XM	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S27 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}		0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S27 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $\overline{VE}$ = 2.4V; Am27S27 Only; V_O = 4.5V			100	μA
		V_{CC} = MAX., $\overline{VE}$ = 2.4V; Am27S27 Only; V_O = 2.4V			40	μA
		V_{CC} = MAX., $\overline{VE}$ = 2.4V; Am27S27 Only; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)		12		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

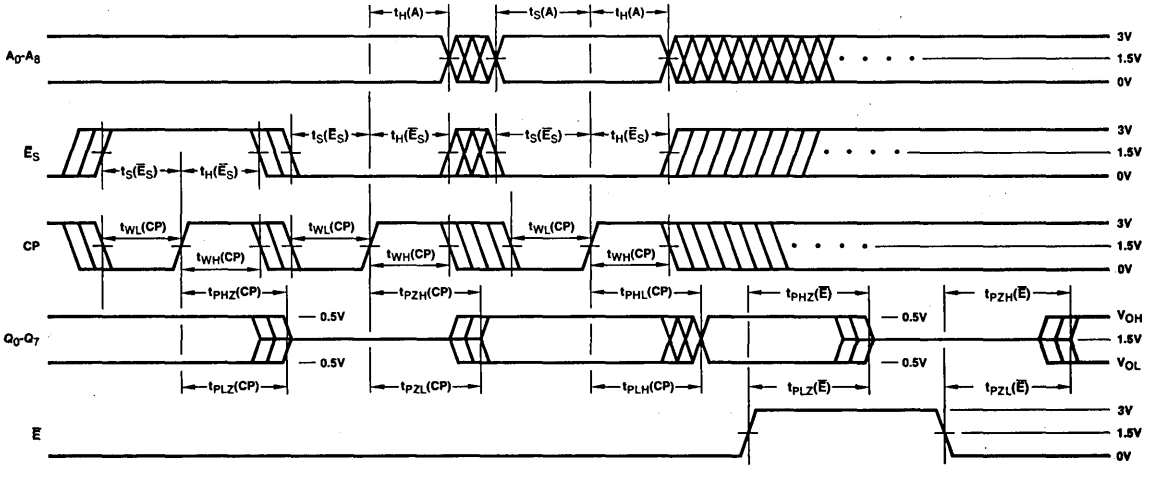
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

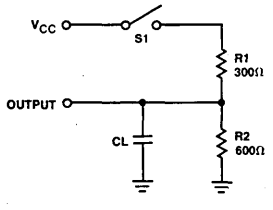
Parameter	Description	Test Conditions	Typ 5V 25°C	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF, S_1 closed. (See AC Test Load below)	40	55		65		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0		0		ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		27		30	ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10	30		40		ns
$t_S(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Setup Time		10	25		30		ns
$t_H(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Hold Time		−10	0		0		ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 1)	C_L = 30pF, S_1 closed for t_{PZL} and open for t_{PZH}	15		35		45	ns
$t_{PZL}(\overline{E})$ $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (Note 1)		15		40		45	ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or High Impedance) (Note 1)	C_L = 5pF (Note 2), S_1 closed for t_{PLZ} and open for t_{PHZ}	15		35		45	ns
$t_{PLZ}(\overline{E})$ $t_{PHZ}(\overline{E})$	Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance) (Note 1)		10		30		40	ns

Notes:
1. t_{PHZ} and t_{PZH} apply to the three-state Am27S27 only.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS

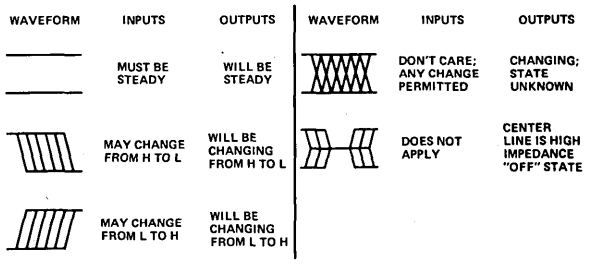


AC TEST LOAD



BPM-040

KEY TO TIMING DIAGRAM



PROGRAMMING

The Am27S26 and Am27S27 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

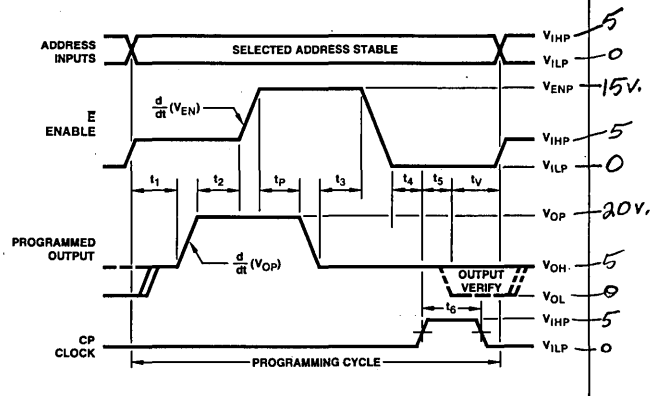
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

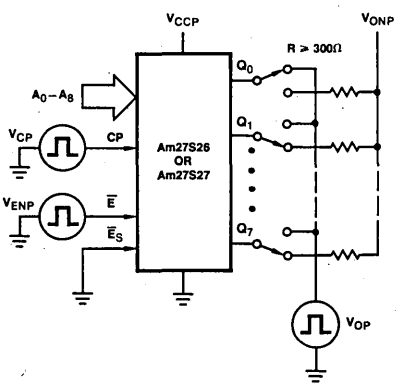
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-041

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-042

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S26 • Am27S27 ADAPTERS AND CONFIGURATOR	715-1412-2	PA22-4 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

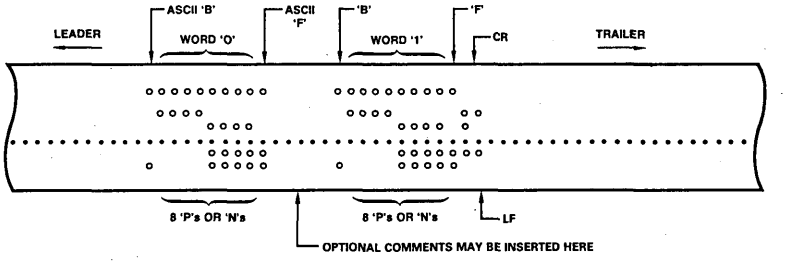
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXI (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    :::::::::::    :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{E}$ AND $\overline{E}_S$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-043

APPLYING THE Am27S26 AND Am27S27 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am27S26/27 registered PROM, the design engineer can upgrade the performance of existing systems or implement new systems taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familiar to many design engineers. This technique is called microprogramming.

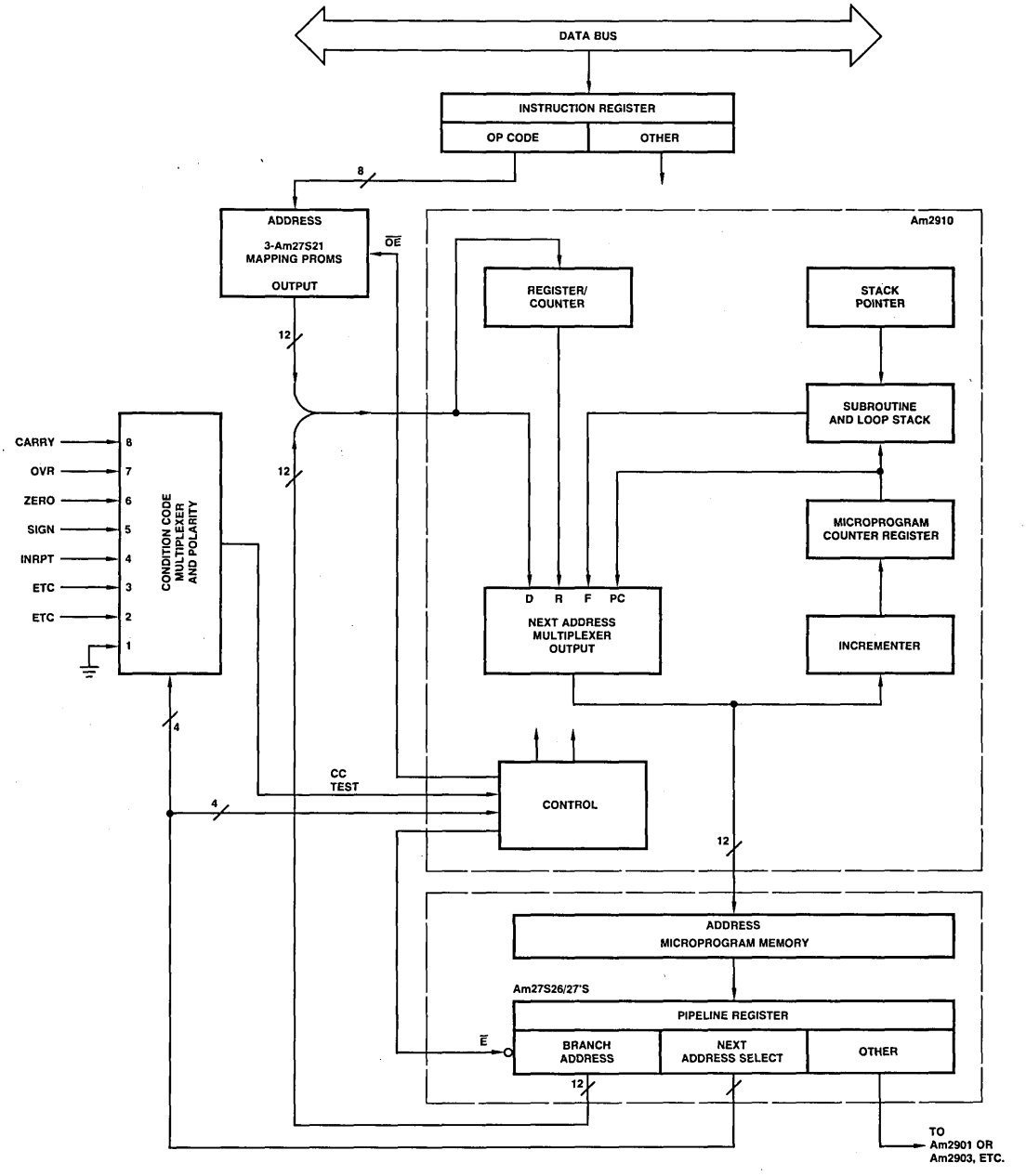


Fig. 1. A Typical Computer Control Unit using the Am27S26/27. BPM-044

APPLYING THE Am27S26 and Am27S27 IN BIPOLAR MICROCOMPUTERS (Cont.)

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROMs for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am27S26/27 registered PROM's. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and the file (F). The starting address decoder (mapping PROM) output and the Am27S26/27's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcycle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am27S26/27 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am27S26/27 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The expansion scheme for increasing the depth of Am27S26/27's is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am27S26/27 registered PROM's is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

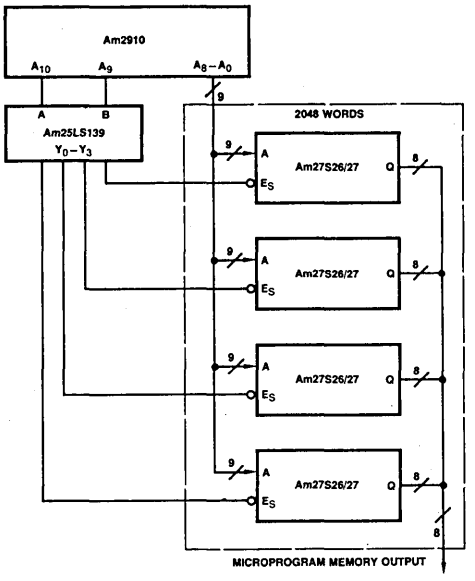


Fig. 2. Word Expansion Scheme for the Am27S26 and Am27S27.

BPM-045

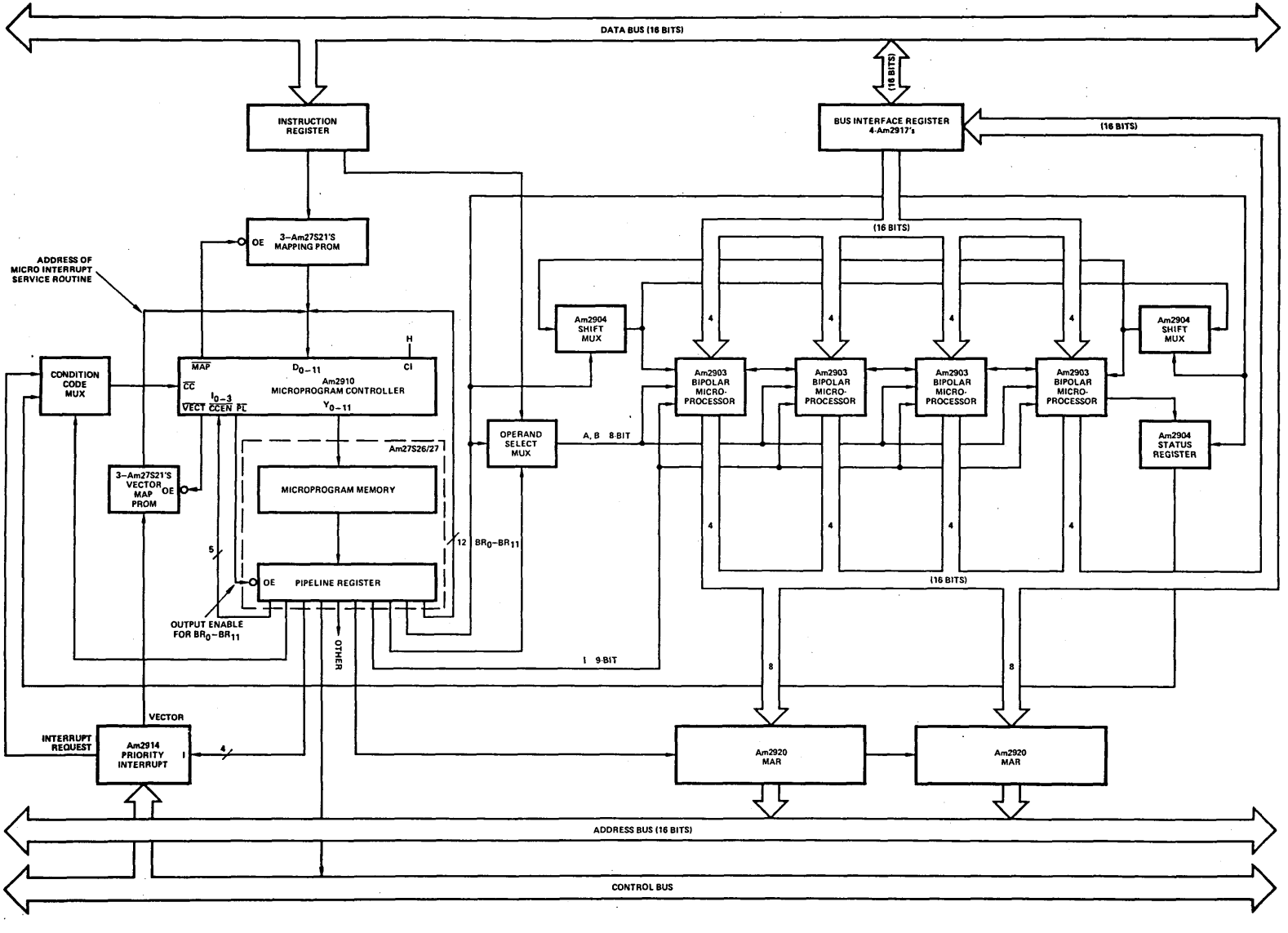
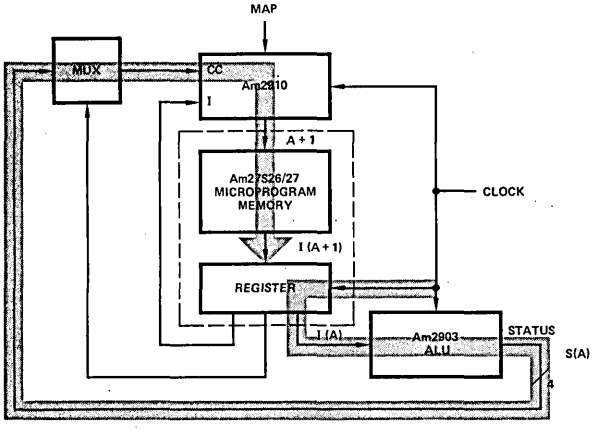


Fig. 3. Typical Bipolar Microcomputer using the Am27S26/27.

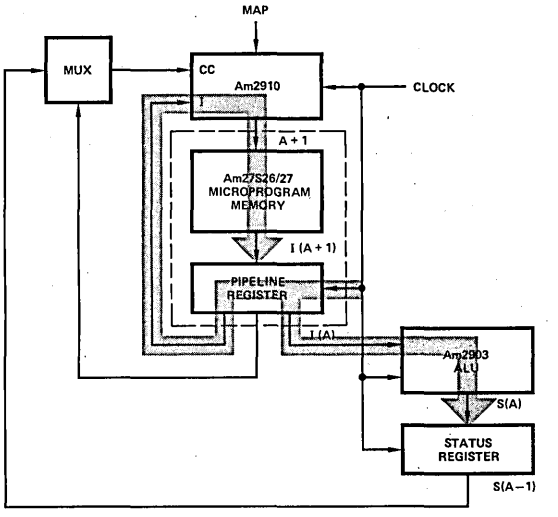
BPM-046

USING THE Am27S26/27 IN A PIPELINED ARCHITECTURE



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

BPM-047



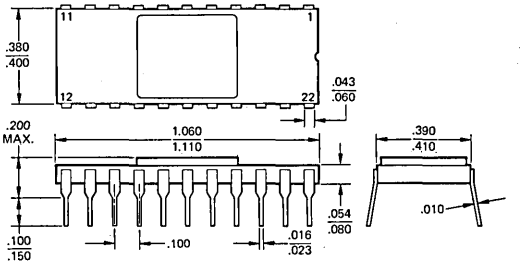
One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am27S26/27 reduces the parts count of the microprogram memory/pipeline by a factor of two.

BPM-048

PHYSICAL DIMENSIONS

Dual In-Line

22-Pin Hermetic



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S26DC
Hermetic DIP	−55°C to +125°C	AM27S26DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S27DC
Hermetic DIP	−55°C to +125°C	AM27S27DM

Am27S28 • Am27S29

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S28 and Am27S29 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test rows are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

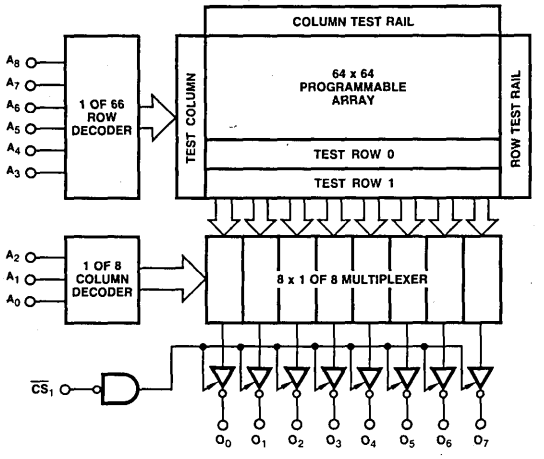
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S28DC
Hermetic DIP	−55°C to +125°C	AM27S28DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S29DC
Hermetic DIP	−55°C to +125°C	AM27S29DM

FUNCTIONAL DESCRIPTION

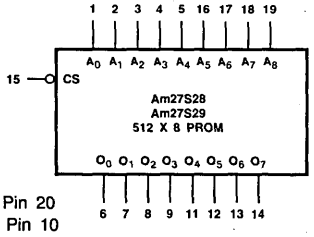
The Am27S28 and Am27S29 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S28 and three-state Am27S29 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-083

LOGIC SYMBOL

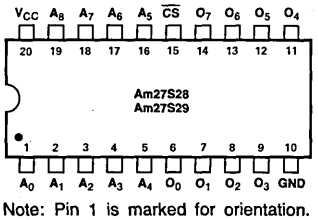


V_{CC} = Pin 20
GND = Pin 10

BPM-084

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

BPM-085

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S28XC, Am27S29XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S28XM, Am27S29XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S29 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S29 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		105	160	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S29 only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S29 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27S29 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

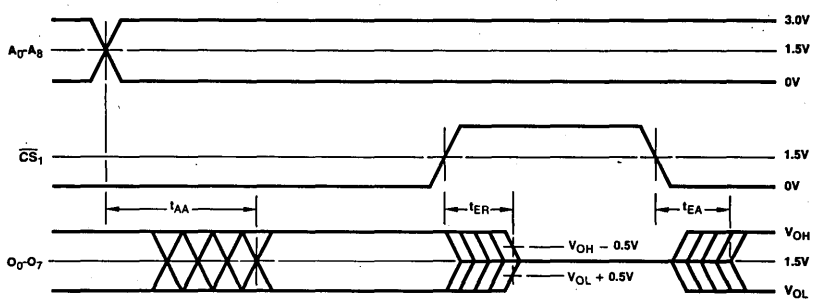
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	35	55	70	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



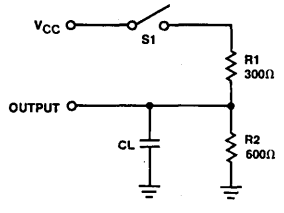
Note: Level on output while CS is HIGH is determined externally.

BPM-086

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD

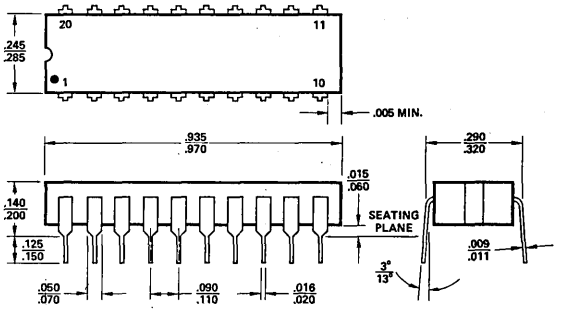


BPM-087

PHYSICAL DIMENSIONS

Dual-In-Line

20-Pin Hermetic



PROGRAMMING

The Am27S28 and Am27S29 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

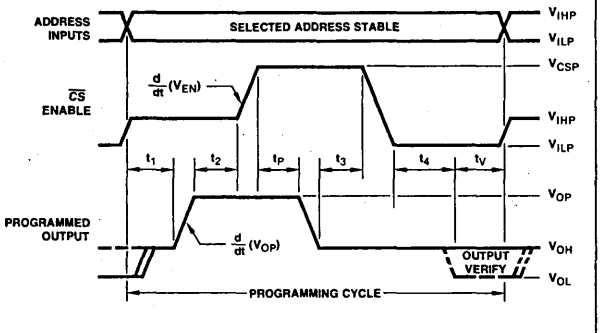
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	v/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

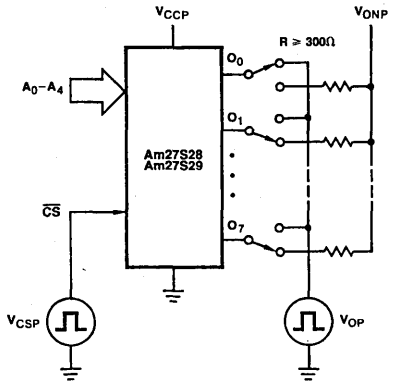
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-088

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-089

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S28 • Am27S29 ADAPTERS AND CONFIGURATOR	715-1413	PA20-4 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

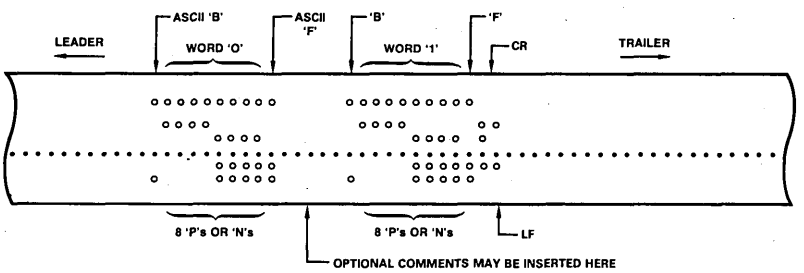
```
ØØØ   BPNPPNNNFF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNFF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-017

Am27S30 • Am27S31

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55 ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S30 and Am27S31 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test rows are preprogrammed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

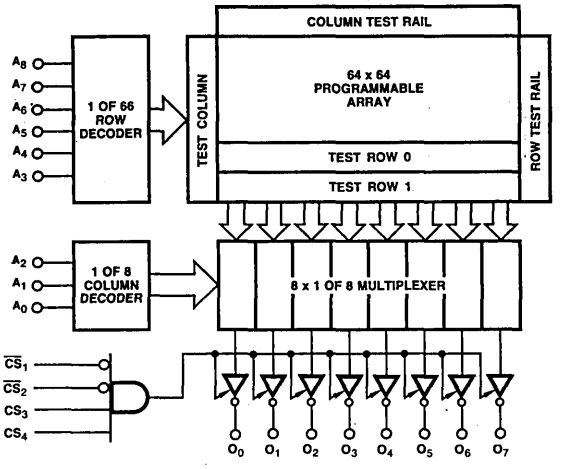
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S30DC
Hermetic DIP	−55°C to +125°C	Am27S30DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S31DC
Hermetic DIP	−55°C to +125°C	AM27S31DM

FUNCTIONAL DESCRIPTION

The Am27S30 and Am27S31 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S30 and three-state Am27S31 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_8 and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and CS_3 and CS_4 HIGH. All other valid input conditions on $\overline{CS}_1$, $\overline{CS}_2$, CS_3 and CS_4 place O_0-O_7 into the OFF or high impedance state.

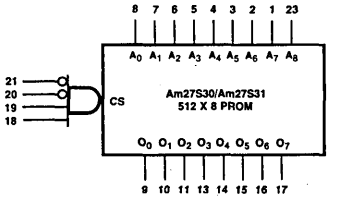
BLOCK DIAGRAM



BPM-114

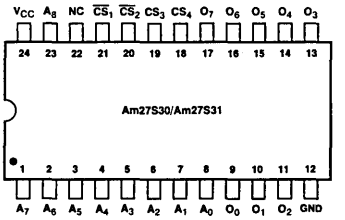
LOGIC SYMBOL

V_{CC} = Pin 24
GND = Pin 12
(Pin 22 Open)



BPM-115

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-116

MAXIMUM RATINGS (Above which the useful life may be impaired)	
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S30XC, Am27S31XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S30XM, Am27S31XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S31 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S31 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		115	175	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS1}}$ = 2.4V; Am27S31 only; V_O = 4.5V			40	µA
		V_{CC} = MAX, $V_{\overline{CS1}}$ = 2.4V; Am27S31 only; V_O = 2.4V			40	µA
		V_{CC} = MAX, $V_{\overline{CS1}}$ = 2.4V; Am27S31 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

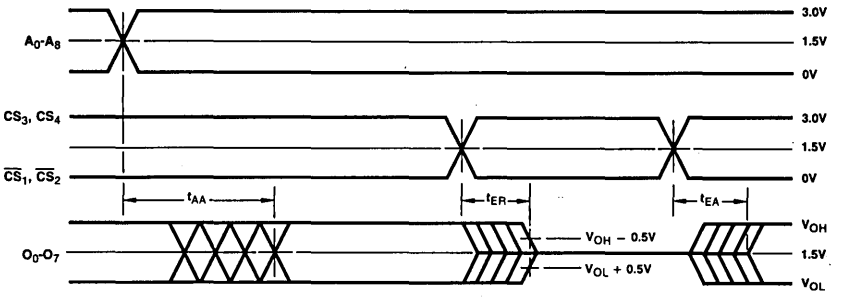
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	35	55	70	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



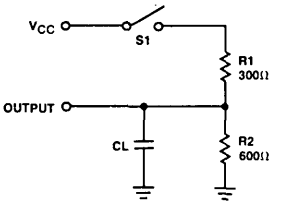
Note: Level on output while chip is disabled is determined externally.

BPM-117

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY	▒▒▒	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▒▒▒	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L	⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
▒▒▒	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



BPM-118

PROGRAMMING

The Am27S30 and Am27S31 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

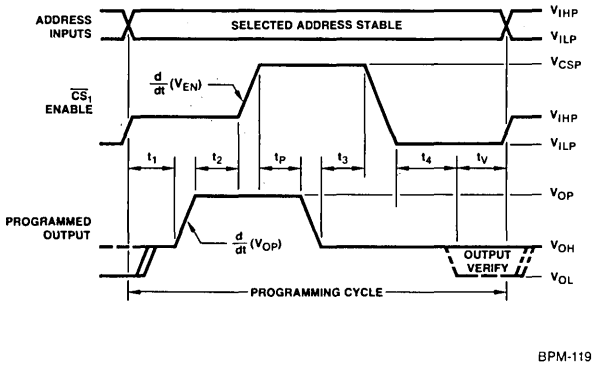
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	v/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

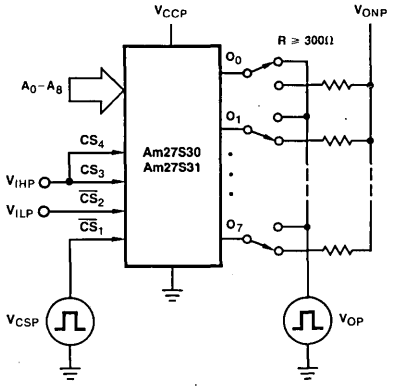
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-119

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-120

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S30 • Am27S31 ADAPTERS AND CONFIGURATOR	715-1545	PA24-13 and 512 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

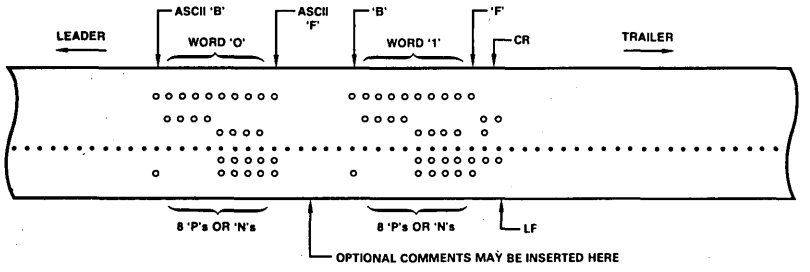
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 .          .          .
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE
($\overline{CS_1}$ AND $\overline{CS_2}$ LOW, CS_3 AND CS_4 HIGH)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
⋮				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

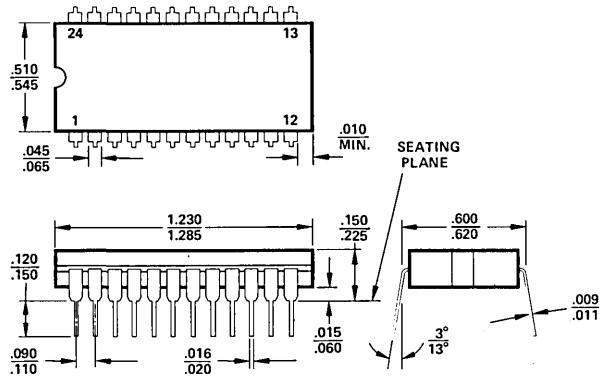
ASCII PAPER TAPE



BPM-017

PHYSICAL DIMENSIONS
Dual-In-Line

24-Pin Hermetic



Am27S32 • Am27S33

4096-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S32 and Am27S33 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

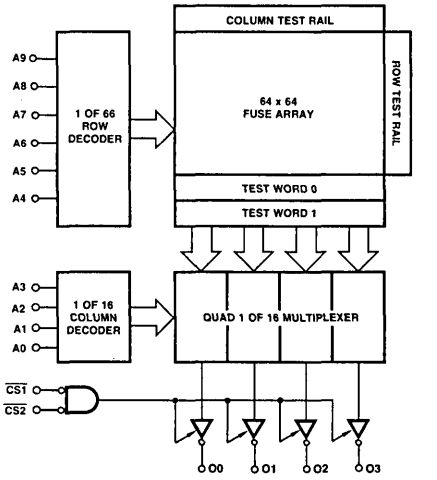
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S32DC
Hermetic DIP	−55°C to +125°C	AM27S32DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S33DC
Hermetic DIP	−55°C to 125°C	AM27S33DM

FUNCTIONAL DESCRIPTION

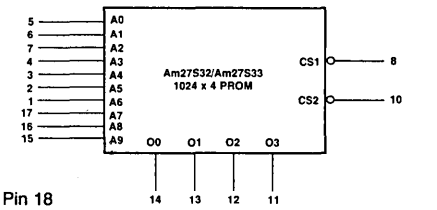
The Am27S32 and Am27S33 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 4 configuration, they are available in both open collector Am27S32 and three-state Am27S33 output versions. After programming, stored information is read on outputs O0–O3 by applying unique binary addresses to A0–A9 and holding the chip select inputs, $\overline{CS1}$ and $\overline{CS2}$, LOW. If either chip select input goes to a logic HIGH, O0–O3 go to the off or high impedance state.

BLOCK DIAGRAM



BPM-090

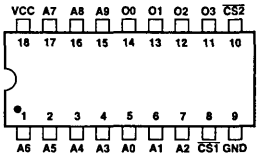
LOGIC SYMBOL



VCC = Pin 18
GND = Pin 9

BPM-091

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BPM-092

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +VCC max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am27S32XC, Am27S33XC	T_A = 0°C to +75°C	VCC = 5.0V ±5%
MIL	Am27S32XM, Am27S33XM	T_A = −55°C to +125°C	VCC = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
VOH (Am27S33 only)	Output HIGH Voltage	VCC = MIN., IOH = −2.0mA VIN = VIH or VIL			2.4			Volts
VOL	Output LOW Voltage	VCC = MIN., IOL = 16mA VIN = VIH or VIL					0.45	Volts
VIH	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
VIL	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
IIL	Input LOW Current	VCC = MAX., VIN = 0.45V				−0.020	−0.250	mA
IIH	Input HIGH Current	VCC = MAX., VIN = 2.7V					25	μA
II	Input HIGH Current	VCC = MAX., VIN = 5.5V					1.0	mA
ISC (Am27S33 only)	Output Short Circuit Current	VCC = MAX., VOUT = 0.0V (Note 2)			−20	−40	−90	mA
ICC	Power Supply Current	All inputs = GND VCC = MAX.		COM'L		105	140	mA
				MIL		105	145	
VI	Input Clamp Voltage	VCC = MIN., IIN = −18mA					−1.2	Volts
ICEX	Output Leakage Current	VCC = MAX. $\overline{VCS1}$ = 2.4V		VO = 4.5V			40	μA
			Am27S33 only	VO = 2.4V			40	
				VO = 0.4V			−40	
CIN	Input Capacitance	VIN = 2.0V @ f = 1MHz (Note 3)				5		pF
COUT	Output Capacitance	VOUT = 2.0V @ f = 1MHz (Note 3)				12		

Notes: 1. Typical limits are at VCC = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

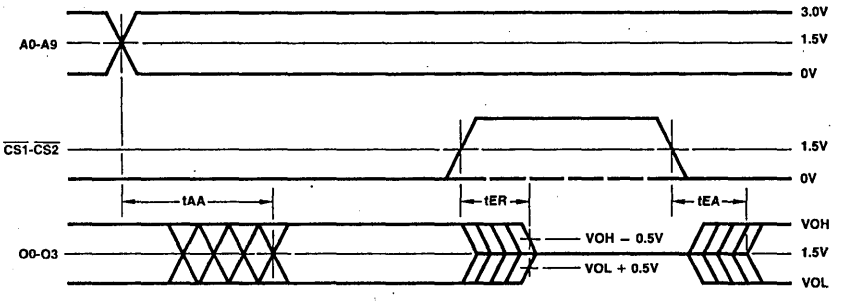
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	38	55	70	ns
t_{EA}	Enable Access Time		10	25	30	ns
t_{ER}	Enable Recovery Time		10	25	30	ns

Notes:
1. tAA is tested with switch S1 closed and CL = 30pF.
2. For open collector outputs, tEA and tER are tested with S1 closed to the 1.5V output level. CL = 30pF.
3. For three state outputs, tEA is tested with CL = 30pF to the 1.5V level; S1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. tER is tested with CL = 5pF. HIGH to high impedance tests are made with S1 open to an output voltage of VOH – 0.5V; LOW to high impedance tests are made with S1 closed to the VOL + 0.5V level.

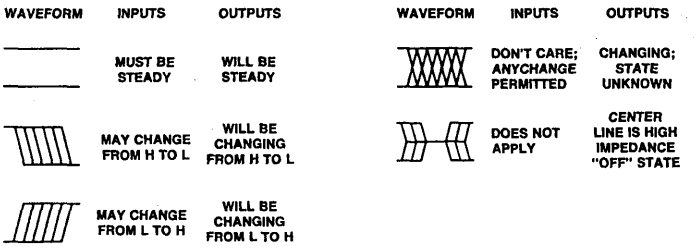
SWITCHING CHARACTERISTICS



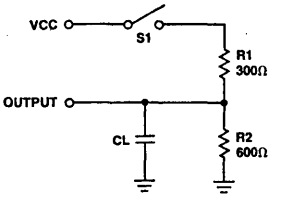
Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

BPM-093

KEY TO TIMING DIAGRAM



AC TEST LOAD



BPM-094

PROGRAMMING

The Am27S32 and Am27S33 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycle. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including VCC should be removed for a period of 5 seconds after which programming may be resumed.

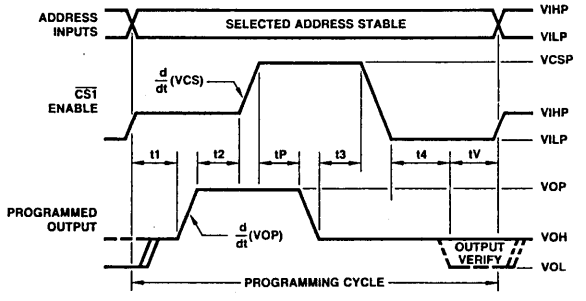
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
VCCP	VCC During Programming	5.0	5.5	Volts
VIHP	Input HIGH Level During Programming	2.4	5.5	Volts
VILP	Input LOW Level During Programming	0.0	0.45	Volts
VCSP	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
VOP	Output Voltage During Programming	19.5	20.5	Volts
VONP	Voltage on Outputs. Not to be Programmed	0	VCCP+0.3	Volts
IONP	Current into Outputs Not to be Programmed		20	mA
d(VOP)/dt	Rate of Output Voltage Change	20	250	V/μsec
d(VCS)/dt	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
tP	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5	15	msec

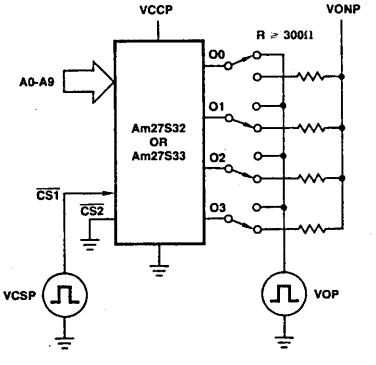
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e. not to the midpoints.
2. Delays t1, t2, t3 and t4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During tv, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to VONP through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-095

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-096

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each base part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S32 • Am27S33 ADAPTERS AND CONFIGURATOR	715-1414	PA 18-6 and 1024 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 1024 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

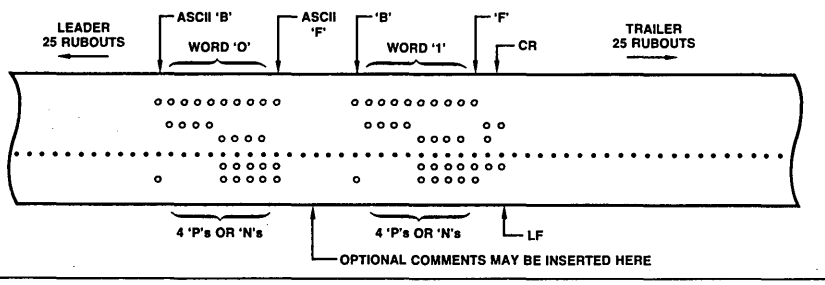
```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 .      .        .
 .      .        .
1024   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE

($\overline{CS1}$ and $\overline{CS2}$ = LOW)

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O3	O2	O1	O0
L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	L	H	H	L	H	H	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	L

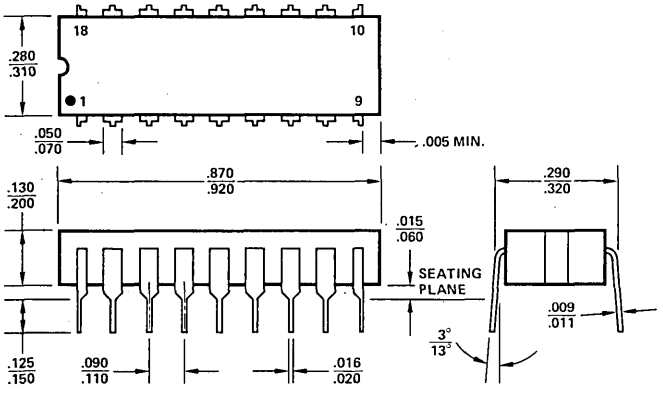
ASCII PAPER TAPE



BPM-097

PHYSICAL DIMENSIONS
Dual-In-Line

18-Pin Hermetic



Am27S180 • Am27S181

8192-Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- High Speed – 60ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S180 and Am27S181 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

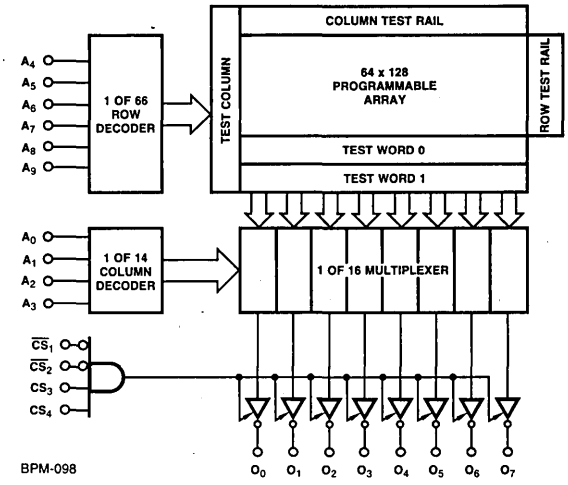
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S180DC
Hermetic DIP	−55°C to +125°C	AM27S180DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S181DC
Hermetic DIP	−55°C to +125°C	AM27S181DM

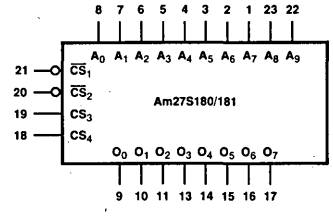
FUNCTIONAL DESCRIPTION

The Am27S180 and Am27S181 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 8 configuration, they are available in both open collector Am27S180 and three-state Am27S181 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_9 and enabling the chip ($\overline{CS}_1$, $\overline{CS}_2$, low and CS_3, CS_4 high). Changes of chip select input levels disables the outputs causing them to go to the off or high impedance state.

BLOCK DIAGRAM



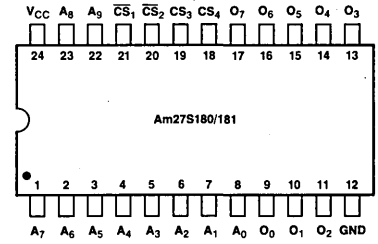
LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

COM'L	Am27S180XC, Am27S181XC	T_A = 0 to 75°C	V_{CC} = 5.0V ±5%
MIL	Am27S180XM, Am27S181XM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S181 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am27S181 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				120	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}1,2}$ = 2.4V $V_{CS3,4}$ = 0.4V		V_O = 4.5V			40	μA
			Am27S181 Only	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)				5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)				12		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

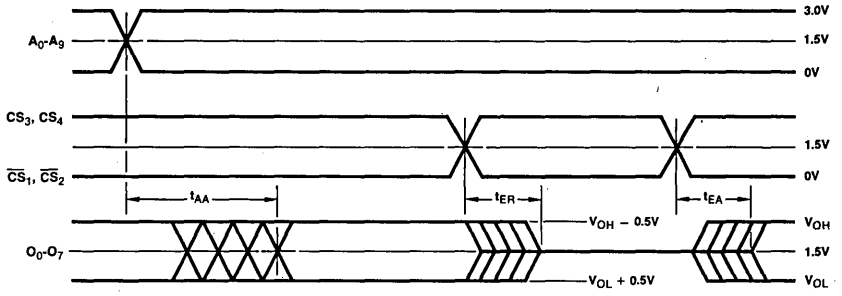
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	40	60	80	ns
t_{EA}	Enable Access Time		20	40	50	ns
t_{ER}	Enable Recovery Time		20	40	50	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

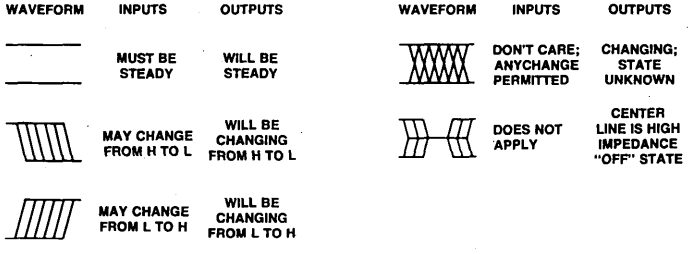
SWITCHING CHARACTERISTICS



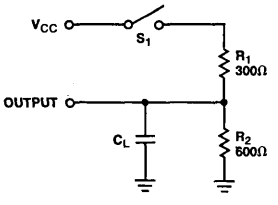
Note: Level on output while chip is disabled is determined externally.

BPM-101

KEY TO TIMING DIAGRAM



AC TEST LOAD



BPM-102

PROGRAMMING

The Am27S180 and Am27S181 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

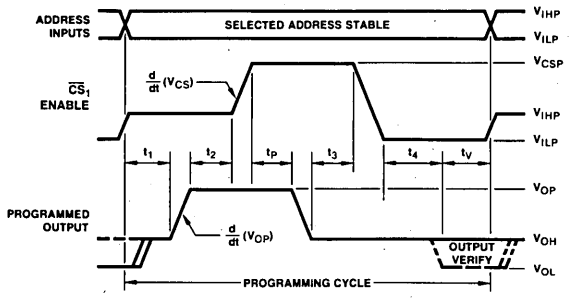
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

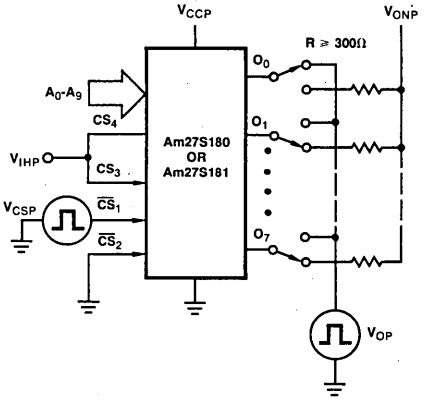
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-103

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-104

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S180 • Am27S181 ADAPTERS AND CONFIGURATOR	715-1545-2	PA24-13 and 1024 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 1024 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

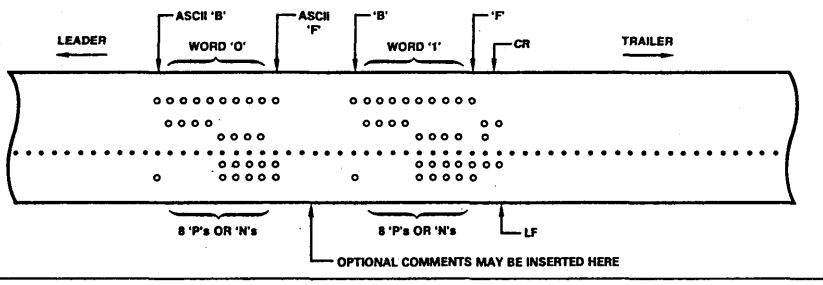
```
ØØØ   BPNPPNNNPF   WORD ZERO Ⓡ Ⓛ
      BPPPPPPNNF   COMMENT FIELD Ⓡ Ⓛ
ØØ2   BNNNPPPPNF   ANY Ⓡ Ⓛ
      BNNNNNNNNF   TEXT Ⓡ Ⓛ
ØØ4   BPNNNNNNPF   CAN Ⓡ Ⓛ
      BNPPNPPNNF   GO Ⓡ Ⓛ
ØØ6   BPNNPPPNNF   HERE Ⓡ Ⓛ
 •    ••••••••••••   •
1023   BNNNNPPPNF   END Ⓡ Ⓛ
```

Ⓡ = CARRIAGE RETURN
Ⓛ = LINE FEED

RESULTING DEVICE TRUTH TABLE
($\overline{CS}_1$ AND $\overline{CS}_2$ LOW, CS_3 AND CS_4 HIGH)

A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

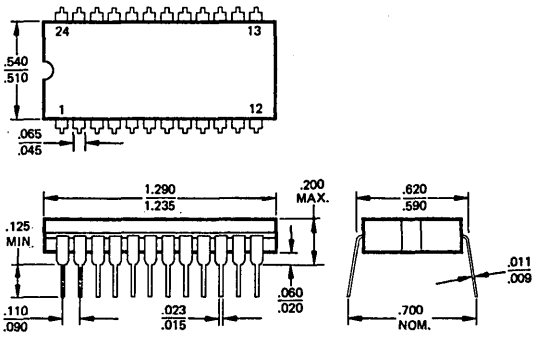
ASCII PAPER TAPE



BPM-105

PHYSICAL DIMENSIONS
Dual-In-Line

24-Pin Hermetic



Am27S184 • Am27S185

8192-Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am27S184 and Am27S185 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

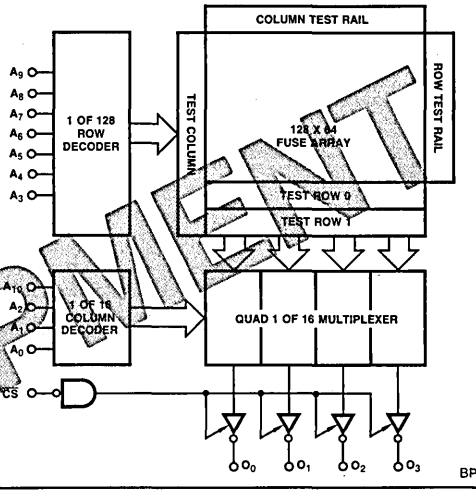
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
	Open Collectors	
Hermetic DIP	0 to +75°C	AM27S184DC
Hermetic DIP	−55 to +125°C	AM27S184DM
	Three-State Outputs	
Hermetic DIP	0 to +75°C	AM27S185DC
Hermetic DIP	−55 to +125°C	AM27S185DM

FUNCTIONAL DESCRIPTION

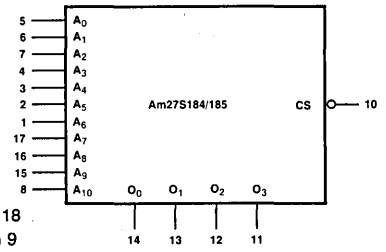
The Am27S184 and Am27S185 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 2048 x 4 configuration, they are available in both open collector Am27S184 and three-state Am27S185 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{10} and holding the chip select input $\overline{CS}$ LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high-impedance state.

BLOCK DIAGRAM



BPM-106

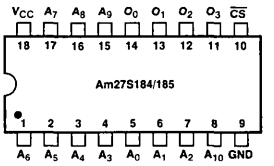
LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

BPM-107

CONNECTION DIAGRAM
Top View



Note 1: Pin 1 is marked for orientation.

BPM-108

PRELIMINARY

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

COM'L	Am27S184XC, Am27S185XC	T_A = 0 to 75°C	V_{CC} = 5.0V ±5%
MIL	Am27S184XM, Am27S185XM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH} (Am27S185 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.020	−.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			40	mA
I_{SC} (Am27S185 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		80	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}}$ = 2.4V; Am27S185 only; V_O = 4.5V			40	μA
		V_{CC} = MAX, $V_{\overline{CS}}$ = 2.4V; Am27S185 only; V_O = V_{CC}			40	μA
		V_{CC} = MAX, $V_{\overline{CS}}$ = 2.4V; Am27S185 only; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

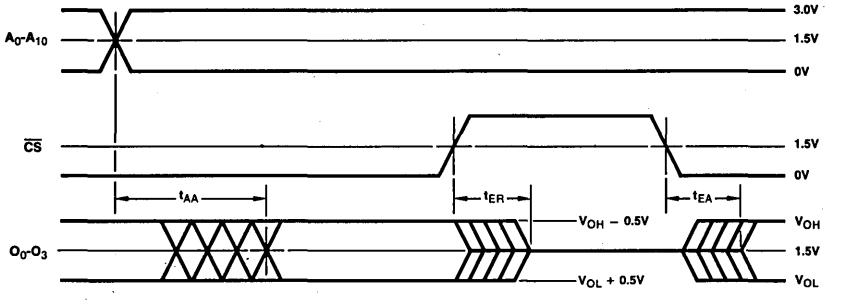
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	40	–	–	ns
t_{EA}	Enable Access Time		10	–	–	ns
t_{ER}	Enable Recovery Time		10	–	–	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

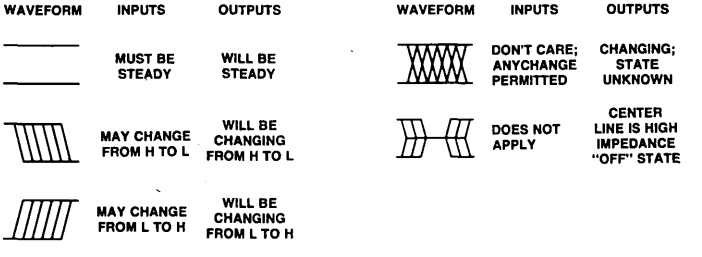
SWITCHING CHARACTERISTICS



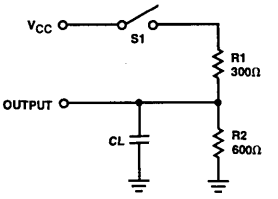
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

BPM-109

KEY TO TIMING DIAGRAM



AC TEST LOAD



BPM-110

PROGRAMMING

The Am27S184 and Am27S185 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

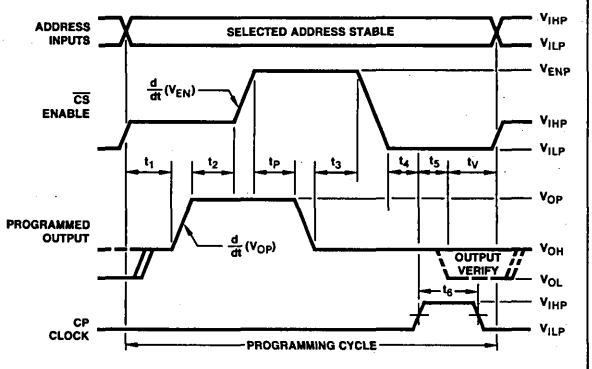
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

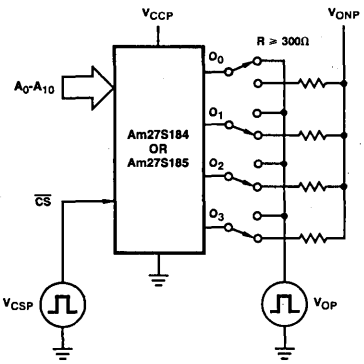
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-111

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-112

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S184 • Am27S185 ADAPTERS AND CONFIGURATOR	715-1616	PA18-8 and 2048 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 2048 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

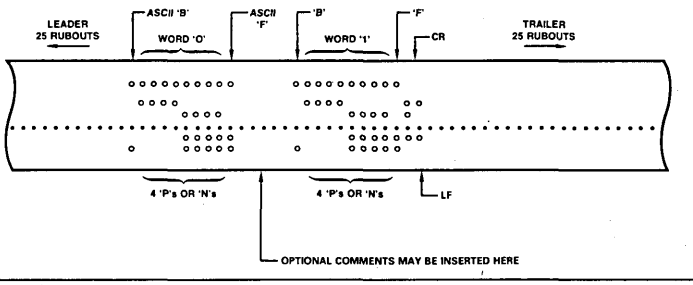
TYPICAL PAPER TAPE FORMAT

ØØØ	BNNNPF	WORD ZERO (R) (L)
	BPPNNF	COMMENT FIELD (R) (L)
ØØ2	BPPPNF	ANY (R) (L)
	BNNNNF	TEXT (R) (L)
ØØ4	BNNNPF	CAN (R) (L)
	BPPNNF	GO (R) (L)
ØØ6	BPPNNF	HERE (R) (L)
•	•	•
2047	BPPPNF	END (R) (L)

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ LOW)

A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	L	L	H	H	L	H	H	L	L
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

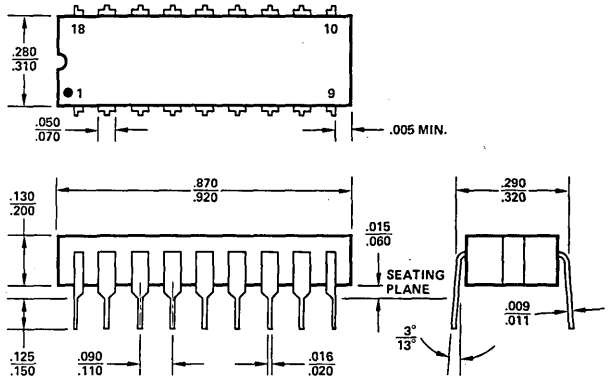
ASCII PAPER TAPE



BPM-113

PHYSICAL DIMENSIONS
Dual-In-Line

18-Pin Hermetic



PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, WA 98027	Pro-Log Corp. 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Ave. DeWitt Center Auburn, CA 95603
PROGRAMMER MODEL(S)	Model 5, 7 and 9 Systems 17 and 19	M900 and M920	
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058	IM 1010 IMAMDGEN1
ADAPTORS AND CONFIGURATOR			
Am27LS18/19	715-1407-1	PA16-6 and 32 x 8 (L)	IM32 x 8-16-AMD
Am27S18/19	715-1407-1	PA16-6 and 32 x 8 (L)	IM32 x 8-16-AMD
Am27S20/21	715-1408-1	PA16-5 and 256 x 4 (L)	IM256 x 4-16-AMD
Am27S12/13	715-1408-2	PA16-5 and 512 x 4 (L)	IM512 x 4-16-AMD
Am27S15	715-1411-1	PA24-14 and 512 x 8 (L)	IM512 x 8-24-27S15-AMD
Am27S25	715-1617	PA24-16 and 512 x 8 (L)	IM512 x 8-24-27S25-AMD
Am27S26/27	715-1412-2	PA22-4 and 512 x 8 (L)	IM512 x 8-22-27S26/27-AMD
Am27S28/29	715-1413	PA20-4 and 512 x 8 (L)	IM512 x 8-20-AMD
Am27S30/31	715-1545	PA24-13 and 512 x 8 (L)	IM512 x 8-24-AMD
Am27S32/33	715-1414	PA18-6 and 1024 x 4 (L)	IM1024 x 4-18-AMD
Am27S180/181	715-1545-2	PA24-13 and 1024 x 8 (L)	IM1024 x 8-24-AMD
Am27S184/185	715-1616	PA18-8 and 2048 x 4 (L)	IM2048 x 4-18-AMD

Below are listed other programming equipment manufacturers who are currently in various stages of implementation and evaluation of programming hardware for AMD Bipolar Generic PROMs:

Accutest Corp.
25 Industrial Ave.
Chelmsford, MA 01824
(617) 256-8124
TWX: 710-347-0620

E-H International, Inc.
515 11th St.
Oakland, CA 94604
Tel: (415) 834-3030
TWX: 910-366-7258

Takeda Riken Industry Co., Ltd.
1-32-1 Asahi-cho Nerima-Ku
Tokyo, Japan 176
Tel: Tokyo: 930-4111
Cable Address: Tritronics Tokyo
Telex: 272-2140

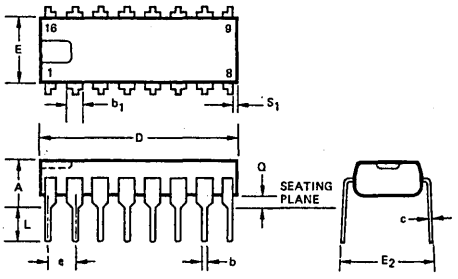
Digitronics Israel Ltd.
3 Tevuot Haaretz St.
Tel-Aviv, Israel
Tel: 03-472010
Telex: 32470, Coin II Attn: Digitronics

Kontron Electronic, Inc.
700 S. Claremont St.
San Mateo, CA 94402
Tel: (415) 348-7291
Telex: 00255-910-374-3001

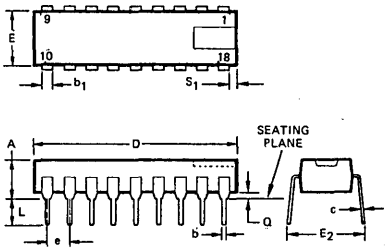
PACKAGE OUTLINES

MOLDED DUAL IN-LINE PACKAGES

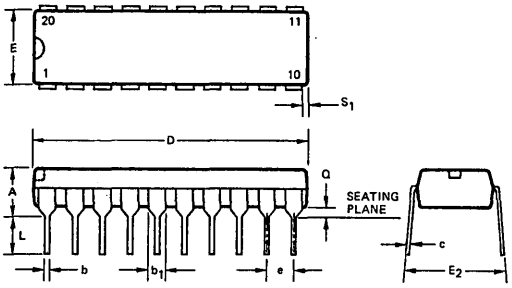
P-16-1



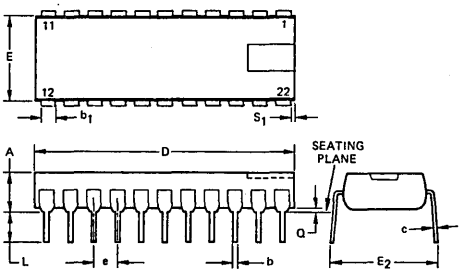
P18-1



P-20-1



P-22-1



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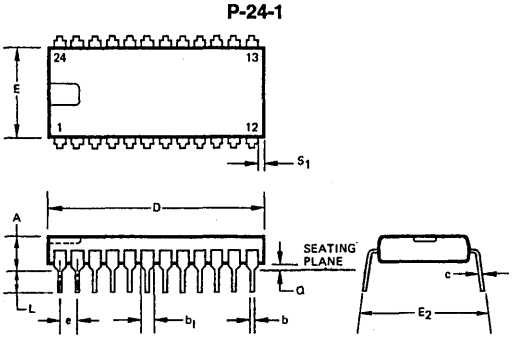


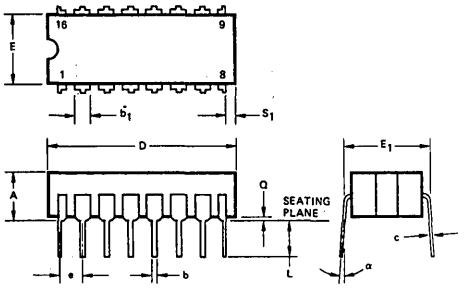
AMD Pkg.	P-16-1		P-18-1		P-20-1		P-22-1		P-24-1	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215
b	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.745	.775	.895	.925	1.010	1.050	1.080	1.120	1.240	1.270
E	.240	.260	.240	.260	.250	.290	.330	.370	.515	.540
E_2	.310	.385	.310	.385	.310	.385	.410	.480	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.010	.040	.030	.040	.025	.055	.015	.045	.035	.065

Notes: 1. Standard lead finish is tin plate or solder DIP.
2. Dimension E_2 is an outside measurement.

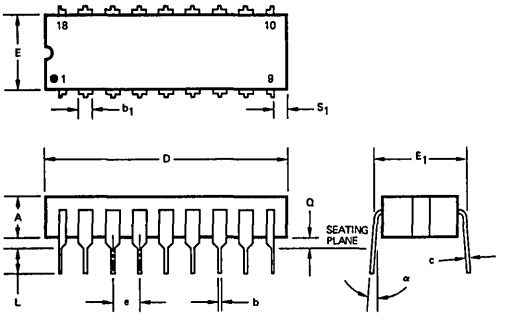
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

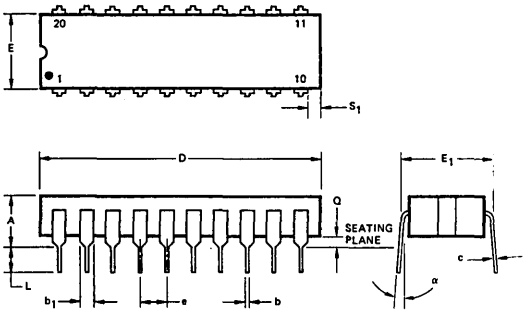
D-16-1



D18-1



D-20-1



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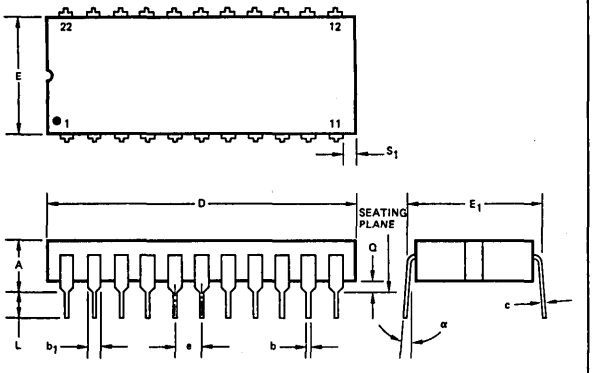
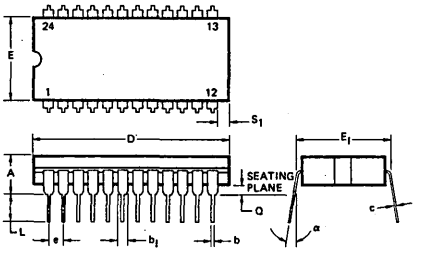
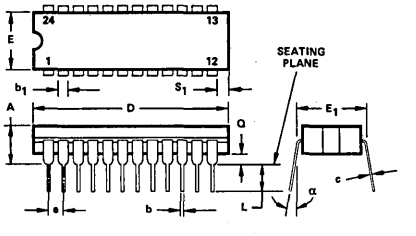


D-24-1



D-24-SLIM



PACKAGE OUTLINES (Cont.)

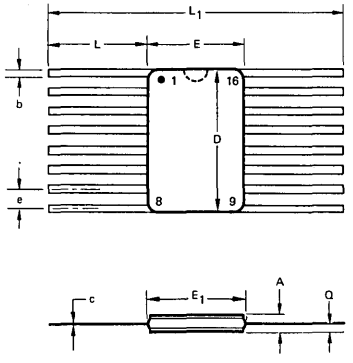
HERMETIC DUAL IN-LINE PACKAGES (Cont.)

AMD Pkg.	D-16-1		D-18-1		D-20-1		D-22-1		D-24-1			
Common Name	CERDIP		CERDIP		CERDIP		CERDIP		CERDIP		SLIM CERDIP	
38510 Appendix C	D-2(1)		–		–		–		D-3(1)		–	
Parameters	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.130	.200	.130	.200	.140	.220	.140	.220	.150	.225	.140	.220
b	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020	.016	.020
b_1	.050	.070	.050	.070	.050	.070	.045	.065	.045	.065	.045	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.745	.785	.870	.920	.935	.970	1.045	1.110	1.230	1.285	1.230	1.285
E	.240	.310	.280	.310	.245	.285	.360	.405	.510	.545	.245	.285
E_1	.290	.320	.290	.320	.290	.320	.390	.420	.600	.620	.290	.320
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.120	.150	.120	.150
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.005		.005		.005		.005		.010		.010	
α	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°	3°	13°
Standard Lead Finish	b				b		b		b			

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

FLAT PACKAGES

F-16-1



Note: Notch is pin 1 index on cerpack.

AMD Pkg.	F-16-1	
Common NAME	CERPACK	
38510 Appendix C	F-5	
Parameters	Min.	Max.
A	.045	.085
b	.015	.019
c	.004	.006
D	.370	.425
D_1		
E	.245	.285
E_1		.290
e	.045	.055
L	.300	.370
L_1	.920	.980
Q	.020	.040
S_1	.005	
Standard Lead Finish	b	

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions E_1 and D_1 allow for off-center lid, meniscus, and glass overrun.

ORDERING INFORMATION

All Advanced Micro Devices' products listed are stocked locally and distributed nationally by Franchised Distributors. See back of this book for the location nearest you. Please consult them for the latest price revisions. For direct factory orders, call Advanced Micro Devices, 901 Thompson Place, Sunnyvale, California 94086, (408) 732-2400, TWX: 910-339-9280, TELEX: 34-6306.

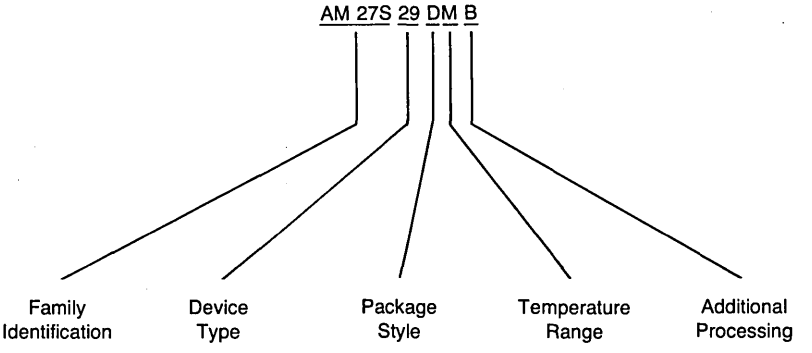
Minimum Order

The minimum direct factory order is $100.00 for a standard product.

The minimum direct factory order for Class B, burned-in, product is $250.00.

Proprietary Product Ordering, Package and Temperature Range Codes

The following scheme is used to identify Advanced Micro Devices' proprietary products.



Package Style

D = Hermetic DIP
F = Flat Package
P = Molded DIP
X = Dice

Temperature Range

C = Commercial
0 to 70°C
M = Military
−55 to +125°C

Additional Processing

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)

STANDARD PRODUCT PROCESSING AND OPTIONS

1. AMD STANDARD PRODUCT – CLASS C PROCESSING

All products manufactured by Advanced Micro Devices, including Bipolar Memory, Bipolar Logic and Interface, Microprocessors, Linear and MOS/LSI meet the quality requirements of MIL-M-38510. In addition all products, both commercial and military temperature range receive the 100% screening procedures defined in the current revision of MIL-STD-883, Method 5004, Class C. This processing is described in Advanced Micro Devices' Product Assurance Document 15-010.

a) Internal visual inspection: Method 2010. Condition B.
b) High temperature storage: Method 1008, Condition C; 150°C, 24 hours.
c) Temperature cycling: Method 1010, Condition C; −65°C, 150°C, 10 cycles.
d) Constant acceleration: Method 2001, Condition E; 30,000 g., Y_1 plane. (Hermetic packages only.)
e) Fine leak: Method 1014, Condition A; 5 x 10^{-8} atm cc per second. (Hermetic packages only.)
f) Gross leak: Method 1014, Condition C, Step 2. (Hermetic packages only.)
g) Final electrical test: 100% D.C. and functional testing at 25°C and Group A sample per Method 5005.

To order this product, use the order number shown for the product desired. Example: Am27S29DM for full military temperature range part in dual-in-line package, Am27S29DC for commercial temperature range in dual-in-line package.

As noted, all material is processed to Class C and no additional price adders are imposed to deliver this level of reliability.

2. CLASS B PROCESSING

Military Temperature Range

Standard product is upgraded to Class B with a 160-hour burn-in at 125°C followed by 100% electrical testing of D.C. parameters at 25°C, 125°C, −55°C and A.C. parameters at 25°C.

Burn-in conditions are steady state power (MIL-STD-883, Method 1015.1, Condition B) for linear circuits, and steady state power and reverse bias (Condition C) for all others. Standard burn-in circuit specifications for any device are available upon request. Condition D burn-in is available to special order. Consult your local AMD sales office for price and delivery.

To order this product, use the order number shown for the product desired and add the suffix "B". Example: Am27S29DMB for military temperature product in dual-in-line package with burn-in as described. This processing meets all of the requirements of MIL-STD-883, Class B product.

Commercial Temperature Range

Standard AMD Class C commercial temperature range product is burned-in for use in non-military systems to a modified Class B program. A 160 hour burn-in, to a method meeting the requirements of Method 1015.1, Conditions A and B, is followed by the standard Class C electrical test procedures.

To order this level of screening, use the order number shown for the commercial device and add the suffix "B". Example: Am27S29DCB.

3. CLASS S PROCESSING (FORMERLY CLASS A)

Class S processing is recommended only for applications where replacement is extremely difficult and reliability is imperative. This material is only produced to special order. Consult AMD for further details.

PRODUCT ASSURANCE
MIL-M-38510 • MIL-STD-883

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Two military documents provide the foundation for this program. They are:

MIL-M-38510 – General Specification for Microcircuits
MIL-STD-883 – Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. All circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.

MIL-STD-883 defines detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of the latest revision of Method 2010, condition B.

Test Method 5004 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C – Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B – Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C followed by more extensive electrical measurements. All other screening requirements are the same.

Class S – Used where replacement is extremely difficult and reliability is imperative. Class S screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C. Molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number, except that linear 100, 200 or 300 series are suffixed "/883B".

Test Method 5005 defines qualification and quality conformance procedures. Subgroups, tests and quality levels are given for Group A (electrical), Group B (mechanical quality related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user.

MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B quality levels on either Class B or Class C product.

All full-temperature-range (−55°C to +125°C) circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.

STANDARD PROCESSING CLASS C Steps 1 Through 25

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

1 **INSPECTION**

Purchased or fabricated starting materials are inspected for conformance to specified requirements. Inspection follows written procedures, and records are analyzed for supplier quality negotiations.

2 **WAFER FABRICATION**

Repeated masking, etching and diffusion processes produce finished dice in wafer form.

3 **IN-PROCESS INSPECTION**

Each wafer is inspected prior to irreversible process steps.

4 **FINISHED WAFER INSPECTION**

Sample wafers from each finished diffusion lot are inspected to confirm lot quality before release for test and assembly.

5 **WAFER ELECTRICAL TEST**

Electrical probe test of every die. A computer-controlled system measures static and dynamic parameters and identifies dice that do not meet electrical requirements.

6 **DIE SEPARATION**

Wafers are separated into individual dice and electrical rejects are removed.

7 **VISUAL INSPECTION**

Separated dice are inspected and selected at high magnification.

8 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, confirming product quality and revealing any need for operator retraining.

9 **DIE ATTACH**

10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices – MIL-STD-883, Method 2010, Condition B (latest revision). Full temperature devices – MIL-M-38510, Para. 3.7 for workmanship (re-bonding limits).

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

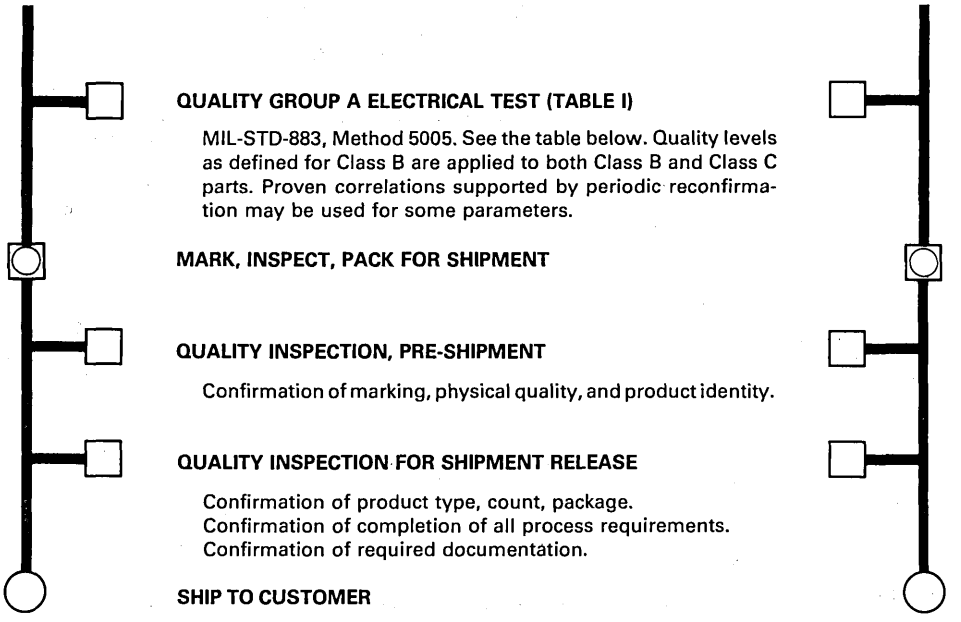
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C or in certain products at the most critical extreme temperature to assure accuracy of device selection.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

MIL-STD-883, Method 5005. See the table below. Quality levels as defined for Class B are applied to both Class B and Class C parts. Proven correlations supported by periodic reconfirmation may be used for some parameters.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

This AMD standard product meets screening requirements of MIL-STD-883, Class C.

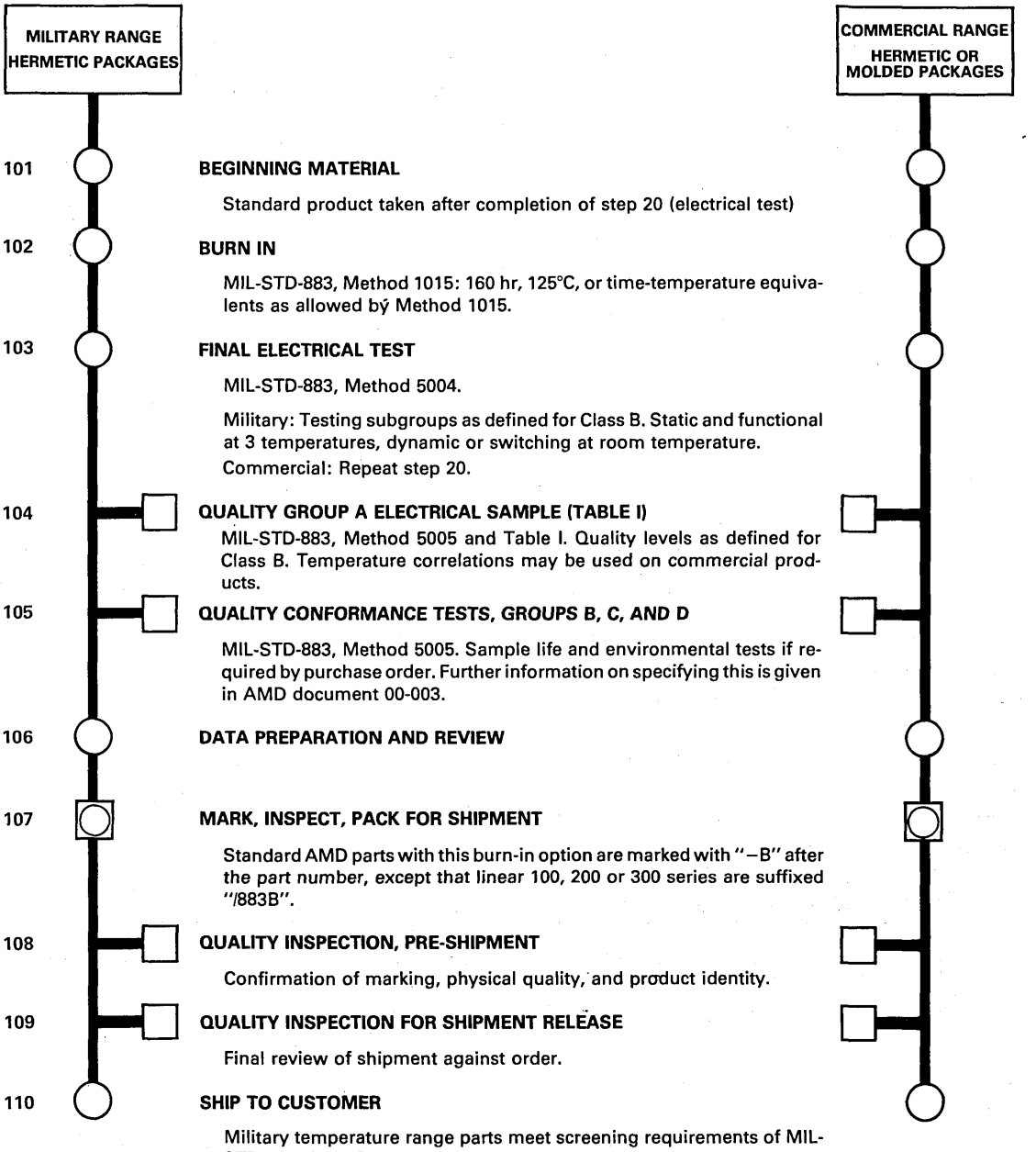
GROUP A ELECTRICAL TESTS
From MIL-STD-883, Method 5005, Table I

Subgroups	LTPD (Note 1)	Initial Sample Size
Subgroup 1 — Static tests at 25°C	5	45
Subgroup 2 — Static tests at maximum rated operating temperature	7	32
Subgroup 3 — Static tests at minimum rated operating temperature	7	32
Subgroup 4 — Dynamic tests at 25°C — Linear devices	5	45
Subgroup 5 — Dynamic tests at maximum rated operating temperature — Linear devices	7	32
Subgroup 6 — Dynamic tests at minimum rated operating temperature — Linear devices	7	32
Subgroup 7 — Functional tests at 25°C	5	45
Subgroup 8 — Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 — Switching tests at 25°C — Digital devices	7	32
Subgroup 10 — Switching tests at maximum rated operating temperature — Digital devices (Note 2)	10	10
Subgroup 11 — Switching tests at minimum rated operating temperature — Digital devices (Note 2)	10	10

1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. These subgroups are usually performed during initial device characterization only.

OPTIONAL EXTENDED PROCESSING
CLASS B
Steps 101 Through 110

Advanced Micro Devices offers several extended processing options to meet customer high-reliability requirements. These are defined in AMD document 00-003. The flow chart below outlines Option B, a 160-hr burn in. Military temperature range devices processed to this flow (in the left column) meet the screening requirements of MIL-STD-883, Class B.



OTHER OPTIONS

Document 00-003, "Extended Processing Options", further defines Option B as well as other screening or sampling options available or special order. Available options are listed here for reference.

Option	Description	Effect
A	Modified Class A screen (Similar to Class S screening)	Provides space-grade product, following most Class S requirements of MIL-STD-883, Method 5004.
B	160-hr operating burn in	Upgrades a part from Class C to Class B.
X	Radiographic inspection (X-ray)	Related to Option A. Provides limited internal inspection of sealed parts.
S	Scanning Electron Microscope (SEM) metal inspection	Sample inspection of metal coverage of die.
V	Preseal visual inspection to MIL-STD-883, Method 2010, Cond. A	More stringent visual inspection of assemblies and die surfaces prior to seal.
P	Particle impact noise (PIN) screen with ultrasonic detection.	Detects loose particles of approximately 0.5 mil size or larger, which could affect reliability in zero-G or high vibration applications.
Q	Quality conformance inspection (Group B, C and D life and environmental tests)	Samples from the lot are stressed and tested per Method 5005. The customer's order must state which groups are required. Group B destroys 16 devices; Group C, 92 devices; Group D, 60 devices.

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