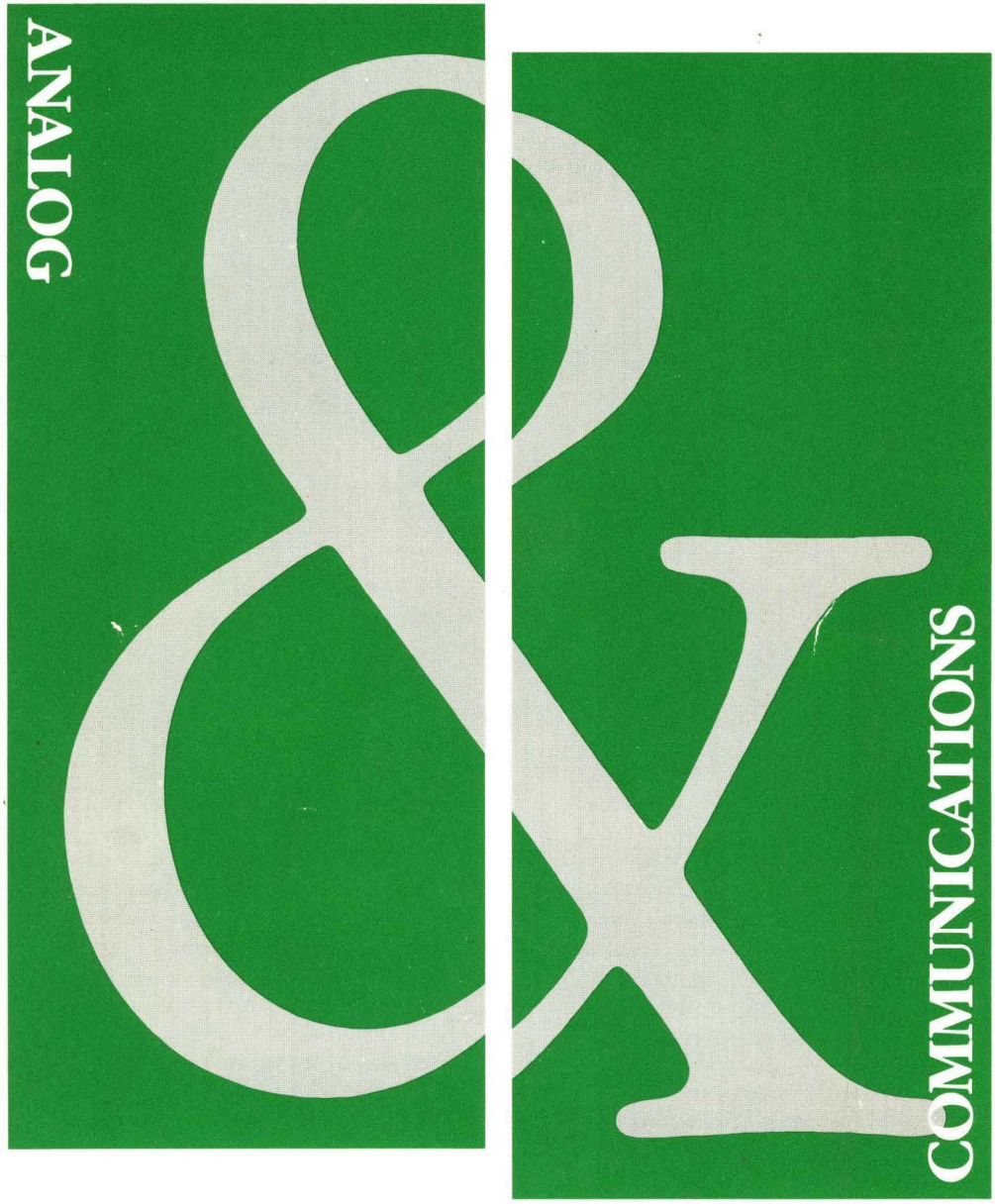
Analog and Communications Products

Data Acquisition
Telecommunications
Local Area Networks
1983 Data Book



ADVANCED MICRO DEVICES

Advanced Micro Devices

Analog and Communications Products Data Book

The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI, Logic & other memories.

MIL-STD-883

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Section X

Selection Guide

OPERATIONAL AMPLIFIERS

Part Number	Description	Parameters* V_{OS}	I_B	I_{OS}	TC V_{OS}	SR
Uncompensated						
LM108	Low Input Current Precision	2mV	2nA	0.2nA	15μV/°C	
LM108A	Low Input Current and Offset Voltage Precision	0.5mV	2nA	0.2nA	5μV/°C	
LM2108A	Dual Precision	0.5mV	2nA	0.2nA	5μV/°C	
Compensated						
LM118	High Speed	4mV	250nA	50nA	20μV/°C (T)	50V/μs
LM148	Quad 741	5mV	100nA	25nA	10μV/°C (T)	5V/μs (T)
LF155	JFET Input General Purpose	5mV	100pA	20pA	5μV/°C (T)	
LF155A	JFET Input General Purpose	2mV	50pA	10pA	3μV/°C (T)	3V/μs
LF156	JFET Input Wideband	5mV	100pA	20pA	5μV/°C (T)	7.5V/μs
LF156A	JFET Input Wideband	2mV	50pA	10pA	3μV/°C (T)	10V/μs

VOLTAGE COMPARATORS

Part Number	Description	Parameters* V_{OS} (T)	I_B (T)	t_{RESP}	V+, V−	V_O, I_O
LM111	General Purpose	3mV	100nA	250ns		50V, 50mA
LM119	Dual General Purpose	4mV	500nA	80ns	+5 to +15V, 0 to −15V	35V, 25mA
LM139	Quad General Purpose Low Power (1mW/comp.)	5mV	100nA	1.3μs	+2 to +36V, ±1 to ±18V	
LM139A	Quad General Purpose	2mV	100nA	1.3μs	+2 to 36V, ±1 to 18V	
Am685	Very Fast ECL Output	2mV	10μA	6.5ns	+2.7 to +7V, −2.7 to −7V	V_{OH} = −0.9V V_{OL} = −1.75V I_O = 30mA
Am686	Very Fast TTL Output	2mV	10μA	12ns	+2.7 to +7V, −2.7 to −7V	
Am687	Dual Very Fast ECL Output	3mV	10μA	8ns	+2.7 to +7V, −2.7 to −7V	
Am687A	Dual Very Fast ECL Output	2mV	10μA	8ns	+2.7 to +7V, −2.7 to −7V	
Am1500	Dual General Purpose	3mV	100nA	250ns		
LH2111	Dual General Purpose	3mV	100nA	250ns		
Am6685	Ultra Fast ECL Output	±0.5mV	15μA	2.5ns	+2.7 to +7V, −2.7 to −7V	V_{OH} = −0.9V V_{OL} = −1.75V I_O = 30mA
Am6687	Dual Ultra Fast ECL Output	±0.5mV	15μA	2.5ns	+2.7 to +7V, −2.7 to −7V	

POWER SUPPLY CONTROLLERS

Part Number	Description	Parameters* I_O	V_O	$\Delta V_{REF}/\Delta I_{REF}$	V_{IN}
Am6300	Power Control Subsystem	100mA	37.5V	0.15% V_{REF}	+5 to +40V
Am6301	Switching Power Supply Controller	70mA	33V	0.4% V_{REF}	+11 to +30V

*All specifications are limit values at 25°C unless otherwise specified. (T) indicates typical value. For a complete description of parameters, please refer to Glossary.

SELECTION GUIDE (Cont.)

DATA ACQUISITION PRODUCTS

Part Number	Description	Parameters* t_{IS}	t_C	
DAC-08	8-Bit High-Speed Multiplying DAC	85ns		
LM1508	8-Bit Multiplying DAC	300ns		
SSS1508	8-Bit Multiplying DAC	135ns		
Am2502/03	8-Bit Successive Approximation Registers			
Am2504	12-Bit Successive Approximation Registers			
Am25L02/03	Low Power 8-Bit Successive Approximation Registers			
Am25L04	Low Power 12-Bit Successive Approximation Registers			
Am6012	12-Bit High-Speed Multiplying DAC	250ns		
Am6014	14-Bit High-Speed Multiplying DAC	500ns		
Am6022	12-Bit Ultra-High-Speed Multiplying DAC	75ns		
Am6070	Companding DAC for Control Systems	300ns		
Am6072	Companding DAC for PCM Communications Systems	300ns		
Am6606	6-Bit 100MHz Quantizer		10ns	
Am6688	4-Bit 100MHz Quantizer		10ns	
Microprocessor Compatible				
Am6080	8-Bit High-Speed Multiplying DAC	160ns		
Am6081	8-Bit High-Speed Multiplying DAC	200ns		
Am6082	12-Bit High-Speed Complete DAC	100ns		
Am6108/Am6148	8-Bit Complete A/D Converter		1μs	
Am6112	12-Bit Complete A/D Converter		3.3μs	

SAMPLE AND HOLDS

Part Number	Description	Acquisition Time to .01%	
LF198	Monolithic Sample and Hold	6μs	
Am6420	High-Speed 12-Bit Accurate Sample and Hold	500ns	

*All specifications are limit values at 25°C unless otherwise specified. (T) indicates typical value. For a complete description of parameters, please refer to Glossary.

Industry Cross Reference

Analog Devices	AMD
ADDAC-08AD	DAC-08AQ
ADDAC-08CD	DAC-08CQ
ADDAC-08D	DAC-08Q
ADDAC-08ED	DAC-08EQ
ADDAC-08HD	DAC-08HQ
AD108A	LM108A
AD108	LM108
AD111	LM111
AD1408-7D	AM1408L7
AD1408-8D	AM1408L8
AD1508-8D	AM1508L8
AD308	LM308
AD311	LM311
AD518	LM118
AD9685	AM685
AD9687	AM687

Fairchild	AMD
μA0801ADM	DAC-08AQ
μA0801CDC	DAC-08CQ
μA0801CPC	DAC-08CN
μA0801DM	DAC-08Q
μA0801EDC	DAC-08EQ
μA0801EPC	DAC-08EN
μA0801HDC	DAC-08HQ
μA0801HPC	DAC-08HN
μA0802ADC	AM1408L8
μA0802APC	AM1408N8
μA0802BDC	AM1408L7
μA0802BPC	AM1408N7
μA0802CDC	AM1408L6
μA0802CPC	AM1408N6
μA0802DM	AM1508L8
μA108AH	LM108AH
μA108H	LM108H
μA111H	LM111H
μA118	LM118
μA139A	LM139A
μA139DM	LM139D
μA139D	LM139D
μA148	LM148
μA198	LF198
μA207H	LM207H
μA208AH	LM208AH
μA208H	LM208H
μA308AH	LM308AH
μA308H	LM308H
μA311H	LM311H
μA311P	LM311N
μA339A	LM339A
μA339D	LM339D
μA339P	LM339N
μA348	LM348
μA398	LF398

Hitachi	AMD
HA17008	DAC-08
HA17012	AM6012
HA17408	AM1408

Harris	AMD
LF156	LF156
LF356	LF356
LM108A	LM108A
LM108	LM108
LM118	LM118
LM148	LM148
LM308A	LM308A
LM308	LM308
LM318	LM318
LM348	LM348

Intersil	AMD
LH2101A	LH2101A
LH2111	LH2111
LM108A	LM108A
LM108	LM108
LM111	LM111
LM139A	LM139A
LM139	LM139
LM308A	LM308A
LM308	LM308
LM311	LM311
LM339A	LM339A
LM339	LM339

Motorola	AMD
DAC-08	DAC-08
DAC-08AQ	DAC-08AQ
DAC-08CP	DAC-08CN
DAC-08CQ	DAC-08CQ
DAC-08EP	DAC-08EN
DAC-08EQ	DAC-08EQ
DAC-08HP	DAC-08HQ
DAC-08HQ	DAC-08HN
DAC-08Q	DAC-08Q
LF155	LF155
LF156	LF156
LF355	LF355
LF356	LF356
LH2101A	LH2101A
LH2111	LH2111

Motorola	AMD
LM108A	LM108A
LM108	LM108
LM111G	LM111H
LM111L	LM111D
LM139A	LM139A

Motorola	AMD
LM139	LM139
LM148	LM148
LM211G	LM211H
LM211L	LM211D
LM308A	LM308A
LM308	LM308
LM311G	LM311H
LM311L	LM311D
LM311N	LM311N
LM339A	LM339A
LM339	LM339
LM348	LM348
MC1408L6	AM1408L6
MC1408L7	AM1408L7
MC1408L8	AM1408L8
MC1508L8	AM1508L8

National	AMD
DAC0800LAJ	DAC-08AQ
DAC0800LCJ	DAC-08EQ
DAC0800LCN	DAC-08EN
DAC0800LJ	DAC-08Q
DAC0801LCJ	DAC-08CQ
DAC0801LCN	DAC-08CN
DAC0802LCJ	DAC-08HQ
DAC0802LCN	DAC-08HN
DAC0806LCJ	AM1408L6
DAC0806LCN	AM1408N6
DAC0807LCJ	AM1408L7
DAC0807LCN	AM1408N7
DAC0808LCJ	AM1408L8
DAC0808LCN	AM1408N8
DAC0808LJ	AM1508L8
LF155AH	LF155AH
LF155H	LF155H
LF156AH	LF156AH
LF156H	LF156H
LF198H	LF198H
LF255H	LF255H
LF256H	LF256H
LF298H	LF298H
LF355AH	LF355AH
LF355H	LF355H
LF355N	LF355N
LF356AH	LF356AH
LF356H	LF356H
LF356N	LF356N
LF357AH	LF357AH
LF398H	LF398H
LH2101AD	LH2101AD
LH2101AF	LH2101AF
LH2101AJ	LH2101AD
LH2111D	LH2111D
LH2111D	AM1500DM
LH2111F	LH2111F

Industry Cross Reference

National	AMD
LH2111J	LH2111D
LH2201AD	LH2201AD
LH2201AF	LH2201AF
LH2201AJ	LH2201AD
LH2211D	LH2211D
LH2211F	LH2211F
LH2211J	LH2211D
LH2301AD	LH2301AD
LH2301AJ	LH2301AD
LH2311D	LH2311D
LH2311J	LH2311D
LM108AD	LM108AD
LM108AF	LM108AF
LM108AH	LM108AH
LM108AJ	LM108AD
LM108D	LM108D
LM108F	LM108F
LM108H	LM108H
LM108J	LM108D
LM111D	LM111D
LM111F	LM111F
LM111H	LM111F
LM111J	LM111D
LM118D	LM118D
LM118F	LM118F
LM118H	LM118H
LM118J	LM118D
LM119D	LM119D
LM119F	LM119F
LM119H	LM119H
LM119J	LM119D
LM139AD	LM139AD
LM139AF	LM139AF
LM139AJ	LM139AJ
LM139D	LM139D
LM139J	LM139D
LM148D	LM148D
LM208AD	LM208AD
LM208AF	LM208AF
LM208AH	LM208AH
LM208AJ	LM208AD
LM208D	LM208D
LM208F	LM208F
LM208H	LM208H
LM208J	LM208D
LM211D	LM211D
LM211F	LM211F
LM211H	LM211H
LM211J	LM211D
LM218D	LM218D
LM218F	LM218F
LM218H	LM218H
LM218J	LM218D
LM219D	LM219D
LM219F	LM219F
LM219H	LM219H
LM219J	LM219J
LM239AD	LM239AD
LM239AJ	LM239AD
LM239D	LM239D

National	AMD
LM318D	LM318D
LM318F	LM318F
LM318H	LM318H
LM318J	LM318D
LM318N	LM318N
LM319D	LM319D
LM319H	LM319H
LM319J	LM319J
LM239J	LM239D
LM248D	LM248D
LM308AD	LM308AD
LM308AF	LM308AF
LM308AH	LM308AH
LM308AJ	LM308AD
LM308AN	LM308AN
LM308D	LM308D
LM308F	LM308F
LM308H	LM308H
LM308J	LM308D
LM308N	LM308N
LM311D	LM311D
LM311F	LM311F
LM311J	LM311D
LM339AD	LM339AD
LM339AJ	LM339AD
LM339AN	LM339AN
LM339N	LM339N
LM348D	LM348D
LM348N	LM348N

NEC	AMD
UDC159A	LM118

Plessey	AMD
SP9685	AM685
SP9687	AM687

PMI	AMD
DAC08	DAC-08
DAC312BR	AM6012DM
DAC312BR	AM6012DM
DAC312FR	AM6012ADC
DAC312FR	AM6012DC
DAC76CX	AM6070DC
DAC76EX	AM6070ADC
DAC78FX	AM6070ADC
DAC78GX	AM6070DC
DAC-76BX	AM6070ADM
DAC-76CX	AM6070DC
DAC-76EX	AM6070ADC
DAC-76X	AM6070DM
DAC-86EX	AM6072DC
PM108A	LM108A
PM108	LM108
PM139	LM139
PM155	LM155
PM156	LM156
PM308A	LM308A

PMI	AMD
PM308	LM308
PM339	LM339
PM355	LM355
PM356	LM356
SSS1408A-6Q	SSS1408A-6Q
SSS1408A-7Q	SSS1408A-7Q
SSS1408A-8Q	SSS1408A-8Q
SSS1508A-8Q	SSS1508A-8Q

RCA	AMD
CA111	LM111
CA139	LM139
CA311	LM311
CA339	LM339

Raytheon	AMD
DAC-08	DAC-08
DAC-08ADM	DAC-08AQ
DAC-08CBM	DAC-08CN
DAC-08CDM	DAC-08CQ
DAC-08DM	DAC-08Q
DAC-08EBM	DAC-08EN
DAC-08EDM	DAC-08EQ
DAC-08HBM	DAC-08HN
DAC-08HDM	DAC-08HQ
DAC-08CBM	DAC-08CN
LH2101A	LH2101A
LH2111	LH2111
LM108A	LM108A
LM108	LM108
LM111	LM111
LM118	LM118
LM139	LM139
LM148	LM148
LM311H	LM311H

Signetics	AMD
LF198	LF198
LF398	LF398
LH2101A	LH2101A
LH2111	LH2111
LM108AF	LM108AD
LM108AT	LM108AH
LM108F	LM108D
LM108T	LM108H
LM111F	LM111D
LM111T	LM111H
LM119D	LM119D
LM119T	LM119H
LM139F	LM139D
LM139	LM139
LM208AF	LM208AD
LM208AT	LM208AH
LM208F	LM208D
LM208T	LM208H
LM211F	LM211D
LM211T	LM211H
LM219D	LM219D

Signetics	AMD
LM219H	LM219H
LM239F	LM239D
LM308AF	LM308AD
LM308AT	LM308AH
LM308F	LM308D
LM308T	LM308H
LM308V	LM308N
LM311F	LM311D
LM311T	LM311H
LM311V	LM311N
LM319A	LM319N
LM319D	LM319D
LM319T	LM319H
LM339A	LM339N
LM339F	LM339D
MC1408-6F	AM1408L6
MC1408-6N	AM1408N6
MC1408-7F	AM1408L7
MC1408-7N	AM1408N7
MC1408-8F	AM1408L8
MC1408-8N	AM1408N8
MC1508-8F	AM1508L8
NE5007F	DAC-08CQ
NE5007N	DAC-08CN
NE5008F	DAC-08EQ

Signetics	AMD
NE5008N	DAC-08EN
NE5009F	DAC-08HQ
NE5009N	DAC-08HN
SE5008F	DAC-08Q
SE5009F	DAC-08AQ

Siemens	AMD
TDA4700A	AM6301PC
TDA4700	AM6301DC

Silicon General	AMD
SG108AD	LM108AD
SG108AT	LM108AH
SG108D	LM108D
SG108T	LM108H
SG111T	LM111H
SG139D	LM139AD
SG308AT	LM308AH
SG308T	LM308H
SG311T	LM311H
SG339AD	LM339AD
SG339D	LM339D

Texas Instruments	AMD
SN52108AFA	LM108AF
SN52108AJA	LM108AD
SN52108AL	LM108AH
SN52108FA	LM108F
SN52108JA	LM108D
SN52108L	LM108H
SN52111FA	LM111F
SN52111J	LM111D
SN52111L	LM111H
SN52118FA	LM118F
SN52118JA	LM118D
SN52118L	LM118H
SN72308AJA	LM308AD
SN72308AL	LM308AH
SN72308JA	LM308D
SN72308L	LM308H
SN72311J	LM311D
SN72311L	LM311H
SN72318JA	LM318D
SN72318L	LM318H

Functionally Equivalent Only

Analog Devices	AMD
AD558	AM6080
AD570	AM6108
AD574A	AM6112
AD7524	AM6080
AD7574	AM6148

Fairchild	AMD
μA760	AM686

Harris	AMD
HA4950	AM686
HA5320	AM6420
HI5712	AM6112

National	AMD
ADC0820	AM6108
ADC1280	AM6112
DAC0832	AM6080
DAC1201	AM6012
DAC1220	AM6012
LM161	AM686

Plessey	AMD
SP9754	AM6688

PMI	AMD
CMP05	AM686
DAC808	AM6080
DAC888	AM6080
SMP10	AM6420

Signetics	AMD
NE5018	AM6080
NE5019	AM6080
NE5118	AM6080
NE5119	AM6080
NE5560	AM6301

Siemens	AMD
SDA5010	AM6606

Silicon General	AMD
SG3524	AM6301

Microprocessor Peripheral Conversion Products – Section II

Am6080

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

2

DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am8086 and the Am2900 Families
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current output
- Choice of 6 coding formats
- Fast settling current output −160ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift − ±5ppm/°C
- Wide range multiplying capability −2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- High speed data latch − 80ns min write time

GENERAL DESCRIPTION

The Am6080 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

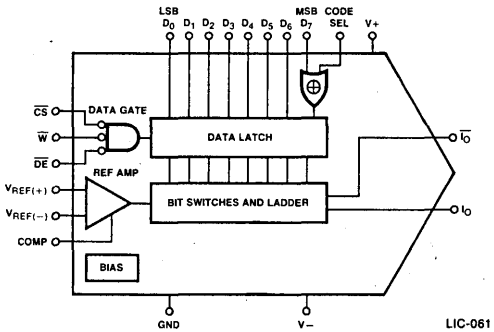
The converter allows a choice of 6 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A high voltage compliance, complementary current output pair is provided. The data latch is very high speed which makes the Am6080 capable of interfacing with high speed microprocessors.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6080 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

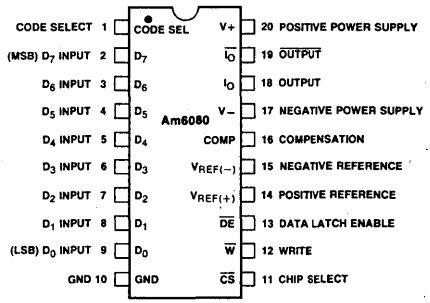
Applications for the Am6080 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

EQUIVALENT CIRCUIT



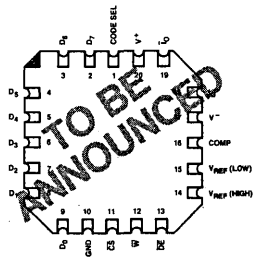
CONNECTION DIAGRAMS – Top Views

D-20-1, P-20-1



Leadless Chip-Pak

L-20-1



Pin 1 marked for orientation.

ORDERING INFORMATION*

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	−55 to +125°C	0.1%	AM6080ADM
Hermetic DIP	−55 to +125°C	0.19%	AM6080DM
Leadless	−55 to +125°C	0.1%	AM6080ALM**
Leadless	−55 to +125°C	0.19%	AM6080LM**
Hermetic DIP	0 to +70°C	0.1%	AM6080ADC
Hermetic DIP	0 to +70°C	0.19%	AM6080DC
Molded DIP	0 to +70°C	0.1%	AM6080APC
Molded DIP	0 to +70°C	0.19%	AM6080PC
Leadless	0 to +70°C	0.1%	AM6080ALC**
Leadless	0 to +70°C	0.19%	AM6080LC**

*Also available with burn-in processing. To order add suffix B to part number.

** Availability to be announced.

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6080ADM, Am6080DM Am6080ALM, Am6080LM	−55 to +125°C	Logic Inputs	−5 to +18V
Am6080ADC, Am6080DC Am6080APC, Am6080PC Am6080ALC, Am6080LC	0 to +70°C	Analog Current Outputs	−12 to +18V
		Reference Inputs (V_{14} V_{15})	V^- to V^+
Storage Temperature	−65 to +150°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for V_+ = +5V, V_- = −15V, I_{REF} = 0.5mA, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

				Am6080A			Am6080			
Parameter	**Description**		**Conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
	Resolution			8	8	8	8	8	8	bits
	Monotonicity			8	8	8	8	8	8	bits
D.N.L.	Differential Nonlinearity			–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity			–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current		V_{REF} = 10.000V $R_{14} = R_{15}$ = 20.000kΩ T_A = 25°C	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco			–	±5	±20	–	±10	±40	ppm/°C
				–	.0005	±.002	–	.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance			−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry		$I_{FS1} - \overline{I_{FS1}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current			–	0.01	1.0	–	0.01	2.0	μA
I_{RR}	Reference Current Range		V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
			V− = −15V	0	0.5	1.1	0	0.5	1.1	
V_{IL}	Logic Input Levels	Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}		Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current		V_{IN} = −5V to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing		V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{15}	Reference Bias Current			–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate		$R_{14(EQ)}$ = 800Ω CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity		V+ = +4.5V to +5.5V, V− = −15V	–	±0.0003	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$			V− = −13.5V to − 16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	
V+	Power Supply Range		I_{REF} = 0.5mA, V_{OUT} = 0V	4.5	–	18	4.5	–	18	Volts
V−				−18	–	−4.5	−18	–	−4.5	
I+	Power Supply Current		V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−				–	−7.4	−9.9	–	−7.4	−9.9	
I+			V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	
I−				–	−7.4	−9.9	–	−7.4	−9.9	
I+			V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	
I−				–	−7.4	−9.9	–	−7.4	−9.9	
P_D	Power Dissipation (Note 1)		V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
			V+ = +5V, V− = −15V	–	160	222	–	160	222	
			V+ = +15V, V− = −15V	–	258	369	–	258	369	

Note 1: Derate Hermetic DIP 10mW/°C above 100°C, Plastic package 6.8mW/°C, Leadless 10mW/°C above 100°C.

Am6080 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
D_0-D_7	D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.
$\overline{CS}$	Chip Select – This active low input signal enables the Am6080. Writing into the data latch occurs only when the device is selected.
$\overline{W}$	Write – This active low control signal enables the data latch when the $\overline{CS}$ and $\overline{DE}$ inputs are active.
$\overline{DE}$	Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.
CODE SEL	Code Select – When CODE SEL = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.
$V_{REF(+)}$ $V_{REF(-)}$	Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.
COMP	Compensation – Frequency compensating terminal for the reference amplifier.
I_O, $\overline{I_O}$	These are high impedance complementary current outputs. The sum of these currents is always equal to I_{FS}

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

X = Don't Care

CODE SELECT

CODE SEL	Function
0	MSB Inverted (Note 1)
1	MSB Non-inverted

Note 1. LSB balance current is added to the $\overline{I_O}$ output.

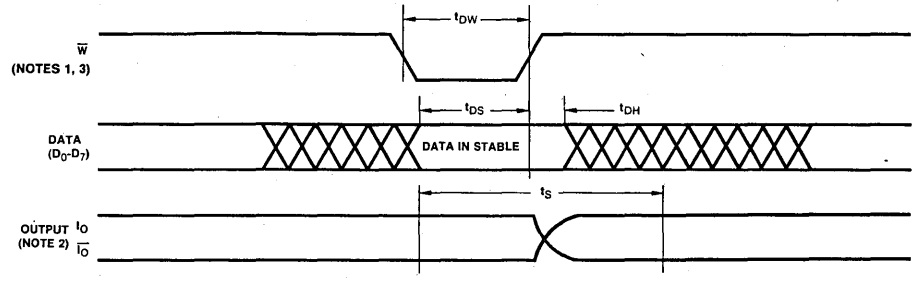
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Typ.	Max.	Military Temp. Grades Min.	Typ.	Max.	Unit
t_S	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to ±½LSB		160			160		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		80	160		80	160	ns
t_{PHL}		All bits switched			80	160		80	160	
t_{DH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{DS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns

Notes: 1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. The internal time delays from $\overline{CS}$, $\overline{W}$ and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM



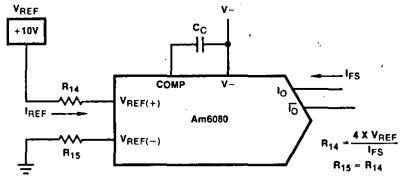
LIC-063

APPLICATION HINTS:

1. Reference current and reference resistor.

There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 2mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10\ Volt}{2mA} = 20K\Omega$$



LIC-064

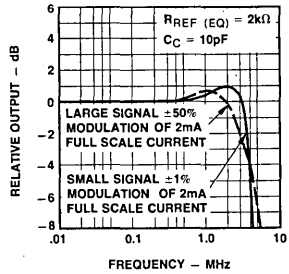
2. Reference amplifier compensation.

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

R_{REF} (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

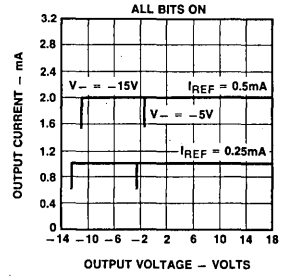
Reference Amplifier Frequency Response



A 0.01μF capacitor is recommended for the fixed reference operation.

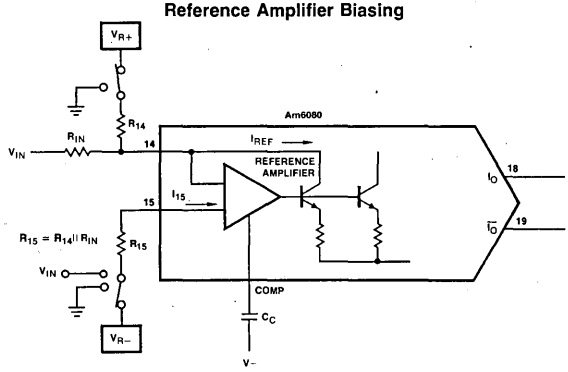
LIC-065

Output Voltage Compliance



LIC-066

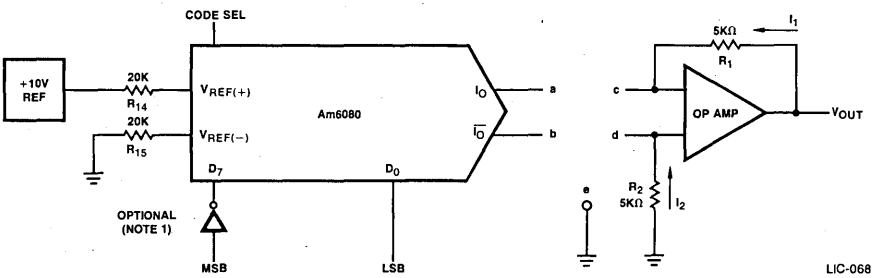
Reference Amplifier Biasing



LIC-067

Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least C = 5pFX $R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less and an additional resistor may be connected from pin 14 to ground to lower the impedance.



CODE FORMAT		CODE SEL	CONNECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	a-c b-e	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
				Positive full scale – LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
				Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
	Complementary binary: one polarity with complementary input code, true zero output.	1	a-e b-c	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
				Positive full scale – LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
				Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	a-c b-d	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
				Positive full scale – LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
				(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
				(–) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	–.040
				Negative full scale – LSB	X	0	0	0	0	0	0	0	1	.008	1.984	–9.880
				Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	–9.960
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented. (need inverter at D_7)	1 (Note 1)	a-c b-d	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
				Positive full scale – LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.980
				(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.040
				(–) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	–.040
				Negative full scale – LSB	X	1	0	0	0	0	0	0	1	.008	1.984	–9.880
				Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	–9.960
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	a-c b-d	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.920
				Positive full scale – LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.840
				+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.080
				Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.000
				– LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	–.080
				Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	–9.920
				Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	–10.000
	2's complement: offset half scale true zero output MSB complemented.	0	a-c b-d	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.920
				Positive full scale – LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.840
				+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.080
				Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.000
				–1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	–.080
				Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	–9.920
				Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	–10.000

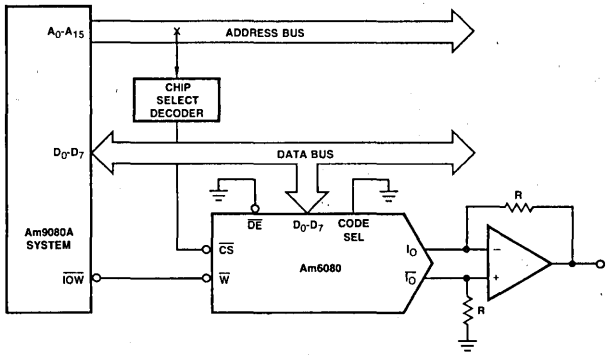
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of these features is desired for this code.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM

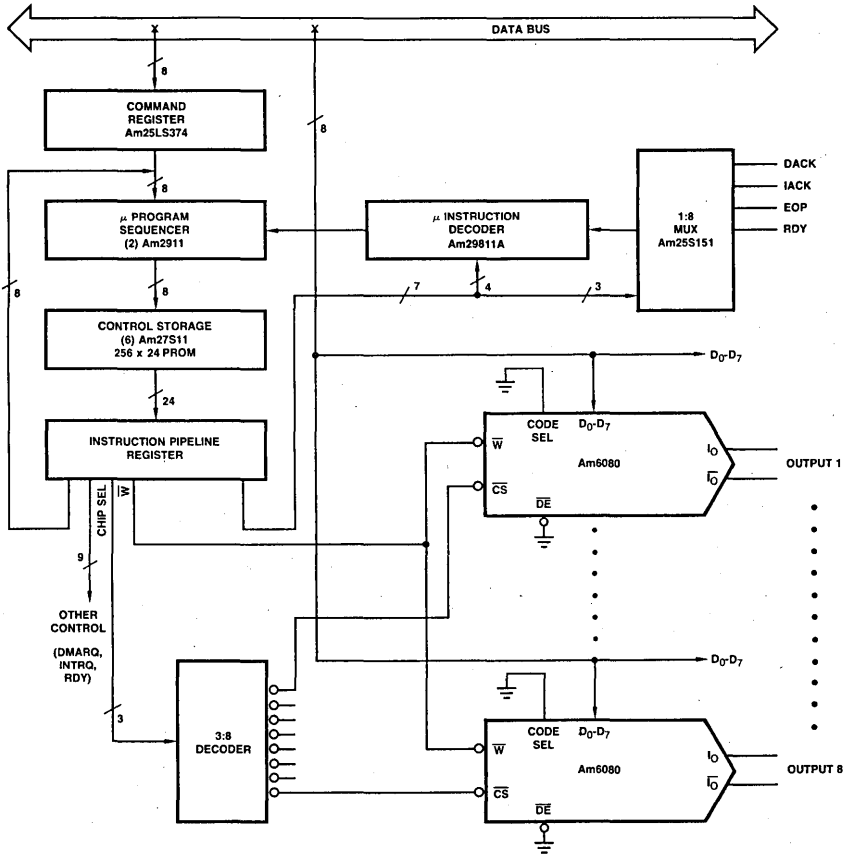


WRITING DATA INTO THE Am6080 (2's Complement)

```
PORT 1          :EQU OOH OUTPUT PORT ADDRESS
MOV A, M        :GET DATA FROM MEMORY
OUT 0 PORT1     :SEND DATA
```

LIC-069

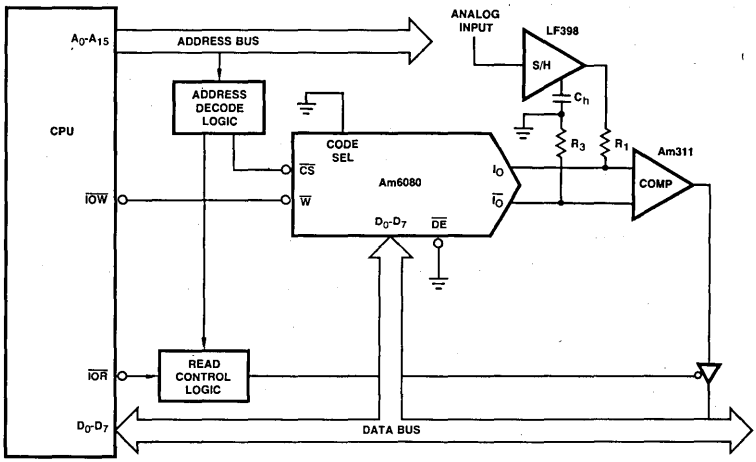
Am2900 DATA SYSTEM: MULTIPLE ANALOG INPUTS



LIC-070

SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL CONVERTER UNDER SOFTWARE CONTROL



LIC-071

Am9080A SOFTWARE FOR A/D CONVERSION USING Am6080.

```
SEQ     SOURCE STATEMENT                                SEQ     SOURCE STATEMENT
 0 PORT1    EQU 00H     ;6080 A/O PORT ADDRESS          13      IN PORT3    ;INPUT FROM COMP
 1 PORT3    EQU 02H     ;COMPARATOR ADDRESS             14      CRA A       ;SET SIGN FLAG
 2          ORG 3E50H                                   15      JM NEXT     ;IF SMALLER GO TO NEXT BIT
 3 START:   LXI SP,STAKS-16 ;INITIAL STAKS POINTER      16      MOV D,E     ;SAVE RESULT .
 4 SAMPLE:  CALL ADCON  ;CALL A/D CONVERSATION          17 NEXT:  MOV A,B     ;GET NEXT TRIAL BIT
 5          JMP SAMPLE  ;NEXT SAMPLE                    18      RAR         ;SHIFT RIGHT ONCE
 6 ADCON:   XRA A       ;CLEAR ACC                      19      RC          ;RETURN ON CARRY
 7          MOV D,A     ;CLEAR D REG                    20      MOV B,A     ;STORE TEST BIT
 8          STC         ;SET CARRY                      21      ADD D       ;ACCUMULATE RESULT
 9          RAR         ;SET BIT 7 TO 1                 22      JMP LOOP    ;TRY NEXT BIT
10          MOV B,A     ;STORE TEST BIT AT B REGISTER   23 STAKS:  DS 16
11 LOOP:    MOV E,A     ;STORE TEST WORD                24      END START
12          OUT PORT1   ;OUTPUT TO A/D
```

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

Signal Processing

CRT Displays
IF Gain Control
8 x 8 Digital Multiplication
Line Driver

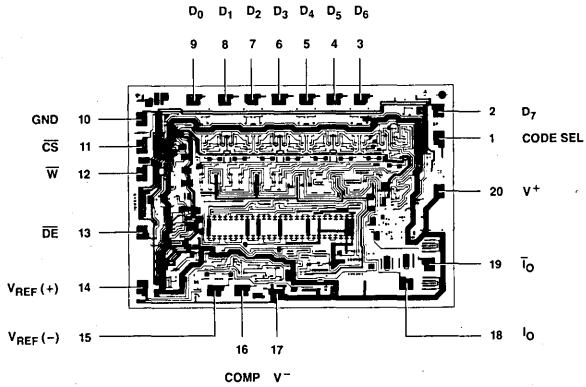
A/D Converters

Ratiometric ADC
Differential Input ADC
Microprocessor Controlled ADC

D/A Converters

Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.083" X 0.121"

Am6081

Microprocessor System Compatible 8-Bit High Speed Multiplying D/A Converter

2

DISTINCTIVE CHARACTERISTICS

- 8-Bit D/A with 8-Bit input data latch
- Compatible with most popular microprocessors including the Am8086 and the Am2900 Families
- Write, Chip Select and Data Enable logic on chip
- DAC appears as memory location to microprocessor
- MSB inversion under logic control
- Differential current outputs
- Output current mode multiplexer with logic selection
- 2-Bit status latch for output select and code select
- Choice of 8 coding formats
- Fast settling current output – 200ns
- Nonlinearity to ±0.1% max over temperature range
- Full scale current pre-matched to ±1 LSB
- High output impedance and voltage compliance
- Low full scale current drift – ±5ppm/°C
- Wide range multiplying capability –2.0MHz bandwidth
- Direct interface to TTL, CMOS, NMOS
- Output range selection with on chip multiplexer
- High speed data latch – 80ns min write time

GENERAL DESCRIPTION

The Am6081 is a monolithic 8-bit multiplying Digital-to-Analog converter with an 8-bit data latch, a 2-bit status latch, chip select and other control signal lines which allow direct interface with microprocessor buses.

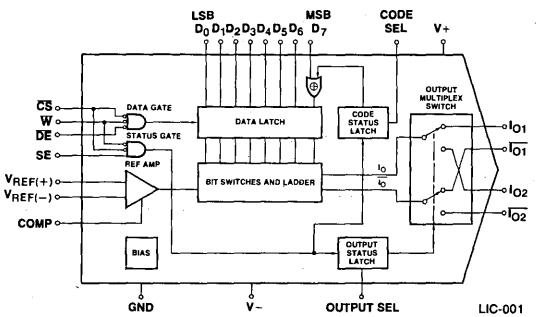
The converter allows a choice of 8 different coding formats. The most significant bit (D_7) can be inverted or non-inverted under the control of the code select input. The code control also provides a zero differential current output for 2's complement coding. A pair of high voltage compliance, dual complementary current output channels is provided and is selected by the output status command. The output multiplexer also allows analog bus connection of several converters, range or output load selection, and time-shared operation between D/A and A/D functions. The data and status latches are high speed which makes the Am6081 capable of interfacing with high speed microprocessors. The DE and SE control signals allow the data and status latches to be updated individually or simultaneously.

Monotonic multiplying performance is maintained over a more than 40 to 1 reference current range. Matching within ±1 LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The Am6081 guarantees full 8-bit monotonicity. Nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the full power supply voltage and temperature range.

Applications for the Am6081 include microprocessor compatible data acquisition systems and data distribution systems, 8-bit A/D converters, servo-motor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers and high speed modems.

EQUIVALENT CIRCUIT

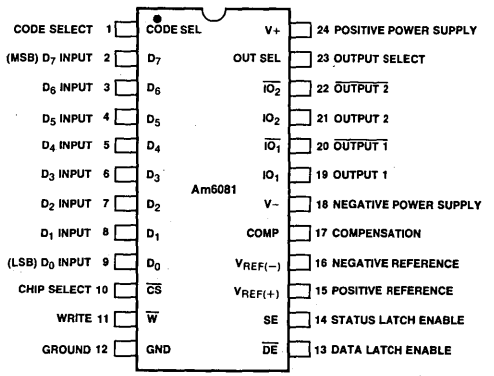


ORDERING INFORMATION*

Package Type	Temperature Range	Nonlinearity	Order Number
Hermetic DIP	–55°C to +125°C	±.1% ±.19%	AM6081ADM AM6081DM
Hermetic DIP	0°C to +70°C	±.1% ±.19%	AM6081ADC AM6081DC
Molded DIP	0°C to +70°C	±.1% ±.19%	AM6081APC AM6081PC

*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAM
Top View
D-24-1, P-24-1



Note: Pin 1 is marked for orientation. LIC-002

Am6081 FUNCTIONAL PIN DESCRIPTION

Symbol **Function**

$\overline{CS}$ Chip Select – This active low input signal enables the Am6081. Writing into the data or status latches occurs only when the device is selected.

$\overline{DE}$ Data Latch Enable – This active low input is used to enable the data latch. The $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ must be active in order to write into the data latch.

SE Status Latch Enable – This active high input is used to enable the status latches. The $\overline{CS}$, SE, and $\overline{W}$ must be active in order to write into the status latches.

$\overline{W}$ Write – This active low control signal enables the data and status latches when the $\overline{CS}$, $\overline{DE}$, and SE inputs are active.

D_0-D_7 D_0-D_7 are the input bits 1-8 to the input data latch. Data is transferred to the data latch when $\overline{CS}$, $\overline{DE}$, and $\overline{W}$ are active and is latched when any of the enable signals go inactive.

CODE SEL Code Select – Input to the CODE SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When CODE SEL latch = 0, the MSB (D_7) is inverted and 1 LSB balance current is added to the $\overline{I_O}$ output.

OUT SEL Output Select – Input to the OUT SEL latch. The latch is transparent when $\overline{CS}$, SE and $\overline{W}$ are active and is latched when any of the above signals go inactive. When the OUT SEL latch is low, the channel 1 output pair (I_{O1}, $\overline{I_{O1}}$) is selected. When the OUT SEL latch is high, the channel 2 output pair (I_{O2}, $\overline{I_{O2}}$) is selected.

$V_{REF(+)}$ $V_{REF(-)}$ Positive and negative reference voltage to the reference bias amplifier. These differential inputs allow the use of positive, negative and bipolar references.

COMP Compensation – Frequency compensating terminal for the reference amplifier.

I_{O1}, $\overline{I_{O1}}$ I_{O2}, $\overline{I_{O2}}$ These high impedance current output pairs are selected by the output select latch. I_{O1} and I_{O2} are true outputs and $\overline{I_{O1}}$ and $\overline{I_{O2}}$ are complementary outputs.

FUNCTION TABLES

DATA LATCH CONTROL

$\overline{CS}$	$\overline{W}$	$\overline{DE}$	Data Latch
0	0	0	Transparent
X	X	1	Latched
X	1	X	Latched
1	X	X	Latched

STATUS LATCH CONTROL

$\overline{CS}$	$\overline{W}$	SE	CODE SEL and OUT SEL Latch
0	0	1	Transparent
X	X	0	Latched
X	1	X	Latched
1	X	X	Latched

CODE SELECT AND OUTPUT SELECT

CODE SEL	OUT SEL	Function
0	–	MSB Inverted (Note 1)
1	–	MSB Non-inverted
–	0	Output Channel 1
–	1	Output Channel 2

X = Don't Care

Note 1. 1 LSB balance current is added to the $\overline{I_O}$ output.

MAXIMUM RATINGS

Operating Temperature		Power Supply Voltage	±18V
Am6081ADM, Am6081DM	−55°C to +125°C	Logic Inputs	−5V to +18V
Am6081ADC, Am6081DC Am6081APC, Am6081PC	0°C to +70°C	Analog Current Outputs	−12V to +18V
		Reference Inputs (V_{15}, V_{16})	V− to V+
Storage Temperature	−65°C to +150°C	Reference Input Differential Voltage (V_{15} to V_{16})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{15})	1.25mA

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	8 bits
Monotonicity	8 bits

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, over the operating temperature range unless otherwise specified. Output characteristics refer to all outputs.

Parameter	Description	Conditions	Am6081A Min.	Am6081A Typ.	Am6081A Max.	Am6081 Min.	Am6081 Typ.	Am6081 Max.	Unit
	Resolution	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
	Monotonicity	Straight coding/Sign Magnitude	8/9	8/9	8/9	8/9	8/9	8/9	bits
D.N.L.	Differential Nonlinearity		–	–	±0.19	–	–	±0.39	%FS
N.L.	Nonlinearity		–	–	±0.1	–	–	±0.19	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{15} = R_{16} = 20.000k\Omega$ $T_A = 25°C$	1.984	1.992	2.000	1.976	1.992	2.008	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		−10	–	+18	−10	–	+18	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS1} - \overline{I_{FS1}}$ or $I_{FS2} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{OSS}	Output Switch Symmetry	$I_{FS1} - I_{FS2}$ or $\overline{I_{FS1}} - \overline{I_{FS2}}$	–	±0.1	±1.0	–	±0.2	±2.0	μA
I_{ZS}	Zero Scale Current		–	0.01	1.0	–	0.01	2.0	μA
I_{DIS}	Output Disable Current	Output of mpx "Off" Channels	–	0.01	0.05	–	0.01	0.05	μA
I_{RR}	Reference Current Range	V− = −5V	0	0.5	0.55	0	0.5	0.55	mA
		V− = −15V	0	0.5	1.1	0	0.5	1.1	
V_{IL}	Logic Input Levels — Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current	$V_{IN} = -5V$ to $+18V$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{16}	Reference Bias Current		–	−0.5	−2.0	–	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{15(EQ)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5V to +5.5V, V− = −15V	–	±0.0005	±0.01	–	±0.0005	±0.01	%FS
$PSSI_{FS-}$		V− = −13.5V to − 16.5V, V+ = +5V	–	±0.0005	±0.01	–	±0.0005	±0.01	
V+	Power Supply Range	$I_{REF} = 0.5mA$, $V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−4.5	−18	–	−4.5	
I+	Power Supply Current	V+ = +5V, V− = −5V	–	9.8	14.7	–	9.8	14.7	mA
I−			–	−7.4	−9.9	–	−7.4	−9.9	
I+		V+ = +5V, V− = −15V	–	9.8	14.7	–	9.8	14.7	
I−			–	−7.4	−9.9	–	−7.4	−9.9	
I+		V+ = +15V, V− = −15V		9.8	14.7	–	9.8	14.7	
I−			–	−7.4	−9.9	–	−7.4	−9.9	
P_D	Power Dissipation	V+ = +5V, V− = −5V	–	86	123	–	86	123	mW
		V+ = +5V, V− = −15V	–	160	222	–	160	222	
		V+ = +15V, V− = −15V	–	258	369	–	258	369	

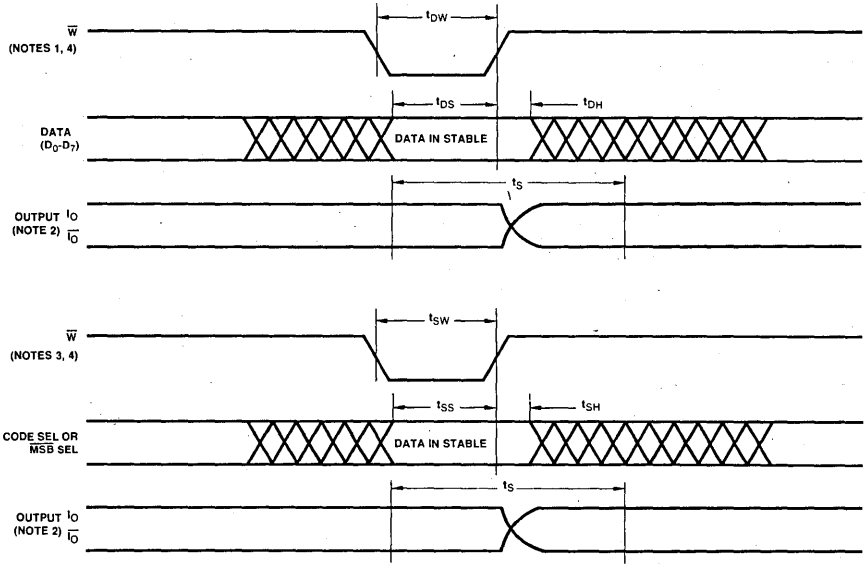
Am6081
AC CHARACTERISTICS

$V_+ = +5V$, $V_- = -15V$, $I_{REF} = 0.5mA$, $R_L < 500\Omega$, $C_L < 15pF$ over the operating temperature range unless otherwise specified

Parameter	Description		Conditions	Commercial Temp. Grades Min.	Typ.	Max.	Military Temp. Grades Min.	Typ.	Max.	Unit
t_S	Settling Time, All Bits Switched		$T_A = 25°C$ Settling to ±½LSB		200			200		ns
t_{PLH}	Propagation Delay	Each bit	$T_A = 25°C$ 50% to 50%		90	180		90	180	ns
t_{PHL}		All bits switched			90	180		90	180	
t_{OS}	Output Switch Settling Time		$T_A = 25°C$ to ±1/2LSB of I_{FS}		250			250		ns
t_{OP}	Output Switch Propagation Delay		$T_A = 25°C$, 50% to 50%		150	300		150	300	ns
t_{DH}	Data Hold Time		See timing diagram	10	−30		10	−30		ns
t_{DS}	Data Set Up Time		See timing diagram	80	35		100	35		ns
t_{DW}	Data Write Time		See timing diagram	80	35		100	35		ns
t_{SH}	Status Hold Time		See timing diagram	10	−70		10	−70		ns
t_{SS}	Status Set Up Time		See timing diagram	200	100		230	100		ns
t_{SW}	Status Write Time		See timing diagram	200	100		230	100		ns

Notes:
1. t_{DW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low, and $\overline{DE}$ low. All three signals must be low to enable the latch. Any signal going inactive latches the data.
2. t_S is measured with the latches open from the time the data becomes stable on the inputs to the time when the outputs are settled to within ±1/2 LSB. All bits switched on or off.
3. t_{SW} is the overlap of $\overline{W}$ low, $\overline{CS}$ low and SE high, all three signals must be active to enable the latch and any signal going inactive will latch the data.
4. The internal time delays from $\overline{CS}$, $\overline{W}$, SE and $\overline{DE}$ inputs to the enabling of the latches are all equal.

TIMING DIAGRAM



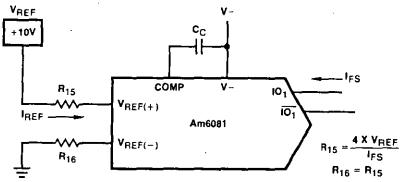
LIC-003

APPLICATION HINTS

1. Reference current and reference resistor

There is a 1 to 4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 2mA$, the value of the R_{15} is:

$$R_{15} = \frac{4 \times 10\ Volt}{2mA} = 20K\Omega$$



LIC-004

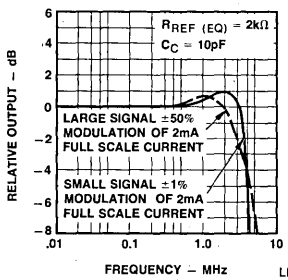
2. Reference amplifier compensation

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on R_{15}. The minimum values to maximize bandwidth without oscillation are as follows:

Table 2
Compensation Capacitor
(I_{FS} = 2mA, I_{REF} = 0.5mA)

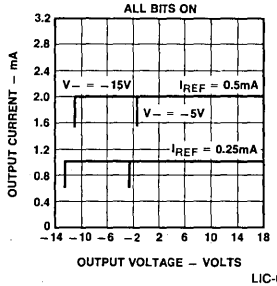
R_{REF} (kΩ)	C_C (pF)
20	100
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response



LIC-005

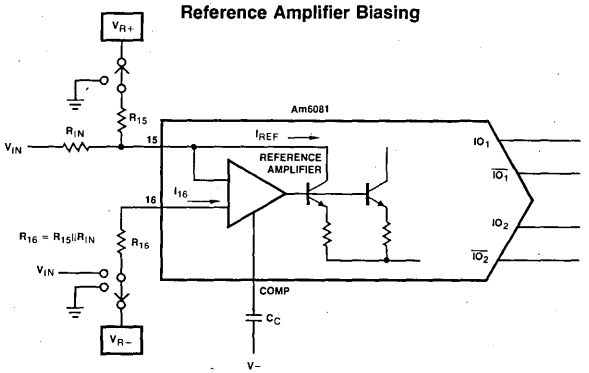
Output Voltage Compliance



LIC-006

A 0.01μF capacitor is recommended for the fixed reference operation.

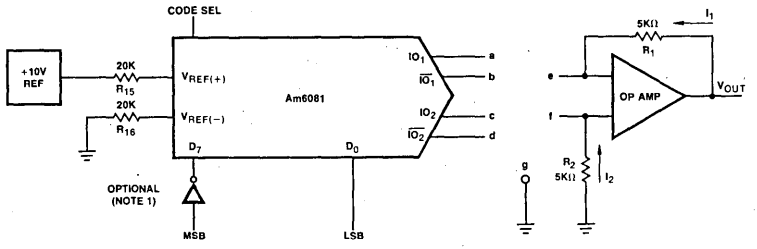
Reference Amplifier Biasing



LIC-007

Reference Configuration	R_{15}	R_{16}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{15}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{15}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{15}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{15}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $C = 5pF \times R_{15(EQ)}$ (in kΩ). For $R_{15} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{15} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 15 should be 800Ω or less and an additional resistor may be connected from pin 15 to ground to lower the impedance.



Note: Connect all unused outputs to ground.

LIC-008

CODE FORMAT		CODE SEL	OUT SEL	CON-NECTIONS	OUTPUT SCALE	OUT SEL	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	I_1 (mA)	I_2 (mA)	V_{OUT}
UNIPOLAR	Straight binary: one polarity with true input code, true zero output.	1	0	a-e b-g	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	0	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	0	9.920
					Zero scale	X	0	0	0	0	0	0	0	0	.000	0	.000
			1	c-e d-g													
	Complementary binary: one polarity with complementary input code, true zero output.	1	0	a-g b-e	Positive full scale	X	0	0	0	0	0	0	0	0	1.992	0	9.960
					Positive full scale − LSB	X	0	0	0	0	0	0	0	1	1.984	0	9.920
					Zero scale	X	1	1	1	1	1	1	1	1	.000	0	.000
			1	c-g d-e													
SIGNED MAGNITUDE	Signed magnitude binary: 8 bits + sign reflected code, overlapping true zero output.	1		a-e c-f	Positive full scale	1	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	1	1	1	1	1	1	1	1	0	1.984	.000	9.920
					(+) Zero scale	1	0	0	0	0	0	0	0	0	.000	.000	.000
					(−) Zero scale	0	0	0	0	0	0	0	0	0	.000	.000	.000
					Negative full scale − LSB	0	1	1	1	1	1	1	1	0	.000	1.984	−9.920
					Negative full scale	0	1	1	1	1	1	1	1	1	.000	1.992	−9.960
	Complementary signed magnitude: 8 bits + sign complementary reflected code, overlapping true zero output.	1		b-e d-f	Positive full scale	1	0	0	0	0	0	0	0	0	1.992	.000	9.960
					Positive full scale − LSB	1	0	0	0	0	0	0	0	1	1.984	.000	9.920
					(+) Zero scale	1	1	1	1	1	1	1	1	1	.000	.000	.000
					(−) Zero scale	0	1	1	1	1	1	1	1	1	.000	.000	.000
					Negative full scale − LSB	0	0	0	0	0	0	0	0	1	.000	1.984	−9.920
					Negative full scale	0	0	0	0	0	0	0	0	0	.000	1.992	−9.960
SYMMETRICAL OFFSET	Straight offset binary: offset half scale, symmetrical about zero, no true zero output.	1	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.008	9.880
					(+) Zero scale	X	1	0	0	0	0	0	0	0	1.000	.992	.040
					(−) Zero scale	X	0	1	1	1	1	1	1	1	.992	1.000	−.040
					Negative full scale − LSB	X	0	0	0	0	0	0	0	1	.008	1.984	−9.880
					Negative full scale	X	0	0	0	0	0	0	0	0	.000	1.992	−9.960
			1	c-e d-f													
	1's complement: offset half scale, symmetrical about zero, no true zero output MSB complemented. (need inverter at D_7)	1 (Note 1)	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.000	9.960
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.008	9.98
					(+) Zero scale	X	0	0	0	0	0	0	0	0	1.000	.992	.04
					(−) Zero scale	X	1	1	1	1	1	1	1	1	.992	1.000	−.04
					Negative full scale − LSB	X	1	0	0	0	0	0	0	1	.008	1.984	−9.88
					Negative full scale	X	1	0	0	0	0	0	0	0	.000	1.992	−9.96
			1	c-e d-f													
OFFSET WITH TRUE ZERO	Offset binary: offset half scale, true zero output MSB complemented remainder add to I_O. (need inverter at D_7)	0 (Note 1)	0	a-e b-f	Positive full scale	X	1	1	1	1	1	1	1	1	1.992	.008	9.92
					Positive full scale − LSB	X	1	1	1	1	1	1	1	0	1.984	.016	9.84
					+ LSB	X	1	0	0	0	0	0	0	1	1.008	.992	.08
					Zero scale	X	1	0	0	0	0	0	0	0	1.000	1.000	.00
					− LSB	X	0	1	1	1	1	1	1	1	1.992	1.008	−.08
					Negative full scale + LSB	X	0	0	0	0	0	0	0	1	.008	1.992	−9.92
					Negative full scale	X	0	0	0	0	0	0	0	0	.000	2.000	−10.00
			1	c-e d-f													
	2's complement: offset half scale true zero output MSB complemented.	0	0	a-e b-f	Positive full scale	X	0	1	1	1	1	1	1	1	1.992	.008	9.92
					Positive full scale − LSB	X	0	1	1	1	1	1	1	0	1.984	.016	9.84
					+1 LSB	X	0	0	0	0	0	0	0	1	1.008	.992	.08
					Zero scale	X	0	0	0	0	0	0	0	0	1.000	1.000	.00
					−1 LSB	X	1	1	1	1	1	1	1	1	.992	1.008	−.08
					Negative full scale + LSB	X	1	0	0	0	0	0	0	1	.008	1.992	−9.92
					Negative full scale	X	1	0	0	0	0	0	0	0	.000	2.000	−10.00
			1	c-e d-f													

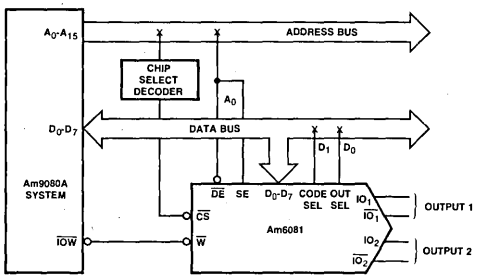
Note 1: An external inverter is necessary since the code select inverts the MSB and adds a 1 LSB balance current to $\overline{I_O}$. Only one of the two features is desired for these codes.

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.
2. The sign on any of the sign-magnitude codes may be changed by reversing the output terminal pair.
3. The polarity of the unipolar codes may be changed by driving the opposite side of the balanced load.

SYSTEM APPLICATIONS

Am9080A DATA SYSTEM: SEPARATE UPDATE OF DATA AND STATUS



SELECT OUTPUT PORT 1

```
MVI A, 2    : SET STATUS TO 0 (SELECT OUTPUT 1)
OUT 1       : SEND STATUS
MOV A, M    : GET DATA FROM MEMORY
OUT 0       : SEND DATA
```

SELECT OUTPUT PORT 2

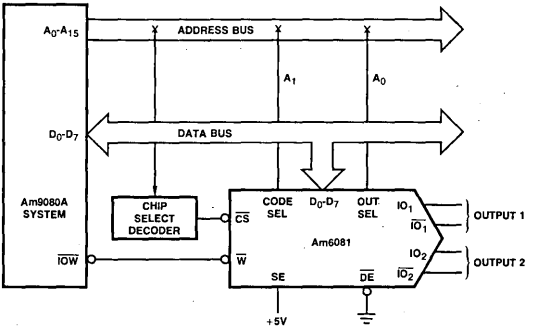
```
MVI A, 3    : SET STATUS TO 1 (SELECT OUTPUT 2)
OUT 1       : SEND STATUS
MOV A,M     : GET DATA FROM MEMORY
OUT 0       : SEND DATA
```

SELECT OUTPUT PORT 2 AND 2's COMPLEMENT CODE

```
MVI A, 1    : SET STATUS TO 3 (OUTPUT 2, MSB COMP)
OUT 1       : SEND STATUS
MOV A, M    : GET DATA FROM MEMORY
OUT 0       : SEND DATA
```

LIC-009

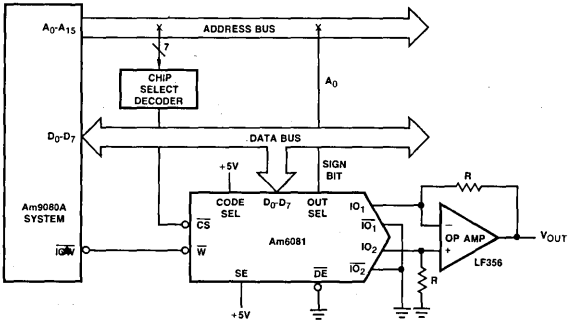
Am9080A DATA SYSTEM: SIMULTANEOUS UPDATE OF DATA AND STATUS




```
MOV A, M    : GET DATA IN ACCUMULATOR
OUT 0       : OUTPUT DATA TO PORT 1, 2'S COMPLEMENT
OUT 1       : OUTPUT DATA TO PORT 2, 2'S COMPLEMENT
OUT 2       : OUTPUT DATA TO PORT 1, STRAIGHT BINARY
OUT 3       : OUTPUT DATA TO PORT 2, STRAIGHT BINARY
```

LIC-010

Am9080A DATA SYSTEM: 8-BIT PLUS SIGN CONVERSION

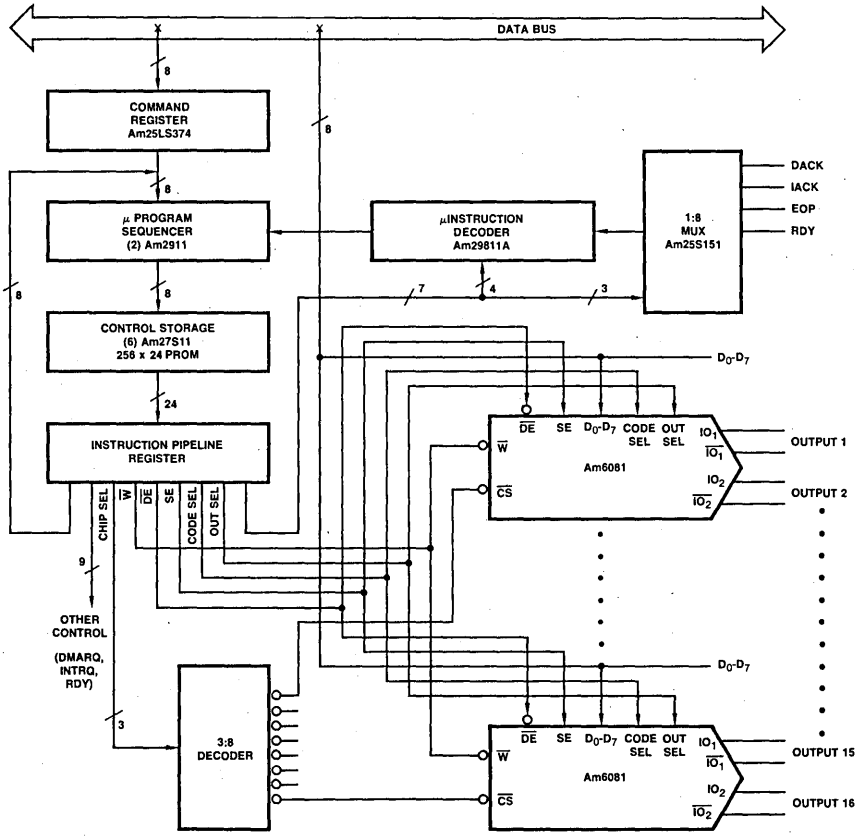



```
MOV A, M    : LOAD MAGNITUDE (8-BITS)
OUT 0       : SEND POSITIVE OUTPUT
OUT 1       : SEND NEGATIVE OUTPUT
```

LIC-011

SYSTEM APPLICATIONS (Cont.)

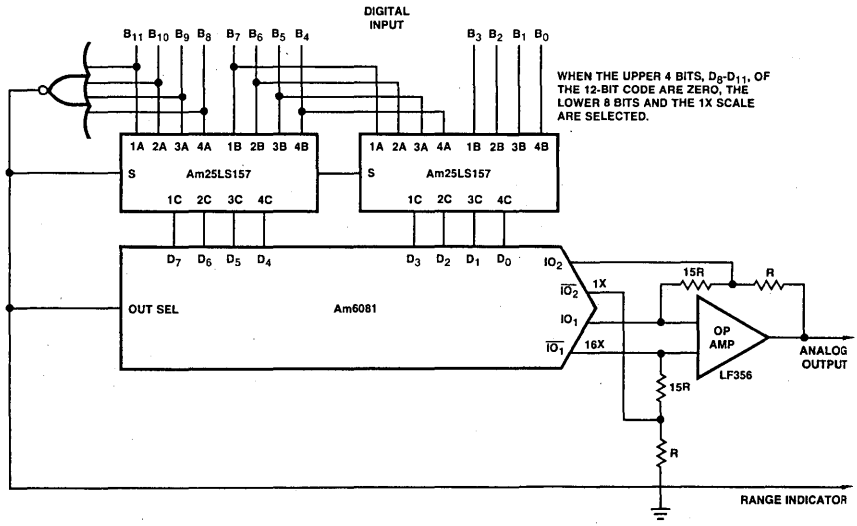
Am2900 DATA SYSTEM: MULTIPLE ANALOG OUTPUTS



LIC-01

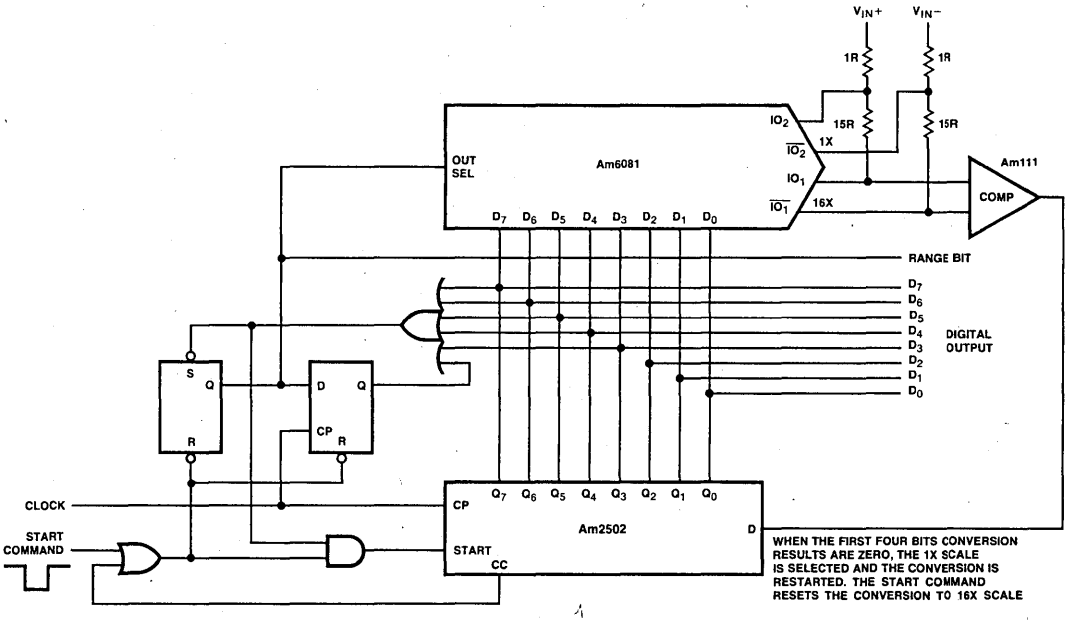
SYSTEM APPLICATIONS (Cont.)

D/A CONVERSION WITH 12-BIT DYNAMIC RANGE



LIC-013

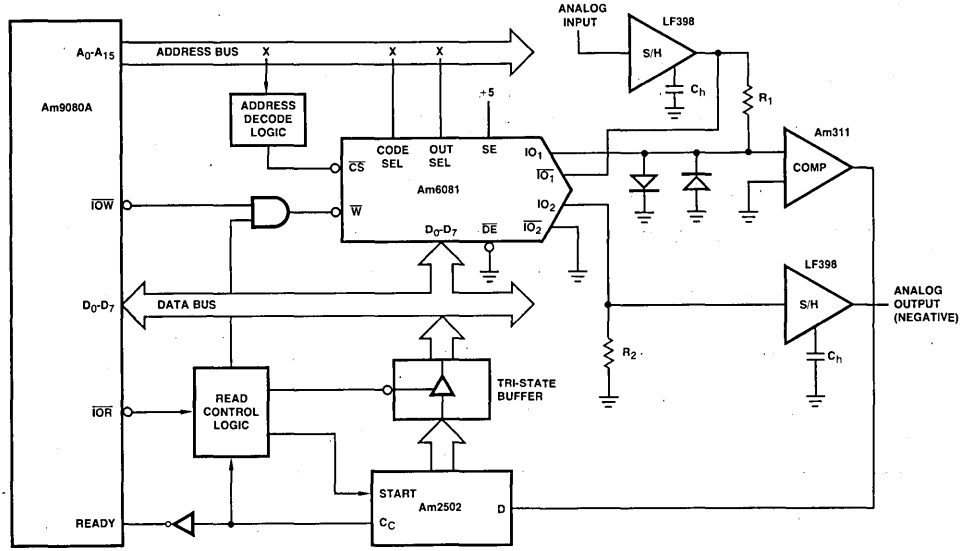
A/D CONVERSION WITH AUTO RANGING AND DIFFERENTIAL INPUT



LIC-014

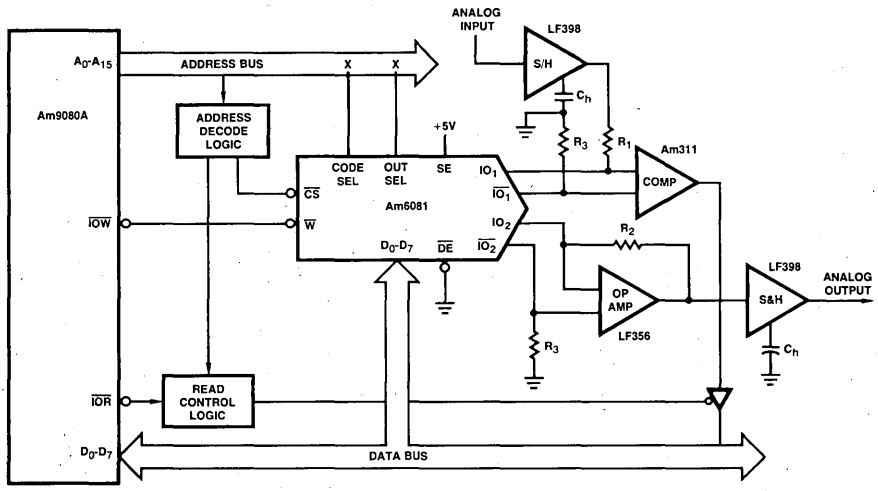
SYSTEM APPLICATIONS (Cont.)

ANALOG/DIGITAL TRANSCEIVER WITH HARDWARE CONTROLLED SUCCESSIVE APPROXIMATION A/D CONVERSION



LIC-015

ANALOG/DIGITAL TRANSCEIVER WITH SOFTWARE CONTROLLED A/D CONVERSION



LIC-016

Am9080A SOFTWARE FOR A/D AND D/A CONVERSION USING Am6081

```
SEQ     SOURCE STATEMENT                          SEQ     SOURCE STATEMENT
0 PORT1 EQU 00H                                   18      CMA
1 PORT3 EQU 02H                                   19      CRA A          ;SET SIGN FLAG
2 PORT2 EQU 01H                                   20      JM NEXT        ;IF SMALLER GO TO NEXT BIT
3       ORG 3E50H                                 21      MOV D,E        ;SAVE RESULT
4 START: LXI SP,STAKS-16  ;INITIAL STAKS POINTER  22 NEXT: MOV A,B      ;GET NEXT TRIAL BIT
5 SAMPLE: CALL ADCON      ;CALL A/D CONVERSATION  23      RAR            ;SHIFT RIGHT ONCE
6       CMA                                       24      RC             ;RETURN ON CARRY
7       CALL DACON        ;CALL D/A CONVERSION    25      MOV B,A        ;STORE TEST BIT
8       JMP SAMPLE        ;NEXT SAMPLE            26      ADD D          ;ACCUMULATE RESULT
9 ADCON: XRA A            :CLEAR ACC              27      JMP LOOP       ;TRY NEXT BIT
10      MOV D,A           ;CLEAR D REG            28 DACON: OUT PORT 2   ;OUTPUT TO D/A
11      STC               ;SET CARRY              29      MVI C,05H      ;LOAD C REG WITH TIME
12      RAR               ;SET BIT 7 TO 1         30      DCR C          ;TIME DELAY
13      MOV B,A           ;STORE TEST BIT AT B REGISTER 31  RZ           ;RETURN
14 LOOP: MOV E,A          ;STORE TEST WORD        32 FILT: RET
15      CMA                                       33 STAKS: DS 16
16      OUT PORT1         ;OUTPUT TO A/D          34      END START
17      IN PORT3          ;INPUT FROM COMP
```

ADVANCED MICRO DEVICES DATA CONVERSION PRODUCTS

Digital to Analog Converters

AmDAC-08 – 8-Bit High Speed Multiplying D/A Converter
Am1508/1408 – 8-Bit Multiplying D/A Converter
Am6070 – 8-Bit Companding D/A Converter for Control Systems (μ-law)
Am6072 – 8-Bit Companding D/A Converter for Telecommunications (μ-law)
Am6080 – 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
Am6081 – 8-Bit High Speed Multiplying D/A Converter System/Microprocessor Compatible
*Am6689 – 8-Bit, Ultra High Speed D/A Converter (ECL)
*Am6012 – 12-Bit High Speed Multiplying D/A Converter

Analog to Digital Converters

*Am6688 – 4-Bit Quantizer (Ultra High Speed A/D Converter)

Successive Approximation Registers

Am2502 – 8-Bit Successive Approximation Registers
Am2503 – 8-Bit Successive Approximation Registers
Am2504 – 12-Bit Successive Approximation Registers

Sample and Hold Amplifiers

LF198/398 –Monolithic Sample and Hold Amplifier
*Am6098 –Precision Sample and Hold Amplifier

Comparators

LM111/311 – Precision Voltage Comparator
LM119/319 – Dual Comparator
Am686 – High Speed Voltage Comparator

High Speed Operational Amplifiers

Am118/318 – High Speed Operational Amplifier
LF155/156/157 – JFET Input Operational Amplifiers
LF355/356/357 – JFET Input Operational Amplifiers

* To be announced.

APPLICATIONS

Instrumentation and Control

Data Acquisition
Data Distribution
Data Transceiver
Function Generation
Servo Controls
Programmable Power Supplies
Digital Zero Scale Calibration
Digital Full Scale Calibration
Digitally Controlled Offset Null

Signal Processing

CRT Displays
Floating Point Analog Processors
IF Gain Control
Four Quadrant Multiplexer
8 x 8 Digital Multiplication
Line Driver

A/D Converters

Ratiometric ADC
Differential Input ADC
Multiple Input Range ADC
Two Channel ADC
Microprocessor Controlled ADC

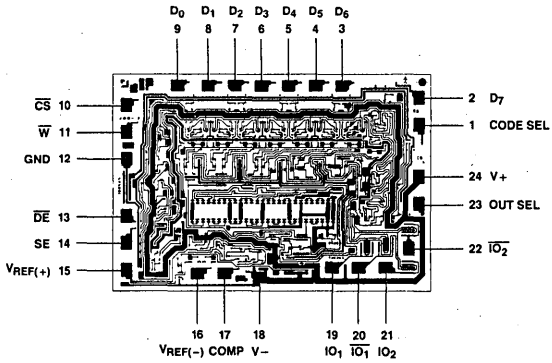
Audio

Music Distribution
Digitally Controlled Gain
Potentiometer Replacement
Digital Recording
Speech Digitizing

D/A Converters

Single Quadrant Multiplying DAC
Two Quadrant Multiplying DAC
Four Quadrant Multiplying DAC
Two Channel DAC
Multiple Output Range DAC

Metallization and Pad Layout



DIE SIZE: 0.083" X 0.121"

Am6082

Complete 12-Bit Microprocessor Compatible DAC

PRELIMINARY DATA

2

DISTINCTIVE CHARACTERISTICS

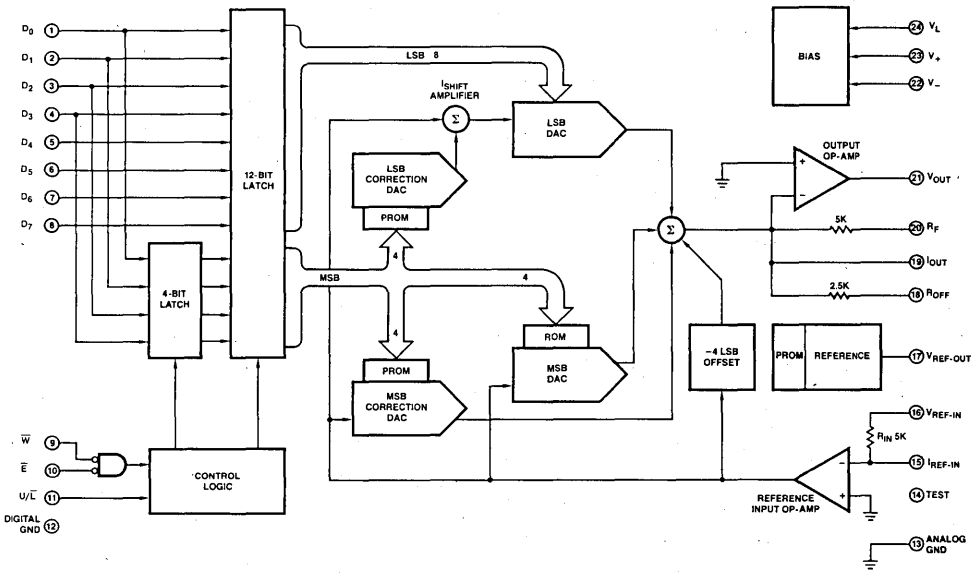
- True 12-bit absolute accuracy with no external adjustments
- Self-contained, no external components required
- Internal latches for easy interface to 8-bit buses
- Interfaces with 8-bit and 16-bit μPs
- Ultra fast data latch eliminates timing problems
- High-speed
  - 100ns settling time current output
  - 500ns settling time voltage output
- True 12-bit performance-monotonic with 12-bit DNL over temperature
- Output ranges: 0 to +10V, −5 to +5V

FUNCTIONAL DESCRIPTION

The Am6082 is a true monolithic 12-bit digital-to-analog converter that contains data latches, output op-amp, voltage reference, application resistors, and all trimming required for 12-bit absolute accuracy with no external components. The data latches and control circuitry allow the device to appear as a memory location to a microprocessor or computer system, while high-speed processing and design give 1/2 LSB voltage settling in less than 1μs.

The device is PROM-trimmed for offset, linearity, full-scale calibration and full-scale tempco at the factory.

BLOCK DIAGRAM



03590A-1

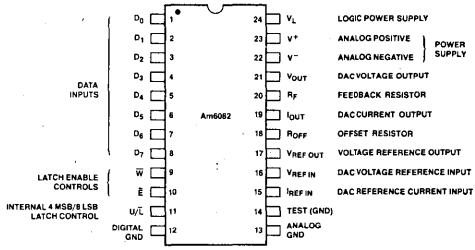
ORDERING INFORMATION

Order Number	Package Type	Temperature Range
Am6082DM	Hermetic DIP	−55 to +125°C
Am6082DC	Hermetic DIP	0 to 70°C
Am6082PC	Plastic	0 to 70°C

CONNECTION DIAGRAM — Top View

D-24-1

P-24-1



Note: Pin 1 is marked for orientation. 03590A-2

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 60sec)	300°C
Logic Supply Voltage (V_L pin)	−0.5 to +6.0V
Analog Positive Supply Voltage (V+ pin)	−0.5 to +16.5V
Analog Negative Supply Voltage (V− pin)	+0.5 to −16.5V
Analog Current Outputs (V_{OUT}, $V_{REF-OUT}$ pins)	±25mA
Digital, Status, and Analog Inputs (D_0-D_7, E, U/L, V_{REF-IN}, I_{REF-IN}, I_{OUT}, R_{OFF}, R_F pins)	±5mA

ELECTRICAL CHARACTERISTICS

($V+ = 15V \pm 5\%$, $V^- = -15V \pm 5\%$, $V_L = 5V \pm 5\%$, $T_A = 0$ to $+70°C$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
	Resolution/Monotonicity		12	12	12	Bits
DNL	Differential Nonlinearity	$T_A = 25°C$		1/2	1	LSB
NL	Nonlinearity	$T_A = 25°C$		±0.3	±1	LSB
	Zero Scale Error	$T_A = 25°C$		0.3	±1	LSB
	Full-Scale Gain Error	$T_A = 25°C$		0.3	±1	LSB
t_{IS}	Current Settling Time	To 1 LSB Output op-amp not used $R_L = 100\Omega$		100		ns
t_{VS}	Voltage Settling Time	To 1 LSB R_F applied to output op-amp		500		ns
t_{PHL}, t_{PLH}	Propagation Delay			35		ns
Reference						
V_{REF}	Reference Voltage	$I_{REF} = 0.5mA$		2.5		Volts
$\Delta V_{REF}/\Delta T_A$	Temperature Stability			0.08		LSB/°C
$\Delta V_{REF}/\Delta V_S$	Line Regulation			0.005		%/Volt
$\Delta V_{REF}/\Delta I_{REF}$	Load Regulation	$0.5mA \leq \Delta I_{REF} \leq 4mA$		0.1%		%/mA
I_{REF} max	Current Limit			15		mA
Output Op-Amp						
V_{OS}	Input Offset Voltage			±3		mV
$\Delta V_{OS}/\Delta T_A$	V_{OS} Tempco			4		µV/°C
A_V	Voltage Gain			15		V/mV
$\Delta V/\Delta t$	Slew Rate			70		V/µs
BW	3dB Bandwidth			13		MHz
V_{SW}	Output Voltage Swing	$R_L \geq 2K\Omega$		+12		Volts
				−6		
I_O	Output Current			±25		mA
Data Latches						
V_H	Input HIGH Voltage		2.0			Volts
V_L	Input LOW Voltage				0.8	Volts
I_{IH}	Input HIGH Current	$V_{IN} = 2.7V$		±2.0		µA
I_{IL}	Input LOW Current	$V_{IN} = 0.4V$		±2.0		µA
t_{DS}	Data Setup Time		20			ns
t_{DH}	Data Hold Time		0			ns
t_{PW}	Latch Enable Pulse Width		12			ns
t_{CS}	Control Setup Time		20			ns

ELECTRICAL CHARACTERISTICS (Cont.)

(V^+ = 15V ±5%, V^- = −15V ±5%, V_L = 5V ±5%, T_A = 0 to +70°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
General Characteristics						
I^+	Analog Positive Supply Current			4		mA
I^-	Analog Negative Supply Current				20	mA
I_{LS}	Logic Supply Current				35	mA
P_{DISS}	Power Dissipation				550	mW

FUNCTIONAL PIN DESCRIPTION

D_0-D_7 **Data Inputs**
LSBs 0 to 7 are loaded into the internal latches through D_0-D_7 when U/L = 0. MSBs 8 to 11 are loaded by lines D_0-D_3 when U/L = 1.

$\overline{W}, \overline{E}$ **Latch Enable Inputs**
Active low.

U/$\overline{L}$ **Controls Loading of Internal Latches**
A write into the four MSBs is done first, then a second write of eight LSBs causes all twelve internal latches to be loaded.

TEST The user should ground this pin, it is used for programming the DAC at the factory.

I_{OUT} **DAC Current Output**
Clamped to a diode voltage bidirectionally from analog ground.

V_{OUT} **DAC Voltage Output**
An internal feedback resistor must be connected around the op-amp to produce a voltage output.

R_F **A 5K Resistor to I_{OUT}**
When connected to V_{OUT} the output voltage varies 0 to 10V.

R_{OFF} **A 2.5K Resistor to I_{OUT}**
When connected to $V_{REF-OUT}$ it offsets the output by half scale.

$V_{REF-OUT}$ **An Internally Developed Voltage Reference**
Tempco optimized to compensate for the internal DAC.

V_{REF-IN} **DAC Reference Input**
2.5 volts in scales to 2.0mA output current.

I_{REF-IN} **DAC Current Reference Input**
0.5mA in scales to 2.0mA output current.

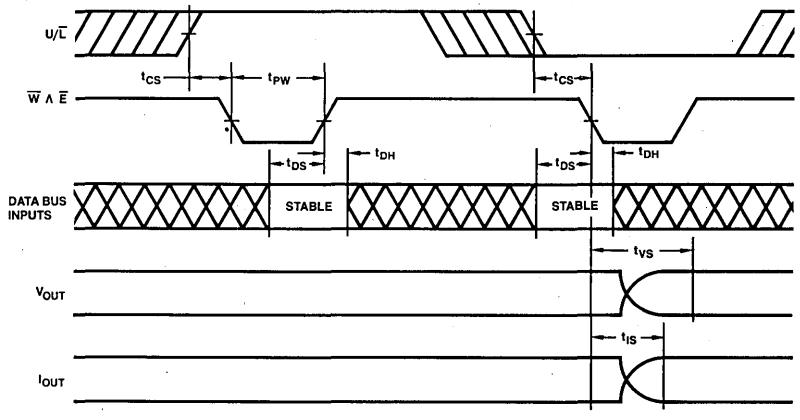
ANALOG GND **Analog Signal Ground Reference**
It should not be different from digital ground by more than ±100mV. Up to 3mA flows in this ground.

DIGITAL GND **Logic Supply Ground**

V+, V− 13 to 16 volts in magnitude, filtered.

V_L Should be 4.5 to 5.5 volts.

SWITCHING WAVEFORMS



03590A-3

THEORY OF OPERATION

The Am6082 is composed of two DACs, a MSB DAC with 15 equal value current segments each worth 1/16 of the full scale current, and an 8-bit binary LSB DAC. The upper 4 bits of data are routed to a ROM within the MSB DAC, which controls the number and physical distribution of the segment currents used. The 4 MSB bits are also used to set up a correction code on a correction DAC, which injects a compensating current into I_{OUT} to minimize output errors. In addition, the LSB DAC is PROM adjusted to interpolate accurately between adjacent MSB segment values.

Since an 8-bit data bus is used to transfer 12-bits of code, two write cycles are required. The four MSBs are written into the MSB latch using pins $D_0 - D_3$ as data inputs when controls $U/\overline{L}$, $\overline{W}$ and $\overline{E}$ are all LOW. The eight LSBs are loaded through pins $D_0 - D_7$ when $U/\overline{L}$ is HIGH and both $\overline{W}$ and $\overline{E}$ are LOW. The D/A output starts immediately on the second write.

The output op-amp is specifically designed for fast settling in the inverting mode. When the R_F feedback resistor is used, the op-amp functions as a current to voltage converter, converting the DAC output current to a voltage between 0 and 10V. R_{OFF} is included to allow a bipolar (−5 to +5V) output.

APPLICATIONS INFORMATION

The Am6082 is a monolithic high speed digital-to-analog converter, with a current settling time of 100ns and a voltage settling time of under 1μs to 0.01% of full scale. It contains an output op-amp, a precision voltage reference application resistors, it is trimmed for 12-bit absolute accuracy without the need for external components and allows easy interfacing to 8- and 16-bit microprocessors.

Unlike most conventional 12-bit DACs, which are laser trimmed, the Am6082 is PROM trimmed at the factory for linearity, voltage offset, full scale tempco and gain. The internal precision voltage reference and its tempco are also PROM trimmed. Since gain and offset are factory trimmed, no external adjustments are necessary.

REFERENCE INPUTS

An internal voltage reference is provided via the $V_{REF\ OUT}$ pin. However, the Am6082 may also use an external voltage or current reference through the $V_{REF\ IN}$ or $I_{REF\ IN}$ inputs respectively. $V_{REF\ IN}$ is connected to $I_{REF\ IN}$ through an internal 5K resistor. The internal reference is used by connecting $V_{REF\ OUT}$ (pin 17) to $V_{REF\ IN}$ (pin 16) to provide a 0.5mA reference current (see Figure 1).

VOLTAGE OUTPUTS

The Am6082 provides either a voltage or a current output. The current output may be taken directly from the I_{OUT} pin, however, if a voltage output is desired, the output op-amp is used with the on chip scale resistors to provide unipolar or bipolar outputs.

Unipolar Operation is shown in Figure 1a. To operate the Am6082 in the voltage output range of 0 to 10V, connect the voltage output of the op-amp V_{OUT} (pin 21) to the feedback resistor R_F (pin 20). The voltage reference output $V_{REF\ OUT}$ (pin 17) should be connected to the voltage reference input $V_{REF\ IN}$ (pin 16).

In Bipolar Operation, the Am6082 may be operated with a ±5V output by connecting the voltage reference output $V_{REF\ OUT}$ (pin 17) to both the reference voltage input $V_{REF\ IN}$ (pin 16) and to the offset resistor R_{OFF} (pin 18). See Figure 1b. Tie V_{OUT} and R_F together as before.

GROUNDING CONSIDERATIONS

Special attention should be paid to system grounding because digital signals can couple into the analog circuits and cause output errors. The Am6082 provides separate analog and digital ground pins which should not be connected together at the chip. As a rule, provide separate ground returns for analog and digital circuits and connect all grounds together at one point, preferably at the power supply. This will minimize interference from ground currents.

INTERFACING

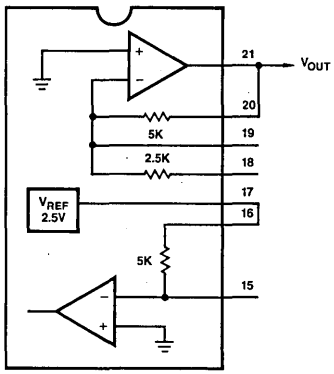
The Am6082 will interface with most microprocessors with a minimum of decoding and timing logic. In most cases, the chip enable control $\overline{E}$ may be driven from an address decoder and the write control $\overline{W}$ may be connected directly to a μP memory write or an I/O write pin (see Figure 2).

TWO'S COMPLEMENT NOTATION

The Am6082 may be operated with a two's complement input format. This is accomplished by inverting the most significant bit, as shown in Figure 3. The exclusive OR of the MSB and the $\overline{U}$/L control will give the correct result.

Figure 1.

a) Unipolar (0 to 10V Output) Operation



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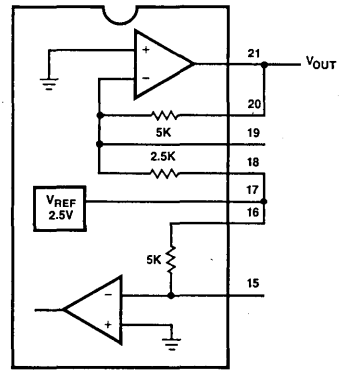
b) Bipolar (−5 to +5V Output) Operation



03590A-5

Figure 2. Microprocessor Interfacing

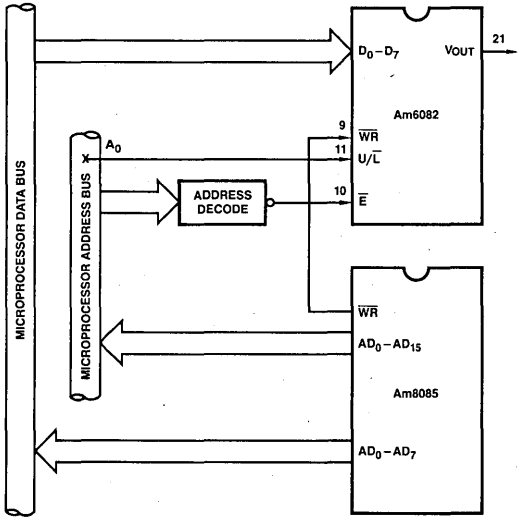


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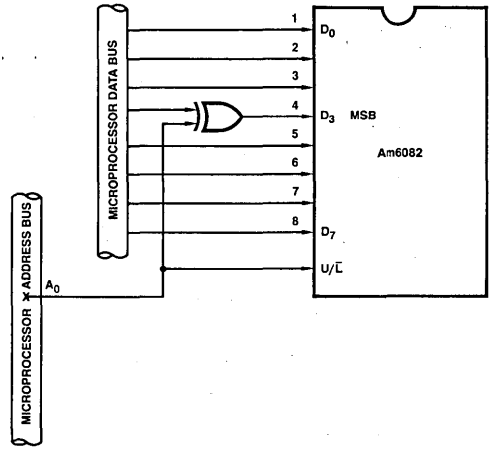
Figure 3. Two's Complement Operation



03590A-7

Am6108 • Am6148

Microprocessor Compatible 8-Bit A/D Converter

DISTINCTIVE CHARACTERISTICS

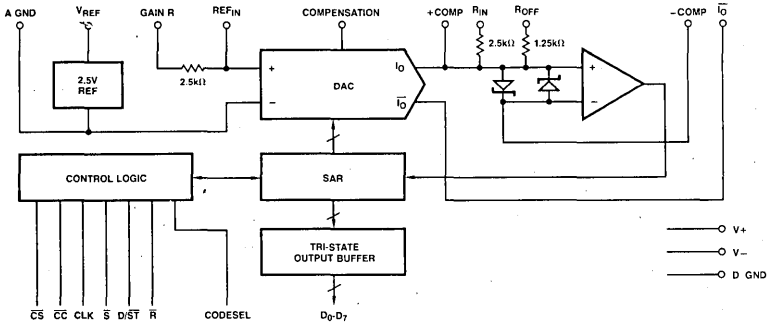
- 1μs conversion time
- Trimmed internal voltage reference
- 0.1% nonlinearity
- Ratiometric operation
- Low operating voltages
- Internal matched gain, reference and offset resistors
- Microprocessor compatible
- 3-state outputs
- Pin-programmable unipolar or bipolar two's complement conversion
- Conversion complete available as interrupt or as multiplexed output on data bus
- Available in slim, 24-pin, 0.3" and standard, 28-pin, 0.6" packages

FUNCTIONAL DESCRIPTION

The Am6108 and Am6148 are microprocessor-compatible, 8-bit, high-speed, analog-to-digital converters. They include a precision reference, DAC, comparator, SAR, scale resistors, 3-state output buffers and control logic. The Am6108 is available in a standard .600-inch-wide, 28-pin package, and the Am6148 is offered in a space-saving, .300-inch-wide, 24-pin package. The Am6108/Am6148 are capable of completing an 8-bit conversion in under one microsecond and can handle input voltage ranges of 0 to +10V, 0 to +5V, and ±5V without external components. With appropriate external resistors, the user can program the device to operate on other input signal ranges (2 or 3 precision resistors are required). Full 8-bit monotonic performance with no missing codes is guaranteed over temperature. Both devices have 3-state outputs for bus compatibility and a status output.

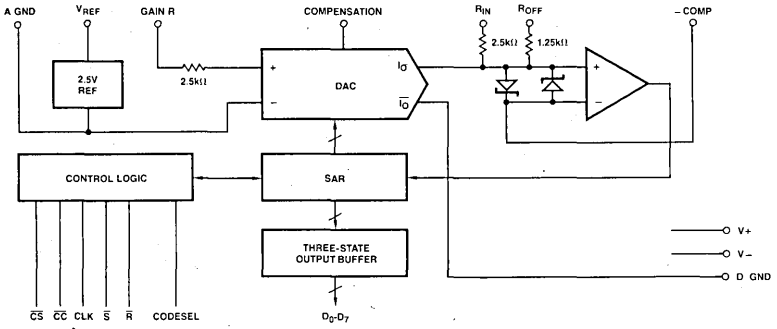
The Am6108/Am6148 are useful in microprocessor-based systems or can be used in a stand-alone mode. The conversion time is short enough to allow most microprocessors to accept data immediately after requesting a conversion. Applications include Analog I/O subsystems, process control and servo-control.

Am6108 EQUIVALENT CIRCUIT



ABI-092

Am6148 EQUIVALENT CIRCUIT



ABI-093

THEORY OF OPERATION

A conversion cycle in the Am6108/Am6148 begins by taking the $\overline{S}$ input low simultaneously with $\overline{CS}$ low and the CLK input low, this resets the Successive Approximation Register (SAR). When $\overline{S}$ is returned high, all bits of the SAR are ones with the exception of the MSB, which is set to a zero. The output of the SAR is fed to a DAC that converts it to a current. The current from the DAC output is then compared with the current generated by the analog input voltage. Based on this comparison, the SAR either keeps the MSB as a zero or resets it to a one before beginning the next approximation. This process of successive removal and testing continues until all bits have been tested. At that time the conversion complete, $\overline{CC}$, output goes low, and the Am6108/Am6148 is ready to output the data byte or begin a new conversion.

Read operations in the Am6108/Am6148 are initiated by taking $\overline{CS}$ and $\overline{R}$ both low to enable the 3-state data outputs. On the Am6108 only, if D/$\overline{ST}$ is held low, then $\overline{CC}$ is output at D_7 and D_6-D_0 are held disabled. This allows the processor to check the status of the converter to determine if the conversion is complete. When $\overline{CS}$ and $\overline{R}$ are both held low with D/$\overline{ST}$ high, the 3-state outputs will not be enabled until $\overline{CC}$ goes low. When the 3-state outputs are enabled there are two formats for reading data out of the Am6108/Am6148: two's complement format is selected by holding CODESEL low during the read, and binary offset is selected by holding CODESEL high. Figure 1 shows the complete decoding of the Am6108/Am6148 control lines.

The full-scale output current of the DAC is determined by the reference current supplied to the GAIN R and/or REF_{IN} inputs of the Am6108/Am6148. The DAC full-scale output current is four times the reference current. The GAIN R input is a 2.5KΩ series resistor that will convert the 2.5V internal reference voltage into a 1mA reference current. The REF_{IN} input, on the Am6108 only, allows the user to provide his own scaling resistor for determining the reference current.

Once the DAC reference current is set up, the Am6108/Am6148 can be operated with either a unipolar or bipolar input signal. Two inputs are provided for unipolar operation, the R_{IN} input has a 2.5KΩ resistor connected between it and the comparator summing node. The R_{OFF} input is identical to R_{IN}, except the value of the resistor is 1.25KΩ. The R_{IN} input is used alone for a unipolar input of 0 to +10V and the R_{OFF} input is used alone for 0 to +5V signals. The bipolar operation of the Am6108/Am6148 requires a half-scale offset current to be supplied to the comparator summing node. This can be accomplished by connecting the R_{OFF} input to the V_{REF} output, which produces a 2mA offset current to the comparator summing node. A −5 to +5V input signal can be applied at R_{IN}. A third input, +COMP, is connected directly to the comparator summing node. This allows the user to provide any external scaling networks desired for the Am6108 operation. This +COMP is not available on the Am6148.

Figure 1. Am6108/ Am6148 Control Signal Decoding

Signals							Function
CLK	$\overline{CS}$	$\overline{S}$	$\overline{R}$	D/$\overline{ST}$*	CODESEL	$\overline{CC}$	
X	1	X	X	X	X	X	Outputs Three-stated
0	0	0	X	X	X	X	Reset SAR
X	0	1	0	0	X	X	Read Status (Am6108 Only)
X	0	1	0	1	X	1	Outputs Three-stated
X	0	1	0	1	0	0	Read Data (Two's Complement Code)
X	0	1	0	1	1	0	Read Data (Binary Offset Code)

*Function available on the Am6108 only. X = Don't Care

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as the number of output bits, or 1 part in 2^n where n is the number of bits.

Monotonicity (Missing Codes): Monotonicity is a property of the D/A within a successive approximation (S/A) A/D. Each increment in the digital code to the D/A is accompanied by an analog output that is greater than, or equal to, that of the proceeding code. Monotonicity of the D/A is a necessary requirement for a S/A A/D to have no missing codes.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input value which produces a given digital output code. An ideal value of a code width is equivalent to FSR/2^n, where n is the number of bits.

Linearity: The deviation of each individual code from an ideal straight line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an *inherent* ±1/2LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2LSB.

Unipolar Offset Error: Difference between the ideal (+½LSB) and the actual analog input level required to produce the first digital code transition (00 . . . . 00 to 00 . . . . 01) over the complete temperature range.

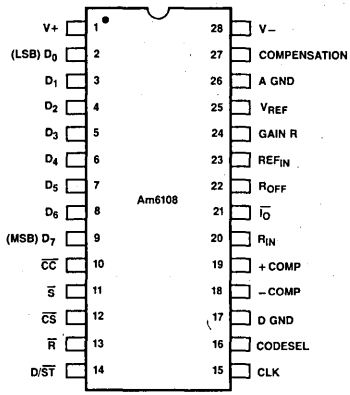
Bipolar Offset Error: Difference between the ideal (1/2FSR - 1/2LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 . . . . 11 to 10 . . . . 00).

Power Supply Sensitivity: A measure of the change in gain and offset of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: The measure of how long it takes for the A/D to arrive at the correct digital output code. It is the time between the clock edge that starts a conversion after receiving a start command and the edge of the status line ($\overline{CC}$) which signifies that the conversion is completed.

CONNECTION DIAGRAMS
Top Views

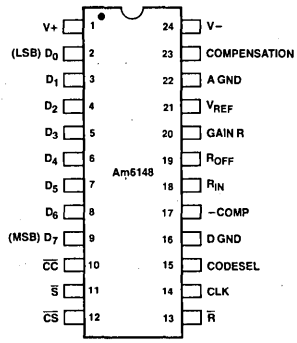
D-28-1



Standard, 0.6" Package

ABI-094

D-24-SLIM



Slim, 0.3" Package

ABI-095

FUNCTIONAL PIN DESCRIPTION

Symbol	Function
V_{REF}	Reference Voltage Output – The output of the internal, precision 2.5 volt reference.
GAIN R	Reference Input Gain Resistor – A 2.5KΩ resistor in series with the positive input of the DAC reference amplifier. When 2.5 volts is applied to this pin, a 1.0mA reference current flows to the DAC. This produces a DAC full scale current of 4mA.
REF_{IN} (Am6108 Only)	Current Reference Input – This pin is directly connected to the positive input of the DAC reference amplifier. The DAC full scale output current is four times the reference current applied to this input.
R_{IN}	Analog Input Resistor – A 2.5KΩ resistor in series with the summing node at the noninverting input to the comparator. It converts the analog input voltage to a current for comparison with the current at the DAC I_O output. When the DAC has a reference current of 1.0mA, this input can be used alone for a 0 to +10 volt input range, or in conjunction with the R_{OFF} input for a −5 to +5 volt range.
R_{OFF}	Input Offset Resistor – A 1.25KΩ resistor in series with the summing node at the noninverting input of the comparator. When this input is connected to the 2.5 volt reference, a half scale offset current enters the summing node. This allows a bipolar input range of −5 to +5 volts at the R_{IN} input. The R_{OFF} pin may also be used as an analog voltage input for a 0 to +5 volt range. When R_{OFF} is not used, this pin should be connected to A GND.
$\overline{I_O}$ (Am6108 Only)	DAC Complementary Current Output – This output should be tied to the digital ground. On the Am6148, $\overline{I_O}$ is internally connected to digital ground.
–COMP	Comparator Inverting Input – Allows the user to add an offset voltage to null the system or as a zero reference. It may also be used as a high-impedance input, normally it is connected to analog ground.
+COMP (Am6108 Only)	Comparator Noninverting Input – This input allows the user to add his own external scaling network to the summing node at the noninverting input of the comparator.
COMPENSATION	Reference Amplifier Compensation – An external capacitor is connected between this pin and V– to provide frequency compensation for the DAC reference amplifier.
$\overline{CS}$	Chip Select – Enables the Am6108/Am6148 for read and start conversion operations.
$\overline{S}$	Start Conversion – An active low input which resets the successive approximation register. When $\overline{S}$ is taken back high, the Am6108/Am6148 begins a conversion.
$\overline{R}$	Read – An active low input which enables the 3-state outputs and allows data to be transferred from the Am6108/Am6148 to the processor.
D/$\overline{ST}$ (Am6108 Only)	Data/Status Control – This input determines whether the Am6108 outputs data, D/$\overline{ST}$ = logic 1, or a status bit, D/$\overline{ST}$ = logic 0, during a read operation. The status bit which appears at output D_7 is the same as the $\overline{CC}$ output. During a status read operation, data outputs D_0–D_6 remain 3-stated. Status output at D_7 is not available on the Am6148.
CODESEL	Code Select – A logic 1 on this input enables the Am6108/Am6148 to output data in binary offset format, a logic 0 results in two's complement format.
CLK	Clock – A TTL level clock is used at this input to produce the internal timing of the Am6108/Am6148 during a conversion.
$\overline{CC}$	Conversion Complete – This active low output indicates the end of a conversion.
D_0–D_7	Data Outputs – Eight 3-state outputs which are used to transfer data from the Am6108/Am6148 to the processor.

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.3 to +7.0V	Voltage at GAIN R, REF_{IN}	V− to V+
V− to D GND	+0.3 to −7.0V	Voltage at R_{IN}, R_{OFF}	±12V
Max Differential V+ to V−	±12V	DAC Compliance Voltage	−2 to +12V
Digital Inputs to D GND	−0.5 to +6.0V	Operating Temperature	0 to +70°C
A GND to D GND	±1V	Storage Temperature	−65 to +150°C
V_{REF} Max Output Current	15mA	Lead Temperature (Soldering 60 sec)	300°C
Max Input Current at REF_{IN}	2mA	Minimum Operating Voltage	9.7V

ELECTRICAL CHARACTERISTICS (These specifications apply for $V^+ = +5V \pm 5\%$, $V^- = -5.2V \pm 5\%$, V_{REF} connected to GAIN R, $0°C \leq T_A \leq 70°C$ and $f_{CLOCK} = 500KHz$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristics						
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Differential Nonlinearity			±1/4	±1/2	LSB
	Linearity			±1/4	±1/2	LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error	V_{IN} = 0 to +5V		±1½	±4	LSB
		V_{IN} a= 0 to +10V		±1	±2	
	Unipolar Offset Error			±1/2	±1	LSB
	Bipolar Gain Error	V_{IN} = −5V to +5V		±1	±2	LSB
	Bipolar Offset Error			±3/4	±1½	LSB
	Positive Power Supply Sensitivity	$V^+ = +5V \pm 5\%$		0.02	0.2	%FS
	Negative Power Supply Sensitivity	$V^- = -5.2V \pm 5\%$		0.02	0.2	%FS
Internal Reference						
V_{REF}	Reference Voltage	I_{REF} = 1mA	2.485	2.5	2.515	Volts
V_{REF}/T_A	Reference Voltage Tempco			20		ppm/°C
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		0.05	0.2	$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	V^+ = +5V ± 5%		0.05	0.2	$\%V_{REF}$
	Noise, f_n = 10KHz to 1MHz			20		μV_{rms}
Analog Inputs						
	Input Resistance					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
	0 to 5V			1.25		KΩ
	Input Capacitance					
	R_{IN}, R_{OFF}, REF_{IN}*, GAIN R			2		pF
	$\overline{I_O}$*			20		pF
	+COMP*			20		pF
	−COMP			2		pF
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				0.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1	V_{IN} = 2.7V			40	μA
I_{IL}	Logic 0	V_{IN} = 0.4V			10	μA

*Function available on the Am6108 only.

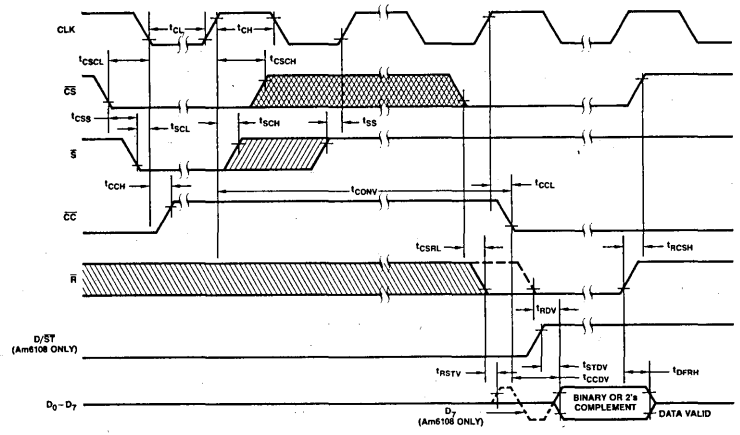
ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			0.5	Volts
I_{SC}	Output Short Circuit Current			−40		mA
I_{OZ}	**Off-State Output Current**					
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Power Requirements						
I^+	Positive Supply Current			44	60	mA
$I-$	Negative Supply Current			−65	−85	mA
	Power Dissipation			600	800	mW

SYSTEM TIMING

Parameters	Description	Min	Typ	Max	Units
t_{CONV}	Conversion Time		1	2	μs
t_{CSS}	$\overline{CS}$ Low to $\overline{S}$ Low	0			ns
t_{CSCL}	$\overline{CS}$ Low to CLK Low	0			ns
t_{SCL}	$\overline{S}$ Low to CLK Low	0			ns
t_{CCH}	$\overline{CC}$ High from CLK Low		35	40	ns
t_{SCH}	$\overline{S}$ High from CLK High	0			ns
t_{SS}	$\overline{S}$ High before CLK High	10			ns
t_{CSCH}	$\overline{CS}$ High from CLK High	0			ns
t_{CCL}	$\overline{CC}$ Low from CLK High	20	30	40	ns
t_{CSRL}	$\overline{CS}$ Low to $\overline{R}$ Low	0			ns
t_{RSTV}	$\overline{R}$ Low to Status Valid on D_7 (Am6108 Only)	15	30	40	ns
t_{STDV}	Status to Data Valid on D_7 (Am6108 Only)	15	30	40	ns
t_{CCDV}	$\overline{CC}$ Low to Data Valid	15	30	40	ns
t_{RDV}	$\overline{R}$ Low to Data Valid	15	30	40	ns
t_{DFRH}	Data Float from $\overline{R}$ High	20	30	40	ns
t_{RCSH}	$\overline{R}$ High to $\overline{CS}$ High	0			ns
t_{CL}	CLK Low	50			ns
t_{CH}	CLK High	50			ns

System Timing



ABI-096

*Function available on the Am6108 only.

APPLICATIONS INFORMATION

The Am6108/6148 contains all the active components required to perform a complete A/D conversion. The device is specified over the complete temperature range and includes the effects of the on-chip voltage reference.

Figures 2 and 3 show the Am6108/6148 used in unipolar and bipolar configurations. Gain and offset errors may be trimmed for optimum performance using external components (discussed later). The maximum offset error, unipolar and bipolar are specified as ±1LSB and ±2LSB respectively over the complete temperature range and in many applications would not require any trimming.

Both Figures 2 and 3 show the Am6108/6148 configured as an I/O port. A conversion is started by performing a write operation to the port address. The $\overline{IOW}$ line strobes the $\overline{S}$ input to start the conversion. Operating with a 10MHz clock, the Am6108/6148 will complete a conversion within 1μsec; therefore with many CPUs, a READ operation could occur immediately after starting the conversion and receive valid data. The Am6108/6148 requires a minimum of nine clock cycles to complete a conversion, which most microprocessors can meet fairly easily. However, if the Am6108/6148 is used with a slower clock, then a circuit similar to Figure 4 may be used to hold the processor in wait states during the read operation until the $\overline{CC}$ output goes low.

The status of the A/D (Am6108 only) can be interrogated via output D_7 when $D/\overline{ST}$ = logic 0 during a read operation. During a status read operation data outputs D_0-D_6 remain three-stated. The status output at D_7 is not available on the Am6148.

The data from the A/D converter can be read out using a normal I/O read operation to the port address. The output code may be offset binary or two's complement depending upon the logical state of CODESEL (logic 1 – offset binary, logic 0 – two's complement).

The Am6108/6148 may also be interfaced with a DMA controller for burst mode operation. Figure 5 shows the Am6108/6148 interfaced with the Am9517A DMA Controller. The DMA mode of operation begins with a software request for block transfer by the Am9517A. The Am6108/6148 begins a conversion each time it receives a request and holds the DMA controller in wait states until each conversion is complete. This cycle is repeated until a complete block of data has been transferred to memory.

Unipolar Configuration (Figure 2)

The Am6108/6148 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of the code. If no trims are used, the Am6108/6148 is guaranteed to have ±1LSB max zero offset error and ±2LSB max gain error (0 to +10V full scale). If the offset trim is not required R_{OFF} (pin 22 – Am6108, pin 19 – Am6148) should be connected to analog ground. The two resistors R_1 and R_2 and potentiometer R_3 are then not needed. If the gain error (full scale) trim is not required, then resistor R_5 should be removed and the analog input connected to R_{IN} directly. The 100Ω full scale adjust potentiometer R_4 is not needed and V_{REF} out is connected directly to GAIN R. When a 0 to +5V input range is required the analog input is connected to R_{OFF} instead of R_{IN}. R_{IN} should be connected to analog ground in this application.

Unipolar Calibration

Connecting R_{OFF} to R_1 and R_2 the initial offset error can be trimmed by R_3. The first A/D transition (0000 0000 to 0000 0001) should occur for an input level of +1/2LSB (19.5mV).

The gain error (full scale) trim is done by applying a signal 1 1/2LSBs below the nominal full scale (9.94 for a 10V input range). R_4 is trimmed to give the last transitions (1111 1110 to 1111 1111).

Bipolar Configuration (Figure 3)

If the offset and gain errors are acceptable, one or both of the trimmers can be removed plus the 50Ω resistor R_3. The analog input is applied directly to R_{IN} and V_{REF} out is connected to GAIN R and R_{OFF} directly.

Bipolar Calibration

Bipolar calibration is similar to unipolar calibration. First, a signal +1/2LSB above negative full scale (−4.9805V) for the ±5V input range) is applied to R_3 and potentiometer R_1 is trimmed to give the first transition (0000 0000 to 0000 0001). Then a signal 1 1/2LSB below positive full scale (+4.9941V) is applied and potentiometer R_2 trimmed to give the last transition (1111 1110 to 1111 1111).

Offset and gain calibration can be more accurately trimmed by summing a small triangular wave voltage to the analog input signal, and the digital outputs monitored to determine the center point of the code transition.

Driving the Am6108/6148

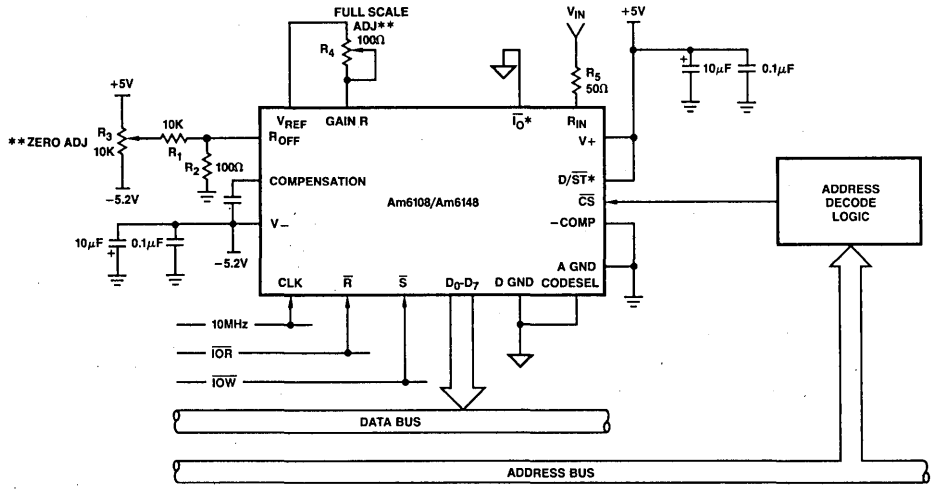
TheAm6108/6148 is a successive approximation typo analog-to-digital converter. During the conversion cycle, the A/D input current is modulated by the DC test current at the A/D clock frequency. Thus, it is important to recognize that the signal source driving the Am6108/6148 must be capable of holding a constant output voltage under dynamically-changing load currents. Many operational amplifiers have closed-loop output impedance equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. At high frequencies, where the loop gain is low, the amplifier output impedance rises to its open-loop value. The output of the amplifier may return to its nominal voltage before the converter makes a comparison, so that little or no error is introduced. However, many precision amplifiers have limited bandwidth, which recover very slowly from output transients. The use of wide-band amplifiers is recommended plus a unity-gain buffer included inside the amplifier's feedback loop.

Supplying Decoupling and Layout Considerations

The Am6108/6148 is built using a very high frequency bipolar process, it is very important that the power supplies be filtered, well regulated and free from high frequency noise. Switching power supplies are not recommended because of the switching spikes present. Decoupling of the supplies with 10μF tantalum in parallel with 0.1μF disc ceramic type capacitors is recommended. If the supplies are still noisy then further filtering can be achieved by inserting low value series resistors (metal film) between the supplies and the decoupling capacitors.

Circuit layout should attempt to keep analog circuitry of the Am6108/6148 and associated components as far away from logic interconnections as possible. The analog ground (A GND) is the ground point for the internal reference, D/A converter and comparator and should be a "high quality" ground. In most cases, the A. GND and D. GND can be connected together at the package, but in some situations, the D. GND can be connected to the most convenient ground, and the A. GND to the analog power return.

Figure 2. Am6108/Am6148 Unipolar Configuration



*Function available on the Am6108 only. **See application information.

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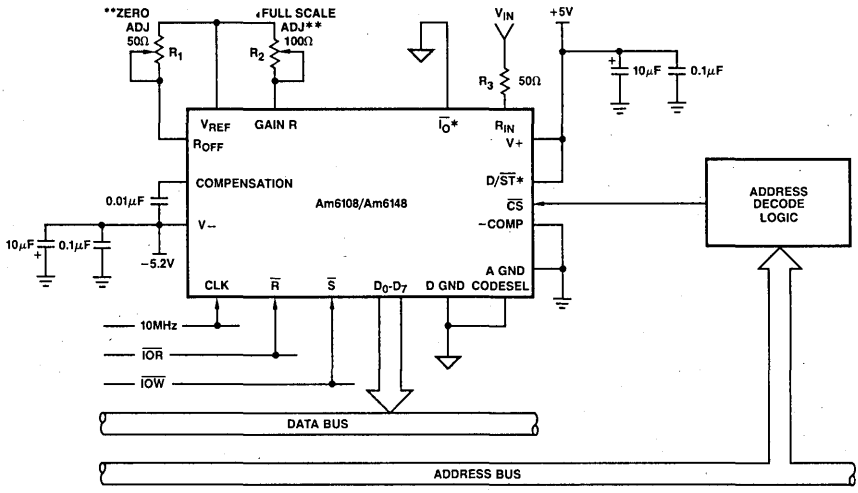
Figure 3. Am6108/Am6148 Bipolar Configuration



*Function available on the Am6108 only. **See application information.

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Figure 4. Am6108/Am6148 $\overline{CC}$ to Microprocessor RDY Interface

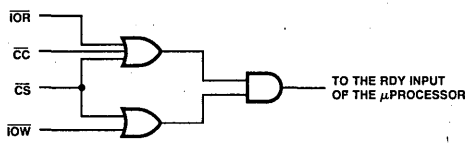

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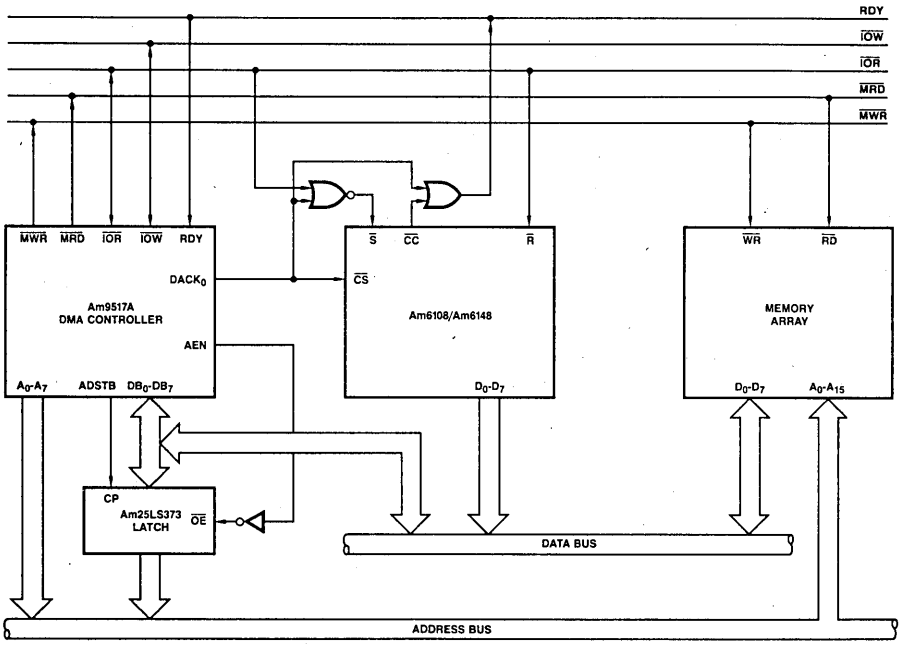
Figure 5. Am6108/Am6148 DMA Configuration



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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
Am6108DC	D-28-1	C	C-1
Am6148DC	D-24-SLIM	C	C-1

Notes: 1. D = Hermetic DIP. Number following letter is number of leads.
2. C = 0 to +70°C.
3. Level C-1 conforms to MIL-STD-883, Class C.

Am6108/6148

Applications and Design Hints
Advanced Micro Devices

INTRODUCTION

The Am6108/6148 is a completely monolithic, high-speed, microprocessor-compatible analog-to-digital converter (ADC) that converts analog input signals into 8-bit digital output code in less than 1 microsecond. The digital output code is selected by the user as either 2's complement or offset binary. Due to the high-speed conversion, "WAIT" states are no longer necessary for most microprocessor based data conversion/acquisition systems or instrumentation.

The Am6108 consists of an 8-bit digital-to-analog converter (DAC), a high-speed comparator, a successive approximation register (SAR), a 2.5V reference and control logic. The 2.5V reference is implemented utilizing the bandgap voltage of silicon. The digital outputs are three-state buffers with standard TTL levels for logic 1 and logic 0. This allows the user to conveniently interface with the microprocessor data bus.

Internal scaling resistors enable the Am6108 to handle input signal ranges of 0 to +5V, ±5V and 0 to +10V with the device operating at +5V and −5.2V.

The Am6108 uses linear differential logic (LDL) to implement the switching functions. LDL is a non-saturating form of logic similar to emitter coupled logic (ECL), however, it offers higher performance with improved density since the logic cell is smaller. Compared to the ECL, LDL speed-power product is significantly lower. Level translators are used to achieve TTL-level compatibility at digital inputs and outputs.

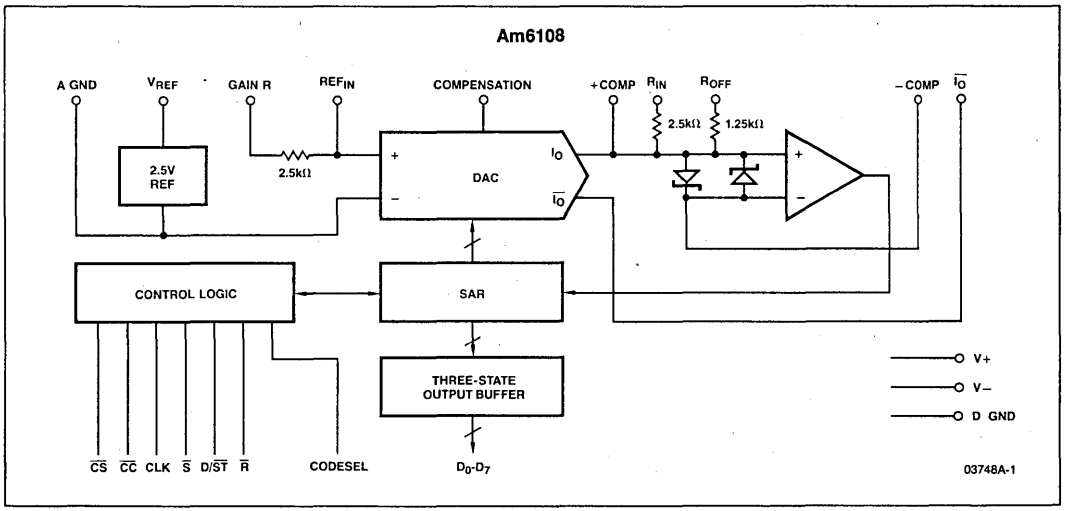


Figure 1a.

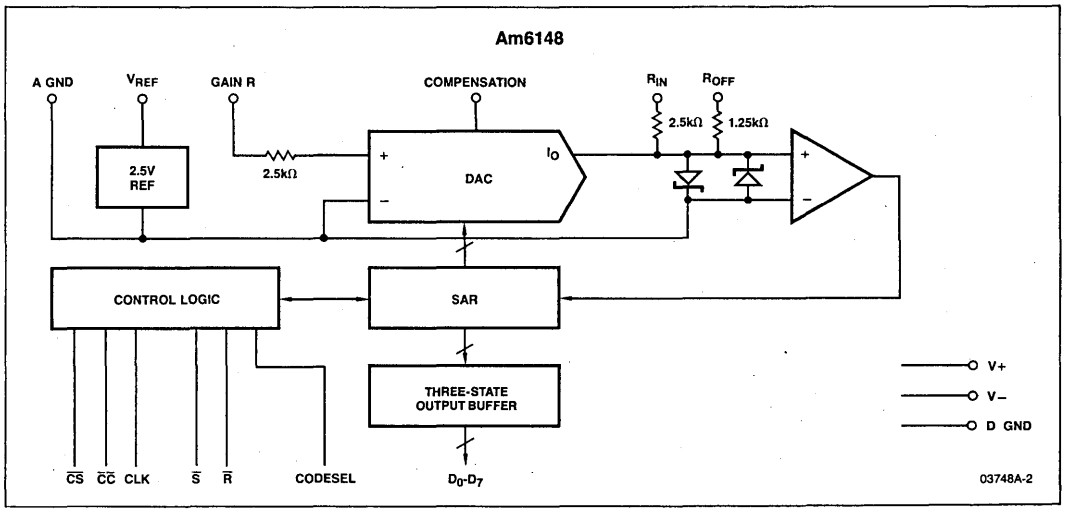


Figure 1b.

DEVICE PERFORMANCE

The Am6108 belongs to a class of converters known as the "successive approximation" type of ADCs. The successive approximation method offers a wide range of speed (conversion time down to less than 1 microsecond) and resolutions of up to 16 bits, and because it makes possible more cost-effective designs it has become the most popular A-D conversion technique.

Am6108/6148 OPERATION

Figure 1(a) shows the block diagram of the Am6108 and 1(b) of the Am6148. When the Chip Select ($\overline{CS}$) and Start ($\overline{S}$) inputs are LOW, the first negative going transition of the clock resets the SAR (S_0 in the timing diagram of Figure 2). During S_0 the Conversion Complete ($\overline{CC}$) status line goes HIGH to indicate a conversion cycle, however, in order to start the active part of the conversion cycle, the $\overline{S}$ line must be taken HIGH.

At S_1, the output of the DAC is compared with the analog input to determine the status of D_7 (MSB). If the DAC output is greater, the comparator output will switch and the result will be stored in the SAR as a logic "0" during S_2. Otherwise, the comparison will result in a logic "1" stored in the SAR. As shown in Figure 2, D_6 status is also determined during S_2. This sequence is done successively from D_7 (MSB) to D_0 (LSB).

During S_9, the $\overline{CC}$ status line goes low to indicate that the conversion is completed and that the digital code representing the analog input is stored in the SAR. The Am6108/6148 conversion time takes nine clock periods; with a 10MHz clock, this means a 900-nanosecond conversion time. Data lines $D_0 - D_7$ are in the high-impedance state while the Am6108/6148 is doing a conversion.

TABLE 1. Am6108/6148 FUNCTION TRUTH TABLE

Control Logic Input Signals							Function
CLK	$\overline{CS}$	$\overline{S}$	R	CC	D/$\overline{ST}$*	CODESEL	
X	I	X	X	X	X	X	Outputs High Impedance
O	O	O	X	X	X	X	Reset SAR
X	O	I	X	X	X	X	Conversion Cycle
X	O	I	O	I	I	X	Outputs High Impedance
X	O	I	O	O	I	O	2's Complement Output
X	O	I	O	O	I	I	Offset Binary Output
X	O	I	O	X	O	X	Read Status*

*Am6108 Only

Table 1 illustrates the truth table associated with the control logic inputs. The READ STATUS function allows the $\overline{CC}$ to be examined via the D_7 line while the other seven data bits are in the high-impedance state. When D_7 is HIGH, the Am6108 is in the conversion cycle; a LOW means that data can be transferred or another conversion cycle can be started. The READ STATUS function on the Am6108 is established by the D/$\overline{ST}$ line going LOW during a READ cycle.

After the conversion cycle, data may be read out of the SAR. Figure 3 shows the timing diagram of the Am6108 read cycle. $\overline{CS}$, $\overline{R}$, D/$\overline{ST}$, and CODESEL are gated internally to control both the data output and selection of desired binary output code (2's complement or offset binary). For example, to obtain the 8-bit data in 2's complement form, the following control line conditions must be satisfied: $\overline{CS}$ = LOW, $\overline{S}$ = HIGH, $\overline{R}$ = LOW, $\overline{CC}$ = LOW, D/$\overline{ST}$ = HIGH (Am6108 only,) and CODESEL = LOW.

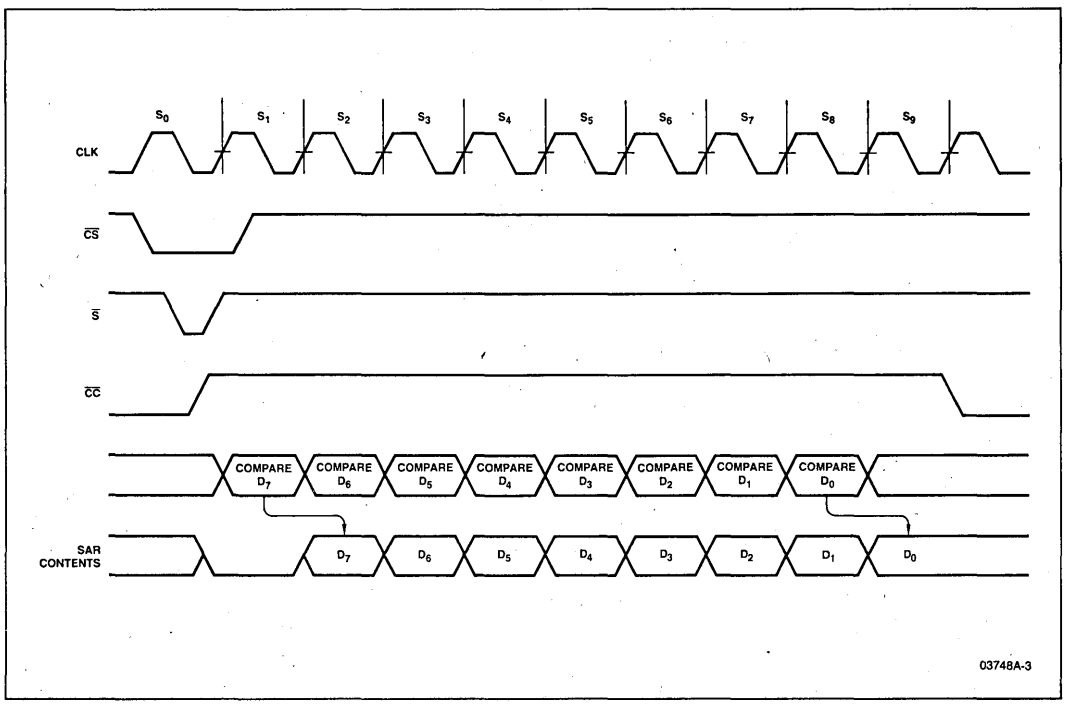


Figure 2. Am6108/6148 Conversion Cycle.

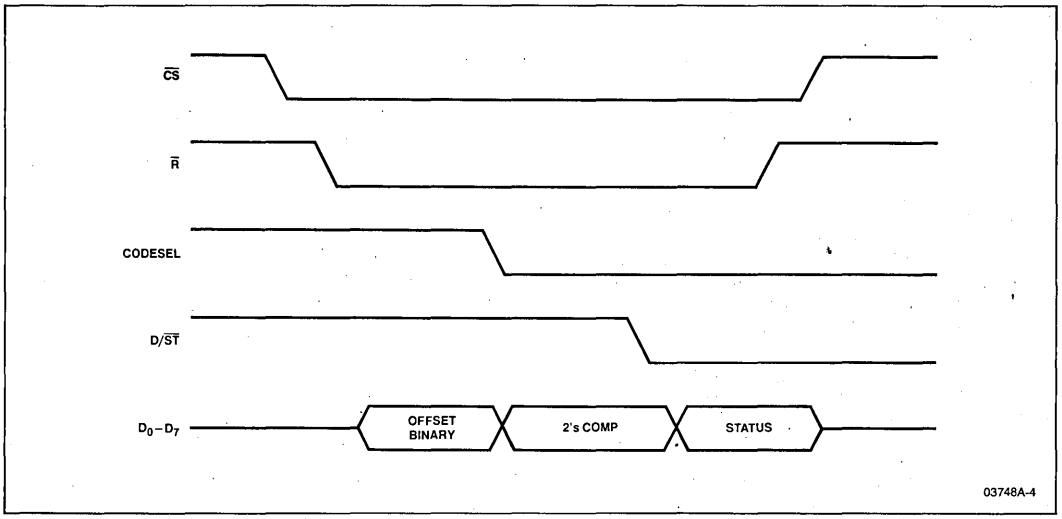


Figure 3. Am6108 Read Cycle.

DAC

The DAC part of the Am6108/6148 is comprised of a reference amplifier, binary weighted current sources and current switches. The binary weighted current sources are implemented using the combination of R-2R resistor scaling. This technique, coupled with the use of diffused resistors, provides better than 8-bit accuracy without any trimming.

The reference amplifier and a reference transistor form a regulator circuit that sets the bias voltage at the bases of the current source transitors. The collector current of the reference transistor is established as $V_{REF}/2.5K\Omega$ (= 1mA).

The current switches, driven by LDL logic signals from the SAR, use current steering logic in the collector of the current source transistors, to switch the bit currents. This technique and the efficient high-speed switching, reduces the settling time of the DAC.

All the current sources are operated at the same emitter current density. To achieve this, the emitter areas are scaled. That is, the MSB current source actually has eight base-emitter junctions with a common collector but each emitter is terminated with a single resistor (R/8) to the negative supply voltage. Since the bit current sources have equal emitter current densities, they all have the same V_{BE} and are matched closely with the V_{BE} of the reference transistor. This structure reduces the settling time of the DAC and minimized the glitching associated with major carries. The changes in the magnitude of the bit current sources due to the variations of h_{FE} and V_{BE}, exhibit excellent tracking over temperature, so that the transfer function of the ADC has no missing codes over the operating temperature range.

COMPARATOR

The essential requirements for a good comparator are low input offset voltage (V_{OS}) for good resolution, fast response, low temperature coefficient of V_{OS} and high input impedance. In a linear integrated circuit this is not easily achieved due to the design trade-offs of the parameters mentioned.

The comparator section has basically three stages. The first is a differential input gain stage buffered by emitter followers. The second stage is a cross-coupled latch followed by another gain stage that also sets the proper voltage levels for driving the LDL circuits. Each gain stage of the comparator is biased at a current proportional to temperature, giving a resolution constant with respect to temperature variations. The voltage swing at the output of the comparator is only 200mV. This low-output voltage swing reduces the comparator's overall gain requirement for the required 8-bit resolution. Along with low-offset voltage and low-bias currents, the response time of the comparator is less than 3ns for a 20mV (1/2LSB with 10V full-scale) overdrive. Even with a 5mV overdrive the response time is still typically 5ns.

During the conversion cycle, the function of the latch is to hold the comparator output stable independent of the analog input. The clock's positive transition enables the latch and transfers current from the input gain stage to the latch stage. The output stage responds with HIGH or LOW level, signifying the result of the comparison between analog input and DAC output. It is important that this result be stable during the process of storing it in the SAR. Among the advantages of comparator operation in the current-switch mode are; speed (transistors are in non-saturated operation), relaxation of common mode rejection requirements and better temperature tracking.

VOLTAGE REFERENCE

The voltage reference used in the Am6108/6148 utilizes an improved version of the basic bandgap reference. At wafer sort, resistor trimming is done by selectively blowing metal link fuses to achieve a final voltage value of ±15mV over temperature.

Load regulation is 0.2% of V_{REF} for loads from 1 to 5mA. Line regulation is also 0.2% for positive supply voltage change of ±5%.

Am6108/6148 IN SYSTEM ENVIRONMENT

Since the advent of microprocessor technology, the design of monolithic data converters (ADC or DAC) has been greatly in-

fluenced by their ability to be interfaced easily with as many different microprocessors as possible. In some applications, the conversion speed of the data converters must adapt to the speed of the microprocessor, or, in other words, the microprocessor cannot afford to "WAIT" for the data conversion to be done. Therefore, the data conversion time must be less than the microprocessor instruction cycle time to avoid WAIT states. This has made more efficient use of microprocessor time possible and pushed the state-of-the-art in the monolithic design of data conversion ICs. For example, if an Am8085A-2 is used as the CPU operating at 4MHz with an ADC that has a conversion time of 5 microseconds as an I/O device, several WAIT states will be needed since valid data from the ADC will not be available during the time a valid $\overline{RD}$ command is generated by the CPU. There are at least three possible actions to solve this problem. 1) make a faster ADC (pushing the state-of-the-art) 2) slow the CPU clock 3) introduce WAIT states to the microprocessor. Items two and three have basically the same effect of decreasing the throughput rate. The option chosen is determined by the processing speed required. Thus, a trade-off is made between the introduction of WAIT states (to accommodate the ADC conversion time) and the CPU clock rate. Refer to Figures 5 and 6 to see how the Am6108/6148 works in a microprocessor based system. The CPU clock is synchronized with the 10MHz ADC clock.

Am6108/6148 with Am8085A-2 (f_C = 4MHz; See Figures 5 and 6)

The control signal ALE is inverted and gated with the decoded port address assigned to the Am6108/6148. With ALE LOW (active,) the first negative clock transition resets the SAR and sets $\overline{CC}$ HIGH to indicate the beginning of a conversion cycle. However, the Am6108/6148 does not start the conversion until after $\overline{ALE}$ has gone high. A valid digital code is not available until sometime during S_9. At this time $\overline{CC}$ goes low to indicate a conversion cycle being completed.

For the Am8085A-2 to read the valid digital code, it must wait for the conversion cycle to be completed. Thus, $\overline{CC}$ is tied directly to the READY line to introduce WAIT states to the microcessor. This extends the $\overline{RD}$ signal and enables the microprocessor to read valid digital codes only from the Am6108/6148. $\overline{RD}$ and $\overline{CC}$ are gated to latch the data from the Am6108/6148 to ensure that only valid data from the ADC is put on the bus.

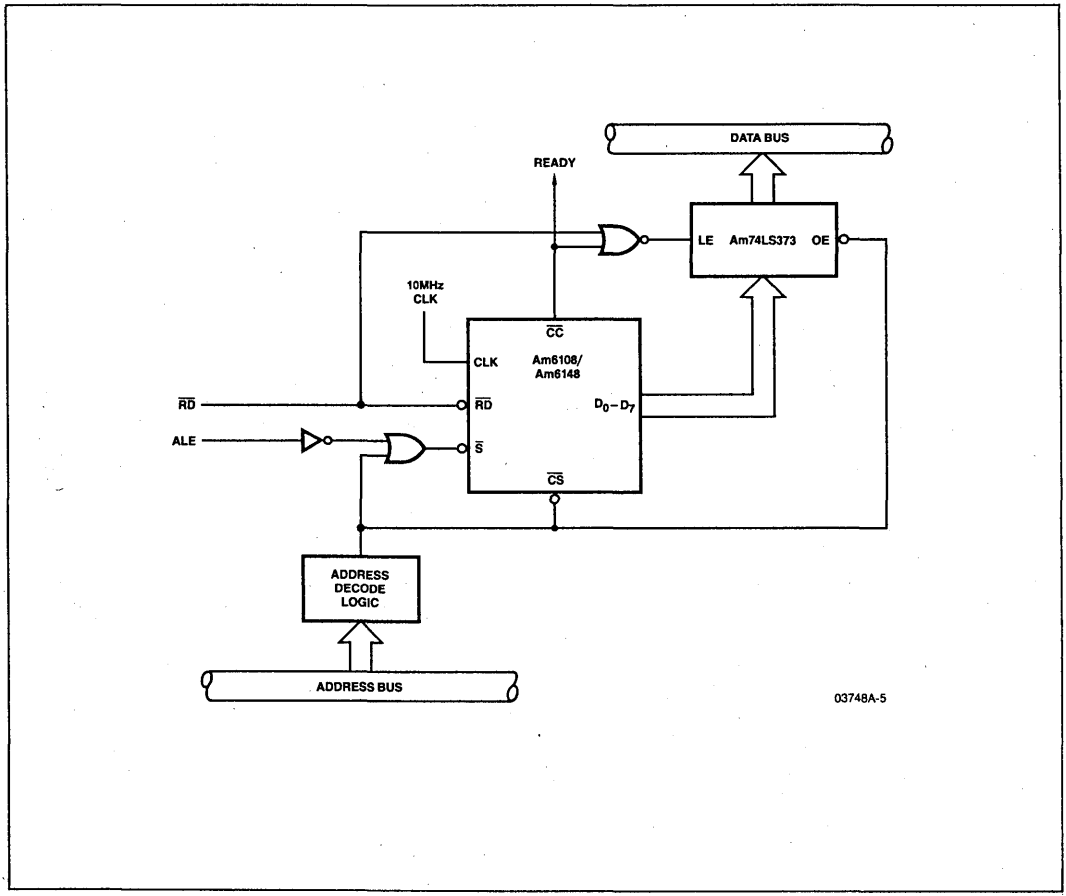


Figure 5. Am6108/6148 Interfaced with Am8085A-2 Control Signals.

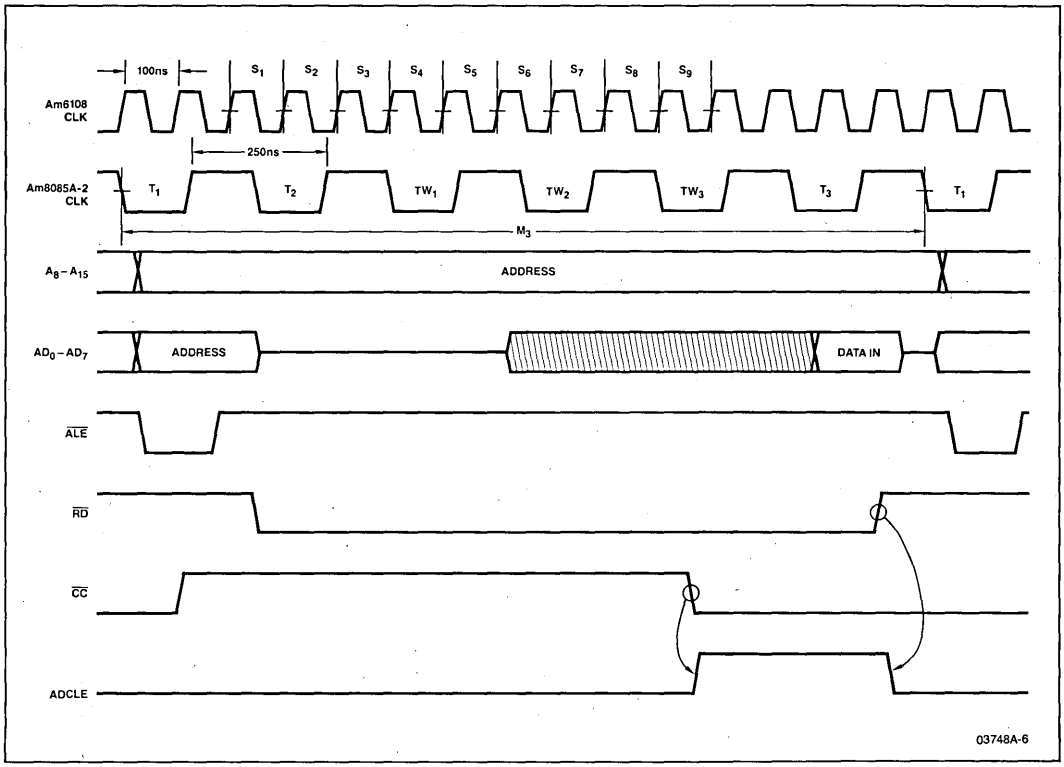


Figure 6. Am6108/6148 Conversion Cycle with 4MHz. Am8085A-2 (with Wait States TW_1, TW_2, TW_3).

Am6108/6148 with Am8085A-2 (f_c = 2MHz; See Figures 6 and 7)

At 2MHz, the Am6108/6148 still runs at maximum clock frequency to fully exploit the high coversion rate of the device.

Figures 6 and 7 show that both the conversion cycle and the microprocessor reading of the ADC's data take 1.5 microsecond. In Figure 6 the CPU has a clock rate of 4MHz and, as a consequence, WAIT states must be introduced. In Figure 7 the CPU clock rate is reduced to 2MHz and no WAIT states are introduced. The main difference between the two schemes is the CPU processing speed.

The Am6108/6148 can convert and transfer data to the microprocessor with only an I/O READ command. In 8080/8085 mnemonics, only the IN command is needed. The following sequence, which could be part of a main program, shows a way of accessing the Am6108/6148 and then storing the data in memory:

```
LDXI  H,xxxx  ;Load register pair H and
              ;L with HEX.
              ;Value specified by xxxx.
IN    Port    ;Load accumulator with
              ;Am6108/6148 data.
MOV   (HL),A  ;Move contents of
              ;accumulator to memory
              ;address pointed to by contents
              ;of registers H and L.
```

In some applications, such as a sampled-data system, it might be required to obtain as much data as possible within 1 millisecond.

Focusing on the ways of implementing a solution, one method is CPU controlled transfer. The sequence of instructions above can be used, then a means of incrementing the contents of H and L registers is provided so that data is stored in contiguous memory locations. If the CPU is running at 4MHz, it will be able to store a maximum of n bytes.

$$n_{Max} = \frac{1 \times 10^{-3} \text{ sec bytes}}{(13 + 7 + 6 + 5)\, 250 \times 10^{-9} \text{ sec}} = 129 \text{ bytes}$$

When the CPU clock is reduced to 2MHz,

$$n_{Max} = \frac{1 \times 10^{-3} \text{ sec}}{(10 + 7 + 6 + 5)\, 500 \times 10^{-9} \text{ sec}} = 71 \text{ bytes}$$

Notice that the difference between the denominators is due to the three WAIT states and the clock period.

Another approach is a hardware implementation using the Am9517A multimode direct memory access (DMA) controller.

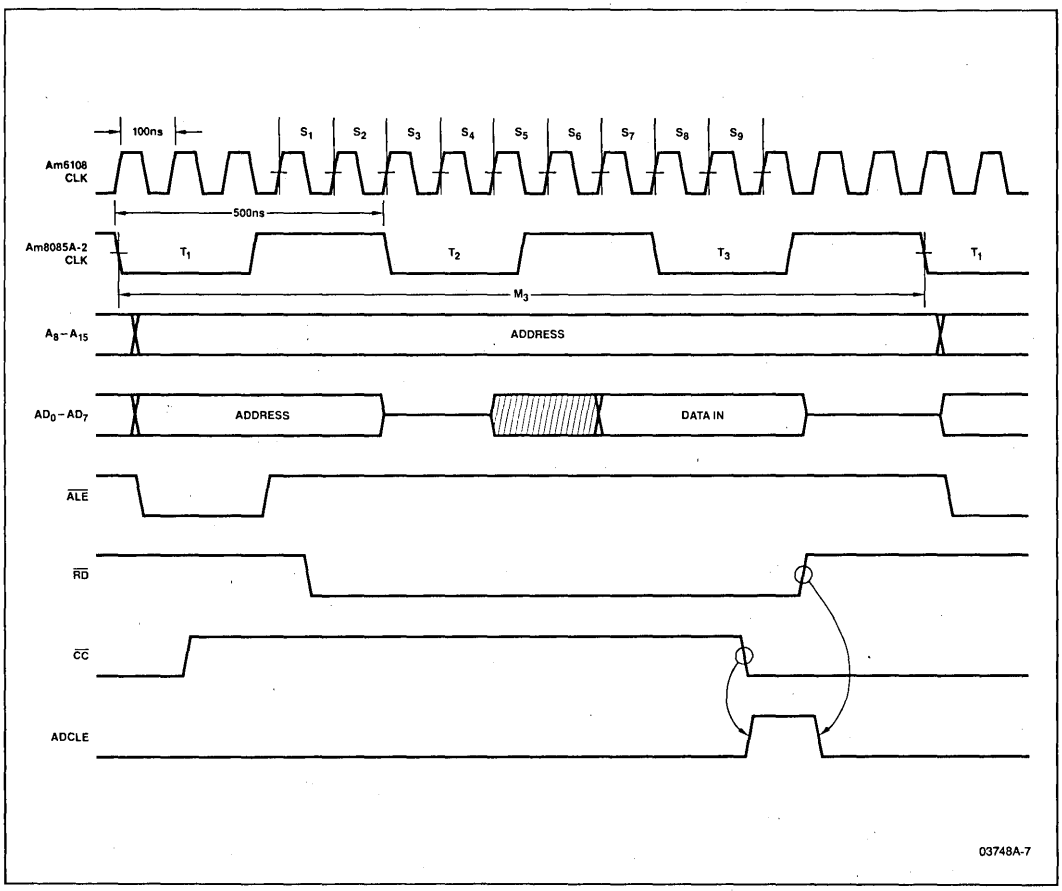


Figure 7. Conversion Cycle with Reduced CPU Clock (without Wait States).

Am9517A Multimode DMA Controller – A Brief Description

DMA is a means of transferring data between peripheral devices and system memory at a much faster rate than CPU-controlled data transfer. During data transfer, the CPU is basically disabled, which means that the DMA controller has to provide all the signals to control the process.

The Am9517A has four channels ($DREQ_0$–$DREQ_3$) from which four peripheral devices may request service. Each channel has four 16-bit registers (base and current address and base and current word count) and a mode register accessible via address lines A_0–A_3. The base registers allow the channels to be automatically reinitialized at the end of a transfer. Auto initialization is selected by programming the mode register. Other internal registers are programmed to set the desired operations and options.

Each of the four channels has four modes of operation selected via the mode register. Two of these are the single transfer mode and the block transfer mode. In the single transfer mode a word is transferred for each DMA channel request. Block transfer allows the Am9517A to make continuous transfer until the word count for the active channel goes to zero.

*Z8002 is a trademark of Zilog, Inc.

Am6108/6148 with Z8002* (16-Bit Microprocessor) and Am9517A (DMA)

Figure 9 shows a method of interfacing the Am9517A and the Am6108/6148 to an Z8002 based system. Figure 10 corresponds to the timing diagram diagram during a DMA transfer.

The Am9517A is in the idle state (S_1) until a valid DREQ is recognized. During this time, the Am9517A may be initialized. The DACK and DREQ lines may be determined to be active HIGH or active LOW by programming the command register. When an active DREQ line is sensed, the Am9517A generates an active HREQ ($\overline{BUSRQ}$) to signal the Z8002 that it wants to control the bus (address, data and control). The Z8002 responds with an active $\overline{BUSAK}$ (HACK), relinquishing the control of the bus to the Am9517A. Once the bus is under the control of Am9517A, DMA transfer may proceed as defined by the internal registers.

As shown in Figure 9, DMA request is generated by hardware, although it can also be done by software. Active $\overline{RESET}$ and $\overline{EOP}$ force the $DREQ_0$ input to go LOW, and CH_0 and XFER initiates a DMA request by setting $DREQ_0$ HIGH.

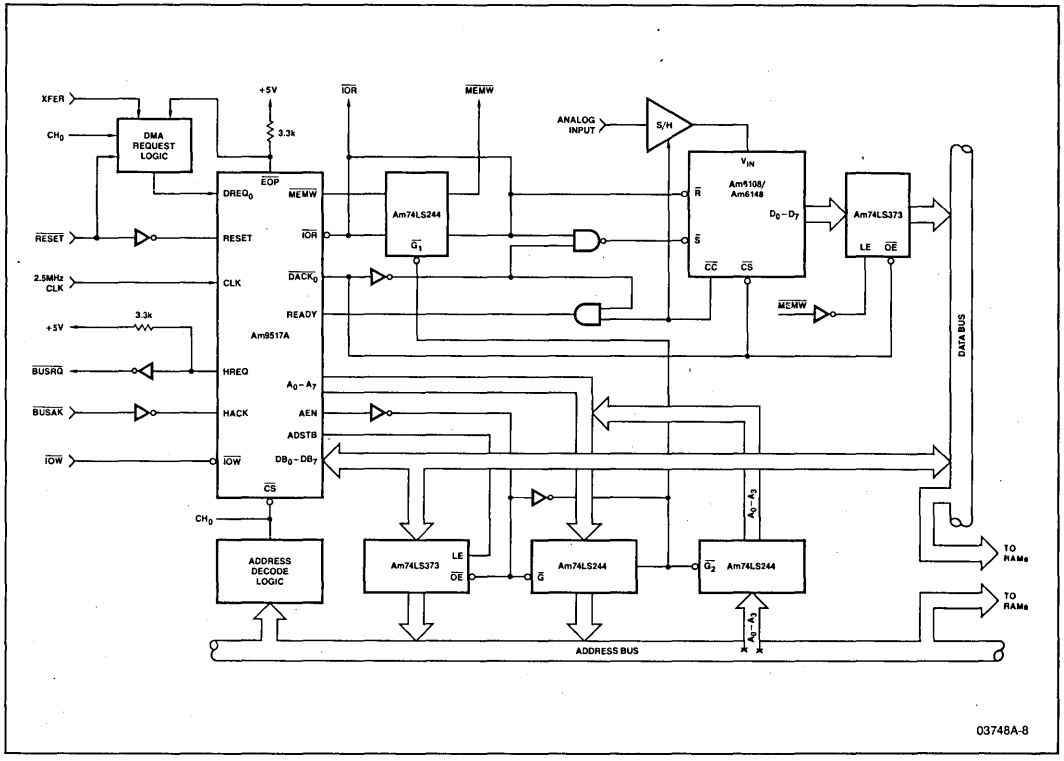


Figure 9. Am6108/6148 under DMA Control.

Figure 10 basically shows the hardware used to make the DMA transfer possible. $\overline{DACK_0}$, the response to an active $DREQ_0$, is used to select the Am6108/6148 and enables the output data latch. $\overline{MEMW}$ is inverted to latch the data from the Am6108/6148. $DACK_0$ is NAND-gated with $\overline{IOR}$ to start the conversion cycle, and the $\overline{CC}$ line is AND-gated with $DACK_0$ and connected to the Am9517A READY input to introduce a WAIT state (SW).

The data transfer rate is $1/1.6\mu s = 625kHz$. Going back to the problem of obtaining as much data as possible in 1msec.,

$$n_{Max} = \frac{1 \times 10^{-3} \text{ sec}}{1.6 \times 10^{-6} \text{ sec}} = 625 \text{ bytes}$$

As the number of bytes required is increased, the method of using DMA transfer becomes even more attractive.

Am6108/6148 with AmZ8002 (16-BitμP) and Z80 (8-BitμP)

Block transfers may be accomplished without the benefit of a DMA controller by the use of either the Z8002 or the Z80. These two microprocessors are attractive because their instruction sets allow the control of block transfers by a single instruction after the inialization of some of the microprocessor internal resisters. These registers are equivalent to the address count and word count registers of the Am9517A DMA controller.

*Z80 is a trademark of Zilog, Inc.

A way of interfacing with the Z80* is illustrated in Figure 12. $\overline{IORQ}$ and the Am6108/6148 $\overline{CS}$ lines are gated together to form the signal that starts a conversion cycle. The conversion cycle is initiated when the Am6108/6148 is selected ($\overline{CS}$ LOW) during T_1 (first clock period) of the I/O cycle. The data latch (Am74LS373) output is enabled only when both $\overline{CS}$ and $\overline{IORQ}$ are active. Data from Am6108/6148 is latched at the end of the conversion cycle ($\overline{CC}$ LOW) when all 8-bits are valid.

Block transfer may be accomplished using the following instructions. The x represents an 8-bit number.

```
LD      B,x     ;Load reg B with number of bytes(up to
                ;256) to be transferred.
LD      C,x     ;Load reg C with the 8-bit port
                ;address of Am6108.
LD      HL,xx   ;Load reg pair H and L with starting
                ;address where block of data is to
                ;be stored.
INIR            ;Transfer x bytes of data (specified
                ;by contents of B-reg) from Am6108
                ;into memory starting at location
                ;specified by contents of H and L reg.
```

If the Z80 is running at 4MHz the throughput rate for the block transfer (excluding the register initializations) is

$$\frac{1}{24\ (250 \times 10^{-9})} = 166.6kHz$$

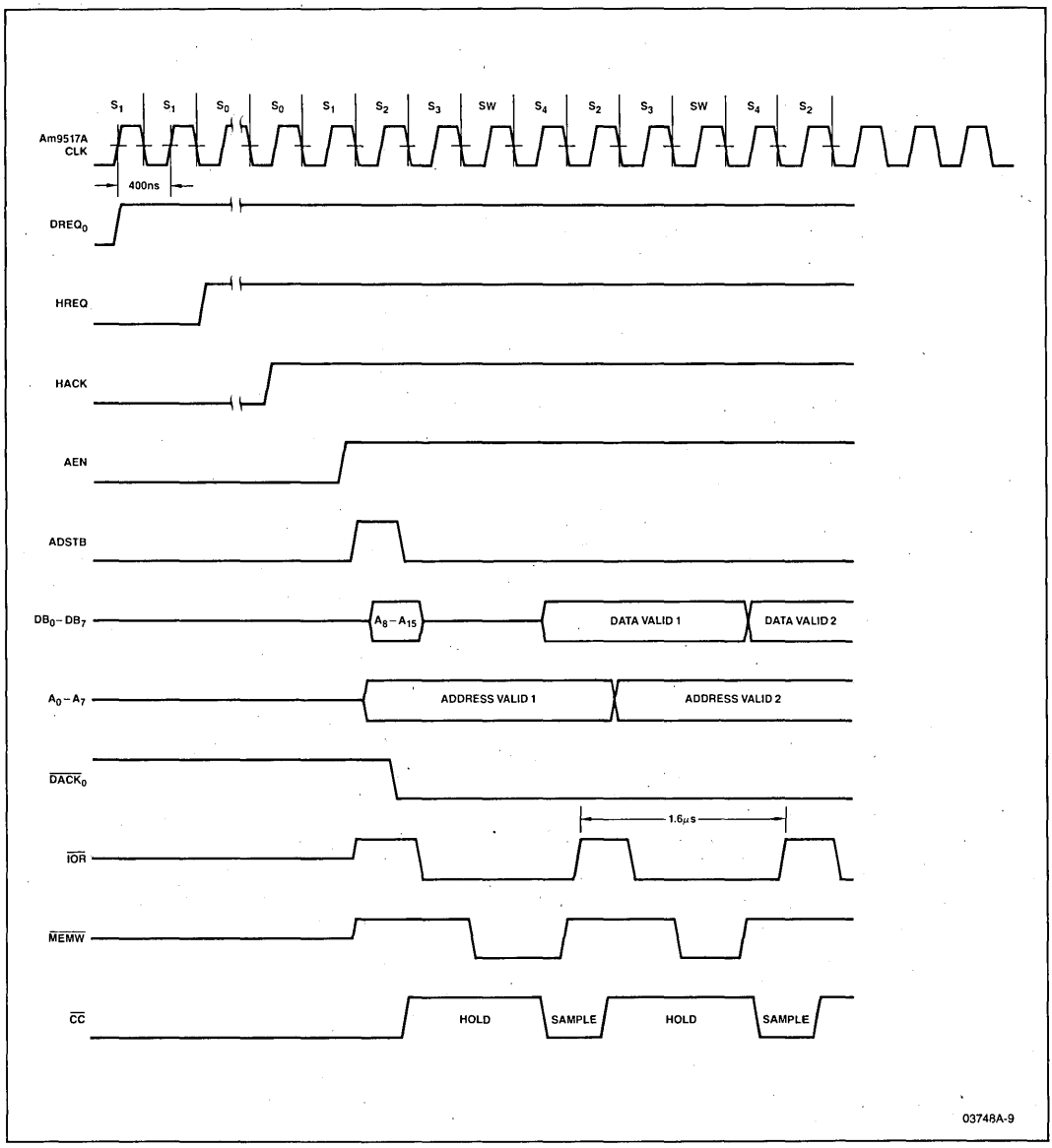


Figure 10. DMA Transfer Timing Diagram (Wait State SW is Inserted by Am6108/6148 $\overline{CC}$ Line). Data Transfer Rate = 625kHz.

Three additional "WAIT" states are added during the I/O cycle as a result of tying the inverted $\overline{CC}$ line to the $\overline{WAIT}$ input line of the Z80. This is shown in the timing diagram of Figure 13.

Interfacing with the Z8002 is somewhat more involved. If we assume that the RAM section is organized such that both byte-oriented and word-oriented transactions are accomodated, interfacing the Am6108/6148 with the Z8002 might be accomplished as shown in Figure 14. Data from Am6108/6148 is steered into either the odd-address or even-address section of the RAM by the least significant bit (A_0). This allows for storing the 8-bit data in contiguous memory locations. Decoding of the status lines ST_0-ST_3 is done only once and the outputs are then available to all the other system elements.

As shown in Figure 15, the conversion cycle starts during state T_1 of the I/O cycle. The decoding of status lines ST_0-ST_3 produce the status signal $\overline{IOR}$. $\overline{AS}$ latches the valid port address assigned to select the 6108 and also issues the start

command. Like the Z80, three additional WAIT states are inserted by connecting the inverted $\overline{CC}$ line to the $\overline{WAIT}$ input line. Programming the Z8002 to do a block transfer is similar to that of the Z80, shown below.

```
LD      R7xx        ;Load reg R7 with no. of bytes (up to 64K)
                    ;to be stored into RAM.
LD      R6,yy       ;Load reg R6 with starting address.
                    ;where data is to be stored.
LD      R5,port     ;Load reg R5 with address assigned
                    ;to Am6108/6148.
INIRB   R5,R6,R7    ;Store xx bytes of data from Am6108 and
                    ;store it starting at memory location yy.
```

where xx and yy represent 16-bit numbers

Disregarding the register initalizations, the throughput rate (which includes the three extra "WAIT" states in the I/O cycle), is shown below.

$$\frac{1}{13\ (250 \times 10^{-9})\ \text{sec}} = 307.6\text{kHz}$$

The two methods of CPU-controlled block transfer are tabulated with the other methods of acquiring data from the Am6108/6148. The Z80-controlled block transfer is limited to a maximum of 256 bytes per issue; the Z8002 is capable of handling groups of up to 64K bytes (Table 2).

TABLE 2. SAMPLED-DATA SYSTEM THROUGHPUT WITH Am6108/6148

Data Transfer Method		Throughput Rate (Max)
CPU Controlled	Am8085A-2 at 4MHz 3 "Wait" States Introduced	129kHz
	Am8085A-2 at 2MHz No "Wait" States	71.4kHz
DMA	Am9517A at 2.5MHz 1 "Wait" State	625kHz
Z80 Block Transfer	Z80 at 4MHz INIR Instruction Used 3 Extra "Wait" States	166.6kHz
AmZ8002 Block Transfer	CPU at 4MHz INIRB Instruction Used 3 Extra "Wait" States	307.6kHz

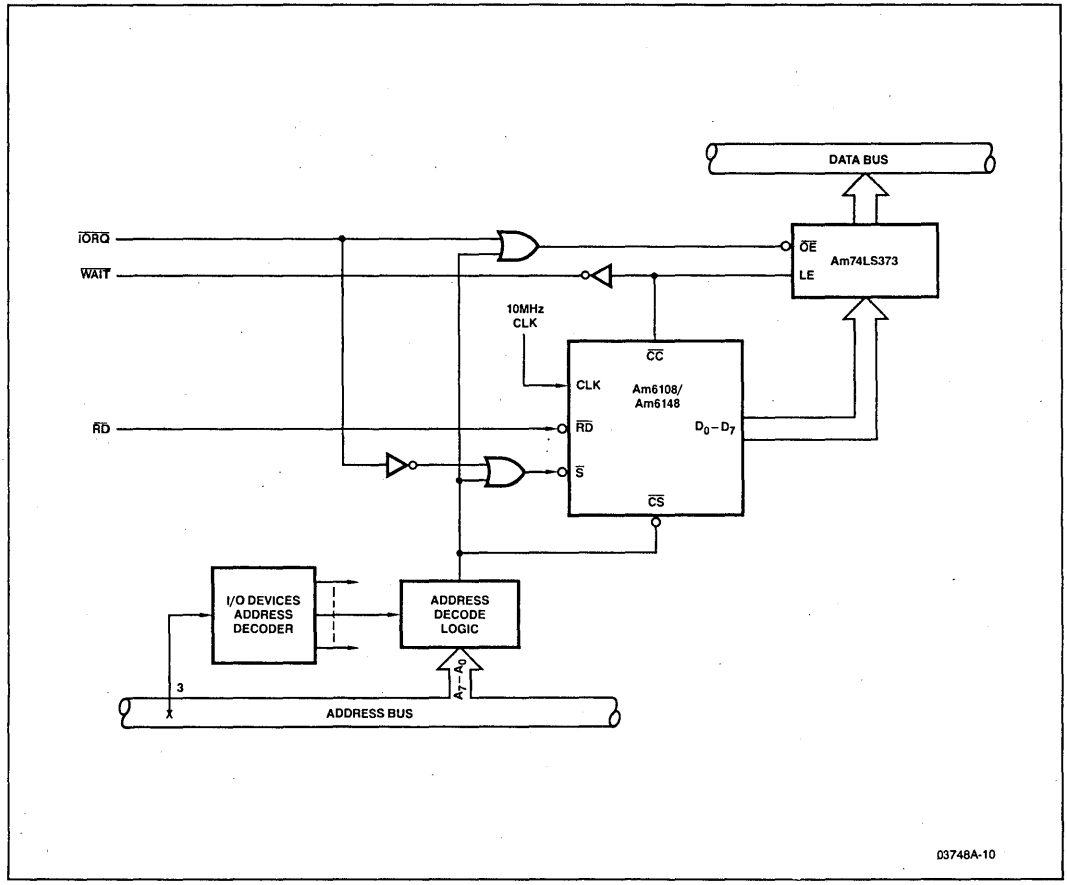


Figure 12. Am6108/6148 Interfacing with Z80.

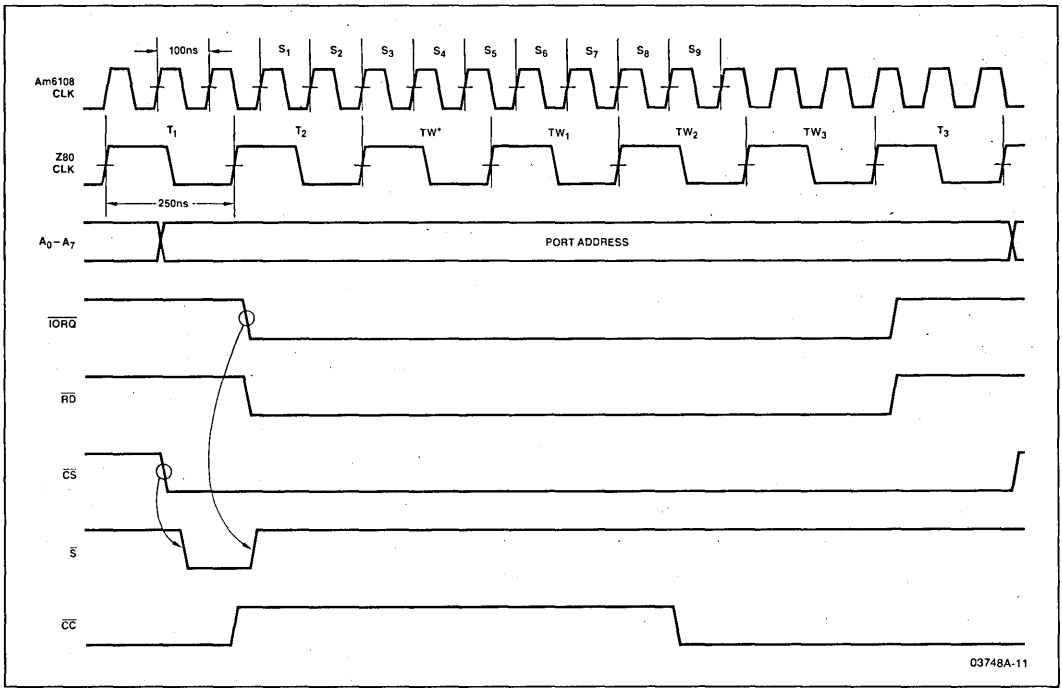


Figure 13. Am6108/6148 Conversion Cycle During Z80 I/O Cycle. (TW* is Automatically Inserted by CPU).

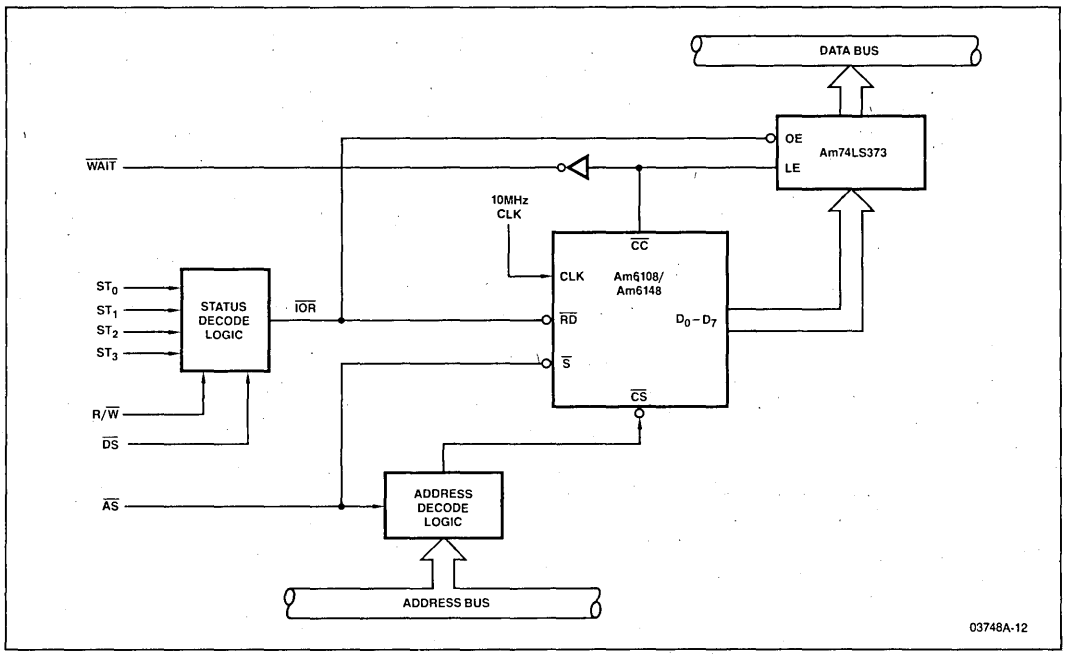


Figure 14. Am6108/6148 Interfacing with AmZ8002 (16-Bit CPU).

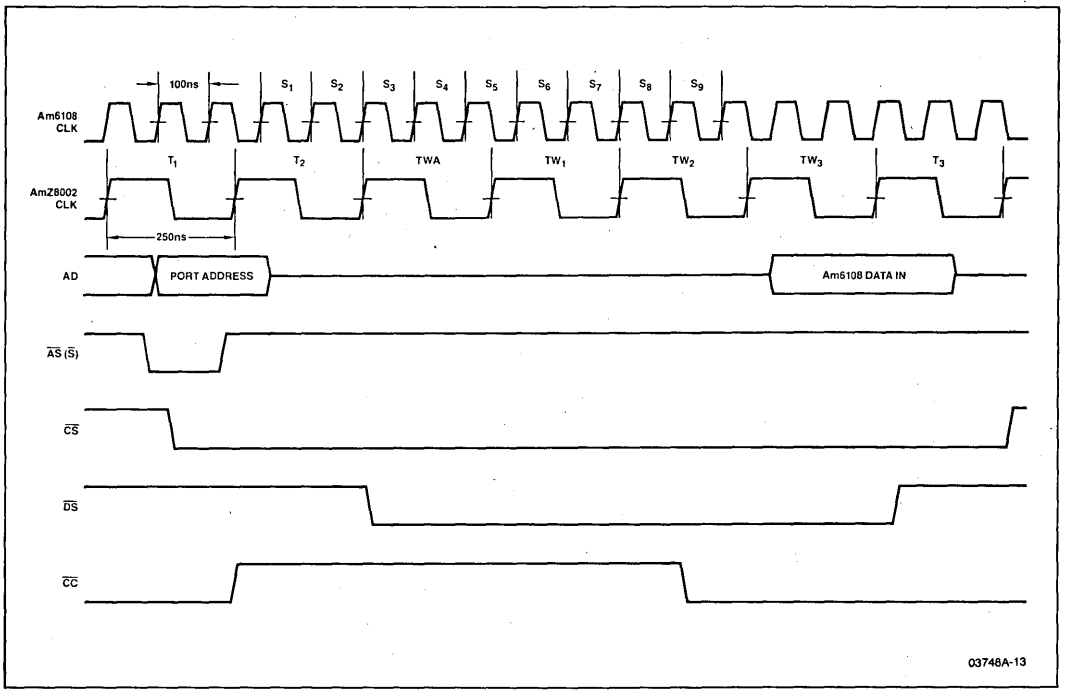


Figure 15. Am6108/6148 Conversion Cycle During AmZ8002 I/O Cycle. (TWA is Automatically Inserted by the CPU).

Error Budget with Sample and Hold

For time-varying analog input signals, and because the analog input must not change more than 1/2LSB while the conversion is going on, a sample (track) and hold (S/H) circuit may be needed at the ADC input. For example, if an ADC has relatively short conversion time of 1.0μs and is required to convert a voltage signal that has a maximum change of 1V/μs, the input signal will change by 1.0V during the conversion cycle. One requirement for accurate 8-bit conversion is that the input signal should not change by more than 19.5mV during the conversion cycle, assuming an input signal range of 0 to 5V.

A sample-hold circuit should only be used when necessary as it can introduce errors which tend to degrade the performance of the ADC.

There is a maximum rate at which an input voltage signal to the S/H circuit can change. This limitation is related to the aperture time of the S/H and the amount of error to be tolerated in the digitizing process. This is expressed as

$$\frac{dV_{IN}}{dt} = \frac{eV_{IN(FS)}}{t_A}$$

where t_A is the S/H aperture time and e is the allowable error. If the error is to be held as 1/4 LSB and t_A is 5ns, then for a 5V full-scale range

$$\frac{dV_{IN}}{dt} = \frac{(1/4)\frac{V_{IN(FS)}}{2^n}}{t_A} = \frac{(1/4)\frac{5V}{2^8}}{5 \times 10^{-9}sec} = 0.976V/ms$$

The aperture time for an ADC is its conversion time. Therefore, the Am6108/6148 has an aperture time equal to 900ns. If we substitute this value to the equation above, we find that dV_{IN}/dt = 5.3mV/μs for a 5V full scale range and 1/4 LSB digitizing error. This means that if the analog input signal to be converted has a maximum change of 5.3mV/μs, a S/H circuit is not needed. This is one of the advantages of a high-speed ADC.

Am6112

Microprocessor Compatible 12-Bit A/D Converter

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

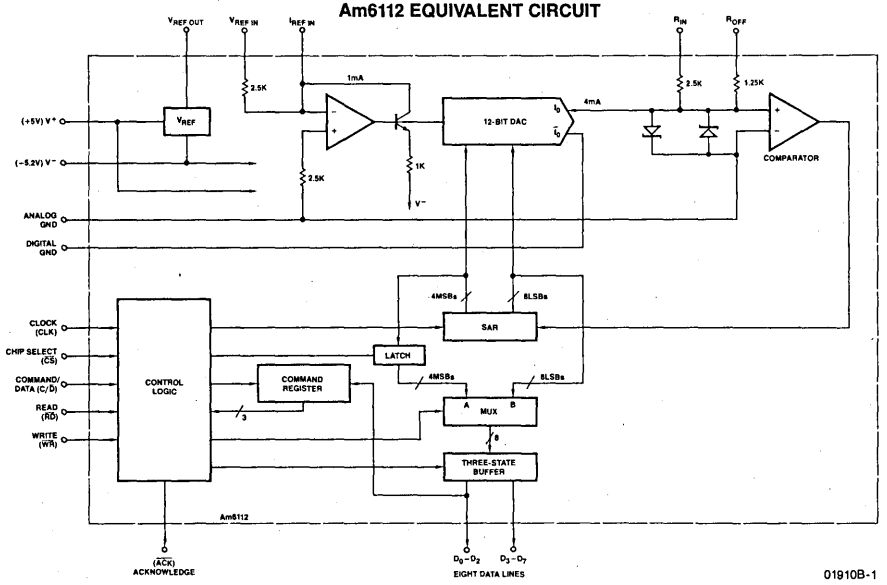
- First totally monolithic, high-speed 12-bit ADC
- 3μs typical conversion time
- Internal precision voltage reference
- No missing codes
- Easy interfacing with 8- and 16-bit microprocessors
- Internal command register for programmable modes of operation
- Offset binary or two's complement output code
- 0 to 10V, or ± 5V input range
- 24-pin package

FUNCTIONAL DESCRIPTION

The Am6112 is the first fully monolithic microprocessor compatible 12-bit high-speed analog-to-digital converter. The Am6112 high-speed A/D contains a precision reference, DAC, comparator, SAR, scale resistors, output three-state buffers and comprehensive control logic, enabling the device to be interfaced with a variety of microprocessors. The Am6112 is capable of completing a 12-bit conversion in typically three microseconds and can handle input voltage ranges of 0 to 10V, and ±5V without external components.

The Am6112 has four modes of microprocessor operation, and a stand-alone mode. These modes are software programmable, except for the stand-alone mode which is pin selectable. Applications include analog I/O subsystems, servo-control and high-speed digital signal processing of analog events.

Am6112 EQUIVALENT CIRCUIT

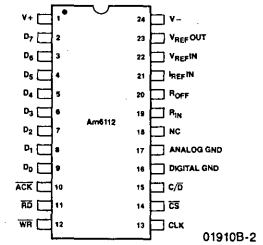


ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type	Temperature Range
AM6112DC	Hermetic DIP	0 to +70°C
AM6112XC	Dice	0 to +70°C
AM6112DM	Hermetic DIP	−55 to +125°C

CONNECTION DIAGRAM — Top View
D-24-1



Note: Pin 1 is marked for orientation.

01910B-ANA

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.3 to +7.0V	Voltage at R_{IN}, R_{OFF}	±12V
V− to D GND	+0.3 to −7.0V	Open Collector Current	20mA
Max Differential V+ to V−	±12V	Operating Temperature	0 to +70°C
Digital Inputs to D GND	−0.5 to +6.0V	Storage Temperature	−65 to +150°C
A GND to D GND	±1V	Lead Temperature (Soldering 60 sec)	300°C
V_{REF} Max Output Current	15mA	Minimum Operating Voltage	9.7V
Max Input Current at REF_{IN}	2mA	Max Package Dissipation	1W
Voltage at GAIN R, REF_{IN}	V− to V+		

ELECTRICAL CHARACTERISTICS (These specifications apply for $V^+ = +5V \pm 5\%$, $V^- = -5.2V \pm 5\%$, V_{REF} connected per connection diagram, $T_A = 25°C$, $F_{Clock} = 150kHz$, 0 to +10V input range, R_{OFF} open, stand-alone mode, unless otherwise stated)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristics						
	Resolution		12	12	12	Bits
	Monotonicity				12	Bits
	Differential Nonlinearity				±1	LSB
	Linearity			±1		LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error			±2		LSB
	Unipolar Offset Error			±1/2		LSB
	Bipolar Gain Error	V_{IN} = −5V to +5V		±4		LSB
	Bipolar Offset Error			±2		LSB
	Positive Power Supply Sensitivity	$V^+ = +5V \pm 5\%$		0.005		%FS
	Negative Power Supply Sensitivity	$V^- = -5.2V \pm 5\%$		0.005		%FS
Internal Reference						
V_{REF}	Reference Voltage	I_{REF} = 1mA	2.490	2.5	2.510	Volts
V_{REF}/T_A	Reference Voltage Tempco			8		ppm/°C
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		0.005		$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	$V^+ = +5V \pm 5\%$, $-5.2 \pm 5\%$		0.005		$\%V_{REF}$
	Noise, N = 10kHz to 1MHz					μV_{RMS}
Analog Inputs						
R_{IN}	**Input Resistance**					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
C_{IN}	**Input Capacitance**					
	R_{IN}, R_{OFF}, REF_{IN}, GAIN R			2		pF
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				0.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1	V_{IN} = 2.7V			40	μA
I_{IL}	Logic 0	V_{IN} = 0.4V			10	μA

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			0.5	Volts
I_{SC}	Output Short Circuit Current			−40		mA
I_{OZ}	Off-State Output Current					
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Power Requirements						
I^+	Positive Supply Current			40	80	mA
$I-$	Negative Supply Current			−60	−80	mA
	Power Dissipation			500	800	mW

SYSTEM TIMING

Parameters	Description	Min	Typ	Max	Units
t_{CONV}	Conversion Time R_{OFF} connected to A_{GND} or $V_{REF\ OUT}$ (Bipolar)		3.3		μs
	R_{OFF} Open (Unipolar)		10		μs
t_{CL}	CLK Low		125		ns
t_{CH}	CLK High		125		ns

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as either the number of output bits, or 1 part in 2^n where n is the number of bits.

Monotonicity (Missing Codes): Monotonicity is a property of the DAC within a successive approximation ADC. Each increment in the digital code to the DAC is accompanied by an analog output that is greater than or equal to that of the proceeding code. Monotonicity of the DAC is a necessary requirement for a successive approximation ADC to have no missing codes.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input which produces a given digital output code. An ideal value of a code width is equivalent to FSR/2^n, where in is the number of bits.

Linearity: The deviation of each individual code from an ideal straight line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an *inherent* ±1/2 LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2 LSB.

Unipolar Offset Error: Difference between the ideal (+1/2 LSB) and the actual analog input level required to produce the first digital code transition (00 . . . . 00 to 00 . . . . 01) over the complete temperature range.

Bipolar Offset Error: Difference between the ideal (1/2 FSR − 1/2 LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 . . . . 11 to 10 . . . . 00).

Power Supply Sensitivity: A measure of the change in gain and offset of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: The measure of how long it takes for the A/D to arrive at the correct digital output code. It is the time between the clock edge that starts a conversion after receiving a start command and the edge of the status line ($\overline{CC}$) which signifies that the conversion is completed.

THEORY OF OPERATION

The Am6112 is a fully μP-compatible programmable 12-bit A/D converter. The device is initialized by writing a 3-bit word into the internal command register via the bidirectional data pins D_0-D_2; in this operation, bits D_1 and D_2 configure the converter into one of four modes, while D_0 provides the choice of either offset-binary or two's complement output code. A fifth mode is pin selectable and is a unique stand-alone mode in which the internal command register is programmed whenever the control inputs READ ($\overline{RD}$) and WRITE ($\overline{WR}$) are LOW together.

The Am6112 has the standard μP peripheral control lines, CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), READ ($\overline{RD}$), plus one non-standard line, COMMAND/DATA (C/$\overline{D}$). The C/$\overline{D}$ control qualifies both the read and write operations. It defines a write operation as either an initialization or an external start conversion command, and during read cycles it steers either the upper or lower data byte to the data outputs.

The Am6112 requires an external clock (CLK) to control the conversion speed. The status output acknowledge ($\overline{ACK}$) is derived from the internal Conversion Complete ($\overline{CC}$) line, which indicates whether a conversion is in progress or completed.

The Successive Approximation Register performs the analog-to-digital conversion by sequentially testing the effect of removing the bit currents (B_{11} to B_0) of the D/A converter, which are all steered to the A/D summing node. The bit currents are binarily scaled versions of the reference current flowing into the D/A converter reference amplifier, and the voltage comparator decides whether the bit currents should be removed or retained. The reference current is obtained from the internal reference voltage source using the scale resistor connected to $V_{REF}OUT$. The Am6112 contains the necessary gain and range selection resistors enabling bipolar signals between −5V and +5V, and unipolar signals from 0 to +10V to be digitized. The device operates from +5 and −5.2V supplies.

Am6112 FUNCTIONAL PIN DESCRIPTION

$V_{REF}OUT$ 2.5V internal voltage reference output.

$V_{REF}IN$ Connected to an external voltage reference ($V_{REF}OUT$) to establish a reference current for the DAC bit currents.

$I_{REF}IN$ External reference current input for ratiometric operation.

R_{IN} Analog voltage input.

R_{OFF} When connected to $V_{REF}OUT$, 1/2 scale offset is generated to accomodate bipolar analog input signals.

D_0-D_7 Three-state data lines. D_0-D_2 are bidirectional data lines, while D_3-D_7 are strictly output data lines. Data is loaded into the internal COMMAND register via D_0-D_2 to select one of four modes of operation. D_0-D_7 are used to output the 8 LSBs (B_0-B_7). D_0-D_3 are used to output the 4 MSBs (B_8-B_{11}) of the 12-bit data, while D_4-D_7 output the sign bit (B_{11}).

$\overline{WR}$ Active low input used to reset the SAR and start a conversion cycle (Modes 0 and 3). This input line is also used to load data into the command register along with C/$\overline{D}$ line held high.

$\overline{RD}$ Active low input used to read the SAR data. SAR data is read in two bytes. The reading of the high byte (B_8-B_{11}) or low byte is user selectable except during Mode 2 via the C/$\overline{D}$ line (see Status Truth Table).

C/$\overline{D}$ Used in loading the COMMAND register with an active $\overline{WR}$ or outputting the HIGH and LOW data bytes with an active $\overline{RD}$ (see Status Truth Table).

$\overline{CS}$ Active low input allows the Am6112 to be involved in I/O operations (see Status Truth Table).

$\overline{ACK}$ Open collector, active low output indicating the status of the Am6112.

CLK Clock input synchronizing and controlling the operation of the Am6112.

V+ +5V power supply input.

V− −5.2 power supply input.

AGND Analog ground.

DGND Digital ground.

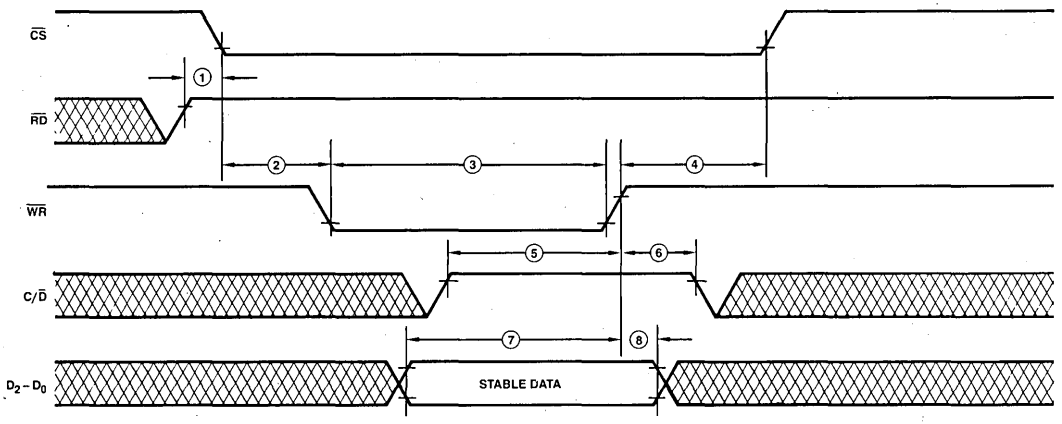
Am6112 Control Signal Decoding

STATUS TRUTH TABLE				
Control Logic Inputs				
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	C/$\overline{D}$	Am6112 Status
1	X	X	X	Output Data Lines (D_7-D_0) in High Impedance State
0	0	0	X	Forced to STAND-ALONE MODE Operation
0	1	0	1	Write into Command Register to Select Mode of Operation
0	0	1	0	Read 8 LSBs (Low Byte), Except in MODE 2
0	0	1	1	Read 4 MSBs (High Byte), Except in MODE 2
0	1	0	0	Start Conversion (MODES 0, 3 and Stand-Alone)
0	0	1	0	Start Conversion, MODE 1

INITIALIZATION TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{RD}-\overline{CS}}$	$\overline{RD}$ HIGH to $\overline{CS}$ LOW ($\overline{RD}$ Setup)	10			ns
2	$t_{\overline{SCS}-\overline{WR}}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW ($\overline{CS}$ Setup)	10			ns
3	$t_{\overline{WR}}$	$\overline{WR}$ Pulse Width	100			ns
4	$t_{\overline{WR}-\overline{CS}}$	$\overline{WR}$ HIGH to $\overline{CS}$ LOW ($\overline{WR}$ Hold)	10			ns
5	$t_{SC/\overline{D}-\overline{WR}}$	C/$\overline{D}$ HIGH to $\overline{WR}$ HIGH (C/$\overline{D}$ Setup)	100	30		ns
6	$t_{HC/\overline{D}-\overline{WR}}$	$\overline{WR}$ HIGH to C/$\overline{D}$ HIGH (C/$\overline{D}$ Hold)	10			ns
7	$t_{SD-\overline{WR}}$	Data Setup Time	100			ns
8	$t_{HD-\overline{WR}}$	Data Hold Time	20			ns

INITIALIZATION TIMING DIAGRAM



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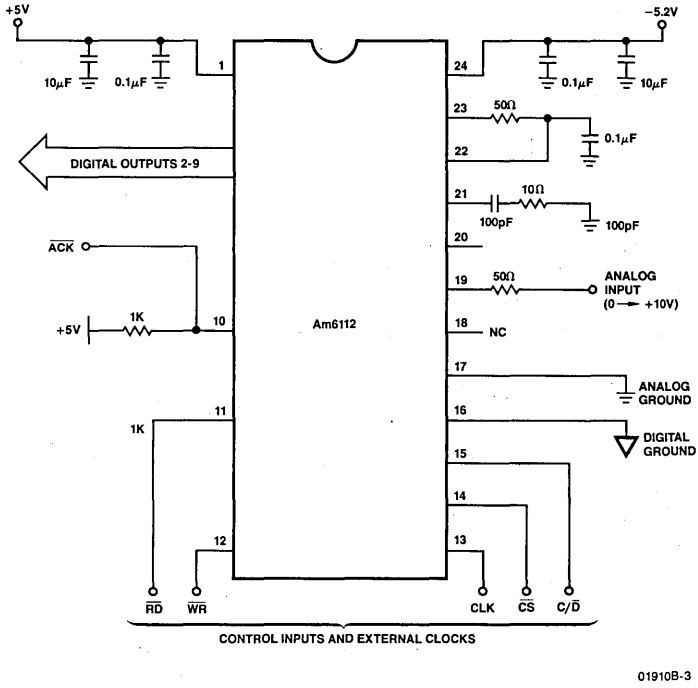
Am6112 COMMAND REGISTER DECODING

Mode/Coding Format Truth Tables			
Command Register Bits			
D_2	D_1	D_0	Mode Description
X	X	0	Offset binary output
X	X	1	Two's complement output code (except stand-alone mode).
0	0	X	MODE 0 – Am6112 under microprocessor control. Conversion cycles started by active $\overline{WR}$. Internal status ($\overline{CC}$) gated with $\overline{RD}$ and $\overline{CS}$.
0	1	X	MODE 1 – Am6112 under microprocessor control. Conversion cycles started by active $\overline{RD}$. Internal status ($\overline{CC}$) gated with $\overline{RD}$ and $\overline{CS}$.
1	0	X	MODE 2 – Am6112 under DMA control (such as the Am9517A). Conversion cycles started by active $\overline{RD}$. Data outputted as 8 LSBs first and then the 4 MSBs. Output data control is done internally and not accessible by the user.
1	1	X	MODE 3 – Am6112 under microprocessor control. Conversion cycles started by active $\overline{WR}$. Internal status ($\overline{CC}$) gated with $\overline{CS}$ only.

TEST CIRCUIT – Top View



CALIBRATION TEXT

Unipolar Configuration (Figure 1)

The Am6112 contains all the active components required to perform a complete 12-bit A/D conversion. All that is necessary, in most situations, is the connection of the power supplies (+5V and −5.2V), analog input, and conversion initiation command, discussed later. The Am6112 has a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of the code. If no trims are used, the Am6112 has a typical zero offset error of ±1/2 LSB, and gain error of ±2 LSB. When no trims are required R_{OFF} should be left open for the best DNL specification (refer to accuracy versus DNL curve). If the gain error (full-scale) trim is not required, potentiometer R_4 should be replaced with 50Ω precision resistor matched to R_5.

Unipolar Calibration

Connecting R_{OFF} to R_1 and R_2, the initial offset error can be trimmed by R_3. The first A/D transition (0000 0000 0000 to 0000 0000 0001) should occur for an input level of +1/2 LSB (1.22mV).

The gain error (full-scale) trim is done by applying a signal 1/2 LSB's below the nominal full-scale (9.9964V). R_4 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

Bipolar Configuration (Figure 2)

If the offset and gain errors are acceptable, potentiometers R_1 and R_2 should be replaced by precision 25 and 50Ω resistors respectively.

Bipolar Calibration

Bipolar calibration is similar to unipolar calibration. First, a signal +1/2 LSB above negative full scale (−4.9988V for the ±5V input range) is applied to R_3 and potentiometer R_1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2 LSB below positive full-scale (4.9963V) is applied and potentiometer R_2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

Offset and gain calibration can be more accurately trimmed by summing a small triangular wave voltage to the analog input signal, and the digital outputs monitored to determine the center point of the code transition.

Figure 1. Am6112 Unipolar Configuration

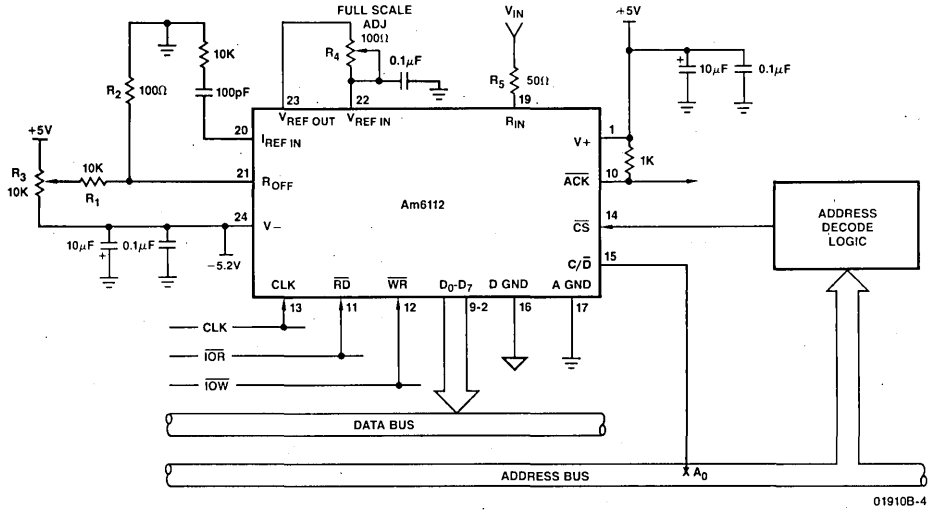
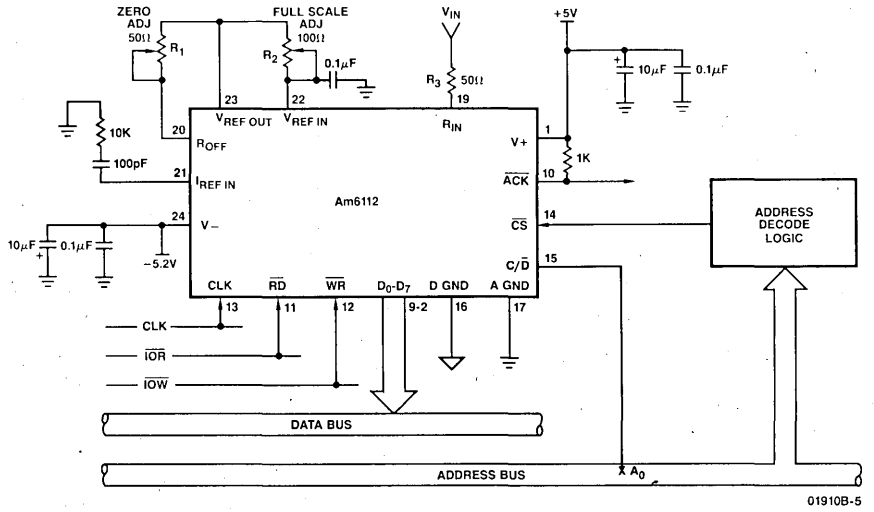


Figure 2. Am6112 Bipolar Configuration



APPLICATIONS INFORMATION

Depending on the processor used and throughput rate required, the user can select up to five operating modes.

In MODE 0, the conversion cycle is started by an active write ($\overline{WR}$) and the next two read ($\overline{RD}$) commands send the data out. The status of the command/data (C/$\overline{D}$) line determines whether the output data consists of the eight LSBs or four MSBs. In this mode, as well as Modes 1 and 2, the $\overline{ACK}$ line reflects the ADC's status during an active read period. For example, if conversion complete ($\overline{CC}$) is high during the entire read period, $\overline{ACK}$ is also high. $\overline{ACK}$ can then be used to extend the I/O read cycle if desired.

In MODE 1, a conversion cycle is started by an active read. Reading of the 12-bit data and the action of the $\overline{ACK}$ output is similiar to Mode 0. This mode is well suited to microprocessors such as the Z80 and Z8000 which have data-block transfer as part of their repertoire. The first 12-bit data output is invalid in this mode because the conversion cycle does not start until the positive transition of the second read pulse.

MODE 2 puts the A/D converter under control of a DMA controller such as the Am9517A. During DMA transfer, the microprocessor is disabled, and the Am9517A provides all the signals to control the conversion process. In Mode 2, the A/D converter internally controls the output of the data bytes. The first read signal sends out the 8 LSBs and simultaneously saves the four MSBs into an internal latch.

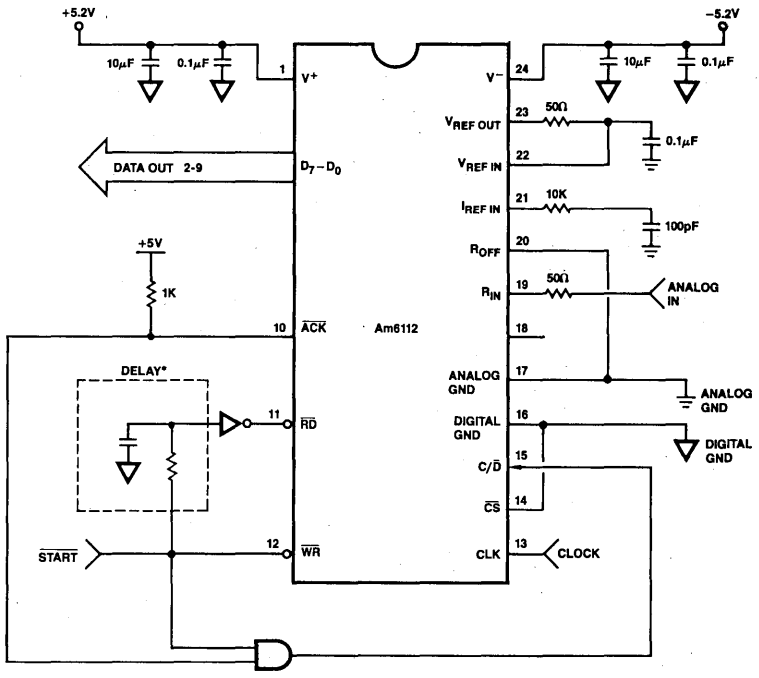
The LOW-to-HIGH transition of the first read initiates another conversion cycle. A second read cycle sends out the latched MSBs at the same time the A/D converter is performing the next conversion. The $\overline{ACK}$ output is internally masked so that the conversion complete ($\overline{CC}$) does not extend the second read cycle.

MODE 3 is similar to Mode 0 except that the $\overline{ACK}$ line reflects the A/D converter's true status. This difference in the decoding of the $\overline{ACK}$ line provides flexibility in the microprocessor handshaking. Although tying the $\overline{ACK}$ line to the microprocessor's Wait input pin might reduce throughput, by adding additional Wait states, it does guarantee full 12-bit conversion cycles.

MODE 4 is a unique stand-alone mode, in which the internal command register is preprogrammed to operate with offset binary data output format. Mode 4 is programmed whenever RD and $\overline{WR}$ are low together. This situation is an illegal state with any microprocessor-based system.

In Figure 3, $\overline{CS}$ can be grounded at all times. Applying a start pulse to the $\overline{WR}$ pin initiates two events. First, because the pulse at $\overline{RD}$ is actually a delayed write signal, sometime after the start signal is applied, both $\overline{RD}$ and $\overline{WR}$ are low at the same time, and the Am6112 is forced to Mode 4 operation. Secondly, $\overline{WR}$ going high after this delay starts the A/D conversion cycle, as long as C/$\overline{D}$ is LOW. The data can be read as soon as $\overline{RD}$ returns low. The $\overline{ACK}$ line acts as a conversion complete signal which provides a simple means of steering the data bytes to the data outputs. $\overline{ACK}$ is gated with $\overline{WR}$ so that C/$\overline{D}$ will always be low whenever a conversion cycle is required.

Figure 3. Stand-Alone Mode



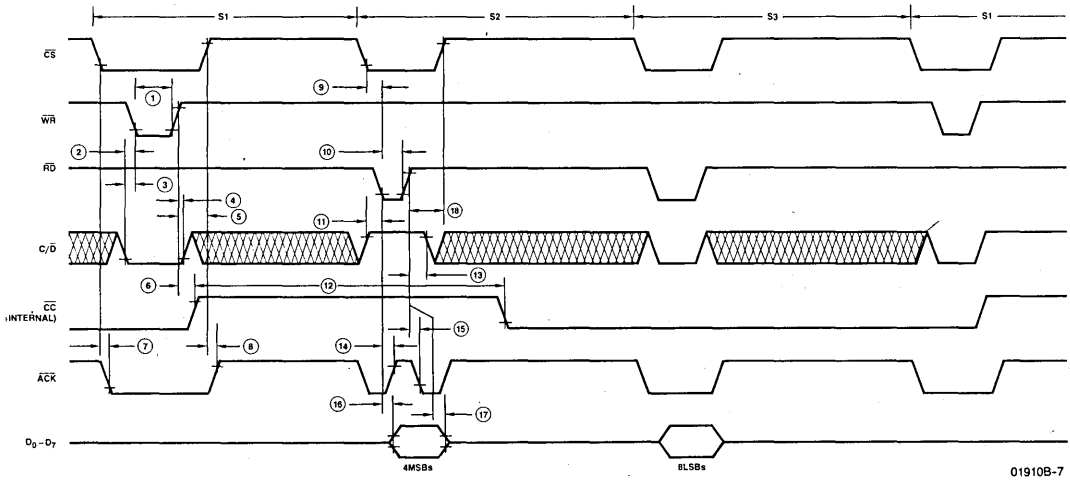
*Delay can be implemented with logic gates.

Am6112
MODE 0 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{WR}L}$	$\overline{WR}$ LOW	100			ns
2	$t_{C/\overline{D}L-WL}$	C/$\overline{D}$ LOW to $\overline{WR}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-WL}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup	20			
4	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
5	$t_{WH-\overline{CS}H}$	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold	20			
6	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
8	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay	20	50	100	ns
9	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW	20			ns
10	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
11	$t_{C/\overline{D}-RL}$	C/$\overline{D}$ to $\overline{RD}$ LOW Setup	20			ns
12	t_{CONV}	Conversion Time	14 CLK			
13	$t_{RH-C/D}$	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold	10			ns
14	$t_{RL-\overline{ACK}H}$	$\overline{RD}$ LOW to $\overline{ACK}$ HIGH Delay		50	100	ns
15	$t_{RH-\overline{ACK}L}$	$\overline{RD}$ HIGH to $\overline{ACK}$ LOW Delay		50	100	ns
16	$t_{RL-DTVLD}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
17	$t_{\overline{CS}H-DTVLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns
18	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to CS HIGH	20			

*Note: t_{CLK} = 1 Clock Period.

MODE 0 TIMING DIAGRAM



S_1 – Start a conversion cycle with an active WR.

S_2 – Read first data byte. The 4 MSBs become valid 6 clock periods after $\overline{CC}$ goes high. Therefore, the 4 MSBs may be read during S_2 while the conversion cycle is in progress. If conversion is done ($\overline{CC}$ going low) prior to S_2, then either the 4 MSBs or the 8 LSBs may be read first and the ACK signal during S_2 and S_3 is the same as during S_1. If the conversion time is longer than S_1 + S_2, then the $\overline{ACK}$ signal can be used to extend the active part of S_2.

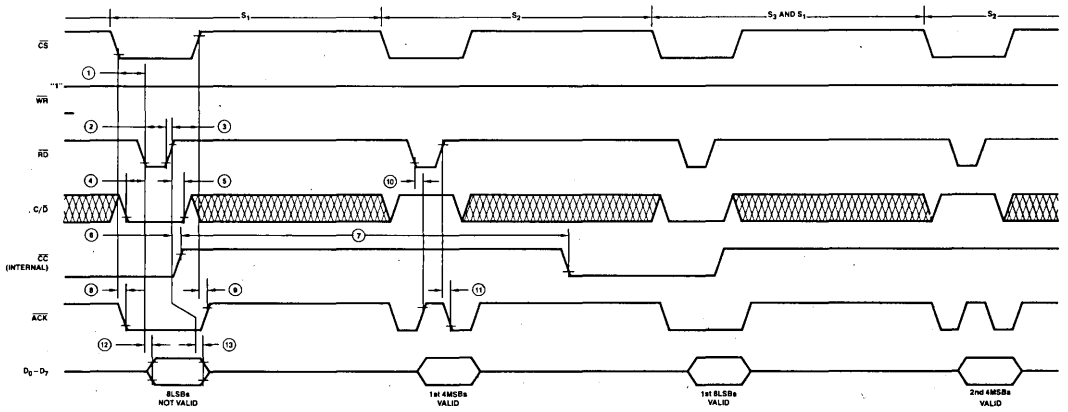
S_3 – Read second data byte.

MODE 1 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{CSL}-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	20			ns
2	$t_{\overline{RDL}}$	$\overline{RD}$ LOW	100			ns
3	$t_{RH-\overline{CSH}}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	20			ns
4	$t_{C/\overline{D}-\overline{CSL}}$	C/$\overline{D}$ to $\overline{RD}$ LOW Setup	10			ns
5	$t_{RH-C/\overline{D}}$	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold	10			ns
6	$t_{RH-\overline{CCH}}$	$\overline{RD}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	t_{CONV}	Conversion Time	14 CLK			
8	$t_{\overline{CSL}-\overline{ACKL}}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
9	$t_{\overline{CSH}-\overline{ACKH}}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
10	$t_{RL-\overline{ACKH}}$	$\overline{RD}$ LOW to $\overline{ACK}$ HIGH Delay		50	100	ns
11	$t_{RH-\overline{ACKL}}$	$\overline{RD}$ HIGH to $\overline{ACK}$ LOW Delay		50	100	ns
12	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
13	$t_{RH-DTHLD}$	RD HIGH to Data Hold	20			ns

*Note: t_{CLK} = 1 Clock Period.

MODE 1 TIMING DIAGRAM



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S_1 – Start the first conversion cycle with an active RD. The 8 LSBs read are not valid.

S_2 – Read the first valid 4 MSBs. The 4 MSBs become valid 6 clock periods after CC goes high. Therefore, the 4 MSBs may be read during S_2 while the conversion cycle is in progress. If conversion ends prior to S_2, then either the 4 MSBs or the 8 LSBs may be read first and the ACK signal during S_2 is the same as during S_1. If the converison time is longer than S_2, then the $\overline{ACK}$ signal can be used to extend the active part of S_2.

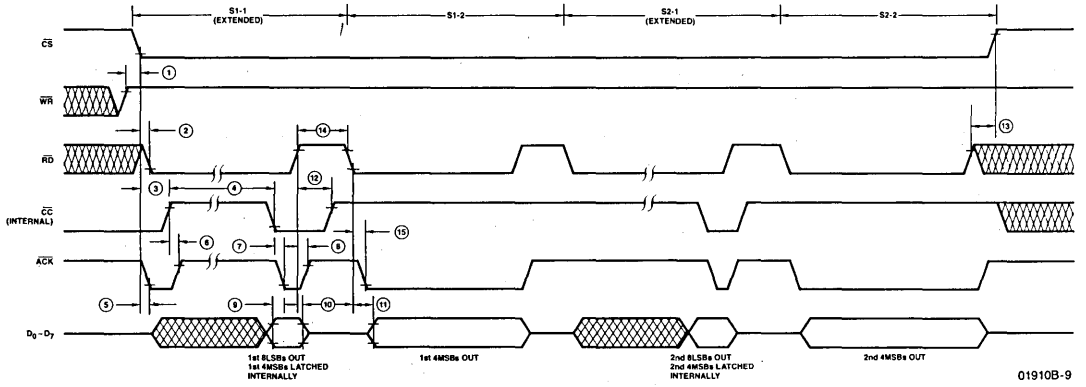
S_3 and S_1 – Read the first valid 8 LSBs and start the next conversion cycle.

Am6112
MODE 2 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{WH-\overline{CSL}}$	$\overline{WR}$ HIGH to $\overline{CS}$ LOW Setup	10			ns
2	$t_{\overline{CSL}-\overline{RDL}}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	10			ns
3	$t_{\overline{CSL}-\overline{CCH}}$	$\overline{CS}$ LOW to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
4	t_{CONV}	Conversion Time	14 CLK			
5	$t_{\overline{CSL}-\overline{ACKL}}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
6	$t_{\overline{CCH}-\overline{ACKH}}$	$\overline{CC}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
7	$t_{\overline{CCL}-\overline{ACKL}}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
8	$t_{RH-\overline{ACKH}}$	$\overline{RD}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
9	$t_{LB-\overline{ACKL}}$	Data to $\overline{ACK}$ LOW	20	50		ns
10	$t_{RH-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20	35		ns
11	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
12	$t_{RH-\overline{CCH}}$	$\overline{RD}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
13	$t_{RH-\overline{CSH}}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	10			ns
14	t_{RH}	$\overline{RD}$ HIGH	50			ns
15	$t_{RL-\overline{ACKL}}$	$\overline{RD}$ LOW to $\overline{ACK}$ LOW		50	100	ns

*Note: t_{CLK} = 1 Clock Period.

MODE 2 TIMING DIAGRAM



$S_{1\text{-}1}$ – Start first conversion with $\overline{CS}$ going LOW. First 4 MSBs are latched internally. First 8 LSBs are valid when $\overline{CC}$ goes LOW. Note that $S_{1\text{-}1}$ cycle is extended by the insertion of wait states using the $\overline{ACK}$ signal. Second conversion starts after $\overline{RD}$ goes HIGH.

$S_{1\text{-}2}$ – Read first 4 MSBs. Note that this cycle is not extended.

$S_{2\text{-}1}$ – This cycle is similar to the $S_{1\text{-}1}$ cycle.

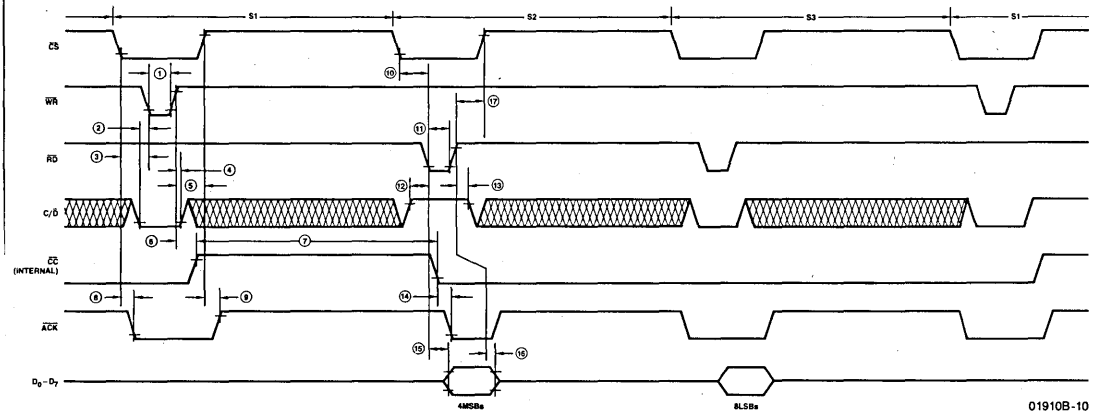
$S_{2\text{-}2}$ – This cycle is similar to the $S_{1\text{-}2}$ cycle except that conversion cycles are inhibited after $\overline{CS}$ goes HIGH.

MODE 3 TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{WR}L}$	$\overline{WR}$ LOW	100			ns
2	$t_{C/\overline{D}-WL}$	C/$\overline{D}$ LOW to $\overline{WR}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-WL}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup	20			
4	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
5	$t_{WH-\overline{CS}H}$	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Setup	20			
6	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	t_{CONV}	Conversion Time	14 CLK			
8	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
9	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
10	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	10			ns
11	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
12	$t_{C/\overline{D}H-RL}$	C/$\overline{D}$ HIGH to $\overline{RD}$ LOW Setup	10			ns
13	$t_{RH-C/\overline{D}H}$	$\overline{RD}$ HIGH to C/$\overline{D}$ HIGH Hold	10			ns
14	$t_{\overline{CC}L-\overline{ACK}L}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW Delay				ns
15	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
16	$t_{\overline{CS}H-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns
17	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH				

*Note: t_{CLK} = 1 Clock Period.

MODE 3 TIMING DIAGRAM



S_1 – Start a conversion cycle with an active $\overline{WR}$.

S_2 – Read first data byte. The 4 MSBs become valid 6 clock periods after $\overline{CC}$ goes high. Therefore, the 4 MSBs may be read during S_2 while conversion cycle is in progress. If conversion is done ($\overline{CC}$ has gone low) prior to S_2, then either the 4 MSBs or the 8 LSBs may be read first and the ACK signal during S_2 and S_3 is the same as during S_1. If conversion ends during active part of S_2 ($\overline{CS}$ low) $\overline{ACK}$ output is as shown above. If the conversion time is longer than S_1 + S_2, then the ACK output can be used to extend the active part of S_2.

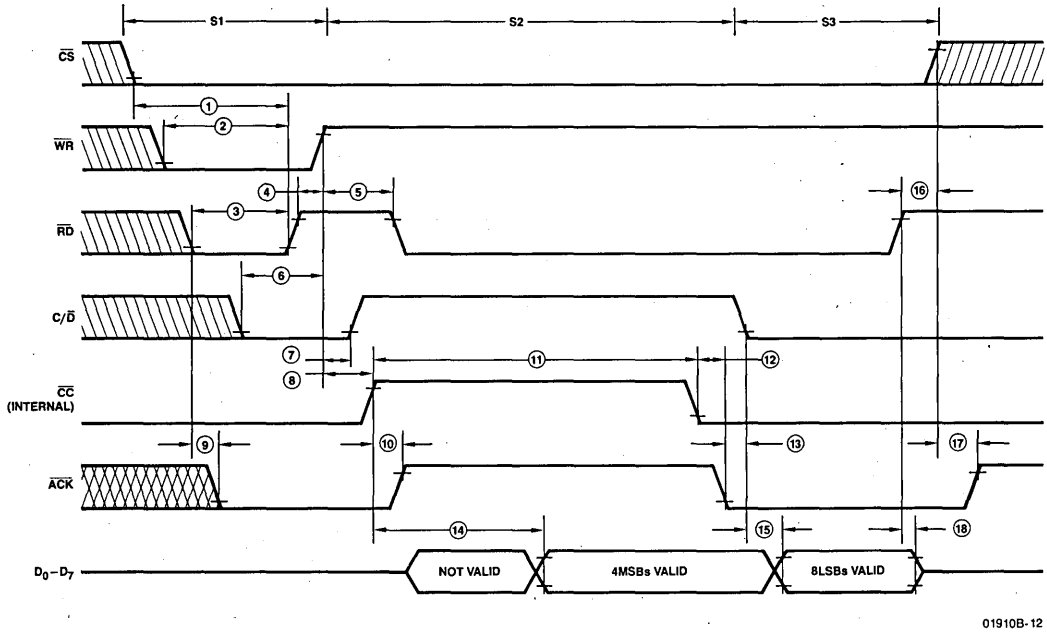
S_3 – Read second data byte.

Am6112
STAND-ALONE MODE TIMING TABLE

Number	Parameters	Description	Min	Typ	Max	Units
1	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	100			ns
2	t_{WL-RL}	$\overline{WR}$ LOW to $\overline{RD}$ LOW Setup	100			ns
3	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
4	t_{RH-WH}	$\overline{RD}$ HIGH to $\overline{WR}$ HIGH Setup	10			ns
5	t_{WH-RH}	$\overline{WR}$ HIGH to $\overline{RD}$ HIGH Hold	20			ns
6	$t_{C/\overline{D}L-WH}$	C/$\overline{D}$ LOW to $\overline{WR}$ HIGH Setup	110			ns
7	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
8	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
9	$t_{RL-\overline{ACK}L}$	$\overline{RD}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
10	$t_{\overline{CC}H-\overline{ACK}H}$	$\overline{CC}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
11	t_{CONV}	Conversion Time	14 CLK			
12	$t_{\overline{CC}L-\overline{ACK}L}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW		50	100	ns
13	$t_{\overline{ACK}L-C/\overline{D}L}$	$\overline{ACK}$ LOW to C/$\overline{D}$ LOW	0			ns
14	$t_{\overline{CC}H-UBVLD}$	$\overline{CC}$ HIGH to Upper Byte Valid (Note 1)		4.5	t_{CLK} + 50*	ns
15	$t_{C/\overline{D}L-LBVLD}$	C/$\overline{D}$ LOW to Lower Byte Valid		50	100	ns
16	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH Setup	10			ns
17	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		50	100	ns
18	$t_{RH-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns

*Note: t_{CLK} = 1 Clock Period.

STAND-ALONE TIMING DIAGRAM



01910B-12

S_1 – Initialize Am6112 to stand-alone mode and start conversion cycle.

S_2 – Read valid 4 MSBs.

S_3 – Read valid 8 LSBs.

Microprocessor Interfacing

The Am6112 provides a variety of interfacing options. For example, Mode 0 is suitable for microprocessor-based systems with low throughput and the conversion process is directly under microprocessor control. This approach results in a minimum of hardware. In operation, the microprocessor initiates a conversion and is then forced into a Wait state which prevents the processor from performing other tasks until the conversion is complete and the A/D converter's data can be read.

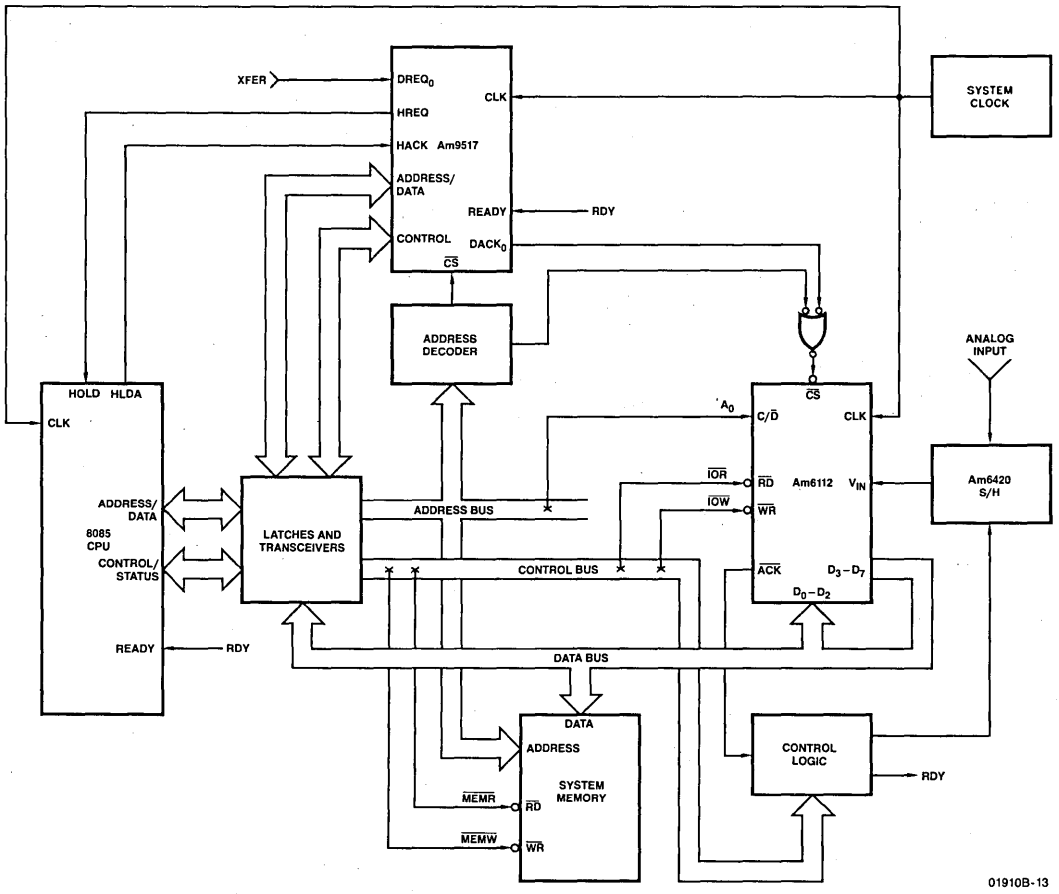
Am6112 with DMA in an 8-Bit System

The 8-bit output data structure of the Am6112 enables it to be easily designed into 8-bit CPU systems. In minimum system configuration with DMA capability, the 8085 CPU programs the Am6112 to operate in Modes 0, 1, 2 or 3 (Figure 4). Except for Mode 2, the CPU controls the conversion cycles and the transfer of data, which can then be stored in the internal register for immediate processing or in system memory for the case of data collection.

The $\overline{ACK}$ of the A/D converter is fed into the CONTROL LOGIC and controls the READY input of the 8085 and the Am9517A DMA controller. This is done to insert Wait states when the Am6112 conversion cycle is longer than the 8085 I/O instruction cycle. The $\overline{ACK}$ signal also controls the Am6420 Sample (track) and Hold (S/H) so that while it is HIGH the S/H is in the HOLD mode, and when it goes LOW the S/H is set to the tracking or sampling mode.

Whenever a DMA transfer is requested on channel 0, the Am9517A responds by setting the HREQ line HIGH to tell the 8085 that it wants to control the bus. The microprocessor relinquishes its control of the bus by making the Hold Acknowledge (HLDA) active. The microprocessor is then basically disabled, and the Am9517A provides all the signals necessary to control the DMA transfer process.

Figure 4. Am6112 In Minimum 8-Bit System Configuration with DMA Capability



Am6112 data transfer may be controlled by CPU (mode 0, -1, -3) or by the Am9517 DMA controller (mode 2) for faster throughput rate.

The DMA controller has four channels ($DREQ_0 - DRE_3$) where four peripheral devices may request service. Each channel has four 16-bit registers (base and current address, and base and current word count) and a mode register accessible via address lines $A_0 - A_3$. The base registers allow the channels to be automatically reinitialized at the end of a DMA transfer, and DMA requests may be either hardware- or software-generated. Auto-initialization is selected by programming the mode register. Other internal registers are programmed to set the desired operations and options.

Among the Am9517 operating modes are two called Single Transfer and Block Transfer. In the Single Transfer mode, a word is transferred for each DMA request, while Block Transfer allows the Am9517A to make continuous transfer until the word count for the active channel goes to zero.

High-Speed Analog I/O Processing

Because the Am9517A cannot control the buses concurrently with the 8085 microprocessor, the microprocessor is idle while DMA transfer is in progress. For large data block transfers, this period can be very significant even though the transfer rate is extremely fast.

The limitation associated with the shared-bus structured can be solved by dedicating a device, such as another microprocessor, to deal with the Am6112 and other I/O devices in conjunction with the main microprocessor. However, most general purpose microprocessor's are not really suited for the task of I/O device control and processing will probably still need a DMA controller to provide DMA capability.

A more powerful and attractive solution uses a dedicated device such as the Am8089 I/O processor (IOP). The Am8089 IOP contains two independent channels with high-speed DMA capability, and its instruction set is extensively I/O-oriented. The bus organization of the IOP is flexible so that data transaction is possible between 8-bit organized I/O devices and 16-bit wide memory or vice versa.

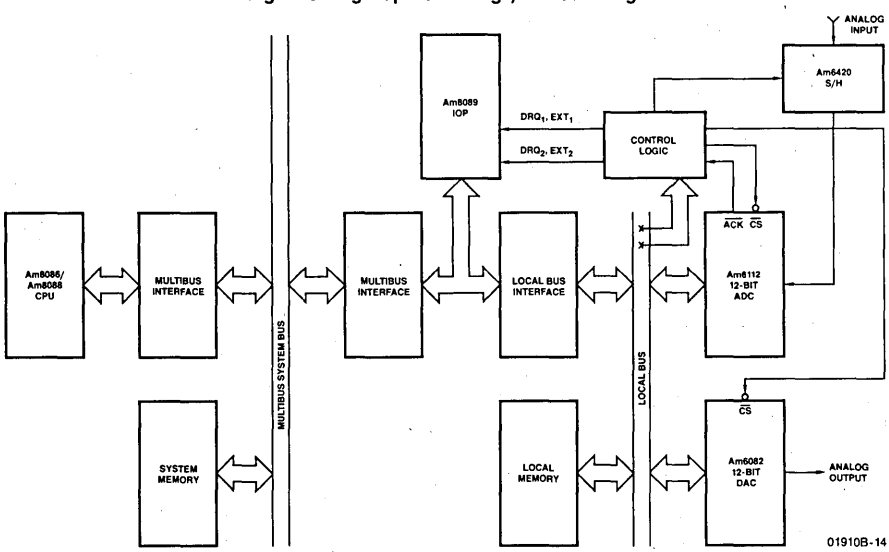
Figure 5 illustrates such a system architecture for high-speed analog I/O processing. Before being able to perform I/O tasks, the Am8089 must be initialized by the Am8086/88 microprocessor, configured in MAXIMUM mode. The system bus is separated from the local bus to allow for parallel processing, and the IOP's channel program may reside in the local memory space to further reduce system bus contention. The Am6112 may be initialized by the IOP, and data transactions from the Am6112, Am6082 and local memory is then confined by the Am8089 to the local bus. DMQ_1 and DMQ_2 are DMA request lines associated with the Am6112 and the Am6082. DMA transfers may be terminated externally via EXT_1 and EXT_2.

High-Resolution System Design Guidelines

The design of high-resolution or low-level analog/digital systems must include a thorough analysis of conditions that can degrade overall system accuracy. Consider the source impedance of the device driving the input of the Am6112. The input impedance of the converter is modulated during the conversion cycle because currents of different values appear at the node where the ADC presents itself as a load to the S/H device. The output impedance of the S/H must be sufficiently low at all operating frequencies to avoid errors and, in addition, the S/H device output must settle to the required voltage level before a bit current comparison can be made. This means that the output transient response of the S/H must be able to cope with the 1/2 clock period settling time requirement for each bit current comparison.

Additional system errors can be caused by improper placement of the circuit components. Analog and digital components must be isolated from each other with lots of ground plane. Analog circuits must be as close together as possible to make the signal paths as short as possible. Ground loops within the analog section must be avoided.

Figure 5. High-Speed Analog I/O Processing



Separate local bus for the analog I/O devices allows for high throughput without sacrificing CPU capabilities. Am8089 does all I/O related routine in parallel with CPU tasks and eliminates system bus contention due to I/O servicing.

Data Acquisition Products – Section III

DAC-08

8-Bit High Speed Multiplying D/A Converter

Distinctive Characteristics

- Fast settling output current – 85nsec
- Full scale current prematched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Nonlinearity to ±0.1% max over temperature range
- High output impedance and compliance
  –10V to +18V
- Differential current outputs
- Wide range multiplying capability
  1.0MHz bandwidth
- Low FS current drift – ±10ppm/°C
- Wide power supply range – ±4.5V to ±18V
- Low power consumption – 33mW @ ±5V

3

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 nsec settling times with very low "glitch" and a low power consumption. Monotonic multiplying performance is attained over more than a 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

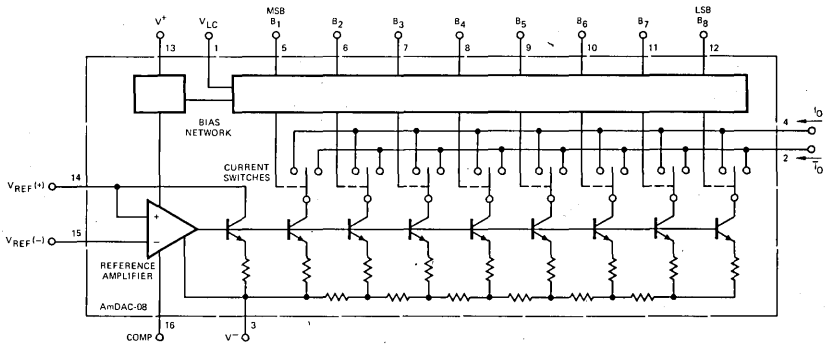
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. All devices are processed to MIL-STD-883.

DAC-08 applications include 8-bit, 1.0μsec A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



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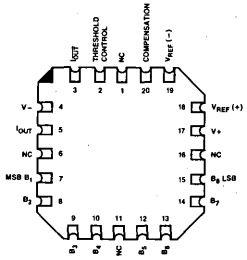
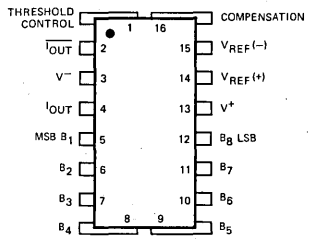
CONNECTION DIAGRAMS – Top Views

Leadless Chip-Pak
L-20-1



P-16-1
D-16-1



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Note: Pin 1 is marked for orientation.

DAC-08
MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

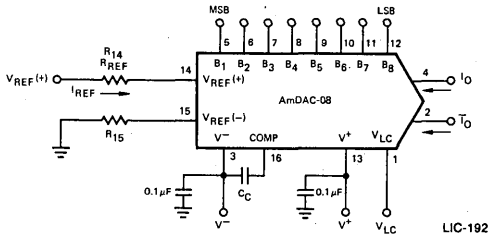
Operating Temperature	
DAC-08AQ, Q, AL, L	–55°C to +125°C
DAC-08EQ, CQ, HQ, EN, CN, HN	0°C to +70°C
Storage Temperature	–65°C to +150°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

V+ supply to V– Supply	36V
Logic Inputs	V– to V+ plus 36V
V_{LC}	V– to V+
Analog Current Outputs	See Fig. 12
Reference Inputs (V_{14}, V_{15})	V– to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	5.0mA

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0mA)

Parameter	Description		Test Conditions		AmDAC-08A AmDAC-08H Min.	AmDAC-08A AmDAC-08H Typ.	AmDAC-08A AmDAC-08H Max.	AmDAC-08 AmDAC-08E Min.	AmDAC-08 AmDAC-08E Typ.	AmDAC-08 AmDAC-08E Max.	AmDAC-08C Min.	AmDAC-08C Typ.	AmDAC-08C Max.	Units
	Resolution				8	8	8	8	8	8	8	8	8	Bits
	Monotonicity				8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity		T_A = MIN. to MAX.				±0.1			±0.19			±0.39	%FS
t_s	Settling Time		To ±1/2 LSB, all bits switched ON or OFF T_A = 25°C	DAC-08A DAC-08		85	135		85	135				ns
				DAC-08E DAC-08C					85	150		85	150	
t_{PLH}, t_{PHL}	Propagation Delay	Each Bit	T_A = 25°C			35	60		35	60		35	60	ns
		All Bits Switched				35	60		35	60		35	60	
TCI_{FS}	Full Scale Tempco					±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance		Full scale current change < 1/2 LSB R_{OUT} > 20MegΩ typ.		–10		+18	–10		+18	–10		+18	Volts
I_{FS4}	Full Scale Current		V_{REF} = 10.000 V R_{14}, R_{15} = 5.000 kΩ T_A = 25°C		1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry		$I_{FS4} - I_{FS2}$			±0.5	±4.0		±1.0	±8.0		±2.0	±16	µA
I_{ZS}	Zero Scale Current					0.1	1.0		0.2	2.0		0.2	4.0	µA
I_{FSR}	Output Current Range		V^- = –5.0 V		0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
			V^- = –12.0 V to –18 V		0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
V_{IL}	Logic Input Levels	Logic "0"	V_{LC} = 0 V				0.8			0.8			0.8	Volts
V_{IH}		Logic "1"			2.0			2.0			2.0			
I_{IL}	Logic Input Current	Logic "0"	V_{LC} = 0 V	V_{IN} = –10 V to +0.8 V		–2.0	–10		–2.0	–10		–2.0	–10	µA
I_{IH}		Logic "1"		V_{IN} = 2.0 V to 18 V		0.002	10		0.002	10		0.002	10	
V_{IS}	Logic Input Swing		V^- = –15V		–10		+18	–10		+18	–10		+18	Volts
V_{THR}	Logic Threshold Range		V_S = ±15V		–10		+13.5	–10		+13.5	–10		+13.5	Volts
I_{15}	Reference Bias Current					–1.0	–3.0		–1.0	–3.0		–1.0	–3.0	µA
dI/dt	Reference Input Slew Rate				4.0	8.0		4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity		V^+ = 4.5 V to 18 V			±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
$PSSI_{FS-}$			V^- = –4.5 V to –18 V I_{REF} = 1.0mA			±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	
I^+	Power Supply Current		V_S = ±5.0V, I_{REF} = 1.0mA			2.3	3.8		2.3	3.8		2.3	3.8	mA
I^-						–4.3	–5.8		–4.3	–5.8		–4.3	–5.8	
I^+			V_S = +5.0V, –15V, I_{REF} = 2.0mA			2.4	3.8		2.4	3.8		2.4	3.8	
I^-						–6.4	–7.8		–6.4	–7.8		–6.4	–7.8	
I^+			V_S = ±15 V, I_{REF} = 2.0mA			2.5	3.8		2.5	3.8		2.5	3.8	
I^-						–6.5	–7.8		–6.5	–7.8		–6.5	–7.8	
P_D	Power Dissipation		±5.0V, I_{REF} = 1.0mA			33	48		33	48		33	48	mW
			+5.0V, –15V, I_{REF} = 2.0mA			108	136		108	136		108	136	
			±15V, I_{REF} = 2.0mA			135	174		135	174		135	174	

BASIC CONNECTIONS



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$$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ FOR ALL LOGIC STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$
$R_{REF} = 5.000k$
$R_{15} \approx R_{REF}$
$C_C = 0.01\mu F$
$V_{LC} = 0V$ (GROUND)

Figure 1. Basic Positive Reference Operation.

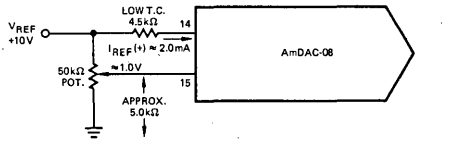

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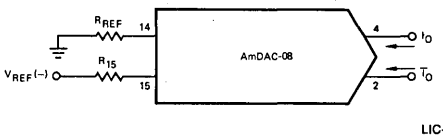
Figure 2. Recommended Full Scale Adjustment Circuit.

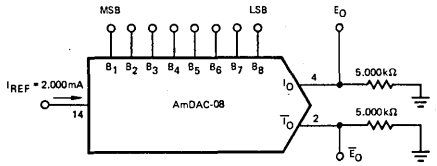


LIC-194

$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note 1. R_{REF} Sets I_{FS}; R_{15} is for Bias Current Cancellation.

Figure 3. Basic Negative Reference Operation.



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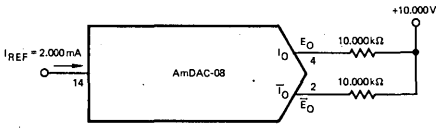
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I}_O$ mA	E_O	$\overline{E}_O$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	000	−9.960	000
FULL SCALE −LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	−.040
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	−.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Figure 4. Basic Unipolar Negative Operation.



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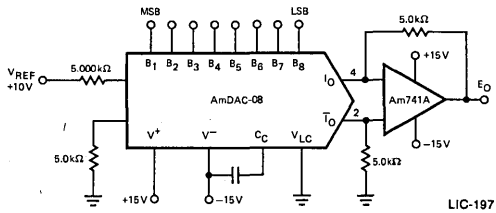
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E}_O$
POS FULL SCALE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+0.080
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 5. Basic Bipolar Output Operation.



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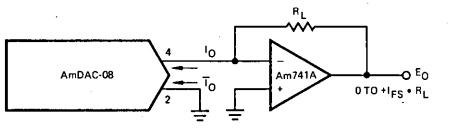
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.960
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	+9.880
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	−0.040
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	−9.880
NEG FULL SCALE	0	0	0	0	0	0	0	0	−9.960

Figure 6. Symmetrical Offset Binary Operation.

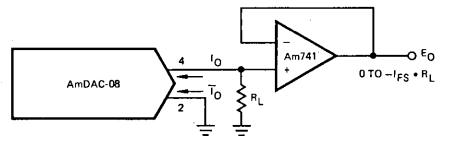
BASIC CONNECTIONS (Cont.)



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND

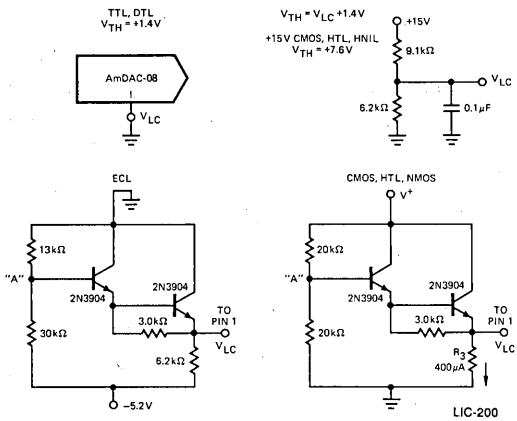
Figure 7. Positive Low Impedance Output Operation.



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

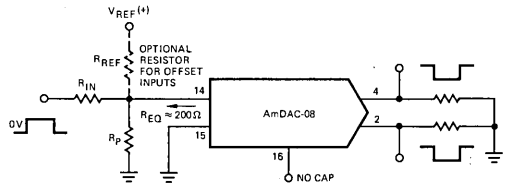
FOR COMPLEMENTARY (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 8. Negative Low Impedance Output Operation.



SET VOLTAGE AT NODE "A" EQUAL TO DESIRED LOGIC THRESHOLD.

Figure 9. Interfacing With Various Logic Families.



TYPICAL VALUES:
R_{IN} = 5k
$+V_{IN}$ = 10V

Figure 10. Pulsed Reference Operation.

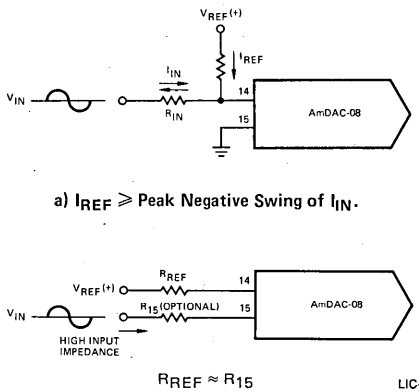
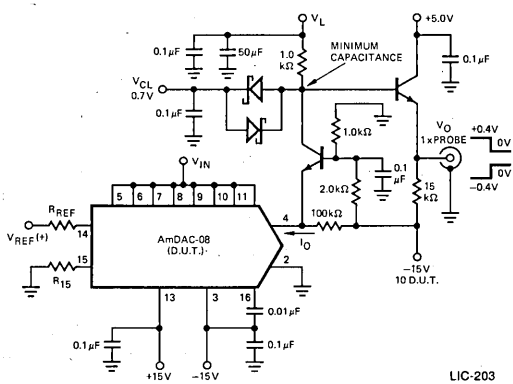


Figure 11. Accomodating Bipolar References.



FOR TURN-ON, V_L = 2.7V
FOR TURN-OFF, V_L = 0.7V

Figure 12. Settling Time Measurement.

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications (Fig. 1), an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15 (Fig. 3); reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Fig. 11. The negative common mode range of the reference amplifier is given by: V_{CM}− = V− plus (I_{REF} X 1.0kΩ) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Fig. 2.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0mA to 4.0μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0kΩ and C_C = 15pF, the reference amplifier slews at 4.0mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2.0mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Fig. 10. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

3

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus (I_{REF} X 1.0kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1.0mA is recommended. For interfacing other logic families, see Fig. 9. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, when $I_O + \overline{I}_O = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I}_O$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} • 1.0kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)(V+) + (I+)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85nsec at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35nsec for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35nsec, with each progressively larger bit taking successively longer. The MSB settles in 85nsec, thus determining the overall settling time of 85nsec. Settling to 6-bit accuracy requires about 65 to 70nsec. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

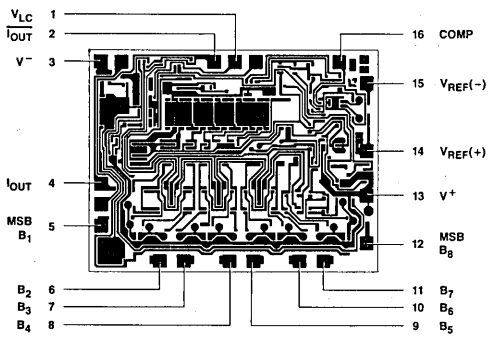
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Fig. 12 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients of "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.068" X 0.088"

ORDERING INFORMATION*

Order Number	Package Type	Temperature Range	Nonlinearity
DAC-08AQ	Ceramic DIP	−55 to +125°C	±0.1%
DAC-08Q	Ceramic DIP	−55 to +125°C	±0.19%
DAC-08AL	Leadless	−55 to +125°C	±0.1%
DAC-08L	Leadless	−55 to +125°C	±0.19%
DAC-08HQ	Ceramic DIP	0 to +70°C	±0.1%
DAC-08EQ	Ceramic DIP	0 to +70°C	±0.19%
DAC-08CQ	Ceramic DIP	0 to +70°C	±0.39%
DAC-08HL	Leadless	0 to +70°C	±0.1%
DAC-08EL	Leadless	0 to +70°C	±0.19%
DAC-08CL	Leadless	0 to +70°C	±0.39%
DAC-08HN	Plastic	0 to +70°C	±0.1%
DAC-08EN	Plastic	0 to +70°C	±0.19%
DAC-08CN	Plastic	0 to +70°C	±0.39%
DAC-08AX	Dice	−55 to +125°C	±0.1%
DAC-08X	Dice	−55 to +125°C	±0.19%
DAC-08HX	Dice	0 to +70°C	±0.1%
DAC-08EX	Dice	0 to +70°C	±0.19%
DAC-08CX	Dice	0 to +70°C	±0.39%

*Also available with burn-in processing. To order add suffix B to part number.

Am1508/1408 • SSS1508A/1408A

8-Bit Multiplying D/A Converter

Distinctive Characteristics

- Improved direct replacement for MC1508/1408
- ±0.19% nonlinearity guaranteed over temperature range
- Improved settling time (SSS1508A/1408A) 250ns, typ.
- Improved power consumption (SSS1508A/1408A) 157mW, typ.
- Compatible with TTL, CMOS logic
- Standard supply voltage: +5.0V and −5.0V to −15V
- Output voltage swing: +0.5V to −5.0V
- High speed multiplying input: 4.0mA/μs

3

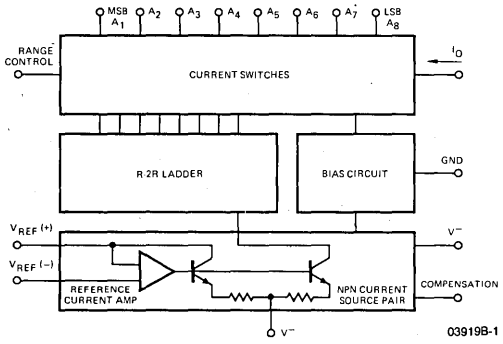
FUNCTIONAL DESCRIPTION

The SSS1508A/1408A, Am1508/1408 are 8-bit monolithic multiplying Digital-to-Analog Converters consisting of a reference current amplifier, an R-2R ladder, and eight high speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full scale output current of 1.992mA would result from a reference input current of 2.0mA.

The SSS1508A/1408A, Am1508/1408 is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building Tracking and Successive Approximation Analog-to-Digital Converters.

BLOCK DIAGRAM



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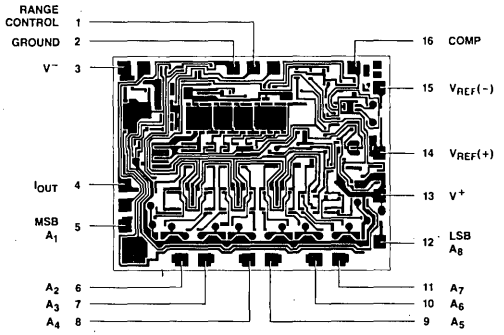
METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.068" X 0.088"

03919B-2

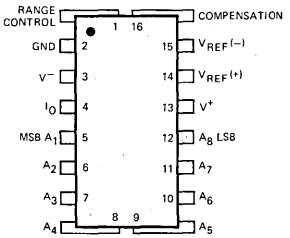
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
Am1408	Hermetic DIP	0 to +70°C	AM1408L8
	Hermetic DIP	0 to +70°C	AM1408L7
	Hermetic DIP	0 to +70°C	AM1408L6
	Hermetic DIP	0 to +70°C	SSS1408A-8Q
	Hermetic DIP	0 to +70°C	SSS1408A-7Q
	Hermetic DIP	0 to +70°C	SSS1408A-6Q
	Plastic DIP	0 to +70°C	AM1408N8
	Plastic DIP	0 to +70°C	AM1408N7
	Plastic DIP	0 to +70°C	AM1408N6
	Dice	0 to +70°C	LD1408
Am1508	Hermetic DIP	−55 to +125°C	AM1508L8
	Hermetic DIP	−55 to +125°C	SSS1508A-8Q
	Dice	−55 to +125°C	LD1508

*Also available with burn-in processing. To order, add suffix B to the part number.

CONNECTION DIAGRAM
Top View

D-16-1
P-16-1



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

(T_A = +25°C unless otherwise noted)

Power Supply Voltage	
V+	+5.5Vdc
V−	−16.5Vdc
Digital Input Voltage, V_5–V_{12}	+5.5, 0Vdc
Applied Output Voltage, V_O	+0.5, −5.2Vdc
Reference Current, I_{14}	5.0mA
Reference Amplifier Inputs, V_{14}, V_{15}	V_{CC}, V_{EE} Vdc

Power Dissipation (Package Limitation), P_D	
Ceramic Package	1000mW
Derate above T_A = +25°C	6.7mW/°C
Operating Temperature Range, T_A	
SSS1508A-8, Am1508	−55°C to +125°C
SSS1408A Series, Am1408 Series	0°C to +75°C
Storage Temperature, T_{stg}	−65°C to +150°C

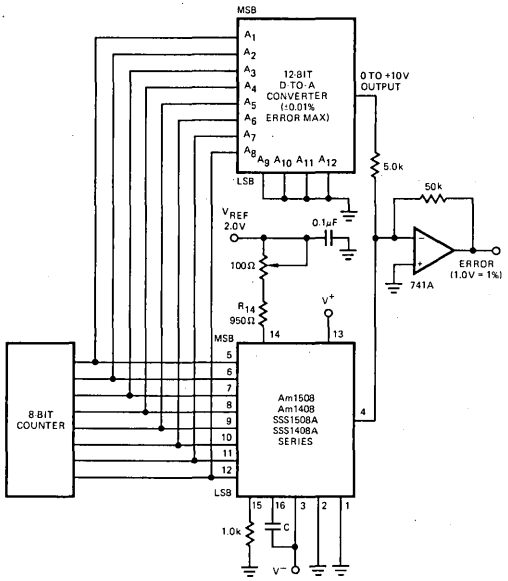
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

(V^+ = 5.0V, V^- = −15V, $\frac{V_{ref}}{R_{14}}$ = 2.0mA, SSS1508A-8/Am1508L8: T_A = −55 to +125°C, SSS1408A/Am1408 Series: T_A = 0 to +75°C unless otherwise noted: All digital inputs at high logic level.)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
E_R	**Relative Accuracy** SSS1508A-8, SSS1408A-8, Am1508L8, Am1408L8				±0.19	% IFS
	SSS1408A-7, Am1408L7				±0.39	
	SSS1408A-6, Am1408L6				±0.78	
t_S	**Settling Time to within 1/2 LSB (includes t_{PLH})** SSS1508A/1408A	T_A = +25°C		250		ns
	Am1508/1408			300		
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = +25°C		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		PPM/°C
V_{IH}	**Digital Input Logic Levels (MSB)** High Level, Logic "1"		2.0			Vdc
V_{IL}	Low Level, Logic "0"				0.8	
I_{IH}	Digital Input Current (MSB)	High Level, V_{IH} = 5.0V		0	0.04	mA
I_{IL}		Low Level, V_{IL} = 0.8V		−0.002	−0.8	
I_{15}	**Reference Input Bias Current (Pin 15)** SSS1508A/1408A			−1.0	−3.0	μA
	Am1508/1408			−1.0	−5.0	
ΔI_O	Output Current Range	V^- = −5.0V	0	2.0	2.1	mA
		V^- = −7.0V to −15V	0	2.0	4.2	
I_O	Output Current	V_{ref} = 2.000V, R_{14} = 1000Ω	1.9	1.99	2.1	mA
I_O (min.)	Output Current (All Bits Low)			0	4.0	μA
V_O	Output Voltage Compliance	V^- = −5V			−0.6, +0.5	Vdc
	($E_r \leq 0.19\%$ at T_A = +25°C)	V^- below −10V			−5.0, +0.5	
SRI_{ref}	Reference Current Slew Rate			4.0		mA/μs
$PSSI_O$	Output Current Power Supply Sensitivity			0.5	2.7	μA/V
I^+	**Power Supply Current** SSS1508A/1408A			2.5	14	mA
I^-				−6.4	−13	
I^+	Am1508/1408			2.5	22	
I^-				−6.4	−13	
ΔV^+	Power Supply Voltage Range	T_A = +25°C	4.5	5.0	5.5	Vdc
ΔV^-			−4.5	−15	−16.5	
P_d	**Power Dissipation** SSS1508A/1408A	All Bits Low V^- = −5.0Vdc		34	136	mW
		All Bits Low V^- = −15Vdc		108	265	
		All Bits High V^- = −5.0Vdc		34		
		All Bits High V^- = −15Vdc		108		
	Am1508/1408	All Bits Low V^- = −5.0Vdc		34	170	
		All Bits Low V^- = −15Vdc		108	305	
		All Bits High V^- = −5.0Vdc		34		
		All Bits High V^- = −15Vdc		108		

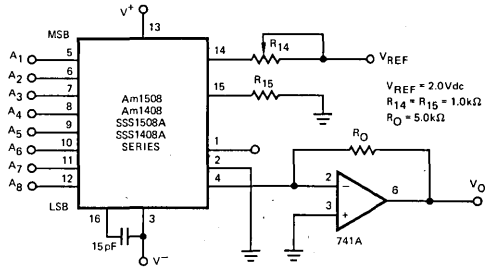
TYPICAL APPLICATIONS

RELATIVE ACCURACY TEST CIRCUIT



03919B-4

USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R_{14}}(R_O)\left[\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{126}+\frac{A_8}{256}\right]$$

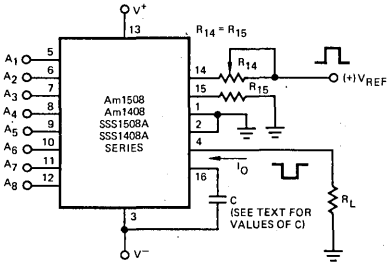
ADJUST V_{REF}, R_{14} OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{126}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

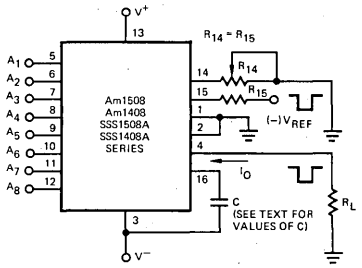
03919B-5

USE WITH POSITIVE V_{REF}



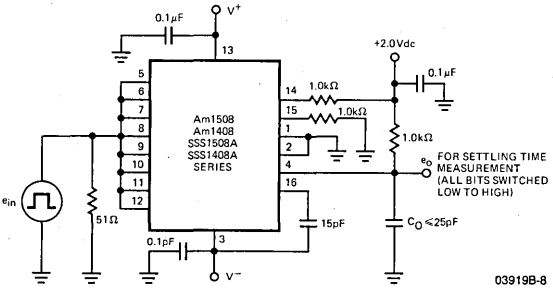
03919B-6

USE WITH NEGATIVE V_{REF}



03919B-7

TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



03919B-8

GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive voltage are shown on the previous page. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0 kilohms, minumum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V^- or ground, but using V^- increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V^- on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0 volts above the V^- supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to +0.5 volts when $V^- = -5.0V$ due to the current switching methods employed in the SSS1508A-8, Am1508.

The negative output voltage compliance of the SSS1508A-8, Am1508 is extended to −5.0V where the negative supply voltage is more negative than −10 volts. Using a full scale current of 1.992mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance but a 2.5-kilohm load increases "worst case" settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −12.0 volts, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the SSS1508A-8, Am1508 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the SSS1508A-8 has a very low full scale current drift with temperature.

The SSS1508A-8/Am1508 Series is guaranteed accurate to within ±1/2 LSB at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown on page 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the SSS1508A-8, Am1508 accuracy is essentially the same between 1.5 and 2.5mA. Then the SSS1508A-8, Am1508 circuits' full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the SSS1508A-8, Am1508.

MULTIPLYING ACCURACY

The SSS1508A-8, Am1508 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the SSS1508A-8, Am1508 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$pF.

The slowest single switch is the least significant bit. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Am2502/3/4 Family

Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- Can be used as serial-to-parallel converter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

3

FUNCTIONAL DESCRIPTION

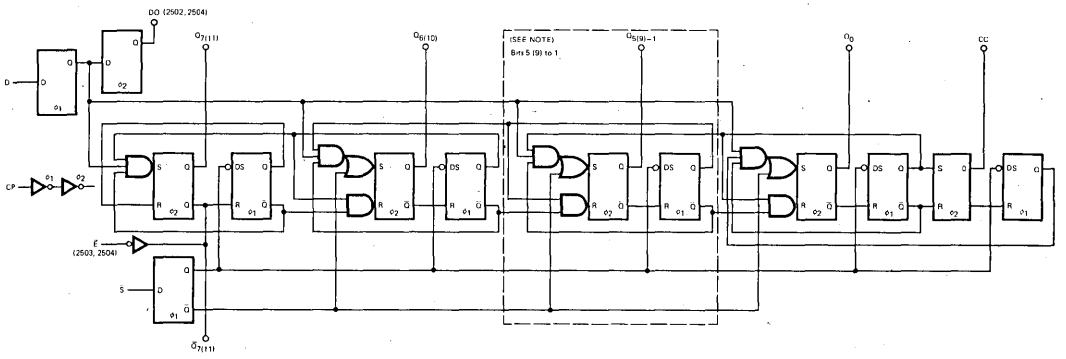
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

LOGIC DIAGRAMS



Notes: 1. Cell logic is repeated for register stages. Q_5 to Q_1 Am2502/3, Q_9 to Q_1 Am2504.
2. Numbers in parentheses are for Am2504.

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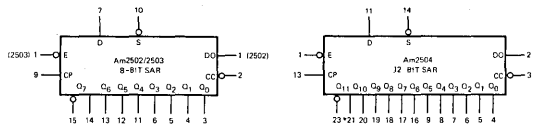
LOGIC SYMBOLS



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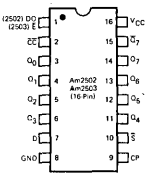
V_{CC} = Pin 16
GND = Pin 8

LIC-226

V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 15 22

CONNECTION DIAGRAMS – Top Views

D-16, P-16



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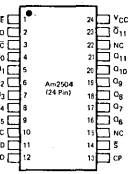
D-24, P-24



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Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS over operating temperature and voltage ranges

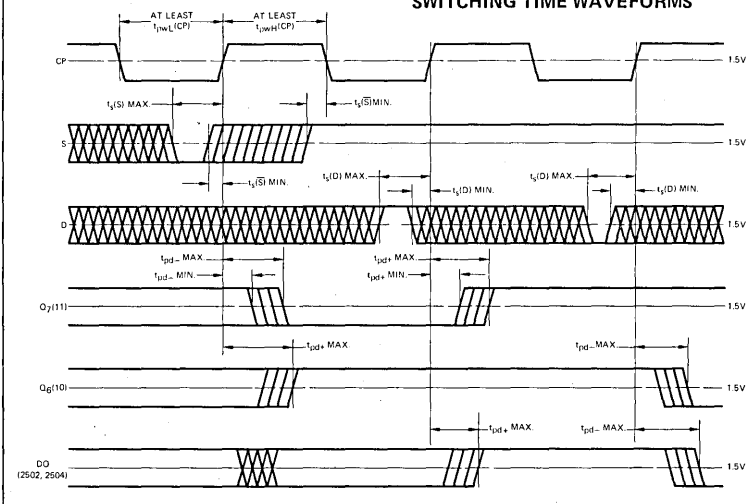
Parameters	Description	Test Conditions			Am2502/3/4 Min	Am2502/3/4 Typ (Note 1)	Am2502/3/4 Max	Am25L02/L03/L04 Min	Am25L02/L03/L04 Typ (Note 1)	Am25L02/L03/L04 Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		2.4	3.6		V
V_{OL}	Output LOW Voltage (Note 2)	V_{CC} = MIN, I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	0.15	0.3		V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8			0.7	V
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		CP, D, $\overline{S}$		−1.0	−1.6		−0.25	−0.4	mA
				$\overline{E}$		−1.5	−2.4		−0.4	−0.6	
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V		CP, D		6.0	40		2.0	20	μA
				E, $\overline{S}$		12.0	80		4.0	40	
	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−10	−25	−45	−4.0	−15	−35	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	Am25(L)02	XM		65	85		25	33	mA
				XC		65	95		25	35	
			Am25(L)03	XM		60	80		22	31	
				XC		60	90		22	33	
			Am25(L)04	XM		90	110		30	42	
				XC		90	124		30	45	

Notes: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. V_{OL}(MAX) = 0.4V with total device fanout of less than 50 TTL Unit Loads (80mA). Otherwise, V_{OL}(MAX) = 0.45V.

SWITCHING CHARACTERISTICS T_A = 25°C, V_{CC} = +5.0V, C_L = 15pF

Parameters	Description		Am2502/3/4 Min	Am2502/3/4 Typ	Am2502/3/4 Max	Am25L02/3/4 Min	Am25L02/3/4 Typ	Am25L02/3/4 Max	Units
t_{pd+}	Turn Off Delay CP to Output HIGH (except Q_{11}, $\overline{Q}_{11}$)		10	29	45	20	75	110	ns
	Turn Off Delay CP to Q_{11} or $\overline{Q}_{11}$ HIGH		10	35	50	30	100	140	
t_{pd-}	Turn On Delay CP to Output LOW		10	27	40	20	75	100	ns
t_s(D)	Setup Time Data Input		−10	4.0	10	−15	8.0	20	ns
t_s(S)	Setup Time Start Input		0	9.0	16	0	20	25	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	Am2503/Am2504) C_P = H, $\overline{S}$ = L		15	23		50	75	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			20	30		60	75	
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46		100	150	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20		70	100	ns
f_{max}	Maximum Clock Frequency		15	25		3.5	5.0		MHz

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

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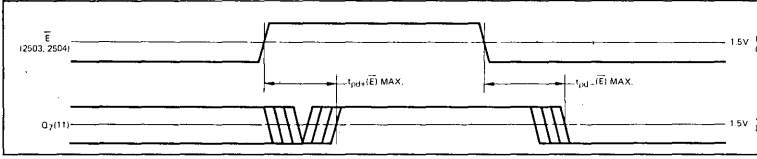

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DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2 L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the register.

$\overline{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$\overline{Q}_7(11)$ The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_L Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{E})$ The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\overline{E})$ The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

$t_s(D)$ Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

$t_s(\overline{S})$ Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

$t_{pw}(CP)$ The minimum clock pulse width (LOW or HIGH) required for proper register operation.

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

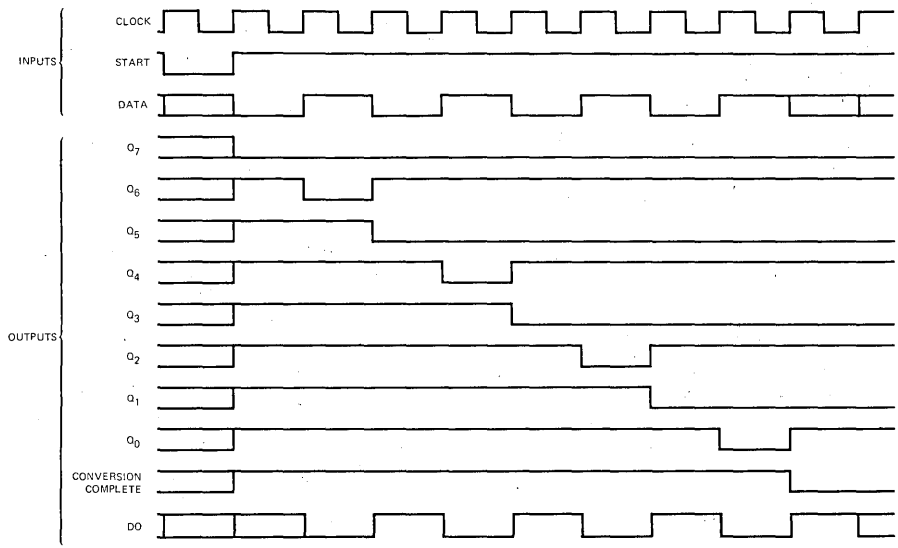
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion. Additional data input gating should be used to eliminate the possibility of false BCD codes.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (Q_{11}) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

Am25(L)02/3 TIMING CHART



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Am2502/3 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ (2503)	1	1.5	2	–	–
DO (2502)	1	–	–	12	6
$\overline{CC}$	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	1	1	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
$\overline{S}$	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
Q_7	14	–	–	12	6
$\overline{Q}_7$	15	–	–	12	6
V_{CC}	16	–	–	–	–

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am2504 LOADING RULES (IN UNIT LOADS)

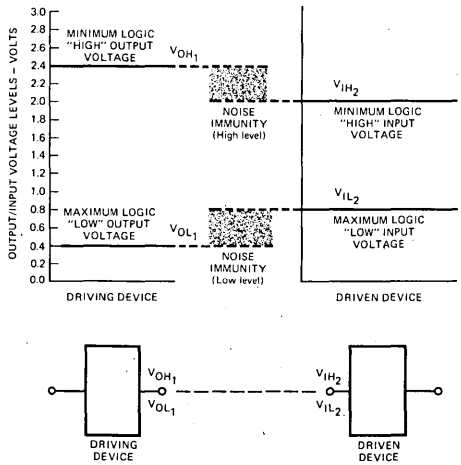
Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$	1	1.5	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–		12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	1	1	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
Q_{11}	21	–	–	12	6
NC	22	–	–	–	–
$\overline{Q}_{11}$	23	–	–	12	6
V_{CC}	24	–	–	–	–

A Standard TTL Unit Load is defined as 40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

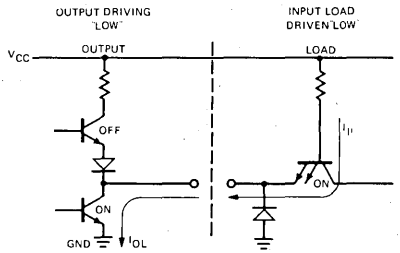
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

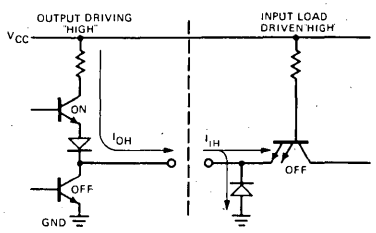
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW

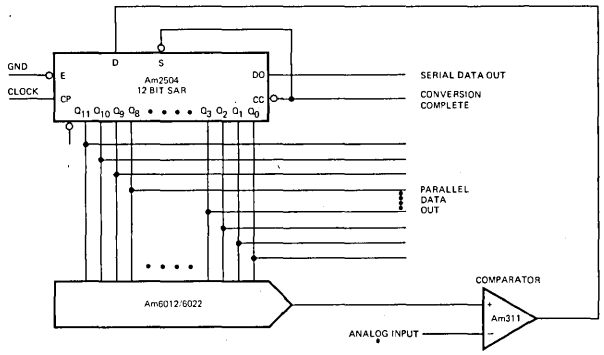


Current Interface Conditions – HIGH



LIC-232

Am2502/3/4 APPLICATION
Continuous Conversion Analog-to-Digital Converter

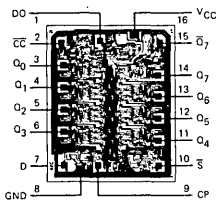


This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second.

LIC-233

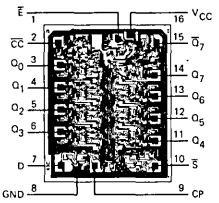
Metallization and Pad Layouts

Am2502



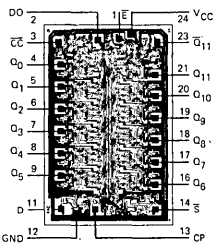
DIE SIZE 0.087" X 0.105"

Am2503



DIE SIZE 0.087" X 0.105"

Am2504



DIE SIZE 0.087" X 0.135"

ORDERING INFORMATION*

Order Number	Order Number	Package Type	Temperature Range	Bits
Am2502DM	Am25L02DM	Hermetic DIP	−55 to +125°C	8
Am2503DM	Am25L03DM	Hermetic DIP	−55 to +125°C	8
Am2504DM	Am25L04DM	Hermetic DIP	−55 to +125°C	12
Am2502FM	Am25L02FM	Flat Package	−55 to +125°C	8
Am2503FM	Am25L03FM	Flat Package	−55 to +125°C	8
Am2504FM	AM25L04FM	Flat Package	−55 to +125°C	12
Am2502XM	Am25L02XM	Dice	−55 to +125°C	8
Am2503XM	Am25L03XM	Dice	−55 to +125°C	8
Am2504XM	Am25L04XM	Dice	−55 to +125°C	8
Am2502DC	Am25L02DC	Hermetic DIP	0 to +70°C	8
Am2503DC	Am25L03DC	Hermetic DIP	0 to +70°C	8
Am2504DC	Am25L04DC	Hermetic DIP	0 to +70°C	12
Am2502PC	Am25L02PC	Plastic	0 to +70°C	8
Am2503PC	Am25L03PC	Plastic	0 to +70°C	8
Am2504PC	Am25L04PC	Plastic	0 to +70°C	12
Am2502XC	Am25L02XC	Dice	0 to +70°C	8
Am2503XC	Am25L03XC	Dice	0 to +70°C	8
Am2504XC	Am25L04XC	Dice	0 to +70°C	12

*Also available with burn-in processing. To order add suffix B to part number.

Am6012/6012A • Am6022/6022A

12-Bit High and Ultra-High Speed Multiplying D/A Converters

DISTINCTIVE CHARACTERISTICS

- All grades 12-bit monotonic over temperature
- Differential nonlinearity to ±0.012% (13 bits) max over temperature (A grades)
- Fast settling output current:
  75ns (Am6022/A)
  250ns (Am6012/A)
- Full scale current: 4mA
- High output impedance and compliance: −5 to +10V
- Differential current outputs
- Low cost
- High-speed multiplying capability
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Low power consumption:
  230mW (Am6012/A)
  500mW (Am6022/A)

GENERAL DESCRIPTION

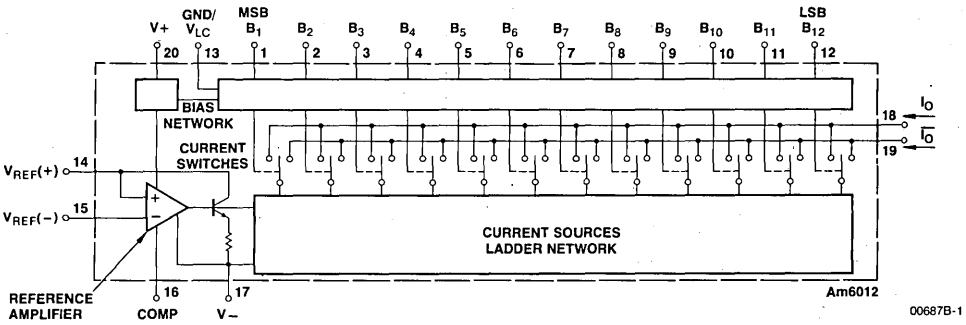
The Am6012/6022 series of 12-bit monolithic multiplying digital-to-analog converters represent new levels of speed, accuracy and low cost. The Am6012 and its high-performance, pin-compatible twin, the Am6022 are the first 12-bit DACs to be built using standard processing without the need for thin-film resistors or active trimming.

The Am6012/6022 design guarantees a more uniform step size than is possible with standard binarily weighted DACs. This ±1/2 LSB differential nonlinearity is desirable in many applications where local linearity is critical. The uniform step size allows finer resolution of levels and in most applications is more useful than conformance to an ideal straight line from zero to full scale.

The Am6012/6022 have high voltage compliance, high impedance dual complementary outputs which increase their versatility and enable differential operation to effectively double the peak to peak output swing. These outputs can be used directly without op amps in many applications. The dual complementary outputs can also be connected in A/D converter applications to present a constant load current and significantly reduce switching transients and increase system throughput. Output full scale current is specified at 4mA, allowing use of smaller load resistors to minimize the output RC delay which usually dominates settling time at the 12-bit level.

The Am6012/6022 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as tight as 0.012% (13 bits), for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range. Device performance is essentially independent of power supply voltage, and devices work over a wide operating range from +5 and, −12V to ±18V.

FUNCTIONAL DIAGRAM



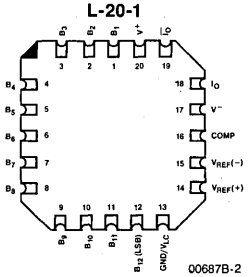
ORDERING INFORMATION

Package Type	Temperature Range	Differential Nonlinearity	Am6012 Order Number	Am6022 Order Number
Ceramic DIP	−55 to +125°C	±0.012%	AM6012ADM	AM6022ADM
Ceramic DIP	−55 to +125°C	±0.025%	AM6012DM	AM6022DM
Ceramic DIP	0 to +70°C	±0.012%	AM6012ADC	Am6022ADC
Ceramic DIP	0 to +70°C	±0.025%	AM6012DC	AM6022DC
Plastic DIP	0 to +70°C	±0.012%	AM6012APC	AM6022APC
Plastic DIP	0 to +70°C	±0.025%	AM6012PC	AM6022PC
Leadless Chip-Carrier	−55 to +125°C	±0.012%	AM6012ALM	AM6022ALM**
Leadless Chip-Carrier	−55 to +125°C	±0.025%	Am6012LM	Am6022LM**
Leadless Chip-Carrier	0 to +70°C	±0.012%	Am6012ALC	Am6022ALC**
Leadless Chip-Carrier	0 to +70°C	±0.025%	Am6012LC	Am6022LC**
Dice	−55 to +125°C	±0.012%	Am6012AXM	Am6022AXM**
Dice	−55 to +125°C	±0.025%	Am6012XM	Am6022XM**
Dice	0 to +70°C	±0.012%	Am6012AXC	Am6022AXC
Dice	0 to +70°C	±0.025%	Am6012XC	Am6022XC

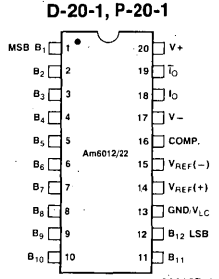
*Also available with burn-in processing. To order, add suffix B to part number.
**To be announced.

CONNECTION DIAGRAMS – Top Views

L-20-1



D-20-1, P-20-1



Note: Pin 1 is marked for orientation.

Am6012/6012A

MAXIMUM RATINGS (above which useful life may be impaired)

Operating Temperature		Power Supply Voltage	±18V
Am6012ADM, Am6012DM	−55 to +125°C	Logic Inputs	−5 to +18V
Am6012ADC, Am6012DC	0 to +70°C	Analog Current Outputs	−8 to +12V
Storage Temperature	−65 to +125°C	Reference Inputs V_{14}, V_{15}	V− to V+
Lead Temperature (Soldering, 60sec)	300°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
		Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for $V^+ = +15V$, $V^- = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified.

Parameter	Description	Test Conditions	Am6012A Min.	Am6012A Typ.	Am6012A Max.	Am6012 Min.	Am6012 Typ.	Am6012 Max.	Units
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	–	±.05	–	–	±0.05	%FS
I_{FS}	Full Scale Current	V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ T_A = 25°C	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range R_{OUT} > 10 megohms typ.	−5	–	+10	−5	–	+10	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$	–	±0.2	±1.0	–	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		–	–	0.10	–	–	0.10	μA
t_S	Settling Time	To ±1/2 LSB, all bits ON or OFF, T_A = 25°C	–	250	500	–	250	500	nsec
t_{PLH} t_{PHL}	Propagation Delay – all bits	50% to 50%	–	25	50	–	25	50	nsec
C_{OUT}	Output Capacitance		–	20	–	–	20	–	pF
V_{IL}	Logic Input Levels, Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"		2.0	–	–	2.0	–	–	Volts
I_{IN}	Logic Input Current	V_{IN} = −5 to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(eq)}$ = 800Ω CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +13.5V to +16.5V, V− = −15V	–	±.00005	±.001	–	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		V− = −13.5V to −16.5V, V+ = +15V	–	±.00025	±.001	–	±.00025	±.001	
V+	Power Supply Range	V_{OUT} = 0V	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−10.8	−18	–	−10.8	
I+	Power Supply Current	V+ = +5V, V− = −15V	–	5.7	8.5	–	5.7	8.5	mA
I−			–	−13.7	−18.0	–	−13.7	−18.0	
I+		V+ = +15V, V− = −15V		5.7	8.5	–	5.7	8.5	
I−			–	−13.7	−18.0	–	−13.7	−18.0	
P_D	Power Dissipation	V+ = +5V, V− = −15V	–	234	312	–	234	312	mW
		V+ = +15V, V− = −15V	–	291	397	–	291	397	

Am6022/6022A

MAXIMUM RATINGS (above which useful life may be impaired)

Operating Temperature		Power Supply Voltage	±18V
Am6022ADM, Am6022DM	−55 to +125°C	Logic Inputs	−5 to V+
Am6022ADC, Am6022DC	0 to +70°C	Analog Current Outputs	−8 to +12V
Storage Temperature	−65 to +125°C	Reference Inputs V_{14}, V_{15}	V− to V+
Lead Temperature (Soldering, 60sec)	300°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
		Reference Input Current (I_{14})	1.25mA

3

ELECTRICAL CHARACTERISTICS

These specifications apply for $V^+ = +15V$, $V^- = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified.

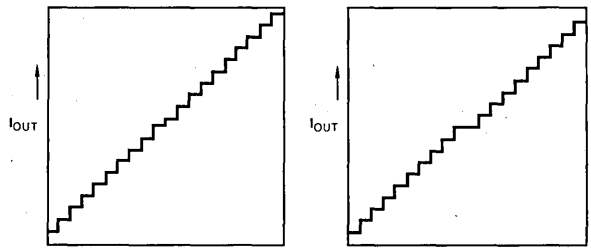
Parameter	Description	Test Conditions	Am6022A Min.	Am6022A Typ.	Am6022A Max.	Am6022 Min.	Am6022 Typ.	Am6022 Max.	Units
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	±0.012	–	–	±0.025	–	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		–	±5	–	–	±10	–	ppm/°C
			–	±.0005	–	–	±.003	–	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range R_{OUT} > 10 megohms typ.	−5	–	+10	−5	–	+10	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$	–	±0.2	–	–	±0.4	–	μA
I_{ZS}	Zero Scale Current			0.10	–	–	0.10	–	μA
t_S	Settling Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	–	75	–	–	75	–	nsec
t_{PLH} t_{PHL}	Propagation Delay – all bits	50% to 50%	–	10	–	–	10	–	nsec
C_{OUT}	Output Capacitance		–	10	–	–	10	–	pF
V_{IL}	Logic Input Levels, Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"		2.0	–	–	2.0	–	–	Volts
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+15$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+15	−5	–	+15	Volts
I_{REF}	Reference Current Range	$V_{REF(-)} = 0V$	0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = 0pF	–	16.0	–		16.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +13.5V to +16.5V, V− = −15V	–	±.00005		–	±0.0005		%FS/%
$PSSI_{FS-}$		V− = −13.5V to −16.5V, V+ = +15V	–	±.00025		–	±.00025		
V+	Power Supply Range	$V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−10.8	−18	–	−10.8	
I+	Power Supply Current	V+ = +5V, V− = −15V	–	11		–	11	–	mA
I−			–	−24	–	–	−24	–	
I+		V+ = +15V, V− = −15V		13.0	–	–	13.0	–	
I−			–	−24	–	–	−24	–	
P_D	Power Dissipation	V+ = +5V, V− = −15V	–	415	–	–	415	–	mW
		V+ = +15V, V− = −15V	–	555	–	–	555	–	

ACCURACY SPECIFICATIONS

The design of the 6012/22 emphasizes differential linearity which is a measure of the uniformity of each step in the transfer characteristic. The circuit design, described in greater detail on page 6, requires resistor matching and tracking tolerances of 8 times lower than that of previous designs to achieve and maintain monotonicity over temperature. This advantage has been used in the 6012A/22A to provide 13-bit differential nonlinearity over temperature, a level of performance not generally available in previous designs, even when using thin film resistors.

The figures illustrate that ±1/2 LSB (13-bit) differential nonlinearity guarantees a converter with 4096 distinct output levels. ±1 LSB D.N.L. guarantees monotonicity, so that when the input code is increased the output will not decrease. Note that nonlinearity, or deviation from an ideal straight line through zero and full scale, cannot be visually determined from the figures. In most applications, 12-bit resolution and differential linearity are more important than linearity. This is especially true in video and graphics, where the human eye has difficulty discerning nonlinearity of less than 5%.

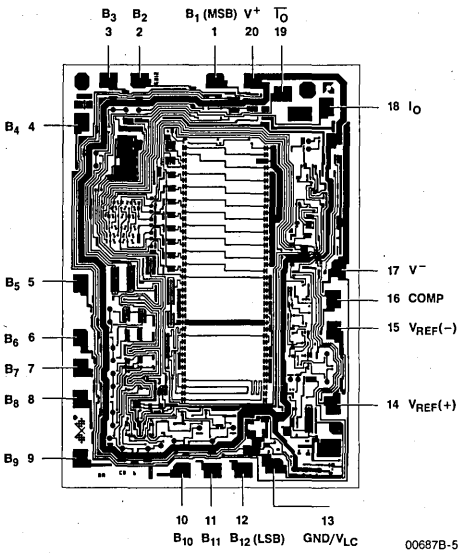
DIFFERENTIAL NONLINEARITY WORST CASE AT TEMPERATURE EXTREME



00687B-4

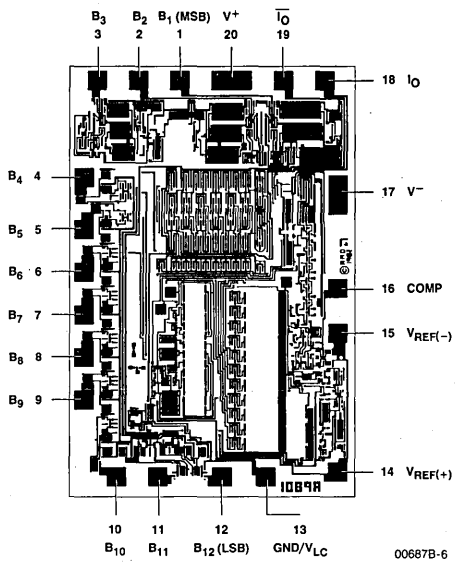
METALLIZATION AND PAD LAYOUT

Am6012



00687B-5

Am6022



00687B-6

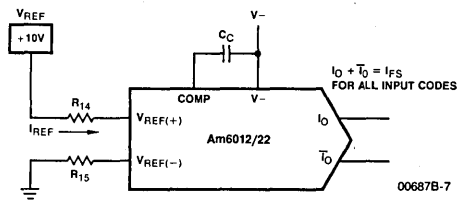
DIE SIZE 0.093" X 0.134"

APPLICATION HINTS:

1. Reference current and reference resistor.

There is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$



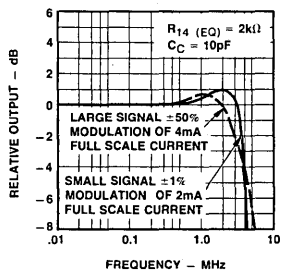
2. Reference amplifier compensation. (Am6012)

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

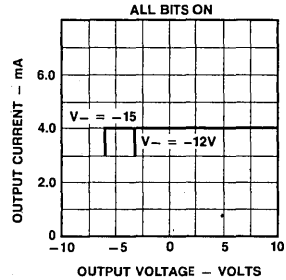
MINIMUM SIZE COMPENSATION CAPACITOR (I_{FS} = 4mA, I_{REF} = 1.0mA)

R_{14} (EQ) (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response

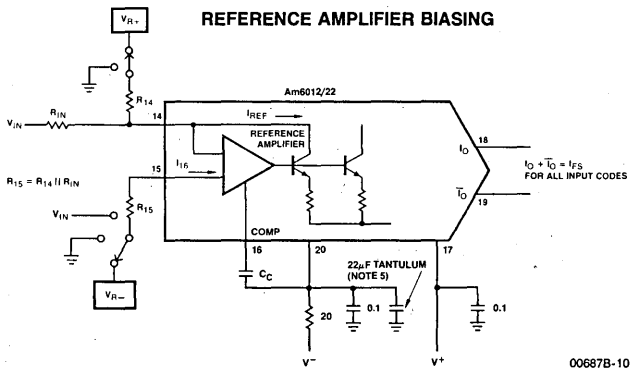


Output Voltage Compliance



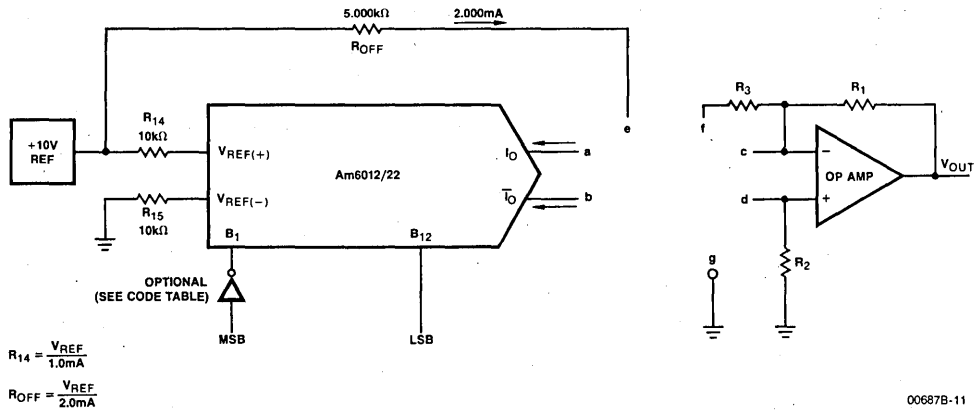
Note: A 0.01μF capacitor is recommended for fixed reference operation.

REFERENCE AMPLIFIER BIASING



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1) Am6012	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1) Am6012	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $C = 5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V– with 20Ω and bypass with 22μF tantulum capacitor.



CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
UNIPOLAR	Straight binary; one polarity with true input code, true zero output.	a-c b-g R1 = R2 = 2.5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a-g b-c R1 = R2 = 2.5K	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
			Positive full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
			Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
SYM-METRICAL OFFSET	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
	's complement; o. et half scale, symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
OFFSET WITH TRUE ZERO	Offset binary; offset half scale, true zero output.	e-a-c b-g R1 = R2 = 5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			− LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000
	2's complement; offset half scale true zero output MSB complemented (need inverter at B1).	e-a-c b-g R1 = R2 = 5K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

SEGMENTED DAC DESIGN INFORMATION

The design of a 12-bit D/A converter has traditionally required precision thin film resistors, a trimming method, and a binarily weighted ladder network. The 6012/22 is a 12-bit DAC which uses diffused resistors and requires no trimming, cutting, blowing, or zapping to guarantee monotonicity for all grades over the temperature range. A proprietary design technique, departing from the traditional R-2R approach used in virtually all high speed high resolution converters, provides inherent monotonicity and differential linearity as high as 13 bits. This guarantees a more uniform step size over the temperature range than available trimmed 12-bit converters. The converter's performance is immune to variations in temperature, time, process, and mechanical stress. The circuit also features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In most converter applications, uniform step size is more important than conformance to an ideal straight line. Most 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±1/2 LSB (±.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. This new circuit uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current switched R-2R DAC since it is slower, has a voltage output, and if implemented at the 12-bit level would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

The technique used in the Am6012 combines the advantages of both the R-2R and 2^nR approaches. It is inherently monotonic, fast, and uses untrimmed resistors which are actually fewer in number than the classic R-2R ladder.

In order to properly describe the new design technique, the standard R-2R ladder approach used in previous 12-bit DAC's will first be discussed. Figure 1 shows the twelve-bit currents which are used in all possible binary combinations to generate 4096 analog output levels. The resistor ladder tolerance is most critical for the major carry, where the 11 least significant bits turn off and the most significant bit turns on. If the MSB is more than 1μA low, or −.05%, the converter will be nonmonotonic. Table 1 shows the maximum tracking error which can be allowed over a 100°C range to maintain monotonicity, which is ±1 LSB D.N.L. Achieving ±1/2 LSB differential nonlinearity is especially difficult since it requires a tracking temperature coefficient of ±1.25 ppm/°C.

Figure 2 shows the transfer characteristic for the new technique, called the segmented DAC. The 4096 output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources, as shown in Figure 3. The resistors which determine monotonocity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_0 is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

At each segment endpoint, monotonicity is assured because no critical resistor tolerances are involved. For example, at the midpoint of the transfer characteristic, as shown in Figure 2, $I_{4,0}$ is actually generated by the same segment resistor as $I_{3,511}$ and has been incremented by the remainder current of the 9-bit DAC.

In the segmented DAC, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high speed fully differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long term characteristics are not degraded.

TABLE 1
RESISTOR SPECIFICATIONS

Ladder Type	No. of Resistors	Initial Matching Required for ±1 LSB DNL (%)	Tracking Required for ±1 LSB DNL (ppm/°C)		Tracking Req'd. for ±1/2 LSB DNL (ppm/°C)
			0 Initial DNL	1/2 LSB Initial DNL	1/4 LSB Initial DNL
Straight R-2R	37	±.05	5	2.5	1.25
Segmented 3 Bits + 9 Bits	24	±.4	40	20	10

Figure 1. Traditional R-2R D/A Converter.

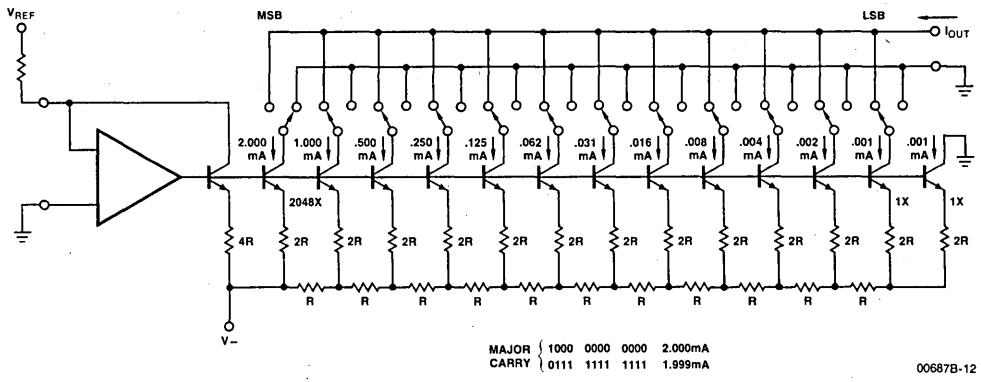


Figure 2. Transfer Characteristic of Segmented Design.

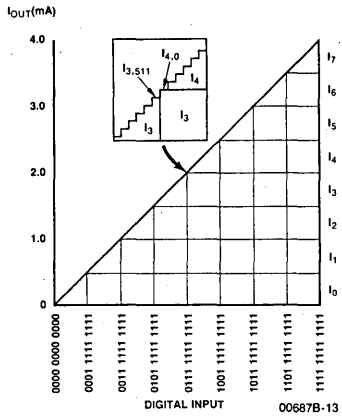


Figure 3. Segmented DAC Functional Diagram Used in Am6012/22.

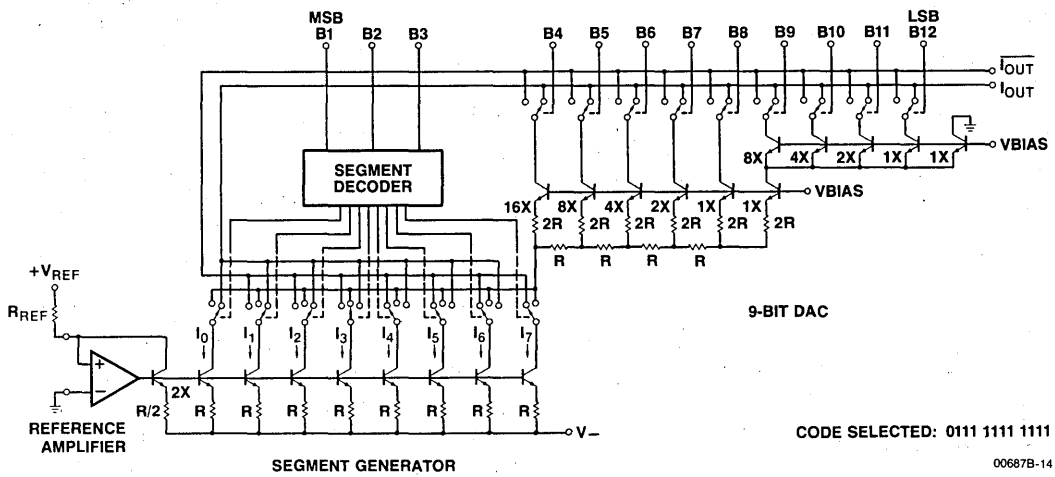
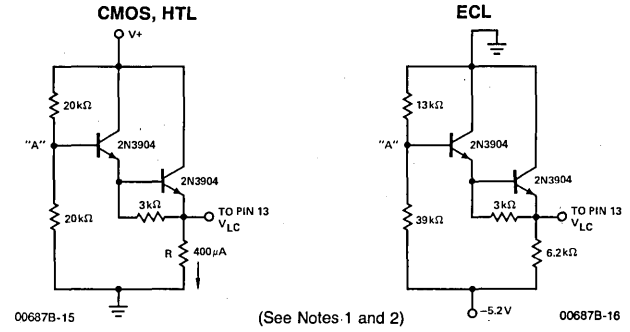


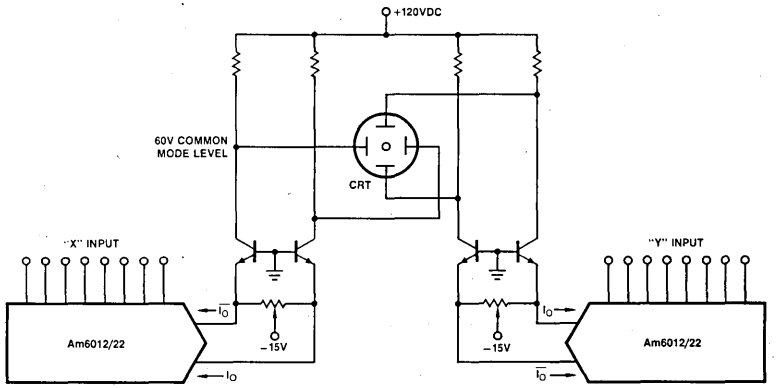
Figure 4. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs.



Notes:
1. Set the voltage "A" to the desired logic input switching theshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the DAC on ±15V supplies.

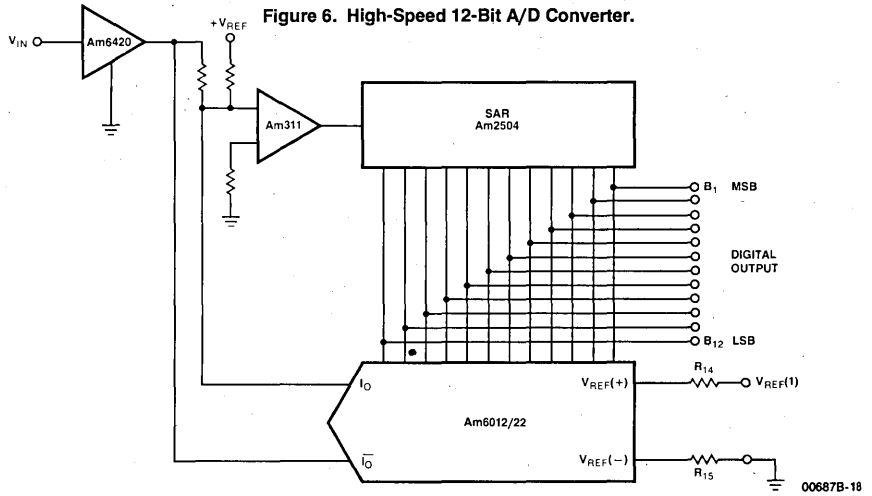
3

Figure 5. CRT Display Driver.



Notes: 1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Figure 6. High-Speed 12-Bit A/D Converter.



Am6012
12-Bit High-Speed DAC

By Brian Gillings
Advanced Micro Devices

00165A-ANA

INTRODUCTION

Advanced Micro Devices' Am6012 is the first 12-bit DAC ever built using standard processing without the requirements of thin film resistors and/or active trimming of individual devices. The result is a high-speed and high-accuracy converter with low cost. Offering a ±½ least significant bit (LSB) differential nonlinearity, the Am6012's uniform step size allows finer resolution of levels, and in most applications is more useful than conformance to an ideal straight line from zero to full scale.

DESCRIPTION OF THE Am6012

Figure 1 shows a simplified schematic for a traditional R-2R D/A converter used in previous 12-bit DACs. Twelve current sources are used in all possible binary combinations to generate the 4096 analog output levels. The resistor ladder tolerance is most critical at the major carry where the 11 least significant bits are turned off and the most significant bit (MSB) turns on. If the MSB is more than −0.05% low, the converter will be nonmonotonic. Achieving the initial resistor matching for ±1LSB differential nonlinearity (±0.05%) has required precision resistors plus some sort of trimming method, such as laser trimming, cutting, blowing or zapping to guarantee monotonicity for all grades over the temperature range. The Am6012 uses a proprietary design technique, departing from the traditional R-2R design, which offers inherent monotonicity and differential nonlinearity as high as 13 bits (0.012%). The performance of the converter is immune to variations in temperature, time, process and mechanical stress.

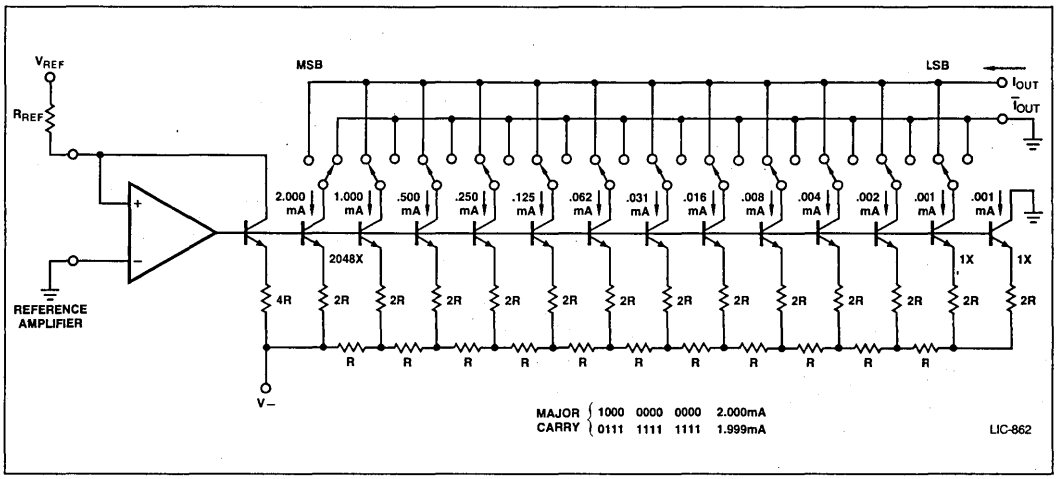


Figure 1. Traditional R-2R D/A Converter

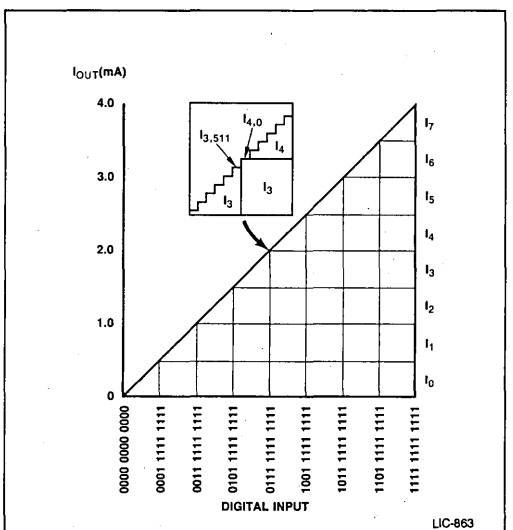


Figure 2. Transfer Characteristic of Segmented Design

Figure 2 shows the transfer characteristic for the new technique called a segmented ladder used in the Am6012. The 4096 output levels are composed of eight groups of 512 steps each.

Each step of the group is generated by a 9-bit DAC and each of the segment slopes is determined by one of eight equal current sources as shown in Figure 3. The resistors that determine monotonicity are in the 9-bit DAC, and the major carry of the 9-bit DAC is repeated in each of the eight segments. This results in the need for eight times lower initial resistor accuracy and provides tracking to maintain a given differential nonlinearity over temperature.

If we assume that the input code is all ZEROES, the first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output I_{OUT}. An increasing digital input code selects a new segment for every 512 counts. The previous segment is fed to output I_{OUT} where the new group is added to it, thus ensuring monotonicity independent of segment resistor values.

In the segment DAC, the precision of the eight main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in a R-2R DAC. Thus, if the resistor tolerances were the same, then the segmented approach would actually be higher in linearity than that of the R-2R design.

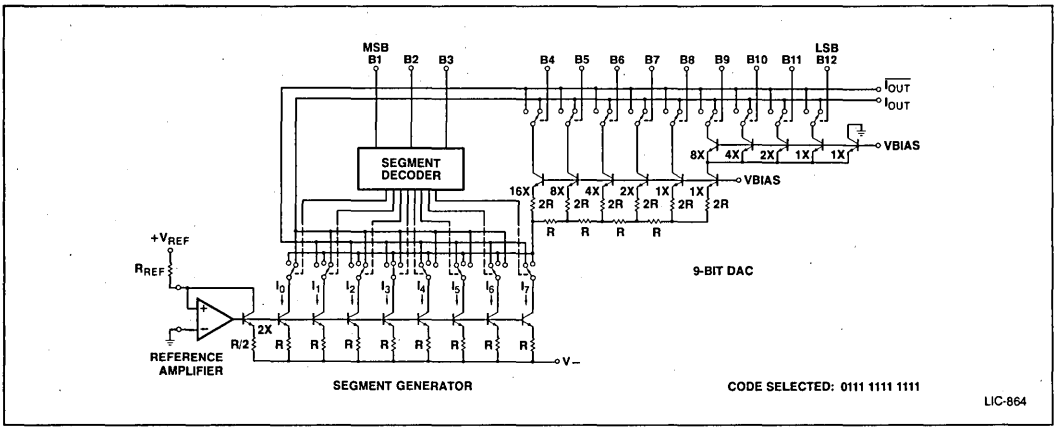


Figure 3. Segmented DAC Functional Diagram Used in Am6012

The 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by using scaled emitters to split the current actively. All of the current switches in the step generator are fully differential switches capable of switching low currents at high speed. This allows the use of a binarily scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Like other monolithic DACs, the Am6012 has two types of errors that cannot be eliminated by adjustment. They are integral nonlinearity and differential nonlinearity. The integral nonlinearity shown in Figure 4 is the maximum deviation of the transfer function from the straight line drawn from actual zero through the full-scale output of the converter. Integral nonlinearity is expressed in LSBs or as a percentage of full-scale. Some products use the "best fit" straight line and specify the deviation in LSBs, however, this straight line will usually not terminate at the full-scale value. The user then must adjust his converter to this full-scale value, but is then unable to calibrate the converter to benefit from the better value offered by this specmanship. Most users are interested in the absolute value of the full-scale output and can calibrate it either manually or automatically.

Differential nonlinearity (DNL) is a measure of the deviation of each individual step size from the ideal least significant bit. A DNL of more than 1LSB defines nonmonotonicity, and a perfect converter has a zero DNL.

The Am6012A is specified as having 13 bits of DNL over temperature, a level of performance generally not available in other 12-bit converters even when using thin film resistors. This ±½LSB (13-bit) DNL guarantees the converter has 4096 separate and distinct output levels, whereas a ±1LSB DNL only guarantees monotonicity. It must be stressed again that these DNL figures are guaranteed over the complete temperature range. Also, DNL gives a measure of curve smoothness. The DAC transfer function may be more than 1LSB nonlinear and yet be smooth and useful with ½LSB DNL. This is especially true in video and graphics where the human eye has difficulty discerning nonlinearity of less than 5%. In most applications, 12-bit resolution and DNL are more important than integral nonlinearity. Figure 5 shows the nonlinearity of an actual device.

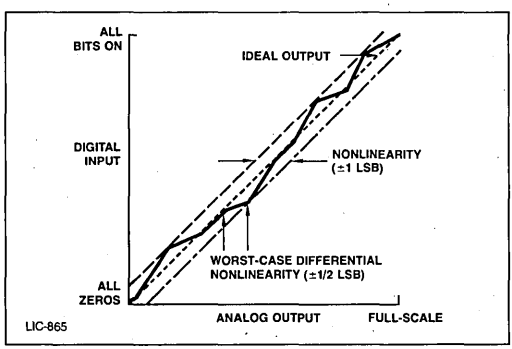


Figure 4. Monotonic DAC with ±1 LSB Nonlinearity and ±1/2 LSB Differential Nonlinearity

MULTIPLYING DAC

The Am6012 uses a fixed reference for most applications, but it can also handle an AC reference source. The output current I_{OUT} is a product of the digital input and analog reference voltage (V_{REF}) or current (I_{REF}).

The output current for current reference can be expressed as:

$$I_O = 4 \cdot I_{REF}\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \frac{B_4}{16} + \frac{B_5}{32} + \frac{B_6}{64} + \frac{B_7}{128} + \frac{B_8}{256} + \frac{B_9}{512} + \frac{B_{10}}{1024} + \frac{B_{11}}{2048} + \frac{B_{12}}{4096}\right)$$

where B_1 is MSB.

The Am6012 has complementary/differential current outputs. The complement of I_O is expressed as:

$$\overline{I_O} = I_{FS} - I_O$$

where the addition of I_O and $\overline{I_O}$ is a constant regardless of the digital code.

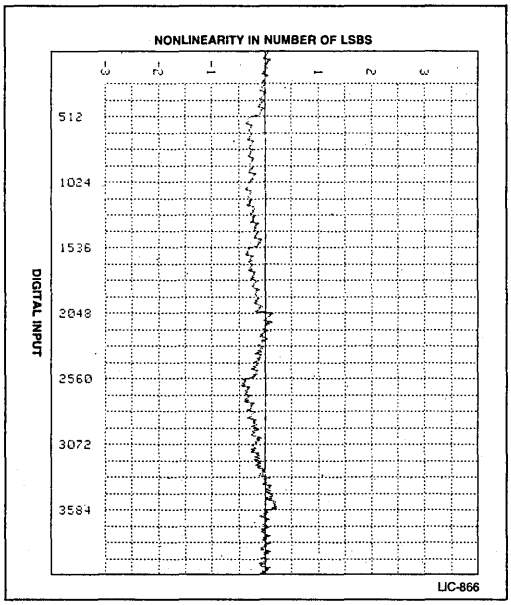


Figure 5. Nonlinearity Plot of Actual Device

Figures 6 and 7 show the relationship of I_{REF} to I_O and $\overline{I_O}$ for the basic DC connections. The reference may be positive or negative, and a bipolar output voltage may be obtained using the high-compliance current outputs alone or with an output op-amp, as described later.

An application of the external positive reference voltage ($+V_{REF}$) forces current through a reference resistor (R_{REF}) into the reference input ($V_{REF(+)}$), which is a virtual ground created by the reference amplifier feedback loop. Reference current (I_{REF}) is defined as:

$$I_{REF} = \frac{+V_{REF}}{R_{REF}}$$

A +10V supply for $+V_{REF}$ is recommended for optimum full-scale temperature operation. Resistor R_{15} minimizes the temperature coefficient of output offset voltage of the reference amplifier by matching it to R_{14}.

In negative reference applications, the external negative reference voltage is applied to the negative reference input ($V_{REF(-)}$) of the Am6012. The voltage at ($V_{REF(+)}$) pin tracks the voltage at ($V_{REF(-)}$). I_{REF} flows from ground through R_{REF} into the ($V_{REF(+)}$) input.

This connection produces high impedance at the ($V_{REF(-)}$) input, thus isolating the signal source from the load. Again, R_{15} is normally used to cancel input bias current errors and is nominally equal to R_{REF}.

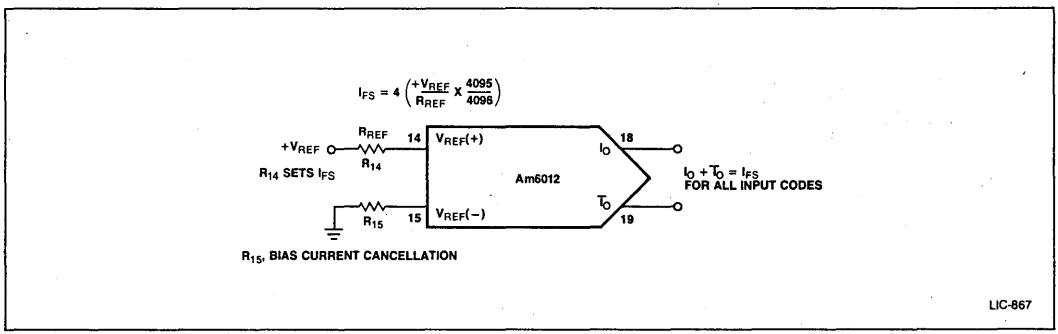


Figure 6. Positive Reference Connection

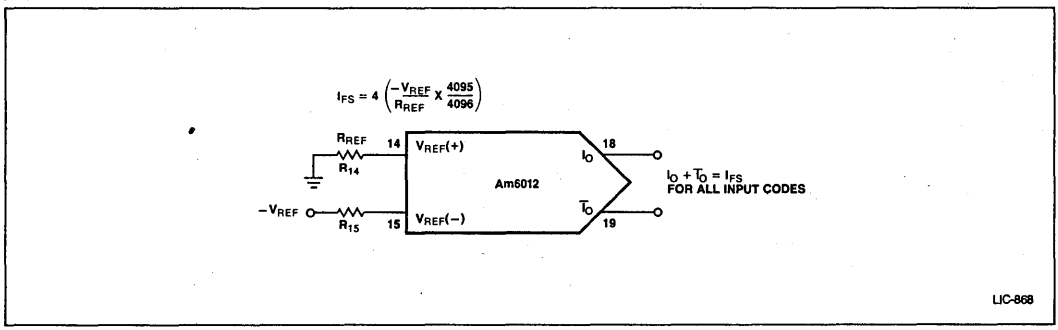


Figure 7. Negative Reference Connection

BIPOLAR OPERATION

Figure 8 shows a low input impedance bipolar connection. The current into ($V_{REF(+)}$) is I_{REF} plus I_{IN}. I_{REF} must be equal to or greater than the maximum negative value of I_{IN}, so the reference amplifier will not turn off. For a high-impedance connection (Figure 9) I_{REF} is calculated from:

$$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$$

where $+V_{REF}$ must be equal to or greater than the maximum positive value of V_{IN}. The I_{REF} current range is set at a minimum of 0.2mA and a maximum of 1.1mA. Fifty percent modulation is recommended to maintain speed and linearity (0.55mA ±0.5mA) over commercial temperature range.

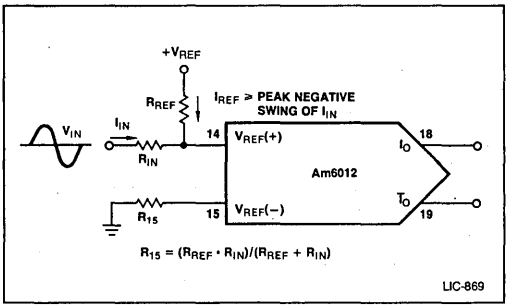


Figure 8. Low Input Impedance Bipolar Reference

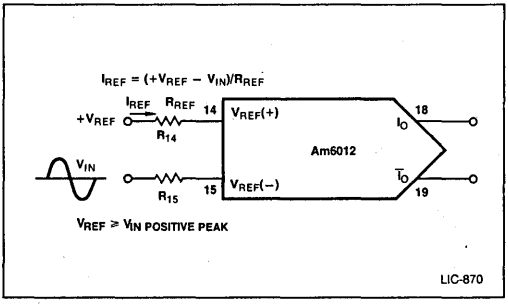


Figure 9. High-Input Impedance Bipolar Reference

REFERENCE AMPLIFIER COMPENSATION

For AC reference applications, a minimum-value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance seen at ($V_{REF(+)}$). Table 1 gives the compensation capacitors required for different values of R_{REF}; and Figure 10 shows the frequency response of the reference amplifier with R_{REF} = 2K and C_C = 10pF.

For the fastest response to a pulse, low values of R_{REF} should be used resulting in a low C_C value. When R_{REF} is 800 ohms, C_C is not required and a full-scale transition of 1μsec maximum and 500nsec typical is obtained. For fixed reference operation a 0.01μF capacitor should be used.

AC COUPLED MULTIPLICATION

Sometimes multiplying applications are more easily achieved by AC coupling, and a high impedance input is often required to avoid loading the high source impedance. Figure 11 uses the C_C pin as the input. This is possible because the C_C connection is $2V_{BE}$ away from the ladder determining resistors internal to the Am6012 and gives wider bandwidth than using the reference amplifier.

TABLE 1. MINIMUM SIZE COMPENSATION CAPACITOR

(I_{FS} = 4mA, I_{REF} = 1.0mA)

$R_{14\ (EQ)}$ (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

VOLTAGE OUTPUTS USING Am6012

The settling time for the Am6012 is specified for the current mode or the fastest operating mode. Many DAC applications require a current-to-voltage conversion. This can be achieved simply by connecting a low-value resistor directly to the output. If the output current is 4mA, a unipolar output would limit the resistor value to 1.25K ohms to ground because of the −5V DAC output voltage compliance limitation. The output settling time is determined by the RC time constant produced by the DAC output capacitance of 20pF (plus stray capacitance) and the value of the load resistor. Settling to 0.01% (±½LSB) of full-scale would require approximately 300nsec, or nine time constants. An operational amplifier

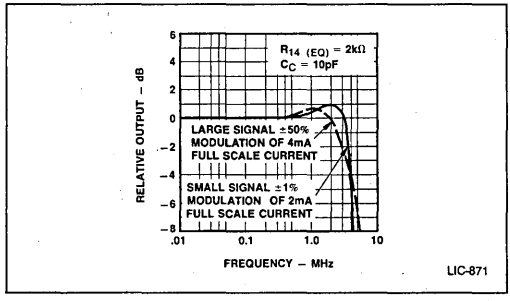


Figure 10. Reference Amplifier Frequency Response

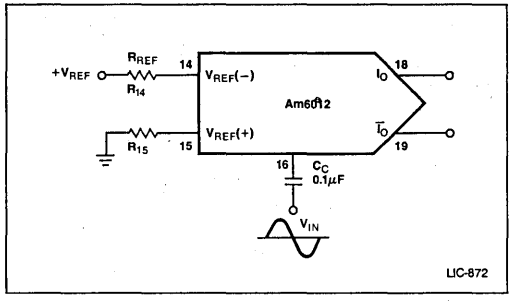


Figure 11. High-Impedance AC-Coupled Multiplication

is required if lower output impedance or larger output swings are desired, but some settling time will be lost because the output response is limited by the amplifier's slew rate and settling time. A feedback capacitor C_f (Figure 12) can compensate for the pole produced by the DAC output capacitance, op-amp input capacitance and the feedback resistor. Careful selection of this capacitor also optimizes the response time. Fastest operation is achieved by minimizing lead lengths, impedances and stray capacitances and bypassing the supplies to the DAC and operational amplifier.

The Am6012 has a maximum zero scale current of 0.1μA over the full temperature range. This represents only 1/10LSB zero offset error. Therefore, the only error that needs to be corrected will be the operational amplifier offset voltage. A typical amplifier, such as the LF156, has an offset voltage (V_{OS}) of 13mV over temperature and 0.5μV/°C per mV change in average temperature coefficient with V_{OS} adjusted to zero. This will produce a total error of 1LSB over temperature, whereas if the LF156A were used only ¼LSB error would occur. In Figure 13 the V_{OS} of the amplifier should be adjusted to zero with all of the bits turned OFF. One LSB is equal to 10/4096V = 2.44mV.

UNIPOLAR OPERATION (Figure 13)

Gain adjustment

Turn all the bits ON and adjust gain trimmer R_1 until the output is 9.9976V. This represents 1LSB less than the nominal 10V full-scale because the DAC outputs 4096 levels including zero so V_{FS} = 4095/4096 (10V) = 9.9976V.

BIPOLAR OPERATION (Figure 14)

This configuration will provide a bipolar output voltage from −10.000V to 9.9951V for an offset binary digital input code.

Offset Adjustment

With all bits OFF, adjust offset trimmer R_2 to give −10.000V at the output.

Gain

Turn all the bits ON, and adjust gain trimmer R_1 to give an output voltage of 9.9951V.

By using Figure 15 and Table 2, different input code formats and output polarities can be accommodated.

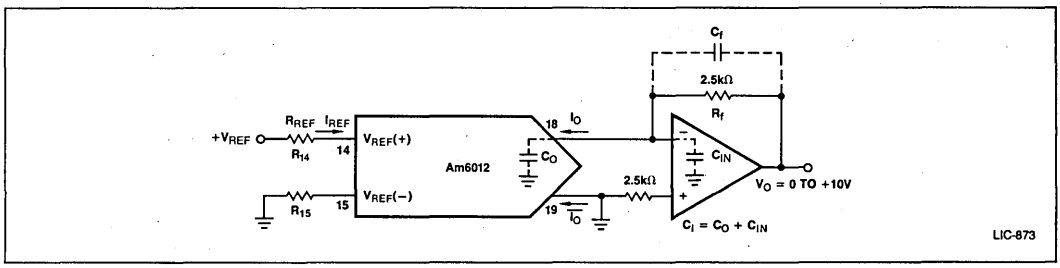


Figure 12. Voltage Output DAC

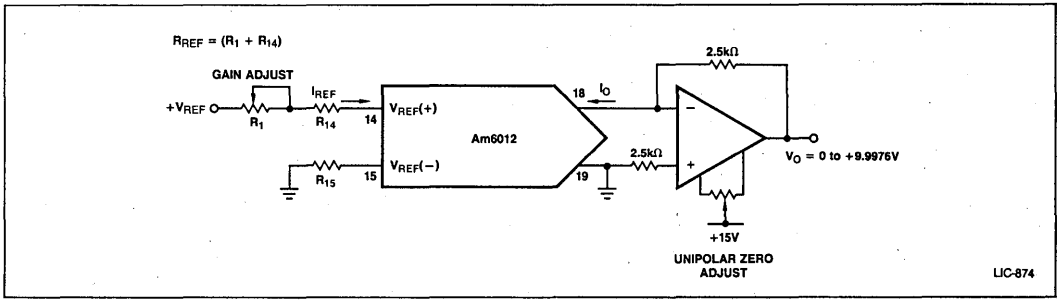


Figure 13. +10V Full-Scale Unipolar DAC

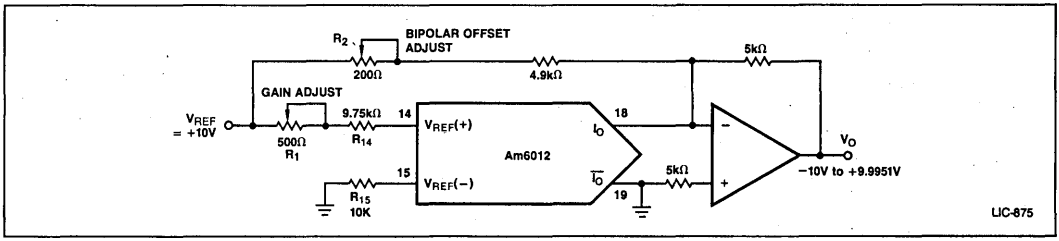


Figure 14. ±10V Full-Scale Bipolar DAC

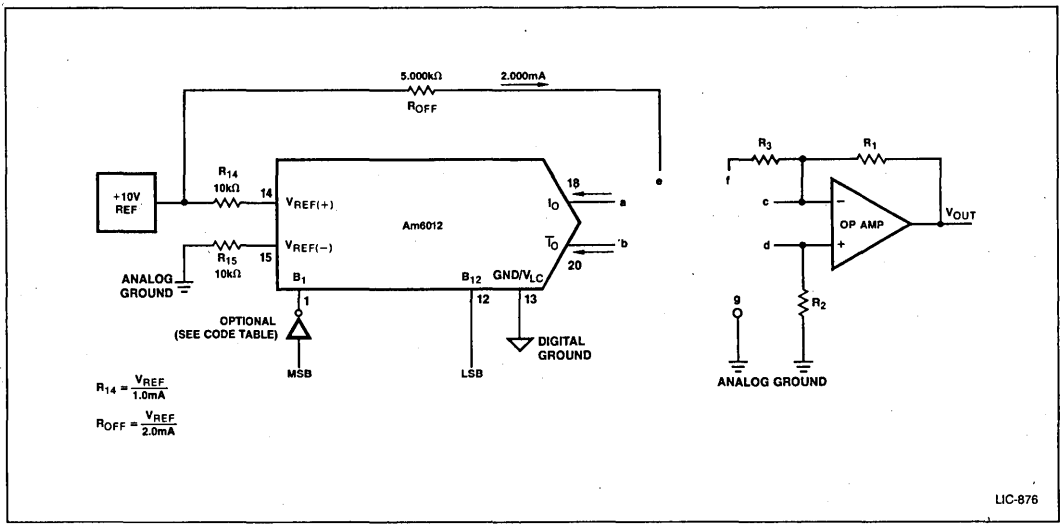


Figure 15. Voltage Output Connection

TABLE 2. INPUT CODE FORMATS

CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
UNIPOLAR	Straight binary; one polarity with true input code, true zero output.	a-c b-g R1 = R2 = 2.5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a-g b-c R1 = R2 = 2.5K	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
			Positive full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
			Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
SYM-METRICAL OFFSET	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
	1's complement; offset half scale, symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
			Negative full scale − LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
OFFSET WITH TRUE ZERO	Offset binary; offset half scale, true zero output.	e-a-c b-g R1 = R2 = 5K	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale − LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			− LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000
	2's complement; offset half scale true zero output MSB complemented (need inverter at B1).	e-a-c b-g R1 = R2 = 5K	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale − LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000

TWO-QUADRANT MULTIPLICATION DAC

There are two types of two-quadrant multiplication: bipolar digital, where the digital code controls the output polarity; and bipolar analog, where the analog reference input controls output polarity.

Figure 14 shows a bipolar digital two-quadrant multiplication with the output polarity controlled by an offset binary-coded input word. Two DACs are required for the bipolar analog method (Figure 16) because the Am6012 reference input cannot reverse the output polarity. A bipolar reference voltage is connected to the upper Am6012 and modulates the reference current by ±0.5mA around the quiescent current of 0.55mA. The lower Am6012 also has a reference current of 0.55mA, and both DACs have the same digital inputs. The lower Am6012 effectively subtracts out the quiescent 0.55mA of the upper Am6012 reference current at all digital input codes by differentially connecting them to an op-amp, thus the output voltage, V_{OUT}, is a product of a digital input code and a bipolar analog reference voltage.

FOUR-QUADRANT MULTIPLICATION

By combining bipolar digital and bipolar analog (two-quadrant multiplication) the output analog polarity is controlled by the analog reference input or by the offset binary digital input code. In Figure 17 two Am6012s are connected to implement a four-quadrant multiplying DAC. The circuit shows that a differential input signal can be accepted and differential output currents produced that can either be connected differentially to an op-amp to produce a voltage output or be used to drive balanced loads such as transformers, transducers and transmission lines.

USING THE Am6012 IN A/D CONVERTERS

Successive approximation is probably the method most widely used for implementing an ADC offering relatively fast conversion times with a low component count. Requiring 'n' comparisons for an 'n' bit conversion makes the technique capable of high speed.

As illustrated in Figure 18, the most significant bit is turned ON first, and the DAC output is compared with the input. The bit is switched OFF or left ON, depending upon whether the input signal is smaller or larger than the DAC output signal. The remaining bits are successively switched ON and comparisons made until all respective bits are either left ON or switched OFF. Each time one bit is tried, the DAC is required to settle to within ±½LSB. The Am2504 Successive Approximation Register (SAR) contains the necessary A/D logic, and the timing diagram (Figure 19) relates to the Am2504. Holding the start input LOW for at least one clock period initiates the conversion. The MSB is set LOW and all of the other bits are set HIGH for the first trial. Each trial takes one clock period, proceeding from the most significant to the least.

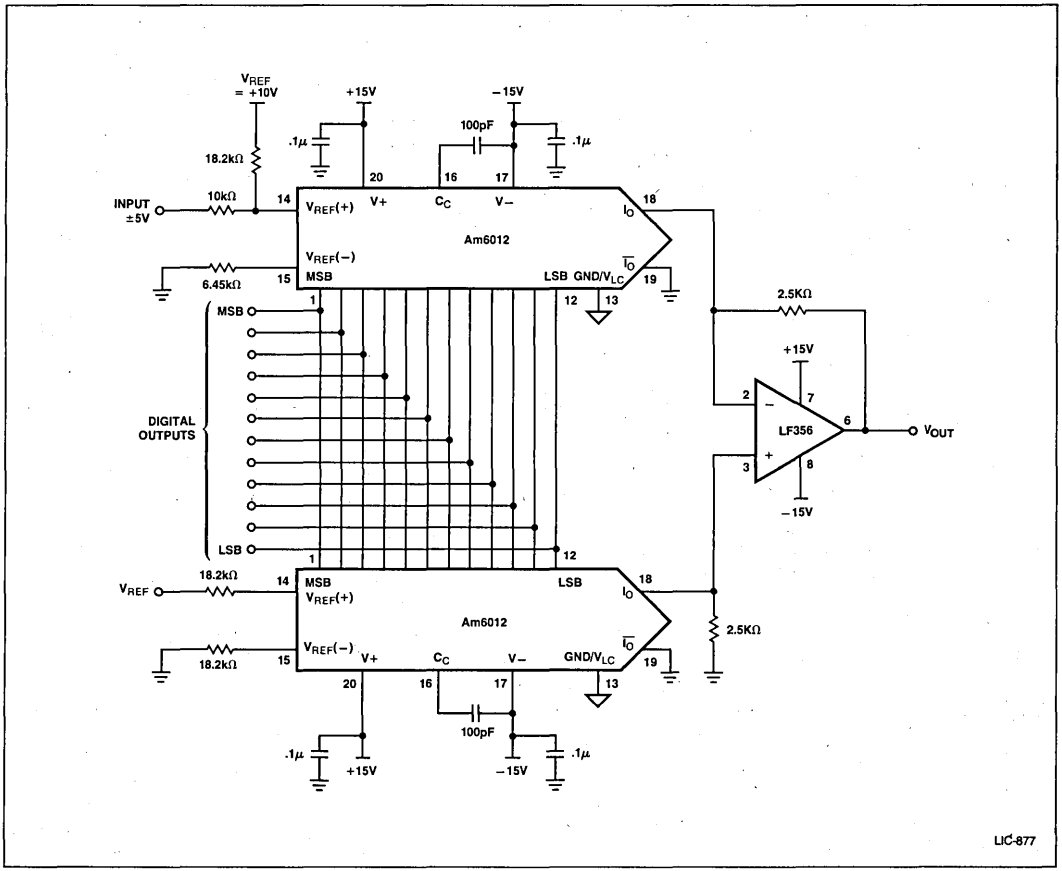


Figure 16. Bipolar Analog Two-Quadrant Multiplication

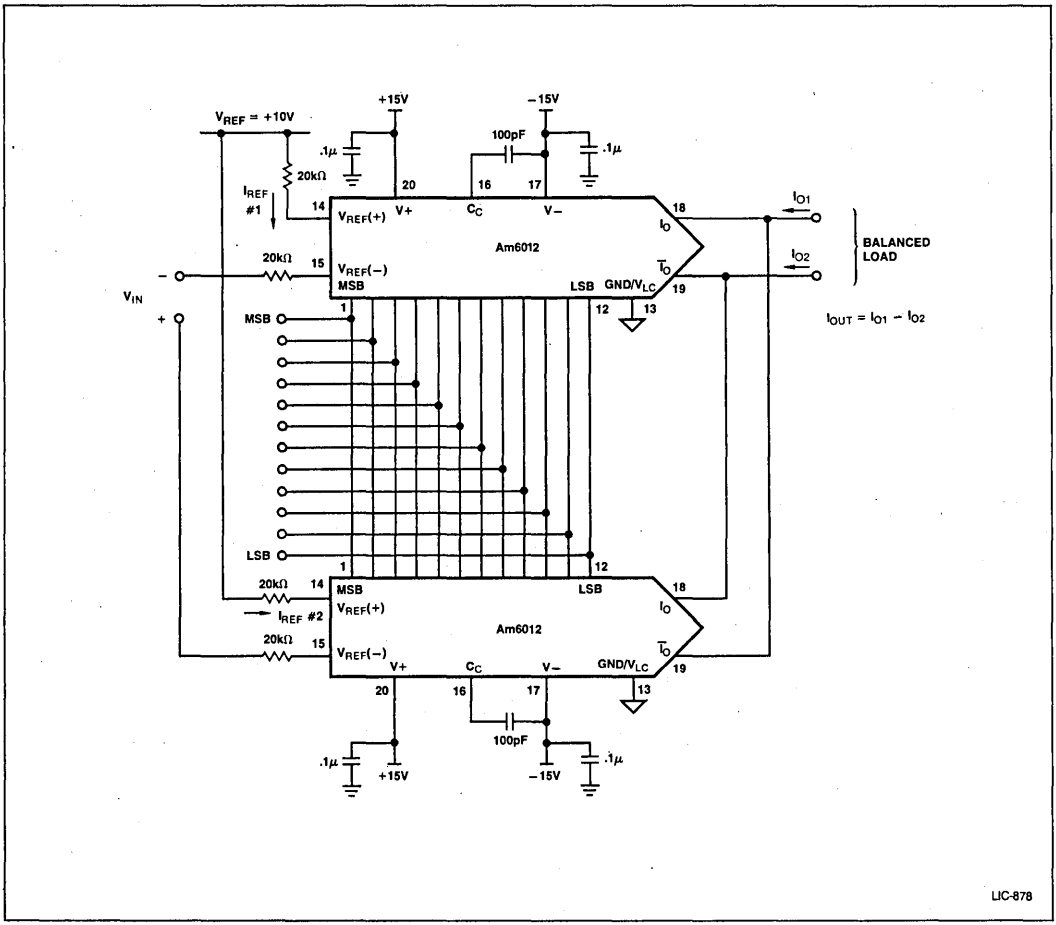


Figure 17. Four-Quadrant Multiplication with High Impedance Input

The time required to complete a 12-bit successive approximation A/D conversion is determined by adding the duration of the 12 trials, the comparator decision delays and one clock cycle. Three dynamic considerations must be taken into account: DAC output current settling time to ±½LSB, the comparator propagation delay, and the SAR propagation delay and setup requirements.

For example, with 300nsec allowed for the DAC to settle to ±½LSB, and 300nsec for the comparator response time plus 50nsec SAR logic delay a complete conversion could result in 8.5μsec.

A major factor affecting the settling time of the DAC is the RC time constant formed by the input resistor (R_{IN}) and the DAC output capacitance (C_O) plus any stray capacitance present at the summing node. The settling to within ±½LSB at 12 bits (±0.01%) requires 9.2 RC time constants. Thus the Am6012, with an output capacitance of 20pF, would influence the settling time if R_{IN} were around 300 ohms. But R_{IN} would become the dominant factor when greater than 500 ohms. Hence, if the A/D full-scale range were 10V and the DAC current was 4mA, then R_{IN} would be equal to 2.5K, resulting in a time constant of 50nsec and a settling time of approximately 500nsec. Lowering the effective resistance at the summing node is a compromise between DAC settling time and comparator overdrive because the ½LSB current is only 0.5μA and, for an equivalent resistance of 500 ohms, would only result in a DAC output voltage corresponding to ½LSB or 0.25mV, which is inadequate for most comparators. With R_{IN} of 2.5K this would result in ½LSB of 1.25mV, which is an adequate overdrive for the Am111s (Figure 18), producing a response time of 200nsec. The propagation delay of the SAR is 50nsec. Hence, the total conversion time is 11.5μsec for a full-scale signal range of 10V.

The input impedance of an ADC changes during the conversion process and can alter the performance of the input amplifier, or sample and hold amplifier if used. Because the comparison point can swing by a large amount, the input current can be modulated. The output impedance of the input amplifier is made LOW by the loop gain of the feedback amplifier. This gain reduces at high frequencies, and the output impedance rises to its open loop value, which is usually between 10 and 200 ohms.

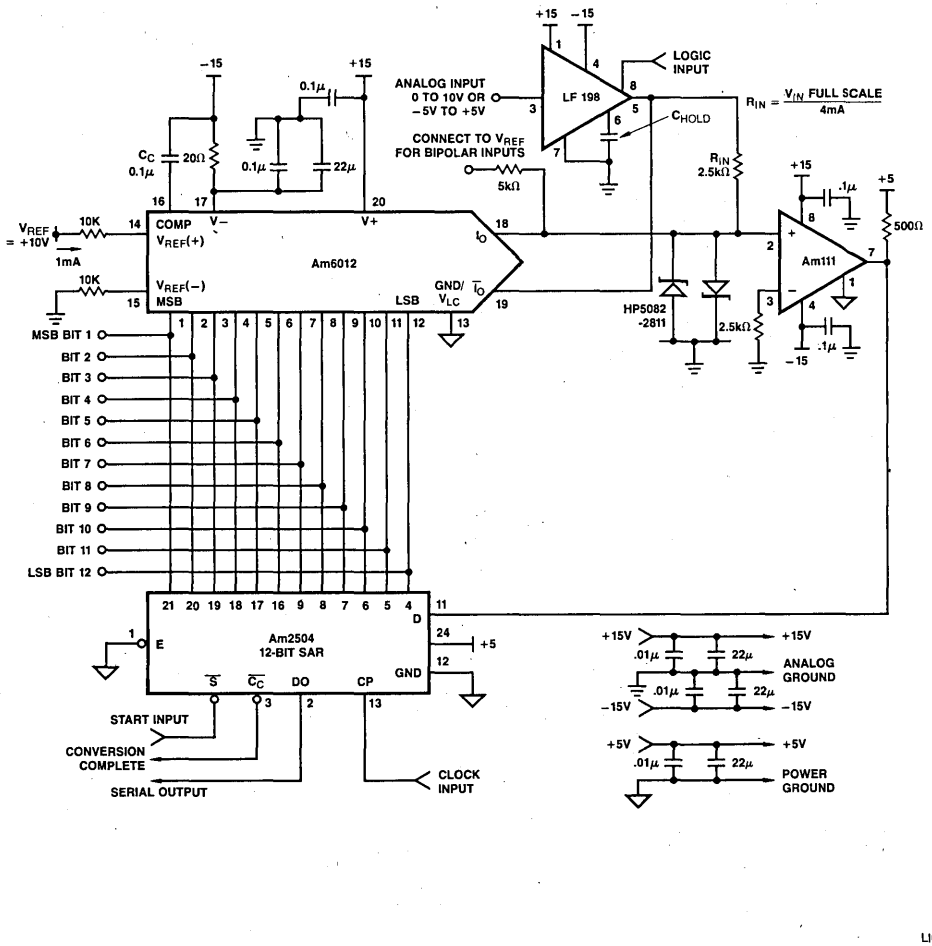


Figure 18. Fast Precision Successive Approximation A/D Converter

Errors can be introduced into the instantaneous input voltage if the bandwidth of the amplifier is not sufficient and the output of the input amplifier does not return to its normal voltage before the converter makes a comparison. The Am6012 offers dual complementary outputs that can present a constant load current to the input signal significantly reducing switching transients and increasing system throughput. Because the full-scale output current of the Am6012 is 4mA, smaller load resistors can be used. These minimize the output RC delay that usually dominates the settling time for a 12-bit ADC. In the design of high-resolution, high-speed ADCs, one must ensure that the analog wiring be kept as short as possible and be separated from the vicinity of digital lines. This precaution refers especially to the comparator output which can capacitively couple edge transients back to the input of the comparator and cause the comparator to oscillate.

Digital ground and analog ground should only meet at one point to prevent digital ground currents from creating voltage errors in the analog ground.

Ground loops should also be avoided within the analog sections since they can introduce errors. Adequately bypassing supplies is essential for high-speed and high-resolution ADCs and should include high-frequency ceramic as well as tantalum capacitors to decouple the high-frequency components of the digital switching transients.

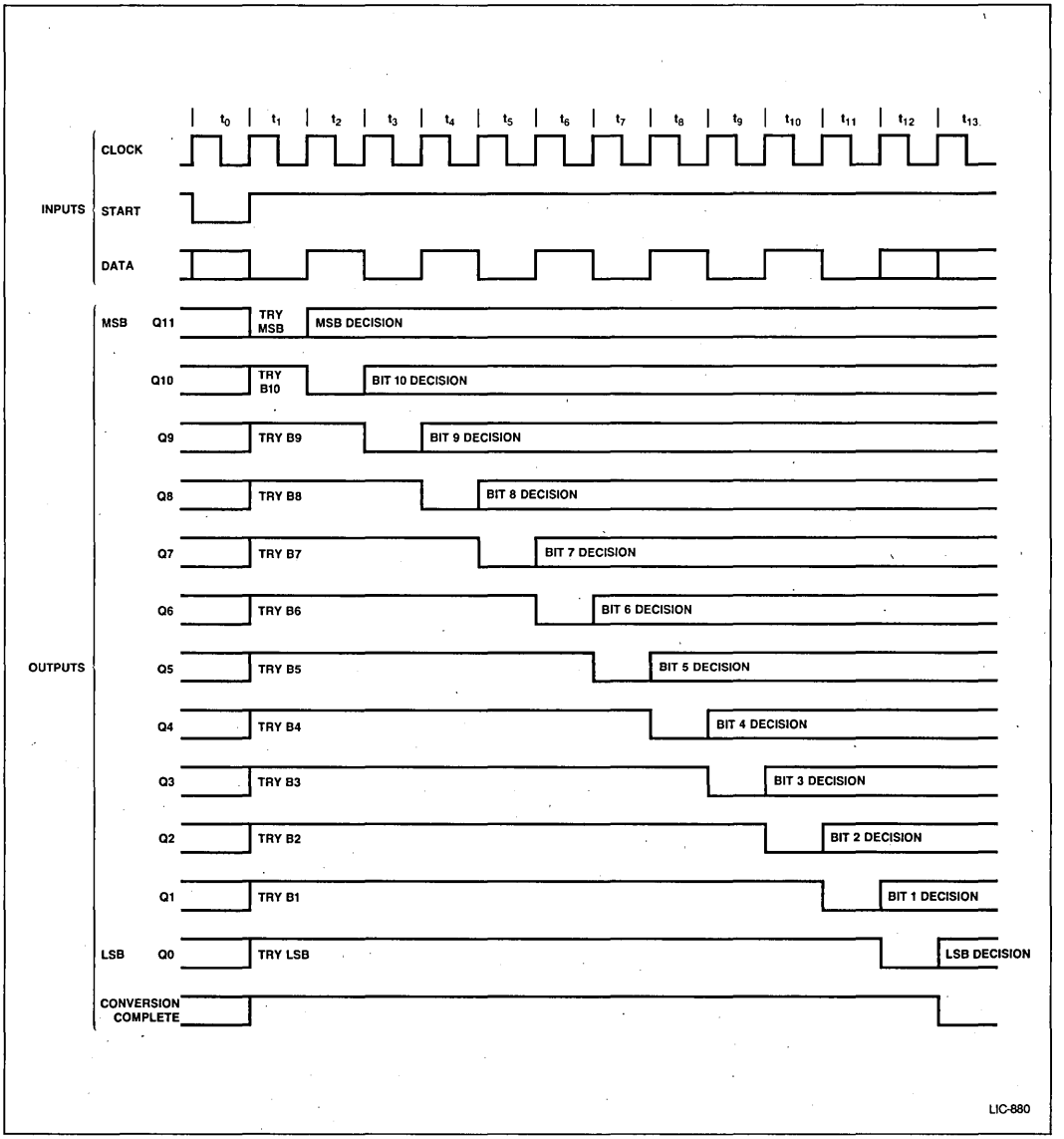


Figure 19. Typical Timing Diagram for Successive Approximation Converter

MICROPROCESSOR-BASED SYSTEM INTERFACING

The Am6012 can be interfaced to a microprocessor-based system. But microprocessors with an 8-bit bus have the problem of interfacing to the 12-bit DAC. This is solved by breaking the 12-bit word into 8- and 4-bit bytes and storing each into a memory location. Figure 20 shows a 12-bit DAC interfaced to the popular Am9080A using an Am9555 Programmable Peripheral Interface. This allows two Am6012s to be connected. For a simpler system the Am9555 could be replaced with a 12-bit latch and some control logic.

Interfacing the Am6012 to a 16-bit microprocessor such as the AmZ8001/8002 is shown in Figure 21. The DAC peripheral location is addressed by the CPU and decoded by the AmZ8136 (8-bit decoder with control storage), which contains input latches, allowing the peripheral address to be latched and decoded from the address bus. The $\overline{AS}$ (address strobe) signal from the CPU informs the decoder when the address is stable and is used as the input register latch command. Two transparent latches are used to latch the data off the address/data bus. The $\overline{DS}$ (data strobe) command produces a $\overline{CS}$ (chip select) to force the AmZ8173 octal

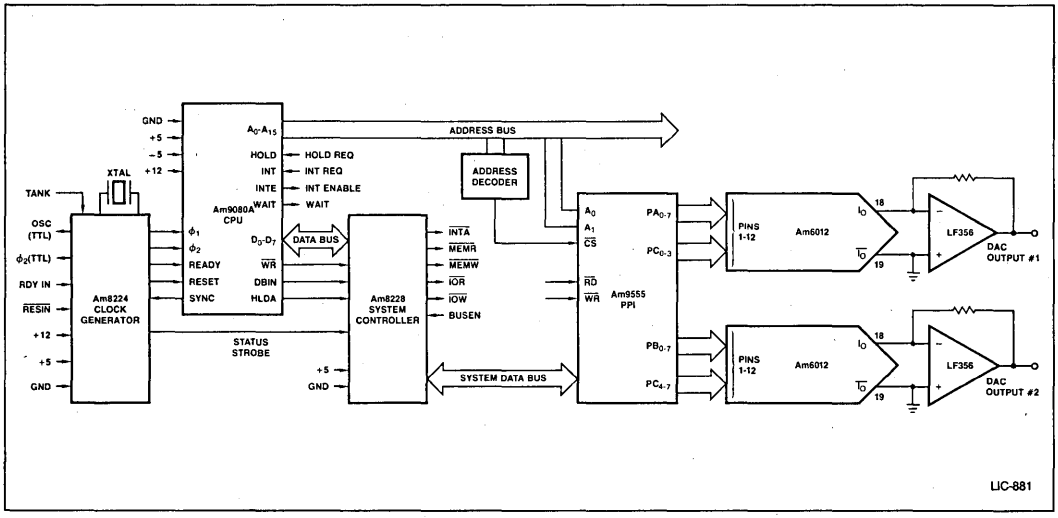


Figure 20. Two Am6012 D/A Converters Controlled by an Am9555 PPI

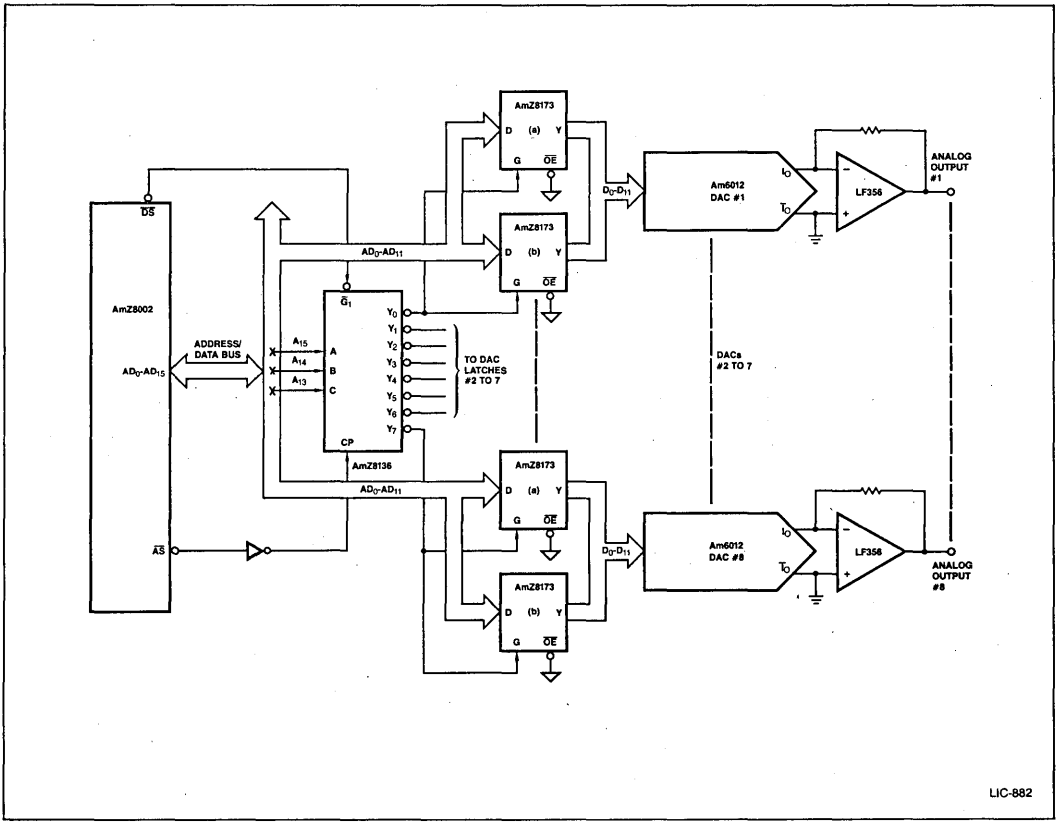


Figure 21. AmZ8000 Interface for Am6012 12-Bit DAC

latches into their transparent mode. When $\overline{DS}$ goes HIGH this causes $\overline{CS}$ to go HIGH and retains the data in the AmZ8173. This prevents erroneous data from appearing at the Am6012 inputs during CPU operations and causing the output from displaying the wrong information. The AmZ8000 has the capability of outputting not only single words of data, but also blocks of data from contiguous memory locations. The time for each data transfer is 10 clock cycles, resulting in a data update time of 2.5μsec. Additional time can be allowed for the DAC to settle by including extra WAIT states. Each wait state period is 250nsec.

When used in a successive approximation type of ADC described earlier, the Am6012 can be interfaced to an Am9080A to allow analog information into the microprocessor system (Figure 22). The ADC data conversion procedure is controlled by the Am9080A Microprocessor set (Am9080A 8-bit microprocessor, Am8224 clock generator and driver, and Am8228 system controller and bus driver). The Am26S02 is used as the START monostable circuit and is activated by ($\overline{CS}$ = 0, and $\overline{IOW}$ = 0). START ADC command sets the $\overline{S}$ input of the SAR circuit Am2504 to a logic 0. The width of the monostable pulse must be greater than the period of the DATA CLOCK signal to initialize the SAR logic. The DATA CLOCK period must be sufficiently long to allow for the worst-case settling time of the Am6012 DAC and comparator Am111 and to ensure valid data at the SAR input. After $\overline{S}$ goes LOW the first clock sets $\overline{C_C}$, changing it to logic ONE, and the sample and hold reverts back to the sample mode. The microprocessor is then allowed to resume its function by removing the logic ZERO from the RDYIN input of the Am8224 chip. Logic ONE at the SAR's $\overline{S}$ input prevents DATA CLOCK from changing the digital data outputs of the SAR after the completion of a conversion. When the microprocessor issues a READ ADC command ($\overline{CS}$ = 0, $\overline{IOR}$ = 0), the data buffer (Am9555) is enabled to transfer the data outputs of the SAR to the system data bus and into the microprocessor accumulator where on a subsequent memory write command stores the data into a memory location. The ADC must be given another START ADC command by the microprocessor before another conversion cycle can be started.

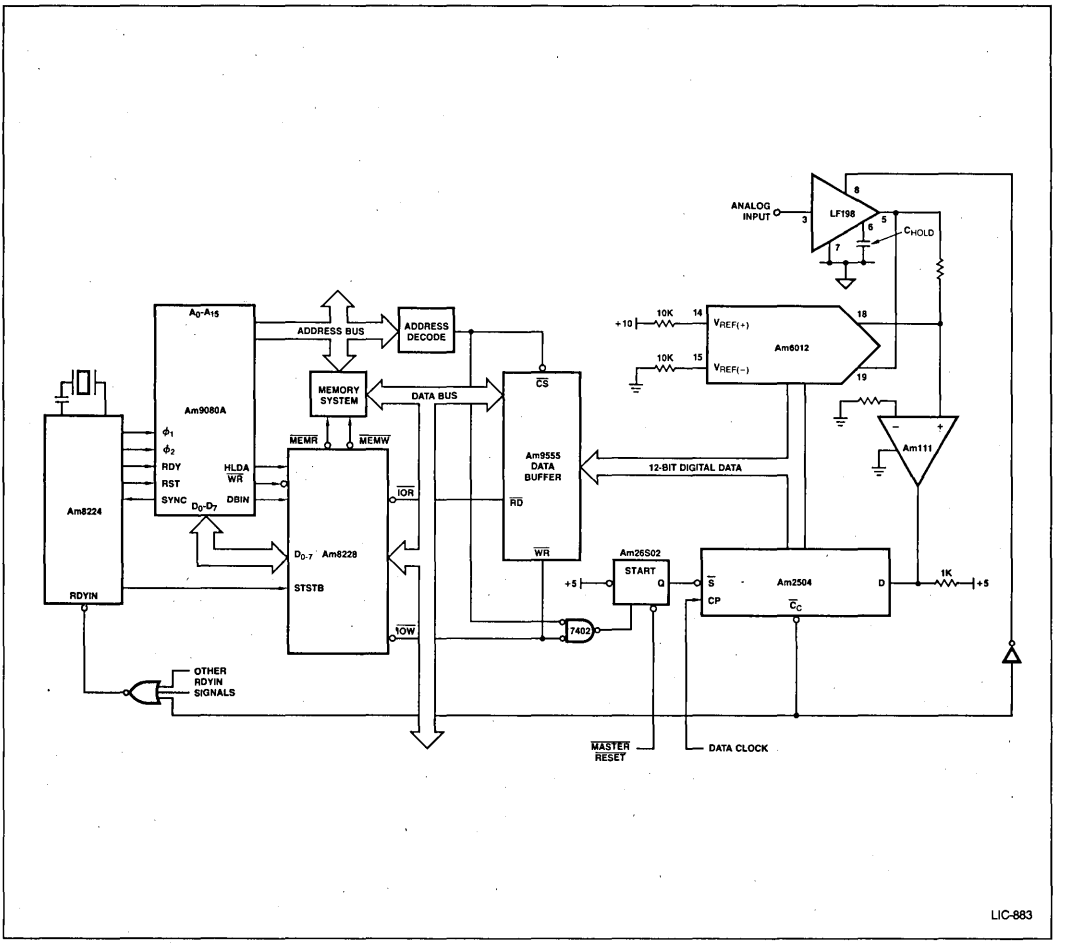


Figure 22. Microprocessor Controlled 12-Bit Analog to Digital Acquisition System

Am6014

14-Bit Multiplying D/A Converter

PRELIMINARY DATA

3

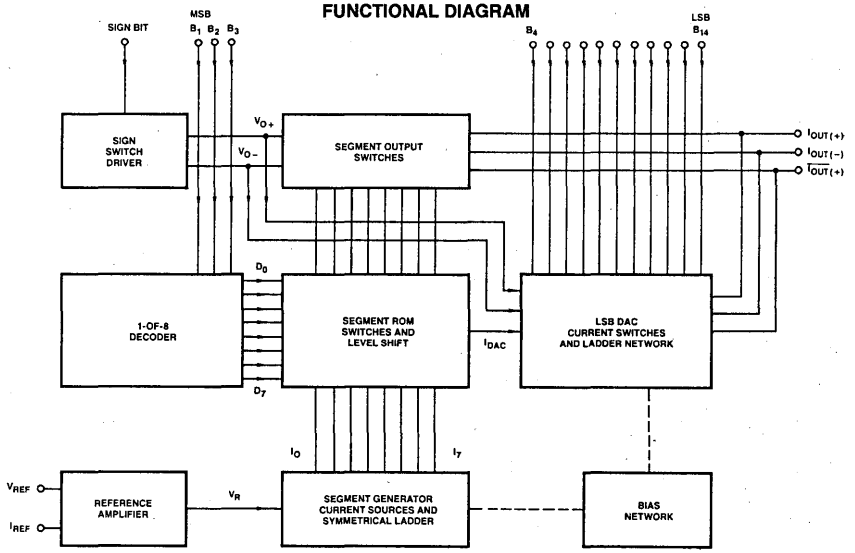
DISTINCTIVE CHARACTERISTICS

- 14 bit monotonic over temperature
- Differential non-linearity to ±0.006% (14 bits)
- Inherently monotonic
- Fast settling output current: 500ns
- Full scale current 8mA
- High output impedance and high output compliance: −5 to +5V
- Differential current outputs
- Sign switch bit enables sign-magnitude input coding for 15 bit dynamic range
- Low power dissipation: 350mW

GENERAL DESCRIPTION

The Am6014 is a monolithic 14-bit multiplying digital-to-analog-converter which uses untrimmed thin film resistors and a segmented ladder design to provide monotonicity and 14-bit differential linearity. It also offers a wide power supply range, high voltage compliance, and complementary high impedance outputs, thus permitting greater versatility and differential operation. Output full scale current is specified at 8mA, allowing use of smaller load resistors to minimize the output RC delay, and a sign-bit input allows sign-magnitude code format capability. The circuit also provides the user with output, gain and thin film reference input scaling resistors which track with the thin film resistors used in the ladder and segment sources.

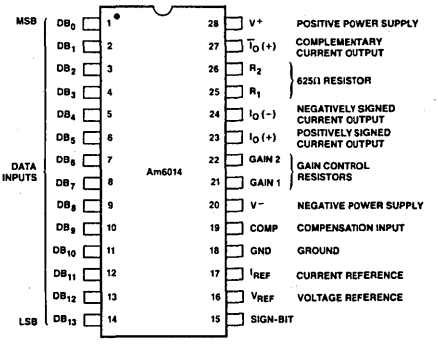
Am6014 BLOCK DIAGRAM FUNCTIONAL DIAGRAM



ORDERING INFORMATION

Order Number	Package	Temperature Range	Differential Nonlinearity
Am6014DM	Hermetic DIP	−55 to +125°C	±0.006%
Am6014DC	Hermetic DIP	0 to +70°C	±0.006%
Am6014XC	Dice	0 to +70°C	±0.006%

CONNECTION DIAGRAM D-28



03922A-ANA

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65 to +150°C
Lead Temperature (soldering, 10sec)	300°C
Power Supply Voltage (V+)	+18V
Power Supply Voltage (V−)	−18V
V+ Supply to V− Supply	25V
Logic Inputs	−5 to +18V
Analog Current Outputs	−8 to +12V
Reference Input Voltage	V− to V+
Reference Input Current	2.5mA
Power Dissipation	700mW

ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -15V$, $I_{REF} = 2.0mA$ $T_A = 0$ to $-70°C$

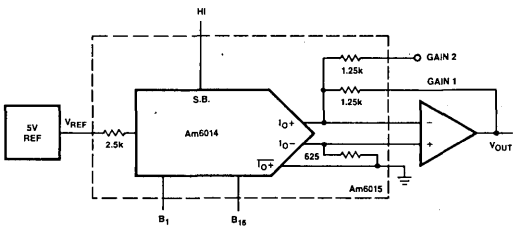
Parameters	Description		Test Conditions	Min	Typ	Max	Units
	Resolution				14		Bits
	Monotonicity				14		Bits
D.N.L.	Differential Nonlinearity		Deviation from ideal step size		14		Bits
N.L.	Nonlinearity		Deviation from ideal straight line		12		Bits
I_{FS}	Full Scale Current		$V_{REF} = 5.0000V$ $R_{REF} = 2.5000K$ ohm $T_A = 25°C$		7.9995		mA
TCI_{FS}	Full Scale Tempco				±.11		LSB/°C
V_{OC}	Output Voltage Compliance		D.N.L. Specification guaranteed over compliance range R_{OUT} > 10megohms typ.		±5		Volts
I_{FSS}	Full Scale Symmetry		$I_{FS} - \overline{I_{FS}}$		±0.4		μA
I_{ZS}	Zero Scale Current				20		nA
t_s	Settling Time (Includes t_{PLH})		To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$		500		ns
t_{PLH} t_{PHL}	Propagation Delay − all bits		50 to 50%		30		ns
C_{OUT}	Output Capacitance				20		pF
V_{IL}	Logic Input Levels	Logic "0"			−	0.8	Volts
V_{IH}		Logic "1"		2.0	−	−	
I_{IN}	Logic Input Current		$V_{IN} = -5$ to $+18V$			40	μA
V_{IS}	Logic Input Swing		$V- = -15V$	−5		+18	Volts
I_{REF}	Reference Current Range			0.4	2.0	2.2	mA
dI/dt	Reference Input Slew Rate		CC = 0pF		8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity		$V+ = 4.5$ to $+5.5V$, $V- = -15V$		±0.001		%FS/%
$PSSI_{FS-}$			$V- = 13.5$ to $-16.5V$, $V+ = 5V$		±0.001		
I+	Power Supply Current		$V+ = +5V$, $V- = -15V$		+5.6		mA
I−					−20		
P_D	Power Dissipation		$V+ = +5V$, $V- = -15V$		370		mW

FUNCTIONAL PIN DESCRIPTIONS

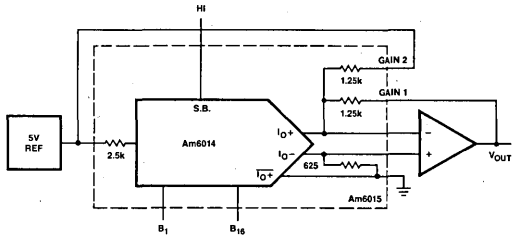
Mnemonic	Description
$DB_0 - DB_{13}$	DB_0 (MSB) through DB_{13} (LSB) are the data input pins to the DAC.
SIGN-BIT	This input pin represents the sign of the data bits $DB_0 - DB_{13}$. If SIGN-BIT is held HIGH, the output current flows from I_O (+); if LOW, current flows from I_O (−).
V_{REF}	Input reference voltage pin. May be used instead of I_{REF}. A 5V input will give a 8mA full scale output. V_{REF} takes advantage of the internal input resistors.
I_{REF}	Input reference current pin. May be used instead of V_{REF}. A 2mA input will give a 8mA full scale output. I_{REF} should be used instead of V_{REF} in situations where high absolute accuracy is required.
COMP	Compensation pin for the input amplifier. Should be connected via a 0.01μF capacitor to ground.
GAIN1	Internal gain resistor (1.25K) connected to I_O (+). May be grounded, allowed to float, or connected to a 5 volt reference for signed magnitude (−10V), unipolar (0 to 10V), and bipolar (−5 to +5V) operation.
GAIN2	Internal gain resistor (1.25K) connected to I_O (+). Should be connected to external op-amp output. External gain resistors should be used in situations demanding high absolute accuracy.
I_O (+)	DAC output pin carries current when SIGN-BIT pin is held HIGH.
I_O (−)	DAC output pin carries current when SIGN-BIT pin is held LOW.
R_1, R_2	Connections to an internal 625 resistor that may be tied between I_O (−) and I_O (+) for sign-magnitude operation.
$\overline{I_O}$ (+)	Complimentary DAC output pin carries current when the SIGN-BIT is HIGH. This current is 7.9995mA less I_O (+).

Figure 1. Typical Output Connections

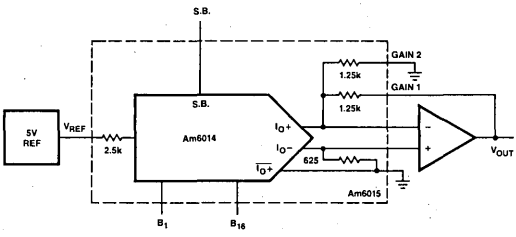
Unipolar 0 to 10V True Zero



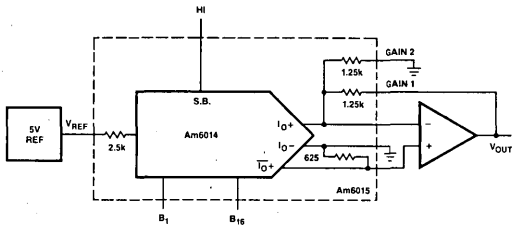
Bipolar −5 to +5V True Zero



Signed Magnitude ±10V True Zero



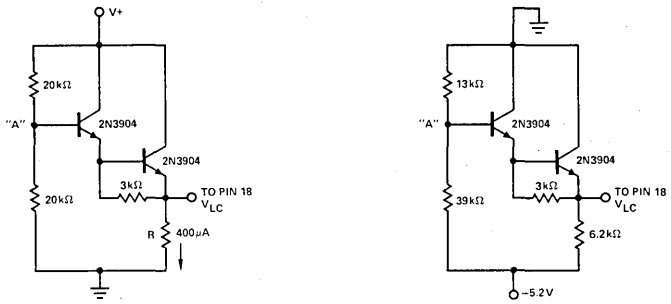
Symmetrical Offset ±10V No True Zero



APPLICATIONS

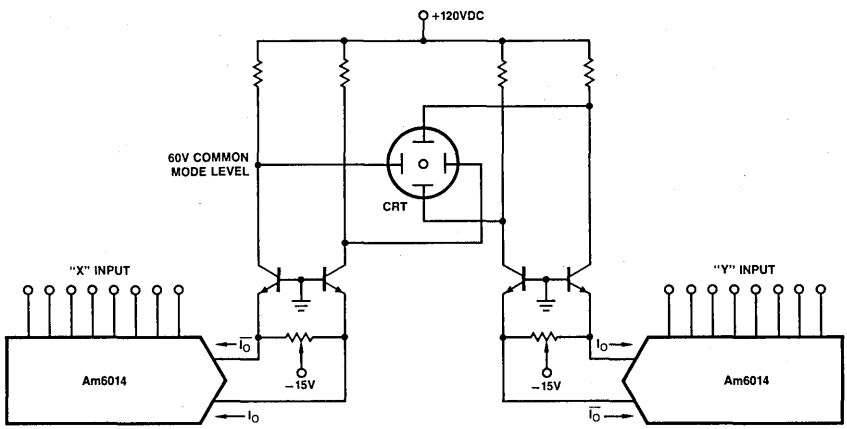
CRT Graphic Displays	Control Systems
Digital Audio	Data Acquisition
PCM Telephony	Data Distributions

Figure 2. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs



Notes: 1. Set the voltage "A" to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the DAC on ±15V supplies.

Figure 3. CRT DISPLAY DRIVER



Notes: 1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Am6070

Companding D-to-A Converter for Control Systems

Distinctive Characteristics

- Tested to μ-255 companding law
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM, audio, and 8-bit μ-P systems
- Output dynamic range of 72 dB
- 12-bit accuracy and resolution around zero
- Sign plus 12-bit range with sign plus 7-bit coding
- Improved pin-for-pin replacement for DAC-76
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

3

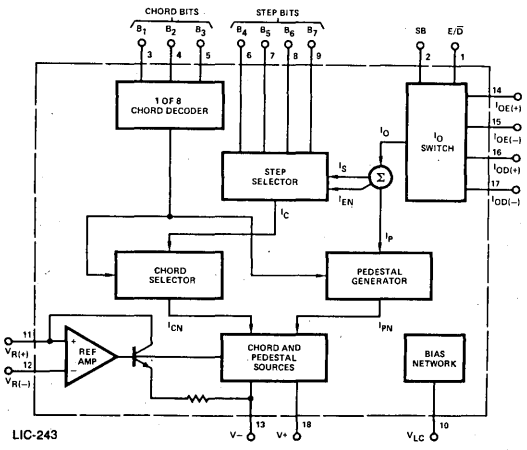
GENERAL DESCRIPTION

The Am6070 monolithic companding D/A converter achieves a 72dB dynamic range which is equivalent to that achieved by a 12-bit converter.

The transfer function of the Am6070 complies with the Bell system μ-255 companding law, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB) and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. Accuracy and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature range.

Applications for the Am6070 include digital audio recording, servo-motor controls, electromechanical positioning, voice synthesis, secure communications, microprocessor controlled sound and voice systems, log sweep generators and various data acquisition systems.

FUNCTIONAL BLOCK DIAGRAM



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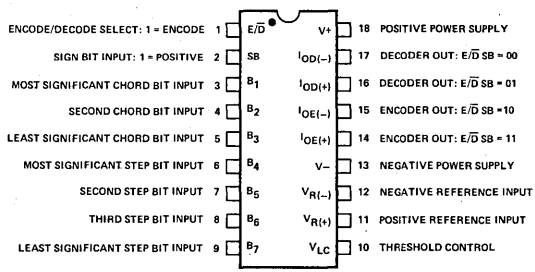
CONNECTION DIAGRAM
D-18-1



Top View
Pin 1 is marked for orientation.

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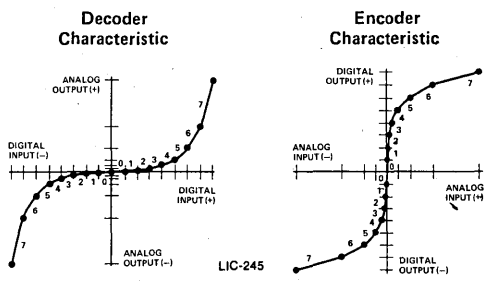
ORDERING INFORMATION*

Part Number	Temperature	Accuracy
Am6070ADM	−55°C to +125°C	±1/2 step
Am6070DM	−55°C to +125°C	±1 step
Am6070ADC	0°C to +70°C	±1/2 step
Am6070DC	0°C to +70°C	±1 step

*Also available with burn-in processing. To order add suffix B to part number.

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS



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MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, (20 log ($I_{7,15}/I_{0,1}$))

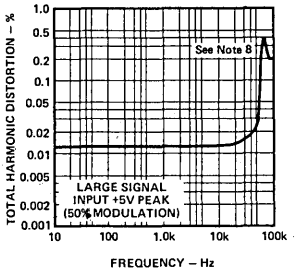
ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 528μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125C, for the military grade, and for all 4 outputs unless otherwise specified.

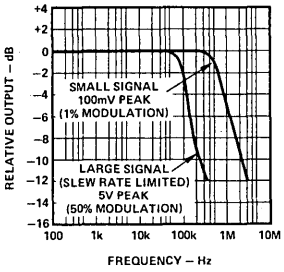
Parameter	Description	Test Conditions	Am6070ADM Am6070ADC Min.	Typ.	Max.	Am6070DM Am6070DC Min.	Typ.	Max.	Units
t_S	Settling Time	To within ±1/2 step at T_A = 25°C output switched from I_{ZS} to I_{FS}		300	500		300	500	ns
$I_{FS(D)}$ $I_{FS(E)}$	Chord Endpoint Accuracy	Guaranteed by output current error specified below.			±1/2			±1	Step
	Step Nonlinearity				±1/2			±1	Step
	Full Scale Current Deviation From Ideal				±1/2			±1	
					±1/2			±1	
ΔI_O	Output Current Error	V_{REF} = 10.000V R_{REF+} = 18.94kΩ R_{REF-} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1.			±1/2			±1	Step
$I_{O(+)} - I_{O(-)}$	Full Scale Symmetry Error	V_{REF} = 10.000V R_{REF+} = 18.94kΩ R_{REF} = 20kΩ −5.0V ≤ V_{OUT} ≤ +18V Error referred to nominal values in Table 1		1/40 1/40	1/8 1/8		1/20 1/20	1/4 1/4	Step Step
I_{EN}	Encode Current	Additional output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
I_{ZS}	Zero Scale Current	Measured at selected output with 000 0000 input		1/40	1/4		1/20	1/2	Step
ΔI_{FS}	Full Scale Drift	Operating temperature range		±1/20	±1/4		±1/10	±1/2	Step
V_{OC}	Output Voltage Compliance	Full scale current change ≤1/2 step	−5.0		+18	−5.0		+18	Volts
I_{DIS}	Disable Current	Output leakage Output disabled by E/$\overline{D}$ and SB		5.0	50		5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	0	2.0	4.2	mA
V_{IL} V_{IH}	Logic Input Levels: Logic "0" / Logic "1"	V_{LC} = 0V	2.0		0.8	2.0		0.8	Volts
I_{IN}	Logic Input Current	V_{IN} = −5.0V to +18V			40			40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5.0		+18	−5.0		+18	Volts
$I_{B\ REF-}$	Reference Bias Current			−1.0	−4.0		−1.0	−4.0	μA
di/dt	Reference Input Slew Rate		0.12	0.25		0.12	0.25		mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	V+ = 4.5 to 18V, V− = −15V V− = 10.8 + −18V, V+ = 15V		±1/20 ±1/10	±1/2 ±1/2		±1/20 ±1/10	±1/2 ±1/2	Step Step
I+ I−	Power Supply Current	V+ = +5.0 to +15V, V− = −15V I_{FS} = 2.0mA		2.7 −6.7	4.0 −8.8		2.7 −6.7	4.0 −8.8	mA
P_D	Power Dissipation	V− = −15V, V_{OUT} = 0, I_{FS} = 2.0mA; V+ = 5.0V		114	152		114	152	mW
		V+ = +15V		141	192		141	192	

TYPICAL PERFORMANCE CURVES

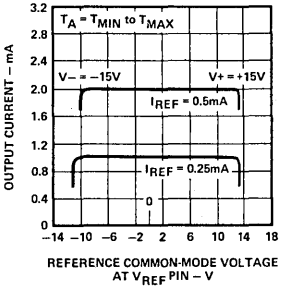
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



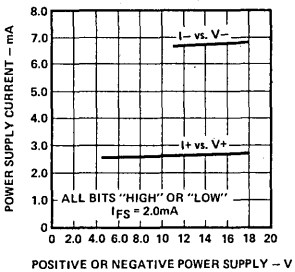
Reference Amplifier Input Frequency Response



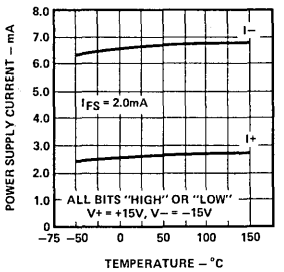
Reference Amplifier Input Common-Mode Range (Note 9)



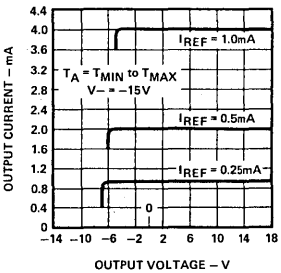
Power Supply Currents Versus Power Supply Voltages



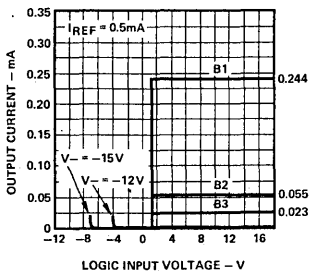
Power Supply Currents Versus Temperature



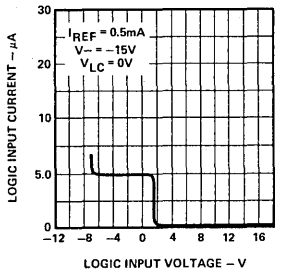
Output Current Versus Output Voltage (Output Voltage Compliance)



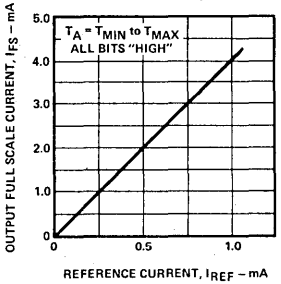
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current



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Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
NOMINAL DECODER OUTPUT CURRENT LEVELS IN μA

	CHORD							
STEP	0	1	2	3	4	5	6	7
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
STEP SIZE	.5	1	2	4	8	16	32	64

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM FULL SCALE

	CHORD							
STEP	0	1	2	3	4	5	6	7
0	–	−47.73	−38.18	−30.82	−24.20	−17.90	−11.74	−5.65
1	−72.07	−46.73	−37.51	−30.24	−23.66	−17.37	−11.22	−5.13
2	−66.05	−45.84	−36.88	−29.70	−23.15	−16.87	−10.73	−4.65
3	−62.53	−45.03	−36.30	−29.18	−22.66	−16.40	−10.27	−4.19
4	−60.03	−44.29	−35.75	−28.70	−22.21	−15.96	−9.83	−3.75
5	−58.10	−43.61	−35.24	−28.24	−21.77	−15.53	−9.41	−3.33
6	−56.51	−42.98	−34.75	−27.80	−21.36	−15.13	−9.01	−2.94
7	−55.17	−42.39	−34.29	−27.39	−20.96	−14.74	−8.63	−2.56
8	−54.01	−41.84	−33.85	−26.99	−20.58	−14.37	−8.26	−2.19
9	−52.99	−41.32	−33.44	−26.61	−20.22	−14.02	−7.91	−1.84
10	−52.07	−40.83	−33.04	−26.25	−19.87	−13.68	−7.57	−1.51
11	−51.25	−40.37	−32.66	−25.90	−19.54	−13.35	−7.25	−1.18
12	−50.49	−39.93	−32.29	−25.57	−19.22	−13.03	−6.93	−0.87
13	−49.80	−39.51	−31.95	−25.25	−18.91	−12.73	−6.63	−0.57
14	−49.15	−39.11	−31.61	−24.94	−18.61	−12.43	−6.34	−0.28
15	−48.55	−38.73	−31.29	−24.63	−18.32	−12.15	−6.06	0.00

THEORY OF OPERATION

Functional Description

The Am6070 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/$\overline{D}$), input signal. A logic 1 applied to the E/$\overline{D}$ input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/$\overline{D}$ input places the Am6070 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ-225 logarithmic law which can be written as follows:

$$Y = 0.18 \text{ℓn} (1 + \mu |X|) \text{ sgn } (X)$$

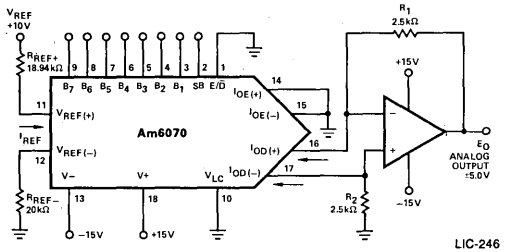
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
μ = 255

The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/$\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 0.5μA found in the first chord near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6070 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/$\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/$\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,

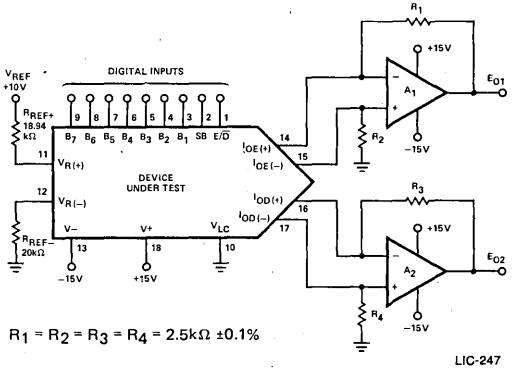


$I_{REF} = V_{REF}/R_{REF}$

IDEAL VALUES: I_{REF} = 528μA, I_{FS} = 2007.75μA

	E/$\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	–5.019V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

LINE SELECTION TABLE

TEST GROUP	E/$\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	I_{OE} (+)	(E_{O1}/R_1)
2	1	0	I_{OE} (–)	(E_{O1}/R_2)
3	0	1	I_{OD} (+)	(E_{O2}/R_3)
4	0	0	I_{OD} (–)	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.25μA, which will bring the ideal encode current value for step 0 on chord 0 to ±0.25μA with respect to the corresponding decode current value of 0.0μA. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6070 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\overline{S}$, and Conversion Complete, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6070. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6070.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6070 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6070 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6070. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6070 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

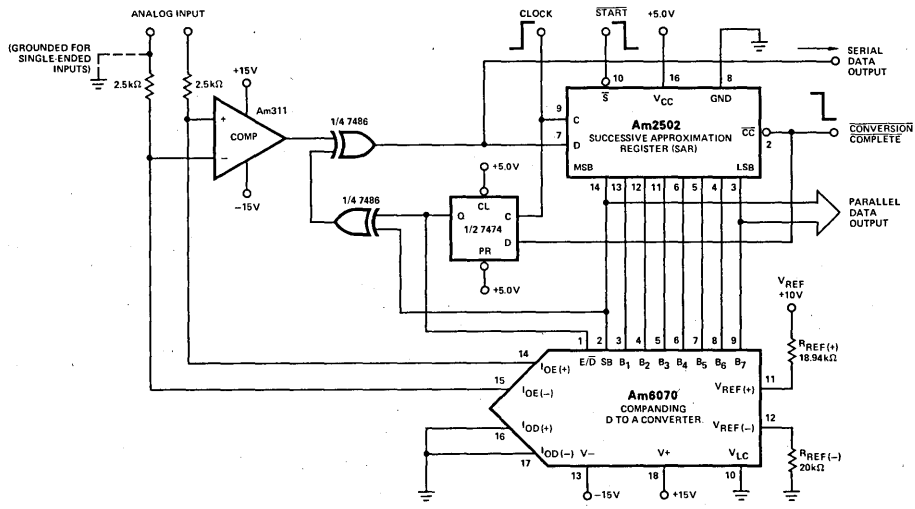


Figure 3. Detailed Encoder Connections.

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2.5kΩ, also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528μA. The corresponding ideal full scale decode and encode current values are 2007.75μA and 2039.75μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current I_{REF} = 528μA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6070 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 528μA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + (2 \bullet I_{REF} \bullet 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

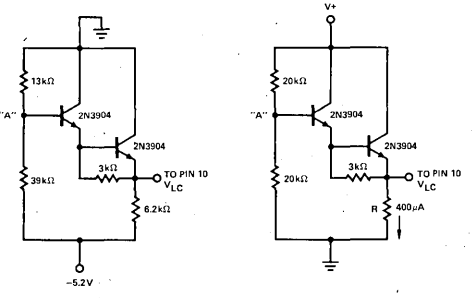
Negative Output Voltage Compliance $V_{OC(-)}$

V− \ I_{REF} (I_{FS})	264μA (1mA)	528μA (2mA)	1056μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6070 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

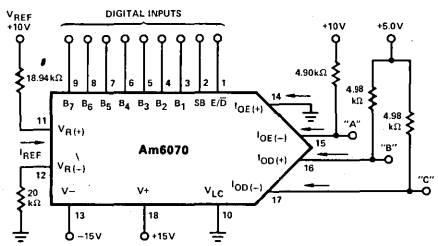
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs. LIC-249



INPUT CODE (E/D, SB, B_1, . . ., B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.02	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections. LIC-250

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Step (S) \ Chord (C)		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:

$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$

where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:

$I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}$ (μA)

where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Normalized Encode Level (Sign Bit Excluded)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
Step Size		2	4	8	16	32	64	128	256

$I_{C,S} = 2[2^C (S+17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

ADDITIONAL DECODE OUTPUT CURRENT TABLES (Cont.)

Table 5
Decoder Step Size Summary

Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 6
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	−48.55
1	93	23.25	1.16%	−38.73
2	219	54.75	2.73%	−31.29
3	471	117.75	5.86%	−24.63
4	975	243.75	12.1%	−18.32
5	1983	495.75	24.7%	−12.15
6	3999	999.75	49.8%	−6.06
7	8031	2007.75	100%	0

APPLICATIONS

The companding D/A converter is particularly suited for applications requiring a wide dynamic range.

Systems requiring fine control resulting in a constant rate of change or set point controls are economically achieved using these devices.

Instrumentation, Control and μ-Processor based applications include:

- Digital data recording
- PCM telemetry systems
- Servo systems
- Function generation
- Data acquisition systems

Telecommunications applications include:

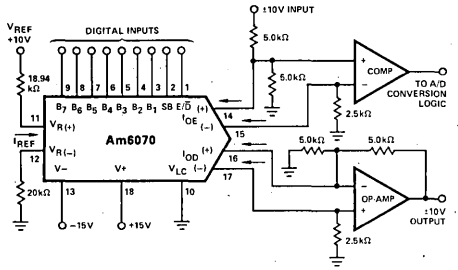
- PCM Codec telephone systems
- Intercom systems
- Military voice communication systems
- Radar systems
- Voice Encryption

Audio Applications:

- Recording
- Multiplexing of analog signals
- Voice synthesis

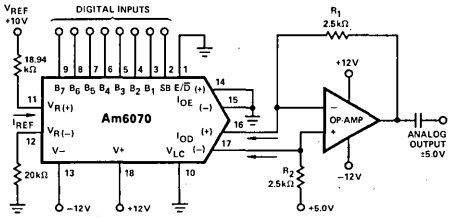
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-251

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



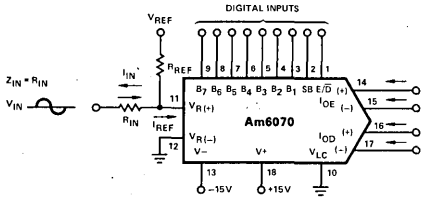
IDEAL VALUES:

I_{REF} = 528μA

I_{FS} = 2007.75μA

LIC-252

LOW INPUT IMPEDANCE CONNECTION

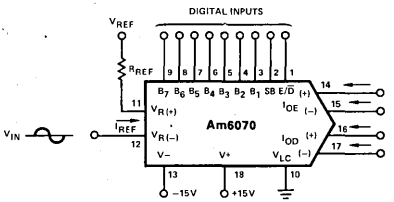


$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

LIC-253

HIGH INPUT IMPEDANCE CONNECTION

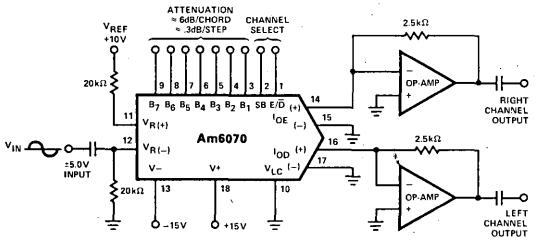


$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

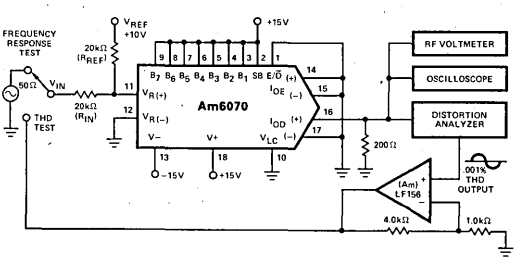
LIC-254

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



LIC-255

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT

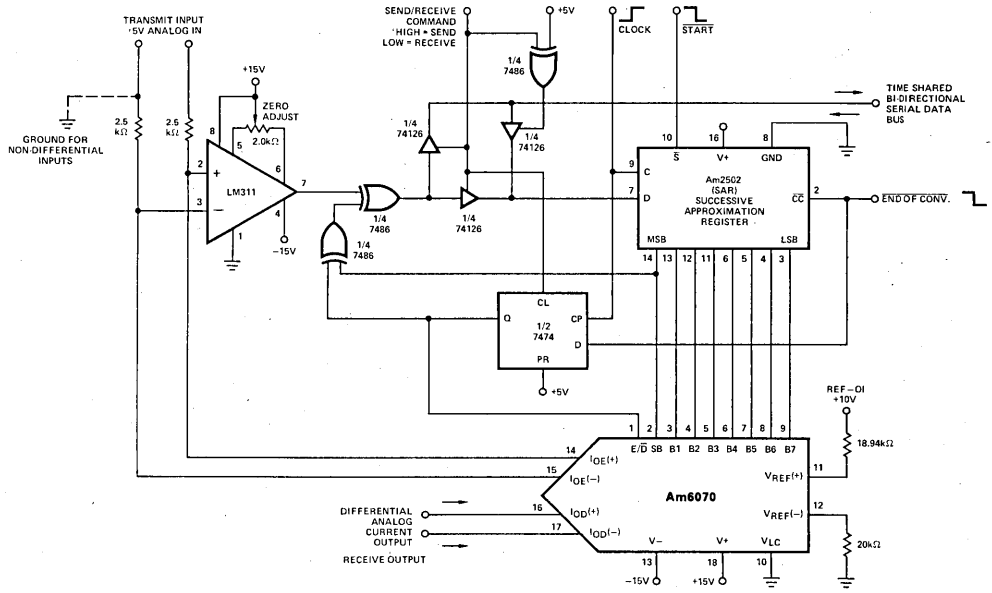


LIC-256

Notes: 4. Low distortion outputs are provided over a 72dB range.

5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

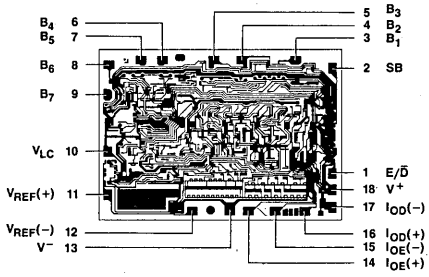
SERIAL DATA TRANSCEIVING CONVERTER
(1/2 OF SYSTEM SHOWN)



LIC-258

Notes:
1. Complementary send/receive commands are required for the two ends.
2. $\overline{\text{START}}$ must be held low for one clock cycle to begin a send or receive cycle.
3. The SAR is used as a serial-in/parallel out register in the receive mode.
4. CLOCK and $\overline{\text{START}}$ may be connected in parallel at both ends.
5. Conversion is completed in 9 clock cycles.
6. Receive output is available for one full clock cycle.

Metallization and Pad Layout



DIE SIZE 0.080" X 0.114"

Am6072

Companding D-to-A Converter for PCM Communication Systems

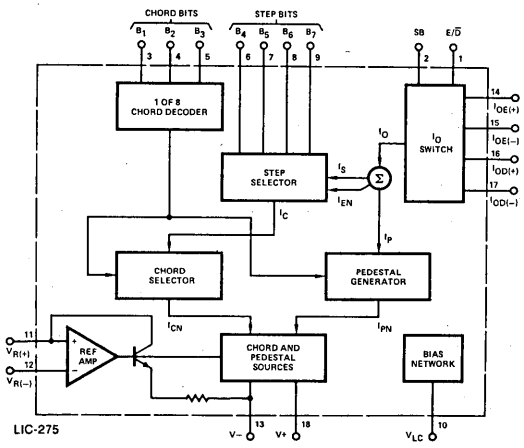
Distinctive Characteristics

- Tested to D3 compandor tracking specification
- Absolute accuracy specified — includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM systems
- Output dynamic range of 72 dB
- Improved pin-for-pin replacement for DAC-86
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

The Am6072 is a monolithic 8-bit, companding digital-to-analog (D/A) data converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6072 complies with the Bell System μ-255 companding law, $Y = 0.18 \ln (1 + \mu x)$, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB), and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this 8-bit format is 72dB. Accuracy and monoticity are assured by the internal circuit design and are guaranteed over the full temperature range. The Am6072 is tested to the Bell D3 channel bank compandor tracking specification for pulse code modulation (PCM) transmission systems. The application of the Am6072 in communication systems provides an increased signal-to-noise ratio, reduces system signal distortion, and stimulates wider usage of computerized channel switching. Other application areas include digital audio recording, voice synthesis, and secure communications. When used in PCM communication systems, the Am6072 functions as a complete PCM decoder with additional encoding capabilities which make it ideal for implementation in CODEC circuits.

FUNCTIONAL BLOCK DIAGRAM



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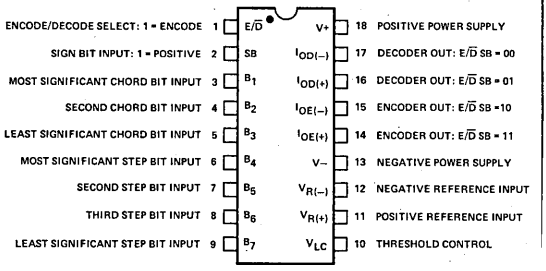
CONNECTION DIAGRAM
Top View
D-18-1



Top View

Pin 1 is marked for orientation.

LIC-276

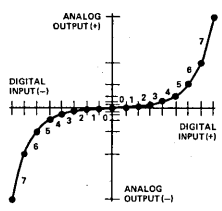
ORDERING INFORMATION*

Part Number	Temperature	Accuracy
Am6072DM	−55°C to +125°C	Conforms to D3 Spec.
Am6072DC	0°C to +70°C	Conforms to D3 Spec.

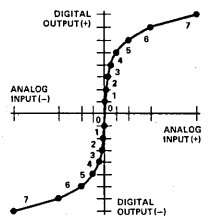
*Also available with burn-in processing. To order add suffix B to part number.

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic



Encoder Characteristic



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MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

3

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, (20 log ($I_{7,15}/I_{0,1}$))

ELECTRICAL CHARACTERISTICS (Note 1)

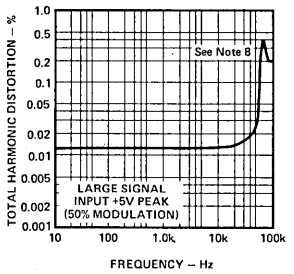
These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 528μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125°C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description		Test Conditions		Min.	Typ.	Max.	Unit
t_s	Settling Time		To within ±1/2 step at T_A = 25°C, Output switched from I_{ZS} to I_{FS}		–	300	500	ns
	Chord Endpoint Accuracy		V_{REF} = +10,000V R_{REF+} = 18.94kΩ R_{REF-} = 20kΩ −5V ≤ V_{OUT} ≤ +18V		See Table 1 for absolute accuracy limits which cover all errors related to the transfer characteristic.			
	Step Nonlinearity							
I_{EN}	Encode Current							
$I_{FS(D)}$ $I_{FS(E)}$	Full Scale Current Deviation from Ideal							
$I_{O(+)}-I_{O(-)}$	Full Scale Current Symmetry Error							
I_{ZS}	Zero Scale Current							
ΔI_{FS}	Full Scale Current Drift							
V_{OC}	Output Voltage Compliance		Output within limits specified by Table 1		−5	–	+18	Volts
I_{DIS}	Disable Current		Leakage of output disabled by E/$\overline{D}$ or SB		–	5.0	50	nA
I_{FSR}	Output Current Range				0	2.0	4.2	mA
V_{IL}	Logic Input Levels	Logic "0"	V_{LC} = 0V		–	–	0.8	Volts
V_{IH}		Logic "1"			2.0	–	–	Volts
I_{IN}	Logic Input Current		V_{IN} = −5V to +18V		–	–	40	μA
V_{IS}	Logic Input Swing		V− = −15V		−5	–	+18	Volts
I_{BREF-}	Reference Bias Current				–	−1.0	−4.0	μA
di/dt	Reference Input Slew Rate				0.12	0.25	–	mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)		V+ = +4.5 to +18V, V− = −15V		–	0.005	0.1	dB
			V− = −10.8V to −18V, V+ = +15V		–	0.01	0.1	
I+ I−	Power Supply Current		V+ = +5V to +15V, V− = −15V, I_{FS} = 2.0mA		–	2.7	4.0	mA
					–	−6.7	−8.8	
P_D	Power Dissipation		V− = −15V, V_{OUT} = 0V I_{FS} = 2.0mA	V+ = +5V	–	114	152	mW
				V+ = +15V	–	141	192	

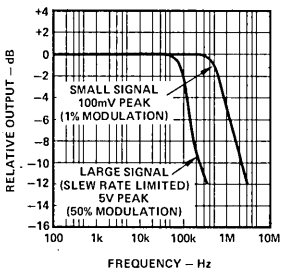
Note 1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) the step size is 0.5μA, while in the last chord near full scale (C_7) the step size is 64μA.

TYPICAL PERFORMANCE CURVES

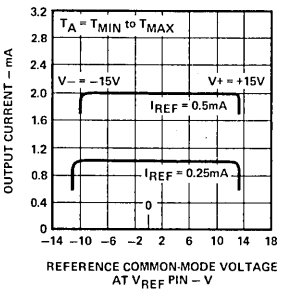
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



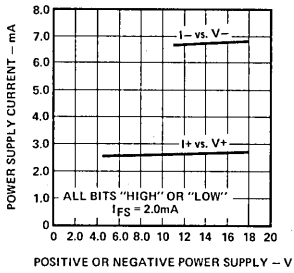
Reference Amplifier Input Frequency Response



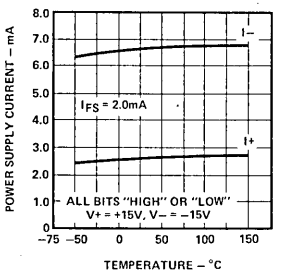
Reference Amplifier Input Common-Mode Range (Note 9)



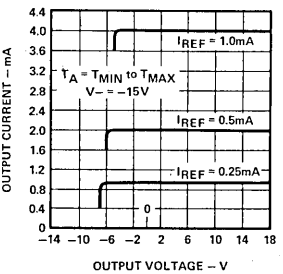
Power Supply Currents Versus Power Supply Voltages



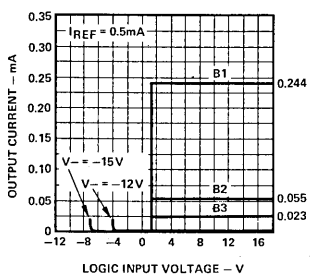
Power Supply Currents Versus Temperature



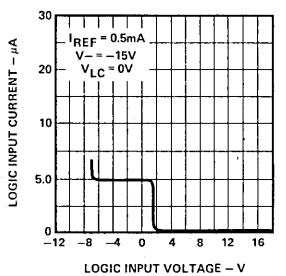
Output Current Versus Output Voltage (Output Voltage Compliance)



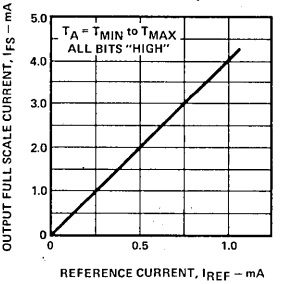
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current



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Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
ABSOLUTE DECODER OUTPUT CURRENT LEVELS IN μA

STEP NO.	CHORD NO. 0	1	2	3	4	5	6	7
0	−.250	7.789	24.048	56.112	120.24	248.49	505.00	1018.02
	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
	.250	8.739	25.473	59.436	127.36	263.22	534.93	1078.34
1	.250	8.733	25.991	59.998	128.01	264.04	536.10	1080.21
	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
	.750	9.798	27.531	63.553	135.60	279.69	567.86	1144.21
2	.750	9.677	27.934	63.885	135.79	279.59	567.19	1142.39
	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
	1.250	10.857	29.590	67.670	143.83	296.15	600.80	1210.08
3	1.250	10.621	29.878	67.771	143.56	295.13	598.28	1204.58
	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
	1.750	11.917	31.648	71.787	152.06	312.62	633.73	1275.95
4	1.750	11.565	31.821	71.658	151.33	310.68	629.37	1266.76
	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
	2.250	12.976	33.706	75.904	160.30	329.09	666.66	1341.82
5	2.250	12.509	33.764	75.544	159.10	326.22	660.46	1328.94
	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
	2.750	14.035	35.765	80.020	168.53	345.55	699.60	1407.69
6	2.750	13.453	35.707	79.431	166.88	341.77	691.56	1391.13
	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
	3.250	15.094	37.823	84.137	176.77	362.02	732.53	1473.56
7	3.250	14.397	37.651	83.317	174.65	357.32	722.65	1453.31
	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
	3.750	16.154	39.882	88.254	185.00	378.49	765.47	1539.43
8	3.750	15.341	39.594	87.204	182.42	372.86	753.74	1515.50
	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
	4.250	17.213	41.940	92.371	193.23	394.96	798.40	1605.30
9	4.248	16.285	41.537	91.090	190.20	388.41	784.83	1577.68
	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
	4.767	18.272	43.998	96.488	201.47	411.42	831.34	1671.16
10	4.720	17.229	43.480	94.977	197.97	403.95	815.92	1639.87
	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
	5.296	19.331	46.057	100.604	209.70	427.89	864.27	1737.03
11	5.192	18.173	45.424	98.863	205.74	419.50	847.02	1702.05
	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
	5.826	19.812	48.115	104.721	217.93	444.36	897.21	1802.90
12	5.664	19.675	47.367	102.750	213.52	435.05	878.11	1764.23
	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
	6.356	20.841	50.174	108.838	226.17	460.82	930.14	1868.77
13	6.136	20.647	49.310	106.636	221.29	450.59	909.20	1826.42
	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
	6.885	21.871	52.232	112.955	234.40	477.29	963.07	1934.64
14	6.608	21.619	51.253	110.523	229.06	466.14	940.29	1888.60
	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
	7.415	22.900	54.290	117.072	242.63	493.76	996.01	2000.51
15	7.080	22.590	53.197	114.409	236.83	481.68	971.39	1950.79
	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
	7.944	23.929	56.349	121.188	250.87	510.23	1028.94	2066.38
STEP SIZE	.5	1	2	4	8	16	32	64

Minimum, ideal and maximum values are specified for each step. The minimum and maximum values are specified to comply with the Bell D3 compandor tracking requirements. All four outputs are guaranteed, the encode outputs being specified to limits a half step higher than those shown above. This takes into account the combined effects of chord endpoint accuracy, step nonlinearity, encode current error, full scale current deviation from ideal, full scale symmetry error, zero scale current, full scale drift, and output impedance over the specified output voltage compliance range. Note that the guaranteed monotonicity ensures that adjacent step current levels will not overlap as might otherwise be implied from the minimum and maximum values shown in the above table.

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

CHORD / STEP	0	1	2	3	4	5	6	7
0	–	−44.73	−35.18	−27.82	−21.20	−14.90	−8.74	−2.65
1	−69.07	−43.73	−34.51	−27.24	−20.66	−14.37	−8.22	−2.13
2	−63.05	−42.84	−33.88	−26.70	−20.15	−13.87	−7.73	−1.65
3	−59.53	−42.03	−33.30	−26.18	−19.66	−13.40	−7.27	−1.19
4	−57.03	−41.29	−32.75	−25.70	−19.21	−12.96	−6.83	−0.75
5	−55.10	−40.61	−32.24	−25.24	−18.77	−12.53	−6.41	−0.33
6	−53.51	−39.98	−31.75	−24.80	−18.36	−12.13	−6.01	+0.06
7	−52.17	−39.39	−31.29	−24.39	−17.96	−11.74	−5.63	+0.44
8	−51.01	−38.84	−30.85	−23.99	−17.58	−11.37	−5.26	+0.81
9	−49.99	−38.32	−30.44	−23.61	−17.22	−11.02	−4.91	+1.16
10	−49.07	−37.83	−30.04	−23.25	−16.87	−10.68	−4.57	+1.49
11	−48.25	−37.37	−29.66	−22.90	−16.54	−10.35	−4.25	+1.82
12	−47.49	−36.93	−29.29	−22.57	−16.22	−10.03	−3.93	+2.13
13	−46.80	−36.51	−28.95	−22.25	−15.91	−9.73	−3.63	+2.43
14	−46.15	−36.11	−28.61	−21.94	−15.61	−9.43	−3.34	+2.72
15	−45.55	−35.73	−28.29	−21.63	−15.32	−9.15	−3.06	+3.00

The −37 dBmo and −50 dBmo output points significant for the Bell D3 system specification can be found between steps 11 and 12 on chord 1, and steps 8 and 9 on chord 0, respectively. Outputs corresponding to points below −50dB are specified in Table 1 for an accuracy of ± a half step.

THEORY OF OPERATION

Functional Description

The Am6072 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/$\overline{D}$), input signal. A logic 1 applied to the E/$\overline{D}$ input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/$\overline{D}$ input places the Am6072 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ-225 logarithmic law which can be written as follows:

$$Y = 0.18 \ell n (1 + \mu |X|) \operatorname{sgn}(X)$$

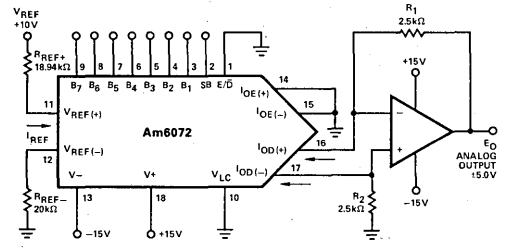
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
μ = 255

The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/$\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 0.5μA found in the first chord near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6072 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/$\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/$\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,



$I_{REF} = V_{REF}/R_{REF}$

IDEAL VALUES: $I_{REF} = 528\mu A$, $I_{FS} = 2007.75\mu A$

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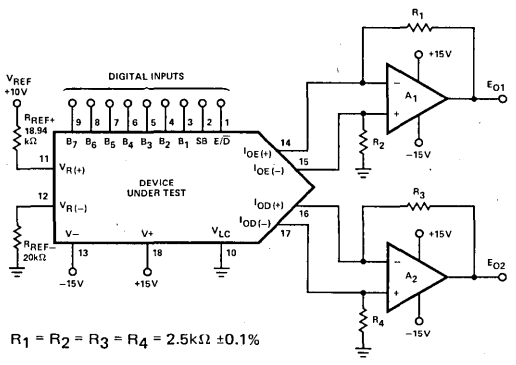
	E/$\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	–5.019V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

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LINE SELECTION TABLE

TEST GROUP	E/$\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE(+)}$	(E_{O1}/R_1)
2	1	0	$I_{OE(-)}$	(E_{O1}/R_2)
3	0	1	$I_{OD(+)}$	(E_{O2}/R_3)
4	0	0	$I_{OD(-)}$	(E_{O2}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.25μA, which will bring the ideal encode current value for step 0 on chord 0 to $\pm$0.25μA with respect to the corresponding decode current value of 0.0μA. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6072 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\overline{S}$, and Conversion Complete, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6072. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6072.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6072 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

3

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6072 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6072. The resulting operational amplifier's output in Figure 2 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6072 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

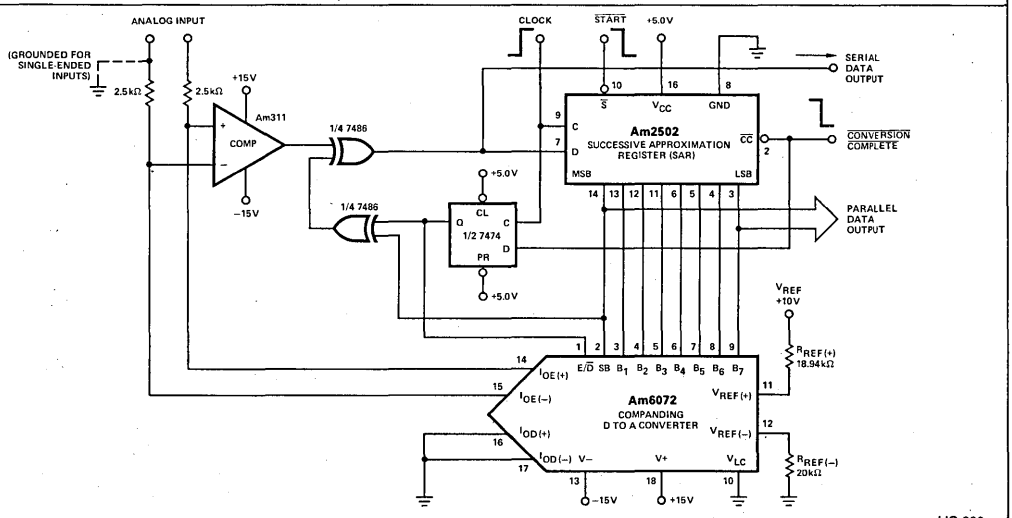

Figure 3. Detailed Encoder Connections.

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2.5kΩ, also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528μA. The corresponding ideal full scale decode and encode current values are 2007.75μA and 2039.75μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current I_{REF} = 528μA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6072 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 528μA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + (2 \bullet I_{REF} \bullet 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

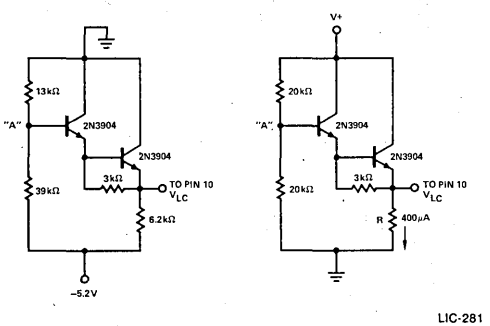
Negative Output Voltage Compliance $V_{OC(-)}$

V− \ I_{REF} (I_{FS})	264μA (1mA)	528μA (2mA)	1056μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6072 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

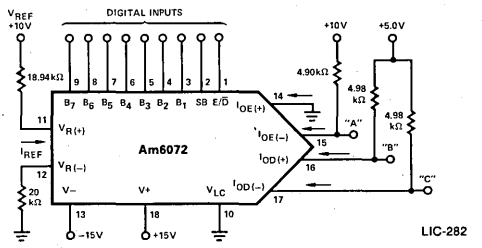
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.



INPUT CODE (E/D̄, SB, B1, . . ., B7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.02	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections.

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Step (S) \ Chord (C)		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:

$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$

where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:

$I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}$ (μA)

where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Decoder Step Size Summary

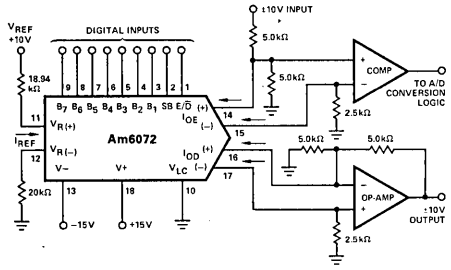
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 5
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	–48.55
1	93	23.25	1.16%	–38.73
2	219	54.75	2.73%	–31.29
3	471	117.75	5.86%	–24.63
4	975	243.75	12.1%	–18.32
5	1983	495.75	24.7%	–12.15
6	3999	999.75	49.8%	–6.06
7	8031	2007.75	100%	0

BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



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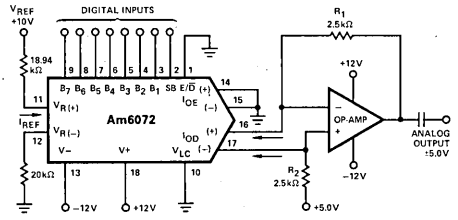
COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



IDEAL VALUES:

$I_{REF} = 528\mu A$

$I_{FS} = 2007.75\mu A$

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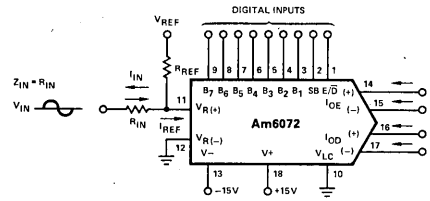
LOW INPUT IMPEDANCE CONNECTION



$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

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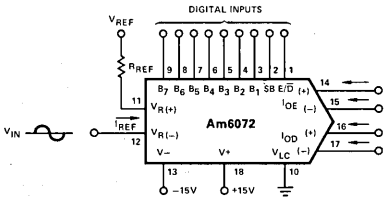
HIGH INPUT IMPEDANCE CONNECTION



$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

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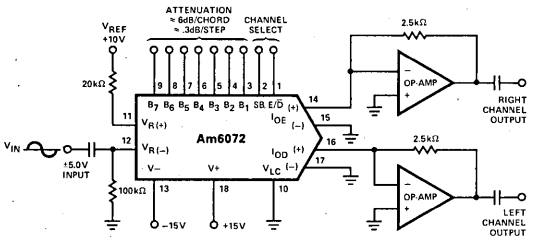
LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



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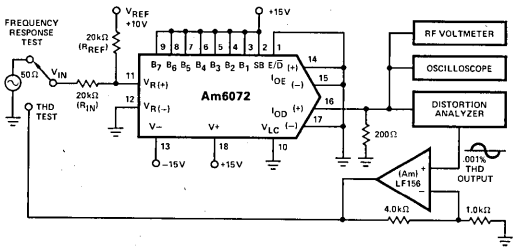
REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



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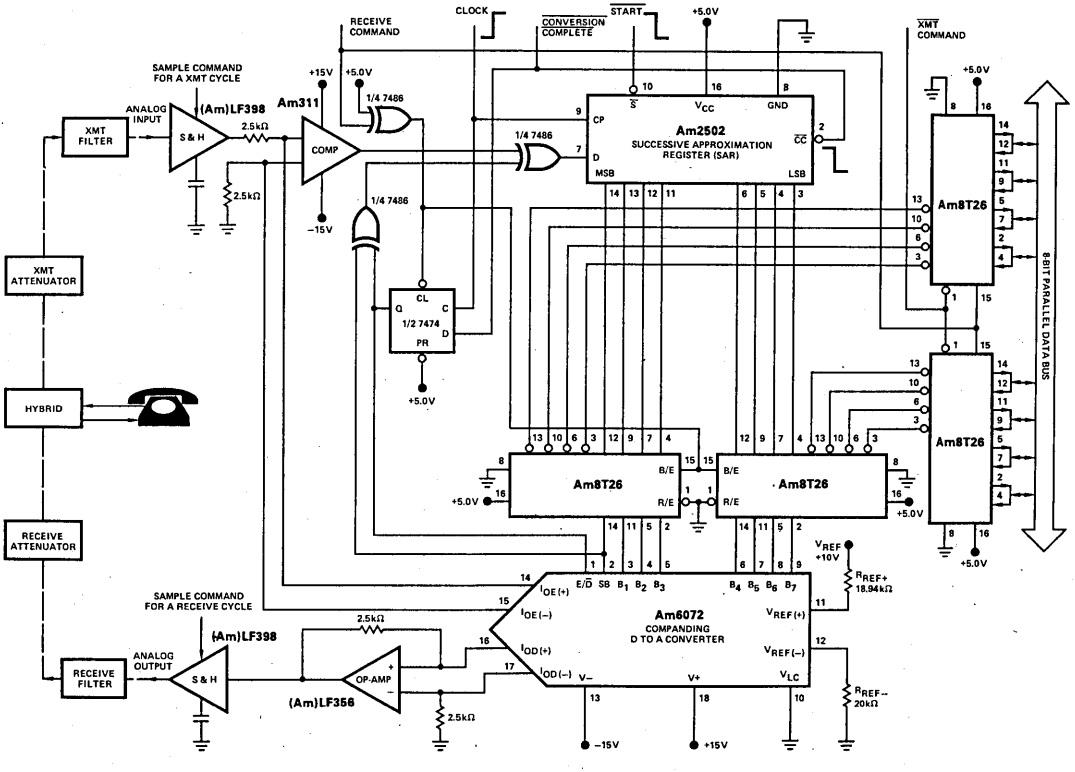
Notes: 4. Low distortion outputs are provided over a 72dB range.
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TIME SHARED CONVERTER CONNECTIONS

SINGLE CHANNEL PCM CODEC – PARALLEL DATA I/O



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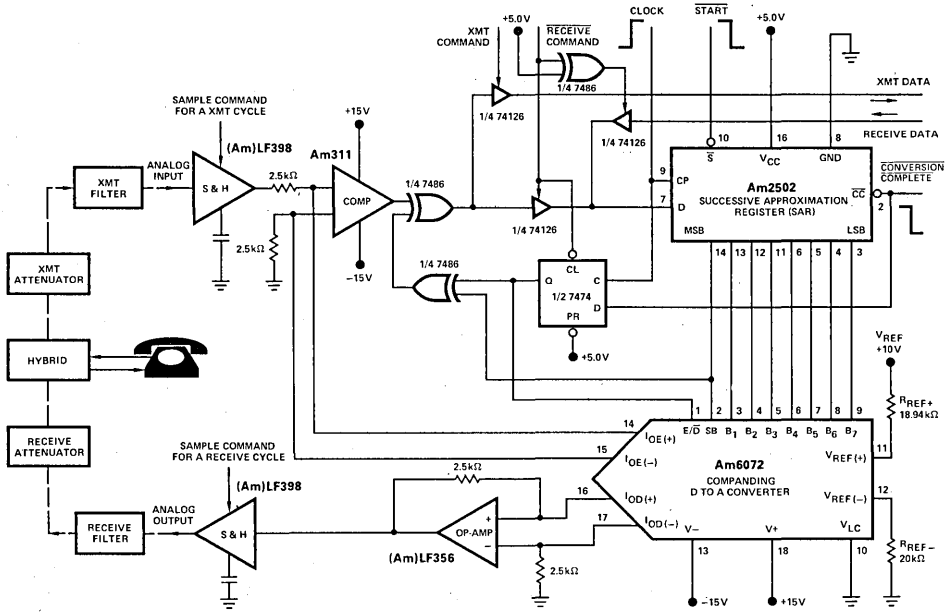
APPLICATION INFORMATION

1. To perform a transmit operation cycle the $\overline{\text{START}}$ pulse must be held low for one clock cycle; the receive operation is performed without the successive approximation register, SAR.
2. $\overline{\text{XMT}}$ and RECEIVE command signals are mutually exclusive.
3. Duration of the RECEIVE command signal must accommodate the Am6072 settling time plus the sampling time required by the sample and hold, (S & H), circuit used at the CODEC's analog output. The receiving data must not change during this time.
4. A $\overline{\text{XMT}}$ command signal must be issued after a high-to-low transition of the CONVERSION COMPLETE, $\overline{\text{CC}}$, signal. Its duration depends on the time required by the digital time division switch circuitry to sample the 8-bit parallel transmit data bus.
5. Data conversion for a transmit operation is completed in 9 clock cycles because the SAR must be initialized before every new conversion. Data conversion for a receive operation corresponds to the Am6072 settling time; the receiving and transmit data transfers can be done simultaneously by employing separate transmit and receive data buses and utilizing data storage devices for the receive data.
6. A sample command pulse for a transmit operation can coincide with the $\overline{\text{START}}$ pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input.
7. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Am6072 settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.

TIME SHARED CONVERTER CONNECTIONS (Cont.)

SINGLE CHANNEL PCM CODEC – SERIAL DATA I/O



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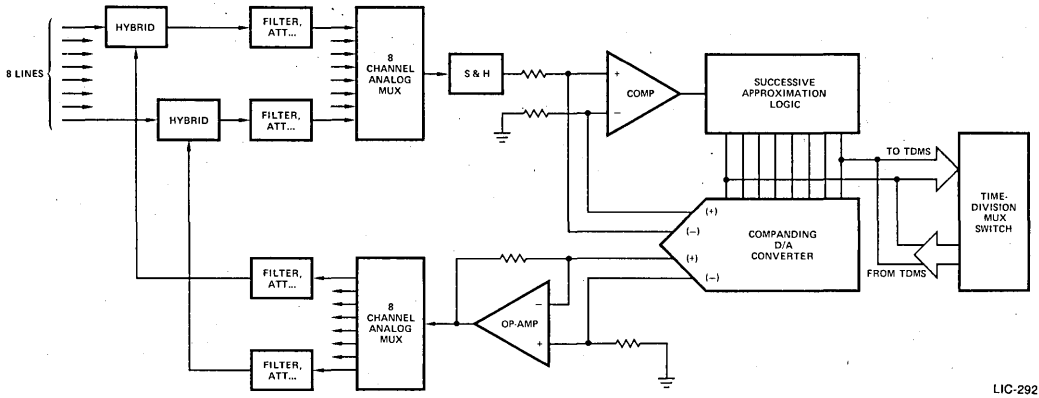
APPLICATION INFORMATION

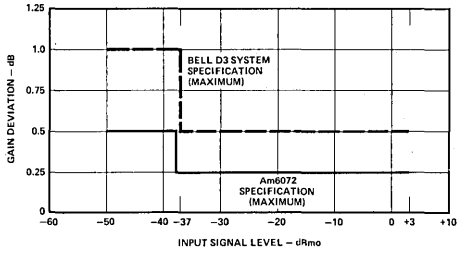
1. Before beginning either a transmit or a receive operation, the START signal must be held low for one complete clock cycle.
2. XMT and RECEIVE command signals are mutually exclusive. Their durations must accommodate the time required for conversion of an outgoing or an incoming series of 8 digital bits, respectively.
3. Data conversion for either operation, transmit or receive, is completed in 9 clock cycles.
4. During the receive cycle the successive approximation register, SAR, is acting as a serial-in to parallel-out shift register, with data supplied from data storage devices.
5. A sample command pulse for a transmit cycle must be issued before a XMT command signal; its duration depends on the sample and hold, S & H, circuit used.
6. A sample command pulse for a receive cycle must be delayed by a time equal to the Am6072 settling time after a high-to-low transition of the CONVERSION COMPLETE, CC, signal occurs.

8 LINE CODEC TDM PCM/PABX SYSTEM – BLOCK DIAGRAM



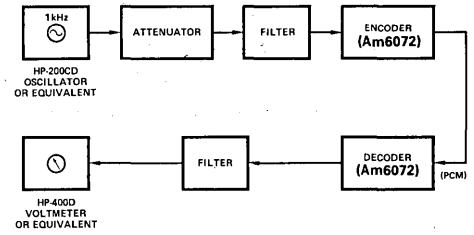
LIC-292

COMPANDOR TRACKING SPECIFICATION



LIC-293

COMPANDOR TRACKING TEST BLOCK DIAGRAM



LIC-294

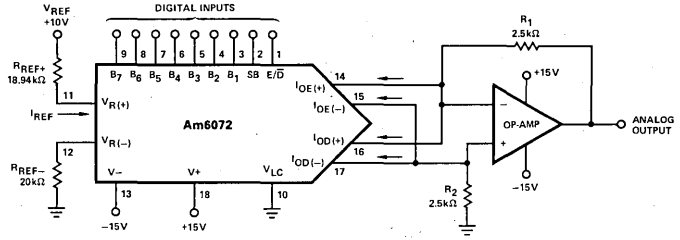
3

D3 NOISE AND DISTORTION SPECIFICATION

The Am6072 has a negligible idle channel noise contribution. Signal-to-quantizing-distortion ratio, (S/D), is guaranteed to exceed the minimum values specified for D3 channels as follows:

Input Level 1020 Hz Sinewave	S/D, C-Message Weighting
0 to –30 dBmo	33 dB
At –40 dBmo	27 dB
At –45 dBmo	22 dB

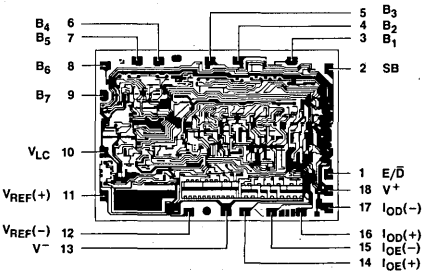
DECODER OPERATION DURING SIGNALLING FRAME



LIC-295

The Am6072 can perform the decoding function in a D3 channel bank system. During signalling frames the least significant bit, B7, of each 8-bit word is used for signalling messages and only seven bits are used for sample coding. In order to minimize the quantizing error during these signalling frames, the Am6072 output is increased by a half step from its corresponding decode output value by switching the E/$\overline{D}$ input from a logic level 0 to a logic 1.

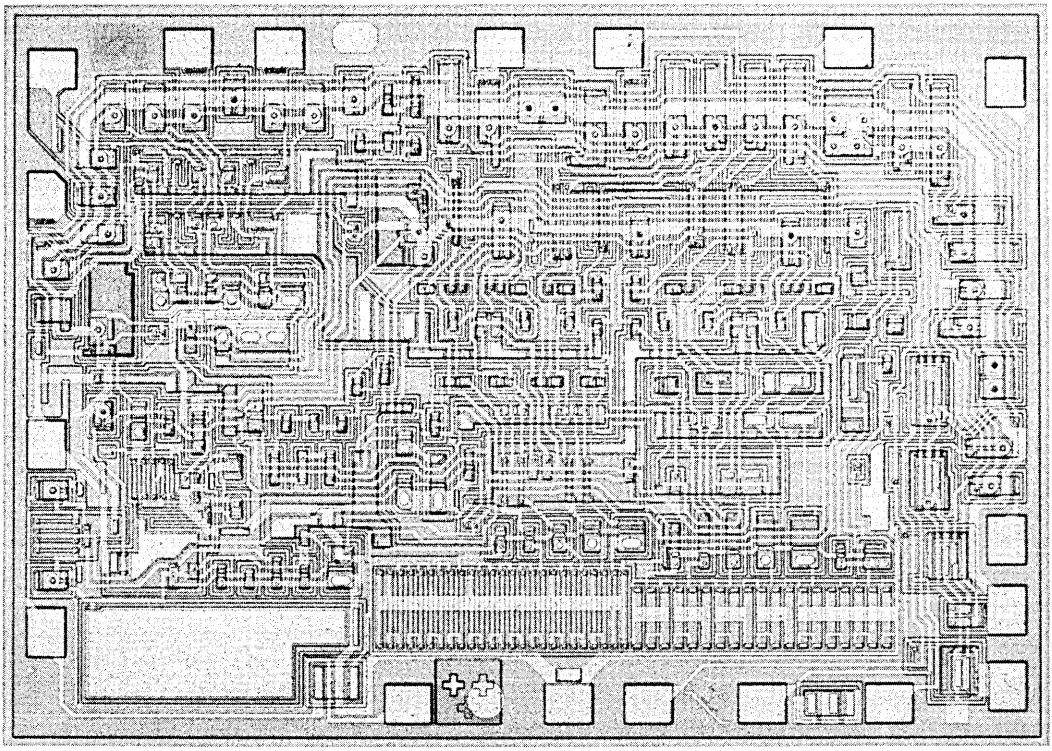
Metallization and Pad Layout



DIE SIZE: 0.080" X 0.114"

Data Conversion with Companding DAC Devices

By Dragan Milojkovic



Am6071 and Am6073 are discontinued devices. References to these devices, and to the A-Law companding curves are supplied for reference only.

INTRODUCTION

Modern electronic systems are replacing many of the analog signal processing and transmission functions with digital data processing. The use of digital electronics can lead to improvements in system cost, performance, accuracy and reliability. Digital systems can transmit many signals on the same line in a multiplexed mode and do not suffer from the same kinds of noise and crosstalk problems that are inherent in analog systems. The digital processing of analog information requires conversion of the analog signal into digital form and the reverse conversion of the digital result back into an analog signal. Analog to digital converters, (ADC), and digital to analog converters, (DAC), perform these functions. The DAC is the key circuit element in both of these processes since it is used in a feedback loop to generate the ADC function. Monolithic technology has advanced dramatically in the last few years making low cost 8-bit DACs a reality today; in the near future, 10 and 12-bit monolithic DACs will also become available. This trend in DAC technology will help accelerate the trend toward more digital processing and transmission of analog information.

Many analog signals vary in amplitude from very small values to very large values. The dynamic range of a converter is a measure of its ability to handle a wide range of input amplitudes and is defined as the ratio of the largest resolvable signal (V_{IN} max.) to the smallest signal (V_{IN} min.) that can be handled. This ratio is often expressed in decibels using the conversion formula 20 log (V_{IN}max/V_{IN}min). Linear DACs resolve a ratio of 2^n:1, (n equals the number of bits), or n • 6dB. An 8-bit linear DAC, for example, resolves a ratio of 256:1 or 48dB.

The accuracy of a converter is a prime concern in most applications. Accuracy is generally specified with respect to the full scale output (as a percent of full scale) or to the smallest step size (i.e., ±1/2LSB refers to ±1/2 of the smallest step size). Linear converters tend to be more accurate as the number of steps increases because the step size decreases. Many systems require high accuracy as a percent of the input signal level rather than as a percent of full scale. The accuracy as a percent of input signal level (reading) decreases as the signal level decreases because the amount of error is constant. An 8-bit linear DAC with an accuracy of .2% of full scale (±1/2 LSB) has an accuracy of .2% of reading for input signals near full scale, but an accuracy of only 20% of reading for an input near 1% of full scale.

For many types of applications, the accuracy and dynamic range of an 8-bit linear DAC are sufficient. However, there are many classes of problems that require a wider dynamic range to handle signal ratios of several thousand to one. Voice processing, speed control and music synthesis fall into this category. A 12-bit linear DAC provides a wider dynamic range, 72dB, and higher accuracy than an 8-bit linear DAC. However, these devices are very expensive, and, furthermore, it turns out that while most applications require the dynamic range of the 12-bit linear DAC they do not require its accuracy. A nonlinear DAC can provide such performance with fewer digital bits. It does so by using a nonlinear transfer characteristic to compress an analog signal into a digital word, and a complementary transfer characteristic to expand the digital values into analog signals with a wide dynamic range.

An 8-bit nonlinear DAC can achieve a 72dB dynamic range with accuracy expressed as a percent of reading that ranges from 1.6% to 3.2% over the entire dynamic range of the device. The overall nonlinear analog to digital and digital to analog conversion procedure is called the companding process. This note will discuss the Am6070 family of Companding DACs and their applications.

Companding Principles

Companding transfer functions were originally developed to satisfy the requirements of telephone voice communication systems. Studies of speech signals have shown that the distribution of amplitudes covers a range of several thousand to one and that the lower amplitude signals occur more often than the large amplitude signals. More attention should, therefore, be paid to the low level signals. It is important to maintain a better signal to distortion ratio (the ratio of signal level to conversion error) for low level signals at the expense of a poorer ratio for the less probable high level signals. In order to accomplish this goal, a logarithmic type of transfer characteristic is used with more steps at low levels and fewer steps at high levels.

A true logarithmic function has a discontinuity at zero and thus cannot be used directly for signal compression. A modified transfer characteristic with the form "log (1+x)" can be used to smooth the characteristic near zero. Two popular schemes have been developed – the μ-law by the Bell system for use in U.S. telephone systems and the A-law by the CCITT for use in European systems. They can be described by the following mathematical equations:

μ-Law: $Y = 0.18 \ln(1+\mu|X|) \operatorname{sgn}(X)$

A-Law: $Y = 0.18 (1 + \ln(A|X|)) \operatorname{sgn}(X), \quad 1/A \leq |X| \leq 1$

$Y = 0.18 (A|X|) \operatorname{sgn}(X), \quad 0 \leq |X| \leq 1/A$

where: X = analog signal level normalized to unity (encoder input or decoder output)

Y = digital signal level normalized to unity (encoder output or decoder input)

μ = 255 and A = 87.6

Both functions require that the size of the analog output change increase for each increasing digital code. In order to implement such a function, an overly complex analog circuit would be needed. This requirement is met, instead, by a piecewise linear approximation. In this approximation, an 8-bit digital word generates 256 analog outputs with a transfer characteristic which is symmetrical about the origin. Figure 1 shows the μ-law and A-law transfer characteristics and the linear 8-bit DAC transfer characteristic. The positive 128 steps are divided into 8 segments or chords of 16 steps each, from step 0 to step 15. The step size is constant within a chord and doubles for each increasing chord. If the step size in the first chord, chord 0, is assigned a value of 1, the next chord, chord 1, has a step size of 2, chord 2 has a step size of 4, etc. The last chord has a step size of 128 units and ends roughly at the value 4000. The 128 steps represent a 7-bit digital word with a dynamic range of 72dB, 20 log (4000:1), which is equivalent to the dynamic range of a 12-bit linear DAC.

The above description describes the μ-law curve. The A-law differs from the μ-law only in the first two chords. The step size in the A-law DAC does not change between the first and second chords, but doubles in all succeeding chords. The A-law DAC has a 1/2 step offset at zero so that the positive and negative zero codes do not generate the same point. The A-law DAC has a dynamic range of 62dB which is equivalent to an 11-bit linear DAC.

Companding DAC

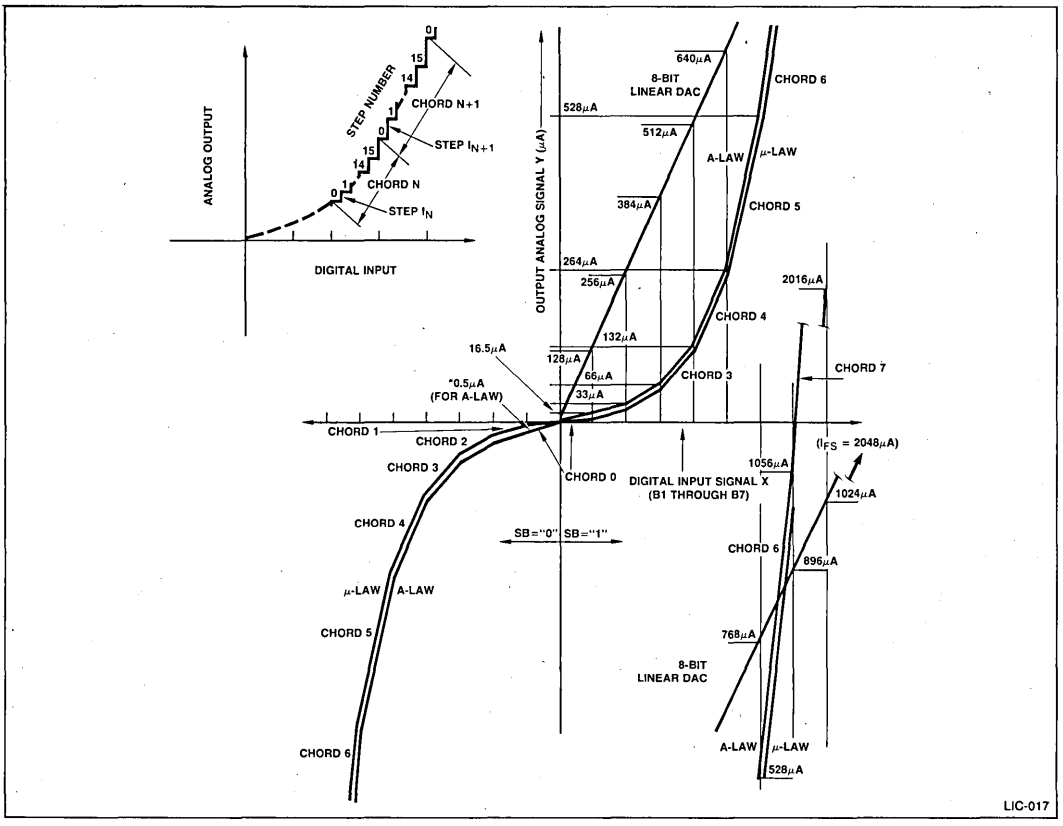


Fig. 1. Transfer Functions for μ-Law and A-Law Decoders.

Analog to Digital Conversion Using DACs

A digital input word to a DAC corresponds to an exact and unique analog output level. The total number of discrete output levels, m, depends on the number of DAC binary inputs, ($m=2^n$, n = number of input bits), and each output level is specified to be within a certain error band of its ideal value. An analog input to an ADC, on the other hand, may have an infinite number of signal levels which must be represented with only a finite number of digital output combinations. The output code, ideally, identifies the digital word that most closely represents the analog input. The classical way to generate a fast ADC function is to use a DAC in a feedback loop together with special ADC logic, employing a comparator and a successive approximation register (SAR). The feedback loop compares the DAC output with the analog input and decides whether the digital code is greater than or less than the input to the DAC. The input to the DAC is then increased or decreased accordingly, and another comparison is made. This technique causes each bit to be changed one at a time, and, by comparing the DAC's output with the analog input, the value of that bit is determined. Modification of one bit at a time, starting with the most significant bit and ending with the least significant bit, leads to an output which with each successive bit becomes a closer approximation of the input level. A total of n comparisons are needed for an n-bit converter.

The overall transfer characteristic of the entire ADC system is shown in Figure 2a. The ADC logic approximates the input analog signal by rounding off to the closest lower digital value. The maximum uncertainty in the digital representation of the analog input will be a full bit. In order to reduce this uncertainty, the ADC transfer curve can be modified to round to the nearest digital code, instead of the lowest, by adding a half step offset to the characteristic as shown in Figure 2b. The ADC now changes its outputs for analog inputs halfway between digital code points and gives a reading with ±1/2 step uncertainty. The half step offset necessary for better ADC accuracy is easily provided by increasing the DAC's analog output level by a half step whenever the DAC is used in an ADC scheme. This additional half step is easy to generate with linear DACs because of their constant step size throughout the entire dynamic range. For a Companding DAC this addition is much more difficult since the step size varies with signal value. In order to alleviate this problem, the Companding DAC has a built in capability to produce an appropriate half step offset signal at its output by a logic command. When this command input ($E/\overline{D}$ pin) is at logic 0, the Companding DAC is in the decode mode and the output will not contain the half step offset current. When the command input is at logic 1, the DAC is in the encode mode, i.e., within an ADC scheme, and the output current is increased by the correct half step for any input mode.

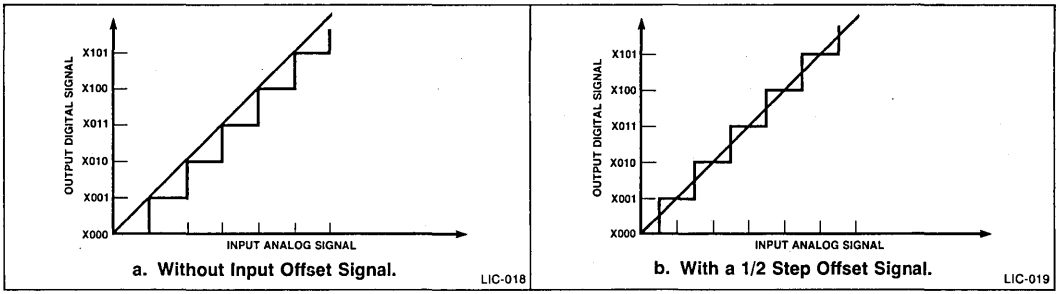


Fig. 2. Transfer Characteristic of an A to D Conversion System.

Companding DACs in Industrial Systems

Companding DACs differ from linear DACs in output dynamic range, transfer function, and the size of intermediate output steps. Comparable 8-bit linear DACs, such as the popular AmDAC-08, have a linear transfer characteristic with 256 linear steps, where each step is 8μA in size. The AmDAC-08 has a dynamic range of only 48dB while the 8-bit Companding DAC, (Am6070), has an output dynamic range of 72dB, which is also achievable with a 12-bit linear DAC. The output current increments of the Companding DAC, corresponding to small output signals, are significantly smaller than 8μA, which is the step size for the AmDAC-08. The step sizes in the first four chords of the Companding DAC transfer function are 0.5μA, 1.0μA, 2.0μA, and 4.0μA, respectively, with a total of 64 steps and a current value at the end of the fourth chord of approximately 100μA. By comparison, the AmDAC-08 uses only 12 uniform steps to resolve a 100μA output current level.

Given the assumption that most industrial systems employ an 8-bit digital data bus, the 8-bit DAC is a logical choice for interfacing with these systems. Companding DACs can be used in the same general applications as the AmDAC-08, particularly for reconstruction of analog signals with dynamic ranges that exceed 48dB. One example is the measurement of gas or liquid pressure, in an industrial environment, by pressure transducers with a pressure range of 0 to 3000PSI. Another example is digital recording of sound signals which usually exhibit a very large dynamic range.

The Companding DAC's logarithmic-like nonlinear transfer function suggests the application of this device for simulation of nonlinear waveforms which can be generated by converting a sequence of bytes, from an 8-bit processor, into an analog signal with an exponential shape. This type of signal can be used in nonlinear control systems such as motor velocity controllers. Additionally, the high resolution and accuracy of the Companding DAC transfer function, for small output signal levels, provide a very smooth and precise analog control signal to devices whose outputs are voltage or current dependent.

In general, the Companding DAC should be used in any system where a large dynamic range is needed. Such systems include servo motor controls, electromechanical positioning, voice and music synthesis and recording, secure communications, log sweep generators, digital control of gain and attenuation, and microprocessor controlled signal generation.

Companding DACs in PCM Transmission Systems

The companding laws were developed to satisfy the requirements of the telephone system for the digital transmission of voice signals. Voice signals exhibit a dynamic range of several thousand to one. To transmit this information with 8-bit words and retain reasonable accuracy at low levels, a companding transfer characteristic must be used to compress the analog signal prior to transmission and to restore the original signal after reception. The transmission of an analog signal in a digital format involves sampling, quantizing (A to D conversion), and compressing the analog signal as shown in Figure 3. The receiver must perform the complementary functions of expansion, digital to analog conversion and filtering to restore the analog signal waveform. The entire procedure is known as pulse code modulation, (PCM), and is the prevalent technique for digital transmission in communication systems. Currently, the Bell μ-law is the standard in the United States and the CCITT A-law is the standard in Europe.

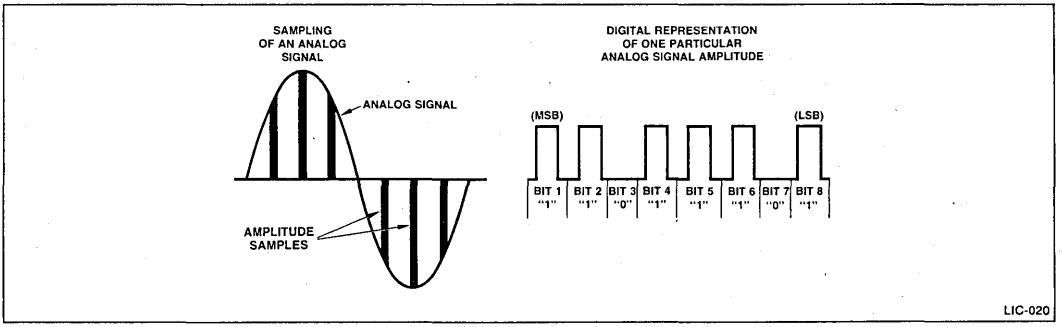


Fig. 3. Pulse Code Modulation Example.

Companding DAC

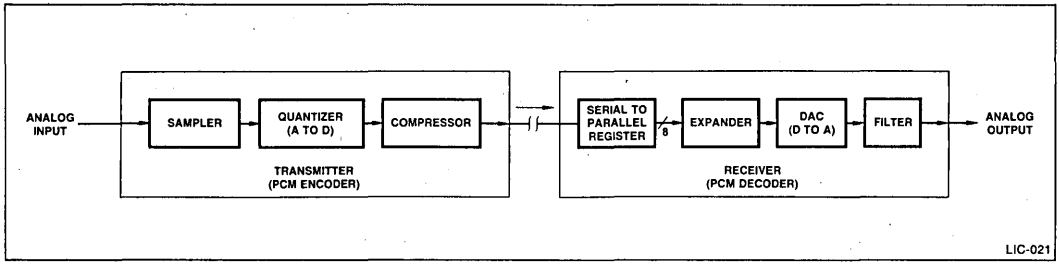


Fig. 4 One-Way PCM Transmission System Block Diagram.

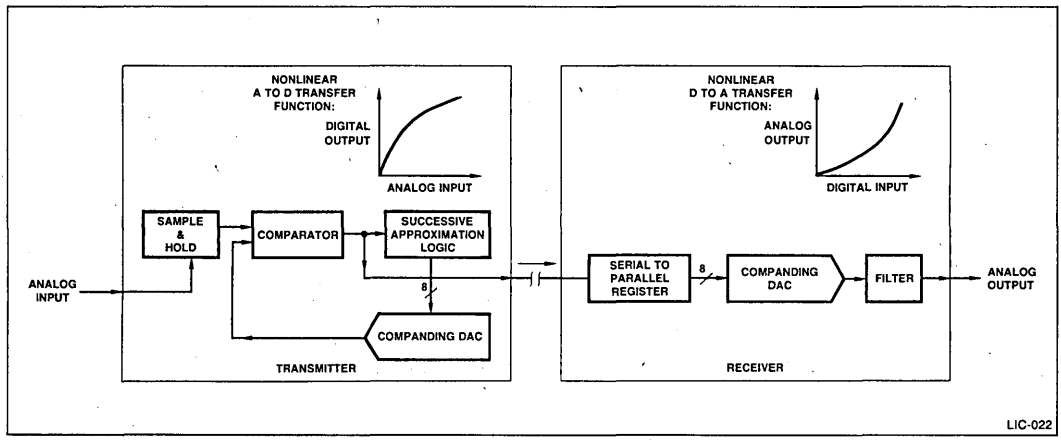


Fig. 5. One-Way PCM Transmission System Implemented with Companding DAC.

A simplified block diagram of a PCM transmission system is shown in Figure 4. The analog signal must be sampled at a rate that is at least twice as fast as the maximum bandwidth of the system, (3.4KHz), in order to achieve satisfactory signal reproduction at the receiver site. (This requirement is based on the Nyquist sampling theorem.) The telephone system uses a sampling rate of 8kHz which allows 125μs between samples. During this time the entire signal sampling, quantizing, encoding, and multiplexing must be completed.

The companding DAC is a complete PCM decoder (receiver) that performs both the decoding and D/A conversion. The DAC has additional encoding capabilities which make it very attractive for use in CODECs (a CODEC is both an Encoder and Decoder). The transfer characteristics of this device closely follow the characteristics defined by the μ-law, (Am6072). A typical connection of a Companding DAC in a PCM transmission system is shown in Figure 5. In the transmitter side, the Companding DAC operates in a feedback loop using an SAR to perform the data encoding function. The corresponding logarithmic transfer curve for the entire feedback loop portion of the transmitter is also shown in Figure 5. The value of the sampled signal is estimated by a series of 9 iterations until its appropriate quantized digital representation appears at the 8-bit parallel data output of the SAR. This 8-bit digital code will be transmitted to the digital inputs of another Companding DAC for the decoding operation. The input/output transfer function for the Companding DAC is also shown in Figure 5.

The Companding DAC can be used in PCM decoders, encoders or complete CODECs. It is a high speed device that is capable of handling more than one channel in a multiplexed system. In multi-channel systems Companding DACs can be configured in a variety of ways depending on the number of channels, the method of transmission, (serial or parallel data), and synchronization of the system. A single Companding DAC can be used, for example, to decode all 24 channels in a standard Bell D3 data bank.

COMPANDING DAC CIRCUIT DESCRIPTION

General Circuit Description

The basic function of the 8-bit, Companding DAC is to convert a digital input value into an analog output current. The output current is a function of the digital data inputs and the input reference current. The full scale current, I_{FS}, is generated by the 7-bit data input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, Encode and Decode, which are controlled by the Encode/Decode, ($E/\overline{D}$), digital control signal. The output dynamic ranges achieved with the sign-plus-7-bit Companding DACs are 62dB (A-law) and 72dB (μ-law) which correspond to the output dynamic ranges of sign-plus-11-bit and sign-plus-12-bit linear binary DACs. Digital data and control inputs provide for easy digital control of converter operations in computer based data conversion systems.

The internal device design assures the accuracy and monotonicity of the Companding DAC over the entire dynamic and temperature ranges by maintaining the chord end points and step size deviations within allowable limits. Parametric deviations and requirements can be expressed in terms of corresponding step fractions which are applied throughout the entire output dynamic range. In industrial environments it is customary to specify allowable deviations from ideal parametric values within ± half a step. However, the μ-law and A-law based PCM communication systems specify the output current deviations in terms of dB, with respect to I_{FS}. Furthermore, these communication requirements in dB cannot be translated to some reasonable "step fraction" deviation which will be common for the entire output dynamic range. Consequently, Companding DACs applied in communication systems must be tested against specific output current values which are calculated separately for each step of the transfer characteristic. This difference between communication and industrial Companding DAC devices is recognized by Advanced Micro Devices which offers μ-law devices for both the industrial market, Am6070 and the telecommunication market, Am6072.

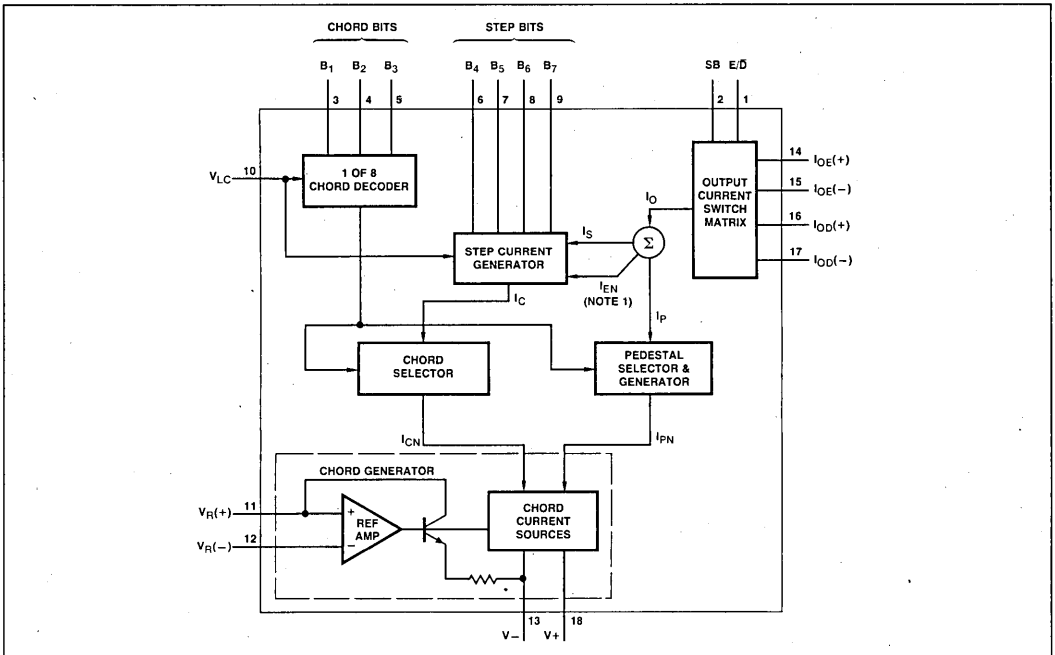
These Companding DACs are manufactured in an 18-pin package. There are seven digital data inputs, (B1 through B7), two control digital input signals, (SB, E/$\overline{D}$), and four analog current outputs, ($I_{OD(+)}$, $I_{OD(-)}$, $I_{OE(+)}$, $I_{OE(-)}$). The maximum output current value or full scale current, I_{FS}, is determined by the value of the reference current, I_{REF}, supplied to the Companding DAC via two analog reference inputs, ($V_{R(+)}$ and $V_{R(-)}$). There are three power supply connections (V−, V+ and Ground).

Detailed Circuit Description

The block diagram of the Companding DAC is shown in Figure 6. The circuit consists of the following five major blocks:

- The chord generator produces the total current for each chord or segment of the curve.
- The pedestal generator generates the pedestal or starting point for each chord.
- The step generator generates the proper step current for each chord.
- The chord decoding logic decodes the chord inputs and controls the inputs to the pedestal and step generator circuits.
- The output switching matrix sums the step and pedestal currents and routes them to the proper output node.

To understand the circuitry of the Companding DAC it is important to understand how the companding curve is generated. The companding curve is a piecewise linear approximation of an exponential characteristic. It consists of 16 linear segments centered around the origin. The curve is symmetrical around the origin so we need only examine the positive portion of the curve. Each segment or chord consists of sixteen steps, step 0 through step 15, and the size of each step doubles as the chord number increases. In order to smooth out the characteristic as the chords change, the step current value for the first step of each higher chord, step 0, is set to be 1 1/2 times larger than the step current values in the lower chord. The succeeding fifteen steps, step 1 to step 15, are 2 times larger than steps of the previous chord. Figure 7 shows a detailed synthesis of the companding function. The first



Note 1: I_{EN} contributes to I_O only in the encode mode specified by E/$\overline{D}$ = "1".

LIC-023

Fig. 6. Companding DAC Functional Block Diagram.

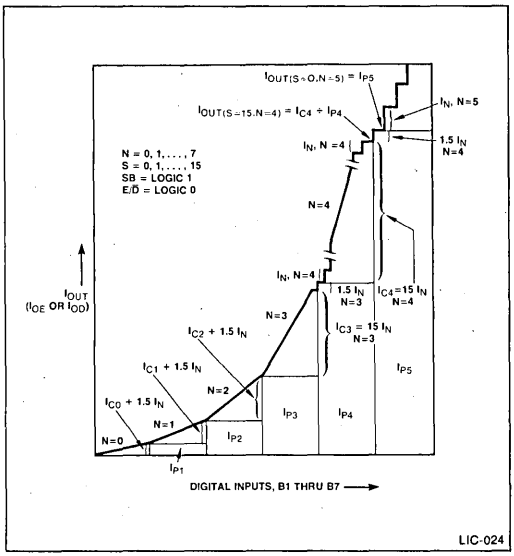


Fig. 7. Construction of μ-Law Transfer Function.

chord, C0, is generated from a current source, I_{C0}. The second chord, C1, starts at current I_{P1}, (known as the pedestal current), and is generated from a current source, I_{C1}, which is twice the value of I_{C0}. The next chord current source, I_{C2}, starts at a pedestal current I_{P2} and has a total value equal to four times I_{C0}. This process continues with each chord N having a total chord current equal to $2^N I_{C0}$ and starting at a pedestal current which equals the summation of all currents in the lower chords:

$$I_{PN} = \sum_{M=0}^{N-1} (I_{CM} + 1.5 \cdot I_M) = 16.5 \sum_{M=0}^{N-1} I_M, (I_{P0} = 0),$$

where I_M is the step current value in chord M.

The generation of the pedestal current by summing the lower chords ensures monotonic behavior in the transition between chords. The selection of the proper step within the given chord is accomplished by routing the chord current, I_{CN}, through a step generator which chooses the proper fraction of the chord current necessary to generate the selected number of steps. The resulting net output current I_{OUT}, can be expressed in terms of step currents, I_N, corresponding to the chord N:

$$I_{OUT} = I_{PN} + S \cdot I_N = (16.5 \sum_{M=0}^{N-1} I_M) + S \cdot I_N, (I_{P0} = 0),$$

where S = step number = 0, 1, . . . , 15 and N = chord number = 0, 1, . . . , 7.

The circuit has 9 digital inputs, an 8-bit word and a control bit. The 8-bit digital input word is broken into three parts. The first bit is the sign bit and specifies whether the output lies in the positive or negative portion of the curve. The next three bits define which of the 8 chords is to be selected. This three bit field has a value designated as N which is between 0 and 7. The last four bits specify one of the sixteen steps and has a value equal to S. The control bit is the E/$\overline{D}$ signal which controls the output switching.

The chord generator is the key element in the DAC. It must generate eight binary weighted chord currents and is similar to an 8-bit linear DAC. The detailed schematic, shown in Figure 8, shows a master/slave ladder arrangement biased from a reference amplifier and transistor. The reference amplifier forces the base voltage of the reference transistor, (Q_0), to the value required to sink the reference current. This voltage will bias the master ladder so that Q1 runs at $2 \cdot I_{REF}$, Q2 at I_{REF}, Q3 at $.5 \cdot I_{REF}$, and Q4A and Q4B at $.25 \cdot I_{REF}$ each. The slave array uses a binary weighted resistor array to generate the lower four chord currents by dividing the current from Q4B. An 8-bit linear DAC does not require the resistor array in the slave ladder but the Companding DAC does, in order to ensure 12-bit linearity in Chord 0. The LSB current in an AmDAC-08 is 8μA $\pm$4μA while the Chord 0 current source in an Am6070 has a value of 8μA $\pm$.5μA.

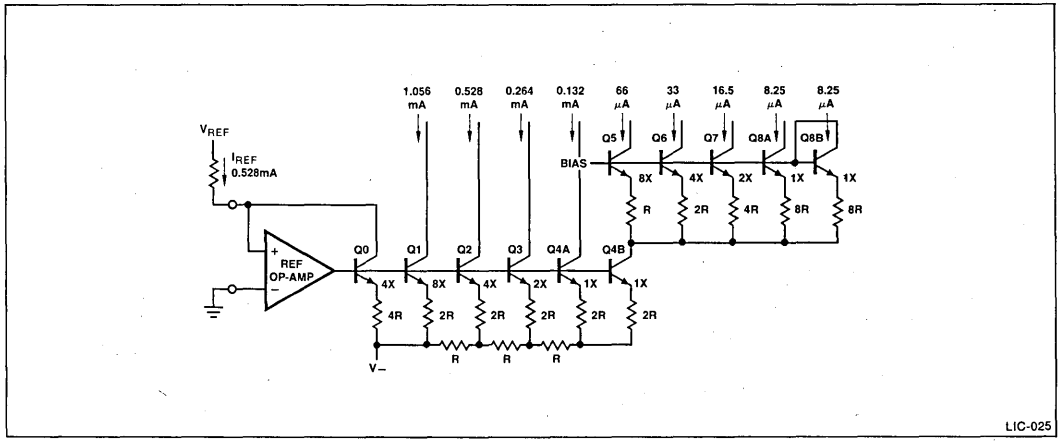


Fig. 8. Chord Current Generator Diagram (Indicated current values correspond to the μ-law DAC).

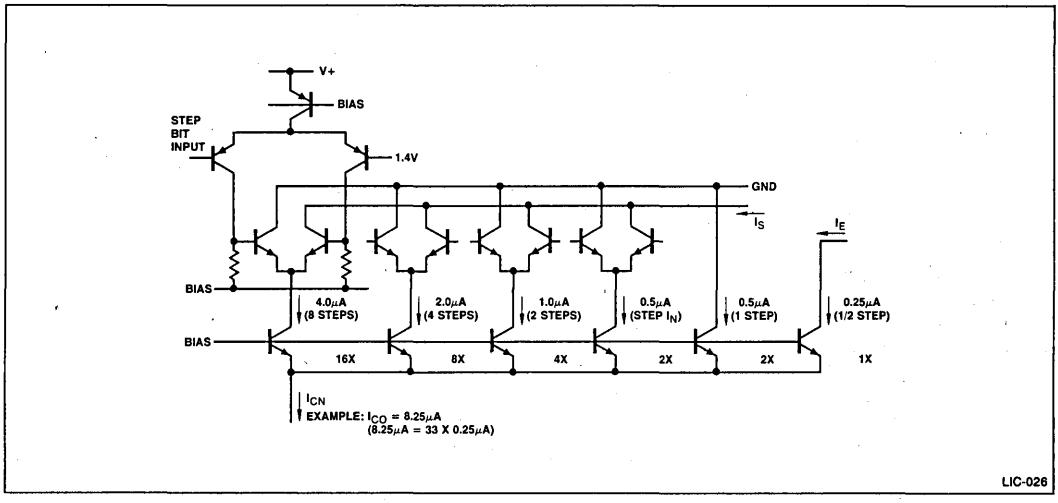


Fig. 9. μ-Law Step Current Generator.

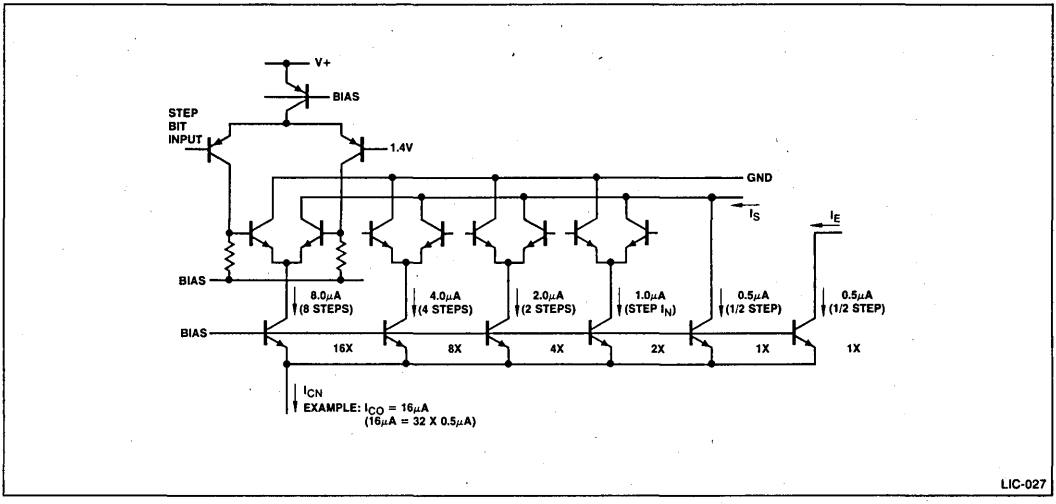


Fig. 10. A-Law Step Current Generator.

The chord select inputs, B1, B2, B3, control a one of eight decoder that selects one of the chords, routes that chord current source to the step generator and switches all the lower order chord current sources to the pedestal generator.

The step generator for the μ-law characteristic is shown in detail in Figure 9. This circuit divides the total chord current source, I_{CN}, into 33 equal parts, and the step current value, I_N, is equal to 2/33 of the chord current source. The 33 parts accommodate the required 1.5 step transition between chords, so that the total internal chord current source is equal to 16.5 steps. The step generator is similar to a four bit DAC but has six current source outputs to generate 8, 4, 2, 1, .1 and 1/2 step currents. This current division can be done using emitter area scaling with enough accuracy to meet the monotonicity and linearity specifications without the use of emitter resistors. The four step bit inputs can choose from 0 to 15 steps to be switched into the output summing network. The 1/2 step current is used as the encode offset current in the encode mode and will track the value of the chord current. When the transition to the next chord is made, the full chord current is switched to the pedestal generator causing a change in the output of 1.5 steps, i.e., from 15 steps to 16.5 steps. The step selector uses a fully differential current switch to ensure high speed performance. This switch does not require capacitive charging and discharging of low current nodes and has a nearly constant 40ns propagation delay over the dynamic range of the varying chord currents, from the first step current on chord 0 of .5μA to the last step current on chord 7 of .5mA.

Companding DAC

The output summing network sums the outputs of the pedestal generator, step generator, and encode current, and routes the current to the output selected by the combination of SB and E/$\overline{D}$. If the E/$\overline{D}$ input is high, the encode current, I_{EN}, is summed with the step and pedestal currents and is routed to $I_{OE(+)}$, if SB is 1, or to $I_{OE(-)}$, if SB is 0. If E/$\overline{D}$ is low, only the step and pedestal currents are summed and sent to the output; the output current is routed to $I_{OD(+)}$ or $I_{OD(-)}$ depending on the state of SB. Only one output will be active and the other outputs will be in a high impedance, off, state.

Generation of the μ-Law and A-Law Characteristics

The μ-law and A-law devices have similar characteristics which differ in the chords near zero. In the μ-law device, the step size doubles when chord 0 ends and chord 1 begins and the first step of chord zero is equal to zero, and the points for positive and negative zero are the same. In the A-law curve, the step size does not change between chord 0 and chord 1. The first two chords are colinear and the step size does not start doubling until chord 2. Additionally, the A-law curve has a 1/2 step offset at the zero point so that positive and negative zero are not equal. These differences in the two companding laws are relatively minor and the two laws can be generated from the same integrated circuit with only minor modifications.

The μ-law curve is generated using the earlier described step generator. If step size in the first chord is set to be .5μA, the internal chord 0 current source must be 8.25μA (16.5 x .5μA). Each succeeding internal chord current source doubles in value so that the last two chord current sources are 528μA and 1056μA. The reference current is equal to 1/2 the largest current source, so the required reference current is 528μA. The full scale output current can be calculated by summing all the internal current sources and subtracting 1.5 steps from the most significant chord, because the full scale current output requires only 15 steps out of the available 16.5 steps to be switched into the output. This gives a full scale current of 2007.75μA. The output current for any point on the companding curve can be calculated in terms of the internal chord 0 source, 8.25μA, and its step value, .5μA, using the following formula:

$$I_{N,S} = ((2^N - 1) \cdot 8.25\mu A) + (S \cdot 2^N \cdot 5\mu A)$$

where N represents the chord number and S the step number. The first term represents the pedestal current value; the second term the value of the steps in the selected chord.

The A-law curve is generated by using the step generator shown in Figure 10. The internal chord current source is divided into 32 equal parts with current source values of 8, 4, 2, 1, 1/2 and 1/2 steps. The zero offset is generated by summing a 1/2 step current with the output of the step generator independent of input code. The range of output values of the step generator is from 1/2 step to 15.5 steps, and the internal chord current source has a value equal to 16 steps. The 1.5 step transition is accomplished by switching the total internal chord current source to the pedestal generator, i.e., adds 1/2 step, (the encode current I_{EN}), and summing the 1/2 step offset current from the next higher chord, which is the same as one step on the lower chord.

The A-law Companding DAC doubles the size of the chord 0 current source I_{C0} from the μ-law I_{C0} value by connecting the collector of Q8B to Q8A instead of its base as indicated in Figure 8, so that it is equal to the chord 1 current source. The reference current is adjusted to set the first chord step size to 1μA and the internal chord 0 current source value to 16μA. The last two chords will have internal current source values of 512μA and 1024μA each. The reference current required to bias the chord generator is 512μA. The full scale output current can be calculated by summing all the internal chord current sources and subtracting 1/2 step from the last chord, because only 15.5 steps of the 16 steps in the last chord are switched to the output. The full scale current is nominally 2016μA. The current at any point on the A-law companding curve can be calculated by using the following formula:

$$I_{N,S} = (2S+1) \cdot .5\mu A, \text{ for } N=0, \text{ and}$$
$$= (2^{N-1} \cdot 16.5\mu A) + (2^{N-1} \cdot S \cdot 1\mu A), \text{ for } N \geq 1.$$

Output Current Tables

All output current values on the A-law transfer characteristic curve are higher than corresponding μ-law current values, because of the larger step sizes in chord 0 for the A-law characteristic. The different step sizes in chord 0 were originally suggested by the International Telegraph and Telephone

TABLE 1
NORMALIZED A-LAW DECODER OUTPUT
(SIGN BIT EXCLUDED)

STEP (S)	CHORD (C)							
	0	1	2	3	4	5	6	7
0	1	33	66	132	264	528	1056	2112
1	3	35	70	140	280	560	1120	2240
2	5	37	74	148	296	592	1184	2368
3	7	39	78	156	312	624	1248	2496
4	9	41	82	164	328	656	1312	2624
5	11	43	86	172	344	688	1376	2752
6	13	45	90	180	360	720	1440	2880
7	15	47	94	188	376	752	1504	3008
8	17	49	98	196	392	784	1568	3136
9	19	51	102	204	408	816	1632	3264
10	21	53	106	212	424	848	1696	3392
11	23	55	110	220	440	880	1760	3520
12	25	57	114	228	456	912	1824	3648
13	27	59	118	236	462	944	1888	3776
14	29	61	122	244	488	976	1952	3904
15	31	63	126	252	504	1008	2016	4032
STEP SIZE	2	2	4	8	16	32	64	128

TABLE 2
NORMALIZED μ-LAW DECODER OUTPUT
(SIGN BIT EXCLUDED)

STEP (S)	CHORD (C)							
	0	1	2	3	4	5	6	7
0	0	33	99	231	495	1023	2079	4191
1	2	37	107	247	527	1087	2207	4447
2	4	41	115	263	559	1151	2335	4703
3	6	45	123	279	591	1215	2463	4959
4	8	49	131	295	623	1279	2591	5215
5	10	53	139	311	655	1343	2719	5471
6	12	57	147	327	687	1407	2847	5727
7	14	61	155	343	719	1471	2975	5983
8	16	65	163	359	751	1535	3103	6239
9	18	69	171	375	783	1599	3231	6495
10	20	73	179	391	815	1663	3359	6751
11	22	77	187	407	847	1727	3487	7007
12	24	81	195	423	879	1791	3615	7263
13	26	85	203	439	911	1855	3743	7519
14	28	89	211	455	943	1919	3871	7775
15	30	93	219	471	975	1983	3999	8031
STEP SIZE	2	4	8	16	32	64	128	256

TABLE 3
IDEAL A-LAW DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	−69.11	−38.74	−35.72	−26.70	−20.68	−14.66	−8.64	−2.62
1	−59.57	−38.23	−32.21	−26.19	−20.17	−14.15	−8.13	−2.11
2	−55.13	−37.75	−31.73	−25.71	−19.68	−13.66	−7.64	−1.62
3	−52.21	−37.29	−31.27	−25.25	−19.23	−13.21	−7.19	−1.17
4	−50.03	−36.85	−30.83	−24.81	−18.79	−12.77	−6.75	−0.73
5	−48.28	−36.44	−30.42	−24.40	−18.38	−12.36	−6.34	−0.32
6	−46.83	−36.05	−30.03	−24.00	−17.98	−11.96	−5.94	+0.08
7	−45.59	−35.67	−29.65	−23.63	−17.61	−11.59	−5.57	+0.46
8	−44.50	−35.31	−29.29	−23.27	−17.24	−11.22	−5.20	+0.82
9	−43.54	−34.96	−28.94	−22.92	−16.90	−10.88	−4.86	+1.16
10	−42.67	−34.62	−28.60	−22.58	−16.56	−10.54	−4.52	+1.50
11	−41.88	−34.30	−28.28	−22.26	−16.24	−10.22	−4.20	+1.82
12	−41.15	−33.99	−27.97	−21.95	−15.93	−9.91	−3.89	+2.13
13	−40.48	−33.69	−27.67	−21.65	−15.63	−9.61	−3.59	+2.43
14	−39.86	−33.40	−27.38	−21.36	−15.34	−9.32	−3.30	+2.72
15	−39.28	−33.12	−27.10	−21.08	−15.06	−9.04	−3.02	+3.00

TABLE 4
IDEAL μ-LAW DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	–	−44.73	−35.18	−27.82	−21.20	−14.90	−8.74	−2.65
1	−69.07	−43.73	−34.51	−27.24	−20.66	−14.37	−8.22	−2.13
2	−63.05	−42.84	−33.88	−26.70	−20.15	−13.87	−7.73	−1.65
3	−59.53	−42.03	−33.30	−26.18	−19.66	−13.40	−7.27	−1.19
4	−57.03	−41.29	−32.75	−25.70	−19.21	−12.96	−6.83	−0.75
5	−55.10	−40.61	−32.24	−25.24	−18.77	−12.53	−6.41	−0.33
6	−53.51	−39.98	−31.75	−24.80	−18.36	−12.13	−6.01	+0.06
7	−52.17	−39.39	−31.29	−24.39	−17.96	−11.74	−5.63	+0.44
8	−51.01	−38.84	−30.85	−23.99	−17.58	−11.37	−5.26	+0.81
9	−49.99	−38.32	−30.44	−23.61	−17.22	−11.02	−4.91	+1.16
10	−49.07	−37.83	−30.04	−23.25	−16.87	−10.68	−4.57	+1.49
11	−48.25	−37.37	−29.66	−22.90	−16.54	−10.35	−4.25	+1.82
12	−47.49	−36.93	−29.29	−22.57	−16.22	−10.03	−3.93	+2.13
13	−46.80	−36.51	−28.95	−22.25	−15.91	−9.73	−3.63	+2.43
14	−46.15	−36.11	−28.61	−21.94	−15.61	−9.43	−3.34	+2.72
15	−45.55	−35.73	−28.29	−21.63	−15.32	−9.15	−3.06	+3.00

3

Consultive Committee (CCITT), in its recommendation for the encoding laws in Pulse Code Modulation communication systems for voice frequency signals of commercial quality.

This recommendation contains several different tables with information for A-law and μ-law encoding requirements. The most important pair of tables contain all 128 distinctive decoder output current values expressed in normalized units. The normalized current output values for A-law and μ-law Companding DACs are presented in Tables 1 and 2, respectively. Step 0 of chord 0 in the A-law table is equal to the value of one normalized unit, whereas the corresponding normalized zero current value in the μ-law table is zero. The actual size of this normalized unit is NOT REQUIRED TO BE THE SAME for A-law and for μ-law, and entries in Tables 1 and 2 should not be used for any comparison of the two encoding laws. Each table, independently, provides the information for a particular encoding law about required relationships between the output current magnitudes. In addition, the input data coding for Table 2, which contains entries for the μ-law normalized output values, is the one's complement of the input data codes suggested by the original CCITT and Bell D3 specification. However, data input coding shown in Tables 1 and 2 is accepted as standard input data coding in order to have consistent data coding for μ-law and A-law Companding DACs. The maximum normalized current values in Tables 1 and 2 are 4032 and 8031, respectively, and these values can be easily derived by summing all of the 128 normalized steps.

Additional conditions beyond the two maximum normalized values are related to the ratios, in μA, between the amplitudes corresponding to full scale current values, and the amplitudes of output currents which are chosen as the reference outputs for A-law and for μ-law decoding devices. These reference outputs are generated as sinusoidal waveforms of 1kHz by applying a periodic sequence of eight 8-bit data words at the Companding DAC's inputs at an 8kHz rate. These sequences are specified separately for both encoding laws. The signal level at the peaks of these reference sinusoidal waveforms is chosen as the reference 0dB level. This level is implied to be the same for both encoding laws. The dB levels, calculated by using the peaks of the 1kHz sinusoidal waveforms with amplitudes which correspond to the theoretical maximum output current values, are specified to be +3.14dB and +3.17dB above the common reference level for the A-law and μ-law decoding devices, respectively. The small difference in the specified theoretical maximum output current levels implies a very small difference between actual full scale current values for A-law and μ-law decoders. In practice, the actual level for the full scale output current values for both laws is set to be +3.00dB above the reference 0dB level. The ideal decoder output values expressed in dB down from the full scale current output for A-law and μ-law are presented in Tables 3 and 4. The reference 0dB level can be found in these tables between steps 5 and 6 on chord 7. Comparison of the numbers corresponding to step 1 in chord 0 shows a difference between the two encoding laws with respect to the output dynamic ranges. The output dynamic range is 62.57dB for A-law, (+3.00dB to −59.57dB), and 72.07dB for μ-law, (+3.00dB to −69.07dB).

In order to make the electrical designs of A-law and μ-law Companding DACs as similar as possible, the normalized unit value of current in Table 1, A-law table, is chosen to be 0.5μA and the normalized unit current quantity in Table 2, μ-law table, is chosen to be 0.25μA. These different "unit" values will cause the steps in chord 0 for A-law Companding DACs to be twice as large as the corresponding μ-law device step sizes. Consequently, the ideal full scale absolute current values corresponding to 4032 and 8031 normalized units are 2016μA for A-law and 2007.75μA for μ-law DACs. Tables 5 and 6 contain all 128 absolute decoder output current values in μA. These tables can be further expressed in terms of percent of full scale current output, which may be important for some "percentage" oriented applications. Tabulated summaries of step and chord endpoint sizes which can be extracted from Tables 1 through 6 are presented in Tables 7 and 8. The last column in these tables points out that the best resolution and accuracy are achieved in chord 0 of the Companding DAC's transfer function.

The output current values presented in Tables 5 and 6 are ideal output currents with ideal reference currents of 528μA and 512μA, respectively. The output current deviations for the communication application of Companding DACs are specified by the compandor tracking system requirements which are illustrated for both decoders in Figures 11 and 12. In both figures a dotted line represents a total gain deviation, in dB, for

TABLE 5
IDEAL A-LAW DECODER OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.500	16.500	33.000	66.000	132.00	264.00	528.00	1056.00
1	1.500	17.500	35.000	70.000	140.00	280.00	560.00	1120.00
2	2.500	18.500	37.000	74.000	148.00	296.00	592.00	1184.00
3	3.500	19.500	39.000	78.000	156.00	312.00	624.00	1248.00
4	4.500	20.500	41.000	82.000	164.00	328.00	656.00	1312.00
5	5.500	21.500	43.000	86.000	172.00	344.00	688.00	1376.00
6	6.500	22.500	45.000	90.000	180.00	360.00	720.00	1440.00
7	7.500	23.500	47.000	94.000	188.00	376.00	752.00	1504.00
8	8.500	24.500	49.000	98.000	196.00	392.00	784.00	1568.00
9	9.500	25.500	51.000	102.000	204.00	408.00	816.00	1632.00
10	10.500	26.500	53.000	106.000	212.00	424.00	848.00	1696.00
11	11.500	27.500	55.000	110.000	220.00	440.00	880.00	1760.00
12	12.500	28.500	57.000	114.000	228.00	456.00	912.00	1824.00
13	13.500	29.500	59.000	118.000	236.00	472.00	944.00	1888.00
14	14.500	30.500	61.000	122.000	244.00	488.00	976.00	1952.00
15	15.500	31.500	63.000	126.000	252.00	504.00	1008.00	2016.00
STEP SIZE	1	1	2	4	8	16	32	64

TABLE 6
IDEAL μ-LAW DECODER OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
STEP SIZE	.5	1	2	4	8	16	32	64

TABLE 7
A-LAW DECODER STEP SIZE AND CHORD SIZE SUMMARY

Chord	Step Size Normalized to Full Scale	Chord Endpoints Normalized to Full Scale	Step Size in μA with 2016μA F. S.	Chord Endpoints in μA with 2016μA F. S.	Step Size as a % of Full Scale	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale	Resolution & Accuracy of Equivalent Binary DAC
0	2	31	1.0	15.5	0.05%	0.77%	−42.28	Sign + 11 Bits
1	2	63	1.0	31.5	0.05%	1.56%	−36.12	Sign + 11 Bits
2	4	126	2.0	63.0	0.1%	3.13%	−30.10	Sign + 10 Bits
3	8	252	4.0	126.0	0.2%	6.25%	−24.08	Sign + 9 Bits
4	16	504	8.0	252.0	0.4%	12.5%	−18.06	Sign + 8 Bits
5	32	1008	16.0	504.0	0.8%	25.0%	−12.04	Sign + 7 Bits
6	64	2016	32.0	1008.0	1.6%	50.0%	−6.02	Sign + 6 Bits
7	128	4032	64.0	2016.0	3.2%	100%	0	Sign + 5 Bits

TABLE 8
μ-LAW DECODER STEP SIZE AND CHORD SIZE SUMMARY

Chord	Step Size Normalized to Full Scale	Chord Endpoints Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Chord Endpoints in μA with 2007.75μA FS	Step Size as a % of Full Scale	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale	Resolution & Accuracy of Equivalent Binary DAC
0	2	30	0.5	7.5	0.025%	0.37%	−48.55	Sign + 12 Bits
1	4	93	1.0	23.25	0.05%	1.16%	−38.73	Sign + 11 Bits
2	8	219	2.0	54.75	0.1%	2.73%	−31.29	Sign + 10 Bits
3	16	471	4.0	117.75	0.2%	5.86%	−24.63	Sign + 9 Bits
4	32	975	8.0	243.75	0.4%	12.1%	−18.32	Sign + 8 Bits
5	64	1983	16.0	495.75	0.8%	24.7%	−12.15	Sign + 7 Bits
6	128	3999	32.0	999.75	1.6%	49.8%	−6.06	Sign + 6 Bits
7	256	8031	64.0	2007.75	3.2%	100%	0	Sign + 5 Bits

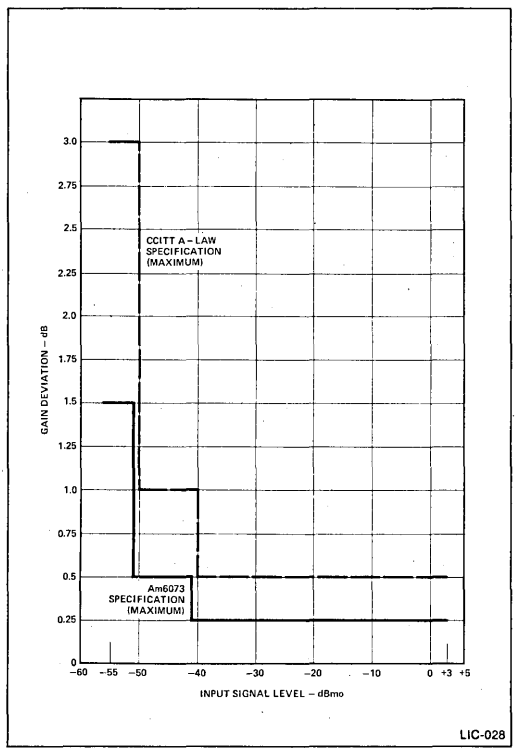


Fig. 11. CCITT A-Law Compandor Tracking Specification.

various signal levels which can be distributed over the encoder and decoder portions of a "one way" communication system. It is understood that encoder and decoder system portions are implemented with corresponding Companding DACs. For the Bell D3 system μ-law tracking specification, the −37dBmo and −50dBmo output current levels can be found between steps 11 and 12 on chord 1, and steps 8 and 9 on chord 0, respectively. For the CCITT A-law compandor tracking specification, the −40dBmo, −50dBmo, and −55dBmo output current levels can be found in the corresponding A-law tables between steps 13 and 14 on chord 0, steps 4 and 5 on chord 0, and steps 2 and 3 on chord 0, respectively. Conversion of the requirements imposed by Figure 12 to absolute current values produces corresponding absolute decode output current tables with minimum, ideal and maximum values specified for each step.

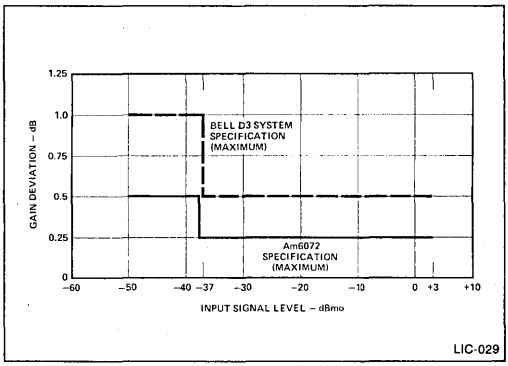


Fig. 12. Bell D3 System Compandor Tracking Specification.

TABLE 9
ABSOLUTE DECODER OUTPUT CURRENT LIMITS IN μA
CONFORMING TO BELL D3 COMPANDOR TRACKING SPECIFICATIONS

STEP NO.	CHORD NO.							
	0	1	2	3	4	5	6	7
0	−.250	7.789	24.048	56.112	120.24	248.49	505.00	1018.02
	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
	.250	8.739	25.473	59.436	127.36	263.22	534.93	1078.34
1	.250	8.733	25.991	59.998	128.01	264.04	536.10	1080.21
	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
	.750	9.798	27.531	63.553	135.60	279.69	567.86	1144.21
2	.750	9.677	27.934	63.885	135.79	279.59	567.19	1142.39
	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
	1.250	10.857	29.590	67.670	143.83	296.15	600.80	1210.08
3	1.250	10.621	29.878	67.771	143.56	295.13	598.28	1204.58
	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
	1.750	11.917	31.648	71.787	152.06	312.62	633.73	1275.95
4	1.750	11.565	31.821	71.658	151.33	310.68	629.37	1266.76
	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
	2.250	12.976	33.706	75.904	160.30	329.09	666.66	1341.82
5	2.250	12.509	33.764	75.544	159.10	326.22	660.46	1328.94
	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
	2.750	14.035	35.765	80.020	168.53	345.55	699.60	1407.69
6	2.750	13.453	35.707	79.431	166.88	341.77	691.56	1391.13
	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
	3.250	15.094	37.823	84.137	176.77	362.02	732.53	1473.56
7	3.250	14.397	37.651	83.317	174.65	357.32	722.65	1453.31
	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
	3.750	16.154	39.882	88.254	185.00	378.49	765.47	1539.43
8	3.750	15.341	39.594	87.204	182.42	372.86	753.74	1515.50
	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
	4.250	17.213	41.940	92.371	193.23	394.96	798.40	1605.30
9	4.248	16.285	41.537	91.090	190.20	388.41	784.83	1577.68
	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
	4.767	18.272	43.998	96.488	201.47	411.42	831.34	1671.16
10	4.720	17.229	43.480	94.977	197.97	403.95	815.92	1639.87
	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
	5.296	19.331	46.057	100.604	209.70	427.89	864.27	1737.03
11	5.192	18.173	45.424	98.863	205.74	419.50	847.02	1702.05
	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
	5.826	19.812	48.115	104.721	217.93	444.36	897.21	1802.90
12	5.664	19.675	47.367	102.750	213.52	435.05	878.11	1764.23
	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
	6.356	20.841	50.174	108.838	226.17	460.82	930.14	1868.77
13	6.136	20.647	49.310	106.636	221.29	450.59	909.20	1826.42
	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
	6.885	21.871	52.232	112.955	234.40	477.29	963.07	1934.64
14	6.608	21.619	51.253	110.523	229.06	466.14	940.29	1888.60
	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
	7.415	22.900	54.290	117.072	242.63	493.76	996.01	2000.51
15	7.080	22.590	53.197	114.409	236.83	481.68	971.39	1950.79
	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
	7.944	23.929	56.349	121.188	250.87	510.23	1028.94	2066.38
STEP SIZE	5	1	2	4	8	16	32	64

The decoder output current values which comply with the Bell D3 compandor tracking requirements are presented in Table 9. A similar table can be generated for the CCITT A-law compandor tracking specification. The corresponding encode output values can be derived from the decode output values by adding a half a step to all entries in a given decode table. The specified limit values include the combined effects of chord end point deviations, step nonlinearity, encode output errors, full scale current deviation from ideal, full scale symmetry error, zero scale current error, full scale drift, and output impedance change over the specified voltage compliance and temperature ranges. The adjacent step current levels in Table 9 for any particular Companding DAC will not overlap, as might be implied from the presented minimum and maximum values, because the device is guaranteed to be monotonic.

If the decode output limits for the μ-law Companding DAC are specified to be ±1/2 step from the ideal values, Table 9 can be replaced by a similar table. The most important difference between the two tables would be found in the limit values corresponding to the lower step current values in chords 1 through 7. The approximate representations of ±1/2 step, ±1 step limits and the corresponding Bell D3 compandor tracking limits in Table 9 are illustrated in Figure 13.

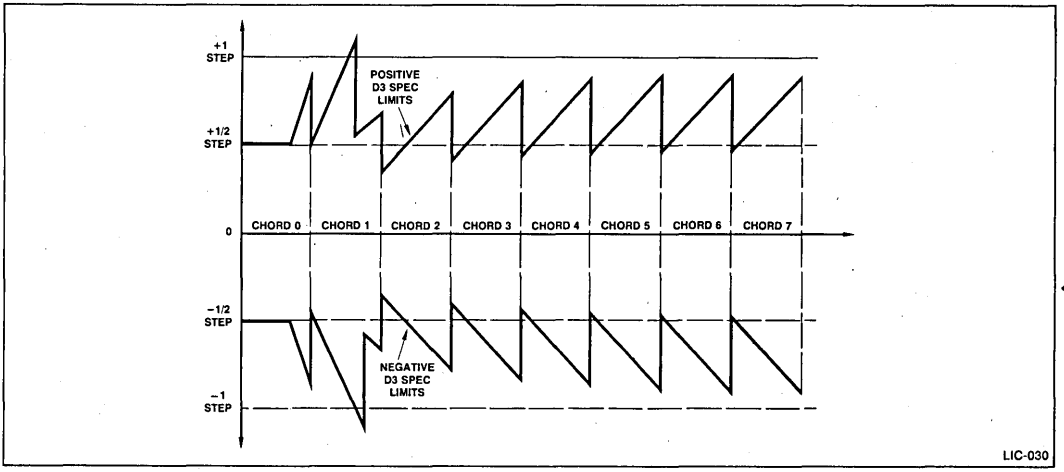


Fig. 13. Output Current Limit Diagrams for D3, ±1/2 Step, and ±1 Step Tolerance Specifications.

Parametric Analysis and Recommendations

A detailed specification for a digital-to-analog converter should include information about important DAC parameters such as resolution, monotonicity, dynamic range, settling time, nonlinearity, full scale and zero scale current errors, gain error, output voltage compliance, input, output and reference signal levels, operating temperature range, power supply range and power dissipation.

The resolution of a DAC is determined by the maximum number of digital input combinations which can be used to generate analog output signals. The resolution for Companding DACs with sign-plus-7 bit digital data input signals is ±128 steps. A converter is monotonic if its analog output always increases with an increase in the digital value of the input data code. Monotonicity for the Am6070/72 devices, is guaranteed over the full operating temperature range and for both groups of 128 steps. Two parameters which are used to describe nonlinear errors in a DAC's transfer function are the DAC's nonlinearity and the differential nonlinearity error. The nonlinearity of a Companding DAC is defined as the maximum deviation of the actual output values from an ideal piece-wise linear characteristic calculated from measurements of the actual full scale and zero scale current values. These two current measurements can be used to compute the corresponding theoretical chord endpoint values, and nonlinearity is measured as the difference between this calculated transfer characteristic and the actual current values at the output of the DAC. The differential nonlinearity of the device is a measure of how much any single step current value varies with respect to its theoretical value, (calculated from the actual full scale output current). Differential nonlinearity of ±1/2 step will ensure monotonic behavior. These errors and all other transfer function related errors are specified for the Am6070 Companding DAC Family by the limit current values in the corresponding Absolute Decoder Output Current Level Table.

The DAC's current outputs have a very high impedance, and the output current will not change its value significantly with changes in the applied voltage at the DAC's outputs. The output voltage compliance range is defined as the maximum range of voltages, at the DAC's output, that can be sustained while meeting the output current specifications. The absolute maximum output voltage swing, (I_{REF} = 528μA), is specified between V− plus 10V and V− plus 36V, where V− is the Companding DAC's negative power supply. The maximum range for the reference inputs $V_{R(-)}$ and $V_{R(+)}$ is specified to be between the V− and V+ power supply values. The maximum power supply range, V+ to V−, is specified at 36V, and maximum power dissipation for temperatures less than 100°C is rated at 500mW.

The settling time for a DAC is defined as the elapsed time, after an input code transition, required for the DAC's output to reach a final value within specified limits. These limits are generally ±1/2 of the corresponding step current value. The settling time is usually specified for the input code transition from zero scale to full scale value, and for the Companding DAC Am6070 family the typical value is 300ns. However, this is not the worst case transition. Because of the different step sizes, the output current settling error band changes as the chord current changes, becoming smaller for lower chords. Settling times in chord 7 are measured when the output settles within ±32μA of its final value, while settling times in chord 0 are measured when the output settles to within ±.25μA of it's final value. The worst case transition is, therefore, the transition from full scale current down to zero scale current value, and requires a settling time of 4μs for μ-law DACs and 2.5μs for A-law DACs.

The currents of each of the four Companding DAC's analog outputs can be measured using the circuit shown in Figure 14. This circuit contains 4 resistors, R1, R2, R3, R4, and two operational amplifiers, A1 and A2. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset current of the operational amplifier also increases the output measurement error. This error is most significant near zero scale. The Am101A and Am308 devices, for example, may be used for A1 and A2, since their maximum offset currents which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltage of the amplifiers, with output resistor values of 2.5kΩ, also contributes to the output measurement error by a factor of 400nA for every mV of offset voltage. Therefore, to minimize this error, the offset voltages of A1 and A2 should be nulled.

Companding DAC

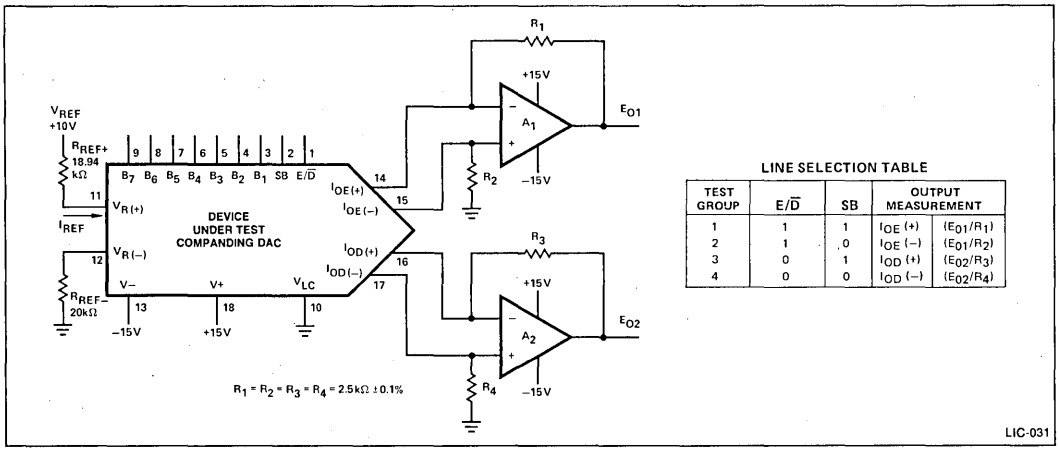


Fig. 14. Companding DAC Output Current DC Test Circuit.

The recommended operating range for the reference current I_{REF} is 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be approximated using the equation $I_{FS} = 3.9 \cdot I_{REF}$. This tight relationship alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors' values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, and will increase the reference amplifier negative common mode input voltage range. However, the device accuracy specifications are not guaranteed at reference currents below 0.5mA.

The ideal value for the reference current, (V_{REF}/R_{REF}), is 528μA for μ-law and 512μA for A-law Companding DACs. The corresponding ideal full scale decode current values are 2007.75μA and 2016μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in the V_{REF} or R_{REF} values produces the same percentage change in the decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of about 0.01μF. The total resistor value should provide the required reference current. The $R_{REF(-)}$ resistor value should approximately equal the $R_{REF(+)}$ value in order to compensate for errors caused by the reference amplifier's input bias current.

An alternative to the positive reference voltage biasing is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

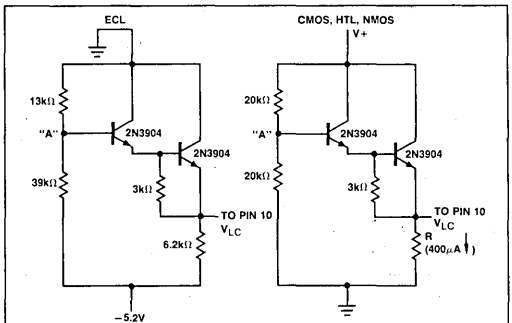
The Companding DAC can be used as a multiplying DAC by varying the reference current. It is important that the reference current have a DC component that guarantees an uninterrupted flow of current INTO the $V_{R(+)}$ terminal. The input reference amplifier has sufficient bandwidth and slew rate, (0.12mA/μs minimum), to handle small signal inputs up to 5% of reference current at frequencies up to 500KHz, and large signal inputs of up to 50% of reference current at frequencies up to 80kHz.

The Companding DAC has a wide output voltage compliance suitable for driving a variety of loads. Using the ideal recommended value for I_{REF} and V− = −15V, the positive voltage compliance limit is +18V and the negative voltage compliance limit is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance limit, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + 2\,(I_{REF} \cdot 1.55k\Omega) + 8.4V,$$

where 1.55kΩ and 8.4V are equivalent worst case values for the Companding DAC.

The V_{LC} input controls the input logic threshold voltage, allowing the device to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 15. For TTL-level logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than −5V.



Notes: 1. Set the voltage "A" to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ± 15V supplies.

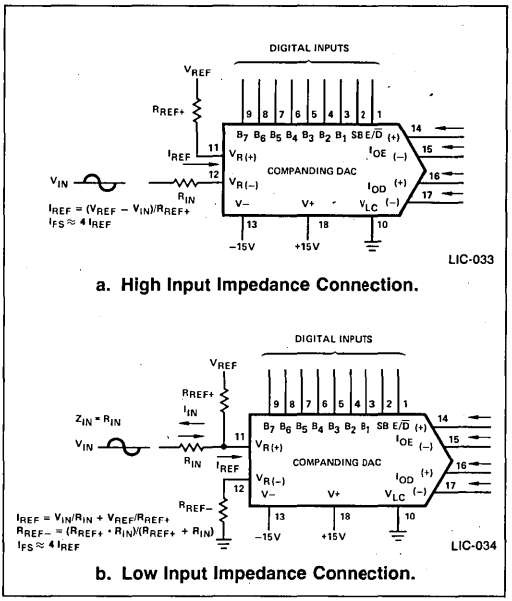
Fig. 15. Interfacing Circuits for ECL, CMOS, HTL and NMOS Logic Inputs.

With the V− voltage between −15V and −11V, the $V_{OC(-)}$ value, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen. With V+ between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.

TYPICAL CIRCUIT APPLICATIONS

Basic Circuit Connections

The Companding DAC belongs to the class of multiplying D to A converters with true current outputs. The input reference current can be generated by a unipolar constant reference voltage source or by a bipolar AC reference voltage. The applied bipolar reference source usually modulates the reference current, I_{REF}, supplied from the constant reference voltage as shown in Figure 16. Figure 16a shows a high input impedance configuration where the bipolar input signal V_{IN} modulates the voltage level at the $V_{R(+)}$ input by forcing the voltage across R_{REF} to be $V_{REF} - V_{IN}$, which in turn modifies I_{REF}. Figure 16b shows low input impedance connections, where I_{REF} equals the sum of the DC reference current from V_{REF} and the AC input current from V_{IN}. For both low impedance and high impedance connections, the minimum reference current value at the reference input, $V_{R(+)}$ should be at least 0.1mA and the maximum value should not exceed 1.0mA.

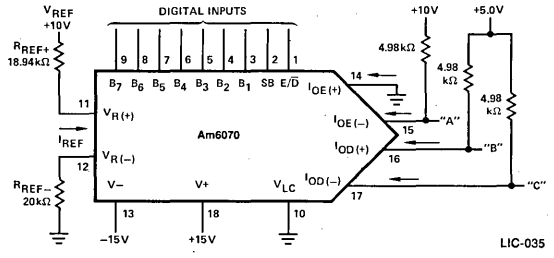


a. High Input Impedance Connection.

b. Low Input Impedance Connection.

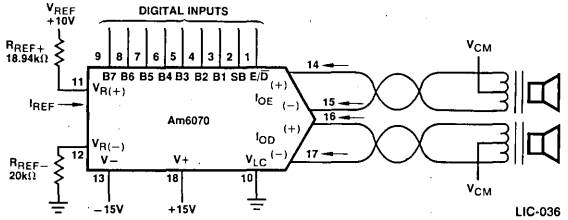
Fig. 16. Companding DAC's Multiplying Connections.

The wide output voltage compliance range, (−5V to +18V with I_{REF} = 528μA and V− = −15V), allows a variety of loads to be driven. Two typical connections are shown in Figure 17. Voltage output relationships for single ended and differential resistive output connections are described in the output voltage table of Figure 17a. The reference current in this resistive load example is set to be 528μA (μ-law Companding DAC). The resulting negative voltage generated by the currents at the outputs A, B, and C, does not exceed the minimum value of −5V, which corresponds to the lower limit of the output voltage compliance range. In the example with balanced load connections, the sum of the common mode voltage, V_{CM}, and the differential voltage across the load should also be within the −5V and +18V output voltage compliance limit.



INPUT CODE (E/D̄, SB, B1, . . ., B7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.02	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

a. Resistive Output Connections.



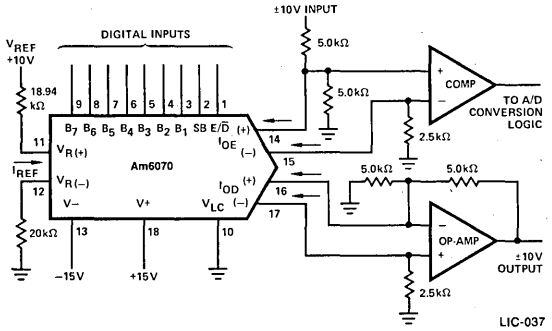
b. Balanced Load Connections.

Fig. 17. Companding DAC's Output Connections.

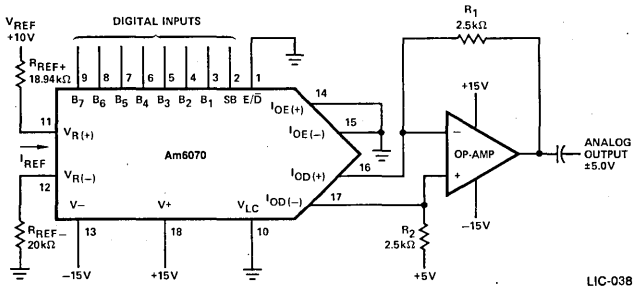
Companding DAC

Operational amplifiers and/or comparators can be driven by Companding DACs. The circuits shown in Figure 18 demonstrate various voltage ranges which can be achieved at the outputs of operational amplifiers. The circuit in Figure 18a provides 0V at the op-amp output whenever the E/$\overline{D}$ input is set to logic 1. When the circuit is in the decode mode, E/$\overline{D}$ = 0 the output voltage polarity is determined by the sign bit input level. With the sign bit set low, the $I_{OD(-)}$ output is active and the corresponding full scale output current, $I_{FS} \approx$ 2mA, will generate a maximum negative voltage of −5V at the op-amp's positive input. The chosen resistor values and their connections provide the op-amp with a gain of 2 and a maximum negative output voltage of −10V. With the sign bit set high the $I_{OD(+)}$ output is active and the op-amp's negative input will be held at virtual ground. With a full scale current of 2mA flowing into the $I_{OD(+)}$ pin, the op-amp will act as a transconductance amplifier supplying 2mA to the $I_{OD(+)}$ pin via the 5kΩ feedback resistor. This current will generate a maximum of +10V at the output, which will make the total output voltage swing between −10V and +10V. The circuit in Figure 18b similarly provides a voltage swing between −5V and +5V across the output capacitor. The output dynamic range expander circuit connections, shown in Figure 19, extend the μ-law Companding DAC's dynamic range from 72dB to 78dB. The A-law Companding DAC's dynamic range can be similarly increased from 62dB to 66dB. In this circuit, the outputs $I_{OD(+)}$ and $I_{OE(+)}$ are tied together, and $I_{OD(-)}$ and $I_{OE(-)}$ are tied together; the E/$\overline{D}$ input is used as a fifth step which represents the least significant digital data input, and provides the desired interleaving between the encode and decode current levels. Each chord now contains 32 uniform steps, with the smallest step size value 0.25μA and the largest value 32μA. The resulting full scale current is equal to the corresponding full scale encode current value, and the ratio between the full scale current value and the smallest current step value, I_{FS}/0.25, exceeds 8000 for the μ-law Companding DAC. The smallest and the largest current step sizes will generate 0.625mV and 80mV changes, respectively, at the op-amp output.

Digital inputs SB and E/$\overline{D}$ can be used together with data inputs B1 through B7 to provide an output multiplexing capability when connected as shown in Figure 20. The logarithmic digital attenuator circuit combines the companding DAC's multiplying capabilities with the multiplexing function which is accomplished by using the SB and E/$\overline{D}$ inputs as channel select inputs. The analog signal, V_{IN}, applied at the $V_{R(-)}$ reference input can be attenuated by approximately 0.3dB per step and 6dB per chord, throughout most of the output dynamic range. The SB and E/$\overline{D}$ inputs provide signal switching combinations which will multiplex the attenuated analog signal into four different analog channels.



a. ±10V Range Encode/Decode Connections.



b. Compliance Extension Using AC Coupled Output.

Fig. 18. Some Output Voltage Expansion Schemes.

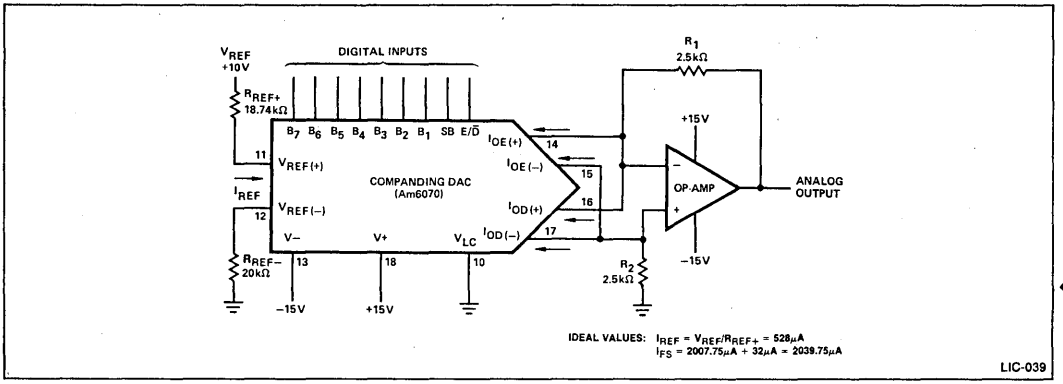


Fig. 19. Output Dynamic Range Expander.

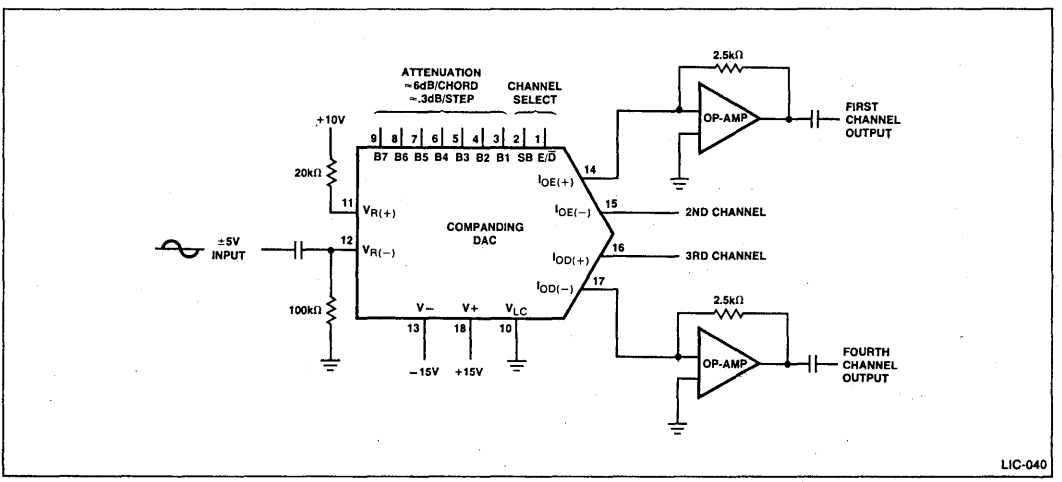


Fig. 20. Logarithmic Digital Attenuator.

For applications where the output dynamic range is to be smaller than 78dB, the circuit connection shown in Figure 21 can be used. With given V_{REF} and V_{IN} values, there are three resistor values, R_{REF}, R1, and R2, which need to be determined. The starting assumption is that a maximum gain of unity from V_{IN} to V_{OUT}, (0dB), is achieved with all digital inputs set to logic 1. The digital inputs all set to logic 0 will determine the minimum gain of the circuit and consequently the desired output dynamic range. Considering the currents flowing through resistors R1, R2, and R_{REF}, and the DAC's output with digital inputs at all 1's, the following relationships can be established:

$$I_{R1} = V'_{OUT}/R1 = I_{OUT} + I_{R2};\ I_{OUT} \approx 3.8\ I_{REF};\ I_{R2} = V_{IN}/R2;$$
$$I_{REF} = (V_{REF} - V_{IN})/R_{REF} \quad (1)$$

The relationship between output voltages V'_{OUT} and V_{OUT} and input voltages, V_{REF} and V_{IN}, can be expressed as follows:

$$V'_{OUT} = 3.8\,(R1/R_{REF})\,V_{REF} - [3.8(R1/R_{REF}) + R1/R2] \cdot V_{IN} \quad (2)$$

$$V_{OUT} = -[3.8\ (R1/R_{REF}) + R1/R2] \cdot V_{IN}$$

In order to have unity gain, $V_{OUT}/V_{IN} = 1$, the coefficient for V_{IN} in the equations (2) must also be 1:

$$-[3.8\ (R1/R_{REF}) + R1/R2] = 1 \quad (3)$$

Two additional conditions for calculating R_{REF}, R1 and R2 values are the minimum gain value G_{min}, and the requirements for the minimum and maximum I_{REF} values, 0.1mA and 1mA, respectively:

$$G_{min,dB} = 20 \log [V_{OUT}/V_{IN}] = -20 \log (R2/R1), \quad (4)$$

and $$0.1mA \leq (V_{REF} - V_{IN})/R_{REF} \leq 1mA \quad (5)$$

The op-amp output in Figure 21 has a DC component that will be attenuated as well as the AC input signal. The output coupling capacitor is used to remove the DC level. However, during switching, the change in DC level will cause a step transient or "click" at the output.

Companding DAC

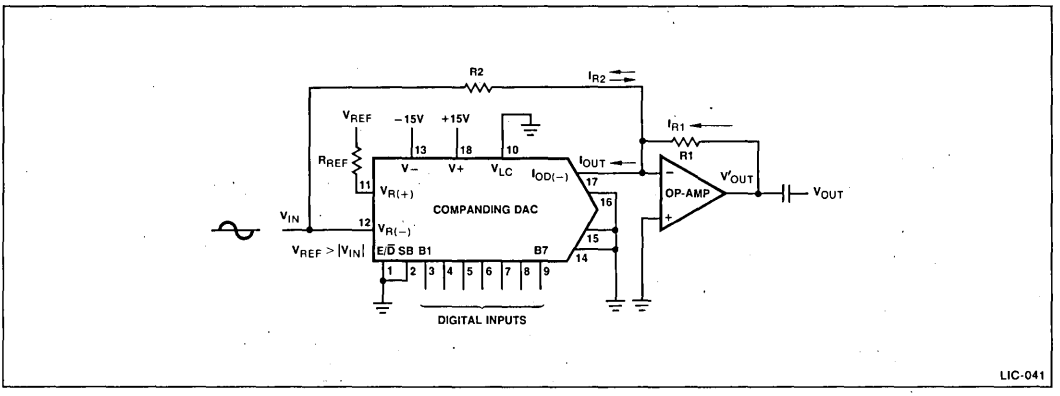


Fig. 21. AC Coupled Digital Attenuator, Adjustable Range.

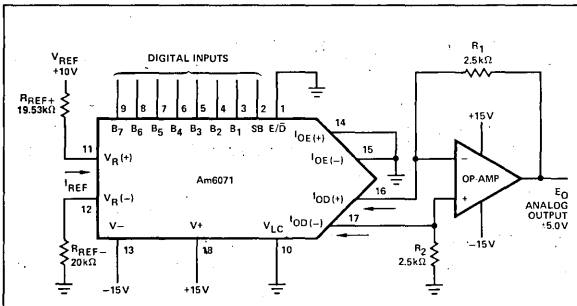
Operating Modes

The Companding DAC has two basic operating modes, decode and encode, which are controlled by the Encode/Decode, E/$\overline{D}$, input signal. A logic 0 applied to the E/$\overline{D}$ input places the Companding DAC in the decode mode, and current will flow into the $I_{OD(+)}$ or $I_{OD(-)}$ output, depending on the state of the sign bit, SB, input. A logic 1 at the E/$\overline{D}$ input places the Companding DAC in the encode mode, which differs from the decode mode by a half step offset current in each chord, and current flows into one of the I_{OE} outputs.

The basic decoder connection for the Companding DAC is shown in Figure 22. The E/$\overline{D}$ input is grounded, which keeps the Companding DAC in the decode mode. The eight digital data inputs generate an output decode current which is converted by an operational amplifier to a bipolar voltage, E_O. Several discrete E_O values are tabulated in Figure 22 for both μ-law and A-law versions of Companding DACs. The values indicated in parenthesis correspond to the A-law Companding DAC.

The Companding DAC can be used together with a Successive Approximation Register, SAR, a comparator, and additional SSI logic elements to perform the encoding or compression of an analog signal. The circuit, Figure 23, represents an Analog-to-Digital data conversion system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input. When the proper $\overline{START}$, $\overline{S}$, and $\overline{CONVERSION\ COMPLETE}$, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with ground which is applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the other input to the exclusive-or gate is held at a logic 0 level by the logic shown in Figure 23. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changes. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Companding DAC. Depending upon the SB input level, the Companding DAC's output current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output.



	E/D̄	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.004V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.0012V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	−0.0012V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.004V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−5.040V

Fig. 22. Detailed Companding DAC Decoder Connection.

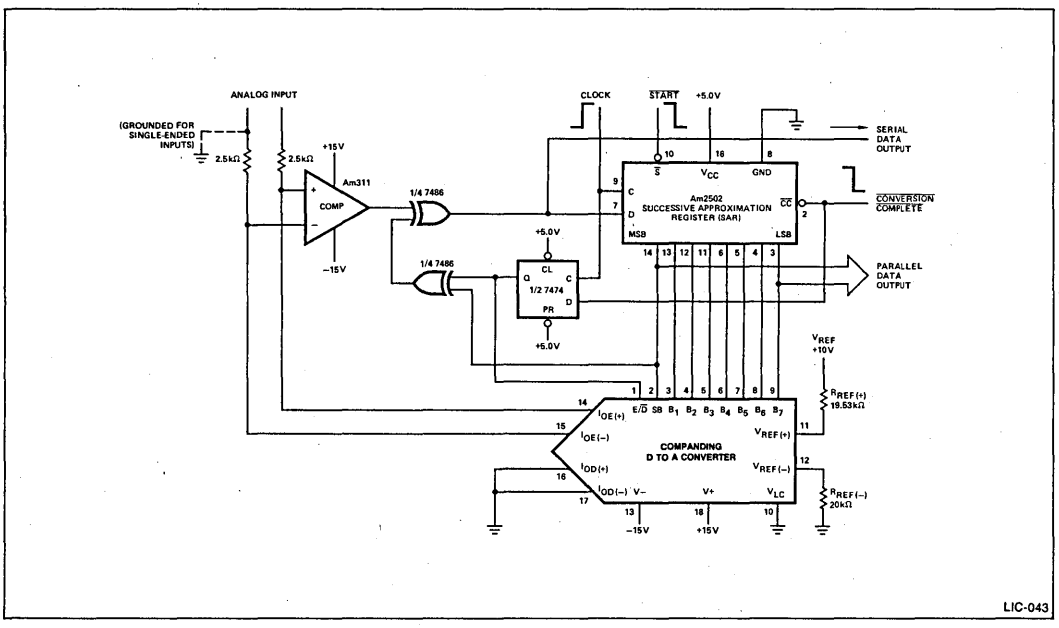


Fig. 23. Detailed Companding DAC Encode Connection.

Nine clock pulses are required to obtain a digital, non-complemented, binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog input signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the input analog signals are usually prevented by using sample and hold circuitry.

When the Companding DAC is used in a feedback loop with a SAR, the data input transitions in the successive approximation search technique exhibit a maximum change of two adjacent bits, and the starting pattern is 0111 1111. The next successive pattern after the first iteration, will be either 00111111 or 10111111. The worst case settling times are experienced during step bit changes in chord 0, where the output current must settle to ±0.25μA. The worst case settling time is about 600ns for code changes in the upper end of chord zero and 1800ns for code changes near zero. The system clock must take into account the settling time of the DAC, the switching speed of the comparator and the time delays in the SAR. In general, the DAC is the slowest component, (comparator Am311's delay is about 200ns and SAR delays are about 46ns), and will determine the clock rate. For optimum accuracy the clock rate should accommodate the 1800ns settling time near zero scale current. However, faster clock rates (1100ns-1800ns) can be used with some degradation in accuracy for signals near zero.

Microprocessor Based Data Acquisition Systems Applications

High output resolution with guaranteed monotonicity over its entire dynamic range and digitally controllable inputs makes the Companding DAC very attractive for application in data acquisition and control systems. The encoding capability, in particular, provides an acquisition system with considerable flexibility, limited only by the rate of change of the acquired analog input signals.

A typical data acquisition system using the Companding DAC is shown in Figure 24. The A to D data conversion procedure is controlled by the 9080A Microprocessor set, (Am9080A 8-bit Microprocessor, Am8224 Clock Generator and Driver, and Am8238 System Controller and Bus Driver). The START one-shot circuit, Am26S02 will be activated by the START A/D command, ($\overline{CS}$ = 0, $\overline{IOW}$ = 0), which will initiate the A to D procedure by setting the $\overline{S}$ input of the SAR circuit, Am2502, to a logic 0. The width of the one-shot pulse must be greater than the period of the DATA CLOCK signal to initialize the SAR logic. The duration of DATA CLOCK period must accommodate the worst settling time of the DAC and comparator Am311, to ensure valid data at the SAR input. The one-shot circuit may be eliminated, provided that the expected worst case settling time does not exceed 1μs and the SYSTEM CLOCK, ϕ1, does not exceed 2MHz. The first data clock after $\overline{S}$ goes low sets the $\overline{CC}$ output high, which in turn switches the input sample and hold circuit, (LF198), into the hold mode and puts the microprocessor into a wait state. After eight subsequent DATA CLOCK periods, (8 x 2μs), the conversion complete signal, $\overline{CC}$, changes from logic 1 to logic 0, which puts the S & H circuit into the sample mode and allows the microprocessor to resume its functions by removing the logic 0 from the RDYIN input of the Am8224 chip. With a logic 1 at the SAR's $\overline{S}$ input, the DATA CLOCK cannot change the SAR's digital data outputs after completion of conversion. Thus, these outputs will be stable and available for subsequent interrogation. The microcomputer will issue a READ A/D command, ($\overline{CS}$ = 0, $\overline{IOR}$ = 0), which enables the three-state data buffer, Am25LS241, and transfers the data outputs of the SAR to the system data bus and into the micro-

Companding DAC

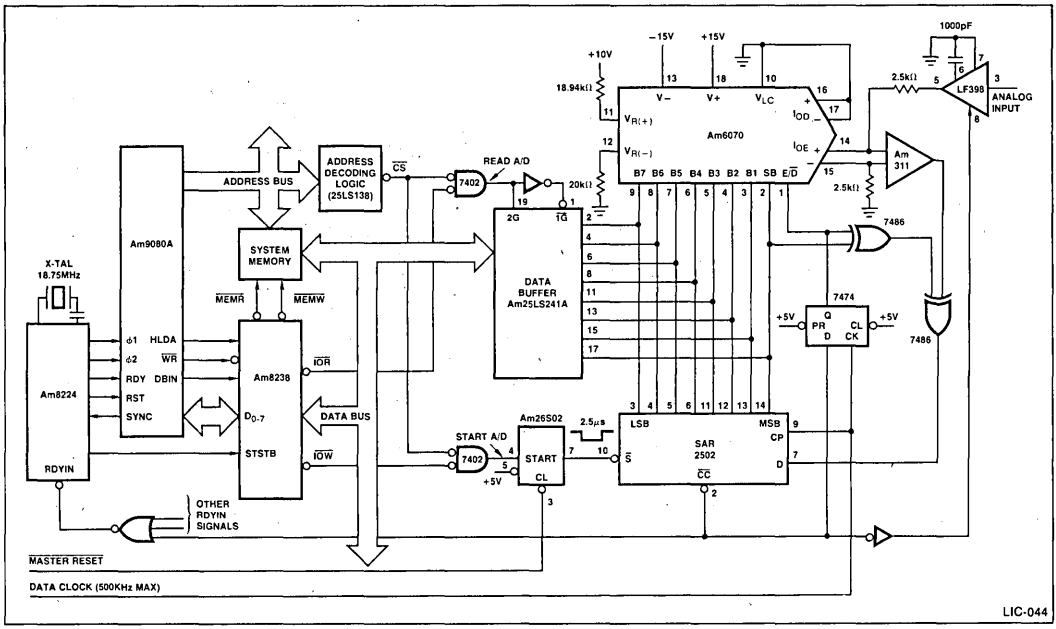


Fig. 24. Microprocessor Controlled Data Acquisition System.

processor's accumulator. A subsequent memory write command, then stores this data in the desired memory location. For the next A to D data conversion, the microprocessor must generate another START A/D signal. An A to D data acquisition can be achieved using only three 9080A instructions.

OUT (to ADC device) −generation of START A/D command
IN (from ADC device) −generation of READ A/D command
STA (to MEMORY) −store digital representation of the acquired analog signal into memory

If the required nine DATA CLOCK periods present a prohibitively long wait state for the processor, the A to D procedure can be more efficiently handled using a suitable interrupt scheme. The logic shown in Figure 25 illustrates the A to D and D to A conversion using three interrupts. The external interrupt signal, VALID RECEIVE DATA, which initializes the A to D conversion, is received and processed by the Am9519 Universal Interrupt Controller. It's output, GINT, is recognized by the 9080A Microprocessor logic and generates the INTA signal at the output of the Am8238. The VALID RECEIVE DATA signal will cause the receive S & H circuit to switch into the hold mode after 5μs, via Am26S02 and associated flip-flop circuitry. This delay is needed to satisfy the sample time requirements for the (Am)LF398 S & H circuit, with C_h = 1000pF. This one-shot circuit may be eliminated if the analog input data is maintained unchanged for about 25μs after recognition of the VALID RECEIVE DATA signal. Upon receipt of an INTA signal, the Am9519 provides the address of an appropriate subroutine to the CPU. This subroutine will initiate the A to D conversion by generating the START A/D command. After A to D conversion is complete, the DATA READY signal, identical to the $\overline{CC}$ signal, generates an interrupt for the 9080A microprocessor to read and store the results of the A to D data conversion via an octal, non-inverting, three-state driver, the Am25LS241A. The $\overline{CC}$ signal at the same time will switch the receiving S & H circuitry into the sample mode. Two sequences of 9080A instructions which perform the acquisition operations described are detailed in Table 10. The corresponding functional flow charts are shown in general form in Figure 26.

The addition of SSI logic shown in Figure 25 generates signals $\overline{CS2}$ and $\overline{CS3}$ which transmit an analog signal generated by the DAC from digital information stored in the system memory. An external interrupt request for transmission of the analog signal, TRANSMISSION REQUEST, will initiate the D to A conversion subroutine. A corresponding word in memory will be fetched into the 9080A accumulator and then latched into the Am25LS374, Octal D type register, via signals $\overline{CS2}$ and $\overline{IOW}$. At the same time, the non-inverting three-state data bus transceivers, Am8T28, will be turned to the direction which corresponds to the D to A conversion procedure. The latch captures valid 9080A accumulator data, which will be used as the digital inputs throughout the D to A conversion procedure. The next instruction in sequence will be a command to start sampling the Companding DAC's decode outputs, ($\overline{CS3}$ = 0, $\overline{IOW}$ = 0), which will be already settled. Assuming that one 9080A I/O instruction takes about 5μs at a system clock frequency of 2MHz, the next command in the instruction sequence may generate a signal VALID TRANSMISSION DATA, (CS3 = 0, $\overline{IOR}$ = 0), which will put the transmission S & H circuitry into the hold mode and return the data transceivers, Am8T28, to the direction which corresponds to the A to D conversion procedure. Input data for the Companding DAC is supplied by the SAR circuitry. A sequence of 9080A instructions which could handle the D to A conversion procedure and analog signal transmission through the programming I/O interrupt scheme shown, is presented in Table 10. The corresponding functional flow chart is shown in Figure 26.

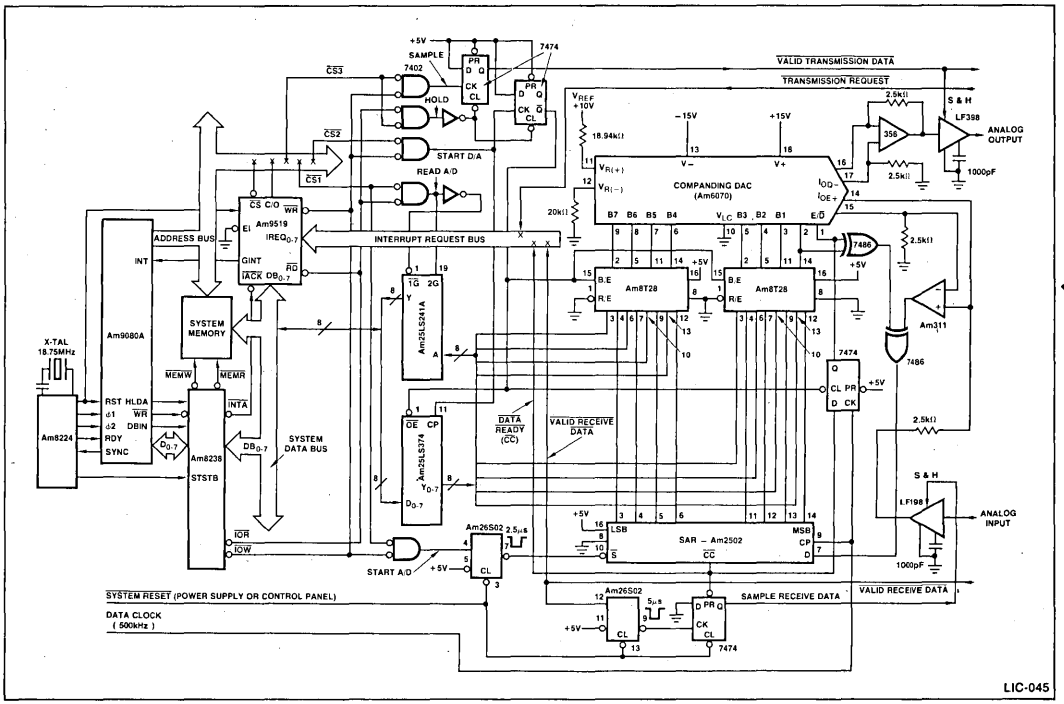


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Fig. 25. Microprocessor Controlled Single Channel Transceiver Converter System.

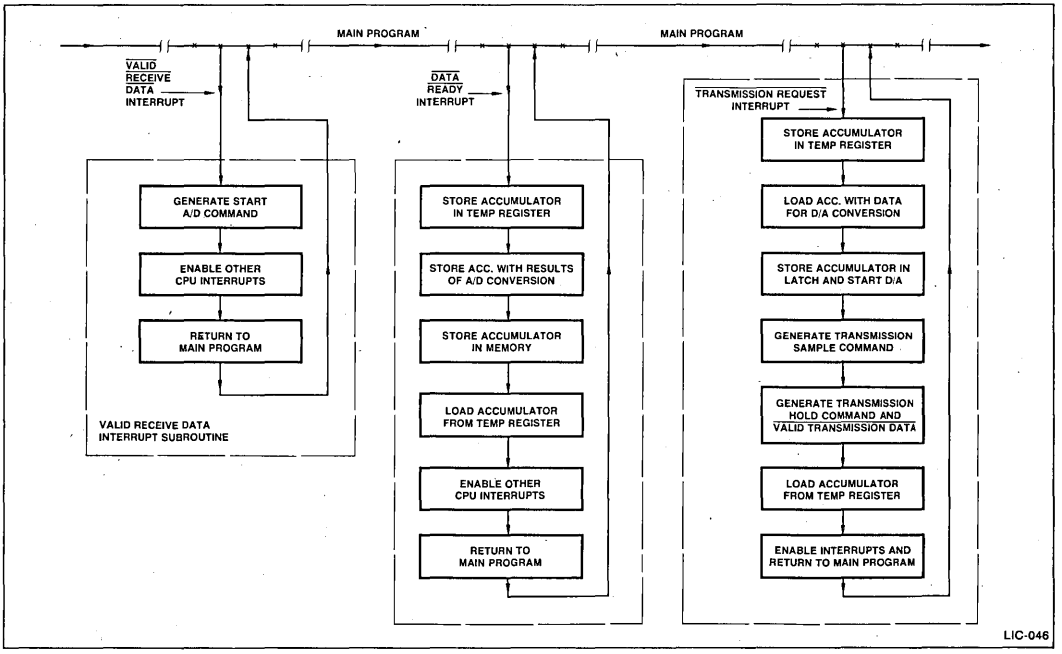

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Fig. 26. Functional Interrupt Subroutine Flow Charts for Data Transceiving Converter.

TABLE 10
INTERRUPT SUBROUTINES FOR SINGLE CHANNEL DATA TRANSCEIVING CONVERTER SYSTEM IMPLEMENTED WITH 9080A INSTRUCTIONS

VALID RECEIVE DATA Interrupt Subroutine:

OUT (to ADC)	– Generate START A/D command.
EI	– Enable other CPU interrupts.
RET	– Return to main program.

DATA READY Interrupt Subroutine:

STA (to TEMP)	– Save accumulator content.
IN (from ADC)	– Read digital results from SAR outputs into accumulator.
STA (to Memory)	– Store accumulator's content into memory.
LDA (from TEMP)	– Restore accumulator's content before subroutine.
EI	– Enable other CPU interrupts.
RET	– Return to main program.

TRANSMISSION REQUEST Interrupt Subroutine:

STA (to TEMP)	– Save Accumulator content.
LDA (from DATA)	– Load accumulator with digital data which will be converted to an analog signal.
OUT (to LATCH)	– Output data for D to A conversion to the latch circuit and START D/A conversion.
OUT (to DAC)	– Generate Transmission SAMPLE command for S & H circuitry, $\overline{CS3} = 0$, $\overline{IOW} = 0$.
IN (from DAC)	– Generate Transmission HOLD command for S & H circuitry, and $\overline{\text{VALID TRANSMISSION DATA}}$ signal.
LDA (from TEMP)	– Restore accumulator's content before interrupt subroutine.
EI	– Enable other CPU interrupts.
RET	– Return to main program.

Motion Control Systems Applications

The high resolution and accuracy of the Companding DAC transfer function for small output signal levels provide a very smooth and precise analog control signal to devices whose outputs are voltage or current dependent. However, when major disturbances are detected in the system, the Companding DAC will produce correspondingly larger control analog signals which cause very fast output response of the controlled analog device. Figure 27 shows the Companding DAC used in a feedback loop to provide a small analog error signal to control the speed and direction of a voltage controlled motor in order to properly position the shaft. The shaft encoder generates an 8-bit digital word which represents the current shaft position of the motor.

There are 256 discrete positions of the shaft which can be identified at the shaft encoder's output. This output will be sampled and latched using an 8-bit register, Am25LS273. The sampling rate is determined by dividing the time for one shaft revolution at the motor's highest speed by 256. The maximum rate will be limited by propagation delays through the comparator and ALU chips and by the settling time of the Companding DAC. The output of the shaft position sampling register, data "B", is digitally compared with the desired shaft position, data "A". The magnitude of the difference between digital words "A" and "B" is directly porportional to the error of the motor shaft position. The sign of this digital subtraction provides information about the polarity of the analog error signal which drives the motor in the direction necessary to decrease the error. The speed of the motor is proportional to the magnitude of the error $|A-B|$. The sign and magnitude of the error are determined by two comparator chips, (Am9324 Four-Bit Comparator), and two ALU chips, (Am25LS381

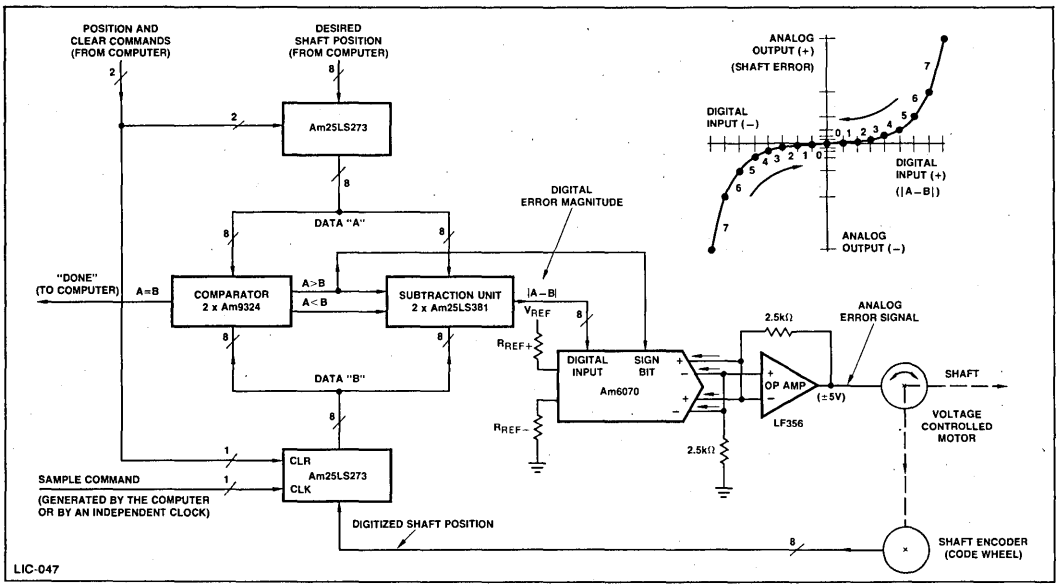


Figure 27. Nonlinear, Computer Controlled, Digital-to-Shaft-Position Conversion System.

Four-Bit Arithmetic Logic Unit). The end of the motor shaft correction procedure is indicated to the computer via the comparator's output "A=B".

The eight digital bits of the error magnitude |A−B| are applied to the seven data inputs of the Am6070 and to the E/$\overline{D}$ input. The Am6070 outputs are connected to provide 32 steps per chord, which totals 256 steps or a 78dB output dynamic range. The smallest and largest step sizes are 0.25μA and 32μA, respectively. The sign bit value is taken from the "A>B" output of the comparator circuit, and determines the polarity of the op-amp, (Am)LF356, output voltage.

The computer function in Figure 27 is mainly confined to initializing the shaft correction procedure by latching the desired shaft position, data "A". Clear commands may be issued during the power-up procedure in order to bring the motor shaft to some initial position. The application of the Companding DAC with its nonlinear transfer characteristic and its nonuniform step sizes which are proportional to the magnitude of the error, |A−B|, significantly reduces system transient response effects such as over-shoots and ringing while minimizing the time required to reach the new shaft position. The system can be programmed to be either critically damped (minimum response time) or under damped (no overshoot).

Figure 28 shows a Companding DAC in a feedback loop which provides small analog error signals for control of the velocity of a voltage controlled motor. This is a paper cutting control system where paper is unwound from a feed roll and cut to size by a mechanical knife. In this application the Companding DAC is in the velocity feedback path and its output is used to generate a velocity profile command signal. The motor rotation is initiated from a front panel by depressing the START button. A COUNT-UP command from a microprocessor sets the binary counter to its count up mode, which drives the Companding DAC inputs. When some predetermined number of counts has been reached, the counter stops and the Companding DAC is held at a constant output value. The incremental encoder produces pulse counts proportional

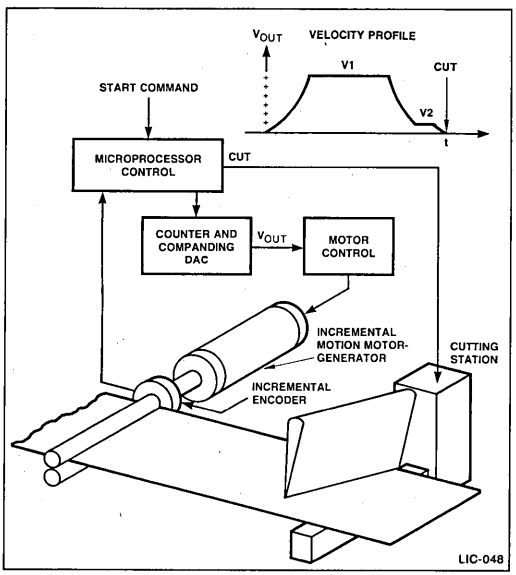


Fig. 28. Paper Cutting Control System.

to the distance of paper travel. The desired paper size expressed as a number of incremental encoder pulse counts is stored in a CPU storage register. The outputs of the incremental encoder are constantly accumulated in an internal CPU counter and are compared with the content of the CPU storage register throughout the entire velocity control procedure. When a match is found, the corresponding COUNT DOWN command is issued to the counter, the internal counter is cleared, and a new value is loaded into the internal storage register.

The values which control the velocity of the motor are stored in a register, external to the CPU, and its content is compared with the outputs of a binary up/down counter during the motor's acceleration and deceleration phases. Whenever a match is achieved, an interrupt signal will be generated and the working mode of the external counter changes. The final stop position is approached in a well controlled manner which stops the paper and cuts it with a minimum of overshoot and error.

Figure 29 shows the necessary logic for generation of the velocity profile control signal. The CPU will first load the external storage register, Am25LS273, via the LOAD signal, to the desired count-up value for the external up/down counter, Am25LS193. Upon recognition of the START request, the CPU issues the COUNT-UP command which enables the 8-bit comparator chip, Am25LS2521. The zero initial digital code at the Companding DAC inputs produces zero voltage at the output, V_{OUT}. Every enabled conversion clock pulse will increase the Companding DAC output current by a corresponding amount, and the V_{OUT} increases in accordance with the Companding DAC transfer characteristic. This portion of the velocity profile control signal corresponds to the motor acceleration phase. When the counter outputs match the content of the external storage register, the interrupt signal $\overline{INT1}$ is generated, and the UP flip-flop is reset.

This stops the up/down counter and the motor continues to rotate with a constant velocity, V1. Duration of the acceleration phase depends on the value initially stored in the external storage register and the frequency of the conversion clock. Upon recognition of the $\overline{INT1}$ signal, the CPU will load a new value into the external storage register, which is used to decelerate the motor from velocity V1 to a lower velocity, V2.

During the constant velocity phase, V1, the encoder pulses accumulate in the CPU counter until the value "m", stored in the CPU internal storage register, is reached. At this time the CPU will issue a COUNT DOWN command and reload the internal storage register with the value "n". The sum of these two values, m+n, should represent the length of the paper expressed in encoder pulses. This value is "p" pulses shorter than the desired ideal paper length.

The COUNT DOWN command initiates the count-down mode of the external up/down counter, PHASE I, and enables the comparator. When the counter outputs match the value stored in the external storage register, the interrupt signal $\overline{INT2}$ is generated and counting stops. The motor continues to rotate with some constant velocity, V2, which is significantly smaller than velocity V1. This velocity, V2, is a function of the conversion clock frequency and the motor's mechanical parameters such as inertia, weight, etc. The mechanical parameters may cause synchronization difficulties between the second deceleration phase of the voltage waveform at V_{OUT} and the actual velocity of the motor. The velocity V2 is much smaller than V1 and allows a smooth, well controlled stop of the motor at the end of the PHASE II of count-down mode, and thus ensures the smallest possible overshoot and error.

Companding DAC

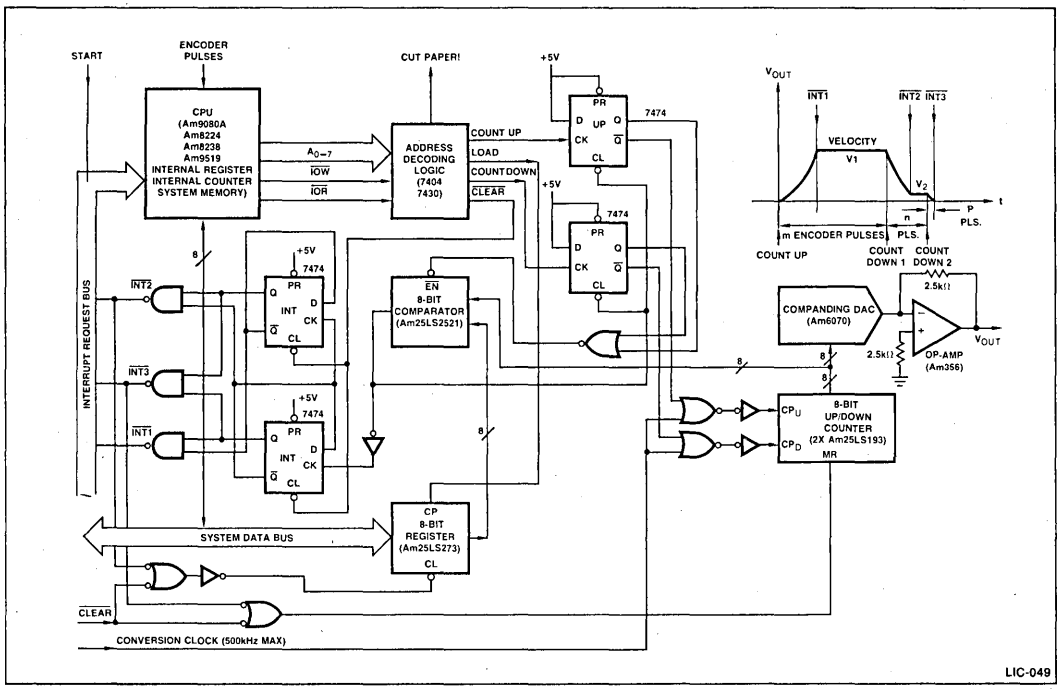


Fig. 29. Microprocessor Controlled Generation of Motor Velocity Control Signal.

The INT2 signal automatically clears the external storage register to all zeros and informs the CPU that the deceleration PHASE I is complete. The CPU continues, internally, to accumulate the encoder pulses until their number becomes "n". At this time the CPU issues a new COUNT DOWN command to initiate PHASE II of the count-down mode, and reloads the internal storage register with a final number "p". This number, when summed with the previous two numbers "m" and "n", determines the final length of paper, m+n+p, and is accumulated in the internal CPU counter during PHASE II of counter's count-down mode. At the end of this phase, the $\overline{INT3}$ signal is generated and counting stops. The number of encoder pulses in the internal counter will be compared with the number "p" stored in the internal storage register. If a satisfactory match is found, the CPU issues a CUT command to the paper cutting station and the paper is cut to the desired size. Finally, the CPU issues the CLEAR command to initialize the INT flip-flops and clear the internal counter. It also reloads both internal and external storage registers with appropriate values, so that a new velocity profile control signal can be generated. Much of the logic shown could be implemented in software, but this would require that much of the microprocessor resources be dedicated to this speed control function.

Audio System Applications

Audio system equipment applications require signal converters which can process bipolar analog audio signals within a ±10V range. A DAC, in an audio system, provides digital gain and/or attenuation of input audio signals. This requires a multiplying DAC, i.e., it must accept an audio signal either in single ended or differential form, and process it as a function of the digital control inputs. Ideally, an audio level control device provides an equal change, in dB, of relative signal level between any two adjacent digital codes or steps throughout its entire output dynamic range. However, differences between steps which exceed 1dB can be annoying to the human ear. For high quality audio systems, the DAC must have low signal distortion, (on the order 0.05% or less over most of the dynamic range), large working dynamic range, (80dB or more), wide bandwidth, large signal to noise ratio, S/N, (80dB or more), and transient-free output gain-change operation which is independent of digital input states.

The Companding DAC with its multiplying feature and its ability to extend its dynamic range up to 78dB, satisfies or exceeds most of these requirements. It handles audio input signals up to ±10V, and its output signal distortion is 0.02% or less over most of the audio signal range. Its nominal level/step resolution is 0.15dB, and its S/N ratio is 80dB or better when referred to a 1V output. However, its total useful audio dynamic range, with a maximum 1dB difference between two adjacent steps, is only 59dB, and its output exhibits DC gain step transient effects, due to the required DC bias current.

The Companding DAC's DC output current potential "click" effects must be suppressed for applications in audio systems where there are large changes in the digital input code. Figure 30 shows the connection for the necessary DC output current compensation. The output dynamic range can be adjusted by varying the value of resistor R2. To suppress the DC step transients, the current I_2 compensates for all DC changes in current I_1. The I_3 current reflects only the AC changes in current I_1 and the current through resistor R2 due to changes in the V_{IN} signal. This allows the attenuated V_{IN} signal to be DC coupled through op-amp A2. The maximum gain for the circuit is assumed to be unity, (0dB), when all digital inputs are set

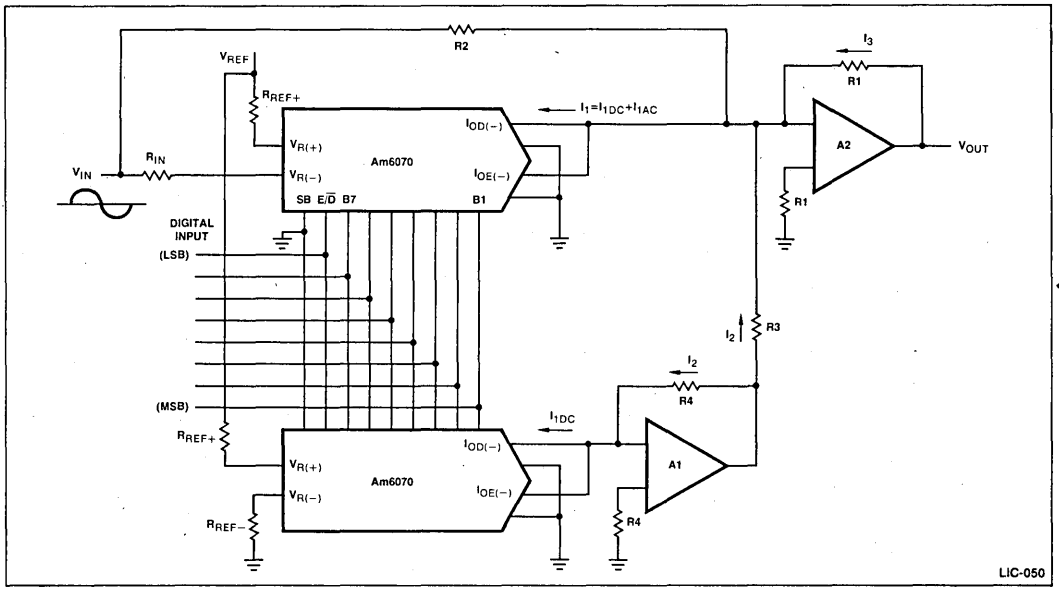


Fig. 30. DC Coupled Digital Attenuator, Adjustable Range.

at logic 1. A determination of the resistor values R_{REF+}, R1 and R2, was discussed in the section on the AC coupled digital attenuator. The R_{REF-} value should be identical to R_{REF+} value and the R3 and R4 values must be equal, so that the current, I_2, will compensate for the DC component of I_1.

The 1dB audio resolution requirement truncates approximately 19dB from the Companding DAC's total dynamic range of 78dB. The level ratio becomes greater than 1dB between the 9th and 8th step of chord 0, (0.25μA/step). If the 1dB resolution criterion is applied to a comparable sign-plus-13 bit linear DAC, the corresponding 1dB requirement also takes off 19dB, and the breakpoint occurs between the 9th and 8th step of the linear 13-bit DAC transfer characteristic. The subtle difference between the 13-bit linear DAC and the sign-plus-8 bit Companding DAC lies in the distribution of the dB ratio values within the steps of the 59dB workable audio dynamic range. For a linearly scaled 13-bit linear DAC, the level ratios in dB among the steps close to the full scale current are very small. The ratios increase as the step numbers decrease toward zero. On the other hand, the sign-plus-8 bit Companding DAC maintains a near constant 0.15dB between steps over the entire dynamic range, with the exception of steps in chord 0.

The 59dB working dynamic range is not wide enough for high quality audio systems which require an 80dB audio control range. To satisfy this requirement, two DACs can be cascaded with their digital inputs driven in parallel. The total dynamic range is now increased to 156dB and the working range, (1dB/step or less), is now approximately 106dB. A cascading scheme for Companding DACs, which also provides for DC transient-free operation, is shown in Figure 31. The advantage of the cascaded Companding DAC's scheme over a similar cascaded linear DAC's scheme is in the number of control bits required to achieve the 106dB range and in the 0.3dB/step uniform attenuation distribution over most of the 106dB range. The audio signal, V_{IN}, is shown in Figure 31 as a single input.

All three Companding DACs in Figure 31 have their SB inputs tied to logic 1. The reference currents for all three DACs should be maintained at positive values throughout the attenuation procedure by proper selection of the input resistor, $R_{IN} = V_{IN}/I_{IN}$, where $I_{IN} < I_{REF}$. In Figure 31, the maximum I_{IN} value is equal to one half of the DC reference current, and the maximum value of V_{IN} is only limited by the output voltage swings of operational amplifiers A2 and A3. The DC transient effects in the cascaded DACs are compensated for by using a Companding DAC followed by the A1 op-amp. The DC compensation circuitry is completely isolated and independent of the AC effects of the applied audio signal V_{IN}, and the only critical requirement is matching R_1 and $R_{REF(+)}$. The step sizes in all chords should be matched for all three Companding DACs. For audio signals with amplitudes not more negative than $-5V$, (Companding DAC's maximum negative output voltage is $-5V$), the A1 op-amp can be eliminated, and the positive inputs of the A2 and A3 op-amps can be driven by the DC compensating DAC directly.

Companding DACs, with their logarithmic transfer function, are natural generators for the attack and decay analog signal waveforms used in electronic organs and musical synthesizers. A waveform's attack, sustain, and decay times, together with additional harmonic content information, determine the sounds of a particular musical instrument. For example, woodwinds have very short attack and decay times. The circuit shown in Figure 32 generates trapezoidal-like waveforms with exponential rise and fall times under the control of an 8-bit microprocessor, Am9080A. Digital inputs are supplied by two pairs of 4-bit binary counters, Am25LS191, which are set to the Count Down mode. All of the counters are simultaneously loaded by the LOAD command which is decoded from the microprocessor's

Companding DAC

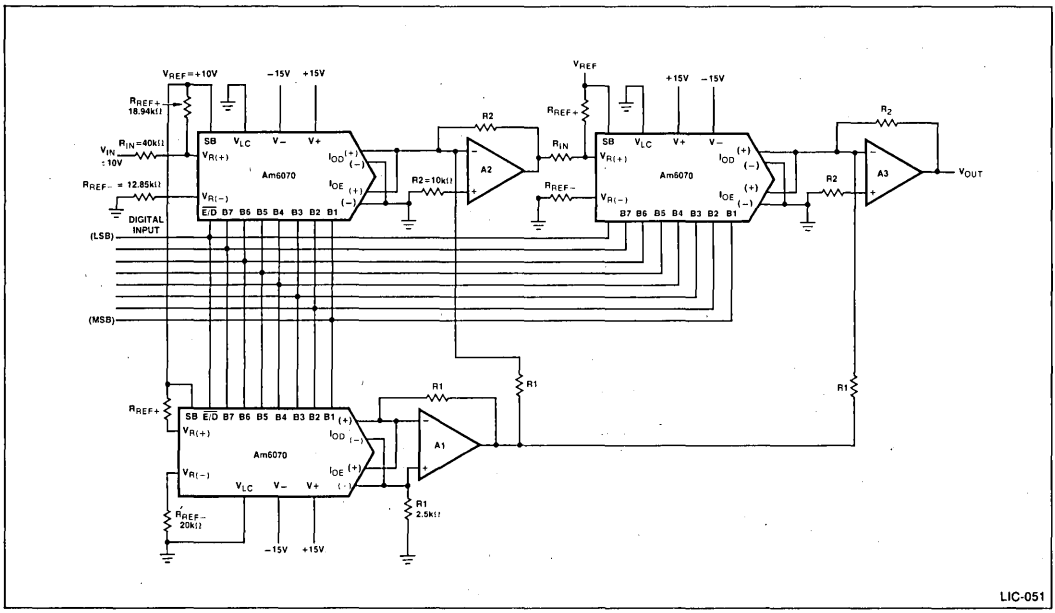


Fig. 31. DC Coupled Cascaded Digital Attenuator.

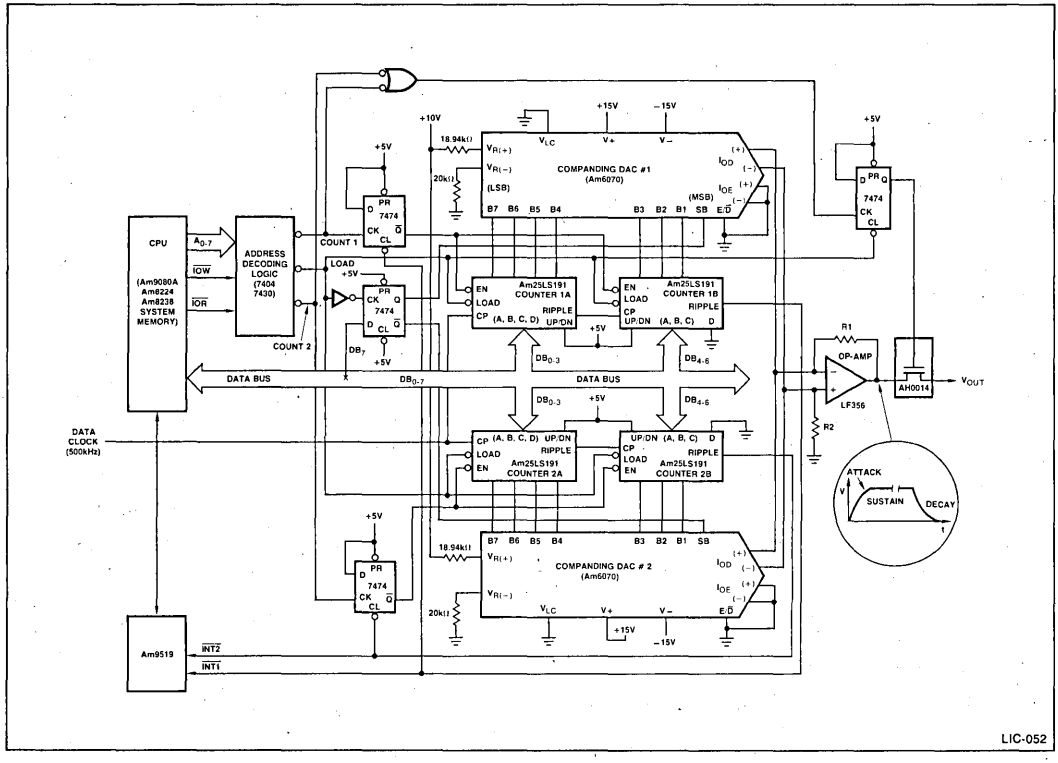


Fig. 32. Microprocessor Controlled Waveform Generator, Attack, Sustain and Decay Signal Waveforms.

address signal combination. Companding DACs 1 and 2 are in the decode mode. The SB inputs are determined by the most significant data bit, DB7, which is stored in the flip-flop during counter loading. The Companding DACs' decode outputs which have the same polarity are tied together and fed into an LF356 operational amplifier. After the settling time required for the Companding DAC's outputs, the currents at the op-amp's inputs should be equal, and its output, V_{OUT}, should be 0V. A command COUNT #1 closes the analog switch, AH0014, and enables counters 1A and 1B via their ENABLE inputs. The 500kHz clock frequency allows sufficient settling time for the Companding DAC's outputs. The initial rise of the op-amp output voltage, V_{OUT}, depends on the number initially stored in the counters, i.e., it depends on the starting point of the Companding DAC transfer characteristic. When Counter #1 reaches zero, the $\overline{INT1}$ signal indicates underflow, further counting stops, and the microprocessor is informed about the end of Counter #1 operation. After a certain sustain time, which can be preprogrammed, the microprocessor issues the COUNT #2 command and the V_{OUT} waveform starts its decay portion. The time duration of the Attack and Decay slopes generated by the logic in Figure 32 are equal and is specified by the starting count in Counters #1 and #2.

Note that the microprocessor can control the counting functions and the external counter could be replaced with simple, octal data latches. With the increased use of digital techniques and microprocessors for control functions in complex audio systems, microprocessor controlled analog waveforms, similar to those generated by the logic in Figure 32, may become very desirable and attractive tools for the generation of various audio effects. However, it is important to remember that the output from the Companding DAC consists of discrete, non-uniform steps and is not continuous. To obtain a real, continuous signal from the output, some filtering or integration may be required.

Telecommunication System Applications

Digital PCM transmission systems compress analog speech signals into a train of 8 digital bits for each sample. They transmit this information and then decode and expand it back into analog signals. The Companding DAC represents a monolithic solution for most requirements of the PCM encoding and decoding procedures. This device replaces a considerable number of discrete and hybrid components in existing PCM transmission schemes. At the same time, the Companding DAC provides increased signal-to-noise ratio in the system, reduces system signal distortions and stimulates further development and wider usage of digital channel switching techniques.

Currently, most transmission systems in the United States follow the Bell D3 communication channel bank specifications, where each channel bank consists of 24 voice channels and the necessary transmission equipment. The entire signal sampling, encoding and multiplexing procedure in the 24 channel bank system must be performed within 125μs. The PCM channel time slot distribution, within a one 125μs time frame, is shown in Figure 33. Each slot contains an 8-bit digital representation of a particular signal sampled from a corresponding voice channel. The total number of bits in the D3 channel bank time frame is calculated as follows: (24 channels x 8 bit/channel)+ 1 signalling bit = 193 bits. The additional single bit is used to identify the beginning of a frame, and data is transmitted at 1.544MHz (193 bits/samples x 8000 samples/sec). In addition, in every sixth frame the

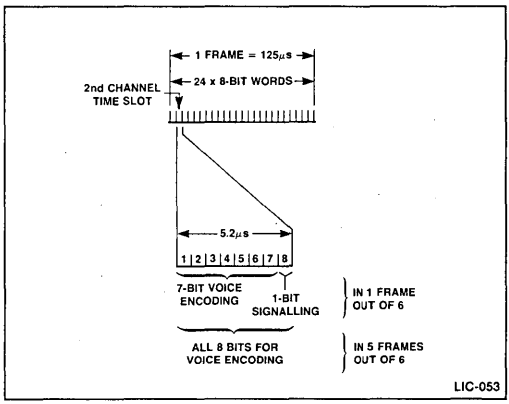


Fig. 33. PCM Channel Timing Frame Format.

least significant bit in each channel slot is used for communication signalling purposes. Consequently, the signal samples in every sixth frame are represented with only 7 digital bits. The increase in signal distortions in this time frame is slight and is not considered significant for PCM voice transmission performance. When the Companding DAC is used as a simple decoder at the receiving side of a system, the connection shown in Figure 19 can be used to minimize distortion caused by the absence of the least significant bit, B7, during these signalling frames. When the signalling frame is recognized, the Companding DAC output is increased by a half step from its corresponding decode output value by switching the E/$\overline{D}$ input from a logic 0 level to a logic 1. However, the European systems, using A-law devices, have 32 channels per bank where the 2 channels are used for signalling information. Each frame requires 256 (32 x 8) bits. The corresponding data transmission rate is 2.048MHz (256 bits/sample x 8000 sample/sec).

In a two-way PCM communication system, a single Companding DAC can perform the time shared encoder and decoder functions known as the CODEC function. The logic state of the E/$\overline{D}$ input determines the operating mode of the Companding DAC and switches the output current to the appropriate outputs. The Companding DAC digital inputs during the encode operation are generated by the successive approximation procedure. In the decode mode, the eight digital inputs are supplied from an external source, either in serial or parallel. The basic diagram for a typical CODEC is shown in Figure 34.

The logic in Figure 34 provides automatic handling of the E/$\overline{D}$ signal levels during the CODEC's XMT mode of operation. The first task of the system is to initialize the SAR circuit by proper manipulation of the $\overline{START}$ input for the successive approximation procedure. The XMT COMMAND should be synchronized with the low-to-high transition of the $\overline{START}$ pulse, and its level must be held at logic 1 for the next 8 CLOCK pulses to keep the three-state XMT buffer, 74126, in the low impedance state. During the A to D conversion period, a serial train of 8 digital bits, which represent the sample at the TRANSMIT ANALOG INPUT in Figure 34, appears on the XMT DATA line. XMT and $\overline{RECEIVE}$ commands are mutually exclusive.

The CODEC in Figure 34 is set to the receive mode of operation by setting the $\overline{RECEIVE}$ command signal to a logic

Companding DAC

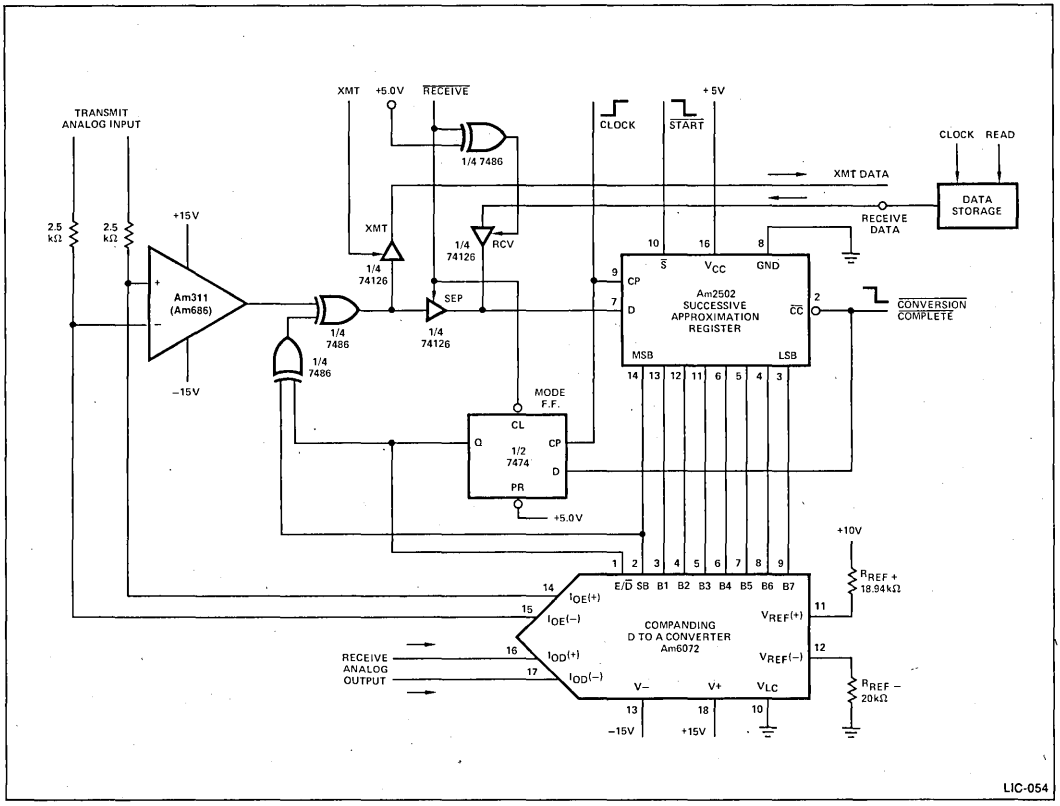


Fig. 34. PCM Encoder/Decoder or Transceiving Converter.

0 level after the $\overline{\text{START}}$ pulse returns to its positive level. A serial data source, DATA STORAGE, supplies a digital train of 8 bits to the serial input D of the SAR circuit via the three-state buffer, RCV, 74126. At the same time, the $\overline{\text{RECEIVE}}$ command signal level keeps the exclusive-or gate output separated from the same SAR's serial D input via another three-state buffer, SEP. The same command also keeps the E/$\overline{\text{D}}$ input of the Companding DAC at logic 0 throughout the entire D to A procedure via the MODE flip-flop in the successive approximation logic. In this CODEC's receive mode, the SAR circuit acts as a serial-to-parallel shift register for the incoming data on the RECEIVE DATA line. After the 8 clock pulses, the outputs of the SAR are ready for the D to A conversion. An analog current representation of the RECEIVE DATA train appears at the RECEIVE ANALOG OUTPUT, after an appropriate settling time. During this time the SAR outputs must remain unchanged and the START signal must remain at logic 1. The $\overline{\text{RECEIVE}}$ command signal must be held at logic 0 for the entire D to A conversion time which includes the Companding DAC's settling time. The CODEC must sample the analog input prior to each A/D conversion. During this sampling period the analog input signal will be changing and the Companding DAC cannot be used to encode this signal. The total encoding time must include the sampling time and the A/D conversion time. If the sampling time period is greater than the time required for the decoding procedure, the Companding DAC can be used as a decoder during this time period and thus, the decoding operation will not require any additional system time.

The CODEC operations in PCM communication systems can be performed on a single channel or on multiple channels in a multiplexed channel switching scheme. The final number of multiplexed channels which can be served by a single Companding DAC with a data sampling rate of 8kHz is limited by the CODEC's sampling and settling times.

Two examples of a single channel PCM CODEC are shown in Figure 35 and 36. The major difference is in the structure of the XMT and RECEIVE data bus. The parallel data I/O CODEC in Figure 35 transmits and receives digital data in parallel form. The parallel data CODEC contains data bus transceivers, (Am)8T26, for handling data in communications systems which might be controlled by one of the popular 8-bit microprocessors. A parallel data I/O CODEC has a considerably shorter D to A conversion time than a serial I/O CODEC.

The circuits shown in Figures 35 and 36 are controlled asynchronously with START, XMT, RECEIVE and their corresponding SAMPLE COMMANDS, which are generated and supplied externally by a communication system. The CLOCK signal is also externally supplied, and in the case of a serial data I/O CODEC, it must be synchronized with the incoming

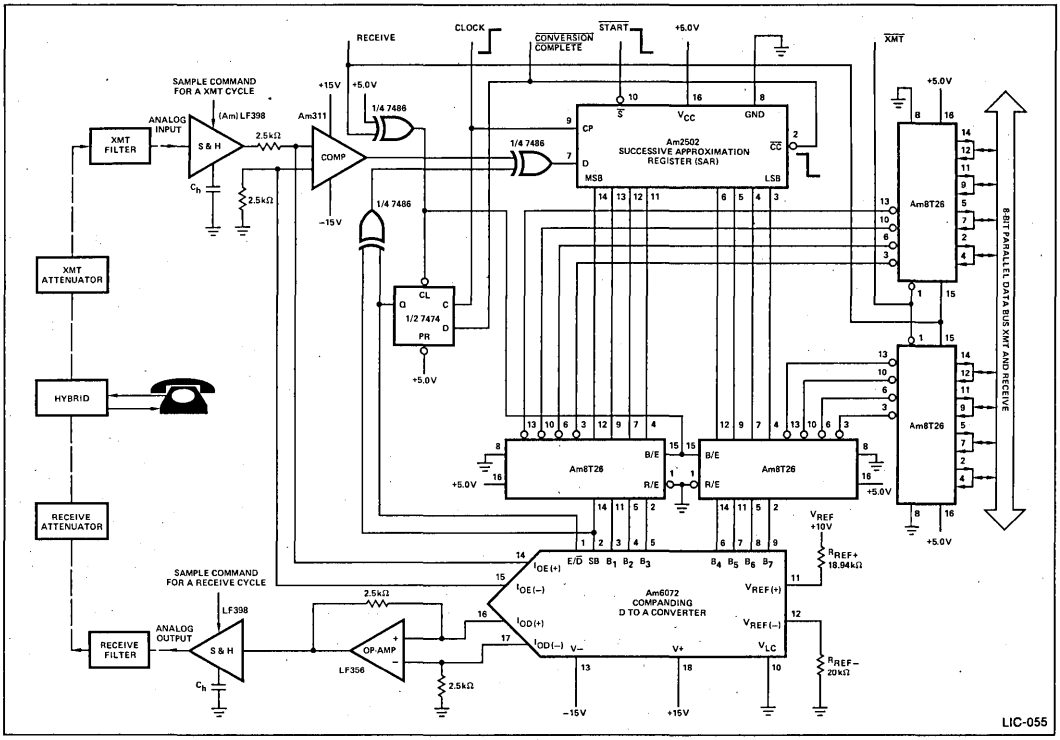


Fig. 35. Single Channel PCM Codec Parallel Data I/O.

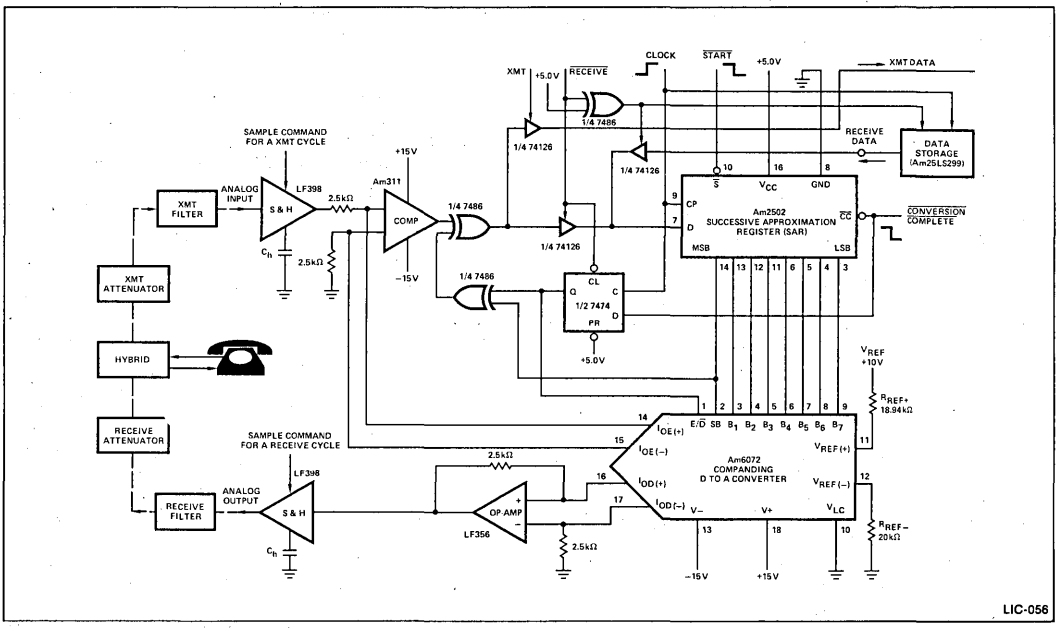


Fig. 36. Single Channel PCM Codec Serial Data I/O.

and outgoing serial data train. The CODEC's only output control signal, CONVERSION COMPLETE, $\overline{CC}$, provides the external communication system with information necessary to generate a XMT signal during the encoding procedure. XMT and RECEIVE commands are mutually exclusive. The transmit and receive data transfers can be performed either alternately or simultaneously. In the latter case the external communication system must employ separate transmit and receive data buses. In addition, storage devices external to the CODEC logic must be provided for the receive data. The code assignment for outgoing or incoming parallel data provides uncomplemented binary values for sign and magnitude. The DAC data bus, as a result, yields "high zeros" density for small output signal amplitudes.

To perform a transmit operation cycle, the START pulse must be held low for one clock cycle. Data conversion for a transmit operation is completed in 9 clock cycles, where the ninth cycle initializes the SAR for the next successive approximation procedure.

The RECEIVE operation in parallel data I/O CODEC is performed without using SAR logic, and the corresponding D to A data conversion does not require a CLOCK signal. Duration of the RECEIVE command signal must accommodate the Companding DAC's settling time, plus the sampling time ($\approx 5\mu s$) required by the S & H circuit, used at the CODEC's analog output. The typical settling time for the worst case input code transition from all ones to all zeros is about $4\mu s$. The receiving data must not change during this time. A XMT command must be issued after a high-to-low transition of the $\overline{CC}$ signal, and its duration depends on the time required by the external system logic to sample the correct content from the 8-bit parallel data bus. A sample command pulse for a transmit operation can coincide with the START pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Companding DAC's settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.

In the serial CODEC the duration of XMT and RECEIVE command signals must similarly accommodate all signal propagation delays, as well as the settling and sampling times, necessary for conversion of an outgoing or an incoming series of 8 digital bits. During the receive operation, the SAR is acting as a serial-in to parallel-out shift register for data supplied from an external serial source. Shifting data into the SAR requires 9 clock pulses. A sample command pulse for a transmit cycle must be issued before an XMT command signal; its duration depends on the S & H sampling time used at the CODEC analog input. A sample command pulse for a receive cycle must be delayed by a time equal to the Companding DAC's settling time after a high-to-low transition of the $\overline{CC}$ signal occurs. The data transmission rate at the receive line is limited only by the shifting speed of the SAR which is rated at 15MHz. The data transmission rate at the serial CODEC's data XMT line is limited by the settling time of the Companding DAC and propagation delays through the comparator, exclusive-or, buffer (74126), and SAR devices.

In a one-way PCM communication system the Companding DAC can be used as the decoder at the receiver end of a system or as a part of the encoder at the transmission end of a system. The transmission data bit rate for 24 communication channels sampled at 8kHz is 1.544 megabits/sec. This transmission rate allocates $0.64\mu s$ for each of 193 bits within a $125\mu s$ long 24-channel time frame. A 24-channel PCM decoder which is capable of handling this transmission bit rate is shown in Figure 37. This schematic does not show the logic necessary for recognition of frame and signalling bits. To handle a single bit in $0.64\mu s$ the total signal propagation time through the 8-bit D-type register, Am25LS273, the Companding DAC, Am6072, and the op-amp must not exceed 8 x $0.64\mu s = 5.12\mu s$. This corresponds to the total shifting time of 8 bits through the serial-in, parallel-out, shift register, Am25LS164. The most critical propagation delay is caused by Companding DAC's worst case settling time which corresponds to the worst possible input transition of 1111111 to 0000000, which can occur during D to A conversion. If $4\mu s$ are taken for the worst case settling times of the DAC and op-amp, only $1.12\mu s$ are left to be distributed to all other time delays in the system. The 4-bit counter, Am25LS161, and 8-bit shift register, Am25LS164, are synchronized with the system supplied data clock at 1.544MHz. The additional logic in Figure 37 consists of analog switches AH0014 and AM9712, and the corresponding SSI control logic. This switching scheme provides a minimum of crosstalk between output analog channels which may occur due to a possible break-before-make switching problem. The output analog channel hold capacitor values depend a lot on the type of a load at these outputs. The Bell D3 specification specifies system performance down to signal levels of −50dB (00000111 code on the transfer curve). Worst case settling time from full scale to −50dB is about $2.5\mu s$. Decoders in excess of 24 channels, can be built using this settling time but they will have somewhat higher distortion for signal levels below −50dB.

In the PCM encoder schematic shown in Figure 38, the maximum settling time for the Am6072 is assumed to be $1.2\mu s$ for the worst input bit change. The Bell D3 specification can be satisfied using a settling time of $1.2\mu s$, which is the worst case settling time in the successive approximation procedure for signals near −50dB (lowest level on D3 specification). There will be some additional error for very low level signals, but the overall system will meet the D3 specification. The additional logic delay in the feedback path is estimated to be 100ns maximum, and is distributed among the comparator, Am686, the digital 2:1 multiplexer, Am74S258, the exclusive-or circuit, 74LS86, and the SAR, Am2502. This yields $1.3\mu s$ for one successive approximation iteration. Further timing analysis shows that, with no additional delays, 12 channels can be encoded within the $125\mu s$:

$1.3\mu s \cdot 8 \cdot 12 = 10.4\mu s \cdot 12 = 124.8\mu s$
Clock = $1/1.3\mu s = 769.23$kHz

Two methods are used in the schematics in Figure 38, to prevent additional delays. First, a special switching scheme of analog input signals is employed to sample a channel from one group while a channel from the other group is encoded. This sampling scheme saves the time required for sampling of an analog input and provides a solution for encoding a maximum number of channels for the given "one-bit iteration" time. This design uses analog multiplexers, AM9712, and sample and hold circuits, (Am)LF398. The analog multiplexer at the Companding DAC output, AH0014, switches to another comparator during the time allocated for the first bit iteration, when the sign bit of a sample is established and no current flows through I_{OE} outputs. Secondly, a one shot circuit is used to modulate the positive period of the first data clock pulse, after the SAR's $\overline{CC}$ signal is generated. The one shot pulse should split the positive portion of this first clock pulse into

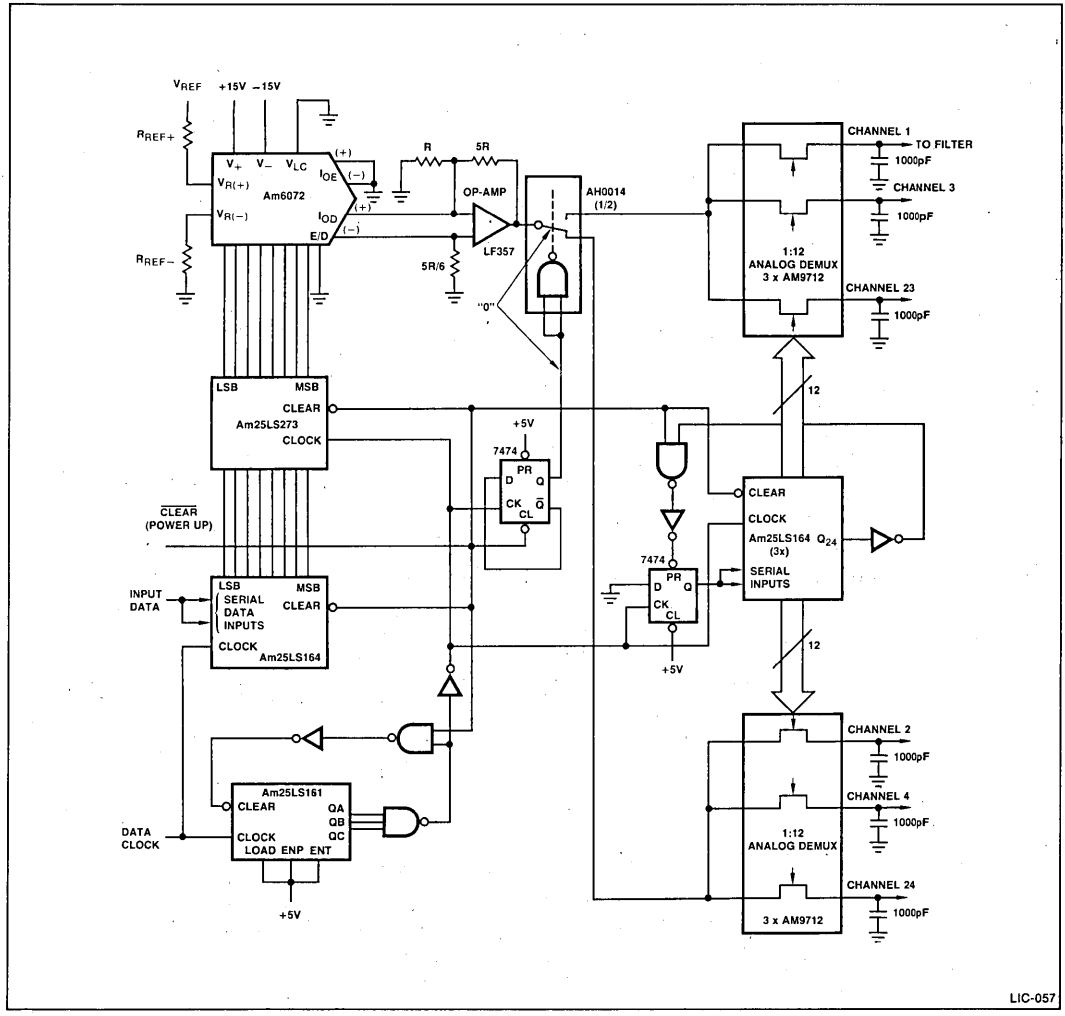
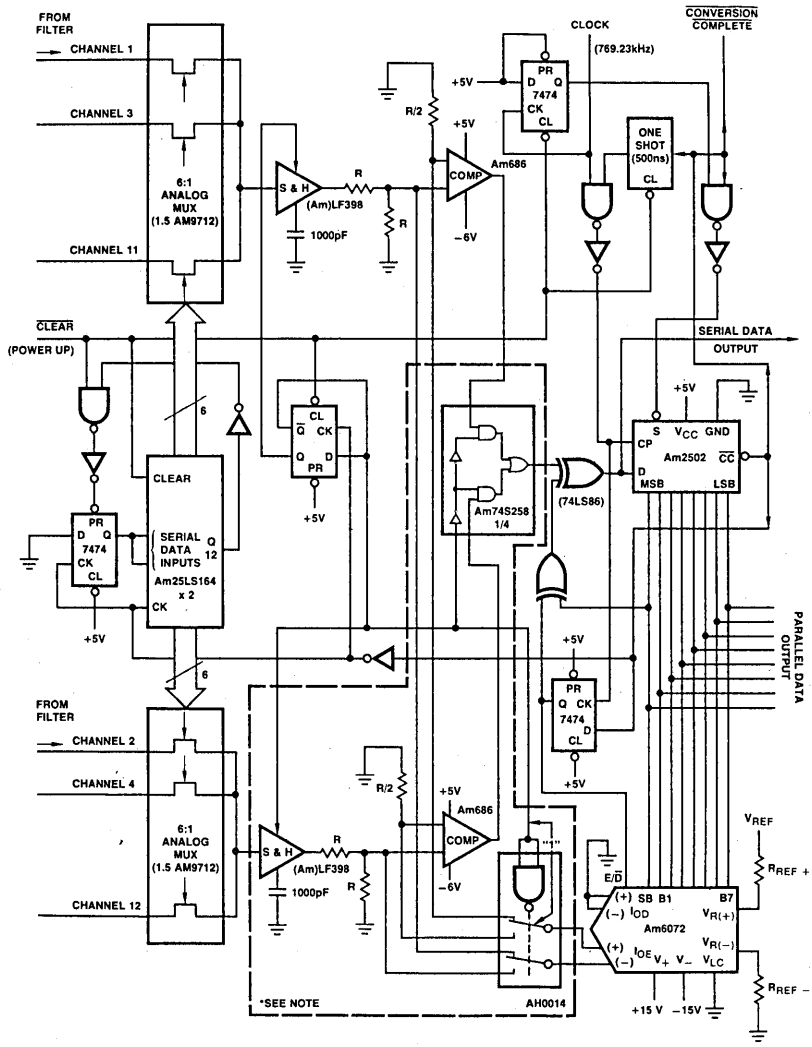


Fig. 37. 24-Channel PCM Decoder.

two positive pulses, and the positive edge of the second pulse will initialize the SAR and eliminate the need for a ninth pulse. The net effect of this pulse modulation is a reduction of the time available to the SAR for the determination of the sign bit value and reduction of the time available for recording the SAR outputs with the correct least significant bit value. However, the time for sign bit evaluation is 1μs, and the LSB value can be taken from the SAR's serial data input D at the time of conversion completion. The encoding logic in Figure 38 is fully synchronized with the system supplied data clock which is input at a frequency of 769.23kHz. A similar encoding scheme provides encoding of 8 channels within the 125μs time without the circuits which are enclosed by dotted lines in Figure 38. Only one S & H circuit and one comparator can be used, and the AH0014 and 74S258 circuits can be eliminated. This D3 system's 8-channel PCM encoder has 15.6μs for an A/D conversion, which allows 5.2μs for the analog multiplexer, (AM9712), and S & H, (LF398), to switch and settle prior to the actual A/D conversion which takes 10.4μs.

One multiplexed CODEC using a single Companding DAC is shown in Figure 39. The CODEC's entire activity is synchronized with a data clock which drives the RECEIVING REGISTER, Am25LS22 (8-bit Serial/Parallel Register), the SAR, Am2502, and the 4-bit binary counter, Am25LS161. Maximum clock frequency is limited by the delays involved in the encoding path and by the data transfer protocol chosen for the XMT and RECEIVE data lines. Using 1.8μs for the Companding DAC's longest settling time and 150ns for all other propagation delays in the encoding path, the minimum time for eight iterations amounts to 8 x 1.95μs = 15.6μs. The corresponding Data Clock frequency is 512.82kHz. A time frame of 125μs contains eight time-slots of 15.6μs each.

Companding DAC



*Note: Circuits enclosed by a dotted line may be eliminated in an 8-channel encoder for the D3 communication system which uses 5.2 μs for the input switching and sampling times, (Am9712 and LF398), and 10.4μs for one A/D conversion.

LIC-058

Fig. 38. 12-Channel PCM Encoder.

The CODEC in Figure 39 has four multiplexed channels, and uses the data conversion protocol illustrated in Figure 40. This protocol allocates equal time to the encoding and decoding procedures. Although this is not the most economical timing scheme, it significantly simplifies the CODEC's logic. The value of the most significant bit, MSB, of the 4-bit counter controls the switching between the encode and decode functions, and the switching of the input and output analog channels in the analog multiplexers, AM9712, via 1 of 4 decoder circuit, Am25LS2539, (Dual 1 of 4 decoder). During the negative half of the MSB period, the S & H circuit is placed in the hold mode, the DATA CLOCK and the outputs of BUFFER REGISTER, Am25LS373, (Octal Transparent Latch), are enabled and the Companding DAC is placed in the encode mode. At the same time, the RECEIVING REGISTER, Am25LS22, is receiving data with its outputs in the high impedance state. All analog switches, XMT and RECEIVE, are open during this negative portion of the MSB signal.

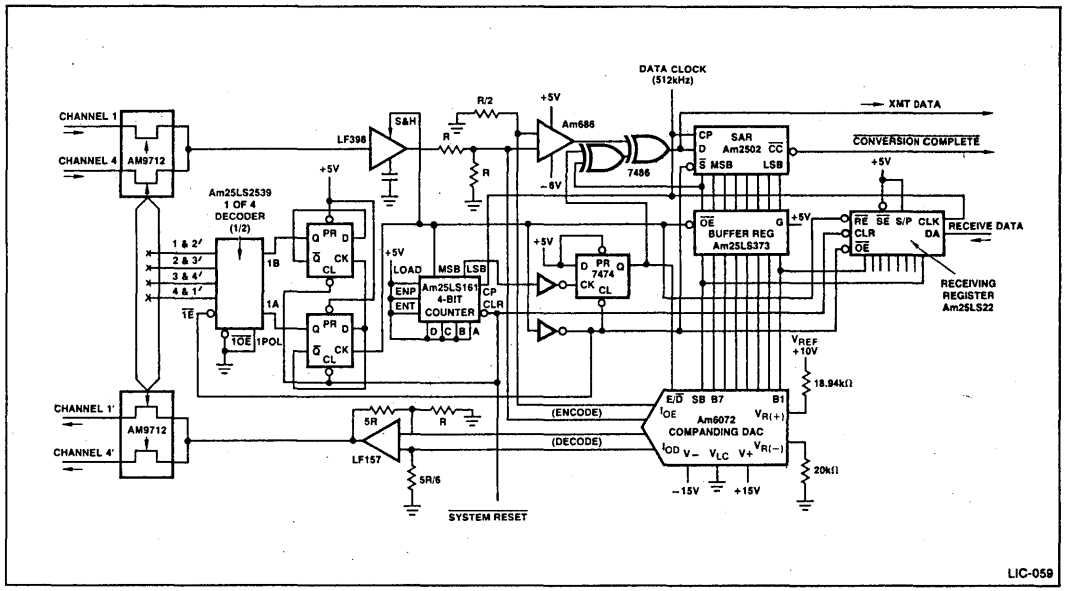


Fig. 39. 4-Channel PCM CODEC with Simultaneous XMT and Receive Data Transfers.

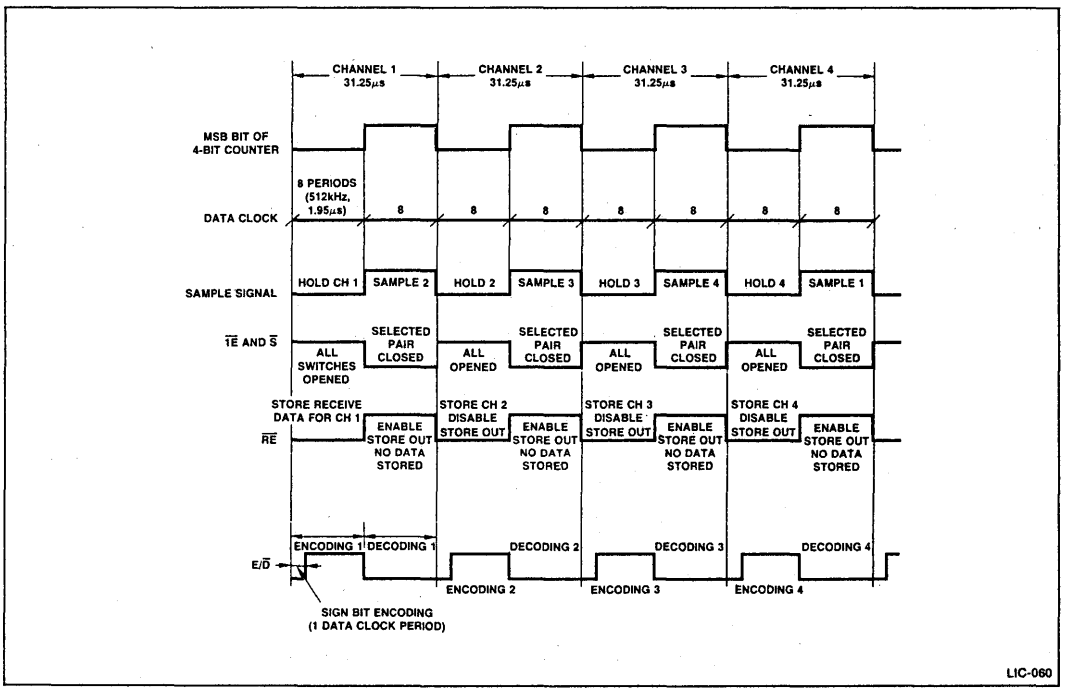


Fig. 40. Ideal Timing Diagrams for 4-Channel PCM CODEC.

Companding DAC

During the positive half of the MSB signal period, data clock inputs to the SAR and RECEIVING REGISTER, and START input to the SAR, are kept at logic 0. The S & H circuit is put into the sample mode, the BUFFER REGISTER is put in the high Z state, the RECEIVING REGISTER outputs are enabled, and the Companding DAC is put into the decode mode. During this positive period, the currently addressed XMT and RECEIVE analog switches are closed. The positive going edge of the MSB signal also updates the address code for the analog switches.

Additional timing analysis reveals that by using different and reduced maximum settling times, for the encode and decode portions of the above described data conversion protocol, the number of multiplexed channels can be significantly increased. However, the necessary logic for control and timing of unequal encode and decode data conversion time periods will be more complex than the logic shown in Figure 39. The same encode/decode alternating timing procedure, with 1.1μs allocated for the A/D settling time, and with only 5.6μs allowed for D to A conversion, (not limited by the DAC), will result in eight multiplexed channels. Systems requiring more than eight channels can be built using multi sample and hold circuits to reduce the input sampling time period. The maximum number of channels, limited by the Companding DAC's settling times, can be further increased by adjusting data clock frequency to its optimal values for each of the successive approximation bit-iterations, repeatedly, for every A/D data conversion.

SUMMARY

The Companding DAC was originally developed for the needs and requirements of PCM communication systems. When used to perform a decoder function, at an 8kHz sampling rate, a single Companding DAC can comfortably serve up to 24 voice channels. As a part of the encoding scheme, the Companding DAC can accommodate 12 D3 communication channels. For implementation in CODEC functions, the Companding DAC is ideal for single channel CODEC schemes. The length of the output current's settling time is the most important parameter to be considered for the Companding DAC's implementation in multiple channel CODEC schemes. An 8 channel CODEC is probably an optimum number of channels which can be served by a single Companding DAC.

The timing restrictions are not of such importance in industrial systems. A logarithmic-like, piece-wise transfer function and the very fine resolution and accuracy of a 12-bit linear DAC which are achievable in the Companding DAC's chord 0, provides industrial systems with a very sensitive tool. In addition, the Companding DAC's compatibility with 8-bit microprocessors offers a very powerful control vehicle in the areas of data acquisition and instrumentation systems. A wide dynamic range of 78dB which can be extended by a cascading scheme to 156dB or more, and a high signal-to-distortion ratio of 80dB, allow usage of the Companding DACs for attenuation functions even in a high fidelity audio system. Industrial applications represent a large potential market for Companding DACs and they should be given serious consideration by industrial system designers.

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Am6606

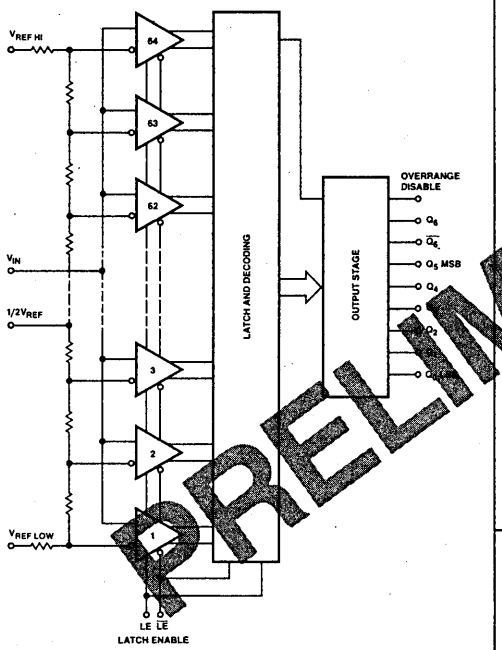
6-Bit 100MHz Quantizer

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- 100MHz sampling rate
- 50MHz full power bandwidth
- 25ps aperture uncertainty time
- 10ns maximum encode delay
- 6-bit resolution, expandable to 8 bits
- 8-bit accuracy
- Large bipolar input voltage range
- ECL output
- Q and $\overline{Q}$ outputs on MSB for two's complement conversion

FUNCTIONAL DIAGRAM



ORDERING INFORMATION*

Order Number	Package	Temperature Range	Maximum Error
Am6606DM-8	Hermetic DIP	−55 to +125°C	±5mV
Am6606DM-7	Hermetic DIP	−55 to +125°C	±10mV
Am6606DM-6	Hermetic DIP	−55 to +125°C	±20mV
Am6606DL-8	Hermetic DIP	−25 to +85°C	±5mV
Am6606DL-7	Hermetic DIP	−25 to +85°C	±10mV
Am6606DL-6	Hermetic DIP	−25 to +85°C	±20mV

*Also available with burn-in processing. To order, add suffix B to the part number.

FUNCTIONAL DESCRIPTION

The Am6606 6-bit quantizer consists of an array of 64 high-speed ECL sampling comparators with master/slave latching, a resistor voltage divider and an ECL compatible binary encoder. It will accurately quantize an analog voltage into 63 equally-spaced levels and send out a 6-bit binary digital word at sampling rates up to 100MHz.

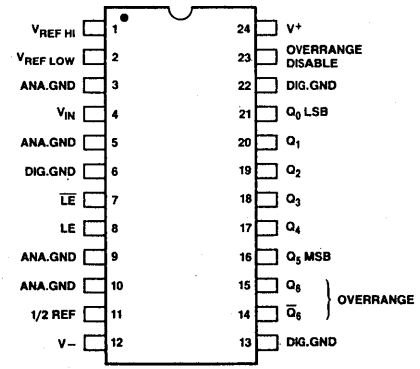
Resolution beyond 6 bits, up to a maximum of 8, may be obtained by stacking quantizers (n bits of resolution requires 2^{n-6} quantizers). An overrange output is provided to indicate that the input signal has exceeded the full-scale limit. An overrange disable input is also provided; when connected to the positive supply, inputs in excess of the full-scale limit will cause bits zero through five to remain at logic ONE instead of resettling to logic ZERO and toggling the overrange bit (Q_6) to a logic ONE. This feature is useful when one Am6606 is used as a stand-alone device, in which an all-zeros output on overrange would be indistinguishable from an all-zeros output caused by a low input signal.

The high-speed latch enable inputs are intended to be driven from the complementary outputs of a standard ECL gate or a high-speed comparator such as the Am685. If LE is driven HIGH and $\overline{LE}$ is driven LOW, the quantizer is in the sample mode and the digital binary output from the device changes as field. When LE is driven LOW and $\overline{LE}$ is driven HIGH, the quantizer changes to the hold mode and the next digital binary output from the new sample is held. No external latches are required if proper attention is paid to the timing of LE and $\overline{LE}$ drive.

The outputs are open emitters, requiring external pull-down resistors of a minimum of 100 ohms to −2V or 330 ohms to −5.2V.

These devices can be used in video data conversion and time base correction, radar signal processing, nuclear pulse height analysis and other systems requiring very high-speed analog-to-digital conversion.

CONNECTION DIAGRAM – Top View
D-24-1



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Am6606
MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage:	Positive	+6V
	Negative	−6V
Input Voltage:	Analog	−5 to +3V
	References	−5 to +3V
	Digital	−5 to 0V
Differential Voltage:	Analog Input to References	±6V
	Analog Gnd to Digital Gnds	±0.1V

Output Current (each output)		15mA
Temperature:	Operating, Am6606DM	−55 to +125°C
	Am6606DL	−25 to +85°C
	Storage	−65 to +150°C
	Junction	+175°C
	Lead (soldering, 60sec)	+300°C
Minimum Operating Voltage (V^+ to V^-)		10V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, note 1, unless otherwise specified)

DC CHARACTERISTICS

Parameter	Description (see definitions)	Test Conditions (Note 1)	Min	Typ	Max			Units
	Resolution		6					Bits
V_{OS}	Error Voltage (each transition)	Am6606 − 8 − 7 − 6	−5 −10 −20		+5 +10 +20			mV mV mV
DNL	Differential Nonlinearity	$\Delta V_{REF} = \Delta V_{REF(min)}$		±1/2				LSB
V_{IN}	Input Voltage			±2.5				V
ΔV_{REF}	Reference Resistor Voltage ($V_{RHI}-V_{RLO}$)	Am6606 − 8 − 7 − 6	0.64 1.28 2.56		5.12 5.12 5.12			V V V
I_{REF}	Reference Current	ΔV_{REF} = 2.56V		15				mA
I_B	Analog Input Current	$V_{IN} \geq V_{RHI}$		375				μA
I_L	Latch Input Current	$V_L \geq V_{OH}$		225				μA
V_{OH}	Output HIGH Voltage			−0.8				V
V_{OL}	Output LOW Voltage			−1.75				V
I^+	Positive Supply Current			140				mA
I^-	Negative Supply Current			100				mA
P_D	Power Dissipation	ΔV_{REF} = 2.56V		1.2				W

AC CHARACTERISTICS

Parameter	Description (see definitions)	Test Conditions (Note 1)	Min	Typ	Max			Units
BW	Full Power Bandwidth	ΔV_{REF} = 2.56V $V_{IN} = \Delta V_{REF}$		50				MHz
f_{MAX}	Maximum Sampling Frequency		100					MHz
t_{pw}	Minimum Sample Time				3			ns
t_{pd}	Encode Delay (each transition)[2]			5				ns
t_s	Minimum Setup Time[2]				3			ns
t_h	Minimum Hold Time[2]				1			ns
t_a	Aperture Uncertainty Time			25				ps
t_{dv}	Data Valid Time			5				ns

Notes: 1. Unless otherwise specified, V^+ = +5.0V, V^- = −5.2V, V_{RHI} = +2.56V, V_{RM} = + 0V, V_{RLO} = −2.56V, t_{pw} = 5ns, and R_L = 100Ω to −2V at all outputs. The Am6606 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse airflow of 500 LFPM or greater.

2. Timing characteristics are for a 100mV analog input pulse level-shifted at each transition point to provide an overdrive of 1mV past the maximum specified error voltage.

FUNCTIONAL PIN DESCRIPTION

REF-HI High end of the reference resistor string. This pin should be tied to a low-impedance reference source. REF-HI voltage must be in the range of:

$$\text{REF-LOW} < \text{REF-HI} \leq +2.56\text{V}$$

1/2-REF This pin is connected to the center of the reference resistor string. It can be connected to a low-impedance source at a voltage halfway between REF-HI and REF-LOW to improve linearity.

REF-LOW This pin is connected to the low end of the reference resistor string and should be connected to a low-impedance reference source. REF-LOW voltage must be in the range:

$$-2.56\text{V} \leq \text{REF-LOW} \leq \text{REF-HI}$$

V_{IN} The signal to be quantized.

LE, $\overline{LE}$ Differential latch enable inputs. These pins should be connected to a differential ECL sample clock.

Q_{0-5} Quantizer data output pins. They are a binary representation of V_{IN}, bit 5 is the MSB bit. All data outputs are ECL compatible.

$Q_{6}, \overline{6}$ These differential overrange outputs are provided to allow Am6606s to be cascaded or stacked for higher resolution systems. Bit 6 will be HIGH when V_{IN} is greater than REF-HI or when overrange disable is tied to V+. These pins are ECL compatible.

OVERRANGE DISABLE When this pin is tied to D.GND, bits 0–5 will be driven LOW whenever V_{IN} is greater than REF-HI (overrange condition). Tying this pin to V+ causes Q_{0-5} to stay HIGH on overrange.

V+ Positive power supply.

V− Negative power supply.

DIG GND The ground for the ECL circuitry. All digital grounds should be tied together and a low-impedance ground path should be maintained.

ANA GND The analog ground. All analog grounds should be tied together and should be tied to the digital ground at only one point in the system.

3

TRUTH TABLE

Input		Output Overrange							
Analog Input (relative to V_{RLO})	O_D	$\overline{Q}_6$	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
$V_{IN} < \frac{1}{64}\Delta V_{REF}$	0V	H	L	L	L	L	L	L	L
$\frac{1}{64}\Delta V_{REF} < V_{IN} < \frac{1}{32}\Delta V_{REF}$	0V	H	L	L	L	L	L	L	H
$\frac{1}{32}\Delta V_{REF} < V_{IN} < \frac{3}{64}\Delta V_{REF}$	0V	H	L	L	L	L	L	H	L
$\frac{3}{64}\Delta V_{REF} < V_{IN} < \frac{1}{16}\Delta V_{REF}$	0V	H	L	L	L	L	L	H	H
$\frac{1}{16}\Delta V_{REF} < V_{IN} < \frac{5}{64}\Delta V_{REF}$	0V	H	L	L	L	L	H	L	L
$\frac{7}{64}\Delta V_{REF} < V_{IN} < \frac{1}{8}\Delta V_{REF}$	0V	H	L	L	L	L	H	H	H
$\frac{1}{8}\Delta V_{REF} < V_{IN} < \frac{9}{64}\Delta V_{REF}$	0V	H	L	L	L	H	L	L	L
$\frac{15}{64}\Delta V_{REF} < V_{IN} < \frac{1}{4}\Delta V_{REF}$	0V	H	L	L	L	H	H	H	H
$\frac{1}{4}\Delta V_{REF} < V_{IN} < \frac{17}{64}\Delta V_{REF}$	0V	H	L	L	H	L	L	L	L
$\frac{31}{64}\Delta V_{REF} < V_{IN} < \frac{1}{2}\Delta V_{REF}$	0V	H	L	L	H	H	H	H	H
$\frac{1}{2}\Delta V_{REF} < V_{IN} < \frac{33}{64}\Delta V_{REF}$	0V	H	L	H	L	L	L	L	L
$\frac{63}{64}\Delta V_{REF} < V_{IN} < \Delta V_{REF}$	0V	H	L	H	H	H	H	H	H
$\Delta V_{REF} < V_{IN}$	0V	L	H	L	L	L	L	L	L
$\Delta V_{REF} < V_{IN}$	5V	L	H	H	H	H	H	H	H

DEFINITION OF TERMS

V_{OS} **ERROR VOLTAGE** – The voltage difference between each nominal transition voltage (n/64 ΔV_{REF} + V_{RLO}) and the actual voltage required to produce the proper change of state at the outputs. The given limits apply over the full input voltage range, for ±5% supply voltage tolerances, and for reference resistor voltages from the specified minimum up to 2.56V. A voltage source of 1/2 ΔV_{REF} + V_{RLO} must be used at the reference resistor midpoint (V_{RM}) in order to obtain the error specifications of the −7 and −8 product grades. This is necessary to reduce the effect of comparator bias current loading on the reference divider over the operating temperature range.

DNL **DIFFERENTIAL NONLINEARITY** – The difference between actual adjacent transition voltages (in LSB) relative to a nominal 1 LSB. This is specified at the minimum reference resistor voltage where the errors are a significant fraction of an LSB. The limits given guarantee monotonicity and no missing codes.

V_{IN} **INPUT VOLTAGE** – The range of applied voltages at the analog and reference inputs over which the error voltage and encode delay specifications apply.

ΔV_{REF} **REFERENCE RESISTOR VOLTAGE** – The external voltage applied across the 64-section resistive divider (V_{RHI} − V_{RLO}). The specified minimum is determined by the error voltage and differential nonlinearity limits, and the maximum is set by transistor emitter-base breakdown voltage. Error voltage caused by resistor divider mismatch increases linearly with voltage; therefore, the error voltage limits are guaranteed only up to 2.56V.

I_{REF} **REFERENCE CURRENT** – The current drawn from the external voltage reference by the reference resistor. It is specified at the maximum reference voltage for which the error specifications apply.

I_B **ANALOG INPUT CURRENT** – The current into the analog input terminal. The value of this current increases as the analog input voltage rises toward full-scale due to the increasing number of comparators being switched on. The limit given is for inputs above full-scale, which is the maximum condition.

I_L **LATCH INPUT CURRENT** – The current into either ECL latch input terminal. The maximum value of this current occurs when a logic HIGH is applied.

V_{OH} **OUTPUT HIGH VOLTAGE** – The logic HIGH voltage at any output with an external 100Ω pulldown resistor returned to −2V.

V_{OL} **OUTPUT LOW VOLTAGE** – The logic LOW voltage at any output with an external 100Ω pulldown resistor returned to −2V.

I^+ **POSITIVE SUPPLY CURRENT** – The current required from the +5V supply to operate the quantizer.

I^- **NEGATIVE SUPPLY CURRENT** – The current required from the −5.2V supply to operate the quantizer.

P_{DISS} **POWER DISSIPATION** – The power dissipated by the quantizer at full-scale (output code 01111) with all outputs terminated in 100Ω to −2V and with 5.12V reference resistor voltage.

F_{FP} **FULL POWER BANDWIDTH** – Maximum full-scale input frequency that can be digitized.

F_{MAX} **MAXIMUM SAMPLING FREQUENCY** – The maximum sampling rate at which the quantizer can correctly encode an analog signal.

t_{pw} **MINIMUM SAMPLE TIME** – The minimum time (at the 50% points) that the quantizer must be sampling (Latch Enable HIGH, Latch Enable LOW) in order to acquire and hold an input signal charge.

t_{pd} **ENCODE DELAY** – The propagation delay measured from the 50% point of the Latch Enable HIGH-to-LOW transition to the 80% point of an output LOW-to-HIGH transition (or the 20% point of an output HIGH-to-LOW transition). The analog input signal applied to cause the outputs to change is 1mV in excess of the guaranteed error voltage limits. Each of the 64 transition points is tested for inputs above and below the nominal transition voltages.

t_s **MINIMUM SETUP TIME** – The minimum time before the negative transition of the Latch Enable signal that an analog input signal change must be present in order to be acquired and encoded by the quantizer.

t_h **MINIMUM HOLD TIME** – The minimum time after the negative transition of the Latch Enable signal that the analog input signal must remain unchanged in order to be acquired and encoded by the quantizer.

t_{dv} **DATA VALID** – The propagation delay measured from the 50% point of the Latch Enable LOW-to-HIGH transition to the 80% point of an output HIGH-to-LOW transition (or the 20% point of an output LOW-to-HIGH transition). The combination of sampling frequency, encode delay, and analog delay determines the time that the output data is valid. The analog delay is measured with a large input signal (79 to 94mV) in excess of the nominal transition voltage, which is the worse condition (minimum delay).

t_a **APERTURE UNCERTANTY TIME** – Time variations or uncertanty between comparators entering the hold mode.

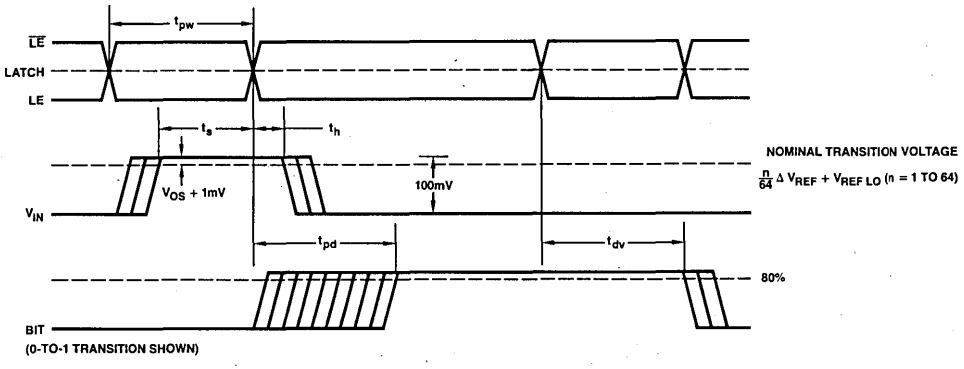
THERMAL CONSIDERATIONS

In order to achieve the high-speed of the Am6606, a large amount of power is required to be dissipated by the package. This increases the temperature of the chip relative to the ambient temperature. To be compatible with other ECL circuits which normally use airflow as a means of package cooling, the Am6606 characteristics are specified for an airflow across the package of 500 linear feet per minute or greater. Thus, even though different ECL packages on a circuit board may have different power dissipations, all will have the same input and output levels, provided each sees the same airflow and temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am6606 is operated without airflow, the change in electrical characteristics due to the increased chip temperature must be taken into account, and the maximum ambient temperature is limited to 70°C with a thermal derating of 60°C/W.

INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am6606 quantizer is no exception. A ground plane must be used to provide a good, low inductance, ground current return path. The impedance at the analog input should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch and should be kept away from the input and voltage reference pins. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150 ohms. Reflections will occur unless the line is terminated in its characteristic impedance, which can be no less than 100 ohms for the Am6606 when terminated to −2V. Best results are usually obtained with the terminating resistor at the end of the driven line. The supply voltage and reference input pins should be well decoupled with RF capacitors connected to the ground plane as close to the device pins as possible.

Am6606 TIMING DIAGRAM

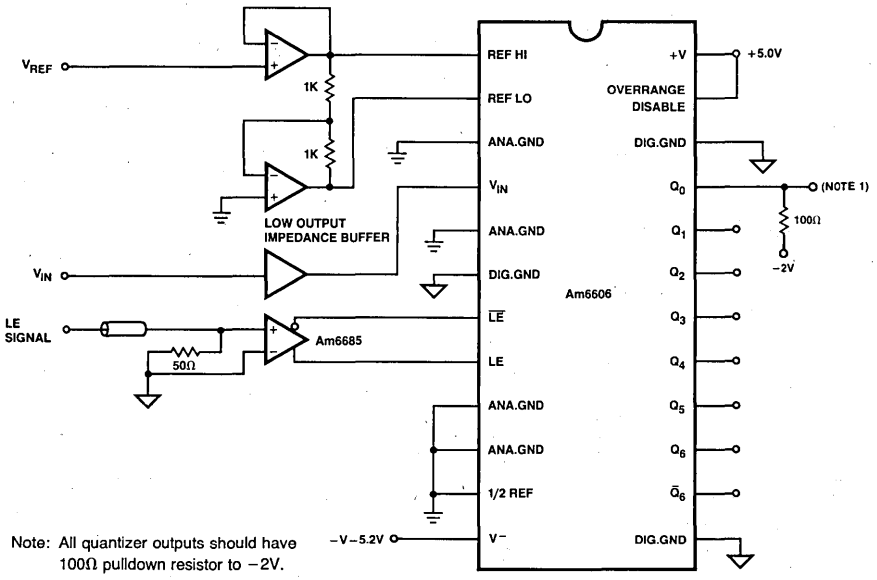


APPLICATIONS INFORMATION

Figure 1 shows the Am6606 in its basic connection. In this example it has been setup for bipolar inputs with the reference inputs buffered by operational amplifiers. An Am685 has been used to drive the Latch Enable inputs; the input to the Am685 should be a square wave centered about ground. A low-impedance buffer should be used to drive the Analog Input in order for the full bandwidth of the device to be utilized. The input capacitance of the Am6606 is approximately 25pF; if the input is driven from a high-impedance source a low pass filter is formed and high frequency inputs will be attenuated. In this application of Figure 1 the Overrange Disable pin has been tied to V+ to cause bits 0–5 to stay HIGH on an overrange and to allow the system to distinguish between overrange and zero, in a 6-bit application.

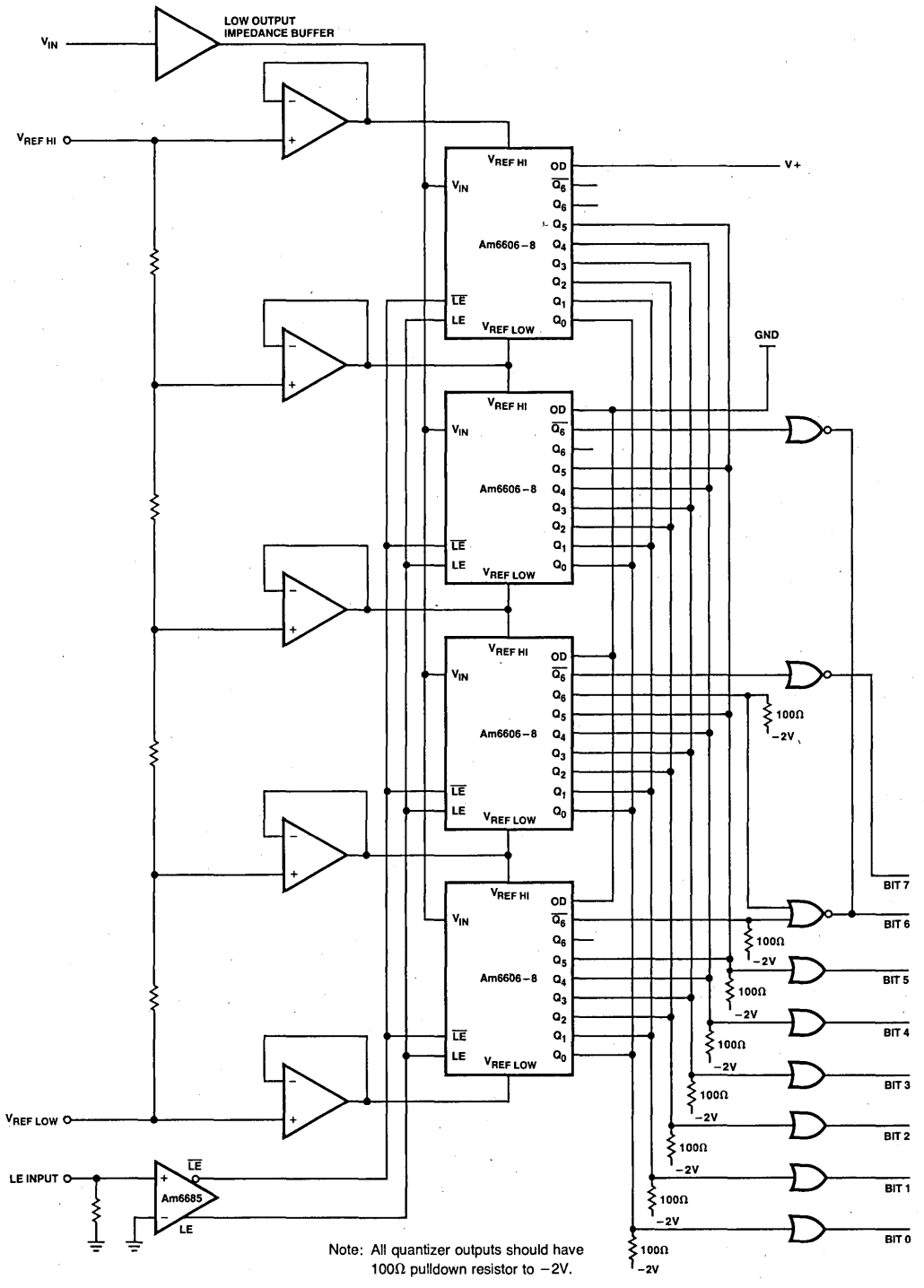
Figure 2 shows four Am6606s connected as a 100MHz 8-bit quantizer. NOR gates are used to decode the Overrange Outputs for bits 6 and 7. The low order bits (0–5) are wire-OR'd together and connected to OR gates to match the delay through the NOR gates. The Overrange Disable pins on the lower three quantizers are tied to D.GND so that they do not interfere with the wire-OR connection. The Overrange Disable of the top quantizer is tied to V+ so that all eight outputs will be HIGH when the input is overrange.

Figure 1. Applications Circuit



Note: All quantizer outputs should have 100Ω pulldown resistor to −2V.

Figure 2.



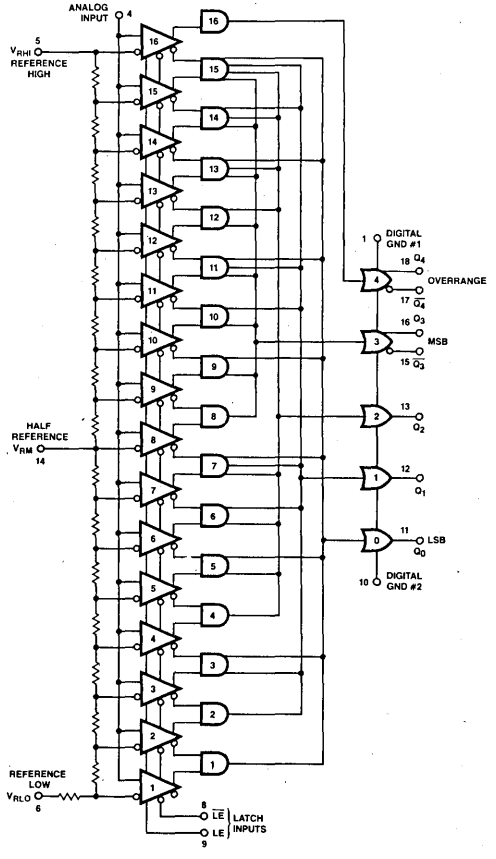
Note: All quantizer outputs should have 100Ω pulldown resistor to −2V.

Am6688
4-Bit Quantizer

DISTINCTIVE CHARACTERISTICS

- 100MHz sampling rate
- 50MHz full power bandwidth
- 10ps aperture uncertainty time
- 5ns maximum encode delay
- 4-bit resolution, expandable to 8 bits
- 8-bit accuracy
- Large bipolar input voltage range
- ECL Output
- Q and $\overline{Q}$ Outputs on MSB for 2's complement conversion

FUNCTIONAL DIAGRAM



LIC-900

FUNCTIONAL DESCRIPTION

The Am6688 4-bit quantizer consists of an array of 16 high-speed ECL sampling comparators, a resistor voltage divider, and an ECL-compatible binary encoder. It will accurately quantize an analog voltage into 15 equally-spaced levels and output a 4-bit binary digital word at sampling rates up to 100MHz.

Resolution above 4-bits, up to a maximum of 8, may be obtained by stacking quantizers (n bits of resolution requires 2^{n-4} quantizers). An overrange output signal is provided to indicate that the input signal has exceeded the full-scale limit. This overrange output is also the enable gating signal used to encode the higher-order bits of the output in a stacked configuration.

The high speed latch enable inputs are intended to be driven from the complementary outputs of a standard ECL gate or a high-speed comparator such as the Am685. If LE is driven high and $\overline{LE}$ is driven low, the quantizer is in the sample mode and operates like a low-gain, high-bandwidth amplifier. When LE is driven low and $\overline{LE}$ is driven high, the quantizer will hold its existing digital binary output word.

The outputs are open emitters, requiring external pull-down resistors to −2V or to −5.2V.

These devices can be used in video data conversion and time-base correction, radar signal processing, nuclear pulse-height analysis, and other systems requiring very high-speed analog-to-digital conversion.

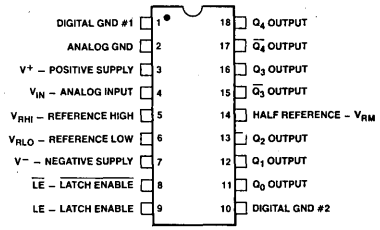
ORDERING INFORMATION*

Order Number	Temperature Range	Maximum Error
Am6688DL-8	−30 to +85°C	±5mV
Am6688DL-7	−30 to +85°C	±10mV
Am6688DL-6	−30 to +85°C	±20mV
Am6688DM-8	−55 to +125°C	±5mV
Am6688DM-7	−55 to +125°C	±10mV
Am6688DM-6	−55 to +125°C	±20mV

*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAM
Top View

Hermetic DIP
D-18-1



Note: Pin 1 is marked for orientation.

LIC-901

01819B-ANA

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage:	Positive	+7V
	Negative	−6V
Input Voltage:	Analog	−5V to +3V
	References	−5V to +3V
	Digital	−5V to 0V
Differential Voltage:	Analog Input to References	±6V
	Analog Gnd to Digital Gnds	±0.1V

Output Current (each output)		15mA
Temperature:	Operating, Am6688DL	−30 to +85°C
	Am6688DM	−55 to +125°C
	Storage	−65 to +150°C
	Junction	+175°C
	Lead (soldering, 60sec)	+300°C
Minimum Operating Voltage (V^+ to V^-)		10V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES

(Unless otherwise specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 1)	Am6688DL Min	Am6688DL Max	Am6688DM Min	Am6688DM Max	Units
	Resolution		4		4		Bits
V_{OS}	Error Voltage (each transition)	Am6688 − 8	−5	+5	−5	+5	mV
		− 7	−10	+10	−10	+10	mV
		− 6	−20	+20	−20	+20	mV
DNL	Differential Nonlinearity	$\Delta V_{REF} = \Delta V_{REF(min)}$	−0.5	0.5	−0.5	0.5	LSB
V_{IN}	Input Voltage		−3.3	+2.7	−3.3	+2.7	V
ΔV_{REF}	Reference Resistor Voltage ($V_{RHI}-V_{RLO}$)	Am6688 − 8	0.16	6.0	0.16	6.0	V
		− 7	0.32	6.0	0.32	6.0	V
		− 6	0.64	6.0	0.64	6.0	V
I_{REF}	Reference Current	$\Delta V_{REF} = 2.56V$	6.0	17	5.0	18	mA
I_B	Analog Input Current	$V_{IN} \geq V_{RHI}$		230		250	μA
I_L	Latch Input Current	$V_L \geq V_{OH}$		200		220	μA
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.93	−0.72	−0.93	−0.72	V
		$T_A = T_{A(min)}$	−1.03	−0.80	−1.08	−0.83	V
		$T_A = T_{A(max)}$	−0.86	−0.64	−0.83	−0.58	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.90	−1.62	−1.90	−1.62	V
		$T_A = T_{A(min)}$	−1.93	−1.65	−1.95	−1.66	V
		$T_A = T_{A(max)}$	−1.86	−1.58	−1.84	−1.54	V
I^+	Positive Supply Current			100		100	mA
I^-	Negative Supply Current			100		100	mA
P_{DISS}	Power Dissipation	$\Delta V_{REF} = 2.56V$		1.2		1.2	W

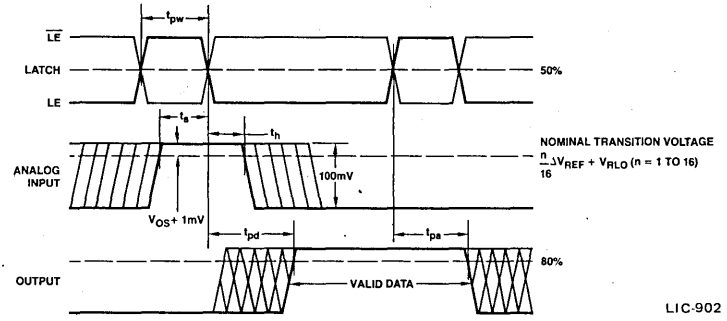
AC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 1)	Am6688DL Min	Am6688DL Max	Am6688DM Min	Am6688DM Max	Units
F_{FP}	Full Power Bandwidth	$T_A = 25°C$, $\Delta V_{REF} = 2.56V$, $V_{IN} = \Delta V_{REF}$	50 (Typ)		50 (Typ)		MHz
F_{MAX}	Maximum Sampling Frequency		100		100		MHz
t_{pw}	Minimum Sample Time			3		3	ns
t_{pd}	Encode Delay (each transition)[2]	$T_{A(min)} \leq T_A \leq 25°C$		5		5	ns
		$T_A = T_{A(max)}$		6		8	ns
t_s	Minimum Set-up Time[2]	$T_A = 25°C$		3		3	ns
t_h	Minimum Hold Time[2]	$T_A = 25°C$		1		1	ns
t_{pa}	Analog Delay (each transition)[2]	$T_{A(min)} \leq T_A \leq 25°C$	3		3		ns
		$T_A = T_{A(max)}$	4		4		ns
t_a	Aperture Uncertainty Time	$T_A = 25°C$	10 (Typ)		10 (Typ)		ps

Notes: 1. Unless otherwise specified, $V^+ = +6.0V$, $V^- = -5.2V$, $V_{RHI} = +2.56V$, $V_{RM} = +1.28V$, $V_{RLO} = 0V$, $t_{pw} = 5ns$, and $R_L = 100\Omega$ to $-2V$ at all outputs. The specifications given for V_{OS}, DNL, and t_{pd} apply over the full V_{IN} range and for ±5% supply voltages. The Am6688 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

2. Timing characteristics are for a 100mV analog input pulse level-shifted at each transition point to provide an overdrive of 1mV past the maximum specified error voltage.

TIMING DIAGRAM



LIC-902

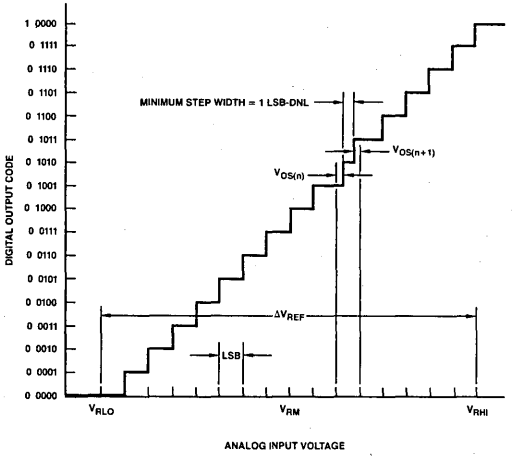
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

3

During the sampling time, the quantizer acts like a low-gain, very wide-bandwidth linear amplifier. The gain is not high enough to hold the outputs in a stable logic state under all conditions; consequently, the outputs may be undefined during this period. The time that the outputs are unstable begins t_{pa} after the Latch Enable goes HIGH, and terminates t_{pd} after it goes LOW. It is best to minimize this time by using as narrow a sampling pulse as possible, since the possibility of oscillation due to external parasitic feedback is greater the longer the device is in the analog mode.

TYPICAL TRANSFER FUNCTION



LIC-903

TRUTH TABLE

Analog Input (relative to V_{RLO})	Q_4	Q_3	Q_2	Q_1	Q_0
$V_{IN} < \frac{1}{16}\Delta V_{REF}$	L	L	L	L	L
$\frac{1}{16}\Delta V_{REF} < V_{IN} < \frac{1}{8}\Delta V_{REF}$	L	L	L	L	H
$\frac{1}{8}\Delta V_{REF} < V_{IN} < \frac{3}{16}\Delta V_{REF}$	L	L	L	H	L
$\frac{3}{16}\Delta V_{REF} < V_{IN} < \frac{1}{4}\Delta V_{REF}$	L	L	L	H	H
$\frac{1}{4}\Delta V_{REF} < V_{IN} < \frac{5}{16}\Delta V_{REF}$	L	L	H	L	L
$\frac{5}{16}\Delta V_{REF} < V_{IN} < \frac{3}{8}\Delta V_{REF}$	L	L	H	L	H
$\frac{3}{8}\Delta V_{REF} < V_{IN} < \frac{7}{16}\Delta V_{REF}$	L	L	H	H	L
$\frac{7}{16}\Delta V_{REF} < V_{IN} \frac{1}{2}\Delta V_{REF}$	L	L	H	H	H
$\frac{1}{2}\Delta V_{REF} < V_{IN} < \frac{9}{16}\Delta V_{REF}$	L	H	L	L	L
$\frac{9}{16}\Delta V_{REF} < V_{IN} < \frac{5}{8}\Delta V_{REF}$	L	H	L	L	H
$\frac{5}{8}\Delta V_{REF} < V_{IN} < \frac{11}{16}\Delta V_{REF}$	L	H	L	H	L
$\frac{11}{16}\Delta V_{REF} < V_{IN} < \frac{3}{4}\Delta V_{REF}$	L	H	L	H	H
$\frac{3}{4}\Delta V_{REF} < V_{IN} < \frac{13}{16}\Delta V_{REF}$	L	H	H	L	L
$\frac{13}{16}\Delta V_{REF} < V_{IN} < \frac{7}{8}\Delta V_{REF}$	L	H	H	L	H
$\frac{7}{8}\Delta V_{REF} < V_{IN} < \frac{15}{16}\Delta V_{REF}$	L	H	H	H	L
$\frac{15}{16}\Delta V_{REF} < V_{IN} < \Delta V_{REF}$	L	H	H	H	H
$V_{IN} > \Delta V_{REF}$	H	L	L	L	L

Am6688
DEFINITION OF TERMS

V_{OS} **ERROR VOLTAGE** – The voltage difference between each nominal transition voltage (n/16 ΔV_{REF} + V_{RLO}) and the actual voltage required to produce the proper change of state at the outputs. The given limits apply over the full input voltage range, for ±5% supply voltage tolerances, and for reference resistor voltages from the specified minimum up to 2.56V. A voltage source of 1/2 ΔV_{REF} + V_{RLO} must be used at the reference resistor midpoint (V_{RM}) in order to obtain the error specifications of the –7 and –8 product grades. This is necessary to reduce the effect of comparator bias current loading on the reference divider over the operating temperature range.

DNL **DIFFERENTIAL NONLINEARITY** – The difference between actual adjacent transition voltages (in LSB) relative to a nominal 1 LSB. This is specified at the minimum reference resistor voltage where the errors are a significant fraction of an LSB. The limits given guarantee monotonicity and no missing codes.

V_{IN} **INPUT VOLTAGE** – The range of applied voltages at the analog and reference inputs over which the error voltage and encode delay specifications apply.

ΔV_{REF} **REFERENCE RESISTOR VOLTAGE** – The external voltage applied across the 16-section resistive divider (V_{RHI} – V_{RLO}). The specified minimum is determined by the error voltage and differential nonlinearity limits, and the maximum is set by transistor emitter-base breakdown voltage. Error voltage caused by resistor divider mismatch increases linearly with voltage; therefore, the error voltage limits are guaranteed only up to 2.56V.

I_{REF} **REFERENCE CURRENT** – The current drawn from the external voltage reference by the reference resistor. It is specified at the maximum reference voltage for which the error specifications apply.

I_B **ANALOG INPUT CURRENT** – The current into the analog input terminal. The value of this current increases as the analog input voltage rises toward full-scale due to the increasing number of comparators being switched on. The limit given is for inputs above full-scale, which is the maximum condition.

I_L **LATCH INPUT CURRENT** – The current into either ECL latch input terminal. The maximum value of this current occurs when a logic HIGH is applied.

V_{OH} **OUTPUT HIGH VOLTAGE** – The logic HIGH voltage at any output with an external 100Ω pulldown resistor returned to –2V.

V_{OL} **OUTPUT LOW VOLTAGE** – The logic LOW voltage at any output with an external 100Ω pulldown resistor returned to –2V.

I^+ **POSITIVE SUPPLY CURRENT** – The current required from the +6V supply to operate the quantizer.

I^- **NEGATIVE SUPPLY CURRENT** – The current required from the –5.2V supply to operate the quantizer.

P_{DISS} **POWER DISSIPATION** – The power dissipated by the quantizer at full-scale (output code 01111) with all outputs terminated in 100Ω to –2V and with 2.56V reference resistor voltage.

F_{FP} **FULL POWER BANDWIDTH** – Maximum full scale input frequency that can be digitized.

F_{MAX} **MAXIMUM SAMPLING FREQUENCY** – The maximum sampling rate at which the quantizer can correctly encode an analog signal.

t_{pw} **MINIMUM SAMPLE TIME** – The minimum time (at the 50% points) that the quantizer must be unlatched (Latch Enable High, Latch Enable LOW) in order to acquire and hold an input signal change.

t_{pd} **ENCODE DELAY** – The propagation delay measured from the 50% point of the Latch Enable HIGH-to-LOW transition to the 80% point of an output LOW-to-HIGH transition (or the 20% point of an output HIGH-to-LOW transition). The analog input signal applied to cause the outputs to change is 1mV in excess of the guaranteed error voltage limits. Each of the 16 transition points is tested for inputs above and below the nominal transition voltages.

t_s **MINIMUM SET-UP TIME** – The minimum time before the negative transition of the Latch Enable signal that an analog input signal change must be present in order to be acquired and encoded by the quantizer.

t_h **MINIMUM HOLD TIME** – The minimum time after the negative transition of the Latch Enable signal that the analog input signal must remain unchanged in order to be acquired and encoded by the quantizer.

t_{pa} **ANALOG DELAY** – The propagation delay measured from the 50% point of the Latch Enable LOW-to-HIGH transition to the 80% point of an output HIGH-to-LOW transition (or the 20% point of an output LOW-to-HIGH transition). The combination of sampling frequency, encode delay, and analog delay determines the time that the output data is valid. The analog delay is measured with a large input signal (79mV to 94mV) in excess of the nominal transition voltage, which is the worse condition (minimum delay).

t_a **APERTURE UNCERTAINTY TIME** – Time variations or uncertainty between comparators entering the hold mode.

THERMAL CONSIDERATIONS

In order to achieve the high speed of the Am6688, a large amount of power is required to be dissipated by the package. This increases the temperature of the chip relative to the ambient temperature. To be compatible with other ECL circuits which normally use air flow as a means of package cooling, the Am6688 characteristics are specified for an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL packages on a circuit board may have different power dissipations, all will have the same input and output levels, provided each sees the same air flow and temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am6688 is operated without airflow, the change in electrical characteristics due to the increased chip temperature must be taken into account, and the maximum ambient temperature is limited to 70°C with a thermal derating of 100°C/W.

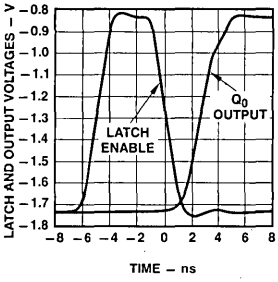
INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am6688 quantizer is no exception. A ground plane must be used to provide a good, low inductance, ground current return path. The impedance at the analog input should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch and should be kept away from the input and voltage reference pins. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150 ohms. Reflections will occur unless the line is terminated in its characteristic impedance, which can be no less than 100 ohms for the Am6688 when terminated to –2V. Best results are usually obtained with the terminating resistor at the end of the driven line. The supply voltage and reference input pins should be well decoupled with RF capacitors connected to the ground plane as close to the device pins as possible.

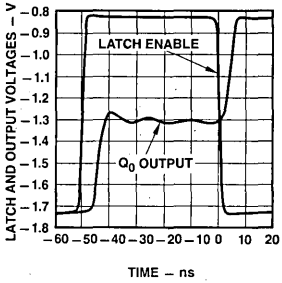
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are T_A = 25°C, V^+ = +6.0V, V^- = −5.2V, V_{RHI} = 2.56V, V_{RM} = +1.28V, V_{RLO} = 0V, t_{pw} = 5ns, and R_L = 100Ω to −2V)

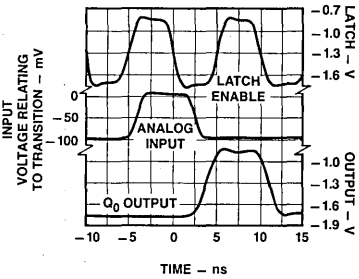
Encode Delay for Narrow Latch Pulse



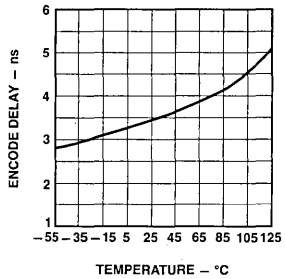
Encode Delay for Wide Latch Pulse



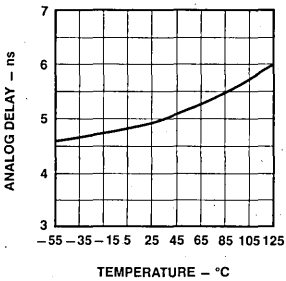
Response at 100MHz Sample Rate



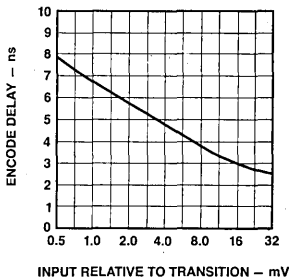
Encode Delay as a Function of Temperature



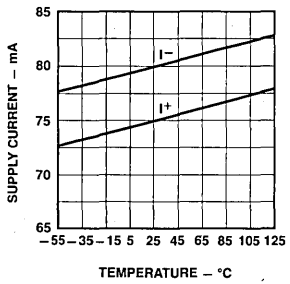
Analog Delay as a Function of Temperature



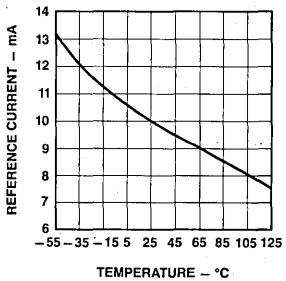
Encode Delay as a Function of Input Voltage



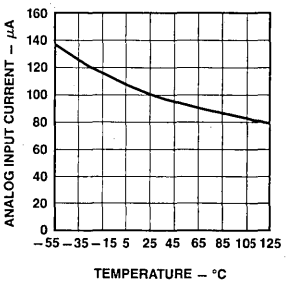
Supply Currents as a Function of Temperature



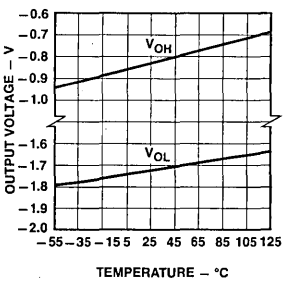
Reference Current as a Function of Temperature



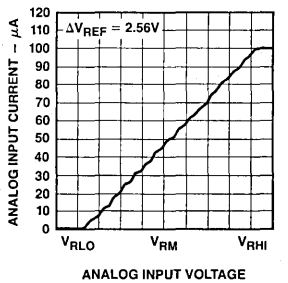
Analog Input Current as a Function of Temperature



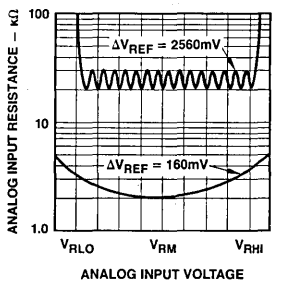
Output Levels as a Function of Temperature



Analog Input Current as a Function of Input Voltage



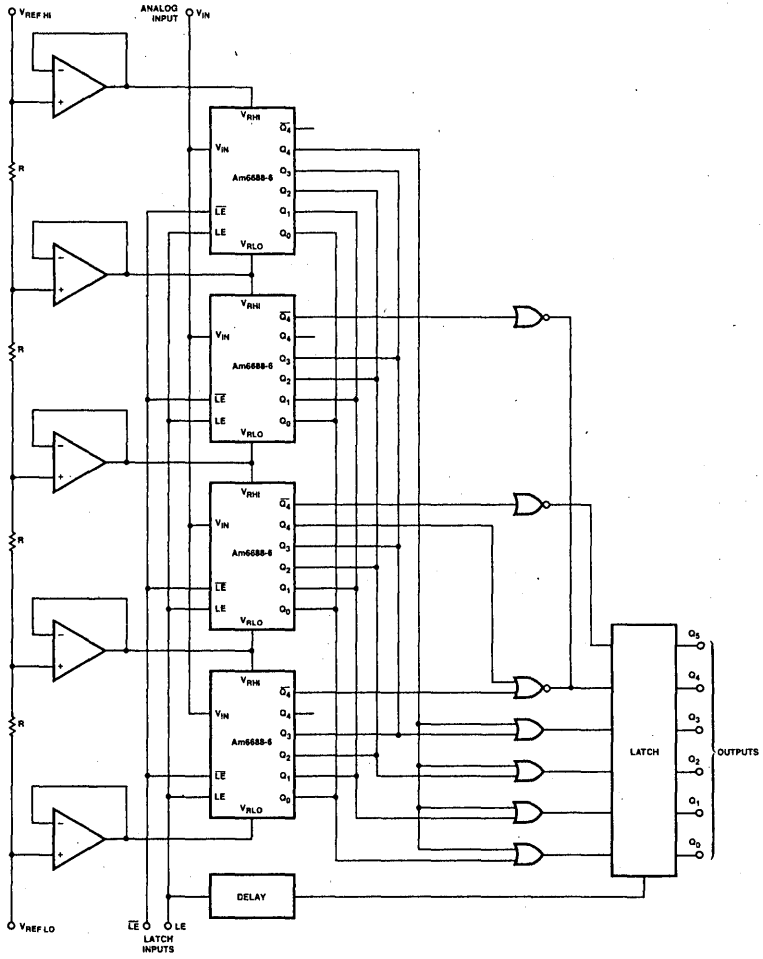
Input Resistance as a Function of Analog Input Voltage



LIC-904

TYPICAL APPLICATION

6-Bit Quantizer



LIC-905

Sample and Holds – Section IV

LF198/298/398

Monolithic Sample and Hold Circuits

Distinctive Characteristics

- Operates from ±5V to ±18V supplies
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at C_h = 0.01μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

GENERAL DESCRIPTION

The LF198/LF298/LF398 are BI-FET monolithic sample and hold circuits with ultra-high DC accuracy, fast acquisition time (6μs to 0.01%) and low droop rate. A bipolar input stage is used to obtain the lowest possible offset voltage and wide bandwidth. These circuits are designed to have high common mode rejection and a gain accuracy of 0.002%. High input impedance ($10^{10}\Omega$) permits their use with a high impedance source without degrading accuracy.

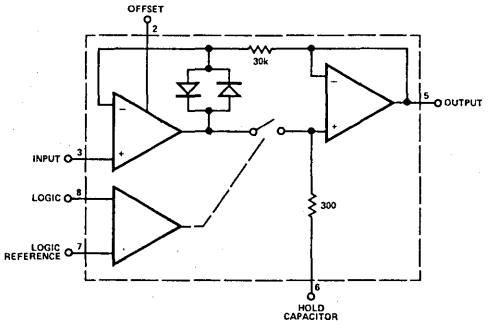
The output buffer has a p-channel JFET input with a typical input current of 30pA, giving a droop rate as low as 5mV/Min with a 1μF hold capacitor. The JFET has a very low noise level and high temperature stability.

A differential logic input allows the logic to be referenced to a separate ground from analog ground, permitting a direct interface to nearly any logic family. The LF198 series guarantees no feed through in the hold mode including input signal swings equal to the power supply.

The LF198A series has tightened electrical specifications.

4

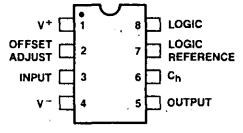
FUNCTION DIAGRAM



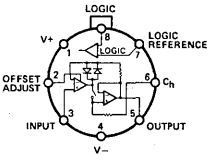
LIC-204

CONNECTION DIAGRAMS – Top Views

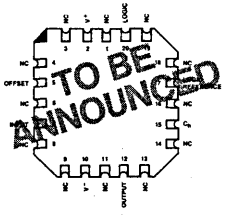
P-8-1



H-8-1



L-20-1



LIC-205

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LF398	Metal Can	0 to +70°C	LF398H
	Plastic	0 to +70°C	LF398N
	Leadless	0 to +70°C	LF398L**
	Dice	0 to +70°C	LD398
LF298	Metal Can	−25 to +85°C	LF298H
	Leadless	−25 to +85°C	LF298L**
LF198*	Metal Can	−55 to +125°C	LF198H
	Leadless	−55 to +125°C	LF198L**
	Dice	−55 to +125°C	LD198

*Also available with burn-in processing. To order add suffix B to part number.
**To be announced.

LF198/298/398
ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Range LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Package Limitation, Note 1)	500mW
Derate above 25°C	6.8mW/°C
Supply Voltage	±18V
Input Voltage	Equal to Supply Voltage
Logic to Logic Reference Differential Voltage (Note 2)	+7V, −30V
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Soldering 10 seconds)	300°C

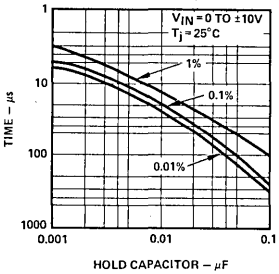
ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	LF198/LF298 Min.	LF198/LF298 Typ.	LF198/LF298 Max.	LF398 Min.	LF398 Typ.	LF398 Max.	Unit
Input Offset Voltage, (Note 6)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k\Omega$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	$T_j = 25°C$, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\mu F$		20			20		μs
Hold Capacitor Charge Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

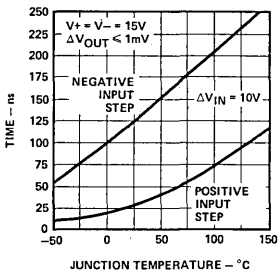
Notes:
1. The maximum junction temperature is 150°C for the LF198, 115°C for the LF298, and 100°C for the LF398. When used at a higher ambient temperature the metal can package must be derated based on a thermal resistance (θjA) of 150°C/W. Derate N package 5.6mW/°C above 36°C.
2. The differential voltage may not exceed this limit. The common mode voltage on the logic pins may equal the supply voltage without causing damage to the device. For the LF198 to operate properly, one of the logic pins must be at least 2V below the positive supply and 3V above the negative supply.
3. The following conditions apply unles otherwise noted: Device is in "sample mode." $T_j = 25°C$, $V_S = \pm 15V$, $-11.5V < V_{IN} < +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V. Logic input voltage = 2.5V.
4. The hold step is produced by a charge which is coupled from the logic input signal to the hold capacitor via parasitic capacitance and internal operating point changes. Stray capacitance equal to 1pF will create a 0.5mV step with a 5 volt logic swing and a 0.01μF hold capacitor. This step can be reduced by increasing the magnitude of the hold capacitor.
5. Leakage current is measured at a junction temperature of 25°C. The junction temperature doubles the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over the full input signal range.
6. These values are guaranteed over the ±5 to ±18V supply range.

TYPICAL PERFORMANCE CHARACTERISTICS

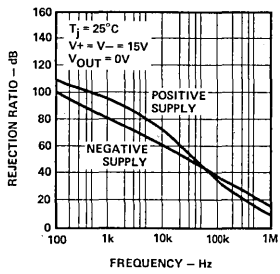
Acquisition Time



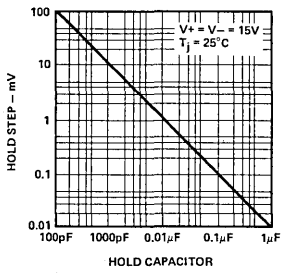
Aperture Time



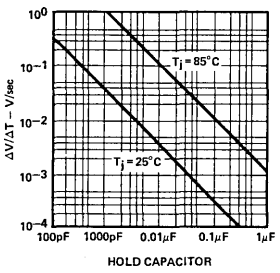
Power Supply Rejection



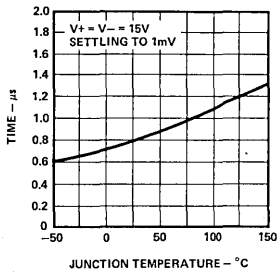
Hold Step



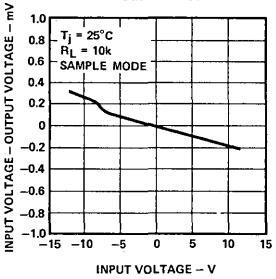
Output Droop Rate



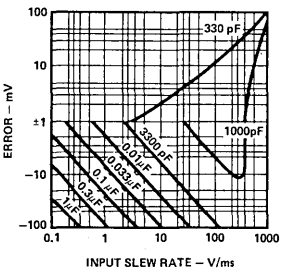
"Hold" Settling Time



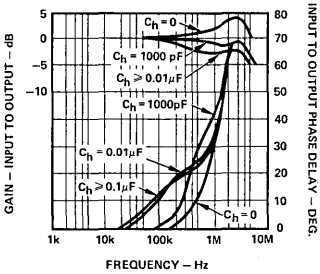
Gain Error



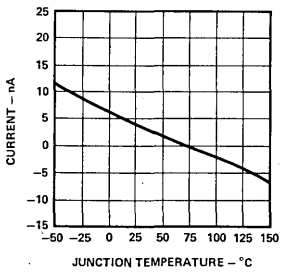
Dynamic Sampling Error



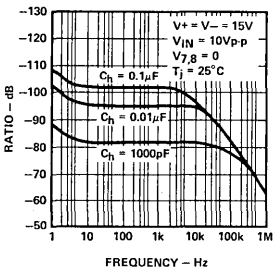
Phase and Gain (Input to Output, Small Signal)



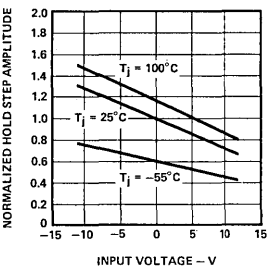
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



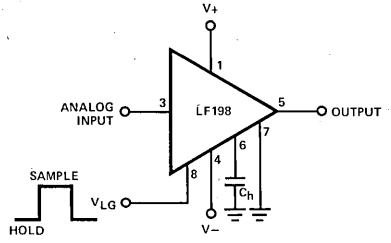
Hold Step Versus Input Voltage



LIC-206

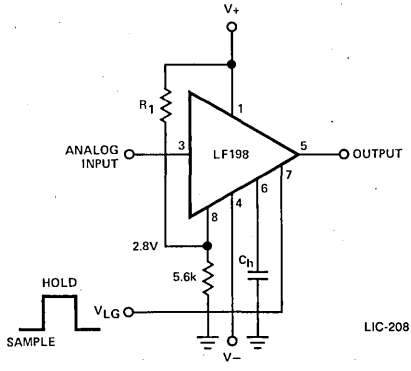
LOGIC INPUT CONFIGURATIONS

TTL AND CMOS
$3V \leqslant V_{LG}(HI\ STATE) \leqslant 7V$



LIC-207

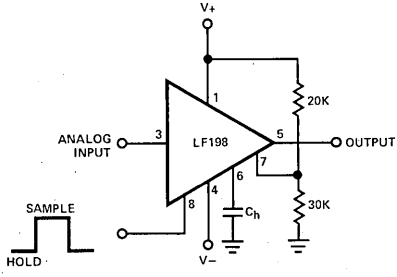
Threshold = 1.4V



LIC-208

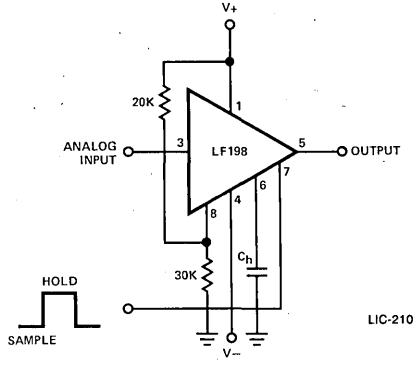
Threshold = 1.4V
R_1 select for 2.8V at Pin 8

CMOS
$7V \leqslant V_{LG}(HI\ STATE) \leqslant 15V$



LIC-209

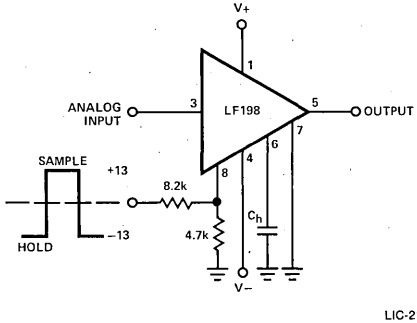
Threshold = 0.6 (V+) + 1.4V



LIC-210

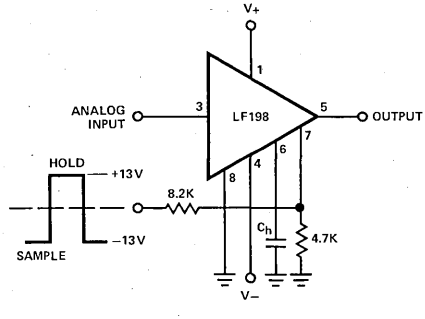
Threshold = 0.6 (V+) − 1.4V

OP AMP DRIVE
OUTPUT VOLTAGE = ±13V



LIC-211

Threshold ≃ 4V



LIC-212

Threshold = −4V

APPLICATION INFORMATION

Freezing the input to an analog-to-digital (A/D) converter is an important application for the sample and hold amplifier. If the analog input to the A/D changes during conversion by the amount ±1/2LSB, an ideal A/D would produce 1 LSB error beyond normal quantization error. A sample and hold amplifier eliminates this problem by holding the input signal to the A/D converter during the conversion interval. The proper choice of hold capacitor value and type is necessary to obtain optimum performance. The capacitor value directly affects several circuit parameters, particularly acquisition time, droop rate, and hold step. The hold step error is inversely proportional to the value of the hold capacitor.

Graphs are provided in this data sheet for use as guides in selecting a suitable value of capacitance. However, the capacitor should have extremely high insulation resistance and low dielectric absorption, or dielectric hysteresis. Polypropylene (below +85°C) and Teflon (above +85°C) types are recommended. The hysteresis error can be significantly reduced if the output of the LF198 is digitized immediately after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10-50ms, thus if A/D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

The logic inputs on the LF198 are fully differential with low input current and will operate from TTL levels up to 15V. Some typical logic input configurations are shown in this data sheet. The logic signal into the LF198 must have a minimum slew rate of 0.2V/μs. Slower signals cause excess hold step errors.

When switched from sample to hold, delay in response to the hold command (aperture time and aperture time uncertainty) can cause the frozen value of a fast moving waveform to differ from the value it had at the instant the hold command is given. However, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip which cancels out some of the error due to aperture time and aperture time uncertainty.

For example, using an analog input of 20 volts p-p at 10kHz, maximum slew rate 0.5V/μs, with no phase delay and 80ns logic delay, one could expect up to (0.08μs) • (0.5V/μs) = 40mV error if the input is sampled during the maximum dv/dt period. A positive going input would give a +40mV error. Assume that the slew rate of the charging amplifier and the RC constant of the analog loop cause a delay of 120ns. If the hold capacitor sees this exact delay, then the analog delay would be (0.5μV/sec)•(.12μs) = −60mV. Total output error is +40mV −60mV = −20mV.

For a sample and hold amplifier in a multiplexed A/D system, acquisition and aperture times are critical parameters. In order to maintain the acquired signal level within the specified accuracy, these times must be considered when selecting the sampling rate. For example, if a 16 channel MUX drives a sample and hold amplifier in which each channel is 5KHz and 2 samples per cycle are needed to satisfy the Nyquist criteria, the minimum sampling rate = 160000 samples/sec. ((5KHz X 16) cycles/sec X 2 samples/cycle). The minimum channel period is the reciprocal of the sampling rate of 6.25μs. During the hold mode the MUX can switch to another channel. This eliminates the need to consider the MUX and source settling time and shortens the channel period.

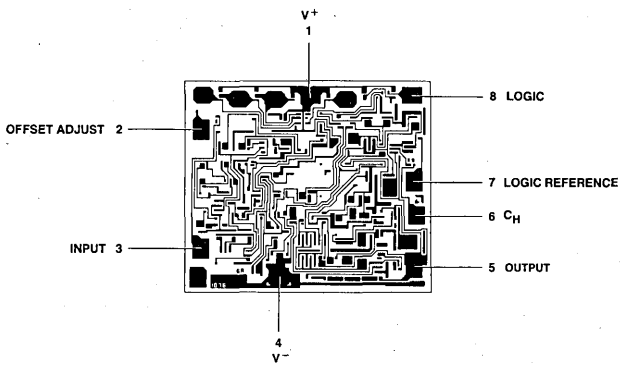
Calculating the sum of the sample and hold acquisition time, aperture time and A/D conversion time is usually a convenient method for estimating maximum channel period.

In multiplex applications, sample and hold feed-through is a significant problem. Since each channel voltage differs, the sample and hold input signal becomes a series of varied height pulses that cause errors in the sample and hold voltage.

Digital feed through occurs when a fast rising logic signal is coupled into the analog input. To minimize it, the logic signal trace in the PCB layout should be kept as far as possible from the analog input. Guarded trace may also be used around the input pin for shielding purposes.

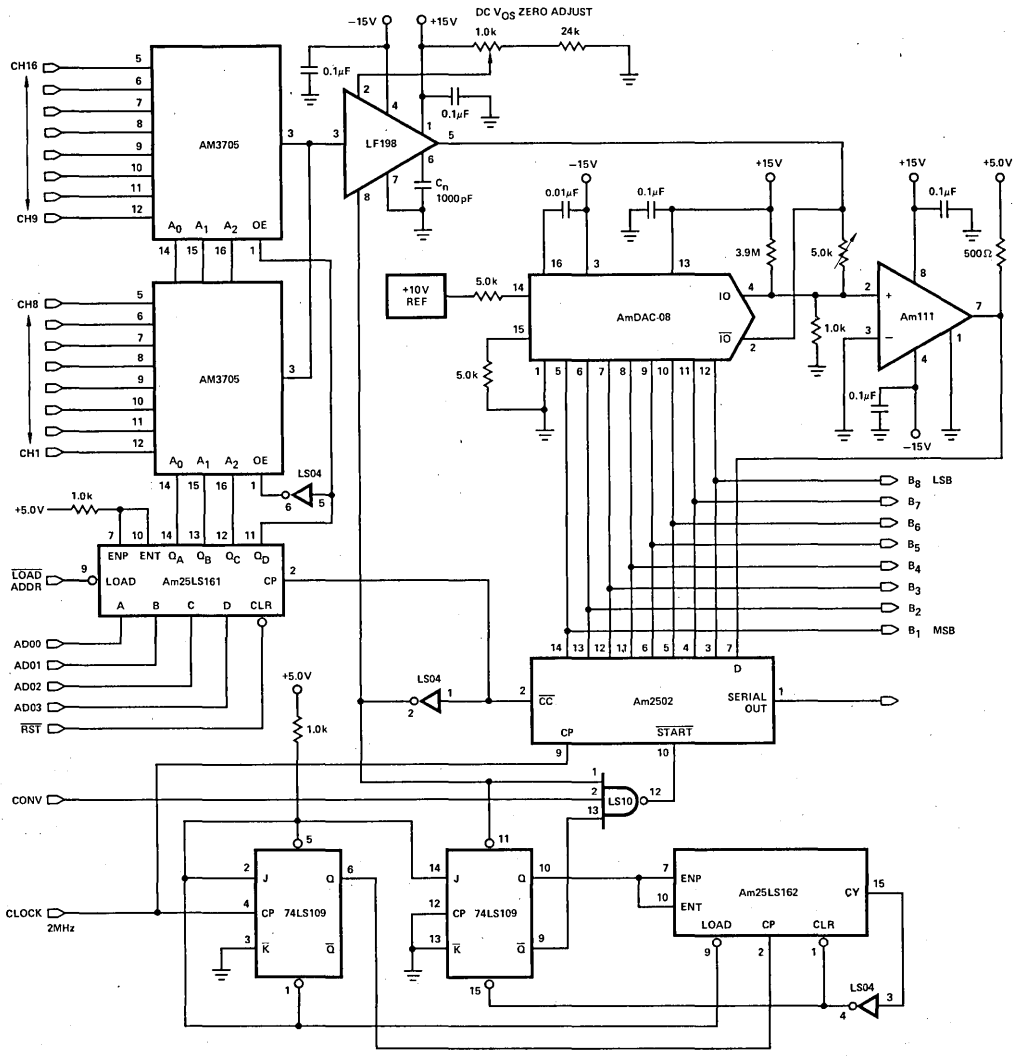
To adjust the DC offset zeroing, the wiper of a 1K potentiometer is connected to the offset adjust pin. One end of the potentiometer is connected to VCC and the other is connected through a resistor to ground. The value of the resistor is selected such that the current flows through it at approximately 6mA.

Metallization and Pad Layout

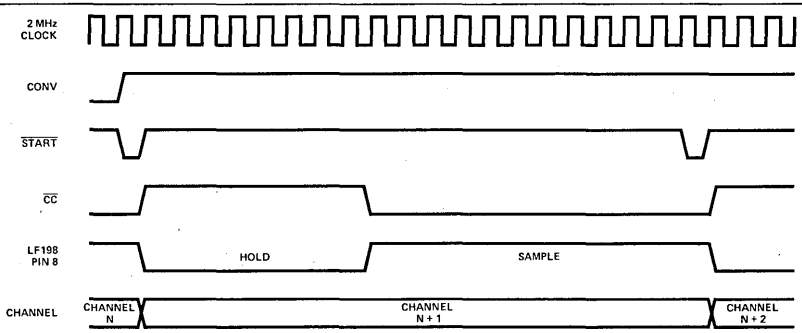


DIE SIZE: 0.051" X 0.070"

APPLICATIONS

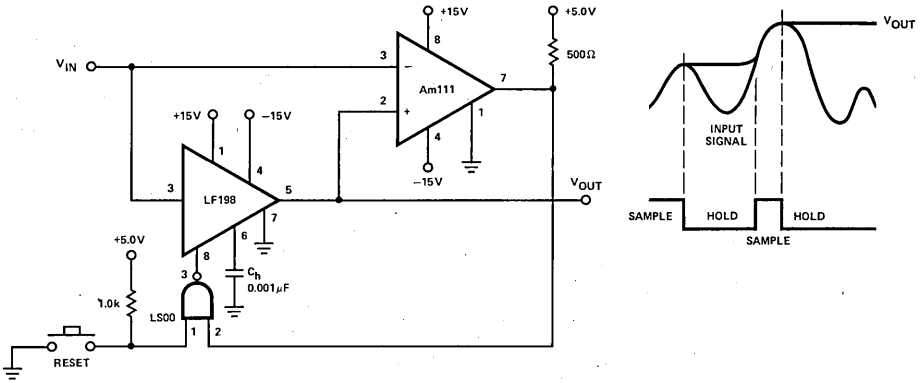


SEQUENTIAL ADDRESSING OVERLAP MODE A/D CONVERSION LIC-213



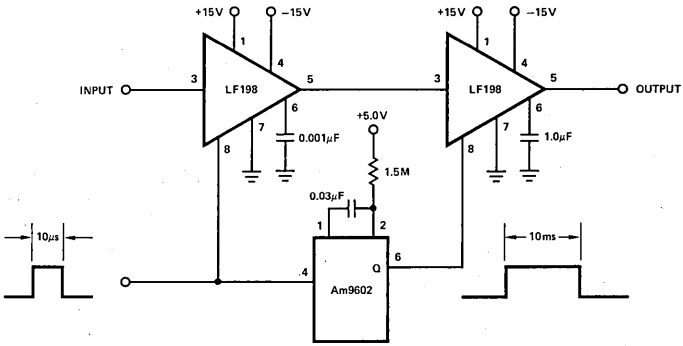
TIMING DIAGRAM FOR SEQUENTIAL ADDRESSING OVERLAP MODE A/D CONVERSION LIC-214

APPLICATIONS (Cont.)



TRACK AND HOLD PEAK RECORDER

LIC-215



FAST ACQUISITION, LOW DROOP SAMPLE AND HOLD

LIC-216

DEFINITION OF TERMS

Acquisition Time – The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture time – The delay between the command to hold and the actual opening of the hold switch.

Aperture time uncertainty – The tolerance, or jitter of the aperture time.

Droop rate – The rate of change of output voltage in the hold mode. It is caused by leakage currents at the hold capacitor node.

Feed-through – During hold, a small part of the input signal feeds through the capacitor of the switch to the hold capacitor and output. This is usually a function of the level and frequency of the input signal and is expressed in dB.

Dynamic sampling error – The error introduced into the outputs due to input voltage varying when the hold command is issued. Error is expressed in mV with a given hold capacitor.

Gain error – The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold step – The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage.

Am6420

High Speed 12-Bit Accurate Sample-and-Hold

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- Acquisition time 500ns (0.01%)
- Droop rate 20μV/μs
- Aperture delay 2ns
- Aperture uncertainty 200ps
- Gain bandwidth 15MHz
- Slew rate 50V/μs
- Sample to hold offset error 0.2mV
- Internal hold capacitor
- Connect in any standard op-amp configuration
- 12-bit accuracy
- Low output impedance over frequency

APPLICATIONS

- Precision data acquisition systems
- Data distribution systems
- Auto zeroing system
- Peak detector

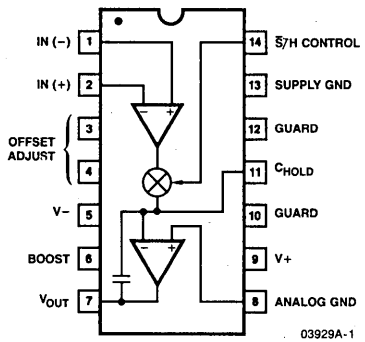
FUNCTIONAL DESCRIPTION

The Am6420 is a monolithic sample-and-hold circuit consisting of a gated high performance operational amplifier and an internal hold capacitor. The integrating connection of the internal capacitor yields a constant hold-step error, which is internally trimmed to a minimum value.

When the Am6420 is in the sample (or track mode), it behaves as an operational amplifier, and any of the standard op-amp feedback networks may be connected around it to control gain, frequency response, etc. When the device is put into the hold mode, its output remains at its last level before the hold signal. In many systems, the Am6420 may replace both an amplifier and a sample-and-hold.

The Am6420 offers a number of improvements over other monolithic, hybrid, and discrete sample-and-hold circuits. Accuracy is better than 0.01% over the full operating temperature range (0 to 70°C commercial, −55 to +125°C military), while dynamic characteristics include fast acquisition time, low droop rate, and a temperature compensated hold-step. High slew rate and bandwidth allow the device to be used at gains greater than unity, thus eliminating the need for a scaling amplifier.

BLOCK DIAGRAM



ORDERING INFORMATION*

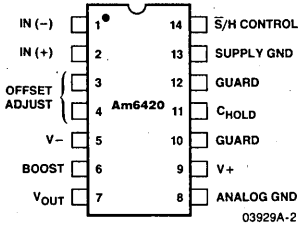
Part Number	Package Type	Temperature Range
Am6420DM	Hermetic DIP	−55 to 125°C
Am6420LM	Leadless**	−55 to 125°C
Am6420DC	Hermetic DIP	0 to 70°C
Am6420LC	Leadless**	0 to 70°C
Am6420XC	Dice	0 to 70°C

*Also available with burn-in processing. To order, add suffix B to the part number.

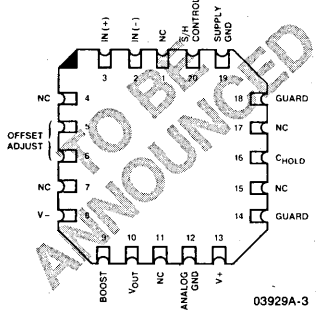
**Availability of Leadless packages will be announced.

CONNECTION DIAGRAMS – Top Views

D-14-1



Leadless Chip-Pak L-20-1



MAXIMUM RATINGS

Supply Voltage, V+ to Supply GND	−0.5 to +16.5V
V− to Supply GND	+0.5 to −16.5V
Max Differential V+ to V−	33V
Differential Input Voltage	25V
$\overline{S}$/H Control Voltage to Ground	−1 to +6V
Output Current	Short Circuit Protected
Operating Temperature Am6420DC	0 to 70°C
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering 60 Seconds)	300°C
Power Dissipation	700mW

ELECTRICAL CHARACTERISTICS $V+ = +15V, V- = -15V, T_A = 25°C$, unless otherwise stated.

Parameters	Description	Test Conditions	Min	Typ	Max	Units
GAIN AND ACCURACY						
A_E	Voltage Gain Error	$A_v = +1$		0.005		%
A	Gain Non-Linearity			0.005		%
INPUT CHARACTERISTICS						
R_{IN}	Input Resistance			5		MΩ
C_{IN}	Input Capacitance			5		pF
I_{OS}	Input Offset Voltage	25°C (On-Chip Trimmed)		±0.2		mV
$\Delta V_{OS}/\Delta t$	Input Offset Tempco			5		μV/°C
I_B	Bias Current	T_A=25°C		80		nA
I_{BM}	Bias Current	T_{MIN} to T_{MAX}		150		nA
V_{CM}	Input Voltage Range	$V_S = \pm15V$		±11		V
TRANSFER CHARACTERISTICS						
GBW	Gain Bandwidth Product			13		MHz
BW	Full Power Bandwidth	$10V_{p-p}$		1.2		MHz
$\Delta V/\Delta t$	Slew Rate	$10V_{p-p}$, C_H = 50pF		50		V/μs
C_{MR}	Common Mode Rejection Rate	V_{CM} = 10V, 1kHz		80		dB
SAMPLE/HOLD CHARACTERISTICS: ($T_A = 25°C$)						
t_{ACQ}	Acquisition Time			500		ns
t_{AD}	Aperture Delay Time			2		ns
t_{AU}	Aperture Uncertainty			200		ps
t_{HS}	Hold Settling Time	0.01%		30		ns
	Droop Rate 25°C			20		μV/μs
	Sample-to-Hold Offset Error, 25°C			0.2		mV
OUTPUT CHARACTERISTICS						
	Output Voltage			+11		V
				−6		
	Output Current	Can Be Externally Boosted		+10		mA
				−2		
	Output Resistance			1		Ω
	Max Load Capacitance			50		pF
	Supply Current			+20		mA
				−15		

PIN DESCRIPTION

IN(−)	The inverting input of the input amplifier.
IN(+)	The noninverting input of the input amplifier.
Offset Adjust	The offset adjust terminals of the input amplifier. A small differential current into these pins can be used to trim the V_{OS} of the input amp.
$\overline{S}$/H Control	This pin controls the internal switch to make the output either track the input ($\overline{S}$/H low) or hold the last value ($\overline{S}$/H high).
V_{OUT}	The output of the on-chip buffer amplifier.
C_{HOLD}	An external hold capacitor can be connected from V_{OUT} to this pin to improve droop rate. The C_{HOLD} pin should be surrounded by a guard ring connected to the guard pins.
Guard	These pins should be connected to the guard ring around the C_{HOLD} pin to prevent leakage. DO NOT connect guard to ground or to V_{OUT} as the guard voltage is internally generated.
Boost	An external resistor from this pin to the negative power supply can be used to increase the current sink capability of the output buffer.
Analog Ground	The output voltage is referenced to this pin; care should be taken to keep the ground free of noise.
Supply Ground	This ground pin should be connected to the system ground.
V+	The positive power supply pin.
V−	The negative power supply pin.

APPLICATIONS INFORMATION

The Am6420 may be connected in an op-amp configuration including voltage followers, inverting and noninverting amplifiers, and active filters. Examples of these connections are shown in Figures 1 through 4. These circuits are intended as examples only and may be changed to meet the exact needs of the system.

The Am6420 input offset voltage is internally trimmed to less than ±0.2mV; in most applications, this is an acceptable error and the offset adjust pins 3 and 4 should be left open. If better input offset is required, it can be adjusted using the circuit shown in Figure 5. With both input grounded, connect a square wave to the $\overline{S}$/H control and adjust the potentiometer for 0 volts at the output in hold mode.

The output sink capability of the Am6420 is nominally −2mA; this can be increased by connecting an external resistor from the boost pin (pin 6) to the negative power supply (pin 5). Boost current is calculated by:

$$I_{boost} = 1.2/R_{boost}$$

Total output sink current should not be more than 10mA, therefore boost current should be limited to 8mA.

The internal hold capacitor (50pF) is optimized for fast acquisition and minimum hold-step error. However, if improved droop rate is desired, an external hold capacitor can be connected from V_{OUT} (pin 7) to C_{HOLD} (pin 11). Acquisition time and droop rate are directly and indirectly proportional, respectively, to hold capacitance. For example, if an external 50pF capacitor were added, the total hold capacitance would be doubled. This would double the acquisition time and decrease the droop rate by 1/2. To maintain stability, a capacitor must be added from C_{HOLD} (pin 11) to ground; the value of this capacitor should be approximately 1/2 of the value of the external hold capacitor (Figure 6), and should be a low leakage type, such as a mica. The hold-step has been trimmed for the internal capacitor; when an external capacitor is used, offset adjustment may be needed to correct the hold-step.

LAYOUT CONSIDERATIONS

In order to take advantage of full accuracy of the Am6420, care should be taken to avoid system errors. One of the most common causes of errors in data acquisition systems is improper grounding. High frequency digital circuits should not be connected to the same ground trace as high accuracy analog circuits; separate ground paths should be provided for analog and digital signals and connected together at only one point in the system. The Am6420 provides two ground pins; all internal circuit grounds except the output amplifiers are connected to the power supply ground. The output amplifier is connected to the analog ground, which should also be used for output return. Recommended ground connections are shown in Figure 7.

To keep leakage current to a minimum and improve droop rate, the C_{HOLD} pin should be surrounded by a guard ring (Figure 8). This ring should be connected to pins 10 and 12 of the Am6420 and *must not be connected to ground or V_{OUT}* since the guard voltage is internally generated and connected to the guard pins.

The Am6420 provides excellent power rejection, however, system performance may be enhanced by proper power supply bypassing. A 0.1μF capacitor and a 10μF tantalum capacitor should be connected from the power supply pins to the power supply ground, as close to the pins as possible.

GLOSSARY OF TERMS

Acquisition Time: The time required for the hold capacitor to be charged to a full-scale value after the sample command is given.

Aperture Delay Time: The time elapsed between the sample command and the actual opening of the switch.

Aperture Uncertainty: The variation in aperture delay time from sample-to-sample.

Droop Rate: The rate at which the output voltage changes while in the hold mode. Droop is caused by the capacitor being discharged through the buffer amplifier's input circuit.

Hold Settling Time: The time required for the buffer output to settle within the specified accuracy band after the switch is opened.

Sample-to-Hold Offset Error: The difference in output voltage between the time-to-hold command is given and the time the output settles to its final value. It is caused by charge injection from the switch to the capacitor during the opening of the switch.

Figure 1. Am6420 in Unity Gain Sample-and-Hold Circuit

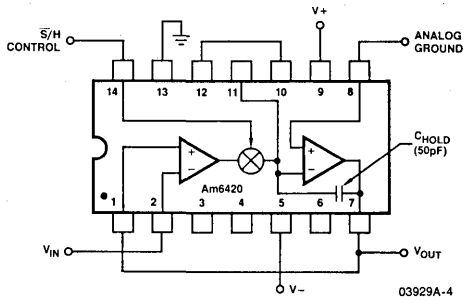


Figure 2. Am6420 Connected as a Noninverting Amplifier

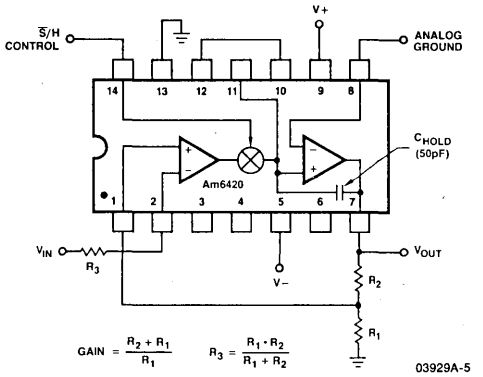


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Figure 3. Am6420 in an Inverting Amplifier Configuration

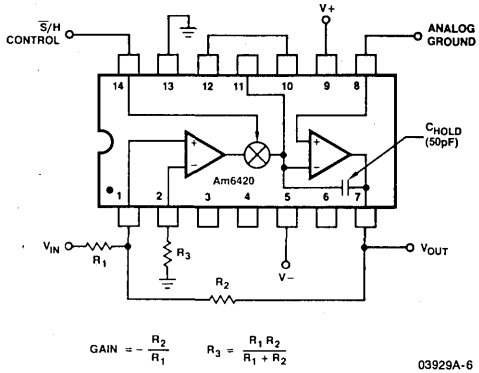


Figure 4. Am6420 in an Active Filter Circuit

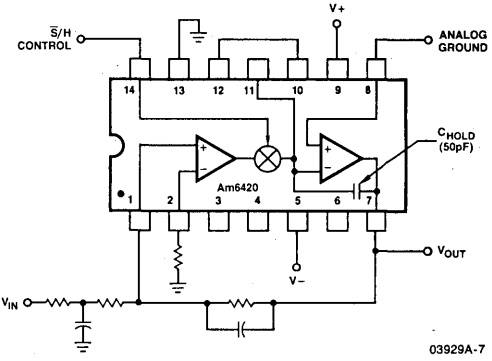


Figure 5. Am6420 V_{OS} Adjustment Circuit

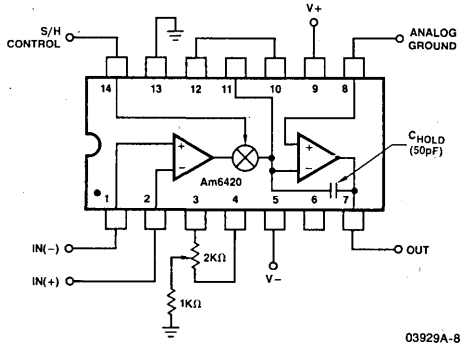


Figure 6. Am6420 with External C_{HOLD}

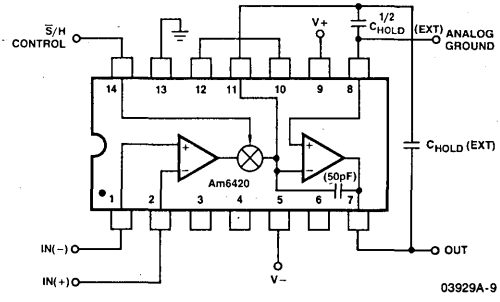


Figure 7. Data Acquisition System Grounding

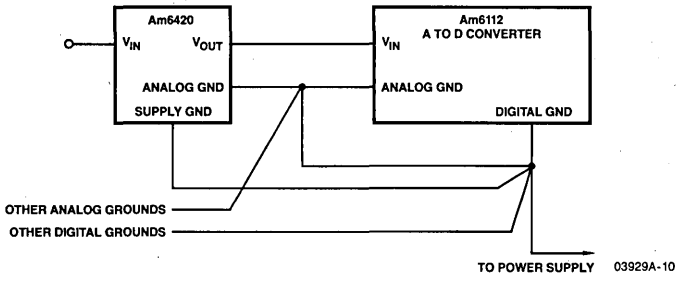
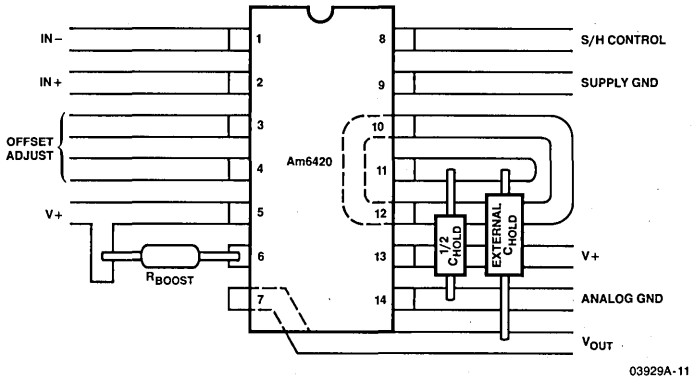


Figure 8. Pad Layout – Top View



Operational Amplifiers – Section V

LM108/208/308
LM108A/208A/308A
Operational Amplifiers

Description: The 108, 208, 308, 108A, 208A and 308A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalents to the National LM108, LM208, LM308, LM108A, LM208A and LM308A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

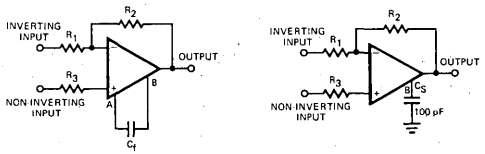
Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

These differential input, precision amplifiers provide low input current and offset voltage competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor and are pin-for-pin interchangeable with the 101A/201A/301A. The 108A, 208A, and 308A are high performance selections from the 108/208/308 amplifier family.

FUNCTIONAL DIAGRAM
Frequency Compensation Circuits



$$C_f \geq C_o\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

C_o = 30 pF

LIC-670

5

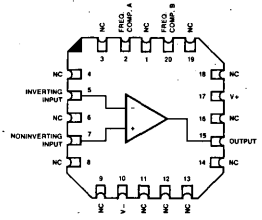
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LM308	Hermetic DIP	0 to +70°C	LM308D
	TO-99	0 to +70°C	LM308H
	Molded DIP	0 to +70°C	LM308N
	Dice	0 to +70°C	LD308
	Leadless	0 to +70°C	LM308L
LM308A	Hermetic DIP	0 to +70°C	LM308AD
	TO-99	0 to +70°C	LM308AH
	Molded DIP	0 to +70°C	LM308AN
	Dice	0 to +70°C	LD308A
	Leadless	0 to +70°C	LM308AL
LM208	Hermetic DIP	−25 to +85°C	LM208D
	TO-99	−25 to +85°C	LM208H
	Leadless	−25 to +85°C	LM208L
LM208A	Hermetic DIP	−25 to +85°C	LM208AD
	TO-99	−25 to +85°C	LM208AH
	Leadless	−25 to +85°C	LM208AL
LM108	Hermetic DIP	−55 to +125°C	LM108D
	TO-99	−55 to +125°C	LM108H
	Dice	−55 to +125°C	LD108
	Leadless	−55 to +125°C	LM108L
LM108A	Hermetic DIP	−55 to +125°C	LM108AD
	TO-99	−55 to +125°C	LM108AH
	Dice	−55 to +125°C	LD108A
	Leadless	−55 to +125°C	LM108AL

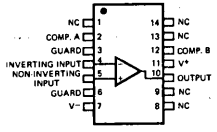
*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAMS – Top Views

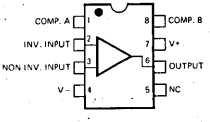
Leadless Chip-Pak
L-20-1



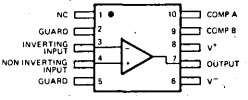
Molded Dual In-Line
P-14-1



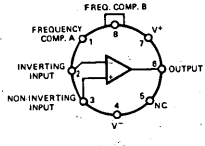
Hermetic Dual In-Line
D-18-1



Flat Package
F-10-1



Metal Can
H-8-1



Notes: 1. On Metal Can, pin 4 is connected to case.
2. On DIP pin 7 is connected to bottom of package.
3. On Flat Package, pin 6 is connected to bottom of package.

LIC-674

LM108/208/308 • LM108A/208A/308A
MAXIMUM RATINGS

Supply Voltage	
LM108, 208, 108A, 208A,	±20 V
LM308, 308A	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM108, 108A	−55°C to +125°C
LM208, 208A	−25°C to +85°C
LM308, 308A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

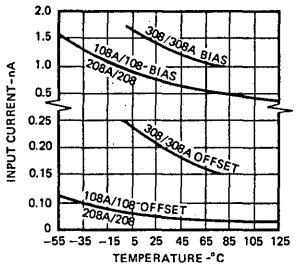
ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise specified (see Note 4)

		LM308			LM308A			LM108 LM208			LM108A LM208A			
Parameters	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20V								0.3	0.6		0.3	0.6	mA
	V_S = ±15V		0.3	0.8		0.3	0.8							
Large Signal Voltage Gain	V_S = ±15V V_{OUT} = ±10V $R_L \geq 10k\Omega$	25	300		80	300		50	300		80	300		V/mV
The Following Specifications Apply over the Operating Temperature Ranges														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	3.0		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15V V_{OUT} = ±10V $R_L \geq 10k\Omega$	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15V R_L = 10kΩ	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	V_S = ±20V T = T_A Max								0.15	0.4		0.15	0.4	mA
	V_S = ±15V T = T_A Max		0.6	1.0		0.6	0.8							

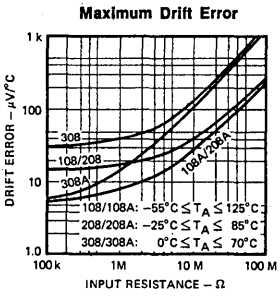
Notes:
1. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9mW/°C for operation at ambient temperatures above 95°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 to ±20V for the 108, 208, 108A and 208A and from ±5 to ±15V for the 308 and 308A.

TYPICAL PERFORMANCE CURVES

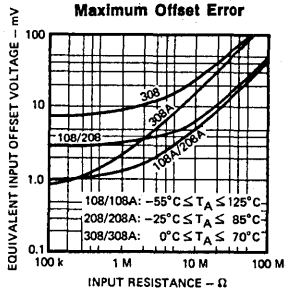
Input Currents



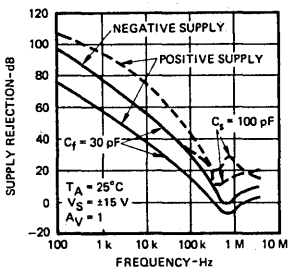
Maximum Drift Error



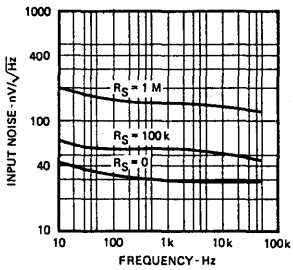
Maximum Offset Error



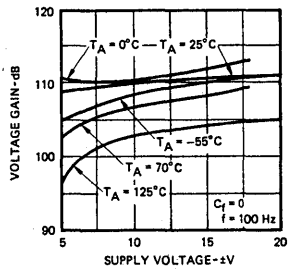
Power Supply Rejection



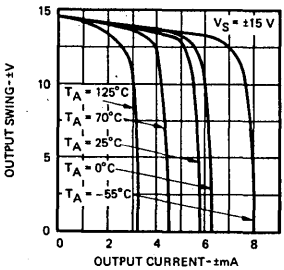
Input Noise Voltage



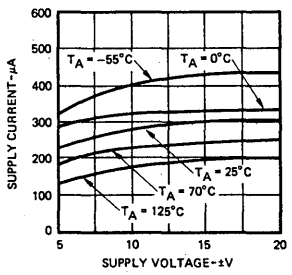
Voltage Gain



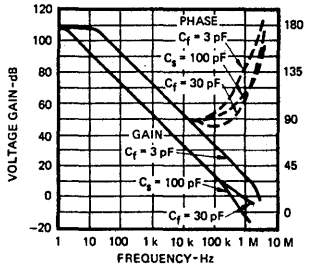
Output Swing



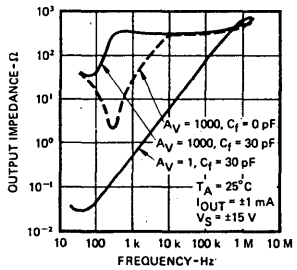
Supply Current



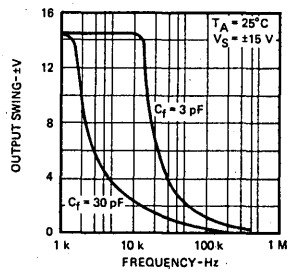
Open Loop Frequency Response



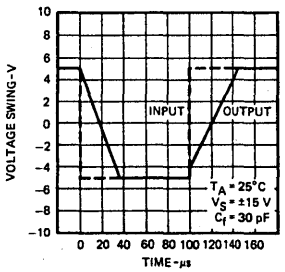
Closed Loop Output Impedance



Large Signal Frequency Response



Voltage Follower Pulse Response



LIC-675

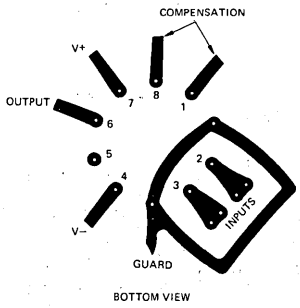
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)

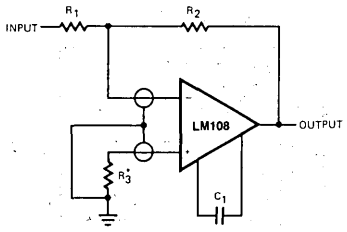


BOTTOM VIEW

Board layout for Input Guarding with TO-99 package.

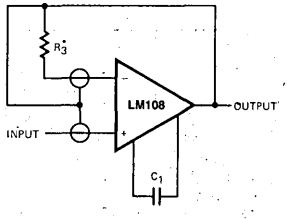
APPLICATIONS

Connection of Input Guards



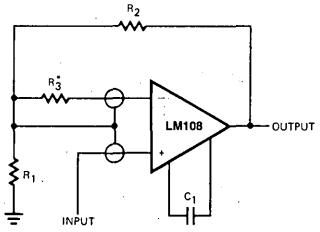
INVERTING AMPLIFIER

LIC-671



FOLLOWER

LIC-672



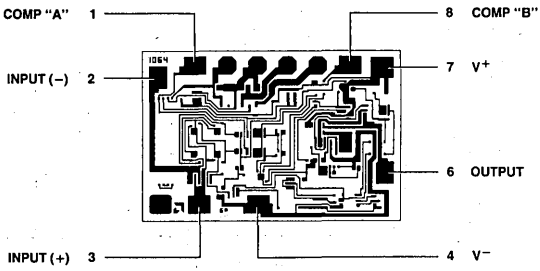
NON-INVERTING AMPLIFIER

LIC-673

*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.046" X 0.068"

LM118/218/318

High-Speed Operational Amplifier

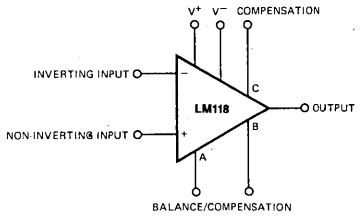
Distinctive Characteristics

- The LM118/218/318 are functionally, electrically, and pin-for-pin equivalent to the National LM118/218/318
- Slew rate: 70V/μs
- Small signal bandwidth: 15MHz
- Internal frequency compensation
- Supply voltage range: ±5V to ±20V
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Available in metal can, hermetic dual-in-line, hermetic flat package or plastic minidip.

FUNCTIONAL DESCRIPTION

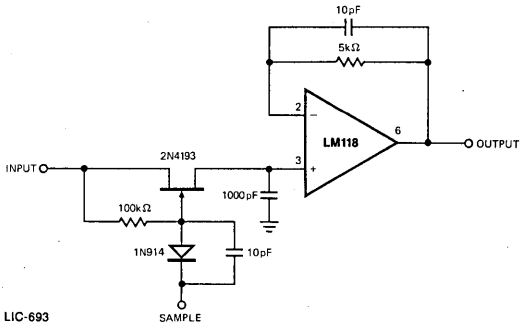
The LM118/218/318 are internally compensated high-speed operational amplifiers featuring minimum slew rate of 50V/μs, low input bias currents, large input voltage range and excellent performance over a wide range of supply voltages and temperature. They have provision for increased speeds when operating in the inverting mode.

FUNCTIONAL DIAGRAM



LIC-692

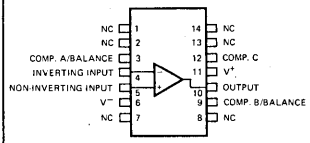
TYPICAL APPLICATIONS
Fast Sample and Hold



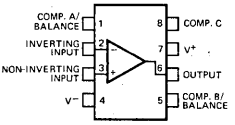
LIC-693

CONNECTION DIAGRAMS – Top Views

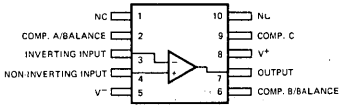
Hermetic Dual In-Line D-14-1



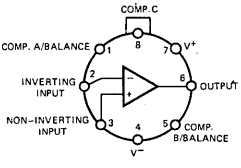
Molded Dual In-Line P-8-1



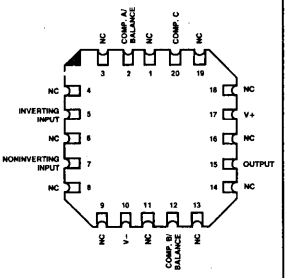
Flat Package F-10-1



Metal Can H-8-1



Leadless Chip-Pak L-20-1



Note: 1. On Metal Can, pin 4 is connected to case.

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ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LM318	Metal Can	0 to +70°C	LM318H
	Hermetic DIP	0 to +70°C	LM318D
	Flat Package	0 to +70°C	LM318F
	Molded DIP	0 to +70°C	LM318N
	Dice	0 to +70°C	LD318
	Leadless	0 to +70°C	LM318L
LM218	Metal Can	−25 to +85°C	LM218H
	Hermetic DIP	−25 to +85°C	LM218D
	Flat Pak	−25 to +85°C	LM218F
	Leadless	−25 to +85°C	LM218L
LM118	Metal Can	−55 to +125°C	LM118H
	Hermetic DIP	−55 to +125°C	LM118D
	Flat Package	−55 to +125°C	LM118F
	Dice	−55 to +125°C	LD118
	Leadless	−55 to +125°C	LM118L

*Also available with burn-in processing. To order add suffix B to part number.

5

LM118/218/318
MAXIMUM RATINGS

Supply Voltage	±20V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage (Note 2)	±5V
Input Voltage (Note 3)	±15V,
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM118	−55°C to +125°C
LM218	−25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

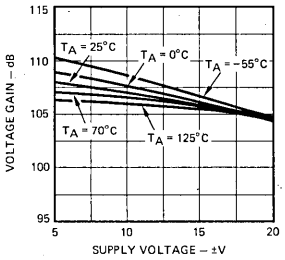
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	LM318 Min.	LM318 Typ.	LM318 Max.	LM118/LM218 Min.	LM118/LM218 Typ.	LM118/LM218 Max.	Units
Input Offset Voltage	$R_S \leq 5k\Omega$		4	10		2	4	mV
Input Offset Current			30	200		6	50	nA
Input Bias Current			150	500		120	250	nA
Input Resistance		0.5	3		1.0	3		MΩ
Supply Current	V_S = ±20V		5	10		5	8	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2k\Omega$	25	200		50	200		V/mV
Slew Rate	A_V = +1, V_S = ±15V (Fig.1) R_L = 2kΩ, C_L = 30pF	50	70		50	70		V/μs
Small Signal Bandwidth	V_S = ±15V		15			15		MHz
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 5k\Omega$			15			6	mV
Input Offset Current				300			100	nA
Input Bias Current				750			500	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2k\Omega$	20			25			V/mV
Input Voltage Range	V_S = ±15V	±11.5			±11.5			V
Common Mode Rejection Ratio	$R_S \leq 5k\Omega$	70			80			dB
Supply Voltage Rejection Ratio	$R_S \leq 5k\Omega$	65			70			dB
Output Voltage Swing	V_S = ±15V, R_L = 2kΩ	±12	±13		±12	±13		V
Supply Current	V_S = ±20V, T_A = 125°C						7	mA

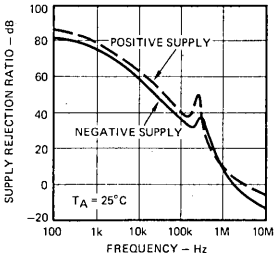
Notes:
1. Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.
2. The inputs are shunted with diodes for overvoltage protection. To limit the current in the protection diodes, resistances of 2 kΩ or greater should be inserted in series with the input leads for differential input voltages greater than ±5 V.
3. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V.

PERFORMANCE CURVES

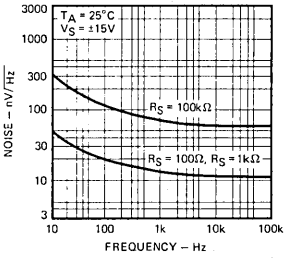
Voltage Gain



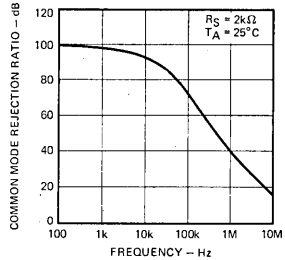
Power Supply Rejection



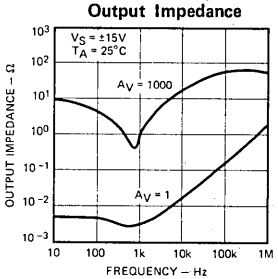
Input Noise Voltage



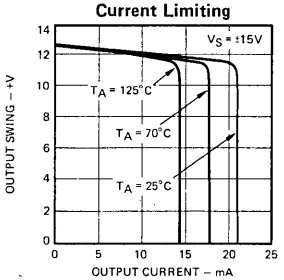
Common Mode Rejection



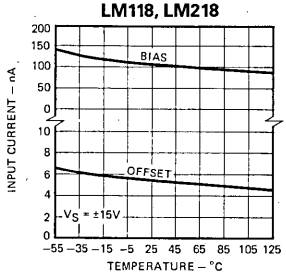
Closed Loop Output Impedance



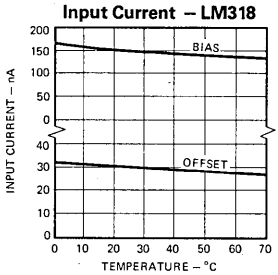
Current Limiting



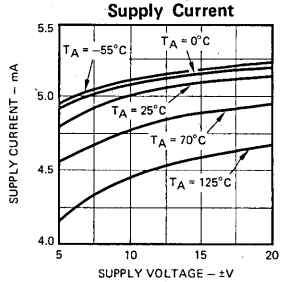
Input Current LM118, LM218



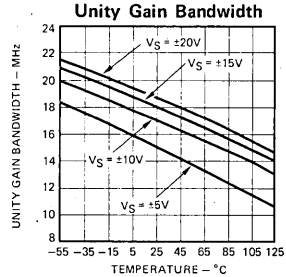
Input Current – LM318



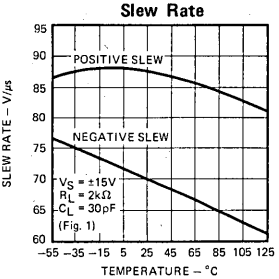
Supply Current



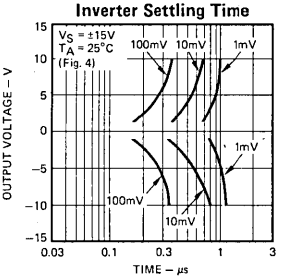
Unity Gain Bandwidth



Voltage Follower Slew Rate



Inverter Settling Time



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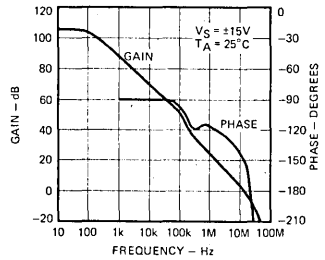
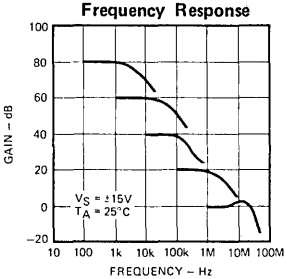
PERFORMANCE CURVES

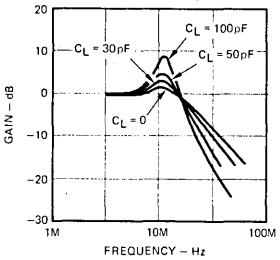
Open Loop Frequency Response



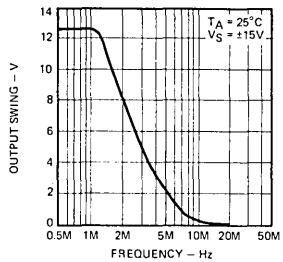
Closed Loop Frequency Response



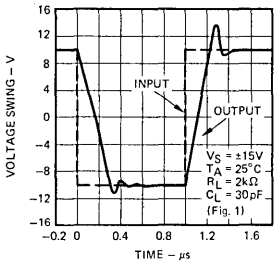
Effect of Capacitive Loading on Closed Loop Frequency Response



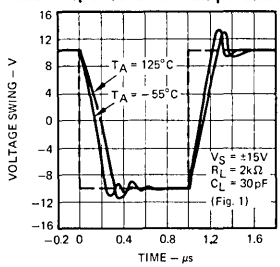
Large Signal Frequency Response



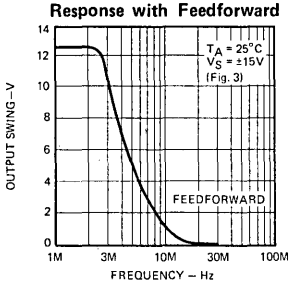
Voltage Follower Pulse Response



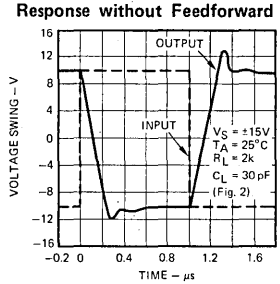
Voltage Follower Pulse Response Over Temperature



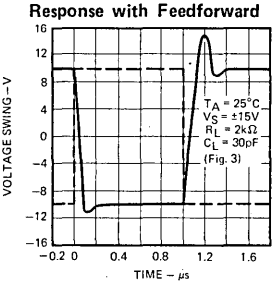
Large Signal Frequency Response with Feedforward



Inverter Pulse Response without Feedforward



Inverter Pulse Response with Feedforward



The high gain and large bandwidth of the LM118 make it mandatory to observe the following precautions in using the device, as is the case with any high-frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance at the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to minimum, or the amplifier must be isolated as shown in the applications.

LIC-696

APPLICATIONS

Voltage Follower (Slew Rate Test Circuit)

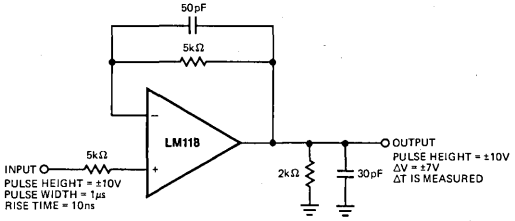


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Figure 1

Inverter

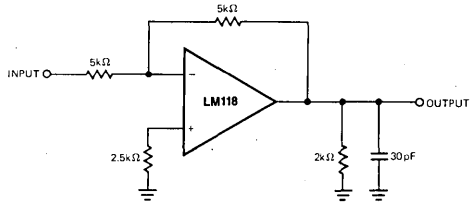
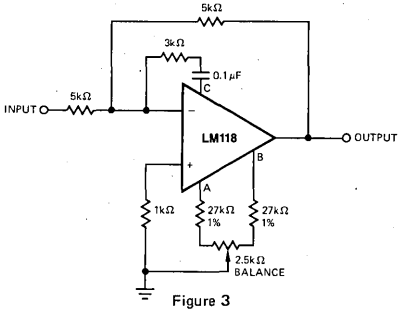


Figure 2

LIC-698

Inverter with Feedforward Compensation for Higher Slew Rate



LIC-699

Figure 3

Compensation for Minimum Settling Time

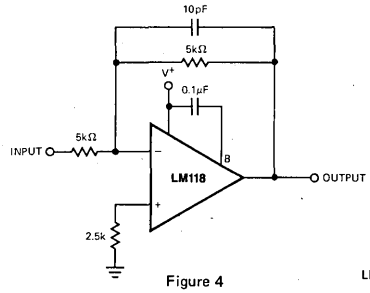
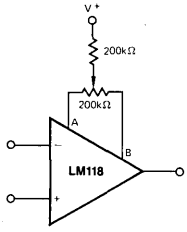


Figure 4

LIC-700

Offset Nulling



LIC-701

Figure 5

Isolating Large Capacitive Loads

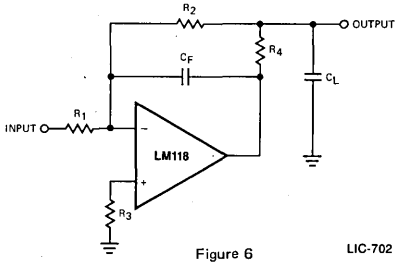


Figure 6

LIC-702

Over Compensation

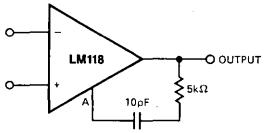
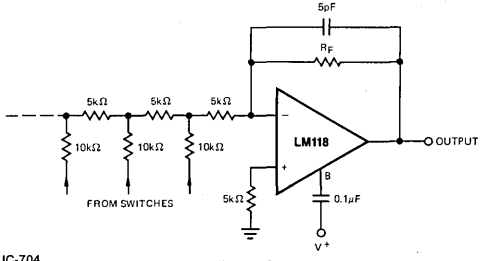


Figure 7

LIC-703

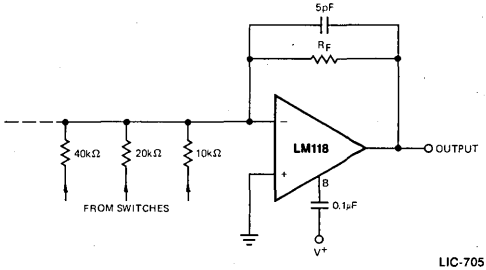
D/A Converter with Ladder Network



LIC-704

Figure 8

D/A Converter with Binary Network



LIC-705

ADDITIONAL APPLICATIONS

High Speed Summing Amplifier with Low Input Bias Currents

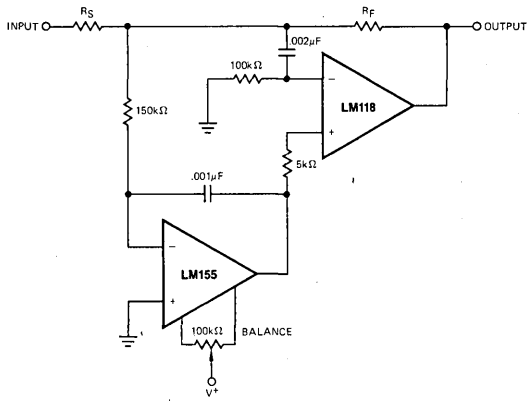
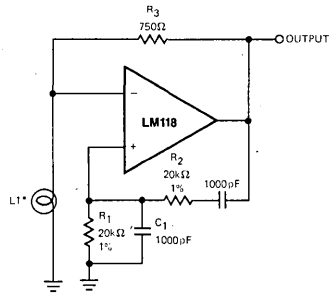


Figure 10

LIC-706

Wien Bridge Oscillator



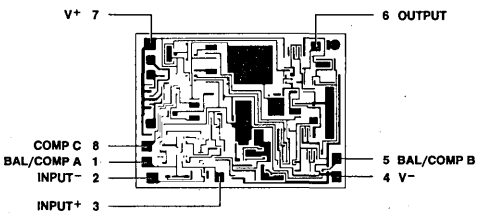
L1—10V—14mA
bulb ELDEMA 1869
R1 = R_2
C1 = C_2

$$f = \frac{1}{2\pi R1C1}$$

Figure 11

LIC-707

Metalization and Pad Layout



DIE SIZE: 0.065″ X 0.087″

LM148

Quad 741 Operational Amplifiers

Distinctive Characteristics

- 741 op amp operating characteristics
- Low supply current drain – 0.6mA/amplifier
- Class AB output stage – no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage – 1.0mV
- Low input offset current – 4.0nA
- Low input bias current – 30nA
- Gain bandwidth product
  LM148 (unity gain) – 1.0MHz
- High degree of isolation between amplifiers – 120dB
- Overload protection for inputs and outputs

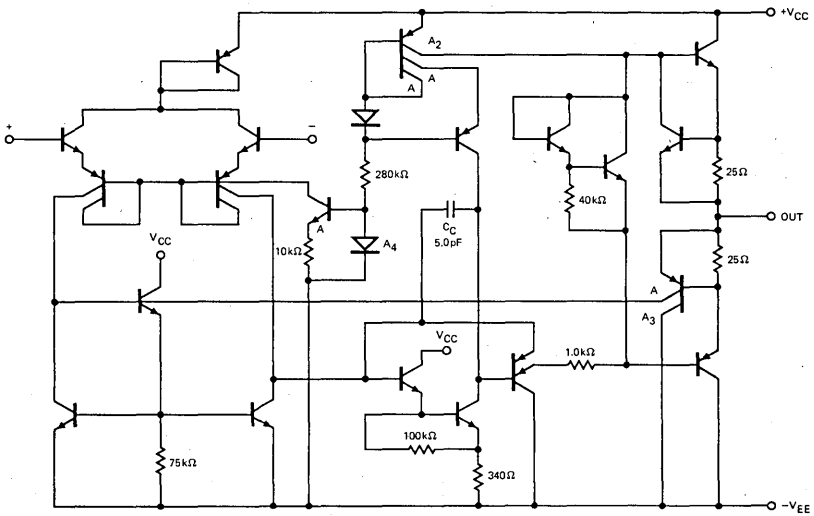
FUNCTIONAL DESCRIPTION

The LM 148 is a true quad 741. It consists of four independent, high gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The Am148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

5

SCHEMATIC DIAGRAM (Each Amplifier)



LIC-712

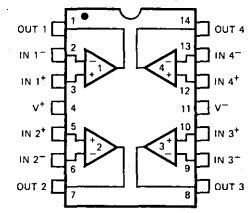
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LM348	Hermetic DIP	0 to +70°C	LM348D
	Molded DIP	0 to +70°C	LM348N
	Dice	0 to +70°C	LD348
	Leadless	0 to +70°C	LM318L
LM248	Hermetic DIP	−25 to +85°C	LM248D
	Leadless	−25 to +85°C	LM248L
LM148	Hermetic DIP	−55 to +125°C	LM148D
	Dice	−55 to +125°C	LD148
	Leadless	−55 to +125°C	LM148L

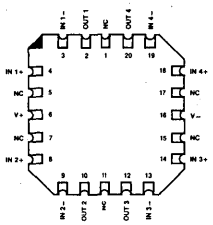
*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAMS – Top Views

Hermetic and Molded DIP
P-14-1, D-14-1



Leadless Chip-Pak
L-20-1



Note: Pin 1 is marked for orientation.

LIC-713

LM148
ABSOLUTE MAXIMUM RATINGS

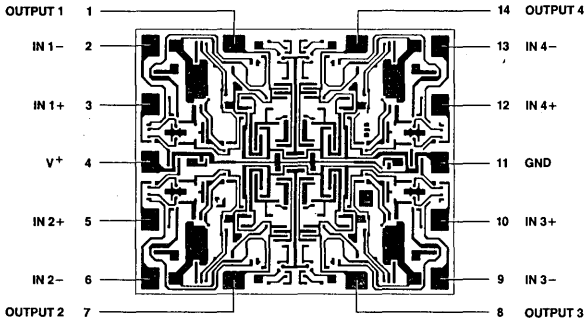
	LM148	LM248	LM348
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage	±22V	±18V	±18V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) — P_d		570mW	500mW
— θ_{jA}		150°C/W	150°C/W
Cavity DIP (D) (J) — P_d	900mW	900mW	900mW
— θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature ($T_{jmax.}$)	150°C	110°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS (Note 3)

Parameters	Conditions		LM148 Min.	LM148 Typ.	LM148 Max.	LM248 Min.	LM248 Typ.	LM248 Max.	LM348 Min.	LM348 Typ.	LM348 Max.	Units
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10k\Omega$			1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$			4.0	25		4.0	50		4.0	50	nA
Input Bias Current	$T_A = 25°C$			30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$		0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = ±15V$			2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$, $V_{OUT} = ±10V$, $R_L \geq 2.0k\Omega$		50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1.0Hz to 20kHz (Input Referred)			−120			−120			−120		dB
Small Signal Bandwidth	$T_A = 25°C$	Am148 Series		1.0			1.0			1.0		MHz
Phase Margin	$T_A = 25°C$	Am148 Series ($A_V = 1$)		60			60			60		degrees
Slew Rate	$T_A = 25°C$	Am148 Series ($A_V = 1$)		0.5			0.5			0.5		V/μs
Output Short Circuit Current	$T_A = 25°C$			25			25			25		mA
Input Offset Voltage	$R_S \leq 10k\Omega$				6.0			7.5			7.5	mV
Input Offset Current					75			125			100	nA
Input Bias Current					325			500			400	nA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$, $R_L > 2.0k\Omega$		25			15			15			V/mV
Output Voltage Swing	$V_S = ±15V$	$R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		V
		$R_L = 2.0k\Omega$	±10	±12		±10	±12		±10	±12		
Input Voltage Range	$V_S = ±15V$		±12			±12			±12			V
Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$		70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10k\Omega$		77	96		77	96		77	96		dB

Notes:
1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
2. The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jmax}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jmax} - T_A)/\theta_{jA}$ or the 25°C P_{dmax}, whichever is less. Derate Dual In-Line package at 9mW/°C for operation at ambient temperatures above 95°C, plastic 6.8mW/°C above 75°C, leadless 10mW/°C above 100°C.
3. These specifications apply for $V_S = ±15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.
4. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.061" X 0.073"

LF155/LF156

Monolithic JFET Input Operational Amplifiers

DISTINCTIVE CHARACTERISTICS

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- Internal compensation and large differential input voltage capability

GENERAL DESCRIPTION

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

The LF155, LF156 series are direct replacements for National LF155, LF156 series.

COMMON FEATURES
(LF155A, LF156A)

Low input bias current	30pA
Low input offset current	3.0pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1.0mV
Low input offset voltage temperature drift	$3.0\mu V/^{\circ}C$
Low input noise current	$0.01pA/\sqrt{Hz}$
High common-mode rejection ratio	100dB
Large dc voltage gain	106dB

UNCOMMON FEATURES

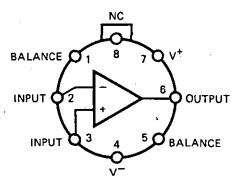
	LF155A	LF156A	Units
Extremely fast settling time to 0.01%	4.0	1.5	μs
Fast slew rate	5.0	12	$V/\mu s$
Wide gain bandwidth	2.5	5.0	MHz
Low input noise voltage	20	12	$nV/\sqrt{Hz}$

APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

CONNECTION DIAGRAM
Top View

Metal Can
H-8-1



Note: 1. Pin 4 is connected to case.

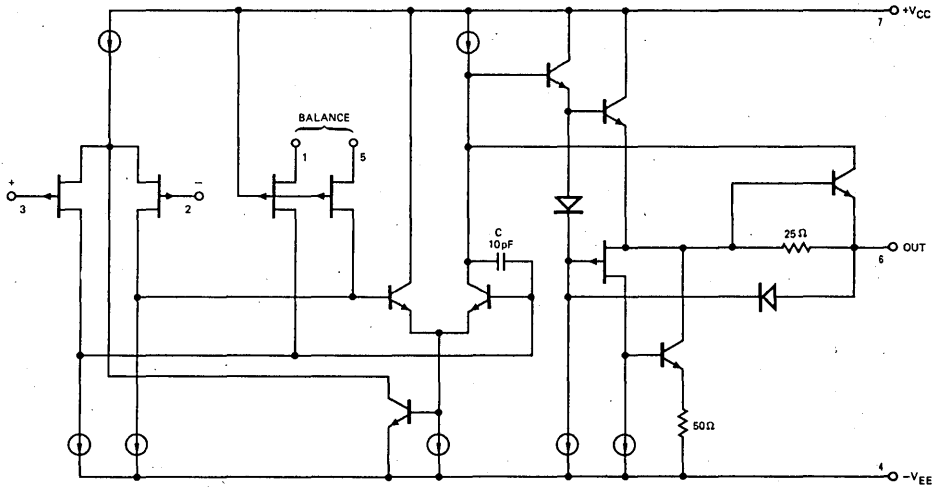
LIC-714

ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LF355	Metal Can	0°C to +70°C	LF355H
	Dice	0°C to +70°C	LD355
LF255	Metal Can	−25°C to +85°C	LF255H
LF155	Metal Can	−55°C to +125°C	LF155H
	Dice	−55°C to +125°C	LD155
LF355A	Metal Can	0°C to +70°C	LF355AH
	Dice	0°C to +70°C	LD355A
LF155A	Metal Can	−55°C to +125°C	LF155AH
	Dice	−55°C to +125°C	LD155A
LF356	Metal Can	0°C to +70°C	LF356H
	Dice	0°C to +70°C	LD356
LF256	Metal Can	−25°C to +85°C	LF256H
LF156	Metal Can	−55°C to +125°C	LF156H
	Dice	−55°C to +125°C	LD156
LF356A	Metal Can	0°C to +70°C	LF356AH
	Dice	0°C to +70°C	LD356A
LF156A	Metal Can	−55°C to +125°C	LF156AH
	Dice	−55°C to +125°C	LD156A

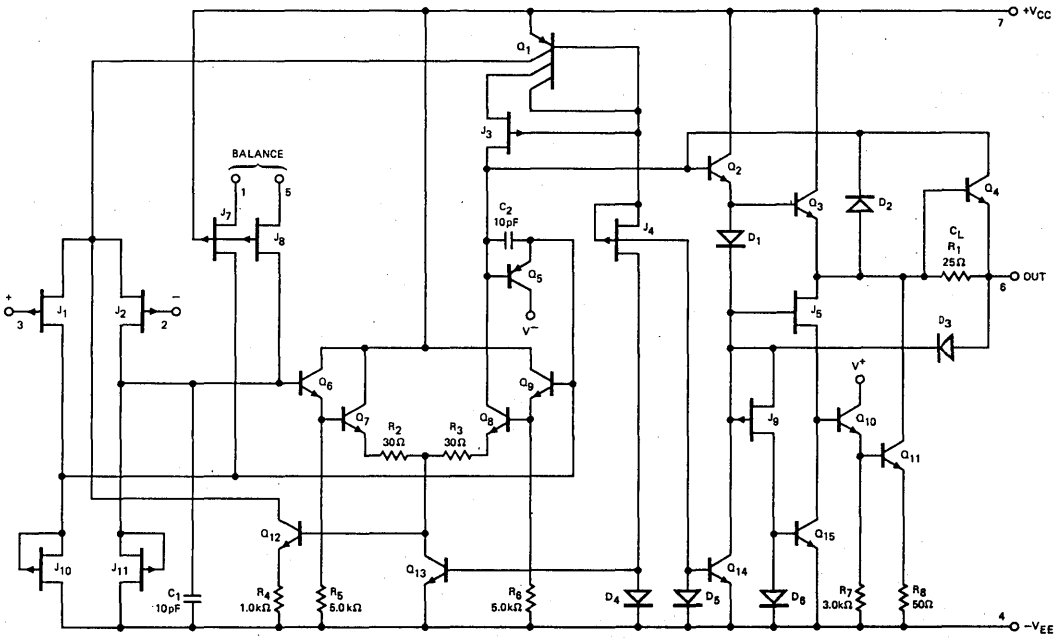
*Also available with burn-in processing. To order, add suffix B to part number.

SIMPLIFIED SCHEMATIC



LIC-715

DETAILED SCHEMATIC



LIC-716

LF155/LF156
ABSOLUTE MAXIMUM RATINGS

	LF155A/6A	LF155/6	LF355A/6A	LF355/6
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H Package)	670mW	670mW	570mW	500mW
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
$T_{J(Max.)}$	150°C	150°C	115°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Note 3)
DC CHARACTERISTICS

Parameters	Description	Test Conditions	LF155A/6A Min.	LF155A/6A Typ.	LF155A/6A Max.	LF355A/6A Min.	LF355A/6A Typ.	LF355A/6A Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1.0	2.0		1.0	2.0	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3.0			3.0		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Note 3, 5)		3.0	10		3.0	10	pA
		$T_J \leq T_{HIGH}$			10			1.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J < T_{HIGH}$			25			5.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = ±15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = ±10V$, $R_L = 2k\Omega$ Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = ±15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		Volts
		$V_S = ±15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = ±15V$	±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE
AC CHARACTERISTICS ($T_A = +25°C$, $V_S = ±15V$)

Parameters	Description	Test Conditions	LF155A/355A Min.	LF155A/355A Typ.	LF155A/355A Max.	LF156A/356A Min.	LF156A/356A Typ.	LF156A/356A Max.	Units
SR	Slew Rate	LF155A/6A: $A_V = 1$,	3.0	5.0		10	12		V/µs
GBW	Gain-Bandwidth Product			2.5		4.0	4.5		MHz
t_S	Settling Time to 0.01%	(Note 7)		4.0			1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 100Hz		25			15		nV/√Hz
		f = 1000Hz		20			12		
i_n	Equivalent Input Noise Current	f = 100Hz		0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01		
C_{IN}	Input Capacitance			3.0			3.0		pF

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

DC CHARACTERISTICS (Note 3)

Parameters	Description	Test Conditions	LF155/6 Min.	LF155/6 Typ.	LF155/6 Max.	LF255/6 Min.	LF255/6 Typ.	LF255/6 Max.	LF355/6 Min.	LF355/6 Typ.	LF355/6 Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3.0	5.0		3.0	5.0		3.0	10	mV
		Over Temperature			7.0			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5.0			5.0			5.0		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_J = 25°C$, (Notes 3, 5)		3.0	20		3.0	20		3.0	50	pA
		$T_J \leq T_{HIGH}$			20			1.0			2.0	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5.0			8.0	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		25	200		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$ Over Temperature	25			25			15			
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k\Omega$	±12	±13		±12	±13		±12	±13		Volts
		$V_S = \pm15V$, $R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1 −12		±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm15V$)

Parameters	LF155A/355A LF155/255 Typ.	LF155A/355A LF155/255 Max.	LF355 Typ.	LF355 Max.	LF156A LF156/256 Typ.	LF156A LF156/256 Max.	LF356A/356 Typ.	LF356A/356 Max.	Units
Supply Current	2.0	4.0	2.0	4.0	5.0	7.0	5.0	10	mA

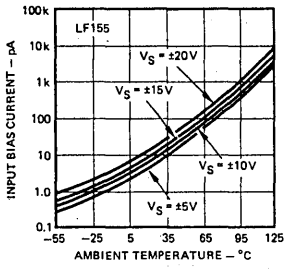
AC CHARACTERISTICS ($T_A = +25°C$, $V_S = \pm15V$)

Parameters	Description	Test Conditions	LF155/255/ LF355 Typ.	LF156/256 Min.	LF156/256/ LF356 Typ.	Units
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5.0	7.5	12	V/μs
GBW	Gain-Bandwidth Product		2.5		5.0	MHz
t_s	Settling Time to 0.01%	(Note 7)	4.0		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 100Hz	25		15	$nV/\sqrt{Hz}$
		f = 1000Hz	20		12	
i_n	Equivalent Input Noise Current	f = 100Hz	0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000Hz	0.01		0.01	
C_{IN}	Input Capacitance		3.0		3.0	pF

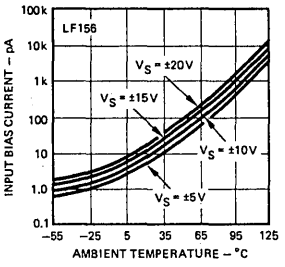
Notes:
1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. These specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A and the LF155/6. For the LF255/6, these specifications apply for $\pm15V \leq V_S \leq \pm20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A, these specifications apply for $\pm15V \leq V_S \leq \pm20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6 these specifications apply for $V_S = \pm15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
4. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
5. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}Pd$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
6. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
7. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

TYPICAL DC PERFORMANCE CHARACTERISTICS

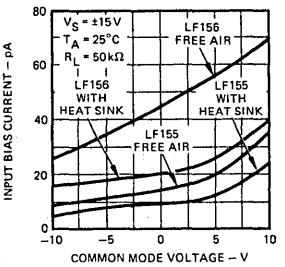
Input Bias Current



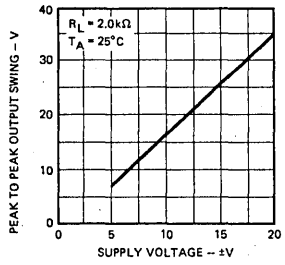
Input Bias Current



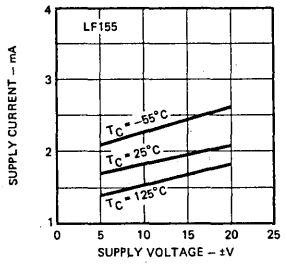
Input Bias Current



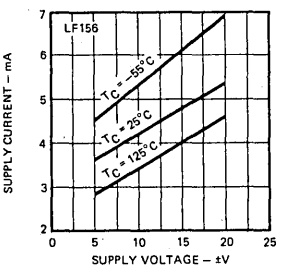
Voltage Swing



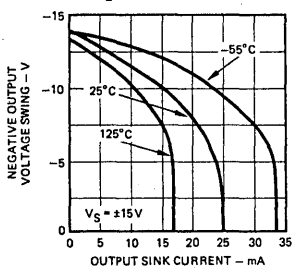
Supply Current



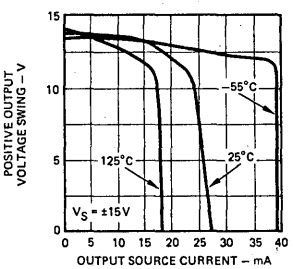
Supply Current



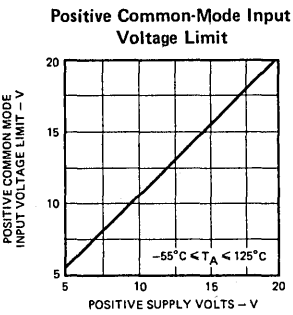
Negative Current Limit



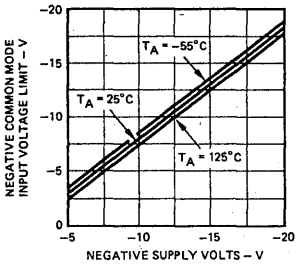
Positive Current Limit



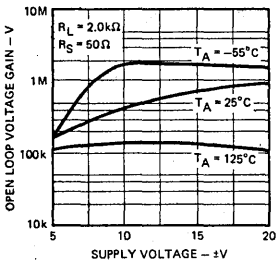
Positive Common-Mode Input Voltage Limit



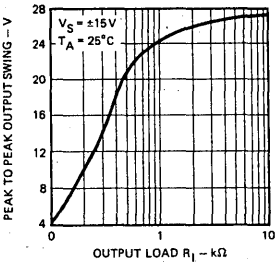
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



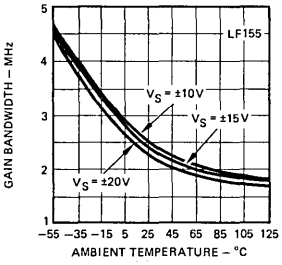
Output Voltage Swing

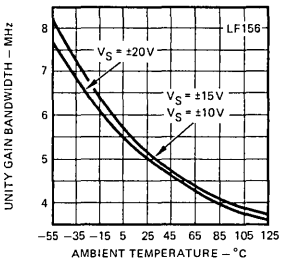


LIC-717

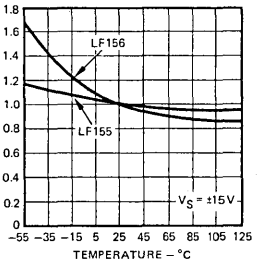
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

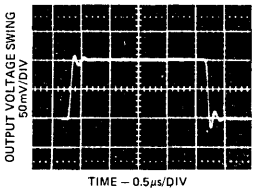




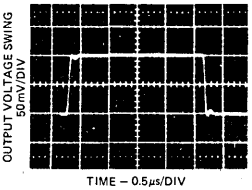
Normalized Slew Rate



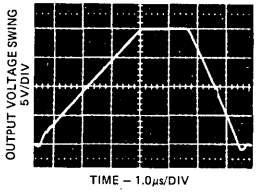
LF155 Small Signal Pulse Response, A_V = +1



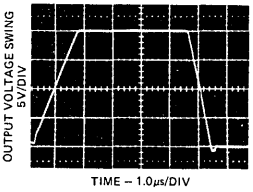
LF156 Small Signal Pulse Response, A_V = +1



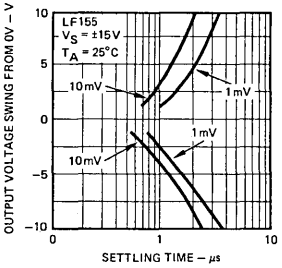
LF155 Large Signal Pulse Response, A_V = +1



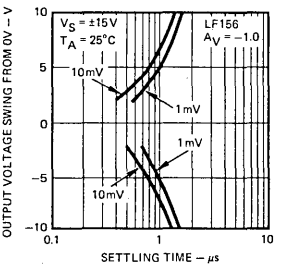
LF156 Large Signal Pulse Response, A_V = +1



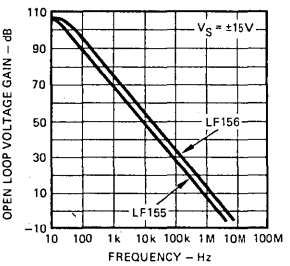
Inverter Settling Time



Inverter Settling Time



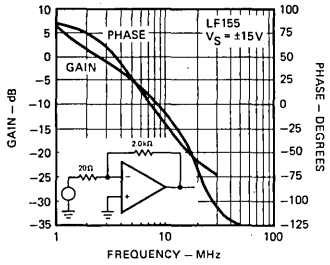
Open Loop Frequency Response



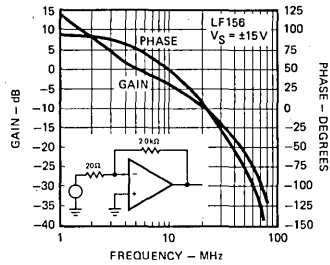
LIC-718

TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont.)

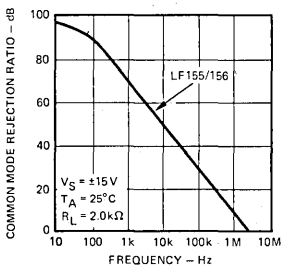
Bode Plot



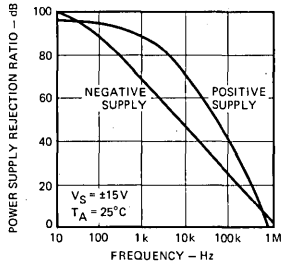
Bode Plot



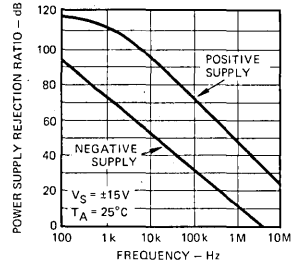
Common-Mode Rejection Ratio



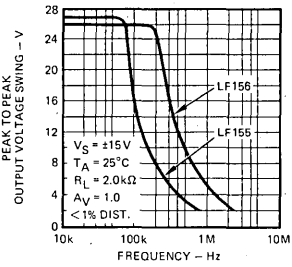
Power Supply Rejection Ratio (LF155)



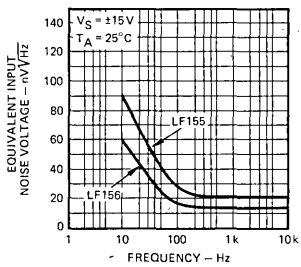
Power Supply Rejection Ratio (LF156)



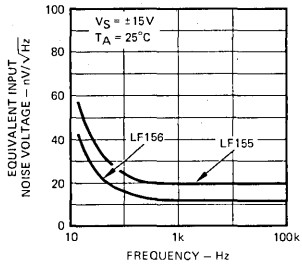
Undistorted Output Voltage Swing



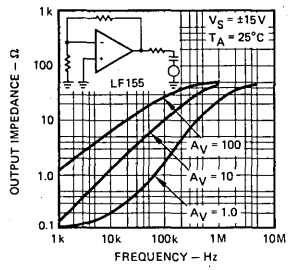
Equivalent Input Noise Voltage



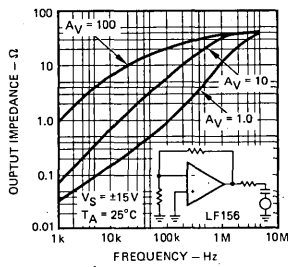
Equivalent Input Noise Voltage (Expanded Scale)



Output Impedance



Output Impedance



LIC-719

APPLICATION HINTS

The LF155/6 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

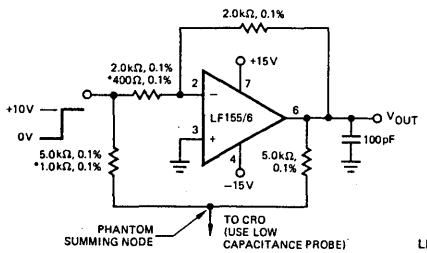
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

5

TYPICAL CIRCUIT CONNECTIONS AND PAD LAYOUT

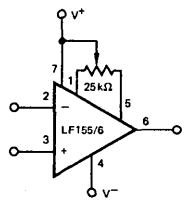
Settling Time Test Circuit



LIC-722

Settling time is tested with the LF155/156 connected as unity gain inverter Output = 10V step.

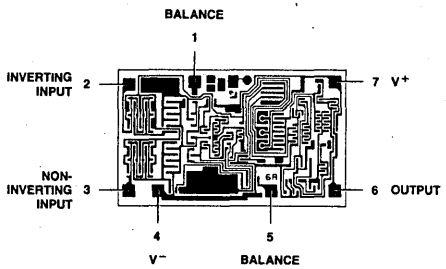
V_{OS} Adjustment



LIC-720

V_{OS} is adjusted with a 25k potentiometer. The potentiometer wiper is connected to V^+.

Metallization and Pad Layout



75 x 45 Mils

LH2108/2208/2308
LH2108A/2208A/2308A

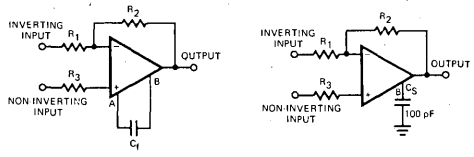
Dual Operational Amplifiers

Description: The 2108, 2208, 2308, 2108A, 2208A, and 2308A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalents to the National LH2108, LH2208, LH2308, LH2108A, LH2208A and LH2308A.

FUNCTIONAL DESCRIPTION

These dual differential input, precision amplifiers provide low input current and offset voltage competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor. The 2108A, 2208A, and 2308A are high performance selections from the 2108/2208/2308 amplifier family.

FUNCTIONAL DIAGRAM
Frequency Compensation Circuits

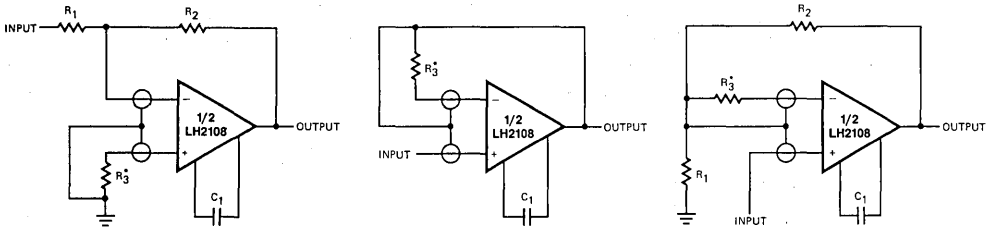


$$C_f \geq C_o\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

C_o = 30 pF

04821A-1

APPLICATIONS
Connection of Input Guards



04821A-2

*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

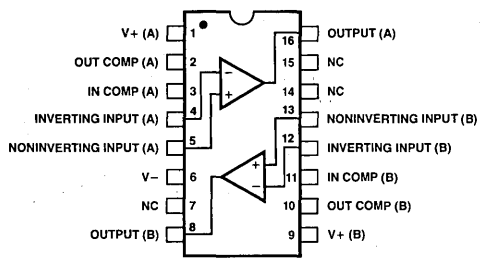
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LH2308	Hermetic DIP	0 to +70°C	LH2308D
LH2208	Hermetic DIP	−25 to +85°C	LH2208D
LH2108	Hermetic DIP	−55 to +125°C	LH2108D
LH2308A	Hermetic DIP	0 to +70°C	LH2308AD
LH2208A	Hermetic DIP	−25 to +85°C	LH2208AD
LH2108A	Hermetic DIP	−55 to +125°C	LH2108AD

Also available with burn-in processing. To order, add suffix B to the part number.

CONNECTION DIAGRAM – Top View

Hermetic
Dual In-Line
D-16-1



Note: Pin 1 is marked for orientation.

LIC-908

04821A-ANA

MAXIMUM RATINGS

Supply Voltage	
LH2108, 2208, 2108A, 2208A	±20V
LH2308, 2308A	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LH2108, 2108A	−55 to +125°C
LH2208, 2208A	−25 to +85°C
LH2308, 2308A	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameters (See definitions)	Test Conditions	LH2308			LH2308A			LH2108 LH2208			LH2108A LH2208A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20V								0.3	0.6		0.3	0.6	mA
	V_S = ±15V		0.3	0.8		0.3	0.8							
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10k\Omega$	25	300		80	300		50	300		80	300		V/mV
The Following Specifications Apply Over the Operating Temperature Ranges														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10k\Omega$	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current (each amplifier)	V_S = ±20V $T_A = T_{HIGH}$								0.15	0.4		0.1.5	0.4	mA
	V_S = ±15V $T_A = T_{HIGH}$		0.6	1.0		0.6	0.8							

Notes:
1. Derate the Dual In-Line package at 9mW/°C for operation at ambient temperature above 95°C.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
4. Unless otherwise specified, these specifications apply for supply voltages from ±5 to ±20V for the 2108, 2208, 2108A and 2208A and from ±5V to ±15V for the 2308 and 2308A.

ADDITIONAL APPLICATION INFORMATION

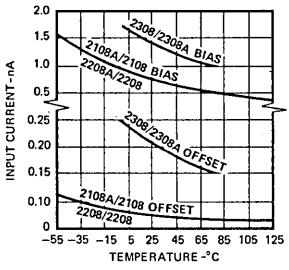
GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 2108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

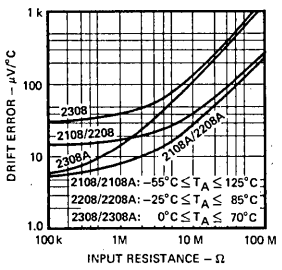
Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

TYPICAL PERFORMANCE CURVES

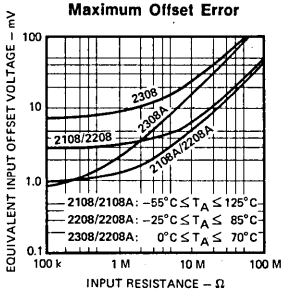
Input Currents



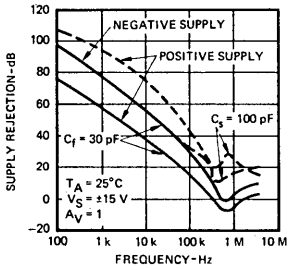
Maximum Drift Error



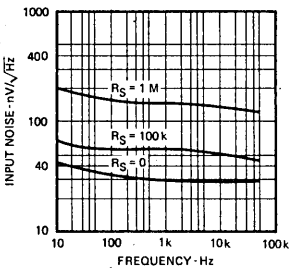
Maximum Offset Error



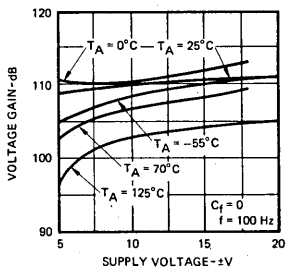
Power Supply Rejection



Input Noise Voltage



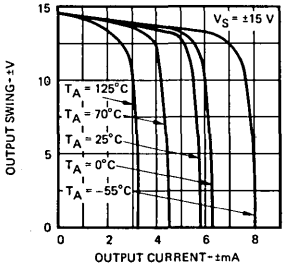
Voltage Gain



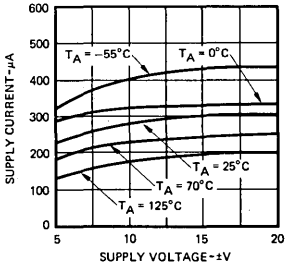
04821A-3

TYPICAL PERFORMANCE CURVES (Cont.)

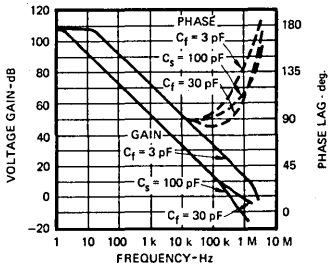
Output Swing



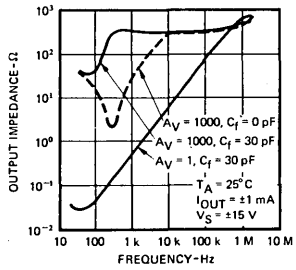
Supply Current Each Amplifier



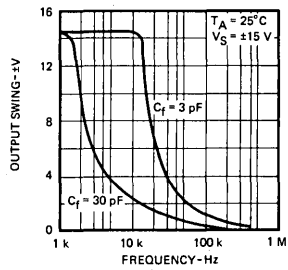
Open Loop Frequency Response



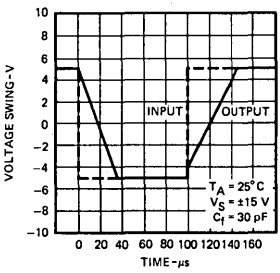
Closed Loop Output Impedance



Large Signal Frequency Response



Voltage Follower Pulse Response



04821A-4

5

Comparators – Section VI

LM111/211/311

Precision Voltage Comparator

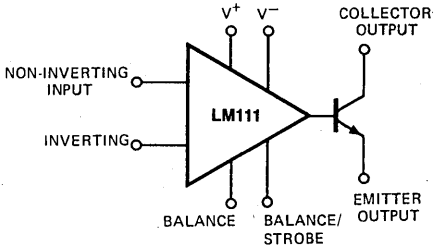
Distinctive Characteristics

- The AMD LM111/211/311 are functionally, electrically, and pin-for-pin equivalent to the National LM 111/211/311
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4mV max.
- Differential Input Voltage Range – ±30V

FUNCTIONAL DESCRIPTION

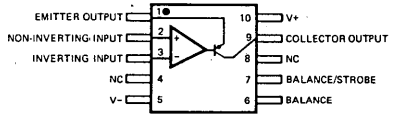
The LM111/211/311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads refered to ground or either supply. Strobing and offset balancing are available and the outputs can be wire ORed.

FUNCTIONAL DIAGRAM



LIC-081

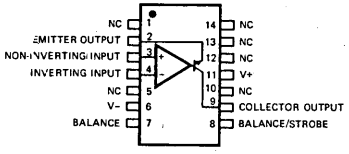
CONNECTION DIAGRAM – Top View
Ceramic Flat Package
F-10-1



Pin 5 is connected to bottom of package. LIC-083

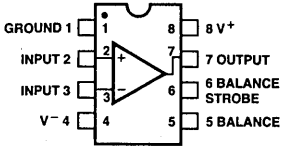
CONNECTION DIAGRAMS – Top Views

Hermetic DIP
D-14-1

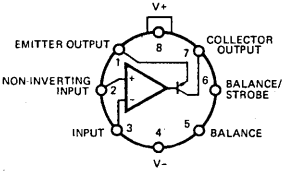


Pin 6 is connected to bottom of package.

Mini-DIP
P-8-1



Metal Can
H-8-1



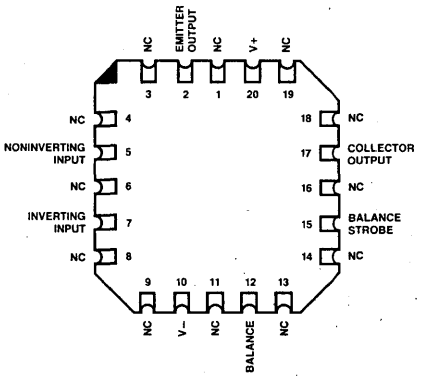
Pin 4 is connected to case. LIC-084

ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LM311	TO-99	0 to +70°C	LM311H
	Hermetic DIP	0 to +70°C	LM311D
	Mini-DIP	0 to +70°C	LM311N
	Dice	0 to +70°C	LD311
	Leadless	0 to +70°C	LM311L
LM211	TO-99	−25 to +85°C	LM211H
	Hermetic DIP	−25 to +85°C	LM211D
	Leadless	−25 to +85°C	LM211L
	Ceramic Flat Package	−25 to +85°C	LM211F
LM111	TO-99	−55 to +125°C	LM111H
	Hermetic DIP	−55 to +125°C	LM111D
	Flat Pak	−55 to +125°C	LM111F
	Dice	−55 to +125°C	LD111
	Leadless	−55 to +125°C	LM111L
	Ceramic Flat Package	−55 to +125°C	LM111F

*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAM – Top View
Leadless Chip-Pak
L-20-1



03934B-ANA

LM111/211/311
MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
LM111/211	50V
LM311	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, −0V
Voltage from Inputs to V^+	−30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LM111	−55°C to +125°C
LM211	−25°C to +85°C
LM311	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

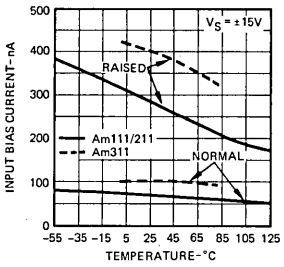
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameters (see definitions)	Test Conditions	LM311 Min.	LM311 Typ.	LM311 Max.	LM111 LM211 Min.	LM111 LM211 Typ.	LM111 LM211 Max.	Units
Input Offset Voltage (Note 3)			2.0	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500 Ω to +5 V, V_E = 0		200			200		ns
Supply Current								
Positive			3.9	7.5		3.9	6.0	mA
Negative			2.6	5.0		2.6	5.0	mA
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{IN} \leq -5$ mV, I_C = 50 mA					0.75	1.5	Volts
	$V_{IN} \leq -10$ mV, I_C = 50 mA		0.75	1.5				Volts
Output Leakage Current	$V_{IN} \geq +5$ mV, V_C to V_E = 50 V					0.2	10.0	nA
	$V_{IN} \geq +10$ mV, V_C to V_E = 40 V		0.2	50.0				nA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{IN} \leq -6$ mV, I_C = 8 mA					0.23	0.40	Volts
	$V_{IN} \leq -10$ mV, I_C = 8 mA		0.23	0.40				Volts
Output Leakage Current	$V_{IN} \geq +6$ mV, V_C to V_E = 50 V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		Volts
Supply Current								
Positive (Note 5)	T_A = 125°C					5.1	6.0	mA
Negative (Note 5)						4.1	5.0	mA

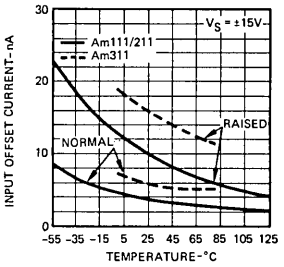
Notes:
1. For the LM111/211/311, derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9mW/°C for operation at ambient temperatures above 95°C, the Flat Packages at 5.4mW/°C for operation at ambient temperatures above 57°C, and the Mini-DIP at 6.6mW/°C above 36°.
2. Unless otherwise specified, these specifications apply for V^+ = +15V, V^- = −15V, V_E = −15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

PERFORMANCE CURVES

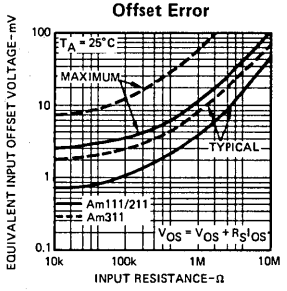
Input Bias Current



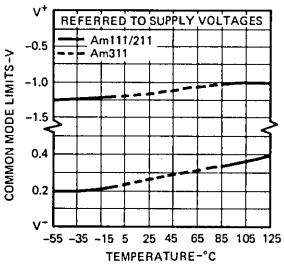
Input Offset Current



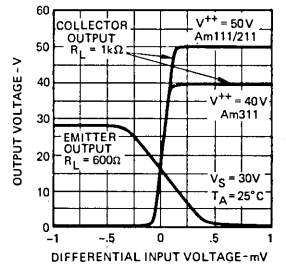
Offset Error



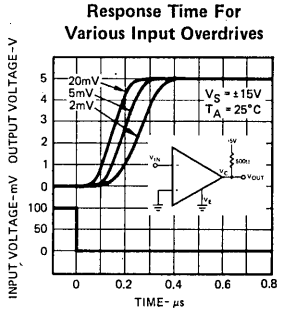
Common-Mode Limits



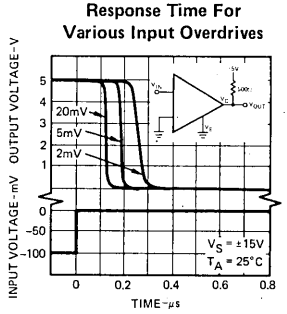
Transfer Function



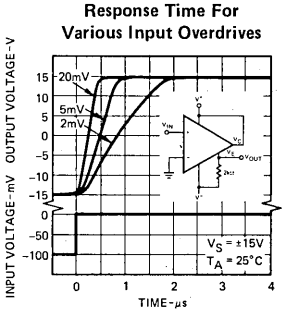
Response Time For Various Input Overdrives



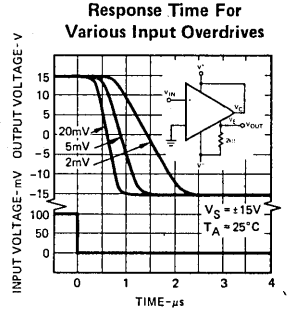
Response Time For Various Input Overdrives



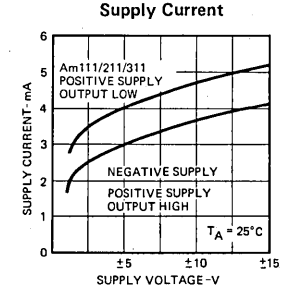
Response Time For Various Input Overdrives



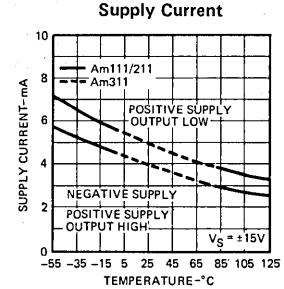
Response Time For Various Input Overdrives



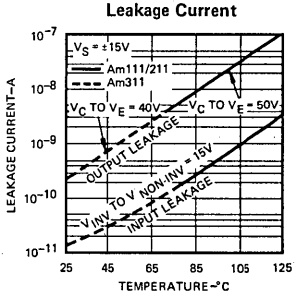
Supply Current



Supply Current



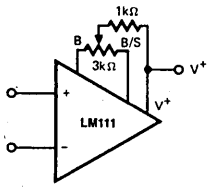
Leakage Current



LIC-085

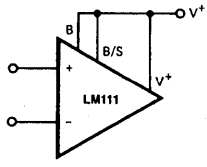
APPLICATIONS

Offset Balancing



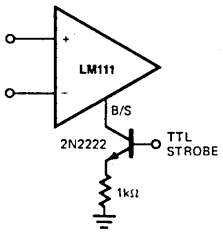
LIC-086

Increasing Input Stage Current*



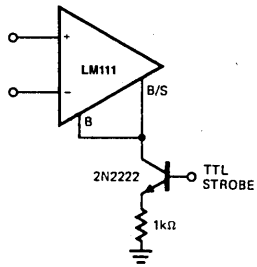
LIC-087

Strobing



LIC-088

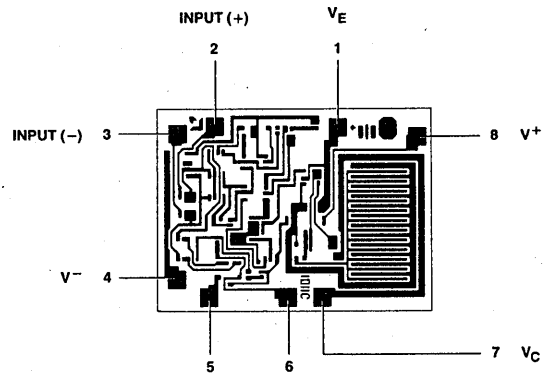
Strobing OFF both Input and Output Stages**



LIC-089

*Increases input bias current and common mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs strobed OFF.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.048" X 0.065"

LM119/219/319

Dual Comparator

Distinctive Characteristics

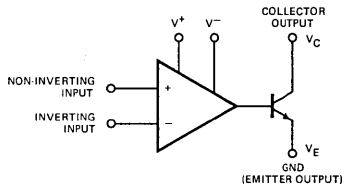
- The AMD LM119/219/319 are functionally, electrically, and pin-for-pin equivalent to the National LM119/219/319.
- Two independent comparators.
- Operates from single 5V supply.
- Output drive – 35V and 25mA.
- Input bias current – 1μA max. (1.2μA for Am319)
- Response time 80ns typical at ±15V.
- Minimum fan out of 2 each side.
- Inputs and outputs isolated from system ground.
- High common mode slew rate.

FUNCTIONAL DESCRIPTION

The LM 119/219/319 are dual high-speed voltage comparators designed to operate over a wide range of voltage supplies down to a single 5V supply and ground. They have higher gain and lower input bias currents than devices such as the μA710. The uncommitted collector of the output stage facilitates RTL, DTL and TTL interfacing, and driving lamps and relays at currents up to 25mA. The device is specified for operation from power supplies up to ±15V and features faster response than the LM111 at the expense of higher power dissipation.

The LM119 performance is specified over the temperature range −55 to 125°C, the LM219 performance is specified over the temperature range −25 to 85°C and the Am319 performance is specified over the temperature range 0 to 70°C.

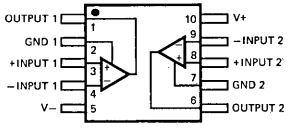
FUNCTIONAL DIAGRAM (One Comparator)



LIC-091

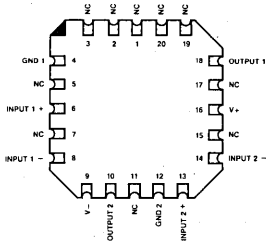
CONNECTION DIAGRAMS – Top Views

Flat Package F-10-1

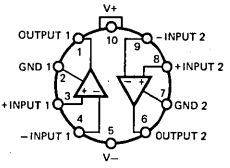


LIC-090 Pin 5 connected to bottom of package.

Leadless Chip-Pak L-20-1



Metal Can H-10-1



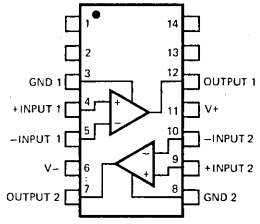
Pin 5 connected to case. LIC-092

ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LM319	TO-99	0 to +70°C	LM319H
	Hermetic DIP	0 to +70°C	LM319D
	Molded DIP	0 to +70°C	LM319N
	Dice	0 to +70°C	LD319
	Leadless	0 to +70°C	LM319L
LM219	TO-99	−25 to +85°C	LM219H
	Hermetic DIP	−25 to +85°C	LM219D
	Flat Pak	−25 to +85°C	LM219F
	Leadless	−25 to +85°C	LM219L
LM119	TO-99	−55 to +125°C	LM119H
	Hermetic DIP	−55 to +125°C	LM119D
	Flat Pak	−55 to +125°C	LM119F
	Dice	−55 to +125°C	LD119
	Leadless	−55 to +125°C	LM119L

*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAM Top View Hermetic and Molded Dual In-Line D-14-1, P-14-1



Pin 6 connected to bottom of package. LIC-093

LM119/219/319

MAXIMUM RATINGS (Above which the useful life may be impaired)

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	36V
Voltage from Ground to V^+	18V
Voltage from Ground to V^-	25V
Differential Input Voltage	±5.0V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10s
Operating Temperature Range	
LM119	−55°C to +125°C
LM219	−25°C to +85°C
LM319	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

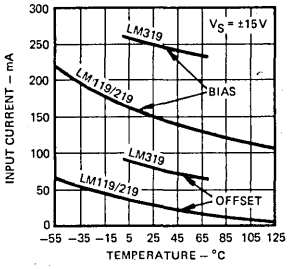
ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Noted) (Note 3)

Parameters (See definitions)		Conditions	LM319 Min.	LM319 Typ.	LM319 Max.	LM119/219 Min.	LM119/219 Typ.	LM119/219 Max.	Units
Input Offset Voltage (Note 4)		$R_S \leq 5k$		2.0	8.0		0.7	4.0	mV
Input Offset Current (Note 4)				80	200		30	75	nA
Input Bias Current				250	1000		150	500	nA
Response Time (Note 5)				80			80		ns
Supply Current	Positive	$V^+ = 5.0V, V^- = 0$		4.3			4.3		mA
		$V_S = \pm 15V$		8.0	12.5		8.0	11.5	
	Negative	$V_S = \pm 15V$		3.0	5.0		3.0	4.5	
Voltage Gain			8.0	40		10	40		V/mV
Saturation Voltage		$V_{in} \leq -5.0mV, I_C = 25mA$					0.75	1.5	Volts
		$V_{in} \leq -10mV, I_C = 25mA$		0.75	1.5				
Output Leakage Current		$V_{in} \geq +5.0mV, V_C$ to $V_E = 35V$					0.2	2.0	μA
		$V_{in} \geq +10mV, V_C$ to $V_E = 35V$		0.2	10				
The Following Specifications Apply Over The Operating Temperature Ranges									
Input Offset Voltage (Note 4)		$R_S \leq 5k$			10			7.0	mV
Input Offset Current (Note 4)					300			100	nA
Input Bias Current					1200			1000	nA
Saturation Voltage		$V_{in} \leq -8.0mV, I_C = 3.2mA$, $T_A \geq 0°C$					0.23	0.4	Volts
		$V_{in} \leq -8.0mV, I_C = 3.2mA$, $T_A \leq 0°C$						0.6	
		$V_{in} \leq -12mV, I_C = 3.2mA$		0.3	0.4				
Output Leakage Current		$V_{in} \geq +8.0mV, V_C$ to $V_E = 35V$					1.0	10	μA
Input Voltage Range		$V_S = \pm 15V$		±13			±13		Volts
		$V^+ = 5.0V, V^- = 0$	1.0		3.0	1.0		3.0	

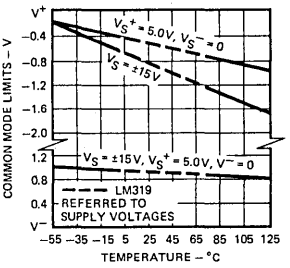
Notes:
1. For supply voltages less than ± 15V the absolute maximum rating is equal to the supply voltage.
2. Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line at 9mW/°C for operation at temperatures above 95°C, and the Flat Package at 5.4mW/°C for operation at temperatures above 57°C.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ± 15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within 1 volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified is for a 100mV input step with 5mV overdrive.

TYPICAL PERFORMANCE CURVES

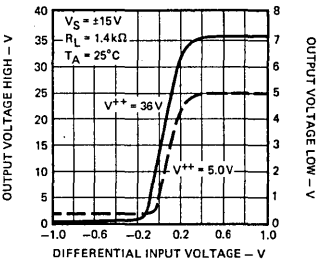
Input Currents



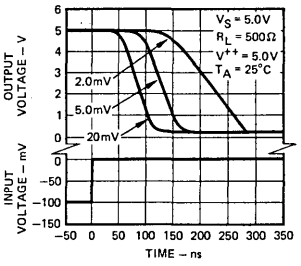
Common Mode Limits



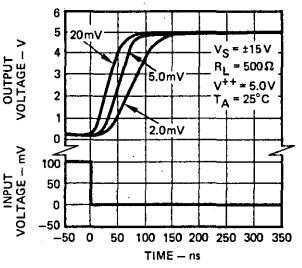
Transfer Function



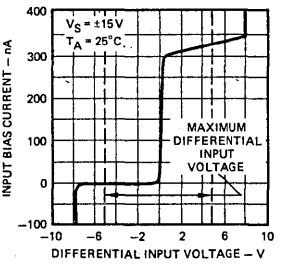
Response Time for Various Input Overdrives



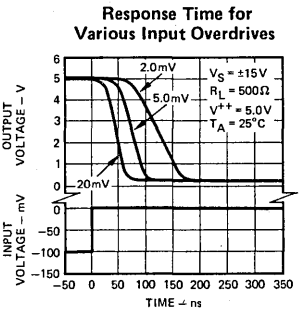
Response Time for Various Input Overdrives



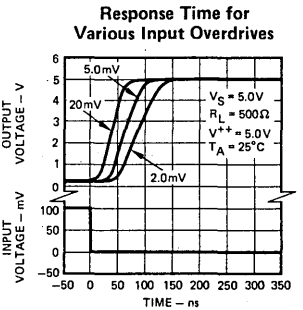
Input Characteristics



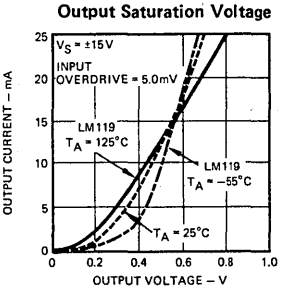
Response Time for Various Input Overdrives



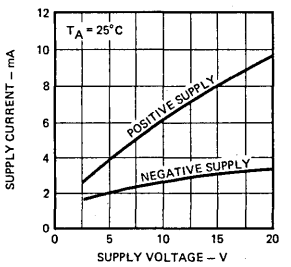
Response Time for Various Input Overdrives



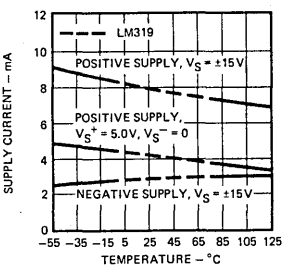
Output Saturation Voltage



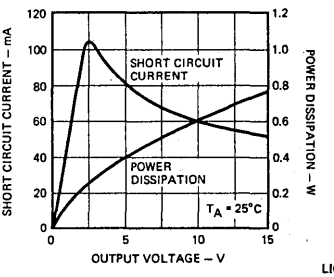
Supply Current



Supply Current



Output Limiting Characteristics



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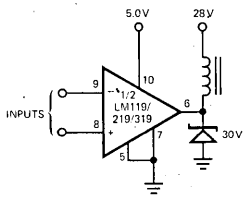
APPLICATIONS

Relay Driver



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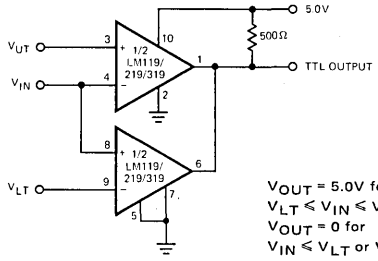
Window Detector



V_{OUT} = 5.0V for
$V_{LT} \leq V_{IN} \leq V_{UT}$
V_{OUT} = 0 for
$V_{IN} \leq V_{LT}$ or $V_{IN} \geq V_{UT}$

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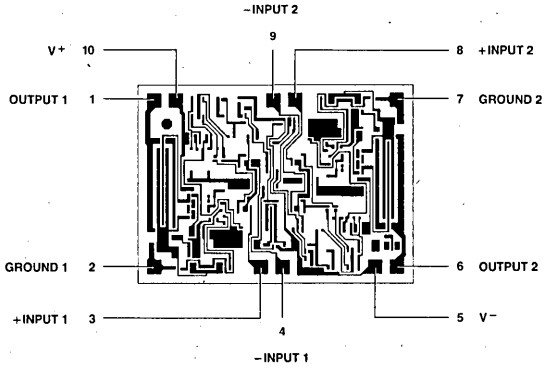
Metallization and Pad Layout



DIE SIZE: 0.078″ X 0.057″

LM139/239/339 • LM139A/239A/339A

Low Offset Voltage Quad Comparators

Distinctive Characteristics

- Four high precision comparators
- Reduced VOS drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Wide single supply voltage range or dual supplies
  $2.0V_{DC}$ to $36V_{DC}$
  $\pm 1.0V_{DC}$ to $\pm 18V_{DC}$
- Very low supply current drain (0.8mA)—independent of supply voltage (1.0mW/comparator) makes these comparators suitable for battery operation.
- Low input bias current – 35nA
- Low input offset current – 3.0nA and offset voltage – 2.0mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage
  1.0mV at 5.0μA
  60mV at 1.0mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

FUNCTIONAL DESCRIPTION

The AMD LM139, LM239, LM339, LM339A, LM239A and LM339A quad comparators are functionally, electrically and pin-for-pin equivalent to the National LM139, LM239, LM339, LM339A, LM239A and LM339A. This series of precision comparators consists of four independent voltage comparators which were specifically designed to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

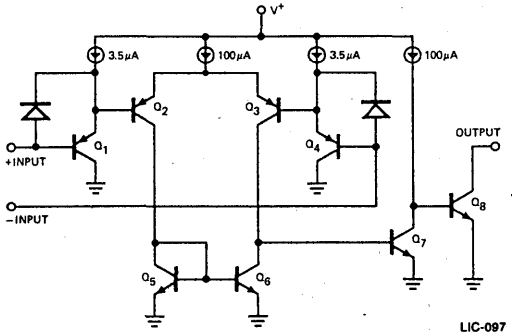
Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139/A series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139/A will directly interface with MOS logic – where the lower power drain of the LM139/A is a distinct advantage over standard comparators.

ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
LM339	Hermetic DIP	0 to +70°C	LM339D
	Molded DIP	0 to +70°C	LM339N
	Dice	0 to +70°C	LD339
	Leadless	0 to +70°C	LM339L
LM239	Hermetic DIP	−25 to +85°C	LM239D
	Leadless	−25 to +85°C	LM239L
LM139	Hermetic DIP	−55 to +125°C	LM139D
	Flat Pack	−55 to +125°C	LM139F
	Dice	−55 to +125°C	LD139
	Leadless	−55 to +125°C	LM139L
LM339A	Hermetic DIP	0 to +70°C	LM339AD
	Molded DIP	0 to +70°C	LM339AN
	Dice	0 to +70°C	LD339A
	Leadless	0 to +70°C	LM339AL
LM239A	Hermetic DIP	−25 to +85°C	LM239AD
	Leadless	−25 to +85°C	LM239AL
LM139A	Hermetic DIP	−55 to +125°C	LM139AD
	Flat Pack	−55 to +125°C	LM139AF
	Dice	−55 to +125°C	LD139A
	Leadless	−55 to +125°C	LM139AL

*Also available with burn-in processing. To order add suffix B to part number.

SCHEMATIC DIAGRAM



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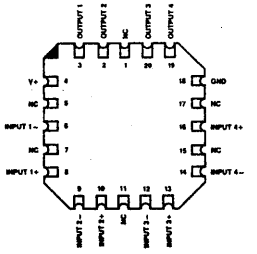
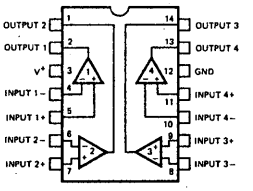
CONNECTION DIAGRAMS – Top Views

Leadless Chip-Pak L-20-1



Hermetic and Molded DIP D-14-1



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage, V+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Ceramic Dip	900 mW
Plastic Dip	570 mW
Flat Pack	800 mW
Output Short Circuit to GND (Note 2)	Continuous
Input Current (V_{in} −0.3 V_{DC}) (Note 3)	50 mA
Operating Temperature Range	
LM339/A	0°C to +70°C
LM239/A	−25°C to +85°C
LM139/A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

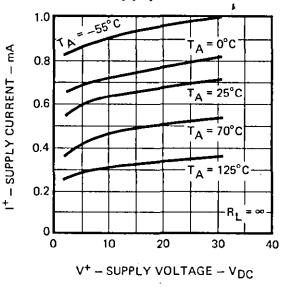
ELECTRICAL CHARACTERISTICS (V^+ = +5.0V_{DC}) (Note 4)

Parameters	Test Conditions	LM239 LM339 Min.	LM239 LM339 Typ.	LM239 LM339 Max.	LM139 Min.	LM139 Typ.	LM139 Max.	LM239A LM339A Min.	LM239A LM339A Typ.	LM239A LM339A Max.	LM139A Min.	LM139A Typ.	LM139A Max.	Units
Input Offset Voltage	T_A = +25°C (Note 9)		±2.0	±5.0		±2.0	±5.0		±1.0	±2.0		±1.0	±2.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = +25°C		25	250		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = +25°C		±5.0	±50		±3.0	±25		±5.0	±50		±3.0	±25	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	T_A = +25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L = ∞ on all Comparators T_A = +25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
Voltage Gain	R_L ≥ 15kΩ, T_A = +25°C, V^+ = I5 V_{DC} (To Support Large V_o Swing)		200			200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = +1.4V_{DC}, V_{R_L} = 5.0V_{DC}, R_L = 5.1kΩ and T_A = +25°C		300			300			300			300		ns
Response Time (Note 7)	V_{R_L} = 5.0 V_{DC} and R_L = 5.1 kΩ T_A = +25°C		1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)}$ ≥ +1.0 V_{DC}, $V_{IN(+)}$ = 0, and V_o ≤ +1.5 V_{DC}, T_A = +25°C	6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$ ≥ +1.0 V_{DC}, $V_{IN(+)}$ = 0, and I_{sink} ≤ 4.0 mA, T_A = +25°C		250	400		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ ≥ +1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_o = 5.0 V_{DC}, T_A = +25°C		0.1			0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			9.0			9.0			4.0			4.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150			±100			±150			±100	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400			300			400			300	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$ ≥ +1.0 V_{DC}, $V_{IN(+)}$ = 0 and I_{sink} ≤ 4.0 mA			700			700			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$ ≥ +1.0 V_{DC}, $V_{IN(-)}$ = 0 and V_o = 30 V_{DC}			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage (Note 8)	Keep all V_{IN}'s ≥ 0 V_{DC} (or V^- if used)			36			36			V^+			V^+	V_{DC}

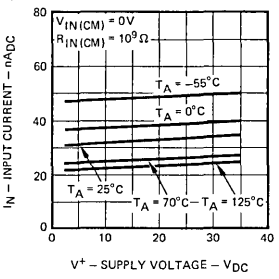
Notes:
1. For high temperature operation, the LM339/A must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239/A and LM139/A must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V^+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal outputs states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC}.
4. These specifications apply for V^+ = +5.0 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM239/A all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C and the LM339/A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V, The upper end of the common-mode voltage range is V^+ −1.5V, but either or both inputs can go to +30 V_{DC} without damage.
7. The response time specified is for a 100mV input step with 5.0mV overdrive. 300ns can be achieved with larger overdrive signals, see typical performance characteristics section.
8. If the voltage applied to any input exceeds V^+, all four comparator outputs will go to the high voltage level. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).
9. At output switch point, $V_O \cong$ 1.4 V_{DC}, R_S = 0Ω with V^+ from 5.0 V_{DC}; and over the full input common mode range (0 V_{DC} to V^+ −1.5 V_{DC}).

TYPICAL PERFORMANCE CHARACTERISTICS

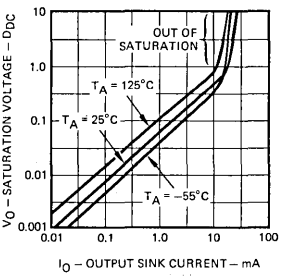
Supply Current



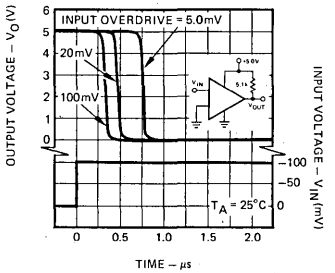
Input Current



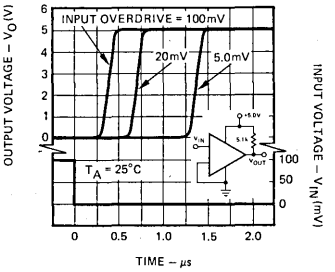
Output Saturation Voltage



Response Time for Various Input Overdrives Negative Transition



Response Time for Various Input Overdrives Positive Transition



LIC-099

APPLICATION HINTS

The LM139/A is a high gain, wide bandwidth device; which like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. The oscillation shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Lowering the input resistors to $<10k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C card attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139/A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2V_{DC}$ to $30\ V_{DC}$.

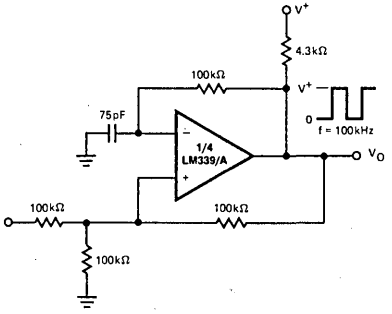
It is not normally necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25° C). An input clamp diode and input resistor can be used as shown in the applications section.

The output of the LM139/A is the uncommitted collector of a grounded-emitter NPN output transistor. Several collectors can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139/A package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp very nearly to ground level for small load currents.

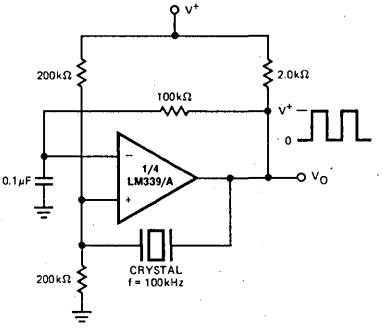
TYPICAL APPLICATIONS

($V^+ = 5.0V_{DC}$)



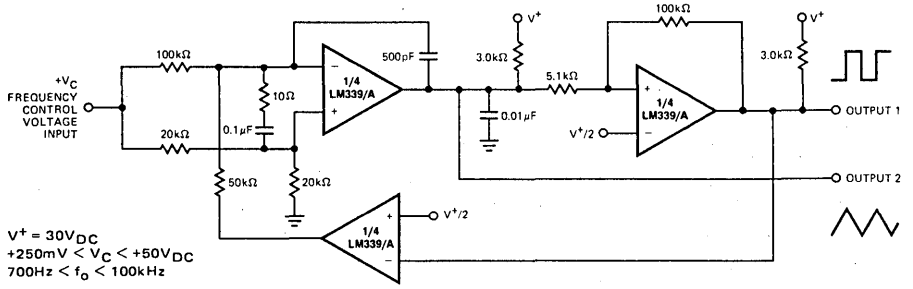
LIC-100

Squarewave Oscillator



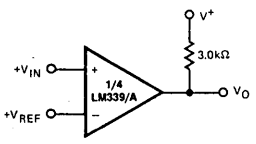
Crystal Controlled Oscillator

LIC-101



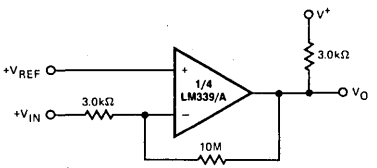
Two-Decade High-Frequency VCO

LIC-102



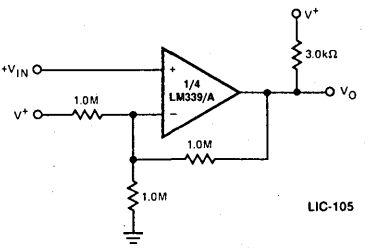
LIC-103

Basic Comparator



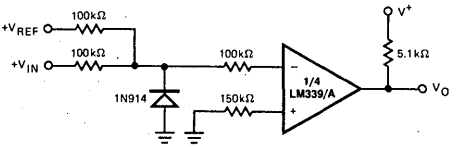
LIC-104

Non-Inverting Comparator with Hysteresis



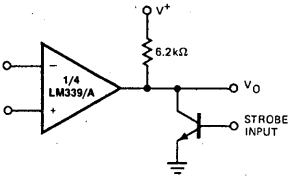
LIC-105

Inverting Comparator with Hysteresis



LIC-106

Comparing Input Voltages of Opposite Polarity



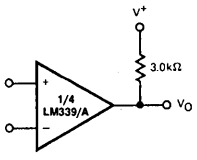
LIC-107

*Or logic gate without pull-up resistor.

Output Strobing

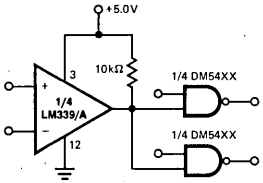
TYPICAL APPLICATIONS (Cont.)

($V^+ = 5.0V_{DC}$)



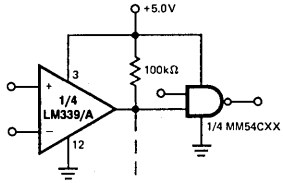
LIC-108

Basic Comparator



LIC-109

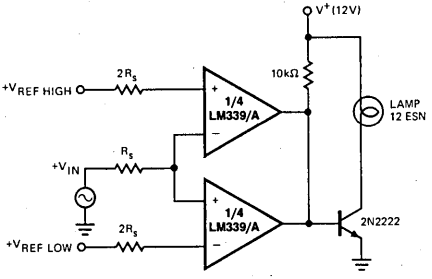
Driving TTL



LIC-110

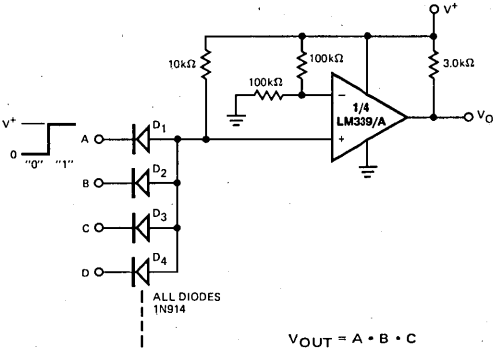
Driving CMOS

($V^+ = 15V_{DC}$)



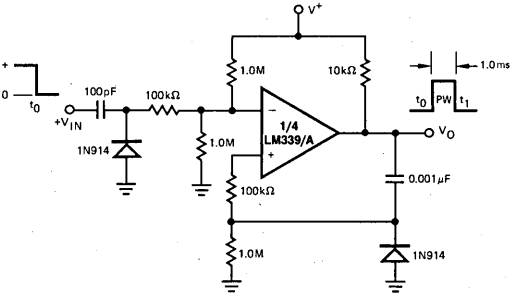
LIC-111

Limit Comparator



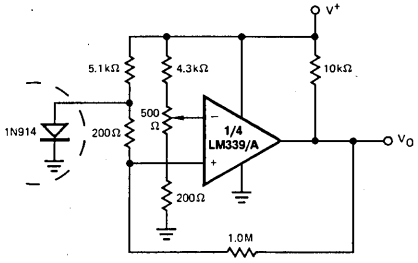
LIC-112

Large Fan-In AND Gate



LIC-113

One-Shot Multivibrator

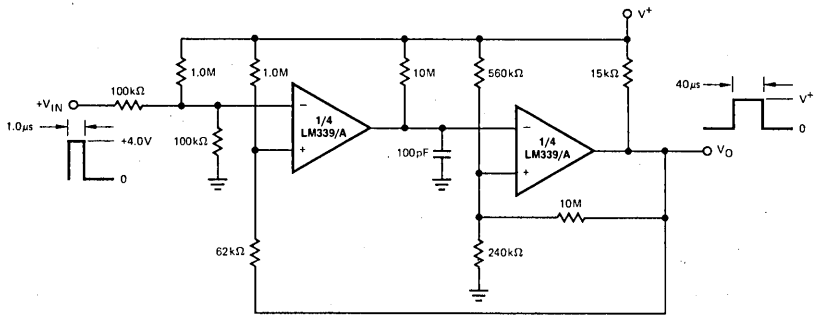


LIC-114

Remote Temperature Sensing

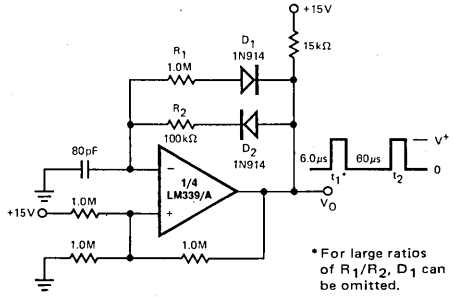
TYPICAL APPLICATIONS (Cont.)

($V^+ = 15V_{DC}$)



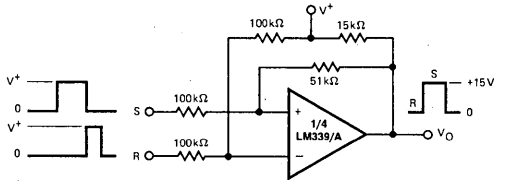
LIC-115

One-Shot Multivibrator with Input Lock Out



LIC-116

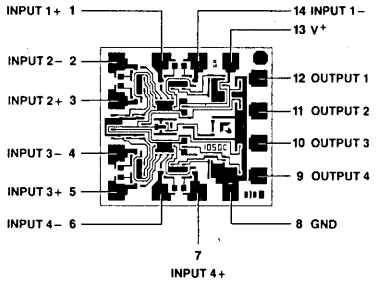
Pulse Generator



LIC-117

Bi-Stable Multivibrator

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.047″ X 0.050″

Am685

Voltage Comparator

Distinctive Characteristics:

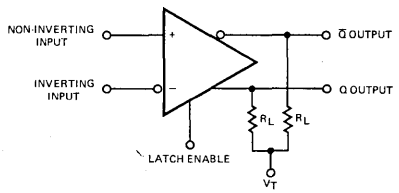
- 6.5ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- 3.0ns Latch setup time
- Complementary ECL outputs
- 50Ω line driving capability

FUNCTIONAL DESCRIPTION

The Am685 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays (6.5 ns) without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is HIGH, the comparator functions normally. When the Latch Enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable must be connected to ground.

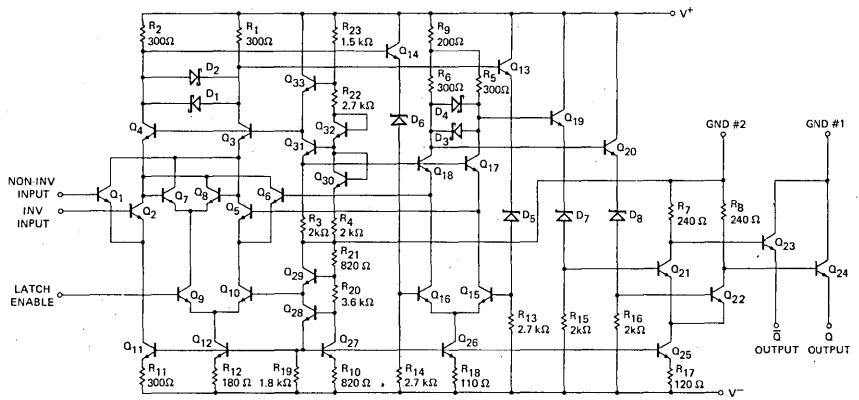
FUNCTIONAL DIAGRAM



LIC-118

The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to –2.0 V, or 200–2000Ω connected to –5.2 V.

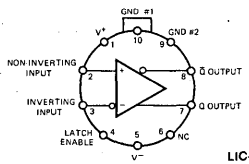
CIRCUIT DIAGRAM



LIC-119

CONNECTION DIAGRAMS – Top Views

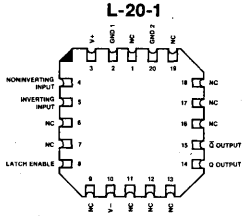
Metal Can
H-10-1



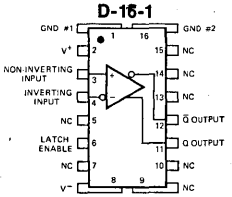
LIC-120

Note 1. On metal package, pin 5 is connected to case. On DIP, pin 8 is connected to case.

Leadless Chip-Pak
L-20-1



Dual In-Line
D-16-1



LIC-121

6

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	500 mW

Operating Temperature Range	
Am685-L	−30°C to +85°C
Am685-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	µA
			−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance (Note 1)	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +3.3$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

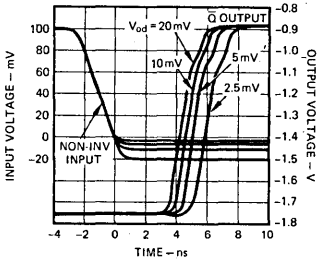
t_{pd+}	Input to Output HIGH	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd+}(E)	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}(E)	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} \leq T_A \leq T_{A(max.)}$		1.0		1.0	ns
t_{pw}(E)	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		5.0	ns

Notes:
1. For TO-99 only; CERDIP = 7pF.
2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +100°C; for the dual in-line package, derate at 9mW/°C for operation at ambient temperatures above +105°C.
3. Unless otherwise specified $V^+ = 6.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
4. Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

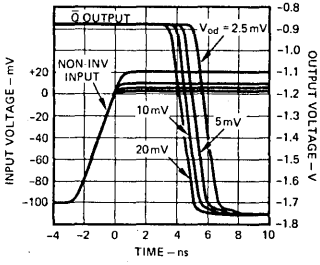
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

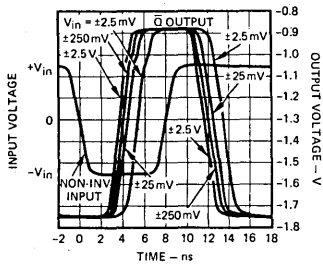
Response for Various Input Overdrives



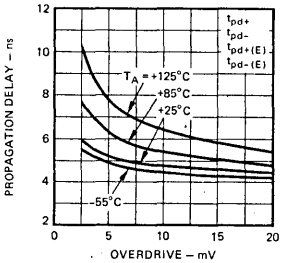
Response for Various Input Overdrives



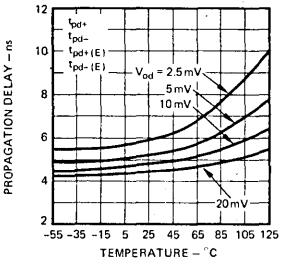
Response for Various Input Signal Levels



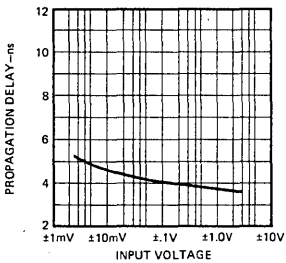
Propagation Delays as a Function of Input Overdrive



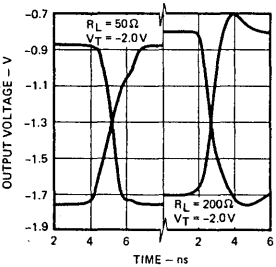
Propagation Delays as a Function of Temperature



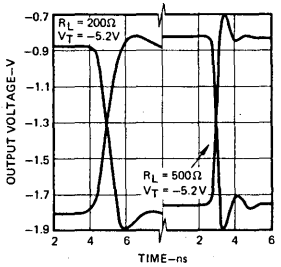
Propagation Delay as a Function of Input Signal Level



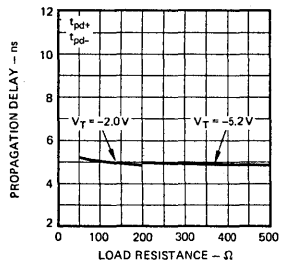
Response for Various Load Resistances



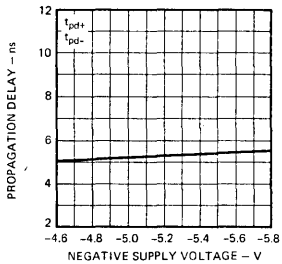
Response for Various Load Resistances



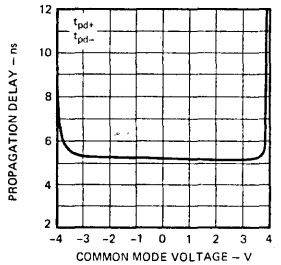
Propagation Delays as a Function of Load Resistance



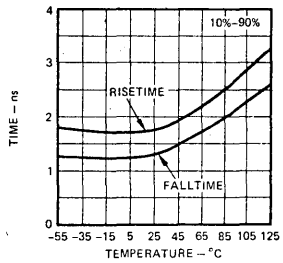
Propagation Delays as a Function of Negative Supply Voltage



Propagation Delays as a Function of Common Mode Voltage



Output Rise and Fall Times as a Function of Temperature



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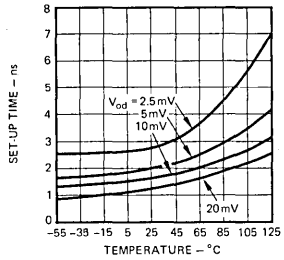
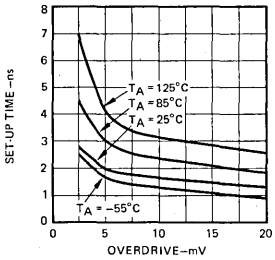
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

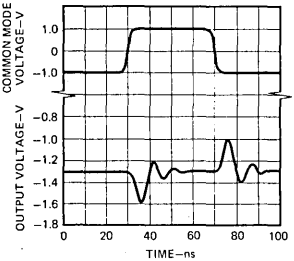
Set-up Time as a Function of Temperature



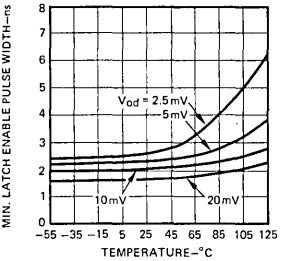
Set-up Time as a Function of Input Overdrive



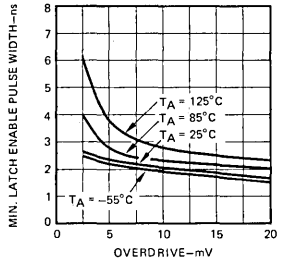
Common Mode Pulse Response



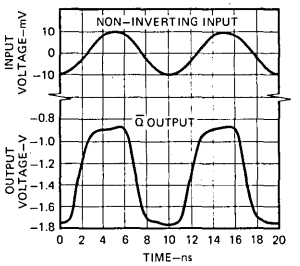
Min. Latch Enable Pulse Width as a Function of Temperature



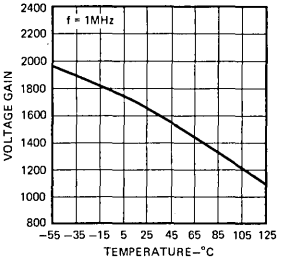
Min. Latch Enable Pulse Width as a Function of Input Overdrive



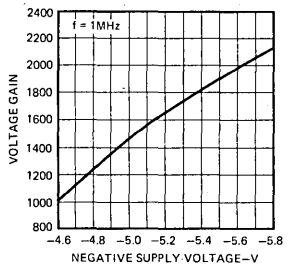
Response to 100MHz Sine Wave



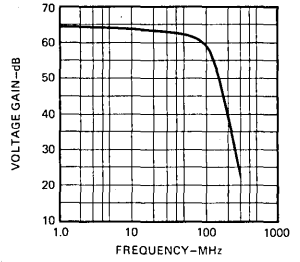
Voltage Gain as a Function of Temperature



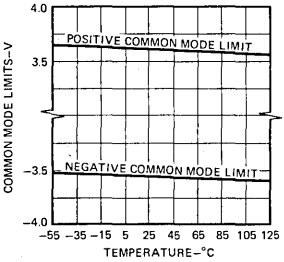
Voltage Gain as a Function of Negative Supply Voltage



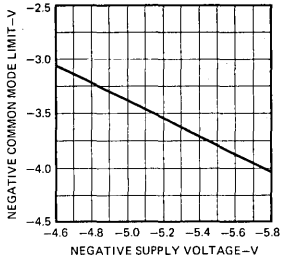
Voltage Gain as a Function of Frequency



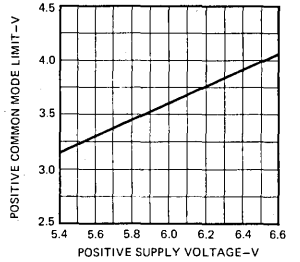
Common Mode Limits as a Function of Temperature



Negative Common Mode Limit as a Function of Negative Supply Voltage



Positive Common Mode Limit as a Function of Positive Supply Voltage



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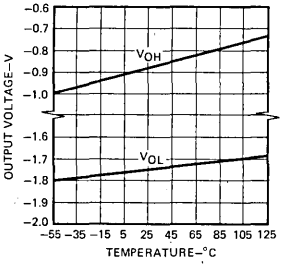
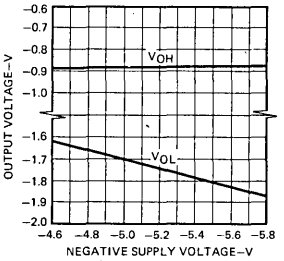
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

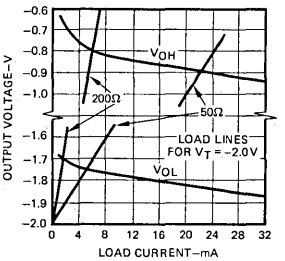
Output Levels as a Function of Temperature



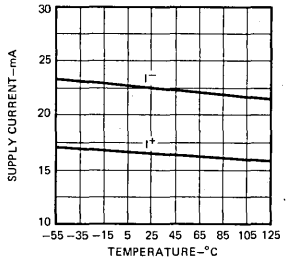
Output Levels As A Function Of Negative Supply Voltage



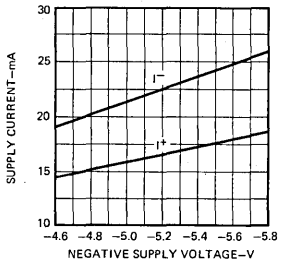
Output Levels As A Function Of DC Loading



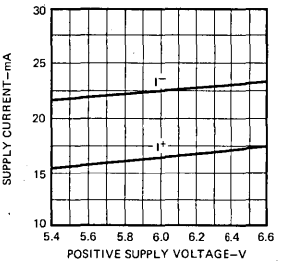
Supply Currents As A Function Of Temperature



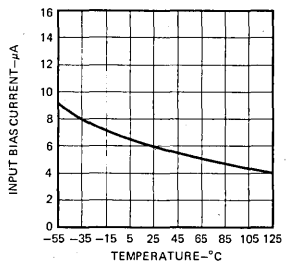
Supply Currents As A Function Of Negative Supply Voltage



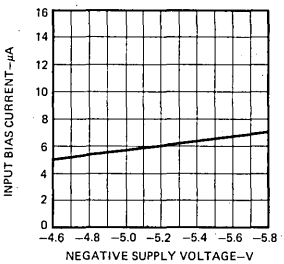
Supply Currents As A Function Of Positive Supply Voltage



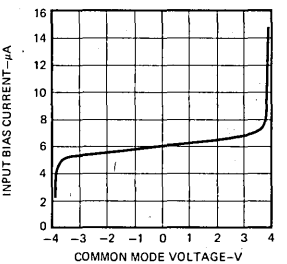
Input Bias Current As A Function Of Temperature



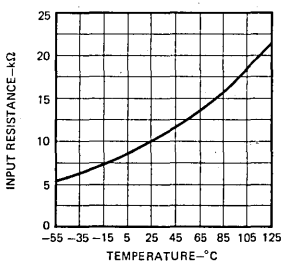
Input Bias Current As A Function Of Negative Supply Voltage



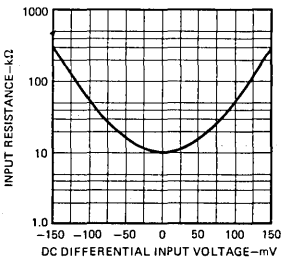
Input Bias Current As A Function Of Common Mode Voltage



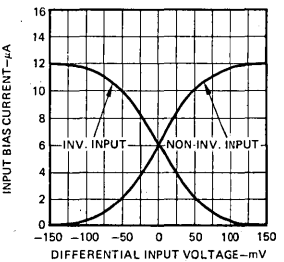
Input Resistance As A Function Of Temperature



Input Resistance As A Function Of DC Differential Input Voltage



Input Current As A Function Of Differential Input Voltage



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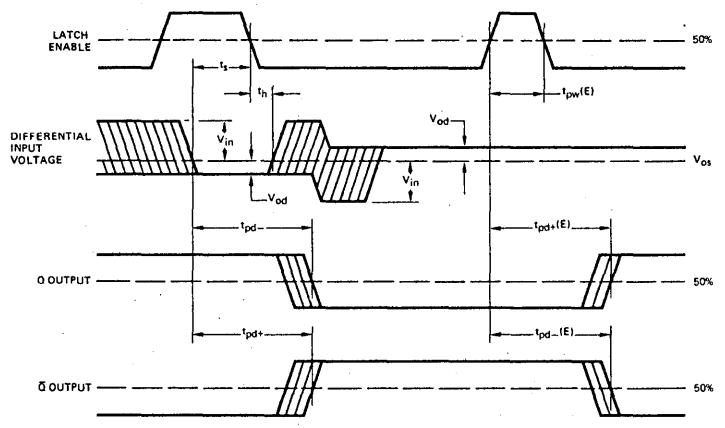
TIMING DIAGRAM



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KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

Figure 1

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

DEFINITION OF TERMS

V_{OS} **INPUT OFFSET VOLTAGE** – That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ **AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE** – The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} **INPUT OFFSET CURRENT** – The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B **INPUT BIAS CURRENT** – The average of the two input currents.

R_{IN} **INPUT RESISTANCE** – The resistance looking into either input terminal with the other grounded.

C_{IN} **INPUT CAPACITANCE** – The capacitance looking into either input terminal with the other grounded.

V_{CM} **INPUT VOLTAGE RANGE** – The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR **COMMON MODE REJECTION RATIO** – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR **SUPPLY VOLTAGE REJECTION RATIO** – The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **OUTPUT HIGH VOLTAGE** – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **OUTPUT LOW VOLTAGE** – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I^+ **POSITIVE SUPPLY CURRENT** – The current required from the positive supply to operate the comparator.

I^- **NEGATIVE SUPPLY CURRENT** – The current required from the negative supply to operate the comparator.

P_{DISS} **POWER DISSIPATION** – The power dissipated by the comparator with both outputs terminated in 50Ω to -2.0V.

SWITCHING TERMS (refer to Fig. 1)

t_{pd+} **INPUT TO OUTPUT HIGH DELAY** – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} **INPUT TO OUTPUT LOW DELAY** – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ **LATCH ENABLE TO OUTPUT HIGH DELAY** – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ **LATCH ENABLE TO OUTPUT LOW DELAY** – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_s **MINIMUM SET-UP TIME** – The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **MINIMUM HOLD TIME** – The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **MINIMUM LATCH ENABLE PULSE WIDTH** – The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

OTHER SYMBOLS

T_A	Ambient temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{in}	Input pulse amplitude
V^+	Positive supply voltage	V_{od}	Input overdrive
V^-	Negative supply voltage	f	Frequency

MEASUREMENT OF PROPAGATION DELAY

A voltage comparator must be able to respond to input signal levels ranging from a few millivolts to several volts, ideally with little variation in propagation delay. The most difficult condition is where the comparator has been driven hard into one state by a large signal, and the next input signal is just barely enough to make it switch to the other state. This forces the input stage of the circuit to swing from a full off (or on) state to a point somewhere near the center of its linear range, thus exercising both its large- and small-signal responses. If the comparator is fast for this condition, it should be as fast or faster for almost any other condition. The unofficial industry standard input signal is a 100mV step with an overdrive of 5mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). The 100mV is more than enough to fully turn on the input stage, but not so large to make measurement a problem. Large pulses would require exceptionally good control on waveform purity, since only a few tenths of a percent of overshoot or ripple would be enough to affect the value of the overdrive and, for sensitive comparators, result in false switching. The propagation delay is measured from the time the input signal crosses the input threshold voltage (i.e., the offset voltage) to the 50% point of either output. This definition ensures that each unit is measured under equal conditions, and also makes the measurement relatively independent of the input rise and fall times.

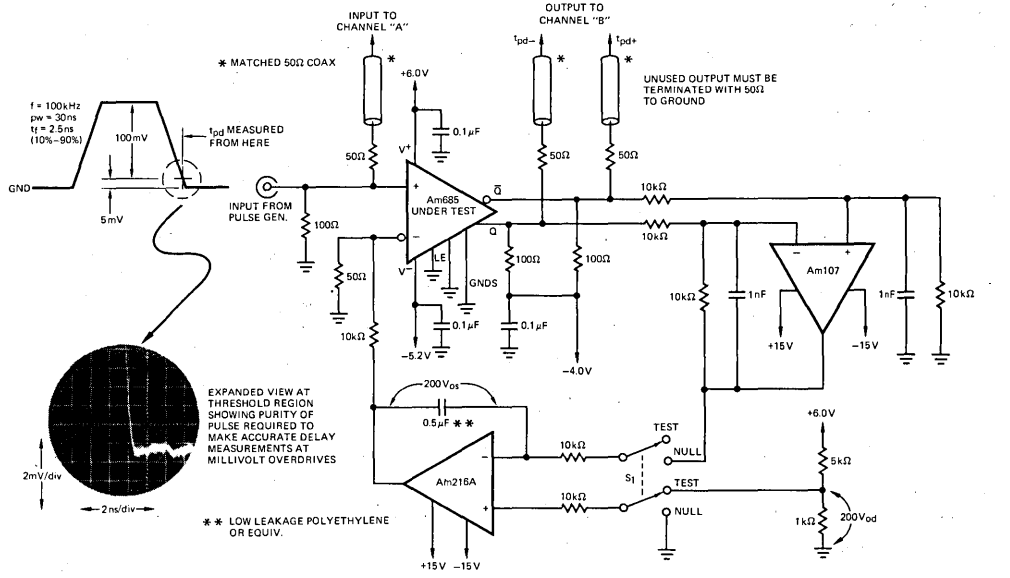

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Figure 2

The test circuit of Figure 2 provides a means of automatically nulling out the offset voltage and applying the overdrive. With S1 in the "NULL" position, the feedback loop around the Am685 via the two operational amplifiers corrects for the offset of the circuit including any dc shift in the ground level of the input signal. When switched to "TEST", the offset is held on the storage capacitor of the Am216A and the overdrive is added at the Am216A non-inverting input. The duty cycle of the signal is made low so that the presence of the input pulse during nulling will not disturb the offset. A solid ground plane is used for the test jig, and capacitors bypass the supply voltages. All power and signal leads are kept as short as possible. The Am685 input and output run directly into the 50Ω inputs of the sampling scope via equal lengths of 50Ω coaxial cable. For the conditions shown in the figure, t_{pd+} is measured at the $\overline{Q}$ output and t_{pd-} at the Q output. If it is desired to measure the opposite output polarities, the polarities of the input signal and overdrive must be reversed.

THERMAL CONSIDERATIONS

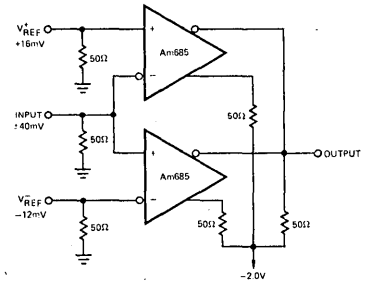
To achieve the high speed of the Am685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the Am685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc., provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

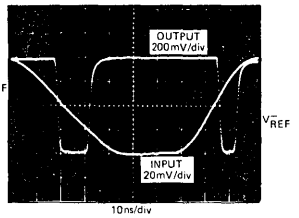
INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am685 is particularly critical because it features very high gain (60dB) at very high frequencies (100MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to -2.0V, but a Thevenin equivalent to V^- can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible.

TYPICAL APPLICATIONS
(T_A = 25°C)

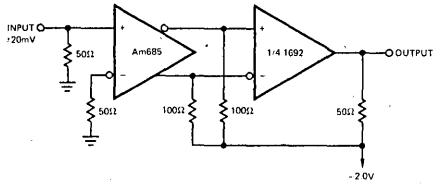
High-Speed Window Detector

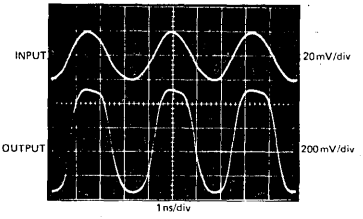




LIC-127

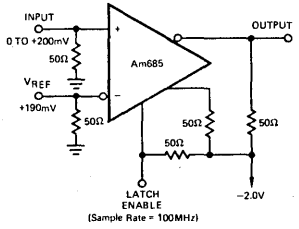
300MHz Line Receiver

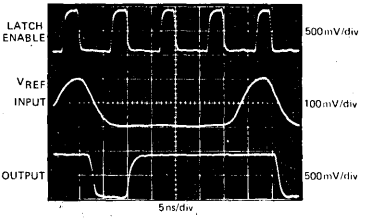




LIC-128

High-Speed Sampling





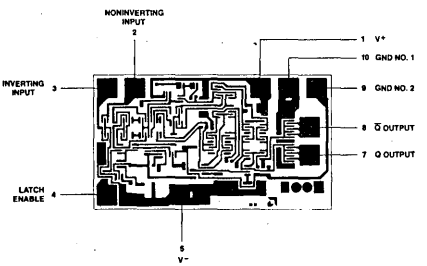
LIC-129

ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
Am685	Metal Can	−30 to +85°C	AM685HL
	Hermetic DIP	−30 to +85°C	AM685DL
Am685	Metal Can	−55 to +125°C	AM685HM
	Hermetic DIP	−55 to +125°C	AM685DM
Am685	Dice	−30 to +85°C	AM685XL
	Dice	−55 to +125°C	AM685XM
Am685	Leadless	−30 to +85°C	AM685LL
	Leadless	−55 to +125°C	AM685LM

*Also available with burn-in processing. To order add suffix B to part number.

Metallization and Pad Layout



DIE SIZE: 0.032" X 0.054"

A New High-Speed Comparator the Am685

By Jim Giles and Alan Seales

INTRODUCTION

Modern electronic systems require more and more that operations be performed in a few nanoseconds so that the delay of the complete system, which may be very complex, be held to a minimum. There are abundant logic circuit elements available that meet this criterion: gold-doped TTL, Schottky TTL, and emitter-coupled logic (ECL), listed in descending order of propagation delay. Where it is necessary to interface from the analog world to the input of a logic system, or to detect very low-level logic signals in the presence of heavy noise, a high-speed precision comparator is needed. If such a comparator had a propagation delay less than 10ns, it could replace costly and complex circuitry that designers are now forced to use in very high-speed analog-to-digital converters, data acquisition systems, and optical isolators, as well as make possible many applications hitherto considered unfeasible. It could also be used as a sensitive line receiver or sense amplifier, in 100MHz sample and hold circuits, and in very high-frequency voltage-controlled oscillators.

The basic requirements for a high-speed precision comparator are few and well-defined: good resolution (high gain), high common-mode and differential voltage ranges, outputs compatible with standard logic levels, and, above all, very fast response to signal levels ranging from a few millivolts to several volts. The industry workhorse, the 710, has come close to meeting these requirements, and except for the most demanding applications, its 40ns propagation delay is adequate. A survey of presently available monolithic IC comparators (Table I) shows that there is really none that meets the requirements of very high-speed systems. The newer TTL-output circuits offer only marginal improvement over the 710 when measured under identical conditions of large input pulse and small overdrive, and the ECL-output comparator, although faster, has such poor resolution that it can be used only for large input signals. Advanced Micro Devices felt there was a need for a family of linear devices to fill the needs of very high-speed systems, with the first circuit being a precision comparator with less than 10ns delay.

Type No.	Logic Family	Propagation Delay	Resolution
Am111	TTL	200ns	0.012mV
μA710	TTL	40ns	1.4mV
Am106	TTL	40ns	0.06mV
μA760	TTL	25ns	0.5mV
NE527/529	TTL	25ns	0.5mV
MC1650	ECL	12ns	30mV

Table I: Propagation Delays of Available Monolithic IC Comparators (100mV Input Step, 5mV Overdrive)

DESIGN OBJECTIVES

In order to achieve the ultimate in speed, it is clear that the comparator outputs must be compatible with ECL, even though at present the majority of systems use TTL. Designers striving for the highest possible speed will already be using ECL in the critical circuit areas of their systems to squeeze the last possible nanosecond out of the overall delay. Further, an ECL circuit requires only one-third the gain of an equivalent TTL circuit for the same resolution owing to its smaller output logic swing. This means that lower impedances can be used and consequently larger bandwidth realized for the same power dissipation. Also, there is no problem interfacing the linear input stages with the digital output gate since an ECL gate is basically a non-saturating overdriven differential amplifier. Properly driving a TTL gate from a linear amplifier is more difficult, however, because it requires a large voltage swing suitably biased to track the input logic threshold with temperature, plus a large peak negative current capability to turn off the gate with minimum delay.

The usefulness and versatility of a comparator can be enhanced by adding a strobe or latch function to the circuit. A strobe simply forces the output of the comparator to one fixed state, independent of input signal conditions, whereas a latch locks the output in the logical state it was in at the instant the latch was enabled. The latch can thus perform a sample and hold function, allowing short input signals to be detected and held for further processing. If the latch is designed to operate directly upon the input stage—so the signal does not suffer any additional delays through the comparator—signals only a few nanoseconds wide can be acquired and held. A latch, therefore, provides a more useful function than a strobe for very high-speed processing.

The most difficult input signal for a comparator to respond to is a large amplitude pulse that just barely exceeds the input threshold. This forces the input stage of the comparator to swing from a full off (or on) state to a point somewhere near the center of its linear range. This exercises both the large-and small-signal responses of the stage. If the comparator has less than 10ns delay under these stringent conditions, then it should be as fast or faster for any other circumstances (see Figure 1). The industry standard measurement is with a

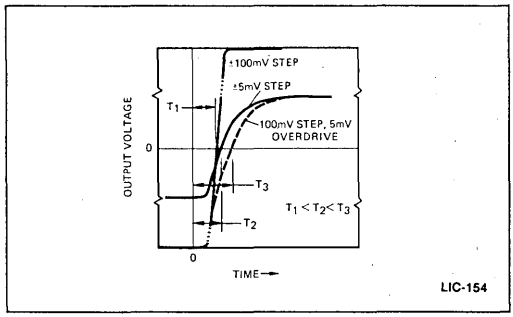


Figure 1. Response to step input signals at output of a differential amplifier

100mV input pulse and an overdrive 5mV above input threshold (this was used for the delays given in Table 1). Pulses larger than 100mV might be used, but this would multiply measurement difficulties, since only a few tenths of a percent aberration or ripple in the pulse generator waveform would be enough to seriously affect the accuracy of the small overdrive, and thus would give misleading results for the propagation delay.

To obtain satisfactory speed for all input signals and particularly for the worst case measurement conditions, the input stage of the comparator must have: 1) wide small-signal bandwidth, 2) high slew rate for large signals, 3) minimum voltage swings, and 4) high gain. The first requirement can be realized by using low-value load resistors, by making every effort in circuit design, device geometry and processing to minimize parasitic capacitances, and by using transistors with the highest f_T possible. The second item calls for high operating currents as well as minimum capacitance. The last two requirements are conflicting, since obtaining high gain normally requires a large voltage swing; therefore some means of clamping the swing must be used that does not degrade the propagation delay.

The overall gain of the complete comparator must also be high because, as illustrated in Figure 1, the propagation delay is less if each stage is well overdriven. To ensure that most of the input overdrive signal is actually used for overdriving, and not consumed in just moving the output from one state to the other, the gain error should be no more than about 10% of the input overdrive. Therefore, for a 5mV overdrive and an ECL output swing of 800mV, the minimum gain must be 1600. It is not practical to strive for much higher gain than this because the small-signal rise time begins to suffer as the stage gain increases. Addition of another stage is undesirable as this also adds delay and increases circuit complexity. It must be remembered that there is a maximum limit on power dissipation that a single integrated circuit package can handle adequately, and this consideration must influence the choice of operating currents and impedance levels throughout the design of the circuit.

With a figure for the total gain required, it is now possible to determine the number of stages and the gain per stage. Since the output stage must be ECL-compatible, its design is fixed, giving a differential-input to single-ended-output gain of about 6. This leaves a differential gain of 270 to be provided by the remainder of the comparator. This is most efficiently divided between two stages, each with a gain somewhat over 16. Both stages should be identical, since minimum overall delay time is obtained when identical stages are cascaded.

A factor not yet discussed that affects the accuracy of the comparator is its input offset voltage. Unless this is trimmed out initially, it must be added to the overdrive in determining the worse-case value of input signal for which the propagation delay specifications will be met. Even with trimming, the temperature drift of high-offset units is typically much greater than that of low-offset units. Therefore, it is desirable to have low initial offset so that trimming is not necessary, and so that the offset temperature coefficient will be good. Also affecting the offset voltage and its drift at higher source resistances are the input currents. To keep this contribution to the total offset low requires high current gains in the input transistors. Therefore, obtaining offsets in the 1–2mV range requires close attention to circuit design, mask layout, and very tight process control (equivalent to that needed for the high-performance, low-frequency operational amplifiers), but with the added kicker of f_Ts well above 1GHz.

As was mentioned, large common-mode and differential voltage ranges are desirable features of a comparator. The limits of the common-mode range in a well-designed circuit should be close to the supply voltages. Since a high-speed comparator will, of necessity, operate at fairly high current levels, the supply voltages must be low to stay within the package power dissipation limits. As a minimum, the common-mode range should be equal to or exceed the differential voltage range to take full advantage of the voltage breakdown characteristics of the input transistors. The basic differential amplifier input stage has a differential voltage breakdown in the range of 5 to 6 volts; the design goal for the common mode range should thus be at least ±3 volts.

In summary, the design objectives for a high-speed precision comparator are as follows:

1) propagation delay <10ns measured at 100mV input step, 5 mV overdrive
2) ECL-compatible outputs
3) latch capability
4) gain >1600
5) input offset voltage <±2mV
6) common -mode range >±3V

CIRCUIT DESIGN

The watchword in designing wideband circuits is simplicity – have the fewest possible active devices in the signal path, the lowest possible impedance levels, and the lowest possible capacitance. The simple, common-emitter differential amplifier can be designed to approach these ideals with one major exception: the deleterious shunting effect of the collector-to-base capacitance upon the driving source resistance is multiplied by the voltage gain of the stage (Miller effect). Even though the impedance levels will be only a few hundred ohms at most, this condition cannot be tolerated if maximum speed is to be achieved. The solution is to add an additional pair of common-base transistors to form a differential cascode amplifier (Figure 2). This circuit has all of the performance features of a common-emitter amplifier and no feedback capacitance.

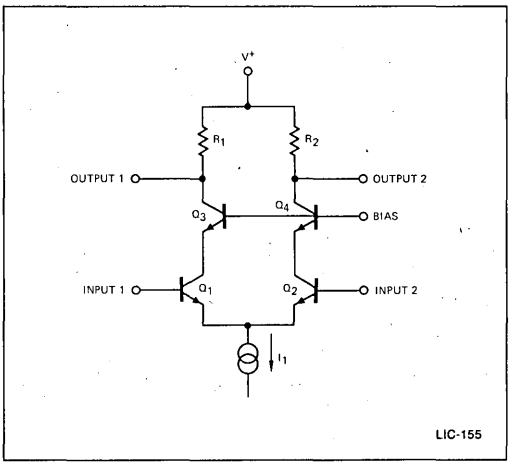


Figure 2. Differential cascode amplifier

Further advantages of the cascode will become apparent later when the latch design is discussed. The only drawback is that there are more devices in the signal path, the positive common-mode range is reduced, and circuitry has to be provided to bias the cascode transistors.

It is now necessary to provide a means of shifting the signal at the output of the cascode (which is very near the positive supply voltage) down to a lower voltage to drive the inputs of the second stage. The use of PNPs is definitely out because of their poor frequency response. This leaves three possibilities: a chain of forward-biased diodes, a programmed voltage drop across a resistor, or a zener diode. The diode chain is useful for level shifts of only a few volts at most, above that, the number of diodes gets too large, with a consequent increase in shunt capacitance and temperature coefficient. The use of a current-source/resistor combination is in the wrong direction for keeping impedance levels low. The resistors could be bypassed with capacitors, but this would offer only marginal improvement, since integrated capacitors have a large shunt component to the substrate. Besides, the addition of four capacitors (for both stages) would result in a large increase in chip area.

The zener diode is definitely superior for high-frequency applications because its shunt capacitance to ground is low, being equal to the collector-to-base capacitance of a transistor. It has no capacitance to the substrate, and its dynamic resistance is quite low. It does have the disadvantage that the level shift is limited to one voltage (6V), which restricts the range of power supply variation the circuit can tolerate. In addition it requires very tight control of the manufacturing process to maintain the matching required. For an input stage gain of 16 the zener voltages have to be matched to better than 0.25% to produce less than 1mV offset voltage at the input.

As shown in Figure 3, the zeners are buffered from the cascode collectors by emitter followers. The pulldown current through the zener-follower combination must be made large enough to discharge the node capacitance when the follower swings in the negative direction. The minimum value necessary is determined by the node capacitance, the signal swing, and the amount of delay that can be tolerated. The amount of signal swing can be reduced by adding clamping diodes across the collectors of the cascode. Regular diode-connected transistors could be used, but would add considerable collector-to-substrate capacitance across the load resistors as well as base-to-emitter capacitance between them. Schottky diodes, on the other hand, require little additional chip area, and are very fast. With clamping, some of the common-mode range lost when the cascode was added can be regained because the cascode transistors can be biased closer to the positive supply without fear of going into saturation at the extremes of the signal swing. The use of Schottky diodes, however, puts a few more gray hairs on the head of the process engineer since he has to control another set of characteristics without affecting the other parameters. The circuit values given in Figure 3 are designed for a minimum differential gain of 16, and a minimum negative-going slew rate at the output of the level-shifter of 1000V/μs.

As mentioned earlier the design of the output stage (Figure 4) can vary little from that of a standard ECL gate. The output emitter followers have to be large enough to handle loading by a 50Ω transmission line (25mA), yet small enough not to add a lot of capacitance that would slow down the response. Therefore, the transistor design must be as efficient as possible with regard to physical size and current-carrying

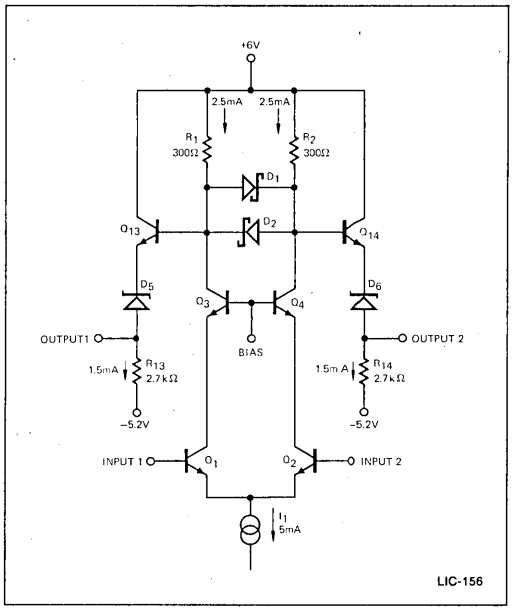


Figure 3. Basic cascode gain stage

capacity. Since the input common-mode level to the gate varies with changes in the power supplies and resistor tolerance, a current source is used to supply the emitters of the gate, rather than the usual resistor to the negative supply. The design of this current source must be such as to provide the correct logical "1" and "0" levels at the output and the proper variation with temperature and power supply changes. The propagation delays to either output of this gate will be equal, whereas they are slightly different in a standard ECL gate owing to the additional capacitive loading on the $\overline{Q}$ output caused by the multiple input transistors.

Implementation of the latch function must be accomplished without interfering with the normal comparator operation or degrading the speed in any way. It must be as close to the input as possible to permit short input signals to be acquired and held. One simple method of adding a latch to a differential

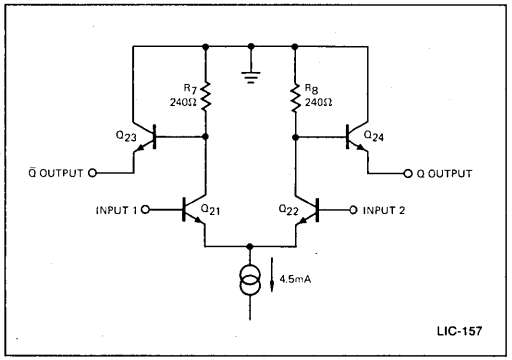


Figure 4. Output gate

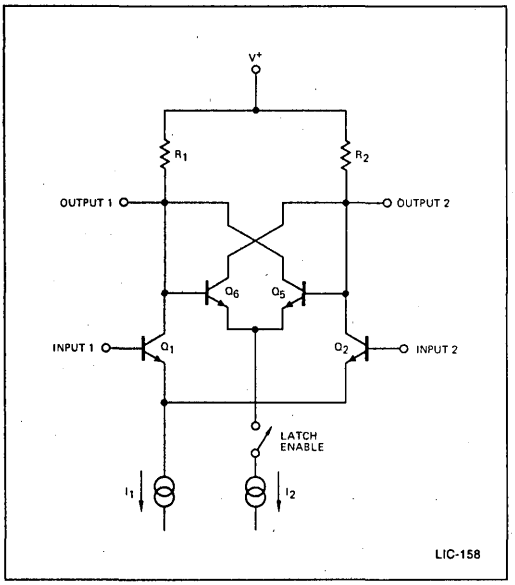


Figure 5. Simple latch circuit

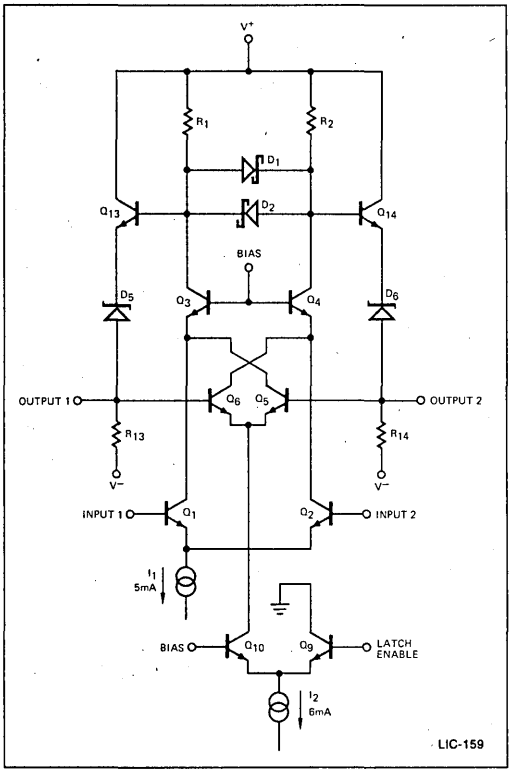


Figure 6. Cascode with latch

amplifier is shown in Figure 5. A pair of transistors, Q_5 and Q_6, are cross-coupled at the collectors of the input transistors, Q_1 and Q_2. The current source I_2 is switched on when it is desired to enable the latch. If I_2 is greater than I_1, the positive feedback via Q_5 and Q_6 will hold the circuit in whatever state it was in when the latch was turned on.

The simple circuit of Figure 5 is not the best for speed because of the added capacitance of Q_5 and Q_6 and the fact that they can saturate unless the signal swings are very small. However, it can be adapted to the cascode stage quite nicely as illustrated in Figure 6. Drive for the positive feedback transistors is taken from the level shifters, and the collectors go to the emitters of the cascode. With this arrangement there is no significant capacitive loading on the gain stage at all. The current source is switched by another differential amplifier, Q_9–Q_{10}, referenced to the ECL logic threshold voltage. This provides the correct input levels for the Latch Enable being driven from a standard ECL gate as well as being very fast, since only currents are being switched.

The latch current source (I_2) must be about 1mA greater than the input current source (I_1) to ensure positive latching for any condition of input signal. Thus, for 5mA in the input stage, at least 6mA must be used to power the latch. This amounts to a lot of power consumed for a function that some users may never even need. However, there is a way to cut the latch standby power down to zero; this is accomplished by the addition of Q_7 and Q_8, as shown in Figure 8.

To understand the function of these transistors, first refer to Figure 7. The differential voltage appearing across the emitters of the cascode transistors is equal to the input signal (for small input signals). This is because the currents through the lower pair of transistors in the cascode are equal to the corresponding currents through the upper pair, and the transistors are matched; therefore the differences in base-emitter voltages must be equal. Thus, Q_7 and Q_8 function as if they were

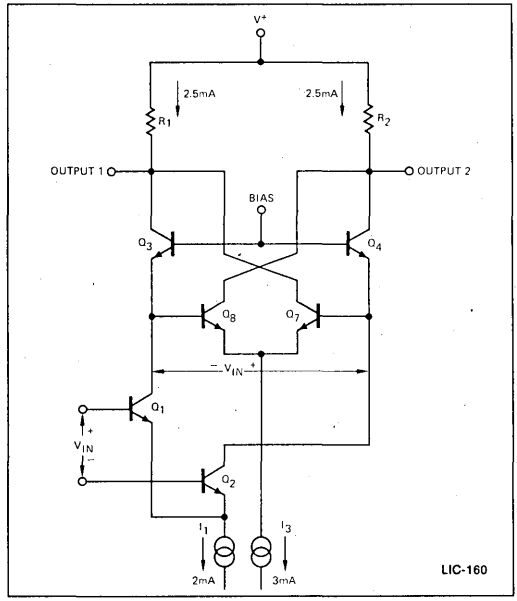


Figure 7. Cascode with "parallel" transistors

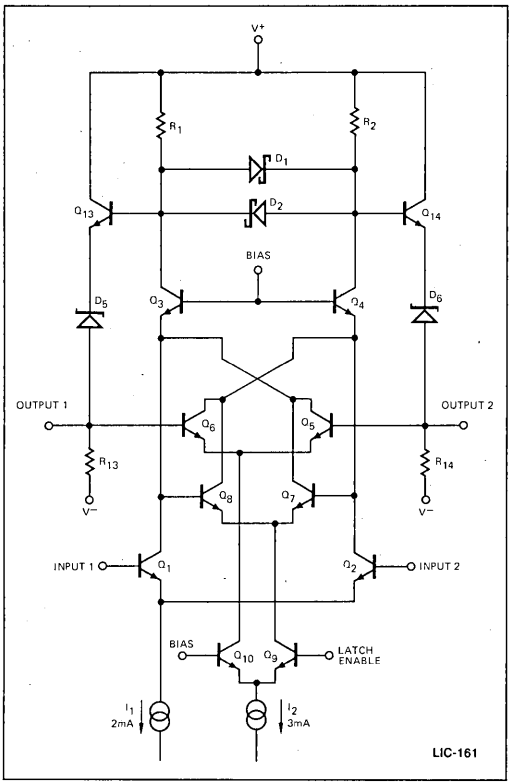


Figure 8. Complete input cascode stage with latch

simply connected in parallel with Q_1 and Q_2, as far as the net effect at the collector load resistors is concerned. To obtain the desired total stage gain, the current I_1 can be 2mA and I_3 can be 3mA.

Now refer to Figure 8. With the latch enable HIGH, Q_9 will be switched on and the 3mA current source will be supplied to the parallel transistors, Q_7–Q_8. The comparator functions normally, and no current is used up in the latch. When the latch enable goes LOW, I_2 will be switched through Q_{10} to the positive feedback transistors, robbing 3mA from the gain stage and giving it to the latch. The latch current is now 1mA greater than the input stage current, but the total current required is still only 5mA. As with the latch transistors, the collectors of the parallel transistors are connected to the emitters of the cascode, so no additional capacitance is added across the load resistors. This places the requirement on Q_7 and Q_8 that they maintain their high f_T at zero collector-to-base voltage.

The use of the parallel transistors has the added bonus that the input bias currents are decreased by more than a factor of two, thus reducing their influence on the offset voltage. The penalty paid is that all three pairs of junctions (Q_1–Q_2, Q_3–Q_4 and Q_7–Q_8) add equally to the input offset. Once again, the processing must be carefully controlled to keep the overall offset within the 2mV goal.

The complete circuit of the comparator is given in Figure 9. It includes some additional refinements as well as the DC biasing. The drive for the latching transistors is taken from the emitters of the second cascode rather than from the level-shifting zeners. This removes their input capacitance from the level shifter and also ensures that Q_{10} cannot saturate. A resistor (R_9) is included to center the common-mode voltage at the input to the gate within its dynamic range; this prevents saturation of the gate or its current source over the expected range of signal swing, temperature drift and supply voltage variations. A separate ground is used for the output emitter followers so that heavy loading at the output will not couple back into the remainder of the circuit. The DC bias chain for the current sources is referenced to ground and the negative supply, so the output logic levels will track those of other ECL circuits connected to the same negative supply. The current sources are designed to stay constant with temperature, which keeps the open-loop gain high at elevated temperatures (>1000 at +125°C), and thus helps to maintain good propagation delay.

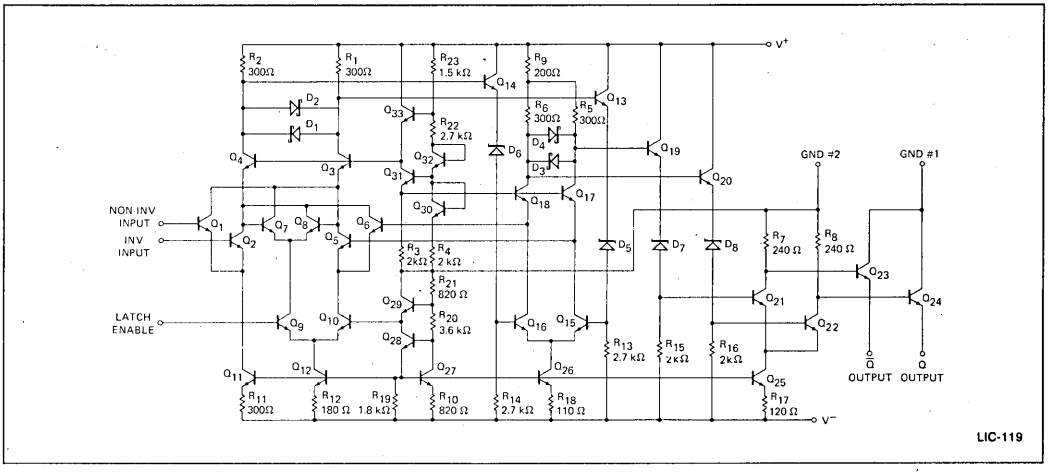


Figure 9. Complete schematic of the Am685 comparator

A New High-Speed Comparator

PROCESS TECHNOLOGY

Circuit design requirements for high speed and a latch function result in an input structure that has three pairs of transistors, the matching of which determines the offset voltage. This dictates that the matching of V_{BE} shall be extremely good between the transistors in each pair in order to meet the 2mV maximum offset voltage target. For the speeds necessary the transistor f_T has to be in the region above 1 GHz, so high-frequency performance can not be compromised. The slew rate of the input stage has to be very high for acceptable response with large input signals. This is achieved by high operating current and low stray capacitances. It is very desirable to keep both the input bias current and the input offset current very low so that the impedances in the source voltages do not introduce intolerable input voltage errors. It would be possible to use a Darlington-connected input stage to achieve these low currents, but the penalty exacted in offset voltage, offset voltage drift, and propagation delay is unacceptable, so high current-gain transistors that match extremely well are needed. The problems are thus centered on achieving very well-matched transistors with high beta and high f_T.

As previously mentioned, it is desirable in a comparator to have a wide common-mode voltage range and high power-supply rejection ratio. This is facilitated by using Schottky diodes to clamp the collector-to-collector swings in the first two stages. Schottky diodes can be fabricated simply by making a window in the oxide over the N-type epitaxial layer and using the same evaporated aluminum as is used for the interconnects (see Figure 10). The contact potential between silicon and aluminum causes a potential barrier to the flow of electrons. Making the metal positive lowers this barrier, allowing electrons to pass over it by virtue of their thermal energy. This process is essentially the same as thermionic emission. Since these electrons are majority carriers, Schottky diodes show extremely fast turn-off characteristics, desirable in this application. Why the Schottky diode is so attractive is that the forward voltage necessary to produce a given current may be several hundred millivolts less than that required to produce the same current in a p-n junction diode of about the same size. It can thus be used as a "clamp" to prevent a bipolar transistor from saturating, when connected from collector to base so as to prevent the forward voltage of the collector-base diode from rising to a level sufficient to cause appreciable current flow in the collector-base diode. This is the common application in Schottky TTL circuits.

In the ECL comparator the use is different. Here they are used back-to-back to limit the differential voltage swings between the collectors in both the first and the second stages. Connected in this way the reverse voltage seen by one Schottky diode is equal to the forward voltage drop of the other diode. Because this voltage is so small reverse leakage is not a great problem. In the simple Schottky diode structure, as described above, the reverse leakage is high. Most of this leakage current is generated at the perimeter of the metal, where there is an electric field concentration. In order to reduce this field the metal is extended all around the opening in the oxide, overlaying this oxide. Spacing the metal from the silicon in this way reduces the field and hence the leakage. In applications where low leakage is critical, the use of a P+ guard ring is called for, but this carries with it extra capacitance, so in view of the fact that the reverse voltage is so low the guard ring technique was discarded for this application. Even so, the diodes used in the comparator have low leakage characteristics with a breakdown at about 45V.

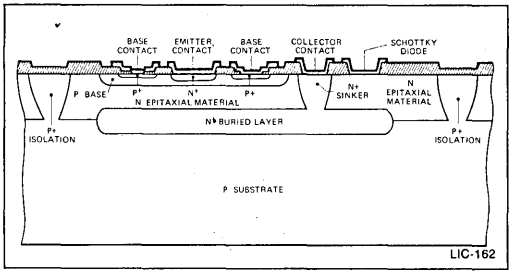


Figure 10. Cross section of transistor and Schottky diode showing sinker and P+ base contact enhancement

At the very high speeds being considered, much effort has to go into reducing capacitances and resistances. Thinning down the epitaxial layer to the minimum required to sustain the voltages encountered is of benefit in two ways: 1) the collector-isolation sidewall area is reduced, lowering the collector-to-substrate capacitance; 2) the collector-series resistance is reduced. The two major contributions to collector-series resistance are the resistance of the epitaxial material between the emitter and the buried N+ layer, and the resistance of the epitaxial layer between the collector contact and the buried layer. However, the first resistance is subject to reduction by conductivity modulation during operation of the device and thus is less important than the second term. The second term can be made very small by using a "sinker", which is a high concentration N-type diffusion from the surface, through the epitaxial layer, to the buried N+ layer. Contact to the collector is then made to the surface of the sinker. (see Figure 10)

Collector-to-base capacitance is held low by using very small dimensions and by using a relatively high epitaxial layer resistivity. The latter also serves to reduce the collector-to-substrate capacitance. A further reduction in collector-to-base capacitance results from using a shallow, high sheet-resistivity diffusion for the base. However, this raises the base resistance, both because the bulk resistance from the contact to the active base region is increased and because the specific contact resistance is increased. These resistances may be reduced by depositing P+ regions under the base contact areas after the main base diffusion.

A compromise has to be made in selecting emitter width. Large emitters are desirable for V_{BE} matching, but very small emitters are essential for high f_T. A stripe emitter, .25-mil wide and 1-mil long, was chosen as optimum. A difference in width, between two otherwise identical emitters, of .01-mil will be sufficient to cause an offset voltage of 1 mV. From this, it can be seen that the photolithography must be extremely carefully controlled, since the offset voltages of three pairs of transistors are summed to give the total offset of the comparator. Because the emitters are so narrow the normal procedure of making a contact cut inside of the emitter cannot be used. Instead, the emitter oxide is simply dissolved in hydrofluoric acid immediately before the aluminum evaporation in order to expose the emitter. As a consequence, the lateral distance between the metal and the emitter-base junction is very small, being equal to the lateral diffusion of the emitter. This means that the sintering process must be carried out at a temperature lower than is customary in linear circuit manufacture in order to avoid short-circuiting the

emitter-base junction by lateral migration of aluminum. An additional reason for lowering the sintering temperature is to avoid penetration of aluminum down through the emitter and base, causing emitter-to-collector shorts.

The requirement for high current gain, for low input bias currents, necessitates narrow base widths. Emitter-to-collector shorts can be a problem in these shallow, narrow-base structures. The probability of shorting can be minimized by careful cleaning procedures and by proper emitter doping levels. Keeping the emitter doping level low also reduces the magnitude of the "emitter dip" effect, whereby the diffusion coefficient of the boron in the region under the emitter is greatly increased by the lattice strain caused by the emitter, resulting in the running-on of the base under the emitter, making it very difficult to achieve a narrow base width.

An area that is neglected in digital circuit processing, because high beta is not necessary, but which is of major importance in linear processing, is the control of surface conditions. If high current gains are to be realized, both the surface area of the emitter-base-depletion region and the surface recombination velocity must be minimized. The former implies that ionic contamination, such as sodium ions, must be eliminated and that the surface state charge density, Qss, should be made as low as possible. The surface recombination velocity is proportional to the fast surface state density and so can be minimized by making this density very low. These three goals; low ionic contamination, low Qss and low fast surface state density are achieved by using the well known techniques of MOS and linear circuit processing, such as annealing in an inert atmosphere and proper choice of sintering cycle.

In the interests of minimum capacitance, the metal interconnects are designed to be narrower than is usual in linear circuits. Special etching techniques have to be employed in order to reproduce these narrow lines reliably. These lines can be seen in the photomicrograph of Figure 11.

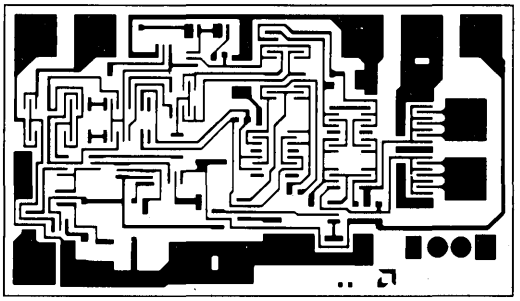


Figure 11. Photomicrograph of the Am685 comparator

PERFORMANCE

The primary design objective for the comparator was to obtain under 10ns propagation delay for large input signals with small overdrive. It should then be as fast or faster for any other input conditions. The performance of the Am685 comparator for a 100mV step input at various overdrives is shown in Figures 12 and 13. The propagation delay is measured from the time the input step crosses the input threshold voltage to the time the output crosses the logic threshold voltage. The input threshold voltage (i.e., the offset voltage) was adjusted for the figures so that the delay can be simply measured by

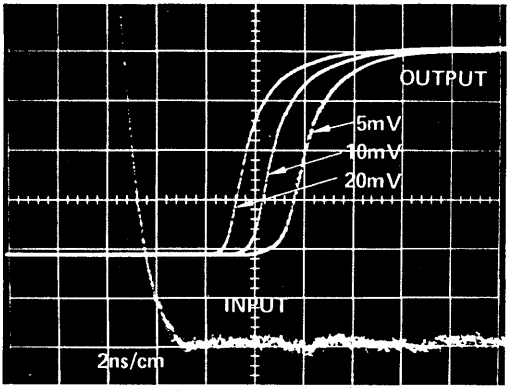


Figure 12. Tpd —"1" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

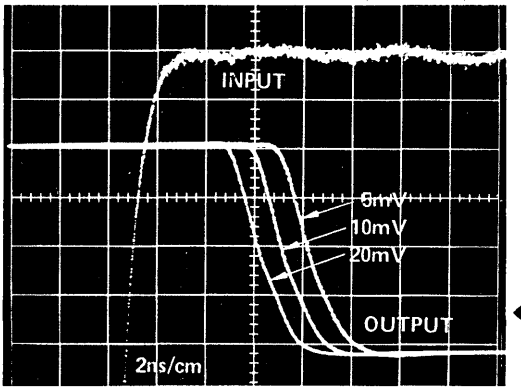


Figure 13. Tpd —"0" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

counting up 5, 10, or 20mV from the bottom of the input pulse. The input pulse, therefore, is displayed on a magnified scale to facilitate this measurement and also to illustrate the purity of input signal required to make accurate measurements at millivolt overdrives.

For a 100mV input step and 5mV overdrive, the propagation delay for a logical "0" is 6.3ns and for a logical "1" is about 300ps less. A graph of delay as a function of overdrive is given in Figure 14. It was previously stated that any other condition

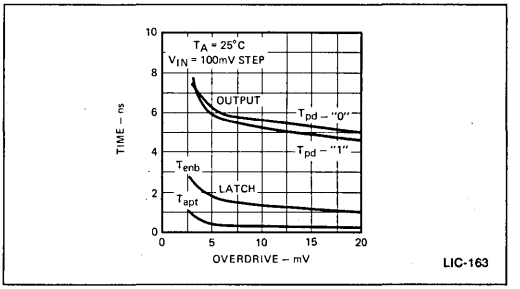


Figure 14. Delay times as a function of input overdrive

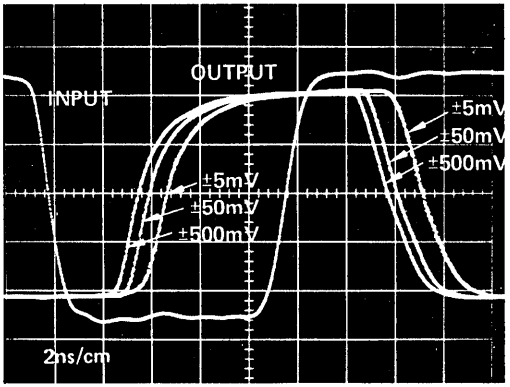


Figure 15. Response to symmetrical input signals

of input signal should give faster response (refer back to Figure 1). This is demonstrated by Figure 15, which illustrates the response of the comparator to symmetrical inputs ranging from ±5mV to ±500mV. The speeds are at least 1 to 2ns faster than for small overdrives.

Figure 16 shows how the delay time varies with temperature. The adverse effects of resistor and gain changes at elevated temperatures result in an increase in delay from 6.3ns at 25°C to 8.4 ns at 85°C and 10.4 ns at 125°C. All of the above data were taken with output loads of 50Ω connected to −2.0V. For lighter loading (such as 500Ω to −5.2V) the output rise and fall times and propagation delays are all slightly faster.

The usefulness of the latch is directly related to how quickly it can be enabled following a change in the input signal. The input signal must be present long enough to pass through the first stage of the comparator before the latching transistors can act upon it. The minimum time that the input must be present before the latch can be turned on is defined as the latch enable time. This is measured as the minimum time that must elapse

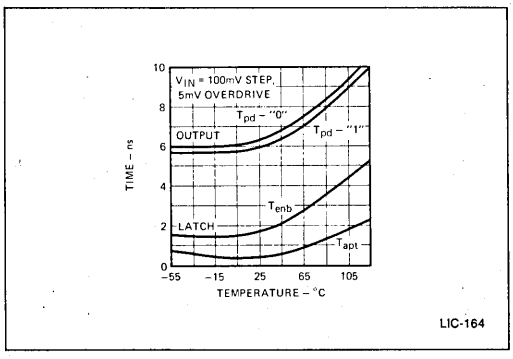


Figure 16. Delay times as a function of temperature

between the time the input step crosses the input threshold voltage and the time the latch enable input crosses the logic threshold voltage for which the comparator outputs will assume the correct states.

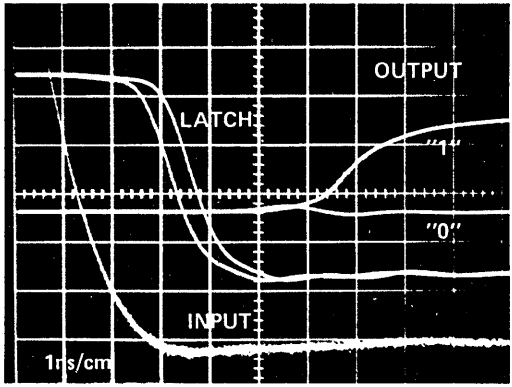


Figure 17. Latch enable time and latch aperature time for 100mV input step, 5mV overdrive (input = 5mV/cm, latch = 200mV/cm, output = 400mV/cm)

The performance of the latch function is illustrated by Figure 17. The input signal is the standard 100mV step with 5mV overdrive and is in the direction to cause the output to switch from a logical "0" to a logical "1". The delay of the latch signal relative to the input is adjusted until the output just switches to a "1"; this is the latch enable time and under these conditions is 1.8 ns. The difference between the latch timing for which the output just barely switches and when it does not switch is the latch aperture time; this is about 500ps for 5mV overdrive. The performance of the latch with input overdrive and temperature generally follows that of the propagation delays (Figure 14 and 16).

The overall performance of the Am685 is summarized in Table II. It is apparent from the table and the previous discussion that the device is ideally suited for applications where both precision and high speed are required, such as in analog-to-digital converters, data acquisition systems, and optical isolators. The device is the first in a family of new wideband linear integrated circuits designed to meet the requirements of very high-speed systems.

Propagation Delay (100mV step, 5mV overdrive)	6.5ns MAX
Input Offset Voltage	2.0mV MAX
Average Temperature Coefficient Of Input Offset Voltage	10μV/°C MAX
Input Offset Current	1.0μA MAX
Input Bias Current	10μA MAX
Common Mode Voltage Range	±3.3V MIN
Common Mode Rejection Ratio	80dB MIN
Supply Voltage Rejection Ratio	70dB MIN
Positive Supply Current	22mA MAX
Negative Supply Current	26mA MAX

Table II: Performance Characteristics of the Am685 Comparator (T_A = 25°C, V^+ = 6.0V, V^- = −5.2V, R_L = 50Ω to −2.0V)

THE A-D APPLICATION

Very fast, precision, analog-to-digital conversion stands to benefit considerably from the availability of a fast comparator. As the block diagram of a fast 10-bit converter in Fig. 18 shows, a typical rapid conversion technique may resemble the use of feedforward compensation in an operational amplifier.

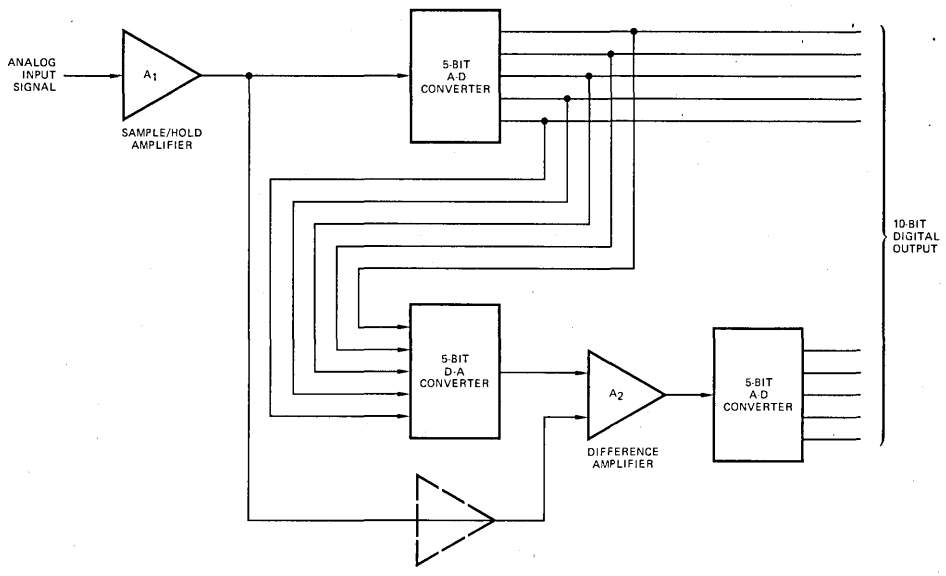
The analog input signal is sampled at the beginning of a conversion period and fed to a fast five-bit a-d converter, which provides the first five most significant bits of the output. These five bits also drive a companion d-a converter, which must be accurate to better than 10 bits. The output of the d-a converter is a replica of the input signal, quantized to five bits. This is compared with the actual input signal stored in the sample-and-hold amplifier. The difference between the two analog levels is the remaining part of the input signal that must be quantized. This difference is amplified and applied to another five-bit a-d converter to provide the five least-significant-bits of the final output.

Typical five-bit a-d converters may consist of 31 106-type comparators connected to the signal source and referenced to the full-scale input in steps of 1/32. The output of each comparator goes into a latch, and the latch outputs are decoded by three stages of TTL gages to develop the five-bit digital output.

Typical propagation delays are 40 ns for the comparators, 22 ns for the latches, and 10 ns for the decoding, resulting in a total delay of 80 ns. Average settling time for the five-bit d-a converter and the difference amplifier together comes to about 200 ns, and the settling time for the input sample-and-hold amplifier is 70 ns. Thus, the over-all conversion time for this 10-bit converter amounts to 430 ns.

Substitution of the high-speed ECL comparator for the 106 type in each of the five-bit converters leads to a significant improvement in propagation delay. The typical delay of the comparator is about 6.5 ns, and no external latch is required. With ECL it is possible to wire-OR outputs, so only one level of decoding gates is required. Allowing 1.5 ns for the gates, the total five-bit conversion time is only 8 ns – a tenfold improvement over the existing circuit.

If the latch function of the comparators is used as the sample-and-hold for the first five-bit converter, the sample-and-hold can be put in parallel with the first quantization step, as shown by the dotted lines in Fig. 18. This eliminates its settling time from the over-all delay of the system. With the new comparator, the total 10-bit conversion time drops to 216 ns, with over 90% of the delay attributable to the d-a converter and the difference amplifier. Moreover, the availability of an 8 ns five-bit converter should provide the impetus to improve the slower sections of the system. A 10-bit a-d converter with a delay under 100 ns is not an extravagant prediction.



If the standard 106-type comparator in this a-d converter is replaced by the 10 ns device, a tenfold improvement in speed is possible. What is more, the ECL makes possible both wired-OR outputs and a single level of decoding for gates.

LIC-165

Figure 18. Analog to digital.

Am686

Voltage Comparators

Distinctive Characteristics

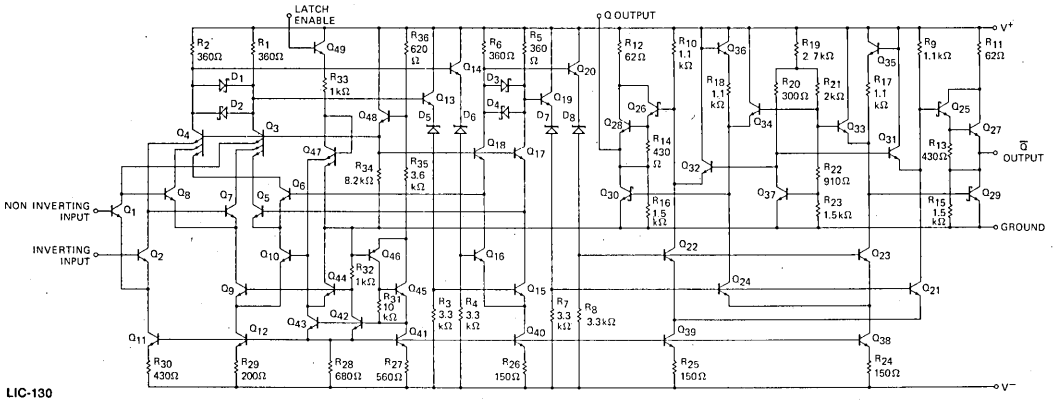
- 12ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary Schottky TTL outputs
- Fanout of 5

FUNCTIONAL DESCRIPTION

The Am686 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with Schottky TTL. The output current capability is adequate for driving 5 standard Schottky inputs. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is LOW, the comparator functions normally. When the Latch Enable is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable may be left open or connected to ground.

CIRCUIT DIAGRAM



LIC-130

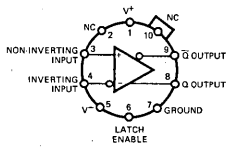
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
Am686	Metal Can	0 to +70°C	AM686HC
	DIP	0 to +70°C	AM686DC
	8-Pin Mini	0 to +70°C	AM686CN
	8-Pin Mini	0 to +70°C	AM686CN-1
Am686	Metal Can	−55 to +125°C	AM686HM
	DIP	−55 to +125°C	AM686DM
Am686	Dice	0 to +70°C	AM686XC
	Dice	−55 to +125°C	AM686XM
Am686	Leadless	0 to +70°C	AM686LC
	Leadless	−55 to +125°C	AM686LM

*Also available with burn-in processing. To order add suffix B to part number.

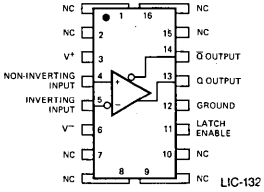
CONNECTION DIAGRAMS – Top Views

Metal Can H-10-1



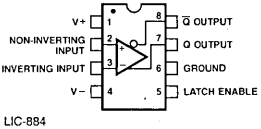
LIC-131

Dual In-Line D-16-1



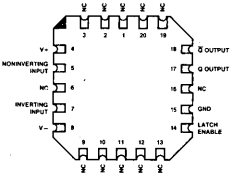
LIC-132

Dual In-Line P-8-1



LIC-884

Leadless Chip-Pak L-20-1



Note: On metal package, pin 5 is connected to case. On DIP, pin 6 is connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7V
Negative Supply Voltage	−7V
Input Voltage	±4V
Differential Input Voltage	±6V
Power Dissipation (Note 2)	600mW
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	−65 to +150°C

Operating Temperature Range	
Am686C and Am686C-1	0 to +70°C
Am686M	−55 to +125°C
Operating Supply Voltage Range	
Am686C and Am686C-1	V^+ = +5.0V ±5%, V^- = −6.0V ±5%
Am686M	V^+ = +5.0V ±10%, V^- = −6.0V ±10%
Minimum Operating Voltage (V^+ to V^-)	9.7V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES

(Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am686C	Am686C-1	Am686M	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, T_A = 25°C $R_S \leq 100\Omega$	3.0 3.5	6.0 10.0	2.0 3.0	mV max mV max
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	10	–	10	µV/°C max
I_{OS}	Input Offset Current	25°C ≤ $T_A \leq T_A$ (max) $T_A = T_A$ (min)	1.0 1.3	1.0 1.3	1.0 1.6	µA max µA max
I_B	Input Bias Current	25°C ≤ $T_A \leq T_A$ (max) $T_A = T_A$ (min)	10 13	12 20	10 16	µA max µA max
V_{CM}	Input Voltage Range		+2.7, −3.3	+2.7, −3.3	+2.7, −3.3	V min
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, −3.3V ≤ V_{CM} ≤ +2.7V	80	–	80	dB min
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$	70	–	70	dB min
V_{OH}	Output HIGH Voltage	I_L = −1.0mA, $V_S = V_S$ (min)	2.7	2.7	2.5	V min
V_{OL}	Output LOW Voltage	I_L = 10mA, $V_S = V_S$ (max)	0.5	0.5	0.5	V max
I^+	Positive Supply Current		42	50	40	mA max
I^-	Negative Supply Current		34	40	32	mA max
P_{DISS}	Power Dissipation		415	500	400	mW max

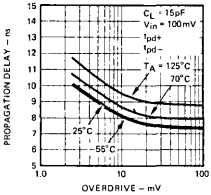
Switching Characteristics (V^+ = +5.0V, V^- = −6.0V, V_{in} = 100mV, V_{od} = 5.0mV, C_L = 15pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min) ≤ $T_A \leq$ 25°C $T_A = T_A$ (max)	12 15	12 –	12 15	ns max ns max
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min) ≤ $T_A \leq$ 25°C $T_A = T_A$ (max)	12 15	12 –	12 15	ns max ns max
Δt_{pd}	Difference in Propagation Delay between Outputs	T_A = 25°C	2.0	2.0	2.0	ns max

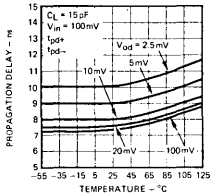
Notes:
2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C; for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.
3. Unless otherwise specified, V^+ = +5.0V, V^- = −6.0V and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.
4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/µs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

PERFORMANCE CURVES

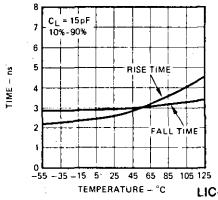
Propagation Delay as a Function of Input Overdrive



Propagation Delay as a Function of Temperature

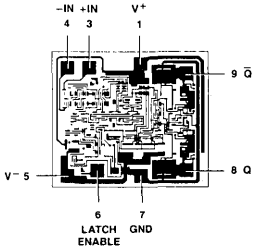


Output Rise and Fall Times as a Function of Temperature



LIC-133

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.046" X 0.053"

Am687 • Am687A

Dual Voltage Comparators

Distinctive Characteristics

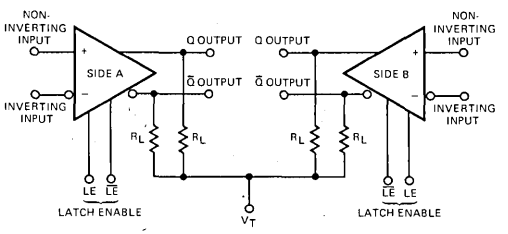
- 8.0ns MAXIMUM PROPAGATION DELAY AT 5mV OVERDRIVE
- Complementary ECL outputs
- 50Ω line driving capability

FUNCTIONAL DESCRIPTION

The Am687 and Am687A are fast dual voltage comparators constructed on a single silicon chip with an advanced high-frequency process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

The comparators are similar to the Am685 high-speed comparator but have been designed to operate from a 5V positive supply (instead of 6V), dissipating less power than two Am685's. Separate latch functions are provided to allow each comparator to be independently used in a sample-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and $\overline{LE}$ is LOW, the comparator functions normally. When LE is driven LOW and $\overline{LE}$ is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

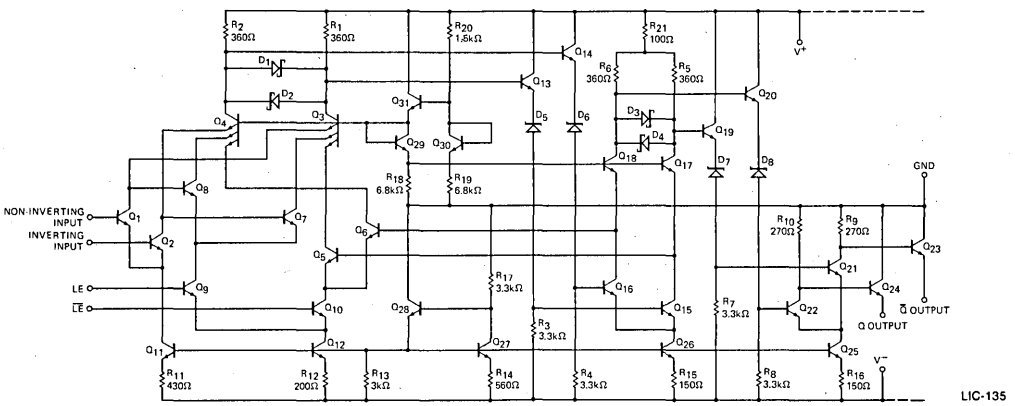
FUNCTIONAL DIAGRAM



LIC-134

The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50-200Ω connected to −2.0V, or 200-2000Ω connected to −5.2V.

CIRCUIT DIAGRAM (Each Comparator)



LIC-135

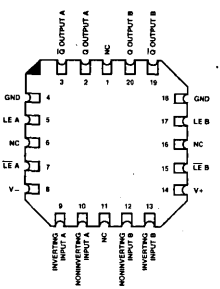
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
Am687A	DIP	−30 to +85°C	AM687ADL
Am687A	DIP	−55 to +125°C	AM687ADM
Am687	DIP	−30 to +85°C	AM687DL
Am687	DIP	−55 to +125°C	AM687DM
Am687	Dice	−30 to +85°C	AM687XL
Am687	Dice	−55 to +125°C	AM687XM
Am687A	Leadless	−30 to +85°C	AM687ALL
Am687A	Leadless	−55 to +125°C	AM687ALM
Am687	Leadless	−30 to +85°C	AM687LL
Am687	Leadless	−55 to +125°C	AM687LM

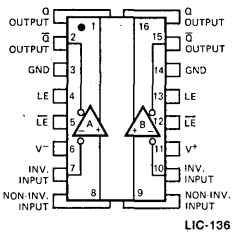
*Also available with burn-in processing. To order add suffix B to part number.

CONNECTION DIAGRAMS – Top Views

L-20-1



D-16-1



LIC-136

Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 2)	600 mW

Operating Temperature Range	
Am687-L, Am687A-L	−30°C to +85°C
Am687-M, Am687A-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C
Minimum Operating Voltage (V^+ to V^-)	9.7 V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics

Symbol	Parameter	Conditions (Note 3)	Am687A-L Am687-L Min.	Am687A-L Am687-L Max.	Am687A-M Am687-M Min.	Am687A-M Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−3.5	+3.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$25°C \leq T_A \leq T_{A(max.)}$	−1.0	+1.0	−1.0	+1.0	µA
		$T_A = T_{A(min.)}$	−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$25°C \leq T_A \leq T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_S	Minimum Latch Set-up Time	$T_A = 25°C$		4.0		4.0	ns

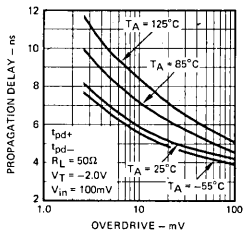
Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.

3. Unless otherwise specified $V^+ = +5.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

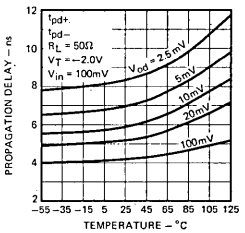
4. Because of the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specification given.

PERFORMANCE CURVES

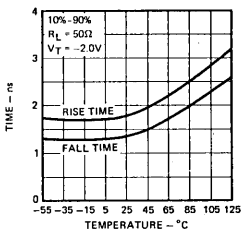
Propagation Delays as a Function of Input Overdrive



Propagation Delays as a Function of Temperature

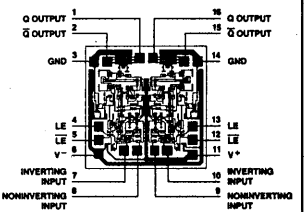


Output Rise and Fall Times as a Function of Temperature



LIC-137

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.056"

Am685/Am686/Am687 Designing with High Speed Comparators

By Leonard Brown

INTRODUCTION

The Am685, Am686 and Am687 are a family of high-speed sampling comparators capable of detecting low-level signals of the order of 5-10mV in 12-15ns over the temperature range $-55^{\circ}C \leqslant T_A \leqslant 125^{\circ}C$. The Am686 is fully TTL-compatible and complementary outputs are available generated from a true differential output stage assuring a maximum output skew of under 2ns at 25°C. The Am685 and Am687 are single and dual ECL-compatible versions, respectively, and have output skews of less than 1ns. A high-speed latch is incorporated in the input stage permitting input signals to be acquired in 4.0ns maximum for the ECL versions and 6.0ns for the TTL device.

Applications of the devices are not limited to high-speed designs as the combination of the excellent DC input characteristics, availability of true differential outputs and the latch function permit unique solutions for slower speed applications where the response time of the comparators can be considered negligible.

THE SAMPLING COMPARATOR

The sampling comparator may be visualized as a conventional voltage comparator with the provision that the outputs may be latched into the logic states determined by the **input signal conditions existing at the time of application of the latch signal.** This is achieved by incorporating the latch circuitry in the input stage of the device. The minimum latch enable pulse width is necessarily less than the propagation delay of the device and, therefore, the comparator can be unlatched for a fraction of its propagation delay (4.0ns for the Am685). The outputs will then change in accordance with the input conditions existing at the time of the latch signal. Note: It is impossible for the comparator to oscillate under these conditions.

If the latch function is not used, the device operates as a conventional voltage comparator.

BACK TO BASICS

Comparators are designed to have both high gain and large bandwidth. This creates instability problems or oscillations when the device outputs are in the transition region. The tendency of a device to oscillate is a function of the layout, (poor layout increasing the amount of feedback caused by parasitic capacitance) and the source impedance of the circuit employed (The higher the source impedance the less parasitic coupling is necessary to cause oscillation.) It is mandatory with comparators of the gain and bandwidth of the Am685, Am686 and Am687 to ensure that power supplies are well decoupled, lead lengths are kept as short as possible, and wherever possible (especially in the case of the Am686), a ground plane should be employed.

In addition to reducing the effects of stray capacitance, a ground plane substantially reduces the possibility of the output current spike coupling back to the inputs through the ground lead when the TTL output stages switch.

The minimum slew rate at which the input signal must cross the threshold region to prevent oscillation, regardless of the particular layout parasitics, may be determined by applying a DC voltage to the input until the circuit just commences to oscillate and increasing this voltage until the oscillation ceases. The minimum necessary input slew rate is then given by $\Delta V/t_{pd}$ MIN, where ΔV is the input voltage required to prevent oscillation and t_{pd} MIN is the minimum propagation delay of the comparator.

The minimum slew rate will be found to be a function of source impedance and source impedance mismatch.

The curves of Figures 1 and 2 show the minimum slew rate for the Am686 as a function of source impedance and source impedance mismatch.

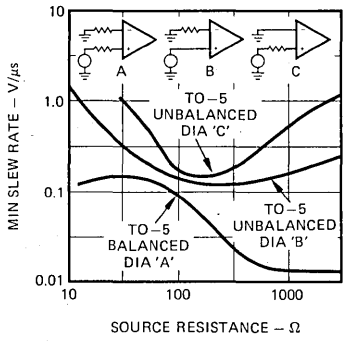


Figure 1. Minimum Slew Rate Versus Source Resistance (TO–5).

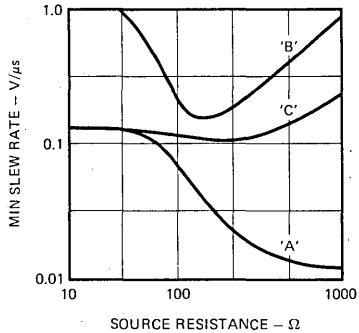


Figure 2. Minimum Slew Rate Versus Source Resistance (DIP).

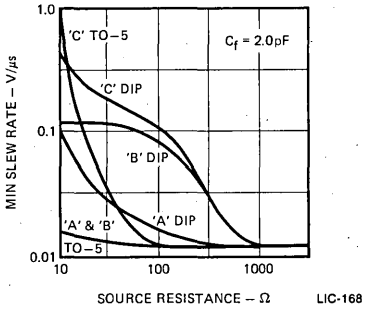


Figure 3. Minimum Slew Rate Versus Source Resistance (TO–5 & DIP).

It can be seen that unbalanced sources dramatically effect the minimum input slew rate required. Note that for optimum performance, the source impedance seen by the comparator should be both DC and AC balanced to reduce the differential feedback to a minimum.

The effect of an AC unbalanced source is seen especially on the Am686 as when the output switches, the output current spike is coupled back to the input. This can be eliminated by forcing the AC unbalance to result in positive feedback, which may be achieved by decoupling the inverting input or applying positive feedback via a 2-4pF capacitor from the Q output to the non-inverting input.

The curves of Figure 3 illustrate the improvement in minimum slew rate when a small amount of positive feedback is employed by virtue of a 2pF feedback capacitor.

OPTIMUM SOURCE CONDITIONS (C_f = 0pF)

With low source impedances (< 50Ω), the majority of the feedback between the output and the input occurs internal to the device. As the source impedance is raised, external feedback increases through the parasitic feedback capacitance until, at high source impedances, the external feedback dominates. This explains the anomolous characteristics of the minimum slew rate curves and suggests that the optimum source resistance for the device is between 300 and 500Ω for unbalanced sources and is approximately 1000Ω for a balanced source.

OPTIMUM SOURCE CONDITIONS (C_f = 2pF)

With a source impedance of 100Ω, the minimum slew rate is 0.15V/μs for the DIP configuration and 0.02V/μs for the TO-5. For balanced sources the minimum slew rate is 0.03V/μs for $R_S \geq 100\Omega$ and for a source impedance between 1kΩ and 3kΩ, the minimum slew rate is <0.02V/μs regardless of impedance, DC imbalance or package type.

The use of the feedback capacitor is recommended when:

1. The input slew rate is within a factor of 2 greater than the minimum theoretical slew rate.
2. System constraints do not permit optimisation of layout and lead lengths.
3. Unbalanced source impedances are used (it is not always possible to provide input conditions which are both DC and AC balanced).

A FAMILY AFFAIR

It must be stressed that the concepts discussed concerning source imbalance and minimum input slew rate apply to all devices in the family. The Am686 was highlighted as it is more sensitive to layout constraints and parasitic feedback because of its significantly higher voltage gain.

Similarly all of the applications which follow may be implemented with any device in the series provided due caution is exercised with regard to the different output logic levels.

THE RELAXATION OSCILLATOR

The principal problems in the design of a classical relaxation oscillator are:

1. The variation in potential to which the energy storage device (normally a capacitor) is charged.
2. The variation in the threshold level at which the capacitor is to be discharged.
3. The variation inherent in the sensor element (normally a comparator) in detecting equivalence between the threshold level and the capacitor's instantaneous potential.

The variations are all functions of both time and temperature and are the primary causes of frequency drift, symmetry error, and jitter.

By taking advantage of two unique properties of the Am686, a relaxation oscillator may be designed to eliminate the first two problems and reduce the third to a second-order effect for oscillation frequencies from 1MHz to 30MHz.

The true differential output stage of the comparator ensures that the Q and $\overline{Q}$ outputs change within 1-2ns of each other. This feature ensures that the outputs can never be in the same logic state instantaneously, either HIGH or LOW, and that the only time they are equal in voltage is when traversing the logic uncertainty levels. This property permits the design of a threshold setting circuit that varies in accordance with the charging voltage applied to the timing capacitor. Therefore, any change in charging potential is automatically compensated by a corresponding change in threshold level.

Second, the combination of the short propagation delay 7-10ns, the minimum difference in propagation delay between outputs and the stability of these delays with temperature assures square wave symmetry of better than 1% @ 1MHz and 5% @ 25MHz and a frequency stability of 1% @ 10MHz and 4% @ 25MHz.

The above statements are true from device to device and over the operating temperature range of –55°C to +125°C. Over the industrial temperature range, a factor of two improvement should be obtained.

CIRCUIT THEORY (Fig. 4)

Assuming the circuit is in an oscillating mode, the voltage appearing at the non-inverting terminal will alternate between V_X and V_Y where:

$$V_X = \frac{R_1}{(R_1 + R_2)} (V_{OH} - V_{OL}) + V_{OL} \quad \text{and}$$

$$V_Y = \frac{R_2}{(R_1 + R_2)} (V_{OH} - V_{OL}) + V_{OL}$$

When $V_{+IN} = V_X$, the timing capacitor C will be charging towards V_{OH}, and when $V_{+IN} = V_Y$, the timing capacitor will be discharging towards V_{OL}.

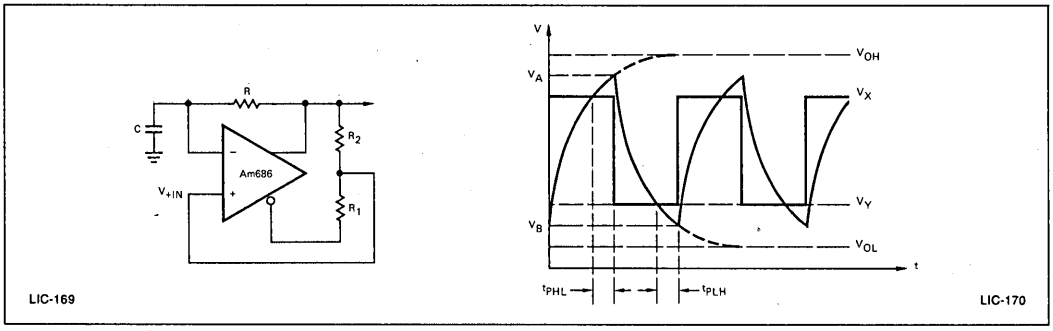


Figure 4. Circuit Design.

After the voltage on the capacitor equals the voltage on the non-inverting input, a finite time will elapse before the output of the circuit changes, during which time (the propagation delay of the Am686) the capacitor will continue to charge towards V_{OH}, or discharge towards V_{OL}.

Therefore, the capacitor will charge to a voltage

$$V_A = V_{OH} - e^{-t_{PHL}/CR} \cdot (V_{OH} - V_X)$$

and discharge to a voltage

$$V_B = V_{OL} + e^{-t_{PLH}/CR} \cdot (V_Y - V_{OL})$$

where t_{PHL} and t_{PLH} = propagation delay of the Am686 from the inputs to the output changing from HIGH – LOW and LOW – HIGH respectively.

The time to charge from V_B to V_A which is the positive half cycle is given by:

$$t^+ = CR \ln \frac{V_{OH} - V_B}{V_{OH} - V_A}$$

substituting for V_A and V_B

$$t^+ = CR \ln \left[\left(\frac{R_1}{R_2} + 1\right) e^{tPHL/CR} - 1\right]$$

Similarily the negative half cycle is given by:

$$t^- = CR \ln \frac{V_A - V_{OL}}{V_B - V_{OL}}$$

$$t^- = CR \ln \left[\left(\frac{R_1}{R_2} + 1\right) e^{tPLH/CR} - 1\right]$$

Note: The only assumptions are:

1. $(V_{OH} - V_{OL})$ of the Q output = $(V_{OH} - V_{OL})$ of the $\overline{Q}$ output.
2. Offset voltage and offset current errors are negligible.
3. $e^{t_{PLH}/CR} \times e^{-t_{PHL}/CR} = 1$

The only factor affecting pulse width variation is, therefore, t_{PHL} and t_{PLH}. As $t_{PHL} > t_{PLH}$ by 1-2ns, it is therefore anticipated that t^+ will be marginally greater than t^-.

MINIMUM OPERATING FREQUENCY

For the Am686, it is specified that the minimum slew rate at the input to insure that the device will not oscillate in the transition region is 1V/μs. This will determine the minimum operating frequency of the circuit.

The rate of change of voltage on the timing node is given by:

$$\rho = \frac{\partial v}{\partial t} = \frac{Vo}{CR} \times e^{-t/CR}$$

In the circuit,

a) $Vo = V_{OH} - V_B$ (assuming positive ramp)

and

b) $t = CR \ln \left[\left(\frac{R_1}{R_2} + 1\right) e^{t_{PHL}/CR} - 1\right]$

As the slew rate is only critical in determining the lowest operating frequency, it may be assumed that $e^{t_{PHL}/CR} = 1$ $(CR >>> t_{PHL})$; therefore, $Vo = V_{OH} - V_B \approx V_{OH} - V_Y$

$$Vo = (V_{OH} - V_{OL}) \frac{R_1}{R_1 + R_2} \qquad \text{and, } t = CR \ln \frac{R_1}{R_2}$$

$$\therefore \rho = \frac{\partial v}{\partial t} = \frac{(V_{OH} - V_{OL})}{CR} \times \frac{R_1}{R_1 + R_2} \times \frac{R_2}{R_1}$$

$$= \frac{\Delta V}{CR} \times \frac{R_2}{R_1 + R_2}$$

where, $\Delta V = (V_{OH} - V_{OL})$

The minimum operating frequency

$$f_{MIN} = \frac{1}{2\,CR \ln \frac{R_1}{R_2}}$$

substituting

$$CR = \frac{\Delta V}{\rho} \frac{R_2}{R_1 + R_2} \qquad f_{MIN} = \frac{\rho}{2\Delta V} \times \frac{(R_1/R_2 + 1)}{\ln R_1/R_2}$$

The expression for minimum frequency indicates that an optimum ratio of R_1/R_2 exists that is independent of any particular RC time constant which may have been chosen.

The ratio may be determined by differentiating f_{MIN} with respect to R_1/R_2.

$$\frac{\partial f_{MIN}}{\partial \frac{R_1}{R_2}} = \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - (\frac{R_1}{R_2} + 1)/\frac{R_1}{R_2})}{(1n\frac{R_1}{R_2})^2}$$

$$= \frac{\rho}{2\Delta V} \times \frac{1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1}}{(1n\frac{R_1}{R_2})^2}$$

Setting $\frac{\partial F}{\partial \frac{R_1}{R_2}} = 0$

$$1n\frac{R_1}{R_2} - 1 - \frac{R_2}{R_1} = 0$$

$$\frac{R_1}{R_2} = \frac{1}{1n\frac{R_1}{R_2} - 1}$$

$$\therefore \frac{R_1}{R_2} = 3.59112$$

Therefore, the lowest frequency the oscillator will perform consistent with the 1V/μs constraint is:

$$f_{MIN} = \frac{1 \times 4.6}{2 \times 3.5\ 1n\ 3.6} = .513MHz$$

D.C. OFFSET ERRORS

The presence of DC errors resulting from the bias and offset currents and offset voltage of the Am686 will cause the V_Y and V_X thresholds to be both shifted either positive or negative by an equal amount δV where δV is the sum of all such errors.

The magnitude of these effects may be calculated as follows:

When the capacitor is discharging –

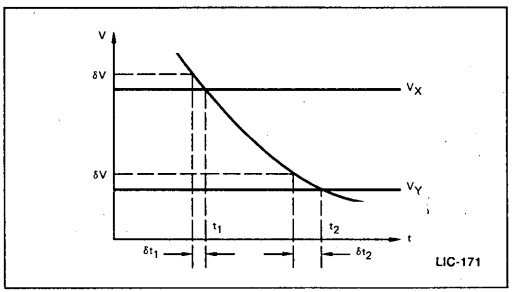


Figure 5.

$$V_{(t)} = V_o e^{-t/CR}$$

$$\frac{dv}{dt} = -\frac{1}{CR} Vo e^{-t/CR} = -\frac{1}{CR} V_{(t)}$$

$$\delta t_1 = -\frac{\delta V}{V_{(t_1)}} CR$$

$$\delta t_2 = \frac{-\delta V CR}{V_{(t_2)}}$$

Δt^- Negative Pulse Width Change =

$$\delta t_2 - \delta t_1 = \delta VCR \frac{V_{(t_2)} - V_{(t_1)}}{V_{(t_1)}\ V_{(t_2)}}$$

As $V_X = V_{t_1}, V_Y = V_{t_2}$

$$\Delta t^- = \frac{\delta VCR\ (V_Y - V_X)}{V_X V_Y}$$

Similarly for the positive pulse

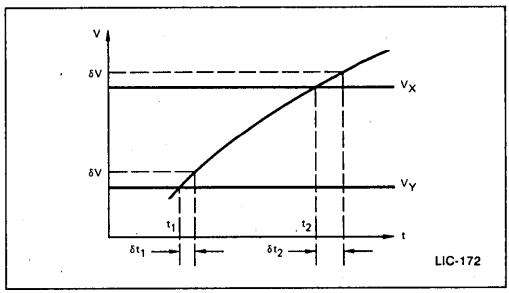


Figure 6.

$$V_{(t)} = Vo\ (1 - e^{-t/CR})$$

Whence, $dv/dt = \frac{1}{CR}(Vo - V_{(t)})$

$$\therefore \delta t_1 = \frac{\delta VCR}{Vo - V_{t_1}}$$

$$\delta t_2 = \frac{\delta VCR}{Vo - V_{t_2}}$$

Positive Pulse Width Change $\Delta t^+ = \delta t_2 - \delta t_1$

$$= \delta VCR \frac{1}{Vo - V_{(t_2)}} - \frac{1}{Vo - V_{(t_1)}}$$

In the circuit $V_{t_2} = V_X, V_{t_1} = V_Y, Vo - V_X = V_Y$

$$\Delta t^+ = \delta VCR \left(\frac{1}{V_Y} - \frac{1}{V_X}\right) = \delta VCR \frac{V_X - V_Y}{V_X V_Y} = -\Delta t^-$$

∴ Offset errors do not affect the frequency of oscillation, only the symmetry of the waveshape.

SYMMETRY ERROR

$$\text{Symmetry } S = \frac{\Delta t^+ - \Delta t^-}{2T} \times 100\% \text{ where } T = CR\ 1n\ \frac{V_Y}{V_X}$$

$$S = \frac{2\Delta t^+}{2T} \times 100\%$$

$$= \frac{\delta VCR\ (V_X - V_Y)}{V_X V_Y} \times \frac{1}{CR\ 1n\ V_Y/V_X}$$

Symmetry is worse for maximum value of $V_X - V_Y$. Maximum value of $V_X - V_Y$ occurs when R_1 and R_2 are arranged for minimum operating frequency, i.e., $R_1/R_2 = 3.6$

Substituing $\delta V = 5mV$

$$V_X/V_Y = 3.6$$

$$V_X V_Y = \frac{1}{4.6} V_{OH} \times \frac{3.6}{4.6} V_{OH}$$

$$V_{OH} = 3.5V \text{ and neglecting } V_{OL}$$

Symmetry is $< 0.38\%$

Note: 1. For any given ratio of $R_1 : R_2$ (i.e., V_X and V_Y), offset voltage Symmetry error is independent of frequency.

2. Symmetry improves to .33% @ $R_1 : R_2 = 2.5$

EXTENDING LOW FREQUENCY PERFORMANCE

If it is necessary to extend the lower limit of the oscillation frequency, a small amount of positive feedback may be introduced by connecting a 2-4pF capacitor between the Q output and the non-inverting input. This will decrease the minimum input slew rate required and enable oscillation frequencies of 1kHz to be achieved without spurious oscillations occuring on the rising or falling edges of the waveform. At frequencies below 1MHz, it is not necessary to take into account any potential frequency shift this additional feedback introduces. (Above 1MHz, it is not necessary to use this additional feedback.)

PERFORMANCE CHARACTERISTICS:

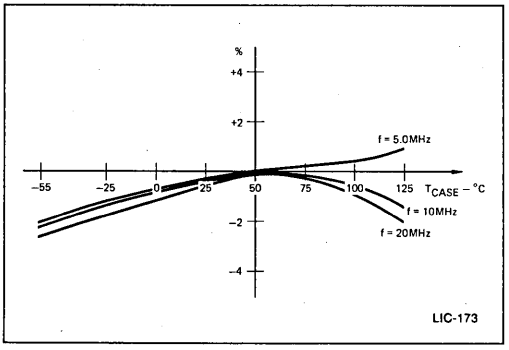


Figure 7. Percentage Change in Frequency Versus Case Temperature.

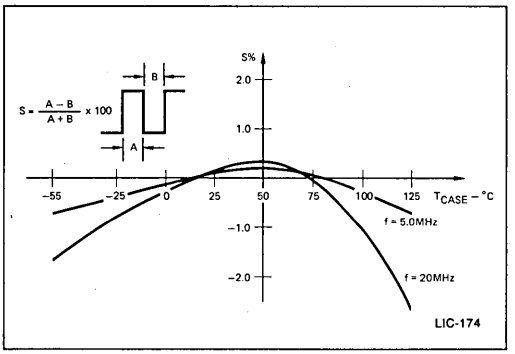


Figure 8. Change in Symmetry Versus Case Temperature.

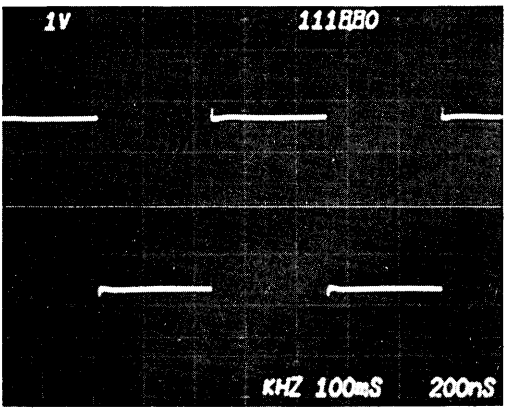


Figure 9. Output Waveform at 1.0MHz.

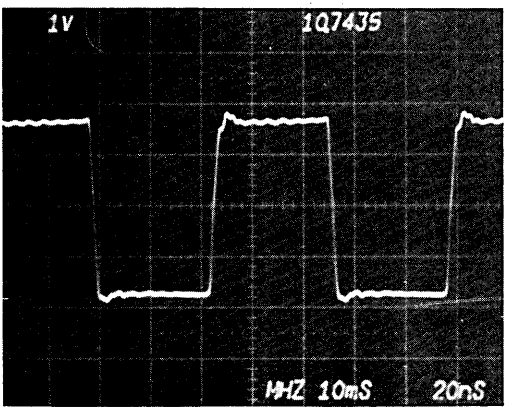


Figure 10. Output Waveform at 10MHz.

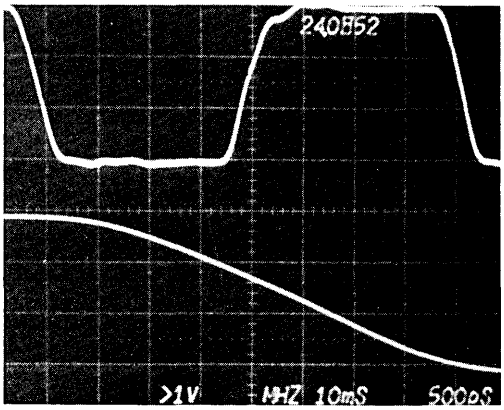


Figure 11. Output Waveform at 24MHz and Expanded Falling Edge Exhibiting <50ps Jitter.

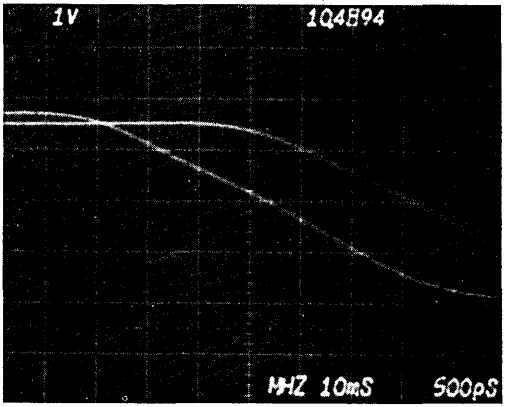


Figure 12. Change in Pulse Width and Jitter from 25°C to 125°C, f = 10MHz.

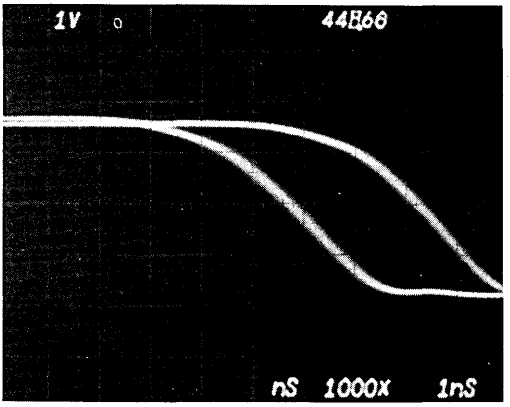


Figure 13. Expanded Fall Time Showing Change in Pulse Width from 25°C to 125°C, f = 1.0MHz, (Jitter ~ 300ps).

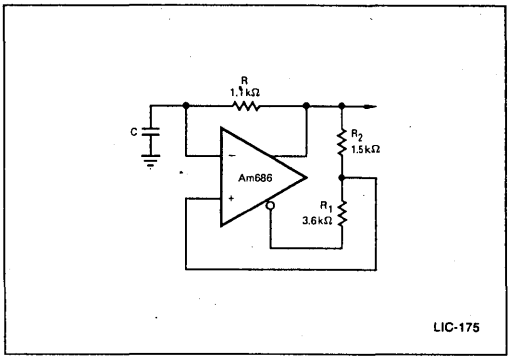


Figure 14. Circuit and Component Values used in Obtaining Performance Characteristics.

LOW LEVEL PULSE DETECTOR

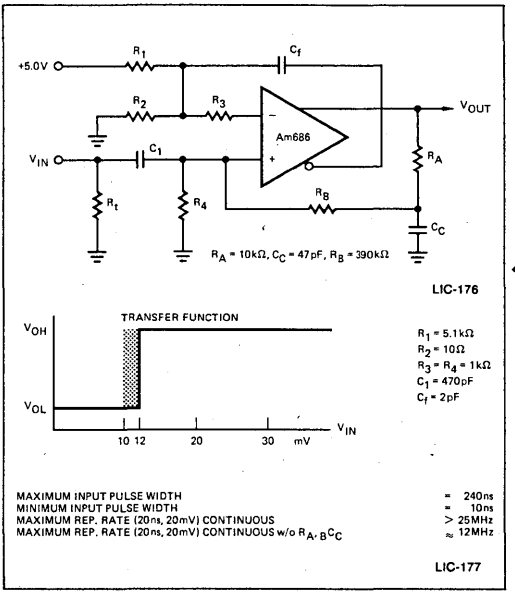


Figure 15.

CIRCUIT OPERATION

The input resistance is essentially determined by R_4 which was chosen to be 1kΩ on the basis that most sources would not be unduly loaded at this value and consequentially higher values would make the circuit excessively prone to oscillation. To minimize bias current errors, the inverting input is connected to the 10mV reference source (R_1 and R_2) through an equal-valued resistor (R_3).

Positive feedback is provided by C_f which provides a 50-60mV, 3-4ns pulse, significantly improving the switching time and narrowing the uncertainty region for pulses just in excess of the 10mV threshold.

Capacitor C_1 provides A-C coupling and thus isolates the circuit from slowly varying signals which may be superimposed on the signal to be detected. Such is the case for a detector sensing the output from a fibreoptic cable receiver. The A-C coupling imposes additional constraints; namely, the repetition rate and duty cycle of the input signal.

The signal which is seen by the non-inverting terminal and then compared to the reference is not simply the peak value of the input pulse but the peak value less the average D.C. value of the input signal.

Assuming a 20mV input pulse, 20ns wide and repeated every 20ns, the signal seen across R_4 will be as follows:

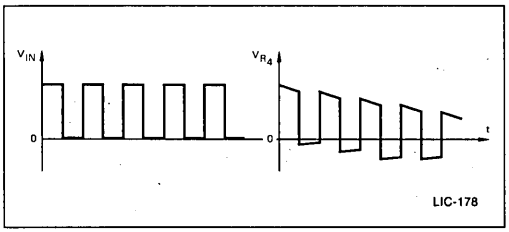


Figure 16.

By the ninth pulse, the peak signal will be 15.2mV dropping to 14.6mV by the end of the pulse; thus, after a pulse train of ~10 pulses, the detector will not detect the incoming signal.

Additionally, consider the case of a 20ns pulse repeated every 60 nanoseconds.

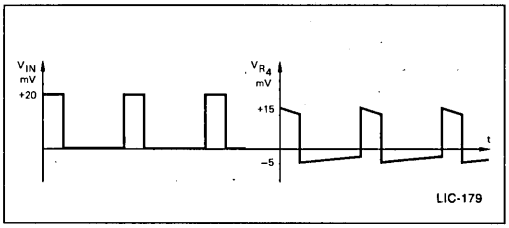


Figure 17.

The peak signal at the input will now be only 15mV; therefore, the maximum repetition rate consistent with providing a 5.0mV overdrive is 1/80ns or 12.5MHz.

Therefore, the circuit will only successfully detect 20mV, 20ns signals if: a) the pulse train is $\leqslant$ 10 pulses or b) the repetition rate $\leqslant$ 12MHz.

To compensate for these problems, a DC feedback signal is generated by R_A, R_B and C_C, which adjusts the reference level accordingly.

R_A and C_C form a low-pass filter that gives a maximum DC level of 1.7 volts at a 1:1 duty cycle. At this duty cycle, it is required to reduce the reference level by 5mV to maintain adequate overdrive. R_B and R_4 form an attenuator and the DC voltage level returned to the non-inverting input = 1.7V x $R_4/(R_4 + R_B)$ = 4.3mV. Using this network permits the circuit to work up to 25MHz, or better than a 1 : 1 duty cycle and removes the limitation imposed by the input A-C coupling.

Note: The response time of the feedback path must be the same as the input network; i.e., $R_AC_C = R_4C_1$ in order for the feedback to follow rapid changes in repetition rate or duty cycle.

PRECISION MONOSTABLE

Commercially available one-shots encounter problems in the generation of narrow (< 100ns) pulses. Namely, there is a significant delay between the input pulse and the output pulse of the order of 20ns and the resultant output pulse width is highly temperature dependent due to the variation in internal delays with temperature. Second, the input pulse must be of the logic level for the type of logic employed in the design — TTL, DTL, RTL, etc. Thus, the circuits are incapable of responding to low-level input signals in the millivolt range.

The Am685 series of sampling comparators can be employed in the design of a custom one-shot to overcome both of these problems.

Figure 18 shows the design of a monostable employing the Am686 to generate precision output pulses in the 20-100ns range and the values shown are for a 50ns pulse width.

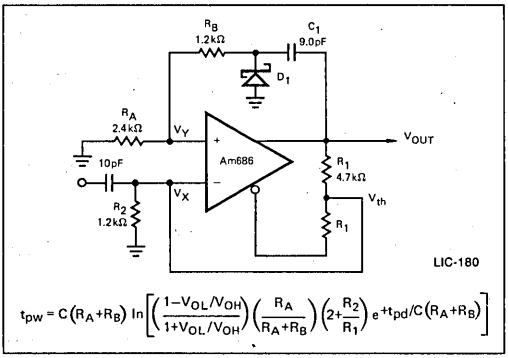


Figure 18.

The timing diagram illustrates the circuit operation.

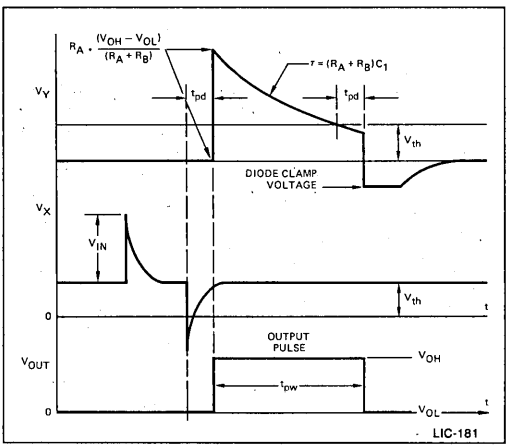


Figure 19.

The circuit triggers on the negative-going edge of the input pulse and the Q output switches high. The output signal is attenuated by R_A and R_B to keep the coupled pulse inside the common mode limits of the device. The output remains high until the voltage on the non-inverting input reaches the threshold set by R_1 and R_2. In order that the pulse width be independent of the input pulse amplitude, it is important to make the input time constant small compared to the desired output pulse width.

A unique feature of the circuit is the use of the differential outputs of the device to set the threshold, V_{th} thus providing temperature compensation and a reduction in pulse width variation from device to device.

Diode D_1 shortens the recovery time of the timing capacitor and permits retriggering 30ns after the end of the pulse with less than a 5% change in pulse width.

Complete isolation of the input signal and the timing network may be achieved by employing the latch function as shown below:

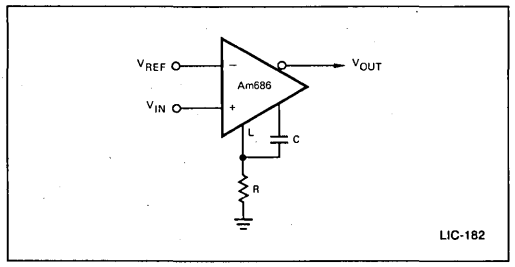


Figure 20.

When the input signal exceed V_{REF}, the output will switch and latch the comparator in the high state. When timing capacitor charges to the latch threshold, the latch will become disabled and the output will switch back to zero, providing the input is now below V_{REF}.

The advantages of this approach are:

1. No interaction between input signal and timing capacitor.
2. The input threshold set by V_{REF} is independent of the timing threshold.

Thus, the input threshold can be varied from millivolts to volts. A practical circuit is shown:

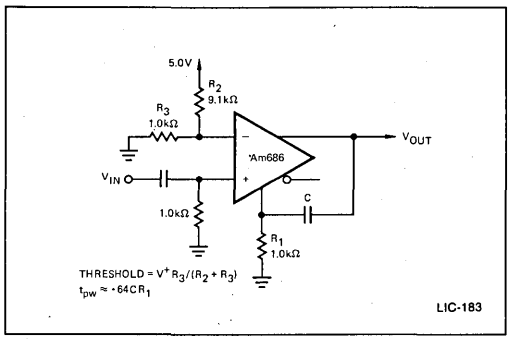


Figure 21.

The circuit is applicable for situations where accuracy of trigger threshold is important, a large variation in input signal level is expected or the input signal level is low. Timing accuracy (pulse width) is independent of the amplitude of the input pulse, but the output pulse width varies with temperature in accordance with the temperature dependence of the latch threshold (~ 3.0mV/°C for Am686).

APPLICATIONS REQUIRING INPUT HYSTERESIS

Comparators are frequently employed in systems where it is required that the transfer function contain a defined amount of hysteresis. Conventional comparators employing positive feedback can be used to generate hysteresis as shown below:

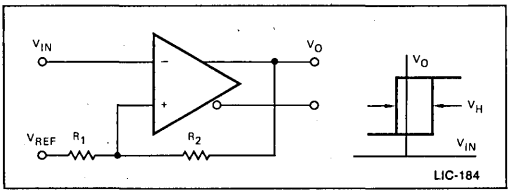


Figure 22.

Drawbacks of this technique include:

1. Response time of hysteresis loop ≥ comparator propagation delay.
2. Hysteresis varies with V_{OH} and V_{OL} changes.
3. Hysteresis is not centered about zero unless an additional reference is used.

By utilizing the latch function on the Am685, Am686 and Am687, hysteresis can be inserted in a manner to overcome these drawbacks; namely:

1. Response time of hysteresis loop << propagation delay.
2. Hysteresis not affected by V_{OH} and V_{OL} changes.
3. Hysteresis is symmetrical about zero.
4. Full input differential capability maintained over complete common mode range.

The hysteresis is obtained by applying a slight bias to the latch inputs. The technique is illustrated in the test circuit shown for the Am687.

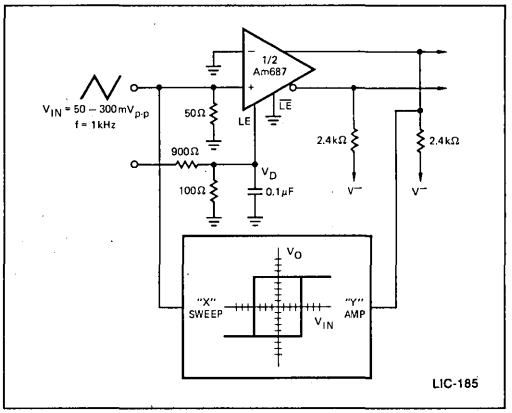


Figure 23.

The hysteresis is essentially symmetrical about zero and between ±5 and ±50mV of hysteresis can be generated before the relationship between the latch voltage and the thresholds become too sensitive.

The hysteresis is independent of changes in the positive supply voltage and the input common mode range and varies only with changes in temperature and negative supply voltage.

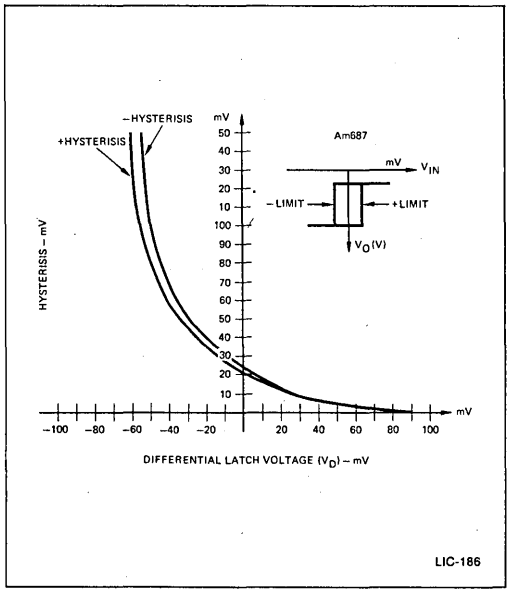


Figure 24. Input Hysteresis Versus Latch Voltage, T_A = 25°C.

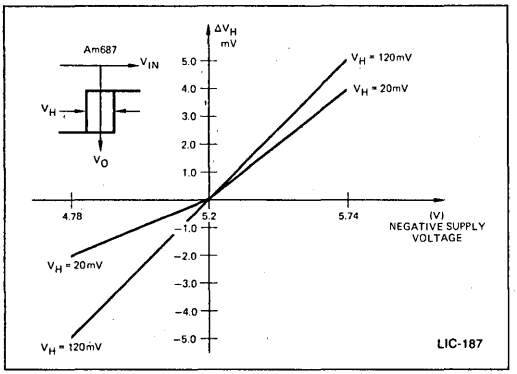


Figure 25. Change in Hysteresis Versus Change in Negative Supply Voltage.

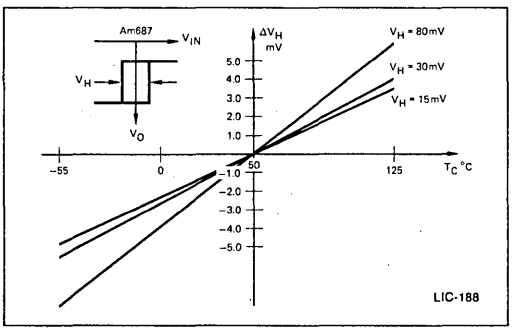
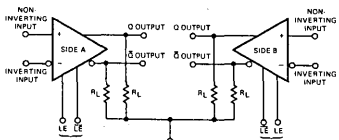


Figure 26. Change in Hysteresis Versus Case Temperature.

COMPARATOR PERFORMANCE SPECIFICATIONS

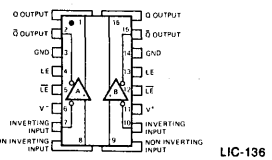
Am687

FUNCTIONAL DIAGRAM



The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to –2.0V, or 200–2000Ω connected to –5.2V.

CONNECTION DIAGRAM
Top View



Note 1. Pin 6 is connected to bottom of case.

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics Symbol	Parameter	Conditions (Note 3)	Am687A-L Am687-L Min.	Am687A-L Am687-L Max.	Am687A-M Am687-M Min.	Am687A-M Am687-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\Omega$, T_A = 25°C.	–3.0	+3.0	–2.0	+2.0	mV
		$R_S \leq 100\Omega$	–3.5	+3.5	–3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	–10	+10	–10	+10	µV/°C
I_{OS}	Input Offset Current	25°C ≤ T_A ≤ $T_{A(max.)}$	–1.0	+1.0	–1.0	+1.0	µA
		$T_A = T_{A(min.)}$	–1.3	+1.3	–1.6	+1.6	µA
I_B	Input Bias Current	25°C ≤ T_A ≤ $T_{A(max.)}$		10		10	µA
		$T_A = T_{A(min.)}$		13		16	µA
V_{CM}	Input Voltage Range		–3.3	+2.7	–3.3	+2.7	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\Omega$, –3.3 ≤ V_{CM} ≤ +2.7 V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\Omega$, ΔV_S = ±5%	70		70		dB
V_{OH}	Output HIGH Voltage	T_A = 25°C	–0.960	–0.810	–0.960	–0.810	V
		$T_A = T_{A(min.)}$	–1.060	–0.890	–1.100	–0.920	V
		$T_A = T_{A(max.)}$	–0.899	–0.700	–0.850	–0.620	V
V_{OL}	Output LOW Voltage	T_A = 25°C	–1.850	–1.650	–1.850	–1.650	V
		$T_A = T_{A(min.)}$	–1.890	–1.675	–1.910	–1.690	V
		$T_A = T_{A(max.)}$	–1.825	–1.625	–1.810	–1.575	V
I^+	Positive Supply Current			35		32	mA
I^-	Negative Supply Current			48		44	mA
P_{DISS}	Power Dissipation			485		450	mW

Switching Characteristics (V_{in} = 100mV, V_{od} = 5mV)

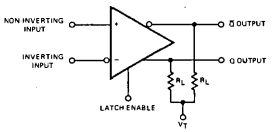
t_{pd+}, t_{pd-}	Propagation Delay, Am687A	$T_{A(min.)} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A(max.)}$		10		12.5	ns
t_{pd+}, t_{pd-}	Propagation Delay, Am687	$T_{A(min.)} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A(max.)}$		14		20	ns
t_s	Minimum Latch Set-up Time	T_A = 25°C		4.0		4.0	ns

Notes: 2. Derate at 9mW/°C for operation at ambient temperatures above +115°C.
3. Unless otherwise specified V^+ = +5.0V, V^- = –5.2V, V_T = –2.0V, and R_L = 50Ω; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am687 and Am687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

COMPARATOR PERFORMANCE SPECIFICATIONS (Cont.)

Am685

FUNCTIONAL DIAGRAM

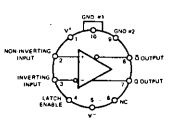


The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0 V, or 200–2000Ω connected to −5.2 V.

LIC-118

CONNECTION DIAGRAMS
Top Views

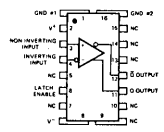
Metal Can



Note 1: On metal package, pin 5 is connected to case. On DIP, pin 8 is connected to case.

LIC-120

Dual-In-Line



LIC-121

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \le 100\,\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \le 100\,\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \le 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	µA
			−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \le 100\,\Omega$, $-3.3 \le V_{CM} \le +3.3$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \le 100\,\Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_A$(min.)	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_A$(max.)	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_A$(min.)	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_A$(max.)	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			22		22	mA
I^-	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

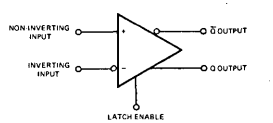
Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

t_{pd+}	Input to Output HIGH	T_A(min.) < T_A < 25°C	4.5	6.5	4.5	6.5	ns
		$T_A = T_A$(max.)	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	T_A(min.) < T_A < 25°C	4.5	6.5	4.5	6.5	ns
		$T_A = T_A$(max.)	5.0	9.5	5.5	12	ns
t_{pd+}(E)	Latch Enable to Output HIGH (Note 4)	T_A(min.) < T_A < 25°C	4.5	6.5	4.5	6.5	ns
		$T_A = T_A$(max.)	5.0	9.5	5.5	12	ns
t_{pd-}(E)	Latch Enable to Output LOW (Note 4)	T_A(min.) < T_A < 25°C	4.5	6.5	4.5	6.5	ns
		$T_A = T_A$(max.)	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	T_A(min.) < T_A < 25°C		3.0		3.0	ns
		$T_A = T_A$(max.)		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	T_A(min) < T_A < T_A(max.)		1.0		1.0	ns
t_{pw}(E)	Minimum Latch Enable Pulse Width (Note 4)	T_A(min.) < T_A < 25°C		3.0		3.0	ns
		$T_A = T_A$(max.)		4.0		5.0	ns

NOTES:
2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual-in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.
3: Unless otherwise specified $V^+ = 6.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

Am686

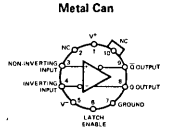
FUNCTIONAL DIAGRAM



LIC-189

CONNECTION DIAGRAMS
Top Views

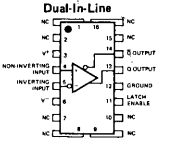
Metal Can



Note 1: On metal package, pin 5 is connected to case. On DIP, pin 6 is connected to case.

LIC-131

Dual-In-Line



LIC-132

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless Otherwise Specified)

Symbol	Parameter	Conditions (Note 3)	Am686-C	Am686-M	Units
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$, $T_A = 25°C$	3.0	2.0	mV MAX.
		$R_S \le 100\Omega$	3.5	3.0	mV MAX.
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \le 100\Omega$	10	10	µV/°C MAX.
I_{OS}	Input Offset Current	25°C < T_A < T_A (max.)	1.0	1.0	µA MAX.
		$T_A = T_A$ (min.)	1.3	1.6	µA MAX.
I_B	Input Bias Current	25°C < T_A < T_A (max.)	10	10	µA MAX.
		$T_A = T_A$ (min.)	13	16	µA MAX.
V_{CM}	Input Voltage Range		+2.7, −3.3	+2.7, −3.3	V MIN.
CMRR	Common Mode Rejection Ratio	$R_S \le 100\Omega$, $-3.3V \le V_{CM} \le +2.7V$	80	80	dB MIN.
SVRR	Supply Voltage Rejection Ratio	$R_S \le 100\Omega$	70	70	dB MIN.
V_{OH}	Output HIGH voltage	$I_L = -1.0$mA, $V_S = V_S$ (min.)	2.7	2.5	V MIN.
V_{OL}	Output LOW Voltage	$I_L = 10$mA, $V_S = V_S$ (max.)	0.5	0.5	V MAX.
I^+	Positive Supply Current		42	40	mA MAX.
I^-	Negative Supply Current		34	32	mA MAX.
P_{DISS}	Power Dissipation		415	400	mW MAX.

Switching Characteristics ($V^+ = +5.0$V, $V^- = -6.0$V, $V_{in} = 100$mV, $V_{od} = 5.0$mV, $C_L = 15$pF) (Note 4)

t_{pd+}	Propagation Delay, Input to Output HIGH	T_A (min.) < T_A < 25°C	12	12	ns MAX.
		$T_A = T_A$ (max.)	15	15	ns MAX.
t_{pd-}	Propagation Delay, Input to Output LOW	T_A (min.) < T_A < 25°C	12	12	ns MAX.
		$T_A = T_A$ (max.)	15	15	ns MAX.
Δt_{pd}	Difference in Propagation Delay between Outputs	$T_A = 25°C$	2.0	2.0	ns MAX.

Notes: 2. For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +95°C; for the dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above 115°C.
3. Unless otherwise specified, $V^+ = +5.0$V, $V^- = -6.0$V and the Latch Enable input is at V_{OL}. The switching characteristics are for a 100mV input step with 5.0mV overdrive.
4. The outputs of the Am686 are unstable when biased into their linear range. In order to prevent oscillation, the rate-of-change of the input signal as it passes through the threshold of the comparator must be at least 1V/µs. For slower input signals, a small amount of external positive feedback may be applied around the comparator to give a few millivolts of hysteresis.

6

Am1500

Dual Precision Voltage Comparator

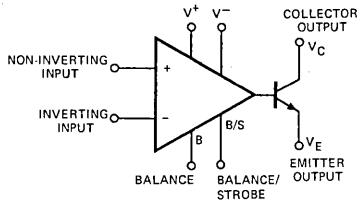
Distinctive Characteristics

- The Am1500 is functionally, electrically, and pin-for-pin equivalent to the National LH2111
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4.0mV max.
- Differential Input Voltage Range – ±30V
- Reduced size and weight

FUNCTIONAL DESCRIPTION

The Am1500 is a voltage comparator featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire-ORed.

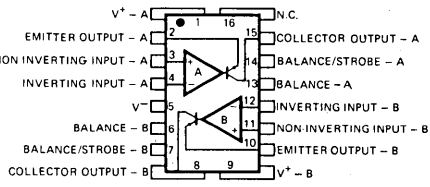
FUNCTIONAL DIAGRAM
(each half)



LIC-138

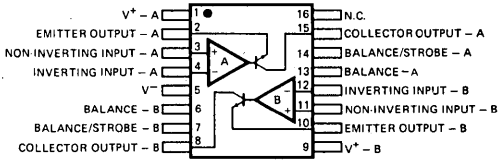
CONNECTION DIAGRAMS
Top Views

Hermetic Dual In-Line D-16-1



LIC-139

Flat Package F-16-1



LIC-140

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
Am1500C	Hermetic DIP	0 to +70°C	AM1500DC
	Flat Pak	0 to +70°C	AM1500FC
Am1500L	Hermetic DIP	−25 to +85°C	AM1500DL
	Flat Pak	−25 to +85°C	AM1500FL
Am1500M	Hermetic DIP	−55 to +125°C	AM1500DM
	Flat Pak	−55 to +125°C	AM1500FM

*Also available with burn-in processing. To order add suffix B to part number.

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
Am1500M, L	50V
Am1500C	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, −0V
Voltage from Inputs to V^+	−30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am1500M	−55°C to +125°C
Am1500L	−25°C to + 85°C
Am1500C	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS

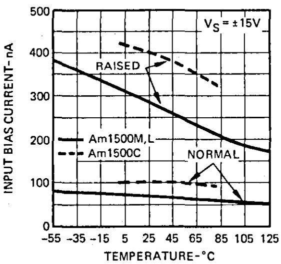
(T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am1500C Min.	Am1500C Typ.	Am1500C Max.	Am1500M Am1500L Min.	Am1500M Am1500L Typ.	Am1500M Am1500L Max.	Units
Input Offset Voltage (Note 3)			2.0	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500Ω to +5V, V_E = 0		200			200		ns
Supply Current—Positive (Note 5)			7.0	15.0		7.0	12.0	mA
—Negative (Note 5)			4.8	10.0		4.8	10.0	
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{in} \leq -5.0$mV, I_C = 50mA					0.75	1.5	V
	$V_{in} \leq -10$mV, I_C = 50mA		0.75	1.5				
Output Leakage Current	$V_{in} \geq +5.0$mV, V_C to V_E = 50V					0.2	10.0	nA
	$V_{in} \geq +10$mV, V_C to V_E = 40V		0.2	50.0				
The Following Specifications Apply Over The Operating Temperature Range								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{in} \leq -6.0$mV, I_C = 8.0mA					0.23	0.40	V
	$V_{in} \leq -10$mV, I_C = 8.0mA		0.23	0.40				
Output Leakage Current	$V_{in} \geq +6.0$mV, V_C to V_E = 50V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		V
Supply Current—Positive (Note 5)	T_A = +125°C					4.8	12.0	mA
—Negative (Note 5)						3.2	10.0	

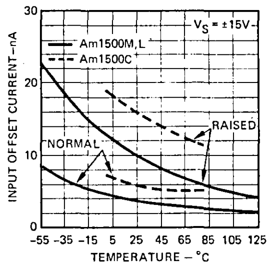
Notes:
1. For the Flat Package derate at 6.5mW/°C for operation at ambient temperatures above 83°C, and the Dual-In-Line at 9mW/°C for operation at ambient temperatures above 95°C.
2. Unless otherwise specified, these specifications apply for V^+ = +15V, V^- = −15V, V_E = −15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5.0mV overdrive.
5. The Am1500 supply current is the sum of the supply currents required by each side.

PERFORMANCE CURVES

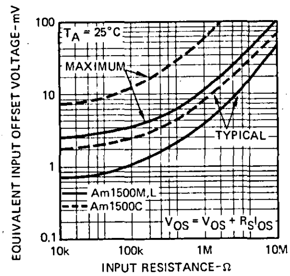
Input Bias Current



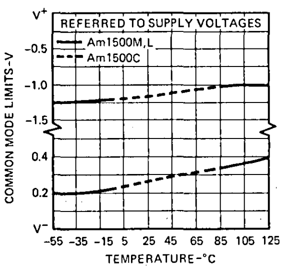
Input Offset Current



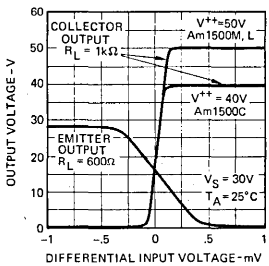
Offset Error



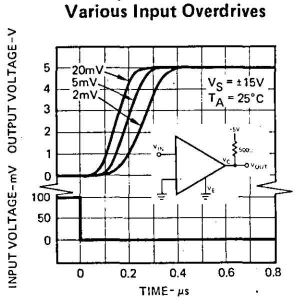
Common Mode Limits



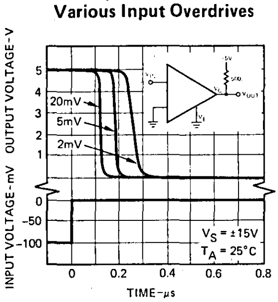
Transfer Function



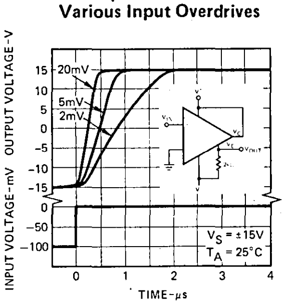
Response Time For Various Input Overdrives



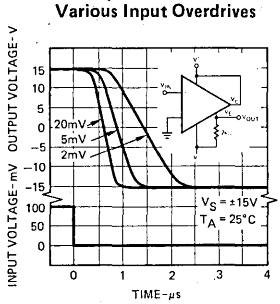
Response Time For Various Input Overdrives



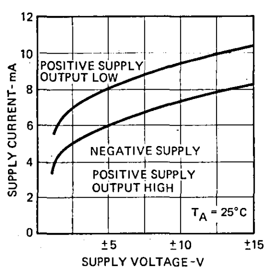
Response Time For Various Input Overdrives



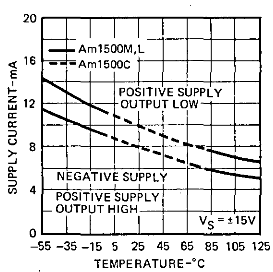
Response Time For Various Input Overdrives



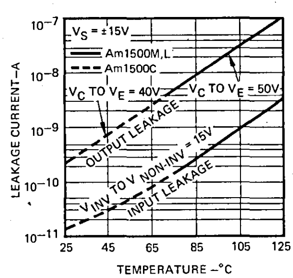
Supply Current



Supply Current



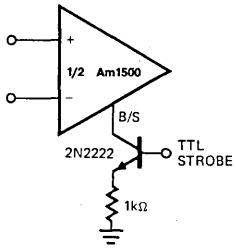
Leakage Current



LIC-141

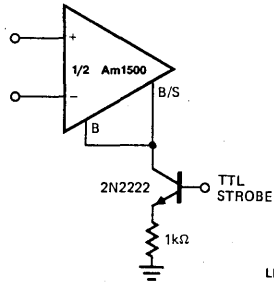
APPLICATIONS

Strobing



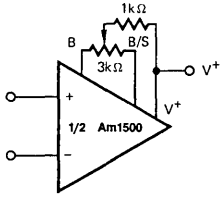
LIC-142

Strobing Off Both Input and Output Stages**



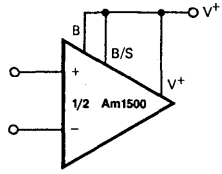
LIC-143

Offset Balancing



LIC-144

Increasing Input Stage Current*



LIC-145

*Increases input bias current and common-mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs storbed OFF.

6

LH2111/2211/2311

Dual Precision Voltage Comparator

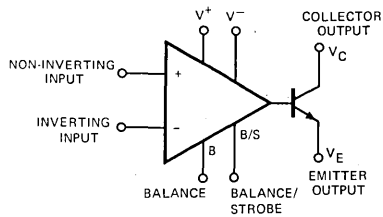
Distinctive Characteristics

- The LH2111/2211/2311 are functionally, electrically, and pin-for-pin equivalent to the National LH2111/2211/2311
- Output Drive – 50V and 50mA
- Input Bias Current – 150nA max.
- Input Offset Voltage – 4.0mV max.
- Differential Input Voltage – ±30V
- Reduced size and weight

FUNCTIONAL DESCRIPTION

The LH2111/2211/2311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire-ORed.

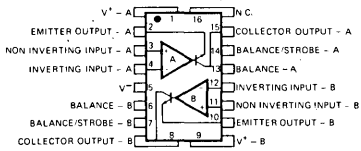
FUNCTIONAL DIAGRAM
(Each Half)



04173A-1

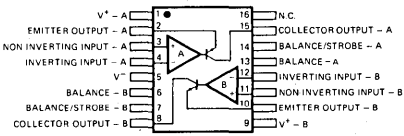
CONNECTION DIAGRAMS
Top Views

Hermetic Dual In-Line D-16-1



04173A-2

Flat Package F-16-1



04173A-3

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LH2311	Hermetic DIP	0 to +70°C	LH2311D
LH2311	Flat Pak	0 to +70°C	LH2311F
LH2211	Hermetic DIP	−25 to +85°C	LH2211D
LH2211	Flat Pak	−25 to +85°C	LH2211F
LH2111	Hermetic DIP	−55 to +125°C	LH2111D
LH2111	Flat Pak	−55 to +125°C	LH2111F

MAXIMUM RATINGS

Voltage from V^+ to V^-	36V
Voltage from Collector Output to V^-	
LH2111/LH2211	50V
LH2311	40V
Voltage from Emitter Output to V^-	30V
Voltage between Inputs	±30V
Voltage from Inputs to V^-	+30V, –0V
Voltage from Inputs to V^+	–30V
Power Dissipation (Note 1)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LH2111	–55°C to +125°C
LH2211	–25°C to +85°C
LH2311	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

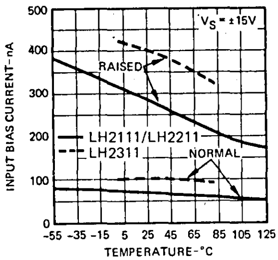
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	LH2311 Min.	LH2311 Typ.	LH2311 Max.	LH2111 LH2211 Min.	LH2111 LH2211 Typ.	LH2111 LH2211 Max.	Units
Input Offset Voltage (Note 3)			2	7.5		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100	nA
Response Time (Note 4)	R_L = 500Ω to +5V, V_E = 0		200			200		ns
Supply Current–Positive (Note 5)			7.0	15.0		7.0	12.0	mA
–Negative (Note 5)			4.8	10.0		4.8	10.0	
Voltage Gain			200			200		V/mV
Saturation Voltage	$V_{IN} \leq -5mV$, I_C = 50mA					0.75	1.5	V
	$V_{IN} \leq -10mV$, I_C = 50mA		0.75	1.5				
Output Leakage Current	$V_{IN} \geq +5mV$, V_C to V_E = 50V					0.2	10.0	nA
	$V_{IN} \geq +10mV$, V_C to V_E = 40V		0.2	50.0				
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage (Note 3)				10.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0	nA
Input Bias Current (Note 3)				300			150	nA
Saturation Voltage	$V_{IN} \leq -6mV$, I_C = 8mA					0.23	0.40	V
	$V_{IN} \leq -10mV$, I_C = 8mA		0.23	0.40				
Output Leakage Current	$V_{IN} \geq +6mV$, V_C to V_E = 50V					0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		V
Supply Current–Positive (Note 5)	T_A = 125°C					4.8	12.0	mA
–Negative (Note 5)						3.2	10.0	

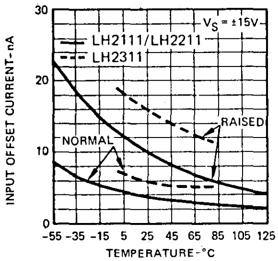
lotes:
1. For the Flat Package derate at 6.5 mW/°C for operation at ambient temperatures above 83°C, and the Dual-In-Line at 9 mW/°C for operation at ambient temperatures above 95°C.
2. Unless otherwise specified, these specifications apply for V^+ = 15V, V^- = –15V, V_E = –15V, and R_L at collector output = 7.5kΩ to +15V.
3. The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.
5. The LH2111 supply current is the sum of the supply currents required by each side.

PERFORMANCE CURVES

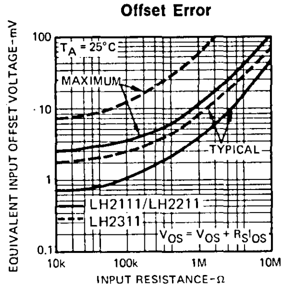
Input Bias Current



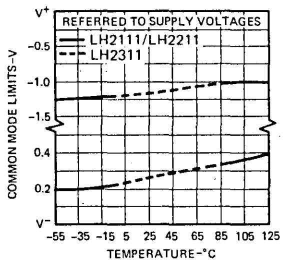
Input Offset Current



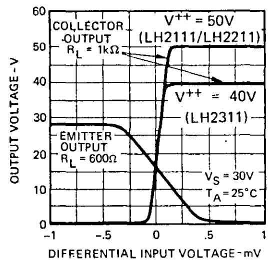
Offset Error



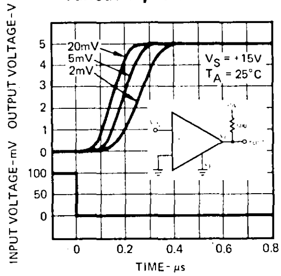
Common Mode Limits



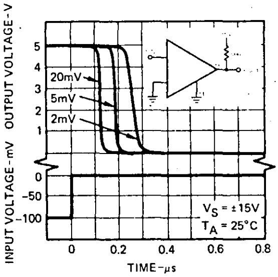
Transfer Function



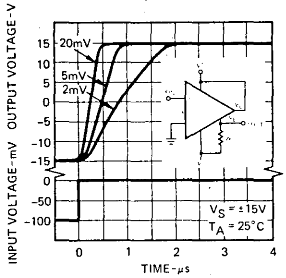
Response Time For Various Input Overdrives



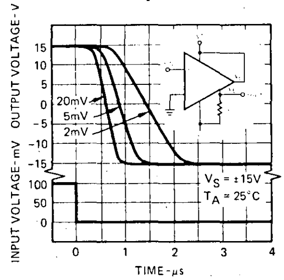
Response Time For Various Input Overdrives



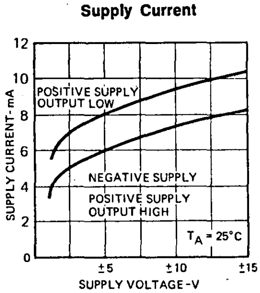
Response Time For Various Input Overdrives



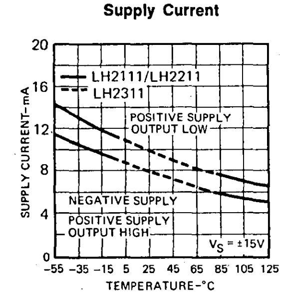
Response Time For Various Input Overdrives



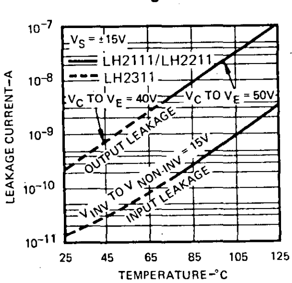
Supply Current



Supply Current



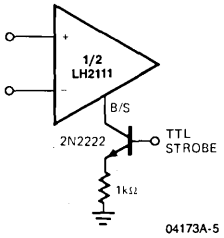
Leakage Current



04173A-4

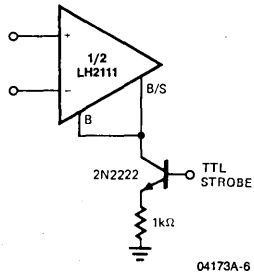
APPLICATIONS

Strobing



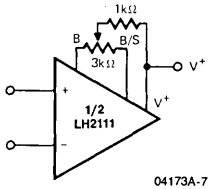
04173A-5

Strobing Off Both Input and Output Stages**



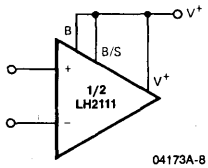
04173A-6

Offset Balancing



04173A-7

Increasing Input Stage Current*



04173A-8

*Increases input bias current and common-mode slew rate by a factor of 3.
**Typical input current = 50pA with inputs strobed OFF.

6

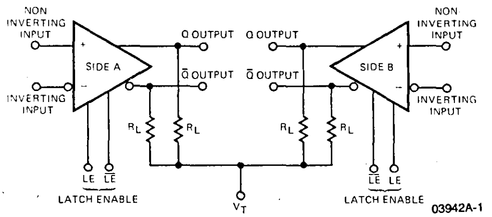
Am6685 • Am6687

Ultra Fast Voltage Comparators
Linear Integrated Circuits
PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- 2.5ns maximum propagation delay at 5mV overdrive
- Complementary ECL outputs
- 50Ω line driving capability
- 1ns latch setup time

FUNCTIONAL DIAGRAM (Am6687)



The outputs are open emitters; therefore external pull-down resistors are required. These resistors may be in the range of 50−200Ω connected to −2.0V, or 200−2000Ω connected to −5.2V.

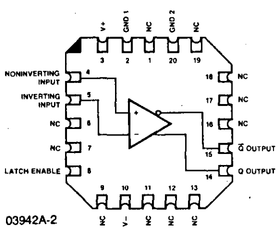
FUNCTIONAL DESCRIPTION

The Am6685/87 are ultra fast dual voltage comparators constructed on a single silicon chip with the advanced IMOX™ process. The circuits feature very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

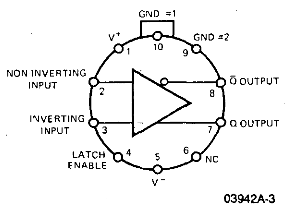
The Am6685 is a single comparator, with V+ specified at +6V, while the Am6687 is a dual comparator, with V+ specified at +5V. Separate latch functions are provided to allow each comparator to be independently used in a sample-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and LĒ is LOW, the comparator functions normally. When LE is driven LOW and LĒ is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, LE must be connected to ground.

Am6685 CONNECTION DIAGRAMS

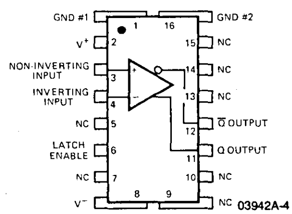
L-20-1



H-10-1



D-16-1



Note 1. On metal package, pin 5 is connected to case.
On DIP, pin 8 is connected to case.

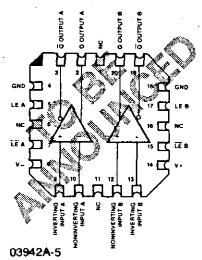
ORDERING INFORMATION*

Order Number Single	Dual	Package Type	Temperature Range
Am6685HM		Metal Can	−55 to +125°C
Am6685DM	Am6687DM	Hermetic DIP	−55 to +125°C
Am6685LM	Am6687LM	Leadless**	−55 to +125°C
Am6685XM	Am6687XM	Dice	−55 to +125°C
Am6685HL		Metal Can	−30 to +85°C
Am6685DL	Am6687DL	Hermetic DIP	−30 to +85°C
Am6685LL	Am6687LL	Leadless**	−30 to +85°C
Am6685XL	Am6687XL	Dice	−30 to +85°C

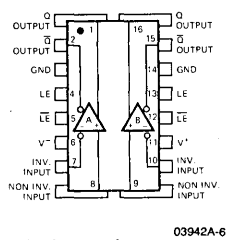
*Also available with burn-in processing. To order, add suffix B to the part number.
**Availability of Leadless packages will be announced.

Am6687 CONNECTION DIAGRAMS – Top Views

L-20-1



D-16-1



Note 1. Pin 6 is connected to bottom of case.

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03942A-ANA

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage		−7V
Negative Supply Voltage		−7V
Input Voltage		±4V
Differential Input Voltage		±6V
Output Current		30mA
Power Dissipation (Note 2)	6685	500mW
	6687	600mW
Operating Temperature Range	Military	−55 to +125°C
	Industrial	−30 to +85°C
Storage Temperature Range		−65 to +150°C
Lead Temperature (Soldering, 60 Sec.)		300°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (T_A = 25°C)

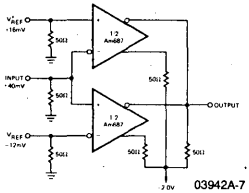
Parameters	Description		Test Conditions (Notes 2, 3)	Typ	Units
V_{OS}	Input Offset Voltage		$R_S \leq 100\Omega$	±0.5	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		$R_S \leq 100\Omega$	3	μV/°C
I_{OS}	Input Offset Current			2	μA
I_B	Input Bias Current			15	μA
V_{CM}	Input Voltage Range			±3.0	V
R_{IN}	Input Resistance			6	kΩ
C_{IN}	Input Capacitance			2	pF
V_{OH}	Output HIGH Voltage			−0.9	V
V_{OL}	Output LOW Voltage			−1.75	V
I^+	Positive Supply Current	6685		15	mA
		6687		30	
I^-	Negative Supply Current	6685		15	mA
		6687		30	
P_d	Power Dissipation	6685		180	mW
		6687		360	

SWITCHING CHARACTERISTICS (V_{IN} = 100mV, V_{OD} = 5mV)

Parameters	Description	Test Conditions (Notes 2, 3)	Typ	Units
t_{pd+}, t_{pd-}	Propagation Delay		2.5	ns
t_h	Minimum Latch Hold Time		1.0	ns
t_s	Minimum Latch Setup Time		1.0	ns
$t_{pd+}(E)$, $t_{pd-}(E)$	Latch Enable to Output HIGH or LOW		2.5	ns
$t_{PW}(E)$	Latch Enable Pulse Width		2.0	ns

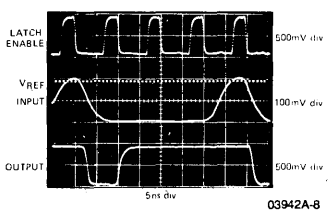
Notes: 2. Derate Dual In-line at 9mW/°C for operation at ambient temperatures above +115°C; metal can, 6.8mW/°C above +95°C.
3. Unless otherwise specified V^+ = +6V for 6685, or +5V for 6687, V^- = −5.2V, V_T = −2.0V, and R_L = 50Ω; all switching characteristics are for a 100mV input step with 5mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. These devices are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

High-Speed Window Detector



03942A-7

TYPICAL APPLICATION (T_A = 25°C)



03942A-8

6

Power Supply Controllers – Section VII

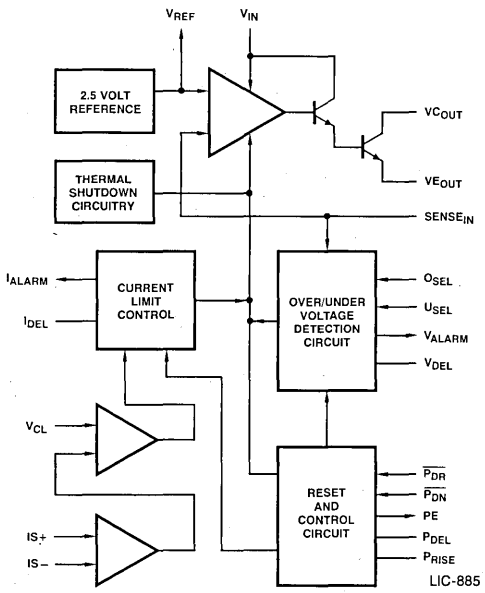
Am6300

Power Control Subsystem

DISTINCTIVE CHARACTERISTICS

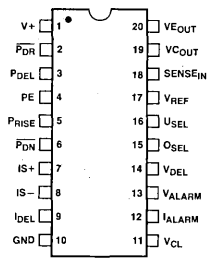
- 2.5V ±0.25% temperature compensated reference
- Versatile 100mA output for driving external NPN or PNP power transistors
- Thermal shutdown
- Logic control power up enable
- Programmable delay and rise time for power supply
- ±5% or ±10% over/under voltage detection/protection
- Programmable current limit detection/protection
- Programmable delays for the over/under voltage and current shutdown circuits
- Status outputs for fault conditions

BLOCK DIAGRAM



LIC-885

CONNECTION DIAGRAM – Top View
D-20-1, P-20-1



Pin 1 is marked for orientation.

LIC-886

GENERAL DESCRIPTION

The Am6300 Power Control Subsystem consists of a regulator section, an over/under voltage detection section, a current limit section and a reset and control section.

The regulator section contains a complete series pass voltage regulator with thermal shutdown, which uses external resistors to set the output voltage. Both the collector and emitter of the regulator output transistor are available to the user for flexibility in driving external power devices. The regulator also contains a precision, trimmed 2.5 volt reference which is capable of supplying 5mA of current for external purposes in addition to controlling the regulator and generating over and under voltage references.

The over/under voltage section compares the voltage at the sense input of the regulator to the internal reference and determines if the difference exceeds the user programmed limits, ±5% or ±10%. If one of the limits is exceeded for a period longer than the user programmed delay, the regulator shuts down and the voltage alarm output is activated. The regulator is reset by activating the power down inputs or removing power from the device.

The current limit section detects overload current by means of an external sense resistor in series with V_{IN}, GND, or the output of the regulator. The user programs the threshold of this detection circuit with external resistors. The regulator shuts down if a current overload is detected for a period longer than a user programmed delay and the current alarm is activated. The regulator is reset by activating the power down inputs or removing power from the device.

The reset and control section provides to the user, the ability to turn the regulator on and off by logic control. The start up of the regulator is delayed by a user programmed interval after the power up signal is received. After this delay the regulator output ramps up at a rate which is also determined by the user. When the output voltage levels off at the preset value, the over/under voltage and current limit circuits are activated and a power up output is activated which can be used to signal to the user that the supply is operating or enable other circuits.

The Am6300 allows the user a great deal of flexibility in power supply configuration and control. It can be operated locally or remotely in a stand alone configuration or with external power transistors to increase the output current. The Am6300 can be cascaded with other Am6300s for a sequenced supply application.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55 to +125°C	AM6300DM*
Hermetic DIP	0 to +70°C	AM6300DC*
Plastic DIP	0 to +70°C	AM6300PC

*Also available with burn-in processing. To order add suffix B to part number.

7

00096C-ANA

MAXIMUM RATINGS

Pulse Voltage at V+ (50ms)	50V	Input Voltage (all pins)	Gnd to V_{In}
Continuous Voltage at V_{In}	40V	Maximum Output Current	100mA
Input-Output Voltage Differential	37.5V	Internal Power Dissipation	1000mW (Note 1)

ELECTRICAL CHARACTERISTICS (Note 2)

Parameters	Description	Test Conditions		Min	Typ	Max	Units
Voltage Regulator							
	Output Error (Note 3)			−1.0		+1.0	$\%V_{OUT}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 12V to 40V	T_A = 25°C		.02	.2	$\%V_{OUT}$
$\Delta V_{OUT}/\Delta I_L$	Load Regulation	I_L = 1mA to 50mA	T_A = 25°C		.03	.15	$\%V_{OUT}$
	Ripple Rejection	f = 1KHz	T_A = 25°C	74	86		dB
I_{BIAS}	Sense Input Bias Current				2	4	μA
V_{IN}	Input Operating Range			5		40	Volts
V_{OUT}	Output Operating Range			2.5		37.5	Volts
V_{IN}-V_{OUT}	Input-Output Differential			2.5		37.5	Volts
I_S	Supply Current	V_{IN} = 40V			5	10	mA
Voltage Reference							
V_{REF}	Reference Voltage	T_A = 25°C		2.480	2.5	2.520	Volts
$\Delta V_{REF}/\Delta V_{IN}$	Line Regulation	V_{IN} = 12 to 40V				.1	$\%V_{REF}$
$\Delta V_{REF}/\Delta I_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA			.15	.30	$\%V_{REF}$
$\Delta V_{REF}/\Delta T_A$	Temperature Stability	0 to 70°C			30		ppm/°C
		−55 to +125°C			25		
I_{SC}	Short Circuit Current	V_{REF} = 0V		10	30	60	mA
Current Overload Circuit							
V_{IS}(diff)/V_{CL}	Trip Point Ratio			.4	.5	.6	V/V
V_{CL}	Trip Point Input Range			0		.4	Volts
V_{IS}(diff)	Sense Voltage Input Range			0		.2	Volts
CMVR	Sense Input Common Mode Range			0		V_{IN}	Volts
I_{BIAS}	Input Bias Current (IS+, IS−)	V_{IS} = 0V to +2V			−8	−20	μA
		V_{IS} = +2V to V_{IN}			+8	+20	
I_{OS}	Input Offset Current (IS+, IS−)				±1	±5	μA
I_{BIAS}	Input Bias Current (V_{CL})				−.25	−1.0	μA
Voltage Protection Circuit							
	+5% Error Trip Point	O_{SEL} = 5V		4.0	5	6.0	$\%V_{OUT}$
	−5% Error Trip Point	U_{SEL} = 5V		−4.0	−5	6.0	$\%V_{OUT}$
	+10% Error Trip Point	O_{SEL} = 0V		8	10	12	$\%V_{OUT}$
	−10% Error Trip Point	U_{SEL} = 0V		−8	−10	−12	$\%V_{OUT}$
Digital Characteristics (Note 4)							
V_{IH}	Input High Level			2.0		V_{IN}	Volts
V_{IL}	Input Low Level			0		.8	Volts
V_{OL}	Open Collector Output Voltage	I_{OL} = 5mA				.4	Volts
		I_{OL} = 15mA				1.5	

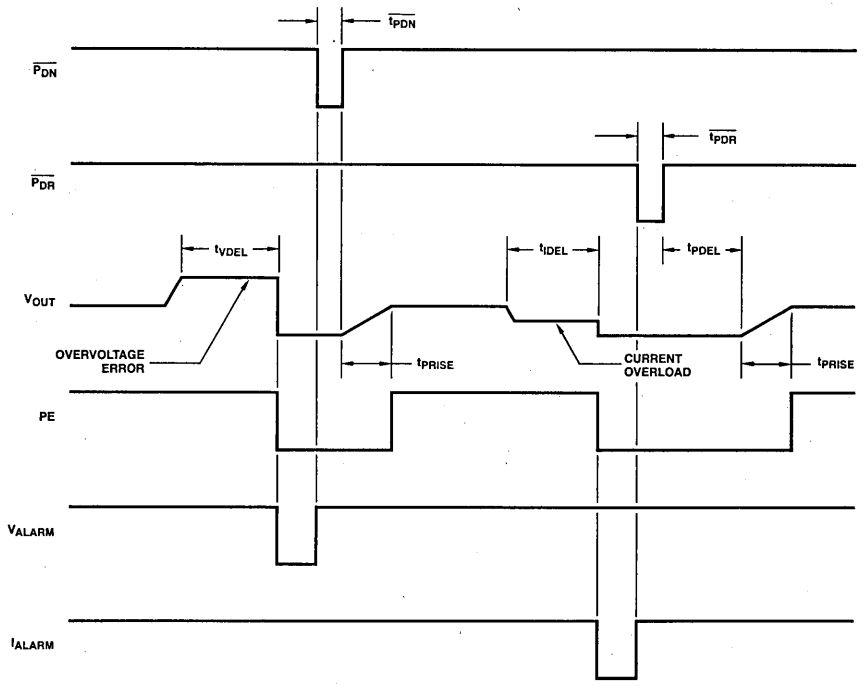
Notes:
1. Power dissipation ratings apply for T_A = 25°C. Derate linearly at 8mW/°C above 25°C for commercial parts and above 50°C for military parts.
2. All specifications are for V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1mA, I_{REF} = 1mA and over the operating temperature range unless otherwise specified.
3. Includes all errors associated with on-chip reference source and temperature effects.
4. Digital Inputs are $\overline{PDN}$, $\overline{PDR}$, OSEL, USEL
   Digital Outputs are V_{ALARM}, I_{ALARM}, $\overline{PE}$.

TIMING CHARACTERISTICS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{IDEL}, t_{VDEL}	Current Overload and Voltage Error Power Down Delays	Without external cap		1.2		μs
		With external cap, additional delay		.22		μs/pF
t_{PDEL}	Power Up Delay (Note 5)	Without external cap		1.2		μs
		With external cap, additional delay		.22		μs/pF
t_{PRISE}	Power Up Rise Time (Note 5)	Without external cap		1.5		μs
		With external cap		.22		μs/pF
t_{PDN}, t_{PDR}	Power Down Reset Pulse Width		10			μs

Note: 5. It is necessary to make the total time $t_{PDEL} + t_{PRISE}$ greater than the rise time of the supply to the Am6300 to insure proper power up.

TIMING WAVEFORMS



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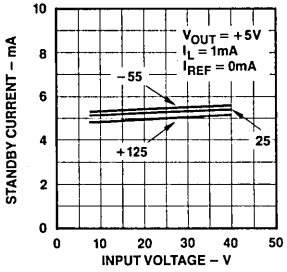
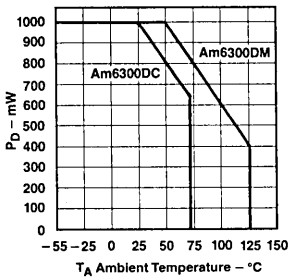
PERFORMANCE CURVES

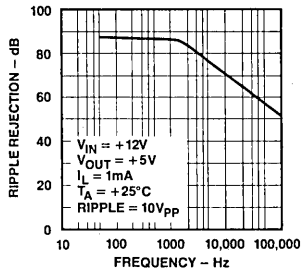
Standby Current Drain As a Function of Input Voltage



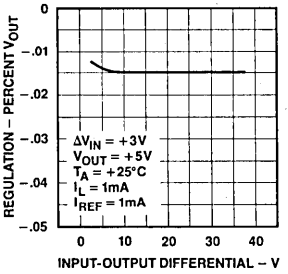
Maximum Power Dissipation As A Function of Ambient Temperature



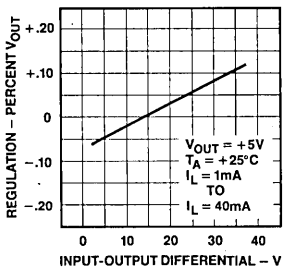
Ripple Rejection



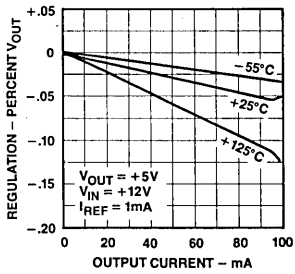
Regulator Line Regulation As a Function of Input-Output Differential



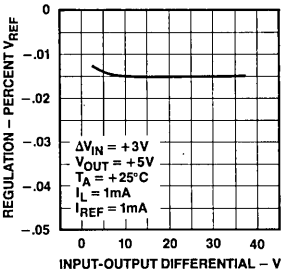
Regulator Load Regulation As a Function of Input-Output Differential



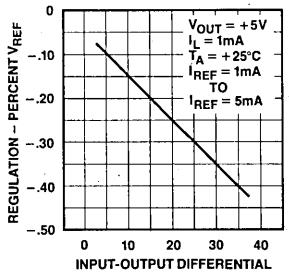
Load Regulation Characteristics



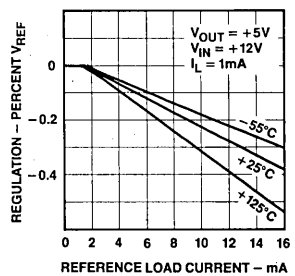
Reference Line Regulation As a Function of Input-Output Differential



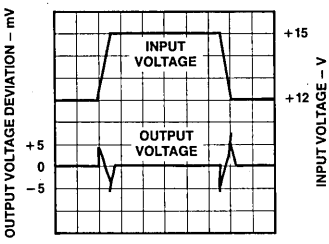
Reference Load Regulation As a Function of Input-Output Differential



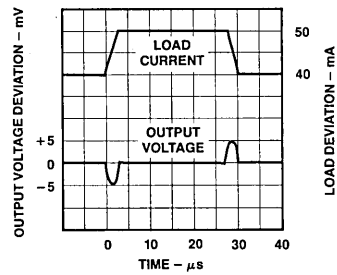
Reference Load Regulation As a Function of Load Current



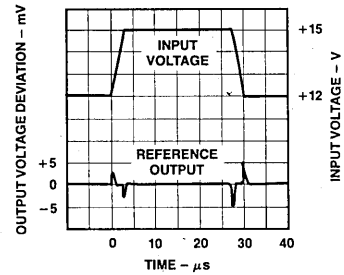
Regulator Line Transient Response



Regulator Load Transient Response



Reference Line Transient Response



Am6300 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
V_{REF}	Reference Voltage Output – The output of the internal, precision, 2.5 volt reference.
VE_{OUT}	Output Transistor Emitter – The emitter of the regulator output transistor.
VC_{OUT}	Output Transistor Collector – The collectors of the regulator output transistor.
$SENSE_{IN}$	Voltage Sense Input – A divided down portion of the output voltage is fed back into the regulator through this pin. The regulator adjusts the output so that this value equals the internal reference voltage, 2.5 volts. This voltage is also used in the over/under voltage detection circuit.
O_{SEL}	Over Voltage Limit Select – This input selects the over voltage limit. A logic 1 selects a +5% limit and a logic 0 selects a +10% limit.
U_{SEL}	Under Voltage Limit Select – This input selects the under voltage limit. A logic 1 selects a −5% limit and a logic 0 selects a −10% limit.
V_{CL}	Current Limit Voltage Input – This input is used to set the differential threshold of the current limit detection circuit. The threshold will be equal to half of the voltage on this pin.
IS+, IS–	Positive and Negative Current Sense Inputs – The differential voltage across the current sense resistor is applied to these inputs and compared to the current limit threshold.
I_{DEL}	Current Limit Delay Control – The delay time during which the current limit can be exceeded without shutting down the regulator is proportional to the value of a capacitor placed between this pin and ground.
V_{DEL}	Voltage Limit Delay Control – The delay during which an over or under voltage limit can be exceeded without shutting down the regulator is proportional to the value of a capacitor placed between this pin and ground.
V_{ALARM}	Voltage Limit Alarm – This open collector output goes low when the regulator shuts down due to an over or under voltage limit being exceeded. The V_{ALARM} output is reset by taking the $\overline{P_{DR}}$ or $\overline{P_{DN}}$ input low or by removing power from the Am6300.
I_{ALARM}	Current Limit Alarm – This open collector output goes low when the regulator shuts down due to the current limit being exceeded. The I_{ALARM} output is reset by taking the $\overline{P_{DR}}$ or $\overline{P_{DN}}$ input low or by removing power from the Am6300.
$\overline{P_{DR}}$	Power Down Reset (With Delay) – An active low input on this pin shuts the regulator down and resets the voltage and current alarms. When this input is taken high again the regulator begins to power up after a user programmed delay.
$\overline{P_{DN}}$	Power Down Reset (Without Delay) – An active low input on this pin shuts the regulator down and resets the voltage and current alarms. When this input is taken high again the regulator begins to power up with no delay.
P_{DEL}	Power Up Delay Control – A capacitor between this pin and ground sets the delay which occurs after $\overline{P_{DR}}$ is taken high and before the regulator begins to power up. The delay time is proportional to the capacitor value.
P_{RISE}	Power Up Rise Time Control – A capacitor connected between this pin and ground controls the rate at which the regulator output rises after the regulator has been enabled. The rise time is proportional to the value of the capacitor.
PE	Power Up Enable – This open collector output goes high when the regulator output voltage has reached its full value. It can be used as a signal to the user that the regulator is operating or to enable other devices.

APPLICATION HINTS

Figure 1 shows the Am6300 configured as a stand-alone, low current regulator. The output voltage is determined by the value of R_1. Various output voltages and corresponding values of R_1 for a fixed output voltage regulator are shown in Table 1.

If it is desired to be able to adjust the regulator output slightly to compensate for the resistor tolerances, R_1 and R_2 may be replaced with the circuit shown in Figure 2. Table 1 also contains values of R_1 for an adjustable output regulator. The values shown will allow approximately ±10% adjustment of the regulator output.

Also shown in Table 1 are minimum values of V_{IN} which will provide the minimum required input to output differential at each output voltage specified. Additionally the maximum value of V_{IN} which will meet the maximum power dissipation requirements is shown in Table 1, for I_{limit} set to 50mA at 25°C.

Should the user desire to set up his own unique output voltage the following equation is used to determine the ratio of R_1 to R_2:

$$\frac{R_1}{R_2} = \frac{(V_{OUT} - 2.5)}{2.5}$$

The values of R_1 and R_2 should be large enough to minimize the load on the regulator output, but sufficiently small to minimize the effects of the bias current to the $SENSE_{IN}$ input. In Figure 1 this current is 1mA which is only 2% of the output current and 500 times greater than the $SENSE_{IN}$ bias current.

The over/under voltage detection circuit of the Am6300 shown in Figure 1 has been set to detect voltage excursions of ±10% of V_{OUT} by connecting the O_{SEL} and U_{SEL} inputs to ground. The voltage detection limits may be reduced to 5% by connecting either or both of these inputs to V_{IN} through a 5kΩ resistor.

The current overload detection limit has been set to 50mA in Figure 1. The limit is set by the values of R_3 and R_4 and is detected by R_S. R_3 and R_4 divide down the 2.5 volt reference and the result is applied to the V_{CL} input. The current limit is detected when the differential across R_S exceeds the voltage at V_{CL} divided by two. The following equation is useful for calculating the ratio of R_3 to R_4,

$$\frac{R_3}{R_4} = \frac{2.5}{2(I_{LIMIT})(R_S)} - 1$$

The value of R_S should be selected so that the product of R_S and I_{LIMIT} is less than or equal to 0.2 volts.

APPLICATION HINTS (Cont.)

The delays associated with the over/under voltage detection, the current overload detection and the power up circuitry have been set with four external capacitors in Figure 1. The 0.1μF capacitors produce approximately 20ms of delay in each function.

Figure 1 also shows the use of LEDs for indicators on the alarm outputs of the Am6300. The values of the current limit resistors, R_{CL}, is determined by the value of V_{IN} selected by the user to supply the proper operating current to the LEDs.

The Am6300 can also be used in high current applications by adding external pass transistors. Figures 3 and 4 show configurations using external NPN and PNP pass transistors. The values of R_1 shown in Table 1 may be used for both fixed and adjustable configurations. The current overload detection limit has been set to 2 amps for both Figure 3 and 4 configurations.

Figure 5 shows the Am6300 configured as a programmable voltage regulator interfaced with a microcomputer system. The Am6080 is a microprocessor compatible DAC which will sink from 0 to 2mA of current depending on the eight bits of data which are latched internally. This current results in a voltage drop through the 10kΩ resistor. Since the regulator maintains the $SENSE_{IN}$ input at 2.5 volts, the regulator output will always be equal to 2.5 volts plus the voltage drop across the 10kΩ resistor. Thus the regulator output is digitally adjustable from 2.5 to 22.5 volts.

The digital inputs to the Am6300 are controlled by the outputs of a 4-bit latch from the processor data bus. This gives the processor full control of the power up/down function and the over/under voltage detection limits. The processor can also check the status of the three alarm outputs of the Am6300 through a 3-state buffer. Since the alarms are open collector outputs, they require 5kΩ pull-up resistors to the +5 volt supply.

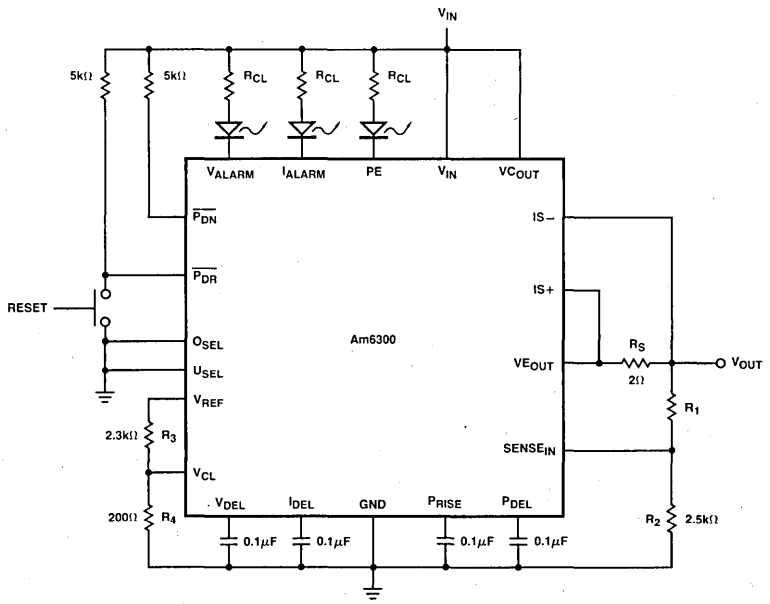


Figure 1. Am6300 Low Current Configuration (I_{LIMIT} = 50mA)

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TABLE 1. COMMON OUTPUT VOLTAGES

V_{OUT} (Volts)	V_{IN} (Max) (Volts)	V_{IN} (Min) (Volts)	R_I (Fixed) kΩ	R_I (Adj) kΩ
2.5	22.5	5	0	NA
5	25	7.5	2.5	2.3
6	26	8.5	3.5	3.3
10	30	12.5	7.5	7.3
12	32	14.5	9.5	9.3
15	35	17.5	12.5	12
20	40	22.5	17.5	17
24	40	26.5	21.5	21
28	40	30.5	25.5	25
30	40	32.5	27.5	27

V_{IN}(MAX) is the max supply voltage which will still meet max internal power dissipation at 25°C with I_{MAX} = 50mA.

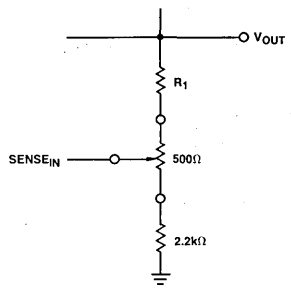

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Figure 2. Am6300 Output Adjustment Circuit

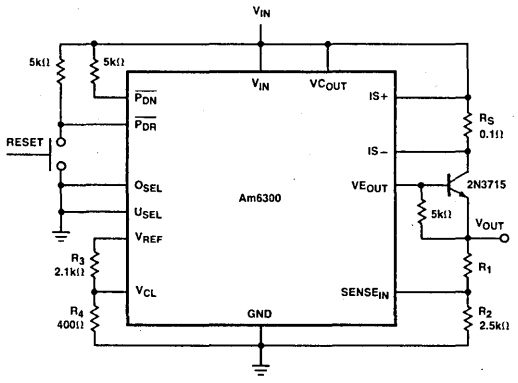


Figure 3. Am6300 High Current Configuration External NPN Pass Transistor

LIC-890

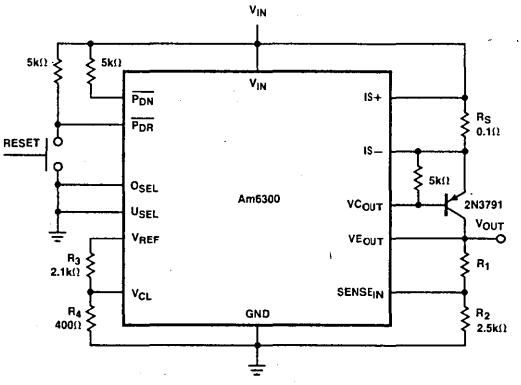
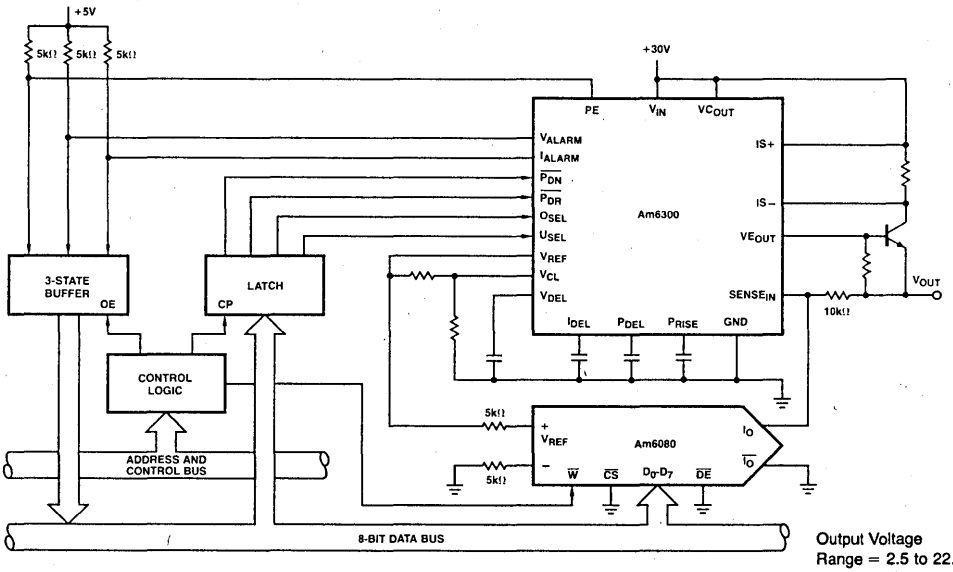


Figure 4. Am6300 High Current Configuration External PNP Pass Transistor

LIC-891



Output Voltage
Range = 2.5 to 22.5 Volts
Resolution ≈ 78.5mV/Step

Figure 5. Am6300 Programmable Voltage Regulator

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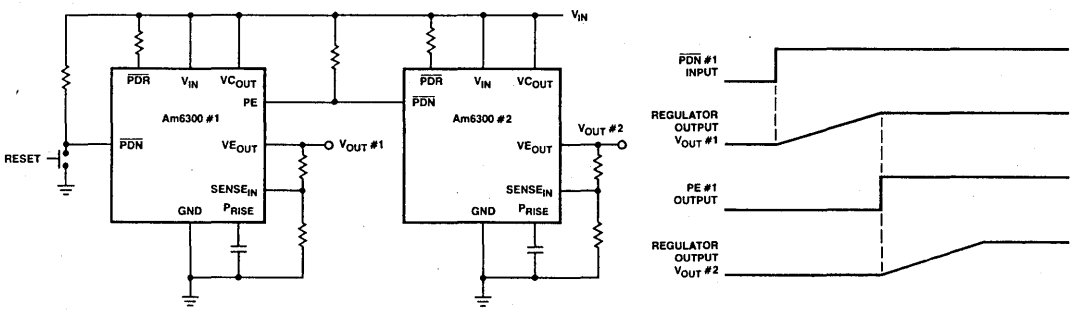
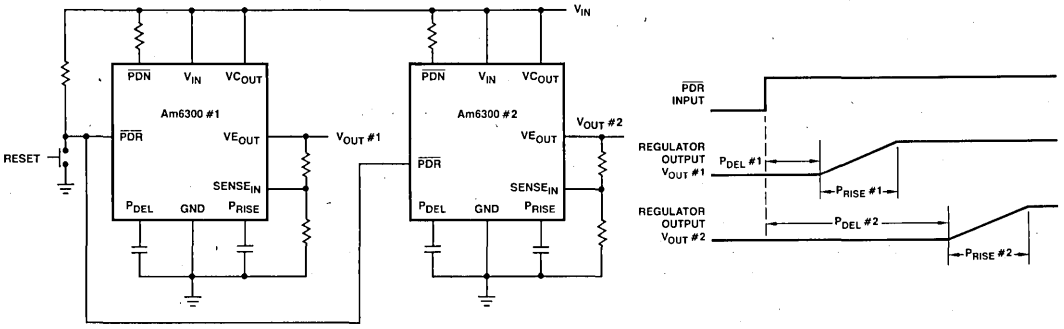
The Am6300 Sequenced Supplies (Using PE Output)



The Am6300 Sequenced Supplies (Using P_{DEL})



Power Supply Control Subsystem

By Brian Gillings and Charles Miller
Advanced Micro Devices

INTRODUCTION

Since the introduction of the monolithic regulator in the mid 1960's, numerous integrated circuits have been introduced to control the voltage regulation of both linear and switching power supply systems. The most recent introductions have combined a high degree of performance with an additional monitoring function.

The Am6300 includes not only the regulator section, but over/under voltage detection, current limit and power control sections, as well. Also included on-chip is a precision 2.5 volt reference, user defined turn-on delay, settable dV/dt during turn on, over/under voltage sensing delay and current limit sensing delay. All of these functions allow the user a great deal of flexibility in power supply configurations and control. The supply can be operated locally or remotely, in a stand-alone configuration or with external power transistors to increase the output current. The Am6300 can be cascaded with other Am6300s for sequenced supply applications. The device also includes internal thermal shutdown to keep the device from overheating.

As systems contain more MSI, LSI and VLSI devices, the power supply and regulator sections take up more of the system's volume. The introduction of regulator ICs, such as the μA723, have provided a high degree of performance, with added benefits of increased reliability and cost savings but they have only addressed the basic function of maintaining a constant output voltage. Most power supply systems also require circuitry for monitoring the performance and protecting the system in the event of fault conditions.

Advanced Micro Devices' objectives were to provide a regulator, similar to the industry standard μA723, which would also include the output monitoring and controlling functions. Figure 1 shows the block diagram of the Am6300. This circuit contains the four basic elements of supply regulators, a reference source, an error detector, a control device, and protection circuitry. Additionally, the Am6300 contains user defined limits for over/under voltage sensing and current limiting. Also included are provisions for controlling the turn on delay and rate of change of output, and programming the sensing circuits for a minimum time duration of fault before triggering the shut down of the regulator.

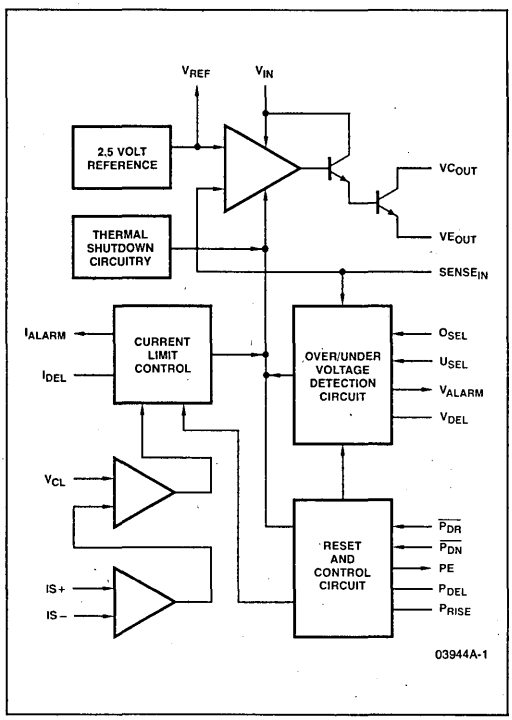


Figure 1. Am6300 Block Diagram

The Am6300 may be powered either by the unregulated supply voltage or by a separate bias voltage (greater than the regulated output by 2.5 volts), at any level between 5 and 40 volts, with a standby current of typically 5mA.

The device is available in either a hermetic or a plastic 20 pin dual in package. Both commercial and military temperature ranges are available.

A detailed description of the circuitry contained in the Am6300 will appear later. However, a review of the more important design considerations in relation to the system aspects will follow, outlining its full range of capabilities.

A precision 2.5V band gap reference is used because it offers low noise and better long term stability than a zener reference. In addition, it has the capability of providing stable performance over an input voltage range of 5 to 40V.

Manufacturing production tolerances are trimmed out, giving an adjusted output voltage to within .25% of 2.5V, a temperature stability of 20 parts per million per degree C over the commercial temperature range and a 40ppm/°C over the military temperature range. In all but the most precise applications, the need for external adjustment is eliminated.

The majority of systems are designed to have over- and under-voltage protection set at either 5 or 10%. The Am6300 includes comparators that detect when these limits are exceeded. The user can define the limits required by programming the requisite pin on the device. This enables different limits to be set for the over- and under-voltage limits. A Current Sensing amplifier compares the differential voltage between the two sense inputs with a user defined reference voltage. Since the common mode voltage range of the current sense amplifier inputs swings from ground to the supply voltage, current sensing can be monitored anywhere within the system. When the sensed voltage exceeds the reference voltage, a current source charges an externally selected capacitor which determines the minimum time a fault condition must exist before shut down occurs. An open collector output is made available to monitor the shut down condition.

A remote reset is required once the regulator has been shut down. The Am6300 has two inputs which may be used for resetting. Power Down ($\overline{\text{PDN}}$) shuts the regulator down when taken LOW, resets the voltage and current detection circuits and switches the regulator on again when taken HIGH. Power Down Reset ($\overline{\text{PDR}}$) works in a similar manner but the regulator switches on after a user defined delay, established by an external capacitor.

The Am6300 also has the facility to control the rate of change of the regulated output following power-up, either from initial power-up or after a $\overline{\text{PDN}}$ or $\overline{\text{PDR}}$ command. The rate of change is controlled by an external capacitor.

The status of the Am6300 is always available via the Power Enable (PE) pin. This is an open collector output, which can be used as a chain priority system in which power-up and shut-down of other supplies are dependent upon the output level.

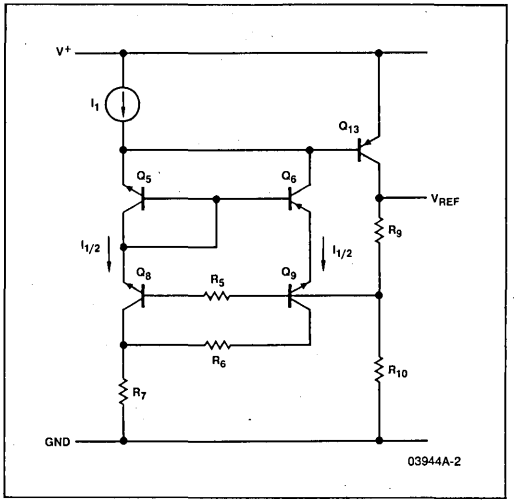


Figure 2. Am6300 Bandgap Reference

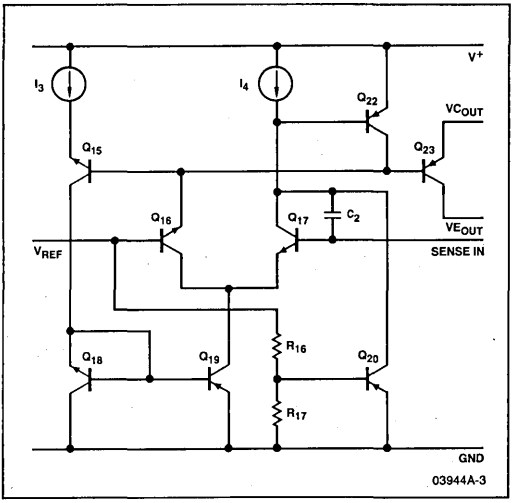


Figure 3. Am6300 Error Amplifier

REFERENCE SOURCE (Figure 2)

The band-gap reference voltage is developed by making the collector currents of Q_8 and Q_9 equal. Since the emitter area of Q_9 is eight times Q_8, their V_{BE}'s will be mismatched and the difference can be expressed as:

$$\Delta V_{BE} = V_{BE8} - V_{BE9} = \frac{kT}{q} \ln 8$$

The band-gap reference voltage is calculated from:

$$V_{BANDGAP} = I_1R_7 + \frac{kT}{q} \ln 8 + V_{BE8} < 1.25 \text{ Volts}$$

V_{REF}, the reference output voltage, is established by the ratio of R_9 and R_{10}, which divides a portion of V_{REF} back to the bases of Q_8 and Q_9. The error between the feedback voltage and the band-gap reference is amplified and coupled back to the output through Q_{13}. The V_{REF} output in the Am6300 is set at 2.5 volts, with production tolerances taken out by adjusting R_7. Typically this results in a reference that is within .25% of 2.5 volts, with a temperature coefficient of 20ppm/°C over the commercial temperature range and 40ppm/°C over the military.

ERROR AMPLIFIER (Figure 3)

The error amplifier, is a single differential amplifier stage composed of Q_{16} and Q_{17}. The biasing of the stage is supplied by equal current sources, I_3 and I_4. The current, I_3, is inverted in Q_{18} and Q_{19}. The area of Q_{19} is approximately twice the value of Q_{18} thus the sink current of Q_{19} is twice I_3. In balance, the collector currents of Q_{16} and Q_{17} will be equal, ignoring effects of base currents of Q_{15}, Q_{22} and Q_{23}.

In an unbalanced, or error condition, where the base of Q_{16} is more positive (negative) than the base of Q_{17}, the collector current of Q_{16} will increase (decrease) and Q_{17} will decrease (increase). The voltage at the bases of Q_{22} and Q_{23} will rise (fall); this results in a higher (lower) current for $V_{E(OUT)}$, the emitter of Q_{23}.

The voltage gain of the error amplifier (typically 3000 at room temperature) is calculated by

$$A_V = \frac{\text{total collector resistance}}{2re} = \frac{R_{C(Q17)} \text{ in parallel with } R_C \text{ (current source)}}{2kT/qI_E}$$

High frequency stability of the error amplifier is ensured by C_1, which gives the amplifier a 6dB/octave roll off. The error voltage is derived by dividing down the output voltage until it equals V_{REF}. The error amplifier will maintain an output voltage equal to V_{REF} multiplied by the closed loop gain of the amplifier set by the user.

The control device is formed by the series pass Darlington pair $Q_{22}-Q_{23}$. The useable output current is theoretically about 100mA, although in practice, applications requiring more than 50mA of current should use an external pass device.

Figure 4 shows the feedback arrangement, consisting of two resistors R_1 and R_2. The required value of V_{OUT} is calculated from:

$$V_{OUT} = V_{REF} \frac{R_1 + R_2}{R_2}$$

where $V_{REF} = 2.5$ volts.

The SENSE IN terminal typically requires about 2μA of bias current. To reduce the error caused by this bias current to around .1%, current flow through R_1 and R_2 should be set approximately 500 times greater. Thus R_2 is set at 2.5kΩ, therefore,

R_1 (kΩ) = (V_{OUT} − 2.5V).

THERMAL SHUTDOWN (Figure 3)

Figure 3 shows the resistive divider formed by R_{16} and R_{17} develop a voltage of 0.3 volts at the base of Q_{20}. As the die temperature approaches approximately 180°C, the V_{BE} of Q_{20} decreases sufficiently to allow the device to be forward biased, thus pulling the collector of Q_{17} low and shutting the regulator down.

7

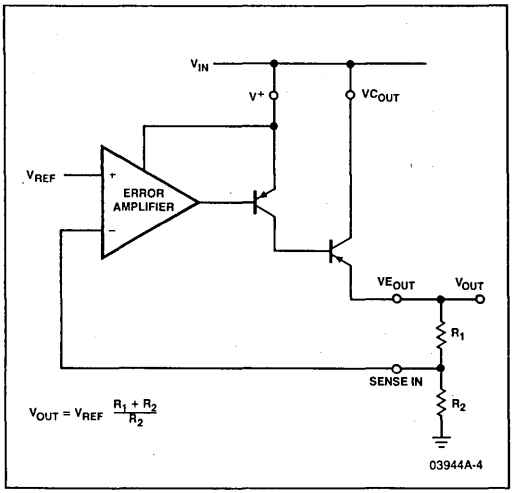


Figure 4. Programming the Am6300 Output Voltage

OVER/UNDER VOLTAGE DETECTION (Figure 5)

Over voltage detection comparators C_1 and C_2 are connected to +5 and +10% levels respectively and are enabled by the OSEL input. A logic 1 selects a +5% limit and a logic 0 a +10%. Similarily, the under voltage comparators C_3 and C_4 provide −5%, logic 1 and −10%, logic 0, selected by the USEL input. The inputs to detection comparators are achieved by dividing down the buffered V_{REF} and SENSE IN voltages. The outputs of the comparators are wired OR'ed, and applied to Q_{58}, which, when on, shunts the output of the current source to ground. Exceeding a selected OV/UV level causes transistor Q_{58} to turn off. If an external capacitor is connected from V_{DEL} to ground it will be charged linearly by the current source, thus causing a delay in shut down that is proportional to the value of the capacitor. With no external capacitor connected, the delay is equal to 1.5μ second. The delay for an externally connected capacitor is an additional 0.22μ second/pF.

A comparator compares the voltage at the collector of Q_{58} with V_{REF}. When Q_{58} reaches V_{REF}, the comparator sets a latch which shuts down the regulator and pulls the open collector of $V_{\overline{ALARM}}$ LOW. The regulator is powered up by either taking $\overline{PDN}$ or $\overline{PDR}$ LOW then HIGH or by momentarily removing the power to the Am6300.

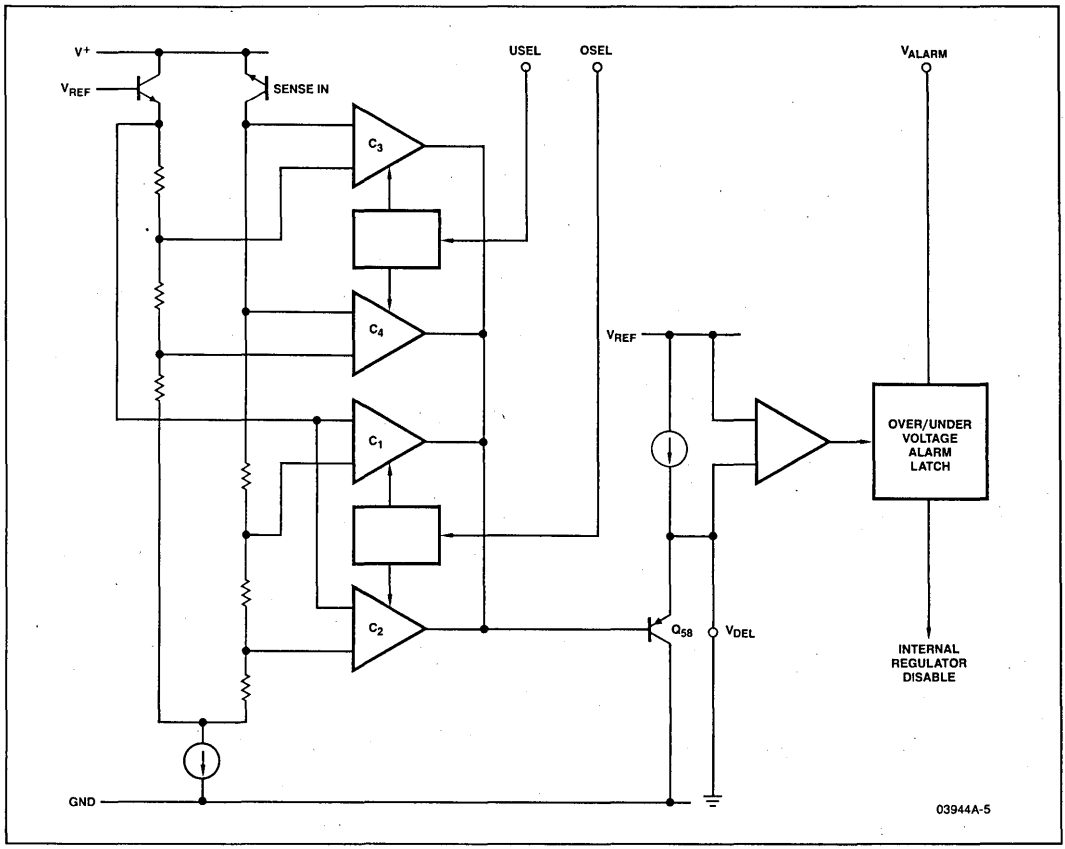


Figure 5. Am6300 Over/Under Voltage Circuit

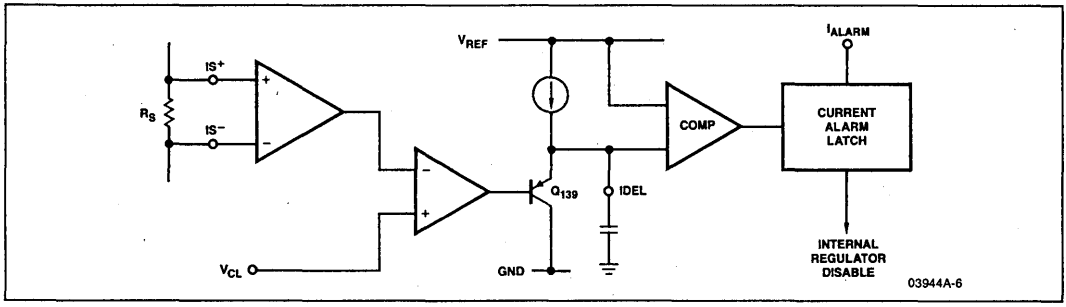


Figure 6. Am6300 Current Overload Circuit

CURRENT LIMITING (Figure 6)

When the differential voltage between I_S^+ and I_S^- of the current sense amplifier (gain of two) exceeds one half of the current limit reference voltage V_{CL}, a comparator detects this condition and switches transistor Q_{139} off. The current limiting circuit is identical to the OV/UV detection circuit above, with Q_{139} replacing Q_{58} and I_{ALARM} replacing V_{ALARM}.

The maximum value of the current sense amplifier's is differential voltage set at 0.2 volts, with a common mode range of 0 volts to the supply voltage. The value of current sense resistor, R_S, can be calculated from:

$$R_S = \frac{V_{CL}}{2I_{CL}}$$

where I_{CL} is the current limit selected.

POWER CONTROL SECTION (Figure 7)

The Am6300 can be logically controlled. The power up, power down and reset sequences of the over/under voltage detection and current limit circuits are all digitally controlled. The logic inputs meet standard logic levels. The input HIGH level is set at 2 volts minimum, but the maximum input voltage can be as HIGH as the supply voltage.

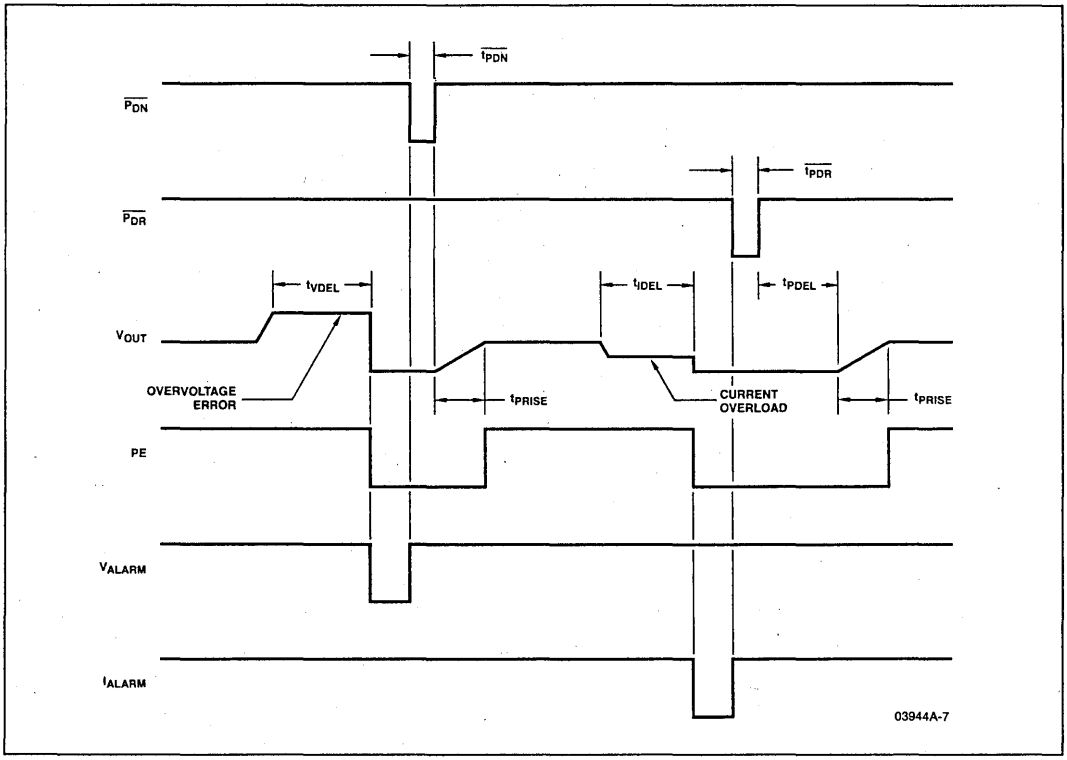


Figure 7. Am6300 System Diagram

Power Supply Control Subsystem

With both sense inputs HIGH, the power up sequence of the Am6300 is initiated by taking either $\overline{PDR}$ or $\overline{PDN}$ inputs HIGH. The difference between $\overline{PDR}$ or $\overline{PDN}$ is that $\overline{PDR}$ has a user defined delay when connecting a capacitor from PDEL to ground before the regulator is powered up.

The output of the Am6300 can be made to ramp linearily from turn-on by connecting an external capacitor from PRISE to ground. This is accomplished by charging the capacitor with a constant current, comparing the SENSE IN voltage with the capacitor voltage and maintaining equality. Thus the rate of change of the output voltage is a function of itself and the capacitor value.

$$\text{The rate of change of output} = \frac{\Delta V_{OUT}}{0.22C + 1.5}$$

in V/μs, where C is expressed in pF.

With no external capacitor, the rise time of the Am6300 power up is 1.5μs.

During the time that the regulator is ramping up, the power control circuitry disables the over/under voltage detection circuit and changes the gain of the current sense amplifier from two to one, thus doubling the current limit. This provides extra current to charge capacitive loads.

APPLICATIONS

The regulator section of the Am6300 can be thought of as a basic voltage regulator. The reference voltage is applied to the positive input of the error amplifier and a sample of the output voltage is fedback to the negative input via a resistive divider. The output voltage is achieved by multiplying the reference voltage by the gain of the error amplifier. The SENSE IN voltage will equal the reference voltage, thus the output will be set by the ratio of the resistors. Referring to Figure 8.

$$\frac{V_{OUT}}{V_{REF}} = \frac{R_1 + R_2}{R_2}$$

Because a small amount of bias current is required by the error amplifier, an error voltage is generated across R_i. To keep this error less than .1%, the current through R_2 should be set at 1mA. This will simplify the selection of R_1, resulting from

$$R_1 = (V_{OUT} - 2.5V)\ k\Omega$$

The required resistor values may not result in readily available values, but the ratio

$$\frac{V_{OUT}}{V_{REF}} = \frac{R_1 + R_2}{R_2}$$

should be maintained.

The spread in V_{REF} is typically less than .25% and in most applications no external trimming is necessary. If adjustment is required, some portion of R_1 and R_2 should be made adjustable.

Figure 8 shows the connection of a low current voltage regulator, I_{MAX} = 50mA. The Am6300 is rated at 100mA load current, but because of the maximum power dissipation of 1000mW and the derating characteristic of 8mW/°C, most low current applications should be limited to around 50mA load current.

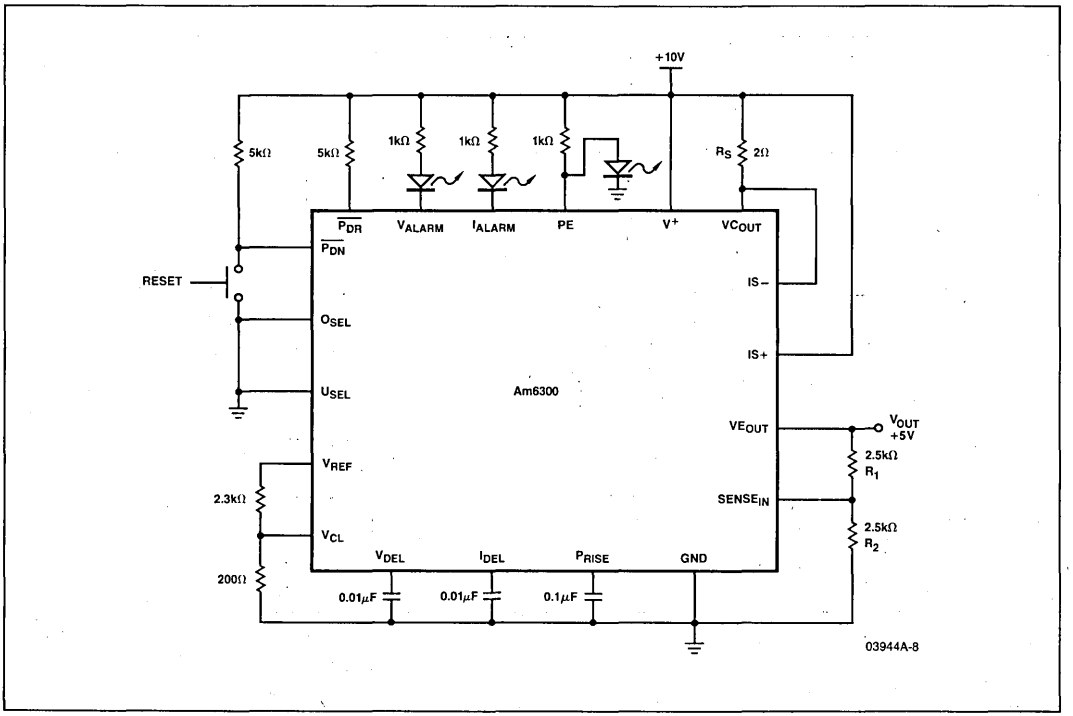


Figure 8. Am6300 Low Current Configuration

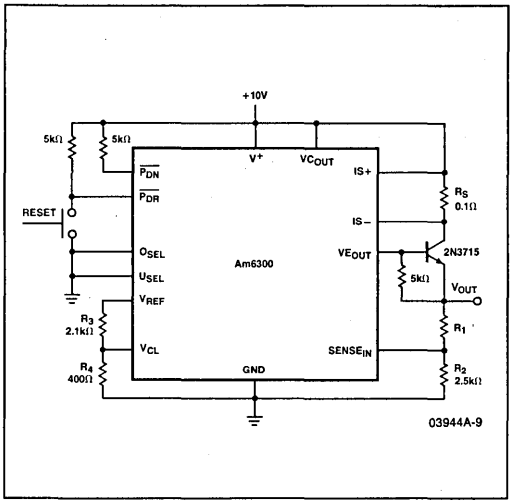


Figure 9 Am6300 High Current Configuration

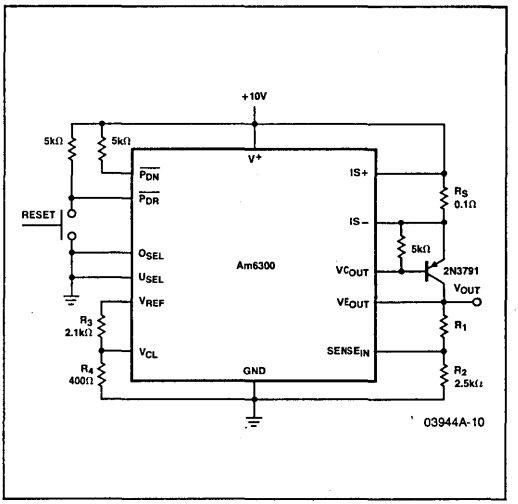


Figure 10. Am6300 High Current Configuration

The current sensing is accomplished by detecting the voltage across R_S, which is placed between V^+ and V_{COUT}. No additional voltage drop is required in the circuit, thus relaxing the minimum differential voltage, V^+ to V_{OUT}. The selection of R_S is given by:

$$R_S = \frac{V_{SENSE}}{I_{CL}}$$

V_{SENSE} has a maximum value of 0.2 volts but the actual value of V_{SENSE} is a function of the current overload reference voltage, V_{CL} and is set at a maximum of 0.4 volts. The ratio of V_{SENSE} to V_{CL} is 0.5, therefore I_{CL} can be related to the overload reference voltage, V_{CL} by

$$I_{CL} = \frac{2V_{CL}}{R_S}$$

V_{CL} is most cases can be conveniently obtained by dividing down the 2.5 volt reference shown. Figure 8 also shows over/under voltage, current limiting and power-up rise time capacitors. The values shown give approximately 2ms for the over/under voltage and current limiting detection circuits to experience fault conditions before shutting down the regulator. To limit the effects of the inrush currents for charging up output load capacitors, the rate of change of the output voltage is limited to .23V/ms.

LED's are connected to the V_{ALARM}, I_{ALARM} and PE open collector outputs to give indications of fault conditions and to show the status of the regulator.

Resetting the regulator after a fault condition is achieved by taking $\overline{PDN}$ LOW.

HIGH CURRENT VOLTAGE REGULATOR

By the use of external pass transistors, the useable current can be increased to several amps, the power dissipation in the Am6300 reduced as well.

The simplest circuit is shown in Figure 9. The internal Darlington pass transistor is extended to a triplet by an external NPN transistor. This NPN could also be a Darlington. Using external NPN power transistors is more economical than using PNP, but the minimum differential voltage between inputs and outputs is increased by the additional V_{BES} of the external transistors.

Figure 10 shows the circuit with a PNP transistor added to overcome the above. The base drive for the PNP is now obtained from the V_{COUT} terminal of the Am6300.

Both Figures 9 and 10 show how including R_S outside the feedback loop reduces the differential voltage between input and output to a minimum, thus reducing the power dissipation within the regulator. The output current for both circuits is rated at 2 amps and the current limiting resistors are 0.1Ω in value, allowing low wattage resistors to be used.

PROGRAMMABLE VOLTAGE REGULATOR

A specialized application for the Am6300 is shown in Figure 11. The output voltage of the regulator is programmable under microprocessor control. The design uses an Am6080, an eight bit microprocessor compatible digital-to-analog converter. The reference current for the DAC is derived from the voltage reference of the Am6300. The programmed output current of the DAC sinks current through R_6. This eastablishes the output voltage of the regulator because the regulator maintains the SENSE IN voltage at 2.5 volts.

The regulator output will be defined by

$V_{OUT} = (2.5 + R_6 I_{DAC})$ volts

Using a value of 10kΩ for R_6, provides an output swing of 2.5 volts to 22.5 volts, selected by the 8 bit code latched into the Am6080.

A four-bit latch is connected between the microprocessor bus and the Am6300 logic control inputs. In this way, start-up, shut-down and reset of the alarms, plus setting the over/under voltage limits, can be controlled by the microprocessor.

The output status and alarm outputs can be monitored by the microporcessor to indicate fault conditions. This will allow the microprocessor to take whatever action is required because of the fault conditions.

Power Supply Control Subsystem

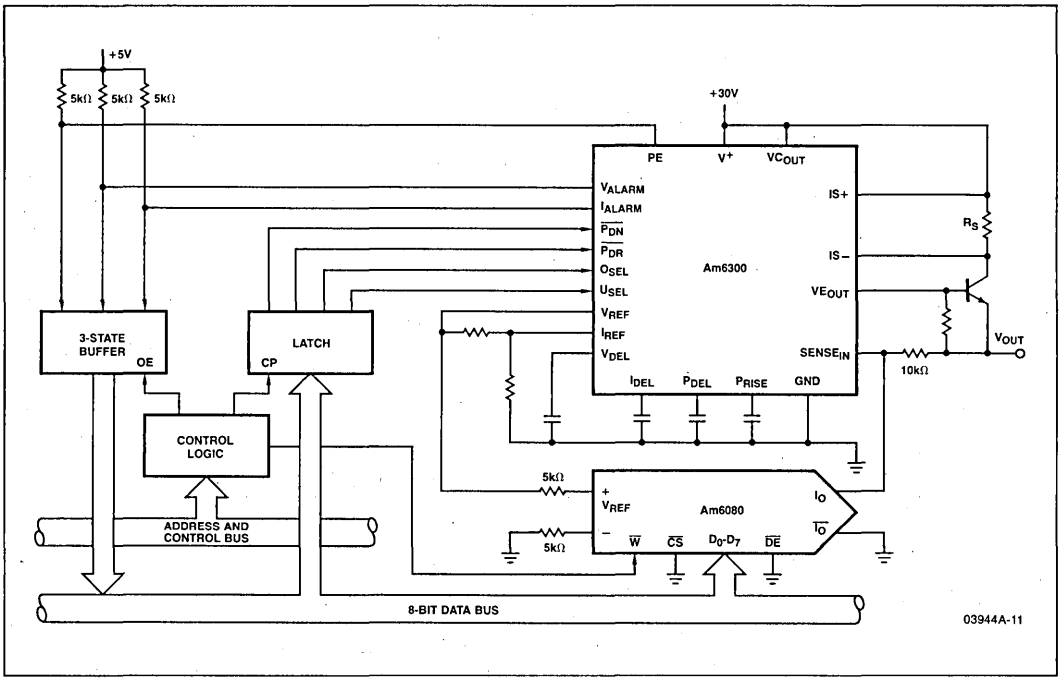


Figure 11. Am6300 Programmable Voltage Regulator

Power Supply IC Programs E²PROMs

The controlled rise-time signals necessary to program 2816 type E²PROMs require pulse generating circuits capable of compensating for RC time and temperature drifts. This circuit (Figure 1), while providing controlled rise-times, can also regulate the programming voltage, control the pulse duration, and monitor the pulse amplitude to assure proper programming. This is accomplished through a unique application of the many control and protection features found on the Am6300 linear power supply controller.

Specifications for 2816 E²PROMs call for a programming pulse amplitude of 21 ±1V with a rising edge RC time constant between 450 and 750μs and a minimum pulse duration of 10ms. Because it contains the error amplifier and pass transistor of a linear power supply, the Am6300 can provide a 21 volt output from any unregulated input voltage between 24 and 40V. Pulse amplitude can be monitored by the Am6300 output voltage protection circuit; tying the O_{SEL} and U_{SEL} pins to +5 volts sets the error limits to ±5%. If an output error greater than ±1V occurs, then the pulse is terminated and the Programming Error Flag goes low to indicate possible incomplete programming.

The rising edge of the pulse is controlled by the soft start circuit of the Am6300. This circuit provides a linear rate of change at the pulse output, and the use of a 4700pF capacitor at P_{RISE} gives the best linear approximation to the recommended exponential rise (Figure 2). Other risetimes can be implemented using the formula: $t_{RISE} = (C_{RISE} \times .22\mu s/pF) + 1.5\mu s$.

Pulse duration is controlled by the current protection circuit which takes the output LOW 10ms after it reaches 21V. A current overload is simulated at the sense pins of the Am6300 and the required pulse duration is set by a .047pF capacitor at the shutdown delay pin. Pulse duration is measured from the completion of the soft start ramp, and can be calculated from the formula: $t_{IDEL} = (C_{IDEL} \times .22\mu s/pF) + 1.2\mu s$. The Programming Complete output goes LOW at the end of each pulse. This output, the Programming Error Flag, and the write input are TTL compatible for ease of system interfacing.

Figure 1. Am6300 EEPROM Programming Pulse Generator

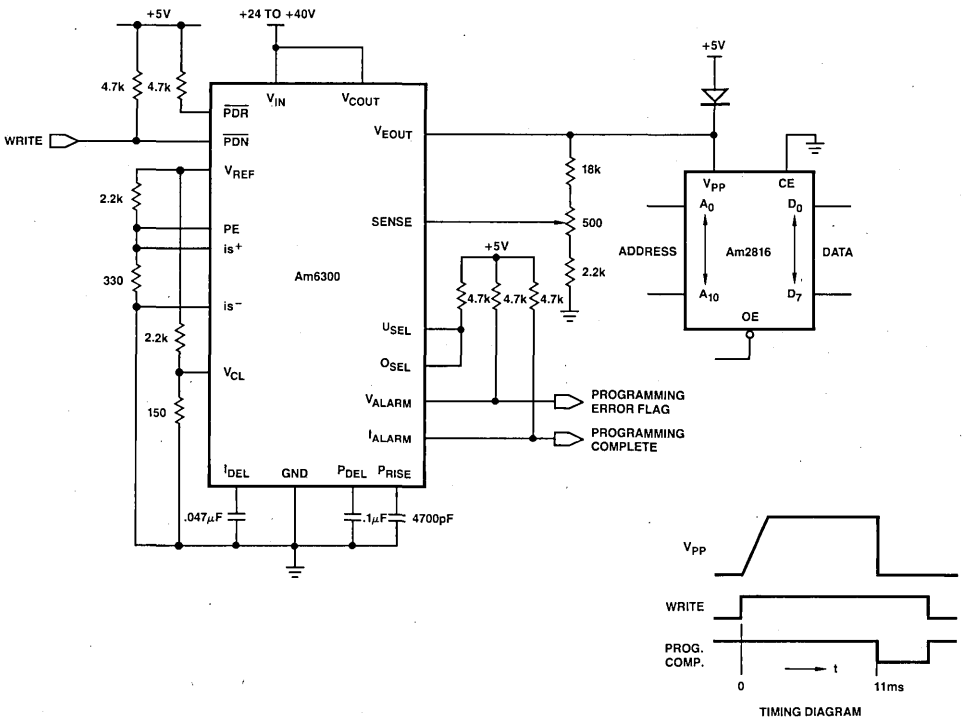


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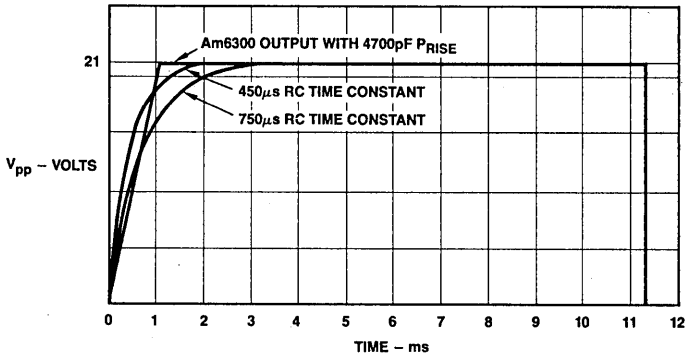
Figure 2. Comparison of Am6300 Output to Recommended Waveforms



Am6301

Switching Power Supply Controller

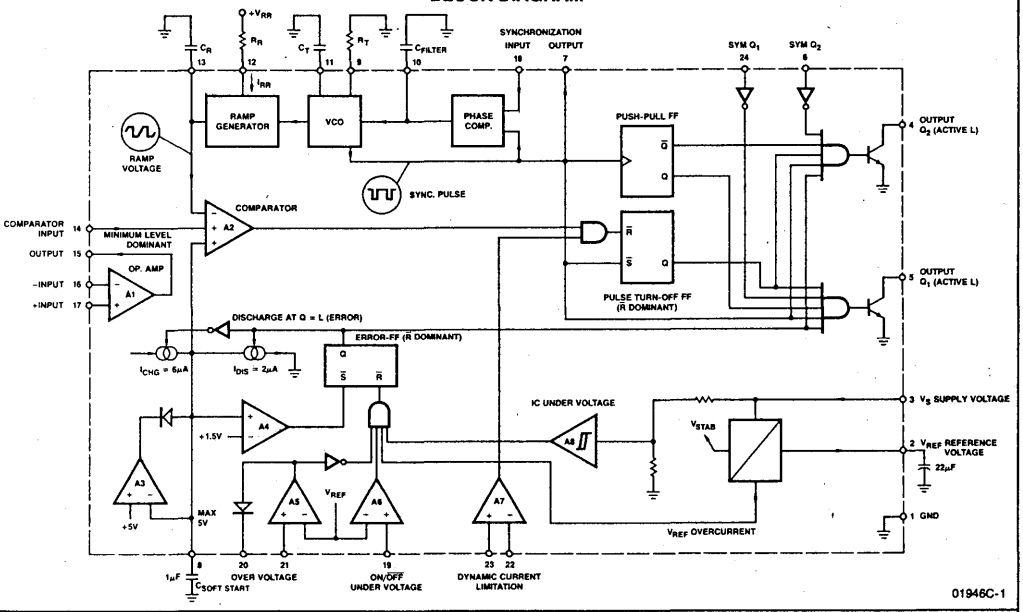
DISTINCTIVE CHARACTERISTICS

- Feed-forward (line hum suppression)
- Output over/under voltage protection
- Input under voltage protection
- Cycle-by-cycle current limiting
- Soft start
- 250kHz max. oscillator frequency
- Phase lock capability
- 96% max. duty cycle
- Double pulse suppression
- Symmetry inputs for push-pull converter
- Remote shutdown
- Pin equivalent to the Siemens' TDA 4700

GENERAL DESCRIPTION

The Am6301 Switching Power Supply Controller contains all the digital and analog functions necessary to control blocking, single-ended, or push-pull switching power supplies. It contains the voltage controlled oscillator, ramp generator, comparator, and reference for basic switched mode power supplies, as well as, a full complement of interface circuits and circuitry to protect both the power supply and its load.

BLOCK DIAGRAM



ORDERING INFORMATION

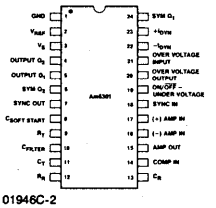
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type	Temperature Range
Am6301DM	Hermetic DIP	−55 to +125°C
Am6301LC	Leadless*	0 to 70°C
Am6301DL	Hermetic DIP	−25 to +85°C
Am6301DC	Hermetic DIP	0 to 70°C
Am6301PC	Plastic DIP	0 to 70°C

*Availability of leadless packages will be announced.

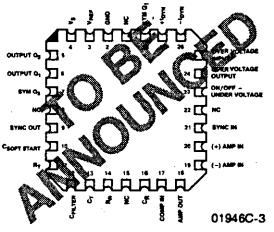
CONNECTION DIAGRAMS – Top Views

D-24-1, P-24-1



01946C-2

L-28-1



01946C-3

Note: Pin 1 is marked for orientation.

01946C-ANA

MAXIMUM RATINGS (Above which useful life may be impaired)

Supply Voltage V_S	33V	Voltage at Q_1, Q_2	33V
Input Voltage (all inputs)	Gnd to V_S	Current at Q_1, Q_2	70mA
Output Voltage A5	33V	Input Current R_{ramp}	1mA
Output Voltage A1	6.5V	Operating Temperature	
Storage Temperature	−65 to +125°C	Am6301DL	−25 to +85°C
Lead Temperature (soldering 60 sec)	300°C	Am6301DC, Am6301PC, Am6301LC	0 to +70°C
Power Dissipation	(Note 3)		

ELECTRICAL CHARACTERISTICS (Note 1)

These specifications apply for 11V ≤ V_S ≤ 30V, f_{VCO} = 15kHz, over the operating temperature range unless otherwise specified.

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Regulator						
V_S	Supply Voltage		11		30	Volts
I_S	Supply Current	C_T = 1nF, F = 100KHz	8	12	20	mA
f_{VCO}	Operating Frequency Range		40		250K	Hz
Reference						
V_{REF}	Reference Voltage	0 ≤ I_{REF} ≤ 5mA	2.35	2.50	2.65	Volts
ΔV_{REF}	Line Regulation	V_S = 25V ± 20%		5	15	mV
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 5mA		10	20	mV
$\Delta V_{REF}/\Delta T_A$	Temperature Stability			250	400	μV/°C
Oscillator						
f_{VCO}	Operating Frequency Range		40		250K	Hz
Δf/f	Initial Tolerance	ΔC_T = 0%, ΔR_T = 0%			±7	%
Δf/f	Frequency Stability	V_S = 25V ± 20%	−1		1	%
t_{VCO}	Fall Time	C_T = 1nF		1		μs
Ramp Generator						
f_{ramp}	Frequency Range		40		250K	Hz
V_{ramp} Hi	Voltage at C_{ramp} High	10μA ≤ I_{ramp} ≤ 400μA		5.5		Volts
V_{ramp} Low	Voltage at C_{ramp} Low	10μA ≤ I_{ramp} ≤ 400μA		1.8		Volts
I_{ramp}	Input Current at R_{ramp}		10		400	μA
Synchronization						
V_{IH}	Synchronization Input		2			Volts
V_{IL}					0.8	Volts
V_{OH}	Synchronization Output	I_{OH} = 200μA	4			Volts
V_{OL}		I_{OL} = 1.6mA			0.4	Volts
I_B	Input Bias Current		−5	−1		μA
Comparator A2						
I_B	Input Bias Current		−2	−1		μA
t_{A2}	Turn-Off Delay (Note 2)	T_A = 25°C		470		ns
V_{IN}	Input Voltage for Duty Cycle	T_{On}/T_{Off} = 0%		1.8		Volts
		T_{On}/T_{Off} = Max		5.0		
Soft Start						
I_{CHG}	Charging Current			6		μA
I_{DIS}	Discharging Current			2		μA
V_{LIM}	Upper Limiting Voltage			5		Volts
V_{TH}	Reset Voltage			1.5		Volts

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Operational Amplifier						
A_{OL}	Open Loop Gain		60	80		dB
V_{OS}	Input Offset Voltage		−10		10	mV
$\Delta V_{OS}/\Delta T_A$	V_{OS} Tempco		−30		30	μV/°C
I_B	Input Bias Current		−2	−0.5		μA
V_{CM}	Common Mode Range		0		5	Volts
I_O	Output Current		−3		1.5	mA
$\Delta V/\Delta t$	Output Slew Rate			1		V/μs
BW	3dB Bandwidth			3		MHz
ϕt	Phase Shift at 3MHz			120		degrees
VSW	Output Voltage Swing	$-3mA \leq I_L \leq 1.5mA$	1.5		5.5	Volts
Symmetry						
V_{IH}	Input Voltage		2			Volts
V_{IL}					0.8	Volts
I_{IL}	Input Low Current		−2	−1		μA
Output States Q_1, Q_2						
V_{OL}	Output Voltage	I_O = 20mA			1.1	Volts
I_{OH}	Output Current	V_{OH} = 30V			2	μA
ON/$\overline{\text{OFF}}$, Under Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 30mV	V_{REF}	V_{REF} + 30mV	Volts
I_B	Input Bias Current		−2	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Dynamic Current Limiting						
V_{CM}	Common Mode Range		0		4	Volts
V_{OS}	Input Offset Voltage		−10		10	mV
I_B	Input Bias Current		−2	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Over Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 30mV	V_{REF}	V_{REF} + 30mV	Volts
I_B	Input Bias Current		−2	−1		μA
I_{OH}	Output Current	V_{OH} = 5V	0		200	μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Supply Under Voltage						
V_{ON}	Turn-On Threshold, V_S Rising		8.8	9.6	10.5	Volts
V_{OFF}	Turn-Off Threshold, V_S Falling		8.5	9	10.0	Volts

Notes:
1. All typical values are specified at V_S = 12V and T_A = 25°C.
2. The A2 comparator turn-off delay is measured from pin 14 to pin 4 or pin 5. The input signal on pin 14 is a negative-going pulse from 3V to 0.5V. The delay is measured from the 2V level on the input to the 2V level on the output. The output current is set at 4mA. The signal on pin 14 goes negative when the ramp voltage is equal to 2V.
3. For T_A greater than 25°C, derate to limit T_J to a maximum of 150°C. For P_D less than 750mW use typical thermal resistance as follows:

Typ	D-24-1	P-24-1	L-28-1	
θ_{JA}	50	120	100	°C/watt
θ_{JC}	15	60	40	°C/watt

MAXIMUM RATINGS (Above which useful life may be impaired)

Supply Voltage V_S	33V	Voltage at Q_1, Q_2	33V
Input Voltage (all inputs)	Gnd to V_S	Current at Q_1, Q_2	70mA
Output Voltage A5	33V	Input Current R_{ramp}	1mA
Output Voltage A1	6.5V	Operating Temperature	
Storage Temperature	−65 to +125°C	Am6301DM	−55 to +125°C
Lead Temperature (soldering 60 sec)	300°C		
Power Dissipation	(Note 1)		

ELECTRICAL CHARACTERISTICS (Note 2)

These specifications apply for $11V \leq V_S \leq 30V$, $f_{VCO} = 15kHz$, over the operating temperature range (−55 to +125°C) unless otherwise specified.

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Regulator						
V_S	Supply Voltage		11		30	Volts
I_S	Supply Current	T_A = −55°C, 25°C		12	20	mA
		T_A = 125°C		10	15	
Reference						
V_{REF}	Reference Voltage	$0 \leq I_{REF} \leq 5mA$	2.25	2.50	2.75	Volts
ΔV_{REF}	Line Regulation	V_S = 25V ± 20%		5	15	mV
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 5mA		10	20	mV
$\Delta V_{REF}/\Delta T_A$	Temperature Stability			250		μV/°C
Oscillator						
f_{VCO}	Operating Frequency Range		40		250K	Hz
Δf/f	Initial Tolerance	ΔC_T = 0%, ΔR_T = 0%			±10	%
Δf/f	Frequency Stability	V_S = 25V ± 20%	−2		2	%
t_{VCO}	Fall Time	C_T = 1nF		1		μs
Ramp Generator						
f_{ramp}	Frequency Range		40		250K	Hz
V_{ramp} Hi	Voltage at C_{ramp} High	$10\mu A \leq I_{ramp} \leq 400\mu A$		5.5		Volts
V_{ramp} Low	Voltage at C_{ramp} Low	$10\mu A \leq I_{ramp} \leq 400\mu A$		1.8		Volts
I_{ramp}	Input Current at R_{ramp}		10		400	μA
Synchronization						
V_{IH}	Synchronization Input		2			Volts
V_{IL}					0.8	Volts
V_{OH}	Synchronization Output	$I_{OH} = 200\mu A$	4			Volts
V_{OL}		I_{OL} = 1.6mA			0.4	Volts
I_B	Input Bias Current		−10	−1		μA
Comparator A2						
I_B	Input Bias Current		−10	−1		μA
t_{A2}	Turn-Off Delay (Note 3)	T_A = 25°C		470		ns
V_{IN}	Input Voltage for Duty Cycle	T_{On}/T_{Off} = 0%		1.8		Volts
		T_{On}/T_{Off} = Max		5.0		
Soft Start						
I_{CHG}	Charging Current			6		μA
I_{DIS}	Discharging Current			2		μA
V_{LIM}	Upper Limiting Voltage			5		Volts
V_{TH}	Reset Voltage			1.5		Volts

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Operational Amplifier						
A_{OL}	Open Loop Gain		60	80		dB
V_{OS}	Input Offset Voltage		−15		15	mV
$\Delta V_{OS}/\Delta T_A$	V_{OS} Tempco		−30		30	μV/°C
I_B	Input Bias Current		−10	−0.5		μA
V_{CM}	Common Mode Range		0		5	Volts
I_O	Output Current		−3		1.5	mA
$\Delta V/\Delta t$	Output Slew Rate			1		V/μs
BW	3dB Bandwidth			3		MHz
ϕ_t	Phase Shift at 3MHz			120		degrees
VSW	Output Voltage Swing	$-3mA \leq I_L \leq 1.5mA$	1.5		5.5	Volts
Symmetry						
V_{IH}	Input Voltage		2			Volts
V_{IL}					0.8	Volts
I_{IL}	Input Low Current		−10	−1		μA
Output States Q_1, Q_2						
V_{OL}	Output Voltage	I_O = 20mA			1.3	Volts
I_{OH}	Output Current	V_{OH} = 30V			10	μA
ON/$\overline{\text{OFF}}$, Under Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 50mV	V_{REF}	V_{REF} + 50mV	Volts
I_B	Input Bias Current		−10	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Dynamic Current Limiting						
V_{CM}	Common Mode Range		0		4	Volts
V_{OS}	Input Offset Voltage		−30		30	mV
I_B	Input Bias Current		−10	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Over Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 50mV	V_{REF}	V_{REF} + 50mV	Volts
I_B	Input Bias Current		−10	−1		μA
I_{OH}	Output Current	V_{OH} = 5V	0		200	μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Supply Under Voltage						
V_{ON}	Turn-On Threshold, V_S Rising		8.5	9.6	11.0	Volts
V_{OFF}	Turn-Off Threshold, V_S Falling		8.2	9	10.5	Volts

Notes: 1. For T_A greater than 25°C, derate to limit the junction temperature, T_J to a maximum of 150°C. For P_D less than 750mW, θ_{JA} = 50°C/watt and θ_{JC} = 15°C/watt.

2. All typical values are specified at V_S = 12V and T_A = 25°C.

3. The A2 comparator turn-off delay is measured from pin 14 to pin 4 or pin 5. The input signal on pin 14 is a negative-going pulse from 3V to 0.5V. The delay is measured from the 2V level on the input to the 2V level on the output. The output current is set at 4mA. The signal on pin 14 goes negative when the ramp voltage is equal to 2V.

Am6301 FUNCTIONAL DESCRIPTION

VOLTAGE-CONTROLLED OSCILLATOR (VCO)

The VCO (voltage-controlled oscillator) generates a sawtooth voltage at C_T. The duration of the falling edge is determined by the selection of C_T. The duration of the rising edge and thus the oscillator frequency is determined by R_T and C_T. Maximum oscillator frequency is 250kHz. The oscillator frequency can be varied for frequency synchronization purposes by varying the voltage at C_{filter}. The falling edge of the VCO generates the synchronization pulse and triggers the ramp generator and other parts of the Am6301.

RAMP GENERATOR – FEED-FORWARD CONTROL

The ramp generator is triggered by the synchronization pulse of the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator must be shorter than the fall time of the VCO. The voltage of the rising edge of the ramp generator and a DC voltage at comparator A2 are compared for pulse width control of the output. The slope of the rising edge is adjusted via the current through R_R. This enables an additional superimposed control of the duty cycle dependent on the input voltage of the Switched Mode Power Supplies (SMPS). This capability (feed-forward) allows for compensation of a known interference (e.g. line hum).

PHASE COMPARATOR – SYNCHRONIZATION

If the Am6301 is operated without external synchronization, the synchronization input must be connected to the synchronization output, so that the phase comparator sets the voltage at C_{filter}. The VCO then oscillates at the frequency set by R_T and C_T. Other circuits can be synchronized with the synchronization output. The Am6301 can be synchronized to an external signal of any duty cycle. The synchronization input and output are TTL compatible.

PUSH-PULL FLIP-FLOP

The push-pull flip-flop is toggled by the falling edge of the VCO. This guarantees that only one of the two push-pull outputs can be enabled at any one time.

COMPARATOR A2 – PULSE WIDTH MODULATION

The two noninverting inputs of the comparator are switched in such a manner that the lowest level is always compared with the inverting input. As soon as the voltage of the rising sawtooth at C_R exceeds the lower of the two levels, both outputs are disabled via the pulse turn-off flip-flop.

REGULATING AMPLIFIER A1

A1 is a high-quality regulating amplifier. It can be used in the control loop to transmit the amplified error voltage onto the free noninverting input of the comparator A2. A voltage change is thus transformed into a duty cycle change. The common mode range of A1 covers 0 to +5V. A1's low output impedance allows the use of feedback for the adjustment of the regulator loop-characteristics.

PULSE TURN-OFF FLIP-FLOP

This flip-flop enables the outputs at the beginning of each half period, and upon an error signal from A7 or a turn-off signal from A2 switches the outputs off for the remainder of the half period. Double pulses at the output cannot occur.

COMPARATOR A3

A3 limits the voltage at the $C_{soft\ start}$ pin (and also one input of A2) to a maximum of 5V. For a specified slope of the rising ramp generator edge, the duty cycle can be limited to a maximum value.

COMPARATOR A4

Comparator A4 has its switching threshold set to 1.5V and its output connected to the error flip-flop, so that when the voltage at capacitor $C_{soft\ start}$ is less than 1.5V the flip-flop is set. The error flip-flop only accepts the set pulse if no reset signal is present. Thus, an output turn-on is prevented as long as an error signal is present.

SOFT START

The output duty cycle is a function of the lower of the two voltages at the noninverting inputs of A2. At the time the Am6301 is turned on, the voltage at capacitor $C_{soft\ start}$ is equal to 0V. As long as no error exists, this capacitor is charged with a current of 6μA to the maximum value of 5V. In the case of an error, $C_{soft\ start}$ is discharged with a current of 2μA. The error flip-flop is set when the $C_{soft\ start}$ voltage is below 1.5V and the outputs are enabled if a reset signal is not present at the same time. The minimum ramp generator voltage is 1.8V, therefore, the soft start circuit only controls the duty cycle after the voltage at $C_{soft\ start}$ exceeds 1.8V.

ERROR FLIP-FLOP

Error signals to input $\overline{R}$ of the error flip-flop cause the outputs to be disabled immediately. The system turns on again using the soft start, after the error has been eliminated.

COMPARATOR A5 – OVER VOLTAGE

The input or output voltages of an SMPS can be monitored using A5. In the case of an over voltage, the error flip-flop immediately disables the IC outputs. After the over voltage is reduced, the SMPS turns back on using the soft start. The output of A5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the over voltage, until the supply voltage is briefly turned off, or the over voltage input is briefly connected to ground. To use this SCR-type action, the voltage to be monitored must be coupled resistively ($\geq$5KΩ) to the over voltage comparator.

COMPARATOR A6 – ON/$\overline{\text{OFF}}$ UNDER VOLTAGE

The comparator A6 reacts to an under voltage relative to V_{REF} and switches the IC outputs off. The input voltage of the SMPS can for example, be monitored, turning the outputs off if the input voltage is below a desired level. When the input voltage returns to the desired level, the Am6301 turns back on using the soft start. This input can also be used as a TTL compatible ON/$\overline{\text{OFF}}$ control.

COMPARATOR A7 – DYNAMIC CURRENT LIMITING CIRCUIT

A7 provides for the recognition of over current in the switching transistors. The system is turned on again at the beginning of the half period after the error is eliminated, the soft start is not used however. The A7 common mode range extends from 0 to +4V so that the smallest voltage drops can be recognized. The delay time from the occurrence of an error to the disabling of the outputs is only 250ns.

COMPARATOR A8 – IC UNDER VOLTAGE

Comparator A8 prevents undefined operating conditions of the IC outputs if the IC supply voltage becomes too low. If $V_S \leq 9V$, the output stage is disabled. This condition is maintained until V_S = 0V. Built-in hysteresis prevents permanent switching at the comparator's switching threshold. At a supply voltage of $V_S \geq 9.6V$, the Am6301 turns on using the soft start.

SYMMETRY

Saturation of the transformer core must be prevented in push-pull converters. The degree of saturation of the transformer can be determined with an external circuit; and, in relation to this, the on times of the outputs can be asymmetrically shortened. If the symmetry correction circuit is not required, the symmetry inputs must be connected to ground. The input levels are TTL compatible.

OUTPUTS, DEADTIME

The two outputs Q_1 and Q_2 are transistors with open collectors. Their saturation voltage is 1V at 20mA. They operate in a push-pull mode and can be connected in parallel to drive single-ended converters with a maximum duty cycle of 96%. The time, during which only one of the two outputs is on, can be varied. The duration of the falling edge at the VCO is the same as the minimum time (dead time) during which both outputs are disabled simultaneously. The dead time, in push-pull SMPS, prevents the power transistors from being on at the same time.

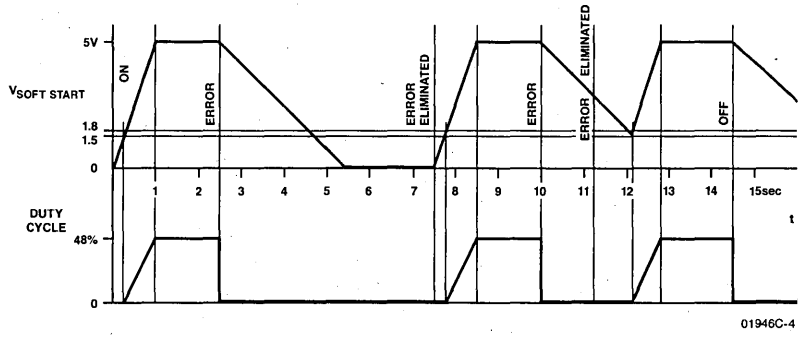


Figure 1. Am6301 System Timing Showing Soft Start, Error Timing, and Remote Shutdown. ($C_{soft\ start}$ = 1μF.)

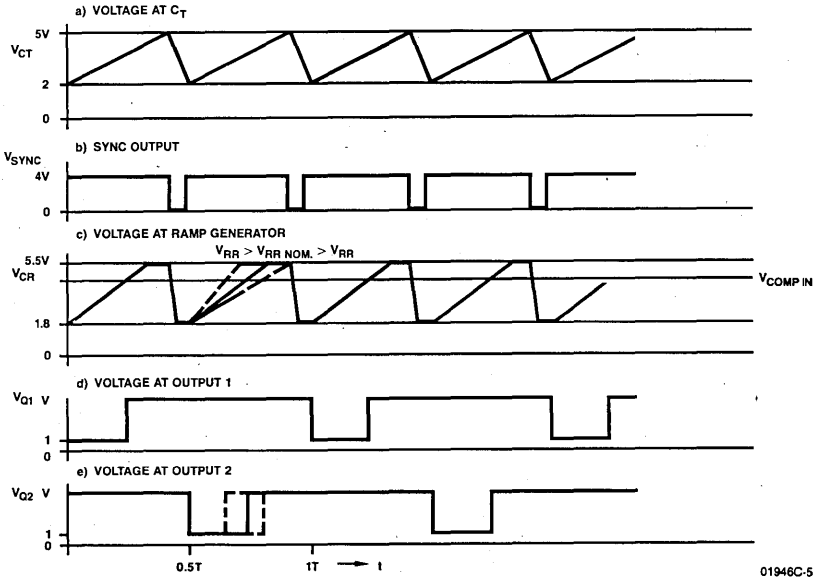


Figure 2. Am6301 Pulse Timing Diagram, Dotted Lines Show the Effect of Feed-Forward Control.

7

APPLICATION INFORMATION

Selection of External Components

Three external components must be selected for the Am6301 phase locked oscillator; these are R_T, C_T, and C_{filter}. Having determined the desired frequency of operation, f_o, and minimum dead time, t_d, the user can find a value for C_T by using Figure 3. R_T is then chosen from C_T and f_o using Figure 4. If the oscillator is to be used in its free-running mode with SYNC OUT tied to SYNC IN, then the C_{filter} pin can be left open. If phase-lock operation is desired, then C_{filter} can be chosen from Table A.

The selection of the ramp generator external components, R_R and C_R, allows the implementation of two functions:

1. Feed-forward control
2. Reduction of the maximum duty cycle

In most applications, C_R is chosen equal to C_T, and the ramp slope is controlled by R_R and the voltage applied to it, V_{RR}. If V_{RR} is connected to the power supply, V_{IN}, then changes in V_{IN} will change the ramp slope. This causes an inversely proportional change in the output duty cycle which compensates for the change of input voltage. R_R can then be selected from the formula:

$$R_R(\Omega) = \frac{3 \cdot R_T \cdot C_T \cdot (V_{RR} - 0.7)}{C_R \cdot \Delta V_{CR}} - (4 \cdot 10^3)$$

The value ΔV_{CR} represents the peak-to-peak amplitude of the ramp and is generally chosen to be less than 3.2V. The ramp voltage varies from 1.8V to 1.8 + ΔV_{CR} volts. One noninverting input of the comparator, A2, is maintained at 5V, therefore, the maximum duty cycle is reduced by ΔV_{CR} values greater than 3.2V.

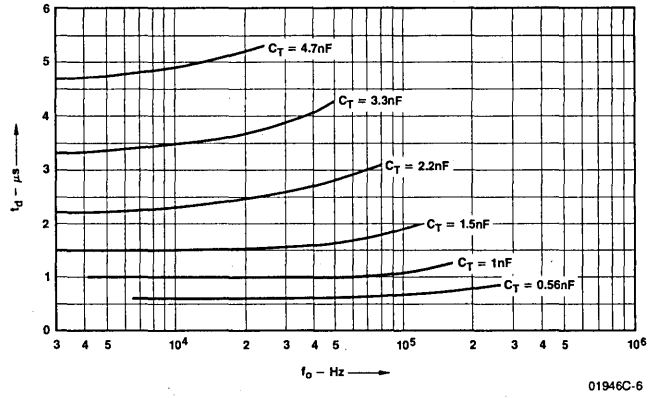


Figure 3. Deadtime t_d versus C_T and f_o.

TABLE A

f_o (kHz)	C_{filter} (nF)
1	470
1–10	47
1–100	4.7
1–250	.47

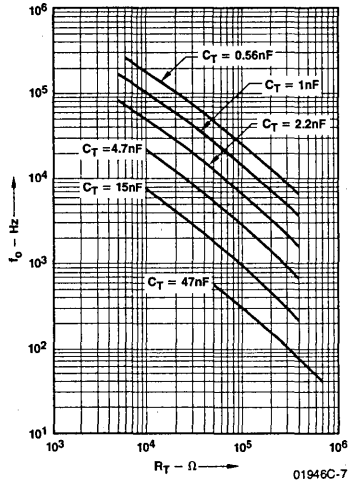
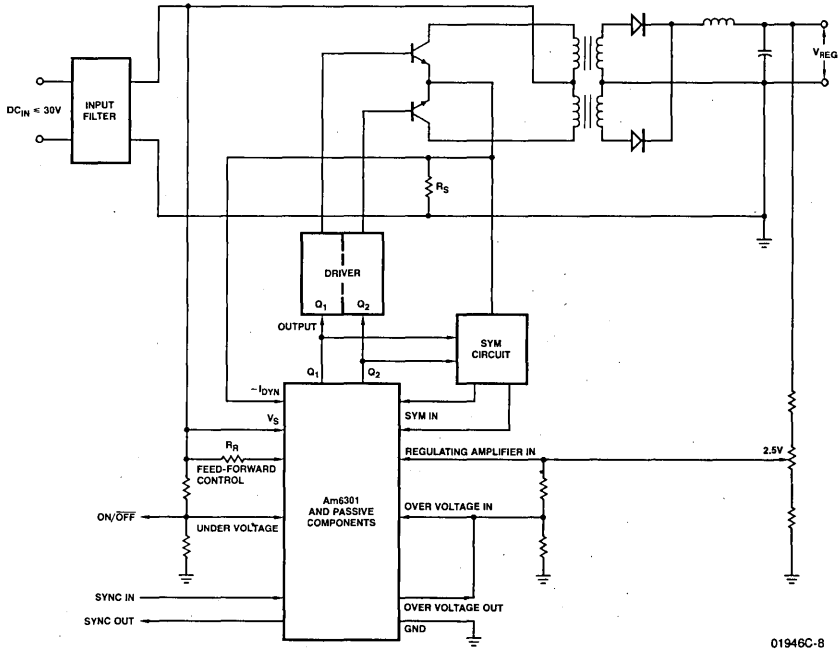
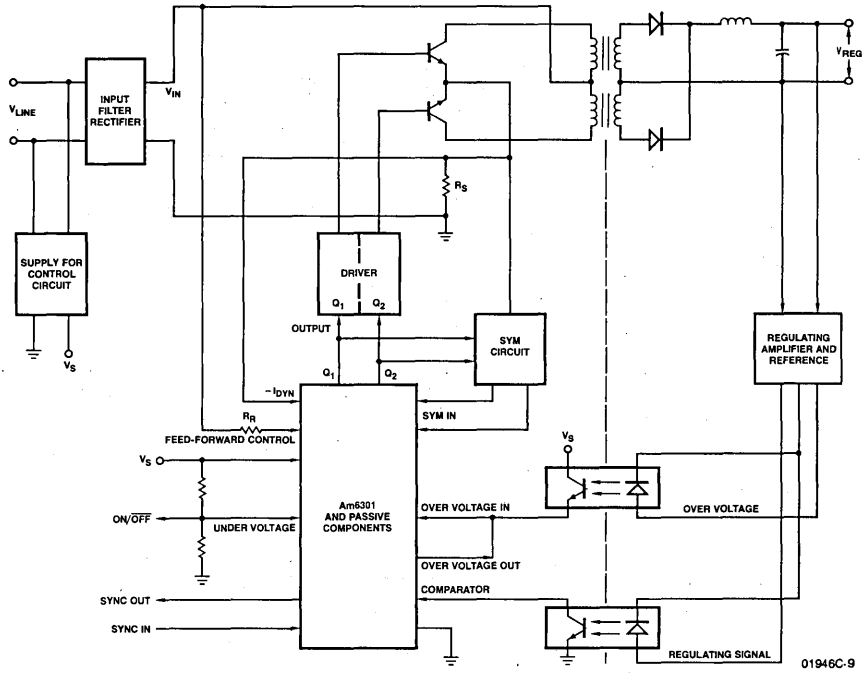


Figure 4. Oscillator Rated Frequency f_o versus R_T and C_T.



Basic Circuit Diagram of a Push-Pull SMPS with Common Ground.



Basic Circuit Diagram of a Push-Pull SMPS with Isolation.
(Am6301 is on the Primary Side.)

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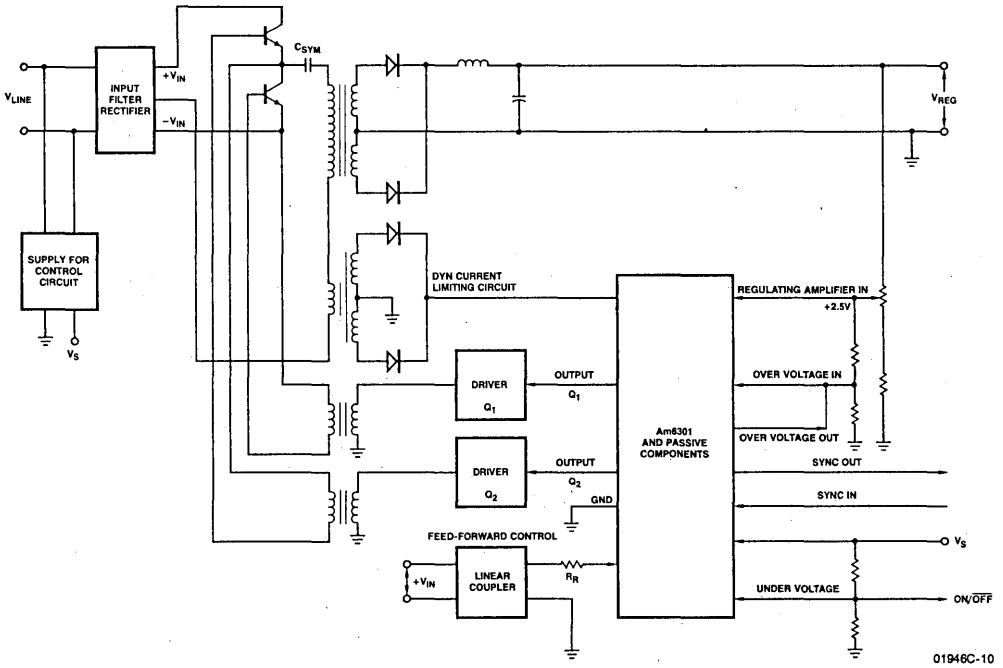
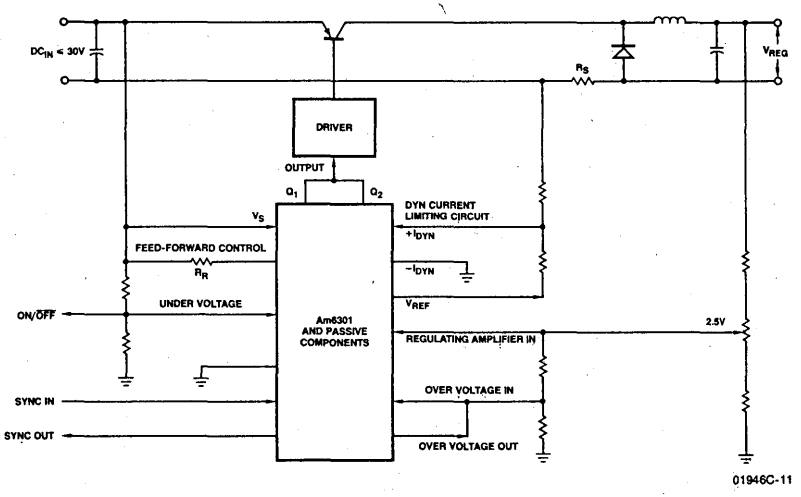


Basic Circuit Diagram of a Half-Bridge SMPS Using the Am6301 on the Secondary Side.



Buck Converter Using the Am6301.

FUNCTIONAL PIN DESCRIPTION

V_{REF} The output of the internal 2.5V reference.

Output Q_1, Q_2 The open collector output transistors capable of sinking 70mA each.

SYMQ_1, Q_2 Transformer unbalance control inputs. With a small amount of external circuitry these inputs can be used to cause asymmetrical output duty cycles. This allows correction for imbalances in the push-pull circuitry.

SYNC OUT The VCO output, used for synchronizing other circuits to the Am6301.

$C_{soft\ start}$ An external capacitor at this pin causes the output duty cycle to increase linearly during power up.

R_T, C_T An external resistor and a capacitor at these pins control the VCO center frequency of the phase locked loop oscillator.

C_{filter} An external filter capacitor for the control voltage of the phase locked loop is connected to this pin.

SYNC IN This pin is connected to one input of the phase comparator in the phase locked loop, the other input is internally connected to the VCO output.

R_R, C_R An external resistor and a capacitor at these pins control the slope of the ramp generator. The feed-forward control works by changing the voltage across R_{ramp} which affects the ramp slope and causes a modulation of the duty cycle.

Comp In The noninverting input of the pulse width modulating comparator.

Amp Out The output of the uncommitted operational amplifier. This amplifier is used as the error amplifier in most systems.

(+) Amp In, (−) Amp In These are the inputs of the uncommitted operational amplifier.

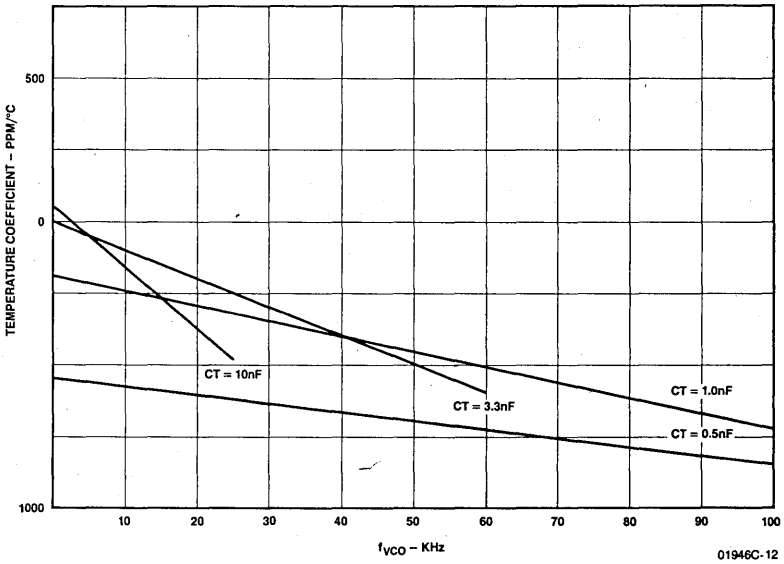
ON/$\overline{\text{OFF}}$ Under Voltage This input disables the outputs when it is connected to a voltage lower than V_{REF}. It can be connected as a remote shutdown or as an under voltage protection.

Over Voltage Input This input disables the outputs whenever it is higher than V_{REF}.

Over Voltage Output The output of the over voltage comparator. This pin can be connected back to the over voltage input for SCR-type protection.

+I_{DYN}, −I_{DYN} Sense inputs for the dynamic current limiting circuit.

Figure 5. Am6301 f_{VCO} Temperature Coefficient.



By permitting feed-forward control, a switched-mode power-supply circuit avoids the tradeoffs necessary with feedback circuits and off-the-line regulators. The result is better line regulation.

Controller IC sacrifices nothing to improve regulation

Line regulation can be improved without making undesirable tradeoffs by using a switched-mode power-supply controller that allows feed-forward control. The single-chip controller, besides offering the usual protection and control features, avoids the problems that would crop up with conventional feedback circuits and off-the-line regulators.

With conventional feedback circuits, line regulation cannot be improved without compromising loop stability. A high-gain feedback path is needed for good line regulation, but low-gain feedback is necessary to prevent oscillations at the resonant frequency of the power supply's output filter. Usually the problem is solved by designing an error amplifier that has high dc gain but low gain near the filter's resonant frequency. Though this solution works reasonably well with dc-input switchers, it is less useful for regulators that work directly off the ac line.

Off-the-line regulators avoid a 60-Hz transformer and other bulky components, thus greatly reducing the size, weight, and cost of the system. But off-the-line operation confronts the switcher with large input ripple voltages. Unfortunately, the resonant frequency of the output filter usually falls near the 120- or 360-Hz frequency of the input ripple; reduction of gain at these frequencies will increase the ripple at the power-supply output. Of course, input filters could be added to reduce the ripple amplitude entering the switcher, but that would sacrifice any size-reduction advantage.

An effective alternative is a controller circuit such as the Am6301, which allows feed-forward control of line variations—even at ripple frequencies. Capable of sensing both the input and output voltages of switched-mode power supplies, the Am6301 allows the designer to tailor both input and output regulation to meet most requirements.

The Am6301 is divided into several functional blocks (Fig. 1). Though some basic connections are made internally, external connections largely determine the final circuit configuration, so the circuitry can be customized to provide various optional features. For example, because the on-chip error amplifier (A_1) is not internally connected to other parts of the circuit, the power-supply designer can tailor the feedback loop to meet specific requirements. Thus, in isolated systems where an external error amplifier must be used, A_1 can be left unconnected, and the isolated control signal can be fed directly to the pulse-width modulation comparator.

The PWM section of the controller includes a voltage-controlled oscillator and ramp generator (capable of 250-kHz operation), a comparator (A_2), a push-pull flip-flop, and a pulse-turn-off flip-flop. Another comparator (A_7) senses current and is connected to the pulse-turn-off flip-flop, which prevents double pulses during dynamic current limiting. A turn-off time of 250 ns enables A_7 to protect the power supply's switching transistors from damage caused by input-current surges.

A number of TTL-compatible control inputs are available, including remote shutdown, synchronization, and symmetry controls. Also, the Am6301 provides overvoltage and undervoltage protection, input undervoltage protection and soft-start capability.

The input controls the output

The dc output voltage of a switched-mode supply is a direct function of the dc input voltage and can be determined from the standard equation:

$$V_{out} = V_{in} \times \text{duty cycle} \times \text{turns ratio} \quad (1)$$

Because the Am6301 allows feed-forward control, it can sense V_{in} and control the pulse-width modulator's

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duty cycle to maintain a constant V_{out}.

The term "feed-forward" applies because the control signal is fed forward from V_{in} instead of being fed back from V_{out} as with most other controller chips. Of course, the Am6301 also allows normal feedback control, and both types of control can be used simultaneously.

Figure 2 shows a simplified schematic of a switched-mode power supply. The effects of input ripple and other line variations on the circuit can be determined from the following equation:

$$V_{out} = [V_{PWM} - V_{ramp}\,(min)] \times A_{SW} \times \text{turns ratio} \qquad (2)$$

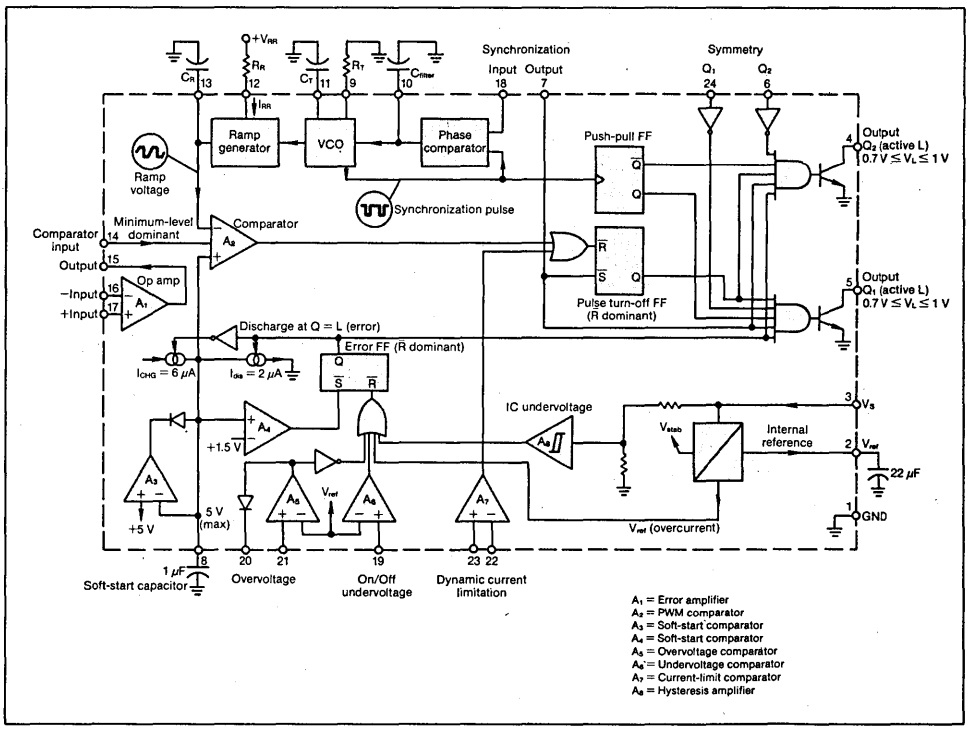
where

$$A_{SW} = \text{switch gain} = \frac{V_{in}}{V_{ramp}(pk\text{-}pk)} \qquad (3)$$

Evidently, an increase in V_{in} will cause a proportionate increase in switch gain. The output voltage will remain constant only if the error amplifier adjusts V_{PWM} to compensate for the change in switch gain. To compensate for the change, the V_{out} must be corrected by an amount equal to the change in V_{PWM} divided by the error-amplifier gain. Therefore, the effect of a change in the input voltage on the output voltage is inversely proportional to the gain of the error amplifier.

For example, a system with an error-amplifier gain of 100 will have a line regulation of approximately 1%. Line regulation could be improved by increasing the error amplifier's gain, but this could cause a loss of loop stability and possible oscillation.

The key to good line regulation is to keep the switch gain constant, which avoids the need for a complex



1. The internal circuitry of the Am6301 switched-mode power-supply controller is divided into functional blocks. Many of the connections are made externally, instead of on chip, for maximum flexibility.

feedback loop to compensate for changes in gain. As shown in Eq. 3, if V_{ramp}(pk-pk) is controlled in direct proportion to V_{in}, the effective switch gain will remain constant. But most switch-mode power-supply controllers do not allow ramp amplitude to be modulated. Since the ramp generator is usually an integral part of the oscillator, the ramp amplitude cannot be changed without affecting the oscillator frequency.

On the other hand, ramp amplitude can be controlled with the Am6301, because its ramp generator and oscillator are separate circuits. The VCO sets the operating frequency and triggers the start of each ramp. Ramp amplitude can then be made directly proportional to V_{in}, simply by connecting V_{in} to the ramp supply voltage as in Fig. 1 (V_{RR}). Ramp supply current (I_{RR}) is mirrored by the ramp generator to charge the ramp capacitor. Because the ramp period remains constant, unless the oscillator frequency is changed, a change in V_{in} produces a proportionate change of V_{ramp}(pk-pk).

Though some other switch-mode controller ICs can provide feed-forward control, they do so with a single ramp-generating oscillator. With these circuits, the oscillator thresholds must be changed (as the ramp charging current is changed) to hold the frequency constant. This requires perfect tracking between the oscillator thresholds and the capacitor charging current; otherwise, the oscillator frequency will be modulated by the feed-forward control. As already shown, however, the design of the Am6301 avoids that problem.

Designing the feed-forward control

To design a feed-forward control circuit with the Am6301, the power-supply designer simply selects two external components for the oscillator—timing capacitor (C_T) and timing resistor (R_T)—and two for the ramp generator—ramp resistor (R_R) and ramp capacitor (C_R). First, the engineer must decide on the required frequency of operation and the dead time. The latter should be greater than the turn-off time of the switch transistors to prevent simultaneous conduction and possible damage. Then C_T and R_T can be selected from graphs (Fig. 3).

The value of the ramp capacitor is usually chosen to be the same as that for the timing capacitor. Then the ramp resistor can be calculated from the following equation:

$$R_R = \frac{[3R_T \times C_T \times (V_{in}(nom)] - 0.7 - (4 \times 10^3)}{C_R \times V_{ramp}(pk\text{-}pk)} \quad (4)$$

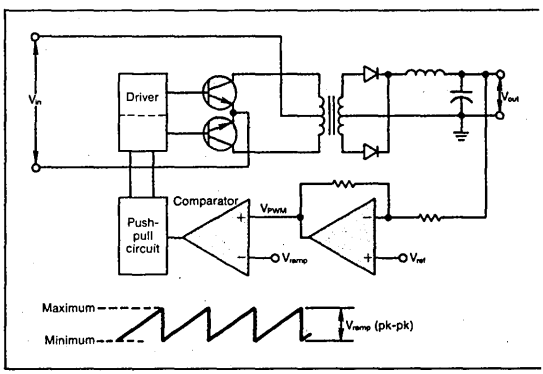
The V_{ramp}(pk-pk) used in the equation is the value for a nominal input voltage (V_{in}). It should be between 2 and 2.9 V. Because of the required one-to-one relationship between the input voltage and the ramp voltage, feed-forward control can be achieved very simply. With V_{in} connected directly to R_R, no adjustment or trimming is needed for proper circuit operation. If the designer decides not to use the feed-forward feature, R_R can be connected to any convenient stable voltage. Then that voltage is substituted for V_{in}(nom) in Eq. 4.

For systems that use several power supplies, switching frequencies may need to be synchronized. This will prevent beat-frequency interference that could otherwise result from subtle differences in the operating frequencies.

The use of separate oscillator and ramp-generator circuits simplifies synchronization. In those controllers where the oscillator also serves as a ramp generator, the synchronization input usually allows

Filter-capacitor values for VCO synchronization

Free-running frequency (kHz)	Capacitance (nF)
1	470
1–10	47
10–100	4.7
100–250	0.47



2. In a switched-mode power supply, feedback from the output controls the width of pulses that drive transistor switches in the primary circuit of the transformer. This basic scheme, however, has only limited effectiveness in compensating for line-voltage variations.

just an external connection to the ramp discharge transistor. But to avoid holding the ramp low for too long, the inputs to the synchronization pin must be narrow pulses. Also, the input pulses can only increase the oscillator frequency, not decrease it.

More flexibility is provided by the Am6301, which uses a phase-locked loop to externally synchronize signals above and below the free-running frequency regardless of duty cycle. This configuration, which requires a VCO, is possible with the Am6301 because the oscillator's amplitude does not affect controller operation.

To use the synchronization feature of the controller chip, the power-supply designer determines the value of a filter capacitor and makes the necessary connections for the synchronization signal. The value can be selected from the table. An external oscillator can generate the synchronization signal, or the sync-out terminal of one IC can be used to synchronize other controller chips. Synchronization signals can be connected directly to the controller chips or via optocouplers if isolation is needed (Fig. 4). The frequency of the synchronization signal must be within 30% of the free-running frequency set by R_T and C_T.

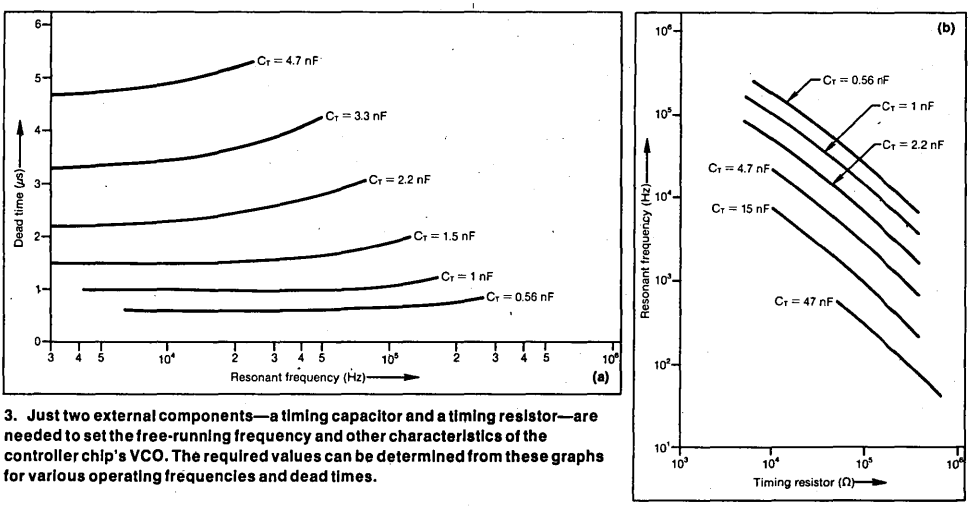
If synchronization is not used, the sync-out pin must be tied to the sync-in pin. When the circuit is so connected, the filter-capacitor pin can be left open.

In systems that use bipolar switch transistors, longer-than-usual dead times may be needed for PWM signals. This is because dead times that are shorter than the switch turn-off time will cause simultaneous conduction of a pair of switches. Then the input will be shorted to ground, and the resulting current surge may cause switch destruction.

Reducing the maximum duty cycle

Dead time can be easily increased with the Am6301 because of the design of the PWM comparator (A_2) and the soft-start section. The soft-start voltage and the control voltage are connected to separate noninverting inputs of A_2, which simplifies the design of the chip and also allows the connection of an external error amplifier. The two inputs to A_2 are switched internally so that the lower of the two levels is always being compared with the ramp voltage.

During power-up, the soft-start voltage controls the pulse width, making it increase linearly. When the soft-start voltage exceeds the error-amplifier voltage, normal regulation takes over. The soft-start voltage then continues to increase until it reaches a 5-V limit set by A_3. In other words, if the ramp



3. Just two external components—a timing capacitor and a timing resistor—are needed to set the free-running frequency and other characteristics of the controller chip's VCO. The required values can be determined from these graphs for various operating frequencies and dead times.

voltage exceeds 5 V, both outputs must be off.

The maximum duty cycle can be reduced by adjusting V_{ramp} (pk-pk) so that the ramp voltage crosses 5 V at the desired maximum duty cycle. The conditions for maximum duty cycle can be approximated by the following formula:

$$\frac{t_{on}(max)}{t_{off}} = \frac{5}{V_{ramp}\ (pk\text{-}pk)+1.8\ V} \times 100\%$$

Some possible problem areas should be examined. Changes in load current cause some minor changes in output voltage due to the nonideal properties of various components. The departures from ideal operation stem from the dynamic resistance of the output rectifier, the resistance of the transformer windings, and the variations of saturation voltage vs collector current for the switch transistors. Because all these factors have only a minor effect, a small amount of dc gain in the feedback loop can easily compensate for them.

A more important consideration, however, is to prevent loop oscillation. Such oscillations occur because of output-filter gain and phase shift at the resonant frequency (f_0), which can be calculated from

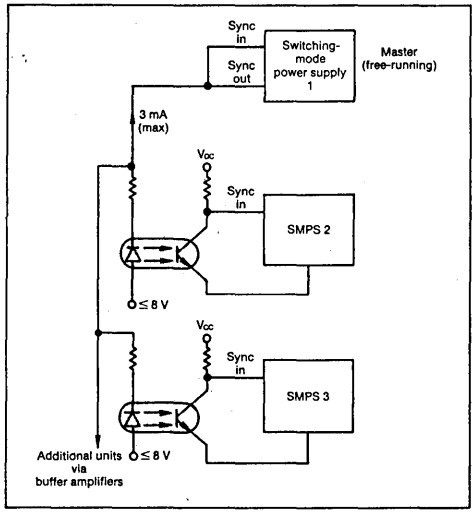
$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

gain and phase shift near the resonant frequency depend on the load resistance (R_0). A useful measure of the effect of the load is the damping constant $R_0/\sqrt{LC}$. This figure can become very high at low load currents. The gain and phase shift increase as the damping constant increases. Worst-case values of approximately 30 dB and 180° occur with damping constants greater than 20. The feedback loop will oscillate in the presence of positive gain and 180° phase shift.

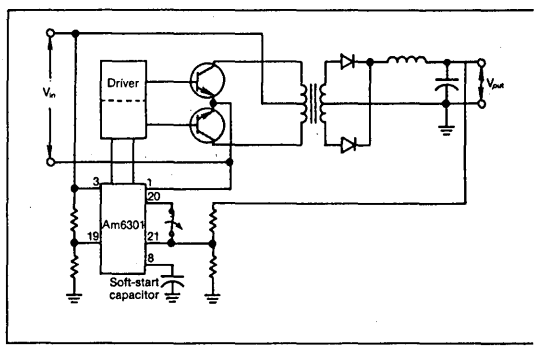
Ensuring stability

Loop stability is guaranteed if the total loop gain is reduced to less than unity at the frequency where total phase shift equals 180°. Power-supply designs must be stabilized individually, which involves drawing gain and phase plots over a frequency range from dc to at least the frequency where the roll-off of the LC filter prevents positive loop gain.

Loop gain equals the sum of the divider gain (equal to R_2/R_1+R_2), error-amplifier gain, switch gain, transformer turns ratio, and LC filter gain. The divider gain, switch gain, and turns ratio stay constant over the frequency range. The gain of the LC filter is unity up to the vicinity of the resonant frequency, f_0. Then there is a sharp peak at f_0 and roll-off thereafter. The gain of the error amplifier, therefore, must be reduced at f_0 by connecting a series R-C across the feedback resistor.



4. If isolation is required, controller chips can be synchronized with a master chip by connecting them together by means of optocouplers. Because of the limited current capability of the chip's sync-out circuit, buffer amplifiers may be needed to drive a large number of chips.



5. Protection against both input undervoltage and output overvoltage is easily applied to power-supply designs based on the Am6301. The only additional components required are resistors for a pair of voltage dividers and a capacitor to provide soft-start capability.

In power supplies that employ push-pull or full-bridge switch configurations, variations in the transistor-switch speeds, or transformer windings can cause a condition known as transformer unbalance, which causes a difference in primary current on opposing half cycles. Because the transformer's primary windings are wound in opposite directions, any unbalance will add to the transformer flux in one direction and subtract from it in the other direction. The result is a net bias, or dc component, in the transformer flux. Therefore, the transformer will be driven closer to saturation in one direction than in the opposite direction.

Transformer saturation must be prevented to protect the switch transistors from current spikes caused by the effective zero impedance of a saturated inductor. The problem is usually solved either by overdesigning the power transformer or by connecting a large dc blocking capacitor in series with the transformer primary. Trouble is, a blocking capacitor tends to be especially large and expensive because of the high breakdown voltage and high capacitance required.

A better solution is to use a circuit that adjusts the output on time. Because it offers one additional input (SYM Q_1 and SYM Q_2 in Fig. 1) to each output AND gate, the Am6301 can be conveniently interfaced with an imbalance-correction circuit.

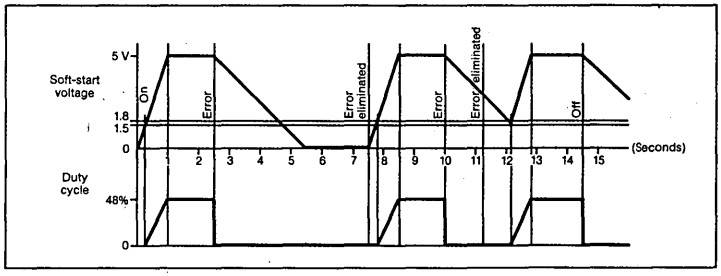
Power-supply protection schemes

Three functional blocks in the Am6301 allow protection circuits to be included in power-supply designs. Overvoltage protection and undervoltage protection are provided by comparators A_5 and A_6, and current protection is provided by comparator A_7. The IC is also protected from low supply voltages by comparator A_8, which shuts down the outputs if the supply voltage falls below 9 V.

The simplicity of the circuits provided in the controller chip allows a great deal of flexibility in power-supply protection. The undervoltage comparator, for example, has its inverting input tied to V_{ref}. Because there is no internal connection to the noninverting input, it can be connected to any signal that must be kept above some minimum value. The low-voltage threshold can be set to any value by the ratio of a pair of resistors (Fig. 5). This feature is often used to sense a power supply's input voltage —shutting down the system when the input is not sufficient for the driver circuit to saturate the switch transistors. Because of its 2.5-V threshold, A_6 can also be used as a TTL-compatible on/off control.

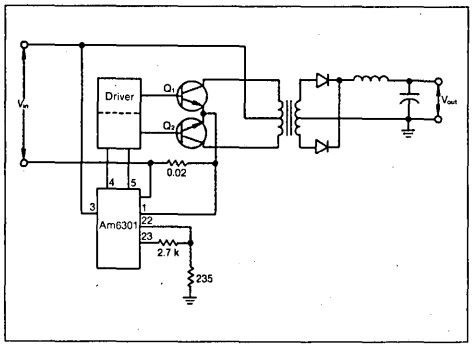
Comparator A_5 senses overvoltages relative to V_{ref}; usually it is employed to sense output voltage. When A_5 or A_6 detects an error, the outputs are immediately disabled and the soft-start capacitor begins to discharge (Fig. 6). If the error has been removed when $V_{soft\ start}$ reaches 1.5 V, comparator A_4 will reset the error latch and the circuit will restart using the soft start. Often, of course, errors that cause a shutdown will reoccur when the circuit restarts. If this happens, the system will cycle up and down until the error is permanently corrected.

Some power-supply designers may prefer an SCR-type overvoltage protection—where the error latch must be manually reset before the supply can restart. With the Am6301, this can be accomplished by tying the A_5 output back to its noninverting input. Then the circuit can be restarted only by briefly breaking that connection or by removing power from the IC.



6. As shown in this timing diagram, the power supply will automatically restart after remote shutdown, provided the error has been eliminated. The soft-start feature avoids damage during turn-on if a system fault still exists.

Switched-mode power-supply IC



7. The controller chip allows cycle-by-cycle dynamic current limiting. To use this feature, the designer needs merely to determine the value of the current-sensing resistor and the current-limiting knee. The circuit shown is set to limit primary current at approximately 10 A.

The Am6301 offers a cycle-by-cycle type of current limiting. The overcurrent comparator, A_7, is connected directly to the pulse-turn-off flip-flop. When an overcurrent is sensed, the outputs are turned off in approximately 250 ns. Outputs are reenabled at the beginning of the next half cycle, unless the overcurrent is still present. Because the pulse-turn-off flip-flop can be reset only by a synchronization pulse, a double pulse on one output cannot occur during current limiting. With this design, the return current in the primary winding can be sensed. Then the switch transistors can be turned off quickly enough to protect them from damage. Of course, this circuit can just as easily be used to sense the output current of a switching power supply, to protect the output section and the load.

Dynamic current limiting merely requires the selection of R_S and the current-limiting knee—an important improvement over older designs, where the threshold was related to the base-emitter voltage of a transistor. In these older designs, the current limit sometimes had to be set to more than 150% of the desired maximum current to allow for the curvature of the limiting knee. In the Am6301, on the other hand, the turn-on error stems only from the V_{OS} of the comparator. The offset voltage has a maximum of 20 mV. This means that, with a 200-mV threshold voltage, turn-on uncertainty is only 10%. The circuit shown in Fig. 7 is set to limit primary current at 10 A ±10%.□

5 Volt 100 Watt Line Operated Supply with Auxiliary ±15V Output

This supply shows several features which users of the Am6301 will find useful. The output transformer and optocouplers provide isolation from the line. The switching devices are power FETs and a simple, direct gate-drive technique is used. A push-pull stage, usually needed only above 200 watts output, was used here to illustrate a technique for symmetry correction. The power output could easily be increased several times by using large magnetics and semiconductors while retaining the same regulation and drive circuitry. Finally, an auxiliary ±15 volt output at .4 amps is provided.

Exceptional regulation and noise performance was obtained with up to 78% DC bus efficiency. Most of the losses occur in the Schottky rectifier on the 5 volt output.

SCHEMATIC DESCRIPTION

The input power passes through an RFI filter consisting of four .005μF capacitors and a common mode supression inductor. A thermistor limits the filter capacitor charging surge current. The rectifier and filter provide a DC bus voltage of 120 to 167 volts: +15 volt driver power is obtained through a zener and series resistor.

The power circuit consists of a commercially available output transformer driven in center-tapped, push-pull configuration by a pair of power FETs, IRF720, rated at 400V, 3A, 1.8 ohm. Primary leakage inductance is snubbed by the diode-R-C networks consisting of 1N4937 diodes, .01μF capacitors and 39k resistors. The FETs are further protected from transients by a pair of transient absorbing zeners, 1.5KE350A.

The main output is rectified by Schottky diodes, SD241, which are snubbed by 10 ohm 0.039μF RC networks. An LC filter and preload resistor complete the output circuit. Auxiliary output is derived from a full wave doubler, IN4935, on winding 8, 9, 10 of the transformer. LC filters and 2.7k preload resistors furnish approximately ±15 volts. These outputs have no feedback for load regulation, but the main output's feedback circuitry gives them good line regulation. For main output loads above 2 amps and auxiliary output loads above 100mA, the auxiliary voltage will stay between 15 and 17 volts. Additional linear regulators could be placed on the outputs if desired.

Feedback is taken from sense terminals. These are linked to the power terminals by 10 ohm resistors to maintain feedback in case the sense to power terminal connections (dotted lines) are omitted. The 5 volt sense points power the following circuits: the 2.4V reference zener (1N4370) via the 2.2k resistor, op amps and the optocouplers via 270 ohm series resistors. A 33 ohm, 22μF filter removes noise spikes from this power feed. The upper op-amp and optocoupler provide the main voltage regulation. The 2k pot sets the feedback voltage at 2.4 volts, for a 5 volt output. The .1μF cap is a spike filter. The positive input of the op-amp is referenced to the 2.4 volt zener. The op-amp runs at full open loop gain for DC and the .1μF from the negative input to the output forms compensation along with the 1k input resistor. The op-amp output drives the LED of the optocoupler. The lower op-amp and optocoupler are for overvoltage protection. The lower 2k pot sets the trip point. The circuitry is similar to the voltage feedback circuit described above, but the compensation capacitor is substituted by a 100k feedback resistor to limit the gain. Any dual or quad op-amp, swinging to within .8 volts of either supply while operating at 5 volts, can be used.

The phototransistor side of the voltage feedback optocoupler is powered by +15V and supplies its output via a 620 ohm load resistor. This voltage is applied to the Am6301 op-amp, connected as an inverting amplifier, with flat gain and no compensation. The noninverting input (pin 17) is held at +2.5V reference (pin 2). The loop will serve the output so that the LED current through the 620 ohm load generates a voltage of 2.5 volts.

The overvoltage optocoupler has a 4.7k load and goes directly to the overvoltage input on the Am6301 (pin 21). When the output reaches the trip point set on the 2k pot, the LED turns on the phototransistor, raising pin 21 from 0 to +15V, triggering the Am6301 into its protection mode.

The 165 volt bus is applied to a divider chain formed by the 39k, 12k, 2k pot and 470 ohm resistors. The 2k pot sets the input undervoltage trip point and its output goes to the Am6301 pin 19. When this point reaches below 2.5 volts, the IC shuts down. The same divider provides a 45 volt attenuated output to the 1 Meg pot and the 220k, which give feedforward current into the ramp terminal (pin 12) of the IC. This reduces 120Hz ripple on the output and allows use of a smaller filter capacitor on the 165V bus.

The push-pull outputs of the Am6301, on pins 4 and 15, are pulled up to +15V by 2.2k load resistors. This drives the inputs of a CMOS hex buffer. The three paralleled gates per side give fast rise drive waves to the 800pF load, presented by the power FET gates.

Dynamic current limiting is obtained by sampling the FET source currents with a .15 ohm sense resistor. This signal is filtered by the 100 ohm/.01μF network and applied to the dynamic limit (pin 22) of the Am6301. The current limit is set by the 200 ohm pot on the 2.5 volt reference. This is adjusted so that the output short circuit current is limited to 25 amps.

Any asymmetry in the voltage or timing of the transformer input will result in a net DC flux, which will tend to saturate the transformer and cause high peak currents in one of the FETs. It is prevented here by using the current sense voltage as an additional input to the feedback op-amp. The .05μF capacitor and 1k series resistor connect spike filtered current sense voltage at pin 22 to the op-amp summing point at pin 16. The RC input network combined with the 5.6k feedback resistor, tailor the response so that it is rolled off below 3kHz and has no effect in the low frequency range, where the voltage feedback loop is operating. At the 25kHz switching frequency, the current sense loop has a gain of −5.6. The result is to superimpose a −1.25 volt pulse on the control voltage at the op-amp output. For equal currents, this has no effect on the pulse widths. If one side has greater current, the pulse goes more negative, causing the PWM circuitry to shorten that pulse and reduce the current to that side. The effect generates unequal drive pulse widths, reducing the current unbalance to zero and equalizing the volt-second product on each winding.

5 Volt 100 Watt Line Operated Supply

Figure 1

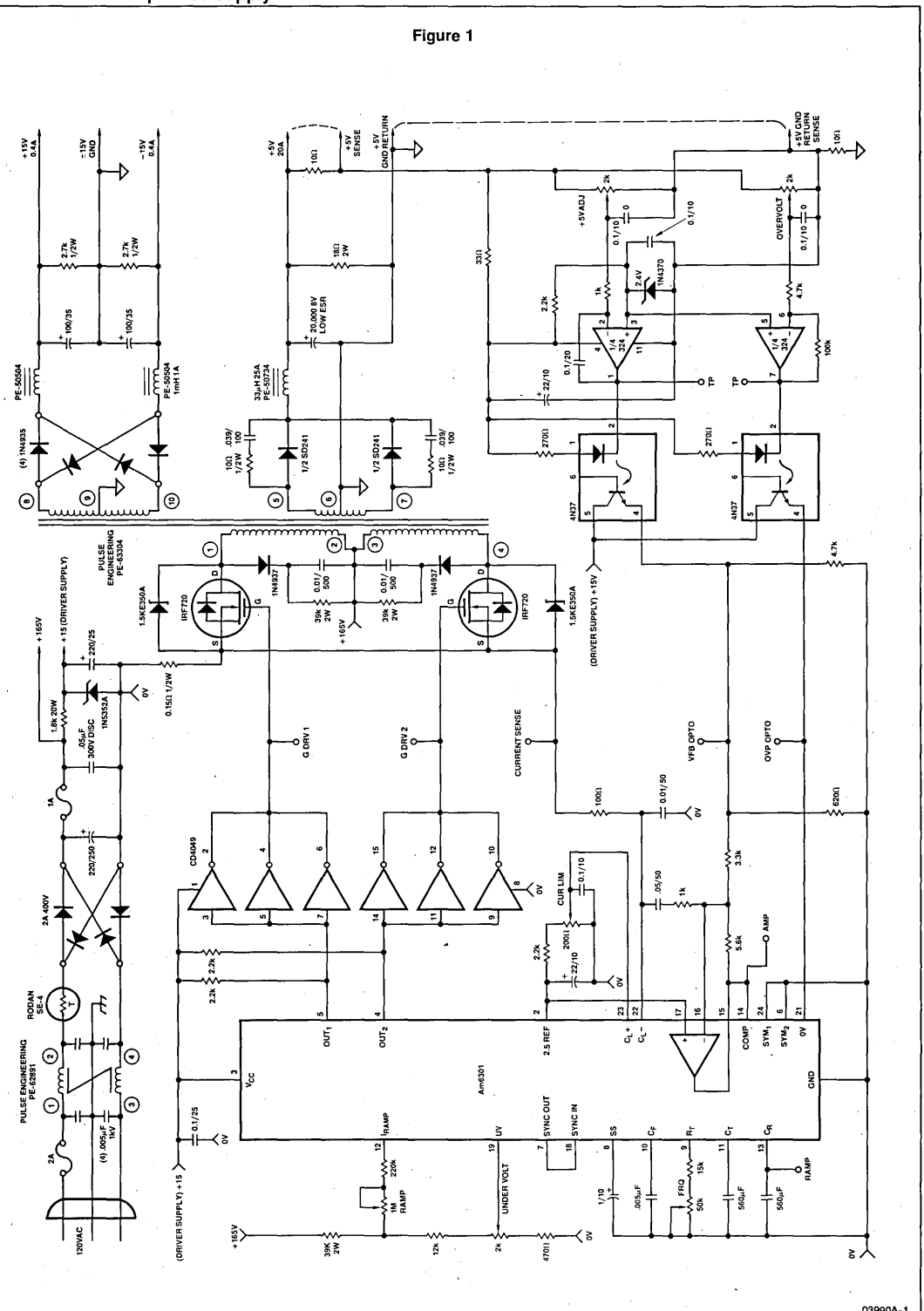


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Figure 2. DC Bus Efficiency

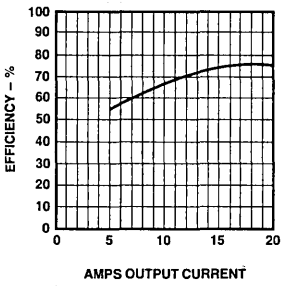


Figure 3. Ripple

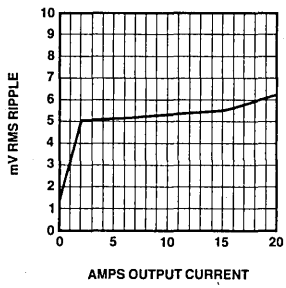
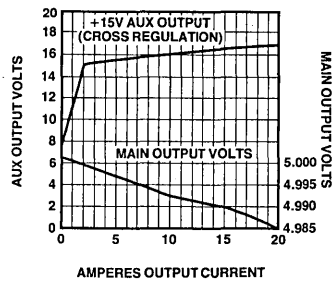


Figure 4.



PERFORMANCE DATA

Figure 2 is a graph of efficiency vs main output current from 0 to full load. Efficiency, measured at 115V line and from the DC bus, was 66% at half load, rising to 73% at full load. If the drive supply zener power is not included, power efficiency is 78%. The drive circuitry actually consumes only 0.81 watts at 15 volts, so a separate drive supply would save considerable power over the zener shown here.

Figure 3 is a graph of RMS ripple, note the low ripple at full load. Ripple is 6mVRMS maximum at full load off a 115V line.

Figure 4 is a graph of main and auxiliary output regulation vs load. Note the slow linear change in auxiliary output with main output current. The ±15 volt outputs fall to 7 volts if there is no load on the main output but stay within 2 volts in a 10-100% main output load range. Main output regulation is 0.32% no load to full load and only 0.02% total from 92 to 130 volts line.

SCOPE PHOTOS

I. FET Switching 20 Amp (Full Load)

#1 – Top – V_{DRAIN} 100V/cm
Bottom – V_{GATE} 10V/cm
Time 5μs/cm

Note 300V peak stress on FET and 120Hz modulation of turn off time due to feedforward.

#2 – Turn off
Top – V_{DRAIN} 100V/cm
Bottom – V_{GATE} 10V/cm
Time 100ns/cm

Note 30ns risetime.

#3 – Turn on
Top – V_{DRAIN} 100V/cm
Bottom – V_{GATE} 10V/cm
Time 100ns/cm

Note plateau in gate wave, 30ns turn on fall time.

#4 – Both FET drains, and sum of both FET currents
Top – Drain #1 100V/cm
Middle – Drain #2 100V/cm
Bottom – Current 1A/cm
Time – 5μs/cm

Note equal currents, small magnetizing current, clean switching waves.

II. Dynamic Symmetry Correction (S.C.)

#5 – Conditions: Full load, 5Ω resistor inserted in series with one FET drain to cause severe unbalance.
Top – Sum of drain currents, No S.C. 1A/cm
Next – Op-amp output, 1V/cm, No S.C.
Next – Sum of drain currents, with S.C. 1A/cm
Bottom – Op-amp output, 1V/cm, with S.C.
Time – 10μs/cm

Note perfect symmetry in lower current trace.

#6 – Ramp and Control Voltage, No S.C. (Superimposed) 1V/cm, 2μs/cm

#7 – Ramp and Control Voltage with S.C. (Superimposed) 1V/cm, 2μs/cm

III. Feedforward

Conditions for all photos: 115V line, 20A load

#8 – Output
Top Trace: – 5V Ripple, AC coupled with feedforward 20mV/cm
Bottom Trace – 5V ripple, AC coupled without feedforward 20mV/cm
Time – 2ms/cm, line sync

Note improvement in 120Hz ripple by a factor of 8 (18dB), with no change in 25kHz ripple.

#9 – Ramp, Oscillator Sync
Top Trace – Ramp, pin 13 with feedforward 2V/cm

Note variable slope and amplitude of ramp as it varies with the 120Hz ripple. "Notch" shows comparison point, at constant control voltage and varying pulse width.

Bottom Trace – Ramp, pin 13 without feedforward 2V/cm
Time – 5μsec/cm

Note fixed ramp slope and amplitude. Comparison point (shown by transients) is moving on the ramp at the 120Hz ripple rate.

#10 – Ramp, Line Sync
Top Trace – Ramp pin 13 with feedforward, 2V/cm

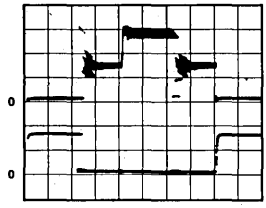
Note variable amplitude at ripple rate, and fixed comparison point amplitude.

Bottom Trace – Ramp, pin 13 without feedforward, 2V/cm

Note fixed amplitude and comparison point varying at ripple rate.

5 Volt 100 Watt Line Operated Supply

I. FET Switching 20 Amp (Full Load)



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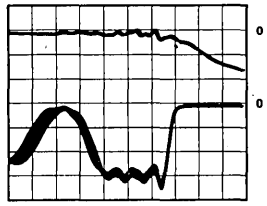

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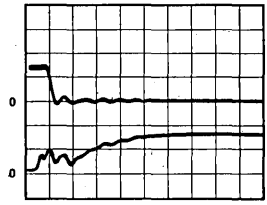

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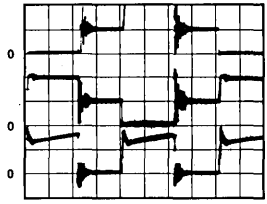
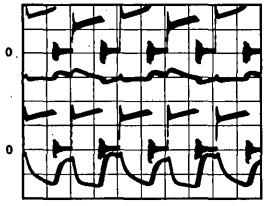
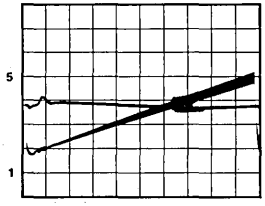


4 03990A-8

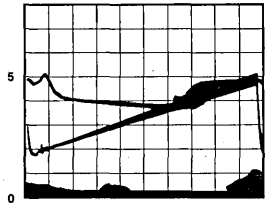
II. Dynamic Symmetry Correction (S.C.)



5 03990A-9

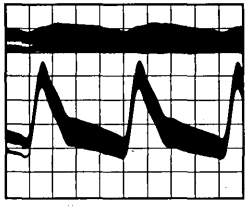


6 03990A-10

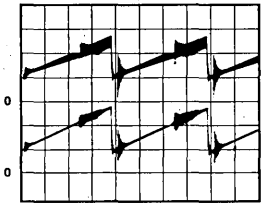


7 03990A-11

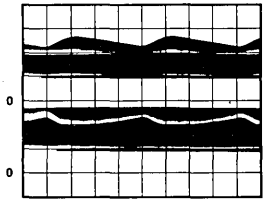
III. Feedforward



8 03990A-12



9 03990A-13



10 03990A-14

Testing of Feed-Forward Control

The effect of feed-forward control can be observed by constructing a simple power supply with switches to control the feed-forward and feedback circuits.

In Figure 1, the feed-forward switch selects either R_1 which is connected to the input voltage or R_2 which is connected to V_{REF}. The feedback switch connects the PWM input to either the error amplifier output (pin 14) or to an external DC voltage source. R_T and C_T are selected from the tables in the Am6301 data sheet. C_R is made equal to C_T so that R_1 and R_2 can be calculated:

$$R_1\ (\Omega) = R_T \cdot [V_{IN}(pk) - 0.7V] - (4 \times 10^3)$$
$$R_2\ (\Omega) = R_T \cdot [1.8V] - (4 \times 10^3)$$

This circuit can be run in four modes depending on the positions of the two switches.

Mode 1: With both control circuits off, a 20% ripple on V_{IN} will cause a 20% ripple on V_{OUT}.

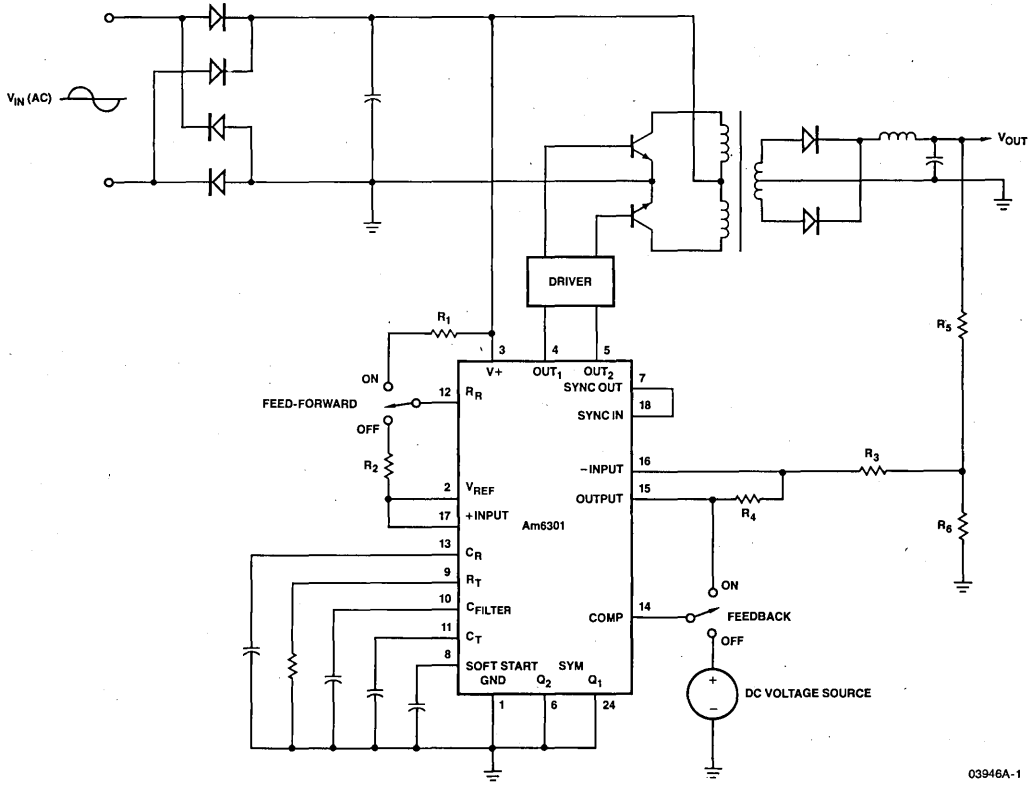
Mode 2: Using feedback only, the output ripple equals the V_{IN} ripple divided by the error amplifier gain. Therefore, an error amplifier gain of 20 will reduce the output ripple to 1/20th of the input ripple.

Mode 3: In the feed-forward only mode, there is no noticeable ripple occuring on the output.

Mode 4: With both control circuits on, the mode slightly improves the line regulation.

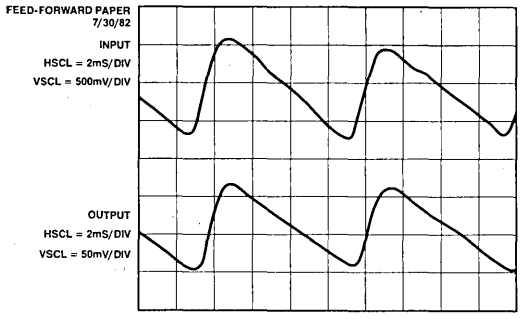
The following four plots show the amount of output ripple in the corresponding four modes described above. The circuit used is shown in Figure 1 with the feedback gain intentionally set to a low value to make the effect of low feedback gain noticeable. Note that no adjustments to the feed-forward circuit were necessary other than power selection of R_1.

The difference in line regulation between Mode 1 and Mode 4 is approximately 26db. This implies that the input filter capacitor used in a Mode 1 implementation could be reduced by a factor of 10 in a Mode 4 circuit and have better line regulation than the original circuit. This represents a considerable reduction in the cost, size and weight of the power supply through advanced circuit design techniques.



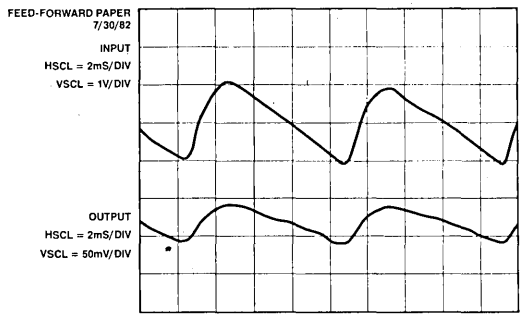
Testing of Feed-Forward Control

Plot 1



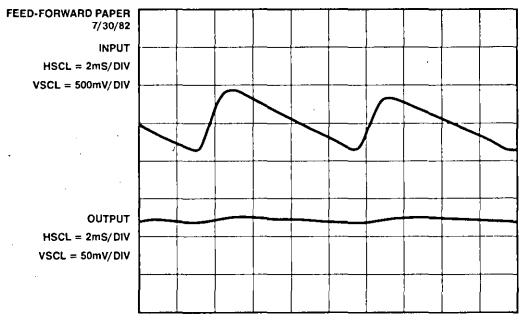
03946A-2

Plot 2



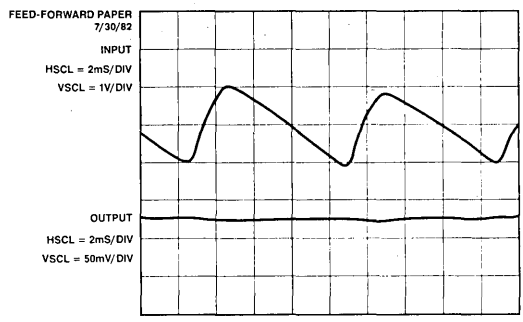
03946A-3

Plot 3



03946A-4

Plot 4



03946A-5

Symmetry Correction

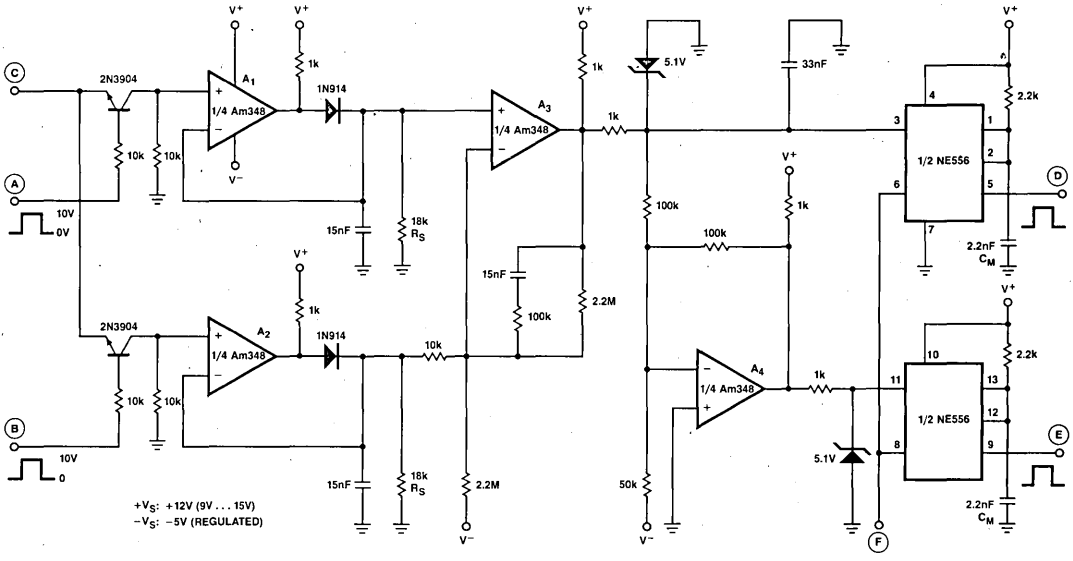
In push-pull and full-bridge switched mode power supplies, variations in switch speeds or transformer windings can cause a condition known as transformer unbalance, which in turn can cause a difference in primary current on opposite half cycles. Because the primary transformer windings are wound in opposite directions, this difference is added to the transformer flux in one direction and subtracted from it in the opposite direction. The result is a DC component in the transformer flux. This drives the transformer closer to the saturation in one direction than in the opposite direction.

Transformer saturation must be prevented to protect the switch transistors from the current spikes that will occur as a result of the effective zero impedance of a saturated inductor. This problem is most often solved by either over-designing the power transformer or by connecting a large DC blocking capacitor in series with the transformer primary. Both of these solutions increase parts cost and board space. The most common solution, the blocking capacitor, is especially large and expensive because of the high breakdown voltage and high capacitance necessary. A circuit to adjust the output ON times individually to correct unbalances could save cost and space in a push-pull SMPS.

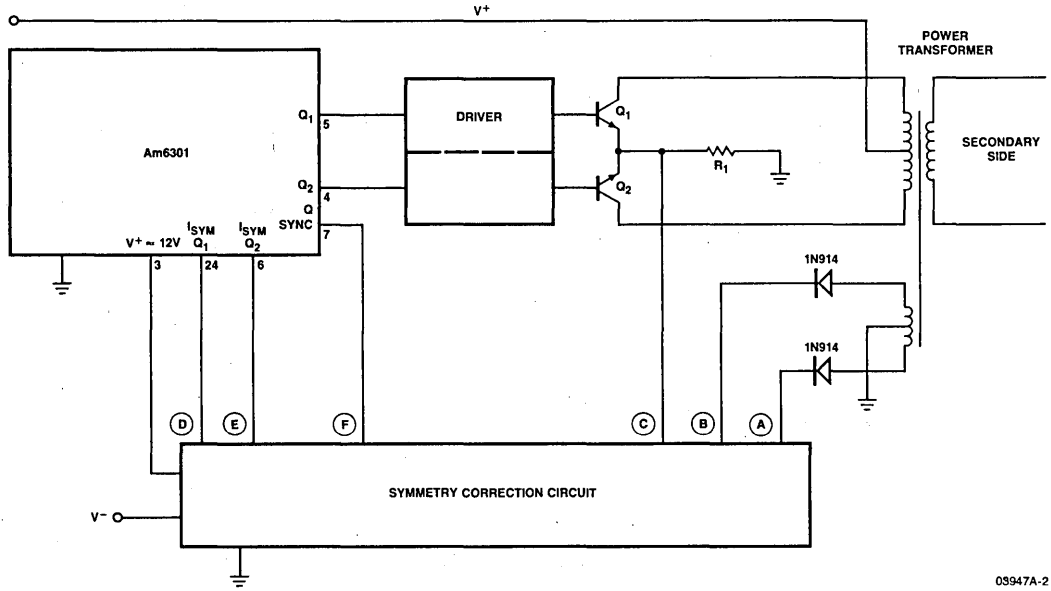
Because it offers one additional input to each output AND gate, SYM Q_1 and SYM Q_2, the Am6301 can be interfaced to an unbalance correction circuit (Figures 5 and 6). The bases of two 2N3904 switching transistors, are driven by an additional winding of the transformer so that the two peak detection circuits (A_1 and A_2) are switched on in phase with the power transistors, T_1 and T_2. These peak detectors store the peak primary currents associated with the push-pull windings. The difference between these currents is amplified by A_3, and used as a control voltage to a monostable multivibrator. The output of A_3 is inverted by unity gain amplifier A_4, and used as the control voltage to a second monostable multivibrator. When a transformer imbalance occurs, correction pulses generated by the control circuit at D and E delay the beginning of one Am6301 output pulse more than the other. The resulting asymmetrical duty cycle corrects the unbalance condition. Component values shown are for 50kHz operation, the values of R_S and C_M must be changed for other frequencies R_S can be found from the formula:

$$R_S = \frac{9}{\text{frequency} \times 0.15\text{nF}}$$

The selection of C_M should be done experimentally. Choose C_M so that the monostable output pulse width is approximately half of the desired correction range when the A_1 output is equal to the A_2 output. Because only two inexpensive ICs are used, system parts cost is not increased significantly.



Symmetry Correction



Networking – Section VIII

System Overview

Advanced Micro Devices is introducing a set of LSI devices that provides the Ethernet system designer, and designers of Ethernet compatible products, a low cost physical and link level interface to the Ethernet Bus.

The Am7990 Ethernet interface family is being designed using a combination of MOS and IMOX™ bipolar technologies. This family consists of the Am7990 Local Area Network Controller for Ethernet (LANCE), and the Am7991 Serial Interface Adapter (SIA). As shown in Figure 1, the Am7990 family provides the complete interface between the device System Bus and the Ethernet Transceiver Cable.

The Am7990 LANCE is a 10M-bit/sec MOS device in a 48-pin package, optimized to perform the link level Ethernet protocol. The CSMA/CD network access, memory management (onboard DMA), error reporting, packet handling, and microprocessor interface functions also reside in the LANCE.

The Am7991 Serial Interface Adaptor provides Manchester encoding and decoding of the serial bit stream and interfaces the TTL output of the LANCE to the differential inputs of the transceiver. It has an on board phase locked loop to recover clock from an incoming signal and can use an external crystal oscillator or TTL inputs to provide clock for transmission.

Coupling the Ethernet Node to the Ethernet Cable requires a transceiver. Commercially available board or module transceivers can be used with the LANCE and SIA. Advanced Micro Devices has a monolithic transceiver in an early phase of development which should lower the cost significantly in this area as well.

BASIC SYSTEM OPERATION

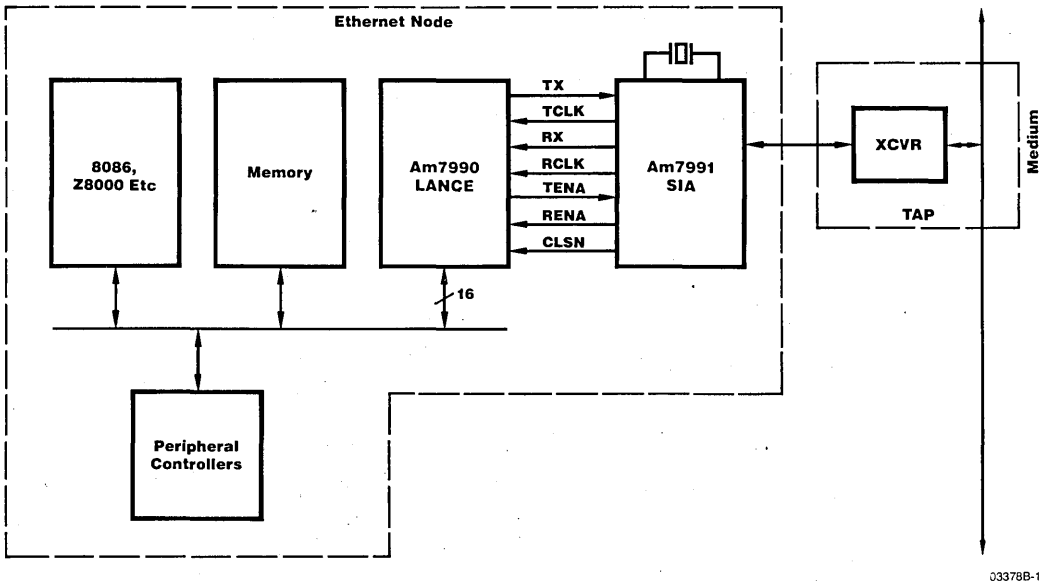
Ethernet is a send and receive half duplex system. The node must function in either transmit or receive mode at any instant in time. Before transmission the node must be sure there is no contention for the bus. The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two nodes attempt to transmit at the same time, the signals will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit and detect the collision. Both continue to transmit for a predetermined length of time to "jam" the network, insuring all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm implemented in the LANCE, before attempting to transmit again. This minimizes the possibility of collision on retransmission.

TRANSMIT MODE

In the transmit mode, the LANCE initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with a preamble, and sync pattern then calculates and appends a 32-bit CRC.

This packet is transmitted serially to the SIA. The Manchester encoder in the SIA takes the transmitted data from the LANCE and creates the Manchester encoded differential signals TRANSMIT+ and TRANSMIT− to drive the Transceiver cable. These differential signals are coupled through the transceiver cable, transceiver and on to the Ethernet coaxial cable.

Figure 1. Ethernet Node Architecture



IMOX is a trademark of Advanced Micro Devices, Inc.

RECEIVE MODE

When carrier is present on the Ethernet coax, the Transceiver will create the differential signals RECEIVE+ and RECEIVE−. These inputs to the SIA are decoded by the Manchester decoder. A phase locked loop synchronizes to the Ethernet Preamble, allowing the decoder to recover clock and data from the encoded signals. These two signals are supplied to the LANCE as the TTL signals RECEIVE DATA and RECEIVE CLOCK. In addition, the SIA creates the signal CARRIER PRESENT while it is receiving data from the cable, indicating to the LANCE that receive data and clock are available. When these signals reach the LANCE, the CRC is calculated and compared to the CRC checksum at the end of the packet. If the calculated CRC doesn't agree with the packet CRC an error bit is set and an interrupt generated to the microprocessor.

ADDRESSING

There are three addressing modes. The first is physical addressing which requires a comparison of the 48-bit destination address in the packet with the node address programmed into the LANCE during initialization. The second mode is multi-cast addressing. This mode can be useful when sending packets to all of one type of a device simultaneously on the network, or for a broadcast situation where all nodes on the network receive the packet. In the final "promiscuous" mode of operation, a node will accept all packets on the coax regardless of their destination address.

ERROR REPORTING

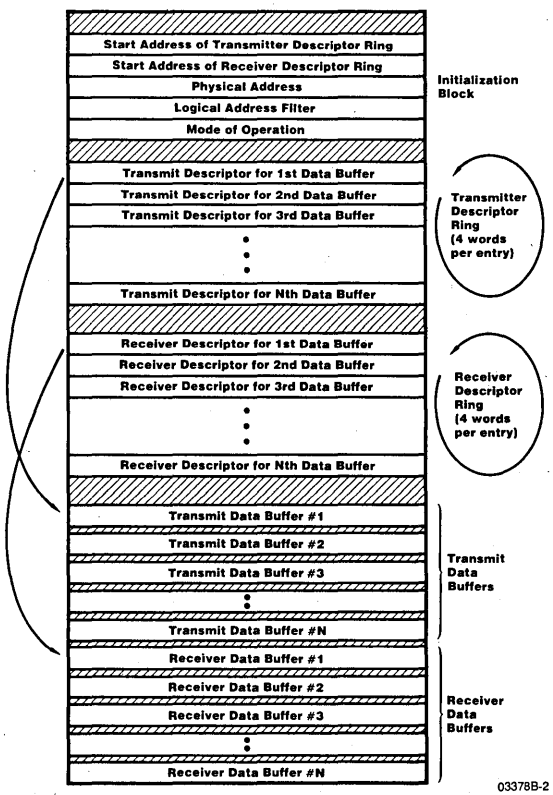
Extensive error reporting is provided by the LANCE through microprocessor interrupt and error bits in a status register. The following are the significant error conditions:

- CRC error on receive
- Babbling error
- Missed packet
- Memory error

BUFFER MANAGEMENT

A key feature of the LANCE and it's on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management consists of circular task queues called descriptor rings for transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring awaiting execution by the LANCE. (Figure 2)

Figure 2. LANCE/Processor Memory Interface



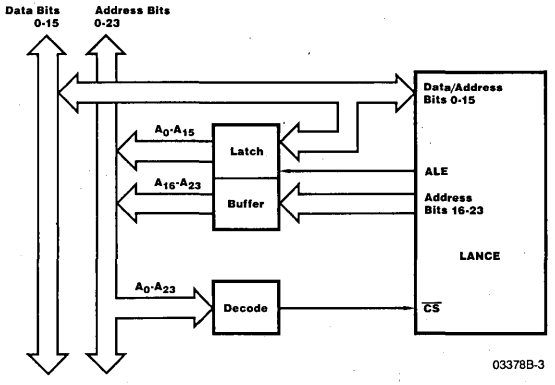
MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the 68000, Z8000*, 8086, and LSI-11** devices.

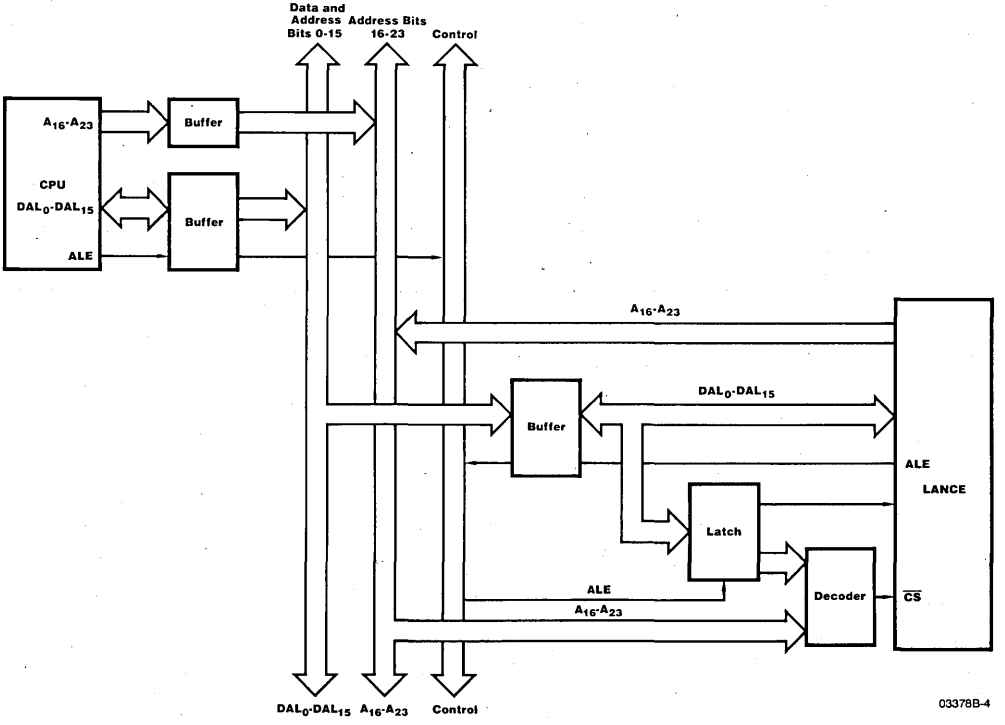
The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. The LANCE interfaces with both multiplexed and demultiplexed data busses (Figure 3) and features control signals for address/data bus transceivers.

Figure 3.

a) Demultiplexed Bus



b) Multiplexed Bus System Overview



*Z8000 is a trademark of Zilog, Inc.

**LSI-11 is a registered trademark of Digital Equipment Corp.

Am7990

Local Area Network Controller for Ethernet (LANCE)

IN DEVELOPMENT

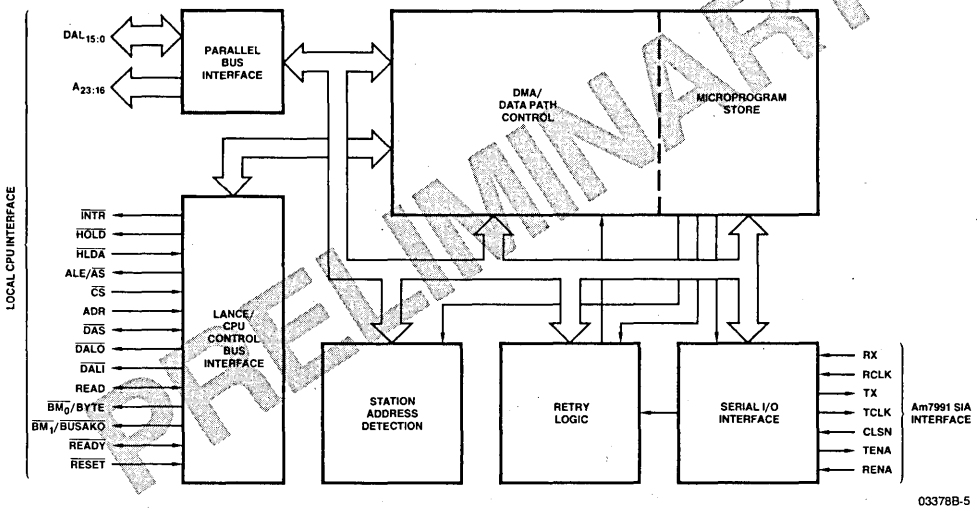
DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet specifications
- Easily interfaced to 8086, 68000, Z8000, LSI-11 microprocessors
- On-board DMA and buffer management
- 24-bit wide linear addressing (Bus Master Mode)
- Network and packet error reporting
- Diagnostic Routines
  - Internal/external loop back
  - CRC logic check
  - Time domain reflectometer
- 48-pin DIP
- Single +5V power supply

GENERAL DESCRIPTION

The Am7990 Local Area Network Controller for Ethernet (LANCE) is a 48-pin VLSI device designed to greatly simplify interfacing a microcomputer or minicomputer to an Ethernet Local Area Network. This chip, in conjunction with the Am7991 Serial Interface Adapter (SIA) and closely coupled local memory and microprocessor, is intended to provide the user with a complete interface module for an Ethernet network. The Am7990 is designed using a scaled N-Channel MOS technology and is compatible with a variety of microprocessors. On-board DMA, advanced buffer management and extensive error reporting and diagnostics facilitate design and improve system performance.

LANCE BLOCK DIAGRAM



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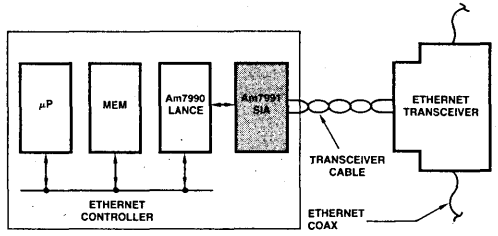
TYPICAL ETHERNET NODE



03378B-6

PIN DEFINITIONS

DAL_{00}–DAL_{15} **Data/Address Lines (Input/Output 3-State).** The time multiplexed Address/Data bus. During the address portion of a memory transfer, DAL_{00}–DAL_{15} contains the lower 16 bits of the memory address. The upper 8 bits of address are contained in A_{16}–A_{23}.

During the data portion of a memory transfer, DAL_{00}–DAL_{15} contains the read or write data, depending on the type of transfer.

The LANCE drives these lines as a Bus Master and as a Bus Slave.

A_{16}–A_{23} **High Order Address Bus (Output 3-State).** The additional address bits necessary to extend the DAL lines to access a 24-bit address. These lines are driven as a Bus Master only.

READ **(Input/Output 3-State).** Indicates the type of operation to be performed in the current bus cycle. This signal is an output when the LANCE is a Bus Master.

High – Data is taken off the DAL by the chip

Low – Data is placed on the DAL by the chip

The signal is an input when the LANCE is a Bus Slave

High – Data is placed on the DAL by the chip

Low – Data is taken off the DAL by the chip

$\overline{BM_0}$/BYTE **$\overline{BM_0}$, $\overline{BM_1}$ Byte Mask (Output).** Pins 15 and 16 are programmable through bit (00) of CSR_3.

$\overline{BM_1}$/$\overline{BUSAKO}$ Asserting $\overline{RESET}$ clears CSR_3.

If CSR_3 (00) BCON = 0
I/O pin 16 = $\overline{BM_1}$ (Output 3-state)
I/O pin 15 = $\overline{BM_0}$ (Output 3-state)

If CSR_3 (00) BCON = 1
I/O pin 16 = $\overline{BUSAKO}$ (Output 3-state)
I/O pin 15 = Byte (Output 3-state)

$\overline{BM_0}$, $\overline{BM_1}$ Byte Mask. Indicates the byte(s) on the DAL to be read or written during this bus transaction. The LANCE drives these lines only as a Bus Master. The chip ignores the Byte Mask lines when it is a Bus Slave and assumes word transfers.

Byte selection is done as outlined in the following table.

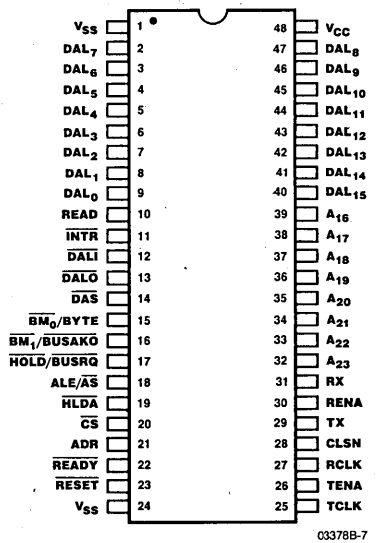
CSR_3 (00) BCON = 0

BM_1	BM_0	
LOW	LOW	Whole word
LOW	HIGH	Upper byte
HIGH	LOW	Lower byte
HIGH	HIGH	None

BYTE An alternate byte selection line. Byte selection is done using the BYTE line and DAL_{00} line, latched during the address portion of the bus transaction. The chip drives BYTE only as a Bus Master and ignores it when a Bus Slave selection is done, (similar to $\overline{BM_0}$, $\overline{BM_1}$).

There are two modes of ordering bytes dependent on bit 02 of CSR_3 (BSWP). This programmable ordering of upper and lower bytes is necessary for compatibility with the various 16-bit microprocessors.

LANCE PIN DESCRIPTION
D-48-1



03378B-7

Note: Pin 1 is marked for orientation.

$\overline{BUSAKO}$ is a bus request daisy chain output. If the chip is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If the LANCE was requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high.

Mode Bits / Signal Line	BSWP = 0 and BCON = 1	BSWP = 1 and BCON = 1
BYTE = L and DAL_{00} = L	Word	Word
BYTE = L and DAL_{00} = H	Illegal	Illegal
BYTE = H and DAL_{00} = H	Upper Byte	Lower Byte
BYTE = H and DAL_{00} = L	Lower Byte	Upper Byte

$\overline{CS}$ **Chip Select (Input).** Indicates, when asserted, that the LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR **Register Address Port Select (Input).** When LANCE is slave, ADR indicates which of the two register ports is selected. ADR LOW selects register data port, ADR HIGH selects register address port. ADR must be valid throughout the data portion of the bus cycle and is only used by the LANCE when CS is low.

ALE/$\overline{AS}$ **Address Latch Enable (Output 3-State).** Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR_3.

8

As ALE, (CSR_3 (01), ACON = 0) the signal transitions from a HIGH to a LOW during the address portion of the transfer and remains low during the data portion. ALE can be used by a Slave device to control a latch on the bus address lines. When ALE is high the latch is open and when ALE goes low the latch is closed.

As $\overline{AS}$ (CSR_3 (01), ACON = 1), the signal pulses LOW during the address portion of the bus transaction. The low to high transition of AS can be used by a slave device to strobe the address into a register.

The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master.

$\overline{DAS}$ **Data Strobe (Input/Output 3-State).** Defines the data portion of the bus transaction. $\overline{DAS}$ is high during the address portion of a bus transaction and low during the data portion. The low to high transition can be used by a Slave device to strobe bus data into a register. $\overline{DAS}$ is driven only as a Bus Master.

$\overline{DALO}$ **Data/Address Line Out (Output 3-State).** An external bus transceiver control line. $\overline{DALO}$ is asserted when the LANCE drives the DAL lines. $\overline{DALO}$ will be low only during the address portion if the transfer is a READ. It will be low for the entire transfer if the transfer is a WRITE. $\overline{DALO}$ is driven only when LANCE is a Bus Master.

$\overline{DALI}$ **Data/Address Line In (Output 3-State).** An external bus transceiver control line. $\overline{DALI}$ is asserted when the LANCE reads from the DAL lines. It will be low during the data portion of a READ transfer and remain high for the entire transfer if it is a WRITE. $\overline{DALI}$ is driven only when LANCE is a Bus Master.

$\overline{HOLD}$/$\overline{BUSRQ}$ **Bus Hold Request (Output Open Drain).** Asserted by the LANCE when if requires access to memory. $\overline{HOLD}$ is held LOW for the entire ensuing bus transaction. The function of this pin is programmed through bit (00) of CSR_3. Bit (00) of CSR_3 is cleared when $\overline{RESET}$ is asserted.

When CSR_3 (00) BCON = 0

I/O pin 17 = $\overline{HOLD}$ (Output Open Drain)

When CSR_3 (00) BCON = 1

I/O pin 17 = $\overline{BUSRQ}$ (Output Open Drain)

$\overline{BUSRQ}$ will be asserted only if I/O pin 17 is high prior to assertion.

$\overline{HLDA}$ **Bus Hold Acknowledge (Input).** A response to $\overline{HOLD}$. When $\overline{HLDA}$ is low in response to the chip's assertion of $\overline{HOLD}$, the chip is the Bus Master. $\overline{HLDA}$ deasserts upon the deassertion of $\overline{HOLD}$.

$\overline{INTR}$ **Interrupt (Output Open Drain).** An attention signal that indicates, when active, that one or more of the following CSR_0 status flags is set: BABL, MERR, MISS, RINT, TINT or IDON. $\overline{INTR}$ is enabled by bit 06 of CSR_0 (INEA = 1).

RX **Receive (Input).** Receive Input Bit Stream.

TX **Transmit (Output).** Transmit Output Bit Stream.

TENA **Transmit Enable (Output).** Transmit Output Bit Stream enable. A level asserted with the Transmit Output Bit Stream, TX, to enable the external transmit logic.

RCLK **Receive Clock (Input).** A 10MHz square wave synchronized to the Receive data and only active while receiving an Input Bit Stream.

CLSN **Collision (Input).** A logical input that indicates that a collision is occurring on the channel.

RENA **Receive Enable (Input).** A logical input that indicates the presence of carrier on the channel.

TCLK **Transmit Clock (Input).** 10MHz clock.

$\overline{READY}$ **(Input/Output Open Drain).** When the LANCE is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that it will accept data if a WRITE or has put data on the DAL lines if a READ. As a Bus Master it is an input and as a Bus Slave an output. $\overline{READY}$ is a response to $\overline{DAS}$ and will return high after $\overline{DAS}$ has gone high.

$\overline{RESET}$ **(Input).** Bus Reset Signal. Causes the LANCE to cease operation and enter an idle state.

V_{CC} Power supply pin +5 volts ± 5%.

V_{SS} Ground.

FUNCTIONAL DESCRIPTION

The parallel interface of the Local Area Network Controller for Ethernet (LANCE) has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: Z8000, 8086, 68000 and LSI-11. The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. A programmable mode of operation allows byte addressing in one of two ways: A Byte/Word control signal compatible with the 8086 and Z8000, or an Upper Data Strobe and Lower Data Strobe signal compatible with microprocessors such as the 68000. A programmable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

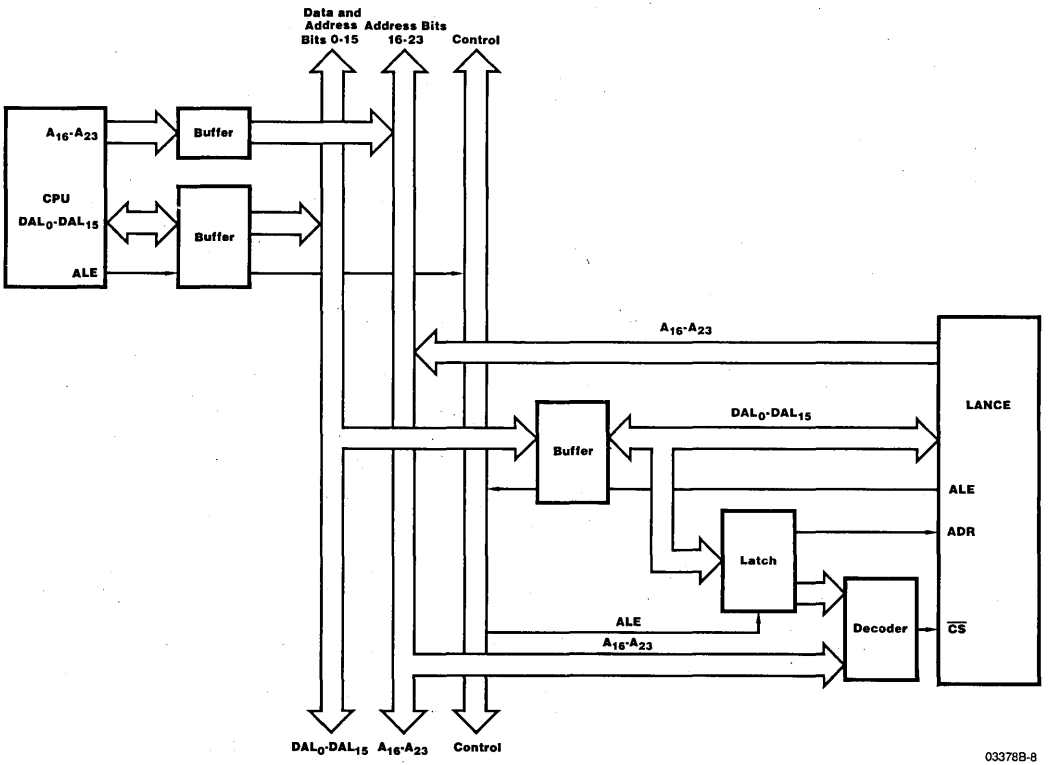
During initialization, the CPU loads the starting address of the initialization block into two internal control registers. The LANCE has four internal control and status registers ($CSR_{0,1,2,3}$) which are used for various functions such as the loading of the initialization block address, different programming modes and status conditions. The host processor communicates with the LANCE during the initialization phase, for demand transmission and periodically to read the status bits following interrupts. All other transfers to and from the memory are handled as DMA under microword control.

Interrupts to the microprocessor are generated by the LANCE: 1) upon completion of its initialization routine, 2) the reception of a packet, 3) the transmission of a packet, 4) transmitter timeout error, 5) a missed packet and 6) memory error.

The cause of the interrupt is ascertained by reading CSR_0. Bit (06) of CSR_0, (INEA) enables or disables interrupts to the microprocessor. In systems where polling is used in place of

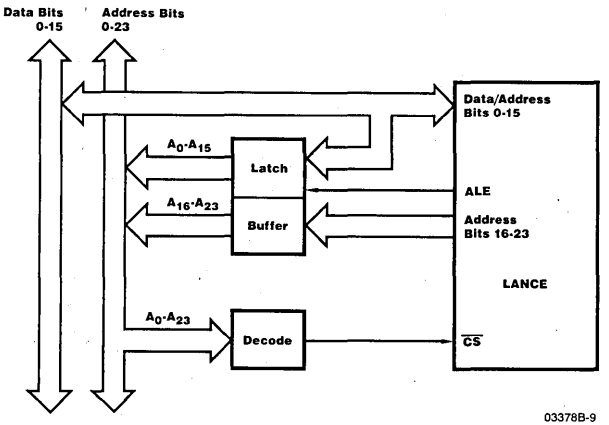
Figure 1. LANCE/CPU Interfacing

a) Multiplexed Bus



03378B-8

b) Demultiplexed Bus



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interrupts, bit (07) of CSR_0 (INTR) indicates an interrupt condition.

The basic operation of the LANCE consists of two distinct modes: transmit and receive. In the transmit mode the LANCE chip directly accesses data in a transmit buffer in memory. It prefaces the data with a preamble, sync pattern, and calculates and appends a 32-bit CRC. This packet is then ready for transmission to the Am7991 SIA.

In the receive mode, packets are sent via the SIA to the LANCE. The packet is loaded into buffer memory. A CRC is calculated and compared with the CRC appended to the data packet. If the calculated CRC checksum doesn't agree with the packet CRC, an error bit is set.

ADDRESSING

Packets can be received using 3 different destination addressing schemes: physical, logical and promiscuous.

The first type is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address, one is group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 63 logical groups. This mode can be useful if sending packets to all of a particular type of device simultaneously (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so-called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

COLLISION DETECTION AND IMPELMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the coax at the same time they will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit; detect the collision, then continue to transmit for a predetermined length of time to "jam" the network and ensure that all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the Ethernet "truncated binary backoff" algorithm in order that the colliding nodes don't try to repeatedly access the network at the same time. Up to 16 attempts to access the network are made by the LANCE before reporting back an error due to excessive collisions.

ERROR REPORTING AND DIAGNOSTICS

Extensive error reporting is provided by the LANCE. Errors conditions reported relate either to the network as a whole or to data packets. Network-related errors are recorded as flags in the CSRs and are examined by the CPU following interrupt. Packet related errors are written into descriptor entries corresponding to the packet.

System errors include:

- Babbling Transmitter
  - Transmitter attempting to transmit more than 1518 data bytes.
- Collision
  - Collision detection circuitry nonfunctional
- Missed packet
  - Insufficient buffer space
- Memory timeout
  - Memory response failure

Packet related errors:

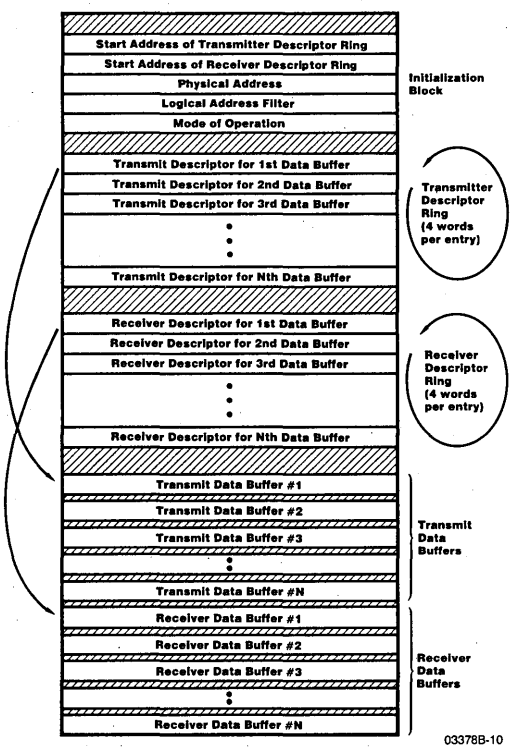
- CRC
  - Invalid data
- Framing
  - Packet did not end on a byte boundary
- Overflow/Underflow
  - Indicates abnormal latency in servicing a DMA request
- Buffer
  - Insufficient buffer space available

The LANCE performs several diagnostic routines which enhance the reliability and integrity of the system. These include a CRC logic check and two loop back modes (internal/external). Errors may be introduced into the system to check error detection logic. A Time Domain Reflectometer is incorporated into the LANCE to aid system designers locate faults in the Ethernet cable. Shorts and opens manifest themselves in reflections which are sensed by the TDR.

BUFFER MANAGEMENT

A key feature of the LANCE and its on-board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings as shown in Figure 2. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an

Figure 2. LANCE/Processor Memory Interface



entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset allowing the host processor to process the data in the buffer.

LANCE INTERFACE

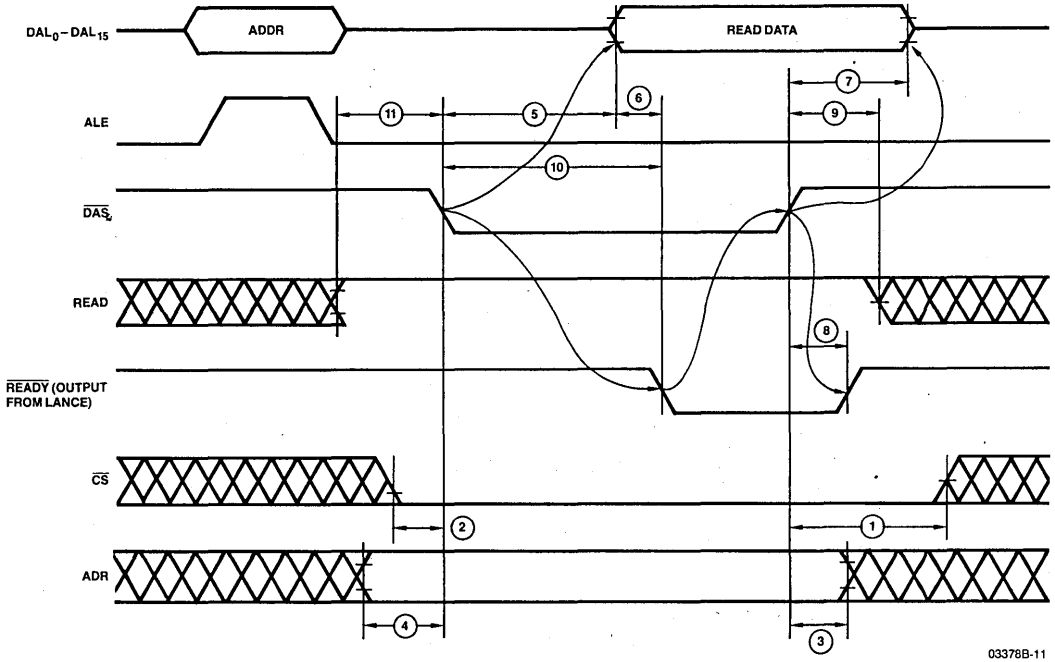
CSR bits such as ACON, BCON and BSWP are used for programming the pin functions used for different interfacing schemes. For example, ACON is used to program the polarity of the Address Strobe signal (ALE/$\overline{AS}$).

BCON is used for programming the pins for handling either the BYTE/$\overline{WORD}$ method for addressing word organized, byte addressable memories where the BYTE signal is decoded along with the least significant address bit to determine upper or lower byte, or an explicit scheme in which two signals labeled as BYTE MASK ($\overline{BM_0}$ and $\overline{BM_1}$) indicate which byte is addressed. When the BYTE scheme is chosen the $\overline{BM_1}$ pin can be used for performing the function $\overline{BUSAKO}$.

BCON is also used to program pins for different DMA modes. In a daisy chain DMA scheme, 3 signals ($\overline{BUSRQ}$, $\overline{HLDA}$, $\overline{BUSAKO}$), are used. In systems using a DMA controller for arbitration, only $\overline{HOLD}$ and $\overline{HLDA}$ are used.

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$ and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600ns in length and can be increased in 100ns increments.

BUS SLAVE READ TIMING



Note: 1. There are two types of delays which depend on which internal register is accessed.
Typ 1 refers to access of CSR_0, CSR_1 and RAP.
Typ 2 refers to access of CSR_1 and CSR_2.

READ SEQUENCE

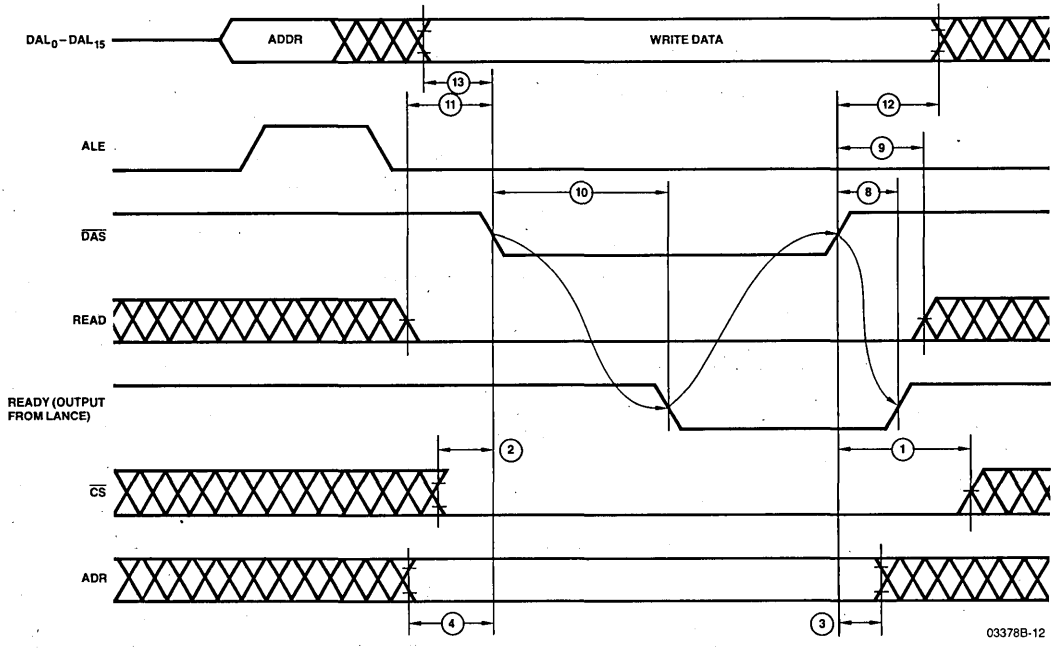
The read cycle is begun by valid addresses being placed on $DAL_{00}-DAL_{15}$ and $A_{16}-A_{23}$. The BYTE MASK signals are placed valid to indicate a word, upper byte or lower byte memory reference and READ indicates the type of cycle. ALE or $\overline{AS}$ are pulsed and the trailing edge of either can be used to latch addresses. $DAL_{00}-DAL_{15}$ go into a 3-state mode and $\overline{DAS}$ falls low to signal the beginning of the memory access. The memory responds by placing $\overline{READY}$ low to indicate that the DAL lines have valid data. The LANCE then latches memory data on the rising edge of $\overline{DAS}$ which in turn ends the memory cycle and $\overline{READY}$ returns high.

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle $\overline{DALO}$ goes inactive before $\overline{DALI}$ becomes active to avoid "spiking" of the bus transceivers.

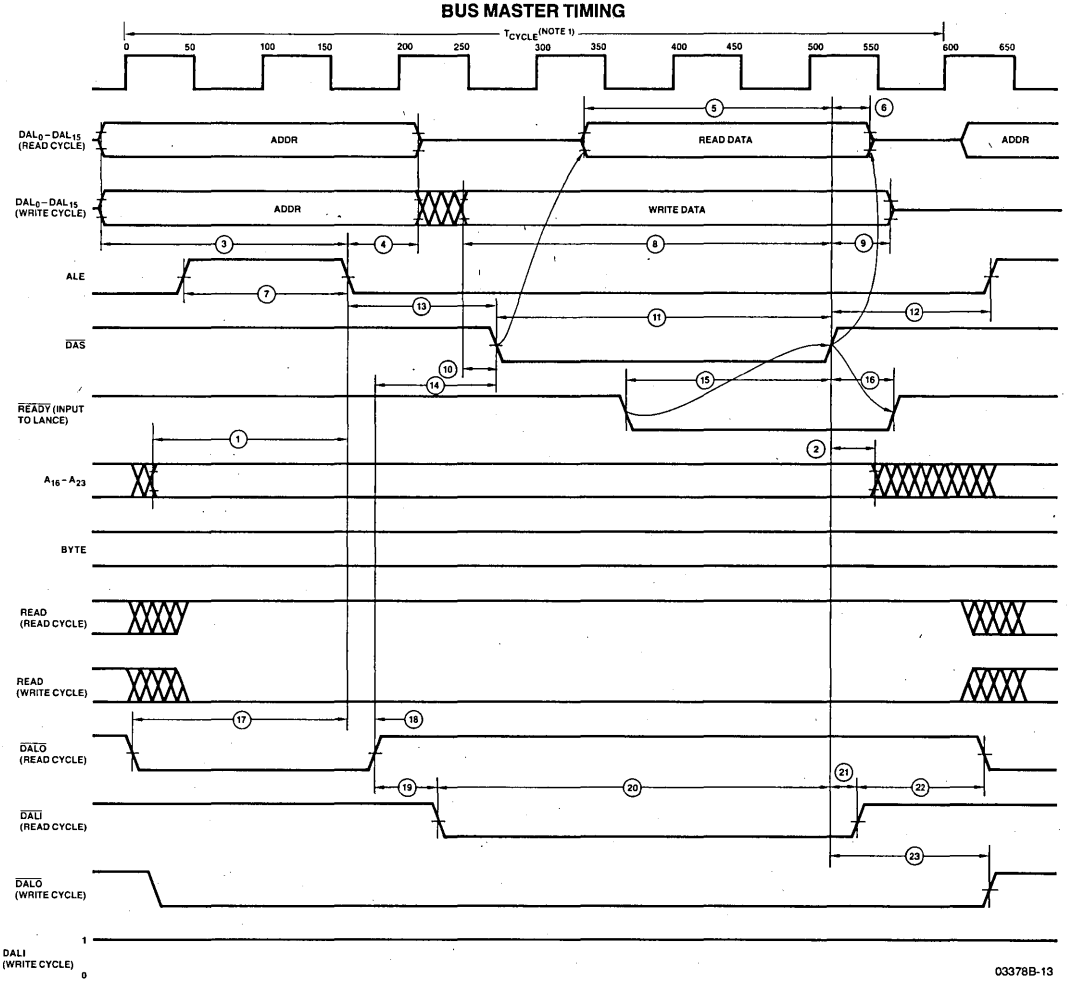
WRITE SEQUENCE

The write cycle is very similar except that the $DAL_{00}-DAL_{15}$ lines change from containing addresses to data after ALE or $\overline{AS}$ go inactive $\overline{DAS}$ goes active after data is valid on the bus. Data to memory is held valid after $\overline{DAS}$ goes inactive.

BUS SLAVE WRITE TIMING

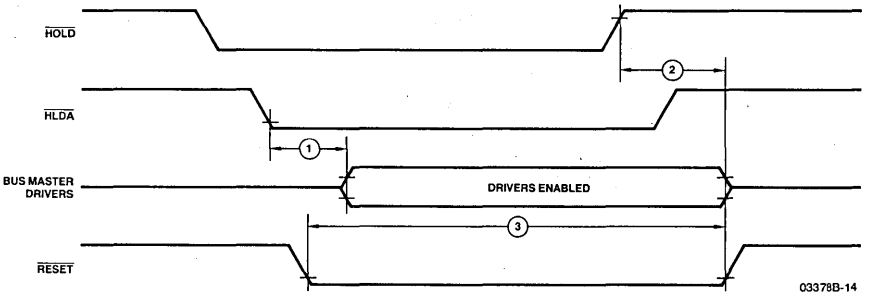


BUS MASTER TIMING



Notes: 1. T_{CYCLE} is the minimum transfer cycle and takes 600ns. Using $\overline{READY}$ it is possible to extend it in multiples of 100ns.
2. The $\overline{READY}$ setup time before negation of DAS is a function of the synchronization time of $\overline{READY}$. This is a critical parameter. The synchronization must occur within two internal clock ticks; 100ns. Therefore, the setup time will be 100ns plus the accumulated propagation delays and the ready slips will occur on 100ns increments.

BUS ACQUISITION TIMING



Note: 1. $\overline{RESET}$ is an asynchronous input to the LANCE and is not part of the Bus Acquisition timing. When $\overline{RESET}$ is asserted, the LANCE becomes a Bus Slave.

PROGRAMMING SPECIFICATION

This section defines the control and Status Registers and the memory data structures required to program the Am7990 (LANCE).

PROGRAMMING THE Am7990 (LANCE)

The Am7990 (LANCE) is designed to operate in an environment that includes close coupling with a local memory and a microprocessor (HOST). The Am7990 LANCE is programmed by a combination of registers and data structures resident within the chip and in memory. There are four Control and Status Registers (CSRs) within the chip which are programmed by the HOST device. Once enabled, the chip has the ability to access memory locations to acquire additional operating parameters.

The Am7990 has the ability to do independent buffer management as well as transfer data packets to and from the Ethernet. There are three memory structures accessed by the Chip:

1. Initialization Block – 12 words in contiguous memory starting on a word boundary. It also contains the operating parameters necessary for device operation. The initialization block is comprised of:
   - Mode of Operation.
   - Physical Address.
   - Logical Address Mask.
   - Location of Receive and Transmit Descriptor Rings.
   - Number of Entries in Receive and Transmit Descriptor Rings.
2. Receive and Transmit Descriptor Rings – Two ring structures, one each for incoming and outgoing packets. Each entry in the rings is 4 words long and each entry must start on a quadword boundary. The Descriptor Rings are comprised of:
   - The address of a data buffer.
   - The length of that data buffer.
   - Status information associated with the buffer.
3. Data Buffers – Contiguous portions of memory reserved for packet buffering. Data buffers may begin on arbitrary byte boundaries.

In general, the programming sequence of the chip may be summarized as:

1. Programming the chip's CSRs by a host device to locate an initialization block in memory. The byte control, byte addressing and address latch enable modes are defined here also.
2. The chip loading itself with the information contained within the initialization block.
3. The chip accessing the descriptor rings for packet handling.

CONTROL AND STATUS REGISTERS

There are four Control and Status Registers (CSRs) resident within the chip. The CSRs are accessed through two bus addressable ports, an address port (RAP) and a data port (RDP).

ACCESSING THE CONTROL AND STATUS REGISTERS

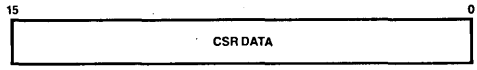
The CSRs are read (or written) in a two step operation. The address of the CSR to be accessed is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP.

Once written, the address in RAP remains unchanged until rewritten.

To distinguish the data port from the address port a discrete I/O pin is provided.

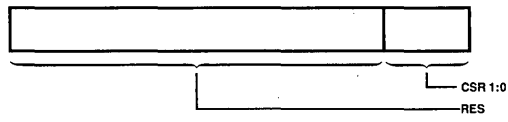
ADR I/O Pin	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

Register Data Port (RDP)



Bit	Name	Description
15:00	CSR Data	Writing data into RDP writes the data into the CSR selected in RAP. Reading the data from the RDP reads the data from the CSR selected in RAP. CSR_1, CSR_2 and CSR_3 are accessible only when the STOP bit of CSR_0 is set. If the STOP bit is not set while attempting to access CSR_1, CSR_2 or CSR_3, the chip will return READY, but a READ operation will return undefined data. WRITE operation is ignored.

Register Address Port (RAP)

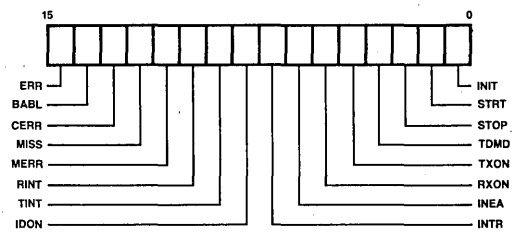


Bit	Name	Description
15:02	RES	Reserved and read as zeroes.
01:00	CSR(1:0)	CSR address select. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET.

CSR(1:0)	CSR
00	CSR_0
01	CSR_1
10	CSR_2
11	CSR_3

CONTROL AND STATUS REGISTER DEFINITION

Control and Status Register 0 (CSR_0)



Bit	Name	Description
15	ERR	ERROR summary is set by the "OR" of BABL, CERR, MISS and MERR. ERR remains set as long as any of the error flags are true. ERR is read only, writing it has no effect. It is cleared by Bus $\overline{\text{RESET}}$, by setting the STOP bit or clearing the individual error flags.
14	BABL	BABBLE is a transmitter timeout error, It indicates that the transmitter has been on the channel longer than the time required to send the maximum length packet. BABL is a flag which indicates excessive length in the transmit buffer. It will be set after 1519 data bytes have been transmitted; the chip will continue to transmit until byte count equals zero unless an interrupt has been generated (INEA = 1). BABL is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
13	CERR	COLLISION ERROR indicates that the collision input to the chip failed to activate within 2μs after a chip initiated transmission was completed. The collision after transmission is a transceiver test feature. CERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
12	MISS	MISSED PACKET is set when the receiver loses a packet because it does not own a receive buffer and the silo has overflowed, indicating loss of data. Silo overflow is not reported because there is no receive ring entry in which to write status. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
11	MERR	MEMORY ERROR is set when the chip is the Bus Master and has not received $\overline{\text{READY}}$ within 25.6μs after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
10	RINT	RECEIVER INTERRUPT is set after the chip updates an entry in the Receive Descriptor Ring. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
09	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the transmit descriptor ring. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
08	IDON	INITIALIZATION DONE indicates that the chip has completed the initialization procedure started by setting the INIT bit. When IDON is set, the chip has read the Initialization Block from memory and stored the new parameters. When IDON is set, an interrupt is generated if INEA = 1. IDON is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
07	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred: BABL, MISS, MERR, RINT, TINT, IDON. If INEA = 1 and INTR = 1, the $\overline{\text{INTR}}$ I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared by RESET or by setting the STOP bit.
06	INEA	INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1, the $\overline{\text{INTR}}$ I/O pin will be low. If INEA = 0, the $\overline{\text{INTR}}$ I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE and cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
05	RXON	RECEIVER ON indicates that the receiver is enabled. RXON is set when STRT is set if DRX = 0 in the

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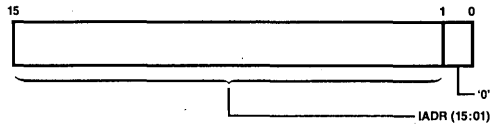
Bit	Name	Description
		MODE register in the initialization block and the initialization block has been read by the chip by setting the INIT bit. RXON is cleared when IDON is set from setting the INIT bit and DRX = 1 in the MODE register or a memory error (MERR) has occurred. RXON is READ ONLY, writing this bit has no effect. RXON is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
04	TXON	TRANSMITTER ON indicates that the transmitter is enabled. TXON is set when STRT is set if DTX = 0 in the MODE register in the initialization block and the INIT bit has been set. TXON is cleared when IDON is set and DTX = 1 in the MODE register or an error has occurred during transmission or a memory error (MERR) has occurred. TXON is READ ONLY, writing this bit has no effect. TXON is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
03	TDMD	TRANSMIT DEMAND, when set, causes the chip to access the Transmit Descriptor Ring without waiting for the polltime interval to elapse. TDMD need not be set to transmit a packet, it merely hastens the chip's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and cleared by the microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit. Writing a "0" in this bit has no effect.
02	STOP	STOP disables the chip from all external activity when set and clears the internal logic. Setting STOP is the equivalent of asserting $\overline{\text{RESET}}$. The chip remains inactive and STOP remains set until the STRT or INIT bit is set. If STRT, INIT and STOP are all set together, STOP will override the other bits and only STOP will be set. STOP is READ/WRITE WITH ONE ONLY and set by RESET. Writing a "0" to this bit has no effect. STOP is cleared by setting either INIT or STRT.
01	STRT	START enables the chip to send and receive packets, perform direct memory access and do buffer management. Setting STRT clears the STOP bit. If STRT and INIT are set together, the INIT function will be executed first.
		STRT is READ/WRITE WITH ONE ONLY. Writing a "0" into this bit has no effect. STRT is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
00	INIT	INITIALIZE, when set, causes the chip to begin the initialization procedure and access the Initialization Block. Setting INIT clears the STOP bit. If STRT and INIT are set together, the INIT function will be executed first. INIT is READ/WRITE WITH "1" ONLY. Writing a "0" into this bit has no effect. INIT is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.

Control and Status Register 1 (CSR_1)

RAP = 1

READ/WRITE: Accessible only when the STOP bit of CSR_0 is a ONE. CSR_1 is unaffected by $\overline{\text{RESET}}$.

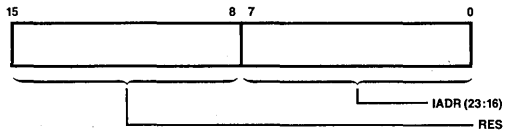


Bit	Name	Description
15:01	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block.
00		Must be zero.

Control and Status Register 2 (CSR_2)

RAP = 2

READ/WRITE: Accessible only when the STOP bit of CSR_0 is a ONE. CSR_2 is unaffected by $\overline{\text{RESET}}$.



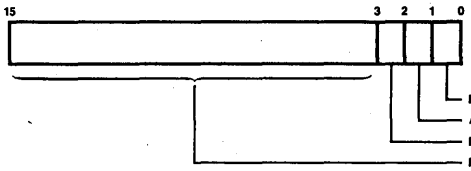
Bit	Name	Description
15:08	RES	Reserved.
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block.

Control and Status Register 3 (CSR_3)

CSR_3 allows redefinition of the Bus Master interface.

RAP = 3

READ/WRITE: Accessible only when the STOP bit of CSR_0 is ONE. CSR_3 is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit in CSR_0.



Bit	Name	Description
15:03	RES	Reserved and read as "0".
02	BSWP	BYTE SWAP allows the chip to operate in systems that consider bits (15:08) to be the least significant byte and bits (07:00) to be the most significant byte. When BSWP = 1, the chip will swap the high and low bytes on DMA data transfers between the silo and bus memory. Only data from silo transfers is swapped, the Initialization Block data and the Descriptor Ring entries are NOT swapped. BSWP is READ/WRITE and cleared by $\overline{\text{RESET}}$ or by setting the STOP bit in CSR_0.
01	ACON	ALE CONTROL defines the assertive state of ALE when the chip is a Bus Master. ACON is READ/WRITE and cleared by $\overline{\text{RESET}}$ and by setting the STOP bit in CSR_0. **ACON ALE** 0 Asserted High 1 Asserted Low
00	BCON	BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by $\overline{\text{RESET}}$ or by setting the STOP bit in CSR_0. **BCON** — **I/O Pin 16** — **I/O Pin 15** — **I/O Pin 17** 0 — $\overline{BM_1}$ — $\overline{BM_0}$ — HOLD 1 — $\overline{\text{BUSAKO}}$ — BYTE — $\overline{\text{BUSRQ}}$

INITIALIZATION

INITIALIZATION BLOCK

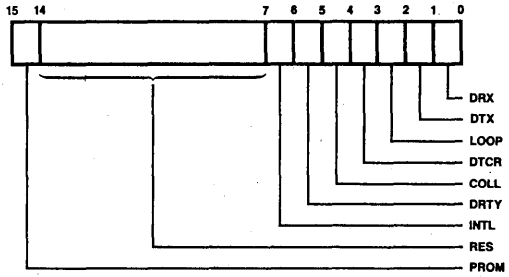
Chip initialization includes the reading of the initialization block in memory to obtain the operating parameters. The following is a definition of the Initialization Block.

The Initialization Block is read by the chip when the INIT bit in CSR_0 is set. The INIT bit should be set before or concurrent with the STRT bit to insure proper parameter initialization and chip operation. After the chip has read the Initialization Block, IDON is set in CSR_0 and an interrupt is generated if INEA = 1.

Higher Addresses	TLEN-TDRA (23:16)	IADR +22
Base Address of Block	TDRA (15:00)	IADR +20
	RLEN-RDRA (23:16)	IADR +18
	RDRA (15:00)	IADR +16
	LADRF (63:48)	IADR +14
	LADRF (47:32)	IADR +12
	LADRF (31:16)	IADR +10
	LADRF (15:00)	IADR +08
	PADR (47:32)	IADR +06
	PADR (31:16)	IADR +04
	PADR (15:00)	IADR +02
	MODE	IADR +00

Mode

The Mode Register allows alteration of the chip's operating parameters. Normal operation is with the Mode Register clear.



Bit	Name	Description
15	PROM	PROMISCUOUS mode. When PROM = 1, all incoming packets are accepted.
14:07	RES	RESERVED
06	INTL	INTERNAL LOOPBACK is used with the LOOP bit to determine where the loopback is to be done. Internal loopback allows the chip to receive its own transmitted packet. Since this represents full duplex operation, the packet size is limited to 32 bytes. INTL is only valid if LOOP = 1, otherwise it is ignored. **LOOP INTL LOOPBACK** 0 X No loopback, normal 1 0 External 1 1 Internal
05	DRTY	DISABLE RETRY. When DRTY = 1, the chip will attempt only one transmission of a packet. If there is a collision on the first transmission attempt, a Retry Error (RTRY) will be reported in Transmit Message Descriptor 3 (TMD_3).
04	COLL	FORCE COLLISION. This bit allows the collision logic to be tested. The chip must be in internal loopback mode for COLL to be valid. If COLL = 1, a collision will be forced during the subsequent transmission attempt. This will result in 16 total transmission attempts with a retry error reported in TMD_3.
03	DTCR	DISABLE TRANSMIT CRC. When DTCR = 0, the transmitter will generate and append a CRC to the transmitted packet. When DTCR = 1, the CRC logic is allocated to the receiver and no CRC is generated and sent with the transmitted packet.

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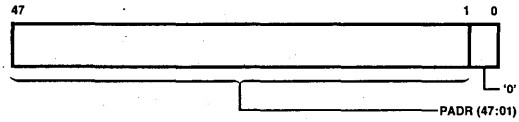
Bit	Name	Description
		During loopback, DTCR = 0 will cause a CRC to be generated on the transmitted packet but no CRC check will be done by the receiver since the CRC logic is shared and cannot generate and check CRC at the same time. The generated CRC will be written into memory with the data and can be checked by the host software. If DTCR = 1 during loopback, the host software must append a CRC value to the transmit data. The receiver will check the CRC on the received data and report any errors.
02	LOOP	LOOPBACK allows the chip to operate in full duplex mode for test purposes. The maximum packet size is limited to 32 bytes. During loopback, the runt packet filter is disabled because the maximum packet is forced to be smaller than the minimum size Ethernet packet (64 bytes). LOOP = 1 allows simultaneous transmission and reception for a message constrained to fit within the silo. The chip waits until the entire message is in the silo before serial transmission begins. The incoming data stream fills the silo from behind as it is being emptied. Moving the received message out of the silo to memory does not begin until reception has ceased. In loopback mode, transmit data chaining is not possible. Receive data chaining is possible if receive buffers are 32 bytes long to allow time for lookahead.
01	DTX	DISABLE THE TRANSMITTER causes the chip to not access the Transmitter Descriptor Ring and therefore no transmissions are attempted DTX = 1 will clear the TXON bit in CSR_0 when initialization is complete.
00	DRX	DISABLE THE RECEIVER causes the chip to reject all incoming packets and not access the Receive Descriptor Ring. DRX = 1 will clear the RXON bit in the CSR_0 when initialization is complete.

Physical Address

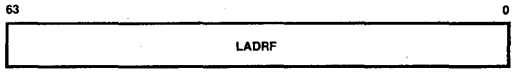


Bit	Name	Descriptor
47:00	PADR	PHYSICAL ADDRESS is the unique 48-bit physical address assigned to the chip. PADR (0) must be zero.

Logical Address Filter

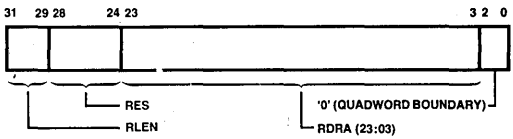
The logical address filter is a 64-bit mask that is used to accept incoming Logical Addresses. The incoming address is sent through the CRC circuit. After all 48 bits of the address have gone through the CRC circuit, the high order 6 bits of the resultant CRC are strobed into a register. This register is used to select one of the 64-bit positions in the Logical Address Filter. If the selected filter bit is a "1," the address is accepted and the packet will be put in memory. The first bit of the incoming address must be a "1" for a logical address. If the first bit is a "0," it is a physical address and is compared against the physical address that was loaded through the initialization block.

The Broadcast address, which is all ones, does not go through the Logical Address Filter and is always enabled. If the Logical Address Filter is loaded with all zeroes, all incoming logical addresses except broadcast will be rejected.



Bit	Name	Descriptor
63:00	LADRF	The 64-bit mask used by the chip to accept logical addresses.

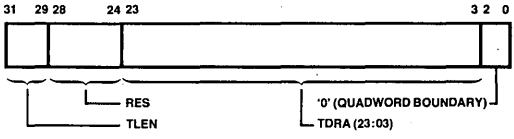
Receive Descriptor Ring Pointer



Bit	Name	Description
15:13	RLEN	RECEIVE RING LENGTH is the number of entries in the receive ring expressed as a power of two.
12:08	RES	RESERVED
07:00 15:03	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Receive Descriptor Ring.
02:00		MUST BE ZEROES. These bits are RDRA (02:00) and must be zeroes because the Receive Rings are aligned on quadword boundaries.

RLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Transmit Descriptor Ring Pointer



Bit	Name	Description
15:13	TLEN	TRANSMIT RING LENGTH is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

12:08	RES	RESERVED
07:00 15:03	TDRA	TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Transmit Descriptor Ring.
02:00		MUST BE ZEROES. These bits are TDRA (02:00) and must be zeroes because the Transmit Rings are aligned on quadword boundaries.

BUFFER MANAGEMENT

Buffer Management is accomplished through message descriptors organized in ring structures in memory. Each message descriptor entry is four words long. There are two rings allocated for the device: a Receive ring and a Transmit ring. The device is capable of polling each ring for buffers to either empty or fill with packets to or from the channel. The device is also capable of entering status information in the descriptor entry. Chip polling is limited to looking one ahead of the descriptor entry the chip is currently working with.

The location of the descriptor rings and their length are found in the initialization block, accessed during the initialization procedure by the chip. Writing a "ONE" into the STRT bit of CSR_0 will cause the chip to start accessing the descriptor rings and enable it to send and receive packets.

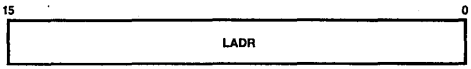
The chip communicates with a HOST device (probably a microprocessor) through the ring structures in memory. Each entry in the ring is either "owned" by the chip or the HOST. There is an ownership bit (OWN) in the message descriptor entry. Mutual exclusion is accomplished by a protocol which states that each device can only relinquish ownership of the descriptor entry to the other device; it can never take ownership, and each device cannot change the state of any field in any entry after it has relinquished ownership.

DESCRIPTOR RINGS

Each descriptor in a ring in memory is a 4 word entry. The following is the format of the receive and the transmit descriptors.

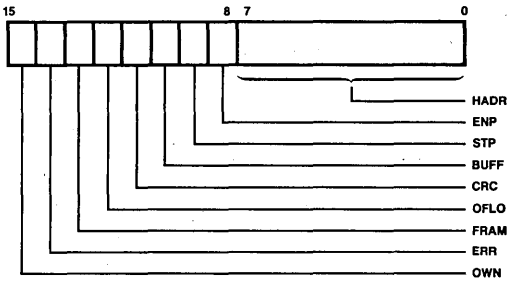
Receive Message Descriptor Entry

Receive Message Descriptor 0 (RMD_0)



Bit	Name	Description
15:00	LADR	The LOW ORDER 16 address bits of the buffer pointed to by this descriptor. LADR is written by the host and unchanged by the chip.

Receive Message Descriptor 1 (RMD_1)



Bit	Name	Description
15	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the chip (OWN = 1). The chip clears the OWN bit after filling the buffer pointed to by the descriptor entry. The host sets the OWN bit after emptying the buffer. Once the chip or host has relinquished ownership of a buffer, it must not change any field in the four words that comprise the descriptor entry.
14	ERR	ERROR summary is the "OR" of FRAM, OFLO, CRC or BUFF. ERR is set by the chip and cleared by the host.
13	FRAM	FRAMMING ERROR indicates that the incoming packet contained a noninteger multiple of eight bits and there was a CRC error. If there was not a CRC error on the incoming packet, then FRAM will not be set even if there was a noninteger multiple of eight bits in the packet. FRAM is set by the chip and cleared by the host.
12	OFLO	OVERFLOW error indicates that the receiver has lost all or part of the incoming packet due to an inability to store the packet in a memory buffer before the internal silo overflowed. OFLO is set by the chip and cleared by the host.
11	CRC	CRC indicates that the receiver has detected a CRC error on the incoming packet. CRC is set by the chip and cleared by the host.
10	BUFF	BUFFER ERROR is set any time the chip does not own the next buf-

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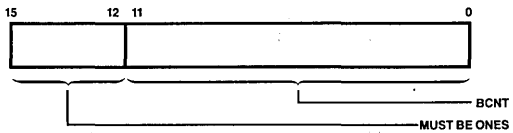
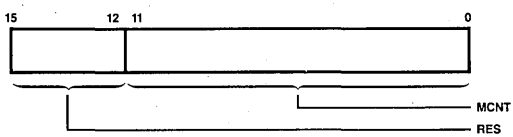
Bit	Name	Description
		fer while data chaining a received packet. This can occur in either of two ways; the OWN bit of the next buffer is zero, or silo overflow occurred before the chip received the next STATUS. BUFF is set by the chip and cleared by the host. If a Buffer Error occurs, an Overflow Error will also occur because the chip tries to acquire the next buffer until the silo overflows.
09	STP	START OF PACKET indicates that this is the first buffer used by the chip for this packet. It is used for data chaining buffers. STP is set by the chip and cleared by the host.
08	ENP	END OF PACKET indicates that this is the last buffer used by the chip for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fit into one buffer and there was no data chaining. ENP is set by the chip and cleared by the host.
07:00	HADR	The HIGH ORDER 8 address bits of the buffer pointed to by this descriptor. This field is written by the host and unchanged by the chip.

Receive Message Descriptor 2 (RMD_2)



Bit	Name	Description
15:12		MUST BE ONES. This field is written by the Host and unchanged by the chip.
11:00	BCNT	BUFFER BYTE COUNT is the length of the buffer pointed to by this descriptor, expressed as a two's complement number. This field is written by the host and unchanged by the chip. Minimum buffer size is 64 bytes.

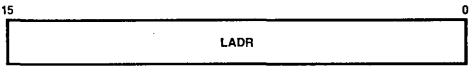
Receive Message Descriptor 3 (RMD_3)



Bit	Name	Description
15:12	RES	RESERVED and read as zeroes.
11:00	MCNT	MESSAGE BYTE COUNT is the length in bytes of the received message. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by the chip and cleared by the host.

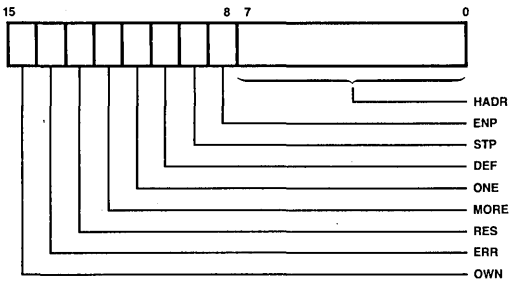
Transmit Message Descriptor Entry

Transmit Message Descriptor 0 (TMD_0)



Bit	Name	Description
15:00	LADR	The LOW ORDER 16 address bits of the buffer pointed to by this descriptor. LADR is written by the host and unchanged by the chip.

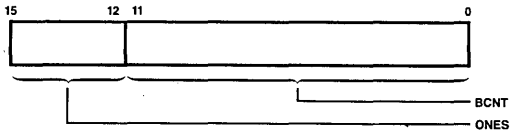
Transmit Message Descriptor 1 (TMD_1)



Bit	Name	Description
15	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the chip (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by this descriptor. The chip clears the OWN bit after transmitting the contents of the buffer. Both the host and the chip must not alter a descriptor entry after it has relinquished ownership.
14	ERR	ERROR summary is the "OR" of LCOL, LCAR, UFLO or RTRY. ERR is set by the chip and cleared by the host.
13	RES	RESERVED bit. The chip will write this bit with a "0."
12	MORE	MORE indicates that more than one retry was needed to transmit a packet. MORE is set by the chip and cleared by the host.
11	ONE	ONE indicates that exactly one retry was needed to transmit a packet. ONE is set by the chip and cleared by the host.
10	DEF	DEFERRED indicates that the chip had to defer while trying to transmit a packet. This condition occurs if the channel is busy when the chip is ready to transmit. DEFER is set by the chip and cleared by the host.

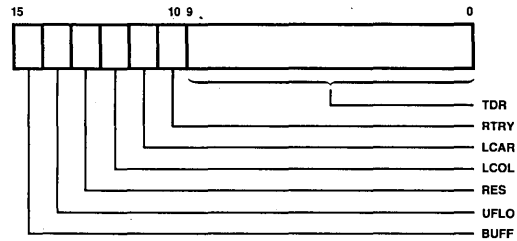
Bit	Name	Description
09	STP	START OF PACKET indicates that this is the first buffer to be used by the chip for this packet. It is used for data chaining buffers. STP is set by the host and unchanged by the chip.
08	ENP	END OF PACKET indicates that this is the last buffer to be used by the chip for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fit into one buffer and there was no data chaining. ENP is set by the host and unchanged by the chip.
07:00	HADR	The HIGH ORDER 8 address bits of the buffer pointed to by this descriptor. This field is written by the host and unchanged by the chip.

Transmit Message Descriptor 2 (TMD_2)



Bit	Name	Description
15:12	ONES	Must be ones. This field is set by the host and unchanged by the chip.
11:00	BCNT	BUFFER BYTE COUNT is the usable length in bytes of the buffer pointed to by this descriptor expressed as a two's complement number. This is the number of bytes from this buffer that will be transmitted by the chip. This field is written by the host and unchanged by the chip. Minimum buffer size is 64 bytes.

Transmit Message Descriptor 3 (TMD_3)



Bit	Name	Description
15	BUFF	BUFFER ERROR is set by the chip during transmission when the chip does not find the ENP flag in the current buffer and does not own the next buffer. This can occur in either of two ways; either the OWN bit of the next buffer is zero, or silo overflow occurred before the chip received the next STATUS signal. BUFF is set by the chip and cleared by the host. If a Buffer Error occurs, an Underflow Error will also occur because the chip tries to read memory data until the silo is empty.
14	UFLO	UNDERFLOW ERROR indicates that the transmitter has truncated a message due to data late from memory. UFLO indicates that the silo has emptied before the end of the packet was reached. UFLO is set by the chip and cleared by the host.
13	RES	RESERVED bit. The chip will write this bit with a "0."
12	LCOL	LATE COLLISION indicates that a collision has occurred after the slot time of the channel has elapsed. The chip does not retry on late collisions. LCOL is set by the chip and cleared by the host.
11	LCAR	LOSS OF CARRIER is set when the carrier input (RENA) to the chip goes false during a chip initiated transmission. The chip does not re-try upon loss of carrier. LCAR is set by the chip and cleared by the host.
10	RTRY	RETRY ERROR indicates that the transmitter has failed in 16 attempts to successfully transmit a message due to repeated collisions on the medium. If DRTY = 1 in the MODE register, RTRY will set after 1 failed transmission attempt. RTRY is set by the chip and cleared by the host.
09:00	TDR	TIME DOMAIN REFLECTOMETRY reflects the state of an internal chip counter that counts from the start of a transmission to the occurrence of a collision. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by the chip and is valid only if RTRY is set.

8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature
Temperature (Ambient) Under Bias
Supply Voltage to Ground Potential Continuous

DC CHARACTERISTICS OVER OPERATING RANGE 0 to +70°C, V_{CC} = 5.0V ± 5%

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input LOW Voltage		−0.5		0.8	V
V_{IH}	Input HIGH Voltage		2		V_{CC} + 0.5V	V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA	0.5			V
V_{OH}	Output HIGH Voltage	I_{OH} = −0.4mA	2.4			V
I_{IL}	Input Leakage	V_{IN} = 0.4V to V_{CC}			±10	μA

ELECTRICAL CHARACTERISTICS

	Parameters	Description	Test Conditions	Min	Typ	Max	Units
BUS SLAVE TIMING							
1	t_{CSH}	Chip Select Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
2	t_{CSS}	Chip Select Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
3	t_{SAH}	ADR Hold Time following $\overline{DAS}$ LOW to HIGH		0			ns
4	t_{SAS}	ADR Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
5	t_{SDO1}	Data Delay following $\overline{DAS}$ HIGH to LOW	CSR_0, RAP, CSR_3		400		ns
	t_{SDO2}		CSR_1, CSR_2		1200		
6	t_{SRDS}	Read Data Setup Time before $\overline{READY}$ HIGH to LOW		75			ns
7	t_{SRDH}	Data Hold Time following $\overline{DAS}$ LOW to HIGH (Read Cycle)		0		35	ns
8	t_{SRYH}	$\overline{READY}$ Hold Time after $\overline{DAS}$ LOW to HIGH		0		35	ns
9	t_{SRH}	READ Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
10	t_{SRO1}	$\overline{READY}$ Driver Turn on Time after $\overline{DAS}$ HIGH to LOW	CSR_0, CSR_3, RAP		600		ns
	t_{SRO2}		CSR_1, CSR_2		1400		
11	t_{SRS}	READ Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
12	t_{SWDH}	Data Hold Time after $\overline{DAS}$ LOW to HIGH (Write Cycle)		0			ns
13	t_{SWDS}	Data Setup Time before $\overline{DAS}$ HIGH to LOW (Write Cycle)		0			ns

ELECTRICAL CHARACTERISTICS

Parameters		Description	Test Conditions	Min	Typ	Max	Units
BUS MASTER TIMING							
1	t_{XAS}	Extended Address Setup Time before ALE HIGH to LOW		75			ns
2	t_{XAH}	Extended Address Hold Time after $\overline{DAS}$ LOW to HIGH		35			ns
3	t_{AS}	Address Setup Time before ALE HIGH to LOW		75			ns
4	t_{AH}	Address Hold Time after ALE HIGH to LOW		35			ns
5	t_{RDAS}	READ Data Setup Time before $\overline{DAS}$ LOW to HIGH		50			ns
6	t_{RDAH}	READ Data Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
7	t_{ALEW}	ALE Width		130			ns
8	t_{WDS}	WRITE Data Setup Time before $\overline{DAS}$ LOW to HIGH		200			ns
9	t_{WDH}	WRITE Data Hold Time $\overline{DAS}$ LOW to HIGH		35			ns
10	t_{DDAS}	WRITE Data Setup Time before $\overline{DAS}$ HIGH to LOW		0			ns
11	t_{DSW}	$\overline{DAS}$ Width		200			ns
12	t_{DALE}	Delay from $\overline{DAS}$ LOW to HIGH to ALE LOW to HIGH		70			ns
13	t_{ADAS}	Delay from ALE HIGH to LOW to $\overline{DAS}$ HIGH to LOW		80			ns
14	t_{RIDF}	Delay from $\overline{DALO}$ LOW to HIGH to $\overline{DAS}$ HIGH to LOW (Read Cycle)		35			ns
15	t_{RDYS}	$\overline{READY}$ Setup Time before $\overline{DAS}$ LOW to HIGH (See Note)		75			ns
16	t_{RDYH}	$\overline{READY}$ Hold Time after $\overline{DAS}$ LOW to HIGH		0			ns
17	t_{OS}	$\overline{DALO}$ Setup Time before ALE HIGH to LOW		110			ns
18	t_{ROH}	$\overline{DALO}$ Hold Time after ALE HIGH to LOW.(Read Cycle)		35			ns
19	t_{ROIF}	Delay from $\overline{DALO}$ LOW to HIGH to $\overline{DALI}$ HIGH to LOW (Read Cycle)		35			ns
20	t_{RIS}	$\overline{DALI}$ Setup Time before $\overline{DAS}$ LOW to HIGH (Read Cycle)		135			ns
21	t_{RIH}	$\overline{DALI}$ Hold Time after $\overline{DAS}$ LOW to HIGH (Read Cycle)		0			ns
22	t_{RIOF}	Delay from $\overline{DALI}$ LOW to HIGH to $\overline{DALO}$ HIGH to LOW (Read Cycle)		55			ns
23	t_{WDSI}	Delay from $\overline{DAS}$ LOW to HIGH to $\overline{DALO}$ LOW to HIGH (Write Cycle)		35			ns

Note: The $\overline{READY}$ setup time before negation of $\overline{DAS}$ is a function of the synchronization time of $\overline{READY}$. The synchronization must occur within two clock ticks (100ns). Therefore, the setup time is 100ns plus any accumulated propagation delays. Ready slips occur on 100ns increments.

ELECTRICAL CHARACTERISTICS

Parameters		Description	Test Conditions	Min	Typ	Max	Units
BUS ACQUISITION TIMING							
1	t_{DON}	Bus Master Driver Enable Time after Assertion of $\overline{HLDA}$		0		150	ns
2	t_{DOFF}	Bus Master Driver Disable Time after Deassertion of $\overline{HOLD}$		0		50	ns
3	t_{RW}	$\overline{RESET}$ Pulse Width[1]		200			ns

Note: 1. $\overline{RESET}$ is an asyncoronous input and does not occur as part of the Bus Acqusition cycle.

Am7991

Ethernet Serial Interface Adapter (SIA)

IN DEVELOPMENT

DISTINCTIVE CHARACTERISTICS

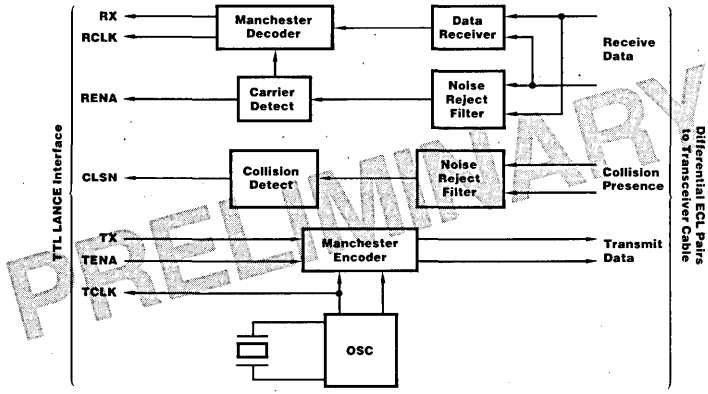
- Compatible with Ethernet specifications
- Crystal controlled Manchester Encoder
- Manchester Decoder acquires clock and data within six bit times with an accuracy of ±3ns
- Guaranteed carrier detection and collision detection threshold limits
  - Carrier/collision detected for greater than −300mV
  - No carrier/collision for less than −175mV
- Input signal conditioning rejects transient noise
  - Transients <10ns for collision detector inputs
  - Transients <16ns for carrier detector inputs
- Receiver decodes Manchester data with up to ±20ns clock jitter
- +5V single power supply
- TTL compatible host interface
- IMOX™ high performance bipolar process
- 24-pin x 0.6" plastic or cerdip

GENERAL DESCRIPTION

The Am7991 Serial Interface Adapter (SIA) interfaces the Am7990 Local Area Network Controller for Ethernet (LANCE) with a standard Ethernet transceiver cable. The SIA provides node data and clock encoding/decoding functions using standard Manchester code. The SIA is compatible with transceiver signalling detailed in the Ethernet specification.

BLOCK DIAGRAM

Serial Interface Adapter (SIA)



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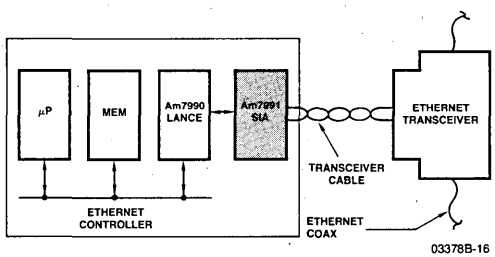
TYPICAL ETHERNET NODE



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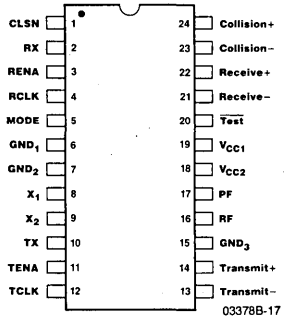
CONNECTION DIAGRAM – Top View

D-24-1



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FUNCTIONAL DESCRIPTION

The Ethernet Serial Interface Adapter (SIA) has two sections, a transmitter and receiver. The transmitter combines separate clock and NRZ data input signals and encodes them into a serial bit stream using standard Manchester II encoding. It also differentially drives up to 50 meters of twisted pair transmission line (Ethernet Transceiver Cable). The receiver performs three functions. It detects the presence of data on the transceiver cable; it detects collision information from the transceiver and provides a collision control output (CLSN) to the Am7990 LANCE, and it reduces a Manchester encoded data stream into separate clock and data outputs.

CRYSTAL CONTROLLED OSCILLATOR

A 20MHz fundamental mode crystal oscillator provides the basic timing reference in the SIA. It is divided by two to create the transmit clock reference (TCLK). Both 20MHz and 10MHz clocks are fed into the Manchester encoder to generate the transitions in the encoded data stream. The 10MHz clock, TCLK, is used by the SIA to internally synchronize transmit data (TX) and transmit enable (TENA). TCLK is also used as a stable bit rate clock by the receive section of the SIA and by other devices in the system (the Am7990 LANCE uses TCLK to drive its internal state machine). The oscillator may use an external crystal or an external TTL Level 20MHz input as a reference.

RECEIVE SECTION

The principle function of the receiver is the separation of the Manchester encoded data stream into clock and NRZ data.

INPUT SIGNAL CONDITIONING

Before the data and clock can be separated it must be determined whether there is "real" data or unwanted noise at the transceiver interface. The Am7991 SIA carrier detection receiver provides a static noise margin of −175 to −300mV for received carrier detection. These DC thresholds assure that no signal less than −175mV is ever decoded and that signals greater than −300mV are always decoded. Transient noise of less than 10ns duration in the collision path and 16ns duration in the data path are also rejected.

The input conditioning stage prevents unwanted idle state noise on the transceiver from causing "false starts" in the controller circuitry assuring valid response to "real" data.

The input signal conditioning section (Figure 1) consists of two data paths. The receive data path is designed to be a zero threshold, high bandwidth receiver. The carrier detection receiver is similar, but with an additional bias generator to require that only data amplitudes larger than the bias level are interpreted as valid data. The noise rejection filter prevents noise transients <16ns from enabling the data receiver output. The collision detector similarly rejects noise transients <10ns.

Received data will have finite rise and fall times, so a non-zero threshold is directly transformed into clock distortion (see Figure 2). The Am7991 SIA data receiver threshold is typically less than ±5mV, minimizing its contribution to RCLK jitters. (Worst case error <0.5ns).

RECEIVER SECTION TIMING

Receive Enable (RENA) is the "carrier present" indication established when a signal of sufficient amplitude (V_{IDC}) and duration (t_{RPWR}) is present at the receive inputs. Receive Clock (RCLK) and Receive Data (RX) become available within 6 bit

Figure 1. Input Signal Conditioning Section

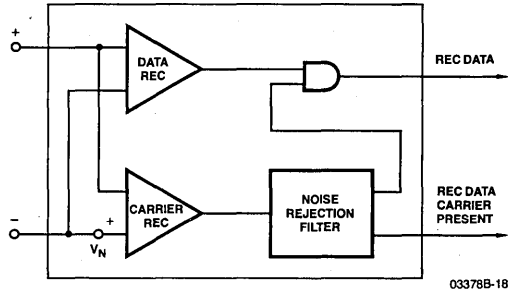

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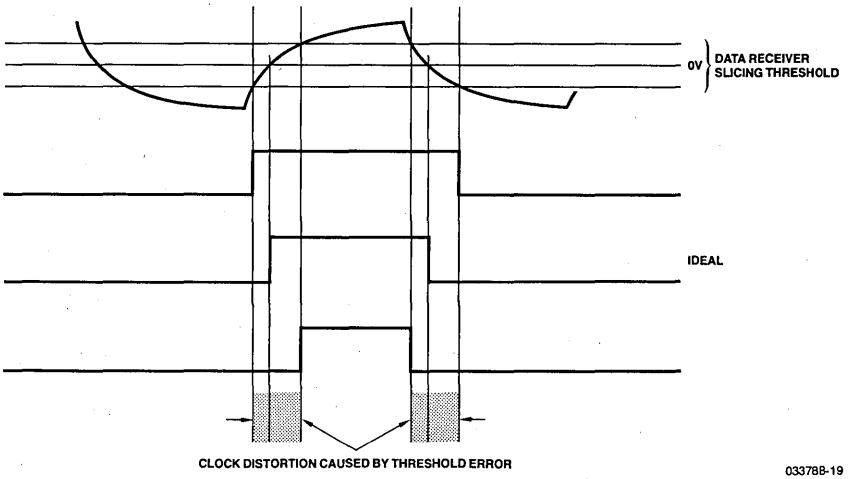
Figure 2.



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times, approximately 600ns from the time RENA is asserted (see Figure 3). At this point the total phase error of RCLK to the data stream is less than ±3ns. The Am7991 SIA is guaranteed to correctly decode a Manchester encoded serial bit stream with up to ±20ns of jitter.

The receiver detects the end of a packet when the normal transition on the differential inputs cease. Three half-bit times after the last LOW-to-HIGH transition, RENA goes LOW. In that same 3 half-bit times, RCLK completes one last cycle, storing the last data bit. It then goes LOW and remains LOW (see Figures 4 and 5).

The collision output flag (CLSN) is asserted when the input to the collision detector differential input is of sufficient amplitude (V_{IDC}) and duration (t_{CPWR}). CLSN will remain HIGH for a minimum of 80ns and a maximum of t_{CPO} following the last LOW-to-HIGH transition of the collision input (see Figure 8).

RECEIVE CLOCK CONTROL

To ensure quick capture of incoming data the receiver phase-locked-loop is frequency locked to the transmit oscillator and it phase locks to incoming data edges.

DIFFERENTIAL I/O TERMINATIONS

The differential input for the Manchester data (receive ±) is externally terminated by two 40.2Ω±1% resistors and one common mode bypass capacitor. The differential input impedance Z_{IDF} and the common mode input Z_{ICM} are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. The collision ± differential input is terminated in exactly the same way as the receive input.

TRANSMIT SECTION TIMING

The transmit enable (TENA) and transmit data (TX) inputs are internally synchronized with TCLK, and must meet setup and hold time requirements with respect to the TCLK rising edge. In the transmit mode, the Am7990 LANCE activates TENA. At the same time the first bit of data is made available on TX.

As long as TENA remains HIGH, data is clocked into the SIA by TCLK and encoded for output to the transceiver (see Figure 6).

When TENA goes LOW, the differential transmit outputs go to one of two idle states. The selection of Mode I causes the output to either go HIGH or remain HIGH at the end of the last bit cell time. In Mode II the output goes HIGH or remains HIGH for t_{TOH} and is then allowed to return to zero differential.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	+7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max
DC Input Voltage (Logic Inputs)	+5.5V
DC Input Voltage (Rec Coil)	−1 to +6V
Transmit ± Output Current	−50 to +5mA
DC Output Current, Into Outputs	100mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
RECEIVER SPECIFICATION						
t_{RCT}	RCLK Cycle Time	t_{OSC} = 50ns	85		118	ns
t_{RCH}	RCLK High Time		38			ns
t_{RCL}	RCLK Low Time		38			ns
t_{RCR}	RCLK Rise Time	C_L = 50pF Figures 10 and 11 (Note 1)	0		8	ns
t_{RCF}	RCLK Fall Time		0		8	ns
t_{RDR}	RX Rise Time		0		8	ns
t_{RDF}	RX Fall Time		0		8	ns
t_{RDH}	RX Hold Time (RCLK to RX Change)		5			ns
t_{RDS}	RX Prop Delay (RCLK to RX Stable)				25	ns
t_{DPH}	RENA Turn-On Delay (V_{IDC} on Receive ± to $CARR_H$)	Figures 1 and 13			180	ns
t_{DPO}	RENA Turn-Off Delay (V_{IDH} on Receive ± to $CARR_L$)	Figures 2 and 13			160	ns
t_{DPL}	RENA Low Time	Figure 4	120			ns
t_{RPWR}	Receive ± Input Pulse Width to Reject (Input < V_{IDC})	Figures 9 and 13			16	ns
t_{RPWO}	Receive ± Input Pulse Width to Turn-On (Input < V_{IDC})	Figures 9 and 13	40			ns
t_{RLT}	Decoder Acquisition Time	Figure 3			600	ns
COLLISION SPECIFICATION						
t_{CPWR}	Collision Input Pulse Width to Reject (Input < V_{IDC})	Figures 9 and 13			10	ns
t_{CPWO}	Collison Input Pulse Width to Turn-On (Collision ± Exceeds V_{IDC})	Figures 7, 9 and 13	26			ns
t_{CPWE}	Collision Input to Turn-Off CSLN (Input > V_{ILDO})	Figures 9 and 13	80			ns
t_{CPWN}	Collision Input to Not Turn-Off CLSN (Input > V_{IDC})				160	ns
t_{CPH}	CLSN Turn-On Delay (V_{IDC} on Collision ± to $CLSN_H$)	Figures 7, 8 and 13			180	ns
t_{CPO}	CLSN Turn-Off Delay (V_{IHD} on Collision ± to $CLSN_L$)				190	ns
TRANSMITTER SPECIFICATION						
t_{TCL}	TCLK Low Time	t_{OSC} = 50ns	45		55	ns
t_{TCH}	TCLK High Time	Figures 10 and 11	45		55	ns
t_{TCR}	TCLK Rise Time		0		8	ns
t_{TCF}	TCLK Fall Time		0		8	ns
t_{TDS}, t_{ES}	TXD and TEN Setup Time	Figures 6 and 7	10			ns
t_{TDH}, t_{EH}	TXD and TEN Hold Time		5			ns
t_{TOCE}	Transmit ± Output, (Bit Cell Center to Edge)	Figures 7 and 12	49.5		50.5	ns
t_{OD}	TCLK High to Transmit ± Output				100	ns
t_{TOR}	Transmit ± Output Rise Time	20-80% Figure 12	1		5	ns
t_{TOF}	Transmit ± Output Fall Time		1		5	ns

Note 1. Assumes equal capacitance loading on RCLK, RX and RENA.

Am7991
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage TTL RCLK, RXD, CARR, CLSN, TCLK	$I_{OH} = -1.0mA$	2.4	3.4		V
V_{OL}	Output Low Voltage TTL RCLK, TCLK, RXD, CARR, CLSN	$I_{OL} = 16mA$,			0.5	V
		$I_{OL} = 1mA$			0.4	
V_{OD}	Differential Output Voltage (Transmit+) − (Transmit−) V_O		600		1200	mV
	$\overline{V_O}$		−600		−1200	
V_{CMT}	Common Mode Output		0		5	V
V_{ODI}	Differential Output Voltage Imbalance (Transmit±) $\lvert\lvert V_O\rvert - \lvert\overline{V_O}\rvert\rvert$			5	100	mV
V_{IH}	Input High Voltage TTL		2.0			V
I_{IH}	Input High Current TTL	V_{CC} = Max, V_{IN} = 2.7V			+50	μA
V_{IL}	Input Low Voltage TTL				0.8	V
I_{IL}	Input Low Current TTL	V_{CC} = Max, V_{IN} = 0.4V			−400	μA
V_{IRD}	Differential Input Threshold (Rec Data)		−25	0	+25	mV
V_{IDC}	Differential Input Threshold (Carrier/Collision±)		−175	−225	−300	mV
I_{CC}	Power Supply Current				TBD	mA
I_I	Input Breakdown Current V_I = +5.5 (TCLK, TEN)				1	mA
V_{IC}	$I_{IN} = -18mA$				−1.2	V
I_{SCO}	RCLK, RXD, TCLK, CLSN, CARR Short Circuit Current		−40		−150	mA
R_{IDF}	Differential Input Resistance	V_{CC} = 0 to Max	1.5K			Ω
R_{ICM}	Common Mode Input Resistance	V_{CC} = 0 to Max	375			Ω
V_{ICM}	Receive and Collision Input Voltage	$I_{IN} = 0$	1	2.5	4	V
I_{ILD}	Receive and Collision Input Low Current	$V_{IN} = -1V$			−5.33	mA
I_{IHD}	Receive and Collision Input High Current	$V_{IN} = 6V$			5.33	mA
I_{IHZ}	Receive and Collision Input High Current	V_{CC} = 0, V_{IN} = +6V			9.0	mA

Figure 3. Receiver Timing – Start of Packet

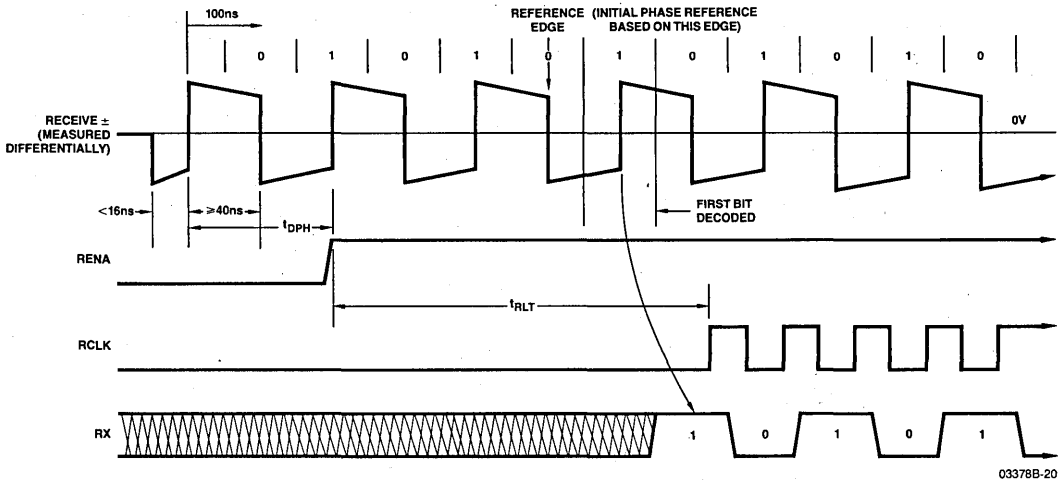

Figure 4. Receiver Timing – End of Packet

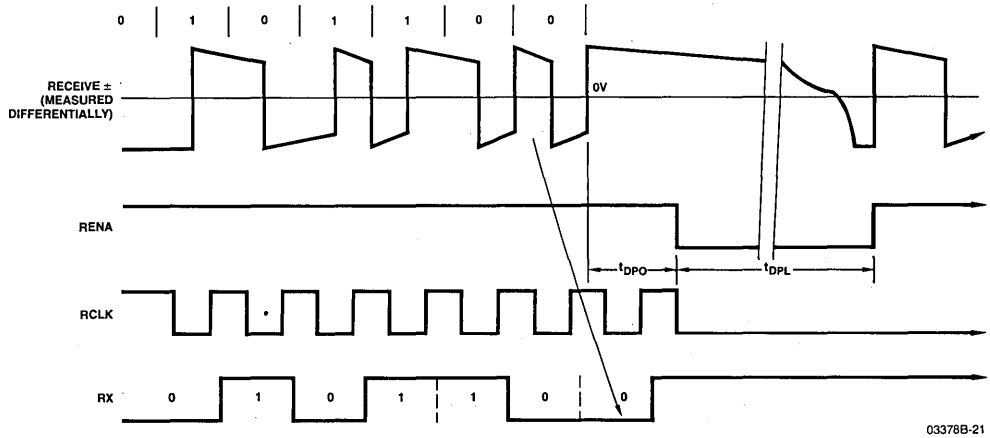

Figure 5. Receiver Timing – End of Packet

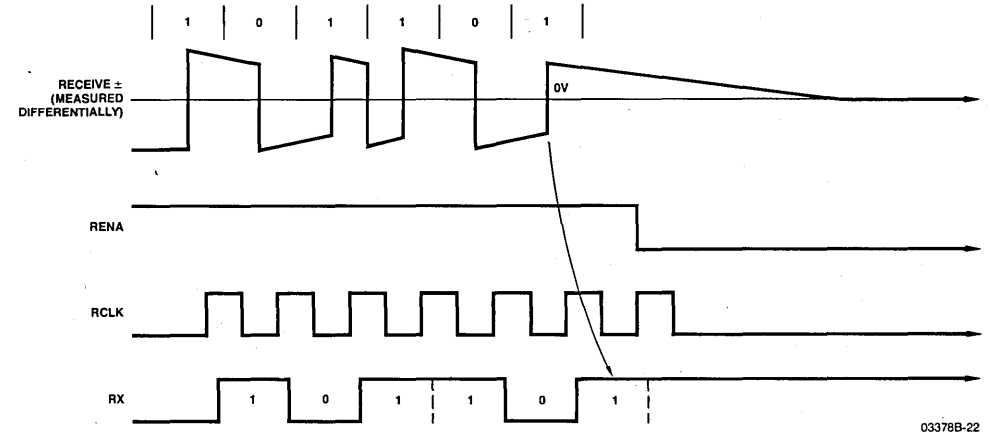

Figure 6. Transmitter Timing – Start of Transmission

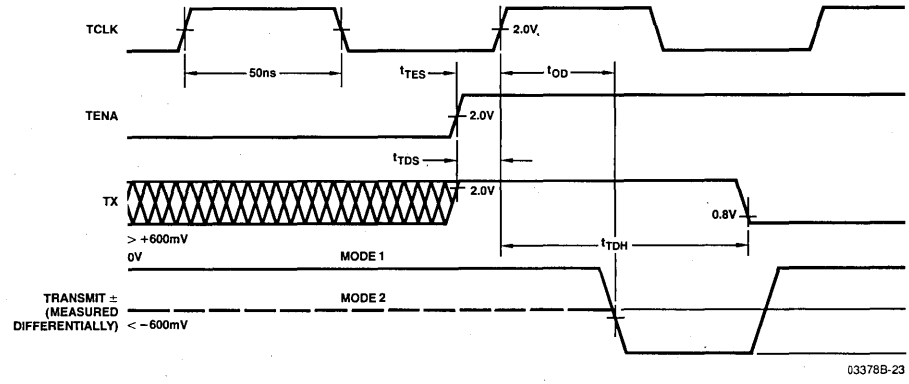

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Figure 7. Transmitter Timing – End of Transmission

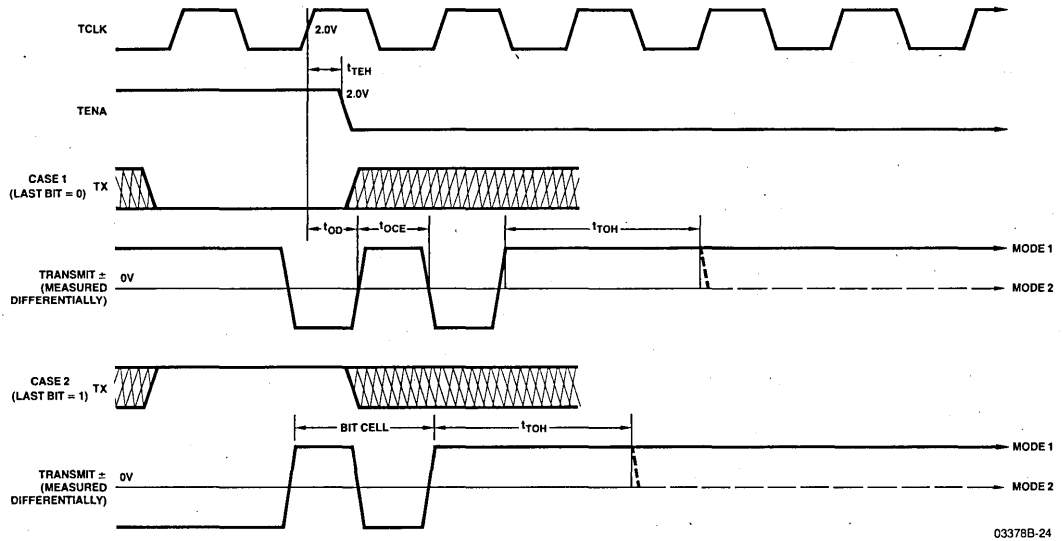


Figure 8. Collision Timing

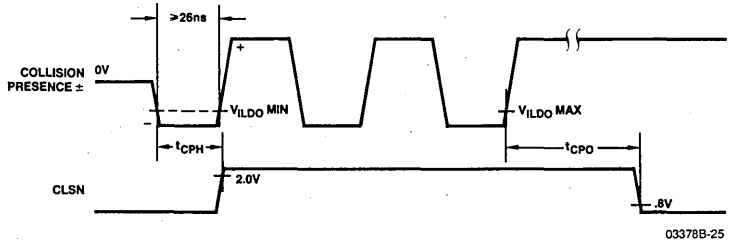


Figure 9. Input Pulse Width Timing

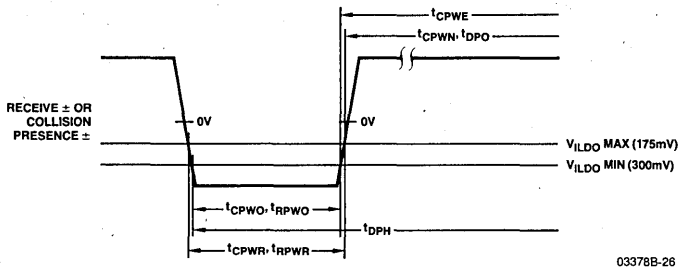


Figure 10. RCLK and TCLK Duty Cycle and Rise/Fall Time

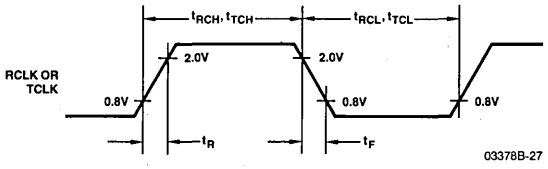


Figure 11. Test Load for RX, RENA, RCLK

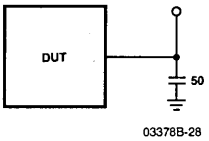


Figure 12. Transmit ± Output Test Circuit

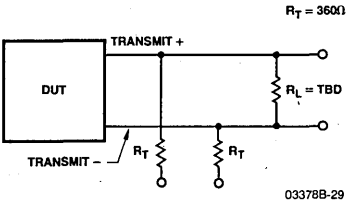
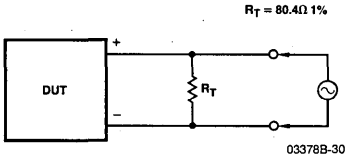


Figure 13. Receive ± and Collision ± Input Test Circuit



8

Design Considerations for the Ethernet Node

By Russell M. de Piña
Advanced Micro Devices

LANCE/System Interface

The LANCE has been designed as a user programmable device and is capable of being interfaced with a wide range of host processors ranging from microprocessors to mainframe systems. Because of its on-board memory management capability, the user may share system memory for packet buffering. The LANCE has a 16-bit time multiplexed address/data bus along with an 8-bit dedicated address bus such that the LANCE may access a 24 bit address space.

The hardware interface between the LANCE and a host processor is friendly. Even though the data/address bus of the LANCE itself is multiplexed, there are no difficulties in interfacing the LANCE with a host processor that has a demultiplexed data bus. Because of the flexibility of this interface, the LANCE can directly interface with any of the popular 16 bit microprocessors (8086, Z8000*, LSI-11**, 68000). Implementations of the LANCE with processors that have both multiplexed and demultiplexed buses will be examined here.

Figure 1a shows the interface block diagram for interconnection between the LANCE and 8086, while figure 1b shows the interface block diagram for the LANCE and Z8000 host processor. Both of these processors employ a multiplexed address/data bus. The interface between the LANCE and the two processors is similar. One major difference is that since the 8086 has separate read/write signals, it may be necessary to incorporate some special logic to convert the single read/write control output signal from the Am7990 into signals compatible with those coming from the A8086. The interface between the LANCE and these processors requires between 13 and 15 SSI/MSI components. Functions such as address decoding are common to other peripherals in the system. If logic already exists in the system for these common functions, the designer can reduce the amount of logic for the LANCE interface to 5-7 SSI/MSI components. If the designer elects to use programmable logic devices, (PALs***) the chip count could be reduced to 3-5 PALs if no common functions can be utilized. If there exist any common functions in the system that may be used, the LANCE/host interface would require only 1-3 PALs.

In both cases, the processors are connected to the LANCE through a common bus. This may be an industry standard or a proprietary bus designed by the user.

The LANCE can be addressed either as part of the processor's I/O address space or as part of the system memory. Since memory transfers usually take less time to execute, it may be more desirable to memory map the LANCE as opposed to mapping it as an I/O port. The control signals are connected to and from the LANCE so that it may talk with the host processor and the rest of the system. The address lines are latched and are then sent to the address decoding logic to produce the chip select signal and to toggle the ADR pin on the LANCE when necessary.

The interface between the LANCE and a host processor with a demultiplexed bus (i.e. 68000) is similar to the multiplexed bus interface in many areas (Figure 2). Because there are dedicated address and data lines with a demultiplexed bus, the address latch that is shown in Figure 2 may be omitted if the address stays valid for a sufficient length of time to allow data transactions to occur.

Software Support

The routines required for software support of the LANCE encompass its various modes of operation as follows:

a. Initialization/Diagnostic
b. Interrupt Processing
c. Receive Mode
d. Transmit Mode
e. Error Detection and Reporting

* Z8000 is a trademark of Zilog, Inc.
** LSI-II is a registered trademark of Digital Equipment Corp.
*** PAL is a registered trademark of Monolithic Memories, Inc.

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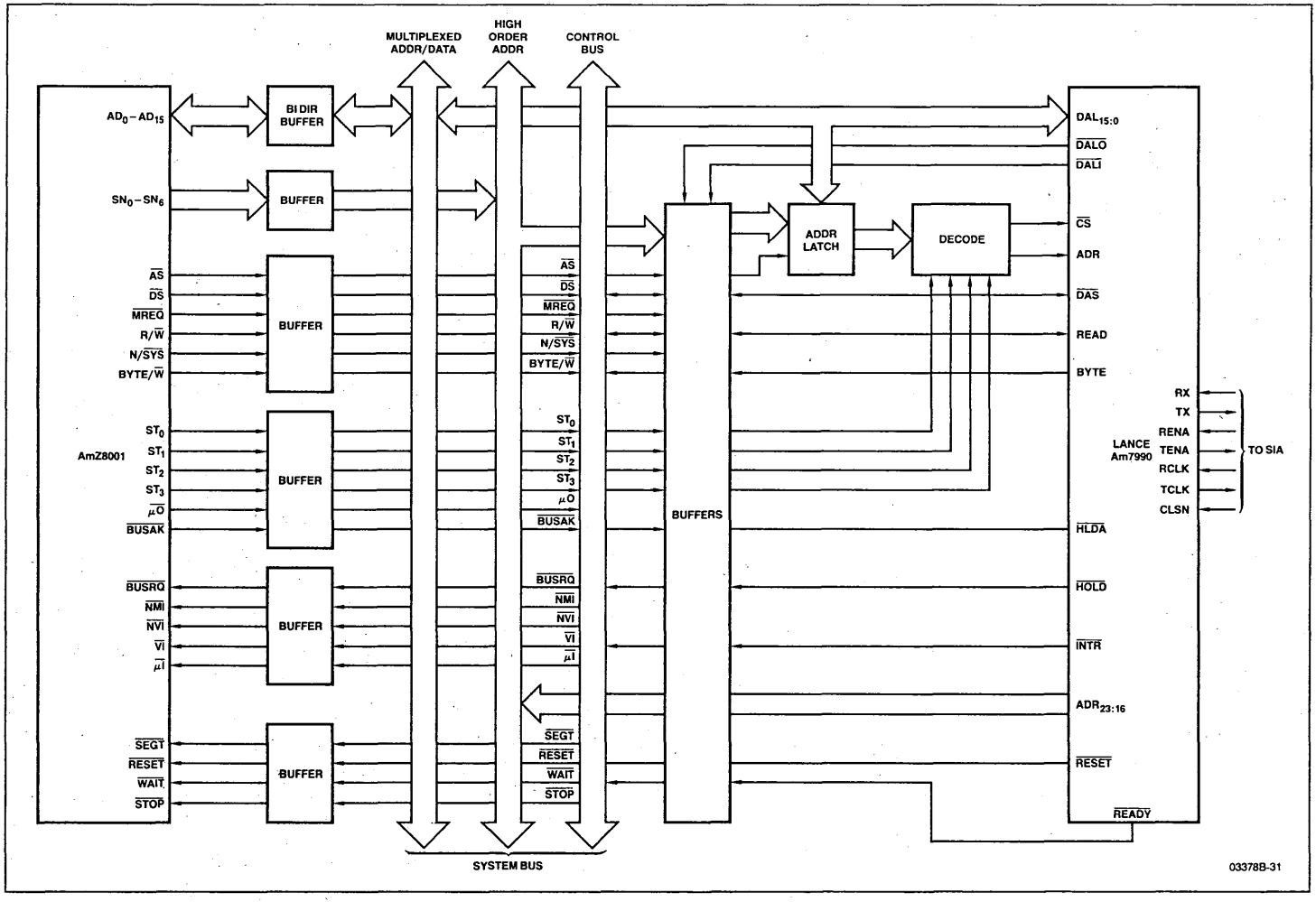


Figure 1a. Z8000/LANCE Interface Block Diagram

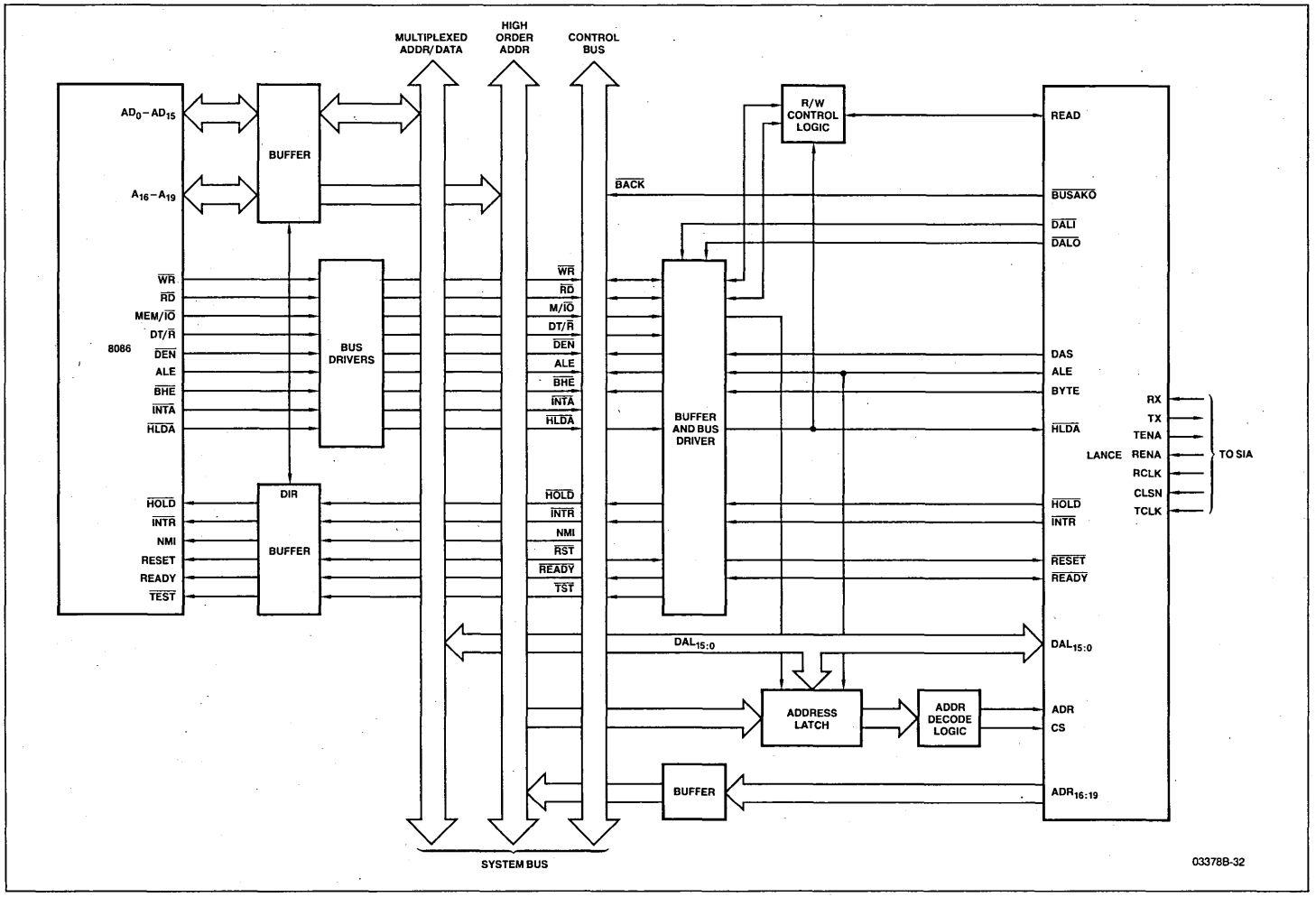


Figure 1b. 8086/LANCE Interface Block Diagram

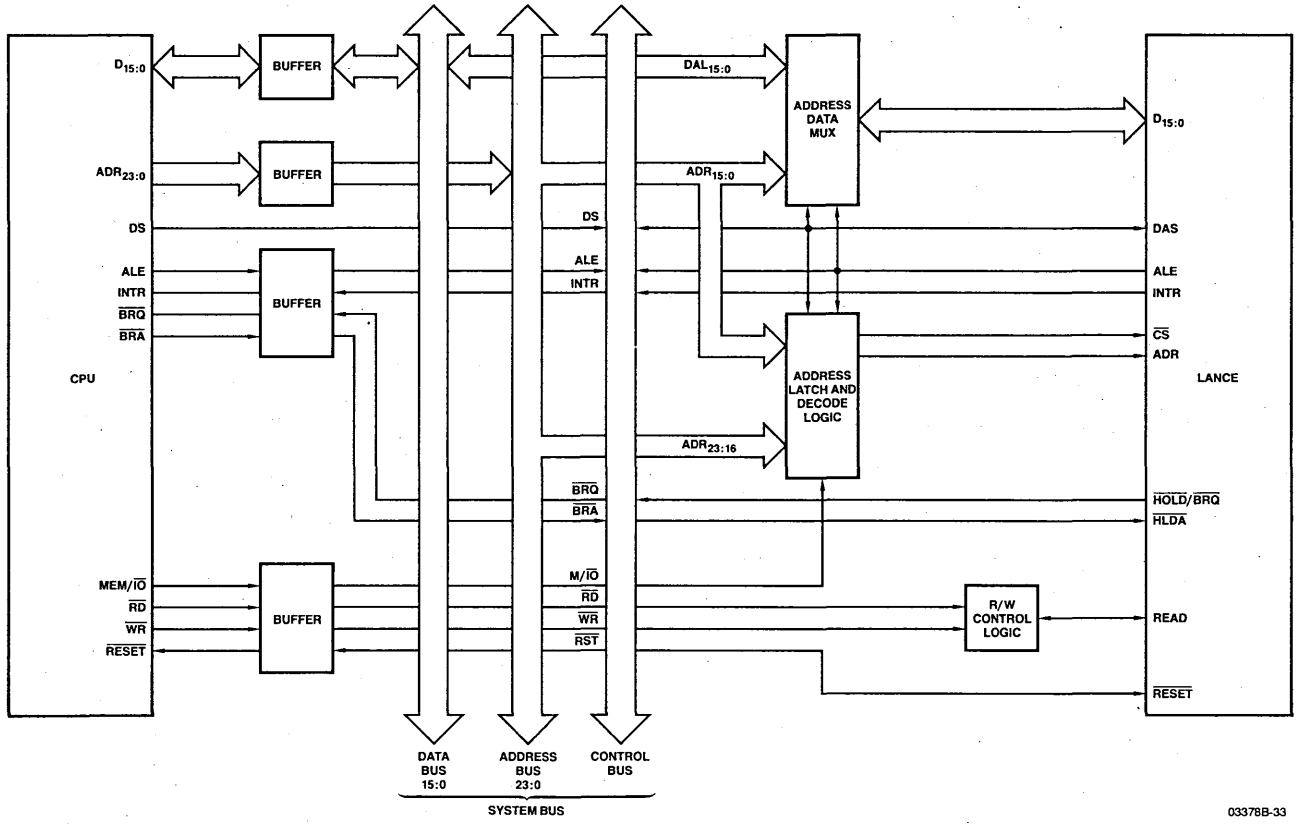


Figure 2. LANCE Interface Block Diagram – Demultiplexed Bus

Initialization and Diagnostics

The initialization routine is used to set up the LANCE so that it may communicate with the host. Diagnostics allows the LANCE to test itself to make sure that it can operate correctly on the network. The three conditions in the system operation which warrant invocation of the initialization diagnostic procedure are:

a. Power on (cold start)
b. Hardware reset (warm start)
c. System error recovery

The initialization routine sets up the four Control and Status Registers (CSRØ-CSR3) with the correct bits set so that the LANCE can operate in the user system. The initialization block (Figure 3) is read by the LANCE and the descriptor rings are initialized by this procedure. Figures 4a and 4b depicts the components of the descriptor rings. The diagnostic procedure is executed as part of the initialization. There are four user programmable diagnostic modes. Each mode requires the user to change bits in the mode register bit mask and reinitialize the LANCE. The four modes are listed as follows:

a. Internal loopback
b. CRC logic check
c. Collision detection
d. External loopback

During internal loopback, the LANCE is able to transmit and receive information simultaneously (i.e., full duplex operation). The LANCE has the ability to operate in full duplex for up to 32 bytes. The message transmitted during internal loopback never leaves the LANCE. If any transmission or reception errors occur, they are effectively isolated to the logic which interfaces the LANCE to the upper levels of the system.

External loopback operates in much the same fashion as internal loopback except that the test packet is actually transmitted on the cable. External loopback compliments internal loopback by isolating faults to the data path between the LANCE and the Ethernet cable. During loopback the LANCE is also able to diagnose faults in the CRC logic system and the collision detection system.

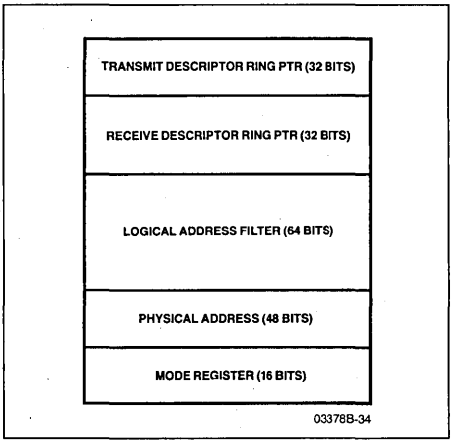


Figure 3. Initialization Block

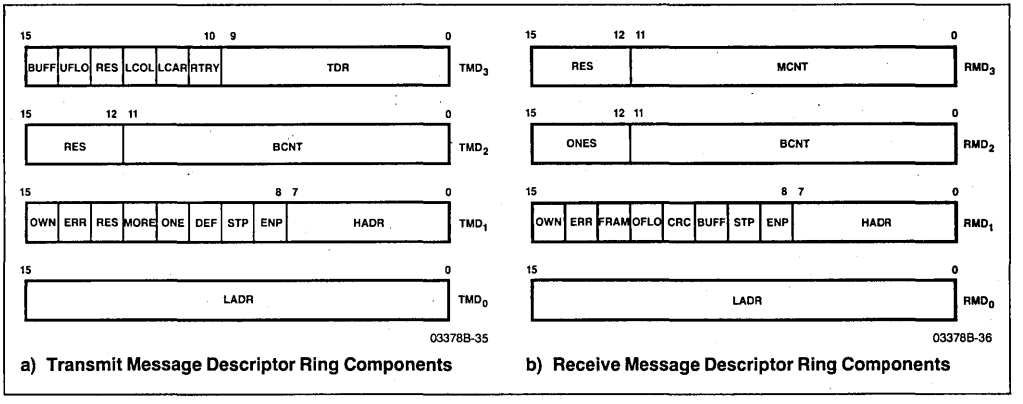


Figure 4.

The CRC generating logic must be checked separately from the checking logic because of the half duplex nature of the LANCE. This is accomplished via the Disable Transmit CRC (DTCR) bit in the mode register. To check the transmit CRC logic, DTCR is set to zero. This enables the transmit CRC generation and disables the receive CRC checking. The processor then constructs a test packet and calculates the CRC in software. THe software calculated CRC is stored in memory. Next, the test packet is looped back into memory via the LANCE. The CRC generated during the transmit phase of loopback is then compared with the previously calculated CRC stored in memory for any mismatch. To test the receive CRC checker DTCR is set to one. This disables the transmit CRC generator and enables the receive CRC checker. The previously calculated checksum is appendend to the packet and checked for error by the receive CRC logic in the LANCE.

The LANCE checks the collision detection capabilities of the node by use of the COLLISION bit in the mode register and by monitoring COLLISION ERROR in CSRØ. To ascertain if the LANCE's internal collision detection logic is functioning, the chip is placed in internal loopback and the COLLISION bit is set. The LANCE is then commanded to loop a test packet. The COLLISION bit will cause the LANCE to detect a collision on each loopback attempt.

After 16 such automatic attempts, the LANCE signals the host that a retry error has occurred. The collision signal path from the transceiver chip to the LANCE is checked by placing the LANCE in external loopback, looping a packet, and then reading the COLLISION ERROR in CSRØ.

Initialization and Diagnostic Routine

The initialization and diagnostic routine flowchart is shown in Figure 5. The flowchart shows that upon invocation of the initialization routine, the host processor first programs Control and Status Register 3 (CSR3) with the appropriate pattern for byte swap, ALE/$\overline{AS}$ control and programming the $\overline{BM}$ lines. Once this is complete, the host then programs CSRØ, CSR1, and CSR2 for performing the internal loopback test. An error counter is then set. Each time the internal loopback test fails, the counter is decremented until either the test passes and the counter is reset or the test fails and the LANCE is turned off and the node deactivated. If the test is passed, the LANCE is then reinitialized for external loopback testing and the test is tried until either the error counter counts down or the test passes. As before, if the error counter counts down, then the node is shut down, otherwise the initialization routine proceeds to the collision detection test. This test is conducted in the same fashion as the two before it, except that when this test is passed, the node is initialized for normal operation and the initialization routine returns control to the calling procedure.

Interrupt Service Latency in LANCE Systems

When transmit and receive interrupts occur, it is desirable to process these interrupts before another packet can arrive at the node. The time required by the system to service the interrupt is called the interrupt service latency. After the LANCE receives a packet, there is a 9.6 μs interpacket delay before another packet appears at the node. Once this next packet appears, there are 34.4 μs during which the internal FIFO is accumulating data, giving a total of 45 μs during which the host must process the receive interrupt and yield the system bus to the LANCE. Since the bus arbitration time is usually on the order of 100-200ns, it is possible to assume that there are 44.8 μs in which to service the interrupt. This is the maximum interrupt service latency in the system for LANCE interrupts.

One method of processing interrupts is to service them in real time. This method is subject to the processor timing. When servicing interrupts in real time, it is necessary to determine the type of interrupt and

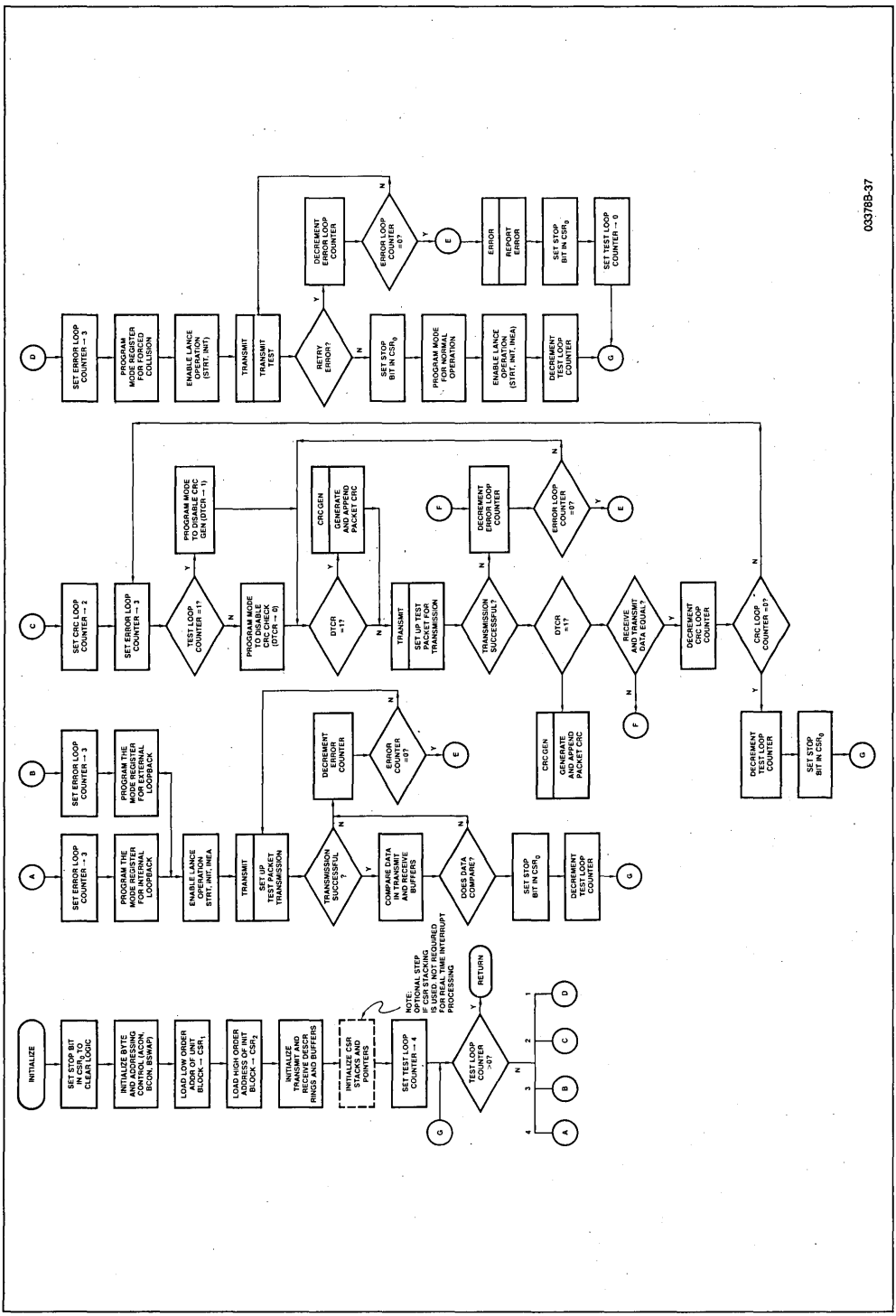


Figure 5. Initialization/Diagnostics Flowchart

take any required action before returning to the interrupted process. Detecting the interrupt type requires reading the bit mask in CSRØ. If the host processor timing is not fast enough, the time interval will run out and the result will be missed packets. In order to determine whether or not it is possible to provide real time interrupt service for the LANCE, the user must first write the code and then compute the timing for execution of the code. If the result is less than 44 μs, then it is possible to service interrupts in real time. If the host is too slow for real time processing, techniques such as CSR stacking are used.

CSR stacking minimizes interrupt service latency by stacking the status information associated with a particular interrupt. Since there are descriptor rings associated with transmission and reception, status information could be placed on two stacks residing in memory, one for transmission and reception interrupts. The depths of these stacks is dictated by the number of descriptors in the transmit and receive descriptor rings. These stacks are organized as shown in Figure 6. There are two pointers in each stack, one for updating entries at the time of interrupts (CSRW) and one for reading the entries at the time of processing (CSRR). An "R" or "T" preceding these mnemonics designates which stack is being used, receive or transmit respectively. Since CSRØ is the only register which contains status information, it is the only register which must be stacked.

Other alternatives include modifying the node architecture (Fig. 11) to offload the processor and gain throughput for real time operation. The folowing paragraph is a description of an interrupt service routine using CSR stacking. The flow chart appears in Figure 7.

Interrupt Service Routine Using CSR Stacking

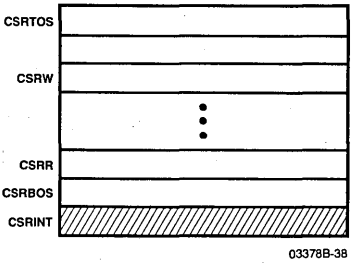
Upon invocation of the interrupt service routine (Figure 7), the host reads the contents of CSRØ and clears it. The host then checks for either a transmit or receive interrupt. The contents of CSRØ are then placed on the appropriate CSR stack and return is made to the calling procedure. If the interrupt is an initialization interrupt, no special processing is required, since the IDON bit is set only during initialization.

The software for the Transmit and Receive modes is very similar. The routines are invoked when any of the upper level programs must cause the transmission of a packet or if a receive packet interrupt occurs. On receive interrupt, the host must process the messages residing in the descriptor ring.

Transmit Driver Routine

The flowchart for the transmit driver routine is shown in Figure 8.

Upon entry, the host processor checks for an available descriptor in the Transmit Descriptor Ring. Once an available descriptor has been found, the start of packet, and/or end of packet bits in TMD1 may be set. The



CSRINT	Pointer to start location of CSRR, CSRW.
CSRR	CSR stack entry for current descriptor being serviced.
CSRW	CSR stack entry for last descriptor used by LANCE.
CSRBOS	Bottom of CSR stack.
CSRTOS	Top of CSR stack.

Note: 1. CSRR always lags behind CSRW.

Figure 6. CSR Stack Organization

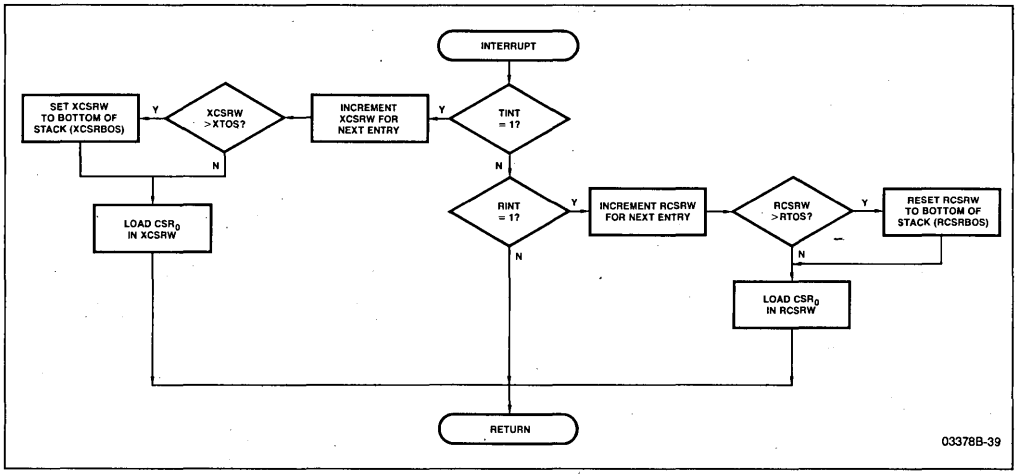
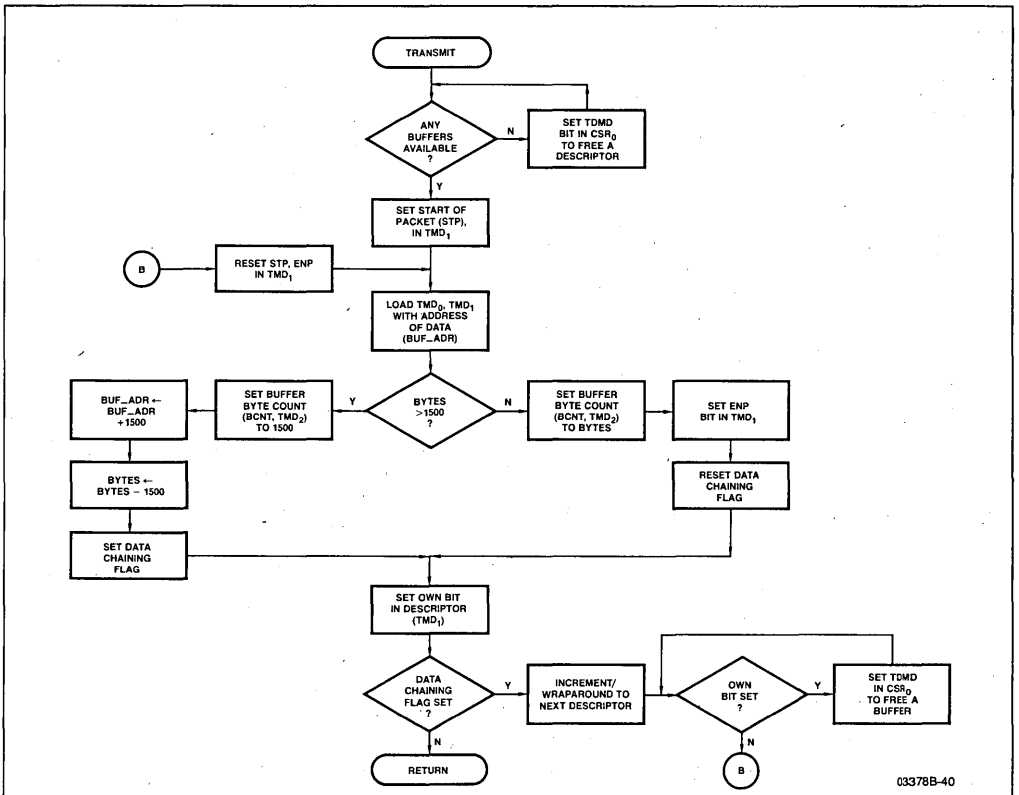


Figure 7. Interrupt Service Routine for LANCE (Using CSR Stacking Technique)



Notes: 1. BUF_ADR – pointer to location of data to be sent.
BYTES – number of bytes to be sent. Both are arguments passed to transmit.
2. This flowchart does not show the use of shadow variables. This should be done otherwise the arguments will be destroyed.

Figure 8. Transmit Routine Flowchart

buffer address is then set in TMDØ and TMD1. The byte count of the message is checked to see if more than 1500 bytes need to be transmitted. If this is the case, then a "data chaining" flag is set so that additional descriptors may be allocated for the transmission of this particular block of data. Otherwise, the entire block may be transmitted as one packet. In either case, the descriptor ring entry currently being pointed at by the host is relinquished to the LANCE for transmission. The status of the data chaining flag is checked. If the flag is set, the remaining number of message bytes are calculated and the process is repeated until the entire block of data is set up for transmission. Control is then transferred back to the calling procedure. The memory location of the data block and its byte count is passed to the transmit driver as arguments.

Receive Driver Routine

After reception of a packet, a receive driver routine (flow chart shown in Figure 9), must be executed to process the received data. The following is a description of such a program.

Upon entry to the receive driver, the pointer for reading the receive CSR stack (RCSRR) is incremented to get the correct value. If the pointer passes the top of the stack, it is wrapped around. The next descriptor pointed at by the processor is then checked to see if the own bit is set. If not, then the error condition is reported and return is made to the calling procedure. Otherwise, the descriptor is then checked to see if the end of packet bit (ENP) is set. If the ENP bit is set, then the CSR stack entry pointed at by RCSRR is checked to see if any errors are present. Receive Message

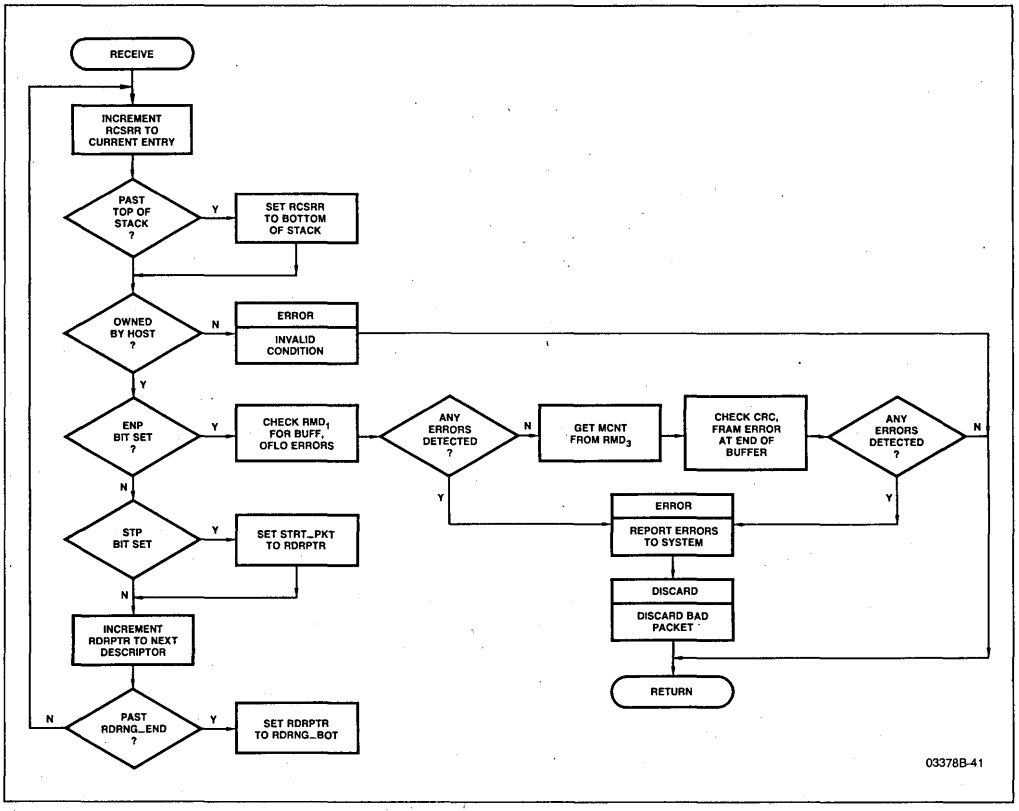


Figure 9. Receive Routine Flowchart

Descriptor 1 is checked also. If no errors are present, the routine returns to the calling procedure. Otherwise, the error is reported and the packet is then discarded and a return is made. If the ENP bit is not set, the start of packet (STP) bit is tested. If STP is set, then a pointer to the descriptor is created to delineate the packet. The purpose of setting a start of packet pointer is to provide a starting point for discarding the packet should any errors exist in a packet whose buffers are chained together. The pointer to the descriptor (RCSRR) is then incremented to the next descriptor and the process is repeated.

The routines described in this section comprise the software support for the direct host interface with the LANCE. The software for reporting errors is assumed to be available to the designer through the operating system or executive of the host processor. The addition of error messages to cover the LANCE are the only modifications required for incorporating the LANCE error conditions into the host processor error detection and reporting software. Because the routines deal specifically with the LANCE, this software encompasses only the first two layers of the ISO/OSI model, the software for covering the upper layers can be defined by the user to fit a specific application. This allows a great deal of flexibility of design for the LANCE interface with any host over a wide spectrum of applications.

LANCE and 8 Bit Microprocessors

Until this point in the discussion, only 16 bit microprocessor interfaces have been discussed. Some designers may desire to create an Ethernet node using an 8 bit microprocessor as the node processor element. Although the LANCE data bus is based on a 16 bit architecture, a minimal amount of extra logic is required to translate the 16 bit system data bus onto an eight bit data bus. Most of the 8 bit microprocessors run at much slower clock speeds than their 16 bit counterparts. In order to compensate for a slow CPU clock, it may be necessary to consider an alternate architecture for the node. In Figure 10, the typical node architecture is shown. The LANCE is tied to a system bus, shares the system memory and can communicate with the host CPU. The CPU performs both the host system functions, and the node processor functions. Figure 11 shows a possible alternate architecture where a second CPU has been added strictly for the purpose of performing network node processor functions. A separate memory is also provided for the LANCE's DMA operations and buffer management.

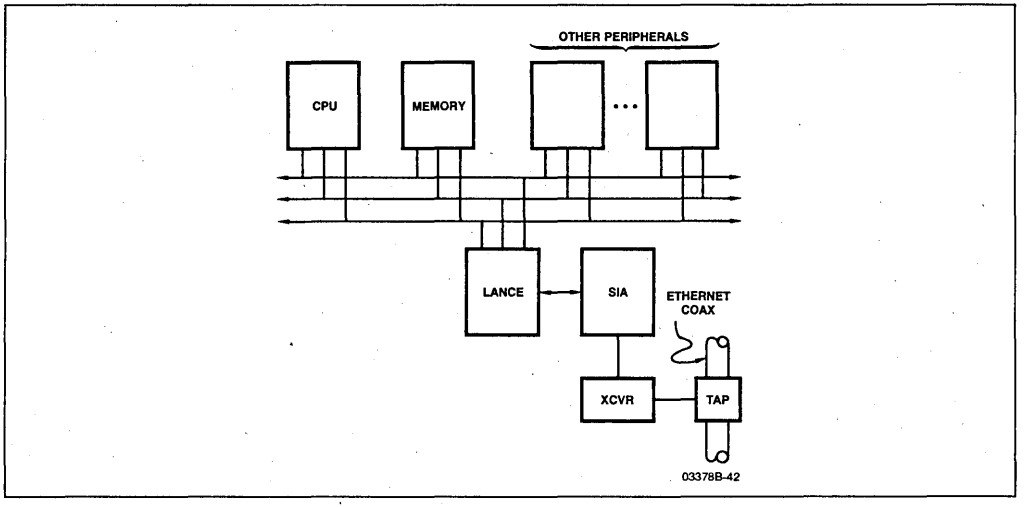


Figure 10. Typical Node Architecture Using an Am7990

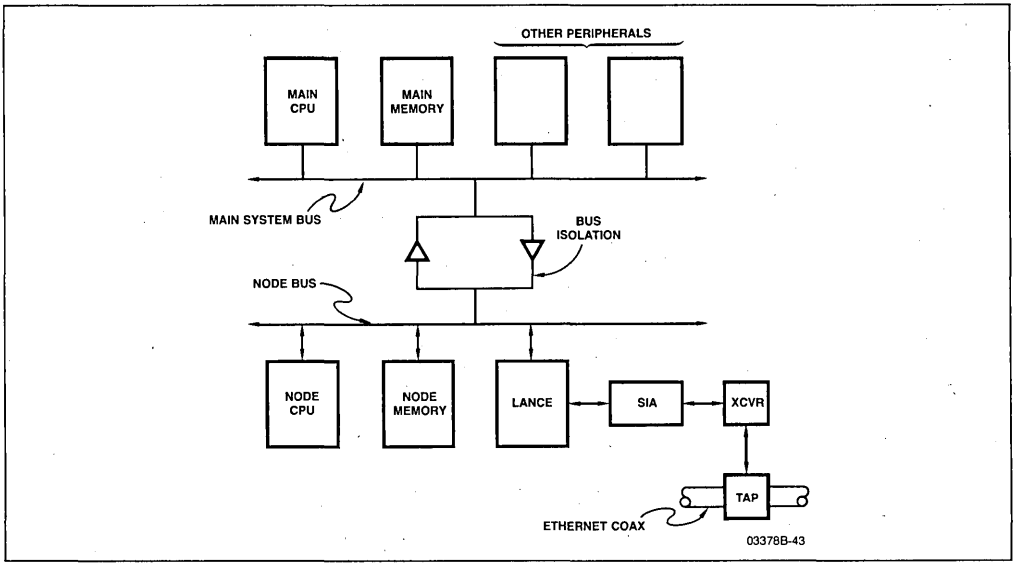


Figure 11. Alternate Node Architecture Using an Am7990 and a Separate CPU for a Node Processor

The node processor communicates with the main CPU across an isolating link which ties the node processor bus to the system bus.

Since the LANCE has a 16 bit data bus, part of the data going between the LANCE and the CPU must be latched so that the data always arrives at its destination in proper format (8 or 16 bit parallel). Figure 12 shows a block diagram of a possible interface between the LANCE and the 8088 microprocessor. This interface is exactly the same as that between the LANCE and the A8086 except that with the 8088 extra latches and buffers are employed to connect the 8 bit microprocessor to a 16 bit data bus. This scheme of interconnection requires that a double read and double write be made during data transactions between the host processor and the LANCE. This extra overhead in the software can cause problems in the system's ability to operate in real time. The maximum time allowed for interrupt service latency is 44.8us. It is therefore desirable to choose a processor whose clock rate is fast enough to avoid violating this interrupt service latency.

The importance of this concept can be conveyed through an example. As an example, an 8088 is used as the host processor and the interface between it and the LANCE is constructed as shown by the block diagram of Figure 12. Using the interrupt service routine flow chart of Figure 7, code is produced to service interrupts coming from the LANCE. The worst case timing for execution of this code is 211 clock cycles which translates to 42.2 us for a 5MHz 8088 and 26.38 us for the 8MHz version. The 8MHz 8088 offers a greater time margin between packets when servicing interrupts over the 5MHz 8088. This time margin can be translated into more reliable operation on the network.

Another point to consider is that of interrupt latency. Earlier, we defined interrupt service latency as the time required to service an interrupt in software. Interrupt latency, on the other hand, is the time the processor requires to respond to the interrupt. In the 8088 example, the worst case interrupt latency specified by the manufacturers is two instructions.

In a single processor environment, it is possible that the processor could be executing some complex instructions at the interrupt and take between 100 and 200 clock cycles just to respond to the interrupt. it. By employing the alternate architecture of Figure 11, certain tasks can be partitioned thus avoiding interrupt latency problems. When considering an 8 bit processor for use with the LANCE, the processor must have a clock rate greater than or equal to 5MHz and the designer should construct the system software to minimze the occurance of missed packets due to interrupt latency.

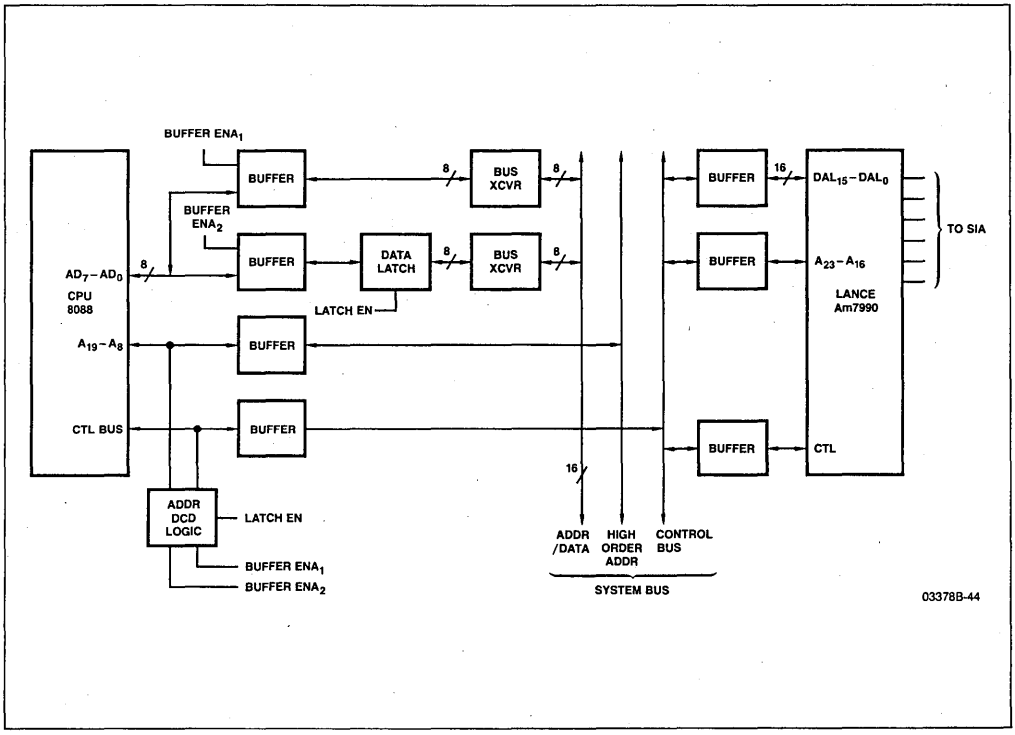


Figure 12. Am7990 (LANCE)/8088 Interface Block Diagram

LANCE Emulator

Associated Computer Consultants

DISTINCTIVE CHARACTERISTICS

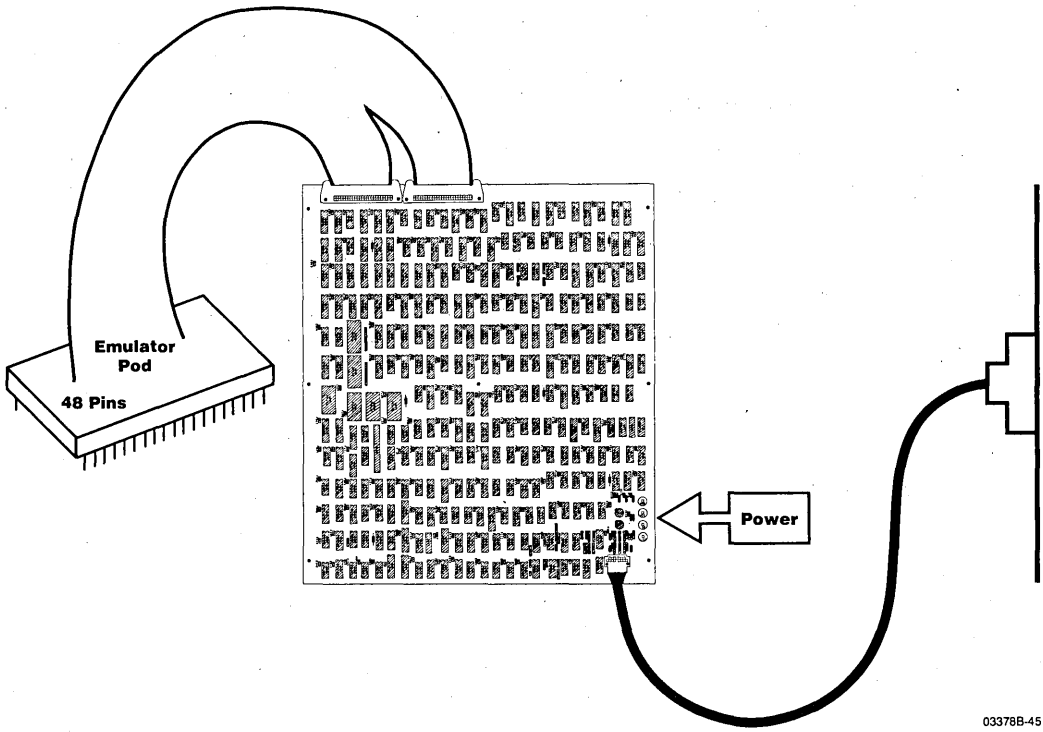
- Real time emulation of LANCE and SIA
- Direct connection to Ethernet transceiver
- Compatible with 8086, Z8000*, 68000, LSI-11**
- 15″ x 17″ printed circuit board for bench top use
- 20″ connector cable with Am7990 LANCE pin-outs
- Power consumption 5 volts at 12 amp, −5V at 0.1 amp, 12V at 0.4 amp
- Fully documented and supported

GENERAL DESCRIPTION

The ACC LANCE Emulator is an in circuit, real time Emulator for the Am7990 LANCE and Am7991 SIA. The Emulator may be used to facilitate both hardware and software development in advance of silicon allowing a shortened time-to-market for Ethernet systems using the AMD chip set.

The 15″ x 17″ printed circuit board has legs and is designed for bench top use. A 20″ cable terminates in a pod with LANCE pin-outs. The pod may be plugged directly into a LANCE socket on the prototype facilitating both hardware design and testing. The pod also may be plugged into a LANCE Development Module (LDM) to provide a complete software and test environment.

BLOCK DIAGRAM



*Z8000 is a trademark of Zilog, Inc.
**LSI-11 is a registered trademark of Digital Equipment Corp.

LANCE Development Module for Multibus

LDM-1

Communication Machinery Corporation

1226 Anacapa
Santa Barbara, California 93101
(805) 963-9679

DISTINCTIVE CHARACTERISTICS

- Provides complete Ethernet test and software development environment for Multibus* applications
- 32K bytes RAM buffers Ethernet data
- Connects into a fully operational Ethernet Controller
- Receives ACC LANCE Emulator to allow upper level protocol and system development
- Menu-driven English response/query software/firmware provides:
  - Debug monitor
  - LANCE/Emulator initialization and operational tests
  - Network testing and evaluation
- Up/down load link simplifies system software development

GENERAL DESCRIPTION

The LANCE Development Module (LDM) and its firmware provide a complete test and development environment for Ethernet systems using the Am7990 LANCE. The LDM interfaces directly to the Multibus, provides 32K bytes of RAM for additional buffering and has sockets for the Am7990 LANCE and Am7991 SIA (AMD Ethernet Controller Chip Set). When the LANCE and SIA are installed in the LDM, it becomes a fully functional Ethernet Controller for Multibus applications.

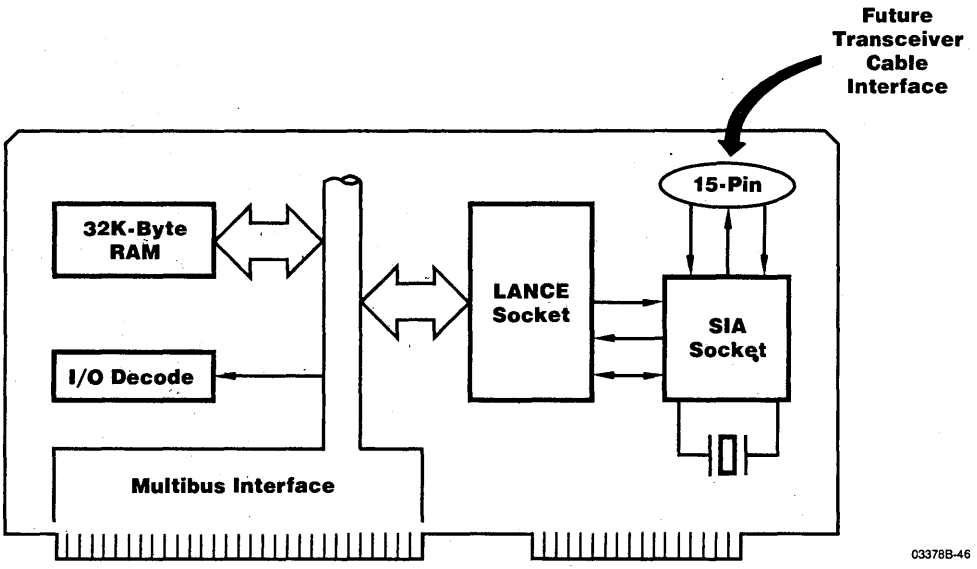
The LANCE socket also accepts the ACC LANCE Emulator. This combination of products provides a complete, low cost Ethernet development package allowing the designer to concentrate on system design, upper level protocol development, LANCE application packages and prototyping.

LANCE Development Firmware has been designed with three elements: Debug monitor, LANCE testing, network testing. The code is menu-driven, with English response/query, and is available in ROM for:

- 8086
- Z8000
- 68000

The LDM-1 is designed to be used in a Multibus development system, supported by an 8086 CPU, in an 8612-type processor board, with power supply and backplane.

BLOCK DIAGRAM



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*Multibus is a registered trademark of Intel Corp.

Firmware Summary

Debug Monitor

- Allows higher level protocol development
- Has all the standard debugger features, including multiple breakpoints, memory display and modify, register display and modify, download, single step

LANCE Test Features

- Internal RAM
- Registers
- Silo
- Host RAM DMA
- Control and status
- Initialization
- Internal or external loopback
- Descriptor rings
- Promiscuous/chaste mode
- Collision handling
- Disable feature

Network Test Features

- Message Generation Mode allows LANCE and network statistics gathering, and external Ethernet device testing
- Echo Mode allows LANCE receive mode testing, external Ethernet device testing, and network statistics gathering
- Receive and transmit throughput
- Statistics gathered:
  - Receive
    - Messages received
    - Bytes received
    - CRC errors
    - Framing errors
  - Transmit
    - Messages sent
    - Bytes sent
    - Deferrals required
    - Retries required
    - Transmit failures

LANCE Development Module for VERSAbus

LDM-2

Communication Machinery Corporation

1226 Anacapa
Santa Barbara, California 93101
(805) 963-9679

DISTINCTIVE CHARACTERISTICS

- Provides complete Ethernet test and software development environment for VERSAbus*
- 32K bytes RAM buffers Ethernet data
- Connects into a fully operational Ethernet Controller
- Receives ACC LANCE Emulator to allow upper level protocol and system development
- Menu-driven English response/query software/firmware provides:
  - Debug Monitor
  - LANCE/Emulator initialization and operational tests
  - Network testing and evaluation
- Up/down load link simplifies system software development

GENERAL DESCRIPTION

The LANCE Development Module (LDM) and its firmware provide a complete test and development environment for Ethernet systems using the Am7990 LANCE. The LDM interfaces directly to the VERSAbus, provides 32K bytes of RAM for additional buffering, and has sockets for the Am7990 LANCE and Am7991 SIA (AMD Ethernet Controller Chip Set). When the LANCE and SIA are installed in the LDM, it becomes a fully functional Ethernet Controller for VERSAbus applications.

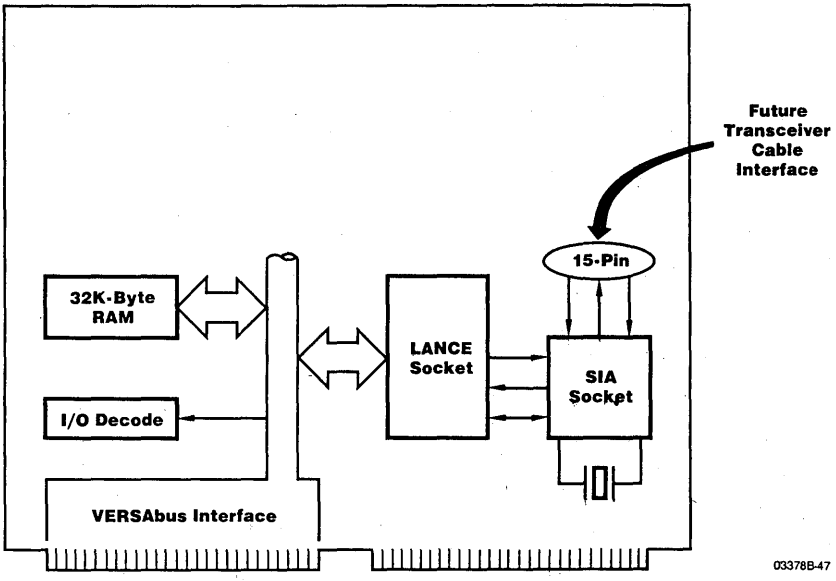
The LANCE socket also accepts the ACC LANCE Emulator. This combination of products provides a complete, low cost Ethernet development package allowing the designer to concentrate on system design, upper level protocol development, LANCE application packages and prototyping.

LANCE Development Firmware has been designed with three elements: Debug monitor, LANCE testing, network testing. The code is menu-driven, with English response/query, and is available in ROM for:

- 8086
- Z8000
- 68000

The LDM-2 conforms to VERSAbus, supported by a 68000 CPU in a VM02-type processor board, with VERSAchassis* .

BLOCK DIAGRAM



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*VERSAbus and VERSAchassis are trademarks of Motorola, Inc.

Firmware Summary

Debug Monitor

- Allows higher level protocol development
- Has all the standard debugger features, including multiple breakpoints, memory display and modify, register display and modify, download, single step

LANCE Test Features

- Internal RAM
- Registers
- Silo
- Host RAM DMA
- Control and status
- Initialization
- Internal or external loopback
- Descriptor rings
- Promiscuous/chaste mode
- Collision handling
- Disable feature

Network Test Features

- Message Generation Mode allows LANCE and network statistics gathering, and external Ethernet device testing
- Echo Mode allows LANCE receive mode testing, external Ethernet device testing, and network statistics gathering
- Receive and transmit throughput
- Statistics gathered:
  - Receive
    - Messages received
    - Bytes received
    - CRC errors
    - Framing errors
  - Transmit
    - Messages sent
    - Bytes sent
    - Deferrals required
    - Retries required
    - Transmit failures

Communications Products – Section IX

Statement of Excellence

AMD is revolutionizing the state-of-the-art in communications components for both voice and data. Utilizing a philosophy of implementing VLSI solutions in silicon, the Am7901 SLAC and Am7910 FSK MODEM are the most powerful, and yet cost effective, devices of their kind on the market today.

This is made possible by AMD's innovative application of Digital Signal Processing techniques. DSP sets a new cost/performance standard for the communications industry and means increased performance through the flexibility of microprogrammable features. DSP means increased system reliability due to its inherent superior stability with time and temperature, and DSP means lower cost application due to the elimination of external components, reduction of board space, and reduced test costs.

AMD's communications products meet the exacting demands of the largest telecom equipment manufacturers around the world. In addition, through simple programmable commands, both the Am7901 and the Am7910 can be configured to meet respective equipment standards anywhere in the world. That's why we call each of them a WORLD-CHIP™.

*WORLD-CHIP is a trademark of Advanced Micro Devices.

Am7901

Subscriber Line Audio-Processing Circuit
WORLD-CHIP™
PRELIMINARY DATA (REVISED)

DISTINCTIVE CHARACTERISTICS

- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user programmable digital filters
  - Trans-hybrid balance
  - Two wire impedance matching
  - Transmit gain adjust
  - Transmit frequency response
  - Receive gain adjust
  - Receive frequency response
- Dynamic time slot assignment
- Only 2 external components (non-precision)
- Dual PCM ports
- Asynchronous transmit and receive operation
- 4.096MHz, 64 channel expanded mode operation
- Built-in test modes
  - Analog loopback
  - Digital loopback
  - Receive path cut-off
  - Transmit path high-pass filter disable
- Complete μP interface for line card
- Control interface to SLIC
- Low standby power
- Selectable linear or μ-law code

GENERAL DESCRIPTION

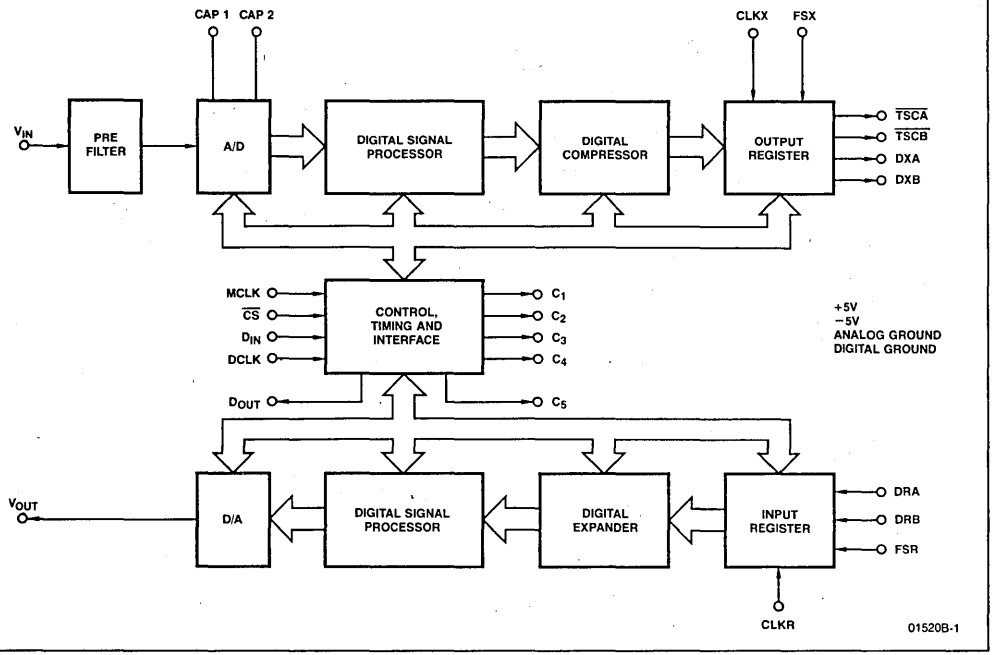
The Subscriber Line Audio-Processing Circuit (SLAC) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into PCM outputs and processes PCM inputs into analog outputs. The SLAC's performance meets or exceeds the applicable AT&T and CCITT specifications. The device consists of three main sections: a transmit processor, a receive processor and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter and a digital signal processor. The analog signals received are converted and digitally processed to generate either 16-bit linear or 8-bit μ-law codes. Either one of two output ports may be selected for PCM data transmission.

The receive section contains a digital signal processor and a D/A converter. Either 16-bit linear or 8-bit μ-law codes are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor compatible serial interface and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of commands.

BLOCK DIAGRAM



DEVICE OPERATION

General

The Am7901 performs the codec and filter functions associated with the 4-wire section of the subscriber line circuitry in a digital switch. When used with the Am7950 SLIC, the SLAC provides a complete solution to the BORSCHT functions. (See Figure 1.)

The SLAC contains auto-zeroed A/D and D/A converters. A microprocessor compatible interface is provided to program the device into a variety of modes. These operating modes include, but are not limited to μ-law or linear code operation, dynamic time slot assignment, and PCM port selection.

The SLAC samples the analog signal at the V_{IN} pin and digitally processes it to produce either a linear or companded (μ-law) PCM code at the DXA or DXB output. Conversely, it receives either a linear or companded (μ-law) PCM code at the DRA or DRB input and digitally processes it to produce an analog output at the V_{OUT} pin. The processing is accomplished at the frame rate (8kHz), and the digital output/input is available for transmission/reception every 125μs. The main sections of the SLAC are shown in Figure 2.

Transmit Signal Processor

In the transmit path, the analog signal is converted, filtered, compressed and made available for output. The transmit signal processing path is shown in Figure 3.

The prefilter is an integrated anti-aliasing filter which prevents signals near the sample rate from folding back into the voiceband during decimation. The A/D is designed to have a wide dynamic range and excellent signal to noise performance. It uses a modified sigma delta loop with a D/A converter to track the input signal at a 512kHz sampling rate.

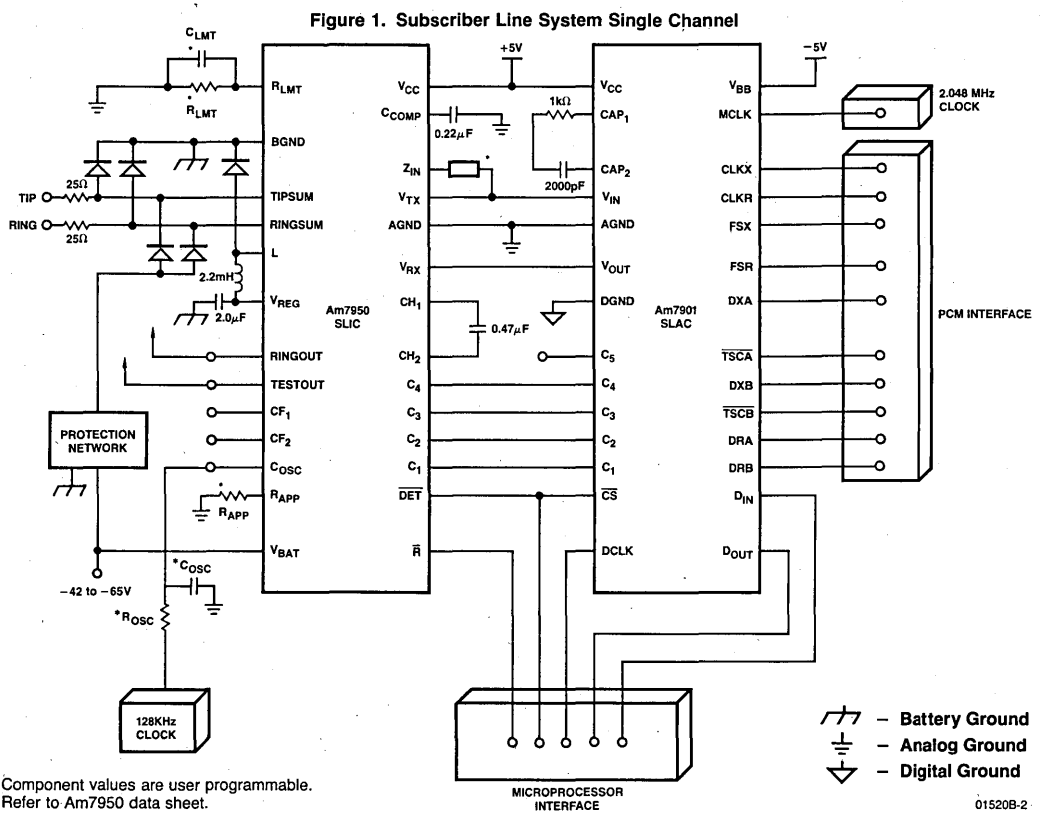
The signal processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The B, X and GX blocks shown in Figure 3 are user programmable filter sections and their coefficients are stored in the Coefficient RAM. These filters may be made transparent when not required in a system. The digital μ-law compressor may be bypassed when linear code operation is desired.

The decimator reduces the high input sample rate.The X filter is a 4 tap FIR section and is part of the frequency response correction network. The GX filter allows the user to program up to 12dB gain in 0.1dB steps in the transmit path. The B filter has 8 taps and operates on samples input from the Receive Signal Processor in order to provide trans-hybrid balancing in the loop. The low pass filter limits the output bandwidth to meet the transmission requirements. The high pass filter rejects 15Hz and 50/60Hz frequencies, and may be disabled during idle periods to allow low frequency leakage testing on the 2 wire line.

Transmit PCM Interface

The Transmit PCM Interface receives either a 16-bit linear code (for linear operation) or an 8-bit compressed code (for μ-law operation) from the digital compressor. This code is loaded into the output register. The Transmit PCM interface logic (Figure 4) controls the transmission of data onto the PCM highway through the output port selection circuitry and the time slot control block.

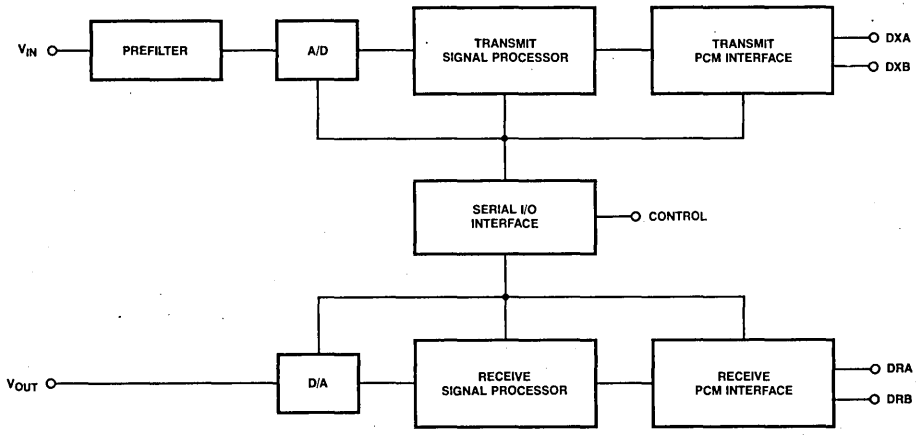
Figure 1. Subscriber Line System Single Channel



*Component values are user programmable. Refer to Am7950 data sheet.

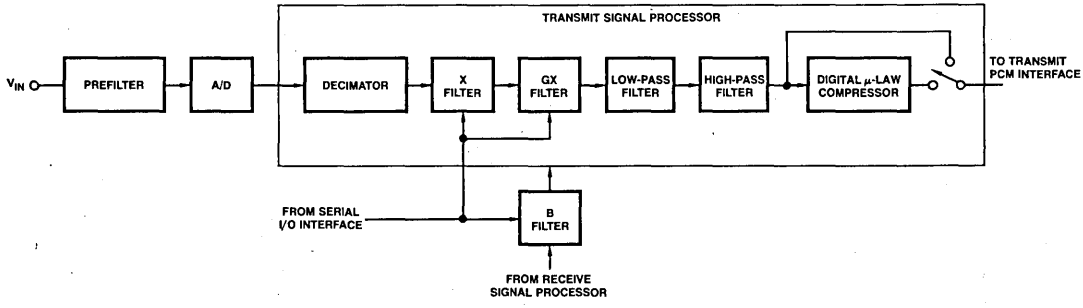
01520B-2

Figure 2. SLAC Block Diagram



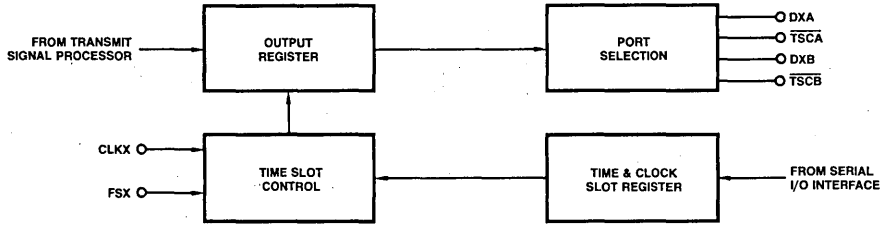
01520B-3

Figure 3. Transmit Signal Processor



01520B-4

Figure 4. Transmit PCM Interface



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The Frame Sync (FSX) pulse identifies the beginning of a Transmit frame and all channels (time slots) are referenced to it. The logic contains user programmable Transmit Time Slot and Transmit Clock Slot registers. The Time Slot register is normally 5 bits wide and allows up to 32 8-bit channels or 16 16-bit channels (using CLKX = 2.048MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give 32 16-bit channels or 64 8-bit channels (using CLKX = 4.096MHz) in each frame. This feature allows any combination of channel assignments and clock frequencies (over a range of 64kHz to 4.096MHz) in a system. For μ-law operation 8 bits/channel are output and for linear code operation 16 bits/channel are output. The data is transmitted most significant bit first. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 CLKX periods to eliminate any clock skew in the system. (See Figure 5 for timing diagrams.)

In the Am7901, the PCM data may be user-programmed to be output onto one of two ports, DXA or DXB. Correspondingly, either $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is also low.

Receive PCM Interface

The Receive PCM interface logic (Figure 6) controls the reception of data from the PCM highway and transfers it for expansion (μ-law only) to the Receive Signal Processor. The operation of this interface is identical to the Transmit section.

The Frame Sync (FSR) pulse identifies the beginning of a Receive frame and all channels (time slots) are referenced to it. (The receive path timing circuitry may be operated completely asynchronously with respect to the transmit path, except when the B or Z filter is used.) The logic contains user programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is normally 5 bits wide and allows up to 32 8-bit channels (using CLKR = 2.048MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give 32 16-bit channels or 64 8-bit channels (using CLKR = 4.096MHz) in each frame. This feature allows any combination of clock frequencies (over a range of 64kHz to 4.096MHz) and channel assignments in a system. For μ-law operation 8 bits/channel are input and for linear code 16 bits/channel are input. The most significant bit of the code must be received first. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 CLKR periods to eliminate any clock skews in the system. (See Figure 7 for timing diagrams.)

In the Am7901, the PCM data may be user-programmed to be input from one of two ports, DRA or DRB.

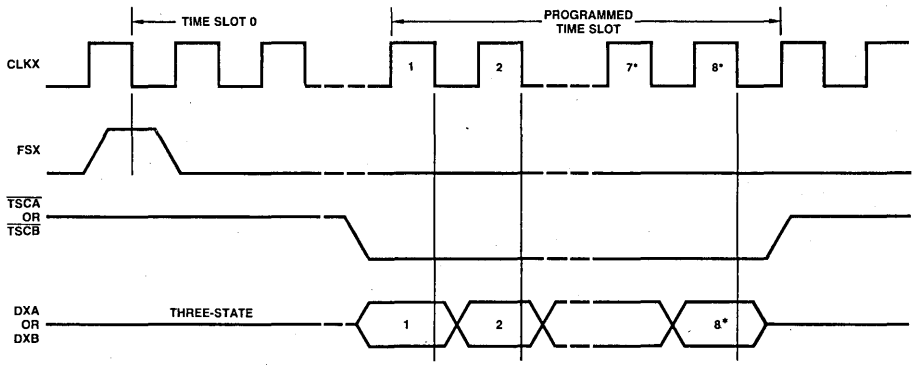
Receive Signal Processor

In the receive path, the digital signal is expanded, filtered, converted to analog and output onto the V_{OUT} pin. The signal processing path is shown in Figure 8.

The signal processor contains an ALU, RAM, ROM and Control logic to implement the filter sections. The Z, R and GR are user programmable (through the Serial I/O Interface) filter sections and their coefficients are stored in the coefficient RAM. These filters may be made transparent when not required in a system.

The low pass filter band-limits the signal. The GR filter allows the user to program a loss of up to 12dB in 0.1dB steps. The R filter is a 4 tap FIR section and is part of the frequency response correction network. The Z filter provides feedback from the Transmit Signal Processor to the Receive Signal Processor and is used to modify the effective input impedance to the system. The interpolator increases the sample rate to the D/A converter.

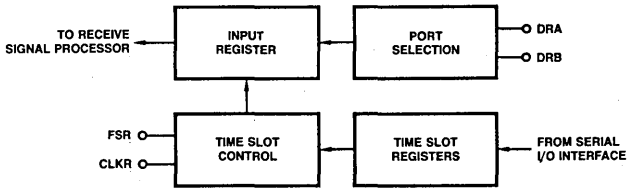
Figure 5. Transmit PCM Timing Diagram



*For Linear Code, the 7th and 8th Clock Cycles Correspond to the 15th and 16th Clock Cycles.

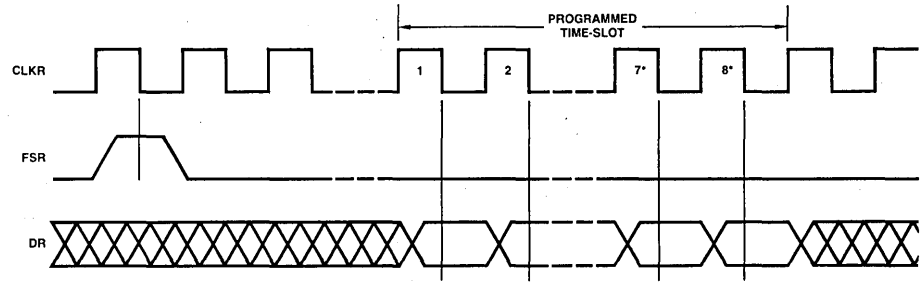
01520B-6

Figure 6. Receive PCM Interface



01520B-7

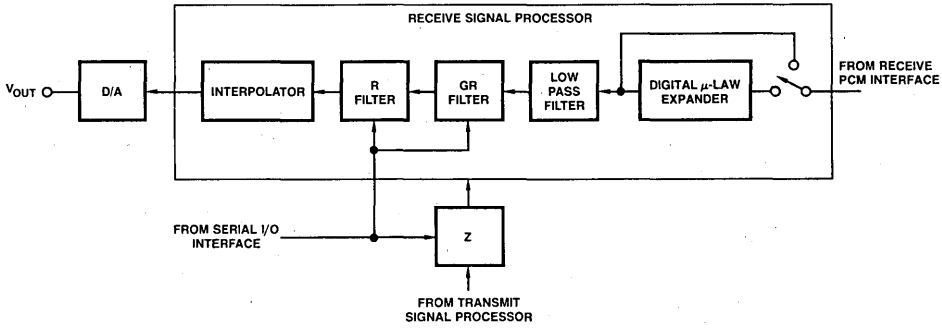
Figure 7. Receive PCM Timing Diagram



*For Linear Code, the 7th and 8th Clock Cycles Correspond to the 15th and 16th Clock Cycles.

01520B-8

Figure 8. Receive Signal Processor



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SERIAL I/O INTERFACE

A microprocessor may be used to program the SLAC and control its operation using the serial I/O Interface. (See Figure 9) Additionally, data programmed previously may be read out for verification. The control word format is shown in Table 1. Commands are provided to:

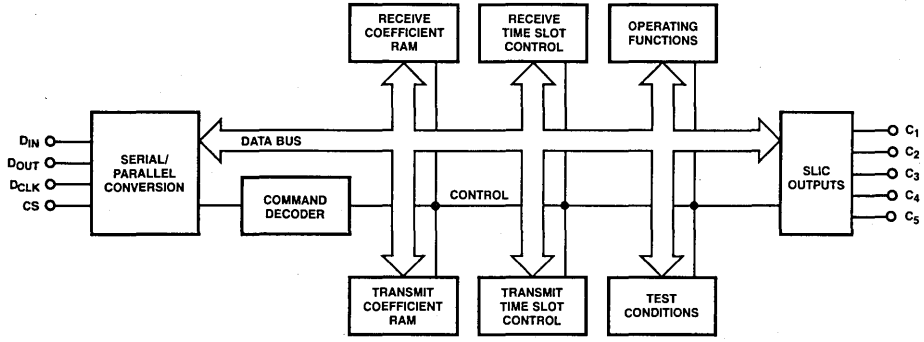
- Set power up/power down modes
- Set up test functions
- Set up operating functions
- Program filter coefficients
- Assign time slots and port selection
- Write to the SLIC latch
- Enable/Disable each user programmable filter

The interface consists of 4 pins, $\overline{CS}$, DCLK, D_{IN} and D_{OUT}. The device is accessed by $\overline{CS}$ and data is serially loaded in on the D_{IN} or read out on D_{OUT} under control of DCLK. Either commands or data words may be written to the SLAC but only data words can be read out. All words are 8 bits wide and are written or read MSB first. (See Figure 10 for the Serial I/O Interface timing diagram.)

For both reception or transmission of words, exactly 8 data clock cycles must be received after $\overline{CS}$ goes low. $\overline{CS}$ must stay high (off period) for a minimum time period before it can go low again (see "Switching Characteristics," note 4). During this off-period, the logic decodes and executes the command. All reading of data must be preceded by an input command requesting the data. Once control data transmission has begun, no new input commands will be accepted until control data transmission is completed.

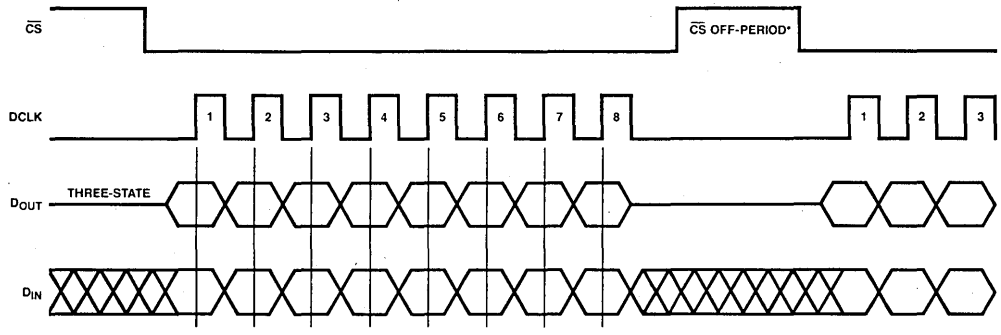
A serial I/O cycle is defined by transitions of $\overline{CS}$ and DCLK. Upon application of supply power, the device expects the first word to be a command. A number of commands require additional data words to be input or output. The SLAC will not accept new commands until all this data has been transferred. But in the write mode, a data word of all zeroes is equivalent to the power down command and the device resets to the standby mode and is ready to receive a new command.

Figure 9. Serial I/O Interface



01520B-10

Figure 10. Serial I/O Interface Timing Diagrams



*See note 4 under "Switching Characteristics."

01520B-11

DIGITAL FILTERS

The SLAC uses digital signal processing to implement the various filters as shown in Figure 11.

The advantages of digital filters are:

- high reliability
- no drift with time or temperature
- unit to unit repeatability
- superior transmission performance

Six of the digital filters in the signal processing sections are user programmable. These allow the user to independently modify the gain in both the transmit and receive paths, provide trans-hybrid balancing in the system and adjust the two wire line termination impedance. The programming capability feature allows the user to optimize the performance of the SLAC for his system. Each programmable filter section has the following type of transfer function:

$$H_z = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots\ldots + h_n z^{-n} \qquad \text{(Eq. 1)}$$

The values of the user defined coefficients (h_i) are assigned via the serial I/O interface (see Table 1). The number of taps (n) provided depends on the particular filter.

The filter function is performed by a series of multiplications and accumulations. A multiply is accomplished by shifting the multiplicand and summing the result with the previous value at that summation node. For example, a one-bit multiply is a shift of M bits where M is related to the position of the binary one in the multiplier (h_i) as expressed in the following equation:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + \ldots B_N 2^{-M_N} \qquad \text{(Eq. 2)}$$

where: $M_i \leq M_{i+1}$

$B_i = \pm 1$

The subscript N is limited to 4 for the GR, GX, R, X and Z filters and N is 3 for the B filter. The multiply is done from the least significant bit to the most significant bit. Notes 11 and 12 on page 12 explain the encoding of the shift codes.

The B, X, R, Z and Gain Coefficients are written in or read out as 8 bit words. The format of the coefficients is shown below:

a. B Coefficients

7 — 4	3 — 0	
$C_{30}m_{30}$	$C_{20}m_{20}$	← 1st word
$C_{10}m_{10}$	$C_{31}m_{31}$	← 2nd word
$C_{21}m_{21}$	$C_{11}m_{11}$	
$C_{32}m_{32}$	$C_{22}m_{22}$	
$C_{12}m_{12}$	⋮	⋮
⋮	⋮	
	$C_{37}m_{37}$	
$C_{27}m_{27}$	$C_{17}m_{17}$	← 12th word

b. X Coefficients

7 — 4	3 — 0	
$C_{40}m_{40}$	$C_{30}m_{30}$	← 1st word
$C_{20}m_{20}$	$C_{10}m_{10}$	← 2nd word
$C_{41}m_{41}$	$C_{31}m_{31}$	
$C_{21}m_{21}$	$C_{11}m_{11}$	⋮
$C_{42}m_{42}$	$C_{32}m_{32}$	
$C_{22}m_{22}$	$C_{12}m_{12}$	
$C_{43}m_{43}$	$C_{33}m_{33}$	
$C_{23}m_{23}$	$C_{13}m_{13}$	← 8th word

c. R, Z Coefficients

7 — 4	3 — 0	
$C_{43}m_{43}$	$C_{33}m_{33}$	← 1st word
$C_{23}m_{23}$	$C_{13}m_{13}$	
$C_{42}m_{42}$	$C_{32}m_{32}$	
$C_{22}m_{22}$	$C_{12}m_{12}$	⋮
$C_{41}m_{41}$	$C_{31}m_{31}$	
$C_{21}m_{21}$	$C_{11}m_{11}$	
$C_{40}m_{40}$	$C_{30}m_{30}$	
$C_{20}m_{20}$	$C_{10}m_{10}$	← 8th word

d. Gain Coefficients

7 — 4	3 — 0	
$C_{40}m_{40}$	$C_{30}m_{30}$	← 1st word
$C_{20}m_{20}$	$C_{10}m_{10}$	← 2nd word

C_{xy} m_{xy} = C is the sign bit and m is the 3-bit code specifying the position of the 1's.
y is the coefficient number
x specifies the relative position of the one in coefficient Y (1 = most significant one, 2 = second one, etc.).

and the coefficients in Equation 1 shown above are described by:

$$h_i = \left(C_{1i} \cdot 2^{-\hat{m}_{1i}}\left(1 + C_{2i} \cdot 2^{-\hat{m}_{2i}}\left(1 + C_{3i} + 2^{-\hat{m}_{3i}}\right.\right.\right.$$
$$\left.\left.\left.(1 + C_{4i} \cdot 2^{-\hat{m}_{4i}})\right)\right)\right)$$

except for the G_x filter where

$$h_i = 1 + \left(C_{1i} \cdot 2^{-\hat{m}_{1i}}\left(1 + C_{2i} \cdot 2^{-\hat{m}_{2i}}\left(1 + C_{3i} \cdot 2^{-\hat{m}_{3i}}\right.\right.\right.$$
$$\left.\left.\left.(1 + C_{4i} \cdot 2^{-\hat{m}_{4i}})\right)\right)\right)$$

where $\hat{m}_{ij} = 7 - m_{ij}$

Two Wire Impedance Matching

A feedback path is provided from the transmit to the receive section via the Z filter. This filter may be programmed to modify the effective termination impedance (Z_{SLIC}) of a SLIC or a transformer hybrid to a desired value. The desired impedance may be complex. This feature allows the user to terminate each SLIC in a Subscriber Line System with a fixed resistor and digitally modify their impedance using the Z filter.

The X and R filters are the Transmit and Receive attenuation distortion correction filters. These filter sections are programmed to compensate the attenuation distortion caused by the Z filter.

Trans-hybrid Balance

In a traditional line card system, a balance network is used with the SLIC to achieve trans-hybrid balancing. If the balance network perfectly matches the subscriber's line, infinite trans-hybrid balancing is achieved. But in general, the matching in traditional systems is poor and trans-hybrid balancing is not very good. Some systems have up to 2 or 3 compromise networks per line that must be selected semi-automatically or manually to provide the balance.

In the SLAC, a feedback path is provided from the receive to the transmit section via the B filter. This filter may be programmed to cancel the received signal from the transmit signal path and achieve a significantly improved level of trans-hybrid balance.

Gain Adjustment

Signal levels in the transmit and receive paths may be modified by programming the GX and GR filters. The GX filter allows the user to add up to 12dB of gain (in 0.1dB steps) in the transmit path. The GR filter allows the user to add up to 12dB of loss (in 0.1dB steps) in the receive path.

Asynchronous Operation

The transmit and receive PCM sections may be operated asynchronously. Each section receives a separate frame sync (FSX, FSR) and clocks (CLKX, CLKR).

Test Features

The SLAC simplifies system testing by providing both digital and analog loop back paths. Under program control, either the DRA or DRB input is looped to the DXA or DXB output (digital loopback) or the V_{IN} input is looped to the V_{OUT} output (analog loopback) through internal paths. To allow testing of the subscriber loop cabling for leakage, the transmit high pass filter may be disabled and auto zero operation interrupted. The receive analog output may be programmed to cut-off. This receive cut-off command may be used to stop oscillations in the four-wire side of the telephone network.

Standby Mode

The SLAC is forced into the standby mode either by power on clear or by reception of the power down code. In this mode, power is switched off from all circuitry that can be turned off. No transmission or reception of PCM data takes place. However, the circuits which contain programmed information retain their data. The serial I/O interface remains active to receive new commands.

Power On Clear

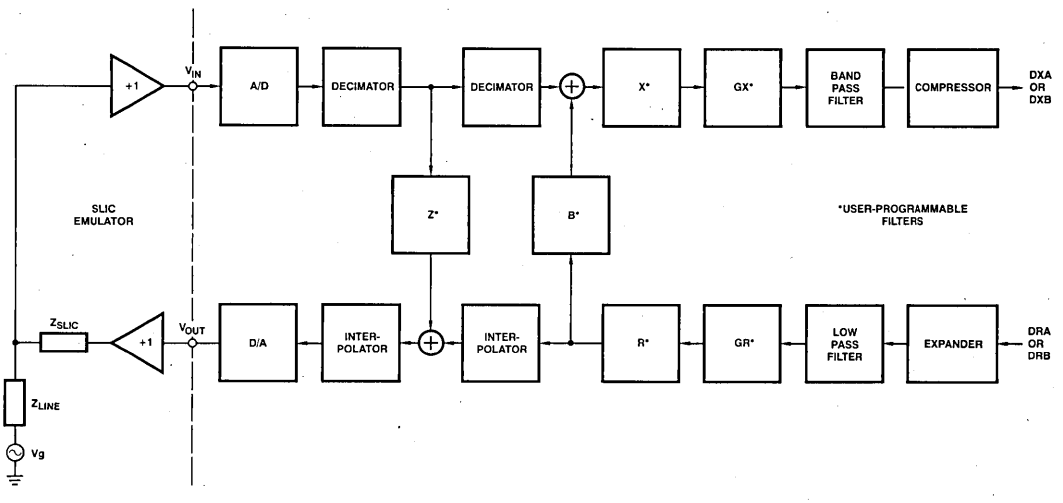
Upon initial application of V_{CC} and V_{BB}, the SLAC is forced into the standby mode. Additionally, once both power supplies are up, if either supply falls below (voltage to be defined) then the SLAC is reset (See Stand-Alone Mode) and is forced into the standby mode.

Stand Alone Mode

In the stand alone mode, the serial interface is not used. The DCLK and D_{IN} pins may be used to control the device. Applying −5V to the DCLK pin resets the device and the D_{IN} pin can subsequently be used to power up or power down the SLAC.

DCLK	D_{IN}	
0	X	Normal mode
1	X	Normal mode
−5V	0	Reset and Power Down
−5V	1	Reset and Power Up

Figure 11. SLAC Signal Processing Flow



The Reset State of the device is:

a) Both Transmit and Receive Time and Clock Slots are set to zero.
b) μ-law is selected
c) B, X, R, Z filters are disabled
d) Both Transmit (GX) and Receive (RX) gains are set to unity
e) SLIC outputs are set high
f) Normal conditions are selected (see Note 9 page 12 – Command Word Format)
g) DXA/DRA ports are selected

μ-Law Conversion Codes

For μ-law operation, the SLAC has a transfer function which complies with the Bell System μ-255 companding law:

$$Y = 0.18 \ln (1 + \mu |X|) \operatorname{sgn} (X)$$

where:
- X = the input signal
- sgn(X) = sign of input signal
- |X| = absolute value of input signal
- μ = 255
- Y = encoder output or decoder input

The resultant output consists of 15 segments or chords. The chords are identified with the sign bit and three chord select bits. Each chord is further divided into 16 steps using 4 bits.

Linear Conversion Codes

For linear code operations, 16-bit words are transmitted or received. The linear code transmitted or received has sign plus 15 bits and one's complement coding is used. The following table illustrates the dynamic range of the linear code.

Positive Output Codes	Negative Output Codes	Normalized Absolute Value
0 1111110 00000000	1 0000001 11111111	32 256
–	–	–
–	–	–
–	–	–
–	–	–
0 0000000 00000001	1 1111111 11111110	1
0 0000000 00000000	1 1111111 11111111	0

Correspondance of the linear code to the μ-law code is demonstrated by the following table for the 1KHz digital milliwatt (0dBmO) signal.

μ-Law							
1	2	3	4	5	6	7	8
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

Linear															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	1	0	1	1	0	0	0	0	0	1	1
1	0	1	0	1	1	1	0	1	0	0	0	0	0	1	1
1	0	1	0	1	1	1	0	1	0	0	0	0	0	1	1
1	1	0	1	1	1	0	1	1	0	0	0	0	0	1	1
0	0	1	0	0	0	1	0	0	1	1	1	1	1	0	0
0	1	0	1	0	0	0	1	0	1	1	1	1	1	0	0
0	1	0	1	0	0	0	1	0	1	1	1	1	1	0	0
0	0	1	0	0	0	1	0	0	1	1	1	1	1	0	0

μ-LAW: POSITIVE INPUT VALUES

1	2	3	4	5	6	7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n (1)	Character Signal(5) Bit Number 1 2 3 4 5 6 7 8	Value at Decoder Output y_n (3)	Decoder Output Value Number
		8159	(128)	(8159)			
			127	7903	1 0 0 0 0 0 0 0	8031	127
8	16 x 256		⋮	⋮	⋮ (2)	⋮	⋮
			113	4319	1 0 0 0 1 1 1 1	4191	112
		4063	112	4063			
7	16 x 128		⋮	⋮	⋮ (2)	⋮	⋮
			97	2143	1 0 0 1 1 1 1 1	2079	96
		2015	96	2015			
6	16 x 64		⋮	⋮	⋮ (2)	⋮	⋮
			81	1055	1 0 1 0 1 1 1 1	1023	80
		991	80	991			
5	16 x 32		⋮	⋮	⋮ (2)	⋮	⋮
			65	511	1 0 1 1 1 1 1 1	495	64
		479	64	479			
4	16 x 16		⋮	⋮	⋮ (2)	⋮	⋮
			49	239	1 1 0 0 1 1 1 1	231	48
		223	48	223			
3	16 x 8		⋮	⋮	⋮ (2)	⋮	⋮
			33	103	1 1 0 1 1 1 1 1	99	32
		95	32	95			
2	16 x 4		⋮	⋮	⋮ (2)	⋮	⋮
			17	35	1 1 1 0 1 1 1 1	33	16
		31	16	31			
1	15 x 2		⋮	⋮	⋮ (2)	⋮	⋮
			2	3	1 1 1 1 1 1 1 0	2	1
	1 x 1		1	1	1 1 1 1 1 1 1 1		
			0	0		0	0

Notes:
1. 8159 normalized value units correspond to T_{MAX} = 3.17 dBmO.
2. The character signal corresponding to positive input values between two successive decision values numbered n and $n + 1$ (see column 4) is $(255 - n)$ expressed as a binary number.
3. The value at the decoder output is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_{n+1}}{2}$ for $n = 1, 2, \ldots, 127$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

TABLE I: CONTROL WORD FORMAT

The control interface consists of data input, data output, data clock and $\overline{CS}$ input. Data is read in (read out) on the serial data input (output). The serial input consists of 8 bit (byte) command words which may be followed with additional bytes of input data or may be followed by the SLAC outputting bytes of data. All words are input with MSB (D_7) first and LSB (D_0) last and all outputs are output with the MSB (D_7) first and the LSB (D_0) last. Words are written or read one at a time, with $\overline{CS}$ going high for at least the minimum off-period (see note 4 under "Switching Characteristics") before the next read or write operation. The first 3 bits of the command word indicate the type of command and the last 5 bits contain either data or further information about the command. The classes of command are:

D_7 D_6 D_5	
0 0 0	Power Down/No Operation
0 0 1	Transmit Time Slot Selection
0 1 0	Receive Time Slot Selection
0 1 1	Clock Slot and Gain Selection Read Slot,Gain and PCM Mode
1 0 0	Set Basic and Operating Functions and PCM Modes
1 0 1	Read/Write Coefficients, Set Test Modes, Select μ-law/Linear code
1 1 0	Data for SLIC Interface
1 1 1	Power Up/No Operation

MSB D_7 D_6 D_5	D_4 D_3 D_2 D_1 D_0 LSB		
0 0 0	0 0 0 0 0	Power Down[1]	
0 0 0	X X X X X	Reserved	
0 0 1	Y Y Y Y Y	Transmit Time Slot Selection[3]	Choose 1 of 32 Time Slots
0 1 0	Y Y Y Y Y	Receive Time Slot Selection[3]	Choose 1 of 32 Time Slots
0 1 1	0 0 Y Y Y	Transmit Clock Slot Selection[3]	Choose 1 of 8 Clock Slots
0 1 1	0 1 Y Y Y	Receive Clock Slot Selection[3]	Choose 1 of 8 Clock Slots
0 1 1	1 0 0 1 0	Transmit Gain Selection	Followed by 2 Bytes of Data[4]
0 1 1	1 1 0 1 0	Receive Gain Selection	Followed by 2 Bytes of Data[4]
0 1 1	1 0 1 0 1	Read Transmit Time and Clock Slot[5]	Followed by 1 Byte of Data[4]
0 1 1	1 0 0 0 1	Read Transmit Gain	Followed by 2 Bytes of Data[4]
0 1 1	1 1 1 0 1	Read Receive Time and Clock Slot[5]	Followed by 1 Byte of Data[4]
0 1 1	1 1 0 0 1	Read Receive Gain	Followed by 2 Bytes of Data[4]
0 1 1	1 0 1 1 1	Read PCM Mode	Followed by 1 Byte of Data[4, 6]
1 0 0	0 A B C D	Operating & Basic Function[7]	
1 0 0	1 E F G H	PCM-Mode Selection[8]	
1 0 1	0 0 0 0 0	Write B Coefficients	Followed by 12 Bytes of Data[4, 12]
1 0 1	0 0 1 0 0	Write X Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 1 0 0 0	Write R Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 1 1 0 0	Write Z Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 0 0 1 1	Read B Coefficients	Followed by 12 Bytes of Data[4, 12]
1 0 1	0 0 1 1 1	Read X Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 1 0 1 1	Read R Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 1 1 1 1	Read Z Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	1 0 0 0 0	Reset to normal conditions[9]	
1 0 1	1 0 0 0 1	Add −6 dB to receive gain	
1 0 1	1 0 0 1 0	Cutoff receive path	
1 0 1	1 0 1 1 1	Test mode – analog loop back	
1 0 1	1 0 1 0 0	Test mode – digital loop back[13]	
1 0 1	1 0 0 1 1	Disable High Pass Filter (set to 1) and freeze auto zero circuit	
1 0 1	1 1 0 0 0	Choose Linear code	
1 0 1	1 1 0 0 1	Choose μ-law	
1 1 0	I J K L M	Outputs to SLIC[10]	
1 1 1	X X X X X	Reserved	
1 1 1	1 1 1 1 1	Power Up[1]	

NOTES:

1. During power down none of the control information is changed, the serial I/O remains active, the PCM outputs are high impedance, the PCM inputs are disabled and the analog output is set to zero with a moderate series impedance to analog ground. Upon power up all data RAMs except the coefficient RAMs are powered up in a cleared state (set to all zeroes). No PCM data is transmitted until after the second FSX pulse is received following the execution of the power up command.
2. These reserved codes are all codes beginning with 000 and 111 except for 00000000 (power down) and 11111111 (power up). These codes may be used by future members of this product family.
3. The Y's are binary codes which program the time slots for transmission and reception of PCM date. Five bits are available for time slot selection which allow one of 32 time slots to be programmed. The three bits of the clock slot selection allow 0 to 7 clock offsets within the time slot to be programmed.
4. All commands that are followed by additional input data to the device (transmit gain selection, receive gain selection, write B, Z, X or R coefficients) must have the input data as the next N words (N = 1, 2, 8, 12) written to the device (framed by the next N transitions of $\overline{CS}$). All commands that are followed by output data (read transmit time and clock slot, read transmit gain, read receive time and clock slot, read receive gain, read PCM mode, read B, Z, X or R coefficients) will cause the device to output data for the next N (N = 1, 2, 8, 12) transitions of $\overline{CS}$ going low and will not accept any input commands until all the data has been output. When in an input mode, data word of 00000000 will automatically power down the device and write 00000000 to the last filter location.
5. Time and clock slots are read out time slot first followed by clock slot.
6. The PCM Modes are read out as the least significant 4 bits of data. The most significant 4 bits are set to 1. The least significant 4 bits contain the following data:

   BIT 3: Data Receive select bit
   BIT 2: Data Transmit select bit
   BIT 1: Receive Expanded Mode bit
   BIT 0: Transmit Expanded Mode bit

   The Data Receive/Transmit select bits define which port is used to receive/transmit data. A 0 means port A has been selected. A 1 means port B has been selected.

   The Receive/Transmit Expanded Mode bits allow up to 64 channels in a Receive/Transmit frame.
7. The operating function command has four 1-bit fields:

   A: A = 1 enables B filter, A = 0 disables B (sets B = 0)
   B: B = 1 enables X filters, B = 0 disables X (sets X = 1)
   C: C = 1 enables R filter, C = 0 disables R (sets R = 1)
   D: D = 1 enables Z filter, D = 0 disables Z (sets Z = 0)
8. The Transmit PCM data may be output onto either the DXA or the DXB port. Either $\overline{TSCA}$ or $\overline{TSCB}$ is correspondingly output. The Receive PCM data may be input onto either the DRA or the DRB port. The Transmit/Receive Expanded Mode bits allow up to 64 channels in Transmit/Receive frame.

   E: E = 1 chooses DRB, E = 0 chooses DRA
   F: F = 1 chooses DXB ($\overline{TSCB}$), F = 0 chooses DXA ($\overline{TSCA}$)
   G: G = 1 sets Receive Expanded Mode bit
      G = 0 clears Receive Expanded Mode bit
   H: H = 1 sets Transmit Expanded Mode bit
      H = 0 clears Transmit Expanded Mode bit
9. Normal conditions are receive gain set to value stored in the receive gain control words, the receive path and high pass filter are enabled and the auto-zero-circuit operates, Z filter coefficients are the value set by the basic and operating function bit D and the device is not in a test mode (no loop back). The test modes are mutually exclusive. Entering a command to set one test mode clears the other test mode (if set). "Reset to normal conditions" does reset a test mode.
10. The outputs to the SLIC are defined below:

    I = C5 L = C2
    J = C4 M = C1.
    K = C3
11. X, R, and Z coefficients are allowed to have only 1 to 4 ones. Each coefficient is encoded in a four bit code where the lower 3 bits represent the number of shifts to the next higher one in the coefficient and the first bit (MSB) defines the coefficient sign. Each one can be either positive or negative (0 = positive, 1 = negative). The maximum number of shifts allowed is 6. The lower 3 bits are encoded for 0(111), 1(110), 2(101), 3(100), 4(011), 5(010) or 6(001) shifts. A code of 1000 implies 0 shifts and no addition and a code of 0000 is not allowed (See note 4). The 4 coefficients use 16 4-bit codes which are input as 8 8-bit words starting with coefficients 0 and ending with coefficient 3X for the X coefficients. The R and Z filter coefficient data starts with coefficient 3 and ends with coefficient 0.
12. B coefficients are allowed to have only 1 to 3 ones. Each coefficient is encoded in a four bit code where the lower 3 bits represent the number of shifts to the next higher one in the coefficient and the first bit (MSB) defines the coefficient sign. Each one can be either positive or negative (0 = positive, 1 = negative). The maximum number of shifts allowed is 6. The lower 3 bits are encoded for 0(111), 1(110), 2 (101), 3 (100), 4 (011), 5 (010) or 6 (001) shifts. A code of 1000 implies 0 shifts and no addition and a code of 0000 is not allowed (See note 4). The 8 coefficients use 24 4-bit codes which are input as 12 8-bit words starting with coefficient 0 and ending with coefficient 7.
13. Digital loopback provides 6dB of gain.

INTERFACE SIGNAL DESCRIPTION

V_{CC}: +5V Power Supply
V_{BB}: −5V Power Supply
DGND: Digital Ground
AGND: Analog Ground

Analog Input (V_{IN})

The analog input is applied to the Transmit path of the SLAC. The signal is sampled, digitally processed and encoded for the PCM output.

Analog Output (V_{OUT})

The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin.

CAP_1, CAP_2

An external series resistor and capacitor are connected to these pins. These components are part of the integrator in the A/D converter. The recommended values of these non-precision components are 1k ± 5% and 2000pF ± 20%.

Master Clock (MCLK)

The Master Clock must be a 2.048MHz ± 50ppm clock input. MCLK is used by the digital signal processors and is not dependent on the PCM input and output clocks.

PCM Outputs (DXA, DXB)

The Transmit PCM data is serially fed out to either the DXA or the DXB port. The port selection is under user program control. For μ-law 8 bits are transmitted and for linear code 16 bits are transmitted. The output is available every 125μs and the data is shifted out in 8/16 bit bursts at the CLKX rate. DXA, DXB are high impedance in between bursts and also in the standby mode.

Time Slot Control ($\overline{TSCA}$, $\overline{TSCB}$)

The Time Slot Control outputs are open drain outputs and are normally high. $\overline{TSCA}$ is low when PCM data is present on the DXA output and $\overline{TSCB}$ is low when PCM data is present on the DXB output.

PCM Inputs (DRA, DRB)

The Receive PCM data is serially received from either the DRA or the DRB port. The port selection is under user program control. For μ-law, 8 bits are received and for linear code 16 bits are received. The data is received in 8 or 16-bit bursts every 125μs at the CLKR rate.

Frame Sync (FSX, FSR)

The Frame Sync pulse is an 8kHz signal which identifies the beginning of a frame. The SLAC references individual time slots with respect to the Frame Sync pulse. FSX is the transmit PCM Frame Sync and FSR is the receive PCM Frame Sync. The FSX pulse must not be longer than 8 clock periods when companded code is used and 16 clock periods when linear code is used.

PCM Clocks (CLKX, CLKR)

The PCM clocks determine the rate at which PCM data is serially shifted into or out of the PCM ports. The maximum clock frequency is 4.096MHz and the minimum clock frequency is 64kHz. CLKX determines the rate at which PCM data is transmitted. CLKR determines the rate at which PCM data is received.

Chip Select ($\overline{CS}$)

The Chip Select input enables the device to either input or output control data.

Data Input (D_{IN})

Control data is serially written via the Data Input port. The input rate is determined by the Data Clock.

Data Output (D_{OUT})

Control data is serially read via the Data Output port. The output rate is determined by the Data Clock. DOUT is high impedance when control data output is completed and $\overline{CS}$ is high.

Data Clock (DCLK)

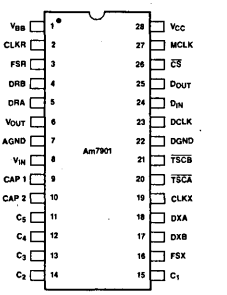
The Data Clock shifts control data either into or out of the SLAC. The maximum clock rate is 2.048MHz. and the minimum clock rate is 2kHz.

Latched Outputs (C_1-C_5)

The serial interface may be used to write data to a register whose outputs are brought out to C_1-C_5. These 5 lines are TTL compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line.

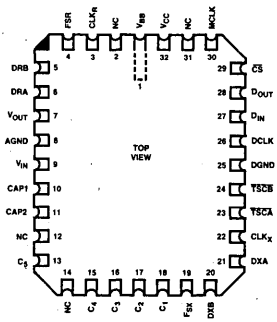
CONNECTION DIAGRAMS – Top Views

D-28-1



01520B-13

Leadless Chip Carrier
L-32-2



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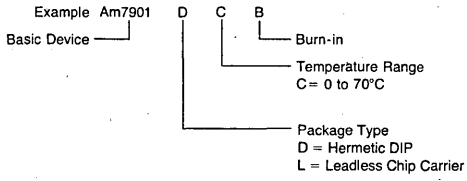
ORDERING INFORMATION



MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−60 to 125°C
Ambient Temperature, Under Bias	0 to 70°C
V_{CC} with Respect to DGND	−0.4 to +6.0V
V_{BB} with Respect to DGND	+0.4 to −6.0V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

NOTICE: Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{BB}	DGND	AGND
Am7901DC	$0°C \leq T_A \leq 70°C$	+5.0V ± 5%	−5.0V ± 5%	0V	0V ± 100mV

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

A 0dBmO signal is equivalent to 1.6 V_{RMS}. A 3dBmO signal is equivalent to 2.260 V_{RMS} which corresponds to the overload point of 3.196 V.

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Z_{IN}	Analog Input Impedance	$-3.2V < V_{IN} < 3.2V$	20			kΩ
Z_{OUT}	Analog Output Impedance	$-3.2V < V_{OUT} < 3.2V$			20	Ω
V_{IOS}	Offset Voltage Allowed on V_{IN}				±5	mV
V_{OOS}	Analog Output Offset Voltage				±200	mV
V_{IR}	Analog Input Voltage Range				±3.2V	V
V_{OR}	Analog Output Voltage Range	$R_L \geq 10k\Omega$, $C_L \leq 50pF$			±3.2V	V
I_{OUT}	Analog Output Current	$-3.2V < V_{OUT} < 3.2V$	350			μA
V_{IL}	Input Low Voltage (All Digital Inputs Except DCLK in Stand Alone Mode)		−0.5		0.8	V
V_{IH}	Input High Voltage (All Digital Inputs)		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (All Digital Outputs)	$I_{OL} = 2mA$			0.45	V
V_{OH}	Output High Voltage (All Outputs Except $\overline{TSC}$)	$I_{OH} = 400\mu A$	2.4			V
I_{OL}	Output Leakage Current				±10	μA
I_{IL}	Input Leakage Current				±10	μA
I_{CC} (S)	V_{CC} Supply Current (Standby)	$V_{CC} = 5.25V$ $V_{BB} = -4.75V$		5.0		mA
I_{BB} (S)	V_{BB} Supply Current (Standby)			0.06		mA
I_{CC} (A)	V_{CC} Supply Current (Active)			28		mA
I_{BB} (A)	V_{BB} Supply Current (Active)			3.0		mA
PSRR (V_{CC})	V_{CC} Power Supply Rejection Ratio	200mV p-p @ 1.02kHz on the appropriate supply	35			dB
PSRR (V_{BB})	V_{BB} Power Supply Rejection Ratio		30			dB
C_I	Input Capacitance (Digital)			5		pF
C_O	Output Capacitance (Digital)			8		pF

Notes: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages. Min and max specifications are over the temperature and supply voltage ranges shown in the above table entitled "Operating Range."

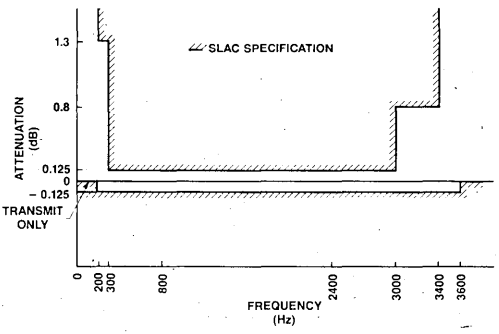
Am7901
TRANSMISSION CHARACTERISTICS

(All measurements are made end-to-end with GX = GR = 0dB and μ-law companded PCM unless otherwise specified.)

Description	Test Conditions	Min	Typ	Max	Units
Attenuation Distortion	800Hz at 0dBmO, or 1000Hz at 0dBmO		See Fig 12		dB
Gain[1] (either path) a) deviation from ideal value b) deviation from initial value	 800Hz at 0dBmO, or 1000Hz at 0dBmO	 −0.2 −0.2		 +0.2 +0.2	 dB dB
Group Delay Distortion (either path)	0dBmO signal		See Fig 13		μs
Group Delay (either path)			150		μs
Harmonic Distortion	(Note 2)			−40	dB
Intermodulation Distortion	a) (Note 3) b) (Note 4)			−35 −49	dB dBmO
Idle Channel Noise (weighted)				−66 19	dBmOp dBrncO
Idle Channel Noise (weighted, receive only)				−77 13	dBmOp dBrncO
Idle Channel Noise (single frequency)				−50	dBmO
Crosstalk a) Go to Return path b) Return to Go path	 300-3400Hz 0dBmO 300-3400Hz 0dBmO			 −70 −70	 dB dB
Gain Tracking			See Fig 14		dB
Signal to Total Distortion			See Fig 15		dB

Notes:
1. The device gains are adjusted during manufacture to guarantee a ±.4dB maximum deviation over lifetime of device.
2. Applied signal is a 0dBmO sine wave within 300 to 3400Hz. The signal measured is any frequency in the range 300 to 3400Hz.
3. Two different frequencies f_1 and f_2 in the range 300-3400Hz and of equal levels in the range −4 to −21dBmO are applied. $2f_1$-f_2 products are measured relative to the level of either f_1 or f_2.
4. Any intermodulation product due to a signal in the range 300-3400Hz with input level −9dBmO and a 50Hz signal with input level − 23dBmO.
5. Noise is measured at the analog output, with the analog input zero and the digital PCM output connected to the digital PCM input.

Figure 12a. Attenuation Distortion (Single Ended)



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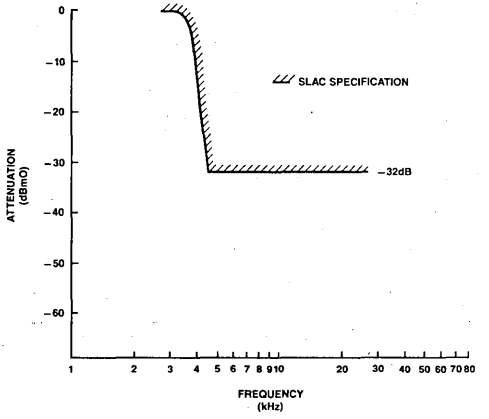
Notes:
1. The reference frequency is 800/1000Hz.
2. Input signal level is 0dBmO.

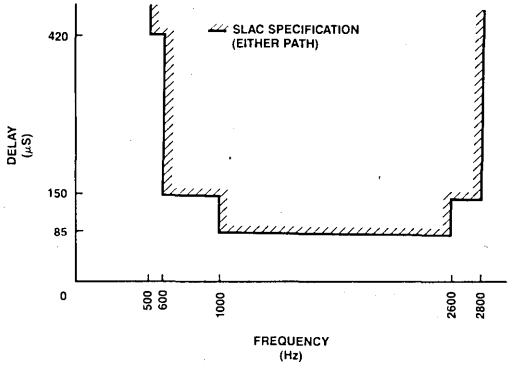
Figure 12b. Out of Band Signals (End to End)



01520B-16

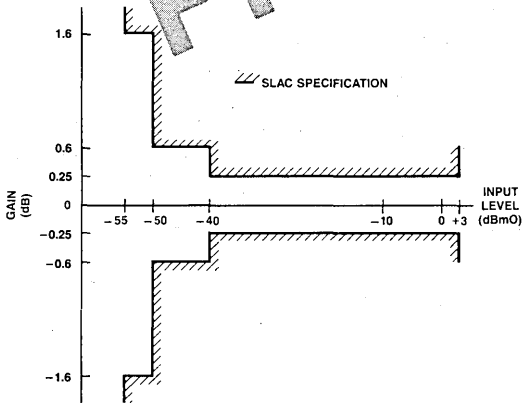
Notes:
1. The reference frequency is 800/1000Hz.
2. Input signal level is 0dBmO.

Figure 13. Group Delay Distortion (Either Path)



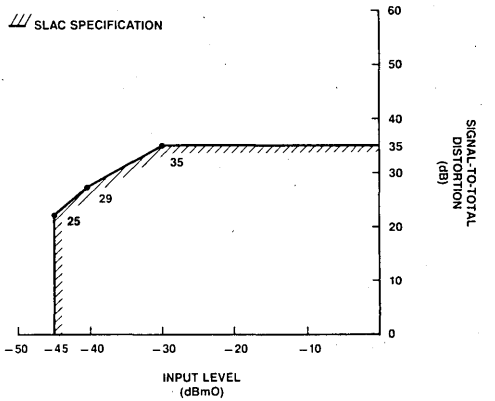
Notes: 1. Input signal is 0dBmO.
2. Minimum value of group delay is taken as reference.

Figure 14. Gain Tracking with Tone (Either Path)



Notes: 1. The input signal is a sine wave in the range of 700 to 1100Hz, (excluding submultiples of 8kHz).
2. The gain variation is relative to the gain at −10dBm0.

Figure 15. Signal-to-Total Distortion with Tone (Either Path)



Note: The input signal is a sine wave in the range of 700 to 1100Hz, (excluding submultiples of 8kHz).

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Am7901
SWITCHING CHARACTERISTICS T_A = 0 to 70°C, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5% (See Note 1)

Parameters	Description	Min	Typ	Max	Units
Serial Interface Input Mode					
t_{DCY}	Data Clock Period	0.488		500	μs
t_{DCH}	Data Clock High Pulse Width (Note 2)	0.220		250	μs
t_{DCL}	Data Clock Low Pulse Width (Note 2)	0.220		250	μs
t_{DCR}	Rise Time of Clock	5		50	ns
t_{DCF}	Fall Time of Clock	5		50	ns
t_{ICSS}	Chip Select Setup Time	150			ns
t_{ICSH}	Chip Select Hold Time	50			ns
t_{ICSL}	Chip Select Pulse Width (Note 3)		$8t_{DCY}$		ns
t_{ICSO}	Chip Select Off Time (Note 4)				ns
t_{IDS}	Input Data Setup Time	50			ns
t_{IDH}	Input Data Hold Time	30			ns
t_{OLH}	Output Latch Hold Time	0.75	1.0	1.6	μs
t_{OLC}	Output Latch Valid	0.80	1.2	1.9	μs
Serial Interface Output Mode					
t_{OCSS}	Chip Select Setup Time	150			ns
t_{OCSH}	Chip Select Hold Time	50			ns
t_{OCSL}	Chip Select Pulse Width (Note 3)		$8t_{DCY}$		ns
t_{OCSO}	Chip Select Off Time (Note 4)				
t_{ODD}	Output Data Turn on Delay			100	ns
t_{ODH}	Output Data Hold Time	30			ns
t_{ODOF}	Output Data Turn Off Delay			100	ns
t_{ODC}	Output Data Valid	30		150	ns
PCM Interface					
t_{PCY}	PCM Clock Period (Note 5)	0.244		15.625	μs
t_{PCH}	PCM Clock High Pulse Width (Note 5)	0.110		15.505	μs
t_{PCL}	PCM Clock Low Pulse Width (Note 5)	0.110		15.505	μs
t_{PCF}	Fall Time of Clock	5		20	ns
t_{PCR}	Rise Time of Clock	5		20	ns
t_{FSS}	Frame Sync Setup Time	50		(t_{PCY} −30)	ns
t_{FSH}	Frame Sync Hold Time	30		(t_{PCY} −50)	ns
t_{TSD}	Delay to $\overline{TSC}$ Valid (Note 6)	(Nt_{PCY} +30)		(Nt_{PCY} +150)	ns
t_{TSO}	Delay to $\overline{TSC}$ Off	30			ns
t_{DXD}	PCM Data Output Delay	50		150	ns
t_{DXH}	PCM Data Output Hold Time	30		100	ns
t_{DXZ}	PCM Data Output Delay to High Z	40		100	ns
t_{DRS}	PCM Data Input Setup Time	50			ns
t_{DRH}	PCM Data Input Hold Time	30			ns

Notes:
1. Min and Max values are valid on all digital outputs except $C_1 - C_5$ with a 150pF load. $C_1 - C_5$ outputs are valid with a 30pF load.
2. The Data Clock may be stopped in the Low state indefinitely without loss of information.
3. Chip select pulse width is nominally 8 t_{DCY} with a minimum value of 7 t_{DCY} + t_{ICSH} + t_{ICSS} and a maximum value of 9 (t_{DCY} − t_{ICSH} − t_{ICSS}).
4. Chip select off time is defined by the type of command being executed.
   Commands attempting access to the coefficient RAMS i.e., Read or Write B, Z, X, R or gain coefficients must have chip select off time of:
   7 t_{MCY} − if device is in power down mode.
   32 t_{MCY} − if device is in power up mode. (Frame sync must also be active.)
   For all other commands, chip select off time is defined as:
   7 t_{MCY} = for both power up or power down modes.
5. The maximum allowed PCM clock frequency is 4.096MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame.The minimum clock frequency is 64kHz.
6. $\overline{TSC}$ is delayed from FS by a typical value of N t_{PCY}, where N is the value stored in the time/clock slot register.

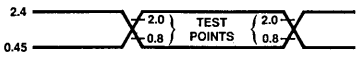
SWITCHING CHARACTERISTICS (Cont.)

Parameters	Description	Min	Typ	Max	Units
Master Clock					
t_{MCY}	Master Clock Period (Note 7)	488.257	488.28	488.305	ns
t_{MCH}	Master Clock High Pulse Width	220	236	258	ns
t_{MCL}	Master Clock Low Pulse Width	220	236	258	ns
t_{MCR}	Rise Time of Clock	5		20	ns
t_{MCF}	Fall Time of Clock	5		20	ns

Note: 7. The Frame Sync pulses (FS_X, FS_R) are 8kHz signals.

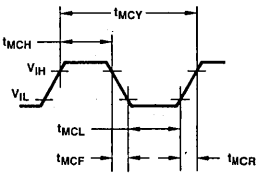
TIMING DIAGRAMS

INPUT AND OUTPUT WAVEFORMS FOR AC TESTS



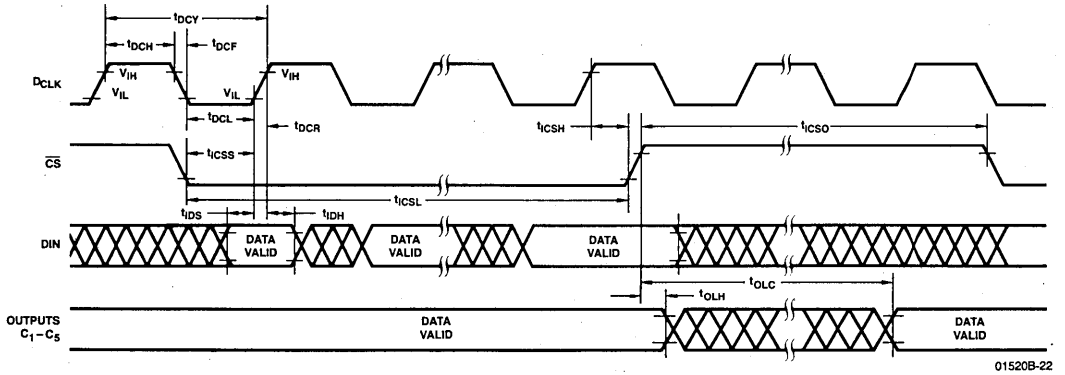
01520B-20

MASTER CLOCK TIMING



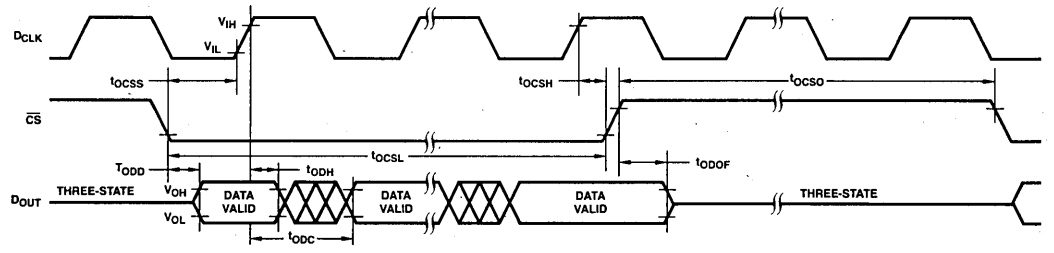
01520B-21

SERIAL I/O INTERFACE (INPUT MODE)



01520B-22

SERIAL I/O INTERFACE (OUTPUT MODE)



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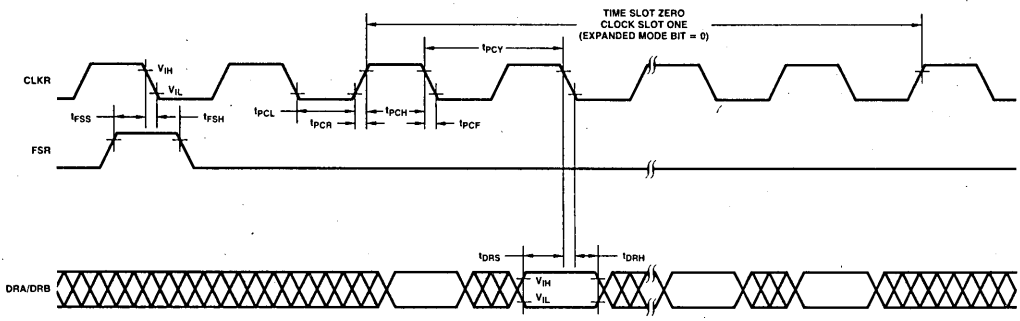
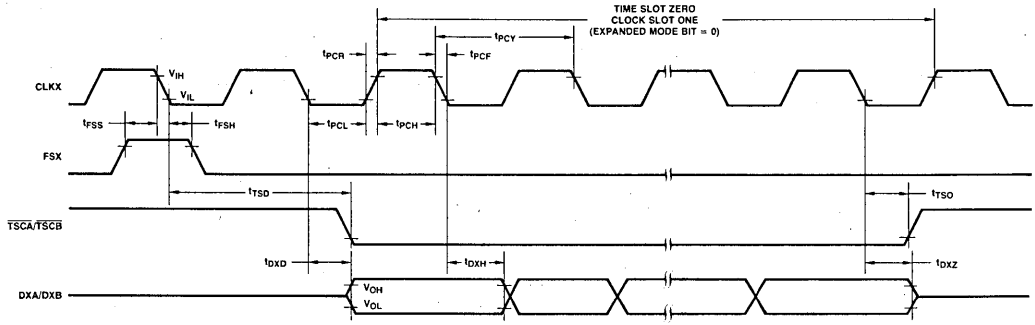
TIMING DIAGRAMS (Cont.)

PCM INPUT TIMING



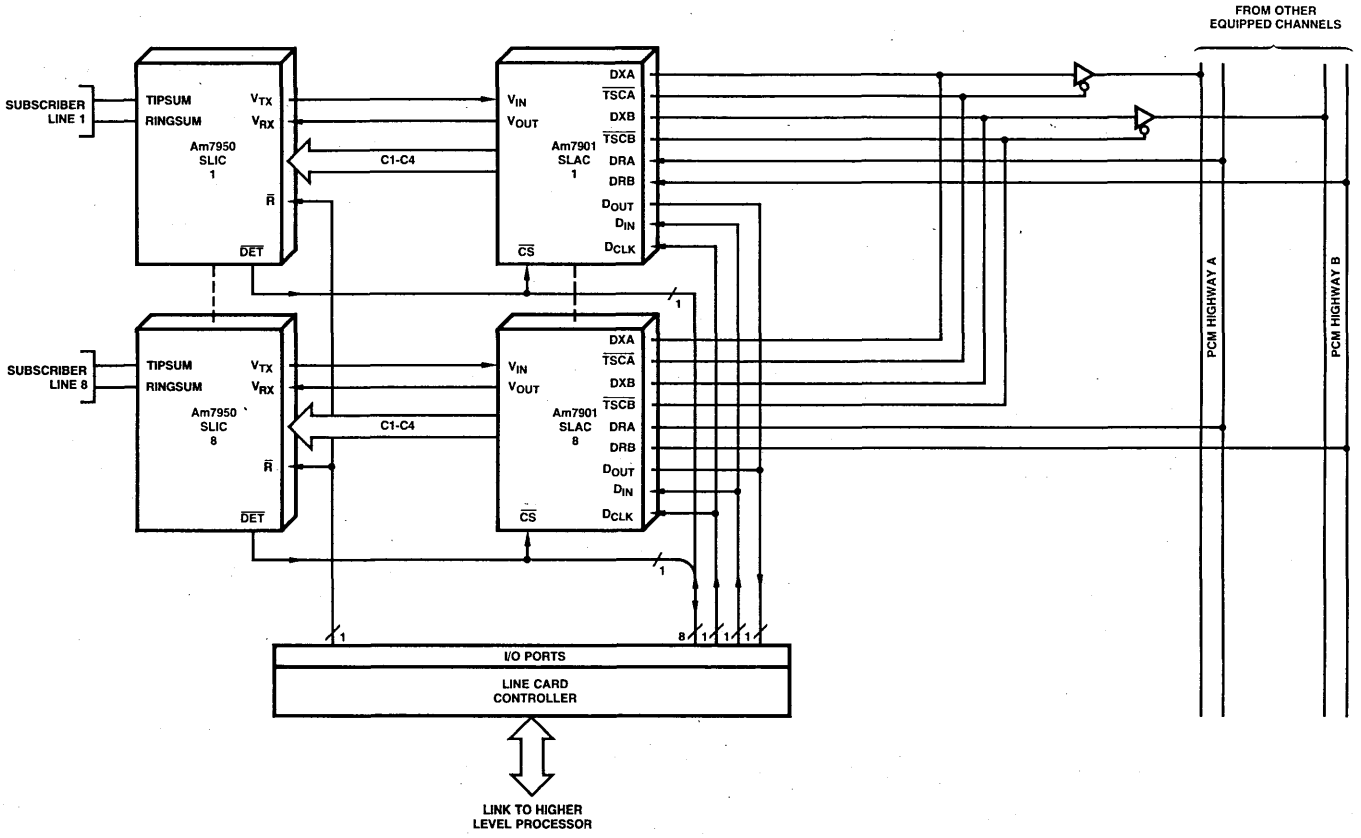
01520B-24

PCM OUTPUT TIMING



01520B-25

AMD
8-CHANNEL SUBSCRIBER LINE CARD



AMD SUBSCRIBER LINE SYSTEM
8-CHANNEL LINE CARD

01520B-26

Am7910

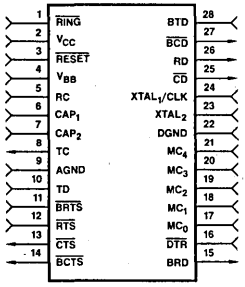
FSK MODEM WORLD-CHIP™

PRELIMINARY DATA (Revised)

DISTINCTIVE CHARACTERISTICS

- Complete FSK MODEM in a 28-pin package – just add line interface
- Compatible with Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications
- No external filtering required
- All digital signal processing, digital filters and ADC/DAC included on-chip
- Includes essential RS-232/CCITT V.24 handshake signals
- Auto-answer capability
- Local copy/test modes
- 1200 bps full duplex on 4-wire line
- Pin-programmable mode section

Figure 1. Connection Diagram



01238C-1

GENERAL DESCRIPTION

The Am7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. It is pin selectable for baud rates of 300, 600 or 1200 bits per second and is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration.

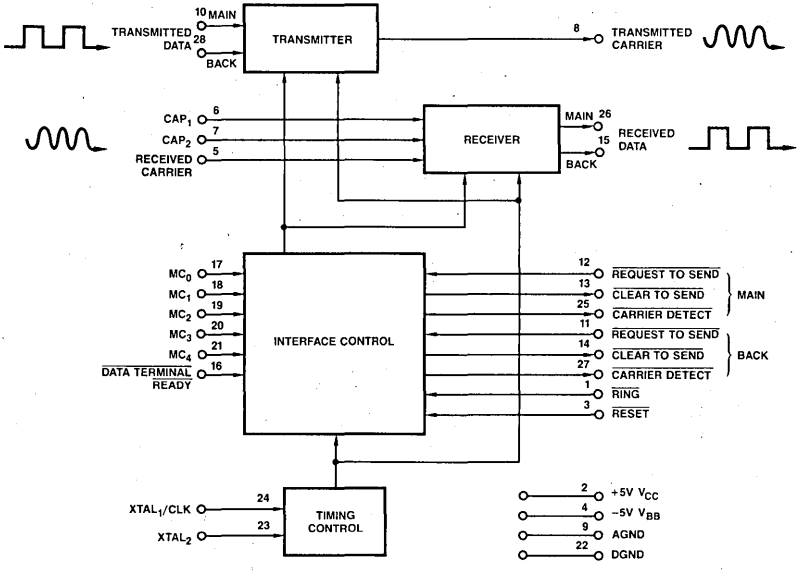
Digital signal processsing techniques are employed in the Am7910 to perform all major functions such as modulation, demodulation and filtering. The Am7910 contains on-chip analog-to-digital and digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A data access arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

The Am7910 is fabricated using N-channel MOS technology in a 28-pin package. All the digital input and output signals (except the external clock signal) are TTL compatible. Power supply requirements are ±5 volts.

Figure 2. Am7910 Block Diagram



01238C-2

INTERFACE SIGNAL DESCRIPTION

MC_0-MC_4 (CONTROL INPUTS)

These five inputs select one of thirty-two modem configurations according to the Bell or CCITT specifications listed in Table 1. Only 19 of these 32 modes are actually available to the user.

Modes 0-8 are the normal operation modes. The 1200 Baud modes can be selected with or without a compromise equalizer.

Modes 16-25 permit loop back of the Am7910 transmitter and receiver. No internal connection is made. The user must externally connect the TRANSMITTED CARRIER pin (Figure 3) to the RECEIVED CARRIER pin if analog loopback is required. For digital loopback, external connection of RECEIVED DATA and TRANSMITTED DATA is required. Whenever a mode in this group is selected, the effect is to set all transmit and receive filters to the same channel frequency band so that loopback can be performed.

Modes 9-15 and 26-31 are reserved and should not be used.

DATA TERMINAL READY ($\overline{DTR}$)

A LOW level on this input indicates the data terminal desires to send and/or receive data via the modem. This signal is gated with all other TTL inputs and outputs so that a low level enables all these signals as well as the internal control logic to function. A HIGH level disables all TTL I/O pins and the internal logic.

REQUEST TO SEND ($\overline{RTS}$)

A LOW level on this input instructs the modem to enter transmit mode. This input must remain LOW for the duration of data transmission. The signal has no effect if $\overline{DATA\ TERMINAL\ READY}$ is HIGH (disabled). A HIGH level on this input turns off the transmitter.

CLEAR TO SEND ($\overline{CTS}$)

$\overline{CLEAR\ TO\ SEND}$ goes LOW at the end of a delay initiated when $\overline{REQUEST\ TO\ SEND}$ goes LOW. Actual data to be transmitted should not be presented to the TRANSMITTED DATA input until a LOW is indicated on the $\overline{CLEAR\ TO\ SEND}$ output. Normally the user should force the TD input HIGH whenever $\overline{CTS}$ is off (HIGH). This signal never goes LOW as long as $\overline{DTR}$ is HIGH (disabled). $\overline{CLEAR\ TO\ SEND}$ goes HIGH at the end of a delay initiated when $\overline{REQUEST\ TO\ SEND}$ goes HIGH.

CARRIER DETECT ($\overline{CD}$)

A LOW on this output indicates that a valid carrier signal is present at the receiver and has been present for at least a time, t_{CDON}, where t_{CDON} depends upon the selected modem configuration (Table 2). A HIGH on this output signifies that no valid carrier is being received and has not been received for a time, t_{CDOFF}. $\overline{CARRIER\ DETECT}$ remains HIGH when $\overline{DTR}$ is HIGH. Values for t_{CDON} and t_{CDOFF} are configuration dependent and are listed in Table 2.

TRANSMITTED DATA (TD)

Data bits to be transmitted are presented on this input serially; HIGH (mark) corresponds to logic 1 and LOW (space) corresponds to logic 0. This data determines which frequency appears at any instant at the TRANSMITTED CARRIER output pin (Table 2). No signal appears at the TRANSMITTED CARRIER output unless $\overline{DTR}$ is LOW and $\overline{RTS}$ is LOW.

RECEIVED DATA (RD)

Data bits demodulated from the RECEIVED CARRIER input are available serially at this output; HIGH (mark) indicates logic 1 and LOW (space) indicates logic 0. Under the following conditions this output is forced to logic 1 because the data may be invalid:

1. When $\overline{CARRIER\ DETECT}$ is HIGH
2. During the internal squelch delay at half-duplex line turn around (202/V.23 modes only)
3. During soft carrier turnoff at half-duplex line turn around (202 mode only)
4. When $\overline{DTR}$ is HIGH
5. When $\overline{RTS}$ ON and $\overline{BRTS}$ OFF in V.23/202 modes only
6. During auto-answer sequence

BACK REQUEST TO SEND ($\overline{BRTS}$)

Since the 1200 bps modem configurations, Bell 202 and CCITT V.23, permit only half duplex operation over two-wire lines, a low baud rate "backward" channel is provided for transmission from the main channel receiver to the main channel transmitter. This input signal ($\overline{BRTS}$) is equivalent to $\overline{REQUEST\ TO\ SEND}$ for the main channel, except it belongs to the backward channel. Note that since the Am7910 contains a single transmitter, $\overline{RTS}$ and $\overline{BRTS}$ should not be asserted simultaneously. $\overline{BRTS}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. In all other modes it is ignored.

For V.23 mode the frequency appearing at the transmitted carrier (TC) output pin is determined by a MARK or SPACE at the back transmitted data (BTD) input (Table 2).

For 202 mode a frequency of 387Hz appears at TC when $\overline{BRTS}$ is LOW and BTD is HIGH. No energy (0.0 volts) appears at TC when $\overline{BRTS}$ is HIGH. BTD should be fixed HIGH for 202 back channel transmission. The signal, $\overline{BRTS}$, then is equivalent to the signal, Secondary Request-to-Send, for 202 S/T modems, or Supervisory Transmitted Data for 202 C/D modems.

BACK CLEAR TO SEND ($\overline{BCTS}$)

This line is equivalent to $\overline{CLEAR\ TO\ SEND}$ for the main channel, except it belongs to the back channel. $\overline{BCTS}$ is meaningful only when a V.23 mode is selected by MC_0-MC_4. This signal is not used in Bell 202 back mode.

BACK CARRIER DETECT ($\overline{BCD}$)

This line is equivalent to $\overline{CARRIER\ DETECT}$ for the main channel, except it belongs to the backward channel. $\overline{BCD}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For V.23 back channel mode, $\overline{BCD}$ turns on when either the MARK or SPACE frequency appears with sufficient level at the received carrier (RC) input.

For 202 back channel mode, $\overline{BCD}$ turns on in response to a 387Hz tone of sufficient level at the RC input. In this case $\overline{BCD}$ is equivalent to the signal, Secondary Received Line Signal Detector, for 202 S/T modems, or Supervisory Received Data for 202 C/D modems.

BACK TRANSMITTED DATA (BTD)

This line is equivalent to TRANSMITTED DATA for the main channel, except it belongs to the back channel. BTD is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For 202 back transmission of on/off keying, BTD should be fixed at a HIGH level.

BACK RECEIVED DATA (BRD)

This line is equivalent to RECEIVED DATA (except clamping) for the main channel, except it belongs to the back channel. BRD is meaningful only when a V.23 mode is selected by MC_0-MC_4. Under the following conditions this output is forced HIGH:

1. $\overline{BRD}$ HIGH
2. $\overline{DTR}$ HIGH
3. V.21/103 mode
4. During auto-answer
5. When $\overline{BRTS}$ ON and $\overline{RTS}$ OFF in V.23 modes only

TRANSMITTED CARRIER (TC)

This analog output is the modulated carrier to be conditioned and sent over the phone line.

RECEIVED CARRIER (RC)

This input is the analog signal received from the phone line. The modem extracts the information contained in this modulated carrier and converts it into a serial data stream for presentation at the RECEIVED DATA (BACK RECEIVED DATA) output.

$\overline{\text{RING}}$

This input signal permits auto-answer capability by responding to a ringing signal from a data access arrangement. If a ringing signal is detected ($\overline{\text{RING}}$ LOW) and $\overline{\text{DTR}}$ is LOW, the modem begins a sequence to generate an answer tone at the TC output.

$XTAL_1$, $XTAL_2$

Master timing of the modem is provided by either a crystal connected to these two inputs or an external clock inserted into $XTAL_1$. The value of the crystal or the external clock frequency must be 2.4576MHz ±.01%.

V_{CC}

+5 volt power supply. (±5%)

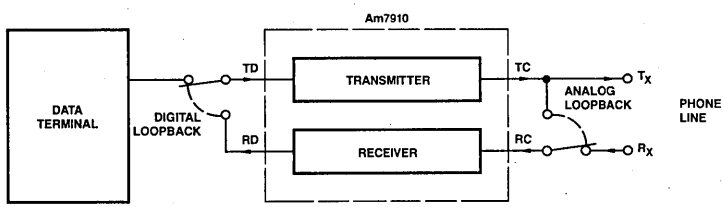
V_{BB}

−5 volt power supply. (±5%)

TABLE 1.

MC_4	MC_3	MC_2	MC_1	MC_0	
0	0	0	0	0	Bell 103 Originate 300bps full duplex
0	0	0	0	1	Bell 103 Answer 300bps full duplex
0	0	0	1	0	Bell 202 1200bps half duplex
0	0	0	1	1	Bell 202 with equalizer 1200bps half duplex
0	0	1	0	0	CCITT V.21 Orig 300bps full duplex
0	0	1	0	1	CCITT V.21 Ans 300bps full duplex
0	0	1	1	0	CCITT V.23 Mode 2 1200bps half duplex
0	0	1	1	1	CCITT V.23 Mode 2 with equalizer 1200bps half duplex
0	1	0	0	0	CCITT V.23 Mode 1 600bps half duplex
0	1	0	0	1	Reserved
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	Bell 103 Orig loopback
1	0	0	0	1	Bell 103 Ans loopback
1	0	0	1	0	Bell 202 Main loopback
1	0	0	1	1	Bell 202 with equalizer loopback
1	0	1	0	0	CCITT V.21 Orig loopback
1	0	1	0	1	CCITT V.21 Ans loopack
1	0	1	1	0	CCITT V.23 Mode 2 main loopback
1	0	1	1	1	CCITT V.23 Mode 2 with equalizer loopback
1	1	0	0	0	CCITT V.23 Mode 1 main loopback
1	1	0	0	1	CCITT V.23 Back loopback
1	1	0	1	0	Reserved
1	1	0	1	1	
1	1	1	0	0	
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

Figure 3. Loopback Configurations



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DGND

Digital signal ground pin.

AGND

Analog signal ground pin (for TRANSMITTED CARRIER and RECEIVED CARRIER).

CAP_1, CAP_2

Connection points of external capacitor/resistor required for proper operation of on-chip analog-to-digital converter.

Recommended values are: C = 2000pF ±10%,
R = 100Ω ±10%.

$\overline{RESET}$

This input signal is for a reset circuit which operates in either of two modes. It automatically resets when power is applied to the device, or it can be activated by application of an external active low TTL pulse.

THEORY OF OPERATION

The Am7910 MODEM consists of three main sections, shown in the block diagram of Figure 2 – Transmitter, Receiver, and Interface Control.

TRANSMITTER (Modulator)

The transmitter, shown in Figure 4, receives binary digital data from a source such as a UART and converts the data to an analog signal using frequency shift keying (FSK) modulation. This analog signal is applied to the phone line through a DAA or acoustic coupler. FSK is a modulation technique which encodes one bit per baud. A logic one applied to the TRANSMITTED DATA (TD) input causes a sine wave at a given frequency to appear at the analog TRANSMITTED CARRIER (TC) output. A logic zero applied to input TD causes a sine wave of a different frequency to appear at the TC ouput. As the data at the TD input switches between logical one and zero, the TC output switches between the two frequencies. In the Am7910 this switching between frequencies is phase continuous. The frequencies themselves are digitally synthesized sine functions.

The frequencies for each modem configuration available in the Am7910 are listed in Table 3a.

The process of switching between two frequencies as in FSK generates energy at many more frequencies than the two used in the modulation. All the transmitted information can be recovered from a frequency band B Hz wide, where B is the bit rate or maximum rate of change of the digital data at the TD input. This band is centered about a frequency, f_C,

where $f_C = f_1 + (f_2 - f_1)/2$

(f_1 = lower of two FSK frequencies)

(f_2 = higher of two FSK frequencies)

In addition to this primary information band, there exist side bands containing redundant information. It is desirable to attenuate these bands for two reasons:

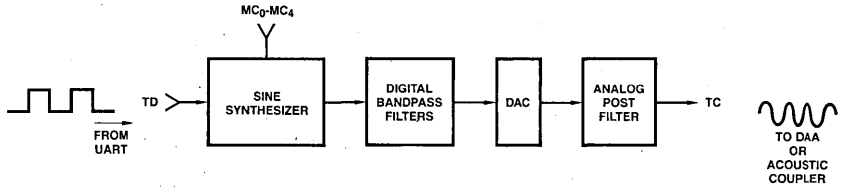
1. The phone companies have specifications on the amount of energy allowed in certain frequency bands on the line.
2. If two independent information channels are present simultaneously on the line (e.g. 300 bps full duplex or 1200 bps half duplex with back), the redundant transmitter components may fall in the frequency band of the local receiver channel and interfere with detection. In the Am7910 these redundant and undesirable components are attenuated by digital bandpass filters.

Following the digital bandpass filters, the filtered FSK signal is converted to an analog signal by an on-chip DAC operating at a high sample rate. This analog FSK signal is finally smoothed by a simple on-chip analog low pass filter.

RECEIVER (Demodulator)

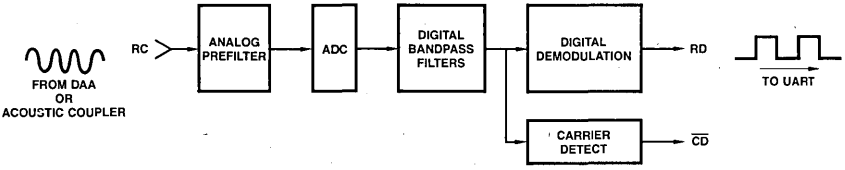
A simplified block diagram of the Am7910 FSK receiver is shown in Figure 5. Data transmitted from a remote site modem over the phone line is an FSK-modulated analog carrier. This carrier is applied to the RECEIVED CARRIER (RC) pin via a DAA or acoustic coupler. The first stage of the demodulator is a simple on-chip analog low pass anti-alias filter. The output of this is converted into digital form and filtered by digital bandpass filters to improve the signal to noise ratio and reject other independent channel frequencies associated with the phone line in the case of full duplex configuration. The bandpass filtered output is digitally demodulated to recover the binary data. A carrier detect signal is also digitally extracted from the received line carrier to indicate valid data.

Figure 4. Transmitter Block Diagram



01238C-4

Figure 5. Receiver Block Diagram



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9

INTERFACE CONTROL

This section controls the handshaking between the modem and the local terminal. It consists primarily of delay generation counters, two state machines for controlling transmission and reception, and mode control decode logic for selecting proper transmit frequencies and transmit and receive filters according to the selected modem type. Inputs and outputs from this section are as follows:

REQUEST TO SEND (Main and Back)
CLEAR TO SEND (Main and Back)
CARRIER DETECT (Main and Back)
RING
MCO-MC4
DATA TERMINAL READY

Internal logic clamps protocol signals to different levels under certain conditions (e.g., initial conditions).

When Bell 103/113 and V.21 modem configurations are selected, the back channel signals are non-functional.

Figures 8 and 9 depict the sequencing of the two state machines. State machine 1 implements main or back channel transmission and the auto-answer sequence. State machine 2 implements reception on main or back channel.

The state machine powers on to the state labelled INITIAL CONDITIONS. Handshake signals are set to or assumed to be the levels listed in Table 2. The machine then waits for DATA TERMINAL READY (DTR) to be turned on. Whenever DTR is turned to the OFF state from an ON condition, each state machine and external signals return to the initial conditions within 25 microseconds. After DTR is turned ON the Am7910 becomes operational as a modem and the state machines proceed as depicted in the flowcharts.

The definitions of the terms Full Duplex and Half Duplex used in these flowcharts are depicted below (Figs. 6 and 7). "Full Duplex" applies to all 103/113, V.21 modes. "Half Duplex" applies to 202 and V.23, both forward and backward channel.

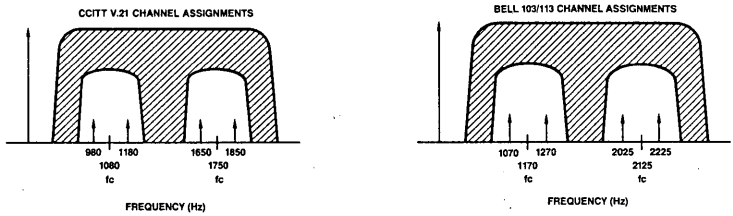
Full Duplex: Data can be transmitted and received simultaneously at a rate of 300 baud. Two independent 300Hz channels are frequency multiplexed into the 3000Hz bandwidth of the phone line. The Am7910 configurations for the Bell 103/113 and CCITT V.21 can be operated full duplex.

Half Duplex: In half duplex with back channel, the modem may transmit at 1200/600 baud and receive at 5/75 baud. Alternatively it may transmit at 5/75 baud and receive at 1200/600 baud. Examples are Bell 202 and CCITT V.23.

TABLE 2.
INITIAL CONDITIONS

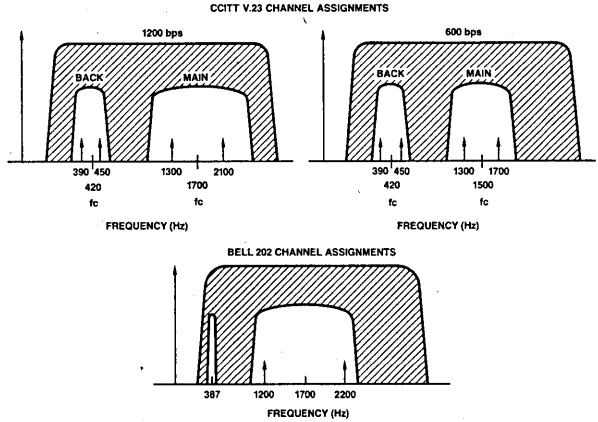
Data Terminal Ready (DTR)	OFF
Request to Send (RTS)	OFF
Clear to Send (CTS)	OFF
Transmitted Data (TD)	Ignored
Back Channel Request to Send (BRTS)	OFF
Back Channel Clear to Send (BCTS)	OFF
Back Channel Transmitted Data (BTD)	Ignored
Ring (RING)	OFF
Carrier Detect (CD)	OFF
Received Data (RD)	MARK
Back Channel Carrier Detect (BCD)	OFF
Back Channel Received Data (BRD)	MARK

Figure 6. Full Duplex



01238C-6

Figure 7. Half Duplex



01238C-7

TABLE 3(a). FREQUENCY PARAMETERS

Modem	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		Answer Tone Freq Hz
			Space Hz	Mark Hz	Space Hz	Mark Hz	
Bell 103 Orig	300	Full	1070	1270	2025	2225	–
Bell 103 Ans	300	Full	2025	2225	1070	1270	2225
CCITT V.21 Orig	300	Full	1180	980	1850	1650	–
CCITT V.21 Ans	300	Full	1850	1650	1180	980	2100
CCITT V.23 Mode 1	600	Half	1700	1300	1700	1300	2100
CCITT V.23 Mode 2	1200	Half	2100	1300	2100	1300	2100
CCITT V.23 Mode 2 Equalized	1200	Half	2100	1300	2100	1300	2100
Bell 202	1200	Half	2200	1200	2200	1200	2025
Bell 202 Equalized	1200	Half	2200	1200	2200	1200	2025
CCITT V.23 Back	75	–	450	390	450	390	–
Bell 202 Back	5	–	*	*	**	**	–

*($\overline{\text{BRTS}}$ LOW) and (BTD HIGH): 387Hz at TC
*($\overline{\text{BRTS}}$ HIGH) or (BTD LOW): 0 volts at TC
**387Hz at RC: $\overline{\text{BCD}}$ LOW
**No 387Hz at RC: $\overline{\text{BCD}}$ HIGH
*Meets new CCITT R20 frequency tolerance.

Frequency tolerance is less than ±0.4Hz with 2.4576MHz Crystal. Except Bell 202 which is +1Hz (1200 Hz, mark)

TABLE 3(b). TIMING PARAMETERS (Refer to Figures 10, 11 and 12 for Timing Diagrams)

Symbol	Description	Bell 103 Orig	Bell 103 Ans	CCITT V.21 Orig	CCITT V.21 Ans	CCITT V.23 Mode 1	CCITT V.23 Mode 2	CCITT V.23 Mode 2 EQ	Bell 202	Bell 202 EQ	CCITT V.23 Back	Bell 202 Back	Units
$t_{RC(On)}$	Request-to-Send to Clear-to-Send ON Delay	208.3	208.3	400	400	208.3	208.3	208.3	183.3	183.3	–	–	msec ±0.3%
$t_{RC(Off)}$	Request-to-Send to Clear-to-Send OFF Delay	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	–	–	msec ±0.25%
$t_{BRC(On)}$	Back Channel Request-to-Send to Clear-to-Send ON Delay	–	–	–	–	–	–	–	–	–	82.3	–	msec ±0.64%
$t_{BRC(Off)}$	Back Channel Request-to-Send to Clear-to-Send OFF Delay	–	–	–	–	–	–	–	–	–	0.5	–	msec ±25%
$t_{CD(On)}$	Carrier Detect ON Delay	94-106	94-106	301-312	301-312	11.4-15.4	11.4-15.4	11.4-15.4	18-22	18-22	–	–	msec
$t_{CD(Off)}$	Carrier Detect OFF Delay	21-40	21-40	21-40	21-40	5.4-13.3	5.4-13.3	5.4-13.3	12.4-23.4	12.4-23.4			msec
$t_{BCD(On)}$	Back Channel Carrier Detect ON Delay	–	–	–	–	–	–	–	–	–	17-25	17-25	msec
$t_{BCD(Off)}$	Back Channel Carrier Detect OFF Delay	–	–	–	–	–	–	–	–	–	21-38	21-38	msec
t_{AT}	Answer Tone Duration	–	1.9	–	3.0	3.0	3.0	3.0	1.9	1.9	–	–	sec ±0.44%
t_{SIL}	Silence Interval before Transmission	1.3	1.3	1.9	1.9	1.9	1.9	1.9	1.3	1.3	–	–	sec ±0.64%
t_{SQ}	Receiver Squelch Duration	–	–	–	–	156.3	156.3	156.3	156.3	156.3	–	–	msec ±3.3%
t_{STO}	Transmitter Soft Turn-Off Duration	–	–	–	–	–	–	–	24	24	–	–	msec ±2.3%
t_{RI}	Minimum $\overline{\text{RI}}$ Low Duration	–	25	–	25	25	25	25	25	25	–	–	μs

9

CALL ESTABLISHMENT

Before two modems can exchange data, an electrical connection through the phone system must be established. Although it may assist in call establishment, a modem typically does not play a major role. A call may be originated manually or automatically and it may be answered manually or automatically.

Manual Calling – Manual calling is performed by a person who dials the number, waits for an answer , then places the calling modem into data transmission mode.

Automatic Calling – Automatic calling is typically performed by an automatic calling unit (ACU) which generates the appropriate dialing pulse or dual-tone sequence required to call the remote (called) modem. The ACU also has the ability to detect an answer tone from the called modem and place the calling modem into data transmission mode.

Manual Answering – Manual answering is performed by a person who hears the phone ring, lifts the receiver, causes the called modem to send an answer tone to the calling modem, and places the called modem into data transmission mode.

Automatic Answering – Automatic answering is performed by a called modem with a data access arrangement (DAA). The DAA detects a ringing signal, takes the phone circuit off-hook (corresponding to lifting the receiver) and instructs the called modem to commence the auto-answer sequence. Next the called modem sends out silence on the line, followed by an answer tone. When this tone is detected by the calling modem, the connection is considered to have been established.

The Am7910 provides assistance for automatic answering through the $\overline{\text{RING}}$ signal as follows. Observe the upper right-hand portion of Figure 8(a). Assume that $\overline{\text{DATA TERMINAL READY}}$ ($\overline{\text{DTR}}$) has recently been asserted to cause exit from the initial conditions. Note that if $\overline{\text{DTR}}$ remains OFF, $\overline{\text{RING}}$ is ignored. Assume also that $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ are OFF and that the mode control lines (MC0-MC4) select a normal modem configuration, not a loopback mode. Automatic answering is initiated by receipt of a LOW level at the $\overline{\text{RING}}$ input, causing entrance to the auto-answer sequence depicted in Figure 8(c).

The Am7910 outputs silence (0.0 volts) at its TRANSMITTED CARRIER (TC) output for a time, t_{SIL}, followed by the answer tone for a time, t_{AT}. The $\overline{\text{CARRIER DETECT}}$ ($\overline{\text{CD}}$) pin is clamped OFF and the RECEIVED DATA (RD) signal is therefore clamped to a MARK (HIGH) during the auto-answer sequence. Upon completion of the answer tone, $\overline{\text{CD}}$ is released. If the mode lines (MC0-MC4) select a 202 or V.23 mode, the transmit filters are set to the forward channel and the receive filters are set to the back channel during the auto answer sequence.

At the end of the auto-answer sequence, return is made to point A in the loop at the upper right-hand portion of Figure 8(a). Note that since the answer flag has been set, the auto-answer sequence cannot be entered again unless $\overline{\text{DTR}}$ is first turned OFF, then ON. At this point the phone line connection has been established and data transmission or reception may begin.

The $\overline{\text{RING}}$ input may be activated from a conditioned DAA Ring Indicator output for automatic answering or it may be activated by a switch for manual answering. Tying $\overline{\text{RING}}$ HIGH will disable the auto-answer function of the Am7910.

DATA TRANSMISSION

Full Duplex

Following call establishment, full duplex data transmission can be started by either the called or calling modem. In other words, if the connection has been established and the modem is looping through point A in Figure 8(a), it no longer matters which is the called and which is the calling modem. Data transmission is initiated by asserting $\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$). At this time the TRANSMITTED DATA (TD) input will be released and a modulated carrier can appear at the TRANSMITTED CARRIER (TC) output. Following a delay, t_{RCON}, $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) will turn ON. At this time, data may be transmitted through the TD input. It is a common protocol for the user to always present a MARK at the TD input before $\overline{\text{RTS}}$ is asserted and during the t_{RCON} delay.

Data transmission continues until $\overline{\text{RTS}}$ is turned OFF. Following a short delay, t_{RCOFF}, $\overline{\text{CTS}}$ turns OFF. As soon as $\overline{\text{RTS}}$ goes OFF, the TD input is ignored and the TC output is set to 0.0 volts (silence). After $\overline{\text{CTS}}$ turns OFF, the state machine returns to point A in Figure 8(a).

Half Duplex

When a half duplex mode is selected (202 or V.23), data transmission can be either on the main channel at 1200/600 baud or on the back channel at 5/75 baud. In normal half duplex operation a single modem is either transmitting on the main and receiving on the back channel or vice versa. In the Am7910 control of the transmitter and receiver filters to the proper channel is performed by $\overline{\text{RTS}}$. When $\overline{\text{RTS}}$ is asserted, the transmitter filters and synthesizer are set to transmit on the main channel; the receiver filters are set to receive on the back channel. Therefore, whenever $\overline{\text{RTS}}$ is on, $\overline{\text{BRTS}}$ should not be asserted since the transmitter cannot be used for the back channel. When $\overline{\text{RTS}}$ is OFF and a half duplex mode is selected, the transmitter filters and synthesizer are set to the back channel; the receiver filters are set to the main channel. If $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ are asserted simultaneously, $\overline{\text{RTS}}$ will take precedence. However, if $\overline{\text{BRTS}}$ is asserted before $\overline{\text{RTS}}$ and the back channel data transmission sequence has been entered (Figure 8(b)), $\overline{\text{RTS}}$ will be ignored until $\overline{\text{BRTS}}$ is turned OFF.

The state machine sequences for main and back channel transmission differ slightly and are depicted in Figure 8. Assume the state machine is idling through point A in Figure 8(a).

Main Channel

This transmission sequence is entered if a 202 or V.23 mode is selected and $\overline{\text{RTS}}$ is asserted. Since the receiver is now forced to the back channel, the RECEIVED DATA (RD) signal is clamped to a MARK; and the $\overline{\text{CARRIER DETECT}}$ signal is clamped OFF. The TRANSMITTED DATA input (TD) is released and a carrier appears at the TRANSMITTED CARRIER output which follows the MARK/SPACE applied to TD. $\overline{\text{RTS}}$ turning ON initiates a delay, t_{RCON}, at the end of which the $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) output goes LOW. When $\overline{\text{CTS}}$ goes LOW data may be transmitted through input TD. Data transmission continues until $\overline{\text{RTS}}$ is turned OFF. At this time several events are initiated. First a delay, t_{RCOFF}, is initiated at the end of which $\overline{\text{CTS}}$ turns OFF. The TD input is ignored as soon as $\overline{\text{RTS}}$ goes OFF. If a 202 mode is selected, a soft turn-off tone appears at the TC output for a time, t_{STO}, followed by silence (0.0 volts). For both 202 and V.23 modes a squelch period, t_{SQ}, is initiated when $\overline{\text{RTS}}$ goes OFF. During this period the $\overline{\text{CD}}$ output is clamped OFF, forcing the RD output to a MARK condition. The squelch period begins as soon as $\overline{\text{RTS}}$ goes OFF and thus overlaps both t_{RCOFF} and t_{STO}. At the end of the squelch period, the state machine returns to the idle loop at point A in Figure 8(a).

The reasons for squelch and soft-turnoff are as follows:

Soft Turn-Off: When $\overline{\text{RTS}}$ is turned OFF at the end of a message, transients occur which may cause spurious space signals to be received at a remote modem. During soft turn-off the modem transmits a soft carrier frequency for a period, t_{STO}, after $\overline{\text{RTS}}$ is

turned OFF. This results in a steady MARK on the RECEIVED DATA (RD) line of the remote modem.

Squelch: The local receiver must be turned OFF after $\overline{RTS}$ is OFF, until the start of carrier detect, so that line transients are not demodulated. The process of disabling the receiver after $\overline{RTS}$ is turned OFF is called squelching.

Back Channel

This transmission sequence, shown in Figure 8(b), is entered if a 202 or V.23 mode is selected, $\overline{RTS}$ is OFF, and $\overline{BRTS}$ is asserted. The $\overline{BACK\ CARRIER\ DETECT}$ ($\overline{BCD}$) output is forced OFF and the BACK RECEIVED DATA (BRD) output is clamped to a MARK. The BACK TRANSMITTED DATA input (BTD) is released and a carrier appears at the TC output which follows the MARK/SPACE applied to BTD. Turning ON $\overline{BRTS}$ initiates a delay, t_{BRCON}, at the end of which the $\overline{BACK\ CLEAR\ TO\ SEND}$ ($\overline{BCTS}$) output goes LOW. When $\overline{BCTS}$ goes LOW data may be transmitted through input BTD. Data transmission continues until $\overline{BRTS}$ is turned OFF. The input BTD is immediately ignored and the TC output is silenced (set to 0.0 volts). Following a short delay, t_{BRCOFF}, the output $\overline{BCTS}$ goes OFF. The signals $\overline{BCD}$ and BRD are released and the state machine returns to idle at point A of Figure 8(a).

In 202 back channel mode, BTD should be tied HIGH. Then $\overline{BRTS}$ controls the ON/OFF keying modulation. When $\overline{BRTS}$ is LOW, 387Hz appears at the TC output; when $\overline{BRTS}$ is HIGH, 0 volts appears at TC.

DATA RECEPTION

Data reception is controlled by state machine 2 and depicted in Figure 9. At power on the machine enters initial conditions and remains there until $\overline{DTR}$ is asserted. It then loops until either $\overline{CARRIER\ DETECT}$($\overline{CD}$) or $\overline{BACK\ CARRIER\ DETECT}$ ($\overline{BCD}$) occurs.

Full Duplex

In full duplex data reception, $\overline{CARRIER\ DETECT}$ may appear at any time after the phone connection has been established. Reception is independent of transmission. When the receiver detects a valid carrier for at least a time, t_{CDON}, the output $\overline{CD}$ is turned ON, the RECEIVED DATA (RD) output is released, and valid data can be obtained at RD. Data is received until the receiver detects loss of carrier for at least a time, t_{CDOFF}. At this time the $\overline{CD}$ output is turned OFF and RD is clamped to a MARK. The state machine returns to the idle loop at point E.

Half Duplex

As discussed in the data transmission section above, when a half duplex mode has been selected, the signal $\overline{RTS}$ controls whether the main channel is transmitting or receiving. The back channel can only do the opposite from the main. If $\overline{RTS}$ is OFF, then $\overline{CARRIER\ DETECT}$ may be asserted and the data reception sequence is identical to that discussed above for full duplex reception. As long as $\overline{RTS}$ remains OFF, $\overline{BACK\ CARRIER\ DETECT}$ will never be asserted. If $\overline{RTS}$ is ON, then $\overline{CARRIER\ DETECT}$ will never be asserted. Instead the receiver will look for a valid carrier in the back channel frequency band. If a valid carrier exists for at least a time, t_{BCDON}, the output $\overline{BACK\ CARRIER\ DETECT}$ ($\overline{BCD}$) is turned ON, the BACK RECEIVED DATA (BRD) output is released and valid data can be obtained at BRD. Data is received until the receiver detects loss of back channel received signal for at least time, t_{BCDOFF}. At this time the $\overline{BCD}$ output is turned OFF. Data output, BRD, is clamped to a MARK if a V.23 mode is selected. For 202 back channel mode, $\overline{BCD}$ represents the received data. The BRD output can be ignored. The state machine returns to the idle loop at point E.

LOOPBACK

Ten modes exist to allow both analog and digital loopback for each modem specification met by the Am7910. When a loopback mode is selected, the signal processing (filters, etc.) for both the transmitter and receiver is set to process the same channel or frequency band. This allows the analog output, TRANSMITTED CARRIER, and the analog input, RECEIVED CARRIER, to be connected for local analog loopback. Alternatively the digital data signals, TD and RD or BTD and BRD, can be connected externally, allowing a remote modem to test the local modem with its digital data signals looped back.

When a loopback mode is selected, the state machine sequences are altered slightly. First, auto-answer is disabled. Second, if a half duplex loopback mode is selected (202 or V.23), the local $\overline{CARRIER\ DETECT}$/$\overline{BCD}$ is not forced OFF when $\overline{RTS}$/$\overline{BRTS}$ is asserted.

The 202 and V.23 main loopback modes allow use in a 4-wire configuration at 1200 bps.

Figure 8(a). Transmit Main Channel State Diagram

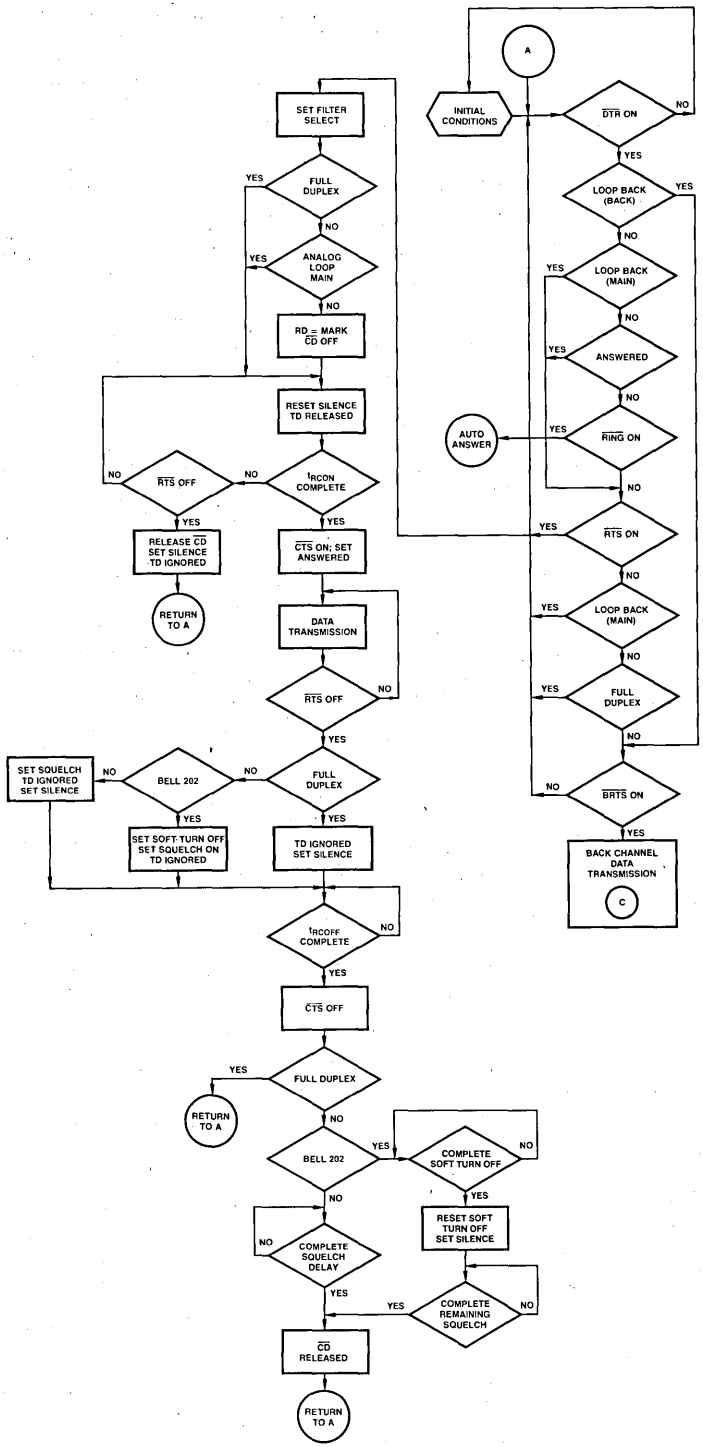


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Figure 8(b). Transmit Back Channel State Diagram

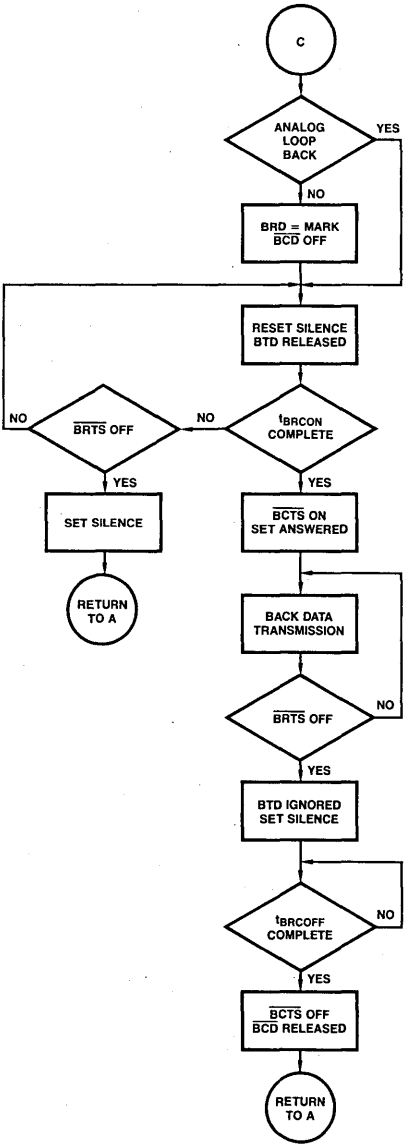

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Figure 8(c). Auto Answer State Diagram

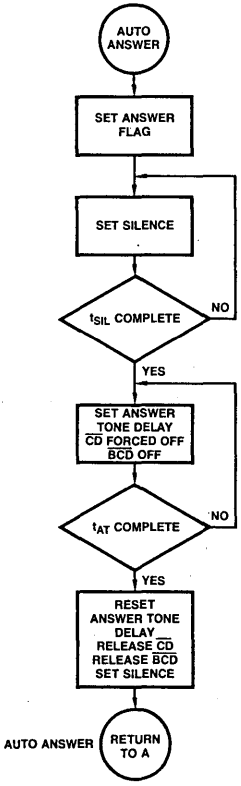

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Figure 9. Receiver Main/Back Channel State Diagram

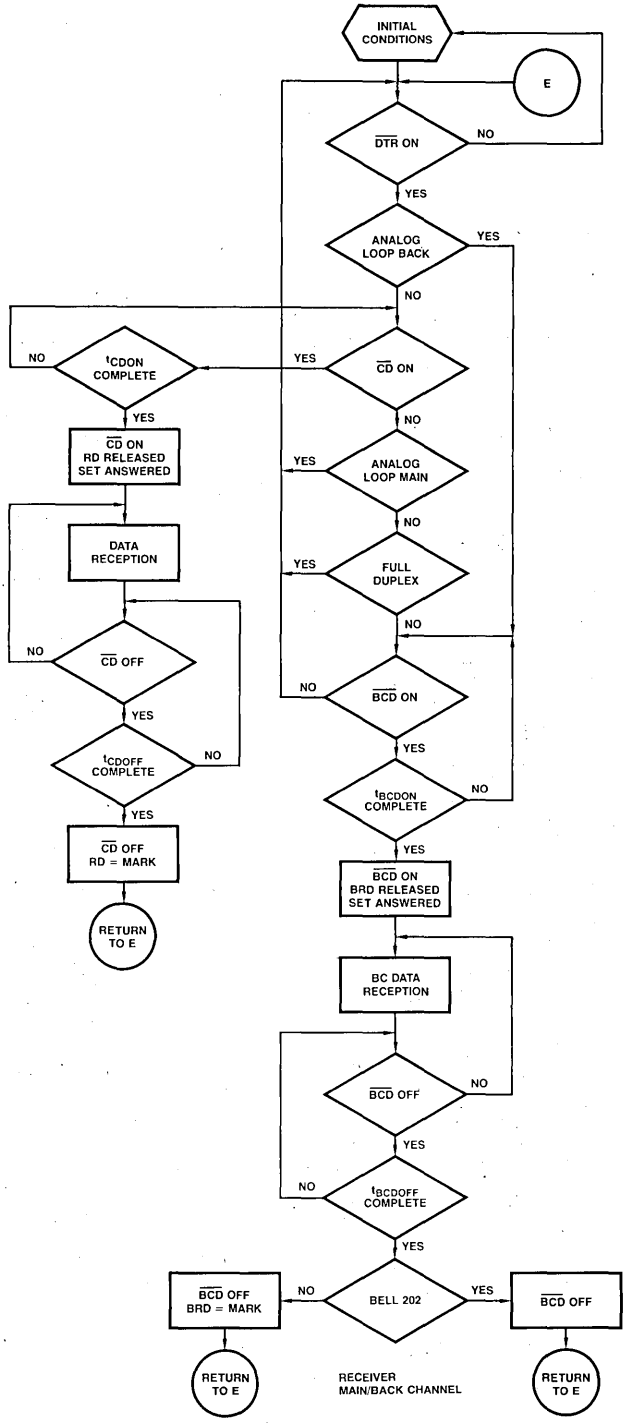

Figure 10. BELL 202 Handshake Timing

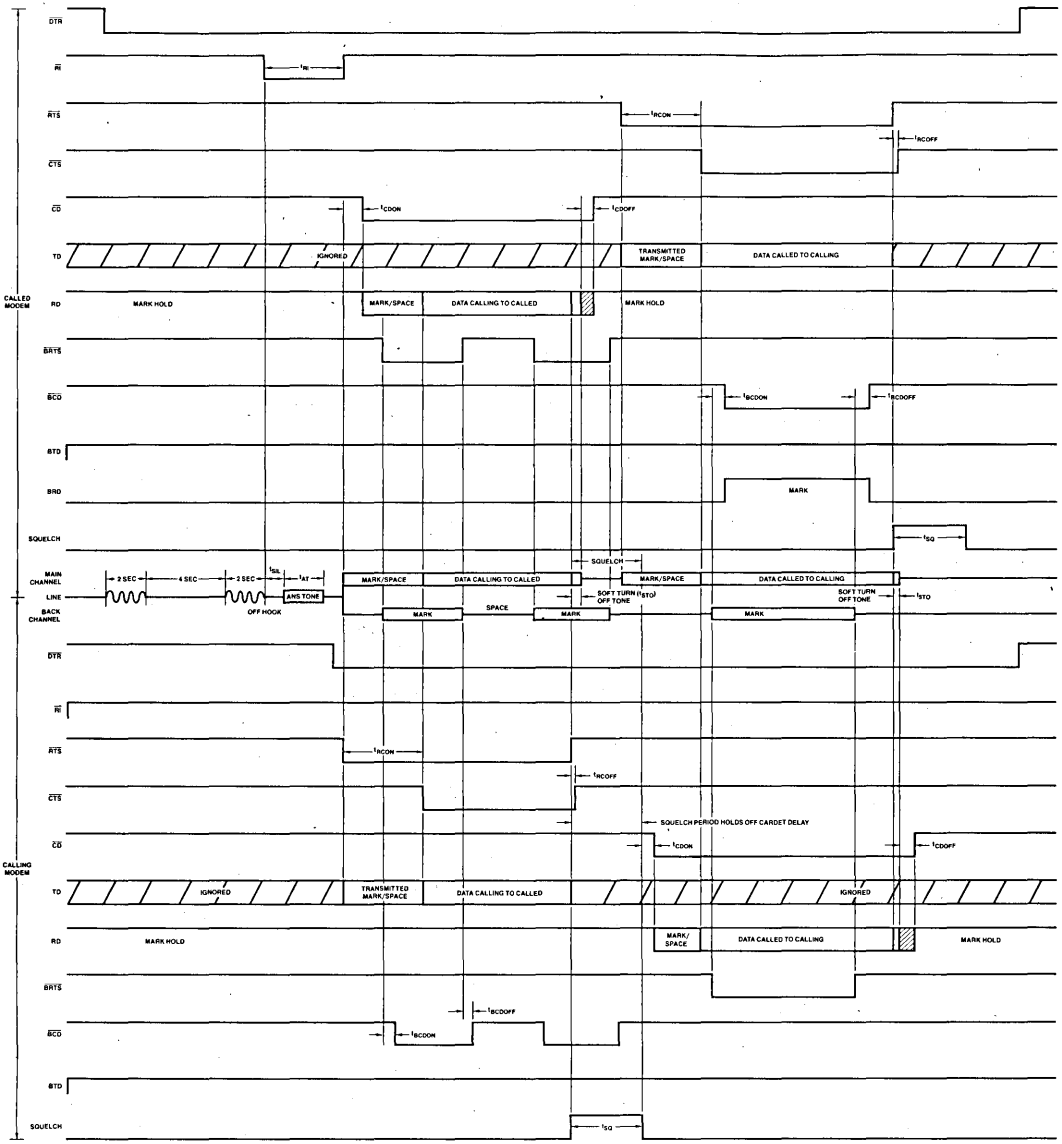

Figure 11. CCITT V.23 Handshake Timing

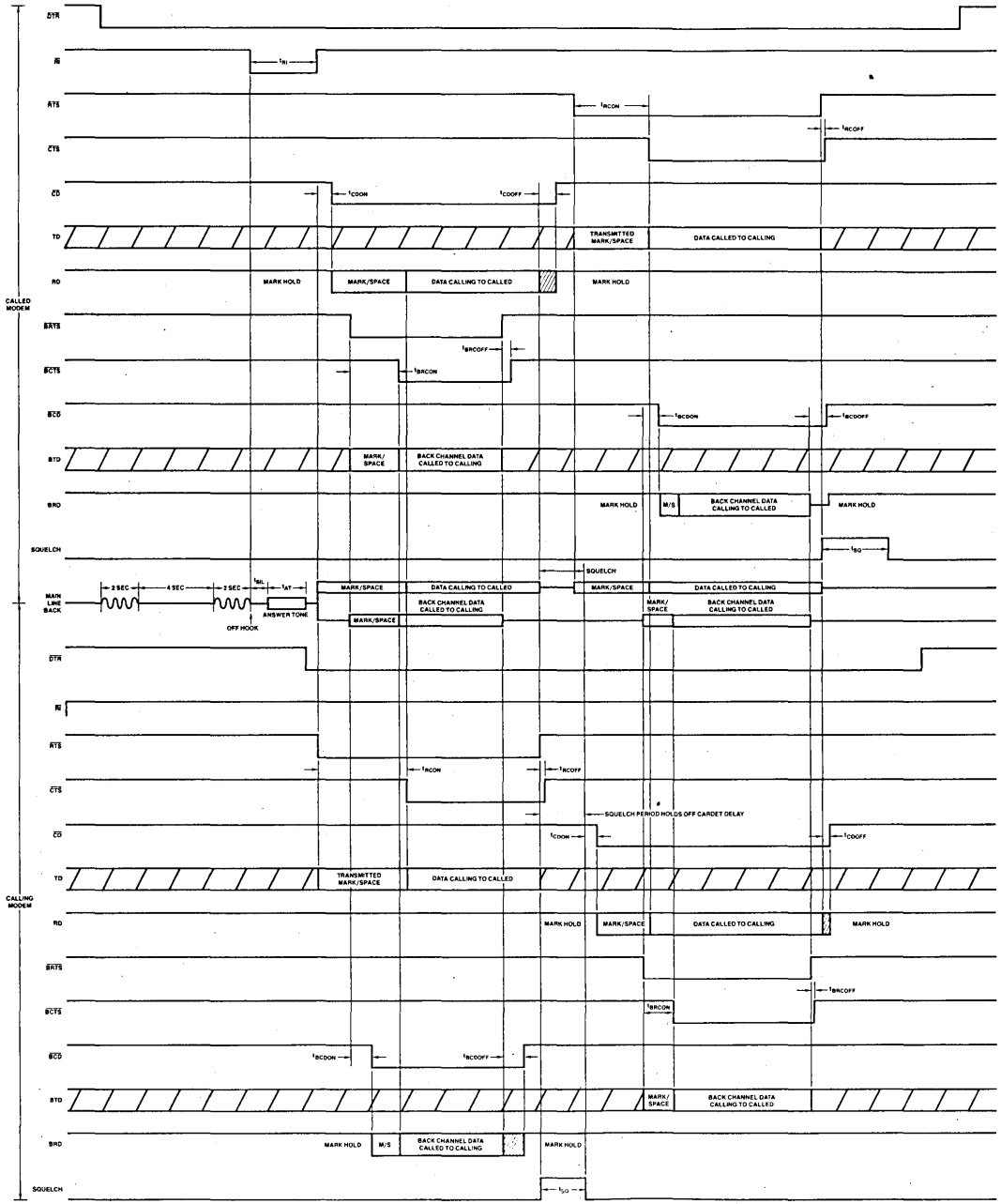

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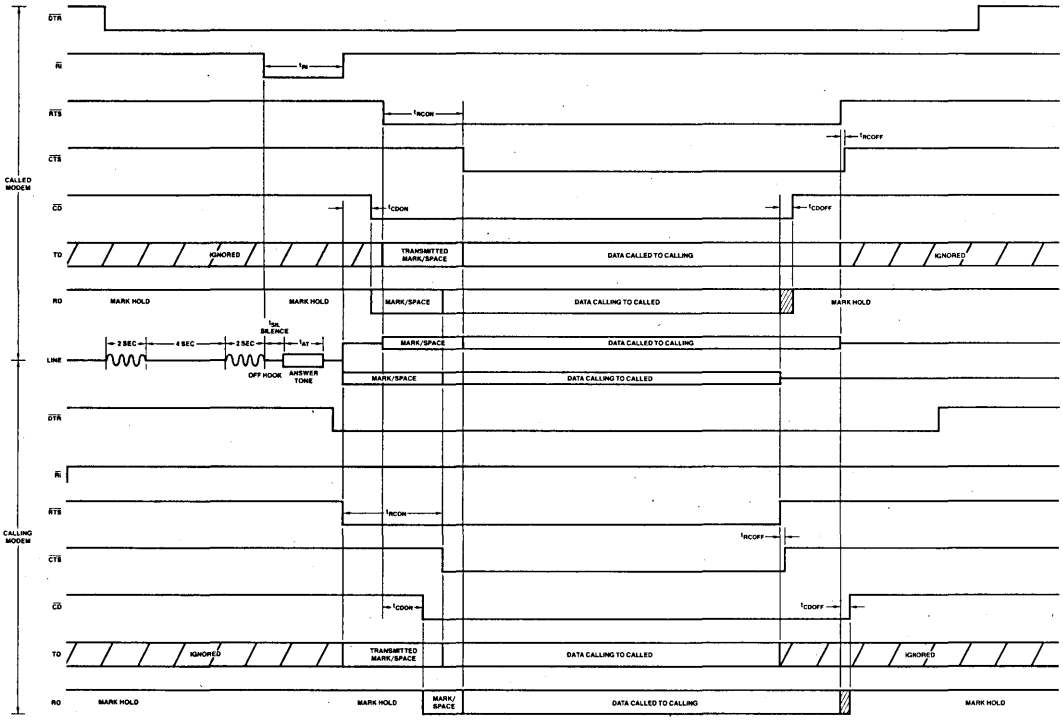
Figure 12. BELL 103/CCITT V.21 Handshake Timing



CLOCK GENERATION

Master timing of the modem is provided by either a crystal connected to the $XTAL_1$ and $XTAL_2$ inputs or an external clock applied to the $XTAL_1$ input.

Crystal

When a crystal is used it should be connected as shown in Figure 13. The crystal should be a parallel resonance type, and its value must be 2.4576MHz ±.01%. A list of crystal suppliers is shown below.

External Clock

This clock signal could be derived from one of several crystal-driven baud rate generators. It should be connected to the $XTAL_1$ input and the $XTAL_2$ input must be left floating. The timing parameters required of this clock are shown in Figure 13 and the values are listed in Table 4.

Figure 13. Clock Generation

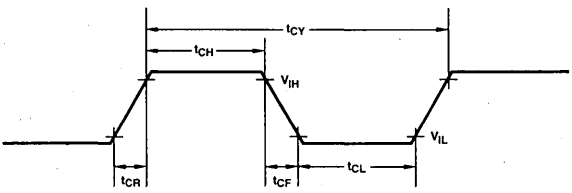
Crystal Information (f_C = 2.4576MHz)

Manufacturer	P/N	C_1	C_2
M-Tron	MP-2	20pF	20pF
Monitor Products	MM-33	20pF	20pF

Note: Rise time of V_{CC} must be greater than 5msec to insure proper crystal oscillator start-up.

*Capacitors values vary with different crystal manufacturers.

(a)



(b)

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TABLE 4.
CLOCK PARAMETERS

Symbol	Parameters	Min	Typ	Max	Units
t_{CY}	Clock Period	406.86	406.9	406.94	ns
t_{CH}	Clock High Time	165			ns
t_{CL}	Clock Low Time	165			ns
t_{CR}	Clock Rise Time			20	ns
t_{CF}	Clock Fall Time			20	ns

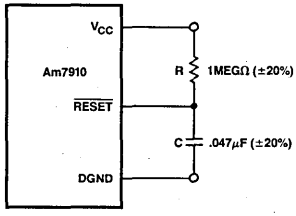
POWER ON RESET

The reset circuit operates in either of two modes.

Automatic Reset

In this mode an internal reset sequence is automatically entered when power is applied to the device. One resistor and one capacitor must be connected externally as shown in Figure 14. Values shown will work with most power supplies. Power supply (V_{CC}) rise time should be less than one half the RC time constant.

Figure 14. Automatic Reset



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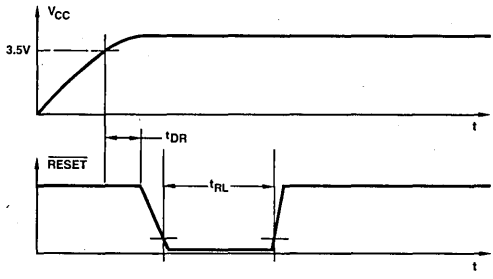
External Reset

In this mode the device may be forced into the reset sequence by application of an active LOW pulse applied to the $\overline{RESET}$ input. The reset must not be applied until the V_{CC} supply has reached at least 3.5V. Timing is diagrammed in Figure 15.

Figure 15. External Reset

TIMING DIAGRAMS



t_{DR} = delay from the time V_{CC} reaches 3.5V and the falling edge of $\overline{RESET}$ signal (>1μs)

t_{RL} = $\overline{RESET}$ LOW duration time (>t_{MCK} = 406ns)

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9

NOMINAL PERFORMANCE SPECIFICATIONS
TRANSMITTER (All Modem Types)

Input Data Format: Serial, asynchronous, standard TTL levels
Modulation Technique:
Binary, phase-coherent Frequency Shift Keying (FSK)
TC Output Level: −3dBm into 600Ω
Frequency Accuracy:
±0.4Hz all modems except Bell 202 (mark)
+1.0Hz Bell 202 (mark)
Harmonics: −45dB from fundamental for single tones

Delay uncertainty for TD logic input change to TC frequency change: ≤8.3μs

Out-of-band energy: See Figure 16

RECEIVER

Output Data Format: Serial, asynchronous, TTL levels
Demodulation Technique: Differential FM Detection
Sensitivity at Receiver Input: 0dBm to −48dBm
Frequency Deviation Tolerance: ±16Hz
Carrier Detect Threshold:

ON	>−43dBm ±1dB
OFF	<−48dBm ±1dB

TEST MEASUREMENT SETUP

Am7910 performance is characterized using the test equipment setup shown in Figure 17. The HP1645A data error analyzer is used to generate 511-bit pseudo random binary sequences (PRBS) at D_{OUT} for testing the modem. The 1645A also receives and analyzes the 511-bit digital pattern at D_{IN} after it has progressed around the test loop. A reference transmitter converts the digital sequence generated by the HP1645A into an FSK signal. The FSK signal is typically adjusted to different levels from −12 to −45dBm. The level-adjusted FSK signal or incident signal then passes through three pieces of equipment which comprise the telephone line simulator. The Wandel and Golterman TLN-1 and DLZ-4 simulate amplitude and group delay characteristics typical of a wide variety of phone lines. Line perturbations, such as amplitude hits and phase hits, may be injected by the Bradley 2A/2B.

The summing amplifier which drives the modem under test has three inputs. One of these inputs is the incident FSK signal which has been passed through a simulated phone line. The second input is from an optionally filtered noise source in order to simulate noise conditions which may be encountered on phone lines. The third input is from the transmitter of the Am7910 under test. This third input simulates the adjacent channel signal seen at the input of the Am7910 receiver due to the duplexer used on 2-wire lines. If 4-wire testing is being performed, the adjacent channel would not normally be included.

The HP3551A or HP3552A Transmission Test Set is used for measuring various levels which the modem under test is to receive. The levels of each of the three inputs to the summing amplifier should be measured independently of the other two inputs. For instance, the incident signal level should be measured by the transmission test set with no adjacent channel or noise present. The dashed line from the noise generator shows that the noise may or may not be measured at the output of the noise generator, depending on whether or not an optional filter is used, or on the characteristics of the filter.

Figure 16. Out-of-Band Transmitter Energy

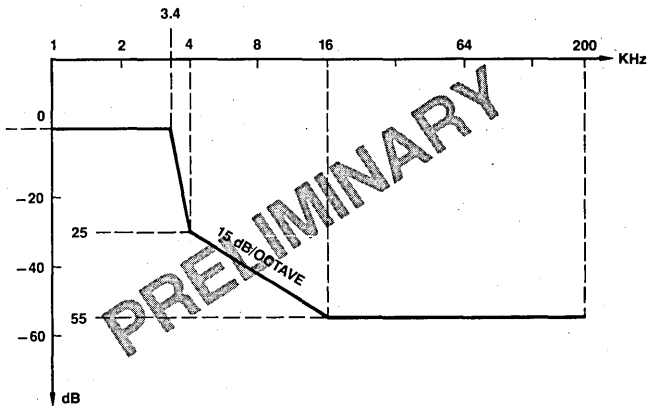

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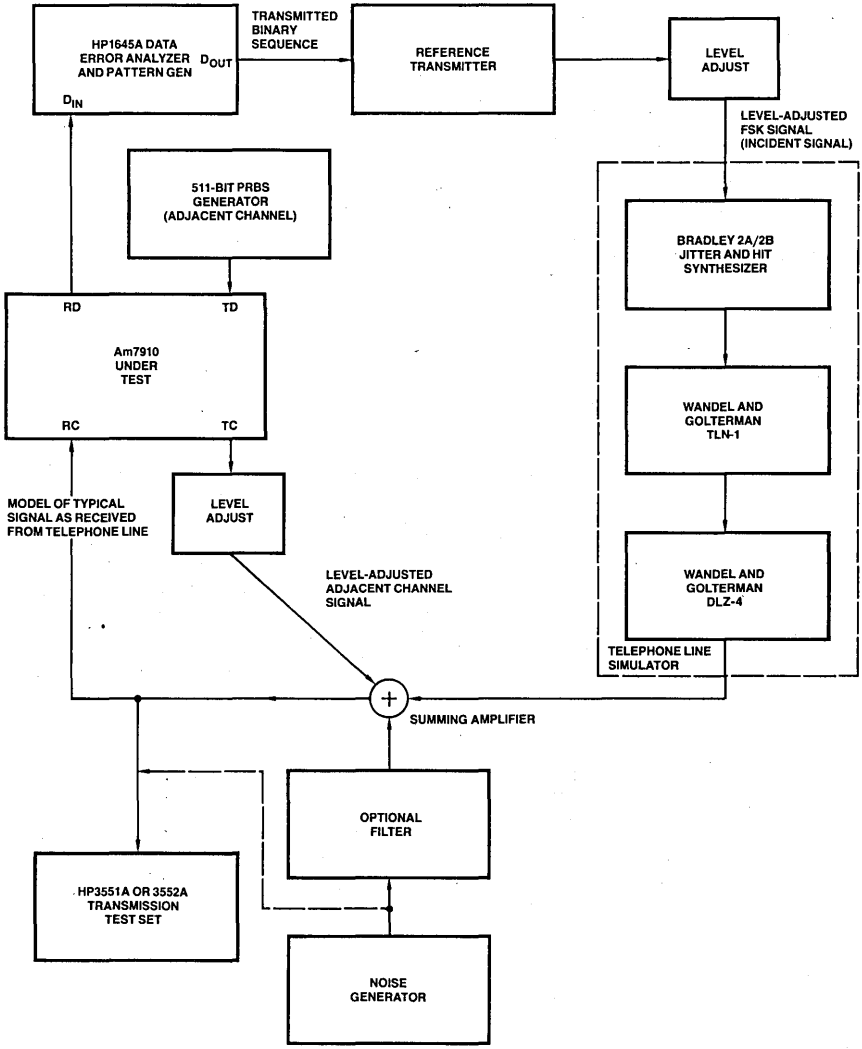
Figure 17. BER and Distortion Measurement Test Setup



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MAXIMUM RATINGS

Storage Temperature	−65 to +125°C
Ambient Temperature under Bias	0 to +70°C
V_{CC} with Respect to V_{DGND}	+6V/−.4V
V_{BB} with Respect to V_{DGND}	−6V/+.4V
All Signal Voltages with Respect to V_{DGND}	±5V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE

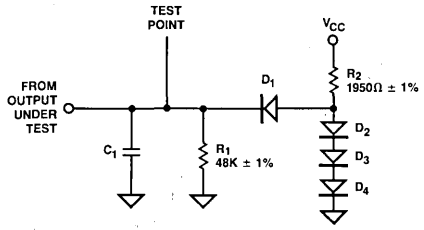
Ambient Temperature	V_{CC}	V_{BB}	V_{AGND}	V_{DGND}
$0°C \leq T_A \leq +70°C$	+5.0V ±5%	−5.0V ±5%	0V ±50mV	0V

DC CHARACTERISTICS

Digital Inputs: TD, $\overline{RTS}$, MC_0–MC_4, $\overline{DTR}$, $\overline{RING}$, BTD, $\overline{BRTS}$
Digital Outputs: RD, $\overline{CTS}$, $\overline{CD}$, BRD, $\overline{BCTS}$, $\overline{BCD}$

Parameters	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -50\mu A$, $C_{LD} = 50pF$	2.4			Volts
V_{OL}	Output LOW Voltage	$I_{OL} = +2mA$, $C_{LD} = 50pF$			0.4	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage		−0.5		+0.8	Volts
V_{IHC}	External Clock Input HIGH ($XTAL_1$)		3.8		V_{CC}	Volts
V_{ILC}	External Clock Input LOW ($XTAL_1$)		−0.5		0.8	Volts
V_{IHR}	External Reset Input HIGH ($\overline{RESET}$)		−0.5		V_{CC}	Volts
V_{ILR}	External Reset Input LOW ($\overline{RESET}$)		3.8		0.8	Volts
I_{IL}	Digital Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$	−10		+10	μA
I_{CC}	V_{CC} Supply Current				125	mA
I_{BB}	V_{BB} Supply Current				25	mA
C_{OUT}	Output Capacitance	$f_C = 1.0MHz$		5	15	pF
C_{IN}	Input Capacitance	$f_C = 1.0MHz$		5	15	pF
Analog Input (RC):						
R_{IN}	Input Resistance	$-1.6V < V_{RC} < +1.6V$	50			Kohms
V_{RC}	Operating Input Signal		−1.6		+1.6	Volts
V_{RCOS}	Allowed DC Input Offset	REF V_{AGND}	−30		+30	mV
Analog Output (TC):						
V_{TC}	Output Voltage	$R_L = 600\Omega$	−1.1		+1.1	Volts
V_{TCOS}	Output DC Offset			±200		mV

STANDARD LOAD CIRCUIT



01238C-20

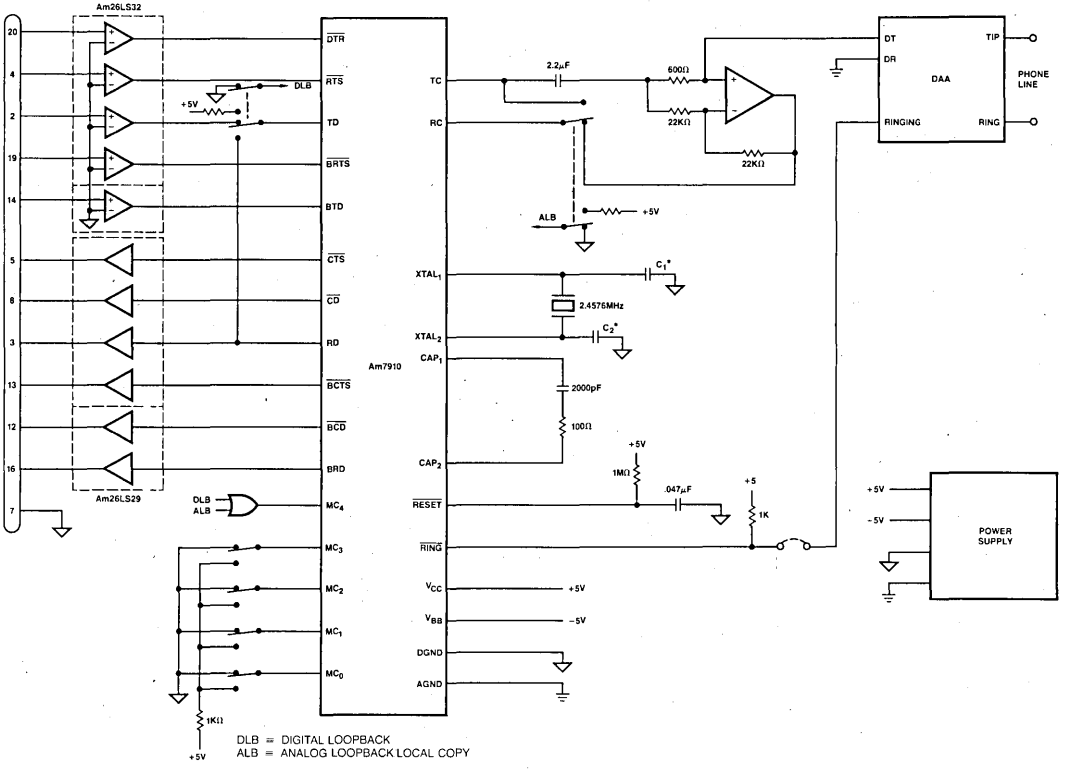
Notes:
1. C_1 = 50pF including stray and wiring capacitance
2. All diodes are IN3064 or equivalent
3. All resistors are 1/8 watt
4. V_{CC} = 5 volts ±1%

APPLICATIONS

Figure 18 depicts a stand-alone Am7910 configuration. An op amp and three resistors provide a duplexor function to put the transmitter output onto the line while receiving adjacent channel data from the line. Connection to the line is via a Data Access Arrangement (DAA). Note the lack of external analog filters. The TTL handshake signals may be level converted to RS-232, RS-422, or V.24 using appropriate devices. Mode control lines are hardwired or connected to switches.

Figure 19 depicts use of the Am7910 when a microprocessor resides in the same physical location. The duplexor/line interface is identical to the above configuration. However, the handshake signals interface directly to a UART-type device which in turn interfaces to a microprocessor. The mode control lines might also be controlled by the microprocessor.

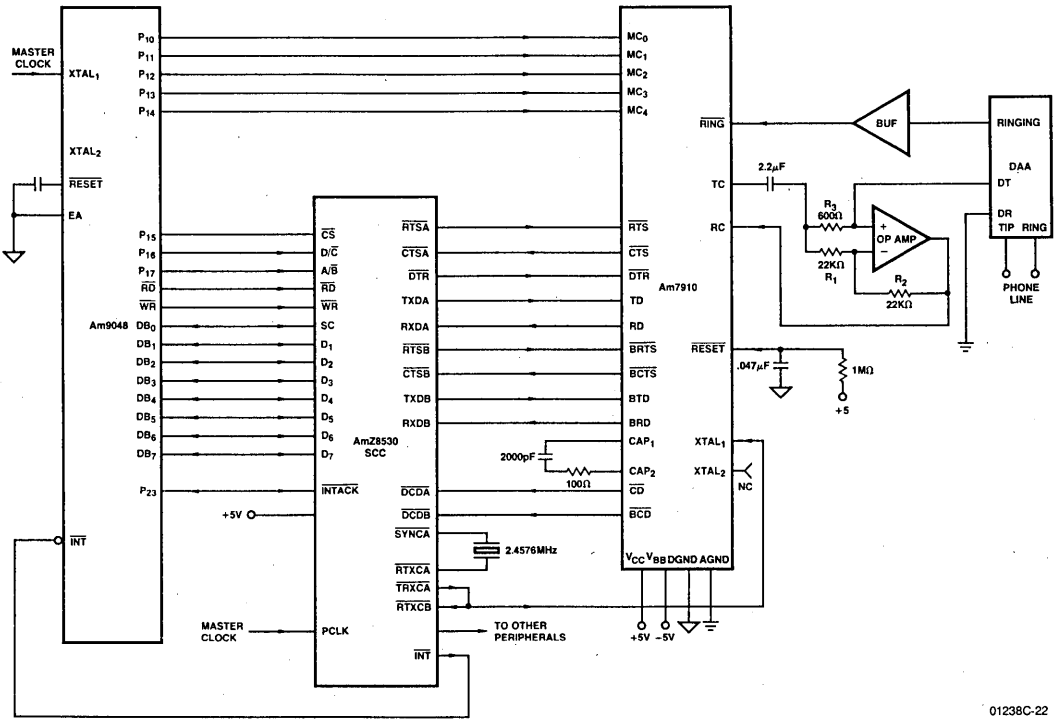
Figure 18. Stand-Alone Am7910 Application



*See Figure 13

01238C-21

Figure 19. Microprocessor Application



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Cerdip	$0° \leq T_A \leq +70°C$	Am7910DC
Plastic DIP		Am7910PC
Leadless Carrier		Am7910LC

Plastic and leadless carrier packages to be announced.

AmZ8030 • AmZ8530 (SCC)

Serial Communications Controller

DISTINCTIVE CHARACTERISTICS

- **Two 1M.bps full duplex serial channels**
  Each channel has independent oscillator, baud-rate generator, and PLL for clock recovery, dramatically reducing external components.
- **Programmable protocols**
  NRZ, NRZI, and FM data encoding supported under program control.
- **Programmable Asynchronous Modes**
  5 to 8 bit characters with prorammable stop bits, clock, break detect, and error conditions.
- **Programmable Synchronous Modes**
  SDLC and HDLC and SDLC loop supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generators and checkers.
- **Z8000* compatible**
  The Z8030 interfaces directly to the Z8000 CPU bus and to the Z8000 interrupt structure.
- **Compatible with non-multiplexed bus**
  The Z8530 interfaces easily to most other CPUs.

GENERAL DESCRIPTION

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats, Synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The SCC is offered in two versions. The AmZ8030 is directly compatible with the Z8000 and 8086 CPUs. The AmZ8530 is designed for non-multiplexed buses and is easily interfaced to most other CPUs, such as 8080, Z80, 6800 68000, and †Multibus.

BLOCK DIAGRAM

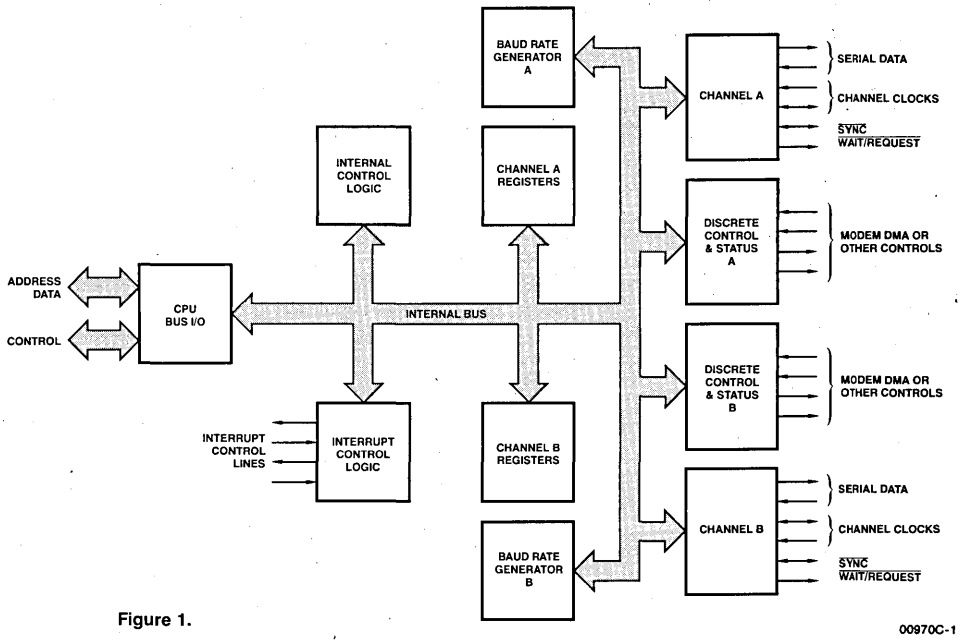


Figure 1.

*Z8000, Z8030 and Z8530 are trademarks of Zilog, Inc. †MULTIBUS is a trademark of Intel.

ARCHITECTURE

The SCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to the Z8000 CPU (AmZ8030) or to a non-multiplexed CPU bus (AmZ8530). Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices (Figure 1).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two synchronous character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the Interrupt Pending bits (A only).

The registers for each channel are designated as follows:

WR0-WR15 – Write Registers 0 through 15.
RR0-RR3, RR10, RR12, RR13, RR15 – Read Registers 0 through 3, 10, 12, 13, 15.

The following table lists the functions assigned to each read or write register. The SCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

DATA PATH

The transmit and receive data path illustrated in Figure 2 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

TABLE 1. READ AND WRITE REGISTER FUNCTIONS

READ REGISTER FUNCTIONS	
RR0	Transmit/Receive buffer status and External status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only)
RR3	Interrupt Pending bits (Channel A only)
RR8	Receive buffer
RR10	Miscellaneous status
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/Status interrupt information

WRITE REGISTER FUNCTIONS	
WR0	CRC initialize, initialization commands for the various modes, shift right/shift left command
WR1	Transmit/Receive interrupt and data transfer mode definition
WR2	Interrupt vector (accessed through either channel)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync characters or SDLC address field
WR7	Sync character or SDLC flag
WR8	Transmit buffer
WR9	Master interrupt control and reset (accessed through either channel)
WR10	Miscellaneous transmitter/receiver control bits
WR11	Clock mode control
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits
WR15	External/Status interrupt control

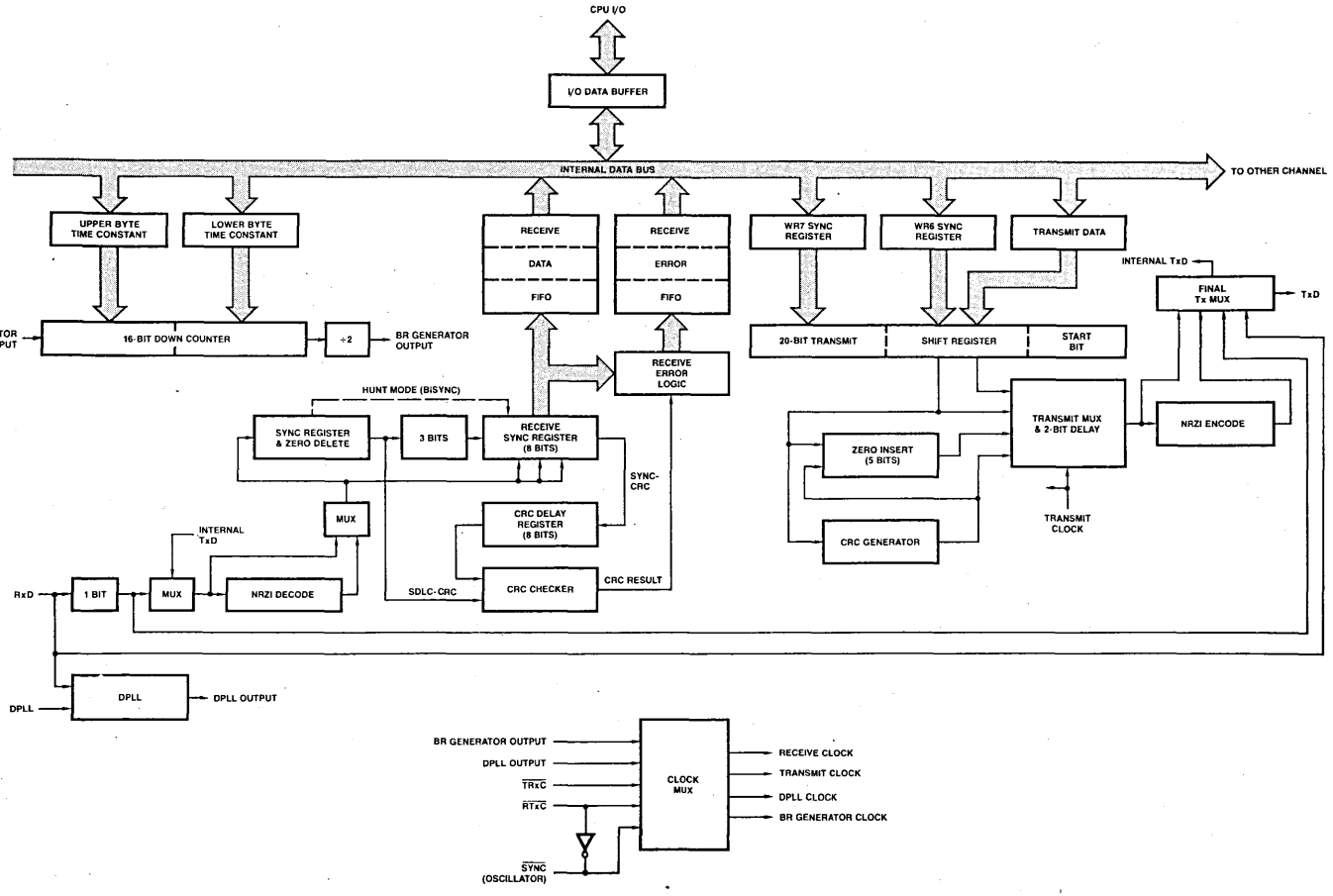


Figure 2. Data Path

FUNCTIONAL DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

DATA COMMUNICATIONS CAPABILITIES

The SCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data-communication protocol. Figure 3 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 18). If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The SCC does not require symmetric transmit and receive clock signals – a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input used for functions such as monitoring a ring indicator.

Synchronous Modes

The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), any 12-bit synchronous pattern (Bisync), or with an external synchronous signal. Leading synchronous characters can be removed without interrupting the CPU.

Five- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multiple incoming synchronous characters as shown in Figure 4.

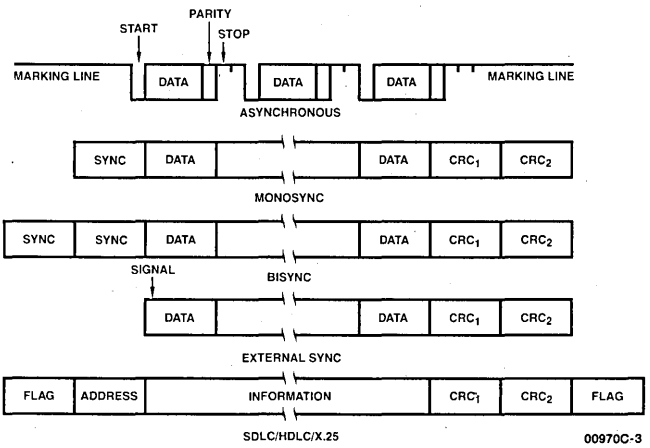


Figure 3. SCC Protocols

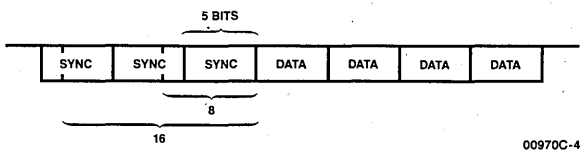


Figure 4. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols such as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all synchronous modes. Users may preset the CRC generator and checker to all 1s or all 0s. The SCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{SYNC}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The SCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC LOOP MODE

The SCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 5).

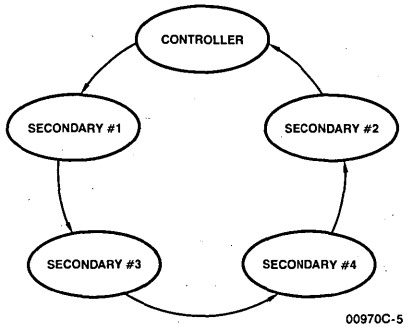


Figure 5. An SDLC Loop

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary one of the EOP to a zero before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the SCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

BAUD RATE GENERATOR

Each channel in the SCC contains a programmable Baud-rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero, the value in the

time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds.)

$$\text{baud rate} = \frac{1}{2\,(\text{time constant} + 2) \times (\text{BR clock period})}$$

Time-Constant Values for Standard Baud Rates at BR Clock = 3.9936MHz

Rate (Baud)	Time Constant (decimal notation)	Error
19200	102	–
9600	206	–
7200	275	0.12%
4800	414	–
3600	553	0.06%
2400	830	–
2000	996	0.04%
1800	1107	0.03%
1200	1662	–
600	3326	–
300	6654	–
150	13310	–
134.5	14844	0.0007%
110	18151	0.0015%
75	26622	–
50	39934	–

DIGITAL PHASE-LOCKED LOOP

The SCC contains a digital phase-locked-loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{TRxC}$ pin (if this pin is not being used as an input).

DATA ENCODING

The SCC may be programmed to encode and decode the serial data in four different ways (Figure 6). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, as 1 is represented by no change in level and a 0 is represented by a change in level. In FM_1 (more properly, bi-phase mark) a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM_0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell,

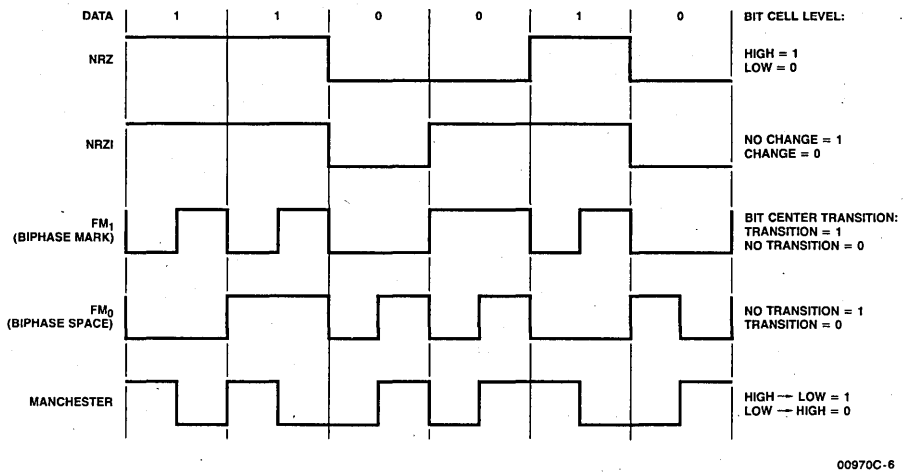


Figure 6. Data Encoding Methods

and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1 the bit is a 0. If the transition is 1/0 the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The SCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes, but works in synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{CTS}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{WAIT/REQUEST}$ on transmit.

The SCC is also capable of local loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The CTS and DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

I/O INTERFACE CAPABILITIES

The SCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the SCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When a SCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 8 and 9).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other two bits are related to the Z-Bus interrupt priority chain (Figure 7). As a Z-Bus peripheral, the SCC may request an interrupt only when no higher-priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the A/D bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the INT output is pulled Low, requesting an interrupt. In the SCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive and External/Status interrupts. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receiver, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so

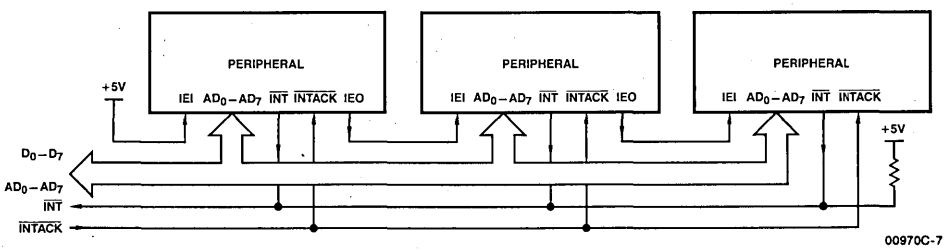


Figure 7. Z-Bus Interrupt Schedule

that it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition.
- Interrupt on all Receive Characters or Special Receive condition.
- Interrupt on Special Receive condition only.

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in Asynchronous mode, End-of-Frame in SDLC mode and, optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt-Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break (asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the SCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{WAIT}/\overline{REQUEST}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{WAIT}/\overline{REQUEST}$ output can be defined under software control as a $\overline{WAIT}$ line in the CPU Block Transfer mode or as a $\overline{REQUEST}$ line in the DMA Block Transfer mode.

To a DMA controller, the SCC $\overline{REQUEST}$ output indicates that the SCC is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{DTR}/\overline{REQUEST}$ line allows full-duplex operation under DMA control.

PROGRAMMING

Each channel has fifteen Write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has eight Read registers from which the system can read Status, Baud rate, or Interrupt information.

The AmZ8030 and AmZ8530 differ in the way the system accesses these registers:

In the AmZ8030 all registers are directly addressable from the multiplexed Address Data bus. See Figure 10 and Figure 11 for timing. The AmZ8030 can operate in either of two modes: when bit 0 in Write Register 0 is reset (or after initialization with a hardware reset) Address lines AD_1 through AD_5 select the register to be read from or written into during Data Stroke $\overline{DS}$. (This is called left shift and is the natural AmZ8000 mode). When bit 0 in Write Register 0 is set, Address lines AD_0 through AD_4 select the register to be read from or written into. (This is called right shift and is more natural for interfacing with other microprocessors.)

Table 2 describes the register addressing for both modes.

Channel A/Channel B selection is made either by AD_0 or by AD_5.

If Bit D_0 in WR0 is reset (or after hardware reset):

AD_5 selects the channel (0 = B, 1 = A)
(this is called "Select Shift Left Mode")

If Bits D_0 and D_1 in WR0 are set, AD_0 selects the channel (0 = B, 1 = A) (this is called "Select Shift Right Mode)

In the AmZ8530 only the four data registers (Read, Write for channels A and B) are directly selected by a High on the $D/\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$ and $A/\overline{B}$ pins. All other registers are addressed indirectly by the content of Write Register 0 in conjunction with a Low on the $D/\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$ and $A/\overline{B}$ pins. If bit 4 in WW0 is 1 and bits 5 and 6 are 0 then bits 0, 1, 2 address the higher registers 8 through 15. If bits 4, 5, 6 contain a different code, bits 0, 1, 2 address the lower registers 0 through 7 as shown on Table 3.

TABLE 2. REGISTER ADDRESSING (AmZ8030 ONLY)

AD_4	AD_3	AD_2	AD_1	Write Register	Read Register
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	(0)
0	1	0	1	5	(1)
0	1	1	0	6	(2)
0	1	1	1	7	(3)
1	0	0	0	Data	Data
1	0	0	1	9	–
1	0	1	0	10	10
1	0	1	1	11	(15)
1	1	0	0	12	12
1	1	0	1	13	13
1	1	1	0	14	(10)
1	1	1	1	15	15

Writing to or reading from any register except RR0, WR0 and the Data Registers thus involves two operations:

First write the appropriate code into WR0, then follow this by a write or read operation on the register thus specified. Bits 0 through 4 in WW0 are automatically cleared after this operation, so that WW0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the $A/\overline{B}$ input (High = A, Low = B)

In both AmZ8030 and AmZ8530 the system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set, and finally, receiver or transmitter enable.

TABLE 3. REGISTER ADDRESSING (AmZ8530 ONLY)

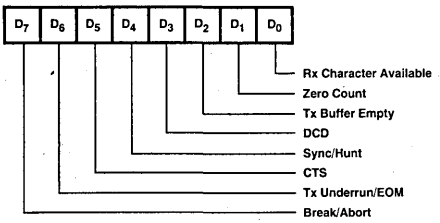
D/C "Point High" Code in WR0:		D_2 in WR0:	D_1 in WR0:	D_0	Write Register	Read Register
High	Either way	X	X	X	Data	Data
Low	Not true	0	0	0	0	0
Low	Not true	0	0	1	1	1
Low	Not true	0	1	0	2	2
Low	Not true	0	1	1	3	3
Low	Not true	1	0	0	4	(0)
Low	Not true	1	0	1	5	(1)
Low	Not true	1	1	0	6	(2)
Low	Not true	1	1	1	7	(3)
Low	True	0	0	0	Data	Data
Low	True	0	0	1	9	–
Low	True	0	1	0	10	10
Low	True	0	1	1	11	(15)
Low	True	1	0	0	12	12
Low	True	1	0	1	13	13
Low	True	1	1	0	14	(10)
Low	True	1	1	1	15	15

READ REGISTERS

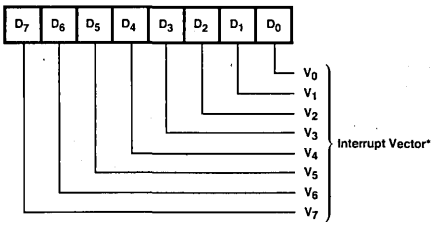
The SCC contains eight read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 8 shows the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

Read Register 0

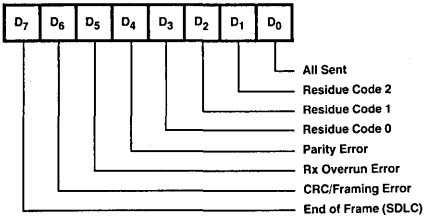


Read Register 2

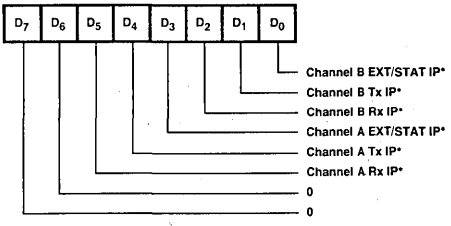


*Modified In B Channel

Read Register 1



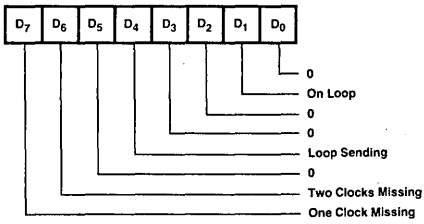
Read Register 3



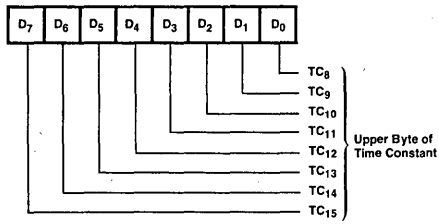
*Always 0 in B Channel

Figure 8. Read Register Bit Functions

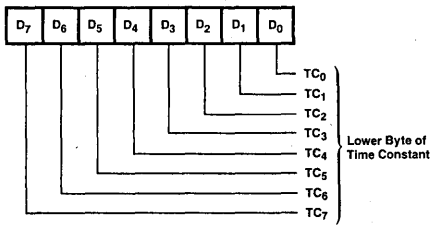
Read Register 10



Read Register 13



Read Register 12



Read Register 15

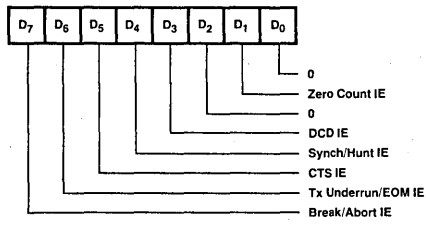
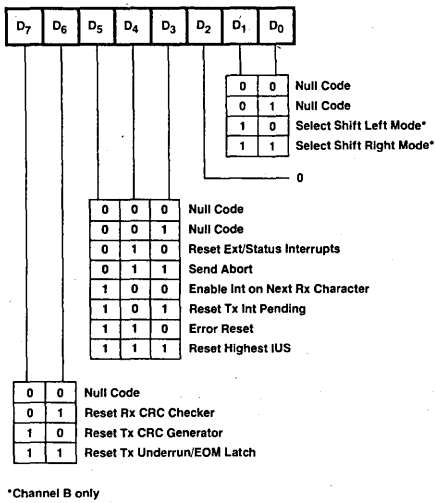


Figure 8. Read Register Bit Functions (Cont.)

WRITE REGISTERS

The SCC contains 15 write registers (16 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 9 shows the format of each write register.

Write Register 0 (AmZ8030)



*Channel B only

Write Register 0 (AmZ8530)

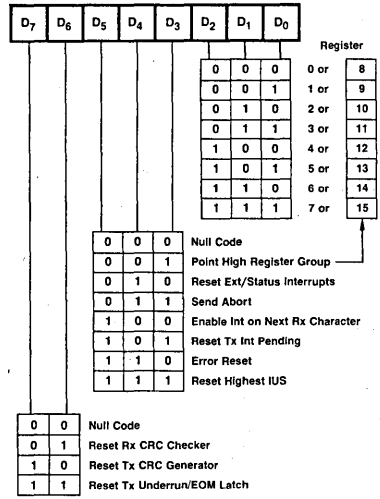
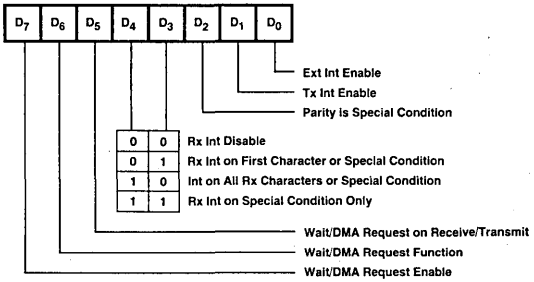
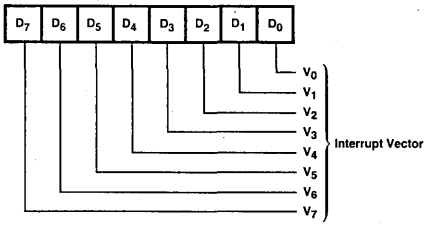


Figure 9. Write Register Bit Functions

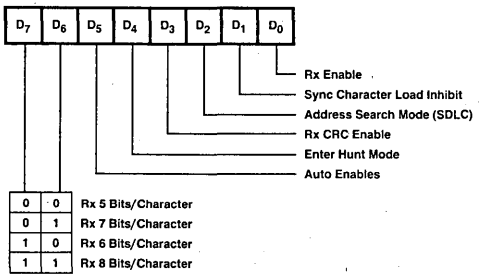
Write Register 1



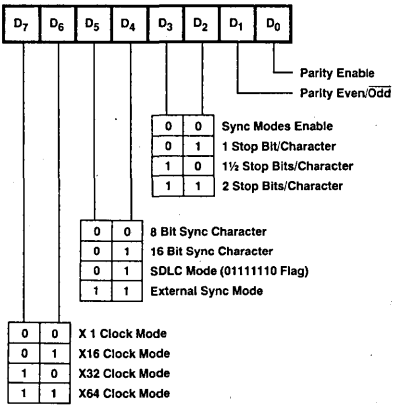
Write Register 2



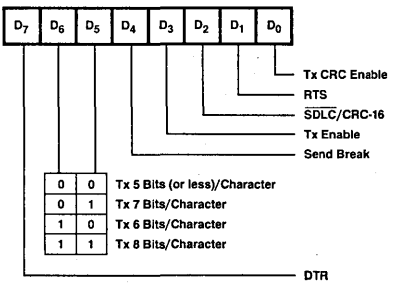
Write Register 3



Write Register 4



Write Register 5



Write Register 6

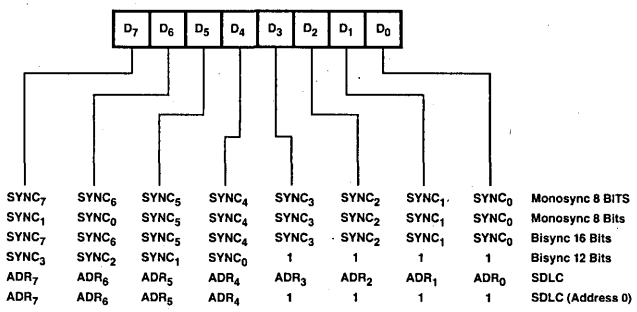
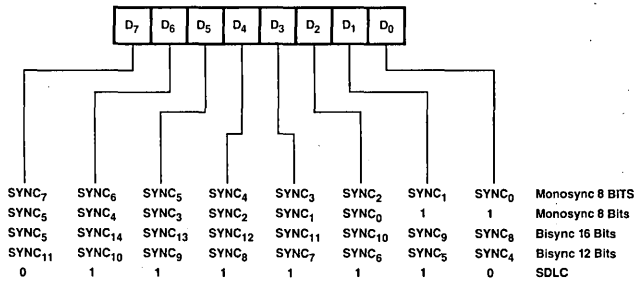
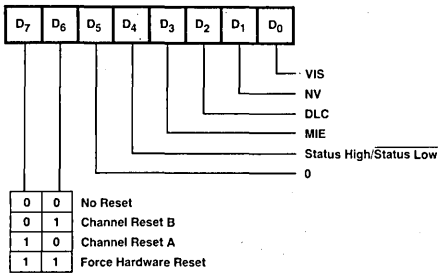


Figure 9. Write Register Bit Functions (Cont.)

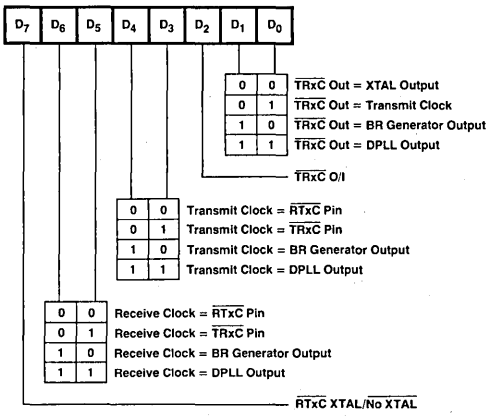
Write Register 7



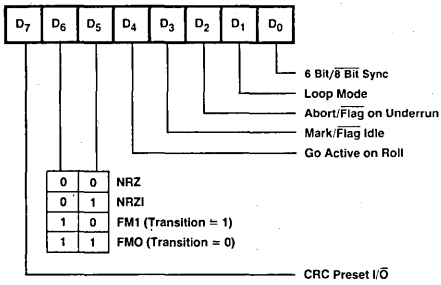
Write Register 9



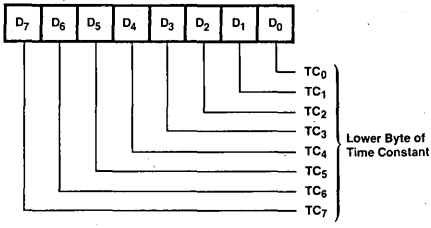
Write Register 11



Write Register 10



Write Register 12



Write Register 13

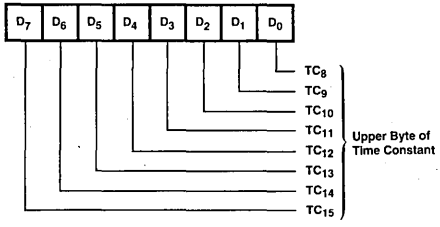


Figure 9. Write Register Bit Functions (Cont.)

Write Register 14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								BR Generator Enable
								BR Generator Source
								$\overline{DTR}$/Request Function
								Auto Echo
								Local Loopback
0	0	0						Null Command
0	0	1						Enter Search Mode
0	1	0						Reset Missing Clock
0	1	1						Disable DPLL
1	0	0						Set Source = BR Generator
1	0	1						Set Source = $\overline{RTxC}$
1	1	0						Set FM Mode
1	1	1						Set NRZI Mode

Write Register 15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								0
								Zero Count IE
								0
								DCD IE
								Sync/Hunt IE
								CTS IE
								Tx Underrun/EOM IE
								Break/Abort IE

Figure 9. Write Register Bit Functions (Cont.)

AmZ8030 TIMING

The SCC generates internal control signals from $\overline{AS}$ and $\overline{DS}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{AS}$ and $\overline{DS}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC to the falling edge of $\overline{DS}$ in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200 ns.

READ CYCLE TIMING

Figure 10 illustrates read cycle timing. The address on AD_0 – AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be High to indicate a read cycle. CS_1 must also be High for the read cycle to occur. The data bus drivers in the SCC are then enabled while $\overline{DS}$ is Low.

WRITE CYCLE TIMING

Figure 11 illustrates write cycle timing. The address on AD_0 – AD_7 and the state if $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be Low to indicate a write cycle. CS_1 must be High for the write cycle to occur. $\overline{DS}$ Low strobes the data into the SCC.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 12 illustrates interrupt acknowledge cycle timing. The address on AD_0 – AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. However, if $\overline{INTACK}$ is Low, the address and $\overline{CS_0}$ are ignored. The state of R/$\overline{W}$ and CS_1 are also ignored for the duration of the interrupt acknowledge cycle. Between the rising edge of $\overline{AS}$ and the falling edge of $\overline{DS}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is High when $\overline{DS}$ falls, the acknowledge cycle was intended for the SCC. In this case, the SCC may be programmed to respond to $\overline{DS}$ Low by placing its interrupt vector on AD_0 – AD_7. It then sets the appropriate interrupt-under-service latch internally.

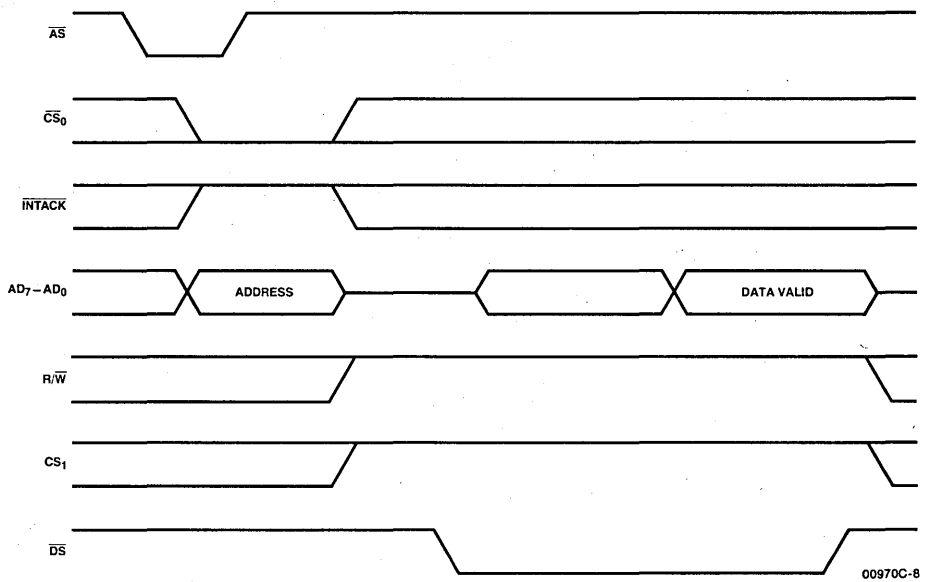


Figure 10. Read Cycle Timing

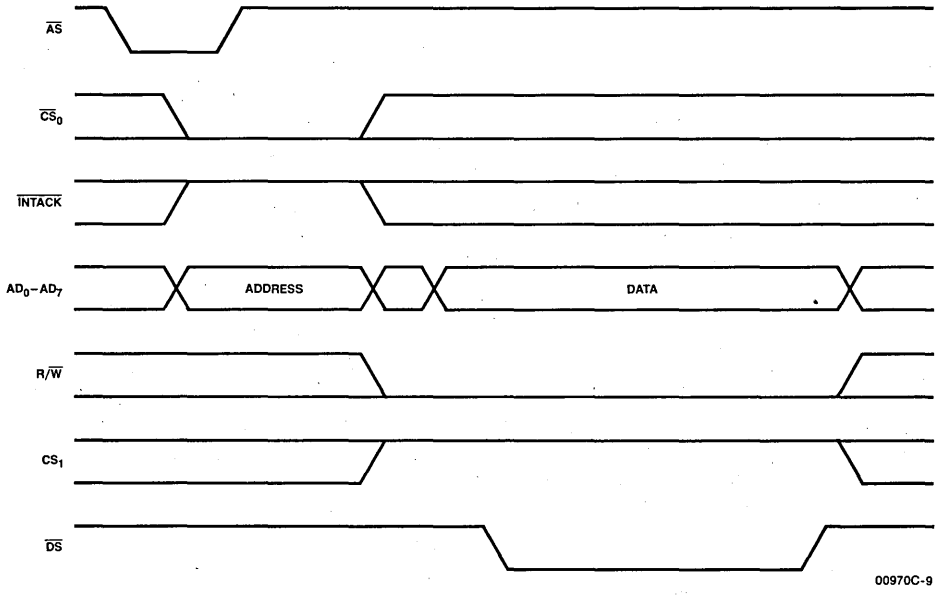


Figure 11. Write Cycle Timing

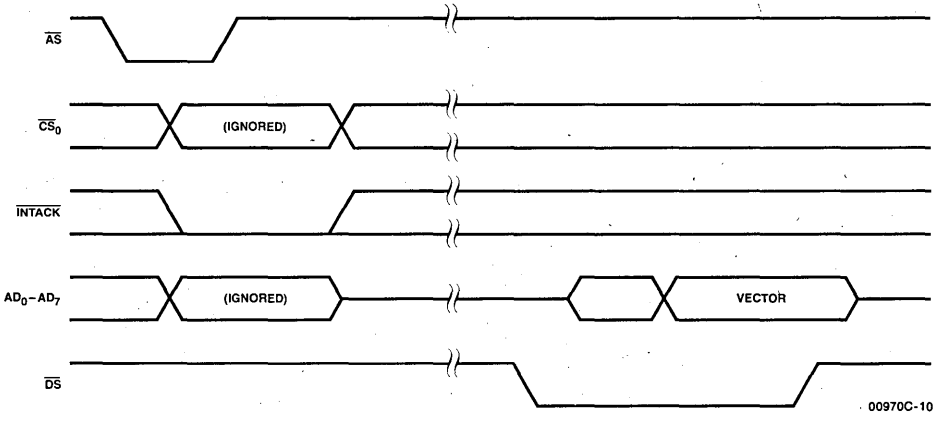


Figure 12. Interrupt Acknowledge Cycle Timing

AmZ8530 TIMING

The SCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions invloving the SCC. The recovery time required for proper operation is specified from the rising edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction invloving the SCC to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200ns.

Read Cycle Timing

Figure 13 illustrates Read cyle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

Write Cycle Timing

Figure 14 illustrates Write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened.

Interrupt Acknowledge Cycle Timing

Figure 15 illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{INTACK}$ goes Low and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is High when $\overline{RD}$ falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to $\overline{RD}$ Low by placing its interrupt vector on D_0-D_7 and it then sets the appropriate Interrupt-Under-Service internally.

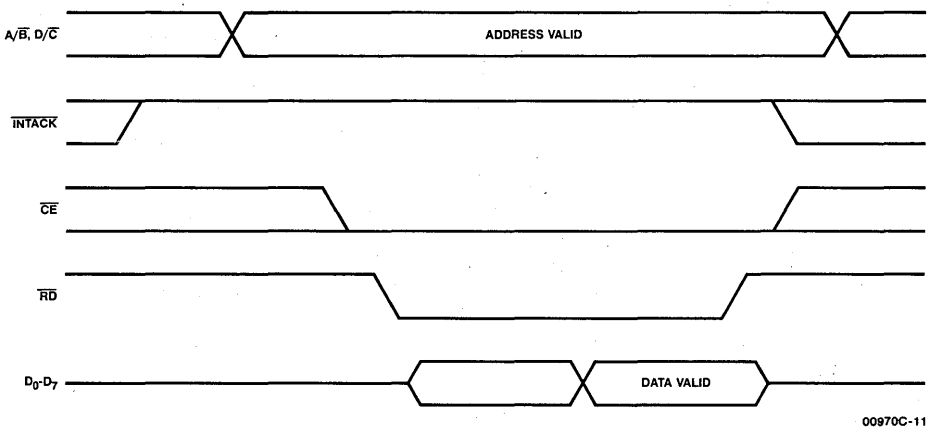


Figure 13. Read Cycle Timing

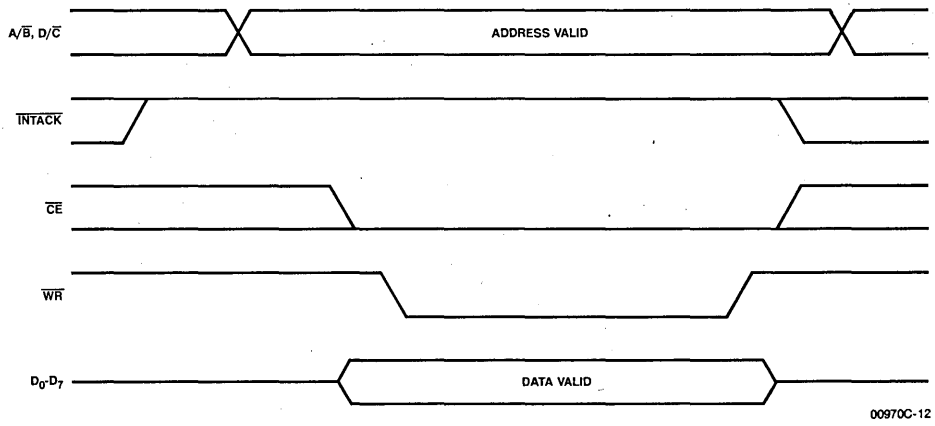


Figure 14. Write Cycle Timing

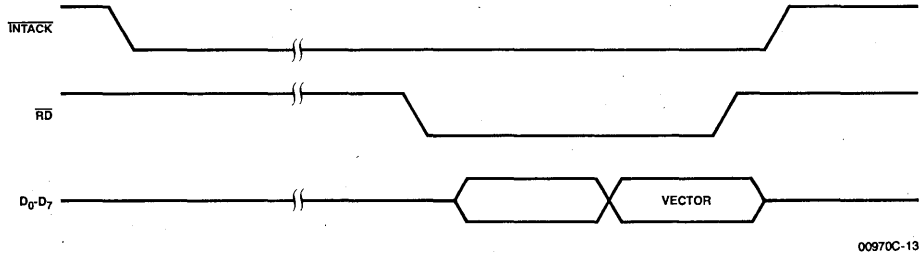


Figure 15. Interrupt Acknowledge Cycle Timing

PIN DESCRIPTIONS FOR AmZ8030

The following section describes the pin functions of the SCC. Figures 16 and 17 detail the respective pin functions and pin assignments.

V_{CC}: +5V Power Supply

GND: Ground

AD_0 – AD_7: Address/Data Bus (bidirectional, active High, 3-state).

These multiplexed lines carry register addresses to the SCC as well as data or control information to and from the SCC.

$\overline{AS}$: Address Strobe (input, active Low).

Addresses on AD_0 – AD_7 are latched by the rising edge of this signal.

$\overline{CS_0}$: Chip Select 0 (input, active Low).

This signal is latched concurrently with the addresses on AD_0 – AD_7 and must be active for the intended bus transaction to occur.

CS_1: Chip Select 1 (input, active High).

This second select signal must also be active before the intended bus transaction can occur. CS_1 must remain active throughout the transaction.

$\overline{CTSA}$, $\overline{CTSB}$: Clear to Send (Inputs, active Low).

If these pins are programmed as Auto Enables, a Low on these inputs enables their respective transmitter. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

$\overline{DCDA}$, $\overline{DCDB}$: Data Carrier Detect (Inputs, active Low).

These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

$\overline{DS}$: Data Strobe (Input, active Low).

This signal provides timing for the transfer of data into and out of the SCC. If $\overline{AS}$ and $\overline{DS}$ coincide, this is interpreted as a reset.

$\overline{DTR}$/$\overline{REQA}$, $\overline{DTR}$/$\overline{REQB}$: Data Terminal Ready/Request (outputs, active Low).

These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

IEI: Interrupt Enable In (input, active High).

IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO: Interrupt Enable Out (output, active High).

IEO is High only if IEI is High and the CPU is not servicing a SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$: Interrupt Request (output, open-drain, active Low).

This signal is activated when the SCC requests an interrupt.

$\overline{INTACK}$: Interrupt Acknowledge (input, active Low).

This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{DS}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of $\overline{AS}$.

PCLK: Clock (input)

This is the master SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be at least 90% of the CPU clock frequency for a Z8000. PCLK is a TTL level signal. Maximum transmit rate is 1/4 PCLK.

RxDA, RxDB: Receive Data (inputs, active High)

These input signals receive serial data at standard TTL levels.

$\overline{RTxCA}$, $\overline{TRxCB}$: Receive/Transmit Clocks (inputs, active Low)

These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud-rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

$\overline{RTSA}$, $\overline{RTSB}$: Request to Send (outputs active Low)

When the Request to Send RTS bit in Write Register 5 (Figure 6) is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the $\overline{RTS}$ pins strictly follow the state of the RTS bit. Both pins can be used as general-purpose outputs.

R/$\overline{W}$: Read/Write (input)

This signal specifies whether the operation to be performed is read or a write.

$\overline{SYNCA}$, $\overline{SYNCB}$: Synchronization (inputs or outputs, active Low)

These pins can act either as inputs, ouputs, or part of the crystal oscillator circuit.

In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 5) but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low two receive clock cycles after the last bit in the Synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as out-puts and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronous pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB: Transmit Data (outputs, active High)

These output signals transmit serial data at standard TTL levels.

$\overline{TRxCA}$, $\overline{TRxCB}$: Transmit/Receive Clocks (Inputs or outputs, active Low)

These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{W}$/$\overline{REQA}$, $\overline{W}$/$\overline{REQB}$: Wait/Request (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function)

These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

PIN DESCRIPTIONS FOR AmZ8530

The following section describes the pin functions of the SCC. Figures 18 and 19 detail the respective pin functions and pin assignments.

V_{CC}: +5V Power Supply

GND: Ground

A/$\overline{B}$. *Channel A/Channel B Select* (input). This signal selects the channel in which the read or write operation occurs.

$\overline{CE}$. *Chip Enable* (input, active Low). This signal selects the SCC for a read or write operation.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

D/$\overline{C}$. *Data/Control Select* (input). This signal defines the type of information transferred to or from the SCC. A High means data is transferred; a Low indicates a command.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accomodate slow rise time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

D_0-D_7. *Data Bus* (bidirectional, 3-state). These lines carry data and commands to and from the SCC.

$\overline{DTR}$/$\overline{REQA}$, $\overline{DTR}$/$\overline{REQB}$. *Data Terminal Ready/Request* (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$. *Interrupt Request* (output, open-drain, active Low). This signal is activated when the SCC requests an interrupt.

$\overline{INTACK}$. *Interrupt Acknowledge* (input, active Low). This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of PCLK.

PCLK. *Clock* (input). This is the master SCC clock used to synchronize internal signals PCLK is a TTL level signal.

$\overline{RD}$. *Read* (input, active Low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

RxDA, RxDB. *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

$\overline{RTxCA}$, $\overline{RTxCB}$. *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

$\overline{RTSA}$, $\overline{RTSB}$. *Request To Send* (outputs active Low). When the Request to Send (RTS) bit in Write Register 5 (Figure 6) is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{SYNCA}$, $\overline{SYNCB}$. *Synchronization* (inputs or outputs, active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 5) but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB. *Transmit Data* (outputs, active High). These output signals transmit serial data at standard TTL levels.

$\overline{TRxCA}$, $\overline{TRxCB}$. *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{WR}$. *Write* (input, active Low). When the SCC is selected, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.

$\overline{W/REQA}$, $\overline{W/REQB}$. *Wait/Request* (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

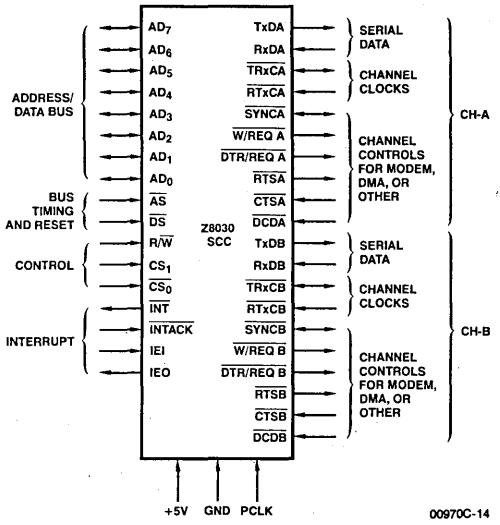
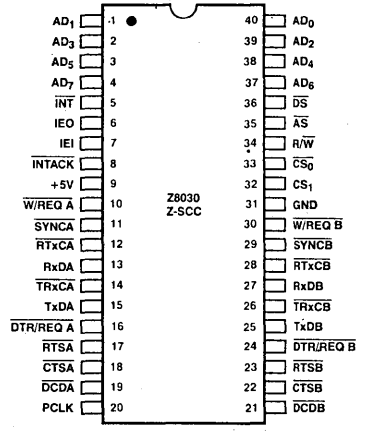


Figure 16. Logic Symbol

D-40
P-40



Note: Pin 1 is marked for orientation. 00970C-15

Figure 17. Connection Diagram

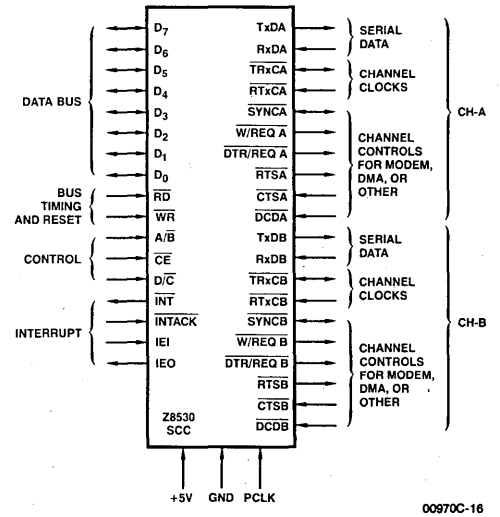
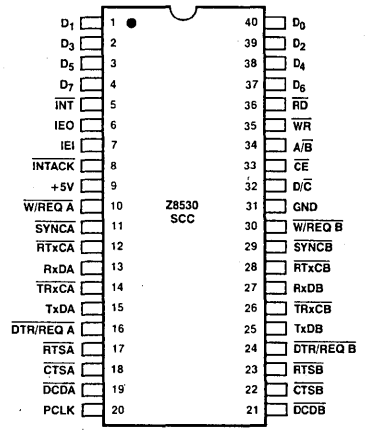


Figure 18. Logic Symbol

D-40
P-40



Note: Pin 1 is marked for orientation. 00970C-17

Figure 19. Connection Diagram

ORDERING INFORMATION

Example Z8030 A D C B

- Basic Device
- Speed: Blank = 4MHz; A = 6MHz
- Package Type: D = Hermetic DIP; P = Molded Plastic
- Temperature Range: C = 0 to +70°C; I = −40 to +85°C; M = −55 to +125°C
- Burn-in

Example Z8530 A D C B

- Basic Device
- Speed: Blank = 4MHz; A = 6MHz
- Package Type: D = Hermetic DIP; P = Molded Plastic
- Temperature Range: C = 0 to +70°C; I = −40 to +85°C; M = −55 to +125°C
- Burn-in

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MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65 to +150°C
Voltage at any Pin Relative to V_{SS}	−0.5 to +7.0V
Power Dissipation	1.8W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

(over which the DC, switching and functional specifications apply)

	4MHz	6MHz
Commercial Operating Range T_A = 0 to +70°C V_{CC} = 5V ± 5%	Z8030DC Z8030PC Z8530DC Z8530PC	Z8030ADC Z8030APC Z8530ADC Z8530APC
Industrial Operating Range T_A = −40 to +85°C V_{CC} = 5V ± 5%	Z8030DI Z8530DI	
Military Operating Range T_A = −55 to +125°C V_{CC} = 5V ± 10%	Z8030DMB Z8530DMB	

Notes: T_A denotes ambient temperature.
Add suffix B to indicate burn-in requirement.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	Standard	2.0		V_{CC} + 0.3	V
		Military	2.2			
V_{IL}	Input LOW Voltage		−0.3		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −250μA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = +2.0mA			0.4	V
I_{IL}	Input Leakage	0.4 ≤ V_{IN} ≤ +2.4V			±10.0	μA
I_{OL}	Output Leakage	0.4 ≤ V_{OUT} ≤ +2.4V			±10.0	μA
I_{CC}	V_{CC} Supply Current				250	mA
C_{IN}	Input Capacitance	Unmeasured pins returned to ground. f = 1MHz over specified temperature range.			10	pF
C_{OUT}	Output Capacitance				15	pF
$C_{I/O}$	Bidirectional Capacitance				20	pF

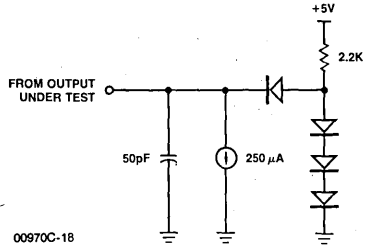
V_{CC} = 5V ± 5% unless otherwise specified, over specified temperature range.

Standard Test Conditions

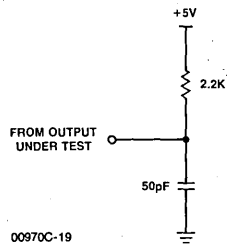
The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75V ≤ V_{CC} ≤ +5.25V
GND = 0V
0°C ≤ T_A ≤ +70°C

Standard Test Load



Open Drain Test Load



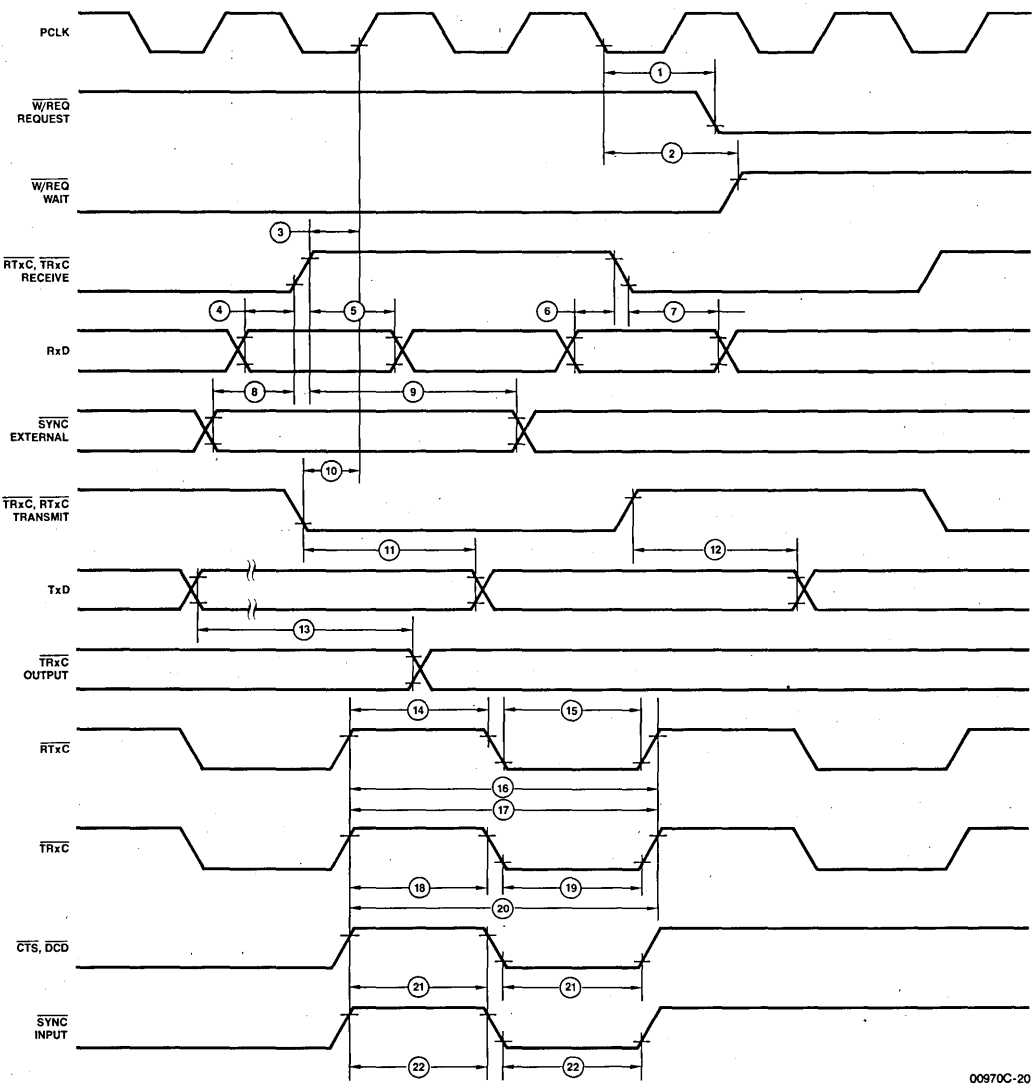
GENERAL TIMING

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay		250		250	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		350	ns
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (Notes 1, 4)	50		50		ns
4	TsRXD(RXCr)	RxD to RxC ↑ Setup Time (XI Mode) (Note 1)	0		0		ns
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (XI Mode) (Note 1)	150		150		ns
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		ns
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (XI Mode) (Notes 1, 5)	150		150		ns
8	TsSY(RXC)	SYNC to RxC ↑ Setup Time (Note 1)	−200		−200		ns
9	ThSY(RXC)	SYNC to RxC ↑ Hold Time (Note 1)	3TcPC +200		3TcPC +200		ns
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time (Notes 2, 4)	0		0		ns
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (XI Mode) (Note 2)		300		300	ns
12	TdTXCr(TXD)	TxC ↑ to TxD Delay (XI Mode) (Notes 2, 5)		300		300	ns
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)					ns
14	TwRTXh	RTxC High Width	180		180		ns
15	TwRTXl	RTxC Low Width	180		180		ns
16	TcRTX	RTxC Cycle Time	400		400		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	250	1000	250	1000	ns
18	TwTRXh	TRxC High Width	180		180		ns
19	TwTRXl	TRxC Low Width	180		180		ns
20	TcTRX	TRxC Cycle Time	400		400		ns
21	TwEXT	DCD or CTS Pulse Width	200		200		ns
22	TwSY	SYNC Pulse Width	200		200		ns

Notes: 1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only if RTxC is used directly as Tx or Rx clock. If used as a DPLL or BR source, specifications are the same as PCLK (4MHz).

*Timings are preliminary and subject to change.

Figure 20. General Timing

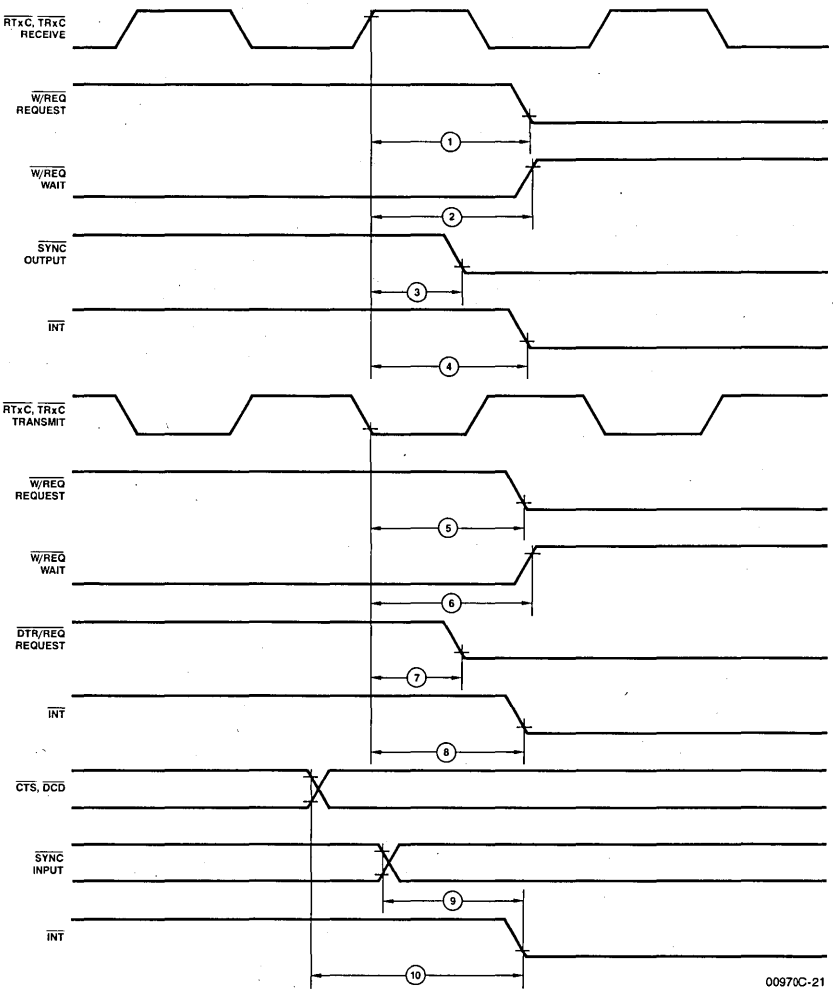


SYSTEM TIMING

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdRXC(REQ)	$\overline{RxC}$ ↑ to $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	TcPC
2	TdRXC(W)	$\overline{RxC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	12	8	12	TcPC
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	4	7	TcPC
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPC
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	TcPC
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	8	5	8	TcPC
7	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	TcPC
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPC
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPC
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPC

Notes: 1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
*Timings are preliminary and subject to change.

Figure 21. System Timing



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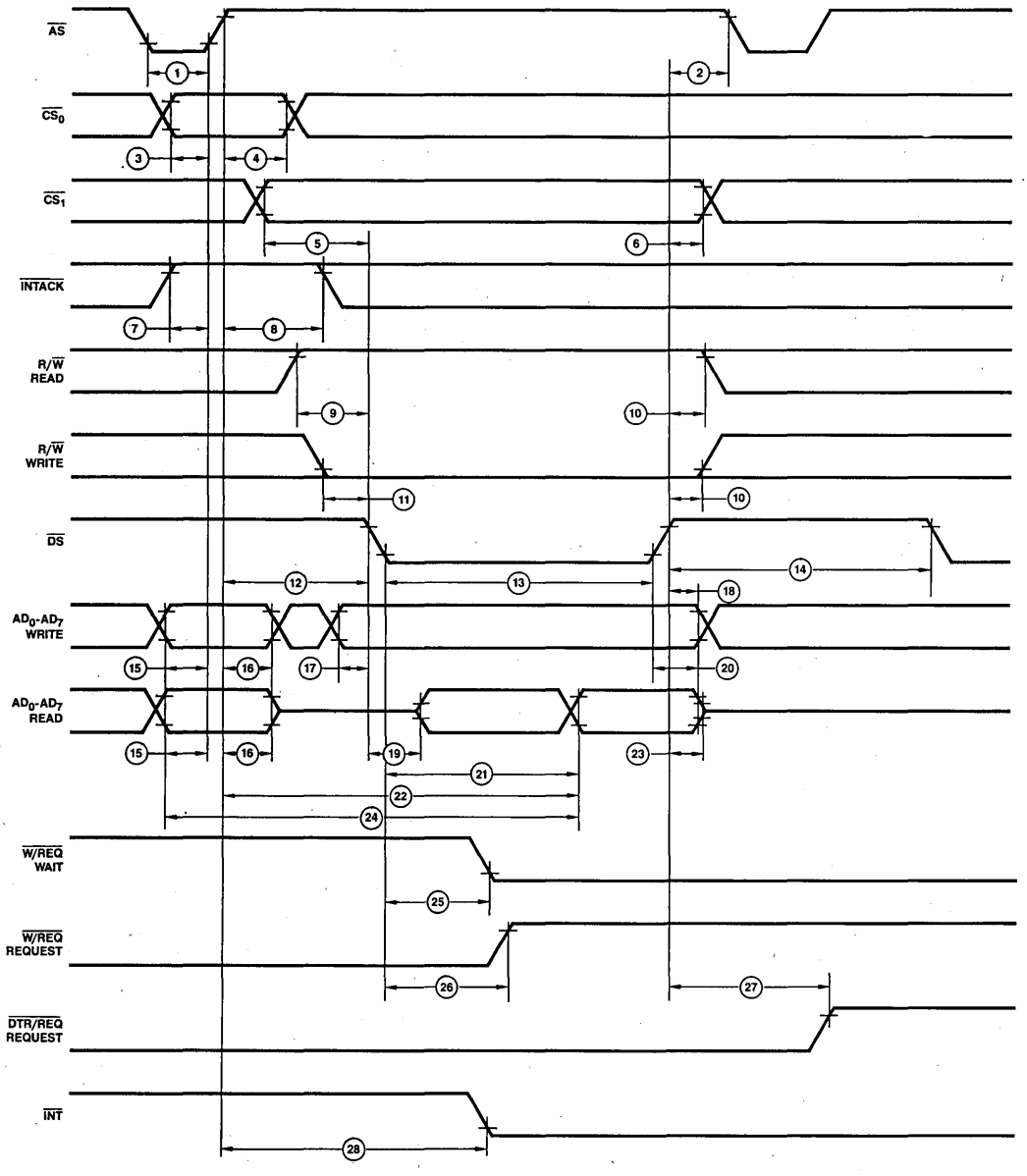
READ AND WRITE TIMING (AmZ8030)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TwAS	$\overline{AS}$ LOW Width	70		50		ns
2	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		ns
3	TsCS0(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time (Note 1)	0		0		ns
4	ThCS0(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time (Note 1)	60		40		ns
5	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time (Note 1)	100		80		ns
6	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time (Note 1)	55		40		ns
7	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns
8	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		ns
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		ns
10	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		ns
11	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0		ns
12	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60		40		ns
13	TwDSI	$\overline{DS}$ LOW Width	390		250		ns
14	TrC	Valid Access Recovery Time (Note 2)	6TcPC +200		6TcPC +130		ns
15	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time (Note 1)	30		10		ns
16	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time (Note 1)	50		30		ns
17	TsDW(DS)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		ns
18	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		ns
19	TdDS(DA)	$\overline{DS}$ ↓ to Data Active Delay	0		0		ns
20	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0		ns
21	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	ns
22	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Valid Delay		520		335	ns

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the 8030.

Figure 22. Read and Write Timing (AmZ8030)



INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (AmZ8030)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
23	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay (Note 3)		70		45	ns
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		570		420	ns
25	TdDS(W)	$\overline{DS}$ ↓ to Wait Valid Delay (Note 4)		240		200	ns
26	TdDSf(REQ)	$\overline{DS}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	ns
27	TdDSr(REQ)	$\overline{DS}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
28	TdAS(INT)	$\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay (Note 4)		500		500	ns
29	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay (Note 5)					ns
30	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		ns
31	TdDSA(DR)	$\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay		250		180	ns
32	TsIEI(DSA)	IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time	120		100		ns
33	ThIEI(DSA)	IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time	0		0		ns
34	TdIEI(IEO)	IEI to IEO Delay		120		100	ns
35	TdAS(IEO)	$\overline{AS}$ ↑ to IEO Delay (Note 6)		250		250	ns
36	TdDSA(INT)	$\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay (Note 4)		500		500	ns
37	TdDS(ASQ)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset	30		15		ns
38	TdASQ(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset	30		30		ns
39	TwRES	$\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset (Note 7)	250		250		ns
40	TwPCl	PCLK Low Width	105	2000	70	1000	ns
41	TwPCh	PCLK High Width	105	2000	70	1000	ns
42	TcPC	PCLK Cycle Time	250	4000	165	2000	ns
43	TrPC	PCLK Rise Time		20		15	ns
44	TfPC	PCLK Fall Time		20		10	ns

Notes:
3. Float delay is defined as the time required for a ±0.5V change in the output with a maximum dc load and minimum ac load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any 8030 in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI($\overline{DSA}$) for the 8030, and TdIEIf(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a 8030 pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the 8030.

All timing references assume 2.0V for a logic "1" and 0.8V for a logic.

Figure 23. Interrupt Acknowledge Timing (AmZ8030)

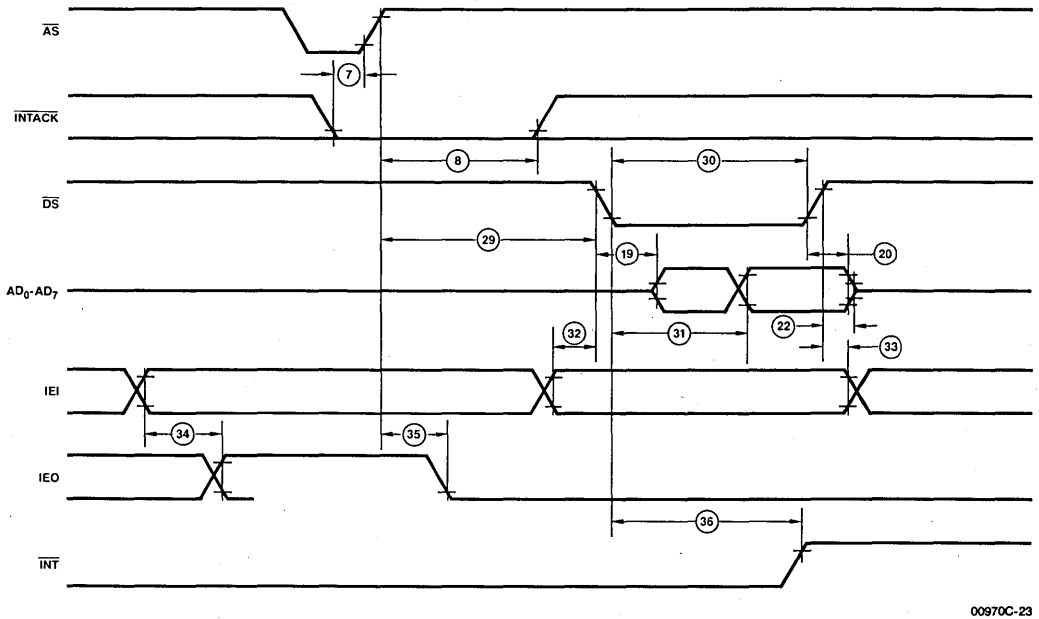


Figure 24. Reset Timing (AmZ8030)

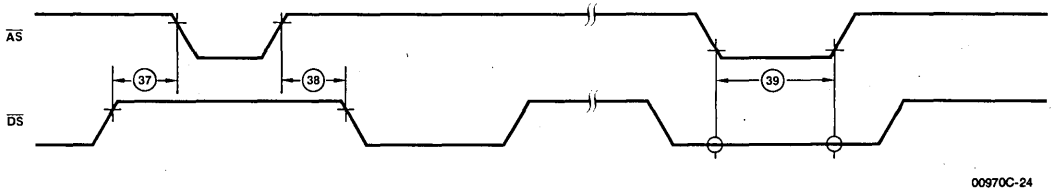
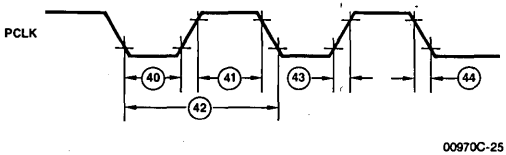


Figure 25. Cycle Timing (AmZ8030)

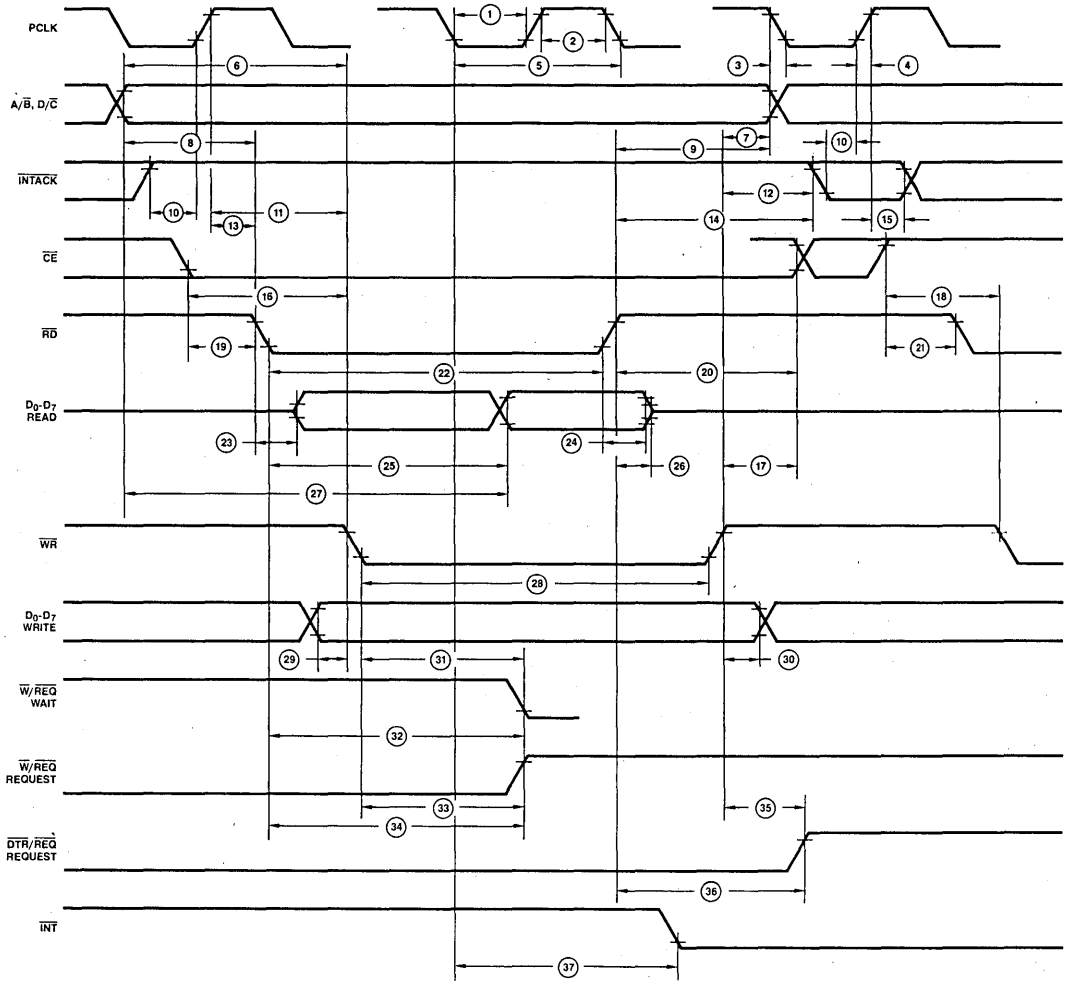


READ AND WRITE TIMING (AmZ8530)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TwPCl	PCLK Low Width	105	2000	70	1000	ns
2	TwPCh	PCLK High Width	105	2000	70	1000	ns
3	TfPC	PCLK Fall Time		20		10	ns
4	TrPC	PCLK Rise Time		20		15	ns
5	TcPC	PCLK Cycle Time	250	4000	165	2000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80		80		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80		80		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	0		0		ns
11	TsIAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time (Note 1)	200		200		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
13	TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	200		200		ns
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		ns
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	100		100		ns
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		ns
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100		70		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note 1)	0		0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	100		70		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	390		250		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250		180	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		70		45	ns

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5V change in the output with a maximum dc load and minimum ac load.

Figure 26. Read and Write Timing (AmZ8530)



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INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (AmZ8530)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420	ns
28	TwWRI	$\overline{WR}$ Low Width	390		250		ns
29	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time	0		0		ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 4)		240		200	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 4)		240		200	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	ns
35	TdWRr(REQ)	$\overline{WR}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 4)		500		500	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 5)					ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	285		250		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		190		180	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	120		100		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250		250	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 4)		500		500	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	30		15		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	30		30		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250		250		ns
49	Trc	Valid Access Recovery Time (Note 3)	6TcPC +200		6TcPC +130		ns

Notes: 3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

*Timings are preliminary and subject to change.

Figure 27. Interrupt Acknowledge Timing (AmZ8530)

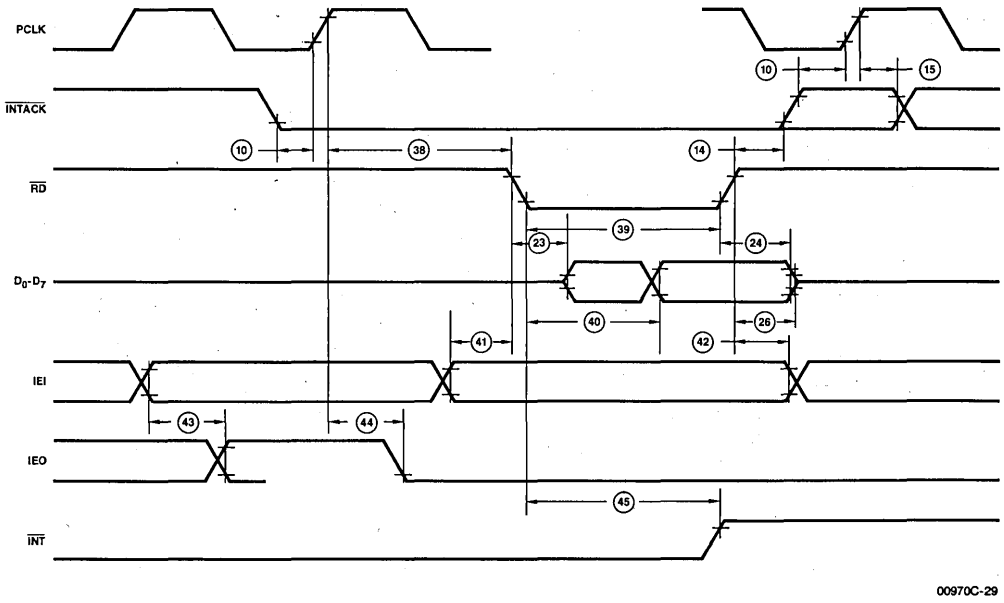


Figure 28. Reset Timing (AmZ8530)

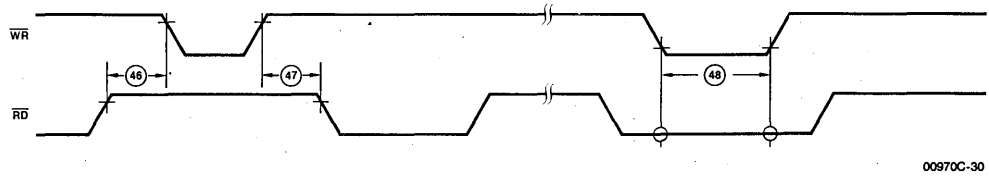
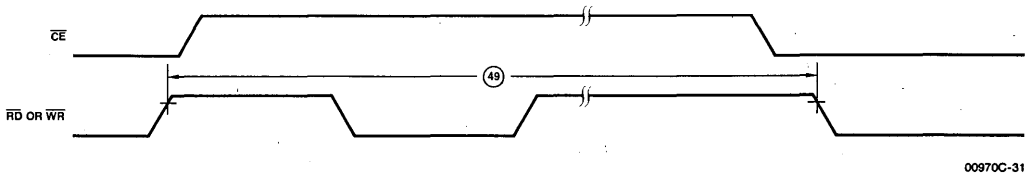


Figure 29. Cycle Timing (AmZ8530)



9

AmZ8031 • AmZ8531 (ASCC)

Asynchronous Serial Communications Controller

DISTINCTIVE CHARACTERISTICS

- **Two 1M.bps full duplex serial channels**
  Each channel has independent oscillator, generator, and PLL for clock recovery, dramatically reducing the need for external components.
- **Programmable protocols**
  NRZ, NRZI, and FM data encoding supported under program control.
- **Programmable Asynchronous Modes**
  5 to 8 bit characters with programmable stop bits clock break detect, and error conditions.
- **Z8000* compatible**
  The Z8031 interfaces directly to the Z8000 CPU bus and to the Z8000 interrupt structure.
- **Compatible with non-multiplexed bus**
  The Z8531 interfaces easily to most other CPUs.

GENERAL DESCRIPTION

Asynchronous Serial Communications Controllers are dual-channel communications peripherals designed for use with 8- and 16-bit microprocessors. They function as serial-to-parallel, and parallel-to-serial converter/controllers, and contain a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops and crystal oscillators, to dramatically reduce the need for external circuitry.

Both channels have facilities for modem control; in cases where these controls aren't needed, they can be used for general purpose I/O.

The AmZ8031 is directly compatible with the Z8000 and 8086 CPUs, while the AmZ8531 is designed for non-multiplexed buses, and is easily interfaced with most other CPUs such as 8080, Z80, 6800, 68000 and Multibus.**

BLOCK DIAGRAM

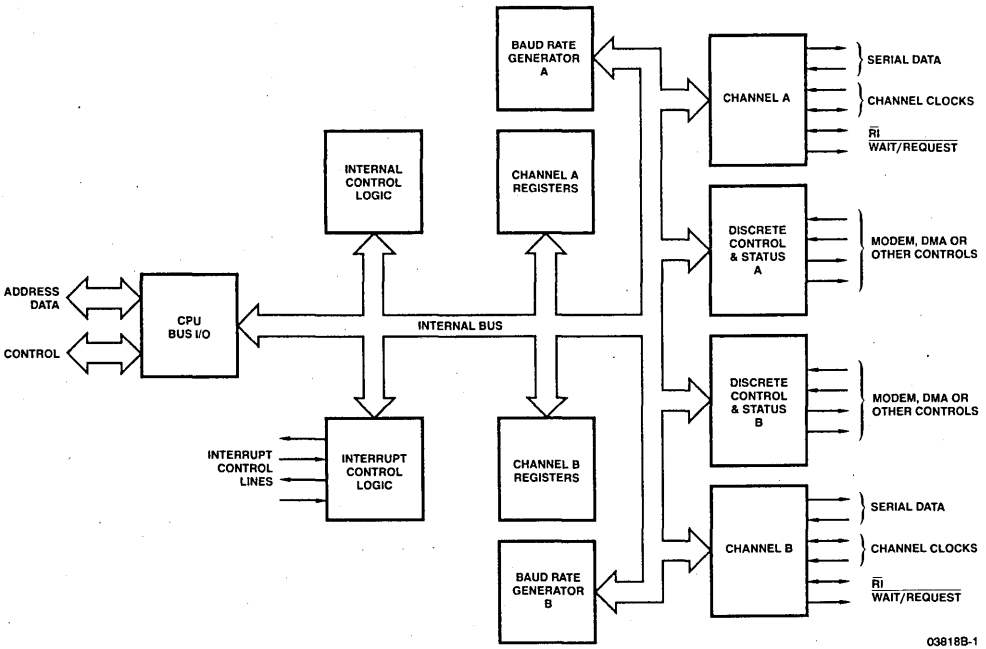
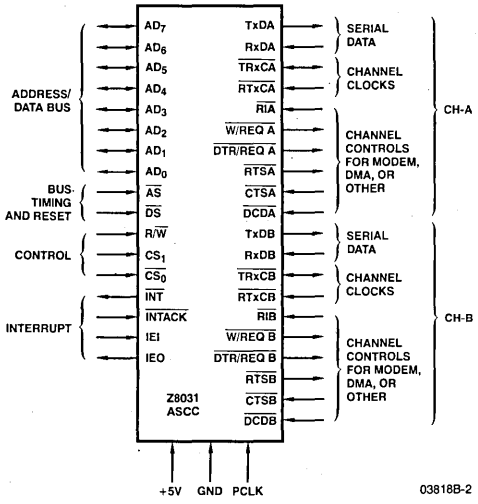


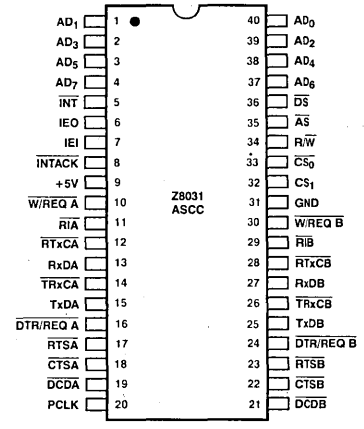
Figure 1.

*Z8000 is a trademark of Zilog. **Multibus is a trademark of Intel.

Z8031 Logic Symbol

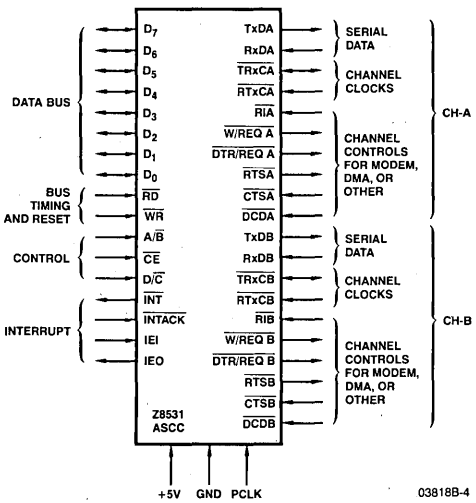


Z8031 Connection Diagram

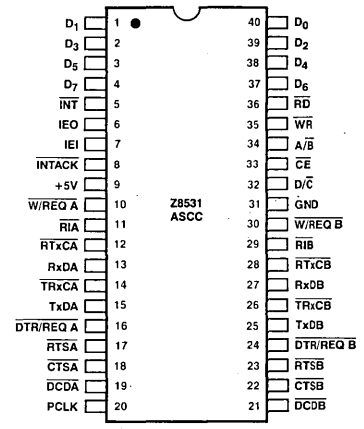


Note: Pin 1 is marked for orientation.

Z8531 Logic Symbol



Z8531 Connection Diagram



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Example Z8031 A D C B

- Basic Device
- Speed: Blank = 4MHz; A = 6MHz
- Temperature Range: C = 0 to +70°C; I = −40 to +85°C; M = −55 to +125°C
- Burn-in
- Package Type: D = Hermetic DIP; P = Molded Plastic

Example Z8531 A D C B

- Basic Device
- Speed: Blank = 4MHz; A = 6MHz
- Temperature Range: C = 0 to +70°C; I = −40 to +85°C; M = −55 to +125°C
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ARCHITECTURE

The ASCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to the Z8000 CPU (AmZ8031) or to a non-multiplexed CPU bus (AmZ8531). Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices (Figure 1).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two synchronous character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the Interrupt Pending bits (A only).

The registers for each channel are designated as follows:

WR0-WR15 – Write Registers 0 through 15.

RR0-RR3, RR10, RR12, RR13, RR15 – Read Registers 0 through 3, 10, 12, 13, 15.

The following table lists the functions assigned to each read or write register. The ASCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

DATA PATH

The transmit and receive data path illustrated in Figure 2 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and an 11-bit transmit shift register that can be loaded from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

TABLE 1. READ AND WRITE REGISTER FUNCTIONS

READ REGISTER FUNCTIONS	
RR0	Transmit/Receive buffer status and External status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only)
RR3	Interrupt Pending bits (Channel A only)
RR8	Receive buffer
RR10	Miscellaneous status
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/Status interrupt information

WRITE REGISTER FUNCTIONS	
WR0	CRC initialize, initialization commands for the various modes, shift right/shift left command
WR1	Transmit/Receive interrupt and data transfer mode definition
WR2	Interrupt vector (accessed through either channel)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync characters or SDLC address field
WR7	Sync character or SDLC flag
WR8	Transmit buffer
WR9	Master interrupt control and reset (accessed through either channel)
WR10	Miscellaneous transmitter/receiver control bits
WR11	Clock mode control
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits
WR15	External/Status interrupt control

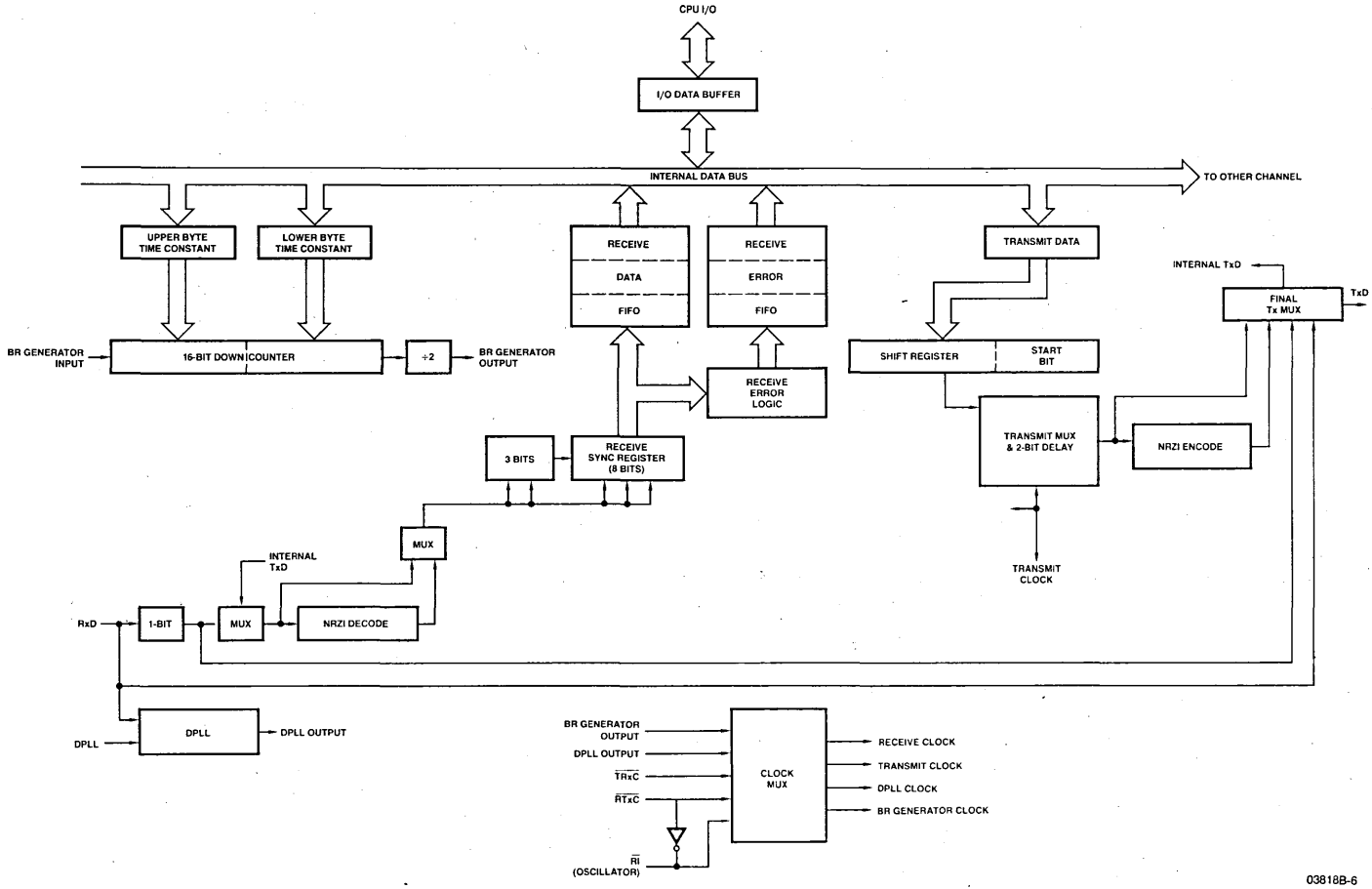


Figure 2. Data Path

FUNCTIONAL DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

DATA COMMUNICATIONS CAPABILITIES

The ASCC provides two independent full-duplex channels programmable for use in any common asynchronous data-communication protocol. Figure 3 and the following description briefly detail this protocol.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 14). If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ASCC does not require symmetric transmit and receive clock signals – a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs.

BAUD RATE GENERATOR

Each channel in the ASCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds.)

$$\text{baud rate} = \frac{1}{2\ (\text{time constant} + 2) \times (\text{BR clock period})}$$

Time-Constant Values for Standard Baud Rates at BR Clock = 3.9936MHz

Rate (Baud)	Time Constant (decimal notation)	Error
19200	102	–
9600	206	–
7200	275	0.12%
4800	414	–
3600	553	0.06%
2400	830	–
2000	996	0.04%
1800	1107	0.03%
1200	1662	–
600	3326	–
300	6654	–
150	13310	–
134.5	14844	0.0007%
110	18151	0.0015%
75	26622	–
50	39934	–

DIGITAL PHASE-LOCKED LOOP

The ASCC contains a digital phase-locked loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the ASCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The

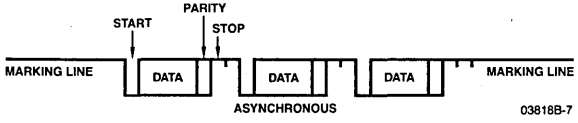


Figure 3. ASCC Protocols

DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the $\overline{RTxC}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ASCC via the $\overline{TRxC}$ pin (if this pin is not being used as an input).

DATA ENCODING

The ASCC may be programmed to encode and decode the serial data in four different ways. In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM_1 (more properly, bi-phase mark) a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM_0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the ASCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1 the bit is a 0. If the transition is 1/0 the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The ASCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes, but works in synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{CTS}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{WAIT/REQUEST}$ on transmit.

The ASCC is also capable of local loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The CTS and DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works with NRZ, NRZI or FM coding of the data stream.

I/O INTERFACE CAPABILITIES

The ASCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the ASCC are automatically updated whenever any function is performed. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When an ASCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 6 and 7).

To speed interrupt response time, the ASCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ASCC (Transmit, Receive and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set

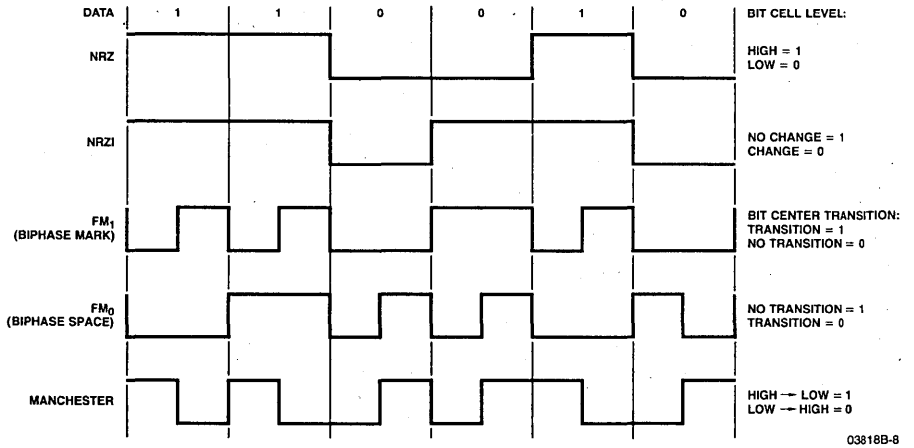


Figure 4. Data Encoding Methods

for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other two bits are related to the Z-Bus interrupt priority chain (Figure 5). As a Z-Bus peripheral, the ASCC may request an interrupt only when no higher-priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the A/D bus.

In the ASCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the INT output is pulled Low, requesting an interrupt. In the ASCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ASCC and external to the ASCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ASCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive and External/Status interrupts. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receiver, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition.
- Interrupt on all Receive Characters or Special Receive condition.
- Interrupt on Special Receive condition only.

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in asynchronous mode and, optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt-Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{RI}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break (asynchronous mode).

CPU/DMA BLOCK TRANSFER

The ASCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{WAIT}/\overline{REQUEST}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{WAIT}/\overline{REQUEST}$ output can be defined under software control as a $\overline{WAIT}$ line in the CPU Block Transfer mode or as a $\overline{REQUEST}$ line in the DMA Block Transfer mode.

To a DMA controller, the ASCC $\overline{REQUEST}$ output indicates that the ASCC is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ line indicates that the ASCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{DTR}/\overline{REQUEST}$ line allows full-duplex operation under DMA control.

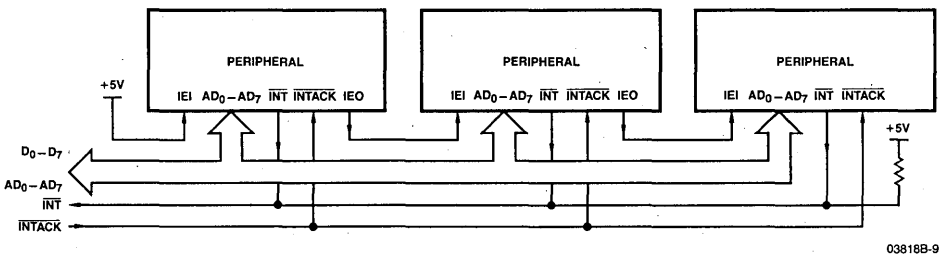


Figure 5. Z-Bus Interrupt Schedule

PROGRAMMING (AmZ8031)

The AmZ8031 contains 11 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

All of the registers in the AmZ8031 are directly addressable. How the AmZ8031 decodes the address placed on the address/data bus at the beginning of a Read or Write cycle is controlled by a command issued in WR0B. In the shift right mode, the channel select $\overline{A/B}$ is taken from AD_0 and the state of AD_5 is ignored. In the shift left mode, $\overline{A/B}$ is taken from AD_5 and the state of AD_0 is ignored. AD_7 and AD_6 are always ignored as address bits and the register address itself occupies $AD_4 - AD_1$.

The system program first issues a series of commands to initialize the basic mode of operation. For example, the character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set, and finally, receiver or transmitter enable.

PROGRAMMING (AmZ8531)

The AmZ8531, register addressing is direct for the data registers only, which are selected by a High on the D/$\overline{C}$ pin. In all other cases (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the AmZ8531, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

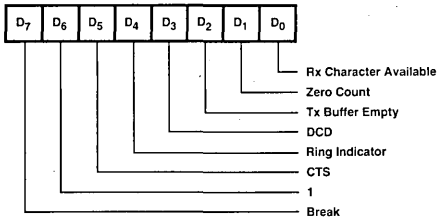
The system program first issues a series of commands to initialize the basic mode of operation. For example, the character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set, and finally, receiver or transmitter enable.

READ REGISTERS

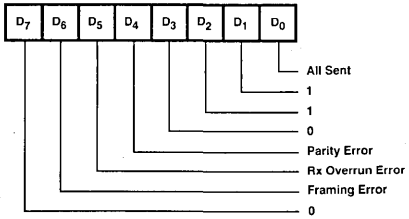
The ASCC contains 8 read registers (actually 9, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10 and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 6 shows the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

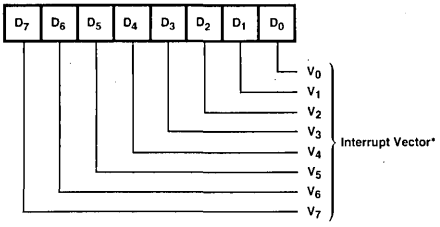
Read Register 0



Read Register 1

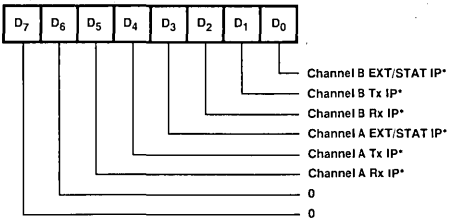


Read Register 2



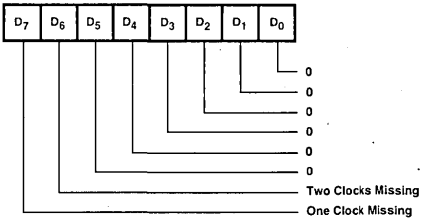
*Modified in B Channel

Read Register 3



*Always 0 in B Channel

Read Register 10



Read Register 12

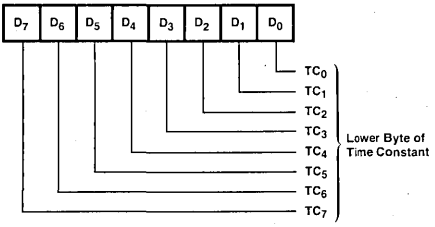
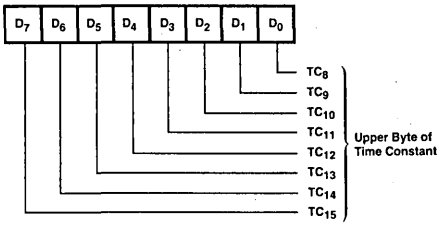


Figure 6. Read Register Bit Functions

Read Register 13



Read Register 15

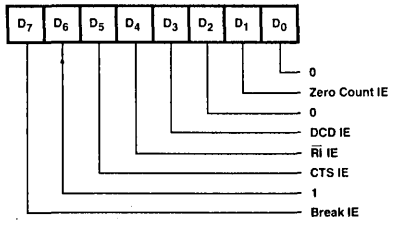
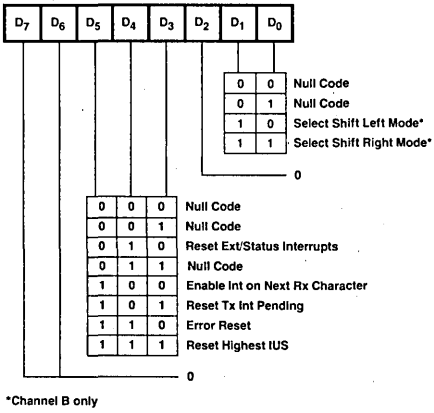


Figure 6. Read Register Bit Functions (Cont.)

WRITE REGISTERS

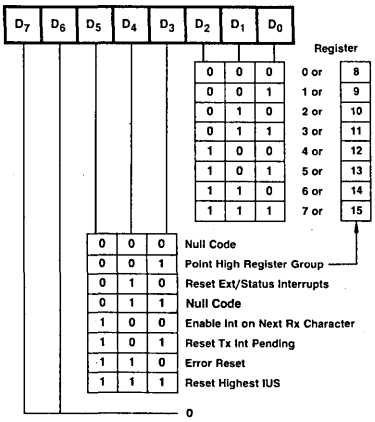
The ASCC contains 11 write registers (12 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 7 shows the format of each write register.

Write Register 0 (AmZ8031)

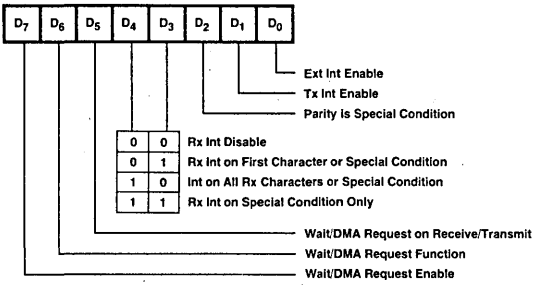


*Channel B only

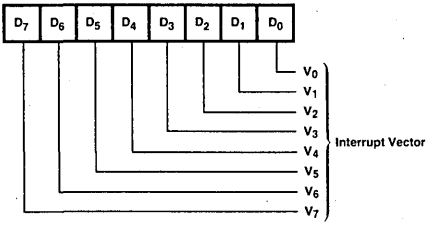
Write Register 0 (AmZ8531)



Write Register 1



Write Register 2



Write Register 3

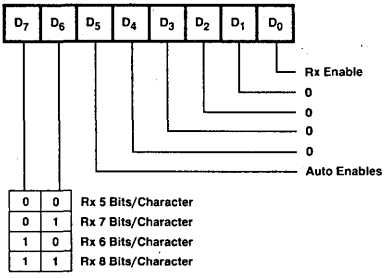
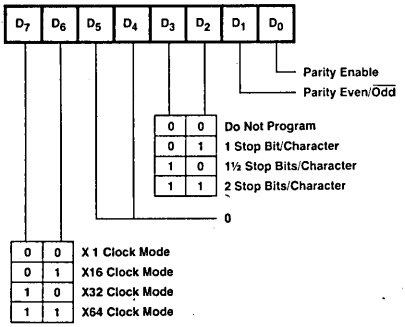
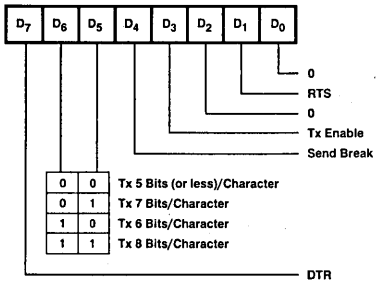


Figure 7. Write Register Bit Functions

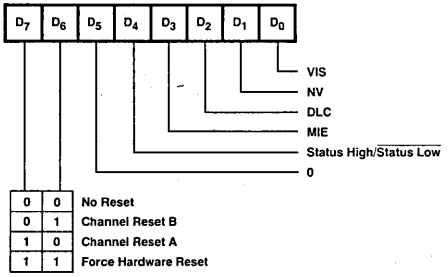
Write Register 4



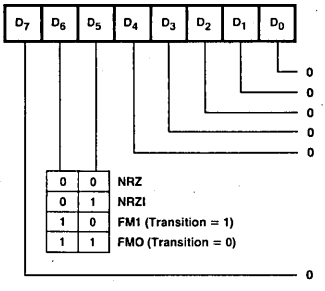
Write Register 5



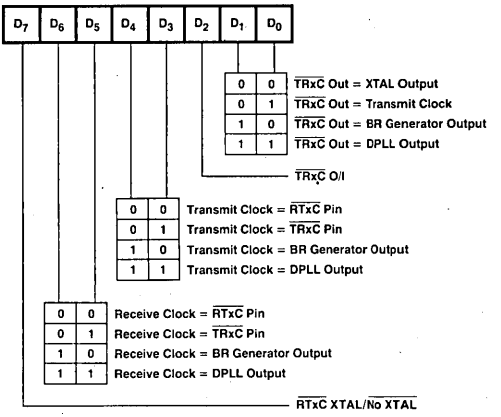
Write Register 9



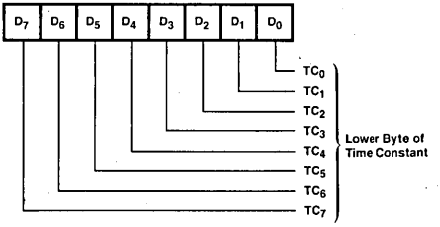
Write Register 10



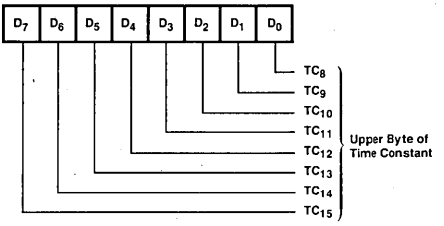
Write Register 11



Write Register 12



Write Register 13



Write Register 14

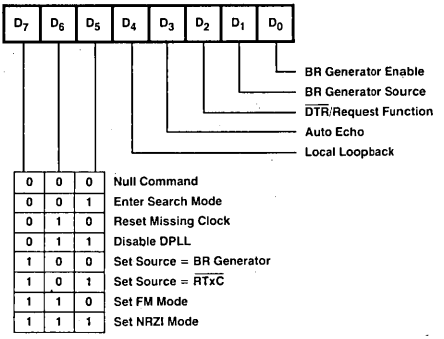


Figure 7. Write Register Bit Functions (Cont.)

Write Register 15

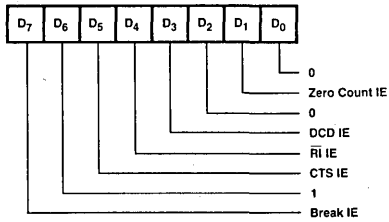


Figure 7. Write Register Bit Functions (Cont.)

AmZ8031 TIMING

The ASCC generates internal control signals from $\overline{AS}$ and $\overline{DS}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{AS}$ and $\overline{DS}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ASCC to the falling edge of $\overline{DS}$ in the second transaction involving the ASCC. This time must be at least 6 PCLK cycles plus 200ns.

READ CYCLE TIMING

Figure 8 illustrates read cycle timing. The address on AD_0-AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/W must be High to indicate a read cycle. CS_1 must also be High for the read cycle to occur. The data bus drivers in the ASCC are then enabled while $\overline{DS}$ is Low.

WRITE CYCLE TIMING

Figure 9 illustrates write cycle timing. The address on AD_0-AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be Low to indicate a write cycle. CS_1 must be High for the write cycle to occur. $\overline{DS}$ Low strobes the data into the ASCC.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 10 illustrates interrupt acknowledge cycle timing. The address on AD_0-AD_7 and the state of $\overline{CS_0}$ and $\overline{INTACK}$ are latched by the rising edge of $\overline{AS}$. However, if $\overline{INTACK}$ is Low, the addess and $\overline{CS_0}$ are ignored. The state of R/$\overline{W}$ and CS_1 are also ignored for the duration of the interrupt acknowledge cycle. Between the rising edge of $\overline{AS}$ and the falling edge of $\overline{DS}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ASCC and IEI is High when DS falls, the acknowledge cycle was intended for the ASCC. In this case, the ASCC may be programmed to respond to $\overline{DS}$ Low by placing its interrupt vector on AD_0-AD_7. It then sets the appropriate interrupt-under-service latch internally.

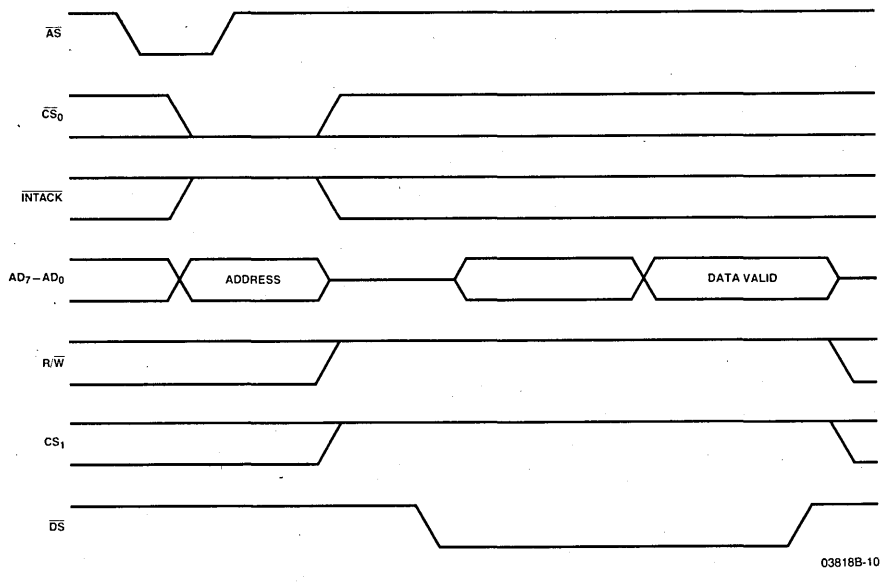


Figure 8. Z8031 Read Cycle Timing

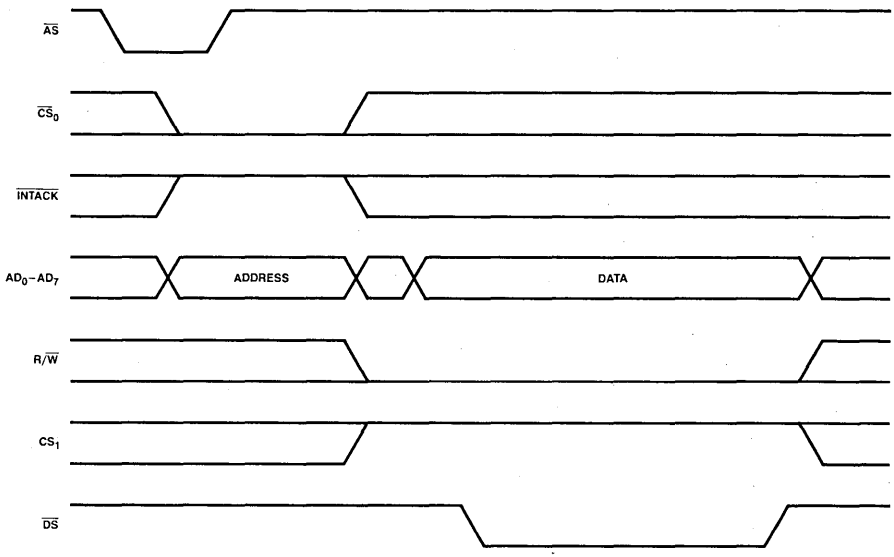


Figure 9. Z8031 Write Cycle Timing

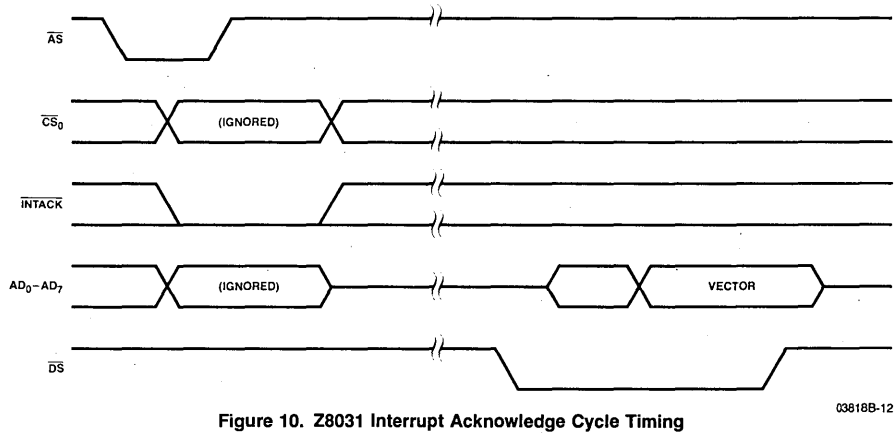


Figure 10. Z8031 Interrupt Acknowledge Cycle Timing

AmZ8531 TIMING

The ASCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ASCC. The recovery time required for proper operation is specified from the rising edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the ASCC to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the ASCC. This time must be at least 6 PCLK cycles plus 200ns.

READ CYCLE TIMING

Figure 11 illustrates read cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

WRITE CYCLE TIMING

Figure 12 illustrates write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 13 illustrates interrupt acknowledge cycle timing. Between the time $\overline{INTACK}$ goes Low and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ASCC and IEI is High when $\overline{RD}$ falls, the acknowledge cycle is intended for the ASCC. In this case, the ASCC may be programmed to respond to $\overline{RD}$ Low by placing its interrupt vector on D_0-D_7 it then sets the appropriate interrupt-under-service latch internally.

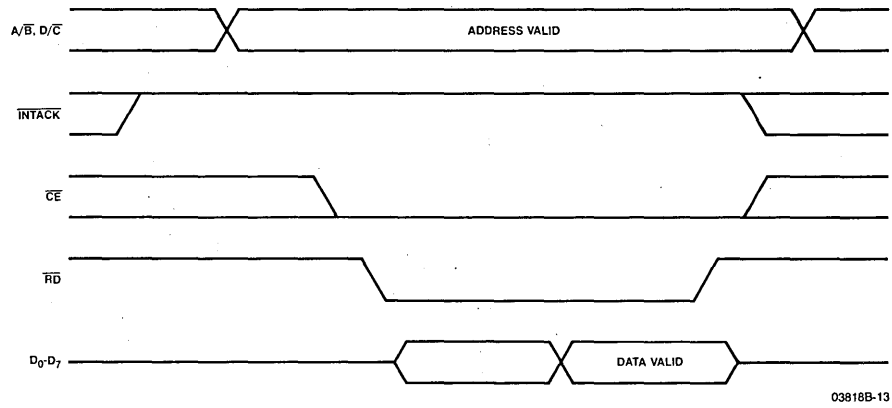


Figure 11. Z8531 Read Cycle Timing

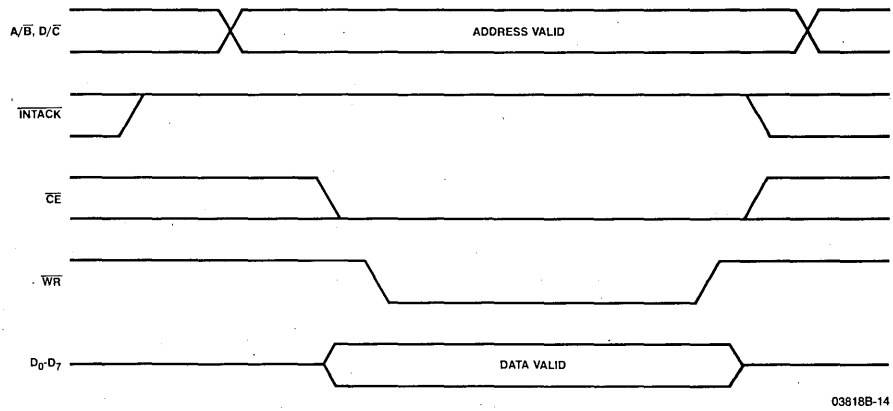


Figure 12. Z8531 Write Cycle Timing

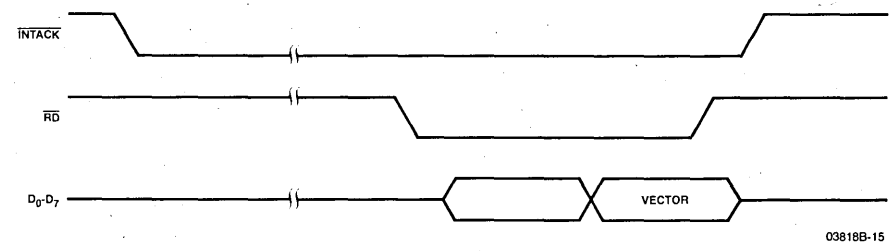


Figure 13. Z8531 Interrupt Acknowledge Cycle Timing

PIN DESCRIPTION FOR AmZ8031

The following section describes the pin functions of the ASCC. Figures 14 and 15 detail the respective pin functions and pin assignments.

V_{CC}: +5V Power Supply

GND: Ground

AD_0 – AD_7: Address/Data Bus (bidirectional, active High, three-state).
These multiplexed lines carry register addresses to the ASCC as well as data or control information to and from the ASCC.

$\overline{AS}$: Address Strobe (input, active Low).
Addresses on AD_0-AD_7 are latched by the rising edge of this signal.

$\overline{CS_0}$: Chip Select 0 (input, active Low).
This signal is latched concurrently with the addresses on AD_0-AD_7 and must be active for the intended bus transaction to occur.

CS_1: Chip Select 1 (input, active High).
This second select signal must also be active before the intended bus transaction can occur. CS_1 must remain active throughout the transaction.

$\overline{CTSA}$, $\overline{CTSB}$: Clear to Send (inputs, active Low).
If these pins are programmed as Auto Enables, a Low on these inputs enables their respective transmitter. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The ASCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

$\overline{DCDA}$, $\overline{DCDB}$: Data Carrier Detect (inputs, active Low).
These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The ASCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

$\overline{DS}$: Data Strobe (input, active Low).
This signal provides timing for the transfer of data into and out of the ASCC. If AS and DS coincide, this is interpreted as a reset.

$\overline{DTR}/\overline{REQA}$, $\overline{DTR}/\overline{REQB}$: Data Terminal Ready/Request (outputs, active Low).
These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

IEI: Interrupt Enable In (input, active High).
IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO: Interrupt Enable Out (output, active High).
IEO is High only if IEI is High and the CPU is not servicing an ASCC interrupt or the ASCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$: Interrupt Request (output, open-drain, active Low).
This signal is activated when the ASCC requests an interrupt.

$\overline{INTACK}$: Interrupt Acknowledge (input, active Low).
This signal indicates an active interrupt acknowledge cycle. During this cycle, the ASCC interrupt daisy chain settles. When $\overline{DS}$ becomes active, the ASCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of $\overline{AS}$.

PCLK: Clock (input).
This is the master ASCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be at least 90% of the CPU clock frequency for a Z8000. PCLK is a TTL level signal.

RxDA, RxDB: Receive Data (inputs, active High).
These input signals receive serial data at standard TTL levels.

$\overline{RTxCA}$, $\overline{TRxCB}$: Receive/Transmit Clocks (inputs, active Low).
These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective $\overline{RI}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

$\overline{RTSA}$, $\overline{RTSB}$: Request to Send (outputs, active Low).
When the Request to Send (RTS) bit in Write Register 5 (Figure 7) is set, the RTS signal goes Low. When the $\overline{RTS}$ bit is reset and Auto Enable is on, the signal goes High after the transmitter is empty. With Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

R/W: Read/Write (input).
This signal specifies whether the operation to be performed is read or a write.

$\overline{RIA}$, $\overline{RIB}$: Ring Indicator (inputs, active Low).
These pins can act either as inputs or as part of the crystal oscillator circuit.

In normal operation (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Ring Indicator status bits in Read Register 0 (Figure 6) but have no other function.

TxDA, TxDB: Transmit Data (outputs, active High).
These output signals transmit serial data at standard TTL levels.

$\overline{TRxCA}$, $\overline{TRxCB}$: Transmit/Receive Clocks (inputs or outputs, active Low).
These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{W}/\overline{REQA}$, $\overline{W}/\overline{REQB}$: Wait/Request (outputs, open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function).
These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the ASCC data rate. The reset state is Wait.

PIN DESCRIPTION FOR AmZ8531

The following section describes the pin functions of the ASCC. Figures 16 and 17 detail the respective pin functions and pin assignments.

V_{CC}: +5V Power Supply.

GND: Ground.

A/$\overline{B}$: Channel A/Channel B Select (input).
This signal selects the channel in which the read or write operation occurs.

$\overline{CE}$: Chip Enable (input, active Low).
This signal selects the ASCC for a read or write operation.

$\overline{CTSA}$, $\overline{CTSB}$: Clear To Send (inputs, active Low).
If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The ASCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

D/$\overline{C}$: Data/Control Select (input).
This signal defines the type of information transferred to or from the ASCC. A High means data is transferred; a Low indicates a command.

$\overline{DCDA}$, $\overline{DCDB}$: Data Carrier Detect (inputs, active Low).
These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accomodate slow rise time signals. The ASCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

D_0-D_7: Data Bus (bidirectional, three-state).
These lines carry data and commands to and from the ASCC.

$\overline{DTR}/\overline{REQA}$, $\overline{DTR}/\overline{REQB}$: Data Terminal Ready/Request (outputs, active Low).
These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.

IEI: Interrupt Enable In (input, active High).
IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO: Interrupt Enable Out (output, active High).
IEO is High only if IEI is High and the CPU is not servicing an ASCC interrupt or the ASCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$: Interrupt Request (output, open-drain, active Low).
This signal is activated when the ASCC requests an interrupt.

$\overline{INTACK}$: Interrupt Acknowledge (input, active Low).
This signal indicates an active interrupt acknowledge cycle. During this cycle, the ASCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the ASCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of PCLK.

PCLK: Clock (input).
This is the master ASCC clock used to synchronize internal signals. PCLK is a TTL level signal.

$\overline{RD}$: Read (input, active Low).
This signal indicates a read operation and when the ASCC is selected, enables the ASCC's bus drivers. During the interrupt acknowledge cycle, this signal gates the interrupt vector onto the bus if the ASCC is the highest priority device requesting an interrupt.

RxDA, RxDB: Receive Data (inputs, active High).
These input signals receive serial data at standard TTL levels.

$\overline{RTxCA}$, $\overline{RTxCB}$: Receive/Transmit Clocks (inputs, active Low).
These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase-locked loop. These pins can also be programmed for use with the respective $\overline{RI}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

$\overline{RTSA}$, $\overline{RTSB}$: Request To Send (outputs, active Low).
When the Request To Send (RTS) bit in Write Register 5 (Figure 7) is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. With Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

TxDA, TxDB: Transmit Data (outputs, active High).
These output signals transmit serial data at standard TTL levels.

$\overline{TRxCA}$, $\overline{TRxCB}$: Transmit/Receive Clocks (inputs or outputs, active Low).
These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{WR}$: Write (input, active Low).
When the ASCC is selected, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.

$\overline{W}/\overline{REQA}$, $\overline{W}/\overline{REQB}$: Wait/Request (outputs, open-drain when programmed for a Wait function, driven High or Low when progammed for a Request function).
These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the ASCC data rate. The reset state is Wait.

ABSOLUTE MAXIMUM RATINGS above which useful life may be impared

Storage Temperature	−65 to +150°C
Voltage at any Pin Relative to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.8W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

(over which the DC, switching and functional specifications apply)

	4MHz	6MHz
Commercial Operating Range T_A = 0 to 70°C V_{CC} = 5V ±5%	Z8031DC Z8031PC Z8531DC Z8531PC	Z8031ADC Z8031APC Z8531ADC Z8531APC
Industrial Operating Range T_A = −40 to +85°C V_{CC} = 5V ±5%	Z8031DI Z8531DI	
Military Operating Range T_A = −55 to +125°C V_{CC} = 5V ±10%	Z8031DMB Z8531DMB	

Notes: T_A denotes ambient temperature.
Add suffix B to indicate burn-in requirement.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −250μA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = +2.0mA			0.4	V
I_{IL}	Input Leakage	0.4 ≤ V_{IN} ≤ +2.4V			±10.0	μA
I_{OL}	Output Leakage	0.4 ≤ V_{OUT} ≤ +2.4V			±10.0	μA
I_{CC}	V_{CC} Supply Current				250	mA
C_{IN}	Input Capacitance	Unmeasured pins returned to ground. f = 1MHz over specified temperature range.			10	pF
C_{OUT}	Output Capacitance				15	pF
$C_{I/O}$	Bidirectional Capacitance				20	pF

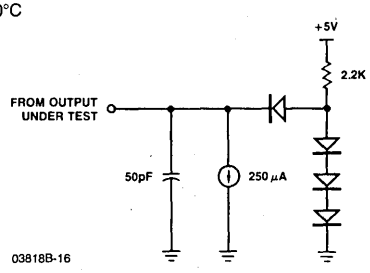
V_{CC} = 5V ± 5% unless otherwise specified, over specified temperature range.

Standard Test Conditions

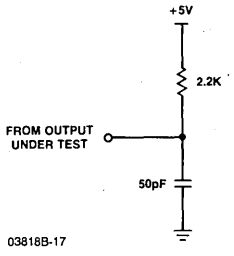
The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75V ≤ V_{CC} ≤ +5.25V
GND = 0V
0°C ≤ T_A ≤ +70°C

Standard Test Load



Open Drain Test Load



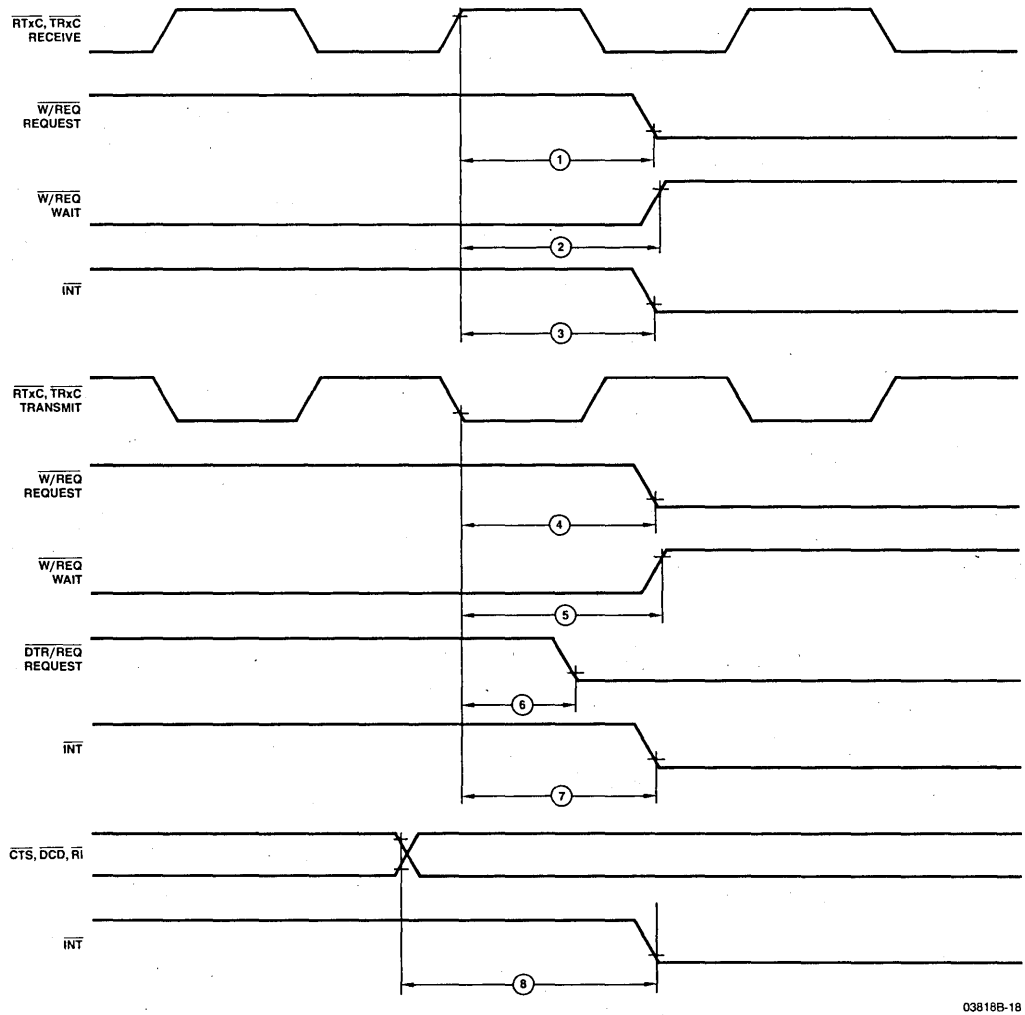
9

SYSTEM TIMING

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdRXC(REQ)	$\overline{RxC}\uparrow$ to $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	TcPC
2	TdRXC(W)	$\overline{RxC}\uparrow$ to Wait Inactive Delay (Notes 1, 2)	8	12	8	12	TcPC
3	TdRXC(INT)	$\overline{RxC}\uparrow$ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPC
4	TdTXC(REQ)	$\overline{TxC}\downarrow$ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	TcPC
5	TdTXC(W)	$\overline{TxC}\downarrow$ to Wait Inactive Delay (Notes 1, 3)	5	8	5	8	TcPC
6	TdTXC(DRQ)	$\overline{TxC}\downarrow$ $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	TcPC
7	TdTXC(INT)	$\overline{TxC}\downarrow$ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPC
8	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPC

Notes: 1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
*Timings are preliminary and subject to change.

Figure 14. System Timing

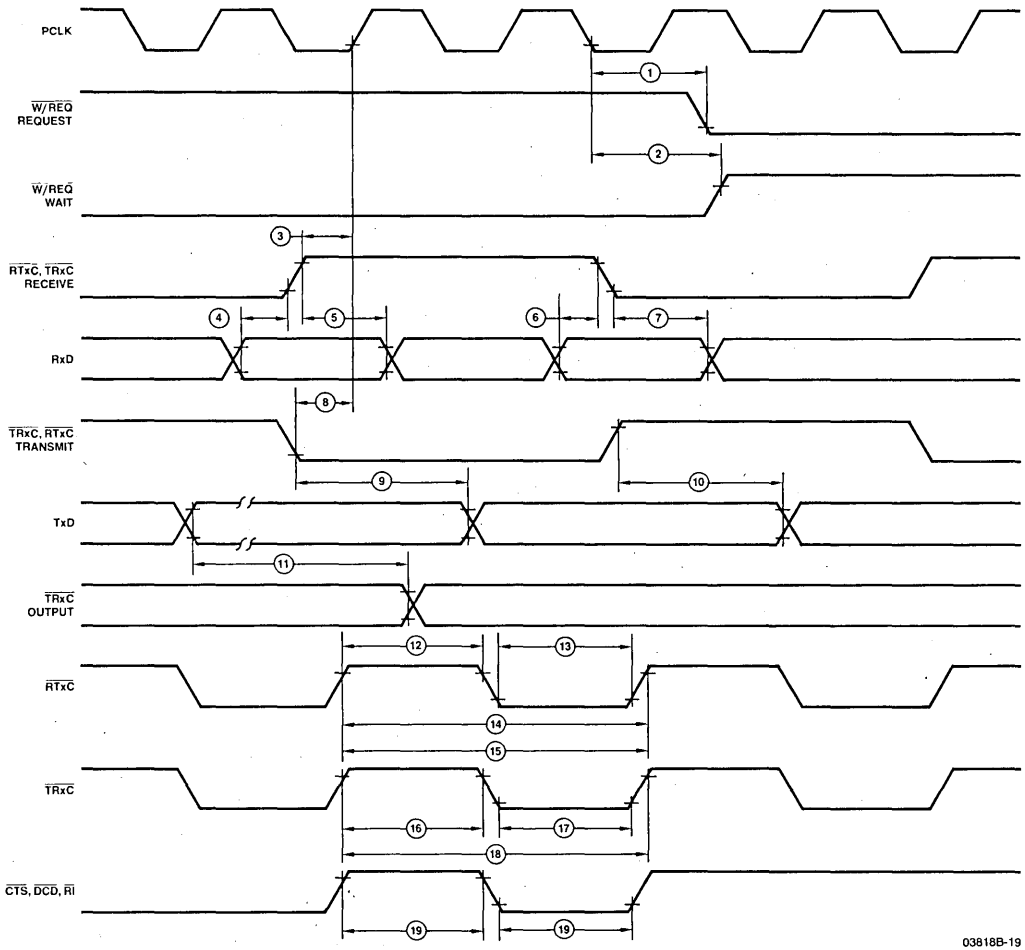


GENERAL TIMING (See Figure 15)

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TdPC(REQ)	PCLK ↓ to W/$\overline{REQ}$ Valid Delay		250		250	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		350	ns
3	TsRXC(PC)	$\overline{RxC}$ ↑ to PCLK ↑ Setup Time (Notes 1, 4)	50		50		ns
4	TsRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Setup Time (X1 Mode) (Note 1)	0		0		ns
5	ThRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Hold Time (X1 Mode) (Note 1)	150		150		ns
6	TsRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Setup Time (X1 Mode) (Notes 1, 5)	0		0		ns
7	ThRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Hold Time (X1 Mode) (Notes 1, 5)	150		150		ns
8	TsTXC(PC)	$\overline{TxC}$ ↓ to PCLK ↑ Setup Time (Notes 2, 4)	0		0		ns
9	TdTXCf(TXD)	$\overline{TxC}$ ↓ to TxD Delay (X1 Mode) (Note 2)		300		300	ns
10	TdTXCr(TXD)	$\overline{TxC}$ ↑ to TxD Delay (X1 Mode) (Notes 2, 5)		300		300	ns
11	TdTXD(TRX)	TxD to $\overline{TRxC}$ Delay (Send Clock Echo)					ns
12	TwRTXh	$\overline{RTxC}$ High Width	180		180		ns
13	TwRTXl	$\overline{RTxC}$ Low Width	180		180		ns
14	TcRTX	$\overline{RTxC}$ Cycle Time	400		400		ns
15	TcRTXX	Crystal Oscillator Period (Note 3)	250	1000	250	1000	ns
16	TwTRXh	$\overline{TRxC}$ High Width	180		180		ns
17	TwTRXl	$\overline{TRxC}$ Low Width	180		180		ns
18	TcTRX	$\overline{TRxC}$ Cycle Time	400		400		ns
19	TwEXT	$\overline{DCD}$ or $\overline{CTS}$ Pulse Width	200		200		ns

Notes: 1. RxC is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. TxC is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
3. Both $\overline{RTxC}$ and $\overline{RI}$ have 30pF capacitors to the ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and $\overline{PCLK}$ or $\overline{TxC}$ and $\overline{PCLK}$ is required.
5. Parameter applies only to FM encoding/decoding.

Figure 15. General Timing

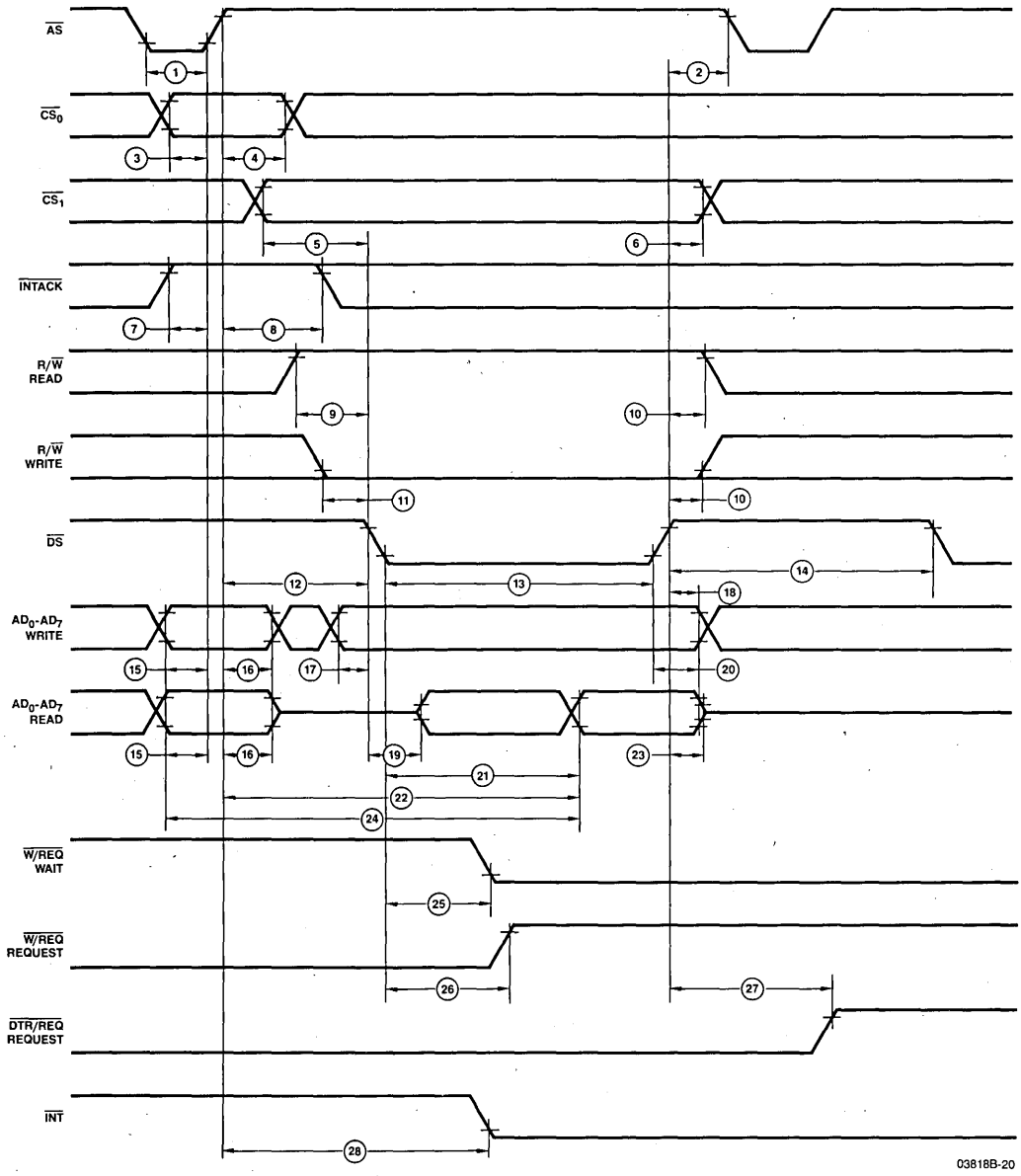


READ AND WRITE TIMING (See Figure 16)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TwAS	$\overline{AS}$ LOW Width	70		50		ns
2	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		ns
3	TsCS0(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time (Note 1)	0		0		ns
4	ThCS0(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time (Note 1)	60		40		ns
5	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time (Note 1)	100		80		ns
6	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time (Note 1)	55		40		ns
7	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns
8	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		ns
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		ns
10	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		ns
11	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0		ns
12	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60		40		ns
13	TwDSI	$\overline{DS}$ LOW Width	390		250		ns
14	TrC	Valid Access Recovery Time (Note 2)	6TcPC +200		6TcPC +130		ns
15	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time (Note 1)	30		10		ns
16	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time (Note 1)	50		30		ns
17	TsDW(DS)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		ns
18	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		ns
19	TdDS(DA)	$\overline{DS}$ ↓ to Data Active Delay	0		0		ns
20	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0		ns
21	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	ns
22	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Valid Delay		520		335	ns

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the 8030.

Figure 16. Z8031 Read and Write Timing



INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (see Figures 17, 18, 19)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
23	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay (Note 3)		70		45	ns
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		570		420	ns
25	TdDS(W)	$\overline{DS}$ ↓ to Wait Valid Delay (Note 4)		240		200	ns
26	TdDSf(REQ)	$\overline{DS}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	ns
27	TdDSr(REQ)	$\overline{DS}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
28	TdAS(INT)	$\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay (Note 4)		500		500	ns
29	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay (Note 5)					ns
30	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		ns
31	TdDSA(DR)	$\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay		250		180	ns
32	TsIEI(DSA)	IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time	120		100		ns
33	ThIEI(DSA)	IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time	0		0		ns
34	TdIEI(IEO)	IEI to IEO Delay		120		100	ns
35	TdAS(IEO)	$\overline{AS}$ ↑ to IEO Delay (Note 6)		250		250	ns
36	TdDSA(INT)	$\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay (Note 4)		500		500	ns
37	TdDS(ASQ)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset	30		15		ns
38	TdASQ(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset	30		30		ns
39	TwRES	$\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset (Note 7)	250		250		ns
40	TwPCl	PCLK Low Width	105	2000	70	1000	ns
41	TwPCh	PCLK High Width	105	2000	70	1000	ns
42	TcPC	PCLK Cycle Time	250	4000	165	2000	ns
43	TrPC	PCLK Rise Time		20		15	ns
44	TfPC	PCLK Fall Time		20		10	ns

Notes:
3. Float delay is defined as the time required for a ±0.5V change in the output with a maximum dc load and minimum ac load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any 8031 in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI(DSA) for the 8031, and TdIEIf(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a 8031 pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the 8031.

*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic.

Figure 17. Z8031 Interrupt Acknowledge Timing

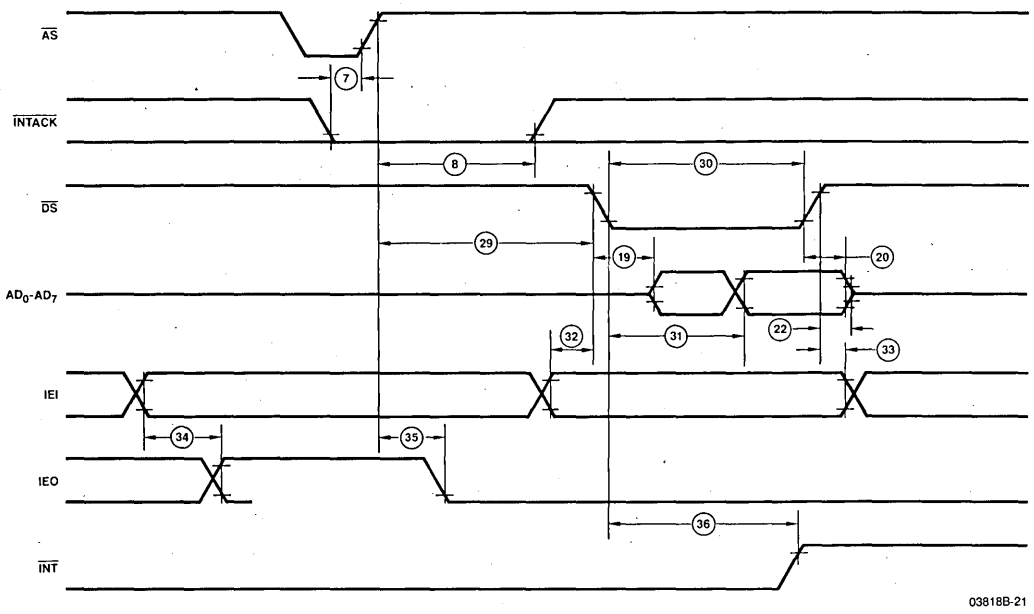


Figure 18. Z8031 Reset Timing

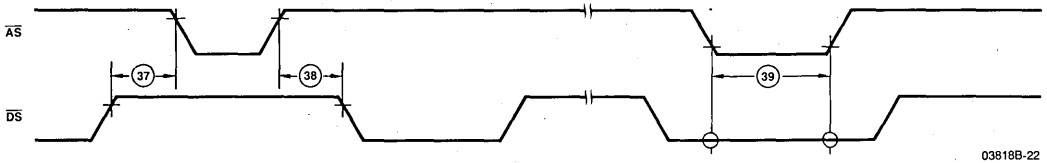
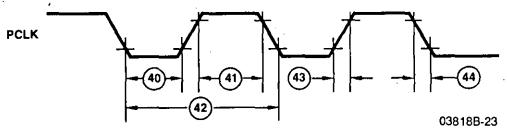


Figure 19. Z8031 Cycle Timing

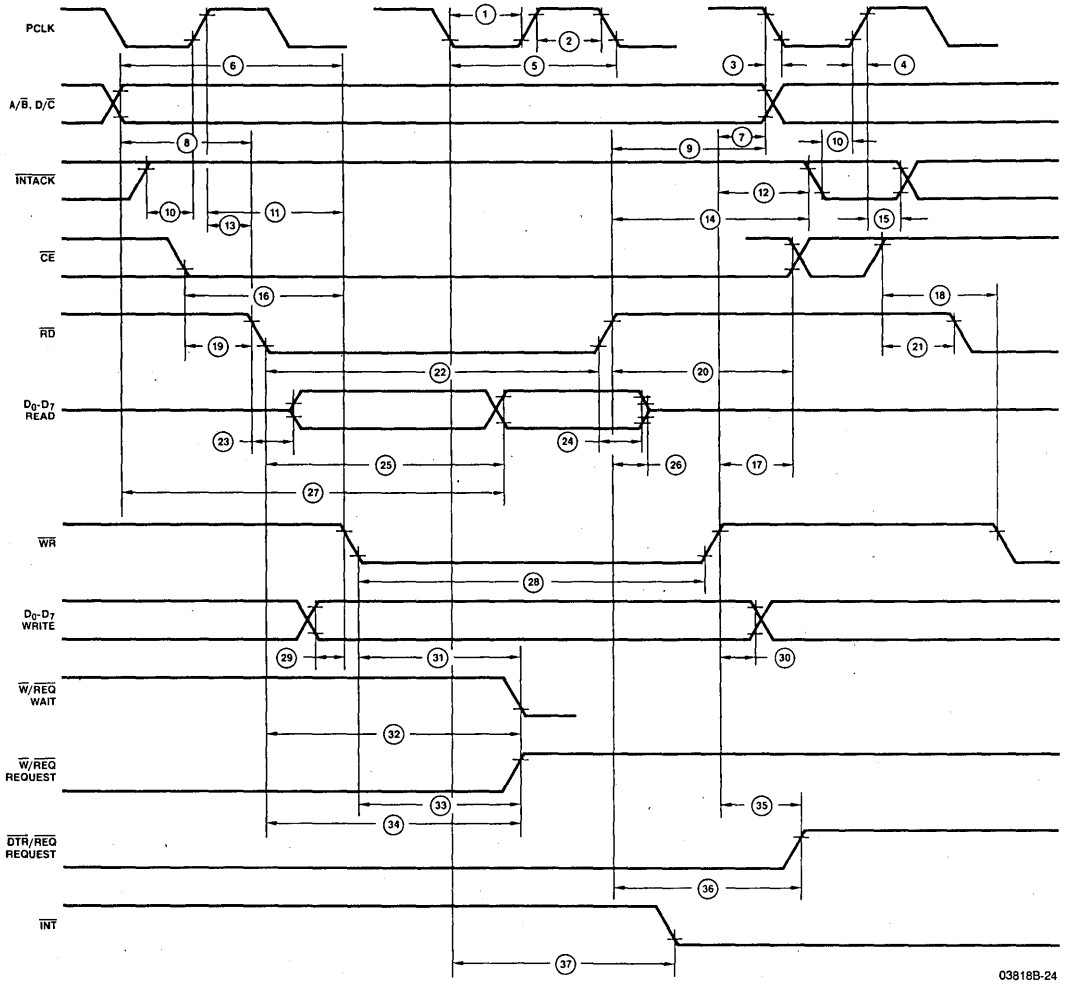


READ AND WRITE TIMING (see Figure 20)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TwPCl	PCLK Low Width	105	2000	70	1000	ns
2	TwPCh	PCLK High Width	105	2000	70	1000	ns
3	TfPC	PCLK Fall Time		20		10	ns
4	TrPC	PCLK Rise Time		20		15	ns
5	TcPC	PCLK Cycle Time	250	4000	165	2000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80		80		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80		80		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	0		0		ns
11	TsIAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time (Note 1)	200		200		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
13	TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	200		200		ns
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		ns
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	100		100		ns
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		ns
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100		70		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note 1)	0		0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	100		70		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	390		250		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250		180	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		70		45	ns

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5V change in the output with a maximum dc load and minimum ac load.

Figure 20. Z8531 Read and Write Timing



03818B-24

INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING (see Figures 21, 22, 23)

Number	Parameter	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420	ns
28	TwWRI	$\overline{WR}$ Low Width	390		250		ns
29	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time	0		0		ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 4)		240		200	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 4)		240		200	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	ns
35	TdWRr(REQ)	$\overline{WR}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 4)		500		500	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 5)					ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	285		250		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		190		180	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	120		100		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250		250	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 4)		500		500	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	30		15		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	30		30		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250		250		ns
49	Trc	Valid Access Recovery Time (Note 3)	6TcPC +200		6TcPC +130		ns

Notes: 3. Parameter applies only between transactions involving the ASCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

Figure 21. Z8531 Interrupt Acknowledge Timing

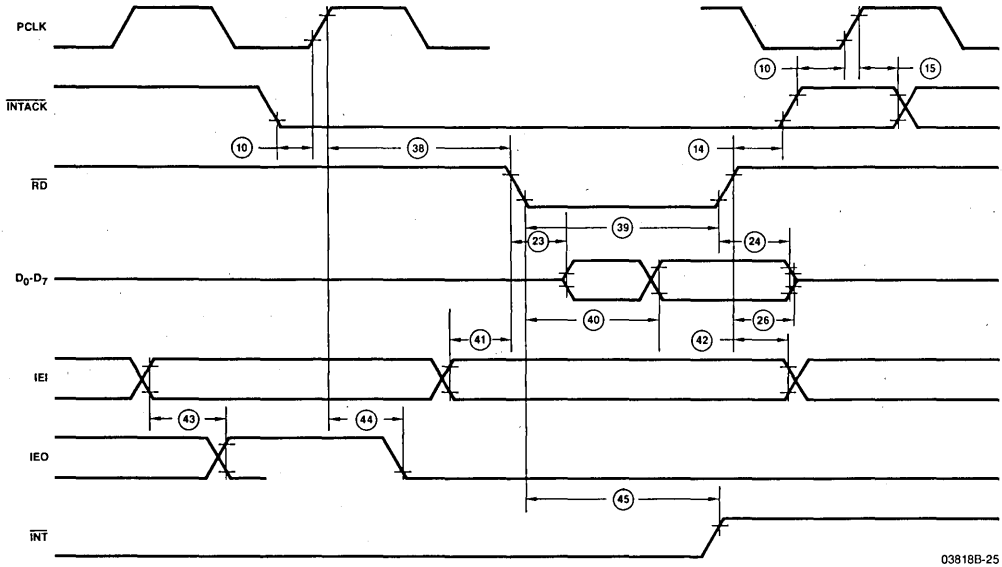


Figure 22. Z8531 Reset Timing

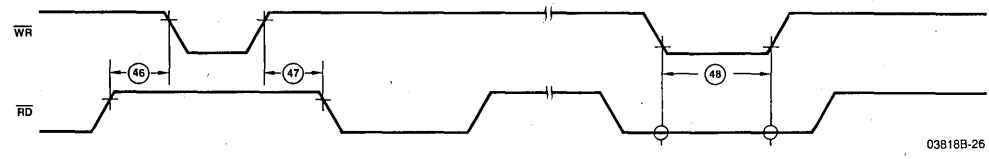
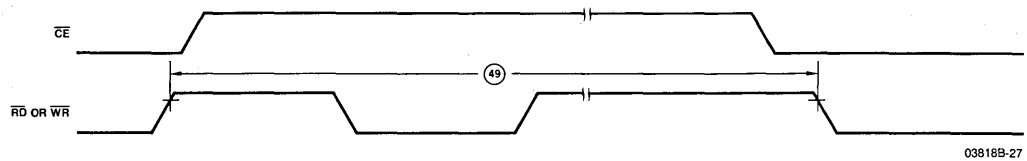


Figure 23. Z8531 Cycle Timing



8051/8031

Single-Chip 8-Bit Microcomputer

8031 – Control oriented CPU with RAM and IO

8051 – An 8031 with factory mask-programmable ROM

DISTINCTIVE CHARACTERISTICS

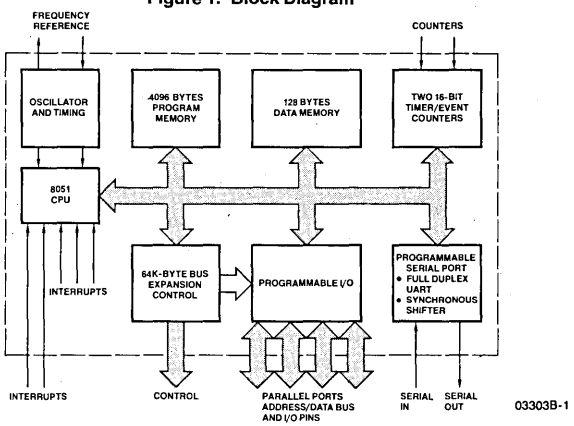
- 4K x 8 ROM
- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128K
- Compatible with 8080 and 8085 peripherals
- Boolean processor
- 8048 architecture enchanced with:
  - Non-paged jumps
  - Direct addressing
  - Four 8-register banks
  - Stack depth up to 128-bytes
  - Multiply, divide, subtract, compare
- Most instructions execute in 1μs
- 4μs multiply and divide

GENERAL DESCRIPTION

The 8051/8031 are members of a family of advanced single-chip microcomputers. The 8051 contains 4K x 8 read-only program memory; 128 x 8 RAM; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the 8051 can be expanded using standard TTL compatible memories and the byte oriented 8080 and 8085 peripherals.

The 8051 microcomputer, like its 8048 predecessor, is efficient both as a controller and as a boolean processor. The 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12MHz crystal, 58% of the instructions execute in 1μs, 40% in 2μs and multiply and divide require only 4μs. Among the many instructions added to the standard 8048 instruction set are multiply, divide, subtract, and compare.

Figure 1. Block Diagram



ORDERING INFORMATION

Operating Range	Package	12MHz w/ROM	12MHz w/o ROM
Commercial $0°C \leq T_A \leq 70°C$ $V_{CC} = +5V \pm 5\%$ $V_{SS} = 0V$	Hermetic DIP	D8051-XXXXX	D8031
	Molded DIP	P8051-XXXXX	P8031
Industrial $-40°C \leq T_A \leq 85°C$ $V_{CC} = +5V \pm 10\%$ $V_{SS} = 0V$	Hermetic DIP	ID8051-XXXXX	ID8031
Military $-55°C \leq T_A \leq 125°C$ $V_{CC} = +5V \pm 10\%$ $V_{SS} = 0V$	Hermetic DIP	MD8051B-XXXXX	MD8031B

*XXXXX is a five digit ROM code identifier assigned by factory.

9

03303B-MMP

LOGIC SYMBOL

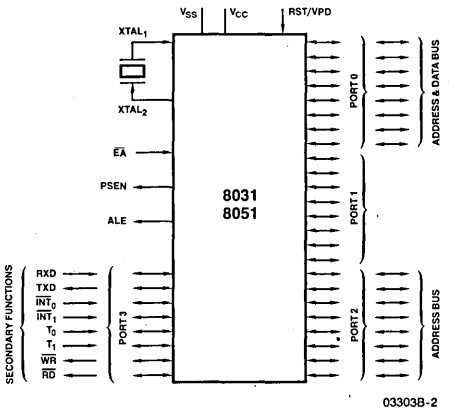


Figure 2.

CONNECTION DIAGRAM
Top View
D-40
P-40

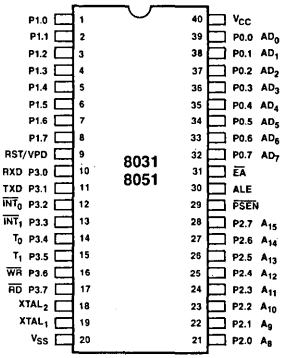


Figure 3.

8051 FAMILY PIN DESCRIPTION

V_{SS}

Circuit ground potential.

V_{CC}

+5V power supply during operation.

PORT 0

Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.

PORT 1

Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.

PORT 2

Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

PORT 3

Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port, and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows:

- RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous).
- TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous).
- $\overline{INT_0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.
- $\overline{INT_1}$ (P3.3). Interrupt 1 input or gate control input for counter 1
- T_0 (P3.4). Input to counter 0.
- T_1 (P3.5). Input to counter 1.
- $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.
- $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST/V_{PD}

A high level on this pin resets the 8051. If V_{PD} is held within its spec (approximately +5V), while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}. A small internal resistor permits power-on reset using only a capacitor connected to V_{CC}.

ALE

Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.

$\overline{PSEN}$

The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

$\overline{EA}$

When held at a TTL high level, the 8051 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the 8051 fetches all instructions from external Program Memory.

$XTAL_1$

Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on $XTAL_2$.

$XTAL_2$

Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

THE 8051 FAMILY

The 8051 is a stand-alone high-performance single-chip computer intended for use in sophisticated real-time applications such as instrumentation, industrial control, and intelligent computer peripherals. It provides the hardware features, architectural enhancements, and new instructions that make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage. A Block Diagram is shown in Figure 1.

The 8031 is a control-oriented CPU without on-chip program memory. It can address 64K-bytes of External Program Memory in addition to 64K-bytes of External Data Memory. For systems requiring extra capability, each member of the 8051 Family can be expanded using standard memories and the byte oriented 8080 and 8085 peripherals. The 8051 is an 8031 with the lower 4K-bytes of Program Memory filled with on-chip mask programmable ROM.

The two pin-compatible versions of this component reduce development problems to a minimum and provide maximum flexibility. The 8051 is suited for low-cost, high volume production; and the 8031 for applications desiring the flexibility of External Program Memory which can be easily modified and updated in the field.

MACRO-VIEW OF THE 8051

On a single die the 8051 microcomputer combines CPU; 4K x 8 read-only program memory; 128 x 8 RAM; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority-level, nested interrupt structure; serial I/O port for either multi-processor communications, I/O expansion or full duplex UART; and on-chip oscillator and clock circuits. This section will provide an overview of the 8051 by providing a high-level description of its major elements: the CPU architecture and the on-chip functions peripheral to the CPU. The generic term "8051" is used to refer collectively to the 8031 and 8051.

8051 CPU ARCHITECTURE

The 8051 CPU manipulates operands in four memory spaces. These are the 64K-byte Program Memory, 64K-byte External Data Memory, 256-byte Internal Data Memory and 16-bit Program Counter spaces. The Internal Data Memory address space is further divided into the 128-byte Internal Data RAM and 128-byte Special Function Register (SFR) address spaces shown in Figure 4. Four Register Banks (each with eight registers), 128 addressable bits and the stack reside in the Internal Data RAM. The stack depth is limited only by the available Internal Data RAM and its location is determined by the 8-bit stack pointer. All registers except the Program Counter and the four 8-Register Banks reside in the Special Function Register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, timers, and a serial port. 128 bit locations in the SFR address space are addressable as bits. The 8051 contains 128 bytes of Internal Data RAM and 20 SFRs.

The 8051 provides a non-paged Program Memory address space to accommodate relocatable code. Conditional branches are performed relative to the Program Counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. Sixteen-bit jumps and calls permit branching to any location in the contiguous 64K Program Memory address space.

The 8051 has five methods for addressing source operands: Register, Direct, Register-Indirect, Immediate, and Base-Register-plus-Index-Register-Indirect Addressing. The first three methods can be used for addressing destination operands. Most instructions have a "destination, source" field that specifies the data type, addressing methods, and operands involved. For operations other than moves, the destination operand is also a source operand.

Registers in the four 8-Register Banks can be accessed through Register, Direct, or Register-Indirect Addressing; the 128 bytes of Internal Data RAM through Direct or Register-Indirect Addressing; and the Special Function Registers through Direct Addressing. External Data Memory is accessed through Register-Indirect Addressing. Look-Up-Tables resident in Program Memory can be accessed though Base-Register-plus-Index-Register-Indirect Addressing.

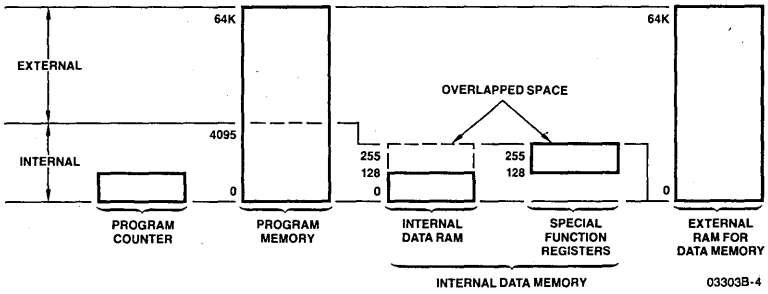
The 8051 is classified as an 8-bit machine since the internal ROM, RAM, Special Function Registers, Arithmetic/Logic Unit, and external data bus are each 8-bits wide. The 8051 performs operations on bit, nibble, byte, and double-byte data types.

The 8051 has extensive facilities for byte transfer, logic, and integer arithmetic operations. It excels at bit handling since data transfer, logic, and conditional branch operations can be performed directly on Boolean variables.

8051 INSTRUCTION SET

The 8051's instruction set is an enhancement of the instruction set familiar to 8048 users. It is enhanced to allow expansion of on-chip CPU peripherals and to optimize byte efficiency and execution speed. Op codes were reassigned to add new high-power operations and to permit new addressing modes which make the old operations more orthogonal. Efficient use of program memory results from an instruction set consisting of 49 single-byte, 45 two-byte, and 17 three-byte instructions. When using a 12MHz oscillator, 64 instructions execute in 1μs and 45

Figure 4. 8051 Family Memory Organization



instructions execute in 2μs. The remaining instructions (multiply and divide) execute in only 4μs. The number of bytes in each instruction and the number of cycles required for execution are listed in Table 1 on pages 14 and 15.

ON-CHIP PERIPHERAL FUNCTIONS

Thus far only the CPU and memory spaces of the 8051 have been described. In addition to the CPU and memories, an interrupt system, extensive I/O facilities, and several peripheral functions are integrated on-chip to relieve the CPU of repetitious, complicated, or time-critical tasks and to permit stringent real-time control of external system interfaces. The extensive I/O facilities include the I/O pins, parallel I/O ports, bidirectional address/data bus, and the serial port for I/O expansion. The CPU peripheral functions integrated on-chip are the two 16-bit counters and the serial port. All of these work together to greatly boost system performance.

INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency ranges from 3μs to 7μs when using a 12MHz crystal.

The 8051 acknowledges interrupt requests from five sources: Two from external sources via the $\overline{INT_0}$ and $\overline{INT_1}$ pins, one from each of the two internal counters and one from the serial I/O port. Each interrupt vectors to a separate location in Program Memory for its service program. Each of the five sources can be assigned to either of two priority levels and can be independently enabled and disabled. Additionally all enabled sources can be globally disabled or enabled. Each external interrupt is programmable as either level- or transition-activated and is active-low to allow the "wire or-ing" of several interrupt sources to the input pin. The interrupt system is shown diagrammatically in Figure 5.

I/O FACILITIES

The 8051 has instructions that treat its 32 I/O lines as 32 individually addressable bits and as four parallel 8-bit ports addressable as Ports 0, 1, 2, and 3. Ports 0, 2, and 3 can also assume other functions. Port 0 provides the multiplexed low-order address and data bus used for expanding the 8051 with standard memories and peripherals. Port 2 provides the high-order address bus when expanding the 8051 with external Program Memory or more than 256 bytes of External Data Memory. The pins of Port 3 can be configured individually to provide external interrupt request inputs, counter inputs, the serial port's receiver input and transmitter output, and to generate the control signals used for reading and writing External Data Memory. The generation or use of an alternate function on a Port 3 pin is done automatically by the 8051 as long as the pin is configured as an input. The configuration of the ports is shown on the 8051 Family Logic Symbol of Figure 2.

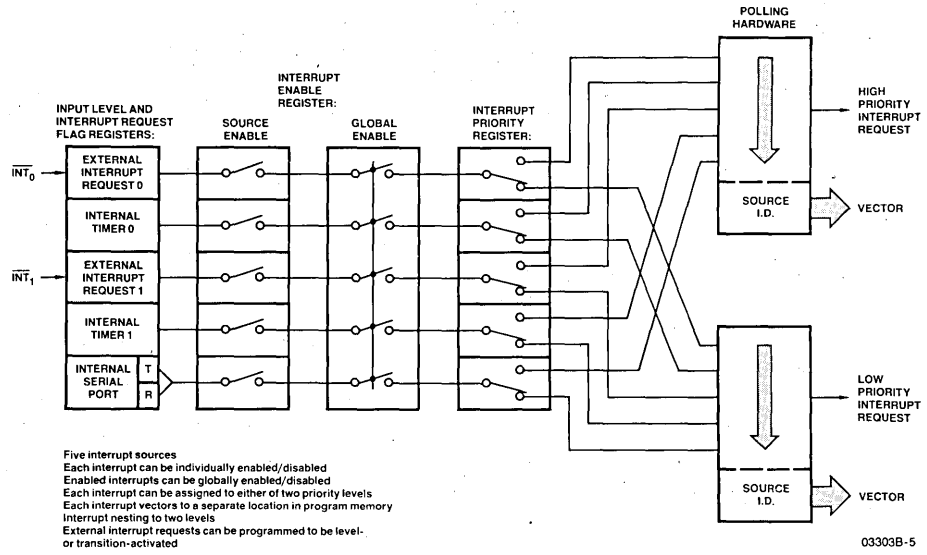
Open Drain I/O Pins

Each pin of Port 0 can be configured as an open drain output or as a high-impedance input. Resetting the microcomputer programs each pin as an input by writing a one (1) to the pin. If a zero (0) is later written to the pin it becomes configured as an output and will continuously sink current. Rewriting the pin to a one (1) will place its output driver in a high-impedance state and configure the pin as an input. Each I/O pin of Port 0 can sink/source eight LS TTL loads.

Quasi-Bidirectional I/O Pins

Ports 1, 2, and 3 are quasi-bidirectional buffers. Resetting the microcomputer programs each pin as an input by writing a one (1) to the pin. If a zero (0) is later written to the pin it becomes configured as an output and will continuously sink current. Any pin that is configured as an output will be reconfigured as an input when a one (1) is written to the pin. Simultaneous to this reconfiguration, the output driver of the quasi-bidirectional port will source current for two oscillator periods. Since current is sourced only when a bit previously written to a zero (0) is up-

Figure 5. 8051 Interrupt System



dated to a one (1), a pin programmed as an input will not source current into the TTL gate that is driving it if the pin is later written with another one (1). Since the quasi-bidirectional output driver sources current for only two oscillator periods, an internal pull-up resistor of approximately 20K- to 40K-ohms is provided to hold the external driver's loading at a TTL high level. Ports 1, 2, and 3 can sink/source four LS TTL loads.

Microprocessor Bus

A microprocessor bus is provided to permit the 8051 to solve a wide range of problems and to allow the upward growth of user products. This multiplexed address and data bus provides an interface compatible with standard memories, 8080 peripherals, and the 8085 compatible memories that include on-chip programmable I/O ports and timing functions. These are summarized in the 8051 Microcomputer Expansion Components chart of Figure 6.

When accessing external memory the high-order address is emitted on Port 2 and the low-order address on Port 0. The ALE signal is provided for strobing the address into an external latch. The program store enable ($\overline{PSEN}$) signal is provided for enabling an external memory device to Port 0 during a read from the Program Memory address space. When the MOVX instruction is executed Port 3 automatically generates the read ($\overline{RD}$) signal for enabling an External Data Memory device to Port 0 or generates the write ($\overline{WR}$) signal for strobing the external memory device with the data emitted by Port 0. Port 0 emits the address and data to the external memory through a push/pull driver that can sink/source eight LS TTL loads. At the end of the read/write bus cycle, Port 0 is automatically reprogrammed to its high impedance state and Port 2 is returned to the state it had prior to the bus cycle. The 8051 generates the address, data, and control signals needed by memory and I/O devices in a manner that minimizes the requirements placed on external program and data memories. At 12MHz, the Program Memory cycle time is 500ns and the access times required from stable address and $\overline{PSEN}$ are approximately 320ns and 150ns respectively. The External Data Memory cycle time is 1μs and the access times required for stable address from read ($\overline{RD}$) or write ($\overline{WR}$) command are approximately 600ns and 250ns respectively.

TIMER/EVENT COUNTERS

The 8051 contains two 16-bit counters for measuring timing events and pulse widths, for counting events, as well as for generating precise, periodic interrupt requests. Each can be programmed independently to one of the following three modes:

Mode 0 – similar to an 8048 8-bit timer or counter with divide by 32 prescaler.

Mode 1 – 16-bit time-interval or event counter.

Mode 2 – 8-bit time-interval or event counter with automatic reload upon overflow.

Additionally, counter 0 can be programmed to a mode that divides it into one 8-bit time-interval or event counter and one 8-bit time-interval counter (Mode 3). When counter 0 is in Mode 3, counter 1 can be programmed to any of the three aforementioned modes, although it cannot set an interrupt request flag or generate an interrupt. This mode is useful because counter 1's overflow can be used to pulse the serial port's transmission-rate generator. Along with their multiple operating modes and 16-bit precision, the counters can also handle very high input frequencies. These range from 0.1MHz to 1.0MHz (from 1.2MHz to 12MHz crystal) when programmed for an input that is a division by 12 of the oscillator frequency and from 0Hz to an upper limit of 50KHz to 0.5MHz (from 1.2MHz to 12MHz crystal) when programmed for external inputs. Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse widths.

Figure 6. 8051 Microcomputer Expansion Components

Category	AMD Part No.	Description	Comments	Program or Data Memory	Crystal Frequency MHz (Max)
Standard EPROMs	2708	1K x 8 450ns Light Erasable	User programmable and erasable.	P	7
	2716-1	2K x 8 350ns Light Erasable		P	8
	2732	4K x 8 450ns Light Erasable		P	8
	2732A-2	4K x 8 200ns Light Erasable		P	12
Standard RAMs	2114A	1K x 4 100ns RAM	Data memory can be easily expanded using standard NMOS RAMs.	D	12
	2148	1K x 4 70ns RAM		D	12
Standard I/O	8212	8-Bit I/O Port	Serves as Address Latch or I/O port.	D	12
	8255A	Programmable Peripheral Interface	Three 8-bit programmable I/O ports.	D	12
	8251A	Programmable Communications Interface	Serial Communications Receiver/Transmitter.	D	12
Standard Peripherals	8286	Bi-directional Bus Driver	8080 and 8085 peripheral devices are compatible with the 8051 allowing easy addition of specialized interfaces.	D	12
	8287	Bi-directional Bus Driver (Inverting)		D	12
	8253A	Programmable Interval Timer		D	12
	8279	Programmable Keyboard/Display Interface (128 Keys)		D	12
Universal Peripheral Interfaces	8041A	ROM Program Memory	Mask programmable to perform custom I/O and control functions	D/P	12/11.7
Memories with on-chip I/O and Peripheral Functions.	8155-2	256 x 8 330ns RAM		D	12

The counters are started and stopped under software control. Each counter sets its interrupt request flag when it overflows from all ones to all zeroes (or auto-reload value). The operating modes and input sources are summarized in Figures 7 and 8. The effects of the configuration flags and the status flags are shown in Figures 9 and 10.

SERIAL COMMUNICATIONS

The 8051's serial I/O port is useful for serially linking peripheral devices as well as multiple 8051s through standard asynchronous protocols with full-duplex operation. The serial port also has a synchronous mode for expansion of I/O lines using CMOS and TTL shift registers. This hardware serial communications interface saves ROM code and permits a much higher transmission rate than could be achieved through software. In response to a serial port interrupt request, the CPU has only to read/write the serial port's buffer to service the serial link. A block diagram of the serial port is shown in Figures 11 and 12. Methods for linking UART (universal asynchronous receiver/transmitter) devices are shown in Figure 13 and a method for I/O expansion is shown in Figure 14.

The full-duplex serial I/O port provides asynchronous modes to facilitate communications with standard UART devices, such as printers and CRT terminals, or communications with other 8051s in multi-processor systems. The receiver is double buffered to eliminate the overrun that would occur if the CPU failed to respond to the receiver's interrupt before the beginning of the next frame. The 8051 can generally maintain the serial link at its maximum rate so double buffering of the transmitter is not needed. A minor degradation in transmission rate can occur in rare events such as when the servicing of the transmitter has to wait for a lengthy interrupt service program to complete. In asynchronous modes, false start-bit rejection is provided on received frames. For noise rejection a best two-out-of-three vote is taken on three samples near the center of each received bit.

When interfacing with standard UART devices, the serial channel can be programmed to Mode 1 which transmits/receives a ten-bit frame or programmed to Mode 2 or 3 which transmits/receives an eleven-bit frame as shown in Figure 15. The frame consists of a start bit, eight or nine data bits, and one stop bit. In Modes 1 and 3, the transmission-rate timing circuitry receives a pulse from counter 1 each time the counter overflows. The input to counter 1 can be an external source or a division by 12 of the oscillator frequency. The auto-reload mode of the counter provides communication rates of 122 to 31,250 bits per second (including start and stop bits) for a 12MHz crystal. In Mode 2 the communication rate is a division by 64 of the oscillator frequency yielding a transmission rate of 187,500 bits per second (including start and stop bits) for a 12MHz crystal.

Figure 7. Timer/Event Counter Modes 0, 1 and 2

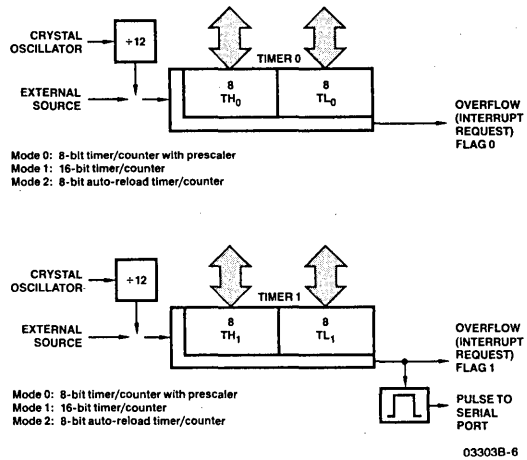


Figure 8. Timer/Event Counter 0 in Mode 3

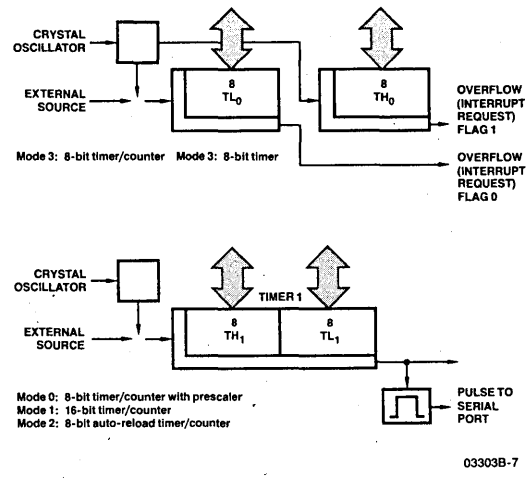


Figure 9. Timer/Counter 0 Control and Status Flag Circuitry

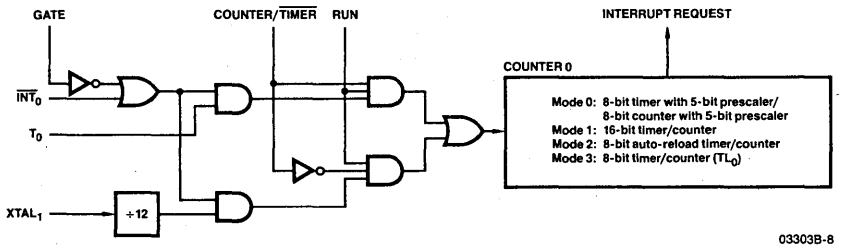


Figure 10. Timer/Counter 1 Control and Status Flag Circuitry

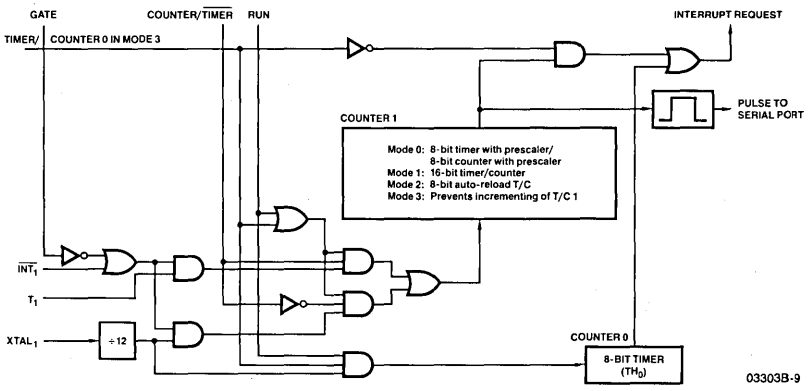


Figure 11. Serial Port – Synchronous Mode 0

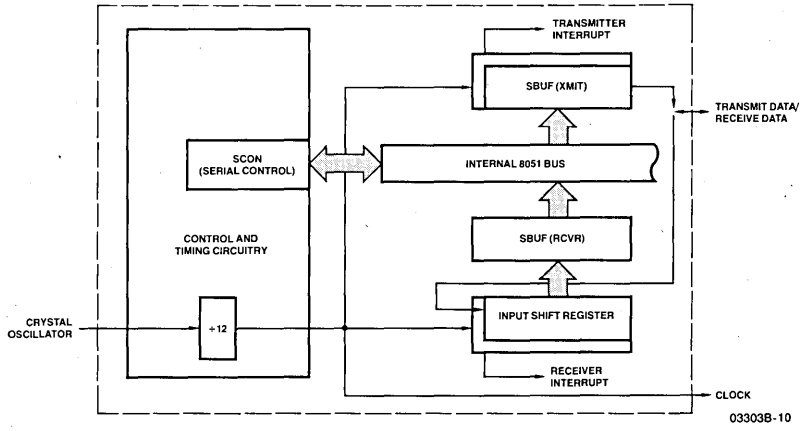


Figure 12. Serial Port – UART Modes 1, 2 and 3

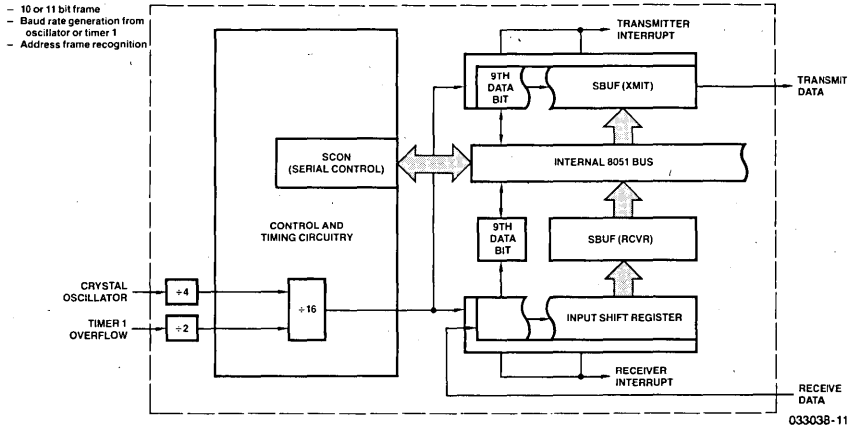


Figure 13. UART Interfacing Schemes

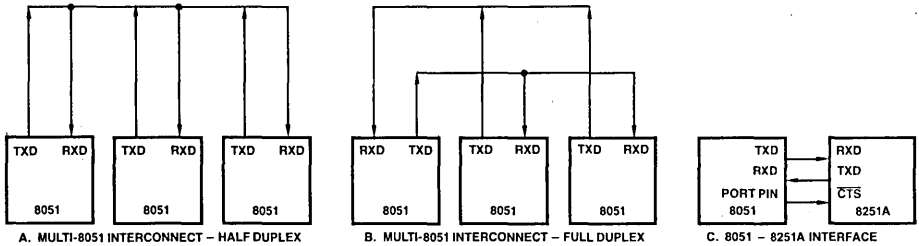


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Figure 14. I/O Expansion Technique

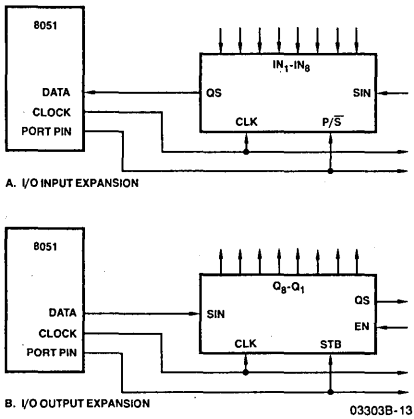

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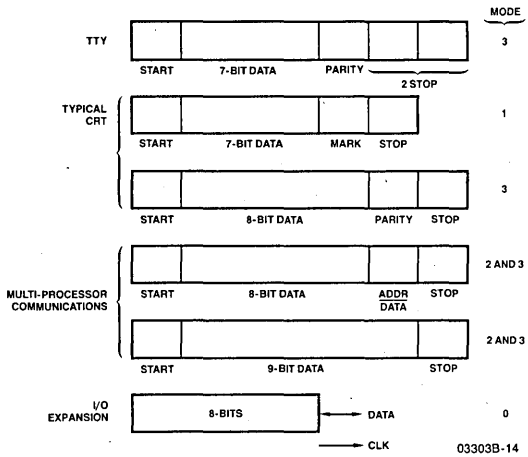
Figure 15. Typical Frame Formats



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Distributed processing offers a faster, more powerful system than a single CPU can provide. This results from a hierarchy of interconnected processors, each with its own memories and I/O. In a multiprocessing environment, a single host 8051 controls other slave 8051s configured to operate simultaneously on separate portions of a program. The interconnected 8051s reduce the load on the host processor and result in a lower-cost system of data transmission. This form of distributed processing is especially effective in a complex process where controls are required at physically separated locations.

In Modes 2 and 3 interprocessor communication is facilitated by the automatic wake-up of slave processors through interrupt driven address-frame recognition. The protocol for interprocessor communications is shown in Figure 16. In synchronous mode (Mode 0) the high speed serial port provides an efficient, low-cost method of expanding I/O lines using standard TTL and CMOS shift registers. The serial channel provides a clock output for synchronizing the shifting of bits to/from an external register. The data rate is a division by 12 of the oscillator frequency and hence is 1M bits per second at 12MHz.

Figure 16. Protocol for Multi-Processor Communications

1. Slaves – Configure serial port to interrupt CPU if the received ninth data bit is a one (1).
2. Master – Transmit frame containing address in first 8 data bits and set ninth data bit (i.e., ninth data bit designates address frame).
3. Slaves – Serial port interrupts CPU when address frame is received. Interrupt service program compares received address to its address. The slave which has been addressed reconfigures its serial port to interrupt the CPU on all subsequent transmissions.
4. Master – Transmit control frames and data frames (these will be accepted only by the previously addressed slave).

ABSOLUTE MAXIMUM RATINGS above which useful life may be impaired*

Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground	−0.5 to +7.0V
Power Dissipation	2W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoid exposure to excessive voltages.

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8051/8031 DC CHARACTERISTICS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage (Except RST/V_{PD} and $XTAL_2$)		2.0		V_{CC} +0.5	V
V_{IH1}	Input High Voltage to RST/V_{PD} for Reset, $XTAL_2$	$XTAL_1$ to V_{SS}	2.5			V
V_{PD}	Power Down Voltage to RST/V_{PD}	V_{CC} = 0V	4.5		5.5	V
V_{OL}	Output Low Voltage, Ports 1, 2, 3 (Note 1)	I_{OL} = 1.6mA			0.45	V
V_{OL1}	Output Low Voltage, Port 0, ALE, $\overline{PSEN}$ (Note 1)	I_{OL} = 3.2mA			0.45	V
V_{OH}	Output High Voltage, Ports 1, 2, 3	I_{OH} = −80μA	2.4			V
V_{OH1}	Output High Voltage, Port 0, ALE, $\overline{PSEN}$	I_{OH} = −400μA	2.4			V
I_{IL}	Logical 0 Input Current, $XTAL_2$, Ports 1, 2, 3	$XTAL_1$ at V_{SS} V_{IL} = 0.45V			−800	μA
I_{IH1}	Input High Current to RST/V_{PD} for Reset	V_{IN} = V_{CC} − 1.5V			500	μA
I_{LI}	Input Leakage Current to Port 0, $\overline{EA}$	0 < V_{IN} < V_{CC}			10	μA
I_{CC}	Power Supply Current			125	160	mA
I_{PD}	Power Down Current			10	20	mA
C_{IO}	Capacitance of I/O Buffer	fc = 1MHz			10	pF

Note 1. V_{OL} is degraded when the 8051 rapidly discharges external capacitance. This AC noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the 8051 as possible.

8051 PROGRAM VERIFICATION

To ensure correct factory masked ROM, the following procedure may be followed. The address of the location to be verified is input on Port 1 (pins 1 through 8) while Port 2 (pins 21 through 28) and PSEN (pin 29) are held low. RST/VPD (pin 9) and ALE (pin 30) are held high. The data to be verified is read out through Port 0 (pins 32 through 39).

Datum	Emitting Ports	Time Interval	Degraded I/O Lines	V_{OL} (peak) (max)
Address	P2, P0	T3, T9	P1, P3	0.8V
Write Data	P0	T6	P1, P3, ALE	0.8V

9

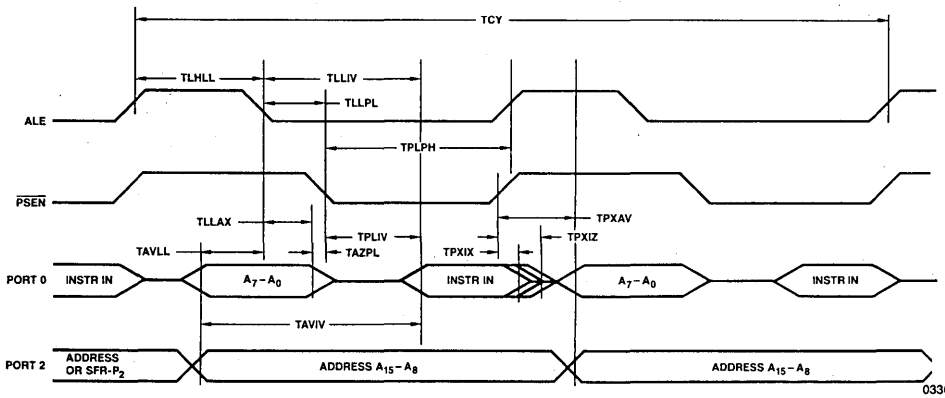
8051/8031 AC CHARACTERISTICS (C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100pF; C_L for All Other Outputs = 80pF)

Parameter	Description	12MHz Clock		Variable Clock 1/TCLCL = 1.2MHz to 12MHz		Units
		Min	Max	Min	Max	
PROGRAM MEMORY						
TCY	Min Instruction Cycle Time (Note 3)	1.0		12TCLCL	12TCLCL	ns
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Setup to ALE	53		TCLCL−30		ns
TLLAX	Address Hold After ALE (Note 1)	48		TCLCL−35		ns
TLLIV	ALE to Valid Instruction In		233		4TCLCL−100	ns
TLLPL	ALE to $\overline{PSEN}$	58		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL−35		ns
TPLIV	$\overline{PSEN}$ to Valid Instruction In		125		3TCLCL−125	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$ (Note 2)		63		TCLCL−20	ns
TPXAV	Address Valid After $\overline{PSEN}$ (Note 2)	75		TCLCL−8		ns
TAVIV	Address to Valid Instruction In		302		5TCLCL−115	ns
TAZPL	Address Float to $\overline{PSEN}$	0		0		ns
EXTERNAL DATA MEMORY						
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TLLAX	Address Hold After ALE (Note 1)	132		2TCLCL−35		ns
TRLDV	$\overline{RD}$ to Valid Data In		250		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL−70	ns
TLLDV	ALE to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203		4TCLCL−130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns
TDVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL−50		ns
TQVWH	Data Setup Before $\overline{WR}$	433		7TCLCL−150		ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	Address Float After $\overline{RD}$		0		0	ns

Notes: 1. TLLAX for access to Program Memory is different from TLLAX for access to Data Memory.
2. Interfacing the 8051 to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.
3. TCY is the minimum instruction cycle time which consists of 12 oscillator clocks or two ALE cycles.

WAVEFORMS

PROGRAM MEMORY READ CYCLE



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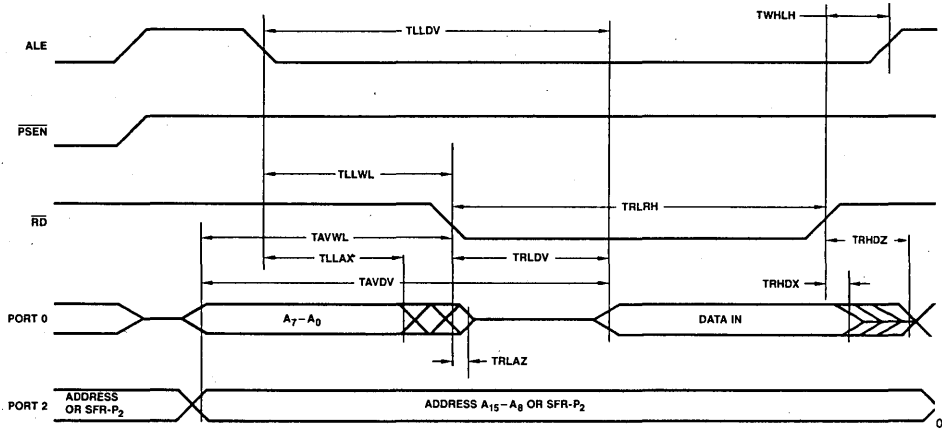
DATA MEMORY READ CYCLE



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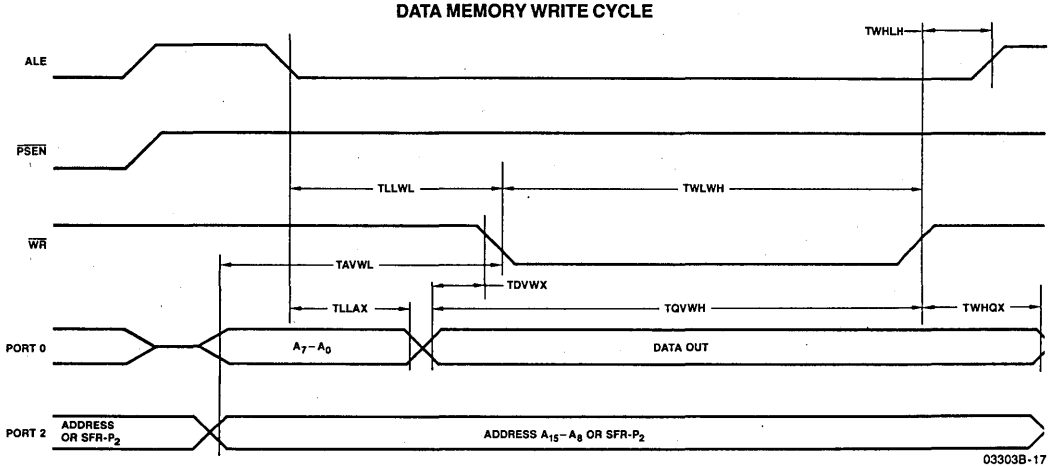
DATA MEMORY WRITE CYCLE



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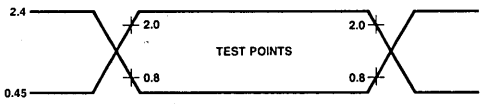
AC TESTING INPUT, OUTPUT, FLOAT WAVEFORMS

INPUT/OUTPUT



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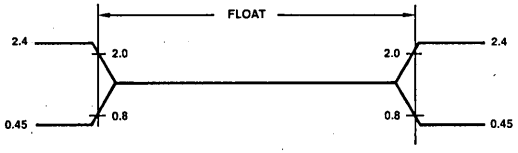
FLOAT



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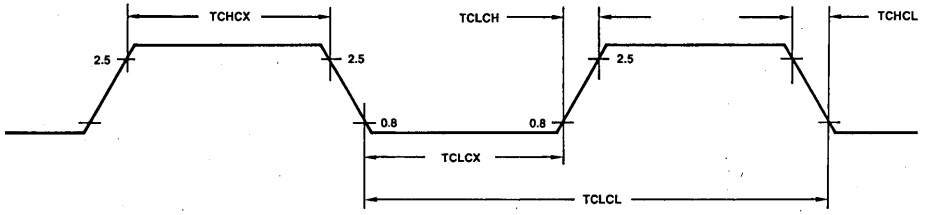
AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0."
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."
For timing purposes, the float state is defined as the point at which a P_0 pin sinks 3.2mA or sources 400μA at the voltage test levels.

EXTERNAL CLOCK DRIVE $XTAL_2$



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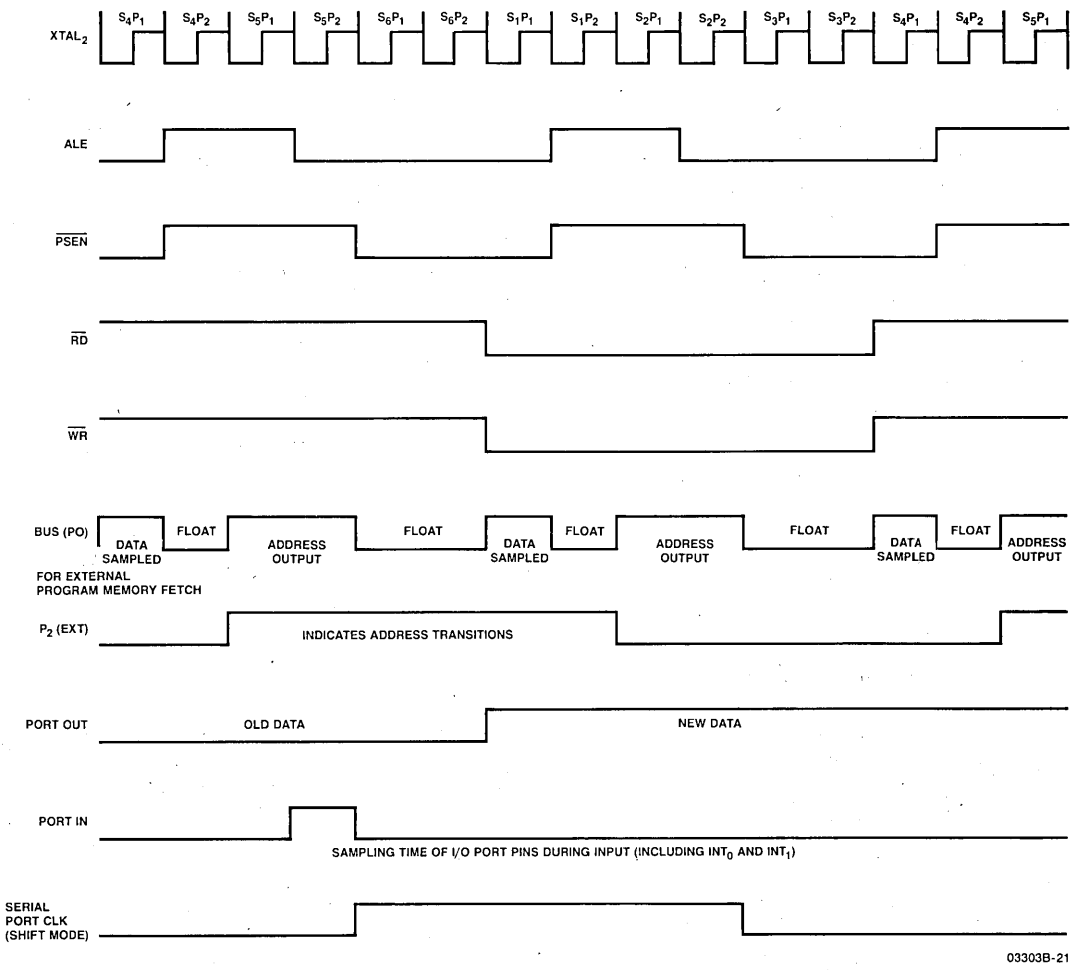
CLOCKING DETAILS

Symbol	Parameters	Variable Clock Freq = 1.2MHz to 12MHz		Unit
		Min	Max	
TCLCL	Oscillator Period	83.3	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	ns
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

WAVEFORMS



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All internal timing is referenced to the internal time states shown at the top of the page. This waveform represents the signal on the X_2 input of the oscillator. This diagram represents when these signals are actually clocked within the chip. However, the time it takes a signal to propagate to the pins is in the range of 50–150ns. Prop delays are dependent on many variables, such as temperature, pin loading. Even the different signals vary. Typically though, /RD and /WR have prop delays of approximately 50ns and the other timing signals approximately 85ns, at room temperature, fully loaded. These differences in prop delays between signals have been integrated into the timing specs.

TABLE 1. 8051/8031 INSTRUCTION SET

INSTRUCTIONS THAT AFFECT FLAG SETTINGS*

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C, bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C, bit	X		
RLC	X			CJNE	X		
SETB C	1						

Interrupt Response Time: To finish execution of current instruction, respond to the interrupt request, push the PC and to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (3 to 7μs @ 12MHz).

*Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

DATA TRANSFER (Note 1)

Mnemonic		Description	Bytes	Cycle
MOV	A,Rn	Move register to Accumulator	1	1
*MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
*MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
*MOV	direct,A	Move Accumulator to direct byte	2	1
*MOV	direct,Rn	Move register to direct byte	2	2
*MOV	direct,direct	Move direct byte to direct byte	3	2
*MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
*MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
*MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
*MOV	DPTR, #data16	Move 16-bit constant to Data Pointer	3	2
*MOVC	A,@A+ DPTR	Move Code byte relative to DPTR to Accumulator	1	2
*MOVC	A,@A+PC	Move Code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move External RAM (8-bit address) to Accumulator	1	2
*MOVX	A,@DPTR	Move External RAM (16-bit address) to Accumulator	1	2
MOVX	@Ri,A	Move Accumulator to External RAM (8-bit address)	1	2
*MOVX	@DPTR,A	Move Accumulator to External RAM (16-bit address)	1	2
*PUSH	direct	Push direct byte onto stack	2	2
*POP	direct	Pop direct byte off of stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
*XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange indirect RAM's least sig nibble with A's LSN	1	1

*New operation not provided by 8048/8049 Family

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cycle
CLR	C	Clear Carry Flag	1	1
*CLR	bit	Clear direct bit	2	1
*SETB	C	Set Carry Flag	1	1
*SETB	bit	Set direct bit	2	1
CPL	C	Complement Carry Flag	1	1
*CPL	bit	Complement direct bit	2	1
*ANL	C,bit	AND direct bit to Carry Flag	2	2
*ANL	C,/bit	AND complement of direct bit to Carry	2	2
*ORL	C,bit	OR direct bit to Carry Flag		
*ORL	C,/bit	OR complement of direct bit to Carry	2	2
*MOV	C,bit	Move direct bit to Carry Flag	2	1
*MOV	bit,C	Move Carry Flag to direct bit	2	2

LOGIC

Mnemonic		Description	Bytes	Cycle
ANL	A,Rn	AND register to Accumulator	1	1
*ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
*ANL	direct,A	AND Accumulator to direct byte	2	1
*ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
*ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
*ORL	direct,A	OR Accumulator to direct byte	2	1
*ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
*XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1
*XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1

Note 1: Special care should be taken (particularly with the 8031) when using the MOV instruction. The MOV instruction should *not* be used to move data on port 0 nor 2 when these ports are used to address external memory.

TABLE 1. 8051/8031 INSTRUCTION SET (Cont.)

LOGIC (Cont.)

Mnemonic		Description	Bytes	Cycle
*XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate Accumulator Left through Carry Flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate Accumulator Right through Carry Flag	1	1
SWAP	A	Exchange nibbles within Accumulator	1	1

ARITHMETIC

Mnemonic		Description	Bytes	Cycle
ADD	A,Rn	Add register to Accumulator	1	1
*ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with carry	1	1
*ADDC	A,direct	Add direct byte to Accumulator with Carry Flag	2	1
ADDC	A,@Ri	Add indirect RAM and Carry Flag to Accumulator	1	1
ADDC	A,#data	Add immediate data and Carry Flag to Accumulator	2	1
*SUBB	A,Rn	Subtract register from Accumulator with Borrow	1	1
*SUBB	A,direct	Subtract direct byte from Accumulator with Borrow	2	1
*SUBB	A,@Ri	Subtract indirect RAM from Accumulator with Borrow	1	1
*SUBB	A,#data	Subtract immediate data from Accumulator with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
*INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
*DEC	direct	Decrement direct byte	2	1
*DEC	@Ri	Decrement indirect RAM	1	1
*INC	DPTR	Increment Data Pointer	1	2
*MUL	AB	Multiply Accumulator times B	1	4
*DIV	AB	Divide Accumulator by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

OTHER

Mnemonic	Description	Bytes	Cycle
NOP	No Operation	1	1

CONTROL TRANSFER (BRANCH)

Mnemonic		Description	Bytes	Cycle
AJMP	addr11	Absolute Jump	2	2
*LJMP	addr16	Long Jump	3	2
*SJMP	rel	Short Jump (relative addr)	2	2
*JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry Flag is set	2	2
JNC	rel	Jump if carry is not set	2	2
*JB	bit,rel	Jump relative if direct bit is set	3	2
*JNB	bit,rel	Jump relative if direct bit is not set	3	2
*JBC	bit,rel	Jump relative if direct bit is set, then clear bit	3	2
*CJNE	A,direct,rel	Compare direct byte to Accumulator and Jump if not Equal	3	2
*CJNE	A,#data,rel	Compare immediate to Accumulator and Jump if not Equal	3	2
*CJNE	Rn,#data, rel	Compare immediate to reg and Jump if not Equal	3	2
*CJNE	@Ri, #data,rel	Compare immed. to indirect RAM and Jump if not Equal	3	2
DJNZ	Rn,rel	Decrement register and Jump if not zero	2	2
*DJNZ	direct,rel	Decrement direct byte and Jump if not zero	3	2

CONTROL TRANSFER (SUBROUTINE)

Mnemonic		Description	Bytes	Cycle
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from Subroutine Call	1	2
RETI		Return from Interrupt Call	1	2

Notes on data addressing modes:

- Rn – Working register R0 – R7 of the currently selected Register bank.
- direct – 128 internal RAM locations, any I/O port, control, or status register.
- @Ri – Indirect internal RAM location addressed by register R0 or R1.
- #data – 8-bit constant included in instruction.
- #data16 – 16-bit constant included as bytes 2 and 3 of instruction.
- bit – 128 software flags, any I/O pin, control, or status bit.

Notes on program addressing modes:

- addr16 – Destination address for LCALL and LJMP may be anywhere within the 64-Kilobyte program memory address space.
- addr11 – Destination address for ACALL and AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
- rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127, −128 bytes relative to first byte of the following instruction.

*New operation not provided by 8048/8049 Family

TABLE 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER

Hex Code	Bytes	Mnemonic	Operands	Hex Code	Bytes	Mnemonic	Operands
00	1	NOP		42	2	ORL	Data addr,A
01	2	AJMP	Code addr	43	3	ORL	Data addr,#data
02	3	LJMP	Code addr	44	2	ORL	A,#data
03	1	RR	A	45	2	ORL	A,data addr
04	1	INC	A	46	1	ORL	A,@R0
05	2	INC	Data addr	47	1	ORL	A,@R1
06	1	INC	@R0	48	1	ORL	A,R0
07	1	INC	@R1	49	1	ORL	A,R1
08	1	INC	R0	4A	1	ORL	A,R2
09	1	INC	R1	4B	1	ORL	A,R3
0A	1	INC	R2	4C	1	ORL	A,R4
0B	1	INC	R3	4D	1	ORL	A,R5
0C	1	INC	R4	4E	1	ORL	A,R6
0D	1	INC	R5	4F	1	ORL	A,R7
0E	1	INC	R6	50	2	JNC	Code addr
0F	1	INC	R7	51	2	ACALL	Code addr
10	3	JBC	Bit addr,code addr	52	2	ANL	Data addr,A
11	2	ACALL	Code addr	53	3	ANL	Data addr,#data
12	3	LCALL	Code addr	54	2	ANL	A,#data
13	1	RRC	A	55	2	ANL	A,data addr
14	1	DEC	A	56	1	ANL	A,@R0
15	2	DEC	Data addr	57	1	ANL	A,@R1
16	1	DEC	@R0	58	1	ANL	A,R0
17	1	DEC	@R1	59	1	ANL	A,R1
18	1	DEC	R0	5A	1	ANL	A,R2
19	1	DEC	R1	5B	1	ANL	A,R3
1A	1	DEC	R2	5C	1	ANL	A,R4
1B	1	DEC	R3	5D	1	ANL	A,R5
1C	1	DEC	R4	5E	1	ANL	A,R6
1D	1	DEC	R5	5F	1	ANL	A,R7
1E	1	DEC	R6	60	2	JZ	Code addr
1F	1	DEC	R7	61	2	AJMP	Code addr
20	3	JB	Bit addr,code addr	62	2	XRL	Data addr,A
21	2	AJMP	Code addr	63	3	XRL	Data addr,#data
22	1	RET		64	2	XRL	A, #data
23	1	RL	A	65	2	XRL	A,data addr
24	2	ADD	A,#data	66	1	XRL	A,@R0
25	2	ADD	A,data addr	67	1	XRL	A,@R1
26	1	ADD	A,@R0	68	1	XRL	A,R0
27	1	ADD	A,@R1	69	1	XRL	A,R1
28	1	ADD	A,R0	6A	1	XRL	A,R2
29	1	ADD	A,R1	6B	1	XRL	A,R3
2A	1	ADD	A,R2	6C	1	XRL	A,R4
2B	1	ADD	A,R3	6D	1	XRL	A,R5
2C	1	ADD	A,R4	6E	1	XRL	A,R6
2D	1	ADD	A,R5	6F	1	XRL	A,R7
2E	1	ADD	A,R6	70	2	JNZ	Code addr
2F	1	ADD	A,R7	71	2	ACALL	Code addr
30	3	JNB	Bit addr,code addr	72	2	ORL	C,bit addr
31	2	ACALL	Code addr	73	1	JMP	@A+DPTR
32	1	RETI		74	2	MOV	A,#data
33	1	RLC	A	75	3	MOV	Data addr,#data
34	2	ADDC	A,#data	76	2	MOV	@R0,#data
35	2	ADDC	A,data addr	77	2	MOV	@R1,#data
36	1	ADDC	A,@R0	78	2	MOV	R0,#data
37	1	ADDC	A,@R1	79	2	MOV	R1,#data
38	1	ADDC	A,R0	7A	2	MOV	R2,#data
39	1	ADDC	A,R1	7B	2	MOV	R3,#data
3A	1	ADDC	A,R2	7C	2	MOV	R4,#data
3B	1	ADDC	A,R3	7D	2	MOV	R5,#data
3C	1	ADDC	A,R4	7E	2	MOV	R6,#data
3D	1	ADDC	A,R5	7F	2	MOV	R7,#data
3E	1	ADDC	A,R6	80	2	SJMP	Code addr
3F	1	ADDC	A,R7	81	2	AJMP	Code addr
40	2	JC	Code addr	82	2	ANL	C,bit addr
41	2	AJMP	Code addr	83	1	MOVC	A,@A+PC

TABLE 2. INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Cont.)

Hex Code	Bytes	Mnemonic	Operands	Hex Code	Bytes	Mnemonic	Operands
84	1	DIV	AB	C2	2	CLR	Bit addr
85	3	MOV	Data addr,data addr	C3	1	CLR	C
86	2	MOV	Data addr,@R0	C4	1	SWAP	A
87	2	MOV	Data addr,@R1	C5	2	XCH	A,data addr
88	2	MOV	Data addr,R0	C6	1	XCH	A,@R0
89	2	MOV	Data addr,R1	C7	1	XCH	A,@R1
8A	2	MOV	Data addr,R2	C8	1	XCH	A,R0
8B	2	MOV	Data addr,R3	C9	1	XCH	A,R1
8C	2	MOV	Data addr,R4	CA	1	XCH	A,R2
8D	2	MOV	Data addr,R5	CB	1	XCH	A,R3
8E	2	MOV	Data addr,R6	CC	1	XCH	A,R4
8F	2	MOV	Data addr,R7	CD	1	XCH	A,R5
90	3	MOV	DPTR,#data	CE	1	XCH	A,R6
91	2	ACALL	Code addr	CF	1	XCH	A,R7
92	2	MOV	Bit addr,C	D0	2	POP	Data addr
93	1	MOVC	A,@A+DPTR	D1	2	ACALL	Code addr
94	2	SUBB	A,#data	D2	2	SETB	Bit addr
95	2	SUBB	A,data addr	D3	1	SETB	C
96	1	SUBB	A,@R0	D4	1	DA	A
97	1	SUBB	A,@R1	D5	3	DJNZ	Data addr,code addr
98	1	SUBB	A,R0	D6	1	XCHD	A,@R0
99	1	SUBB	A,R1	D7	1	XCHD	A,@R1
9A	1	SUBB	A,R2	D8	2	DJNZ	R0,code addr
9B	1	SUBB	A,R3	D9	2	DJNZ	R1,code addr
9C	1	SUBB	A,R4	DA	2	DJNZ	R2,code addr
9D	1	SUBB	A,R5	DB	2	DJNZ	R3,code addr
9E	1	SUBB	A,R6	DC	2	DJNZ	R4,code addr
9F	1	SUBB	A,R7	DD	2	DJNZ	R5,code addr
A0	2	ORL	C,/bit addr	DE	2	DJNZ	R6,code addr
A1	2	AJMP	Code addr	DF	2	DJNZ	R7,code addr
A2	2	MOV	C,bit addr	E0	1	MOVX	A,@DPTR
A3	1	INC	DPTR	E1	2	AJMP	Code addr
A4	1	MUL	AB	E2	1	MOVX	A,@R0
A5		Reserved		E3	1	MOVX	A,@R1
A6	2	MOV	@R0,data addr	E4	1	CLR	A
A7	2	MOV	@R1,data addr	E5	2	MOV	A,data addr
A8	2	MOV	R0,data addr	E6	1	MOV	A,@R0
A9	2	MOV	R1,data addr	E7	1	MOV	A,@R1
AA	2	MOV	R2,data addr	E8	1	MOV	A,R0
AB	2	MOV	R3,data addr	E9	1	MOV	A,R1
AC	2	MOV	R4,data addr	EA	1	MOV	A,R2
AD	2	MOV	R5,data addr	EB	1	MOV	A,R3
AE	2	MOV	R6,data addr	EC	1	MOV	A,R4
AF	2	MOV	R7,data addr	ED	1	MOV	A,R5
B0	2	ANL	C,/bit addr	EE	1	MOV	A,R6
B1	2	ACALL	Code addr	EF	1	MOV	A,R7
B2	2	CPL	Bit addr	F0	1	MOVX	@DPTR,A
B3	1	CPL	C	F1	2	ACALL	Code addr
B4	3	CJNE	A,#data,code addr	F2	1	MOVX	@R0,A
B5	3	CJNE	A,data addr,code addr	F3	1	MOVX	@R1,A
B6	3	CJNE	@R0,#data,code addr	F4	1	CPL	A
B7	3	CJNE	@R1,#data,code addr	F5	2	MOV	Data addr,A
B8	3	CJNE	R0,#data,code addr	F6	1	MOV	@R0,A
B9	3	CJNE	R1,#data,code addr	F7	1	MOV	@R1,A
BA	3	CJNE	R2,#data,code addr	F8	1	MOV	R0,A
BB	3	CJNE	R3,#data,code addr	F9	1	MOV	R1,A
BC	3	CJNE	R4,#data,code addr	FA	1	MOV	R2,A
BD	3	CJNE	R5,#data,code addr	FB	1	MOV	R3,A
BE	3	CJNE	R6,#data,code addr	FC	1	MOV	R4,A
BF	3	CJNE	R7,#data,code addr	FD	1	MOV	R5,A
C0	2	PUSH	Data addr	FE	1	MOV	R6,A
C1	2	AJMP	Code addr	FF	1	MOV	R7,A

8251A

Programmable Communication Interface

DISTINCTIVE CHARACTERISTICS

- Synchronous operation up to 64K baud
- Asynchronous operation up to 19.2K baud
- Full duplex, double-buffered transmitter and receiver
- Fully programmable with several speed and character modes
- Error detection for parity, overrun, and framing
- Compatible with 8080/85/86/88 microprocessors
- Single +5V supply and TTL clock
- False start bit detection; automatic break detect and handling.
- Supports bi-sync

GENERAL DESCRIPTION

The AMD 8251A is the enhanced version of the industry standard 8251. Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for data communications with 8-bit, 16-bit, and single-chip microprocessors. The 8251A is used as a peripheral device and is programmed by the CPU to operate using serial data transmission techniques. The 8251A interfaces easily with a modem.

The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The 8251A communicates with the CPU via direct control lines and 8-bit control words on the system bus. The CPU can query the USART status at any time.

The 8251A is fabricated with a N-channel silicon gate process and is packaged in a plastic or ceramic 28-pin DIP.

Figure 1. Block Diagram

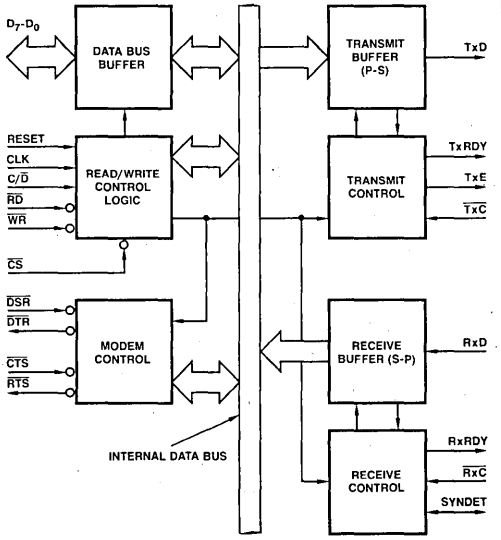
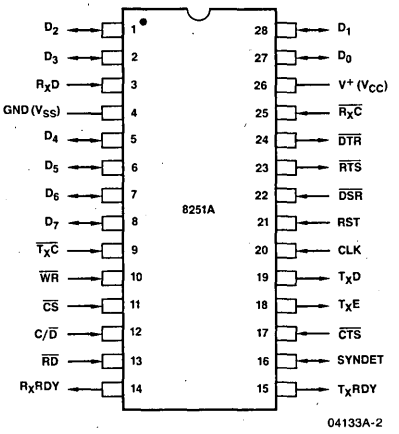


Figure 2. Pin Configuration

D-40
P-40



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Device Number 3MHz
Molded DIP	$0°C \leq T_A \leq 70°C$	P8251A
Hermetic DIP		D8251A
Hermetic DIP	$-40°C \leq T_A \leq +85°C$	ID8251A
Hermetic DIP	$-55°C \leq T_A \leq +125°C$	MD8251AB

FEATURES AND ENHANCEMENTS

The 8251A is an advanced design of the industry standard USART 8251. The 8251A operates with a wide range of microprocessors and microcomputers.

The 8251A incorporates all the key features of the 8251/9551 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of a false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous baud rate from DC to 64K.

MAXIMUM RATINGS

Ambient Temperature Under Bias	−55 to 125°C
Storage Temperature	−65 to +150°C
Voltage to Any Pin with Respect to Ground	−0.5 to +7.0V
Power Dissipation	1.0W

Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE

Part Number	T_A	V_{CC}	V_{SS}
P8251A D8251A	$0°C \leq T_A \leq 70°C$	5.0V ±5%	0V
ID8251A	$-40°C \leq T_A \leq 85°C$	5.0V ±10%	0V
MD8251AB	$-55°C \leq T_A \leq 125°C$	5.0V ±10%	0V

DC CHARACTERISTICS

Com'l $T_A = 0$ to 70°C, $V_{CC} = 5V \pm 5\%$
Ind $T_A = -40$ to 85°C, $V_{CC} = 5V \pm 10\%$
Mil $T_A = -55$ to 125°C, $V_{CC} = 5V \pm 10\%$

Parameter	Description	Test Conditions		Min	Max	Min	Max	Units
V_{IL}	Input Low Voltage			−0.5	0.8	−0.5	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}	2.2	V_{CC}	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.2mA$			0.45		0.45	V
V_{OH}	Output High Voltage	$I_{OL} = -400\mu A$		2.4		2.4		V
I_{OFL}	Output Float Leakage	$V_{OUT} = V_{CC}$ to 0.45V			±10		±10	μA
I_{IL}	Input Leakage	$V_{IN} = V_{CC}$ to 0.45V			±10		±10	μA
I_{CC}	Power Supply Current	All Outputs = High	Com'l		100		150	mA
			Ind		150		150	

CAPACITANCE ($T_A = 25°C$, $V_{CC} = GND = 0V$)

Parameter	Description	Test Conditions	Min	Max	Units
C_{IN}	Input Capacitance	fc = 1MHz		10	pF
$C_{I/O}$	I/O Capacitance	Unmeasured Pins Returned to GND		20	pF

AC CHARACTERISTICS (GND = 0V)

Com'l $T_A = 0$ to 70°C, $V_{CC} = 5V \pm 5\%$
Ind $T_A = -40$ to 85°C, $V_{CC} = 5V \pm 10\%$
Mil $T_A = -55$ to 125°C, $V_{CC} = 5V \pm 10\%$

Bus Parameters (Note 1)

Parameter	Description	Test Conditions	Min	Max	Min	Max	Units
READ CYCLE							
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	Note 2	0		−75		ns
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	Note 2	0		75		ns
t_{RR}	$\overline{READ}$ Pulse Width		250		300		ns
t_{RD}	Data Delay from $\overline{READ}$	3, $C_L = 150pF$		200		280	ns
t_{DF}	$\overline{READ}$ to Data Floating		10	100	5	120	ns
WRITE CYCLE							
t_{AW}	Address Stable Before $\overline{WRITE}$		0		75		
t_{WA}	Address Hold Time for $\overline{WRITE}$		0		75		
t_{WW}	$\overline{WRITE}$ Pulse Width		250		300		
t_{DW}	Data Setup Time for $\overline{WRITE}$		150		200		
t_{WD}	Data Hold Time for $\overline{WRITE}$		20		80		
t_{RV}	Recovery Time Between WRITES	Note 4	6		6		

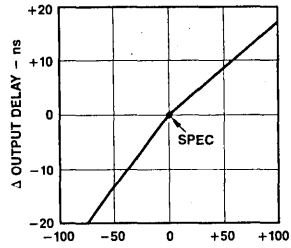
AC CHARACTERISTICS (Cont.) (GND = 0V)

Com'l T_A = 0 to 70°C, V_{CC} = 5V ±5%
Ind T_A = −40 to 85°C, V_{CC} = 5V±10%
Mil T_A = −55 to 125°C, V_{CC} = 5V ±10%

Parameter	Description	Test Conditions	Min	Max	Min	Max	Units
OTHER TIMINGS							
t_{CY}	Clock Period	Notes 5, 6	320	1350	320	1350	ns
t_{ϕ}	Clock High Pulse Width		120	$t_{CY}-90$	150	$t_{CY}-100$	ns
t_{ϕ}	Clock Low Pulse Width		90		100		ns
t_R, t_F	Clock Rise and Fall Time			20		20	ns
t_{DTx}	TxD Delay from Falling Edge of TxC			1		1	μs
f_{Tx}	Transmitter Input Clock Frequency 1x Baud Rate		DC	64	DC	64	kHz
	16x Baud Rate		DC	310	DC	310	kHz
	64x Baud Rate		DC	615	DC	615	kHz
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate		12		12		t_{CY}
	16x and 64x Baud Rate		1		1		t_{CY}
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate		15		15		t_{CY}
	16x and 64x Baud Rate		3		3		t_{CY}
f_{Rx}	Receiver Input Clock Frequency 1x Baud Rate		DC	64	DC	64	kHz
	16x Baud Rate		DC	310	DC	310	kHz
	64x Baud Rate		DC	615	DC	615	kHz
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate		12		12		t_{CY}
	16x and 64x Baud Rate		1		1		t_{CY}
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate		15		15		t_{CY}
	16x and 64x Baud Rate		3		3		t_{CY}
t_{TxRDY}	TxRDY Pin Delay from Center of Last Bit	Note 7		8		8	t_{CY}
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$	Note 7		400		6	t_{CY}
t_{RxRDY}	RxRDY Pin Delay from Center of Last Bit	Note 7		26		24	t_{CY}
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$	Note 7		400		6	t_{CY}
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$	Note 7		26		24	t_{CY}
t_{ES}	External SYNDET Setup Time After Rising Edge of $\overline{RxC}$	Note 7	18		16		t_{CY}
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Last Bit	Note 7	20		20		t_{CY}
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)	Note 7	8		8		t_{CY}
t_{CR}	Control to READ Setup Time ($\overline{DSR}$, $\overline{CTS}$)	Note 7	20		20		t_{CY}

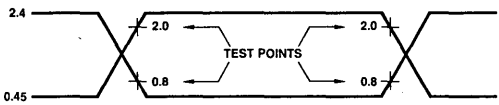
Notes:
1. AC timings measured V_{OH} = 2.0 V_{OL} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Chip Select (CS) and Command/Data (C/D) are considered as Addresses.
3. Assumes that Address is valid before R_D↓.
4. This recovery time is for after a Mode Instruction only. Write Data is allowed only when TxRDY = 1. Recovery time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$: For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$.
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE – pF



04133A-3

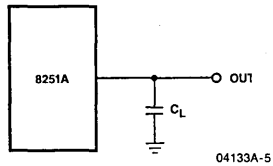
AC TESTING INPUT, OUTPUT WAVEFORM



04133A-4

AC testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

AC TESTING LOAD CIRCUIT

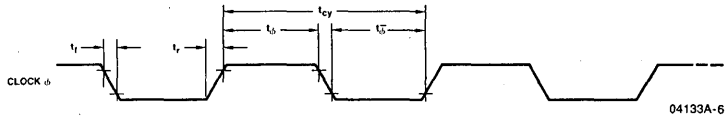


04133A-5

C_L = 150pF

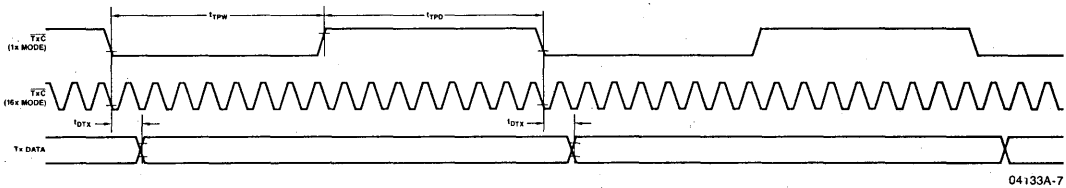
WAVEFORMS

SYSTEM CLOCK INPUT



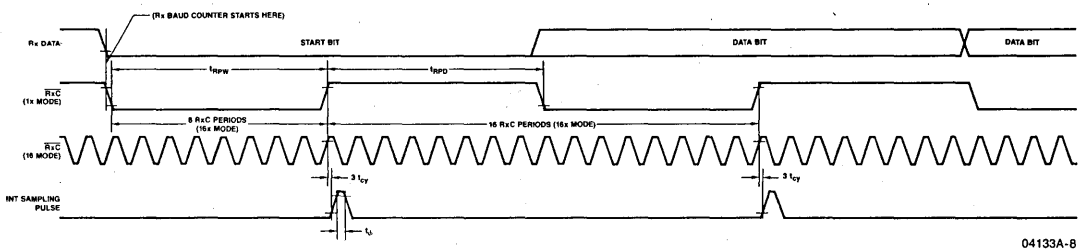
04133A-6

TRANSMITTER CLOCK AND DATA



04133A-7

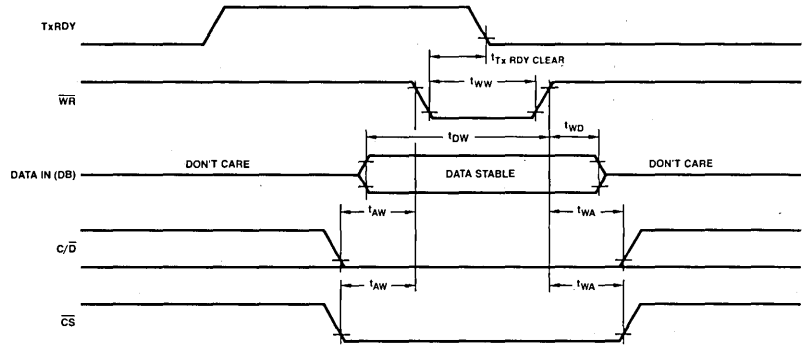
RECEIVER CLOCK AND DATA



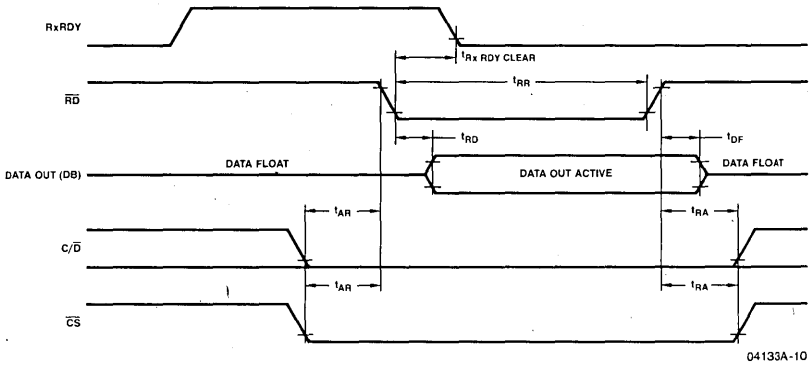
04133A-8

WAVEFORMS (Cont.)

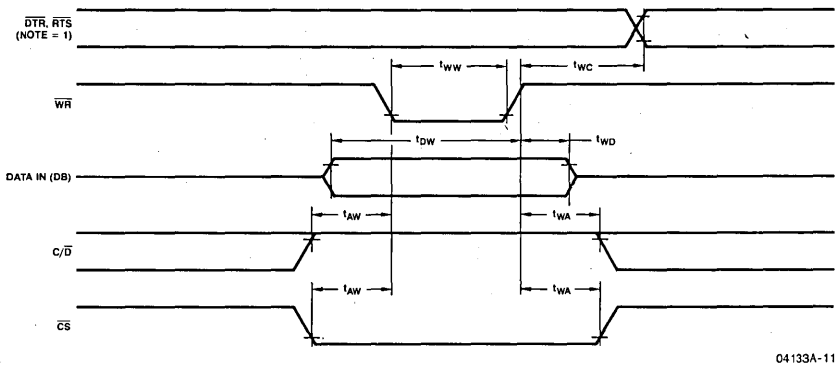
WRITE DATA CYCLE (CPU → USART)



READ DATA CYCLE (CPU ← USART)

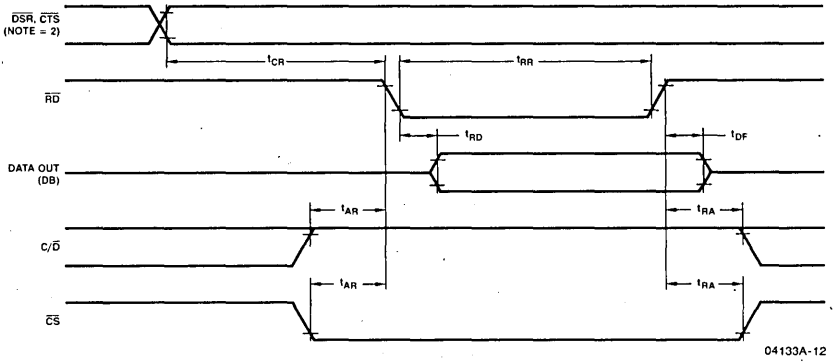


WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → USART)



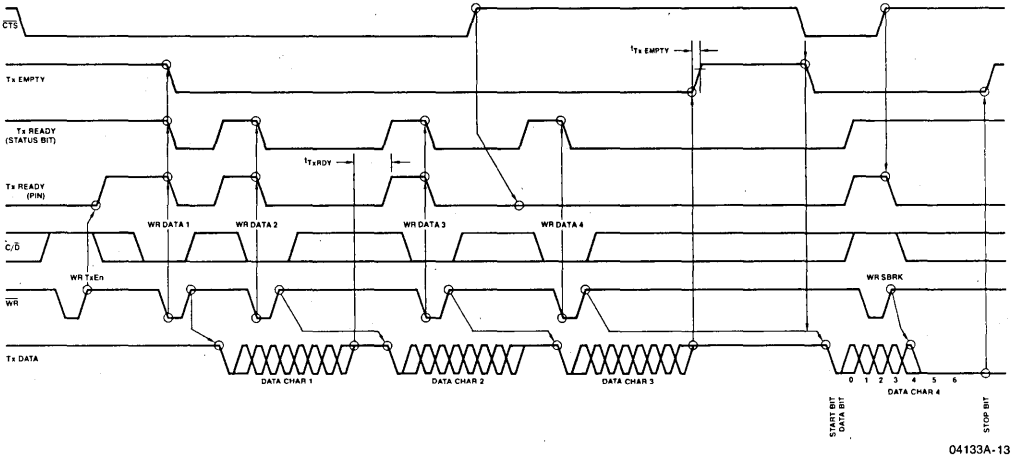
WAVEFORMS (Cont.)

READ CONTROL OR INPUT PORT (CPU ↓ USART)



Notes: 1. T_{WC} includes the response timing of a control byte.
2. T_{CR} includes the effect of CTS on the TxENable circuitry.

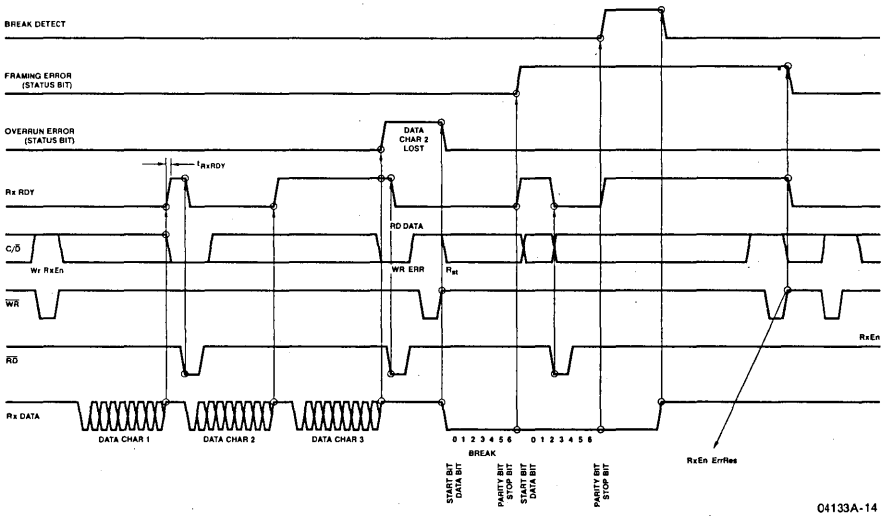
TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE)



Example format = 7 bit character with parity and 2 stop bits.

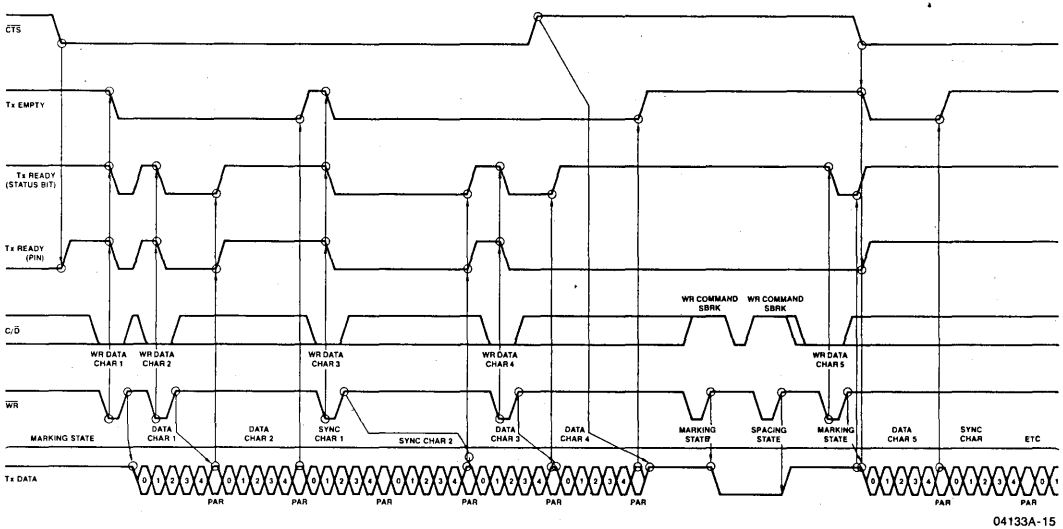
WAVEFORMS (Cont.)

RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



Example Format = 7 bit character with parity and 2 stop bits.

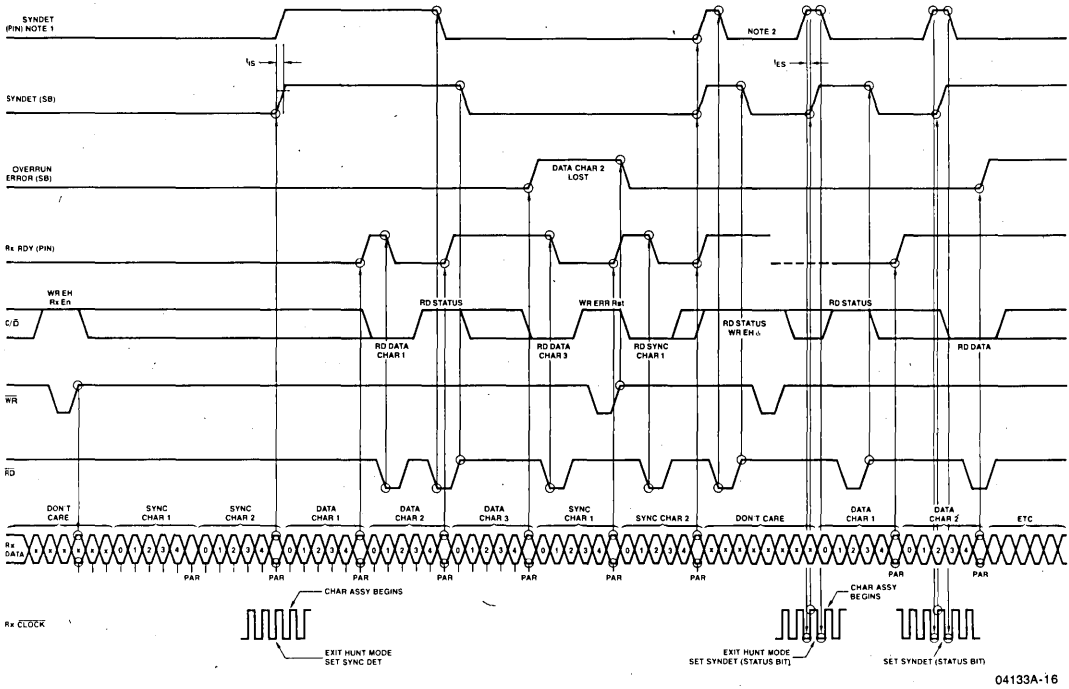
TRANSMITTER·CONTROL AND FLAG TIMING (SYNC MODE)



Example Format = 5 bit character with parity, 2 sync characters.

WAVEFORMS (Cont.)

RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)



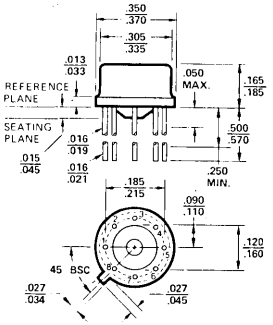
Notes: 1. Internal sync, 2 sync characters, 5 bits, with parity.
2. External sync, 5 bits, with parity.

Section X

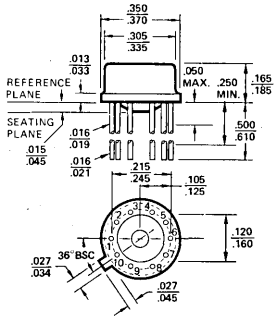
Package Outlines

METAL CAN PACKAGES

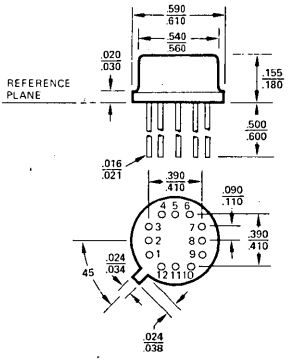
H-8-1



H-10-1



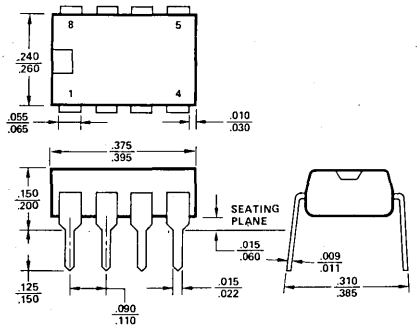
G-12-1



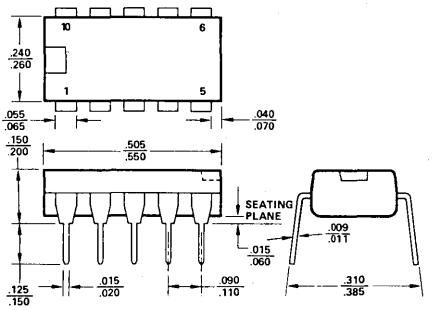
Note. Standard lead finish is bright acid tin plate or gold plate.

MOLDED DUAL IN-LINE PACKAGES

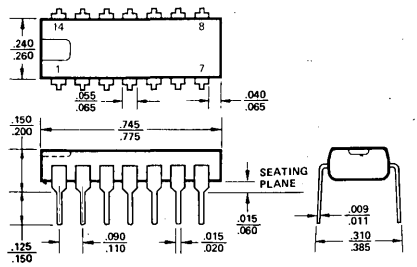
P-8-1



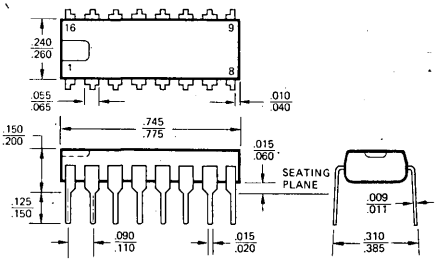
P-10-1



P-14-1



P-16-1



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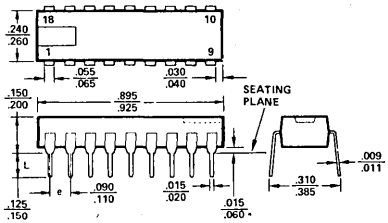
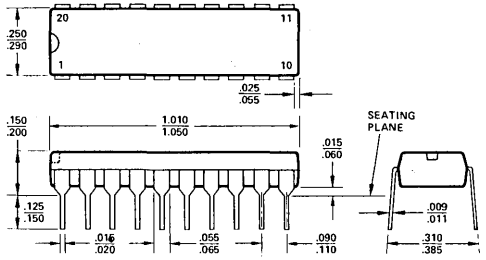
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES (Cont.)

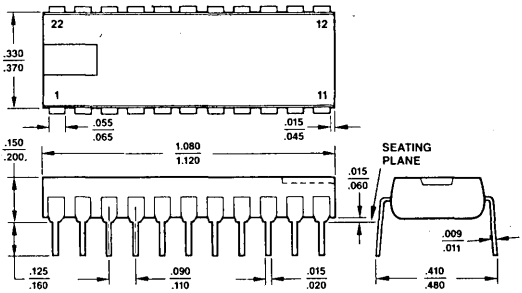
P-18-1



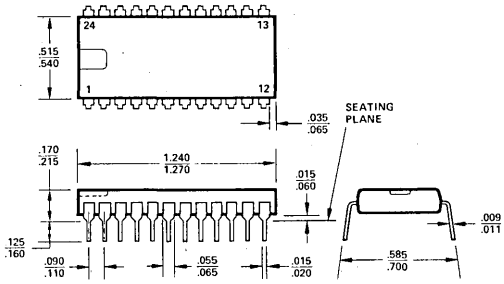
P-20-1



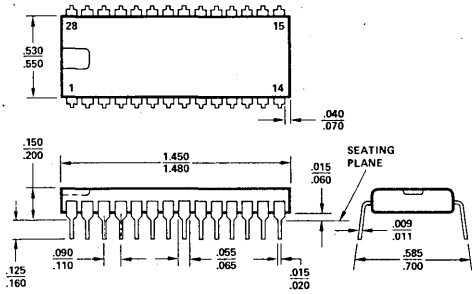
P-22-1



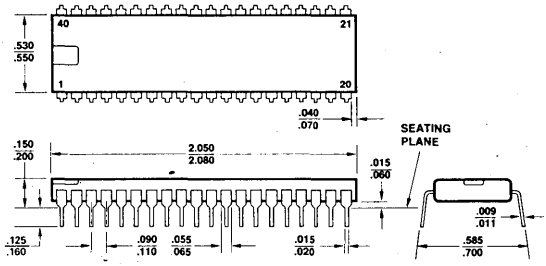
P-24-1



P-28-1



P-40-1

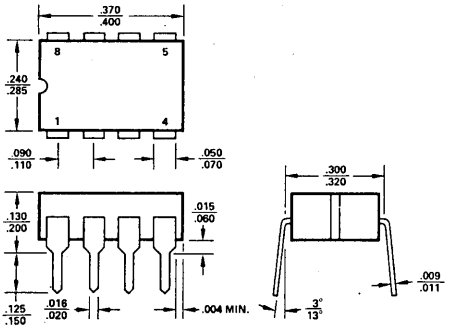


Note . Standard lead finish is tin plate or solder dip.

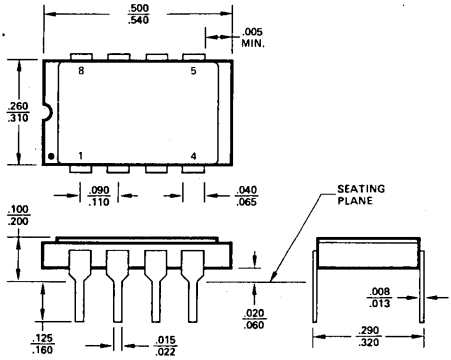
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

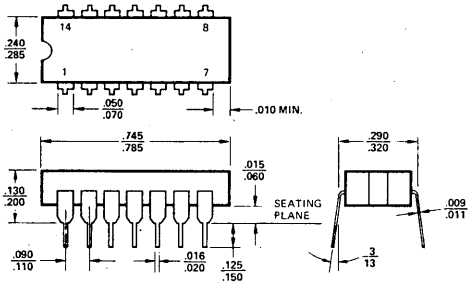
D-8-1



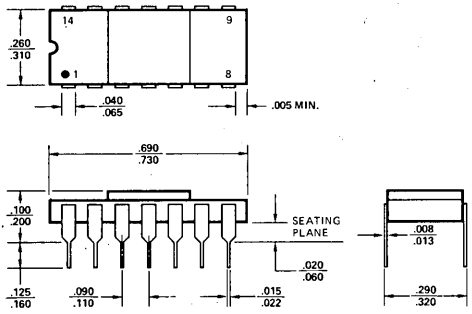
D-8-2



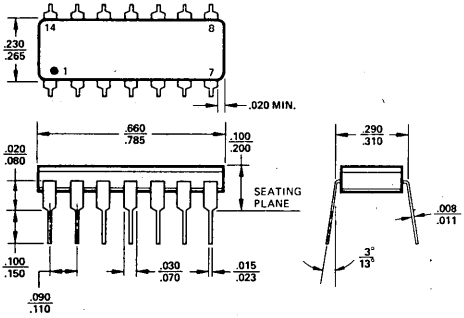
D-14-1



D-14-2



D-14-3

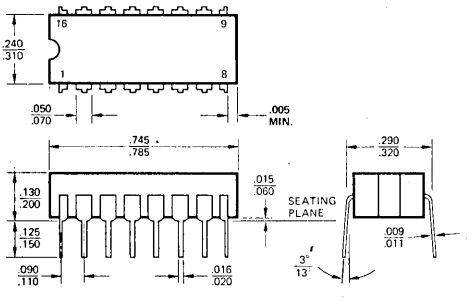


10

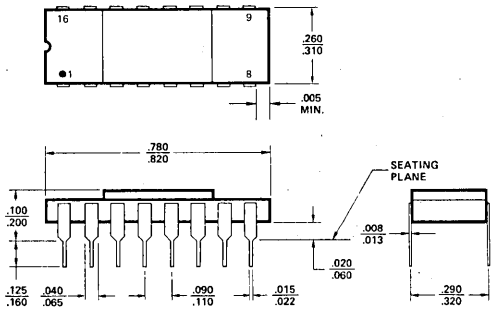
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

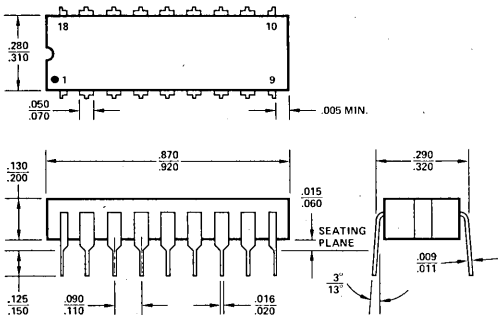
D-16-1



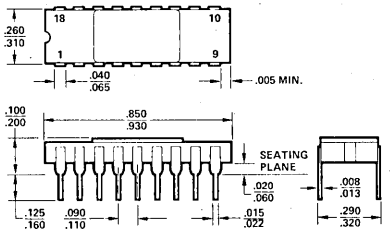
D-16-2



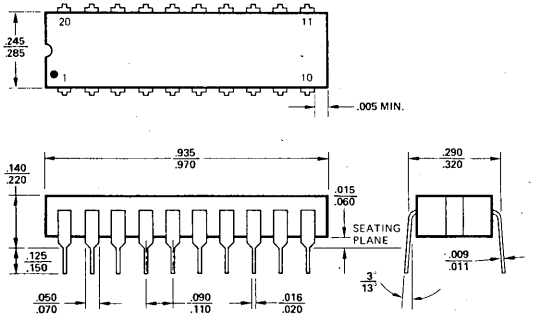
D-18-1



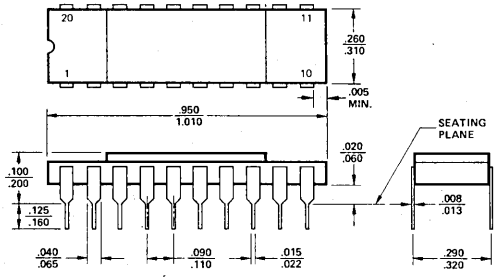
D-18-2



D-20-1



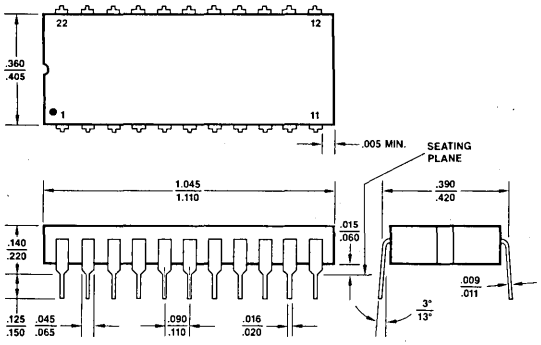
D-20-2



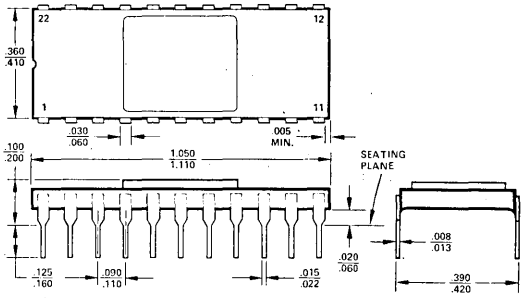
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

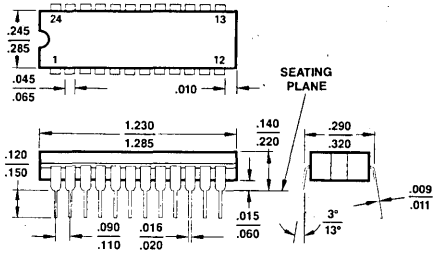
D-22-1



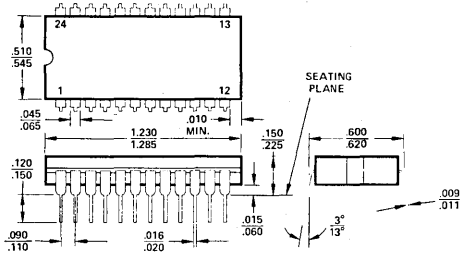
D-22-2



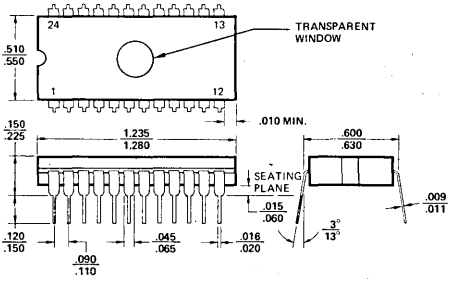
D-24-SLIM



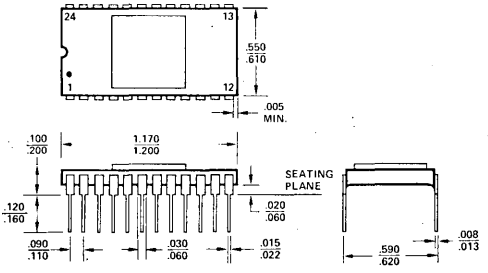
D-24-1 and D-24-4



D-24-4*



D-24-2

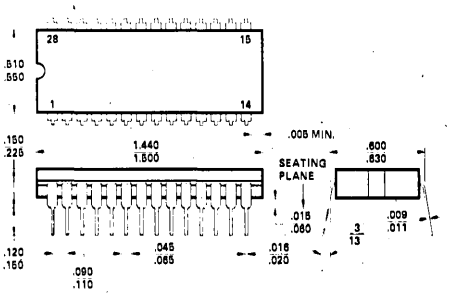


10

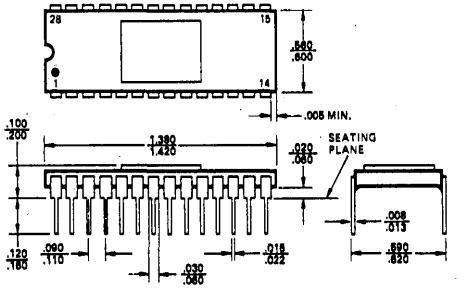
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

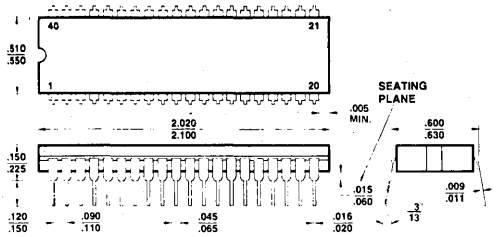
D-28-1



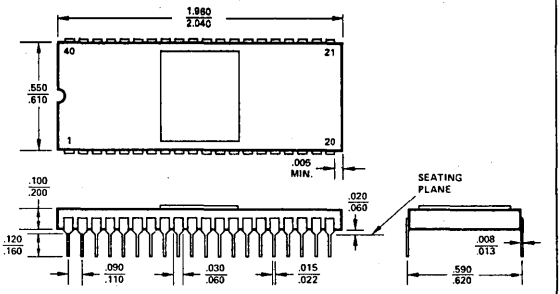
D-28-2



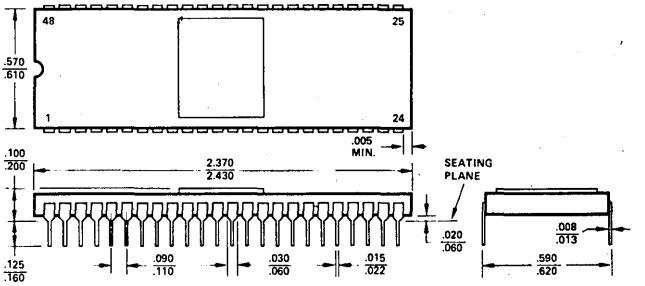
D-40-1



D-40-2



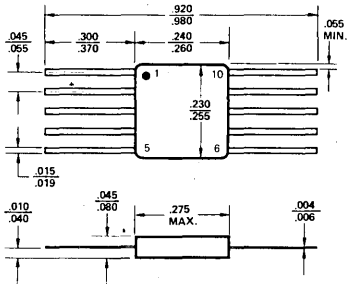
D-48-2



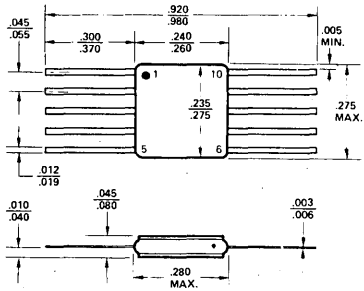
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

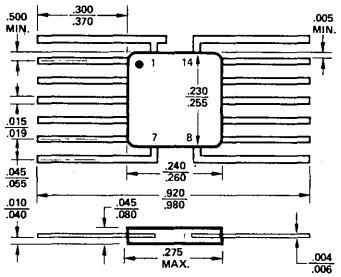
F-10-1



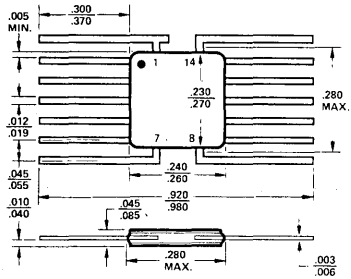
F-10-2



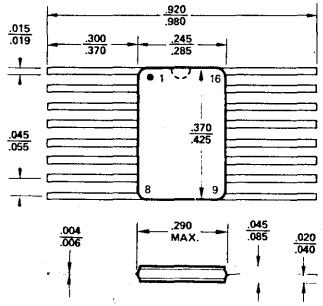
F-14-1



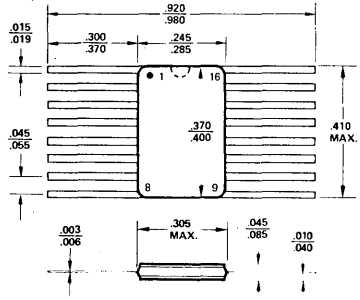
F-14-2



F-16-1

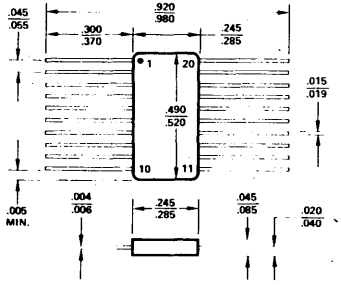


F-16-2

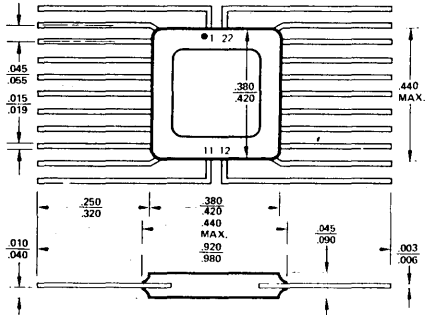


Note: Notch is pin 1 index on cerpack.

F-20-1



F-22-1

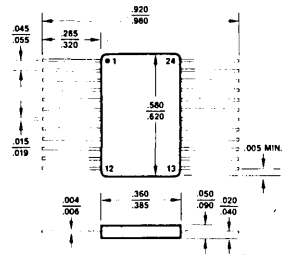


10

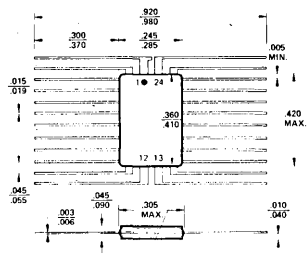
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES (Cont.)

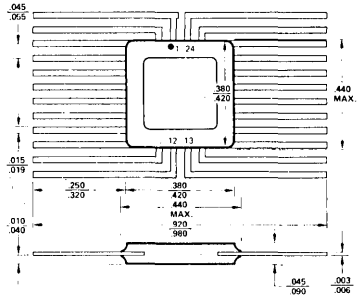
F-24-1



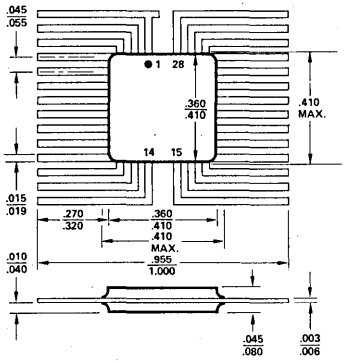
F-24-2



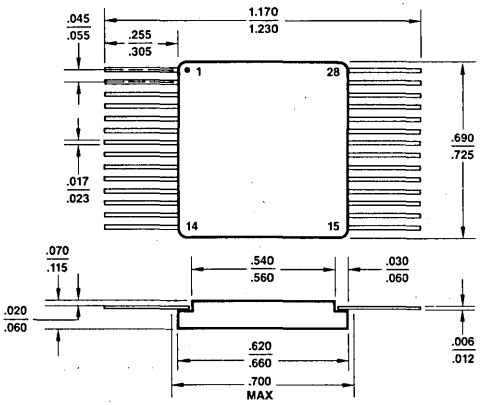
F-24-3



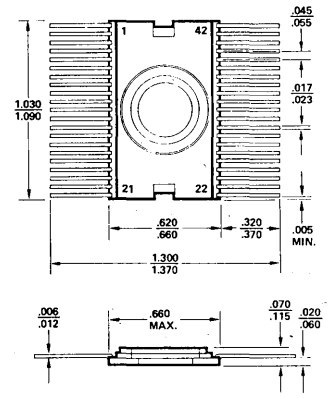
F-28-1



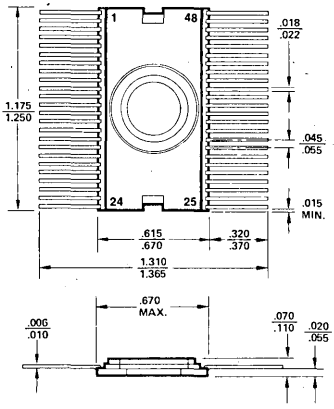
F-28-2 and F-28-3



F-42-1



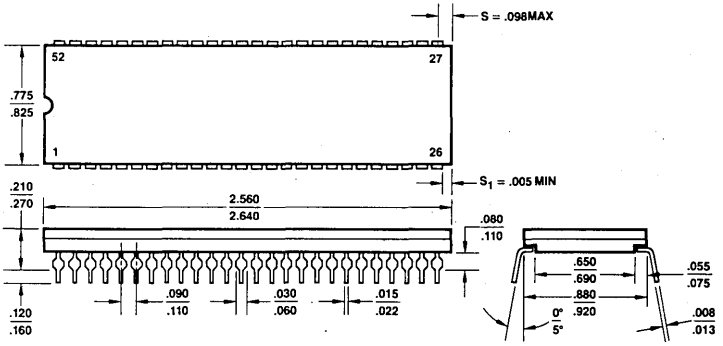
F-48-2



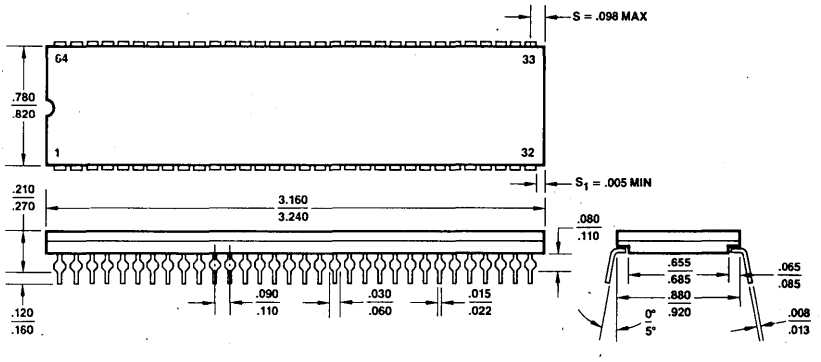
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

D-52-3



D-64-3

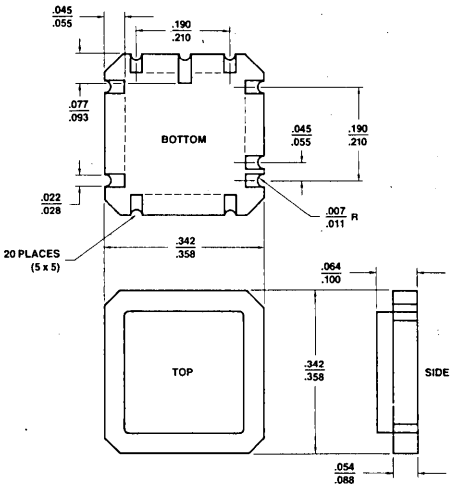


10

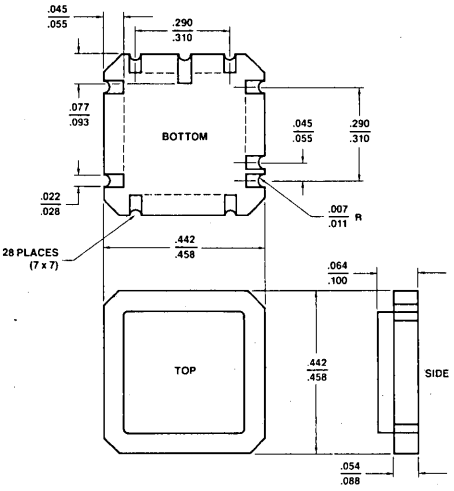
PACKAGE OUTLINES (Cont.)

SQUARE CHIP CARRIER FAMILY

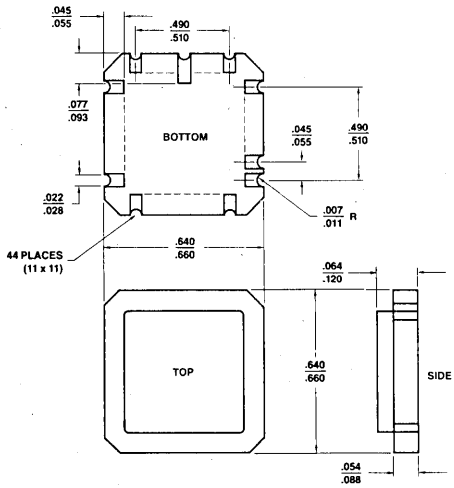
L-20-1



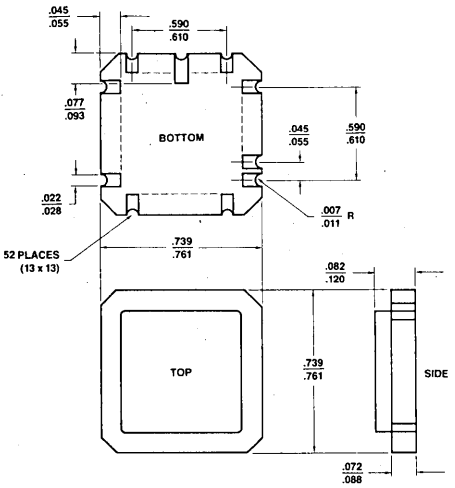
L-28-1



L-44-1



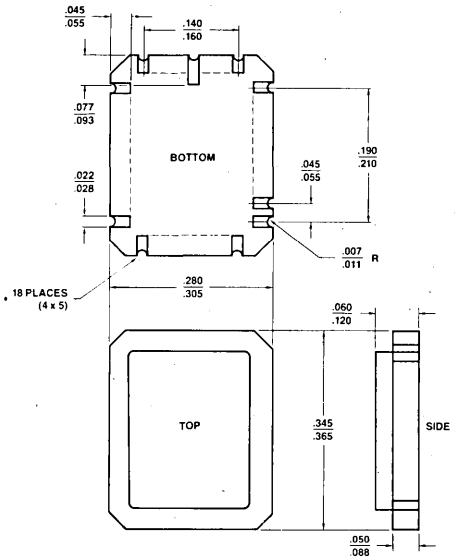
L-52-1



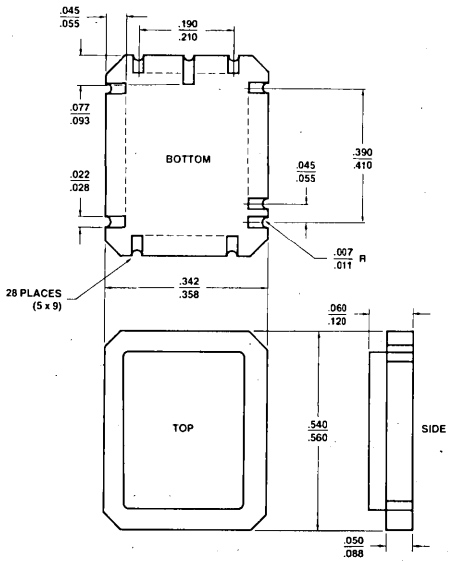
PACKAGE OUTLINES (Cont.)

RECTANGULAR CHIP CARRIER FAMILY

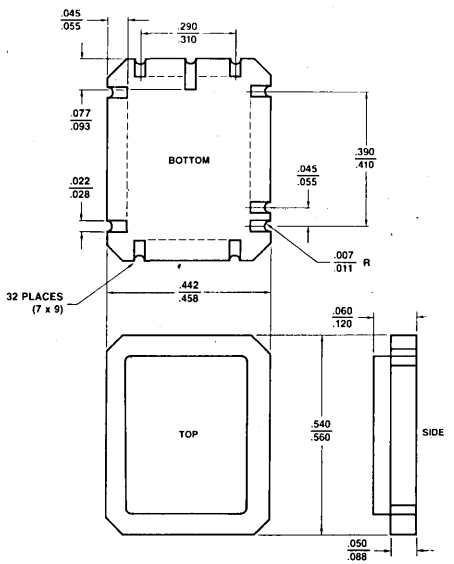
L-18-2



L-28-2



L-32-2



Glossary

Acquisition Time (S/H)
The time required for the hold capacitor to be charged to a percentage of full scale after the sample command is given. (μs)

Aperture Delay Time (S/H)
The time elapsed between the hold command and the actual opening of the switch. (ns)

Aperture Jitter (S/H)
The variation in aperture delay time from sample to sample. (ps)

Average Temperature Coefficient of Input Offset Current
The ratio of the change in input offset current over the operating temperature range. (pA/°C)

Average Temperature Coefficient of Input Offset Voltage
The ratio of the change in input offset voltage over the operating temperature range. (μV/°C)

Bandwidth
The width of the frequency range at which the gain of the device is 3dB below its maximum. (MHz)

Bipolar Offset Error (ADC)
Difference between the ideal (1/2FSR − 1/2LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 . . . . 11 to 10 . . . . 00).

Clamped Output High Voltage
The voltage necessary to turn on (forward bias) the clamping diode on the output pin. (V)

Clamped Output Low Voltage
The voltage necessary to turn off (reverse bias) the clamping diode on the output pin. (V)

Common Mode Gain
The ratio of the output voltage change to the input common mode voltage producing that change.

Common Mode Input Overload Recovery Time
The time delay between the removal of an overrange common mode input voltage, and resumption of normal device operation. (ns)

Common Mode Input Resistance
The value of resistance seen when looking into both inputs. (Ω)

Common Mode Input Voltage Swing
The peak value of the common mode input voltage at which the device will operate in a linear fashion. (V)

Common Mode Output Voltage
The output voltage resulting from the application of a voltage common to both inputs, and the average of the two output voltages of a differential output amplifier. (V)

Common Mode Rejection Ratio
The ratio of the change in input offset voltage to the total change in common mode voltage producing it. (dB)

Common Mode Voltage
The arithmetic mean of the voltage present at the differential inputs with respect to the device ground reference. (V)

Conversion Time (ADC)
The measure of the length of time required by an ADC to arrive at the correct digital output code, measured from the clock edge that starts a conversion to the edge of the status line ($\overline{CC}$) which signifies that the conversion is completed. (μs)

Differential Input Bias Current
The current required in the differential input stage into operation. (nA)

Differential Input Capacitance
The effective capacitance between the two inputs, with the amplifier operating in an open-loop configuration. (pF)

Differential Input Impedance
The impedance seen looking between the input terminals. (MΩ)

Differential Input Offset Current
The difference in currents required by the transistors in the input stage to bias the input stage to its quiescent operation point. (nA)

Differential Input Overload Recovery Time
The time delay between the removal of an overrange differential input voltage, and resumption of normal device operation. (ns)

Differential Input Resistance
The effective resistance between the two inputs with the amplifier operating in an open-loop configuration. (MΩ)

Differential Input Threshold Voltage
The voltage difference between the + and − inputs required to guarantee the output logic state. (V)

Differential Input Voltage Range
The range of applied input voltage for which operation remains within specifications. (V)

Differential Nonlinearity (ADC)
The deviation between the actual code width of an ADC from the ideal code width. The code width is defined as the range of analog input value which produces a given digital output code. An ideal value of a code width is equivalent to FSR/2^n, where n is the number of bits.

Differential Nonlinearity (DAC)
The maximum deviation of the analog output between any two adjacent output states from the ideal value. Converters with differential nonlinearity errors greater than ±1LSB may still be monotonic.

Differential Output Resistance
The resistance measured between the two output terminals. (MΩ)

Differential Output Voltage Swing
The peak differential output voltage that can be obtained without clipping the output voltage waveform. (V)

Differential Voltage Gain
The ratio of the change in differential output voltage to the change in differential input voltage.

Droop Rate (S/H)
The rate at which the output voltage changes while in the hold mode. Droop is caused by the capacitor being discharged through the buffer amplifier. (μV/μs)

Enable HIGH
The time required for the output to change from three-state high-impedance to HIGH after a control input change. (ns)

Enable LOW
The time required for the output to change from three-state high-impedance to LOW after a control input change. (ns)

GLOSSARY (Cont.)

Equivalent Input Noise Current
The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance. (pA/$\sqrt{Hz}$)

Equivalent Input Noise Voltage
The input noise voltage that would reproduce the noise seen at the output if all amplifier noise sources and the source resistance were set to zero. (nV/$\sqrt{Hz}$)

Feedback Sense Voltage
The voltage measured on the feedback terminal of the regulator, when the device is operating in regulation. (V)

Frequency Response
The width of the frequency range between the two points at which the gain of the device is 3dB below its maximum. (MHz)

Gain Bandwidth Product
The frequency at which the small signal AC gain of the device reduces to unity. (MHz)

Gain Error (ADC)
The difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain and the ideal gain of FS-2LSB.

Gain Error (DAC)
The difference between the actual analog output range and the ideal analog output range. Gain error is expressed as a percentage of full scale LSBs.

High Frequency Current Gain
The small signal AC current at a specified frequency. (mA/μA)

HIGH to Disable
The time required for the output to change from HIGH to three-state high-impedance after a control input change.

Hold Settling Time (S/H)
The time required for the buffer output to settle within the specified accuracy band after the switch is opened.

Hold Step Error
The voltage step at the output of the sample and hold from sample mode with a steady (DC) analog input voltage. (mV)

Hold Time
The time a signal must be retained at one input after an active transition occurs at another input terminal. (ns)

Hysteresis
The voltage difference between the switching points of the device. Also called Threshold Voltage.

Inherent Quantization Error (ADC)
Quantization Error is a direct consequence of the resolution of the ADC. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent $\pm$1/2LSB conversion error, even for a perfect ADC.

Input Bias Current
The average of the two input currents with no signal applied. (nA or pA)

Input Bias Current Drift
The change in input bias current with temperature, supply voltage or time.

Input Capacitance
The equivalent capacitance of either input with the other input grounded. (pF)

Input Common Mode Voltage Range
The range of common mode input voltage over which the device will operate within specifications. (V)

Input Current at Maximum Input Voltage
The current which flows when the absolute maximum allowed input voltage is applied to the input. (mA)

Input Forward Current
See Input LOW Current.

Input Noise Voltage
The rms noise voltage present at the amplifier output divided by the gain of the amplifier, measured with the inputs connected to ground through a low resistance. (nV/$\sqrt{Hz}$)

Input Offset Current
The difference in current into the two input terminals with the output voltage at zero. In a comparator, it is the difference between the two input currents with the output at the logic threshold voltage. Also, it is defined as the difference in input currents required to give equal output currents from a matched pair of devices. (nA or pA)

Input Offset Current Drift
The change in input offset current produced with time, voltage or temperature.

Input Offset Voltage
The voltage applied between the input terminals to obtain zero output voltage. In Comparators, it is the voltage applied to the input terminals to give the logic threshold voltage at the output. It is also defined as the input voltage differential required to give equal output currents from a matched pair of devices. (mV)

Input Offset Voltage Drift
The change in input offset voltage with time, voltage or temperature.

Input-Output Voltage Differential
The voltage range between the unregulated input voltage and the regulated output voltage in which a regulator operates within specifications.

Input Resistance
The equivalent resistance seen looking into either input terminal with the other terminal grounded. (MΩ)

Large Signal Voltage Gain
The ratio of the output voltage swing to the change in input voltage. (V/mV)

Line Regulation (PSC)
The change in output voltage for a specified change in input voltage. (mV or %)

Load Regulation (PSC)
The change in output voltage for a specified change in load current. (mV or %)

LOW to Disable
The time required for an output to change from a LOW-level to a three-state high-impedance after a control input change. (ns)

GLOSSARY (Cont.)

Monotonicity (ADC)
Monotonicity is a property of the DAC within a successive approximation (S/A) ADC. Each increment in the digital code to the DAC is translated into an analog output that is greater than, or equal to, that of the preceding code. Monotonicity of the DAC is a necessary requirement for a S/A ADC to have no missing codes.

Monotonicity (DAC)
Monotonicity is a property of the DAC output whereby each increment in the digital code is accomplished by an analog output that is greater than, or equal to that of the preceding code. Monotonicity is usually expressed in number of bits.

Negative Current
Current flowing out of the device. (mA)

Noise Figure
The ratio of the input signal-to-noise ratio to the output signal-to-noise ratio. Usually expressed as common log. (dB)

1/F Noise
The noise measured at a specified low frequency below the frequency range where the device noise spectrum is essentially flat. (nV)

Nonlinearity Error (DAC)
Maximum deviation from straight line drawn between the end points, zero and full scale outputs, expressed as a percentage of full-scale range or LSBs.

Open Loop Voltage Gain
The ratio of the output signal voltage to the differential input signal voltage, with no feedback applied. (dB or V/mV)

Oscillator Pull-In Range
The range of free-running frequency over which the oscillator can be locked to the incoming signal.

Output Common Mode Voltage
The arithmetic mean of the two output voltages for devices with differential outputs.

Output Impedance
The equivalent impedance seen looking into the output terminal. (Ω)

Output Leakage Current
The leakage current into the output transistor at the specified output voltage for uncommitted or open-collector outputs. (μA)

Output Noise Voltage
The rms value of the noise voltage measured at the output with constant load current and no input ripple. (μV)

Output Offset Voltage
The voltage difference between the two outputs with both inputs grounded. (V)

Output Resistance
The small signal AC resistance seen looking into the output with no feedback applied and the output DC voltage near zero. For comparators, it is the resistance seen looking into the output with the DC output level at the logic threshold. (Ω)

Output Saturation Voltage
The DC voltage between output and ground when the device is in the saturated condition. (V)

Output Short Circuit Current
The current flowing out of an output when that output is short circuited to ground. (mA)

Output Sink Current
The maximum current into the collector of an open-collector device. (mA)

Output Voltage Compliance (DAC)
The voltage range over which a current output DAC can be moved and maintain specified accuracy. (V)

Output Voltage Range
The range of output voltages over which the specifications apply. (V)

Output Voltage Swing
The peak output voltage swing that can be obtained without clipping the output voltage waveform. (V)

Overshoot
The difference between the peak amplitude of the output and the final value of the output divided by the output times 100%. (%)

Peak Output Current
The maximum current delivered by the device for a period too short for thermal protection to be activated. (A)

Phase Margin
The difference between the phase shift at the frequency where the open loop gain equals unity and 180°. (°)

Pulse Width
The time between the leading and trailing edges of a pulse. (ns)

Power Bandwidth
The maximum frequency at which the maximum output can be maintained without significant distortion.

Power Dissipation (Max)
The maximum power that can be dissipated with a given heat sink. (mW)

Power Supply Current
The current required from the power supply to operate a device with no load and no signal applied. (mA)

Power Supply Rejection Ratio
The ratio of the change in input offset voltage to the change in power supply voltage. (μV/V)

Power Supply Sensitivity
The ratio of the change of a specified parameter to the change in supply voltage.

Propagation Delay
The time interval between application of an input signal and a subsequent output change. (ns)

Quiescent Current
The amount of current drawn by a device with no signal applied to the input and no load. (mA)

Quiescent Output Current
The output current with no signal applied to the input. (mA)

Reference (Control) Current
The current drawn or supplied by the reference (control) terminal. (μA)

Resolution (ADC)
The number of possible analog input levels an ADC will resolve. Expressed as the number of output bits, or 1 part in 2^n where n is the number of bits.

GLOSSARY (Cont.)

Resolution (DAC)
The number of states (2^n) into which the full scale range may be divided or resolved, where n = numbers of bits. Generally expressed in number of bits.

Response Time
The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level. (ns)

Reverse Recovery Time
The time taken for the reverse recovery current to fall to a specified value after removal of the reverse bias. (ns)

Ripple Rejection
The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage. (dB)

Rise Time
The time interval required for a signal to rise from 10% to 90% of its final amplitude. (ns or μs)

Sample-to-Hold Offset Error (S/H)
The difference in output voltage between the time the hold command is given and the time the output settles to its final value. It is caused by charge injection from the switch to the capacitor during the opening of the switch.

Settling Time
The time from a step change of input to the time the corresponding output settles to within a specified percentage of the final value. (ns)

Set-Up Time
The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

Short-Circuit Current Limit
The output current with the output shorted to ground. (mA)

Short-Circuit Load Current
The maximum output current which the device will provide into a short-circuit.

Slew Rate
The maximum rate of change of output under large signal conditions. (V/μs)

Standby Current Drain
(see Quiescent Current.)

Storage Time
The propagation delay due to stored charges within the device. (ns)

Supply Current
The current flowing into the supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

Supply Regulation
The change in internal device supply voltage for a specified change in external power supply voltage.

Supply Voltage
The range of power supply over which the device is guaranteed to operate within the specified limits. (V)

Supply Voltage Rejection Ratio
See Power Supply Rejection.

Switching Speed
See Propagation Delay.

Temperature Coefficient
See Average Temperature Coefficient of specific parameter.

Temperature Stability
The percentage change in output voltage over a specified temperature range (V/°C)

Threshold Voltage
The input voltage required to force the output logic level to change state. (V)

Toggle Frequency/Operating Frequency
The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

Total Harmonic Distortion
The rms value of the harmonic content of a signal expressed as a percentage of the rms value of its fundamental.

Transient Response
The closed loop step function response of the circuit under small conditions.

Unipolar Offset Error
The difference between the ideal (+1/2LSB) and the actual analog input level required to produce the first digital code transition (00 . . . . 00 to 00 . . . . 01) over the complete temperature range.

Unity Gain Bandwidth
The frequency at which the open loop gain is reduced to unity. (MHz)

Voltage Gain
The ratio of the output voltage to the input voltage under small signal conditions. For comparators, it is the ratio of the change in output voltage to the change in voltage between the input terminals, with the DC output in the vicinity of the logic threshold. (dB or V/mV)

Zero Scale Error (DAC)
The measured analog current or voltage output when the digital input code corresponds to an analog value of zero. Zero scale error is usually expressed in units of current or voltage.

DICE POLICY

Advanced Micro Devices, interface and linear products are all available in dice form.

ELECTRICAL CHARACTERISTICS

Each die is electrically tested to the commercial or military grade DC parameters to guardbanded limits at 25°C to ensure performance over the temperature range.

QUALITY ASSURANCE

All dice are glass passivated with only the bonding pads exposed to provide scratch protection. All dice are provided without gold backing.

SHIPPING PACKAGES/ORDER INFORMATION

All dice are packaged in containers with individual compartments which prevent damage to the die during shipping.

Minimum order for AMD dice is 10 pcs.

SPECIAL CHIP PROCESSING

If there is a need for additional testing or processing, contact AMD for detailed information.

See following pages on ordering information for detail ordering number.

ORDERING INFORMATION (0 to +70°C)

Device Number*	Order Number					
	Metal Can	Hermetic DIP	Molded DIP	Leadless Chip-Pak	Flat Package	Dice
Microprocessor Peripheral Conversion Products						
Am6080		Am6080DC	Am6080PC	Am6080LC		Am6080XC
Am6080A		Am6080ADC	Am6080APC	Am6080ALC		Am6080AXC
Am6081		Am6081DC	Am6081PC			Am6081XC
Am6081A		Am6081ADC	Am6081APC			Am6081AXC
Am6082		Am6082DC	Am6082PC	Am6082LC*		Am6082XC**
Am6108		Am6108DC		Am6108LC*		Am6108XC**
Am6148		Am6148DC		Am6148LC*		Am6148XC**
Am6112		Am6112DC		Am6112LC*		Am6112XC**
Data Acquisition Products						
DAC-08		DAC-08CQ DAC-08EQ DAC-08HQ		DAC-08CL DAC-08EL DAC-08HL		DAC-08CX DAC-08EX DAC-08HX
Am1408		Am1408L8 Am1408L7 Am1408L6	Am1408N8 Am1408N7 Am1408N6			LD1408
SSS1408A		SSS1408A-8Q SSS1408A-7Q SSS1408A-6Q				
Am2502		Am2502DC	Am2502PC			Am2502XC
Am2503		Am2503DC	Am2503PC			Am2503XC
Am2504		Am2504DC	Am2504PC			Am2504XC
Am25L02		Am25L02DC	Am25L02PC			Am25L02XC
Am25L03		Am25L03DC	Am25L03PC			Am25L03XC
Am25L04		Am25L04DC	Am25L04PC			Am25L04XC
Am6012		Am6012DC	Am6012PC	Am6012LC		Am6012XC
Am6012A		Am6012ADC	Am6012APC	Am6012ALC		Am6012AXC
Am6014		Am6014DC				Am6014XC
Am6022		Am6022DC	Am6022PC	Am6022LC*		Am6022XC
Am6070		Am6070DC				Am6070XC
Am6070A		Am6070ADC				Am6070AXC
Am6072		Am6072DC				Am6072XC

*Availability of leadless packages for these devices will be announced.
**Availability of dice to be announced.

ORDERING INFORMATION (0 to +70°C)

Device Number*	Order Number					
	Metal Can	Hermetic DIP	Molded DIP	Leadless Chip-Pak	Flat Package	Dice
Sample and Holds						
LF198	LF398H		LF398N	LF398L*		LD398
Am6420		Am6420DC		Am6420LC*		
Operational Amplifiers						
LM108	LM308H	LM308D	LM308N	LM308L		LD308
LM108A	LM308AH	LM308AD	LM308AN	LM308AL		LD308A
LM118	LM318H	LM318D	LM318N	LM318L	LM318F	LD318
LM148		LM348D	LM348N	LM348L		LD348
LF155	LF355H					LD355
LF155A	LF355AH					LD355A
LF156	LF356H					LD356
LF156A	LF356AH					LD356A
LH2108		LH2308D				
LH2108A		LH2308AD				
Comparators						
LM111	LM311H	LM311D	LM311N	LM311L		LD311
LM119	LM319H	LM319D	LM319N	LM319L	LM319F	LD319
LM139		LM339D	LM339N	LM339L		LD339
LM139A		LM339AD	LM339AN	LM339AL		LD339A
Am686	Am686HC	Am686DC	Am686CN-1 Am686CN	Am686LC		Am686XC
Am1500		Am1500DC			Am1500FC	
LH2111		LH2311D			LH2311F	
Power Supply Controllers						
Am6300		Am6300DC	Am6300PC			
Am6301		Am6301DC	Am6301PC			

*Availability of leadless packages for these devices will be announced.

ORDERING INFORMATION (−25 to +85°C)

Device Number*	Order Number					
	Metal Can	Hermetic DIP	Molded DIP	Leadless Chip-Pak	Flat Package	Dice
Data Acquisition Products						
Am6606		Am6606DL-8 Am6606DL-7 Am6606DL-6				Am6606XL-6**
Am6688		Am6688DL-8 Am6688DL-7 Am6688DL-6				Am6688XL-6
Sample and Holds						
LF198	LF298H			LF298L*		
Operational Amplifiers						
LM108	LM208H	LM208D		LM208L	LM208F	
LM108A	LM208AH	LM208AD		LM208AL	LM208AF	
LM118	LM218H	LM218D		LM218L	LM218F	
LM148		LM248D		LM248L		
LF155	LF255H					
LF155A	LF255AH					
LF156	LF256H					
LF156A	LF256AH					
LH2108		LH2208D				
LH2108A		LH2208AD				
Comparators						
LM111	LM211H	LM211D		LM211L	LM211F	
LM119	LM219H	LM219D		LM211L	LM219F	
LM139		LM239D		LM239L		
LM139A		LM239AD		LM239AL		
Am685	Am685HL	Am685DL		Am685LL		Am685XL
Am687		Am687DL		Am687LL		Am687XL
Am687A		Am687ADL		Am687ALL		
Am1500		Am1500DL			Am1500FL	
LH2111		LH2211D			LH2211F	
Am6685	Am6685HL	Am6685DL				Am6685XL**
Am6687		Am6687DL				Am6687XL**
Power Supply Controllers						
Am6301		Am6301DL		Am6301LL*		

*Availability of leadless packages for these devices will be announced.
**Availability of dice to be announced.

ORDERING INFORMATION (−55 to +125°C)

Device Number*	Order Number					
	Metal Can	Hermetic DIP	Molded DIP	Leadless Chip-Pak	Flat Package	Dice
Microprocessor Peripheral Conversion Products						
Am6080		Am6080DM		Am6080LM		Am6080XM
Am6080A		Am6080ADM		Am6080ALM		Am6080AXM
Am6081		Am6081DM				Am6081XM
Am6081A		Am6081ADM				Am6081AXM
Am6082		Am6082DM		Am6082LM*		Am6082XM**
Am6108		Am6108DM		Am6108LM*		Am6108XM**
Am6148		Am6148DM		Am6148LM		Am6148XM**
Am6112		Am6112DM		Am6112LM*		Am6112XM**
Data Acquisition Products						
DAC-08		DAC-08Q		DAC-08L		DAC-08X
DAC-08A		DAC-08AQ		DAC-08AL		DAC-08AX
Am1408/ 1508		Am1508L8				CD1508
SSS1408A/ 1508A		SSS1508A-8Q				
Am2502		Am2502DM			Am2502FM	Am2502XM
Am2503		Am2503DM			Am2503FM	Am2503XM
Am2504		Am2504DM			Am2504FM	Am2504XM
Am25L02		Am25L02DM			Am25L02FM	Am25L02XM
Am25L03		Am25L03DM			Am25L03FM	Am25L03XM
Am25L04		Am25L04DM			Am25L04FM	Am25L04XM
Am6012		Am6012DM		Am6012LM		Am6012XM
Am6012A		Am6012ADM		Am6012ALM		Am6012AXM
Am6014		Am6014DM				
Am6022		Am6022DM		Am6022LM*		
Am6070		Am6070DM				Am6070XM
Am6070A		Am6070ADM				Am6070AXM
Am6072		Am6072DM				Am6072XM
Am6606		Am6606DM-8 Am6606DM-7 Am6606DM-6				Am6606XM-6**
Am6688		Am6688DM-8 Am6688DM-7 Am6688DM-6				Am6688XM-6

*Availability of leadless packages for these devices will be announced.
**Availability of dice to be announced.

ORDERING INFORMATION (−55 to +125°C)

Device Number*	Order Number					
	Metal Can	Hermetic DIP	Molded DIP	Leadless Chip-Pak	Flat Package	Dice
Sample and Holds						
LF198	LF198H			LF198L*		LD198
Am6420		Am6420DM		Am6420LM*		
Operational Amplifiers						
LM108	LM108H	LM108D		LM108L	LM108F	LD108
LM108A	LM108AH	LM108AD		LM108AL	LM108AF	LD108A
LM118	LM118H	LM118D		LM118L	LM118F	LD118
LM148		LM148D		LM148L		LD148
LF155	LF155H					LD155
LF155A	LF155AH					LD155A
LF156	LF156H					LD156
LF156A	LF156AH					LD156A
LH2108		LH2108D			LH2108F	
LH2108A		LH2108AD			LH2108AF	
Comparators						
LM111	LM111H	LM111D		LM111L	LM111F	LD111
LM119	LM119H	LM119D		LM119L	LM119F	LD119
LM139		LM139D		LM139L	LM139F	LD139
LM139A		LM139AD		LM139AL	LM139AF	LD139A
Am685	Am685HM	Am685DM		Am685LM		Am685XM
Am686	Am686HM	Am686DM		Am686LM		
Am687		Am687DM		Am687LM		Am687XM
Am687A		Am687ADM		Am687ALM		
Am1500		Am1500DM			Am1500FM	
LH2111		LH2111D			LH2111F	
Am6685	Am6685HM	Am6685DM				Am6685XM**
Am6687		Am6687DM				Am6687XM**
Power Supply Controllers						
Am6300		Am6300DM				
Am6301		Am6301DM				

**Availability of dice to be announced.

World-Wide Sales Offices

Advanced Micro Devices

Advanced Micro Devices maintains a network of representatives and distributors in the U.S. and around the world. For a sales agent nearest you, call one of the AMD offices listed below.

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