Bipolar/MOS Memories

1986 Data Book

ADVANCED MICRO DEVICES

Advanced Micro Devices

Bipolar/MOS Memories Data Book

The International Standard of Quality guarantees a 0.05% AQL on all electrical parameters, AC and DC, over the entire operating range.

INT·STD·500

901 Thompson Place, P.O. Box 3453, Sunnyvale, California 94088
(408) 732-2400 TWX: 910-339-9280 TELEX: 34-6306

ISSN 0888-4714

ADVANCE INFORMATION DATA SHEETS

This publication contains information which is intended to help you evaluate a proposed product under development at Advanced Micro Devices, Inc. AMD reserves the right at any time and without notice to discontinue work on this product or to make changes to the product. AMD assumes no responsibility for any errors which may appear in this publication and makes no commitment to update the information contained herein.

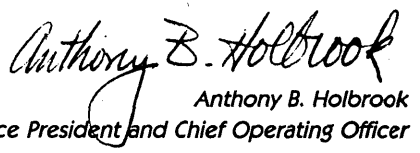
PRELIMINARY AND FINAL DATA SHEETS

Advanced Micro Devices reserves the right to make changes to its products at any time without notice, assumes no responsibility for any errors which may appear in this publication and makes no commitment to update the information contained herein. We recommend that you confirm the latest applicable product data through your local AMD sales office before placing your order.

ADVANCED INFORMATION, PRELIMINARY, FINAL DATA SHEETS

AMD further assumes no responsibility for the use of any of its products, conveys no license under any patent, copyright, trademark or other right, and makes no representations that the circuits or any illustrated applications are free from patent infringement or will be suitable for any particular use or purpose. Reference should be made to AMD's Standard Terms and Conditions of Sale for a complete statement of the terms, conditions and limitations applicable to AMD's limited product warranty and patent indemnity.

"Winning requires excellence in product design as well as in continuous innovation. At AMD, memory products are the technology drivers, the leading edge devices in the company's commitment to out-invent the competition."



Anthony B. Holbrook
Executive Vice President and Chief Operating Officer

Advanced Micro Devices, a leading innovator of semiconductors, has long recognized that memory technology leads the development of all other technologies. AMD's emphasis on memories is further enhanced by the company's dual-technology strengths in both bipolar and MOS (including CMOS).

In developing this array of premium memories, AMD has achieved impressive innovations. The architecture of the Am90C644 dual-array memory, built in one of AMD's advanced CMOS technologies, is optimized for high-performance video applications. The world's leading CMOS 1Mbit EPROM, the Am27C1024, is the result of AMD's unique CMOS process for UV-erasable, electrically programmable memories.

Not only does AMD provide memory products in state-of-the-art CMOS technologies, the company produces a broad spectrum of bipolar memories. The evolution of AMD's ion-implanted, oxide-isolated IMOX™ technology has led to the development of high-performance products with increased speed and density. The latest result of this process is the world's first 128K bipolar PROM, the Am27S51, with a 35ns access time.

To accommodate these continuing innovations in process technology, AMD now has two 6-inch wafer fabrication facilities in Austin, Texas, for CMOS production. San Antonio, Texas, is the site of the world's first 6-inch bipolar VLSI wafer fabrication plant. This fabrication area will concentrate on products in the most advanced IMOX technology.

To reduce system costs, AMD is introducing complex, high-lead-count, surface-mount devices in bipolar and MOS (including CMOS) technologies. These and other state-of-the-art packages also increase board density and decrease system delay times.

AMD also offers the industry's most stringent quality guarantee. Every AMD part is guaranteed to 500 ppm (parts per million) on all electrical parameters, over the entire operating range. The company's INT-STD-500 program ensures high quality in every product manufactured by AMD, for military, industrial, and commercial customers.

INTRODUCTION

NUMERICAL DEVICE INDEX

Bipolar PROM

Functional Index and Selection Guide

Listed according to organization and access time.

Part Number	APL	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Page No.
Am27S195A	✓	32 x 8	15/20	115/115	3S	16	D,P,F,L	2-63
Am27S18A	✓	32 x 8	25/35	115/115	OC	16	D,P,F,L	2-37
Am27S19A	✓	32 x 8	25/35	115/115	3S	16	D,P,F,L	2-37
Am27S18	✓	32 x 8	40/50	115/115	OC	16	D,P,F,L	2-37
Am27S19	✓	32 x 8	40/50	115/115	3S	16	D,P,F,L	2-37
Am27LS18[1]	✓	32 x 8	55/70	80/80	OC	16	D,P,F,L	2-37
Am27LS19[1]	✓	32 x 8	55/70	80/80	3S	16	D,P,F,L	2-37
Am27S20A	✓	256 x 4	30/40	130/130	OC	16	D,P,F,L	2-74
Am27S21A	✓	256 x 4	30/40	130/130	3S	16	D,P,F,L	2-74
Am27S20	✓	256 x 4	45/60	130/130	OC	16	D,P,F,L	2-74
Am27S21	✓	256 x 4	45/60	130/130	3S	16	D,P,F,L	2-74
Am27S12A	✓	512 x 4	30/40	130/130	OC	16	D,P,F,L	2-22
Am27S13A	✓	512 x 4	30/40	130/130	3S	16	D,P,F,L	2-22
Am27S12	✓	512 x 4	50/60	130/130	OC	16	D,P,F,L	2-22
Am27S13	✓	512 x 4	50/60	130/130	3S	16	D,P,F,L	2-22
Am27S28A	✓	512 x 8	35/45	160/160	OC	20	D,P,L	2-100
Am27S29A	✓	512 x 8	35/45	160/160	3S	20	D,P,L	2-100
Am27S31A	✓	512 x 8	35/45	175/175	3S	24	D,P,F,L	2-107
Am27S28	✓	512 x 8	55/70	160/160	OC	20	D,P,L	2-100
Am27S29	✓	512 x 8	55/70	160/160	3S	20	D,P,L	2-100
Am27S31	✓	512 x 8	55/70	175/175	3S	24	D,P,F,L	2-107
Am27S15	✓	512 x 8	60/90	175/185	3S	24	D,P,F,L	2-30
Am27S25SA	✓	512 x 8	37[2]/45[2]	185/185	3S	24	D,P,F,L	2-82
Am27S25	✓	512 x 8	77[2]/85[2]	185/185	3S	24[3]	D,P,F,L	2-82
Am27S25A	✓	512 x 8	50[2]/60[2]	185/185	3S	24[3]	D,P,F,L	2-82
Am27S27		512 x 8	82[2]/95[2]	185/185	3S	22[6]	D,P,L	2-92
Am10P14	✓	1024 x 4	10/15	−185[4]/−175[4]	3S	20	D,P	2-1
Am100P14	✓	1024 x 4	10/–	−180[4]/–	3S	20	D,P	2-1
Am10KP14	✓	1024 x 4	10/15	−185[4]/−175[4]	3S	24	D,P	2-1
Am27S32A	✓	1024 x 4	35/45	140/145	OC	18	D,P,F,L	2-114
Am27S33A	✓	1024 x 4	35/45	140/145	3S	18	D,P,F,L	2-114
Am27S32	✓	1024 x 4	55/70	140/145	OC	18	D,P,F,L	2-114
Am27S33	✓	1024 x 4	55/70	140/145	3S	18	D,P,F,L	2-114
Am27S65A	✓	1024 x 4	33[2]/40[2]	185/185	3S	24[3]	D,P,F,L	2-183
Am27S65	✓	1024 x 4	45[2]/55[2]	185/185	3S	24[3]	D,P,F,L	2-183
Am27S180A	✓	1024 x 8	35/50	185/185	OC	24	D,P,F,L	2-44
Am27S181A	✓	1024 x 8	35/50	185/185	3S	24	D,P,F,L	2-44
Am27S280A	✓	1024 x 8	35/50	185/185	OC	24[3]	D,P,F,L	2-44
Am27S281A	✓	1024 x 8	35/50	185/185	3S	24[3]	D,P,F,L	2-44
Am27PS181A	✓	1024 x 8	50/65	185/80[5]	3S	24	D,P,F,L	2-44
Am27PS281A	✓	1024 x 8	50/65	185/80[5]	3S	24	D,P,F,L	2-44
Am27S180	✓	1024 x 8	60/80	185/185	OC	24	D,P,F,L	2-44
Am27S181	✓	1024 x 8	60/80	185/185	3S	24	D,P,F,L	2-44
Am27S280	✓	1024 x 8	60/80	185/185	OC	24[3]	D,P,F,L	2-44
Am27S281	✓	1024 x 8	60/80	185/185	3S	24[3]	D,P,F,L	2-44
Am27PS281	✓	1024 x 8	65/75	185/80[5]	3S	24[3]	D,P,F,L	2-44
Am27S35A	✓	1024 x 8	55[2]/60[2]	185/185	3S	24[3]	D,P,F,L	2-121
Am27S37A	✓	1024 x 8	55[2]/60[2]	185/185	3S	24[3]	D,P,F,L	2-121

Bipolar PROM (Cont'd.)

Part Number	APL	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Page No.
Am27S35	✓	1024 x 8	65[2]/75[2]	185/185	3S	24[3]	D,P,F,L	2-121
Am27S37	✓	1024 x 8	65[2]/75[2]	185/185	3S	24[3]	D,P,F,L	2-121
Am27PS181	✓	1024 x 8	65/75	185/80[5]	3S	24	D,P,F,L	2-44
Am27S184A	✓	2048 x 4	35/45	150/150	OC	18	D,P,F,L	2-54
Am27S185A	✓	2048 x 4	35/45	150/150	3S	18	D,P,F,L	2-54
Am27S185	✓	2048 x 4	50/55	150/150	3S	18	D,P,F,L	2-54
Am27LS184	✓	2048 x 4	50/55	120/125	OC	18	D,P,F,L	2-54
Am27LS185	✓	2048 x 4	60/65	120/125	3S	18	D,P,F,L	2-54
Am27PS185	✓	2048 x 4	60/65	150/75[5]	3S	18	D,P,F,L	2-54
Am27S75A	✓	2048 x 4	37[2]/47[2]	185/185	3S	24[3]	D,P,F,L	2-197
Am27S75	✓	2048 x 4	45[2]/55[2]	185/185	3S	24[3]	D,P,F,L	2-197
Am27S191SA	✓	2048 x 8	20/30	185/185	3S	24	D,P,F,L	2-63
Am27S291SA	✓	2048 x 8	20/30	185/185	3S	24	D,P,F,L	2-63
Am27LS191A	✓	2048 x 8	35/45	90/90	3S	24	D,P,F,L	2-63
Am27LS291A	✓	2048 x 8	35/45	90/90	3S	24	D,P,F,L	2-63
Am27S190A	✓	2048 x 8	35/50	185/185	OC	24	D,P,F,L	2-63
Am27S191A	✓	2048 x 8	35/50	185/185	3S	24	D,P,F,L	2-63
Am27S290A	✓	2048 x 8	35/50	185/185	OC	24[3]	D,P,F,L	2-63
Am27S291A	✓	2048 x 8	35/50	185/185	3S	24[3]	D,P,F,L	2-63
Am27S190	✓	2048 x 8	50/65	185/185	OC	24	D,P,F,L	2-63
Am27S191	✓	2048 x 8	50/65	185/185	3S	24	D,P,F,L	2-63
Am27S290	✓	2048 x 8	50/65	185/185	OC	24[3]	D,P,F,L	2-63
Am27S291	✓	2048 x 8	50/65	185/185	3S	24[3]	D,P,F,L	2-63
Am27PS191	✓	2048 x 8	65/75	185/80[3]	3S	24	D,P,F,L	2-63
Am27PS291	✓	2048 x 8	65/75	185/80[5]	3S	24[3]	D,P,F,L	2-63
Am27S45SA	✓	2048 x 8	35[2]/40[2]	185/185	3S	24	D,P,F,L	2-148
Am27S47SA	✓	2048 x 8	35[2]/40[2]	185/185	3S	24	D,P,F,L	2-148
Am27S45A	✓	2048 x 8	60[2]/70[2]	185/185	3S	24[3]	D,P,L	2-148
Am27S47A	✓	2048 x 8	60[2]/70[2]	185/185	3S	24[3]	D,P,L	2-148
Am27S45	✓	2048 x 8	70[2]/80[2]	185/185	3S	24[3]	D,P,L	2-148
Am27S47	✓	2048 x 8	NA[2]	185/185	3S	24	D,P,L	2-148
Am100P44	✓	4096 x 4	15/–	NA	3S	20	D,P	2-8
Am10P44	✓	4096 x 4	15/20	–185[4]/–175[4]	3S	20	D,P	2-8
Am27S41A	✓	4096 x 4	35/50	165/170	3S	20	D,P,L	2-132
Am27PS41	✓	4096 x 4	50/65	170/85[5]	3S	20	D,P,L	2-132
Am27S41	✓	4096 x 4	50/65	165/170	3S	20	D,P,L	2-132
Am27S85A	✓	4096 x 4	39[2]/47[2]	185/185	3S	24[3]	D,P,F,L	2-211
Am27S85	✓	4096 x 4	50[2]/60[2]	185/185	3S	24[3]	D,P,F,L	2-211
Am27S43A	✓	4096 x 8	40/55	185	3S	24	D,P,F,L	2-141
Am27S43	✓	4096 x 8	55/65	185	3S	24	D,P,F,L	2-141
Am27S55A	✓	4096 x 8	30[2]/38[2]	175/180	3S	24[3]	D,P	2-173
Am27S55	✓	4096 x 8	38[2]/46[2]	175/180	3S	24[3]	D,P	2-173
Am27S95A	✓	8192 x 4	35[2]/43[2]	175/180	3S	28[6]	D,P	2-225
Am27S95	✓	8192 x 4	48[2]/55[2]	175/180	3S	28[6]	D,P	2-225
Am100P88	✓	8192 x 8	15/–	NA	3S	28	D,P	2-15
Am10P88	✓	8192 x 8	15/20	NA	3S	28	D,P	2-15
Am27S49A	✓	8192 x 8	40/55	190/190	3S	24	D,P,L	2-160
Am27S49-45	✓	8192 x 8	45/–	190/–	3S	24	D,P,F,L	2-160
Am27S49	✓	8192 x 8	55/65	190/190	3S	24	D,P,L	2-160
Am27S51A	✓	16,384 x 8	35/45	190/190	3S	28	D,P,F,L	2-166
Am27S51	✓	16,384 x 8	55/65	190/190	3S	28	D,P,F,L	2-166

Notes: 1. Replaces Am27LS08/09
2. Contains built-in pipeline registers. Cycle time includes clock setup and clock to output time.
3. 300-mil lateral pin spacing.
4. Power supply current specified as I_{EE} minimum.
5. I_{CC} are power up and power down current limits respectively.
6. 400 mil lateral pin spacing.

Bipolar MEMORY RAM

Functional Index and Selection Guide

BIPOLAR ECL RAM

Listed according to organization and access time.

Part Number	APL	Organization	Access Time COM'L/MIL* Max.	I_{EE} COM'L/MIL* Max.	ECL Series	Number of Pins	Packages	Page No.
Am10469		512 x 9	9.5**	-240	10K	24	D	3-16
Am100469		512 x 9	9.5**	-240	100K	24	D	3-16
Am100415A		1024 x 1	15	-150	100K	16	D,F	3-1
Am10415SA		1024 x 1	15/20	-150/-165	10K	16	D,F	3-7
Am100415		1024 x 1	20	-150	100K	16	D,F	3-1
Am10415A		1024 x 1	20/25	-150/-165	10K	16	D,F	3-7
Am10415		1024 x 1	35/40	-150/-165	10K	16	D,F	3-7
Am100474-10		1024 x 4	10	-230	100K	24	D,F	3-38
Am10474-10/-		1024 x 4	10/-	-230/-255	10K	24	D,F	3-44
Am100474-15		1024 x 4	15	-200	100K	24	D,F	3-38
Am10474-15/-		1024 x 4	15/20	-230	10K	24	D,F	3-44
Am100474-25		1024 x 4	25	-200	100K	24	D,F	3-38
Am10474-25/-		1024 x 4	25/30	-200	10K	24	D,F	3-44
Am100470SA		4096 x 1	15	-230	100K	18	D,F	3-23
Am10470SA		4096 x 1	15/20	-230/-255	10K	18	D,F	3-29
Am100470A		4096 x 1	25	-195	100K	18	D,F	3-23
Am10470A		4096 x 1	25/30	-200/-220	10K	18	D,F	3-29
Am100470		4096 x 1	35	-195	100K	18	D,F	3-23
Am10470		4096 x 1	35/40	-200/-220	10K	18	D,F	3-29
Am10480-15/-		16384 x 1	15/-	-220	10K	20	D,F,L	3-54
Am10480-25/-		16384 x 1	25/-	-200/-	10K	20	D,F,L	3-54
Am100480-15		16384 x 1	15	-220	100K	20	D,F,L	3-49
Am100480-25		16384 x 1	25	-200	100K	20	D,F,L	3-49

*10K ECL is available with full military temperature range (-55 to +125°C).
**T_{AVMV}-Address to MISS

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military -55°C to +125°C
E = Extended -55°C to +85°C or +100°C
I = Industrial -40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

BIPOLAR TTL RAM

Listed according to organization and access time.

Part Number	APL	Organization	Access Time COM'L/MIL Max.	I_{CC} COM'L/MIL Max.	Output	Number of Pins	Packages (Note 1)	Page No.
Am3101A		(See Am27S02)						
Am74/5489		(See Am3101)						
Am74/5489-1		(See Am3101-1)						
Am74/54S189		(See Am27S03)						
Am74/54S289		(See Am27S02)						
Am27S02A	✓	16 x 4	25/30	100/105	OC	16	D,P,F,L	3-85
Am27S03A	✓	16 x 4	25/30	100/105	3S	16	D,P,F,L	3-85
Am27S06A	✓	16 x 4	25/30	100/105	OC	16	D,P,F,L	3-101
Am27S07A	✓	16 x 4	25/30	100/105	3S	16	D,P,F,L	3-101
Am27S02	✓	16 x 4	35/50	100/105	OC	16	D,P,F,L	3-85
Am27S03	✓	16 x 4	35/50	100/105	3S	16	D,P,F,L	3-85
Am27S06	✓	16 x 4	35/50	100/105	OC	16	D,P,F,L	3-101
Am27S07	✓	16 x 4	35/50	100/105	3S	16	D,P,F,L	3-101
Am3101-1	✓	16 x 4	35/50	100/105	OC	16	D,P,F,L	3-117
Am3101	✓	16 x 4	50/60	100/105	OC	16	D,P,F,L	3-117
Am27LS02	✓	16 x 4	55/65	35/38	OC	16	D,P,F,L	3-77
Am27LS03	✓	16 x 4	55/65	35/38	3S	16	D,P,F,L	3-77
Am27LS06	✓	16 x 4	55/65	35/38	OC	16	D,P,F,L	3-93
Am27LS07	✓	16 x 4	55/65	35/38	3S	16	D,P,F,L	3-93
Am31L01-1	✓	16 x 4	55/65	35/38	OC	16	D,P,F,L	3-109
Am31L01	✓	16 x 4	80/90	35/38	OC	16	D,P,F,L	3-109
Am27LS00A	✓	256 x 1	35/45	115/115	3S	16	D,P,F,L	3-69
Am27LS01A	✓	256 x 1	35/45	115/115	OC	16	D,P,F,L	3-69
Am27LS00	✓	256 x 1	45/55	70/70	3S	16	D,P,F,L	3-69
Am27LS01	✓	256 x 1	45/55	70/70	OC	16	D,P,F,L	3-69
Am27LS00-1	✓	256 x 1	45/55	70/70	3S	16	D,P,F,L	3-69
Am27LS01-1	✓	256 x 1	45/55	70/70	OC	16	D,P,F,L	3-69
Am93412A		256 x 4	35/45	155/170	OC	22[3]	D,P,F,L	3-134
Am93422A		256 x 4	35/45	155/170	3S	22[3]	D,P,F,L	3-134
Am93L412A		256 x 4	45/55	80/90	OC	22[3]	D,P,F,L	3-125
Am93L422A		256 x 4	45/55	80/90	3S	22[3]	D,P,F,L	3-125
Am93412		256 x 4	45/60	155/170	OC	22[3]	D,P,F,L	3-134
Am93422		256 x 4	45/60	155/170	3S	22[3]	D,P,F,L	3-134
Am93L412		256 x 4	60/75	80/90	OC	22[3]	D,P,F,L	3-125
Am93L422		256 x 4	60/75	80/90	3S	22[3]	D,P,F,L	3-125
Am93469	✓	512 x 9	20/-	185	3S	24	D,F	3-161
Am2150	✓	512 x 9	20/-	185	OC/3S	24	D,F	3-62
Am93L469	✓	512 x 9	45/-	70	3S	24	D,P,F	3-158
Am21L50	✓	512 x 9	45/-	70	OC/3S	24	D,P,F	3-59
Am93415SA		1024 x 1	20/30	155/170	OC	16	D,P,F,L	3-150
Am93425SA		1024 x 1	20/30	155/170	3S	16	D,P,F,L	3-150
Am93415A		1024 x 1	30/40	155/170	OC	16	D,P,F,L	3-150
Am93425A		1024 x 1	30/40	155/170	3S	16	D,P,F,L	3-150
Am93415		1024 x 1	45	155	OC	16	D,P,F,L	3-150
Am93425		1024 x 1	45	155	3S	16	D,P,F,L	3-150
Am93L415A		1024 x 1	45/55	65/75	OC	16	D,P,F,L	3-143
Am93L425A		1024 x 1	45/55	65/75	3S	16	D,P,F,L	3-143
Am93L415		1024 x 1	60	65	0C	16	D,P,F,L	3-143
Am93L425		1024 x 1	60	65	3S	16	D,P,F,L	3-143

Temperature Ranges:
C = Commercial (0 to +70°C)
M = Military (−55 to +125°C)
E = Extended Commercial (−55 to +85°C or +100°C)
I = Industrial (−40 to +85°C)

Notes: 1. D = Ceramic DIP,P = Plastic DIP,F = Flatpack,L = Leadless Chip Carrier.
2. Complement of data in is available on the outputs in the write mode when both $\overline{CS}$ and $\overline{WE}$ are low.
3. Flatpack is 24 pin.

MOS Memory

Functional Index and Selection Guide

1K STATIC RAMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time (ns)	Power Dissipation (mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am9122-25		256 x 4	25	N/A	660	22	5	C	D,P	4-208
Am9122-35		256 x 4	35	N/A	660/743	22	5	C,M	D,P	4-208
Am91L22-35		256 x 4	35	N/A	440	22	5	C	D,P	4-208
Am91L22-45		256 x 4	45	N/A	440/495	22	5	C,M	D,P	4-208
Am9101D		256 x 4	250	47	330	22	5	C	D,P	4-164
Am9111D		256 x 4	250	47	330	18	5	C	D,P	4-176
Am9112D		256 x 4	250	47	330	16	5	C	D,P	4-188
Am9101C		256 x 4	300	47	330/358	22	5	C,M	D,P	4-164
Am9111C	✓	256 x 4	300	47	330/358	18	5	C,M	D,P	4-176
Am9112C	✓	256 x 4	300	47	330/358	16	5	C,M	D,P	4-188
Am91L01C		256 x 4	300	38	198/220	22	5	C,M	D,P	4-164
Am91L11C	✓	256 x 4	300	38	198/220	18	5	C,M	D,P	4-176
Am91L12C	✓	256 x 4	300	38	198/220	16	5	C,M	D,P	4-188
Am9101B		256 x 4	400	47	303/330	22	5	C,M	D,P	4-164
Am9111B	✓	256 x 4	400	47	303/330	18	5	C,M	D,P	4-176
Am9112B	✓	256 x 4	400	47	303/330	16	5	C,M	D,P	4-188
Am91L01B		256 x 4	400	38	182/203	22	5	C,M	D,P	4-164
Am91L11B	✓	256 x 4	400	38	182/203	18	5	C,M	D,P	4-176
Am91L12B	✓	256 x 4	400	38	182/203	16	5	C,M	D,P	4-188
Am9101A		256 x 4	500	47	303/330	22	5	C,M	D,P	4-164
Am9111A	✓	256 x 4	500	47	303/330	18	5	C,M	D,P	4-176
Am9112A	✓	256 x 4	500	47	303/330	16	5	C,M	D,P	4-188
Am91L01A		256 x 4	500	38	182/203	22	5	C,M	D,P	4-164
Am91L11A	✓	256 x 4	500	38	182/203	18	5	C,M	D,P	4-176
Am91L12A	✓	256 x 4	500	38	182/203	16	5	C,M	D,P	4-188

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C
I = Industrial −40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

4K STATIC RAMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am9150-20		1024 x 4	20	N/A	990	24/28	5	C	D,L	4-225
Am9150-25	✓	1024 x 4	25	N/A	990	24/28	5	C,M	D,L	4-225
Am91L50-25		1024 x 4	25	N/A	715	24/28	5	C	D,L	4-225
Am2148-35		1024 x 4	35	165	990	18	5	C	D,L	4-37
Am2149-35		1024 x 4	35	N/A	990	18	5	C	D,L	4-37
Am9150-35	✓	1024 x 4	35	N/A	990	24/28	5	C,M	D,L	4-228
Am91L50-35		1024 x 4	35	N/A	715	24/28	5	C	D,L	4-228
Am9151-40		1024 x 4	40*	N/A	990	24	5	C	D	4-228
Am2148-45	✓	1024 x 4	45	165	990	18	5	C,M	D,L	4-37
Am2149-45	✓	1024 x 4	45	N/A	990	18	5	C,M	D,L	4-37
Am21L48-45	✓	1024 x 4	45	110	688	18	5	C	D,L	4-37
Am21L49-45		1024 x 4	45	N/A	688	18	5	C	D,L	4-37
Am9150-45	✓	1024 x 4	45	N/A	990	24/28	5	C,M	D,L	4-225
Am91L50-45		1024 x 4	45	N/A	715	24/28	5	C	D,L	4-225
Am9151-50		1024 x 4	50*	N/A	990	24	5	C,M	D	4-225
Am2148-55	✓	1024 x 4	55	165	990	18	5	C,M	D,L	4-37
Am2149-55	✓	1024 x 4	55	N/A	990	18	5	C,M	D,L	4-37
Am21L48-55		1024 x 4	55	110	688	18	5	C	D,L	4-37
Am21L49-55		1024 x 4	55	N/A	688	18	5	C	D,L	4-37
Am9151-60		1024 x 4	60*	N/A	990	24	5	C,M	D	4-225
Am2148-70	✓	1024 x 4	70	165	990	18	5	C,M	D,L	4-37
Am2149-70	✓	1024 x 4	70	N/A	990	18	5	C,M	D,L	4-37
Am21L48-70		1024 x 4	70	110	688	18	5	C	D,L	4-37
Am21L49-70		1024 x 4	70	N/A	688	18	5	C	D,L	4-37
Am9114E	✓	1024 x 4	200	N/A	385/440	18	5	C,M	D,P	4-198
Am91L14E		1024 x 4	200	N/A	275/330	18	5	C	D,P	4-198
Am9114C	✓	1024 x 4	300	N/A	385/440	18	5	C,M	D,P	4-176
Am9124C	✓	1024 x 4	300	165/182	385/440	18	5	C,M	D,P	4-198
Am91L14C	✓	1024 x 4	300	N/A	275/330	18	5	C,M	D,P	4-198
Am91L24C	✓	1024 x 4	300	110/121	275/330	18	5	C,M	D,P	4-198
Am9114B	✓	1024 x 4	450	N/A	385/440	18	5	C,M	D,P	4-198
Am9124B	✓	1024 x 4	450	165/182	385/440	18	5	C,M	D,P	4-198
Am91L14B	✓	1024 x 4	450	N/A	275/330	18	5	C,M	D,P	4-198
Am91L24B		1024 x 4	450	110/121	275/330	18	5	C,M	D,P	4-198
Am2147-35		4096 x 1	35	165	990	18	5	C	D,L	4-27
Am2147-45	✓	4096 x 1	45	165	990	18	5	C,M	D,L,F	4-27
Am21L47-45	✓	4096 x 1	45	83	688	18	5	C	D,L	4-27
Am2147-55	✓	4096 x 1	55	165	990	18	5	C,M	D,L	4-27
Am21L47-55	✓	4096 x 1	55	83	688	18	5	C	D,L	4-27
Am2147-70	✓	4096 x 1	70	110/165	880/990	18	5	C,M	D,L,F	4-27
Am21L47-70	✓	4096 x 1	70	83	688	18	5	C	D,L	4-27
Am21L41-12		4096 x 1	120	55	303	18	5	C	D,P	4-1
Am21L41-15		4096 x 1	150	28	220	18	5	C	D,P	4-1
Am21L41-20		4096 x 1	200	28	220	18	5	C	D,P	4-1
Am9044E		4096 x 1	200	N/A	385/440	18	5	C	D,P	4-134
Am9244E		4096 x 1	200	165/182	385/440	18	5	C	D,P	4-134
Am21L41-25	✓	4096 x 1	250	28	220	18	5	C	D,P	4-27
Am9044D		4096 x 1	250	N/A	385/440	18	5	C,M	D,P	4-134
Am90L44D		4096 x 1	250	N/A	275/330	18	5	C	D,P	4-134
Am9244D	✓	4096 x 1	250	165/182	385/440	18	5	C,M	D,P	4-134
Am92L44D		4096 x 1	250	110/121	275/330	18	5	C	D,P	4-134
Am9244C	✓	4096 x 1	300	165/182	385/440	18	5	C,M	D,P	4-134
Am92L44C	✓	4096 x 1	300	110/121	275/330	18	5	C,M	D,P	4-134
Am9044C	✓	4096 x 1	300	N/A	385/440	18	5	C,M	D,P	4-134

4K STATIC RAMs (Cont'd.)

Part Number	APL	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am9244B	✓	4096 x 1	400	165/182	385/440	18	5	C,M	D,P	4-134
Am92L44B	✓	4096 x 1	400	110/121	275/330	18	5	C,M	D,P	4-134
Am9044B	✓	4096 x 1	450	N/A	385/440	18	5	C,M	D,P	4-134
Am90L44B	✓	4096 x 1	450	N/A	275/330	18	5	C,M	D,P	4-134

*Cycle Times

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C
I = Industrial −40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

8K STATIC RAMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am2130-70		1024 x 8	70	165/220	935/1018	48/52	5	C	S,P,L,J	4-9
Am2130-10	✓	1024 x 8	100	165/220	935/1018	48/52	5	C,M	S,P,L,J	4-9
Am2130-12	✓	1024 x 8	120	165/220	935/1018	48/52	5	C,M	S,P,L,J	4-9

16K STATIC RAMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am9128-70		2048 x 8	70	165	770	24	5	C	D,P,L	4-217
Am9128-90	✓	2048 x 8	90	165	990	24	5	M	D,L	4-217
Am9128-10		2048 x 6	100	83	660	24	5	C	D,P,L	4-217
Am9128-12	✓	2048 x 8	120	165	825	24	5	M	D,L	4-217
Am9128-15	✓	2048 x 8	150	83/165	550/825	24	5	C,M	D,P,L	4-217
Am9128-20	✓	2048 x 8	200	165	770/825	24	5	C,M	D,P,L	4-217
Am99C58-25		4096 x 4	25	220	990	24/28	5	C	D,L	4-262
Am99C59-25		4096 x 4	25	N/A	990	24/28	5	C	D,L	4-262
Am99C60-25		4096 x 4	25	220	990	24/28	5	C	D,L	4-264
Am2168-35		4096 x 4	35	165	660	20	5	C	D,P,L	4-57
Am2169-35		4096 x 4	35	N/A	660	20	5	C	D,P,L	4-57
Am99C58-35		4096 x 4	35	220	990	24/28	5	C,M	D,L	4-262
Am99C59-35		4096 x 4	35	N/A	990	24/28	5	C,M	D,L	4-262
Am99C60-35		4096 x 4	35	220	990	24/28	5	C,M	D,L	4-264
Am2169-40		4096 x 4	40	N/A	660	20	5	C	D,P,L	4-57
Am2168-45		4096 x 4	45	165	660/880	20	5	C,M	D,P,L	4-57
Am99C58-45		4096 x 4	45	220	990	24/28	5	C,M	D,L	4-262
Am99C59-45		4096 x 4	45	N/A	990	24/28	5	C,M	D,L	4-262
Am99C60-45		4096 x 4	45	220	990	24/28	5	C,M	D,L	4-264
Am99C68-45	✓	4096 x 4	45	110	550/660	20	5	C,M	D,P	4-279
Am99CL68-45	✓	4096 x 4	45	110	550/660	20	5	C,M	D,P	4-279
Am2169-50	✓	4096 x 4	50	N/A	660/880	20	5	C,M	D,P,L	4-57
Am2168-55	✓	4096 x 4	55	165	660/880	20	5	C,M	D,P,L	4-57
Am99C68-55	✓	4096 x 4	55	110	550/660	20	5	C,M	D,P	4-279
Am99CL68-55	✓	4096 x 4	55	110	550/660	20	5	C,M	D,P	4-279
Am2168-70	✓	4096 x 4	70	165	660/880	20	5	C,M	D,P,L	4-57
Am2169-70	✓	4096 x 4	70	N/A	660/880	20	5	C,M	D,P,L	4-57
Am99C68-70	✓	4096 x 4	70	110	550/660	20	5	C,M	D,P	4-279
Am99CL68-70	✓	4096 x 4	70	110	550/660	20	5	C,M	D,P	4-279
Am2167-35	✓	16384 x 1	35	110	660	20	5	C	D,P,L	4-47
Am2167-45	✓	16384 x 1	45	110/165	660/880	20	5	C,M	D,P,L	4-47
Am2167-55	✓	16384 x 1	55	110/165	660/880	20	5	C,M	D,P,L	4-47
Am2167-70	✓	16384 x 1	70	110/165	660/880	20	5	C,M	D,P,L	4-47

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C
I = Industrial −40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

64K STATIC RAMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am99C416-45	✓	4096 x 6	45	138	605	40	5	C	D	4-259
Am99C416-55	✓	4096 x 6	55	138	605	40	5	C	D	4-259
Am99C416-70	✓	4096 x 6	70	138	605	40	5	C	D	4-259
Am99C88H-35	✓	8192 x 8	35	138	605	28/32	5	C	D,P,L,J	4-300
Am99C88H-45	✓	8192 x 8	45	138/165	605/688	28/32	5	C,M	D,P,L,J	4-300
Am99C88H-55	✓	8192 x 8	55	138/165	605/688	28/32	5	C,M	D,P,L,J	4-300
Am99C88-70	✓	8192 x 8	70	28	330	28/32	5	C,M,E	S,L	4-289
Am99C88H-70	✓	8192 x 8	70	138/165	605/688	28/32	5	C,M	D,P,L,J	4-300
Am99CL88-70		8192 x 8	70	6	220	28/32	5	C	S,L	4-289
Am99CS88-70	✓	8192 x 8	70	55	330	28/32	5	M	S,L	4-289
Am99C88-10	✓	8192 x 8	100	28	330	28/32	5	C,M,E	S,L	4-289
Am99CL88-10		8192 x 8	100	6	220	28/32	5	C	S,L	4-289
Am99CS88-10	✓	8192 x 8	100	55	330	28/32	5	M	S,L	4-289
Am89C88-12		8192 x 8	120	28	495	28	5	C	P	
Am89CL88-12		8192 x 8	120	17	330	28	5	C	P	
Am99C88-12	✓	8192 x 8	120	28	330	28/32	5	C,M,E	S,L	4-289
Am99CL88-12		8192 x 8	120	6	220	28/32	5	C	S,L	4-289
Am99CS88-12	✓	8192 x 8	120	55	330	28/32	5	M	S,L	4-289
Am89C88-15		8192 x 8	150	28	495	28	5	C	P	
Am89CL88-15		8192 x 8	150	17	330	28	5	C	P	
Am99C88-15	✓	8192 x 8	150	28	330	28/32	5	C,M,E	S,L	4-289
Am99CL88-15		8192 x 8	150	6	220	28/32	5	C	S,L	4-289
Am99CS88-15	✓	8192 x 8	150	55	330	28/32	5	M	S,L	4-289
Am99C88-20	✓	8192 x 8	200	28	330	28/32	5	M,E	S,L	4-289
Am99CS88-20	✓	8192 x 8	200	55	330	28/32	5	M	S,L	4-289
Am99C89-45	✓	8192 x 9	45	138	660	28	5	C	D,P	4-302
Am99C89-55	✓	8192 x 9	55	138	660	28	5	C	D,P	4-302
Am99C89-70	✓	8192 x 9	70	138	660	28	5	C	D,P	4-302
Am99C164-35	✓	16,384 x 4	35	TBD	605	22	5	C	D,P,L	4-253
Am99C165-35	✓	16,384 x 4	35	TBD	605	24	5	C	D,P,L	4-253
Am99C164-45	✓	16,384 x 4	45	TBD	495/605	22	5	C,M	D,P,L	4-253
Am99C165-45	✓	16,384 x 4	45	TBD	495/605	24	5	C,M	D,P,L	4-253
Am99C164-55	✓	16,384 x 4	55	TBD	495/605	22	5	C,M	D,P,L	4-253
Am99C165-55	✓	16,384 x 4	55	TBD	495/605	24	5	C,M	D,P,L	4-253
Am99C164-70	✓	16,384 x 4	70	TBD	495/605	22	5	C,M	D,P,L	4-253
Am99C165-70	✓	16,384 x 4	70	TBD	495/605	24	5	C,M	D,P,L	4-253
Am99C328-45		32,768 x 8	45	TBD	660	28	5	C	D,P	4-257
Am99C328-55		32,768 x 8	55	TBD	660/770	28	5	C,M	D,P	4-257
Am99C328-70		32,768 x 8	70	TBD	660/770	28	5	C,M	D,P	4-257
Am99C328-10		32,768 x 8	100	TBD	660/770	28	5	C,M	D,P	4-257
Am99C641-25	✓	65,536 x 1	25	110	715	22	5	C	D,P,L	4-267
Am99C641-35	✓	65,536 x 1	35	110	605	22	5	C	D,P,L	4-267
Am99C641-45	✓	65,536 x 1	45	110	495	22	5	C,M,E	D,P,L	4-267
Am99C641-55	✓	65,536 x 1	55	110	495	22	5	C,M,E	D,P,L	4-267
Am99C641-70	✓	65,536 x 1	70	110	495	22	5	C,M,E	D,P,L	4-267

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C
I = Industrial −40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

256K DYNAMIC RAMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time(ns)	Power Dissipation(mW)		Pins	Supply Voltage (V)	Temp Range	Package	Page No.
				Standby	Active					
Am90C644-10		65,536 x 4	100	176	605	24	5	C	P	4-143
Am90C255-08		262,144 x 1	80	22	468	16/18	5	C	P,J	4-68
Am90CL255-08		262,144 x 1	80	22	468	16/18	5	C	P,J	4-83
Am90C256-08		262,144 x 1	80	22	468	16/18	5	C	P,J	4-86
Am90CL256-08		262,144 x 1	80	22	468	16/18	5	C	P,J	4-108
Am90C257-08		262,144 x 1	80	22	468	16/18	5	C	P,J	4-111
Am90CL257-08		262,144 x 1	80	22	468	16/18	5	C	P,J	4-131
Am90C255-10		262,144 x 1	100	22	358	16/18	5	C	P,J	4-68
Am90CL255-10		262,144 x 1	100	22	358	16/18	5	C	P,J	4-83
Am90C256-10		262,144 x 1	100	22	358	16/18	5	C	P,J	4-86
Am90CL256-10		262,144 x 1	100	22	358	16/18	5	C	P,J	4-108
Am90C257-10		262,144 x 1	100	22	358	16/18	5	C	P,J	4-111
Am90CL257-10		262,144 x 1	100	22	358	16/18	5	C	P,J	4-131
Am90C255-12		262,144 x 1	120	22	330	16/18	5	C	P,J	4-68
Am90CL255-12		262,144 x 1	120	22	330	16/18	5	C	P,J	4-83
Am90C256-12		262,144 x 1	120	22	330	16/18	5	C	P,J	4-86
Am90CL256-12		262,144 x 1	120	22	330	16/18	5	C	P,J	4-108
Am90C257-12		262,144 x 1	120	22	330	16/18	5	C	P,J	4-111
Am90CL257-12		262,144 x 1	120	22	330	16/18	5	C	P,J	4-131

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C
I = Industrial −40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

UV ERASABLE PROMs (NMOS)

Listed according to organization and access time.

Part Number	APL	Organization	Access Time (ns)	Temp. Range	Operating Power— Act/Stby Max (mW) (0°C–70°C)	Supply Voltages	Outputs	Number of Pins
Am2716B-100		2048 x 8	100	C	500/125	5V/±10	3-State	24
Am2716B-105		2048 x 8	100	C	500/125	5V±5	3-State	24
Am2716B-150		2048 x 8	150	C,I	500/125	5V/±10	3-State	24
Am2716B-155		2048 x 8	150	C,I	500/125	5V/±5	3-State	24
Am2716B-200		2048 x 8	200	C,I,E	500/125	5V/±10	3-State	24
Am2716B-205		2048 x 8	200	C,I,E	500/125	5V/±5	3-State	24
Am2716B		2048 x 8	250	C,I,E	500/125	5V/±5	3-State	24
Am2716B-250		2048 x 8	250	C,I,E	500/125	5V/±10	3-State	24
Am2716B-350		2048 x 8	350	C,I,E	500/125	5V/±10	3-State	24
Am2716B-355		2048 x 8	350	C,I,E	500/125	5V/±5	3-State	24
Am2716B-455		2048 x 8	450	C,I,E	500/125	5V/±5	3-State	24
Am2732B-100		4096 x 8	100	C	500/125	5V/±10%	3-State	28
Am2732B-105		4096 x 8	100	C	500/125	5V±5%	3-State	28
Am2732B-150		4096 x 8	150	C,I	500/125	5V/±10	3-State	28
Am2732B-155		4096 x 8	150	C,I	500/125	5V/±5%	3-State	28
Am2732B-200		4096 x 8	200	C,I,E	500/125	5V/±10	3-State	28
Am2732B-205		4096 x 8	200	C,I,E	500/125	5V/±5	3-State	28
Am2732B		4096 x 8	250	C,I,E	500/125	5V/±5	3-State	28
Am2732B-250		4096 x 8	250	C,I,E	500/125	5V/±10	3-State	28
Am2732B-350		4096 x 8	350	C,I,E	500/125	5V/±10	3-State	28
Am2732B-355		4096 x 8	350	C,I,E	500/125	5V/±5	3-State	28
Am2732B-455		4096 x 8	450	C,I,E	500/125	5V/±5	3-State	28
Am2764A-1		8192 x 8	150	C,I	375/125	5V±5%	3-State	28
Am2764A-15		8192 x 8	150	C,I	375/125	5V±10%	3-State	28
Am2764A-2		8192 x 8	200	C,I	375/125	5V±5%	3-State	28
Am2764A-20	✓	8192 x 8	200	C,I,L,M	375/125	5V±10%	3-State	28
Am2764A		8192 x 8	250	C,I,L	375/125	5V±5%	3-State	28
Am2764A-25	✓	8192 x 8	250	C,I,L,M	375/125	5V±10%	3-State	28
Am2764A-3		8192 x 8	300	C,I,L	375/125	5V±5%	3-State	28
Am2764A-30	✓	8192 x 8	300	C,I,L,M	375/125	5V±10%	3-State	28
Am2764A-4		8192 x 8	450	C,I,L	375/125	5V±5%	3-State	28
Am27128A-1		16,384 x 8	150	C,I	500/125	5V±5%	3-State	28
Am27128A-15		16,384 x 8	150	C,I	500/125	5V±10%	3-State	28
Am27128A-2		16,384 x 8	200	C,I	500/125	5V±5%	3-State	28
Am2764A-20	✓	16,384 x 8	200	C,I,L,M	375/125	5V±10%	3-State	28
Am27128A		16,384 x 8	250	C,I,L	500/125	5V±5%	3-State	28
Am2764A-25	✓	16,384 x 8	250	C,I,L,M	375/125	5V±10%	3-State	28
Am27128A-3		16,384 x 8	300	C,I,L	500/125	5V±5%	3-State	28
Am2764A-30	✓	16,384 x 8	300	C,I,L,M	500/125	5V±10%	3-State	28
Am27128A-4		16,384 x 8	450	C,I,L	500/125	5V±5%	3-State	28
Am27256-1		32,768 x 8	170	C	500/125	5V±5%	3-State	28
Am27256-17		32,768 x 8	170	C	500/125	5V±10%	3-State	28
Am27256-2		32,768 x 8	200	C,I,L	500/125	5V±5%	3-State	28
Am27256-20	✓	32,768 x 8	200	C,I,L,M	500/125	5V±10%	3-State	28
Am27256		32,768 x 8	250	C,I,L	500/125	5V±5%	3-State	28
Am27256-25	✓	32,768 x 8	250	C,I,L,M	500/125	5V±10%	3-State	28
Am27256-3		32,768 x 8	300	C,I,L	500/125	5V±5%	3-State	28
Am27256-30	✓	32,768 x 8	300	C,I,L,M	500/125	5V±10%	3-State	28
Am27256-4		32,768 x 8	450	C,I,L	500/125	5V±5%	3-State	28
Am27512		65,536 x 8	250	C	500/125	5V±5%	3-State	28
Am27512-25		65,536 x 8	250	C	500/125	5V±10%	3-State	28
Am27512-3		65,536 x 8	300	C	500/125	5V±5%	3-State	28
Am27512-30		65,536 x 8	300	C	500/125	5V±10%	3-State	28
Am27512-45	✓	65,536 x 8	450	M	500/125	5V±10%	3-State	28

UV ERASABLE PROMs (CMOS)

Listed according to organization and access time.

Part Number	APL	Organization	Access Time (ns)	Temp. Range	Operating Power— Act/Stby Max (mW) (0°C–70°C)	Supply Voltages	Outputs	Number of Pins
Am27C256-150*		32,768 x 8	150	C	150/0.5	5V±10%	3-State	28
Am27C256-155*		32,768 x 8	150	C	150/0.5	5V±5%	3-State	28
Am27C256-200*		32,768 x 8	200	C,I	150/0.5	5V±10%	3-State	28
Am27C256-205*		32,768 x 8	200	C,I	150/0.5	5V±5%	3-State	28
Am27C256*		32,768 x 8	250	C,I,E	150/0.5	5V±5%	3-State	28
Am27C256-250*		32,768 x 8	250	C,I,E	150/0.5	5V±10%	3-State	28
Am27C256-455*		32,768 x 8	450	C,I,E	500/1	5V±5%	3-State	28
Am27C512-170*		65,536 x 8	170	C	150/0.5	5V±10%	3-State	28
Am27C512-175*		65,536 x 8	170	C	150/0.5	5V±5%	3-State	28
Am27C512-200*		65,536 x 8	200	C,I	150/0.5	5V±10%	3-State	28
Am27C512-205*		65,536 x 8	200	C,I	150/0.5	5V±5%	3-State	28
Am27C512*		65,536 x 8	250	C,I,E	150/0.5	5V±5%	3-State	28
Am27C512-250*		65,536 x 8	250	C,I,E	150/0.5	5V±10%	3-State	28
Am27C512-455*		65,536 x 8	450	C,I,E	500/1	5V±5%	3-State	28
Am27C1024-200		65,536 x 16	200	C	250/1	5V±10%	3-State	40
Am27C1024-205		65,536 x 16	200	C	250/1	5V±5%	3-State	40
Am27C1024		65,536 x 16	250	C	250/1	5V±5%	3-State	40
Am27C1024-250		65,536 x 16	250	C	250/1	5V±10%	3-State	40

*In Development

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C
I = Industrial −40°C to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack
L = Leadless Chip Carrier

ONE TIME PROGRAMMABLE (OTP) ROMs (NMOS, CMOS)

Listed according to organization and access time.

Part Number	APL	Organization	Access Time (ns)	Temp. Range	Operating Power— Act/Stby Max (mW) (0°C–70°C)	Supply Voltages	Outputs	Number of Pins
Am2764A-2*		8192 x 8	200	C	500/125	5V±5%	3-State	28
Am2764A*		8192 x 8	250	C	500/125	5V±5%	3-State	28
Am27128A-2*		16,384 x 8	200	C	500/125	5V±5%	3-State	28
Am27128A*		16,384 x 8	250	C	500/125	5V±5%	3-State	28
Am27256-2*		32,768 x 8	200	C	500/125	5V±5%	3-State	28
Am27256*		32,768 x 8	250	C	500/125	5V±5%	3-State	28
Am27C256-2*		32,768 x 8	200	C	150/0.5	5V±5%	3-State	28
Am27C256*		32,768 x 8	250	C,I,E	150/0.5	5V±5%	3-State	28
Am27C512-2*		65,536 x 8	200	C	150/0.5	5V±5%	3-State	28
Am27C512*		65,536 x 8	250	C,I,E	150/0.5	5V±5%	3-State	28

ELECTRICALLY ERASABLE PROMs

Listed according to organization and access time.

Part Number	APL	Organization	Access Time (ns)	Temp. Range	Operating Power— Act/Stby Max (mW) (0°C–70°C)	Supply Voltages	Outputs	Number of Pins
Am2817A-2		2048 x 8	200	C,I	500/200	5V±5%	3-State	28
Am2817A-20		2048 x 8	200	C,I	500/200	5V±10%	3-State	28
Am2817A		2048 x 8	250	C,I,E	500/200	5V±5%	3-State	28
Am2817A-25	✓	2048 x 8	250	C,I,E	500/200	5V±10%	3-State	28
AM2817A-3		2048 x 8	350	C,I,E	500/200	5V±5%	3-State	28
Am2817A-35	✓	2048 x 8	350	C,I,E	500/200	5V±10%	3-State	28
Am9864-2*		8192 x 8	200	C,I	500/200	5V±5%	3-State	28
Am9864-20*		8192 x 8	200	C,I	500/200	5V±10%	3-State	28
Am2864A-2*		8192 x 8	200	C,I	500/200	5V±5%	3-State	28
Am2864A-20*		8192 x 8	200	C,I	500/200	5V±10%	3-State	28
Am2864B-2*		8192 x 8	200	C,I	500/200	5V±5%	3-State	28
Am2864B-20*		8192 x 8	200	C,I	500/200	5V±10%	3-State	28
Am2864A*		8192 x 8	250	C,I,E	500/200	5V±5%	3-State	28
Am2864A-25*	✓	8192 x 8	250	C,I,E	500/200	5V±10%	3-State	28
Am2864B		8192 x 8	250	C,I,E*	500/200	5V±5%	3-State	28
Am2864B-25	✓	8192 x 8	250	C,I,E*	500/200	5V±10%	3-State	28
Am9864		8192 x 8	250	C,I,E*	500/200	5V±5%	3-State	28
Am9864-25	✓	8192 x 8	250	C,I,E*	500/200	5V±10%	3-State	28
Am2864A-3*		8192 x 8	300	C,I,E	500/200	5V±5%	3-State	28
Am2864A-30*	✓	8192 x 8	300	C,I,E	500/200	5V±10%	3-State	28
Am2864B-3		8192 x 8	300	C,I,E	500/200	5V±5%	3-State	28
Am2864B-30	✓	8192 x 8	300	C,I,E	500/200	5V±10%	3-State	28
Am9864-30	✓	8192 x 8	300	E	500/200	5V±10%	3-State	28
Am2864A-35*	✓	8192 x 8	350	C,I,E	500/200	5V±10%	3-State	28
Am2864A-355*		8192 x 8	350	C,I,E	500/200	5V±5%	3-State	28
Am2864B-35	✓	8192 x 8	350	C,I,E	500/200	5V±10%	3-State	28
Am2864B-355		8192 x 8	350	C,I,E	500/200	5V±5%	3-State	28
Am9864-3		8192 x 8	350	C,I,E	500/200	5V±5%	3-State	28
Am9864-35	✓	8192 x 8	350	C,I,E	500/200	5V±10%	3-State	28
Am28C256-200*		32,768 x 8	200	C	300/5	5V±10%	3-State	28
Am28C256-205*		32,768 x 8	200	C	300/5	5V±5%	3-State	28
Am28C256*		32,768 x 8	250	C	300/5	5V±5%	3-State	28
Am28C256-250*		32,768 x 8	250	C	300/5	5V±10%	3-State	28
Am28C256-300*		32,768 x 8	300	C	300/5	5V±10%	3-State	28
Am28C256-305*		32,768 x 8	300	C	300/5	5V±5%	3-State	28
Am28C256-350*		32,768 x 8	350	C	300/5	5V±10%	3-State	28
Am28C256-355*		32,768 x 8	350	C	300/5	5V±5%	3-State	28

*In Development

SPECIAL FUNCTIONAL PRODUCTS

Listed according to organization and access time.

Part Numbers	APL	Organization	Performance Criteria	Pins	Temp Range	Package	Function
Am99C19		1024 x 9	45ns cycle/20 MHz throughput	28	C,M	D	First In/First Out (FIFO)
Am99C10		256 x 48	50ns Data to match output	24	C	D	Content Addressable Memory (CAM)

Temperature Ranges

C = Commercial 0°C to 70°C
M = Military −55°C to +125°C
E = Extended −55°C to +85°C or +100°C

Package Types

D = Cerdip
P = Plastic
F = Flatpack

Bipolar Programmable Read Only Memory (PROM) Index

For more information on Bipolar PROMs, see Section 7:

- Testing High-Performance Bipolar Memory
- Bipolar Generic PROM Series Reliability Report
- Bipolar PROMs as Programmable Logic Products
- Generic Programming Information
- Guide to Analysis of Programming Problems

Am10P14/Am100P14/Am10KP14

4,096-Bit (1024 x 4) ECL Bipolar PROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

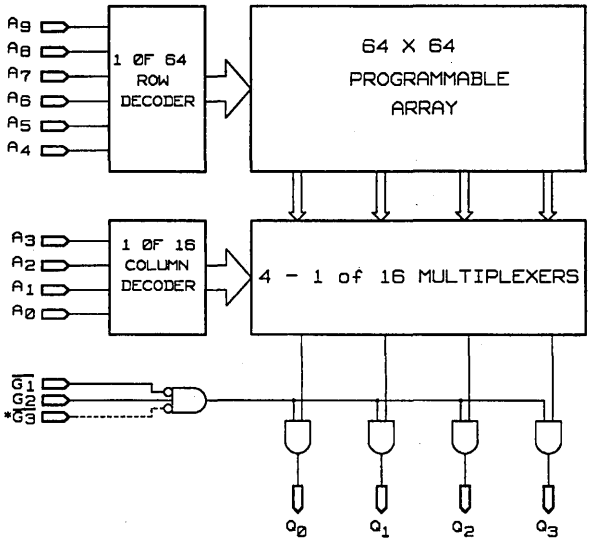
- Fast Access time (8 ns typ.) — improves system cycle times
- Power dissipation decreases with increasing temperature
- Internally voltage compensated providing flat AC performance
- Open emitter outputs (50 Ω drive), wired-OR capability

GENERAL DESCRIPTION

The Am10P14, Am10KP14, & Am100P14 (1024-words by 4-bits) are Schottky array, ECL Programmable Read-Only Memories (PROMs).

The 10K Versions are compatible with standard voltage-compensated 10K series ECL. The 100K Versions are compatible with standard temperature and voltage-compensated 100K series ECL. Both are capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is provided by both active LOW ($\overline{G_1}$ & $\overline{G_3}$) and active HIGH (G_2) output enables and an unterminated emitter follower output capable of wired-OR bus connection.

BLOCK DIAGRAM



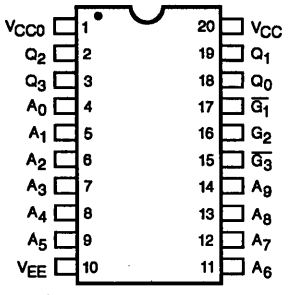
BD006370

PRODUCT SELECTOR GUIDE

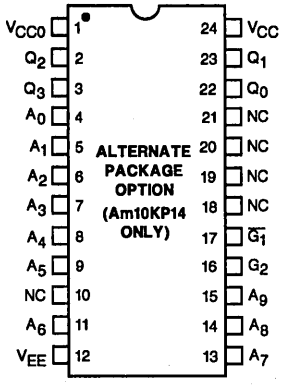
Part Number	Am10P14		Am10KP14		Am100P14
Address Access Time (ns)	10	15	10	15	10
Operating Range	C	M	C	M	C

Publication # 08111 Rev. A Amendment /0
° Issue Date: May 1986

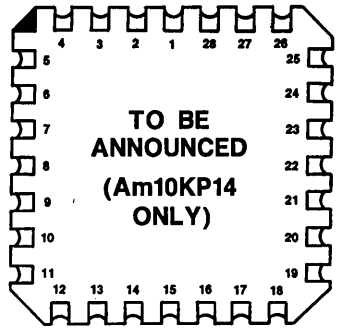
CONNECTION DIAGRAMS
Top View



CD009530

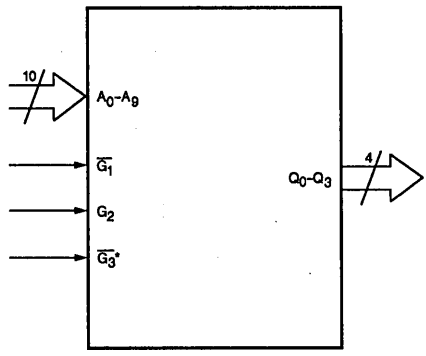


CD009540



CD009550

LOGIC SYMBOL



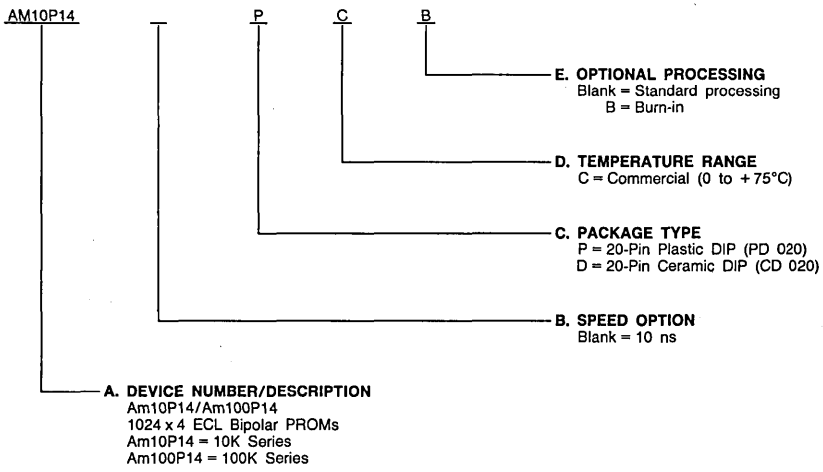
LS002430

V_{CC}/V_{CC0} = Positive Power Supply
V_{EE} = Negative Power Supply

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM10P14	PC, PCB, DC, DCB
AM100P14	
AM10KP14	PC*, PCB*, DC*, DCB*

*P = 24-Pin Plastic DIP (PD 024)
D = 24-Pin Ceramic DIP (CD 024)
This is an Alternate Package option and is denoted by a "K" within the Device Number.

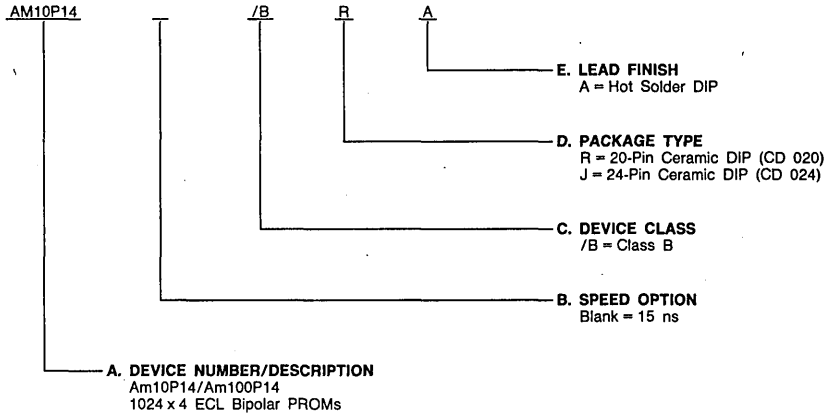
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package type
E. Lead Finish



Valid Combinations	
AM10P14	/BRA
AM10KP14	/BJA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The Outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, G_2, $\overline{G_3}$* Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all outputs to V_{OL}.

*G_3 is not available on Am10KP14.

$$\text{Enable} = \overline{G_1} \cdot G_2 \cdot \overline{G_3}$$

$$\text{Disable} = \overline{\overline{G_1} \cdot G_2 \cdot \overline{G_3}}$$

$$= G_1 + \overline{G_2} + G_3$$

V_{CC}/V_{CCO} Device Power Supply Pins
The most positive of the logic power supply pins.

V_{EE} Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to V_{CC}/V_{CCO} Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
DC Voltage Applied to Outputs
During Programming ..... 2.2 V
DC Voltage Applied to V_{CCO}
During Programming ..... 16 V
Output Current (DC HIGH Output) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

10K Series

Commercial (C) Devices
Temperature T_A ..... 0 to +75°C
Supply Voltage ..... −5.46 V to −4.94 V

Military (M) Devices
Temperature T_C ..... −55 to +125°C
Supply Voltage ..... −5.72 V to −4.68 V

100K Series

Commercial (C) Devices
Temperature T_C ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military products 100% tested at −55°C, +25°C, 125°C

2

DC CHARACTERISTICS over operating range unless otherwise specified

100K Series

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	−1025	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		−1035		mV
V_{OLC}	Output Voltage LOW				−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		−1165	−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		−1810	−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)			220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ (Min.)			170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		−195		mA

10K Series (Commercial)

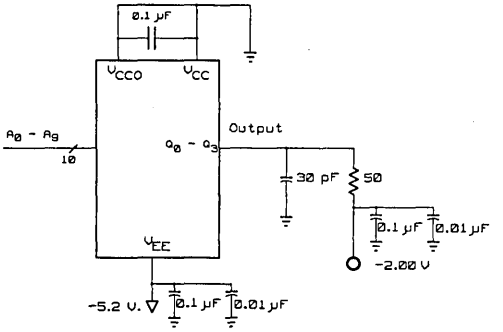
Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$T_A = 0°C$	−1000	−840	mV
				$T_A = +25°C$	−960	−810	
				$T_A = +75°C$	−900	−720	
V_{OL}	Output Voltage LOW			$T_A = 0°C$	−1870	−1665	mV
				$T_A = +25°C$	−1850	−1650	
				$T_A = +75°C$	−1830	−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		$T_A = 0°C$	−1020		mV
				$T_A = +25°C$	−980		
				$T_A = +75°C$	−920		
V_{OLC}	Output Voltage LOW			$T_A = 0°C$		−1645	mV
				$T_A = +25°C$		−1630	
				$T_A = +75°C$		−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		$T_A = 0°C$	−1145	−840	mV
				$T_A = +25°C$	−1105	−810	
				$T_A = +75°C$	−1045	−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		$T_A = 0°C$	−1870	−1490	mV
				$T_A = +25°C$	−1850	−1475	
				$T_A = +75°C$	−1830	−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)		$T_A = 0°C$		220	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$T_A = 0°C$		170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = 0°C$	−200		mA
				$T_A = +75°C$	−185		mA

10K Series (Military)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$T_A = -55°C$	−1070	−860	mV
				$T_A = +125°C$	−860	−650	
V_{OL}	Output Voltage LOW			$T_A = -55°C$	−1900	−1690	mV
				$T_A = +125°C$	−1800	−1570	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		$T_A = -55°C$	−1090		mV
				$T_A = +125°C$	−880		
V_{OLC}	Output Voltage LOW			$T_A = -55°C$		−1670	mV
				$T_A = +125°C$		−1550	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		$T_A = -55°C$	−1215	−860	mV
				$T_A = +125°C$	−1005	−650	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		$T_A = -55°C$	−1900	−1515	mV
				$T_A = +125°C$	−1800	−1395	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)		$T_A = -55°C$		250	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ (Min.)		$T_A = -55°C$		170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = -55°C$	−210		mA
				$T_A = +125°C$	−175		mA

Notes: 1. Guaranteed with transverse air flow exceeding 400 linear feet/minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

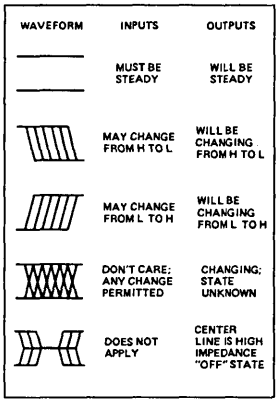
SWITCHING TEST CIRCUITS



TC003600

Notes: 1. All device test loads should be located within 2" of device output pin.
2. Decoupling of power supplies should be as close to device pins as possible.
3. Load capacitance includes all stray and fixture capacitance.

KEY TO SWITCHING WAVEFORMS



KS000010

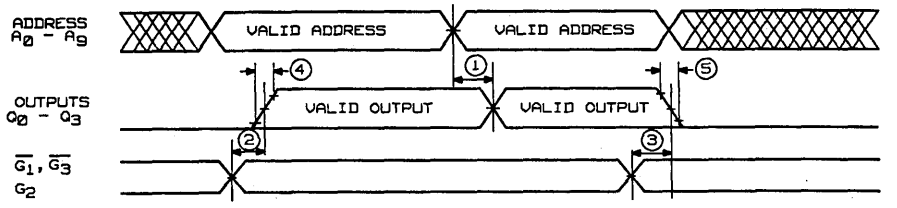
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	10K Version COM'L Max.	10K Version MIL Max.	100K Version COM'L Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	10	15	10	ns
2	TGVQL	Delay from Output Enable Valid to Output LOW	5	10	5	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid	5	10	5	ns
4	TQLQH	Output Rise Time	5	5	5	ns
5	TQHQL	Output Fall Time	5	5	5	ns

See also Switching Test Circuit and Notes 1, 2, & 3.

Notes: 1. Tests are performed with 20% to 80% input transition time of 2.5 ns or less, and input pulse levels of −1.7 V to −0.9 V using specified Switching test load.
2. Timing is measured from 50% of input transition to 50% of output transition.
3. Output rise and fall times are measured from 20% to 80% of output transition.

SWITCHING WAVEFORMS



WF021640

Am10P44/Am100P44

16,384-Bit (4096 x 4) ECL Bipolar PROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

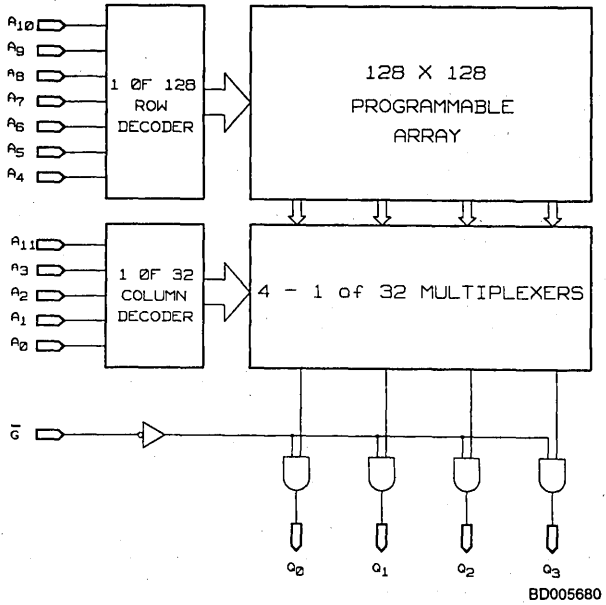
- Fast access time (12 ns typical) improves system cycle times
- Power dissipation decreases with increasing temperature
- Internally voltage compensated providing flat AC performance
- Open emitter outputs (50-Ω drive), wired-OR capability

GENERAL DESCRIPTION

The Am10P44 and Am100P44 (4096 words by 4 bits) are Schottky array, ECL Programmable Read-Only Memories (PROMs).

The 10K Versions are compatible with standard voltage compensated 10K series ECL. The 100K versions are compatible with standard temperature and voltage compensated 100K series ECL. Both are capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is provided by an active LOW output enable ($\overline{G}$) and an unterminated emitter-follower output capable of wired-OR bus connection.

BLOCK DIAGRAM

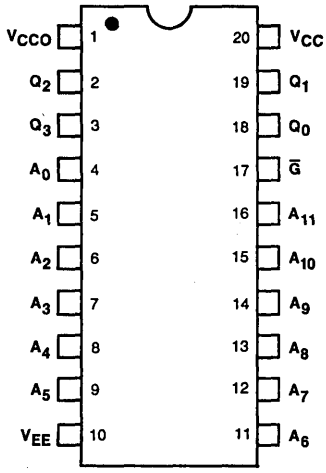


PRODUCT SELECTOR GUIDE

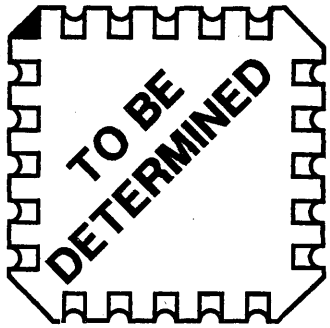
Part Number	10P44	10P44	100P44
Address Access Time (ns)	15	20	15
Operating Range	C	M	C

Publication # 07248 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

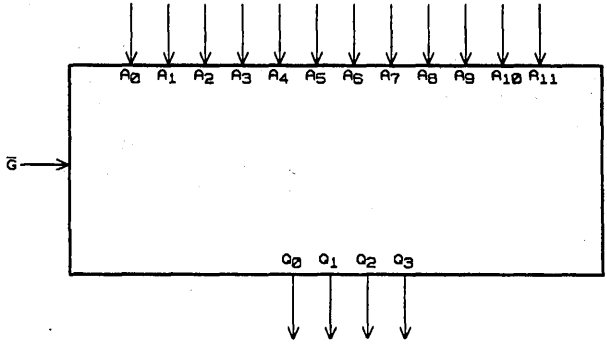


CD008070



CD009060

LOGIC SYMBOL

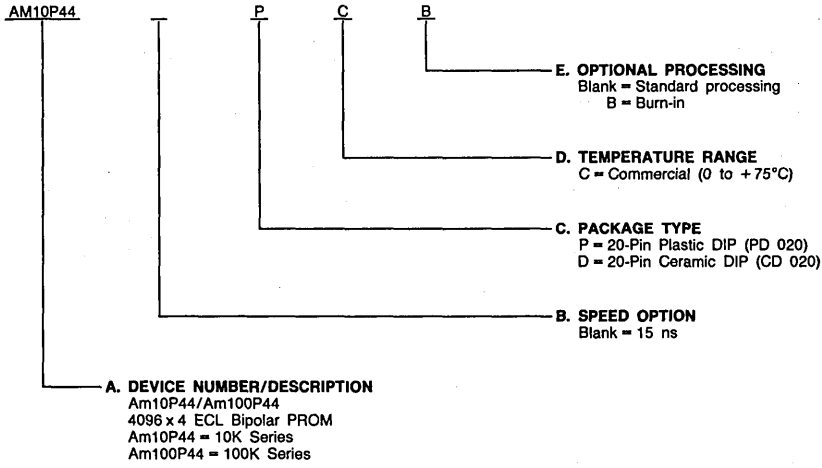


LS002021

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM10P44	PC, PCB, DC, DCB
AM100P44	

Valid Combinations

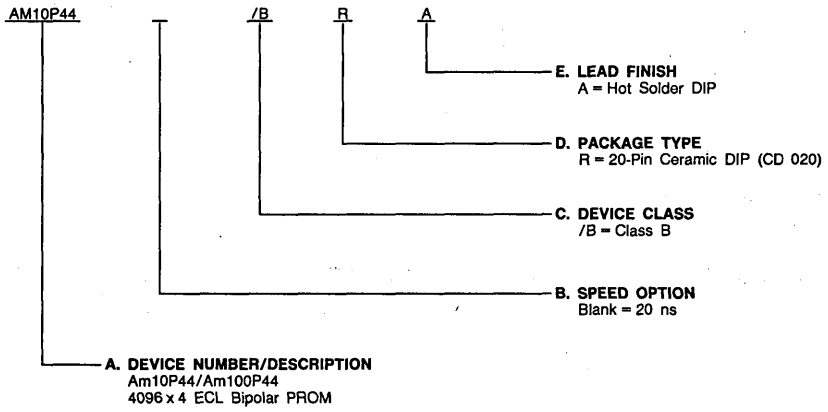
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package type
E. Lead Finish



Valid Combinations	
AM10P44	/BRA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address (Inputs)
The 12-bit field presented at the address inputs selects one of 4096 memory locations to be read from.

$Q_0 - Q_3$ Data Port (Outputs)
The outputs whose state represents the data read from the selected memory locations.

$\overline{G}$ Output Enable (Output)
Provides direct control of the Q output buffers. Outputs disabled forces all outputs to V_{OL}.
Enable = $\overline{G}$
Disable = G

V_{CC}, V_{CCO} Device Power Supply Pins
The most positive of the logic power supply pins.

V_{EE} Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −55 to +125°C
Supply Voltage (V_{EE}) to Ground ..... −7.0 to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
DC Voltage Applied
to Outputs During Programming ..... 2.2 V
DC Voltage Applied
to V_{CCO} During Programming ..... 16 V
DC Output Current ..... −30 to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.46 to −4.94 V

10K Series

Military (M) Devices
Temperature ..... −55 to +125°C
Supply voltage ..... −5.72 to −4.68 V

100K Series

Commercial (C) Devices
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 to −4.2V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military Products 100% tested at −55°C, +25°C, +125°C

DC CHARACTERISTICS over operating range unless otherwise specified

10K Series (Commercial)

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50Ω to −2.0V	$T_A = 0°C$	−1000	−840	mV
				$T_A = +25°C$	−960	−810	
				$T_A = +75°C$	−900	−720	
V_{OL}	Output LOW Voltage			$T_A = 0°C$	−1870	−1665	mV
				$T_A = +25°C$	−1850	−1650	
				$T_A = +75°C$	−1830	−1625	
V_{OHC}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		$T_A = 0°C$	−1020		mV
				$T_A = +25°C$	−980		
				$T_A = +75°C$	−920		
V_{OLC}	Output LOW Voltage			$T_A = 0°C$		−1645	mV
				$T_A = +25°C$		−1630	
				$T_A = +75°C$		−1605	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$T_A = 0°C$	−1145	−840	mV
				$T_A = +25°C$	−1105	−810	
				$T_A = +75°C$	−1045	−720	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$T_A = 0°C$	−1870	−1490	mV
				$T_A = +25°C$	−1850	−1475	
				$T_A = +75°C$	−1830	−1450	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$T_A = 0°C$		220	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$T_A = 0°C$		170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = 0°C$	−185		mA
				$T_A = +75°C$	−200		mA

Table continues on following page.
Notes: See notes following Military DC characteristics table.

10K Series (Military)

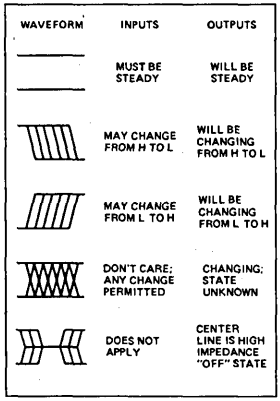
Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50Ω to −2.0V	$T_A = -55°C$	−1070	−860	mV
				$T_A = +125°C$	−860	−650	
V_{OL}	Output LOW Voltage			$T_A = -55°C$	−1900	−1690	mV
				$T_A = +125°C$	−1800	−1570	
V_{OHC}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		$T_A = -55°C$	−1090		mV
				$T_A = +125°C$	−880		
V_{OLC}	Output LOW Voltage			$T_A = -55°C$		−1670	mV
				$T_A = +125°C$		−1550	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$T_A = -55°C$	−1215	−860	mV
				$T_A = +125°C$	−1005	−650	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		$T_A = -55°C$	−1900	−1515	mV
				$T_A = +125°C$	−1800	−1395	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		$T_A = -55°C$		250	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		$T_A = -55°C$		170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = -55°C$	180		mA
				$T_A = +125°C$	−180		mA

100K Series

Parameter Symbols	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	−1025	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		−1035		mV
V_{OLC}	Output Voltage LOW				−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		−1165	−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		−1810	−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)			220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ (Min.)			170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		190		mA

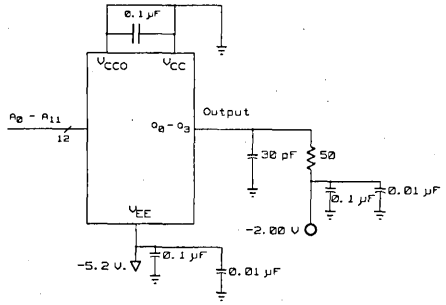
Notes: 1. Guaranteed with transverse air flow exceeding 400 linear F.P.M.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING TEST CIRCUIT



TC002811

Notes: 1. All device test loads should be located within 2" of device output pin.
2. Decoupling of power supplies shoul be as close to device pins as possible.
3. Load capacitance includes all stray and fixture capacitance.

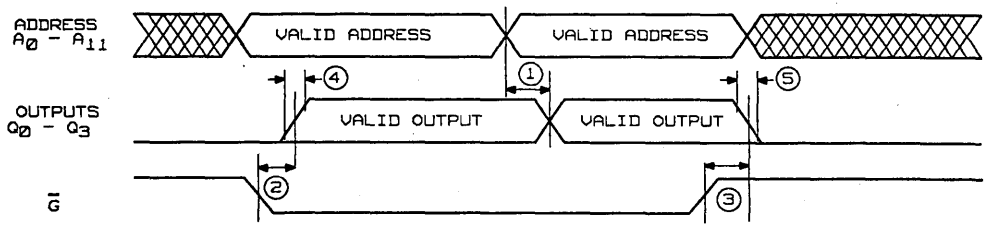
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbols	Parameter Description	10K Version COM'L Max.	10K Version MIL Max.	100K Version COM'L Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	15	20	15	ns
2	TGVQL	Delay from Output Enable Valid to Output LOW	10	15	10	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid	10	15	10	ns
4	TQLQH	Output Rise Time	5	5	5	ns
5	TQHQL	Output Fall Time	5	5	5	ns

See also Switching Test Circuit and Notes 1, 2, and 3.

Notes: 1. Tests are performed with 20% to 80% input transition time of 2.5 ns or less, and input pulse levels of −1.7 V to −0.9 V using specified Switching test load.
2. Timing is measured from 50% of input transition to 50% of output transition.
3. Output rise and fall times are measured from 20% to 80% of output transition.

SWITCHING WAVEFORMS



WF020050

Am10P88/Am100P88

65,536-Bit (8192 x 8) ECL Bipolar PROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

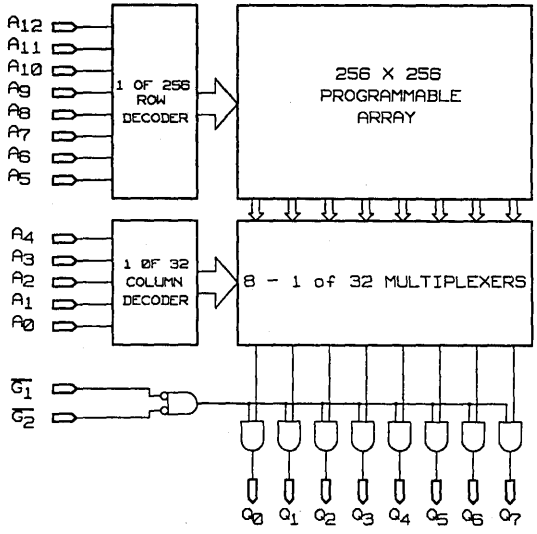
- Fast Access time (12 ns typ.) — improves system cycle times
- Power dissipation decreases with increasing temperature
- Internally voltage compensated providing flat AC performance
- Open emitter outputs (50 Ω drive), wired-OR capability

GENERAL DESCRIPTION

The Am10P88 & Am100P88 (8192-words by 8-bits) are Schottky array, ECL Programmable Read-Only Memories (PROMs).

The 10K Versions are compatible with standard voltage-compensated 10K series ECL. The 100K Versions are compatible with standard temperature and voltage-compensated 100K series ECL. Both are capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is provided by active LOW ($\overline{G_1}$ & $\overline{G_2}$) output enables and an unterminated emitter follower output capable of wired-OR bus connection.

BLOCK DIAGRAM



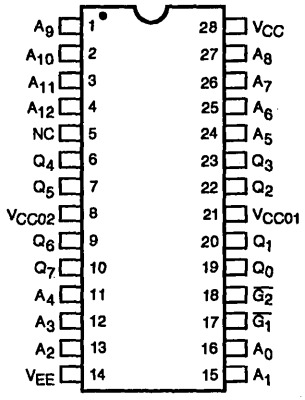
BD006360

PRODUCT SELECTOR GUIDE

Part Number	Am10P88		Am100P88
Address Access Time (ns)	15 ns	20 ns	15 ns
Operating Range	C	M	C

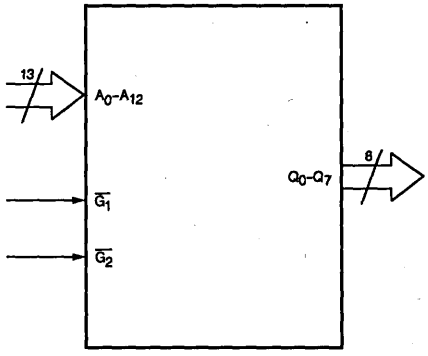
Publication # 08112 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009520

LOGIC SYMBOL

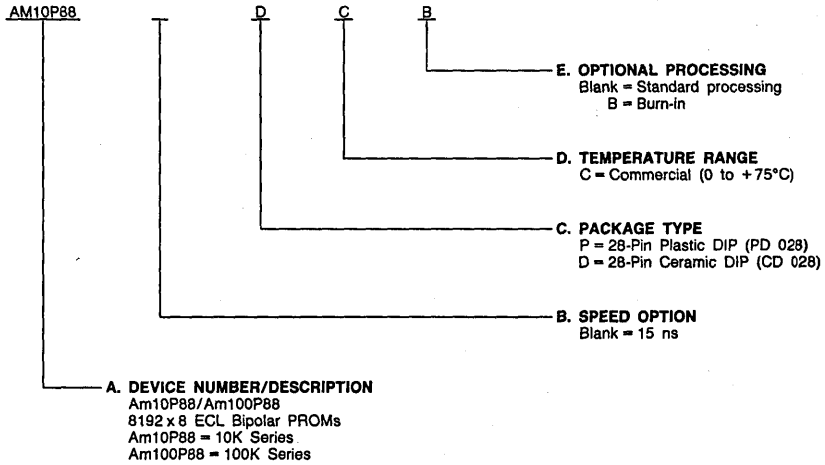


LS002420

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM10P88	DC, DCB, PC, PCB
AM100P88	

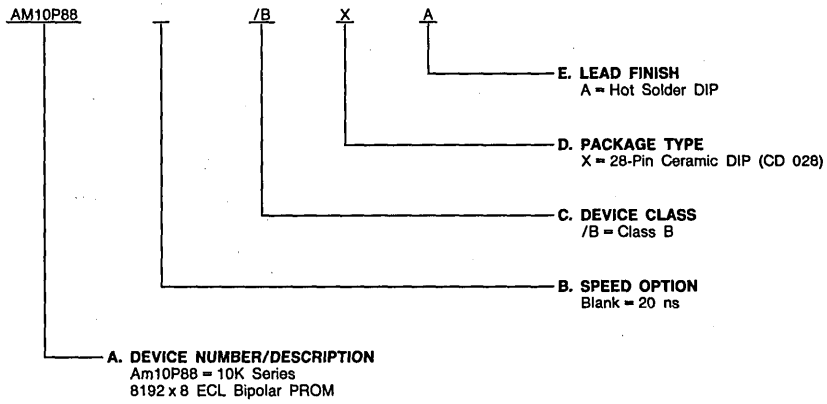
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package type
E. Lead Finish



Valid Combinations	
AM10P88	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{12}$ Address Inputs
The 13-bit field presented at the address inputs selects one of 8192 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, $\overline{G_2}$ Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all outputs to V_{OL}.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2}$$

$$\text{Disable} = \overline{\overline{G_1} \cdot \overline{G_2}} = G_1 + G_2$$

V_{CC}, V_{CCO1}, V_{CCO2} Device Power Supply Pins
The most positive of the logic power supply pins.

V_{EE} Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to V_{CC}/V_{CCO} Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
DC Voltage Applied to Outputs
During Programming ..... 2.2 V
DC Voltage Applied to V_{CCO}
During Programming ..... 16 V
Output Current
(DC HIGH Output) ..... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

10K Series

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.46 V to −4.94 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... −5.72 V to −4.68 V

100K Series

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.7 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military products 100% tested at −55°C, +25°C, +125°C

DC CHARACTERISTICS over operating range unless otherwise specified

100K Series

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH\ (Max.)}$ or $V_{IL\ (Min.)}$	Loading is 50 Ω to −2.0 V	−1025	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH\ (Min.)}$ or $V_{IL\ (Max.)}$		−1035		mV
V_{OLC}	Output Voltage LOW				−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		−1165	−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		−1810	−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH(Max.)}$			220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL(Min.)}$			170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		−220		mA

10K Series (Commercial)

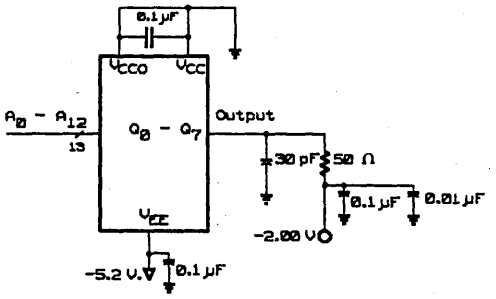
Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50Ω to −2.0V	$T_A = 0°C$	−1000	−840	mV
				$T_A = +25°C$	−960	−810	
				$T_A = +75°C$	−900	−720	
V_{OL}	Output Voltage LOW			$T_A = 0°C$	−1870	−1665	mV
				$T_A = +25°C$	−1850	−1650	
				$T_A = +75°C$	−1830	−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		$T_A = 0°C$	−1020		mV
				$T_A = +25°C$	−980		
				$T_A = +75°C$	−920		
V_{OLC}	Output Voltage LOW			$T_A = 0°C$		−1645	mV
				$T_A = +25°C$		−1630	
				$T_A = +75°C$		−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		$T_A = 0°C$	−1145	−840	mV
				$T_A = +25°C$	−1105	−810	
				$T_A = +75°C$	−1045	−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		$T_A = 0°C$	−1870	−1490	mV
				$T_A = +25°C$	−1850	−1475	
				$T_A = +75°C$	−1830	−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)		$T_A = 0°C$		220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ (Min.)		$T_A = 0°C$		170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = 0°C$	−265		mA
				$T_A = +75°C$	−215		mA

10K Series (Military)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50Ω to −2.0V	$T_A = -55°C$	−1070	−860	mV
				$T_A = +125°C$	−860	−650	
V_{OL}	Output Voltage LOW			$T_A = -55°C$	−1900	−1690	mV
				$T_A = +125°C$	−1800	−1570	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		$T_A = -55°C$	−1090		mV
				$T_A = +125°C$	−880		
V_{OLC}	Output Voltage LOW			$T_A = -55°C$		−1670	mV
				$T_A = +125°C$		−1550	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		$T_A = -55°C$	−1215	−860	mV
				$T_A = +125°C$	−1005	−650	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		$T_A = -55°C$	−1900	−1515	mV
				$T_A = +125°C$	−1800	−1395	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)		$T_A = -55°C$		250	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ (Min.)		$T_A = -55°C$		170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		$T_A = -55°C$	−280		mA
				$T_A = +125°C$	−230		mA

Notes: 1. Guaranteed with transverse air flow exceeding 400 linear feet/minute.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

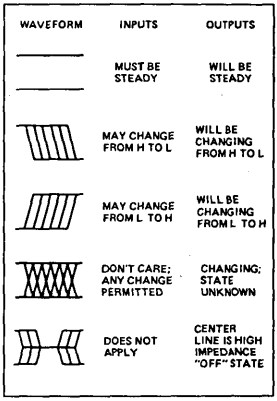
SWITCHING TEST CIRCUIT



TC003591

Notes: 1. All device test loads should be located within 2" of device output pin.
2. Decoupling of power supplies should be as close to device pins as possible.
3. Load capacitance includes all stray and fixture capacitance.

KEY TO SWITCHING WAVEFORMS



KS000010

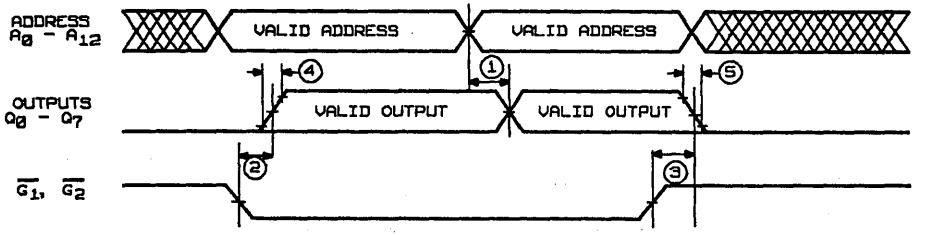
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	10K Version COM'L Max.	10K Version MIL Max.	100K Version COM'L Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	15	20	15	ns
2	TGVQL	Delay from Output Enable Valid to Output LOW	10	15	10	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid	10	15	10	ns
4	TQLQH	Output Rise Time	5	5	5	ns
5	TQHQL	Output Fall Time	5	5	5	ns

See also Switching Test Circuit and Notes 1, 2, & 3.

Notes: 1. Tests are performed with 20% to 80% input transition time of 2.5 ns or less and input pulse levels of -1.7 V to -0.9 V using specified Switching test load.
2. Timing is measured from 50% of input transition to 50% of output transition.
3. Output rise and fall times are measured from 20% to 80% of output transition.

SWITCHING WAVEFORM



WF021630

Am27S12/13

2,048-Bit (512 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

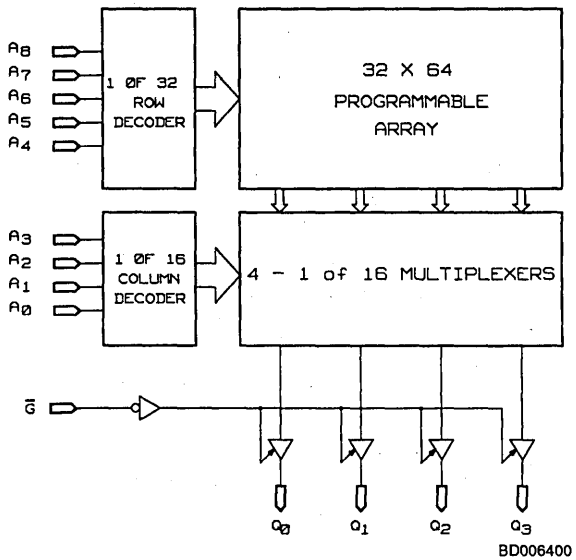
- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

The Am27S12/13 (512 words by 4 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S12) and three-state (Am27S13) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by an active LOW output enable ($\overline{G}$).

BLOCK DIAGRAM



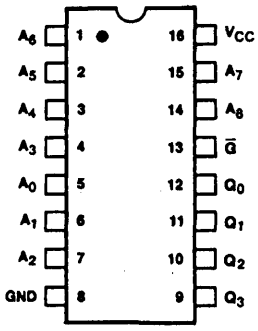
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	Am27S12A		Am27S12	
Three-State Part Number	Am27S13A		Am27S13	
Address Access Time	30 ns	40 ns	50 ns	60 ns
Operating Range	C	M	C	M

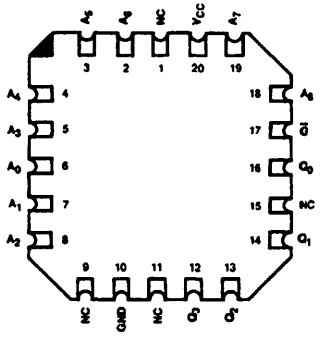
Publication # 03208 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

DIPs*



CD000591

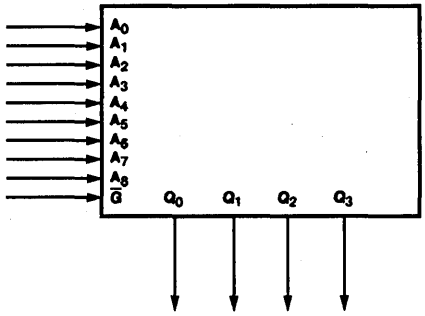


CD000601

*Also available in 16-Pin Flatpacks. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

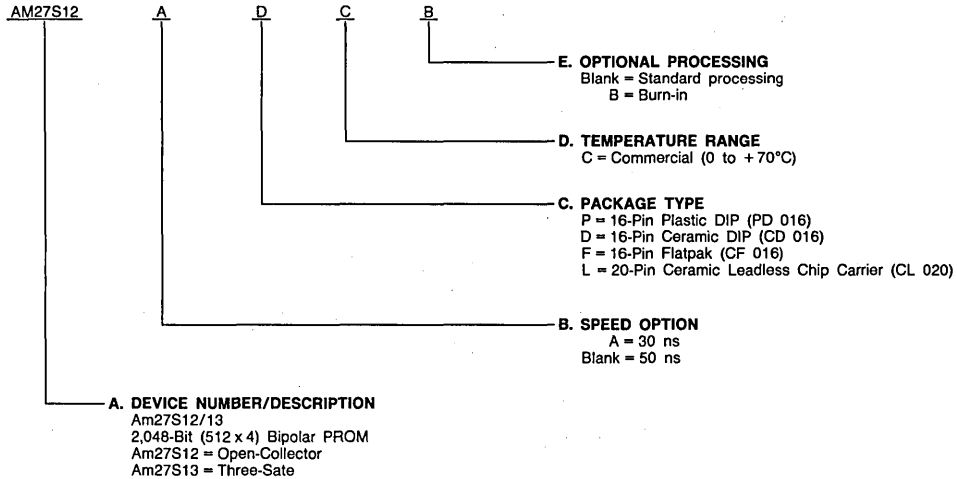


LS000091

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S12	DC, DCB, PC, PCB, LC, LCB, FC, FCB
AM27S12A	
AM27S13	
AM27S13A	

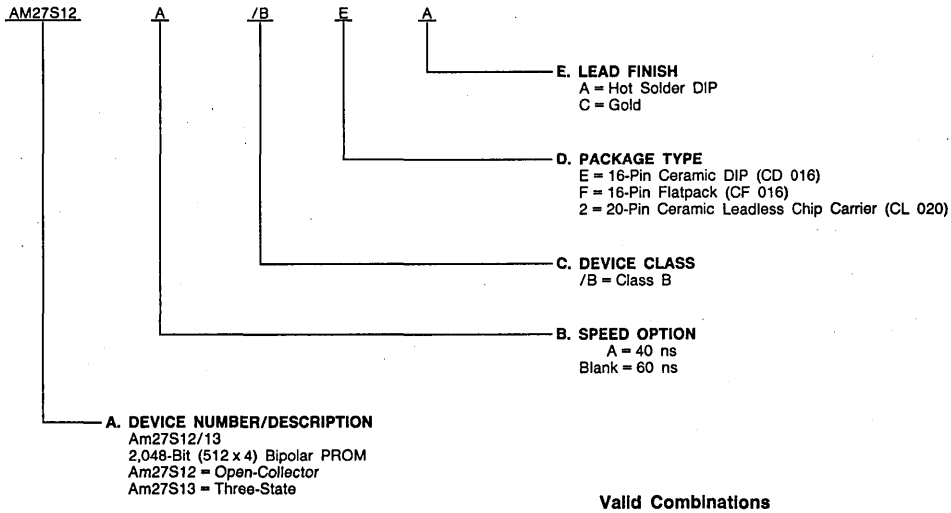
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S12	/BEA, /BFA, /B2C
AM27S12A	
AM27S13	
AM27S13A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_6$ Address Inputs
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G}$ Output Enable
Provides direct control of the Q output three-state buffers. Outputs disabled force all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}$

Disable = G

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Applying the Am27S12 and Am27S13

The Am27S12 and Am27S13 can be used with a high-speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output, causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12 or Am27S13 PROMs.

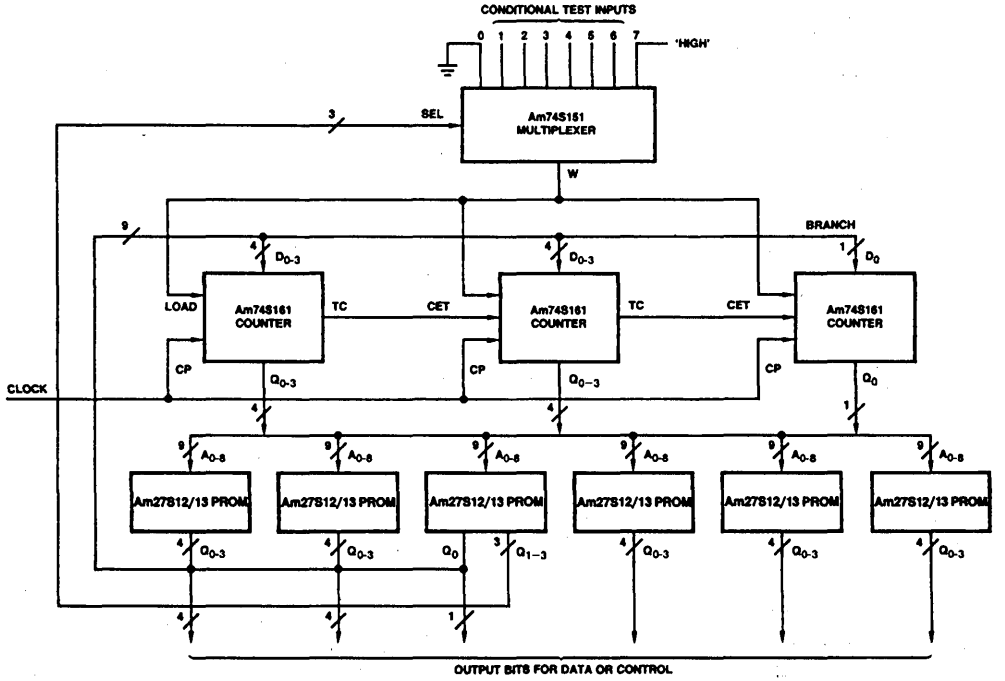


Figure 1. Typical Application for Am27S12/13

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military Parts 100% tested at −55, 25, and 125°C

2

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	μA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 3)			−20	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.				130	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. V_G = 2.4 V	(Note 1)	V_O = V_{CC}		40	μA
				V_O = 0.4 V		−40	

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

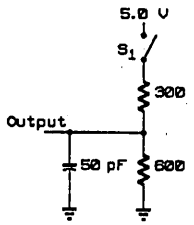
*See the last page of this spec for Group A Subgroup Testing information.

Capacitance

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz	4	pF
C_{OUT}	Output Capacitance		8	

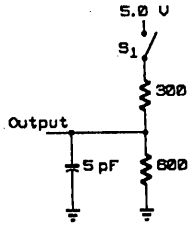
Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUITS



TC003441

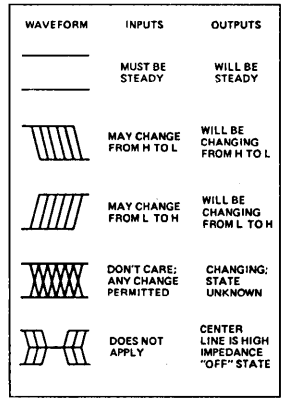
A. Output Load for all tests except TGVQZ



TC003451

B. Output Load for TGVQZ

KEY TO SWITCHING WAVEFORM



KS000010

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

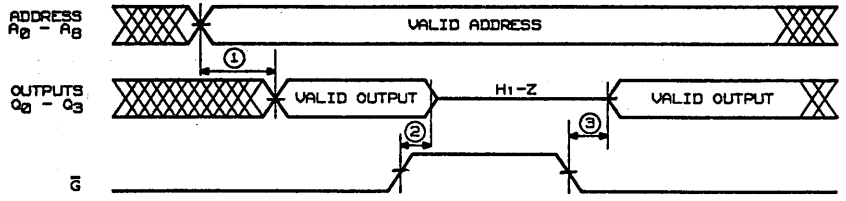
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		30		40		50		60	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuits.
Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V ouput levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021180

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S15

4096-Bit (512 x 8) Bipolar PROM
with Output Data Latches

DISTINCTIVE CHARACTERISTICS

- On-chip data latches
- Latched true and complemented output enables for easy word expansion
- Predetermined OFF outputs on power-up
- Fast access time — 60 ns commercial and 90 ns military maximum
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Member of generic PROM series utilizing standard programming algorithm

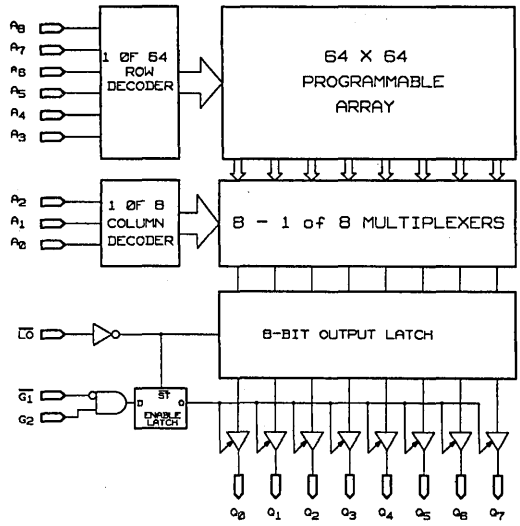
GENERAL DESCRIPTION

The Am27S15 (512-words by 8-bits) is a fully decoded, Schottky array, TTL Programmable Read-Only Memory (PROM), incorporating on-chip data and enable latches. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls.

This device will operate in a transparent mode when the Output Latch Enable signal (LO) is held HIGH. When the Output Latch Enable signal is LOW, the output conditions present at the time of the HIGH-to-LOW transition of LO will be latched into the part.

If LO is LOW upon power-up, the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



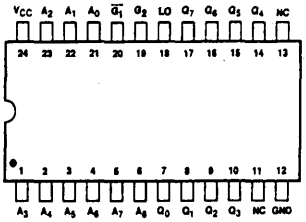
BD006290

PRODUCT SELECTOR GUIDE

Part Number	Am27S15	
Address Access Time	60ns	90ns
Operating Range	C	M

Publication # 03183 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

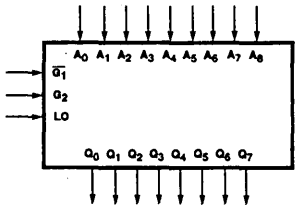


CD001011

Note: Pin 1 is marked for orientation. NC = No Connection.

2

LOGIC SYMBOL



LS000101

ORDERING INFORMATION (Cont'd.)
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option *(if applicable)*
C. Package Type
D. Temperature Range
E. Optional Processing

AM27S15 — D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

C. PACKAGE TYPE
P = 24-Pin Plastic DIP (PD 024)
D = 24-Pin Ceramic DIP (CD 024)

B. SPEED OPTION
Blank = 60 ns

A. DEVICE NUMBER/DESCRIPTION
Am27S15
4096-Bit (512 x 8) Bipolar PROM
with Output Data Latches

Valid Combinations	
AM27S15	PC, PCB, DC, DCB

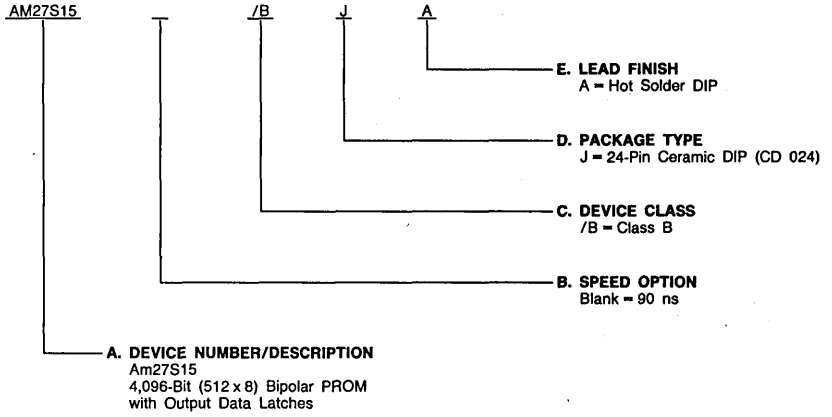
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S15	/BJA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address Inputs
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

LO Output Latch Enable
The LO signal controls both the data and enable latches. The LOW-to-HIGH transition of LO "Opens" the data and enable latches. The HIGH-to-LOW transition of LO "Closes" the data and enable latches.

$Q_0 - Q_7$ Data Output Port
Parallel data output from the data latches. The disabled state of these outputs is floating or high impedance.

$\overline{G_1}$, G_2 Output Enable
Controls the state of the Q-output, three-state drivers in conjunction with LO.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military products 100% tested at case temperature −55°C, +25°C, +125°C.

2

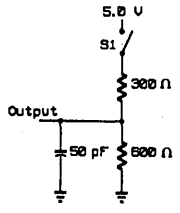
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7			Volts
			MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input Low Level	Guaranteed input logical LOW voltage for all inputs (Note 3)	COM'L			0.85	Volts
			MIL			0.80	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V	COM'L			−0.100	mA
			MIL			−0.150	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−70	mA
			MIL	−15		−65	
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.	COM'L			175	mA
			MIL			185	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max., V_{G1} = 2.4 V V_{G2} = 0.4 V	V_O = 4.5 V			40	µA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2)			8		

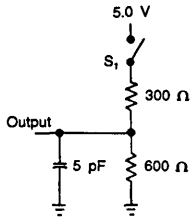
Notes: 1. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
2. These parameters are not 100% tested, but are periodically sampled.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS

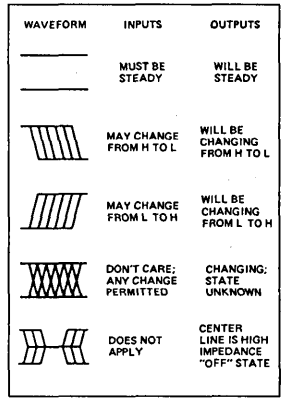


TC003442



TC003730

KEY TO SWITCHING WAVEFORMS



KS000010

A. Output Load for All AC Tests Except TGVQZ

B. Output Load for TGVQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)*

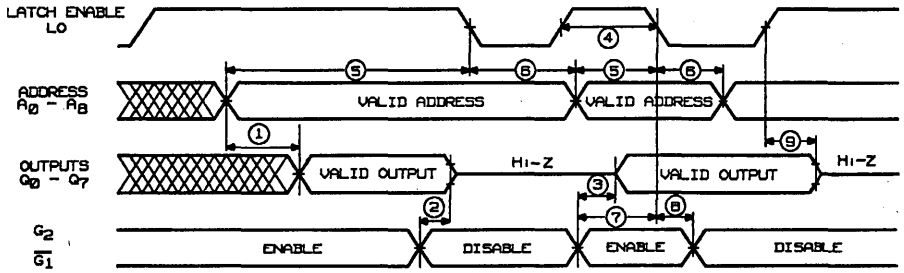
No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid		60		90	ns
2	TG1HQZ TG2LQZ	Delay from Output Enable (HIGH or LOW) to Output Hi-Z (Note 2)		40		50	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid (HIGH or LOW)		40		50	ns
4	TLOHLOL	Latch Enable Pulse Width (HIGH)	30		40		ns
5	TAVLOL	Address Valid to Latch Enable LOW Setup Time	60		90		ns
6	TLOLAX	Latch Enable LOW to Address Change Hold Time	0		5		ns
7	TGVLOL	Output Enable Valid to Latch Enable LOW Setup Time	40		50		ns
8	TLOLGX	Latch Enable LOW to Output Enable Change Hold Time	10		10		ns
9	TLOHQZ	Delay from LO HIGH to Output Disabled (Note 2)		35		45	ns

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TG1HQZ, TG2LQZ, and TLOHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORM



WF021651

2

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TG1HQZ TG2LQZ	9, 10, 11
3	TGVQV	9, 10, 11
4	TLOHLOL	9, 10, 11
5	TAVLOL	9, 10, 11
6	TLOLAX	9, 10, 11
7	TGVLOL	9, 10, 11
8	TLOLGX	9, 10, 11
9	TLOHQZ	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S18/19

256-Bit (32 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Ultra high speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High-programming yield
- Low-current PNP inputs
- High-current open collector and three-state outputs
- Fast chip select

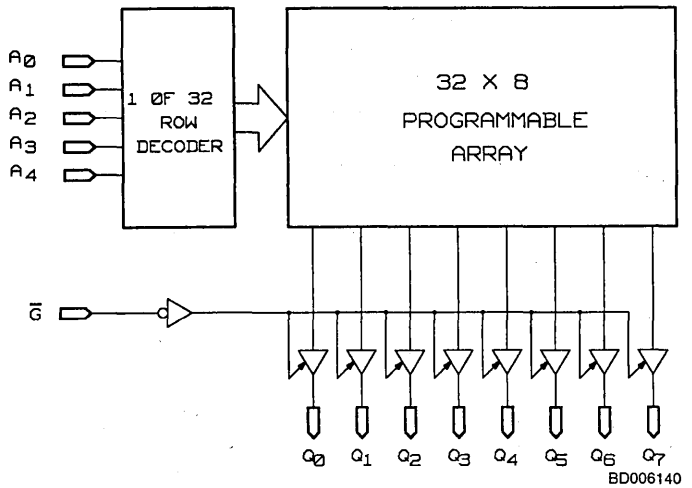
GENERAL DESCRIPTION

The Am27S18/19 (32-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S18) and three-state (Am27S19) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversions, or logic replacements. Easy word depth expansion is facilitated by an active LOW output enable ($\overline{G}$).

This device is also available in a low-power version Am27LS18/19.

BLOCK DIAGRAM



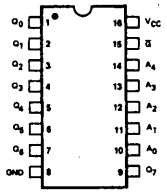
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	27S19SA		27S18A		27S18		27LS18	
Three-State Part Number	27S19SA		27S19A		27S19		27LS19	
Address Access Time	15 ns	20 ns	25 ns	35 ns	40 ns	50 ns	55 ns	70 ns
Operating Range	C	M	C	M	C	M	C	M

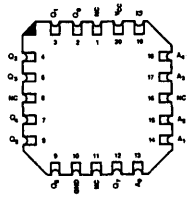
Publication # 03209 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

DIPs*



CD000521

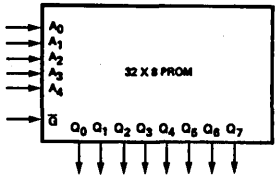


CD000531

Note: Pin 1 is marked for orientation.

*Also available in 16-pin flatpack. Connections identical to DIPs.

LOGIC SYMBOL



LS000072

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM27S19 SA D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

C. PACKAGE TYPE
P = 16-Pin Plastic DIP (PD 016)
D = 16-Pin Ceramic DIP (CD 016)
F = 16-Pin Flatpak (CF 016)
L = 20-Pin Ceramic Leadless Chip Carrier (CL 020)

B. SPEED OPTION
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
Am27S18/19
256-Bit (32 x 8) Bipolar PROM
Am27S18 = Open-Collector
Am27S19 = Three-Sate

Valid Combinations	
AM27S18/19	PC, PCB, DC, DCB, FC, FCB, LC, LCB
AM27S18A/19A	
AM27S19SA	
AM27LS18/19	

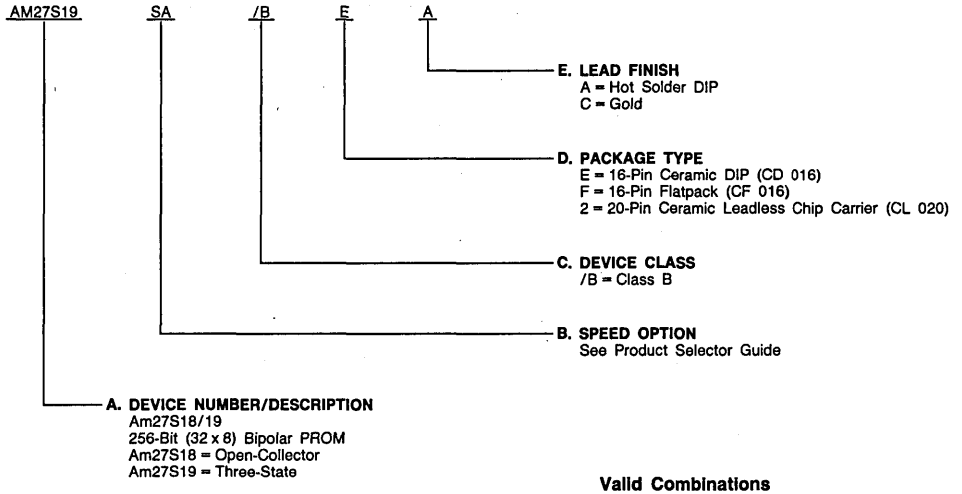
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S18/19	/BEA, /BFA, /B2C
AM27S18A/19A	
AM27S19SA	
AM27LS18/19	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_4$ Address Inputs
The 5-bit field presented at the address inputs selects one of 32 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The outputs whose state represents the data read from the selected memory locations

$\overline{G}$ Output Enable
Provides direct control of the Q output three-state buffers. Outputs disabled forces all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}$

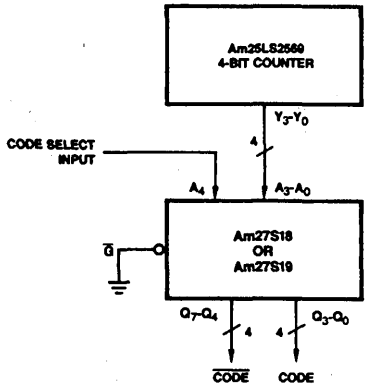
Disable = G

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

The Am27S18 and Am27S19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal of BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18 or Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



AF000161

TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

AF000170

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... −0.5 V to 5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military products 100% tested at −55°C, 25°C and 125°C.

2

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	μA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 3)			−20	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.		27S Devices		115	mA
				27LS Devices		80	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}}$ = 2.4 V	Note 1	V_O = V_{CC}		40	μA
				V_O = 0.4 V		−40	

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

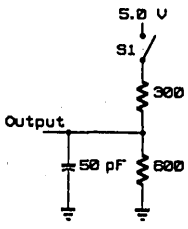
*See the last page of this spec for Group A Subgroup Testing information.

Capacitance

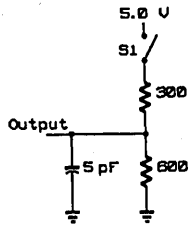
Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz	4	pF
C_{OUT}	Output Capacitance		8	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUITS

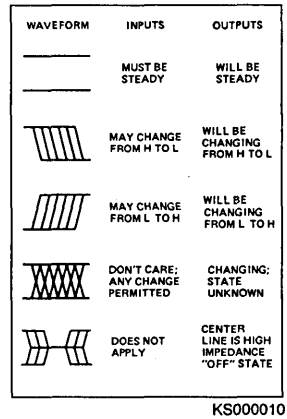


TC003440



TC003450

KEY TO SWITCHING WAVEFORMS



KS000010

A. Output Load for all tests except TGVQZ

B. Output Load for TGVQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

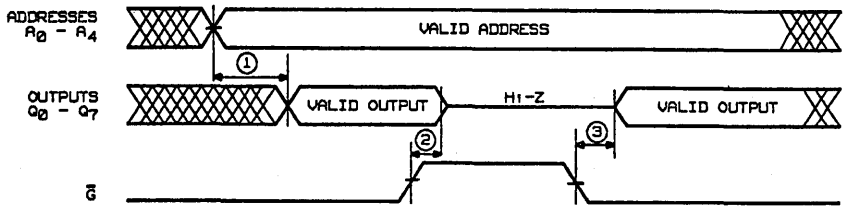
No.	Parameter Symbol	Parameter Description	Version	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	SA		15		20	ns
			A		25		35	
			STD		40		50	
			LS		55		70	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	SA		13		20	ns
			A		20		25	
			STD		25		30	
			LS		40		50	
3	TGVQV	Delay from Output Enable Valid to Output Valid	SA		13		20	ns
			A		20		25	
			STD		25		30	
			LS		40		50	

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021160

2

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S180/27S181/PS181
Am27S280/27S281/PS281

8,192-Bit (1024 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Rapid recovery from power-down state provides minimum delay

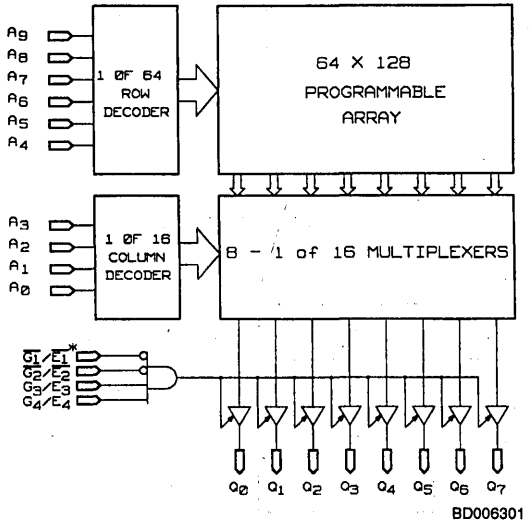
GENERAL DESCRIPTION

The Am27S180/27S181 (1024 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S180) and three-state (Am27S181) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by both active LOW ($\overline{G_1}$ and $\overline{G_2}$) and active HIGH (G_3 and G_4) output enables.

This device is also available in a 300-mil. lateral-center DIP (Am27S280/27S281), as well as a power-switched three-state version (Am27PS181/27PS281).

BLOCK DIAGRAM



*E nomenclature applies to the power-switched versions only (Am27PSXX).

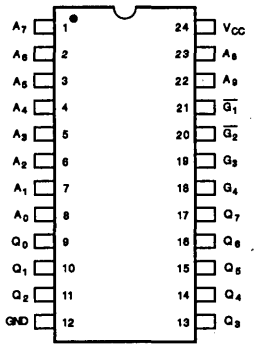
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	Am27S180A, Am27S280A		Am27S180, Am27S280		-		-	
Three-State Part Number	Am27S181A, Am27S281A		Am27S181, Am27S281		Am27PS181A, Am27PS281A		Am27PS181 Am27PS281	
Address Access Time	35 ns	50 ns	60 ns	80 ns	50 ns	65 ns	65 ns	75 ns
Operating Range	C	M	C	M	C	M	C	M

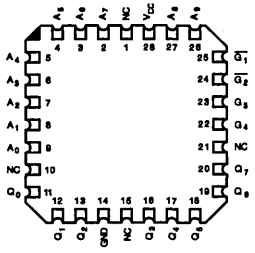
Publication # 03182 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

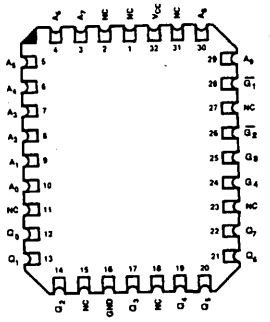
DIP*



CD000791



CD009561

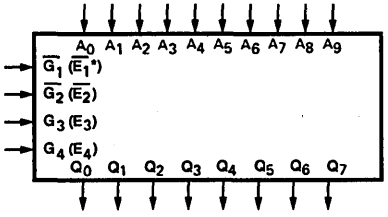


CD000821

*Also offered in a 300-mil DIP and a 24-pin Flatpack. Connections are identical to those listed here for the 600-mil DIP.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS000191

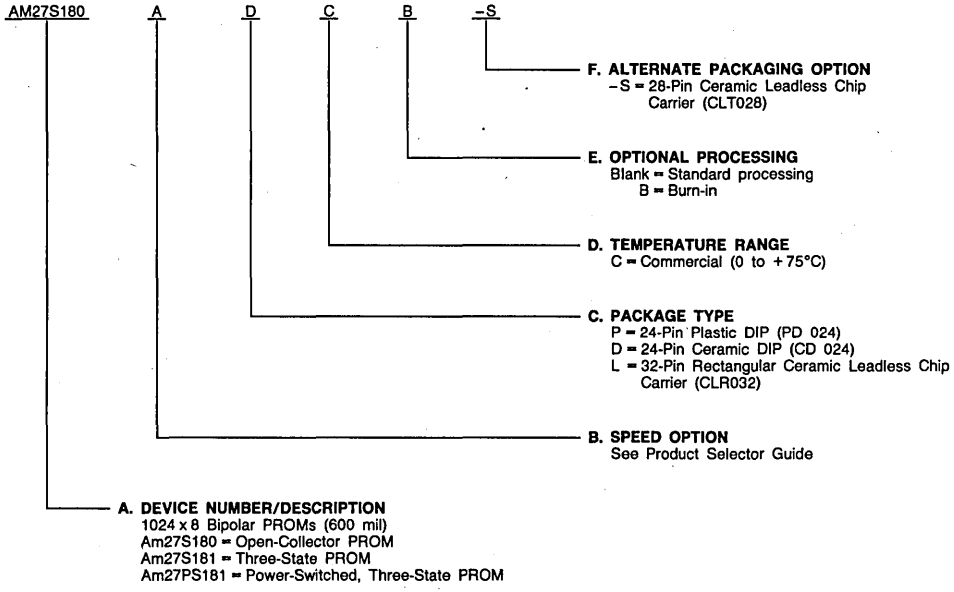
*E nomenclature applies to AM27PS-power switched versions only.

ORDERING INFORMATION (Cont'd.)

Am27S180/27S181/27PS181

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S180	PC, PCB, DC, DCB, LC, LCB, LC-S LCB-S
AM27S180A	
AM27S181	
AM27S181A	
AM27PS181	
Am27PS181A	

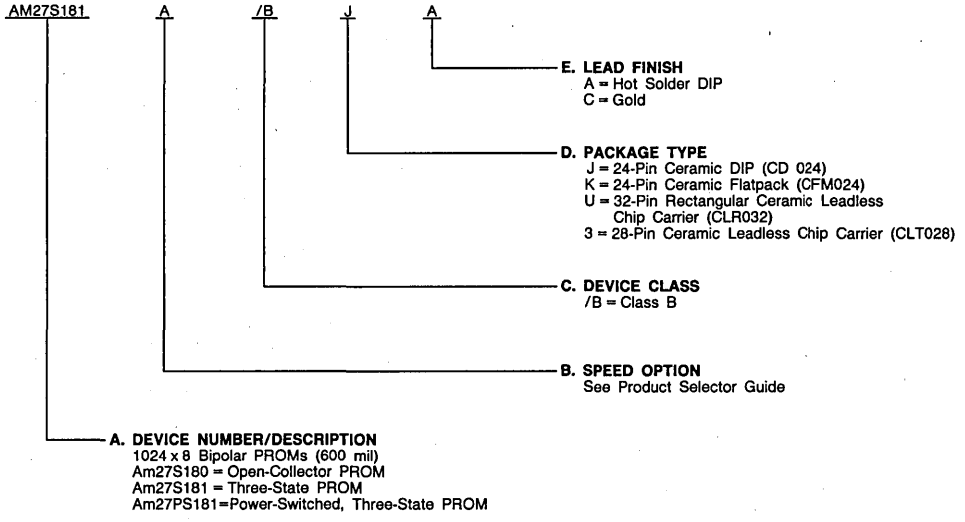
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S180	/BJA, /BKA, /BUC, /B3C,
AM27S180A	
AM27S181	
AM27S181A	
AM27PS181	
AM27PS181A	

Valid Combinations

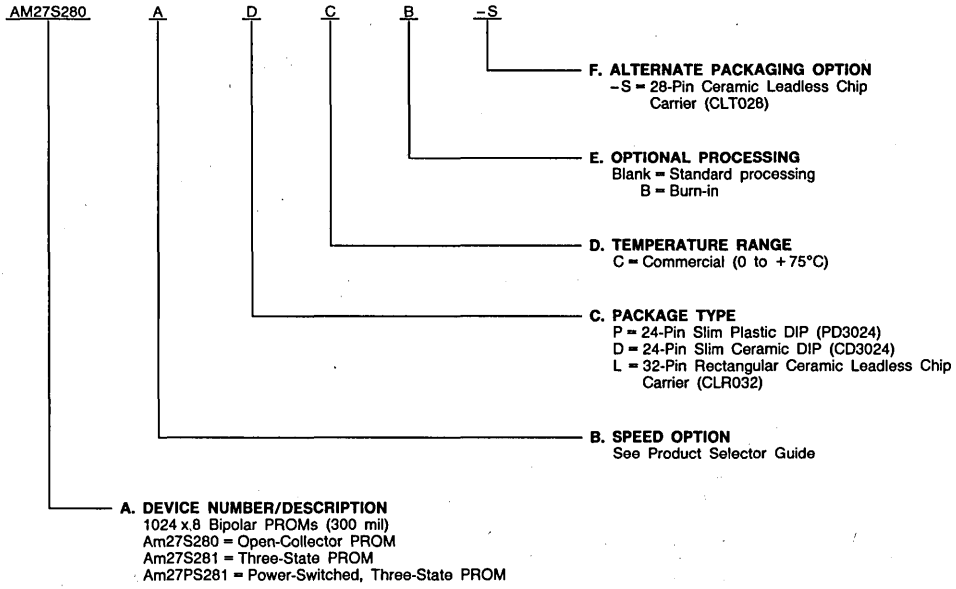
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ORDERING INFORMATION

Am27S280/27S281/27PS281

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S280	PC, PCB, DC, DCB, LC, LCB, LC-S, LCB-S
AM27S280A	
AM27S281	
AM27S281A	
AM27PS281	
Am27PS281A	

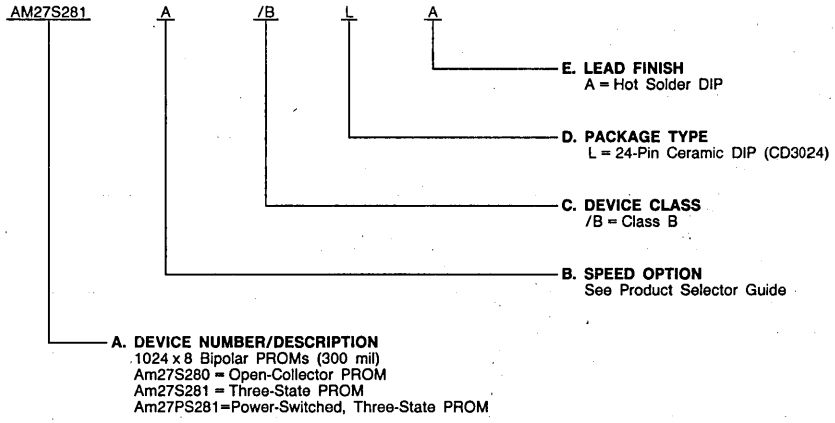
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S280	/BLA
AM27S280A	
AM27S281	
AM27S281A	
AM27PS281	
AM27PS281A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

FUNCTIONAL DESCRIPTION

Notes on Power Switching

The Am27PS181 and Am27PS281 are power switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS181 and Am27PS281 are selected, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 1.)

2. Address access time (TAVQV) can be optimized if a chip enable setup time (TEVAV) of greater than 25 ns is observed. Negative setup times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

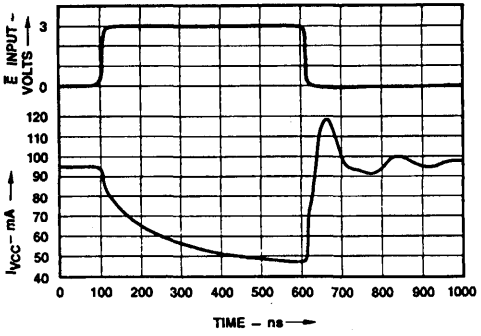
Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−90	mA
			MIL	−15		−90	
I_{CC}	Power Supply Current	All Inputs = GND				185	mA
I_{CCD}	Power-Down Supply Current	$\overline{E_1}$ = 2.7 V	All other inputs = GND			80	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G_1}}$ = 2.4 V	V_O = V_{CC}			40	µA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2)			8.0		

Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.
2. These parameters are not 100% tested, but are periodically sampled.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

*See the last page of this spec for Group A Subgroup Testing information.

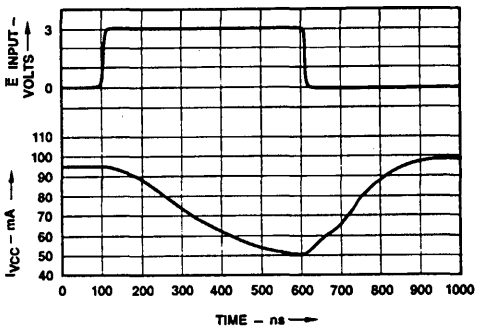
TYPICAL DC and AC CHARACTERISTICS

Typical I_{VCC} Current Surge without 0.1 μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



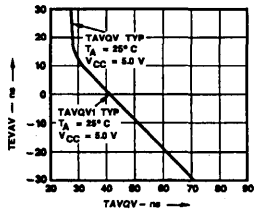
OP001221

Typical I_{VCC} Current Surge with 0.1 μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



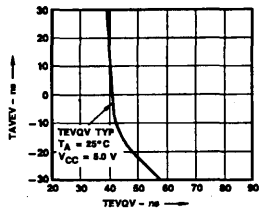
OP001231

Figure 1. I_{CC} Current



OP001112

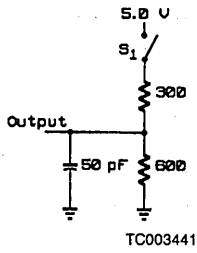
Figure 2A. TAVQV versus TEVAV



OP001122

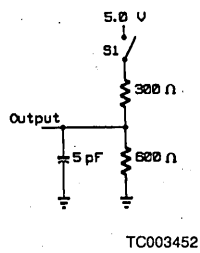
Figure 2B. TEVQV versus TAVEV

SWITCHING TEST CIRCUITS



TC003441

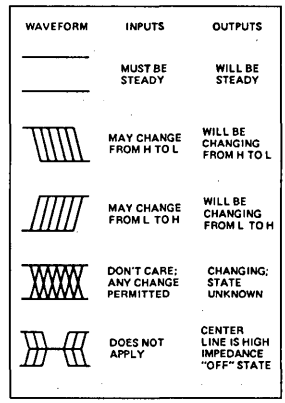
Diagram 1. Output Load for all Switching tests except TGVQZ



TC003452

Diagram 2. Output Load for TGVQZ

KEY TO SWITCHING WAVEFORMS



KS000010

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.
S_1 is closed for all other Switching tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

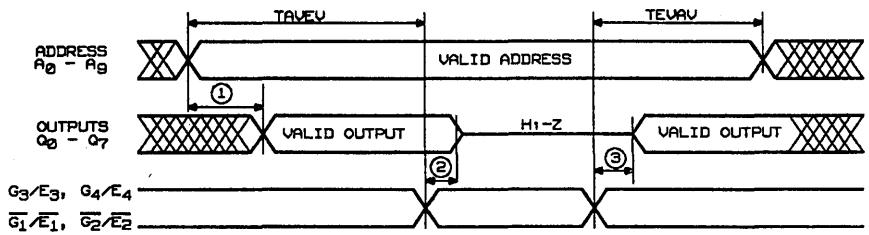
No.	Parameter Symbol	Parameter Description	Version	Am27S Version COM'L Max.	Am27S Version MIL Max.	Am27PS Version COM'L Max.	Am27PS Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	A	35	50	50	65	ns
			STD	60	80	65	75	
2	TGVQZ TEVQZ	Delay from Output Enable Valid to Output Hi-Z	A	25	30	25	30	ns
			STD	40	50	35	45	
3	TGVQV TEVQV	Delay from Output Enable Valid to Output Valid	A	25	30	65	75	ns
			STD	40	50	80	90	
4	TAVQV1	Power-Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A			65	75	ns
			STD			80	90	

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Diagram 1.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage + 0.5 V output levels using the test load in Diagram 2.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORM



WF021681

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CCD}*	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
2	TEVQZ	9, 10, 11
3	TGVQV	9, 10, 11
3	TEVQV	9, 10, 11
4	TAVQV1*	9, 10, 11
5	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

*Power-switched versions only (Am27PSXXX)

Am27S184/185/PS185

8,192-Bit (2048 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time "A" version (35 ns Max.) — Fast access time Standard version (50 ns Max.) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

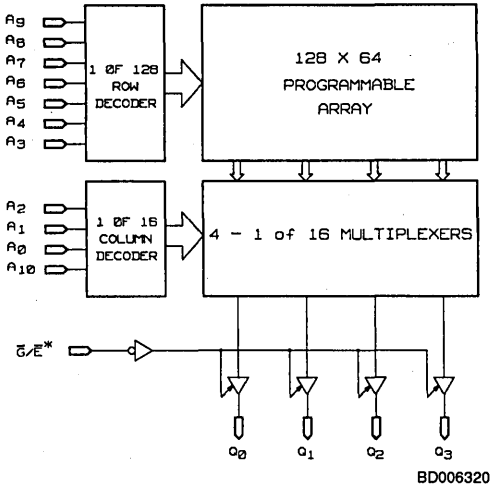
GENERAL DESCRIPTION

The Am27S184/185 (2048-words by 4-bits) is a Schottky TTL Programable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S184) and three-state (Am27S185) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy-word depth expansion is facilitated by an active LOW ($\overline{G}$) output enable.

This device is also offered in a low-power, three-state version, the Am27LS185, as well as a power-switched three-state version.

BLOCK DIAGRAM



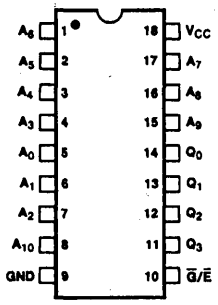
BD006320

PRODUCT SELECTOR GUIDE

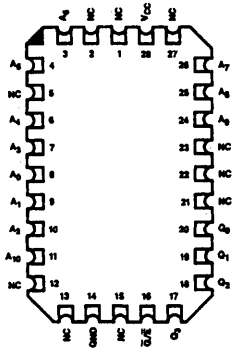
Open-Collector Part Number	27S184A		27S184					
Three-State Part Number	27S185A		27S185		27LS185		27PS185	
Address Access Time	35 ns	45 ns	50 ns	55 ns	60 ns	65 ns	50 ns	55 ns
Operating Range	C	M	C	M	C	M	C	M

Publication # 03192 | Rev. C | Amendment /0
Issue Date: May 1986

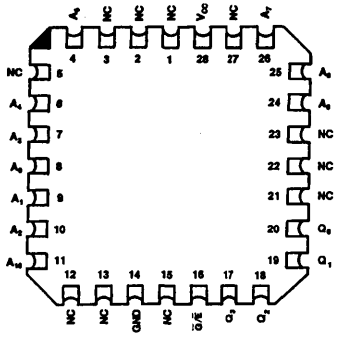
CONNECTION DIAGRAMS
Top View



CD000372



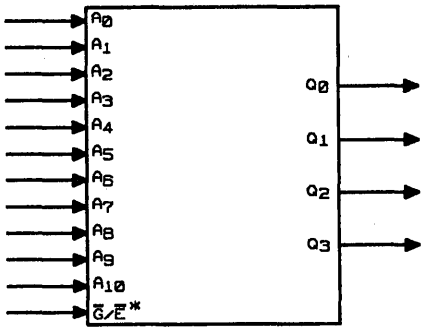
CD000382



CD009500

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



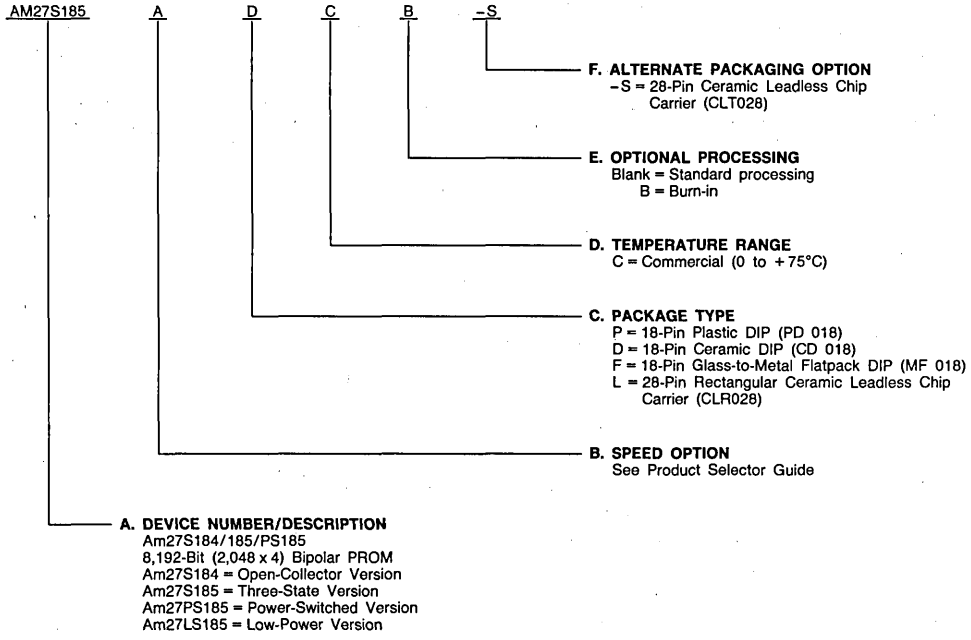
LS002410

*E nomenclature applies only to Am27PS power-switched versions.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S184	PC, PCB, DC DCB, FC, FCB, LC, LCB, LC-S, LCB-S
AM27S184A	
AM27S185	
AM27S185A	
AM27PS185	PC, PCB, DC, DCB, LC, LCB, LC-S, LCB-S
AM27LS185	

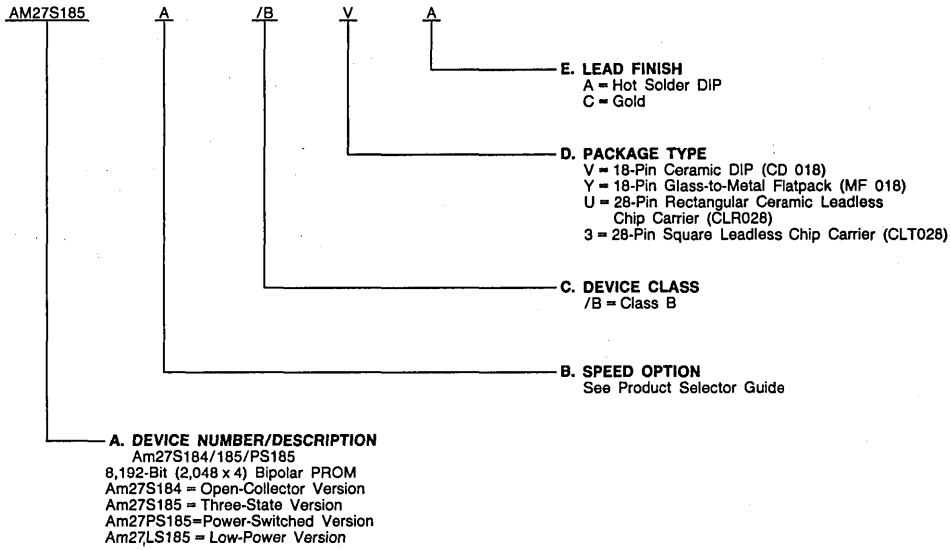
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S184	/BVA, /BYC, /BUC, /B3C,
AM27S184A	
AM27S185	
AM27S185A	
AM27PS185	
AM27LS185	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{10}$ Address Inputs
The 11-bit field presented at the address inputs selects one of 2,048 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G}/\overline{E}$* Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}$/E*
Disable = G/E*

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Power Switching

The Am27PS185 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS185 is selected by a low level on $\overline{CS}$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1 μf ceramic capacitor be connected from pin 18 to pin 9 at each device. (See Figure 1.)

2. Address access time (TAVQV1) can be optimized if a chip enable set-up time (TEVAV) of greater than 25 ns is observed. Negative set-up times on chip enable (TEVAV=tl0) should be avoided. (For typical and worse case characteristics see Figures 2A and 2B.)

*$\overline{E}$ Nomenclature applies only to Am27PS power-switched versions.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

2

DC CHARACTERISTICS over operating range unless otherwise specified*

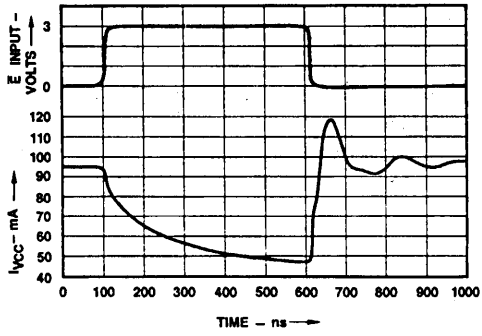
Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	µA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0.0 V (Note 3)	STD, LS devices	−20		−90	mA
			PS devices	−15		−90	
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.	STD, PS devices			150	mA
			LS devices			125	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}}$ = 2.4 V	V_O = V_{CC}			40	µA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4)			8.0		

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

*See the last page of this spec for Group A Subgroup Testing information.

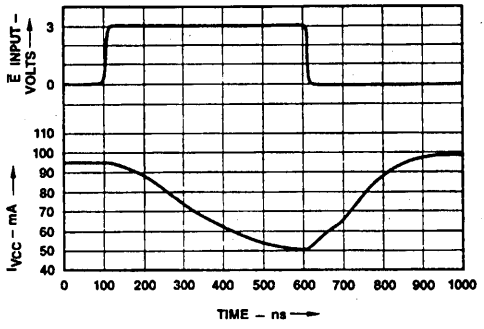
TYPICAL DC and AC CHARACTERISTICS

Typical I_{VCC} Current Surge without 0.1 μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



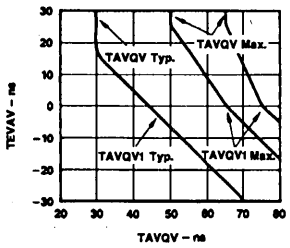
OP001221

Typical I_{VCC} Current Surge without 0.1 μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



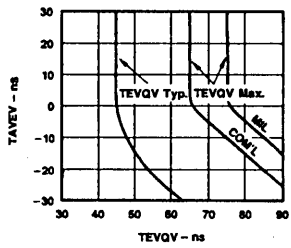
OP001231

Figure 1. I_{CC} Current



OP001191

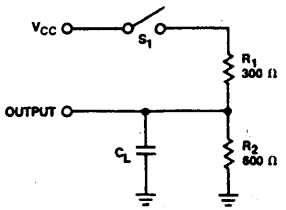
Figure 2A. TAVQV vs TEVAV (Am27PS191/291)



OP001201

Figure 2B. TEVQV vs TAVEV

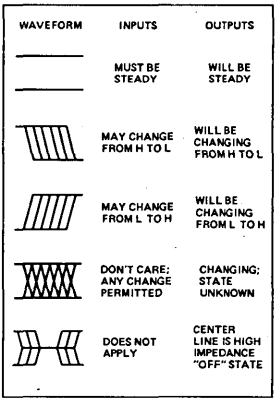
SWITCHING TEST CIRCUIT



TC000171

Notes: 1. TAVQV is tested with switch S_1 closed and C_L = 50 pF.
2. For open-collector outputs, TGVQZ and TGVQV are tested with S_1 closed to the 1.5 V output level. C_L = 50 pF.
3. For three-state outputs, TGVQZ is tested with C_L = 50 pF to the 1.5 V level: S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQV is tested with C_L = 5 pF. HIGH to high-impedance tests are made to an output steady state HIGH voltage −0.5 V with S_1 open; LOW to high-impedance tests are made to the steady state LOW +0.5 V level with S_1 closed.

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

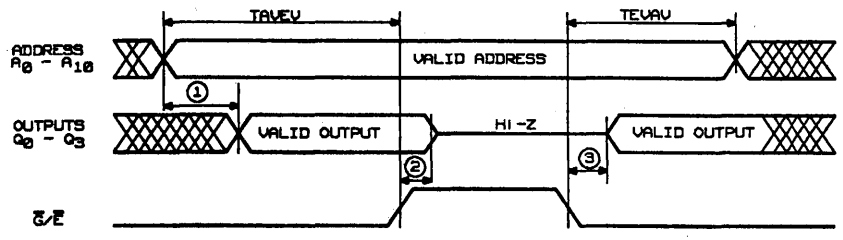
No.	Parameter Symbol	Parameter Description	Version	27S Version COM'L Min.	27S Version COM'L Max.	27S Version MIL Min.	27S Version MIL Max.	27PS Version COM'L Min.	27PS Version COM'L Max.	27PS Version MIL Min.	27PS Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	A		35		45					ns
			STD		50		55		50		55	
			LS		60		65					
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A		25		30					ns
			STD		25		30		25		30	
			LS		25		30					
3	TGVQV	Delay from Output Enable Valid to Output Valid	A		25		30					ns
			STD		25		30		60		65	
			LS		25		30					
4	TAVQV1	Power Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A									ns
			STD						60		65	

See also Switching Test Circuit.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021620

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
4	TAVQV1	9, 10, 11
5	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S190/27S191/PS191/LS191
Am27S290/27S291/PS291/LS291

16,384-Bit (2048 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction (27PS devices)
- Plug in replacement for industry standard product — no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Rapid recovery from power-down state provides minimum delay (27PS devices)

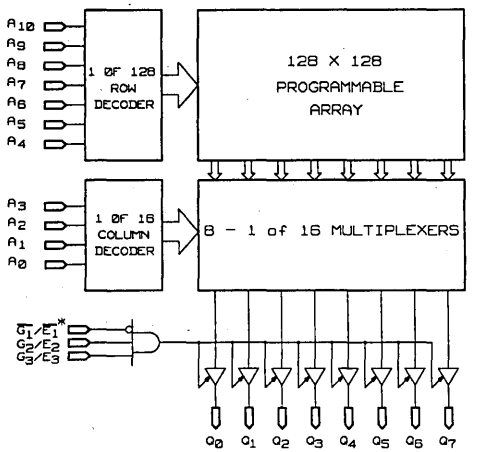
GENERAL DESCRIPTION

The Am27S190/191 (2048-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S190) and three-state (Am27S191) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by both active LOW ($\overline{G_1}$) and active HIGH (G_2 and G_3) output enables.

This device is also available in 300-mil, lateral center DIP (Am27S290/27S291). Additionally, this device is offered in a low-power, three-state version, the Am27LS191 and Am27LS291, as well as a power-switched, three-state version, the Am27PS191 and Am27PS291.

BLOCK DIAGRAM



*E nomenclature applies to the power-switched versions only (Am27PSXXX).

PRODUCT SELECTOR GUIDE

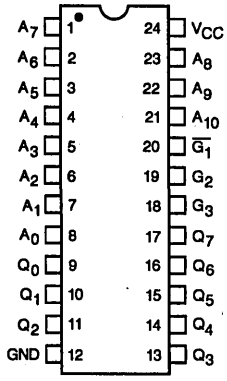
Open-Collector Part Number	-		Am27S190A, Am27S290A		Am27S190, Am27S290		-		-		-	
Three-State Part Number	Am27S191SA, Am27S291SA		Am27S191A, Am27S291A		Am27S191, Am27S291		Am27LS191*, Am27LS291*		Am27PS191A, Am27PS291A		Am27PS191, Am27PS291	
Address Access Time (ns)	20	30	35	50	50	65	35	45	50	65	65	75
Operating Range	C	M	C	M	C	M	C	M	C	M	C	M

*Advance Information applies only to "SA" version.

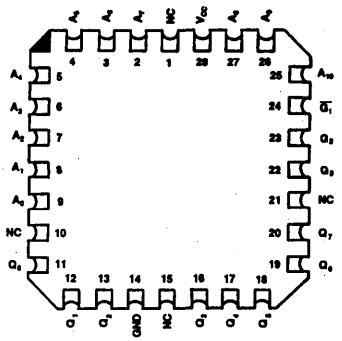
Publication # 02121 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

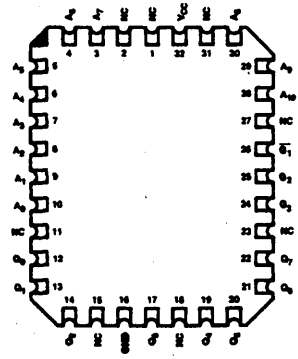
DIP*



CD000391



CD009510

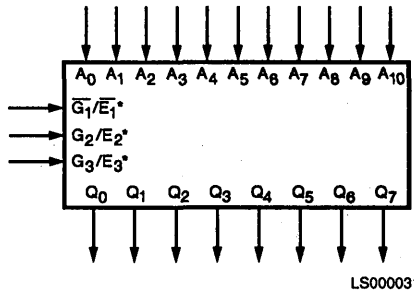


CD000401

*Also offered in a 300-mil DIP and a 24-pin Flatpack. Connections are identical to those listed here for the 600-mil DIP.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS000031

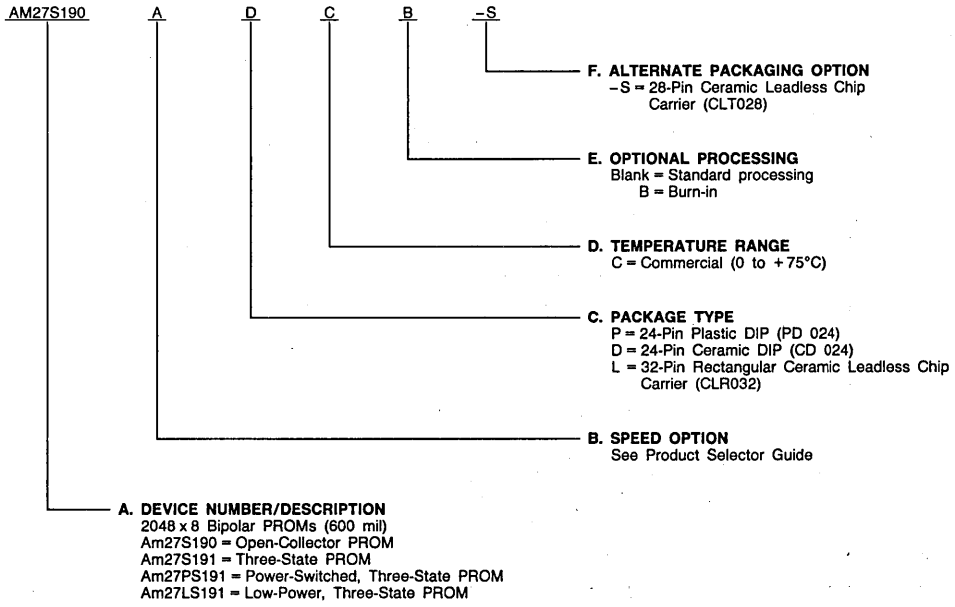
*E nomenclature applies to the power-switched versions only (Am27PSXXX).

ORDERING INFORMATION (Cont'd.)

(Am27S190/27S191/27PS191/27LS191)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S190	PC, PCB, DC, DCB, LC, LCB, LC-S, LCB-S
AM27S190A	
AM27S191	
AM27S191A	
AM27S191SA	
AM27PS191	
AM27PS191A	
AM27LS191A	

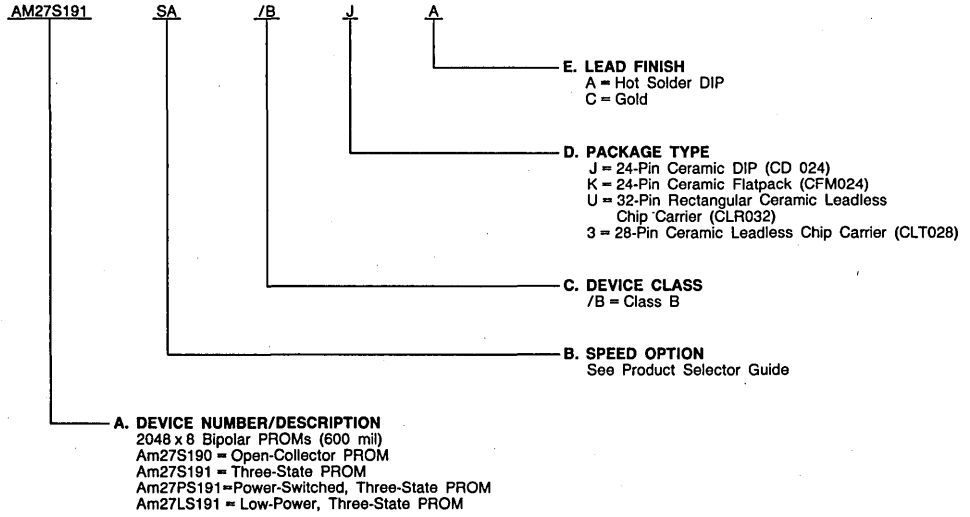
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S190	/BJA, /BKA, /BUC, /B3C
AM27S190A	
AM27S191	
AM27S191A	
AM27S191SA	
AM27PS191	
AM27PS191A	
AM27LS191A	

Valid Combinations

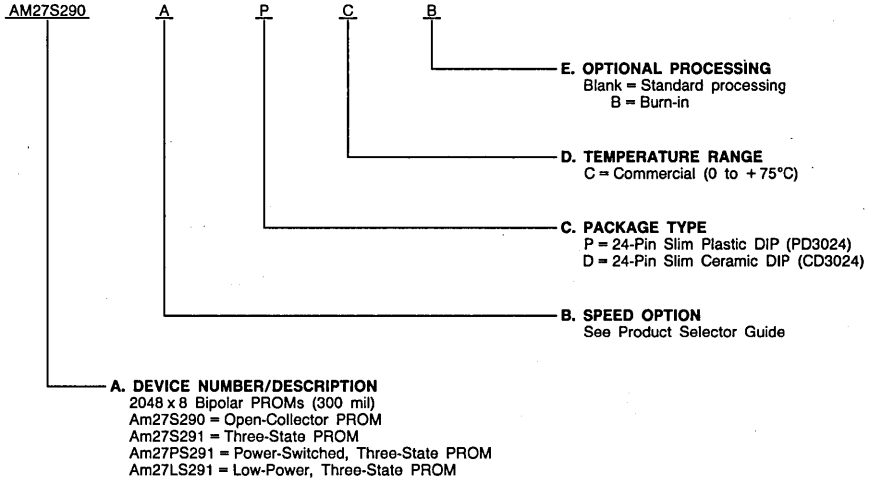
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ORDERING INFORMATION

(Am27S290/27S291/27PS291/27LS291)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S290	PC, PCB, DC, DCB
AM27S290A	
AM27S291	
AM27S291A	
AM27S291SA	
AM27PS291	
AM27PS291A	
AM27LS291A	

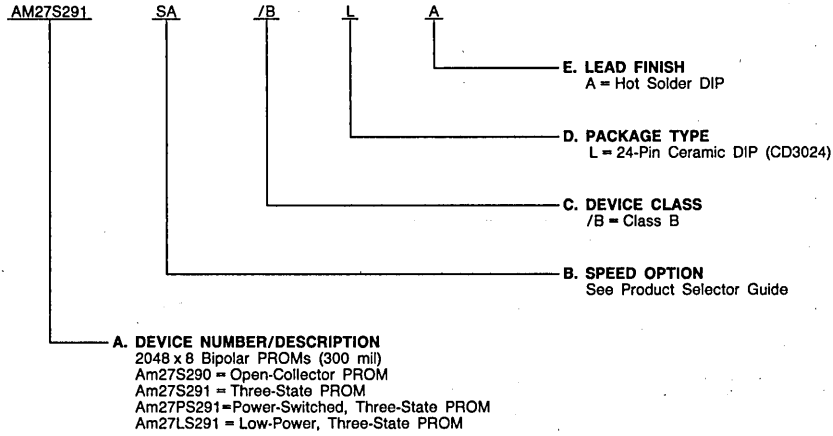
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S290	/BLA
AM27S290A	
AM27S291	
AM27S291A	
AM27S291SA	
AM27PS291	
AM27PS291A	
AM27LS291A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{10}$ Address Inputs
The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, G_2, G_3 Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an "OFF" state and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \bullet G_2 \bullet G_3$$

$$\text{Disable} = \overline{G_1} \bullet G_2 \bullet G_3 = G_1 + \overline{G_2} + \overline{G_3}$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Notes on Power Switching

The Am27PS191 and Am27PS291 are power-switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS191 and Am27PS291 are selected, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 1.)

2. Address access time (TAVQV) can be optimized if a chip enable set-up time (TEVAV) of greater than 25ns is observed. Negative set-up times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = 25°C, 125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

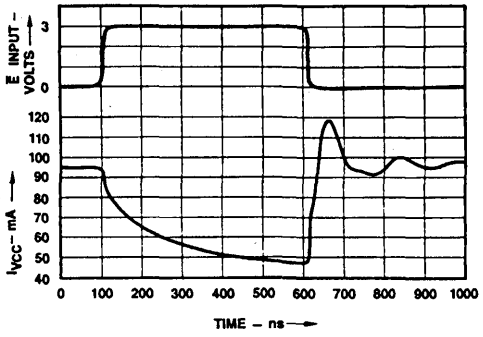
Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−90	mA
			MIL	−15		−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.	27S Devices			185	mA
			27LS Devices			90	
I_{CCD} (27PS Devices Only)	Power Down Supply Current	All inputs = GND				80	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{GT}}$ = 2.4 V	V_O = V_{CC}			40	µA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2)			8.0		

Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.
2. These parameters are not 100% tested, but are periodically sampled.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

*See the last page of this spec for Group A Subgroup Testing information.

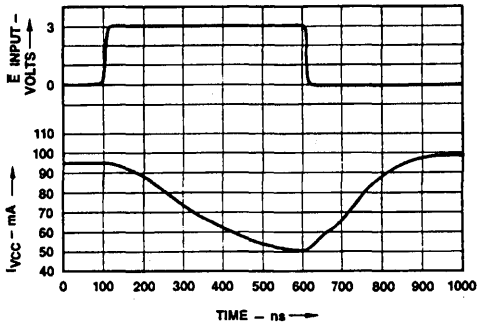
TYPICAL DC and AC OPERATING CHARACTERISTICS

Typical I_{VCC} Current Surge without 0.1 μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



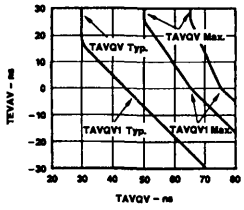
OP001221

Typical I_{VCC} Current Surge without 0.1 μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



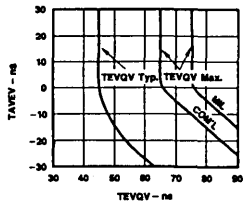
OP001231

Figure 1. I_{CC} Current



OP001191

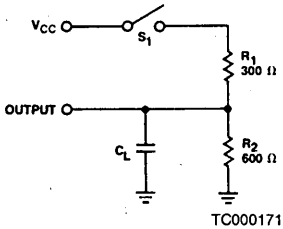
Figure 2A. TAVQV vs TEVAV (Am27PS191/291)



OP001201

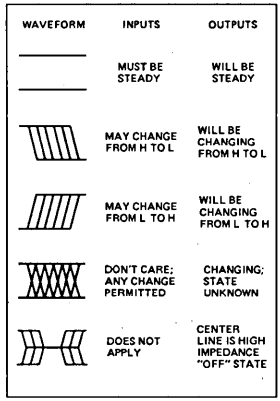
Figure 2B. TEVQV vs TAVEV

SWITCHING TEST CIRCUIT



TC000171

KEY TO SWITCHING WAVEFORMS



KS000010

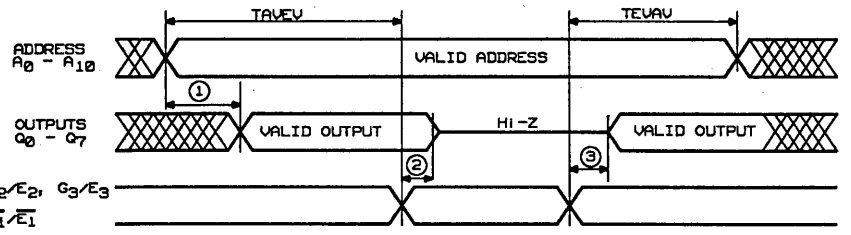
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Version	Am27S Version COM'L Max.	Am27S Version MIL Max.	Am27PS Version COM'L Max.	Am27PS Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	SA*	20	30			ns
			A	35	50	50	65	
			STD	50	65	65	75	
			LS	35	45			
2	TGVQZ TEVQZ	Delay from Output Enable Valid to Output Hi-Z	SA*	15	20			ns
			A	25	30	25	30	
			STD	25	30	35	45	
			LS	20	25			
3	TGVQV TEVQV	Delay from Output Enable Valid to Output Valid	SA*	15	20			ns
			A	25	30	65	75	
			STD	25	30	80	90	
			LS	20	25			
4	TAVQV1	Power-Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A			65	75	ns
			STD			80	90	

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels.
3. TAVQV is tested with switch S_1 closed and $C_L = 50$ pF.
4. TGVQV is tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. TGVQZ is tested with $C_L = 5$ pF. HIGH to high impedance tests are made with S_1 open to an output voltage of steady state HIGH −0.5 V with S_1 open; LOW-to-high impedance tests are made to the steady state LOW +0.5 V level with S_1 closed.

SWITCHING WAVEFORMS



WF021570

*See the last page of this spec for Group A Subgroup Testing information.

*Advance Information

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups	Parameter Symbol	Subgroups
V_{OH}	1, 2, 3	I_{IH}	1, 2, 3
V_{OL}	1, 2, 3	I_{SC}	1, 2, 3
V_{IH}	1, 2, 3	I_{CC}	1, 2, 3
V_{IL}	1, 2, 3	I_{CEX}	1, 2, 3
I_{IL}	1, 2, 3	I_{CCD}*	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
2	TEVQZ	9, 10, 11
3	TGVQV	9, 10, 11
3	TEVQV	9, 10, 11
4	TAVQV1*	9, 10, 11
	Functional Tests	7, 8

*Power-switched versions only (Am27PSXXX).

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S20/21

1,024-Bit (256 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

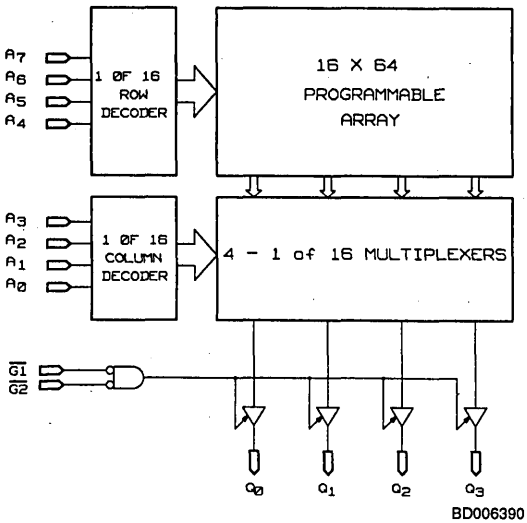
- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

The Am27S20/21 (256 words by 4-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S20) and three-state (Am27S21) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code version, or logic replacement. Easy word-depth expansion is facilitated by active LOW ($\overline{G_1}$ and $\overline{G_2}$) output enables.

BLOCK DIAGRAM



BD006390

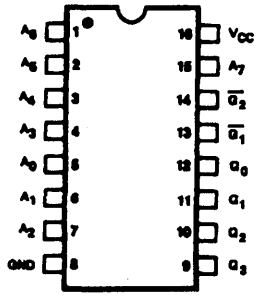
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	27S20A		27S20	
Three-State Part Number	27S21A		27S21	
Address Access Time	30 ns	40 ns	45 ns	60 ns
Operating Range	C	M	C	M

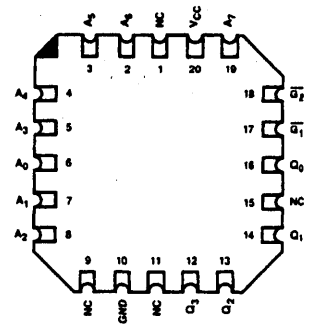
Publication # 03206 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

DIPs*



CD000571

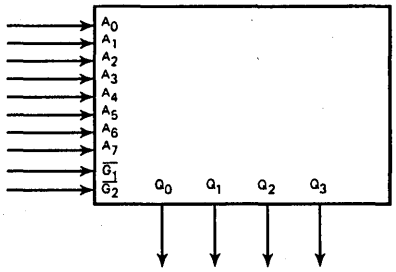


CD000581

*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

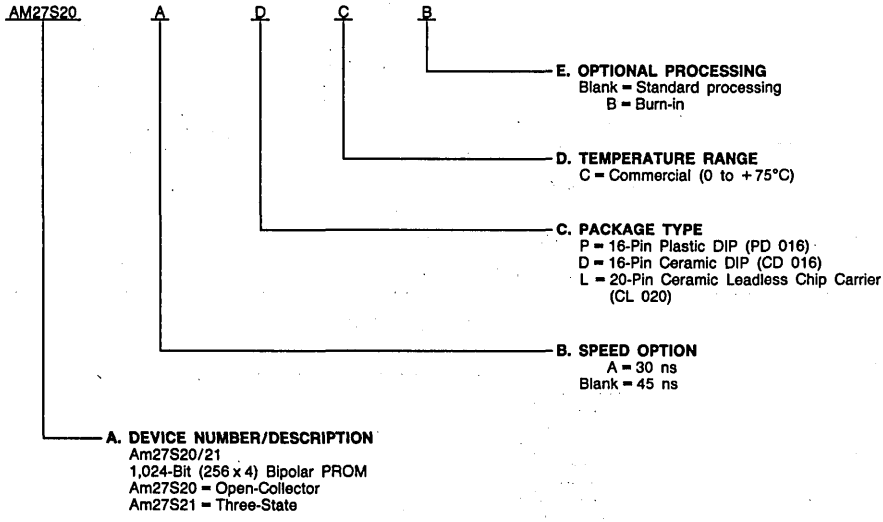


LS000081

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S20	DC, DCB, PC, PCB, LC, LCB
AM27S20A	
AM27S21	
AM27S21A	

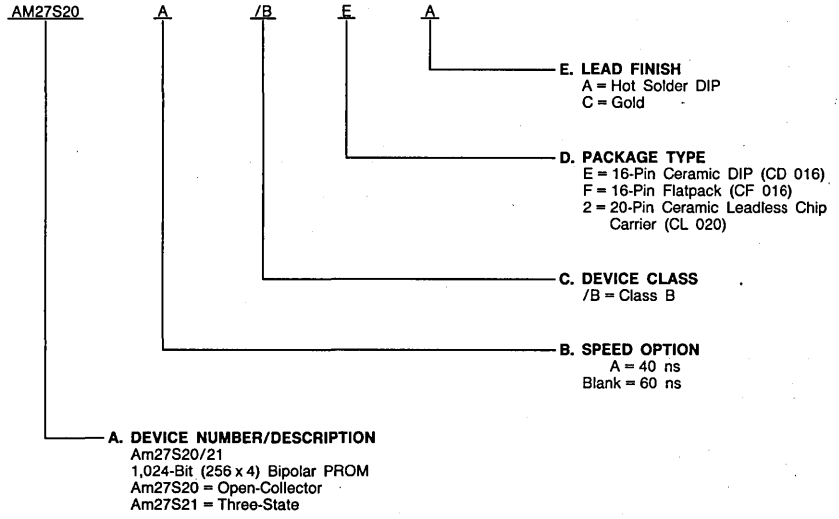
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S20	/BEA, /BFA /B2C
AM27S20A	
AM27S21	
AM27S21A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_7$ Address Inputs (Inputs)
The 8-bit field presented at the address inputs selects one of 256 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port (Outputs)
The output whose state represents the data read from the selected memory locations.

$\overline{G_1}$, $\overline{G_2}$ Output Enable
Provides direct control of the Q output buffers. Outputs disabled force all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2}$$

$$\text{Disable} = \overline{G_1 \cdot G_2} = G_1 + G_2$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Applying The Am27S20 and Am27S21

Typical application of the Am27S20 and Am27S21 is shown below. The Am27S20 and the Am27S21 are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the $A_0 - A_7$ inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{G_1}$ input of the Am27S20/21 such that when the $\overline{G_1}$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20 or in the three-state mode in the case of the Am27S21. In both cases the $\overline{G_2}$ input is grounded; thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.

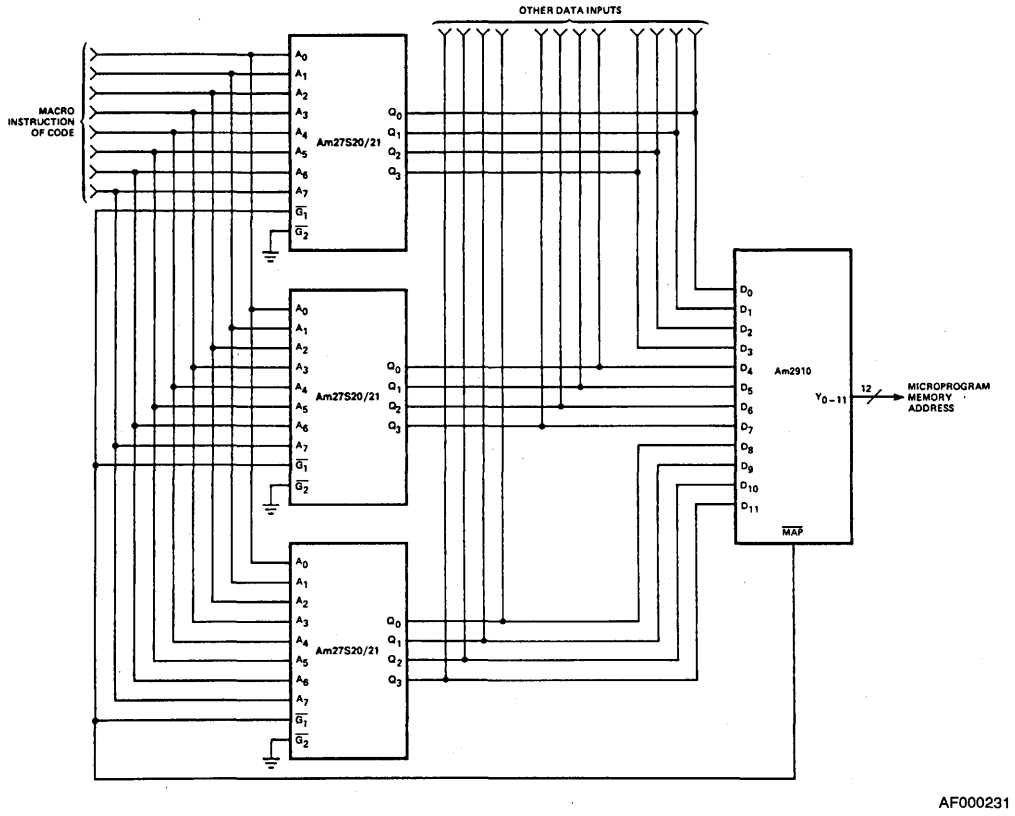


Figure 1. Microprogramming Instruction Mapping

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature (T_C) ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at −55°C, 25°C, and 125°C.

2

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	μA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V (Note 3)			−20	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.			130	mA	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max., V_{G_1} = 2.4 V		V_O = V_{CC}			μA
			(Note 1)	V_O = 0.4 V			

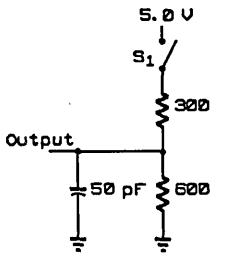
Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

* See the last page of this spec for Group A Subgroup Testing information.

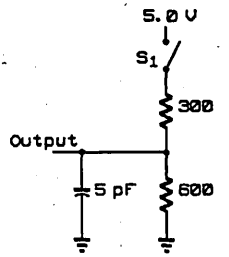
Capacitance

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz	4	pF
C_{OUT}	Output Capacitance		8	

SWITCHING TEST CIRCUITS



TC003460

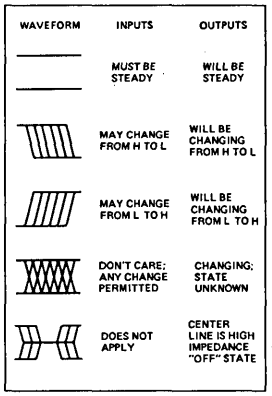


TC003470

A. Output Load for all tests except TGVQZ

B. Output Load for TGVQZ

KEY TO SWITCHING WAVEFORMS



KS000010

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

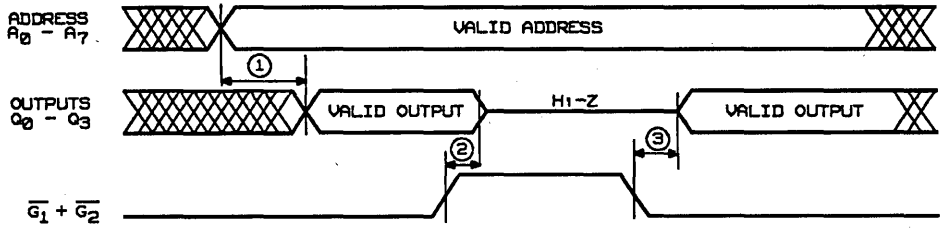
No.	Parameter Symbol	Parameter Description	"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		30		40		45		60	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		20		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		20		30	ns

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage + 0.5 V output levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021170

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S25

4096-Bit (512 x 8) Bipolar Registered PROM
With $\overline{\text{Preset}}$ and $\overline{\text{Clear}}$ Inputs

DISTINCTIVE CHARACTERISTICS

- 'SA' version offers ultrafast AC performance (25 ns set-up and 12 ns clock-to-output)
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common Preset ($\overline{\text{PS}}$) and Clear ($\overline{\text{CR}}$) inputs
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ > 98%)

GENERAL DESCRIPTION

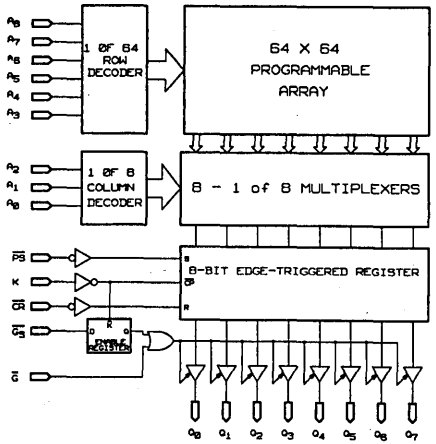
The Am27S25 (512 words by 8 bits) is a fully decoded, Schottky array, TTL Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains both asynchronous and synchronous output enables as well as common asynchronous preset and clear register controls.

Upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



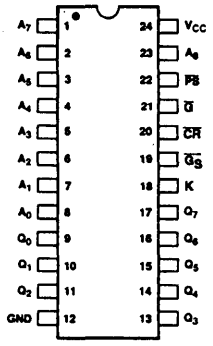
BD006130

PRODUCT SELECTOR GUIDE

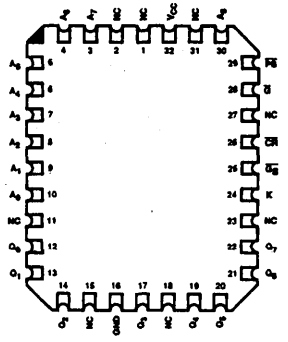
Part Number	Am27S25SA		Am27S25A		Am27S25	
Address Set-up Time (ns)	25	30	30	35	50	55
Clock-to-Ouput Delay (ns)	12	15	20	25	27	30
Operating Range	C	M	C	M	C	M

Publication # 03300 | Rev. D | Amendment /0
Issue Date: May 1986

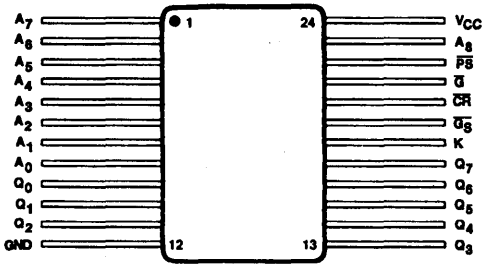
CONNECTION DIAGRAMS
Top View



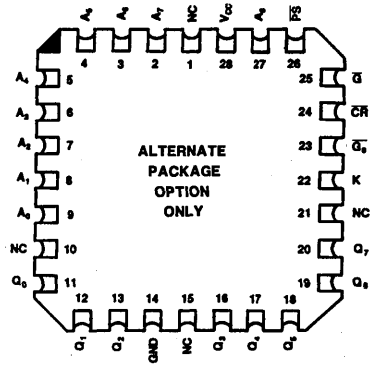
CD001021



CD000632



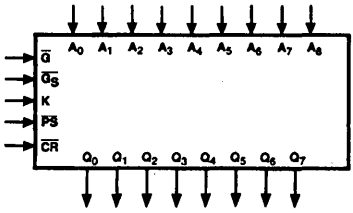
CD008011



CD008022

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



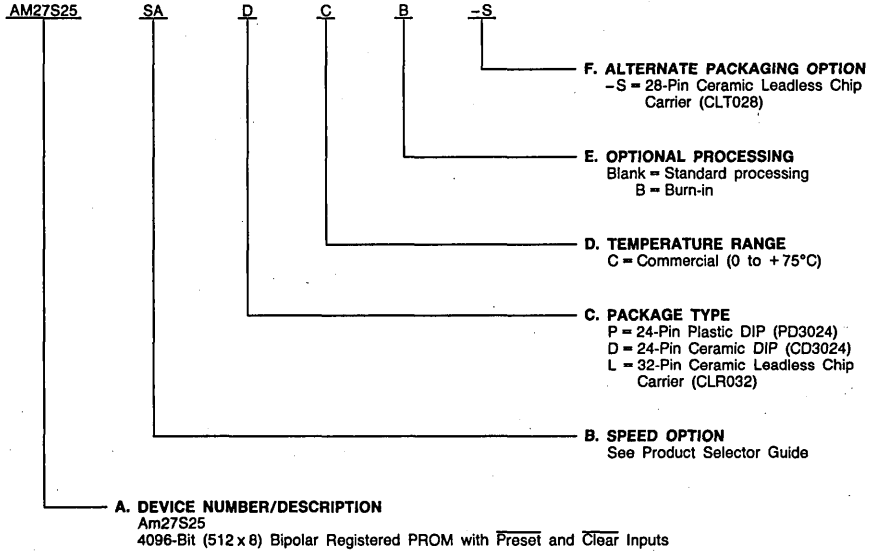
LS000113

ORDERING INFORMATION (Cont'd)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S25	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S
AM27S25A	
Am27S25SA	

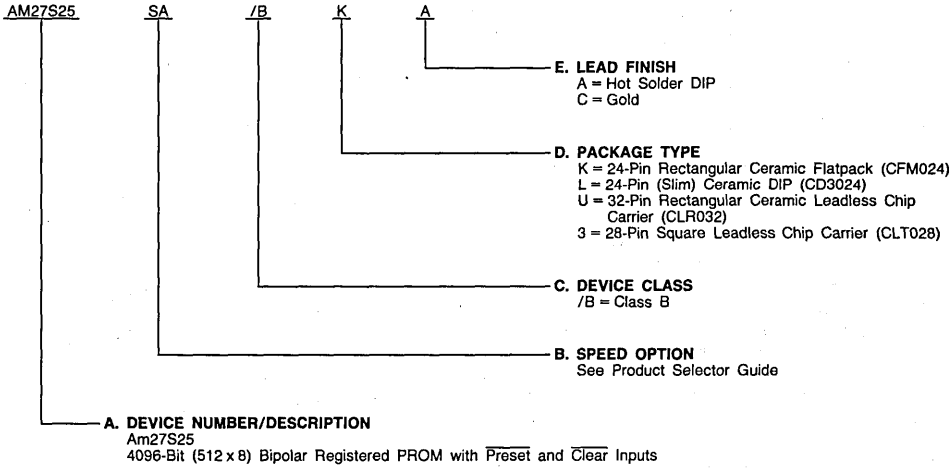
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
Am27S25	/BKA, /BLA, /BUC, /B3C
Am27S25A	
Am27S25SA	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address (Inputs)
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

K Clock
CP is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of CP.

$Q_0 - Q_7$ Data Port (Outputs, Three-State)
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high-impedance.

$\overline{G}$ Asynchronous $\overline{\text{Output Enable}}$
Provides direct control of the Q_n output three-state drivers, independent of CP.

$\overline{G_S}$ Synchronous $\overline{\text{Output Enable}}$
Controls the state of the Q_n output three-state drivers, in conjunction with CP. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

$\overline{PS}$ Asynchronous $\overline{\text{Preset}}$
Control pin used to force the state of the output data registers HIGH, independent of CP. This can be used to generate a condition for system interrupt or initialization.

$\overline{CR}$ Asynchronous $\overline{\text{Clear}}$
Control pin used to force the state of the output data registers LOW, independent of CP. This can be used to generate a condition for system interrupt or initialization.

V_{CC} Power Supply Pin
The most positive of the logic power supply pins.

GND Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

When V_{CC} power is first applied, the synchronous enable ($\overline{G_S}$) flip-flop will be in the set condition causing the outputs ($Q_0 - Q_7$) to be in the OFF or high-impedance state. Reading data is accomplished by first applying the binary word address to the address inputs ($A_0 - A_8$) and a logic LOW to the synchronous enable ($\overline{G_S}$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (K), data is transferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable ($\overline{G}$) is also LOW, stored data will appear on the outputs ($Q_0 - Q_7$). If $\overline{G_S}$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state regardless of the state of $\overline{G}$. The outputs may be disabled at any time by switching $\overline{G}$ to a HIGH level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered Asynchronous Preset ($\overline{PS}$) and Clear ($\overline{CR}$) inputs. These functions are common to all registers and are useful during power-up timeout sequences. With outputs enabled, the $\overline{PS}$ input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the $\overline{CR}$ input is LOW, the internal flip-flops of the data register are reset and a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55°C to +125°C
Supply Voltage ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at −55°C, 25°C, and 125°C.

2

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V			−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−20	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.			185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. V_E = 2.4 V	V_O = V_{CC}		40	μA
			V_O = 0.4 V		−40	

Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled at initial characterization and at any time the design is modified where capacitance may be affected.

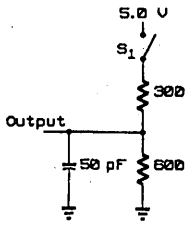
*See the last page of this spec for Group A Subgroup Testing information.

Capacitance

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		12	

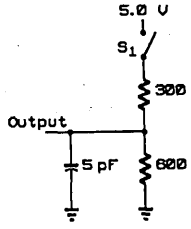
Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUITS



TC003441

A. Output Load for all tests except TGVQZ and TKHQZ



TC003451

B. Output Load for TGVQZ and TKHQZ

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Note 1)

No.	JEDEC Parameter Symbol	Parameter Description		Am27S25SA Min.	Am27S25SA Max.	Am27S25A Min.	Am27S25A Max.	Am27S25 Min.	Am27S25 Max.	Units
1	TAVKH	Address to K HIGH Setup Time	COM'L	25		30		50		ns
			MIL	30		35		55		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		0		ns
			MIL	0		0		0		
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 3)	COM'L	4	12		20		27	ns
			MIL	4	15		25		30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	15		20		20		ns
			MIL	20		20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW)	COM'L		20		25		35	ns
			MIL		25		30		45	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (See Note 2)	COM'L		20		25		35	ns
			MIL		25		30		45	
7	TGSVKH	$\overline{GS}$ to K HIGH Setup Time	COM'L	10		10		15		ns
			MIL	10		10		15		
8	TKHGSX	$\overline{GS}$ to K HIGH Hold Time	COM'L	0		5		5		ns
			MIL	0		5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs	COM'L		20		25		35	ns
			MIL		25		30		45	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (See Note 2)	COM'L		20		25		35	ns
			MIL		25		30		45	
11	TPSLQV TCRLQV	Delay from $\overline{PS}$ or $\overline{CR}$ LOW to Output Valid (HIGH or LOW)	COM'L		20		20		25	ns
			MIL		25		25		30	
12	TPSHKH TCRHKH	Asynchronous $\overline{PS}$ or $\overline{CR}$ Recovery Time	COM'L	15		20		20		ns
			MIL	20		25		25		
13	TPSLPSH TCRLCRH	Asynchronous $\overline{PS}$ or $\overline{CR}$ Pulse Width (LOW)	COM'L	15		20		20		ns
			MIL	20		25		25		

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A. under Switching Test Circuits.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B. under Switching Test Circuits.
3. Minimum delay is guaranteed by design and supported by characterization data.

*See the last page of this spec for group A Subgroup Testing Information.

SWITCHING WAVEFORMS

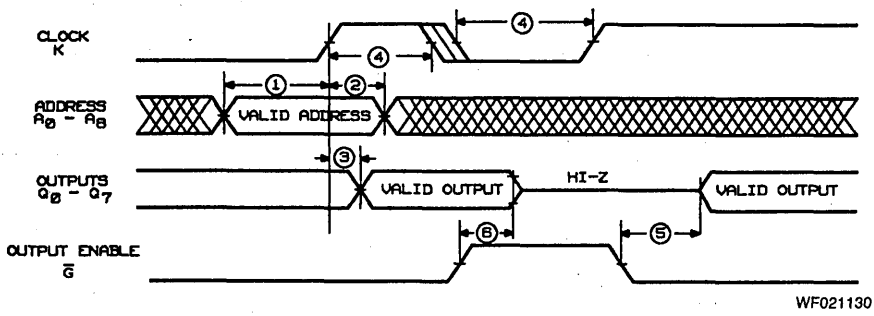


Diagram A. Using Asynchronous Enable

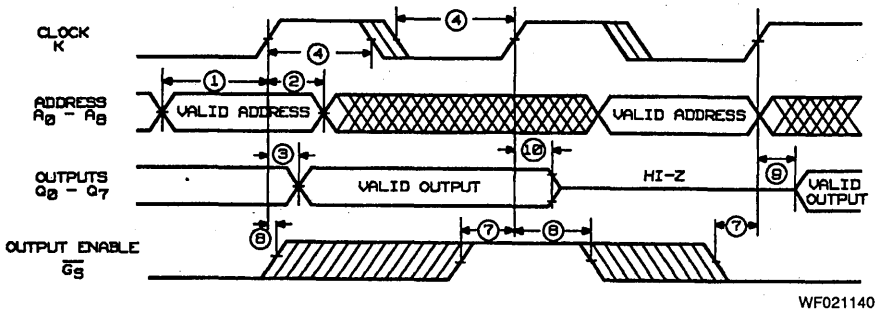


Diagram B. Using Synchronous Enable

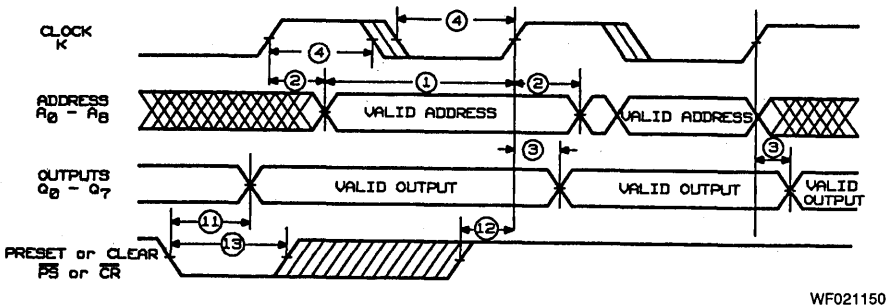


Diagram C. Using Asynchronous $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVKH	9, 10, 11
2	TKHAX	9, 10, 11
3	TKHQV1	9, 10, 11
4	TKHKL TKLKH	9, 10, 11
5	TGLQV	9, 10, 11
6	TGHQZ	9, 10, 11
7	TGSVKH	9, 10, 11
8	TKHGSX	9, 10, 11
9	TKHQV2	9, 10, 11
10	TKHQZ	9, 10, 11
12	TPSHKH TCRHKH	9, 10, 11
13	TPSLPSH TCRLCRH	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S27

4,096-Bit (512 x 8) Bipolar Registered PROM

DISTINCTIVE CHARACTERISTICS

- On-chip, edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 55 ns address setup and 27 ns clock to output times
- Excellent performance over the military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)

GENERAL DESCRIPTION

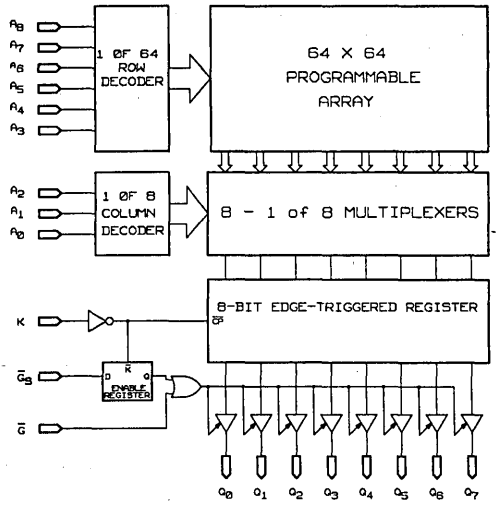
The Am27S27 (512 words by 8 bits) is a fully decoded, Schottky array, TTL-Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains both asynchronous and synchronous output enables.

Upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



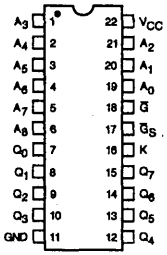
BD006181

PRODUCT SELECTOR GUIDE

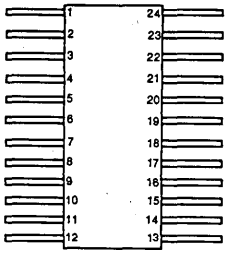
Part Number	Am27S27	
Address Setup Time	55 ns	65 ns
Clock-to-Output Delay	27 ns	30 ns
Operating Range	C	M

Publication # 03185 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



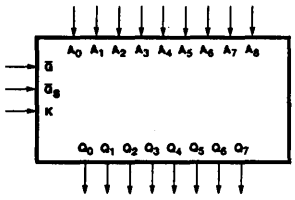
CD000671



CD009361

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



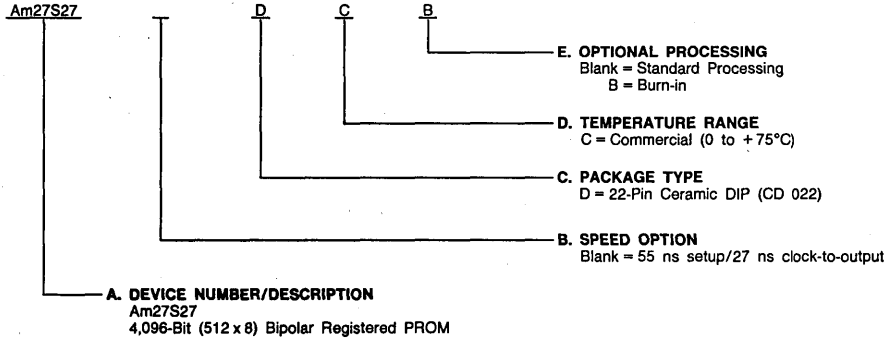
LS000131

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
Am27S27	DC, DCB

Valid Combinations

Valid Combinations list configurations planned to supported in volume for this device. Consult the local AMD sales office to confirm availability of specific combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

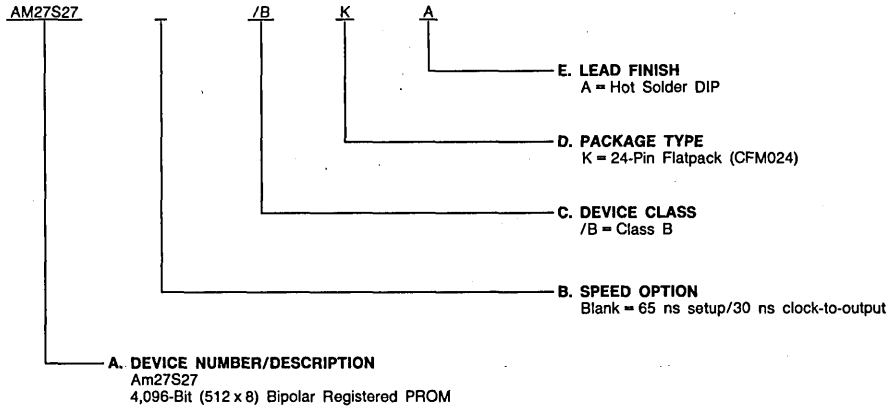
APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

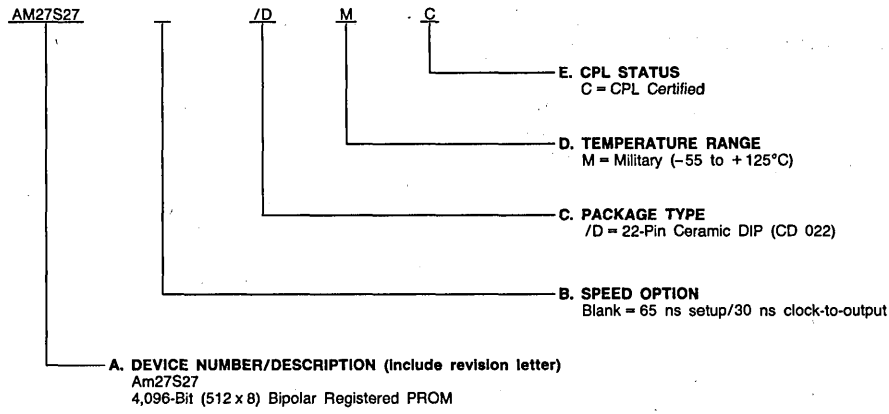
APL Products:
A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

CPL Products:
A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status

APL Products



CPL Products



	Valid Combinations	
APL	AM27S27	/BKA
CPL	AM27S27	/DMC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address Inputs
The 9-bit field presented at the address inputs selects one of the 512 memory locations to be read from.

K Clock
The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

$Q_0 - Q_7$ Data Output Port
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

$\overline{G}$ Asynchronous Output Enable
Provides direct control of the Q output three-state drivers independent of K.

$\overline{GS}$ Synchronous Output Enable
Controls the state of the Q output three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

2

FUNCTIONAL DESCRIPTION

When V_{CC} power is first applied, the synchronous enable ($\overline{G}_S$) flip-flop will be in the set condition causing the outputs, $Q_0 - Q_7$, to be in the OFF or high-impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, $A_0 - A_8$, and a logic LOW to the synchronous output enable, $\overline{G}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, K, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{G}$, is also LOW, stored data will appear on the outputs, $Q_0 - Q_7$. If $\overline{G}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state. The outputs may be disabled at any time by switching $\overline{G}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature (T_C) ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at −55°C, 25°C, and 125°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

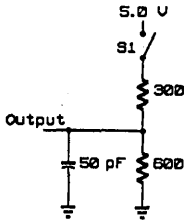
Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V			−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−20	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.		185	mA	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{VE}$ = 2.4 V	V_O = 4.5 V	40		μA
			V_O = 0.4 V	−40		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

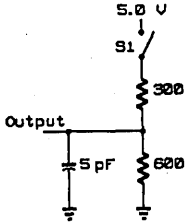
*See the last page of this spec for Group A Subgroup Testing information.

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		12	

SWITCHING TEST CIRCUITS

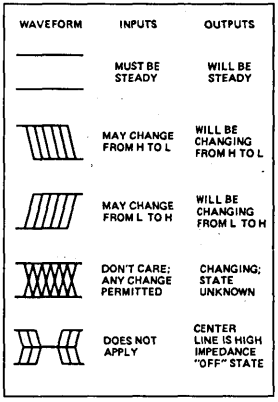


TC003440



TC003450

KEY TO SWITCHING WAVEFORMS



KS000010

A. Output Load for all tests except TGVQZand TKHQZ

B. Output Load for TGVQZ and TKHQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (see Note 1)*

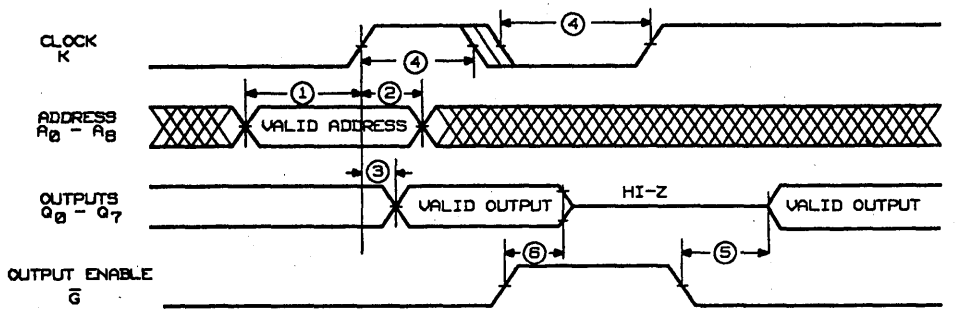
No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
1	TAVKH	Address to K HIGH Setup Time	55		65		ns
2	TKHAX	Address to K HIGH Hold Time	0		0		ns
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)		27		30	ns
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	30		40		ns
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW)		40		45	ns
6	TGHQZ	Asynchronous Output Enable HIGH to Output High Z (see Notes 2)		30		40	ns
7	TGSVKH	$\overline{GS}$ to K HIGH Setup Time	25		30		ns
8	TKHGSX	$\overline{GS}$ to K HIGH Hold Time	0		0		ns
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs		35		45	ns
10	TKHQZ	Delay from K HIGH to Output Hi-Z (see Notes 2)		35		45	ns

See also Switching Test Circuit Diagrams.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A,
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B.

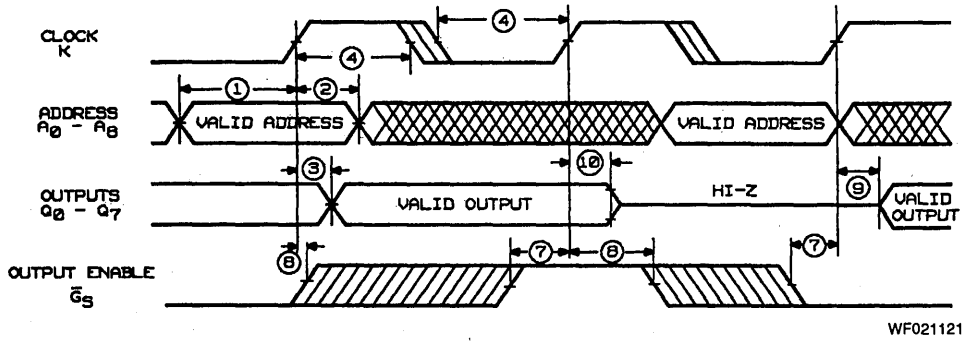
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021110

Diagram A. Using Asynchronous Enable



WF021121

Diagram B. Using Synchronous Enable

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_I	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVKH	9, 10, 11
2	TKHAX	9, 10, 11
3	TKHQV1	9, 10, 11
4	TKHKL TKLKH	9, 10, 11
5	TGLQV	9, 10, 11
6	TGHQZ	9, 10, 11
7	TGSVKH	9, 10, 11
8	TKHGSX	9, 10, 11
9	TKHQV2	9, 10, 11
10	TKHQZ	9, 10, 11
	Functional Tests	7, 8

Am27S28/27S29

4,096-Bit (512 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

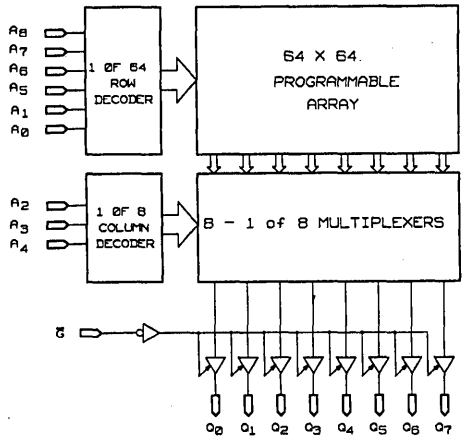
- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

The Am27S28/29 (512-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open collector (Am27S28) and three-state (Am27S29) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word depth expansion is facilitated by an active LOW ($\overline{G}$) output enable.

FUNCTIONAL BLOCK DIAGRAM



BD006182

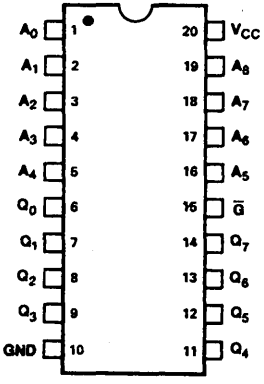
PRODUCT SELECTOR GUIDE

Open Collector Part Number	Am27S28A		Am27S28	
Three-State Part Number	Am27S29A		Am27S29	
Address Access Time	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M

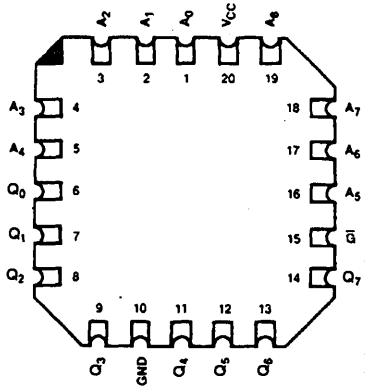
Publication # 03328 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS*

Top View



CD000681

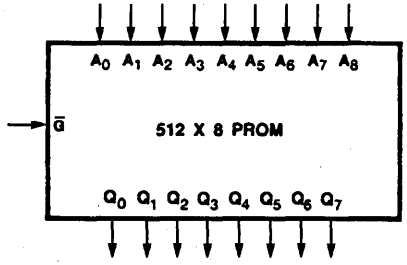


CD000691

*Also offered in 20-pin Flatpack. Connections are identical to those listed here.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS000141

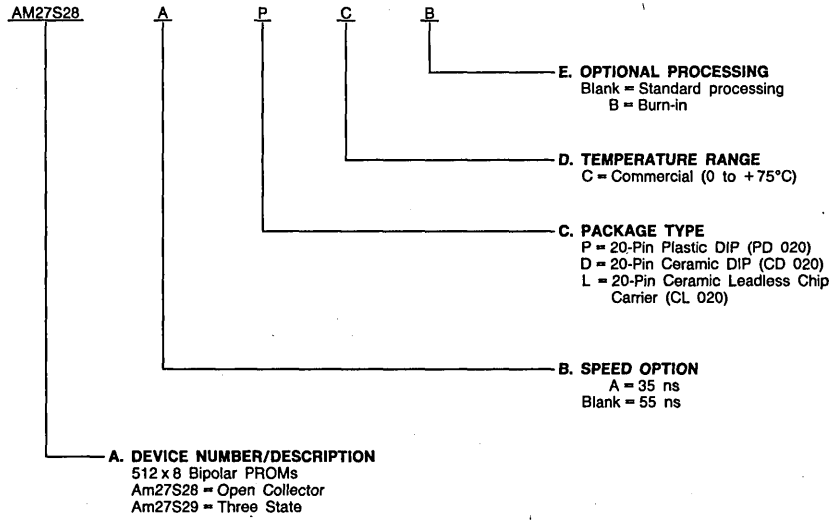
V_{CC}/ = Power Supply
GND/ = Ground

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S28	PC, PCB, DC, DCB, LC, LCB
AM27S28A	
AM27S29	
AM27S29A	

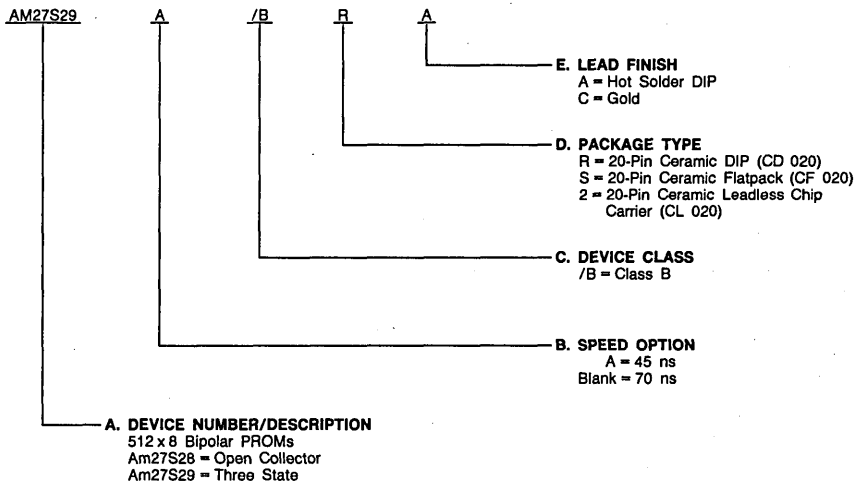
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S28	/BRA, /BSA /B2C
AM27S28A	
AM27S29	
AM27S29A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address (Inputs)
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G}$ Output Enable (Input)
Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an OFF state, and all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}$

Disable = G

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES*

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at −55°C, 25°C, and 125°C.

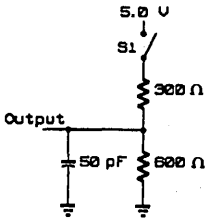
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}					0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V					−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V					25	μA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 3)			−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.					160	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}}$ = 2.4 V		V_O = V_{CC}			40	μA
			(Note 1)	V_{OUT} = 2.4 V			40	
				V_{OUT} = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4)				8		

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

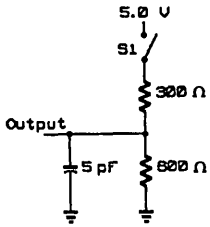
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS



TC003442

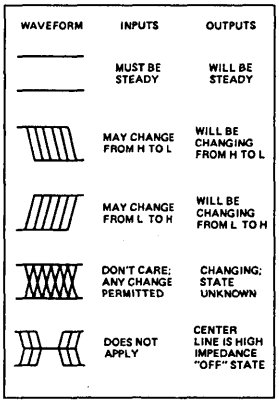
A. Output Load for all A-C tests except TGVQZ



TC003452

B. Output Load for TGVQZ

KEY TO SWITCHING WAVEFORMS



KS000010

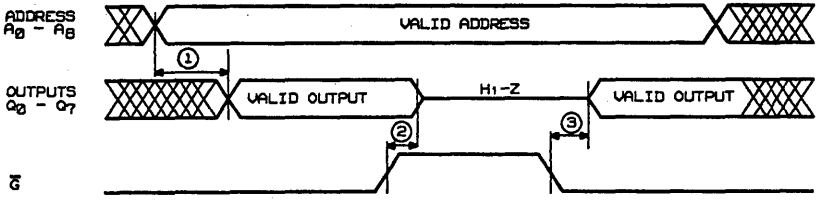
Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	"A" Version COM'L Min.	"A" Version COM'L Max.	"A" Version MIL Min.	"A" Version MIL Max.	Standard Version COM'L Min.	Standard Version COM'L Max.	Standard Version MIL Min.	Standard Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuits.
Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Figure 1.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V ouput levels using the test load in Figure 2.

SWITCHING WAVEFORMS



WF021240

*See the last page of this spec for Group A Subgroup Testing information.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups
TAVQV	9, 10, 11
TGVQZ	9, 10, 11
TGVQV	9, 10, 11
Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S31

(512 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

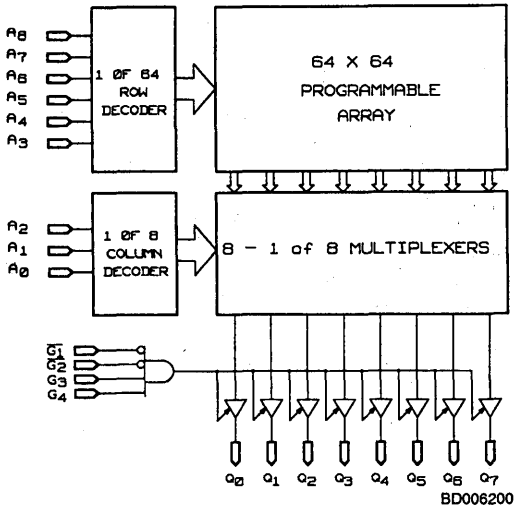
- High Speed — 35ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

The Am27S31 (512-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state output version compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by both active LOW ($\overline{G_1}$ and $\overline{G_2}$) and active HIGH (G_3 and G_4) output enables.

BLOCK DIAGRAM



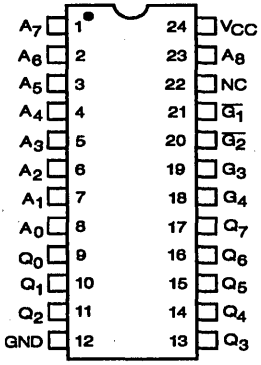
PRODUCT SELECTOR GUIDE

Part Number	27S31A		27S31	
Address Access Time	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M

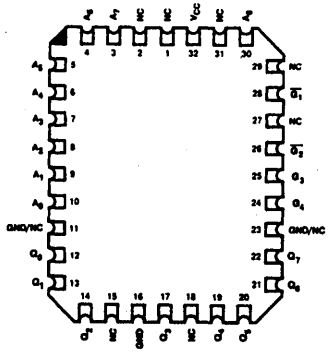
Publication # 03207 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

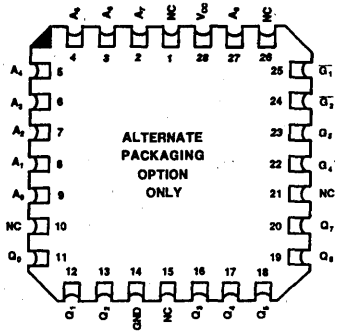
DIP*



CD000701



CD000711

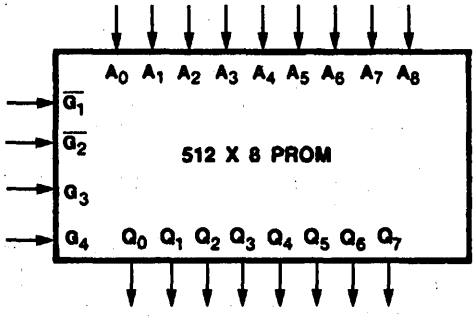


CD009460

*Also available in 24-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



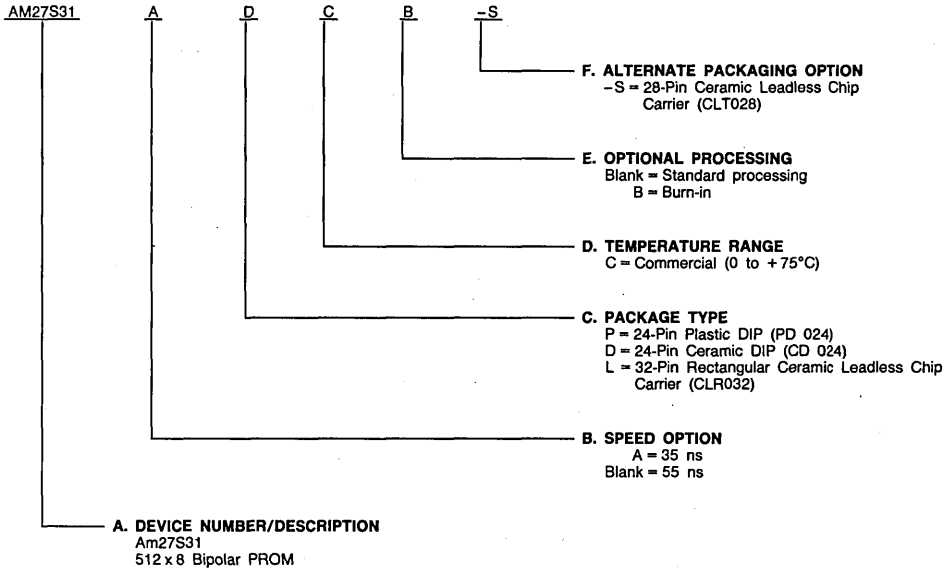
LS000151

VCC/ = Power Supply
GND/ = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S31	PC, PCB, DC, DCB, LC, LC-S, LCB, LCB-S
AM27S31A	

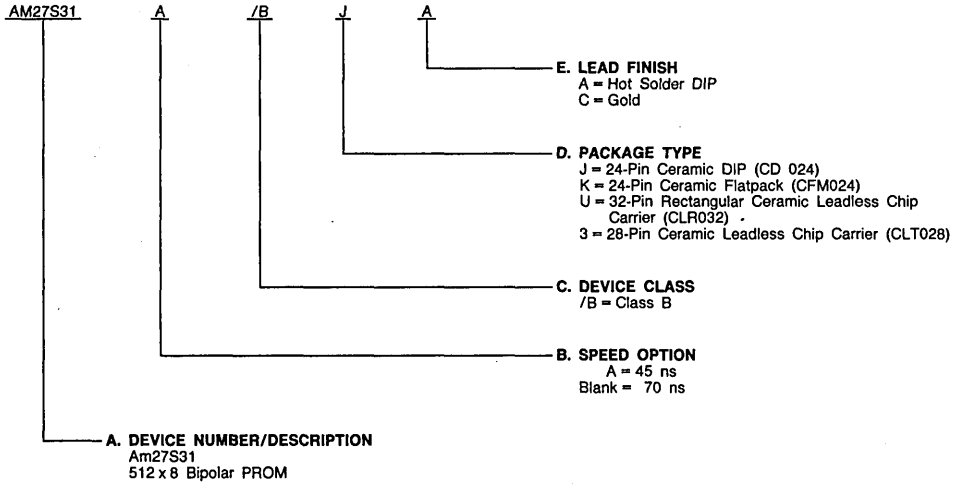
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S31	/BJA, /BKA, /BUC, /B3C
AM27S31A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address Inputs
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The Outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, $\overline{G_2}$, G_3, G_4 Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot G_4$$

$$\text{Disable} = \overline{\overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot G_4} = G_1 + G_2 + \overline{G_3} + \overline{G_4}$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at −55°C, 25°C, and 125°C.

2

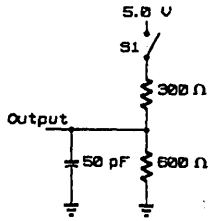
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}					0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V					−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V					25	μA
I_{SC} (Note 1)	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 3)			−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.					175	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}_i}$ = 2.4 V		V_O = V_{CC}			40	μA
			(Note 1)	V_O = 2.4 V			40	
				V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4)				8		

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

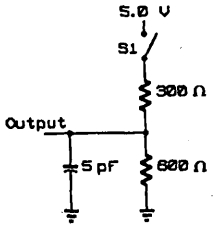
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS



TC003442

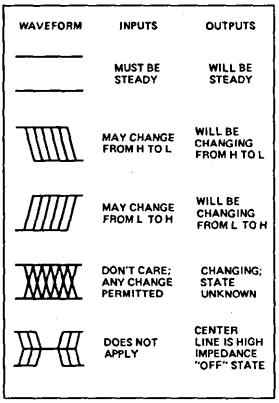
A. Output Load for all A-C tests except TGVQZ



TC003452

B. Output Load for TGVQZ

KEY TO SWITCHING WAVEFORMS



KS000010

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

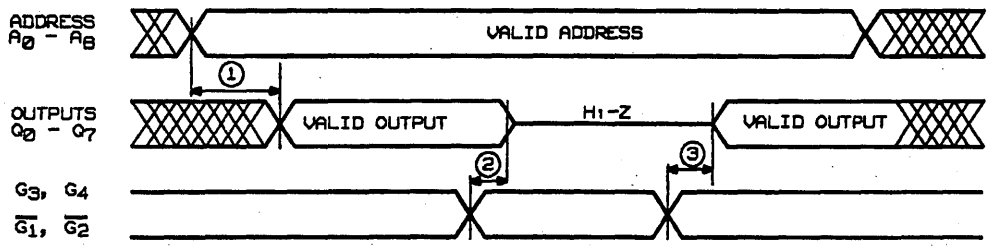
No.	Parameter Symbol	Parameter Description	"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.		Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V ouput levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021260

2

SUBGROUP A TESTING INFORMATION

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups
TAVQV	9, 10, 11
TGVQZ	9, 10, 11
TGVQV	9, 10, 11
Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S32/27S33

4,096-Bit (1024 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

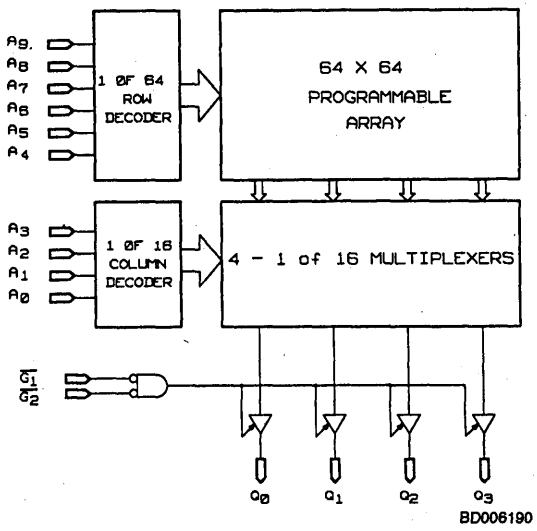
- High speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low-current PNP inputs
- High-current open-collector and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

The Am27S32/27S33 (1024-words by 4-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S32) and three-state (Am27S33) output versions. These outputs are compatible with low-power Schotkky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by active LOW ($\overline{G_1}$ & $\overline{G_2}$) output enables.

BLOCK DIAGRAM



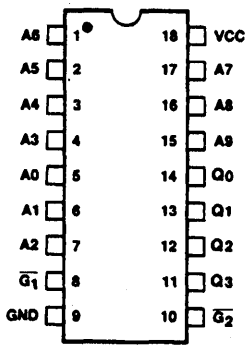
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	Am27S32A		Am27S32	
Three-State Part Number	Am27S33A		Am27S33	
Address Access Time	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M

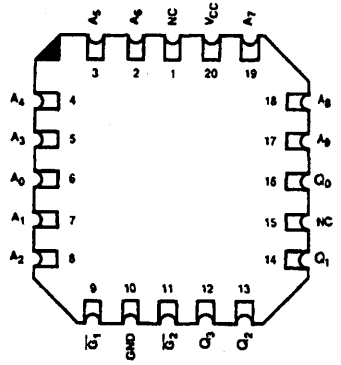
Publication # 03226 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

DIP*



CD000721

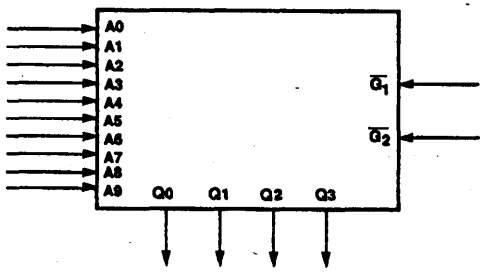


CD000731

*Also available in 18-pin Flatpack. Connections are identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

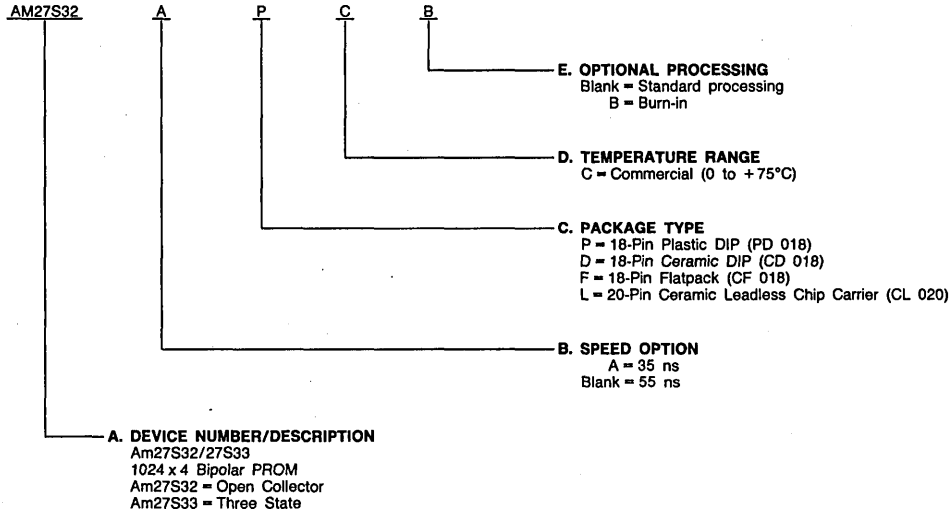


LS002500

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S32	PC, PCB, DC, DCB, FC, FCB, LC, LCB
AM27S32A	
AM27S33	
AM27S33A	

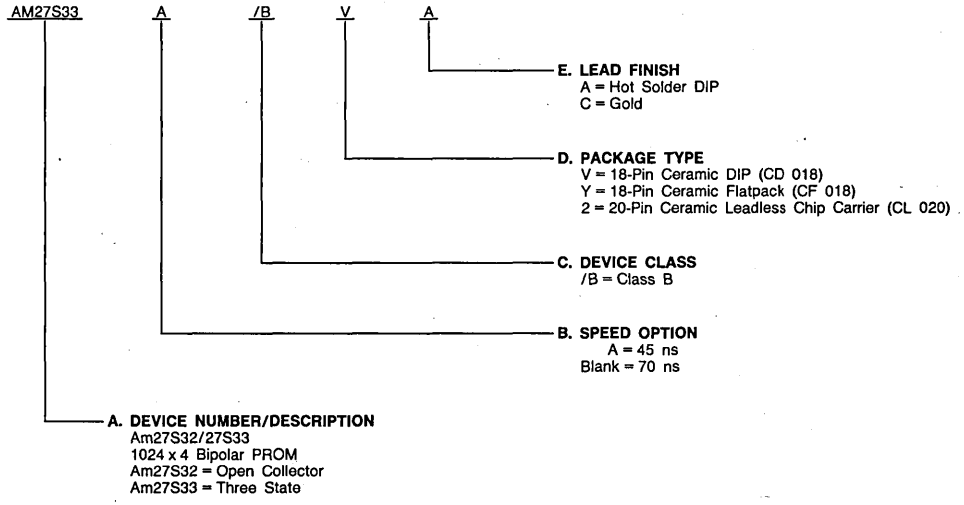
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S32	/BVA, /BYA, /B2C
AM27S32A	
AM27S33	
AM27S33A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}, \overline{G_2}$ Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2}$$

$$\text{Disable} = \overline{\overline{G_1} \cdot \overline{G_2}} = G_1 \cdot G_2$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +475 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = −55°C, 25°C, and 125°C.

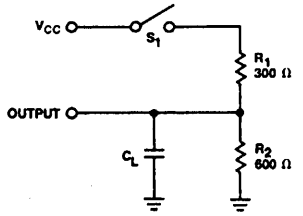
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	μA
I_{SC} (Note 1)	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 3)		−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.	COM'L			140	mA
			MIL			145	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max., $\overline{V_{G1}}$ = 2.4 V	V_O = V_{CC}			40	μA
			(Note 1) V_O = 2.4 V			40	
			V_O = 0.4 mV			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4)			8		

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

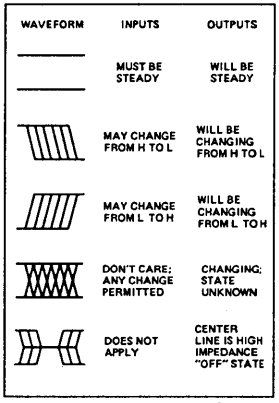
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



TC000171

KEY TO SWITCHING WAVEFORM



KS000010

Notes: 1. TAVQV is tested with switch S_1 closed and $C_L = 50$ pF.
2. For open collector outputs, TGVQV and TGVQZ are tested with S_1 closed to the 1.5 V output level. $C_L = 50$ pF.
3. For three-state outputs, TGVQV is tested with $C_L = 5$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. TGVQZ is tested with $C_L = 5$ pF. HIGH to high-impedance tests are made with S_1 open to an output voltage of steady state HIGH −0.5 V; LOW to high-impedance tests are made with S_1 closed to the steady state LOW +0.5 V level.

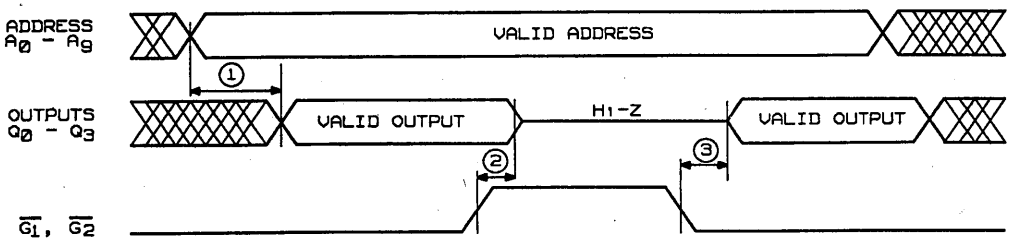
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	"A" Version COM'L Min.	"A" Version COM'L Max.	"A" Version MIL Min.	"A" Version MIL Max.	Standard Version COM'L Min.	Standard Version COM'L Max.	Standard Version MIL Min.	Standard Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuit.
Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021250

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S35/Am27S37

8,192-Bit (1024 x 8) Bipolar Registered PROM
with Programmable $\overline{\text{INITIALIZE}}$ Input

DISTINCTIVE CHARACTERISTICS

- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Versatile programmable asynchronous or synchronous enable for simplified word expansion
- Buffered common $\overline{\text{INITIALIZE}}$ input either asynchronous (Am27S35) or synchronous (Am27S37)
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)

GENERAL DESCRIPTION

The Am27S35 and the Am27S37 (1024-words by 8-bits) are fully decoded, Schottky array, TTL Programmable Read-Only Memories (PROMs), incorporating D-type master-slave data registers on chip. These devices have three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

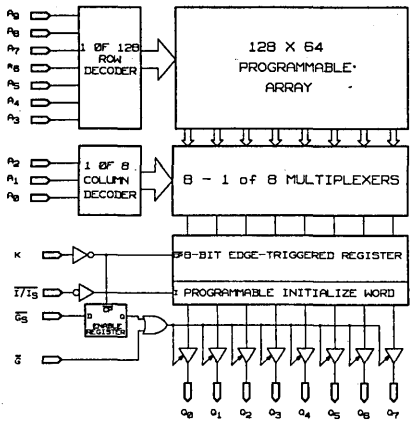
These devices contain an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, these devices contain both asynchronous ($\overline{G}$) and synchronous ($\overline{G_S}$) output enables.

These devices contain a single pin initialize function capable of loading any arbitrary microinstruction for system interrupt or initialization. On the Am27S35 this function operates asynchronously, independent of clock. The Am27S37 provides synchronous operation of this function.

Upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



BD006351

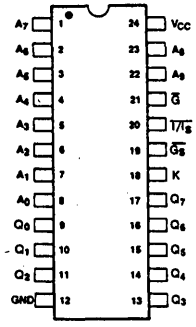
PRODUCT SELECTOR GUIDE

Part Number Asynchronous Initialize	Am27S35A		Am27S35	
Part Number Synchronous Initialize	Am27S37A		Am27S37	
Address Setup Time	35 ns	40 ns	40 ns	45 ns
Clock-to-Output Delay	20 ns	20 ns	25 ns	30 ns
Operating Range	C	M	C	M

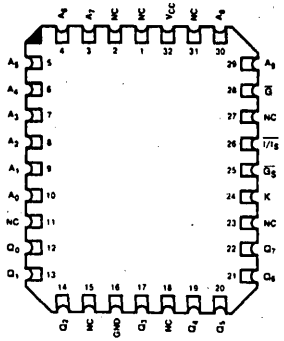
Publication # 03187 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

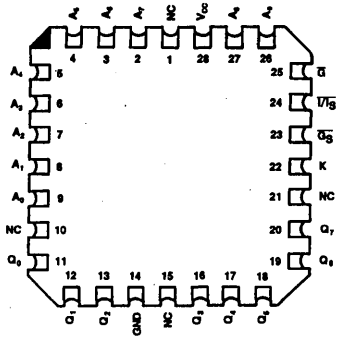
DIP*



CD000741



CD000751

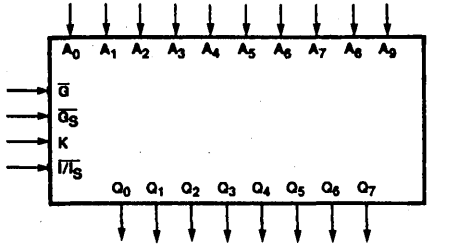


CD009620

*Also available in 24-pin Flatpack.
Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



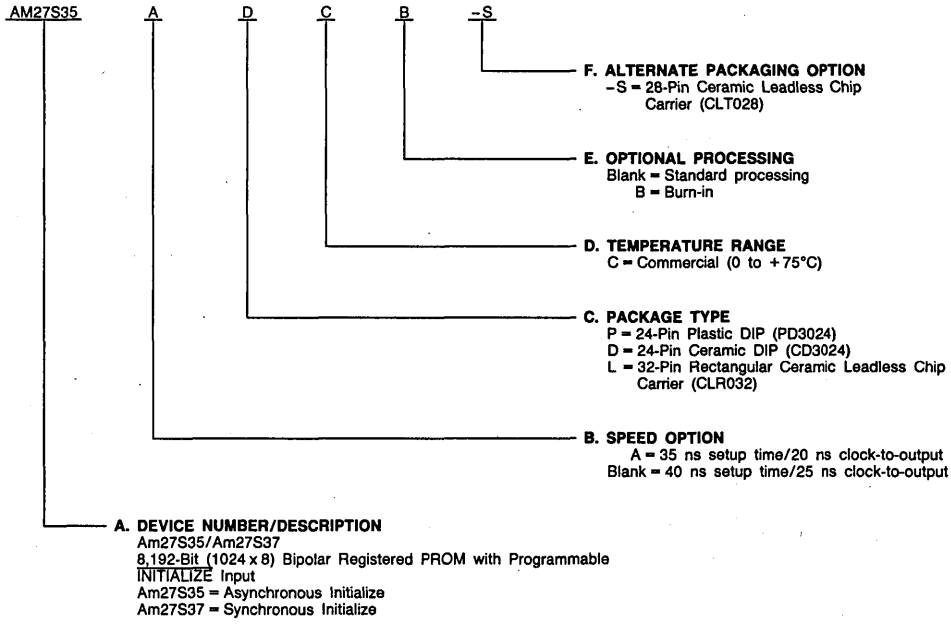
LS000172

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S35	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S
AM27S35A	
AM27S37	
AM27S37A	

Valid Combinations

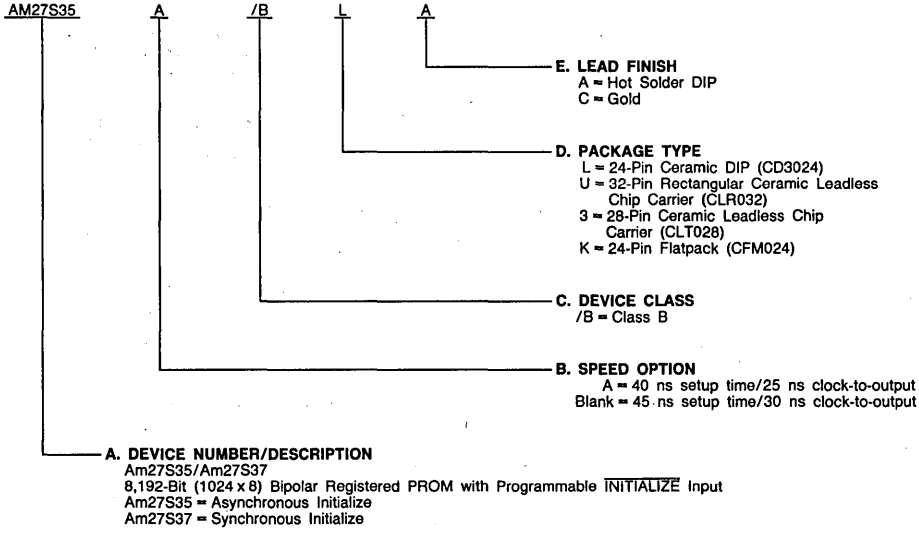
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S35	/BLA, /BKA /BUC, /B3C
AM27S35A	
AM27S37	
AM27S37A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

K Clock
The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

$Q_0 - Q_7$ Data Output Port
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

$\overline{G}$ Asynchronous Output Enable
Provides direct control of the Q-output, three-state drivers independent of K.

$\overline{G_S}$ Synchronous Output Enable
Controls the state of the Q-output, three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word-depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

$\overline{I}$ Asynchronous Initialize (Am27S35)
Control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

$\overline{I_S}$ Synchronous Initialize (Am27S37)
Control pin used to initialize the output data registers from a programmable word in conjunction with K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

2

FUNCTIONAL DESCRIPTION

The Am27S35A/35 and Am27S37A/37 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 1024-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S35A/35 and Am27S37A/37 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{G_S}$) flip-flop will be in the set condition causing the outputs (Q_0–Q_7) to be in the OFF or high-impedance state. Reading data is accomplished by first applying the binary word address to the address inputs (A_0–A_9) and a logic LOW to the synchronous enable ($\overline{G_S}$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (K), data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable ($\overline{G}$) is also LOW, stored data will appear on the outputs (Q_0–Q_7). If ($\overline{G_S}$) is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state regardless of the value of ($\overline{G}$). The outputs may be disabled at any time by switching ($\overline{G}$) to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{I}$) causes the contents of an additional (1025th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{I}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{I}$ performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power-up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S35A/35 has an asynchronous initialize input ($\overline{I}$). Applying a LOW to the $\overline{I}$ input causes an immediate load of the programmed initialize word into the slave flip-flops of the register independent of all other inputs (including K). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{G}$) LOW.

The Am27S37A/37 has a synchronous $\overline{I_S}$ input. Applying a LOW to the $\overline{I_S}$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including K). To bring this data to the device outputs, the synchronous enable ($\overline{G_S}$) should be held LOW until the next LOW-to-HIGH transition of the clock (K). Following this, the data will appear on the outputs after the asynchronous enable ($\overline{G}$) is brought LOW.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

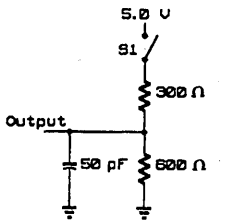
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.				185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{V_S}$ = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 3)			12		

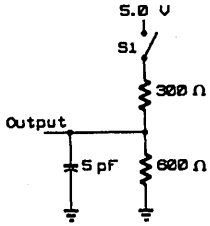
Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Only one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS



TC003442



TC003452

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

A. Output Load for All AC Tests Except TGHQZ and TKHQZ

B. Output Load for TGHQZ and TKHQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)*

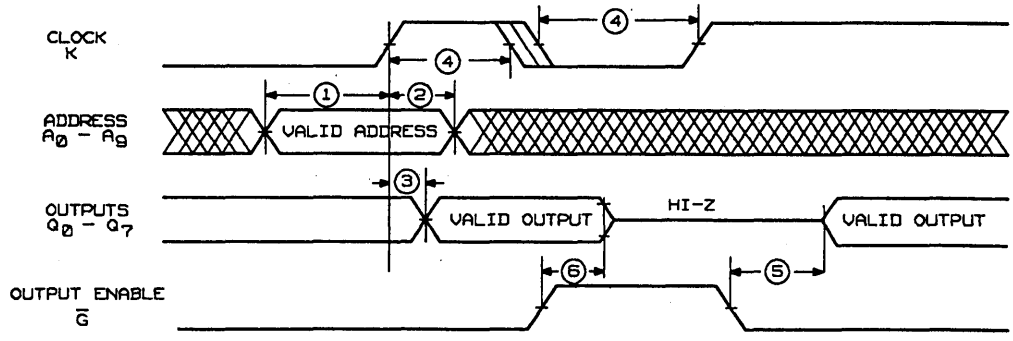
No.	Parameter Symbol	Parameter Description		"A" Version Min.	"A" Version Max.	Standard Version Min.	Standard Version Max.	Units
1	TAVKH	Address to K HIGH Setup Time	COM'L	35		40		ns
			MIL	40		45		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		
3	$TKHQV_1$	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)	COM'L		20		25	ns
			MIL		25		30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	20		20		ns
			MIL	20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)	COM'L		25		30	ns
			MIL		30		35	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (See Notes 2 & 3)	COM'L		25		30	ns
			MIL		30		35	
7	TGSVKH	$\overline{GS}$ to K HIGH Setup Time (See Note 4)	COM'L	15		15		ns
			MIL	15		15		
8	TKHGSX	$\overline{GS}$ to K HIGH Hold Time (See Note 4)	COM'L	5		5		ns
			MIL	5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (See Note 4)	COM'L		25		30	ns
			MIL		30		35	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (See Notes 2 & 4)	COM'L		25		30	ns
			MIL		30		35	
11	TILQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)	COM'L		30		35	ns
			MIL		35		40	
12	TIHKH	Asynchronous $\overline{I}$ Recovery Time (See Note 5)	COM'L	20		20		ns
			MIL	20		25		
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (See Note 5)	COM'L	25		25		ns
			MIL	30		30		
14	TISVKH	$\overline{IS}$ to K HIGH Setup Time (See Note 6)	COM'L	25		30		ns
			MIL	30		35		
15	TKHISX	$\overline{IS}$ to K HIGH Hold Time (See Note 6)	COM'L	0		0		ns
			MIL	0		0		

See also Switching Test Circuits.

Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.
3. Applies only when Asynchronous Enable ($\overline{G}$) function is used.
4. Applies only when Synchronous Enable ($\overline{GS}$) function is used.
5. Applies only to the Am27S35 (Asynchronous Initialize ($\overline{I}$)) version.
6. Applies only to the Am27S37 (Synchronous Initialize ($\overline{IS}$)) version.

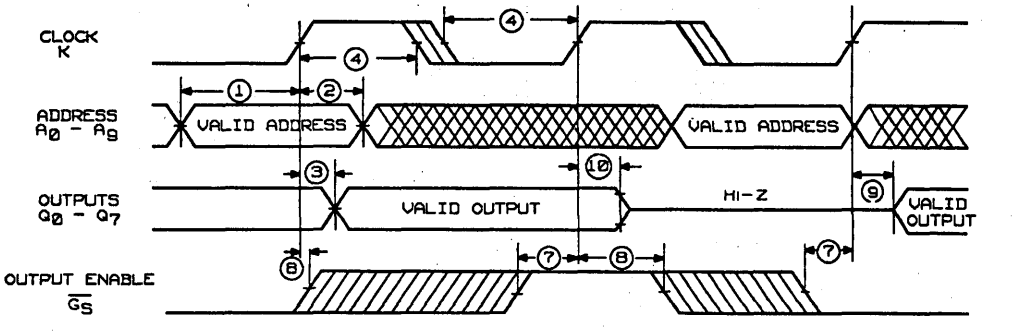
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Cont'd.)



WF021580

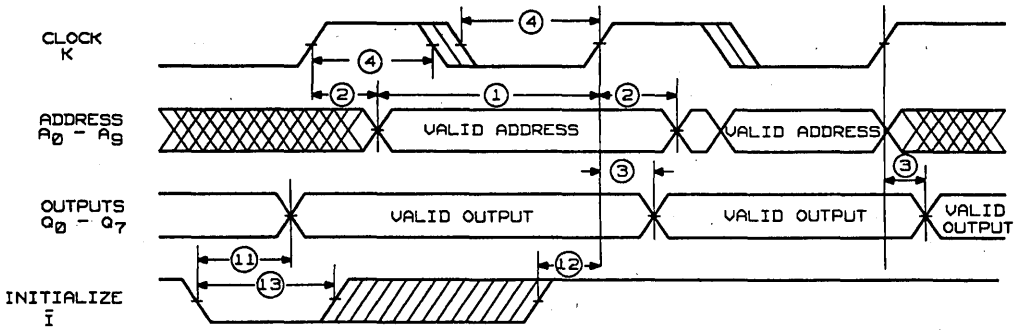
Timing Set 1. Using Asynchronous Enable



WF021611

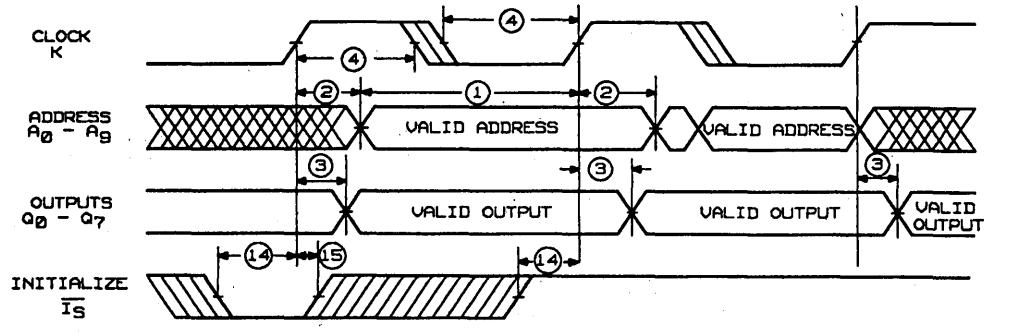
Timing Set 2. Using Synchronous Enable

SWITCHING WAVEFORMS



WF021590

Timing Set 3. Using Asynchronous Initialize
Am27S35 Only



WF021601

Timing Set 4. Using Synchronous Initialize
Am27S37 Only

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVKH	9, 10, 11	9	TKHQV2	9, 10, 11
2	TKHAX	9, 10, 11	10	TKHQZ	9, 10, 11
3	TKHQV1	9, 10, 11	11	TILQV	9, 10, 11
4	TKHKL TKLKH	9, 10, 11	12	TIHKH	9, 10, 11
5	TGLQV	9, 10, 11	13	TILIH	9, 10, 11
6	TGHQZ	9, 10, 11	14	TISVKH	9, 10, 11
7	TGSVKH	9, 10, 11	15	TKHISX	9, 10, 11
8	TKHGSX	9, 10, 11		Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S41/27PS41

16,384-Bit (4,096 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time "A" version (35 ns Max.) — Fast access time Standard version (50 ns Max.) — allow
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

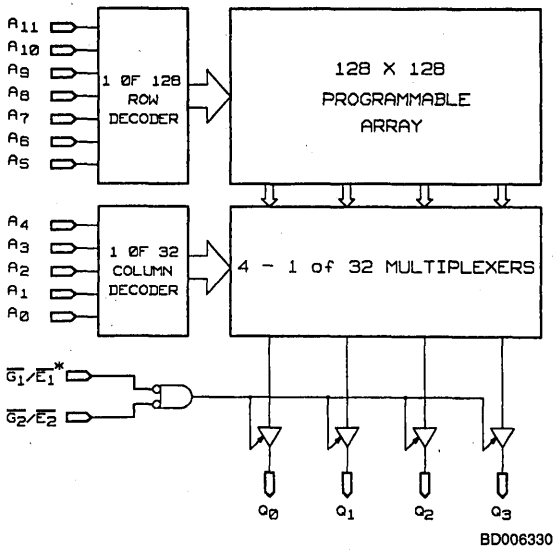
GENERAL DESCRIPTION

The Am27S41 (4,096-words by 4-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy-word depth expansion is facilitated by active LOW ($\overline{G_1}$ & $\overline{G_2}$) output enables.

This device is also offered in a power-switched version, the Am27PS41.

BLOCK DIAGRAM



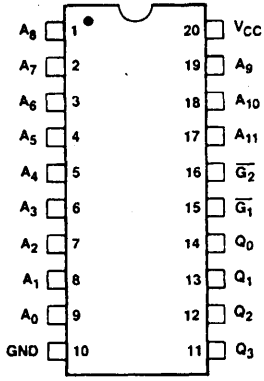
*E nomenclature applies only to Am27PS power-switched versions.

PRODUCT SELECTOR GUIDE

Part Number	27S41A		27S41		27PS41	
Address Access Time	35 ns	50 ns	50 ns	65 ns	50 ns	65 ns
Operating Range	C	M	C	M	C	M

Publication # 02122 Rev. C Amendment /0
Issue Date: May 1986

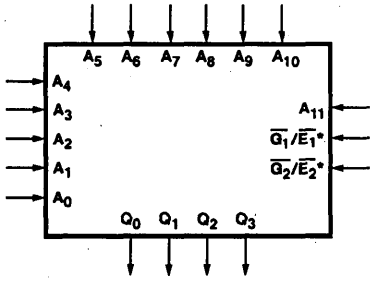
CONNECTION DIAGRAMS
Top View



CD000411

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



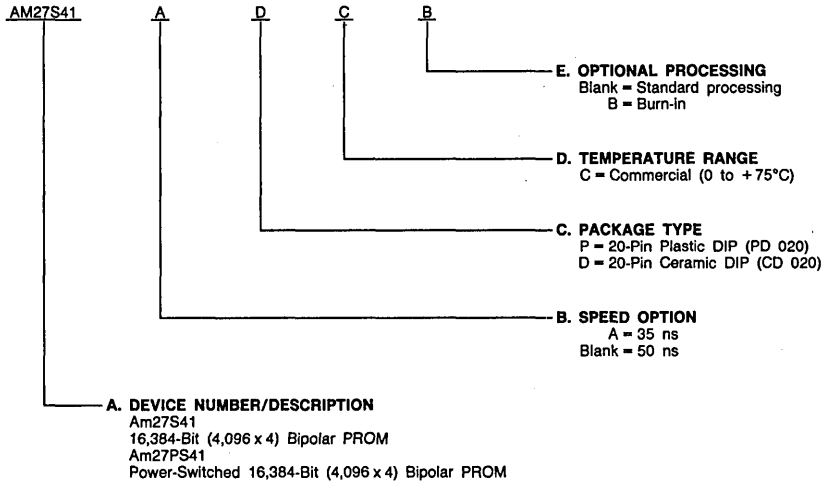
LS000041

*E nomenclature applies only to Am27PS power-switched versions.

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S41	PC, PCB, DC, DCB
AM27S41A	
AM27PS41	

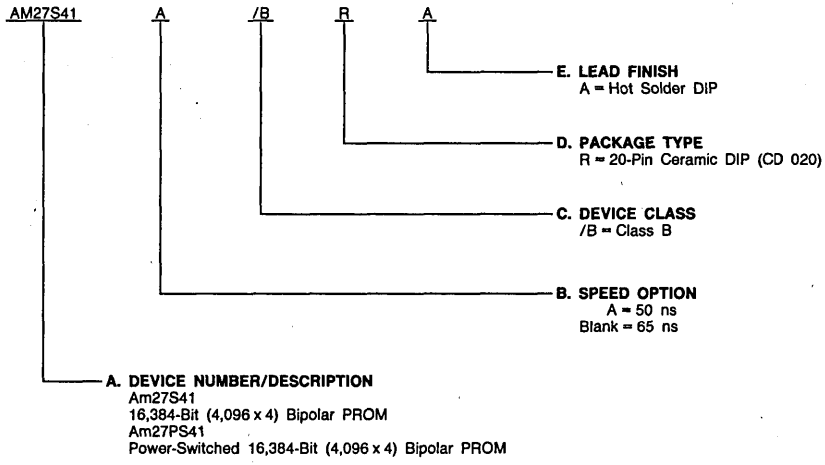
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S41	/BRA
AM27S41A	
AM27PS41	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs
The 12-bit field presented at the address inputs selects one of 4,096 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port
The outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, $\overline{G_2}$ Output Enable
Provides direct control of the Q-output, three-state buffers. Outputs disabled forces all outputs to a floating or high-impedance state. On power-switched version, the disabled state reduces the I_{CC} to I_{CCD}.

Enable = $\overline{G_1} \cdot \overline{G_2}$

Disable = $\overline{\overline{G_1} \cdot \overline{G_2}}$

= $G_1 \cdot G_2$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Power Switching

The Am27PS41 is a power-switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS41 is selected by a low level on $\overline{E_1}$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1 µf ceramic capacitor be connected from pin 20 to pin 10 at each device. (See Figure 1.)

2. Address access time (TAVQ1) can be optimized if a chip enable set-up time (TEVAV) of greater than 25 ns is observed. Negative set-up times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to + 5.5 V
DC Input Current ..... −30 mA to +5 mA

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military Products 100% tested at case temperature −55°C, +25°C, 125°C

2

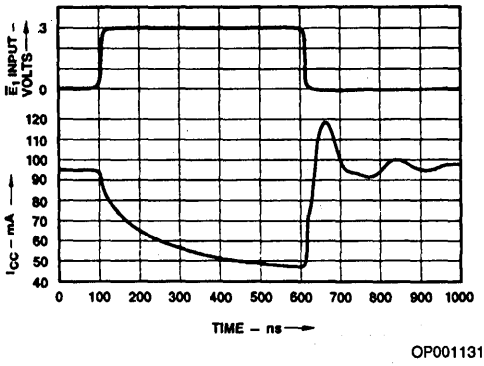
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}	COM'L			0.45	Volts
			MIL			0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 1)	COM'L	−20		−90	mA
			MIL	−15		−90	
I_{CC}	Power Supply Current	V_{CC} = Max. All inputs = 0.0 V	COM'L			165	mA
			MIL			170	
I_{CCD}	Am27PS Version Power Down Supply Current	V_{CC} = Max. $V_{\overline{E}_1}$ = 2.4 V, All other inputs = 0.0 V				85	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}_1}$ = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 2)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 2)			8.0		

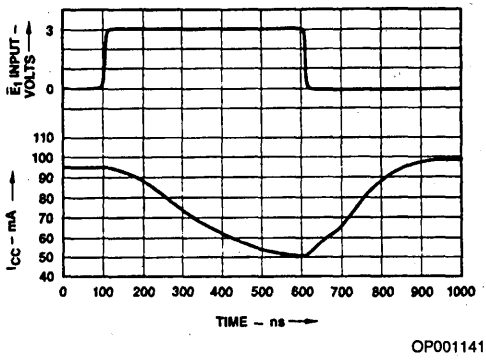
Notes: 1. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
2. These parameters are not 100% tested, but are periodically sampled.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

*See the last page of this spec for Group A Subgroup Testing information.

TYPICAL DC and AC OPERATING CHARACTERISTICS



Typical I_{CC} Current Surge without 0.1 mF (I_{CC} is Current Supplied by V_{CC} Power Supply)



Typical I_{CC} Current Surge with 0.1 mF (I_{CC} is Current Supplied by V_{CC} Power Supply)

Figure 1. I_{CC} Current

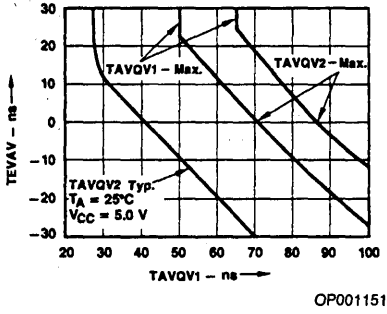


Figure 2A. TAVQV1 versus TEVAV

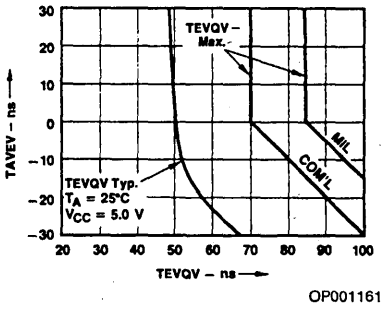
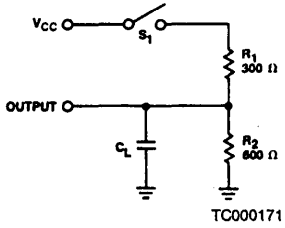


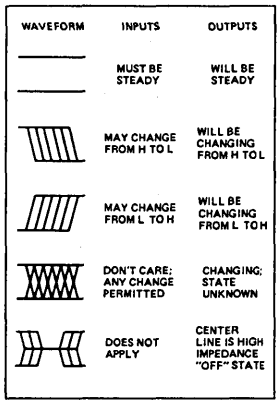
Figure 2B. TEVQV versus TAVEV

SWITCHING TEST CIRCUIT



TC000171

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

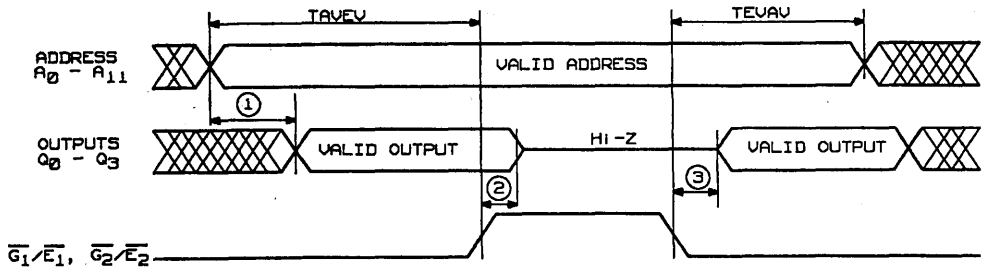
No.	Parameter Symbol	Parameter Description	Version	27S Version COM'L Min.	27S Version COM'L Max.	27S Version MIL Min.	27S Version MIL Max.	27PS Version COM'L Min.	27PS Version COM'L Max.	27PS Version MIL Min.	27PS Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	A		35		50					ns
			STD		50		65		50		65	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A		25		30					ns
			STD		25		30		25		30	
3	TGVQV	Delay from Output Enable Valid to Output Valid	A		25		30					ns
			STD		25		30		60		65	
4	TAVQV1	Power Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A						60		65	ns
			STD						80		90	

See Switching Test Circuit.

Notes: 1. TAVQV is tested with switch S_1 closed and $C_L = 5$ pF. TEVAV is defined as chip enable setup time.
2. For the three-state output, TGVQZ is tested with $C_L = 5$ pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQV is tested with $C_L = 5$ pF. HIGH to high-impedance tests are made with S_1 open to an output voltage of steady state HIGH −0.5 V; LOW to high-impedance tests are made with S_1 closed to the steady state LOW +0.5 V level.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021670

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
4	TAVQV1	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S43

32,768-Bit (4096 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

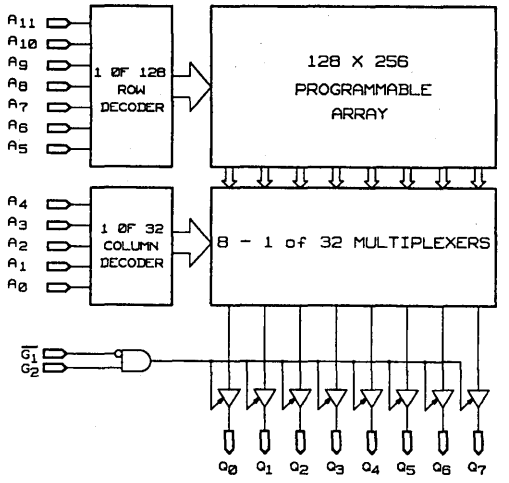
- Ultra-fast access time
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)

GENERAL DESCRIPTION

The Am27S43 (4096-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls.

BLOCK DIAGRAM



BD006310

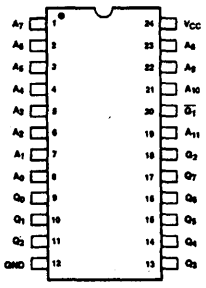
PRODUCT SELECTOR GUIDE

Part Number	27S43A		27S43	
Address Access Time	40 ns	55 ns	55 ns	65 ns
Operating Range	C	M	C	M

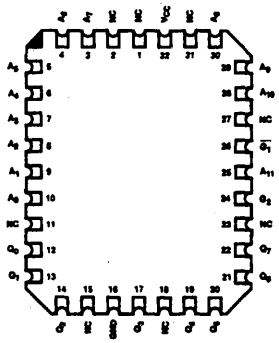
Publication # 03190 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

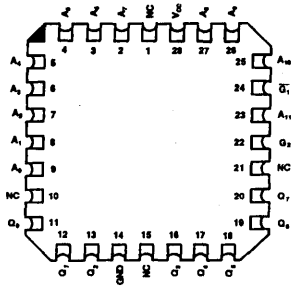
DIP*



CD000501



CD000511

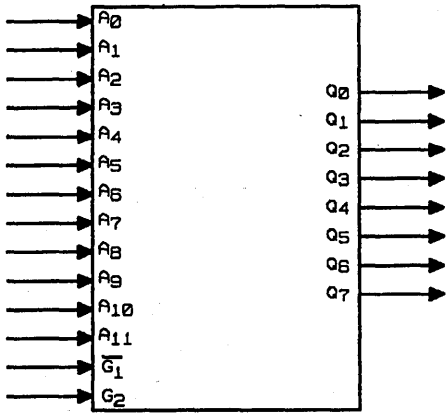


CD009490

*Also available in 24-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

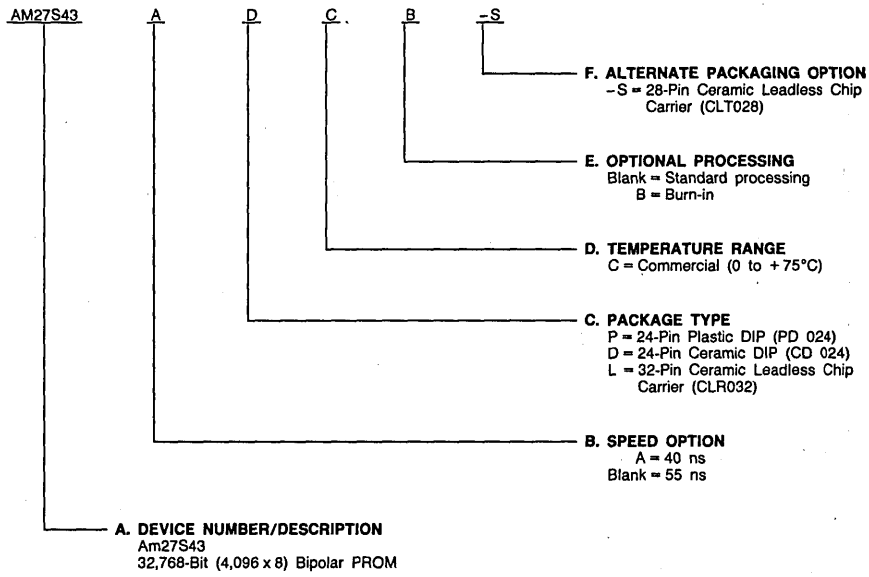


LS002401

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S43	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S
AM27S43A	

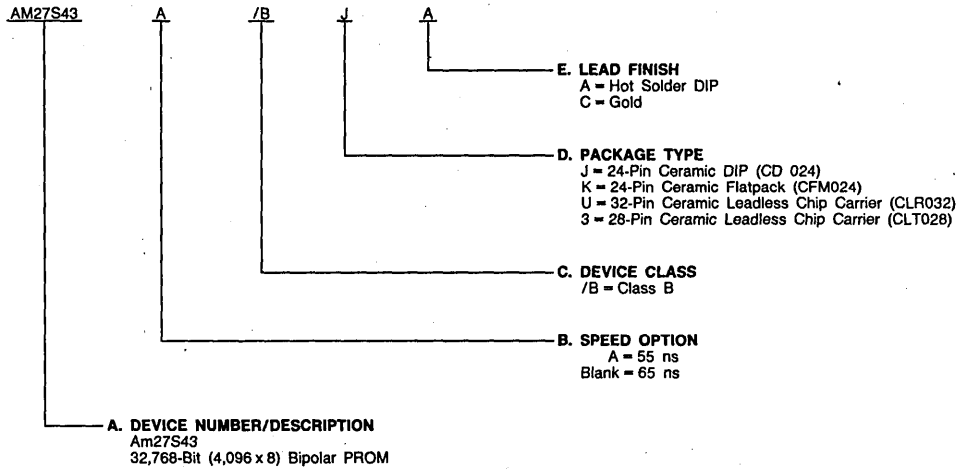
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S43	/BJA, /BKA, /BUC, /B3C
AM27S43A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address (Inputs)
The 12-bit field presented at the address inputs selects one of 4,096 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which when disabled are in a floating or high-impedance state.

$\overline{G_1}, \overline{G_2}$ Output Enable (Input)
Provides direct control of the Q-output, three-state buffers. Outputs disabled forces all outputs to to a floating or high-impedance state.

$$\text{Enable} = \overline{\overline{G_1} \cdot G_2}$$

$$\text{Disable} = \overline{G_1} \cdot G_2 = G_1 \cdot \overline{G_2}$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = +25°C, +125°C, and −55°C.

2

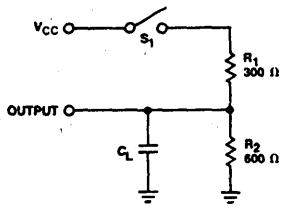
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−15		−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.	COM'L			185	mA
			MIL			185	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. V_{G1} = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 3)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 3)			8.0		

Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

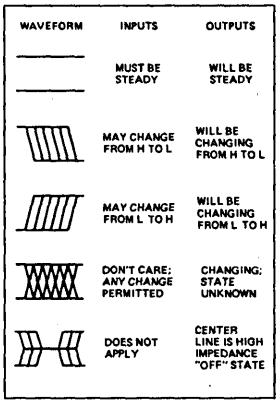
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



TC000171

KEY TO SWITCHING WAVEFORMS



KS000010

Notes: 1. TAVQV is tested with Switch S_1 closed and C_L = 30 pF.
2. For three-state outputs, TGVQZ is tested with C_L = 30 pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQV is tested with C_L = 5 pF. HIGH to high-impedance tests are made with S_1 open to an output voltage of V_{OH} −0.5 V; LOW to high-impedance tests are made with S_1 closed to the V_{OL} +0.5 V level.

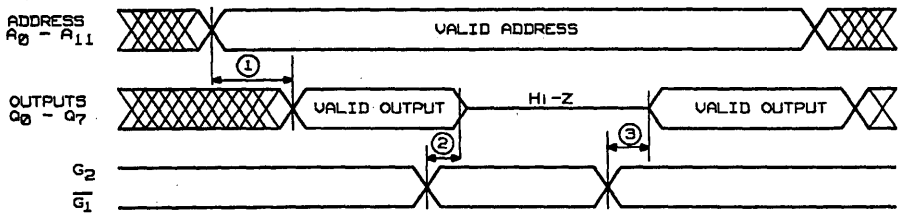
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		40		55		55		65	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		30		35		35		40	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		30		35		35		40	ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF021660

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S45/Am27S47

16,384-Bit (2048 x 8) Bipolar Registered PROM
with Programmable $\overline{\text{INITIALIZE}}$ Input

DISTINCTIVE CHARACTERISTICS

- "SA" version offers superior performance with 25 ns setup time and 10 ns clock-to-output delay*
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Versatile programmable asynchronous or synchronous enable for simplified word expansion
- Buffered common $\overline{\text{INITIALIZE}}$ input either asynchronous (Am27S45) or synchronous (Am27S47)
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)

GENERAL DESCRIPTION

The Am27S45 and the Am27S47 (2048-words by 8-bits) are fully decoded, Schottky array, TTL Programmable Read-Only Memories (PROMs), incorporating D-type master-slave data registers on chip. These devices have three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

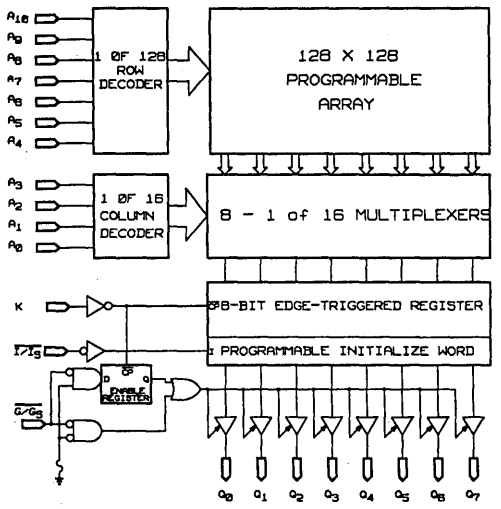
These devices contain an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To Offer the system designer maximum flexibility, these devices contain a user programmable asynchronous or synchronous output enable. The unprogrammed state of the enable pin operates as an Asynchronous Enable ($\overline{G}$) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ($\overline{G_S}$).

These devices contain a single pin initialize function capable of loading any arbitrary microinstruction for system interrupt or initialization. On the Am27S45 this function operates asynchronously, independent of clock. The Am27S47 provides synchronous operation of this function.

If the architecture has been programmed to synchronous enable, upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



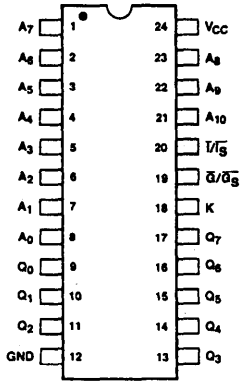
BD006381

Publication # 03186 | Rev. C | Amendment /0
Issue Date: May 1988

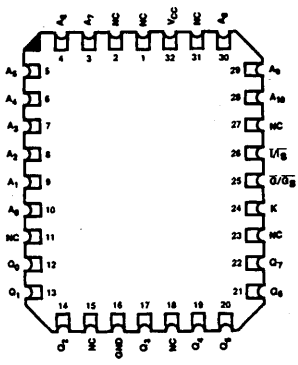
PRODUCT SELECTOR GUIDE

Part Number Asynchronous Initialize	27S45SA*		27S45A		27S45	
Part Number Synchronous Initialize	27S47SA*		27S47A		27S47	
Address Setup Time (ns)	25	28	40	45	45	50
Clock-to-Output Delay (ns)	10	12	20	25	25	30
Operating Range	C	M	C	M	C	M

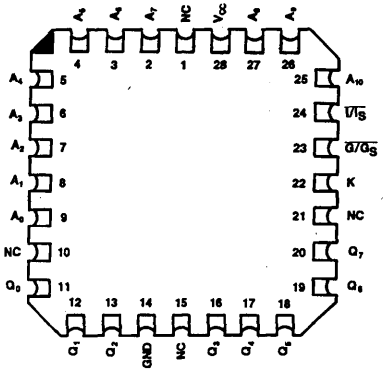
CONNECTION DIAGRAMS
Top View



CD000461



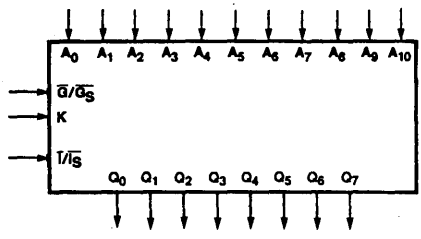
CD000471



CD009630

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



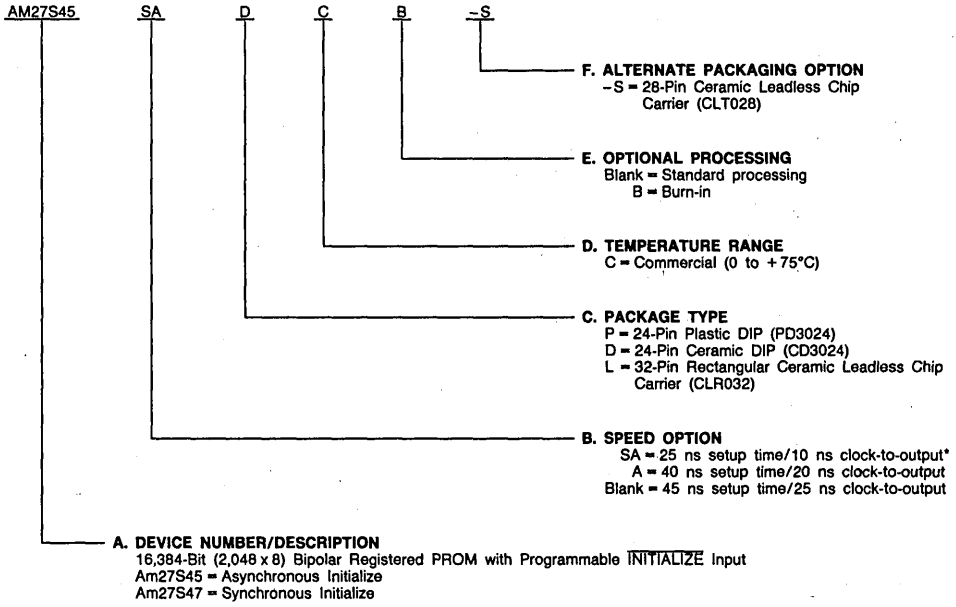
LS000051

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S45SA	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S
AM27S45A	
AM27S45	
AM27S47SA	
AM27S47A	
AM27S47	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

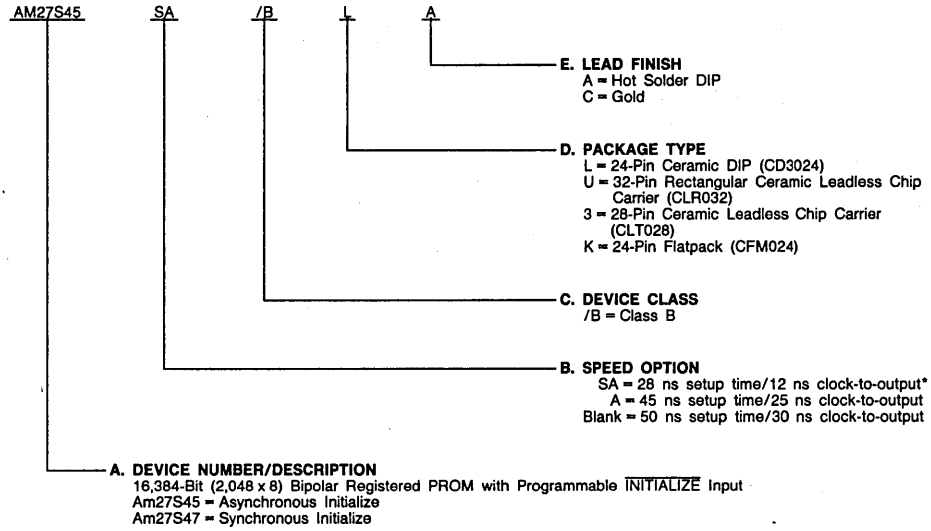
*Advance Information. Subject to Change.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S45SA	/BLA, /BKA, /BUC, /B3C
AM27S45A	
AM27S45	
AM27S47SA	
AM27S47A	
AM27S47	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

*Advance Information. Subject to Change.

PIN DESCRIPTION

$A_0 - A_{10}$ Address (Input)
The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

K Clock (Input)
The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

$Q_0 - Q_7$ Data Output Port
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

$\overline{I}$ Asynchronous Initialize (Input) (Am27S45)
Control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

$\overline{I_S}$ Synchronous Initialize (Input) (Am27S47)
Control pin used to initialize the output data registers from a programmable word in conjunction with K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

This device contains a single-bit architecture word which, according to programming, will provide one of the following functions.

$\overline{G}$ Asynchronous Output Enable (Input)
Provides direct control of the Q-output, three-state drivers independent of K.

$\overline{G_S}$ Synchronous Output Enable (Input)
Controls the state of the Q-output, three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word-depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

FUNCTIONAL DESCRIPTION

The Am27S45A/45 and Am27S47A/47 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 2048-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S45A/45 and Am27S47A/47 also offer maximum flexibility for system design by providing either synchronous or asynchronous initialize, and synchronous or asynchronous output enable.

When V_{CC} power is first applied, the state of the outputs will depend on whether the enable has been programmed to be a synchronous or asynchronous enable. If the synchronous enable ($\overline{G_S}$) is being used, the register will be in the set condition causing the outputs (Q_0 to Q_7) to be in the OFF or high-impedance state. If the asynchronous enable ($\overline{G}$) is being used, the outputs will come up in the OFF or high-impedance state only if the enable ($\overline{G}$) input is at a logic HIGH level. Reading data is accomplished by first applying the binary word address to the address inputs (A_0 through A_{10}) and a logic LOW to the enable input. During the address setup time, the stored data is accessed and loaded into the master flip-flops of the data register. Upon the next LOW-to-HIGH transition of the clock input (K), data is transferred to the slave flip-flops which drive the output buffers, and the accessed data will appear at the outputs (Q_0 through Q_7). If the asynchronous enable ($\overline{G}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable back to the logic LOW state. For devices using the synchronous enable ($\overline{G_S}$), the outputs will go into the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the next positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change, since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{I}$) causes the contents of an additional (2049th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{I}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{I}$ performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S45A/45 has an asynchronous initialize input ($\overline{I}$). Applying a LOW to the $\overline{I}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register independent of all other inputs (including K). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{G}$) LOW.

The Am27S47A/47 has a synchronous $\overline{I_S}$ input. Applying a LOW to the $\overline{I_S}$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including K). To bring this data to the outputs of a device with a synchronous enable, the synchronous enable ($\overline{G_S}$) should be held LOW until the next LOW-to-HIGH transition of the clock (K). For a device with an asynchronous enable, the data will appear at the device outputs after the next LOW-to-HIGH clock transition if the enable ($\overline{G}$) is held LOW.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

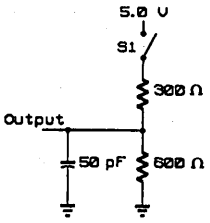
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}					0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V					−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}					40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)			−20		−90	mA
I_{CC}	Power Supply Current	Am27S45/Am27S47 Standard & "A" versions V_{CC} = Max., All inputs = 0.0 V					185	mA
		Am27S45/Am27S47 "SA" version only V_{CC} = Max., All inputs = 0.0 V (Note 5)	COM'L	T_A = 0°C			195	
				T_A = 25°C			190	
				T_A = 75°C			175	
			MIL	T_C = −55°C			210	
				T_C = 25°C			190	
				T_C = 125°C			160	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.					185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}}$ = 2.4 V	(Note 3)	V_O = V_{CC}			40	µA
				V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4)				5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4)				12		

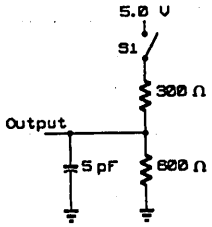
Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. These parameters are not 100% tested, but are periodically sampled.
5. I_{CC} limits at temperature extremes are guaranteed by correlation to +25°C test limits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS



TC003442

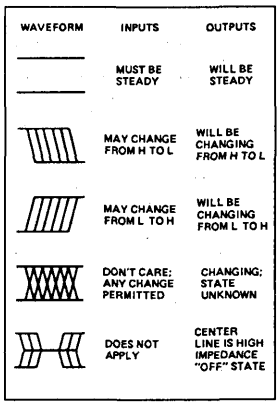


TC003452

A. Output Load for all AC tests except TGHQZ and TKHQZ

B. Output Load for TGHQZ and TKHQZ

KEY TO SWITCHING WAVEFORMS



KS000010

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)*

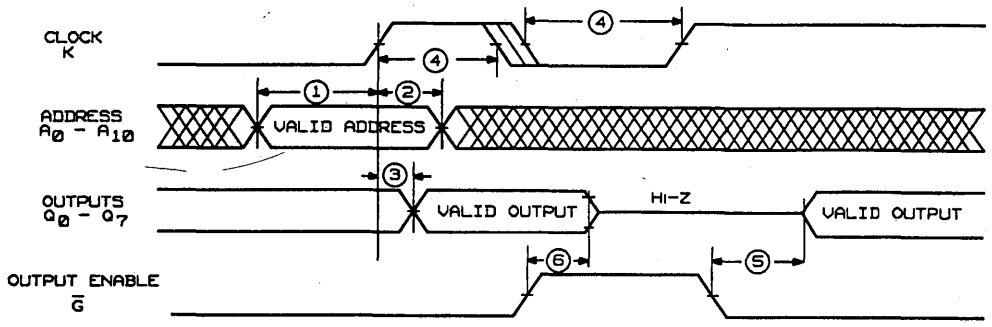
No.	Parameter Symbol	Parameter Description		"SA" Version Min.	"SA" Version Max.	"A" Version Min.	"A" Version Max.	Standard Version Min.	Standard Version Max.	Units
1	TAVKH	Address to K HIGH Setup Time	COM'L	25		40		45		ns
			MIL	28		45		50		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		0		ns
			MIL	0		0		0		
3	$TKHQV_1$	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 7)	COM'L	4	10		20		25	ns
			MIL	4	12		25		30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	15		20		20		ns
			MIL	20		20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (Note 3)	COM'L		17		25		30	ns
			MIL		20		30		35	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (Notes 2 & 3)	COM'L		17		25		30	ns
			MIL		20		30		35	
7	TGSVKH	$\overline{G_S}$ to K HIGH Setup Time (Note 4)	COM'L	10		15		15		ns
			MIL	15		15		15		
8	TKHGSX	$\overline{G_S}$ to K HIGH Hold Time (Note 4)	COM'L	5		5		5		ns
			MIL	5		5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (Note 4)	COM'L		17		25		30	ns
			MIL		20		30		35	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (Notes 2 & 4)	COM'L		17		25		30	ns
			MIL		20		30		35	
11	TILQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (Note 5)	COM'L		17		30		35	ns
			MIL		20		35		40	
12	TIHKH	Asynchronous $\overline{I}$ Recovery Time (Note 5)	COM'L	17		20		20		ns
			MIL	20		20		20		
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (Note 5)	COM'L	15		25		25		ns
			MIL	20		30		30		
14	TISVKH	$\overline{I_S}$ to K HIGH Setup Time (Note 6)	COM'L	15		25		30		ns
			MIL	20		30		35		
15	TKHISX	$\overline{I_S}$ to K HIGH Hold Time (Note 6)	COM'L	0		0		0		ns
			MIL	0		0		0		

See also Switching Test Circuits.

Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A. under Switching Test Circuits.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B. under Switching Test Circuits.
3. Applies only when Asynchronous Enable ($\overline{G}$) function is used.
4. Applies only when Synchronous Enable ($\overline{G_S}$) function has been programmed.
5. Applies only to the Am27S45 (Asynchronous Initialize ($\overline{I}$)) version.
6. Applies only to the Am27S47 (Synchronous Initialize ($\overline{I_S}$)) version.
7. Minimum delay time is guaranteed by design and supported by characterization data.

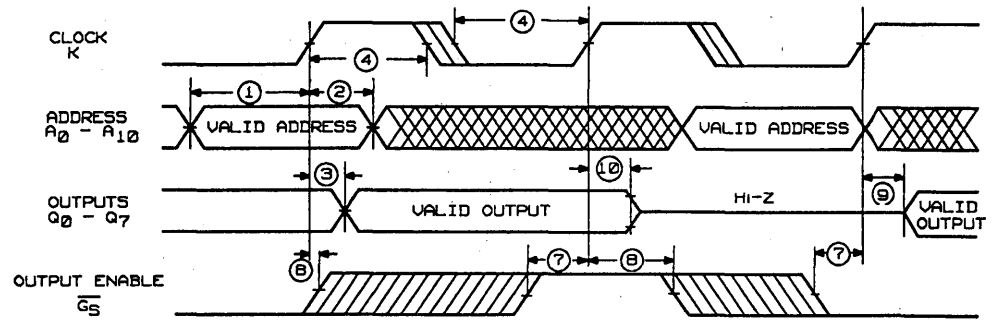
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Cont'd.)



WF021691

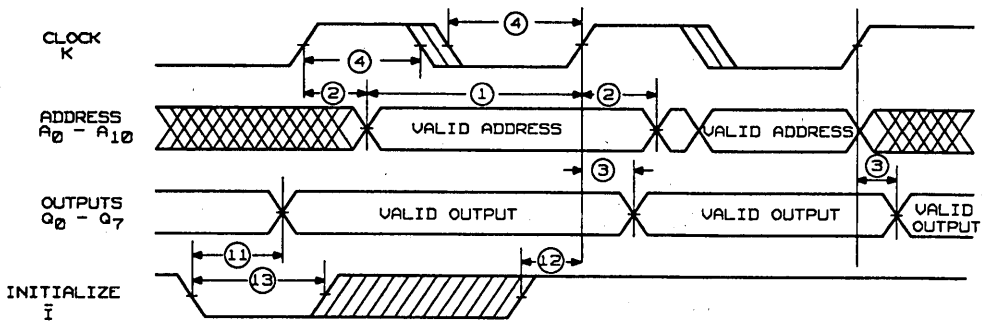
Timing Set 1. Using Asynchronous Enable



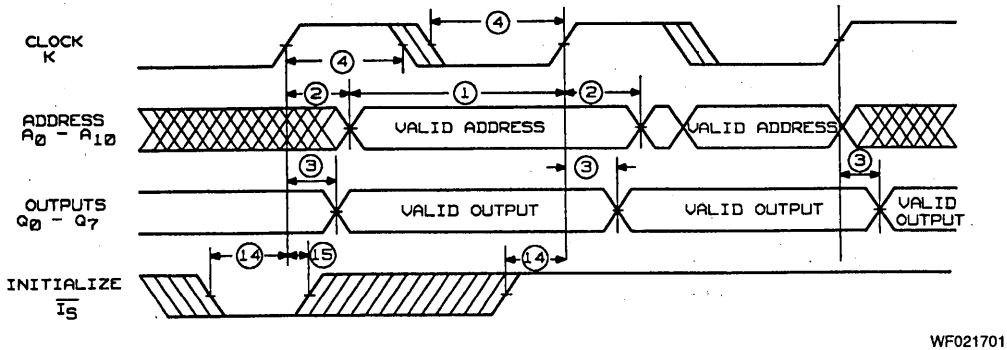
WF021711

Timing Set 2. Using Synchronous Enable

SWITCHING WAVEFORMS



Timing Set 3. Using Asynchronous Initialize
Am27S45 Only



Timing Set 4. Using Synchronous Initialize
Am27S47 Only

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVKH	9, 10, 11	9	TKHQV2	9, 10, 11
2	TKHAX	9, 10, 11	10	TKHQZ	9, 10, 11
3	TKHQV1	9, 10, 11	11	TILQV	9, 10, 11
4	TKHKL TKLKH	9, 10, 11	12	TIHKH	9, 10, 11
5	TGLQV	9, 10, 11	13	TILIH	9, 10, 11
6	TGHQZ	9, 10, 11	14	TISVKH	9, 10, 11
7	TGSVKH	9, 10, 11	15	TKHISX	9, 10, 11
8	TKHGSX	9, 10, 11		Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S49/27S49A-45/27S49A

8192 x 8 Generic Series IMOX™ Bipolar PROM

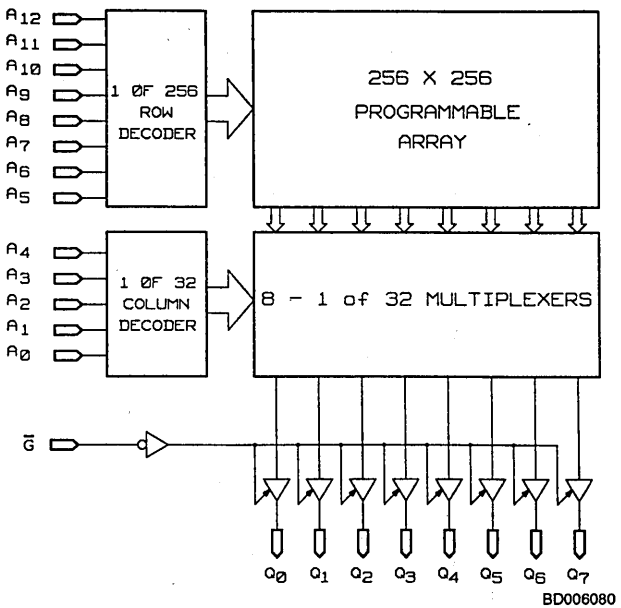
DISTINCTIVE CHARACTERISTICS

- Fast access time
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range

GENERAL DESCRIPTION

The Am27S49A and Am27S49 are high-speed, electrically programmable Schottky read only memories, organized in 8192 x 8 configuration. Outputs are three-state. After programming, stored information is read on outputs $Q_0 - Q_7$ by applying unique binary addresses to $A_0 - A_{12}$ and holding the Output Enable ($\overline{G}$) input, LOW. If $\overline{G}$ goes to logic HIGH, $Q_0 - Q_7$ goes to the OFF, or high-impedance state.

BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

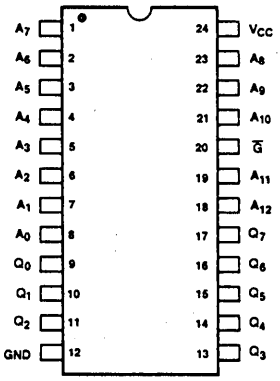
Part Number	Am27S49A		Am27S49A-45	Am27S49	
Address Access Time (ns)	40	55	45	55	65
Operating Range	C Devices	M Devices	C Devices only	C Devices	M Devices

IMOX is a trademark of Advanced Micro Devices, Inc.

Publication # 04943 Rev. E Amendment /0
Issue Date: May 1986

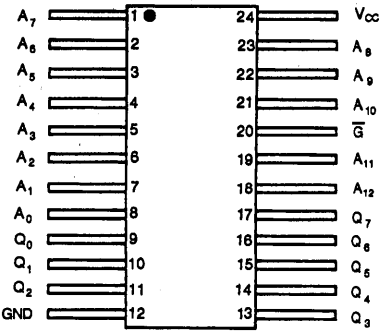
CONNECTION DIAGRAMS
Top View

DIPs



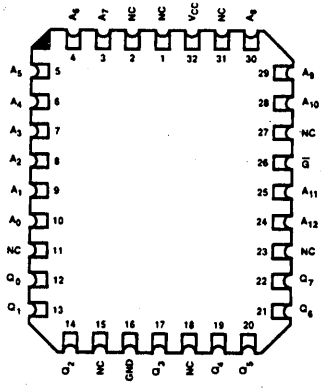
CD001031

Flatpack

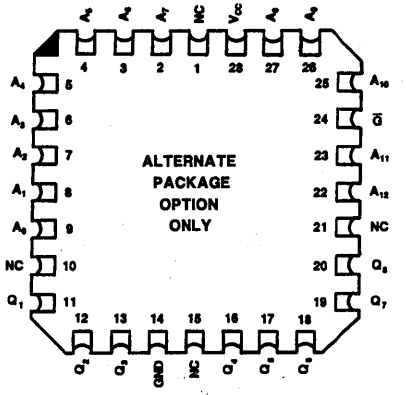


CD009360

LCCs



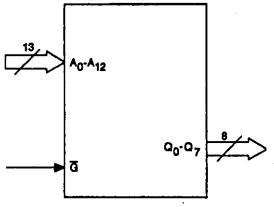
CD000971



CD008021

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



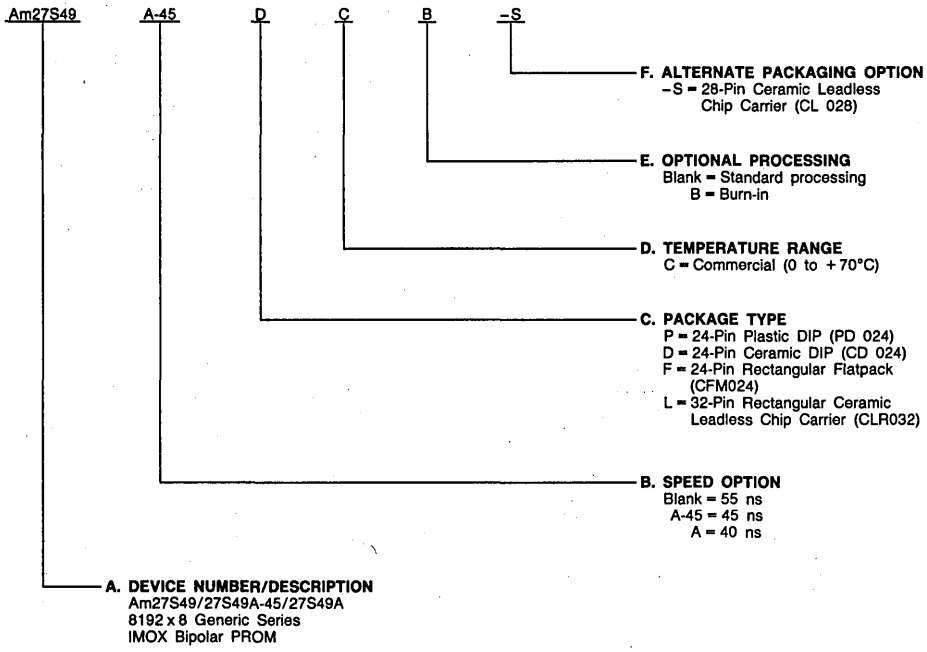
LS002330

VCC = Positive Power Supply
GND = Negative Power Supply

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S49	DC, DCB, PC, PCB, FC, FCB, LC, LCB, LC-S, LCB-S
AM27S49A-45	
AM27S49A	

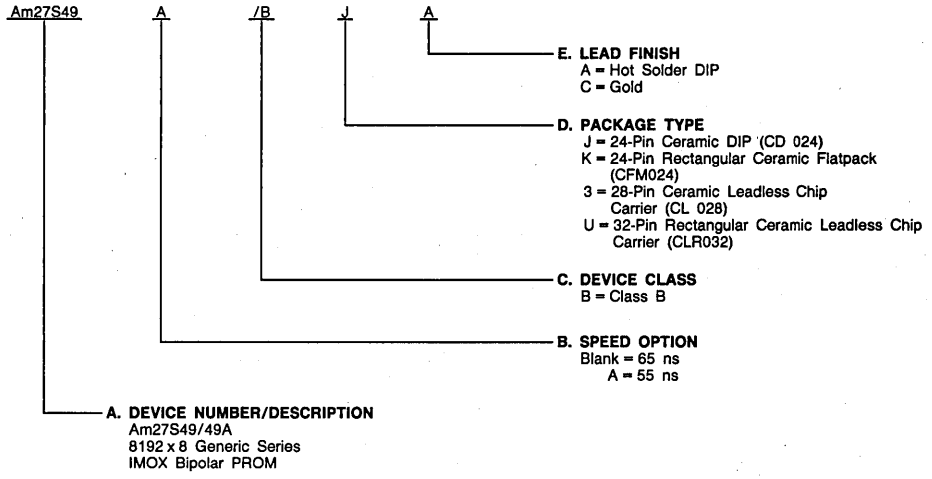
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
Am27S49	/BJA, /BKA, /B3C, /BUC
Am27S49A	

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{12}$ Address (Inputs)
The 13-bit field presented at the address inputs selects one of 16,384 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port (Outputs, Three-State)
The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which when disabled, are in a floating or high-impedance state.

$\overline{G}$ Output Enable (Input, Active LOW)
Provides direct control of the Q-output three-state buffers.

V_{CC} Power-Supply Pin
The most positive of the logic power-supply pins.

GND Power-Supply Pin
The most negative of the logic power-supply pins.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

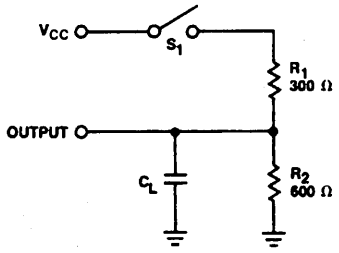
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V			−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−15	−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.	COM'L		190	mA
			MIL		190	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. V_{CS} = 2.4 V	V_O = V_{CC}		40	µA
			V_O = 0.4 V		−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 3)				pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 3)				

Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

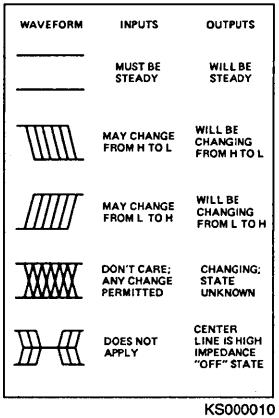
SWITCHING TEST CIRCUIT



TC000171

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30 pF.
2. For three-state outputs, t_{EA} is tested with C_L = 30 pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5 pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5 V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5 V level.

KEY TO SWITCHING WAVEFORMS



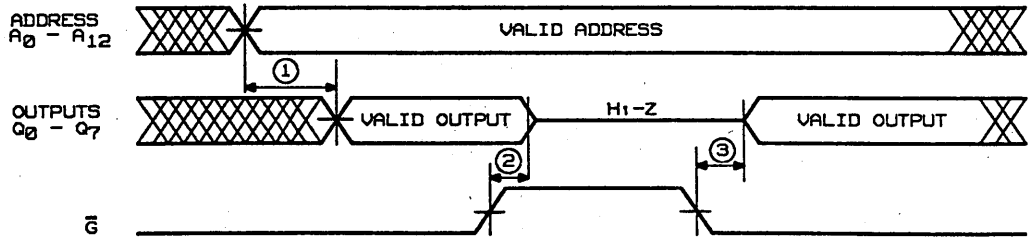
KS000010

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description		Am27S49A Min.	Am27S49A Max.	Am27S49A-45 Min.	Am27S49A-45 Max.	Am27S49 Min.	Am27S49 Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time	C Devices		40		45		55	ns
			M Devices		50		–		65	
2	TGVQZ	Delay from Output Enable Valid to Output High Z	C Devices		30		30		35	ns
			M Devices		35		–		40	
3	TGVQV	Delay from Output Enable Valid to Output Valid	C Devices		30		30		35	ns
			M Devices		35		–		40	

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V — See Switching Test Circuit diagram.

SWITCHING WAVEFORMS



WF021480

Am27S51

131,072-Bit (16,384 x 8) Bipolar PROM

ADVANCE INFORMATION

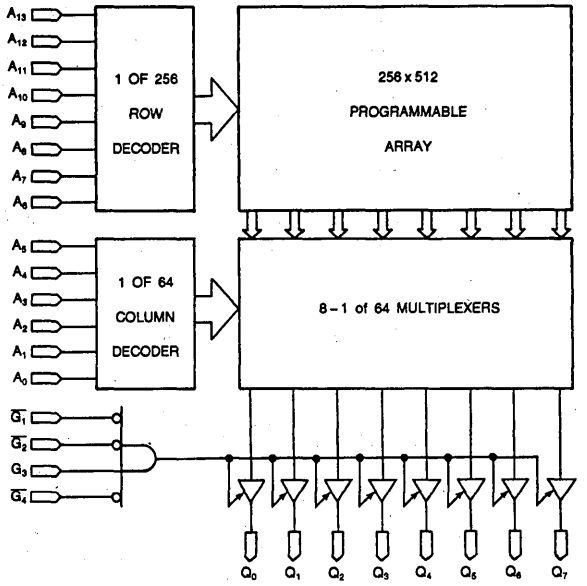
DISTINCTIVE CHARACTERISTICS

- Ultra fast access time (35 ns max.) "A" version, and fast access time (55 ns max.) standard version
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%).
- AC performance is factory tested, utilizing programmed test words and columns.
- Voltage and temperature compensated, providing extremely flat AC performance over Military Range.
- Member of generic PROM series, utilizing standard programming algorithm.

GENERAL DESCRIPTION

The Am27S51/51A (16,384 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM). This device has three-state outputs, compatible with low-power Schottky bus standards, capable of satisfying the requirements of a variety of microprogrammable controls.

BLOCK DIAGRAM



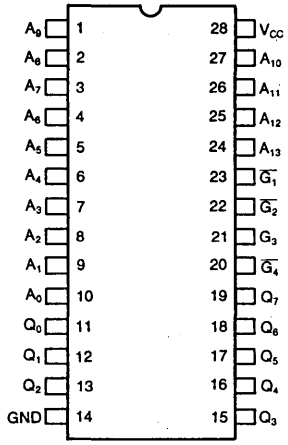
BD005362

PRODUCT SELECTOR GUIDE

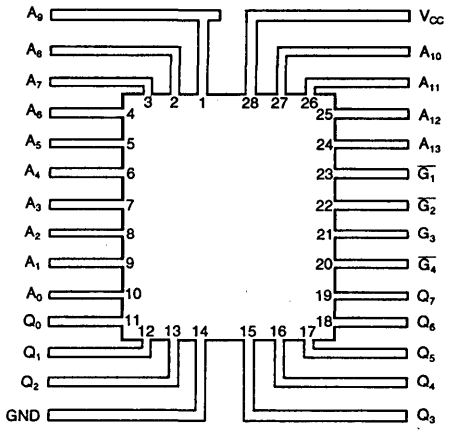
Part Number	Am27S51A		Am27S51	
Address Access Time	35 ns	45 ns	55 ns	65 ns
Operating Range	C	M	C	M

Publication # 06915 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

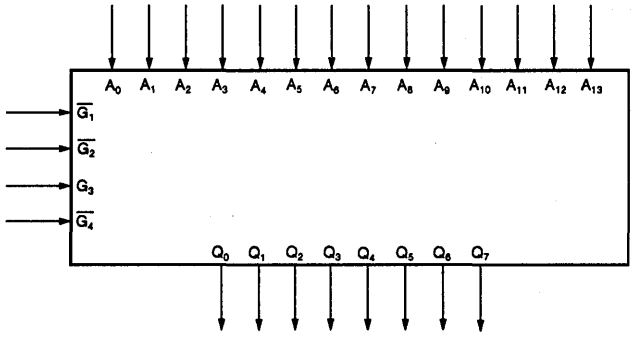


CD006070



CD006081

LOGIC SYMBOL

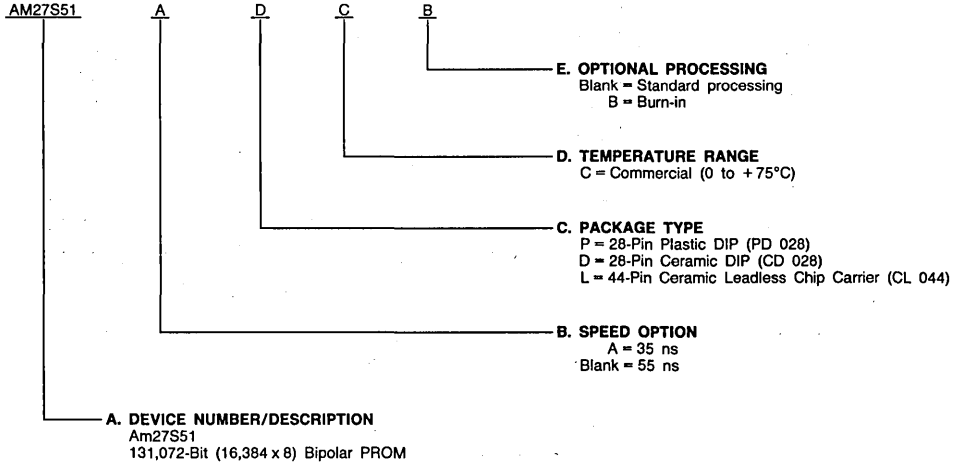


LS002510

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



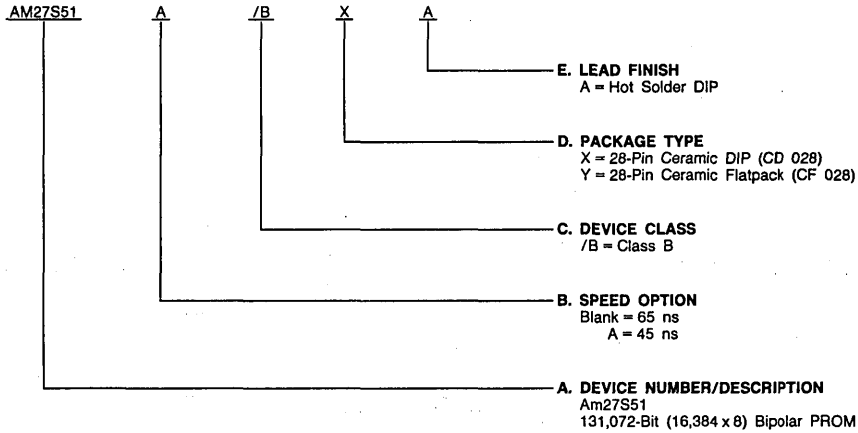
Valid Combinations	
AM27S51	DC, DCB PC, PCB LC, LCB
AM27S51A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S51	/BXA, /BYA
AM27S51A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{13}$ Address (Inputs)
The 14-bit field presented at the address inputs select one of 16,384 memory locations to be read from.

$Q_0 - Q_7$ Data Out Port (Output, Three-State)
The outputs whose state represents the data read from the selected memory locations. These outputs are three-state buffers which when enabled, are in a floating or high-impedance state.

$\overline{G_1}$, $\overline{G_2}$, G_3, $\overline{G_4}$ Output Enables
Provides direct control of the Q-output three-state buffers.
Disable = $G_1 + G_2 + \overline{G_3} + G_4$ – FALSE
Enable = $\overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}$ – TRUE

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 to +5.25 V
Military (M) Devices
Case Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military product 100% tested at −55°C, 25°C, and 125°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0			Volts
V_{IL}	Input LOW Level	Guranteed input logical LOW voltage for all inputs (Note 1)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−15		−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.				190	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max., G_3 = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 3)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 3)			8.0		

Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

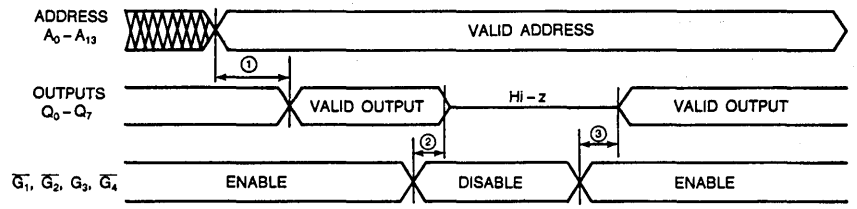
No.	Parameter Symbol	Parameter Description	"A" Version				Standard Version				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		65	
2	TGVQZ	Delay from Output Enable Valid to Output Hi−Z		25		30		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		25		30		25		30	

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A. under Switching Test Circuits.
2. TGVQZ is measured to the steady state HIGH − 0.5 V and steady state LOW + 0.5 V output levels using the test load in B. under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

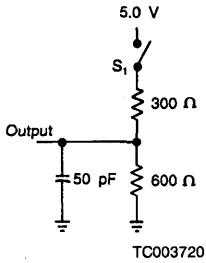
SWITCHING WAVEFORM



WF010542

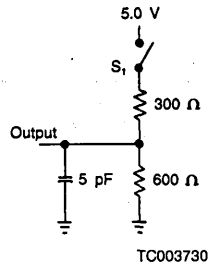
2

SWITCHING TEST CIRCUITS



TC003720

A. Output Load for all A-C tests except TGVQZ



TC003730

B. Output Load for TGVQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S55

32,768-Bit (4096 x 8) Bipolar Registered PROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- "A" version offers superior performance with 20 ns set-up time and 10 ns clock-to-output delay
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- User-programmable for Asynchronous Enable, Synchronous Enable, Asynchronous Initialize, or Synchronous Initialize
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (Typ. > 98%)

GENERAL DESCRIPTION

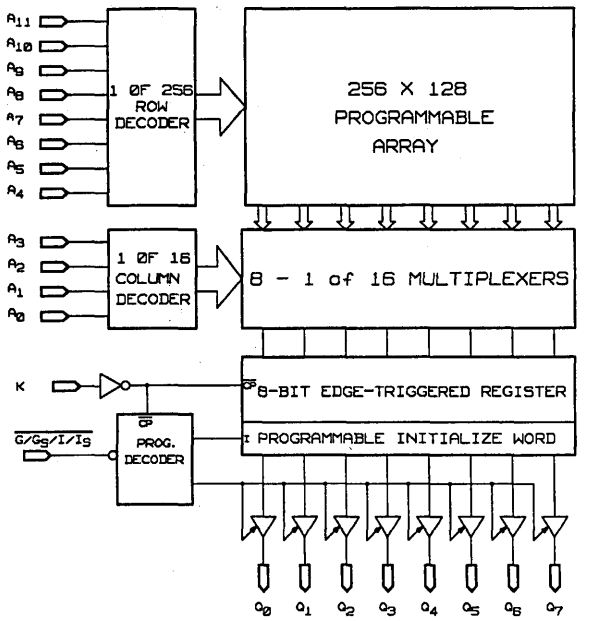
The Am27S55 (4096 words by 8 bits) is a fully decoded Schottky Array TTL Programmable Read-Only Memory (PROM) incorporating D-type master-slave data registers on-chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains a single programmable multi-functional input ($\overline{G}/\overline{G_S}/\overline{I}/\overline{I_S}$). The unprogrammed state of this pin operates as an Asynchronous Enable ($\overline{G}$) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ($\overline{G_S}$), Asynchronous Initialize ($\overline{I}$), or Synchronous Initialize ($\overline{I_S}$).

If the architecture has been programmed to synchronous enable, upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



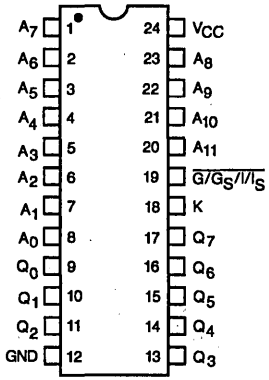
BD006440

Publication # 08130 | Rev. A | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

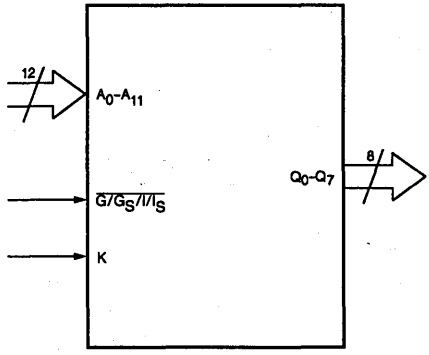
Part Number	Am27S55A		Am27S55	
Address Setup Time (ns)	20	25	25	30
Clock-to-Output Delay (ns)	10	13	13	16
Operating Range	C	M	C	M

CONNECTION DIAGRAM
Top View



CD009590

LOGIC SYMBOL

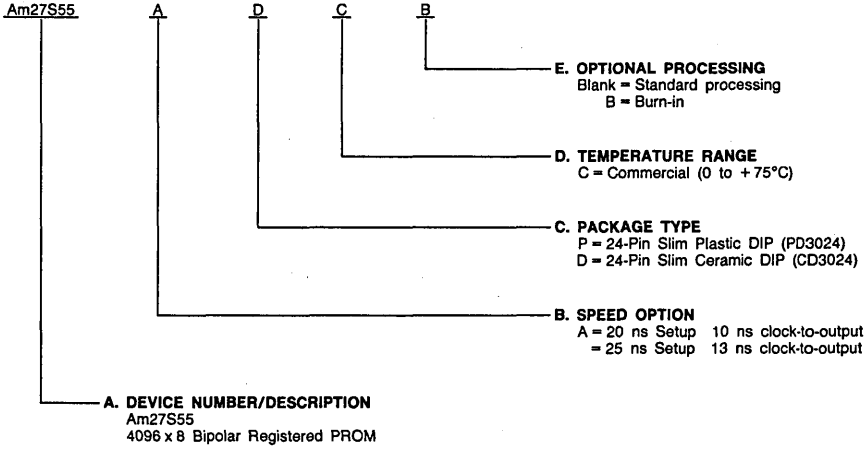


LS002450

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S55	DC, DCB
AM27S55A	PC, PCB

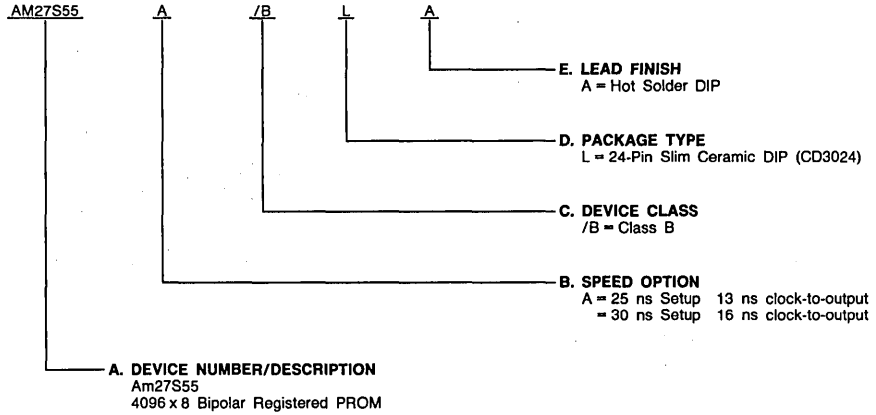
Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S55	/BLA
AM27S55A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address (Inputs)
The 12-bit field presented at the address inputs selects one of 4096 memory locations to be read from.

K Clock (Input)
The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

$Q_0 - Q_7$ Data Output Port (Output)
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high-impedance.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

This device contains a two bit architecture word which, when programmed, will provide one of the following functions:

$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ Asynchronous/Synchronous Output Enable/ Asynchronous/Synchronous Initialize (Input)
With the architecture word unprogrammed, this pin operates as an Asynchronous Output Enable ($\overline{G}$) and provides direct control of the DQ output three-state drivers independent of K. With proper programming of the architecture word, this pin will function as a Synchronous Output Enable ($\overline{GS}$) which will control the state of the DQ output three-state drivers in conjunction with K. This is useful where more than one registered PROM is bused together for word-depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The architecture word may also be programmed so that this pin will function as an Asynchronous Initialize ($\overline{I}$) which is a control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed, this pin will function as a Synchronous Initialize ($\overline{IS}$) which will initialize the output data registers from a programmable word in conjunction with K. This can be used for a system interrupt or reset which must be synchronized with K.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
Except During Programming ..... −0.5 V to V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
DC Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military Products 100% tested at −55°C, +25°C, 125°C

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{IH}	Input Voltage (HIGH)	Guaranteed Input HIGH Voltage (Note 1)			2.0		Volts
V_{IL}	Input Voltage (LOW)	Guaranteed Input LOW Voltage (Note 1)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
V_{OH}	Output Voltage (HIGH)	V_{CC} = Min., I_{OH} = −2 mA V_{IN} = V_{IH} or V_{IL}			2.4		Volts
V_{OL}	Output Voltage (LOW)	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
I_{IH}	Input Current (HIGH)	V_{CC} = Max.	V_{IN} = 2.7 V			25	µA
			V_{IN} = 5.5 V			40	
I_{IL}	Input Current (LOW)	V_{CC} = Max., V_{IN} = 0.45 V				−250	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_O = 0 V (Note 2)			−20	−90	mA
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}/\overline{GS}}$ = 2.4 V (Note 3)	V_{OUT} = V_{CC}			40	µA
			V_{OUT} = 0.4 V			−40	
I_{CC}	Power Supply Current	V_{CC} = Max., All Inputs = 0.0 V	COM'L	T_A = 0°C		185	mA
				T_A = 25°C		175	
				T_A = 75°C		165	
			MIL	T_C = −55°C		195	
				T_C = 25°C		180	
				T_C = 125°C		155	

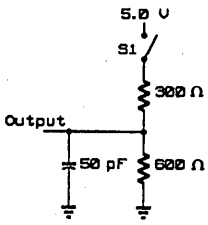
Notes: 1. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.
2. Not more than one output should be shorted at a time. Duration of the short-circuit should not be more than one second.
3. For devices which have been programmed for Synchronous Enable ($\overline{GS}$), the device must be clocked after applying these voltages to perform this measurement.

Capacitance*

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.00 V, T_A = 25°C V_{IN}/V_{OUT} = 2.0 V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		12	

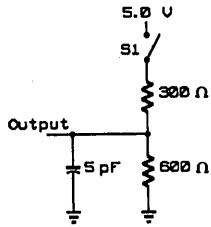
*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUITS



TC003442

A. Output Load for all Switching tests except TGHQZ and TKHQZ

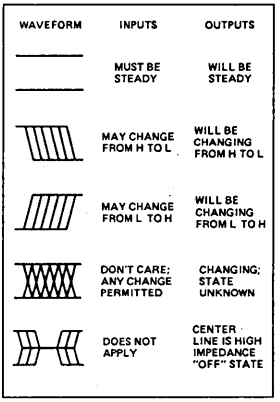


TC003452

B. Output Load for TGHQZ and TKHQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other Switching tests.
3. Load capacitance includes all stray and fixture capacitance.

KEY TO SWITCHING WAVEFORMS



KS000010

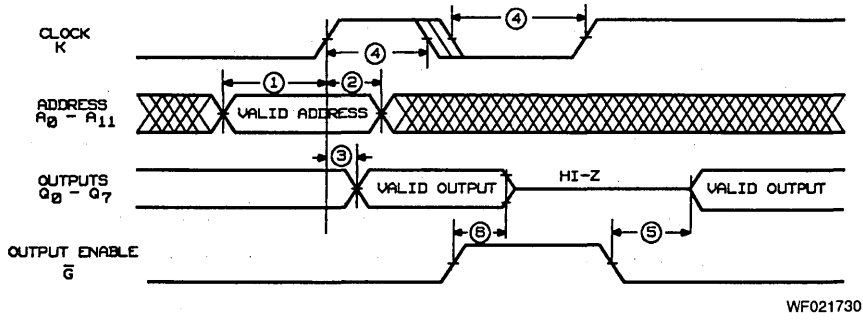
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

No.	Parameter Symbol	Parameter Description		"A" Version Min.	"A" Version Max.	Standard Version Min.	Standard Version Max.	Units
1	TAVKH	Address to K HIGH Setup Time	COM'L	20		25		ns
			MIL	25		30		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)	COM'L		10		13	ns
			MIL		13		16	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	15		20		ns
			MIL	20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (Note 3)	COM'L		15		20	ns
			MIL		20		25	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (Notes 2 & 3)	COM'L		15		20	ns
			MIL		20		25	
7	TGSVKH	$\overline{G_S}$ to K HIGH Setup Time (Note 4)	COM'L	10		15		ns
			MIL	15		15		
8	TKHGSX	$\overline{G_S}$ to K HIGH Hold Time (Note 4)	COM'L	5		5		ns
			MIL	5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (Note 4)	COM'L		13		18	ns
			MIL		18		21	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (Notes 2 & 4)	COM'L		13		18	ns
			MIL		18		21	
11	TILQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (Note 5)	COM'L		17		20	ns
			MIL		20		25	
12	TIHKH	Asynchronous $\overline{I}$ Recovery Time (Note 5)	COM'L	17		20		ns
			MIL	20		25		
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (Note 5)	COM'L	15		20		ns
			MIL	20		20		
14	TISVKH	$\overline{I_S}$ to K HIGH Setup Time (Note 6)	COM'L	15		20		ns
			MIL	20		25		
15	TKHISX	$\overline{I_S}$ to K HIGH Hold Time (Note 6)	COM'L	0		0		ns
			MIL	0		0		

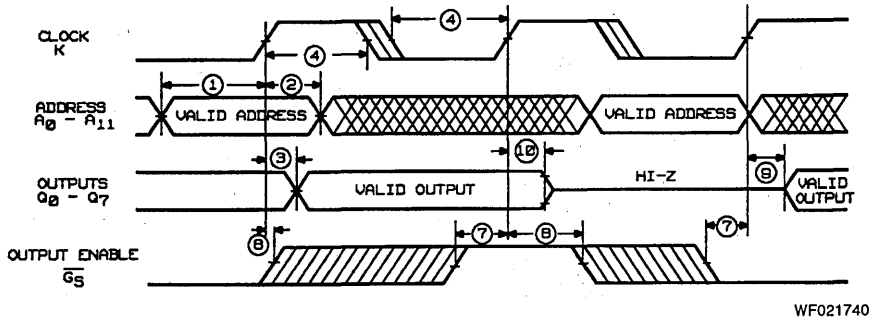
See also Switching Test Loads

Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in Diagram A.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in Diagram B.
3. Applies only when Asynchronous Enable ($\overline{G}$) function is used.
4. Applies only when Synchronous Enable ($\overline{G_S}$) has been programmed.
5. Applies only when (Asynchronous Initialize ($\overline{I}$)) has been programmed.
6. Applies only when (Synchronous Initialize ($\overline{I_S}$)) has been programmed.

SWITCHING WAVEFORMS (Cont'd.)

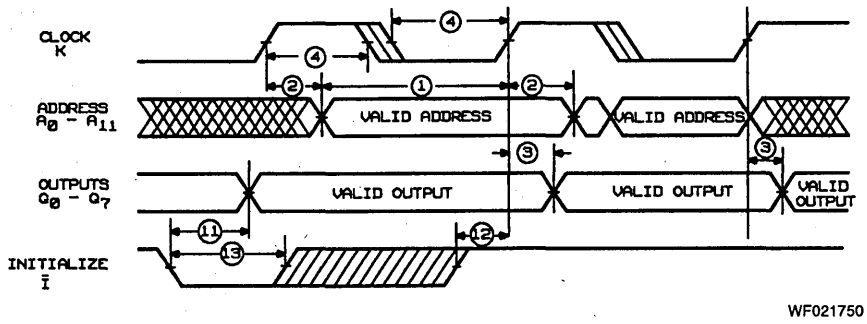


Timing Set 1 - Using Asynchronous Enable

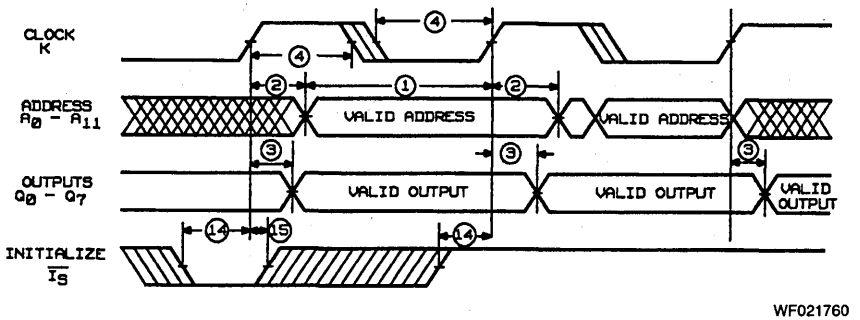


Timing Set 2 - Using Synchronous Enable

SWITCHING WAVEFORMS



Timing Set 3 - Using Asynchronous Initialize



Timing Set 4 - Using Synchronous Initialize

Am27S65

4096-Bit (1024 x 4) Bipolar Registered PROM
with SSR ™ Diagnostics Capability

DISTINCTIVE CHARACTERISTICS

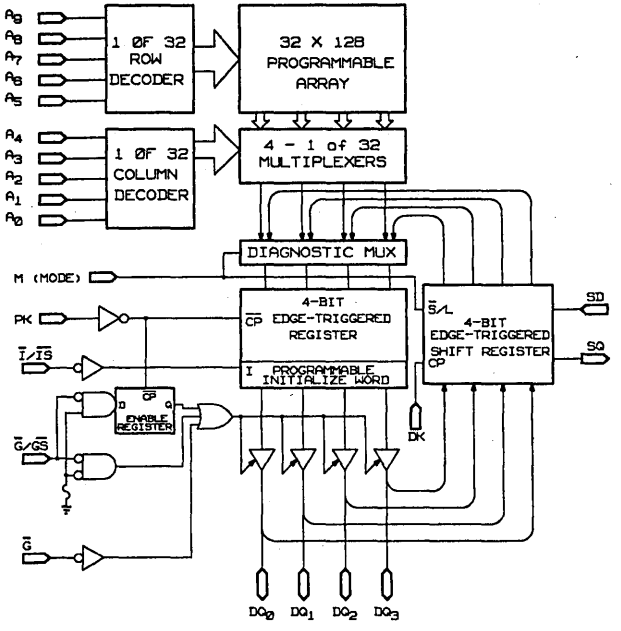
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable Enable Pin for Asynchronous or Synchronous Enable operation
- User-programmable Initialization Pin for Asynchronous or Synchronous Initialize operation
- Slim, 24-pin, 300-mil lateral center package permits a reduction in board space over standard discrete PROM and registers
- Consumes approximately ½ the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)
- Increased drive capability, 24 mA I_{OL}

GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains user-programmable architecture for Enable and Initialize. The unprogrammed state of these pins operates as Asynchronous inputs ($\overline{G}$) and ($\overline{I}$), respectively. An architecture word permits the programming of the functionality of these pins to Synchronous Enable ($\overline{GS}$) and Synchronous Initialize ($\overline{IS}$). A non-programmable Asynchronous Enable ($\overline{G}$) is also provided.

BLOCK DIAGRAM



BD005830

SSR is a trademark of Advanced Micro Devices, Inc.

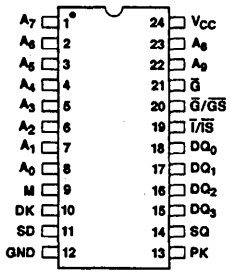
Publication # 05271 | Rev. C | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

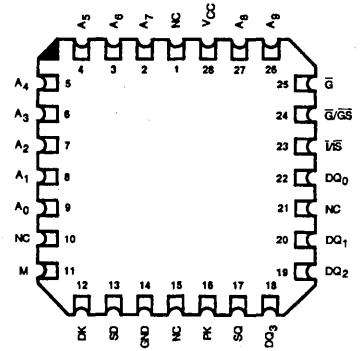
Part Number	27S65A	27S65	27S65A	27S65
Address Set-up Time	23 ns	30 ns	27 ns	35 ns
Clock-to-Output Delay	10 ns	15 ns	13 ns	20 ns
Operating Range	C	C	M	M

CONNECTION DIAGRAMS

Top View



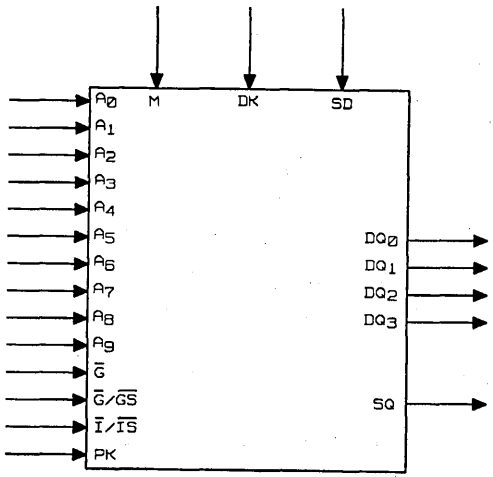
CD000541



CD004901

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

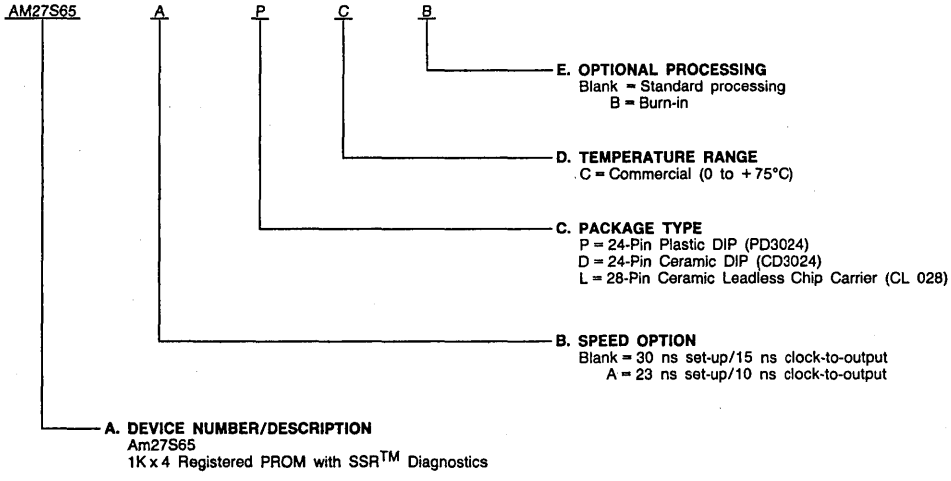


LS002100

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S65	PC, PCB, DC, DCB, LC, LCB
AM27S65A	

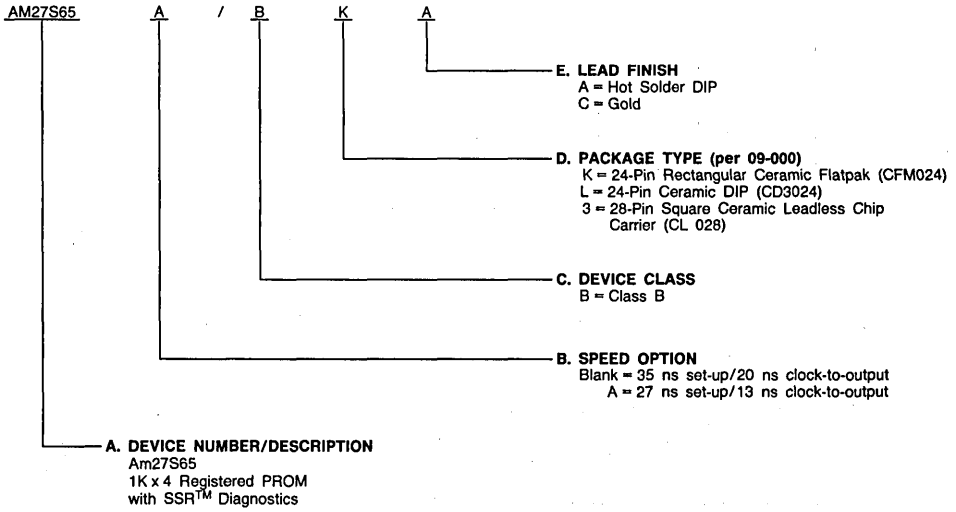
Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S65	/BKA, /BLA, /B3C
AM27S65A	

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the parallel registers. The data source may be the memory array, the shadow register, or the initialize word if programmed for synchrounous initialize architecture. Transfer occurs on the LOW-to-HIGH transition of PK.

$DQ_0 - DQ_3$ Data I/O Port
Parallel data output from the pipeline register or parallel data input to the shadow register.

M Mode (Input)
Control input which controls the source data for both sets of registers, MODE input is LOW in the normal mode of operation. The PROM Array is the input source for the output data registers. The shadow register is in the shift mode ($SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output registers or output data bus information may be loaded into the shadow register.

DK Diagnostic Clock (Input)
The Diagnostic clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DK.

SD Serial Data Input
This pin performs two functions depending on the state of the MODE input. If M is LOW, the SD pin is the data transfer pin for serial data ($SD \longrightarrow S_0$). IF the M input is HIGH, the SD pin operates as a control pin where SD asserted LOW permits output data to be loaded into the shadow register on the next LOW-to-HIGH transtion of DK. SD asserted HIGH represents a NO-OP function on this device.

SQ Serial Data Output
This pin operates as a transfer pin for serial data. When M input is LOW, $SQ = S_3$. When M is HIGH and SD operates as a control pin, the SQ pin operates as a pass through of SD control. SQ is an active totem-pole output.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

This device contains a two bit architecture word which, according to programming, will provide the following functions:

$\overline{G}/\overline{GS}$ Asynchronous/Synchronous Output Enable
With the architecture word unprogrammed this pin operates as an Asynchronous Output Enable ($\overline{G}$) and provides direct control of the DQ output three-state drivers independent of PK. With proper programming of the architecture word this pin will function as a Synchronous Output Enable ($\overline{GS}$) which will control the state of the DQ output three-state drivers in conjunction with PK. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such must be synchronized with the data.

$\overline{I}/\overline{IS}$ Asynchronous/Synchronous Initialize
With the architecture word unprogrammed this pin functions as an Asynchronous Initialize ($\overline{I}$) which is a control pin used to initialize the output data registers from a programmable word independent of PK. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed this pin will function as a Synchronous Initialize ($\overline{IS}$) which will initialize the output data registers from a programmable word in conjunction with PK. This can be used for a system interrupt or reset which must be synchronized with PK.

2

MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DK. M (MODE) and SD determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PK. M (MODE) selects whether the data source is the PROM Array or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DK and loaded into the pipeline register from the data input via PK as long as no set up or hold times are violated.

Inputs					Outputs			Operation
SD	M	DK	PK	$\overline{IS}$*	SQ	Shadow Register	Pipeline Register	
X	L	↑	–	X	S_3	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SD$	NA	Serial Shift; $SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$
X	L	–	↑	H	S_3	NA	$Q_n \leftarrow$ ARRAY DATA	Normal Load Pipeline Register from PROM
X	L	–	↑	L	S_3	NA	$Q_n \leftarrow$ INIT DATA	Synchronous Initialize Pipeline Register*
L	H	↑	–	X	SD	$S_n \leftarrow Q_n$	NA	Load Shadow Register from Outputs ($DQ_0 - DQ_3$)
X	H	–	↑	X	SD	NA	$Q_n \leftarrow S_n$	Load Pipeline Register from Shadow Register
H	H	↑	–	X	SD	Hold	NA	No-Op; Hold Shadow Register

FUNCTION TABLE DEFINITIONS

INPUTS

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

OUTPUTS

SQ = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

APPLICATIONS

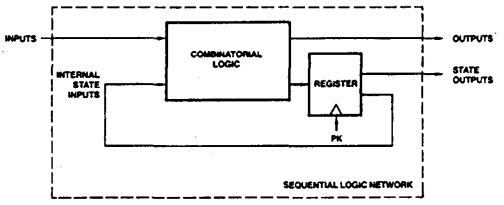
APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals — address, data, control, and status — to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.



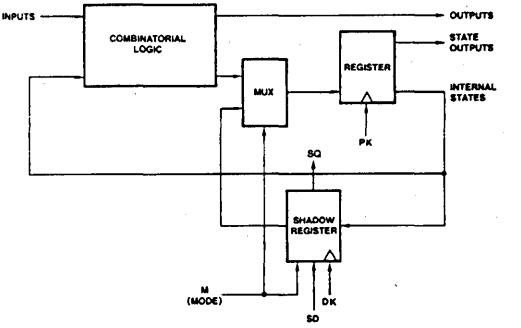
AF000181

Figure 1.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.



AF000191

Figure 2.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Votage ..... −55 to +125°C
Supply Voltage ..... −0.5 V to 7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... 0.5 to V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... 0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperatures ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperatures ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

Military products 100% tested at −55°C, 25°C, 125°C

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{IH}	Input Level (HIGH)	Guaranteed Input HIGH Voltage (See Note 1)			2.0		Volts
V_{IL}	Input Level (LOW)	Guaranteed Input LOW Voltage (See Note 1)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
V_{OH}	Output Voltage (HIGH)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} (DQ_0 − DQ_3) = −2 mA		2.4		Volts
			I_{OH} (SQ) = −0.5 mA				
V_{OL}	Output Voltage (LOW)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} (DQ_0 − DQ_3) = 24 mA			0.5	Volts
			MIL I_{OL} (DQ_0 − DQ_3) = 18 mA				
			I_{OL} (SQ) = 4 mA				
I_{IH}	Input Current (HIGH)	V_{CC} = Max.	V_{IN} = 2.7 V			25	µA
			V_{IN} = 5.5 V			40	
I_{IL}	Input Current (LOW)	V_{CC} = Max., V_{IN} = 0.4 V				−250	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0 V (Note 2)	DQ_0 − DQ_3		−20	−90	mA
			SQ		−10	−85	
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}}$ = 2.4 V	V_{OUT} = V_{CC}			50	µA
			V_{OUT} = 0.4 V			−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All Inputs = 0 V (Note 3)	COM'L	T_A = 75°C		150	mA
				T_A = 25°C		160	
				T_A = 0°C		165	
			MIL	T_C = 125°C		145	mA
				T_C = 25°C		165	
				T_C = −55°C		175	

Notes: 1. There are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. **Do Not** attempt to test these values without suitable equipment and fixturing (See Notes on Testing).
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. I_{CC} limits at temperature extremes are guaranteed by correlation to 25°C test limits.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25°C	5	pF
C_{OUT}	Output Capacitance	V_{IN}/V_{OUT} = 2.0 V@ f = 1 MHz	12	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

*See last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1.) *

No.	Parameter Symbol	Parameter Description	"A" Versions COM'L Min.	"A" Versions COM'L Max.	"A" Versions MIL Min.	"A" Versions MIL Max.	Standard Versions COM'L Min.	Standard Versions COM'L Max.	Standard Versions MIL Min.	Standard Versions MIL Max.	Units
1	TAVPKH	Address to PK (HIGH) Setup Time	23		27		30		35		ns
2	TPKHAX	Address to PK (HIGH) Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 7)	4	10	4	13	4	15	4	20	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)		22		25		25		30	
6	TGHDQZ	Asynchronous Output Enable HIGH to Output HIGH-Z (See Notes 2 & 3)		17		22		20		25	
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (See Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (See Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PKGHIGH to Output Valid, for initially High-Z outputs (See Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH tou Output High-Z (See Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (See Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (See Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Hold Time (See Note 6)	5		5		5		5		ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A, B, &C.
2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH – 0.5 V and Steady State LOW + 0.5 V output levels using the test load in C.
3. Applies only if the architecture is configured for Asynchronous $\overline{Enable}$.
4. Applies only if the architecture word has been programmed for a Synchronous $\overline{Enable}$ input.
5. Applies only if the architecture word has been programmed for a Asynchronous $\overline{Initialize}$ input.
6. Applies only if the architecture word has been programmed for a Synchronous $\overline{Initialize}$ input.
7. Minimum Delay times are guaranteed by design and supported by characterization data.

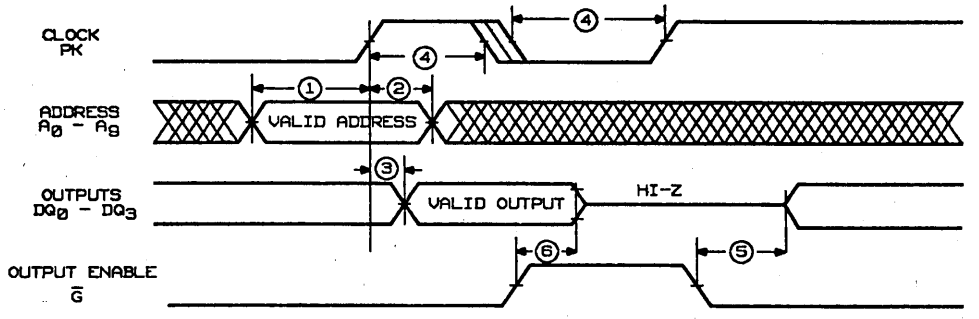
DIAGNOSTIC MODE SWITCHING CHARACTERISTICS over operating range unless other specified (See Note 1.)*

No.	Parameter Symbol	Parameter Description	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHSDX	Serial Data In to DK HIGH Hold Time	0		0		
18	TMVPKH	Mode to PK HIGH Setup Time	35		40		
19	TPKHMX	Mode to PK HIGH Hold Time	0		0		
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		
21	TDKHMX	Mode to DK HIGH Hold Time	0		0		
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		
23	TDKHDQX	Output Data In to DK HIGH Hold Time	0		0		
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)	25		25		
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	

See also A-C TEST LOADS

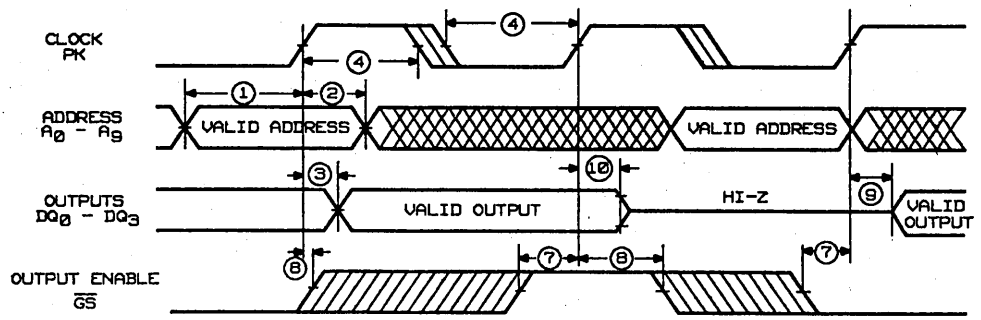
*See last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



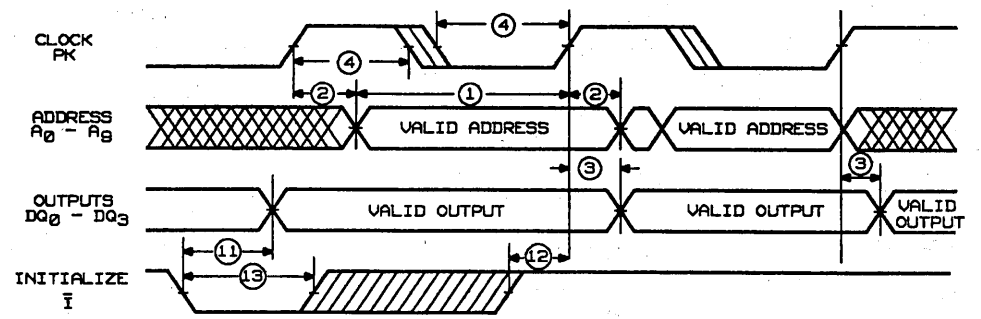
WF020650

Timing Set 1—Using Asynchronous Enable



WF020660

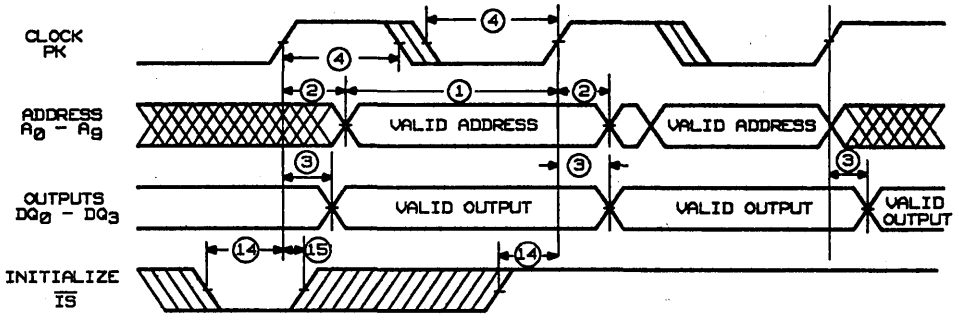
Time Set 2—Using Synchronous Enable



WF020670

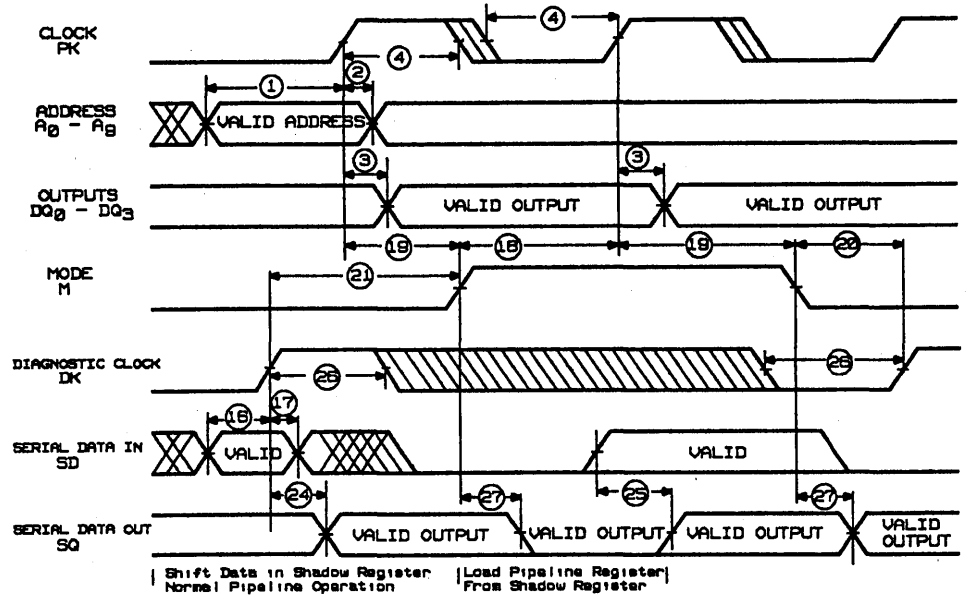
Timing Set 3—Using Asynchronous Initialize

SWITCHING WAVEFORMS (Cont.)



WF020680

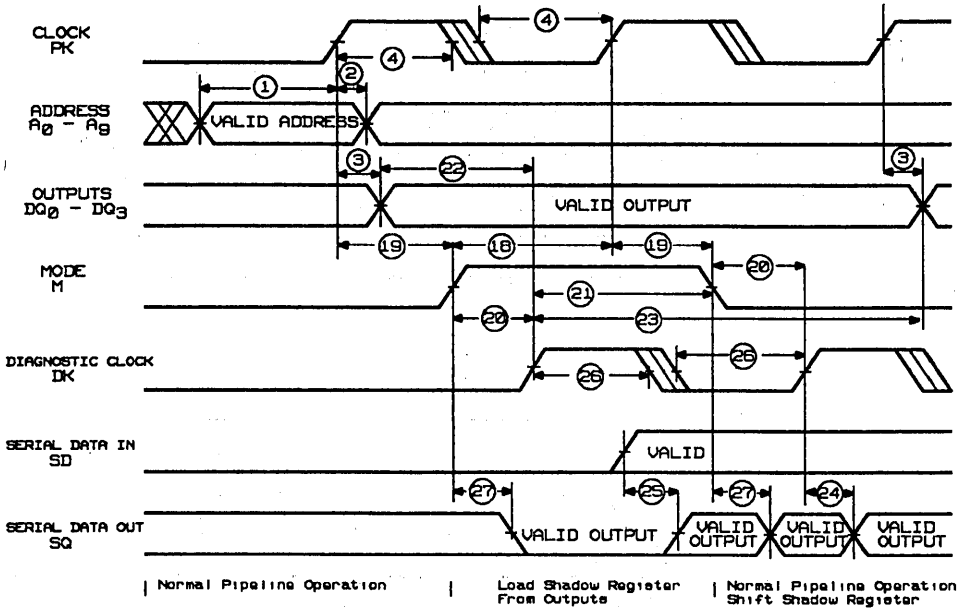
Timing Set 4—Using Synchronous Initialize



WF020690

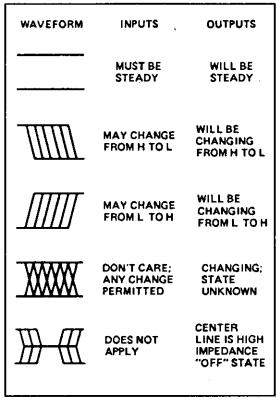
Timing Set 5—Diagnostic Test Mode (System Control)

SWITCHING WAVEFORMS (Cont.)



Timing Set 6—Doagnostic Test Mode (System Observation)

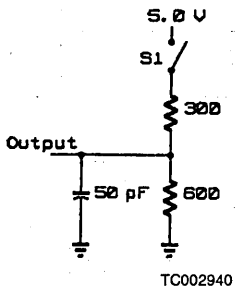
KEY TO SWITCHING WAVEFORMS



KS000010

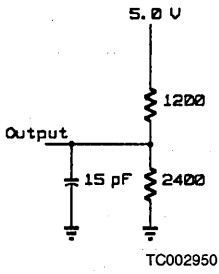
2

A-C TEST LOADS



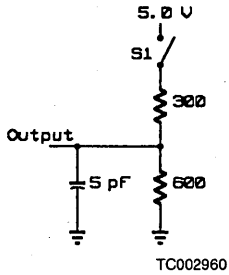
TC002940

A. Output load for $DQ_0 - DQ_3$



TC002950

B. Output load for SQ



TC002960

C. Output load for TGHDQZ and TPKHDQZ on Outputs $DQ_0 - DQ_3$

Notes: 1. All device test loads should be loaded within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all the AC tests.
3. Load capacitance includes all stray and fixture capacitance.

NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful:

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{SC}	1, 2, 3
I_{CEX}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVPKH	9, 10, 11	16	TSDVDKH	9, 10, 11
2	TPKHAX	9, 10, 11	17	TDKHSDX	9, 10, 11
3	TPKHDQV1	9, 10, 11	18	TMVPKH	9, 10, 11
4	TPKHPKL	9, 10, 11	19	TPKHMX	9, 10, 11
4	TPKLPKH	9, 10, 11	20	TMVDKH	9, 10, 11
5	TGLDQV	9, 10, 11	21	TDKHMX	9, 10, 11
6	TGHDQZ	9, 10, 11	22	TDQVDKH	9, 10, 11
7	TGSVPKH	9, 10, 11	23	TDKHDQX	9, 10, 11
8	TPKHGSX	9, 10, 11	24	TDKHSQV	9, 10, 11
9	TPKHDQV2	9, 10, 11	25	TSDVSQV	9, 10, 11
10	TILDQV	9, 10, 11	26	TDKHDKL	9, 10, 11
11	TILDQV	9, 10, 11	26	TDKLDKH	9, 10, 11
12	TIHPKH	9, 10, 11	27	TMHSQV	9, 10, 11
13	TILIH	9, 10, 11	27	TMLSQV	9, 10, 11
14	TISVPKH	9, 10, 11		Functional Tests	7, 8
15	TPKHISX	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S75

8192-Bit (2048 x 4) Bipolar Registered PROM
with SSR™ Diagnostics Capability

DISTINCTIVE CHARACTERISTICS

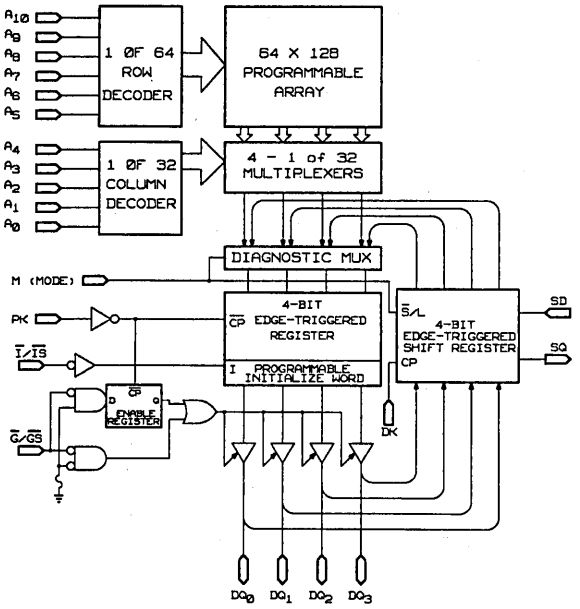
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable synchronous and asynchronous Enables
- User-programmable for synchronous or asynchronous Initialize
- Slim, 24-pin, 300-mil lateral center package permits a reduction in board space over standard discrete PROM and registers.
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability.
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%).
- Increased drive capability, 24 mA I_{OL}

GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains user programmable architecture for Enable and Initialize. The unprogrammed state of these pins operates as Asynchronous inputs ($\overline{G}$) and ($\overline{I}$) respectively. An architecture word permits the programming of the functionality of these pins to Synchronous Enable ($\overline{GS}$) and Synchronous Initialize ($\overline{IS}$).

BLOCK DIAGRAM



BD005840

SSR is a trademark of Advanced Micro Devices, Inc.

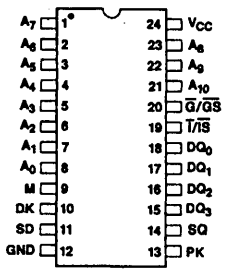
Publication # 05272 | Rev. C | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

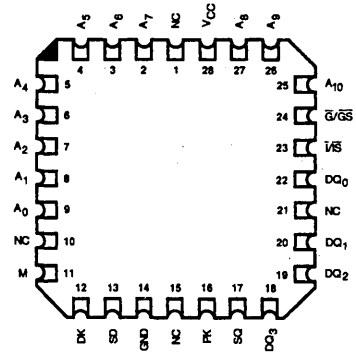
Part Number	27S75A	27S75	27S75A	27S75
Address Set up Time	25 ns	30 ns	30 ns	35 ns
Clock-to-Output Delay	12 ns	15 ns	17 ns	20 ns
Operating Range	C	C	M	M

CONNECTION DIAGRAMS

Top View



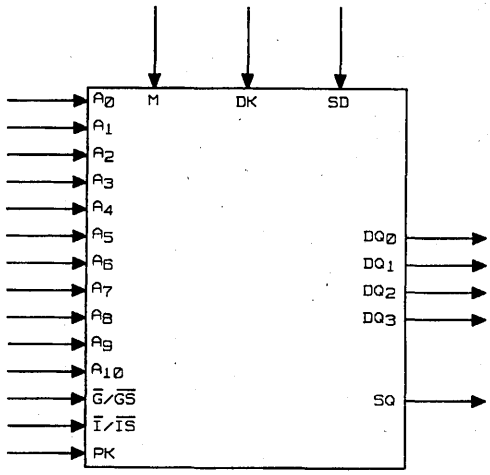
CD000552



CD004903

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

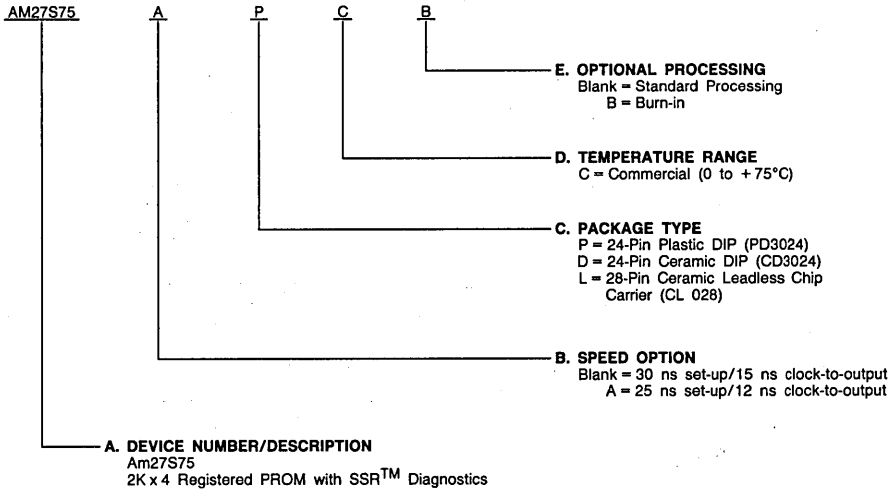


LS002110

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S75	PC, PCB, DC
AM27S75A	DCB, LC, LCB

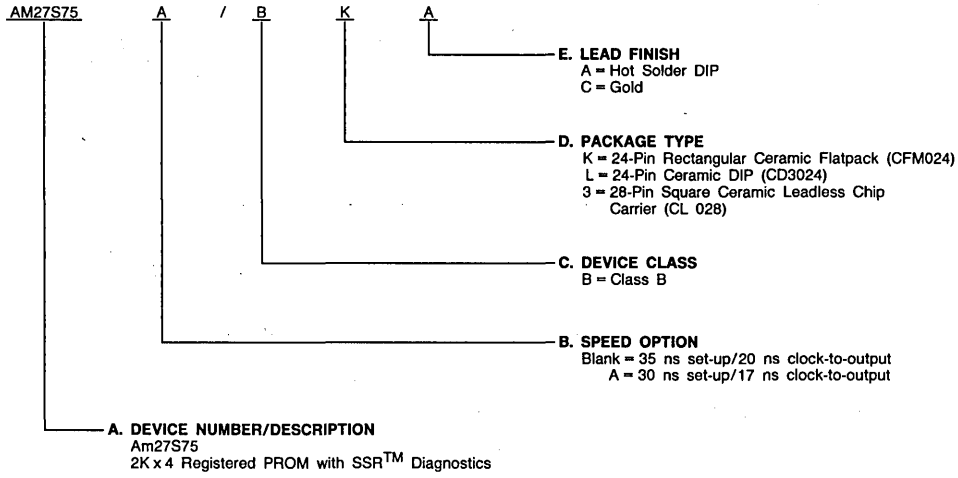
Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S75	/BKA, /BLA, /B3C
AM27S75A	

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{10}$ Address Inputs
The 11-bit field presented at the address inputs selects one of 2048 memory locatios to be read from.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the parallel registers. The data source may be the memory array, the shadow register, or the initialize word if programmed for synchronous initialize word if programmed for synchronous initialize architecture. Transfer occurs on the LOW-to-HIGH transition of PK.

$DQ_0 - DQ_3$ Data I/O Port
Parallel data output from the pipeline register or parallel data input to the shadow register.

M Mode (Input)
Control input which controls the source data for both sets of registers. MODE input is LOW in the normal mode of operation. The PROM array is the input source for the output data registers. The shadow register is in the shift mode ($SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output register or output data bus information may be loaded into the shadow register.

DK Diagnostic Clock (Input)
The diagnostic clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DK.

SD Serial Data Input
This pin performs two functions depending on the state of the MODE input. If M is LOW, the SD pin is the data transfer pin for serial data ($SD \rightarrow S_0$). If the M input is HIGH, the SD pin operates as a control pin where SD asserted LOW permits output data to be loaded into the shadow register on the next LOW-toHIGH transition of DK. SD asserted HIGH represents a NO-OP function on this device.

SQ Serial Data Output
This pin operates as a transfer pin for serial data. When M input is LOW, $SQ = S_3$. When M is HIGH and SD operates as a control pin, the SQ pin operates as a pass through of SD control. SQ is an active totem-pole output.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

This device contains a two bit architecture word which, according to programming, will provide the following functions:

$\overline{G}/\overline{GS}$ Asynchronous/Synchronous Output Enable
With the architecture word unprogrammed this pin operates as an Asynchronous Output Enable ($\overline{G}$) and provides direct control of the DQ output three-state drivers independent of PK. With proper programming of the architecture word this pin will function as a Synchronous Output Enable ($\overline{GS}$) which will control the state of the DQ output three-state drivers in conjunction with PK. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

$\overline{I}/\overline{IS}$ Asynchronous/Synchronous Initialize
With the architecture word unprogrammed this pin functions as an Asynchronous Initialize ($\overline{I}$) which is a control pin used to initialize the output data registers from a programmable word independent of PK. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed this pin will function as a Synchronous Initialize ($\overline{IS}$) which will initialize the output data registers from a programmable word in conjunction with PK. This can be used for a system interrupt or reset which must be synchronized with PK.

MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DK. M (MODE) and SD determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PK. M (MODE) selects whether the data source is the PROM Array or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DK and loaded into the pipeline register from the data input via PK as long as no set up or hold times are violated.

Inputs					Outputs			
SD	M	DK	PK	$\overline{IS}$*	SQ	Shadow Register	Pipeline Register	Operation
X	L	↑	–	X	S_3	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SD$	NA	Serial Shift; $SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$
X	L	–	↑	H	S_3	NA	$Q_n \leftarrow$ ARRAY DATA	Normal Load Pipeline Register from PROM
X	L	–	↑	L	S_3	NA	$Q_n \leftarrow$ INIT DATA	Synchronous Initialize Pipeline Register*
L	H	↑	–	X	SD	$S_n \leftarrow Q_n$	NA	Load Shadow Register from Outputs ($DQ_0 - DQ_3$)
X	H	–	↑	X	SD	NA	$Q_n \leftarrow S_n$	Load Pipeline Register from Shadow Register
H	H	↑	–	X	SD	Hold	NA	No-Op; Hold Shadow Register

MODE SELECT TABLE DEFINITIONS

INPUTS

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

OUTPUTS

SQ = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

APPLICATIONS

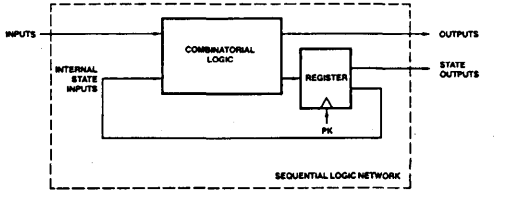
APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control, and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.



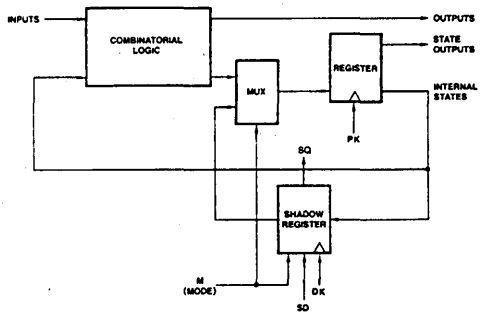
AF000181

Figure 1.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.



AF000191

Figure 2.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temparature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 to V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

Military Product 100% tested at −55°C, 25°C, 125°C

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
V_{IH}	Input Voltage HIGH	Guarantee Input HIGH Voltage (Note 1)			2.0		Volts
V_{IL}	Input Voltage LOW	Guarantee Input LOW Voltage (Note 1)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
V_{OH}	Output Voltage (HIGH)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} (DQ_0 − DQ_3) = −2 mA		2.4		Volts
			I_{OH} (SQ) = −0.5 mA				
V_{OL}	Output Voltage (LOW)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} (DQ_0 − DQ_3) = 24 mA			0.5	Volts
			MIL I_{OL} (DQ_0 − DQ_3) = 18 mA				
			I_{OL} (SQ) = 4 mA				
I_{IH}	Input Current (HIGH)	V_{CC} = Max.	V_{IN} = 2.7 V			25	µA
			V_{IN} = 5.5 V			40	
I_{IL}	Input Current (LOW)	V_{CC} = Max., V_{IN} = 0.40 V				−250	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0 V (Note 2)	DQ_0 − DQ_3		−20	−90	mA
			SQ		−10	−85	
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{CS}/\overline{GS}$ = 2.4 V (Note 3)	V_{OUT} = V_{CC}			50	mA
			V_{OUT} = 0.4 V			−150	
I_{CC}	Power Supply Current	V_{CC} = Max., All Inputs = 0.0 V (Note 4)	COM'L	T_A = 0°C		175	mA
				T_A = 25°C		170	
				T_A = 75°C		160	
			MIL	T_C = −55°C		185	
				T_C = 25°C		175	
				T_C = 125°C		150	

Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. I_{CC} limits at temperature extremes are guaranteed by correlation to 25°C test limits.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25°C V_{IN}/V_{OUT} = 2.0 V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		12	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

*See last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1.)*

No.	Parameter Symbol	Parameter Description	"A" Versions				Standard Versions				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVPKH	Address to PK HIGH Setup Time	25		30		30		35		ns
2	TPKHAX	Address to PK HIGH Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH) or LOW) (Note 7)	4	12	4	17	4	15	4	20	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)		22		25		25		30	ns
6	TGHDQZ	Asynchronous Output Enable HIGH to Output High Z (See Note 2 & 3)		17		22		20		25	ns
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (See Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (See Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PK HIGH to Output Valid, for initially High Z outputs (See Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH to Output High Z (See Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (See Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (See Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	5		5		5		5		ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A & B.
2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH −0.5 V and Steady State LOW +0.5 V output levels, using the test load in C.
3. Applies only if the architecture is configured for Asynchronous $\overline{Enable}$.
4. Applies only if the architecture word has been programmed for a Synchronous $\overline{Enable}$ input.
5. Applies only if the architecture word has been programmed for a Asynchronous $\overline{Initialize}$ input.
6. Applies only if the architecture word has been programmed for a Synchronous $\overline{Initialize}$ input.
7. Minimum Delay times are guaranteed by design and supported by characterization data.

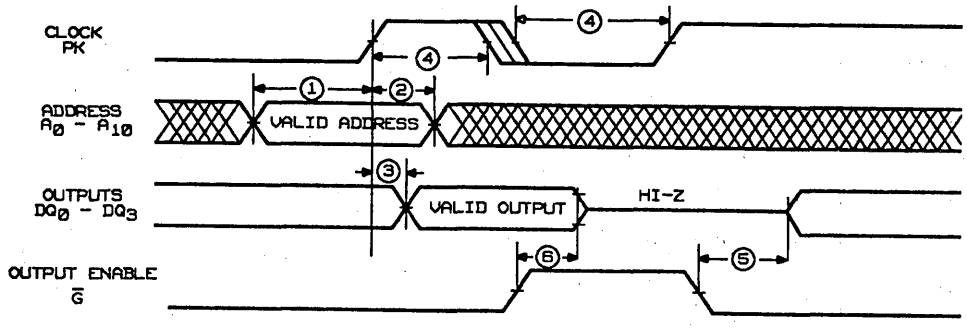
DIAGNOSTIC MODE SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1)*

No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHSDX	Serial Data In to DK HIGH Hold Time	0		0		
18	TMVPKH	Mode to PK HIGH Setup Time	35		40		
19	TPKHMX	Mode to PK HIGH Hold Time	0		0		
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		
21	TDKHMX	Mode to DK HIGH Hold Time	0		0		
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		
23	TDKHDQX	Output Data In to DK HIGH Hold Time	0		0		
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)	25		25		
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	

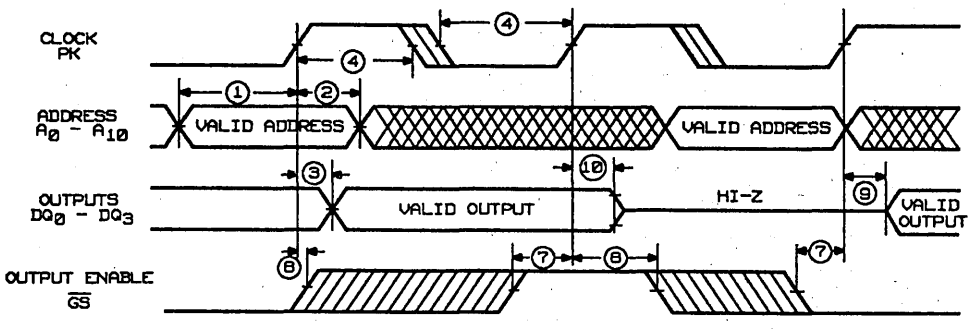
See also A-C TEST LOADS.

*See last page of this spec for Group A Subgroup Testing information.

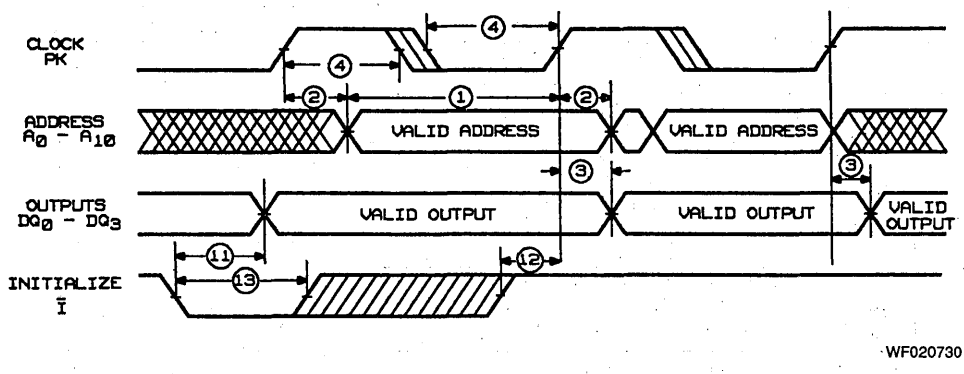
SWITCHING WAVEFORMS



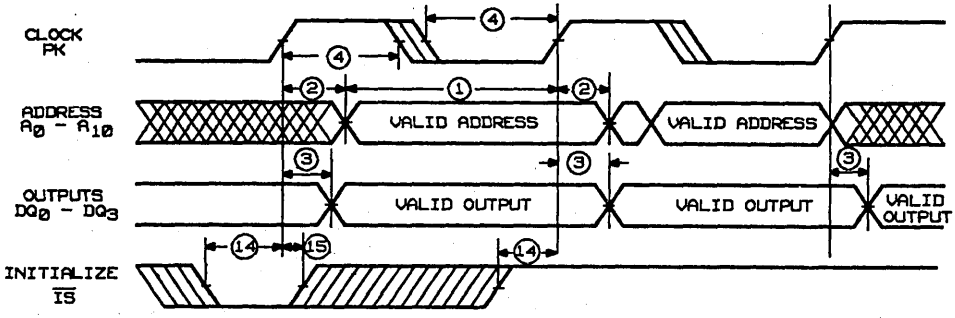
Timing Set 1 – Using Asynchronous Enable



Timing Set 2 – Using Synchronous Enable

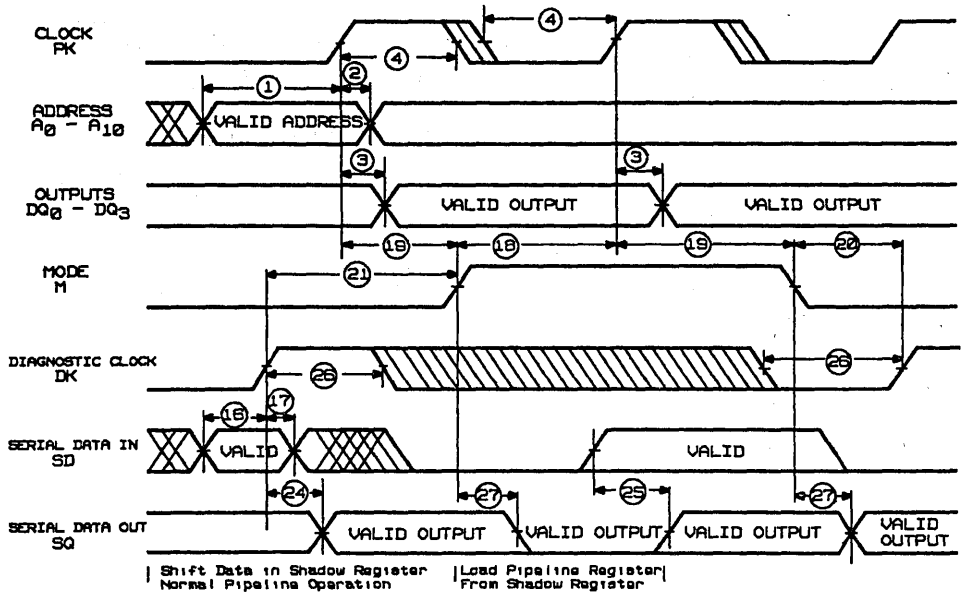


Timing Set 3 – Using Asynchronous Initialize



WF020740

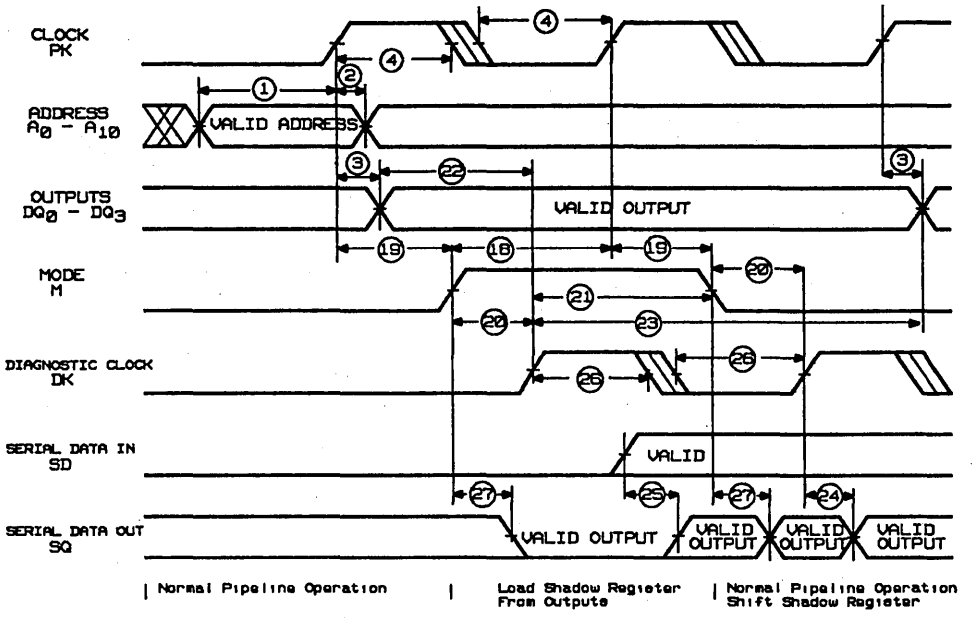
Timing Set 4 – Using Synchronous Initialize



WF020750

Timing Set 5 – Diagnostic Test Mode (System Control)

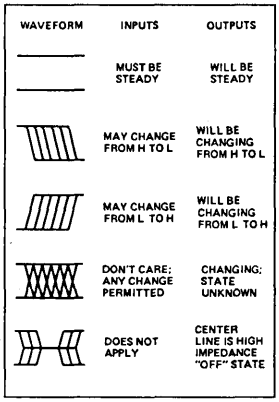
SWITCHING WAVEFORMS (Cont.)



WF020760

Timing Set 6 – Diagnostic Test Mode (System Observation)

KEY TO SWITCHING WAVEFORMS

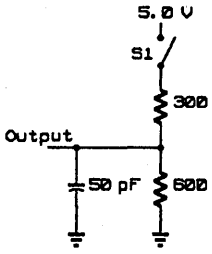


KS000010

2

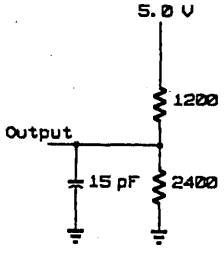
A-C TEST LOADS

A. Output Load for $DQ_0 - DQ_3$



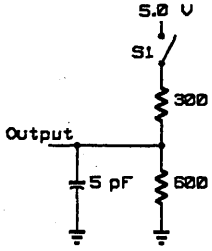
TC002910

B. Output Load for SQ



TC002920

C. Output Load for TGHDQZ and TPKHDQZ on Outputs $DQ_0 - DQ_3$



TC002930

Notes: 1. All devices test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{SC}	1, 2, 3
I_{CEX}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVPKH	9, 10, 11	16	TSDVDKH	9, 10, 11
2	TPKHAX	9, 10, 11	17	TDKHSDX	9, 10, 11
3	TPKHDQV1	9, 10, 11	18	TMVPKH	9, 10, 11
4	TPKHPKL	9, 10, 11	19	TPKHMX	9, 10, 11
4	TPKLPKH	9, 10, 11	20	TMVDKH	9, 10, 11
5	TGLDQV	9, 10, 11	21	TDKHMX	9, 10, 11
6	TGHDQZ	9, 10, 11	22	TDQVDKH	9, 10, 11
7	TGSVPKH	9, 10, 11	23	TDKHDQX	9, 10, 11
8	TPKHGSX	9, 10, 11	24	TDKHSQV	9, 10, 11
9	TPKHDQV2	9, 10, 11	25	TSDVSQV	9, 10, 11
10	TPKHDQZ	9, 10, 11	26	TDKHDKL	9, 10, 11
11	TILDQV	9, 10, 11	26	TDKLDKH	9, 10, 11
12	TIHPKH	9, 10, 11	27	TMHSQV	9, 10, 11
13	TILIH	9, 10, 11	27	TMLSQV	9, 10, 11
14	TISVPKH	9, 10, 11		Functional	7, 8
15	TPKHISX	9, 10, 11		Tests	

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S85

16,384-Bit (4096 x 4) Registered PROM
with SSR™ Diagnostics Capability

DISTINCTIVE CHARACTERISTICS

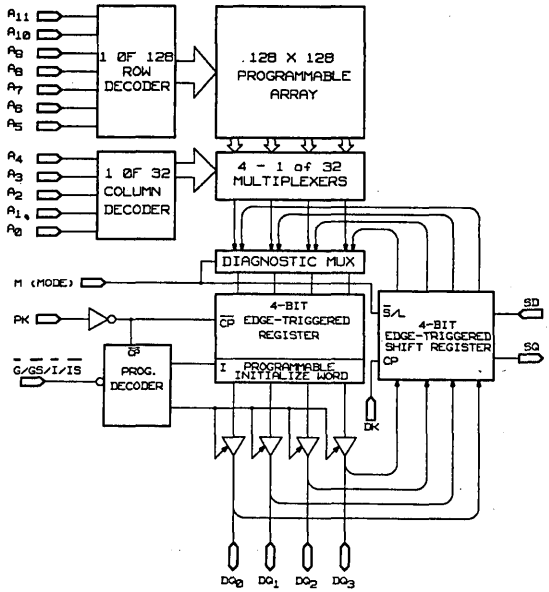
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable for Asynchronous Enable, Synchronous Enable, Asynchronous Initialize, or Synchronous Initialize
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register.
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability.
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%).
- Increased drive capability, 24 mA I_{OL}

GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains a single programmable multi-functional input ($\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$). The unprogrammed state of this pin operates an Asynchronous Enable ($\overline{G}$) input. An architecture word permits the programming of the functionality of this pin to Synchronous Enable ($\overline{GS}$), Asynchronous Initialize ($\overline{I}$), or Synchronous Initialize ($\overline{IS}$).

BLOCK DIAGRAM



BD005850

Publication #	Rev.	Amendment
05273	D	/0

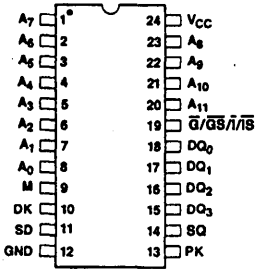
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

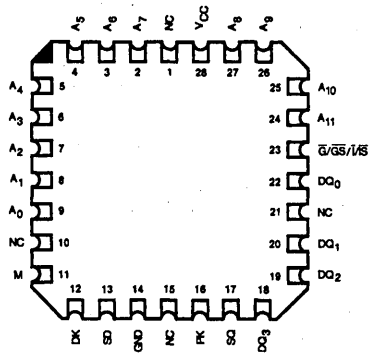
Part Number	27S85A	27S85	27S85A	27S85
Address Set-up Time	27 ns	35 ns	30 ns	40 ns
Clock-to-Output Delay	12 ns	15 ns	17 ns	20 ns
Operatinge Range	C	C	M	M

CONNECTION DIAGRAMS

Top View



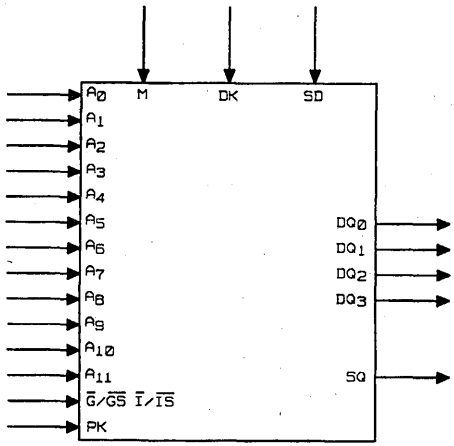
CD000561



CD004902

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

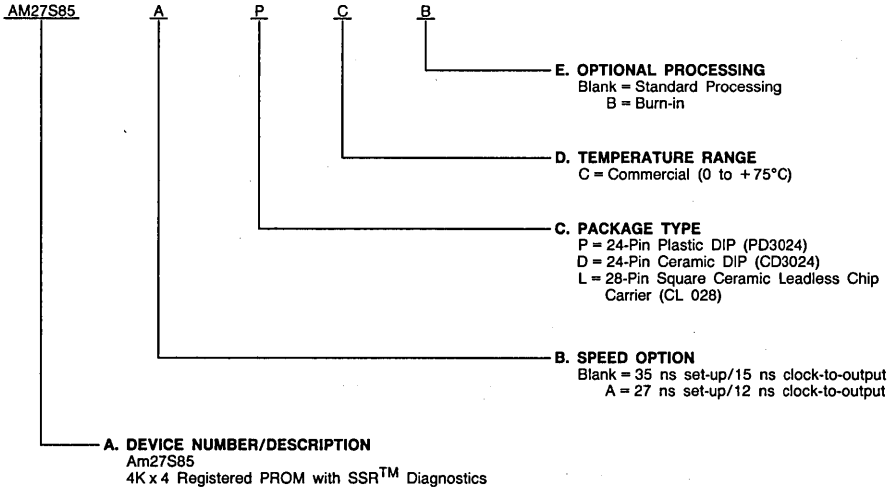


LS002111

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S85	PC, PCB, DC, DCB, LC, LCB
AM27S85A	

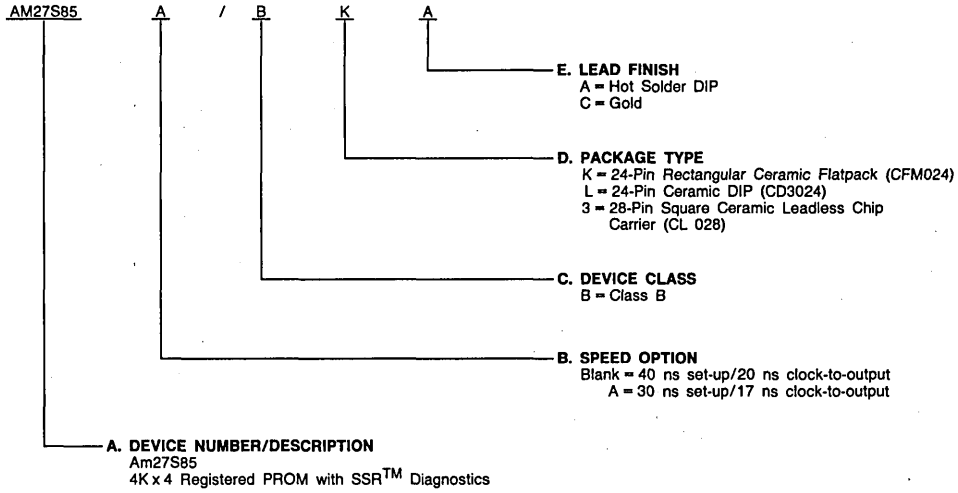
Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S85	/BKA, /BLA, /B3C
AM27S85A	

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs
The 12-bit field presented at the address inputs selects one of 4096 memory locatios to be read from.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the parallel registers. The data source may be the memory array, the shadow register, or the initialize word if programmed for synchronous initialize architecture. Transfer occurs on the LOW-to-HIGH transition of PK.

$DQ_0 - DQ_3$ Data I/O Port
Parallel data output from the pipeline register or parallel data input to the shadow register.

M Mode (Input)
Control input which controls the source data for both sets of registers. MODE inputs is LOW in the normal mode of operation. The PROM array is the input source for the output data registers. The shadow register is in the shift mode ($SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output register or output data bus information may be loaded into the shadow register.

DK Diagnostic Clock (Input)
The diagnostic clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DK.

SD Serial Data Input
This pin performs two functions depending on the state of the MODE input. If M is LOW, the SD pin is the data transfer pin for serial data ($SD \rightarrow S_0$). If the M input is HIGH, the SD pin operates as a control pin where SD asserted LOW permits output data to be loaded into the shadow register on the next LOW-toHIGH transition of DK. SD asserted HIGH represents a NO-OP function on this device.

SQ Serial Data Output
This pin operates as a transfer pin for serial data. When M input is LOW, $SQ = S_3$. When M is HIGH and SD operates as a control pin, the SQ pin operates as a pass through of SD control. SQ is an active totem-pole output.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

This device contains a two bit architecture word which, according to programming, will provide the following functions:

$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ Asynchronous/Synchronous Output Enable/ Asynchronous/Synchronous Initialize
With the architecture word unprogrammed this pin operates as an Asynchronous Output Enable ($\overline{G}$) and provides direct control of the DQ output three-state drivers independent of PK. With proper programming of the architecture word this pin will function as a Synchronous Output Enable ($\overline{GS}$) which will control the state of the DQ output three-state drivers in conjunction with PK. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The architecture word may also be programmed so that this pin will functions as an Asynchronous Initialize ($\overline{I}$) which is a control pin used to initialize the output data registers from a programmable word independent of PK. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed this pin will function as a Synchronous Initialize ($\overline{IS}$) which will initialize the output data registers from a programmable word in conjunction with PK. This can be used for a system interrupt or reset which must be synchronized with PK.

MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DK. M (MODE) and SD determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PK. M (MODE) selects whether the data source is the PROM Array or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DK and loaded into the pipeline register from the data input via PK as long as no set up or hold times are violated.

Inputs					Outputs			
SD	M	DK	PK	$\overline{IS}$*	SQ	Shadow Register	Pipeline Register	Operation
X	L	↑	–	X	S_3	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SD$	NA	Serial Shift; $SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$
X	L	–	↑	H	S_3	NA	$Q_n \leftarrow$ ARRAY DATA	Normal Load Pipeline Register from PROM
X	L	–	↑	L	S_3	NA	$Q_n \leftarrow$ INIT DATA	Synchronous Initialize Pipeline Register*
L	H	↑	–	X	SD	$S_n \leftarrow Q_n$	NA	Load Shadow Register from Outputs ($DQ_0 - DQ_3$)
X	H	–	↑	X	SD	NA	$Q_n \leftarrow S_n$	Load Pipeline Register from Shadow Register
H	H	↑	–	X	SD	Hold	NA	No-Op; Hold Shadow Register

MODE SELECT TABLE DEFINITIONS

INPUTS

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

OUTPUTS

SQ = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

APPLICATIONS

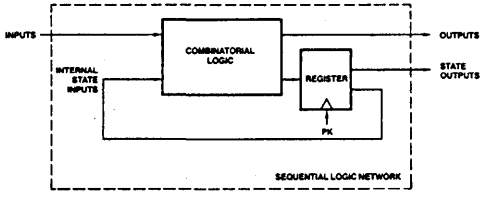
APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control, and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.



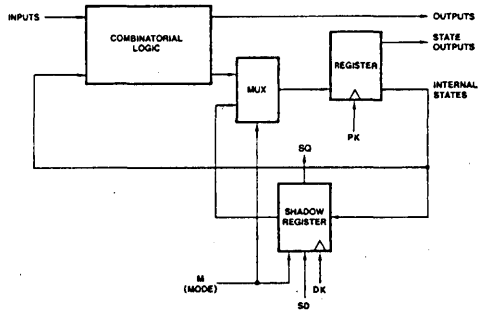
AF000181

Figure 1.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessaryl An easier method must exist. Serial Shadow Register diagnostics provides this method.

SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.



AF000191

Figure 2.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temparature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 to V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

Military product 100% tested at −55°C, 25°C and 125°C

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{IH}	Input Voltage HIGH	Guarantee Input HIGH Voltage (Note 1)		2.0		Volts
V_{IL}	Input Voltage LOW	Guarantee Input LOW Voltage (Note 1)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
V_{OH}	Output Voltage (HIGH)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} (DQ_0 − DQ_3) = −2 mA	2.4		Volts
			I_{OH} (SQ) = −0.5 mA			
V_{OL}	Output Voltage (LOW)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} (DQ_0 − DQ_3) = 24 mA		0.5	Volts
			MIL I_{OL} (DQ_0 − DQ_3) = 18 mA			
			I_{OL} (SQ) = 4 mA			
I_{IH}	Input Current (HIGH)	V_{CC} = Max.	V_{IN} = 2.7 V		25	µA
			V_{IN} = 5.5 V		40	
I_{IL}	Input Current (LOW)	V_{CC} = Max., V_{IN} = 0.40 V			−250	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0 V (Note 2)	DQ_0 − DQ_3	−20	−90	mA
			SQ	−10	−85	
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}/\overline{GS}}$ = 2.4 V (Note 3)	V_{OUT} = V_{CC}		50	mA
			V_{OUT} = 0.4 V		−150	
I_{CC}	Power Supply Current	V_{CC} = Max., All Inputs = 0.0 V (Note 4)	COM'L T_A = 0°C		185	mA
			COM'L T_A = 25°C		175	
			COM'L T_A = 75°C		165	
			MIL T_C = −55°C		195	
			MIL T_C = 25°C		180	
			MIL T_C = 125°C		155	

Notes: 1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. I_{CC} limits at temperature extremes are guaranteed by correlation to 25°C test limits.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25°C V_{IN}/V_{OUT} = 20 V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		12	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

*See last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1)*

No.	Parameter Symbol	Parameter Description	"A" Versions				Standard Versions				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVPKH	Address to PK HIGH Setup Time	27		30		35		40		ns
2	TPKHAX	Address to PK HIGH Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH) or LOW) (Note 7)	4	12	4	17	4	15	4	20	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)		22		25		25		30	ns
6	TGHDQZ	Asynchronous Output Enable HIGH to Output High Z (See Note 3)		17		22		20		25	ns
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (See Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (See Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PK HIGH to Output Valid, for initially High Z outputs (See Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH to Output High Z (See Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (See Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (See Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	5		5		5		5		ns

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A & B.
2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH −0.5 V and Steady State LOW +0.5 V output levels, using the test load in C.
3. Applies only if the architecture is configured for Asynchronous $\overline{Enable}$.
4. Applies only if the architecture word has been programmed for a Synchronous $\overline{Enable}$ input.
5. Applies only if the architecture word has been programmed for a Asynchronous $\overline{Initialize}$ input.
6. Applies only if the architecture word has been programmed for a Synchronous $\overline{Initialize}$ input.
7. Minimum Delay times are guaranteed by design and supported by characterization data.

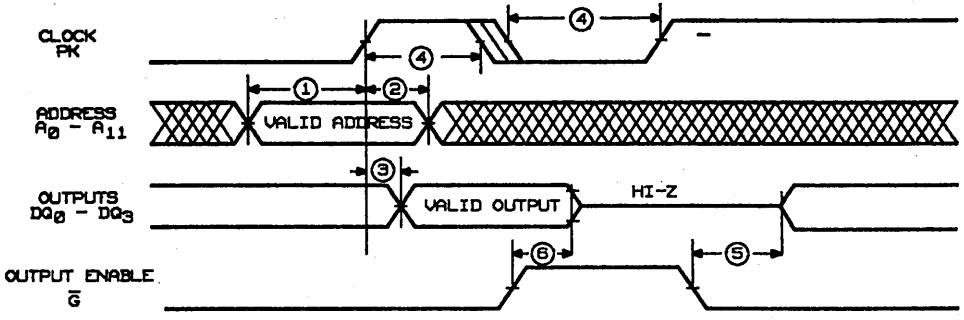
DIAGNOSTIC MODE SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1)*

No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHSDX	Serial Data In to DK HIGH Hold Time	0		0		
18	TMVPKH	Mode to PK HIGH Setup Time	35		40		
19	TPKHMX	Mode to PK HIGH Hold Time	0		0		
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		
21	TDKHMX	Mode to DK HIGH Hold Time	0		0		
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		
23	TDKHDQX	Output Data In to DK HIGH Hold Time	0		0		
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)	25		25		
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	

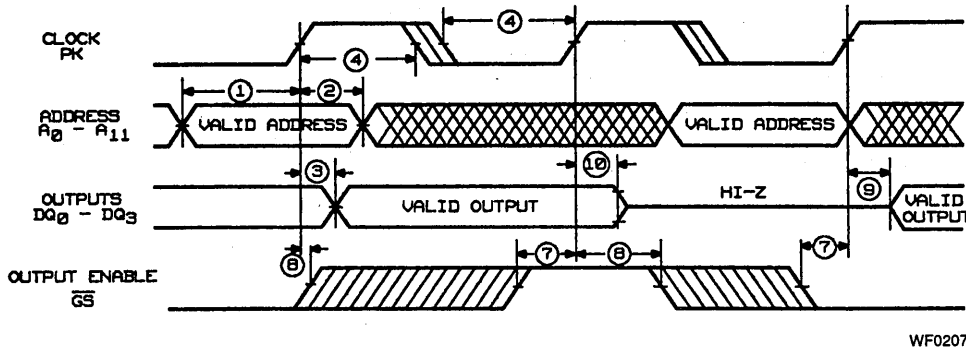
See also A-C TEST LOADS.

*See last page of this spec for Group A Subgroup Testing information.

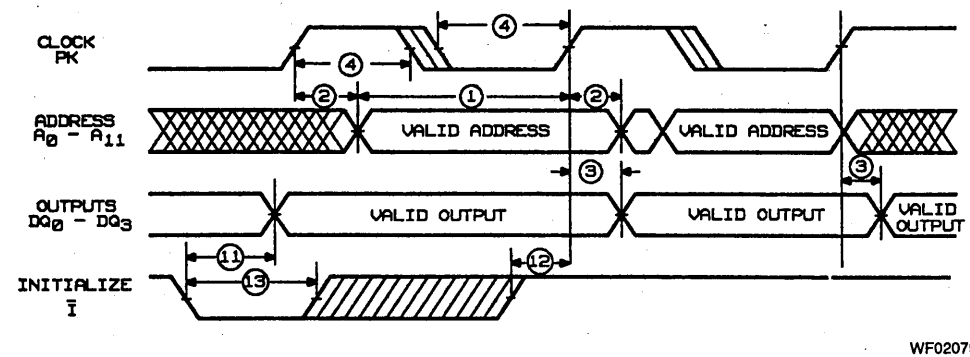
SWITCHING WAVEFORMS



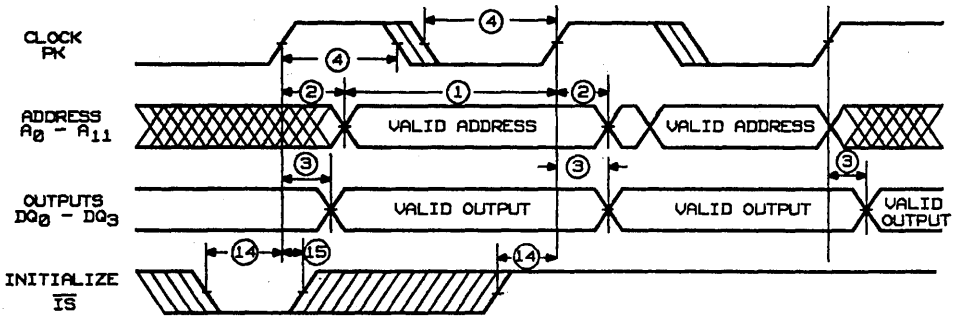
Timing Set 1 – Using Asynchronous Enable



Timing Set 2 – Using Synchronous Enable

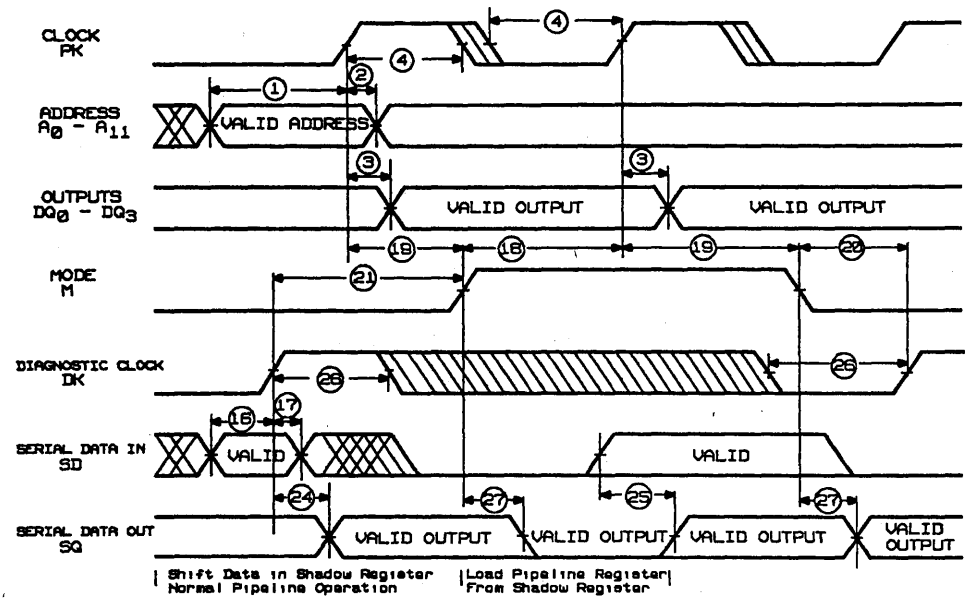


Timing Set 3 – Using Asynchronous Initialize



WF020800

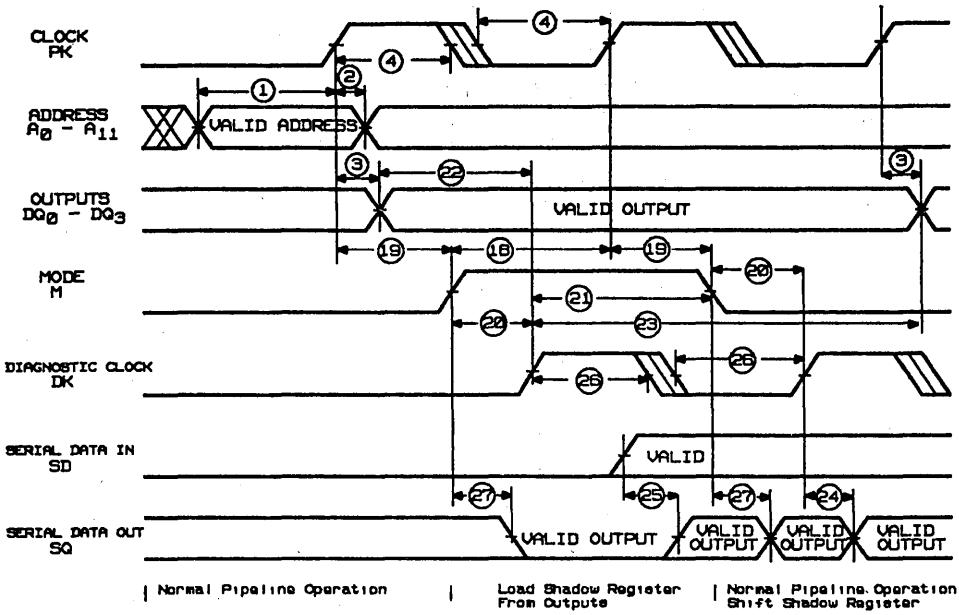
Timing Set 4 – Using Synchronous Initialize



WF020810

Timing Set 5 – Diagnostic Test Mode (System Control)

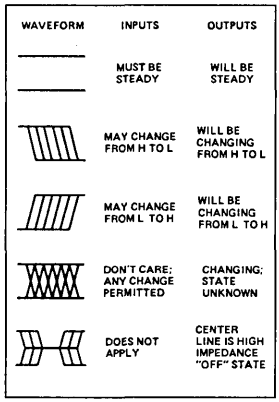
SWITCHING WAVEFORMS (Cont.)



WF020820

Timing Set 6 – Diagnostic Test Mode (System Observation)

KEY TO SWITCHING WAVEFORMS

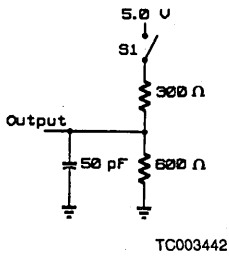


KS000010

2

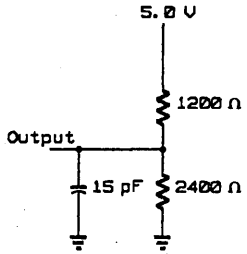
A-C TEST LOADS

A. Output Load for $DQ_0 - DQ_3$



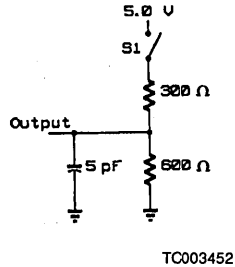
TC003442

B. Output Load for SQ



TC002951

C. Output Load for TGHDQZ and TPKHDQZ on Outputs $DQ_0 - DQ_3$



TC003452

Notes: 1. All devices test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{SC}	1, 2, 3
I_{CEX}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVPKH	9, 10, 11	16	TSDVDKH	9, 10, 11
2	TPKHAX	9, 10, 11	17	TDKHSDX	9, 10, 11
3	TPKHDQV1	9, 10, 11	18	TMVPKH	9, 10, 11
4	TPKHPKL	9, 10, 11	19	TPKHMX	9, 10, 11
4	TPKLPKH	9, 10, 11	20	TMVDKH	9, 10, 11
5	TGLDQV	9, 10, 11	21	TDKHMX	9, 10, 11
6	TGHDQZ	9, 10, 11	22	TDQVDKH	9, 10, 11
7	TGSVPKH	9, 10, 11	23	TDKHDQX	9, 10, 11
8	TPKHGSX	9, 10, 11	24	TDKHSQV	9, 10, 11
9	TPKHDQV2	9, 10, 11	25	TSDVSQV	9, 10, 11
10	TILDQV	9, 10, 11	26	TDKHDKL	9, 10, 11
11	TILDQV	9, 10, 11	26	TDKLDKH	9, 10, 11
12	TIHPKH	9, 10, 11	27	TMHSQV	9, 10, 11
13	TILIH	9, 10, 11	27	TMLSQV	9, 10, 11
14	TISVPKH	9, 10, 11		Functional Tests	7, 8
15	TPKHISX	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S95

32,768 Bit (8192 x 4) Bipolar Registered PROM
with SSR ™ Diagnostics Capability
ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

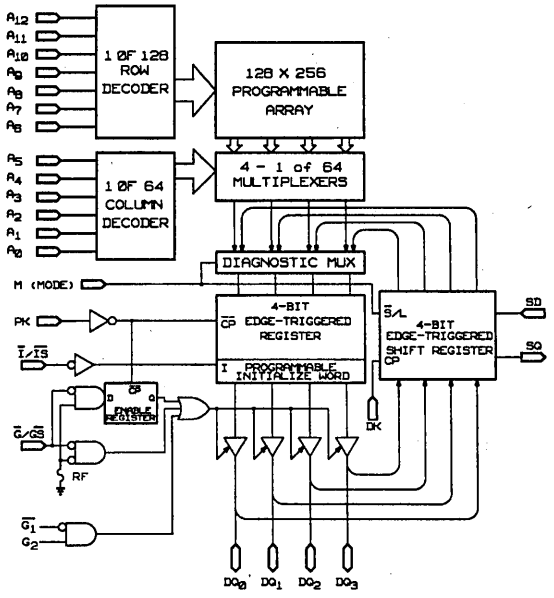
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable Enable Pin for Asynchronous or Synchronous Enable operation
- User-programmable Initialization Pin for Asynchronous or Synchronous Initialize operation
- Slim, 28-pin, 400-mil lateral center package permits a reduction in board space over standard discrete PROM and registers
- Consumes approximately ½ the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)
- Increased drive capability, 24 mA I_{OL}

GENERAL DESCRIPTION

This device contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies, the shadow register is intended to operate in the background of the normal output data register. This shadow register can be used in a systematic way to control and observe the output data register to exercise desired system functions during a diagnostic test mode.

To offer the system designer maximum flexibility, this device contains user-programmable architecture for Enable and Initialize. The unprogrammed state of these pins operates as Asynchronous inputs ($\overline{G}$) and ($\overline{I}$), respectively. An architecture word permits the programming of the functionality of these pins to Synchronous Enable ($\overline{GS}$) and Synchronous Initialize ($\overline{IS}$). Two non-programmable Asynchronous Enables ($\overline{G_1}$ and G_2) are also provided.

BLOCK DIAGRAM



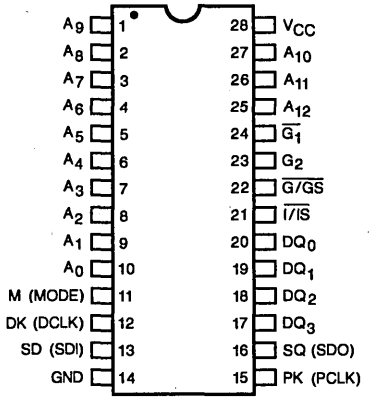
BD006520

Publication # 08129 | Rev. A | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

Part Number	27S95A	27S95
Address Set-up Time	25 ns	30 ns
Clock-to-Output Delay	10 ns	13 ns
Operating Range	C	M

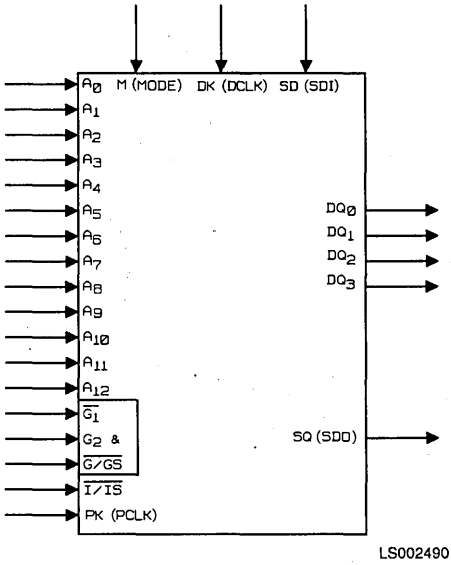
CONNECTION DIAGRAM
Top View



CD009670

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



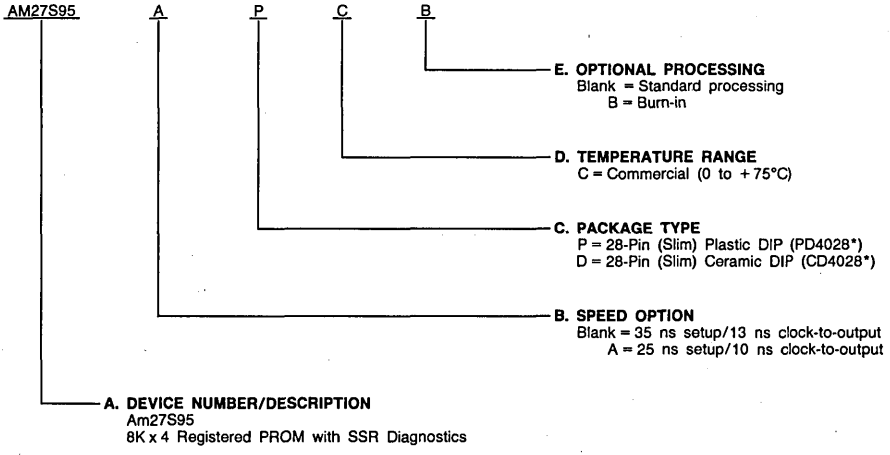
LS002490

*SSR is a trademark of Advanced Micro Devices, Inc.

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S95	PC, PCB, DC, DCB
AM27S95A	

Valid Combinations

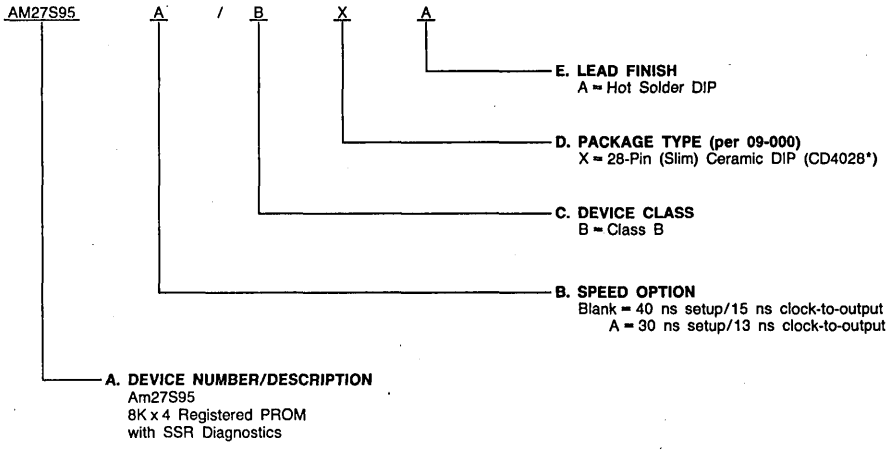
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*Preliminary. Subject to change.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S95	/BXA
AM27S95A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

*Preliminary. Subject to Change.

PIN DESCRIPTION

$IA_0 - A_{12}$ Address Inputs (Inputs)
The 13-bit field presented at the address inputs selects one of 8192 memory locations to be read from.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the parallel registers. The data source may be the memory array, the shadow register, or the initialize word if programmed for synchrounous initialize architecture. Transfer occurs on the LOW-to-HIGH transition of PK.

$DQ_0 - DQ_3$ Data I/O Port (Outputs)
Parallel data output from the pipeline register or parallel data input to the shadow register.

M Mode (Input)
Control input which controls the source data for both sets of registers, MODE input is LOW in the normal mode of operation. The PROM Array is the input source for the output data registers. The shadow register is in the shift mode ($SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output registers or output data bus information may be loaded into the shadow register.

DK Diagnostic Clock (Input)
The Diagnostic clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DK.

SQ Serial Data Input (Input)
This pin performs two functions depending on the state of the MODE input. If M is LOW, the SD pin is the data transfer pin for serial data ($SD \longrightarrow S_0$). IF the M input is HIGH, the SD pin operates as a control pin where SD asserted LOW permits output data to be loaded into the shadow register on the next LOW-to-HIGH transtion of DK. SD asserted HIGH represents a NO-OP function on this device.

SQ Serial Data Output
This pin operates as a transfer pin for serial data. When M input is LOW, $SQ = S_3$. When M is HIGH and SD operates as a control pin, the SQ pin operates as a pass through of SD control. SQ is an active totem-pole output.

$\overline{G_1}$, G_2 Asynchronous Output Enable
Provides direct control of the DQ output three-state drivers independent of PK.

This device contains a two bit architecture word which, according to programming, will provide the following functions:

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

$\overline{G}/\overline{GS}$ Asynchronous/Synchronous Output Enable
With the architecture word unprogrammed this pin operates as an Asynchronous Output Enable ($\overline{G}$) and provides direct control of the DQ output three-state drivers independent of PK. With proper programming of the architecture word this pin will function as a Synchronous Output Enable ($\overline{GS}$) which will control the state of the DQ output three-state drivers in conjunction with PK. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such must be synchronized with the data.

$\overline{I}/\overline{IS}$ Asynchronous/Synchronous Initialize
With the architecture word unprogrammed this pin functions as an Asynchronous Initialize ($\overline{I}$) which is a control pin used to initialize the output data registers from a programmable word independent of PK. This can be used to generate any arbitrary microinstruction for system interrupt or reset. When the architecture word is properly programmed this pin will function as a Synchronous Initialize ($\overline{IS}$) which will initialize the output data registers from a programmable word in conjunction with PK. This can be used for a system interrupt or reset which must be synchronized with PK.

MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DK. M (MODE) and SD determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PK. M (MODE) selects whether the data source is the PROM Array or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DK and loaded into the pipeline register from the data input via PK as long as no set up or hold times are violated.

Inputs					Outputs			Operation
SD	M	DK	PK	$\overline{IS}$*	SQ	Shadow Register	Pipeline Register	
X	L	↑	–	X	S_3	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SD$	NA	Serial Shift; $SD \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SQ$
X	L	–	↑	H	S_3	NA	$Q_n \leftarrow$ ARRAY DATA	Normal Load Pipeline Register from PROM
X	L	–	↑	L	S_3	NA	$Q_n \leftarrow$ INIT DATA	Synchronous Initialize Pipeline Register*
L	H	↑	–	X	SD	$S_n \leftarrow Q_n$	NA	Load Shadow Register from Outputs ($DQ_0 - DQ_3$)
X	H	–	↑	X	SD	NA	$Q_n \leftarrow S_n$	Load Pipeline Register from Shadow Register
H	H	↑	–	X	SD	Hold	NA	No-Op; Hold Shadow Register

FUNCTION TABLE DEFINITIONS

INPUTS

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW clock transition
↑ = LOW-to-HIGH clock transition

OUTPUTS

SQ = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

APPLICATIONS

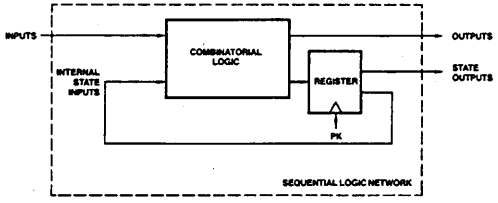
APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals — address, data, control, and status — to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.



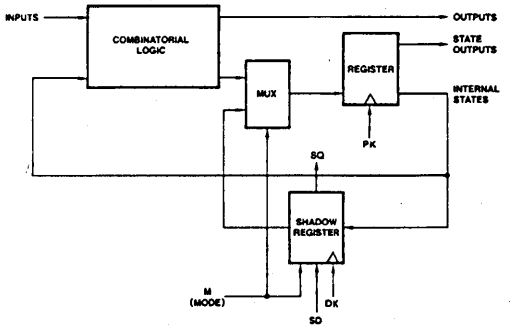
AF000181

Figure 1.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.



AF000191

Figure 2.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Voltage ..... −55 to +125°C
Supply Voltage ..... −0.5 V to 7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... 0.5 to V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec.) ..... 250 mA
DC Input Voltage ..... 0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperatures, T_A ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperatures, T_C ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{IH}	Input Level (HIGH)	Guaranteed Input HIGH Voltage (See Note 1)		2.0		Volts
V_{IL}	Input Level (LOW)	Guaranteed Input LOW Voltage (See Note 2)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
V_{OH}	Output Voltage (HIGH)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} (DQ_0 − DQ_3) = −2 mA	2.4		Volts
			I_{OH} (SQ) = −0.5 mA			
V_{OL}	Output Voltage (LOW)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} (DQ_0 − DQ_3) = 24 mA		0.5	Volts
			MIL I_{OL} (DQ_0 − DQ_3) = 18 mA			
			I_{OL} (SQ) = 4 mA			
I_{IH}	Input Current (HIGH)	V_{CC} = Max.	V_{IN} = 2.7 V		25	μA
			V_{IN} = 5.5 V		40	
I_{IL}	Input Current (LOW)	V_{CC} = Max., V_{IN} = 0.4 V			−250	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0 V (Note 2)	DQ_0 − DQ_3	−20	−90	mA
			SQ	−10	−85	
I_{CEX}	Output Leakage Current	V_{CC} = Max. $\overline{VG}$ = 2.4 V	V_{OUT} = V_{CC}		50	μA
			V_{OUT} = 0.4 V		−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All Inputs = 0 V (Note 3)	COM'L T_A = 75°C		165	mA
			COM'L T_A = 25°C		175	
			COM'L T_A = 0°C		185	
			MIL T_C = 125°C		155	mA
			MIL T_C = 25°C		180	
			MIL T_C = −55°C		195	

Notes: 1. There are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. **Do Not** attempt to test these values without suitable equipment and fixturing (See Notes on Testing).
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. I_{CC} limits at temperature extremes are guaranteed by correlation to 25°C test limits.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = 25°C	5	pF
C_{OUT}	Output Capacitance	V_{IN}/V_{OUT} = 2.0 V@ f = 1 MHz	12	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1)

No.	Parameter Symbol	Parameter Description	"A" Versions				Standard Versions				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVPKH	Address to PK (HIGH) Setup Time	25		30		35		40		ns
2	TPKHAX	Address to PK (HIGH) Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH or LOW) (Note 7)	4	10	4	13	4	13	4	15	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)		22		25		25		30	
6	TGHDQZ	Asynchronous Output Enable HIGH to Output HIGH-Z (See Notes 2 & 3)		17		22		20		25	
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (See Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (See Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PKGHIGH to Output Valid, for initially High-Z outputs (See Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH tou Output High-Z (See Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (See Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (See Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Hold Time (See Note 6)	5		5		5		5		ns

Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A, B, &C.
2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH – 0.5 V and Steady State LOW + 0.5 V output levels using the test load in C.
3. Applies only if the architecture is configured for Asynchronous $\overline{Enable}$.
4. Applies only if the architecture word has been programmed for a Synchronous $\overline{Enable}$ input.
5. Applies only if the architecture word has been programmed for a Asynchronous $\overline{Initialize}$ input.
6. Applies only if the architecture word has been programmed for a Synchronous $\overline{Initialize}$ input.
7. Minimum Delay times are guaranteed by design and supported by characterization data.

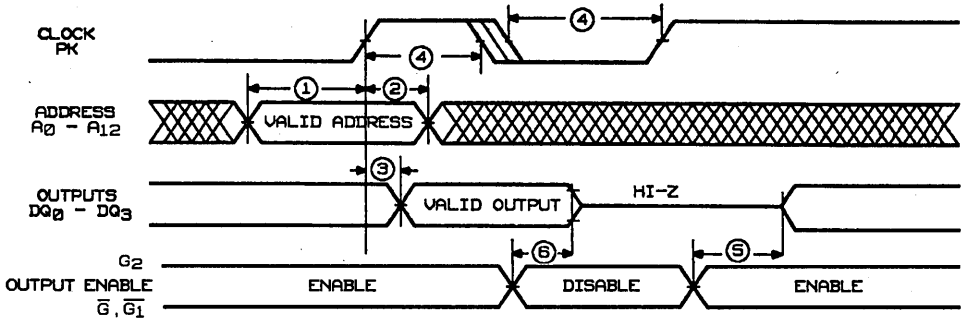
DIAGNOSTIC MODE SWITCHING CHARACTERISTICS over operating range unless other specified

(See Note 1)

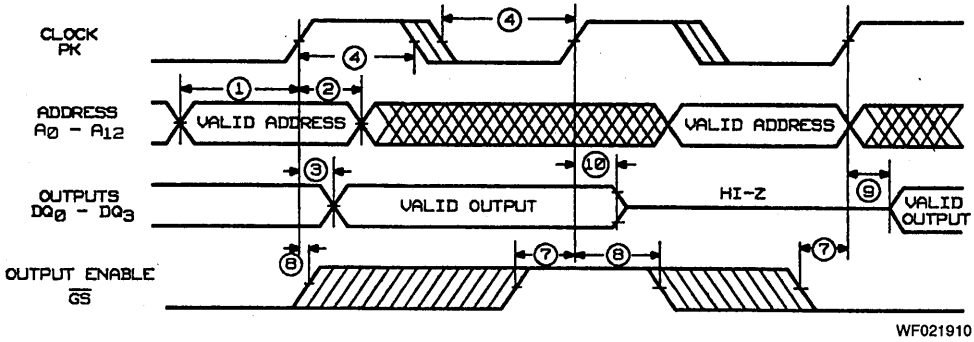
No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHSDX	Serial Data In to DK HIGH Hold Time	0		0		
18	TMVPKH	Mode to PK HIGH Setup Time	35		40		
19	TPKHMX	Mode to PK HIGH Hold Time	0		0		
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		
21	TDKHMX	Mode to DK HIGH Hold Time	0		0		
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		
23	TDKHDQX	Output Data In to DK HIGH Hold Time	0		0		
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)	25		25		
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	

See also A-C TEST LOADS

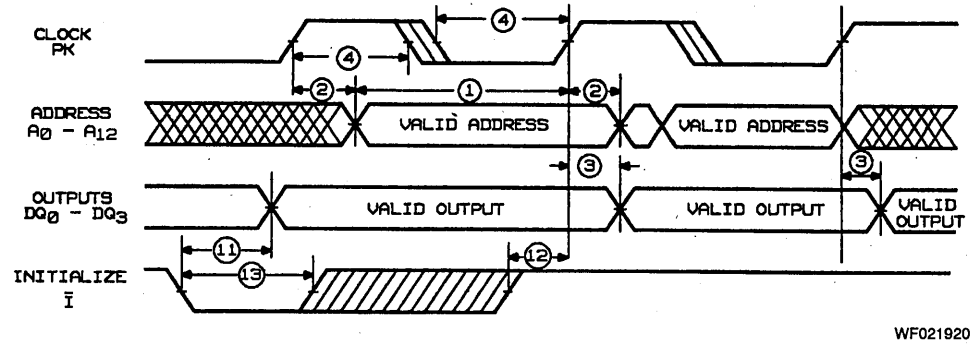
SWITCHING WAVEFORMS (Cont'd.)



Timing Set 1—Using Asynchronous Enable

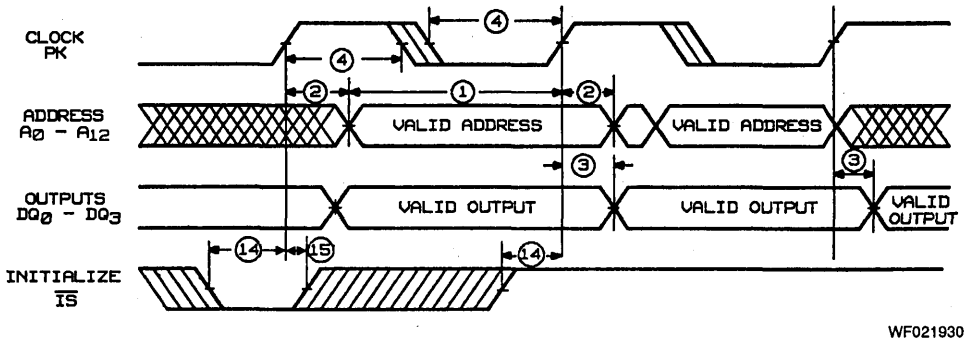


Time Set 2—Using Synchronous Enable



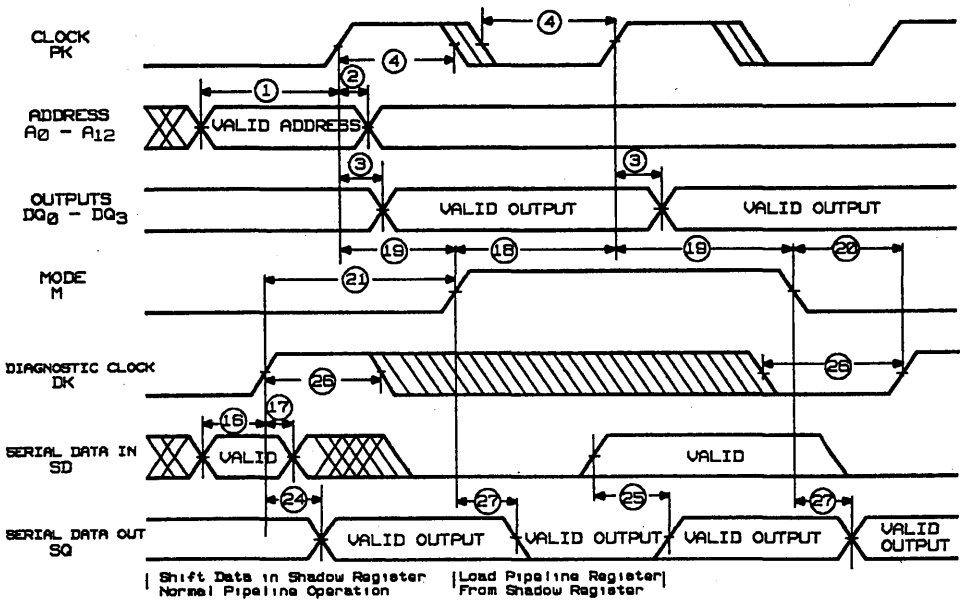
Timing Set 3—Using Asynchronous Initialize

SWITCHING WAVEFORMS (Cont'd.)



WF021930

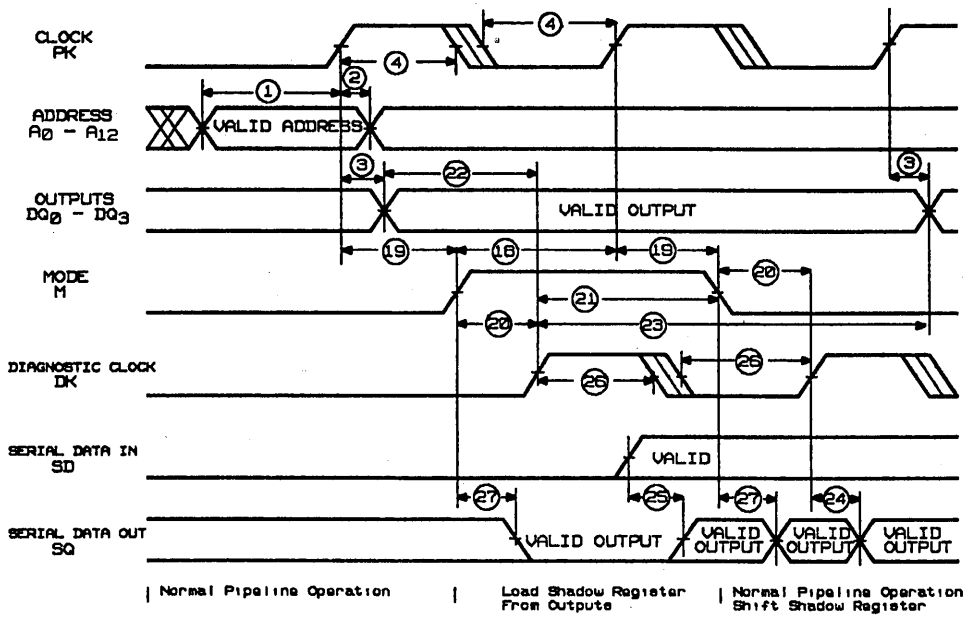
Timing Set 4—Using Synchronous Initialize



WF021940

Timing Set 5—Diagnostic Test Mode (System Control)

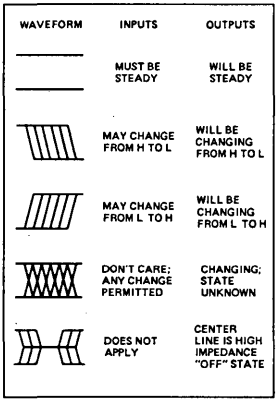
SWITCHING WAVEFORMS



WF021950

Timing Set 6—Diagnostic Test Mode (System Observation)

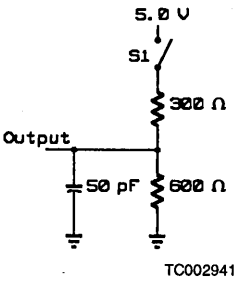
KEY TO SWITCHING WAVEFORMS



KS000010

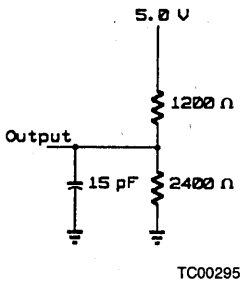
2

A-C TEST LOADS



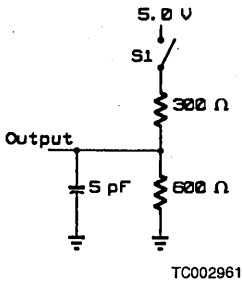
TC002941

A. Output load for all AC Tests for $DQ_0 - DQ_3$ except TGHDQZ and TPKHDQZ



TC002951

B. Output load for SQ



TC002961

C. Output load for TGHDQZ and TPKHDQZ on Outputs $DQ_0 - DQ_3$

Notes: 1. All device test loads should be loaded within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all the AC tests.
3. Load capacitance includes all stray and fixture capacitance.

NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful:

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{SC}	1, 2, 3
I_{CEX}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVPKH	9, 10, 11	16	TSDVDKH	9, 10, 11
2	TPKHAX	9, 10, 11	17	TDKHSDX	9, 10, 11
4	TPKHPKL	9, 10, 11	18	TMVPKH	9, 10, 11
4	TPKLPKH	9, 10, 11	19	TPKHMX	9, 10, 11
5	TGLDQV	9, 10, 11	20	TMVDKH	9, 10, 11
6	TGHDQZ	9, 10, 11	21	TDKHMX	9, 10, 11
7	TGSVPKH	9, 10, 11	22	TDQVDKH	9, 10, 11
8	TPKHGSX	9, 10, 11	23	TDKHDQX	9, 10, 11
9	TPKHDQV2	9, 10, 11	24	TDKHSQV	9, 10, 11
10	TPKHDQZ	9, 10, 11	25	TSDVSQV	9, 10, 11
11	TILDQV	9, 10, 11	26	TDKHDKL	9, 10, 11
12	TIHPKH	9, 10, 11	26	TDKLDKH	9, 10, 11
13	TILIH	9, 10, 11	27	TMHSQV	9, 10, 11
14	TISVPKH	9, 10, 11	27	TMLSQV	9, 10, 11
15	TPKHISX	9, 10, 11		Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Bipolar Random-Access Memories (RAM) Index

Am100415

1024 x 1 IMOX™ II ECL Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fast access time (8 ns typ.) — improves system cycle speeds
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

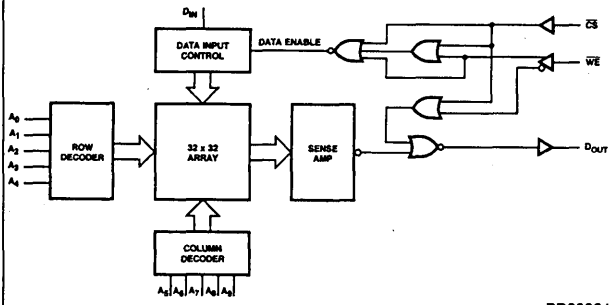
The Am100415 is a fully decoded 1024-bit ECL RAM organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and an unterminated OR-tieable emitter follower output.

An active-LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000640

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH = −0.9 V
L = LOW = −1.7 V
X = Don't Care

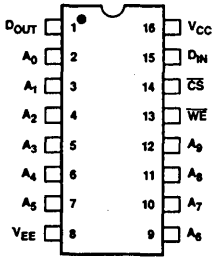
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

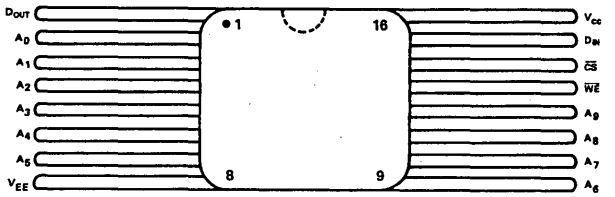
Part Number	Am100415-10	Am100415A	Am100415
Address Access Time (t_{AA})	10 ns	15 ns	20 ns
Write Pulse Width (t_W)	10 ns	10 ns	12 ns
Write Recovery (t_{WR})	10 ns	12 ns	15 ns
Chip Select Access/ Recovery (t_{ACS}/t_{RCS})	8 ns	8 ns	8 ns
Write Disable (t_{WS})	10 ns	10 ns	10 ns
Power Supply (I_{EE})	150 mA	150 mA	150 mA

Publication # 01418 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



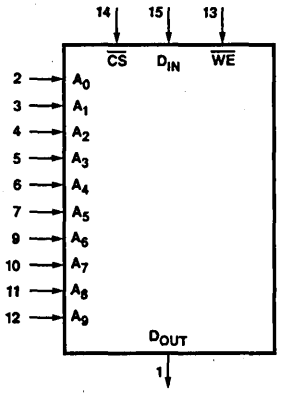
CD000920



CD009800

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



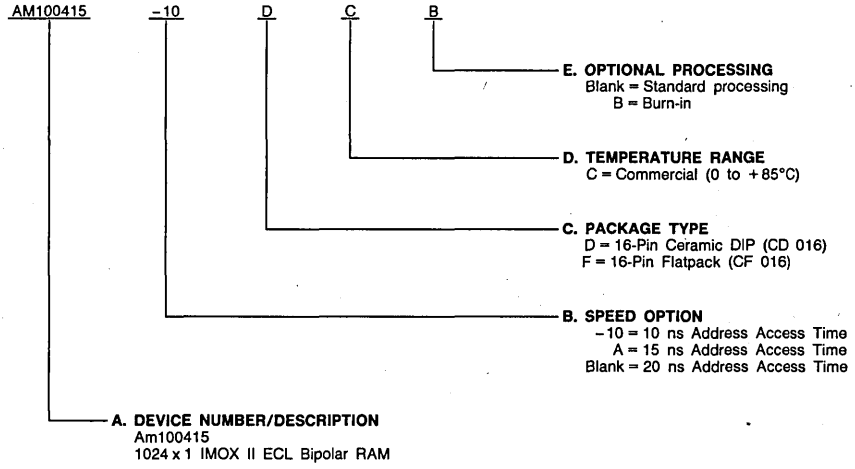
LS000241

V_{CC} = Pin 16
V_{EE} = Pin 8

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM100415-10	DC, DCB FC, FCB
AM100415A	
Am100415	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to
GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

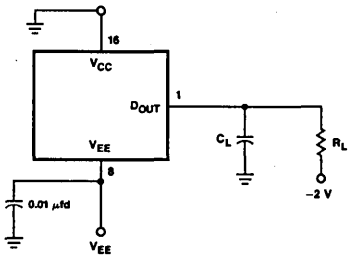
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS $V_{EE} = -4.5$ V, $V_{CC} = GND$ (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		B(Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	−1025	−955	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1715	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for all inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for all inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$				220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 8)	All Inputs and Outputs Open		−150	−105		mA

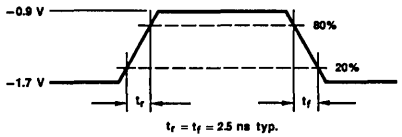
Notes:
1. Typical values are at $V_{EE} = -4.5$ V, $T = 25°C$ and maximum loading.
2. Output load = 50 Ω and 30 pF to −2.0 V
   $T = T_A = 0$ to +85°C for Ceramic DIPs.
   Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   $T = T_C = 0$ to +85°C for Flatpacks and Leadless Chip Carriers
   θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING TEST CIRCUIT



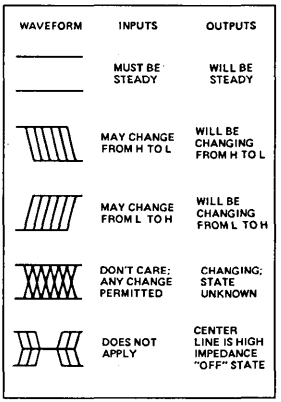
TC000221

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING WAVEFORMS



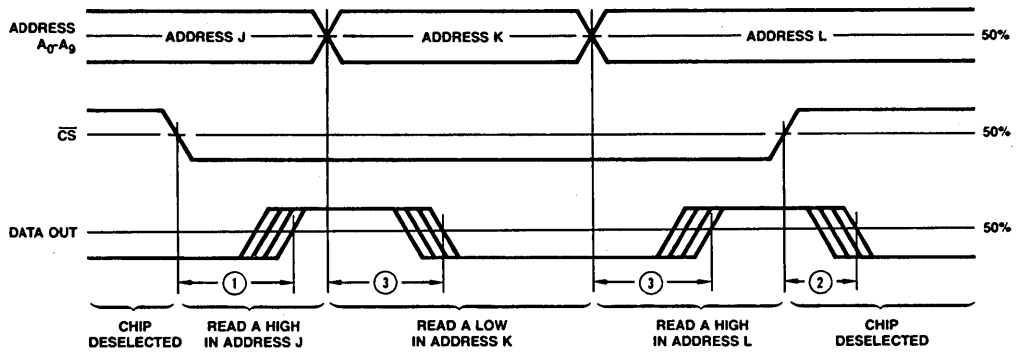
KS000010

R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)

SWITCHING CHARACTERISTICS V_{EE} = −4.27 to −4.73 V (Note 2)

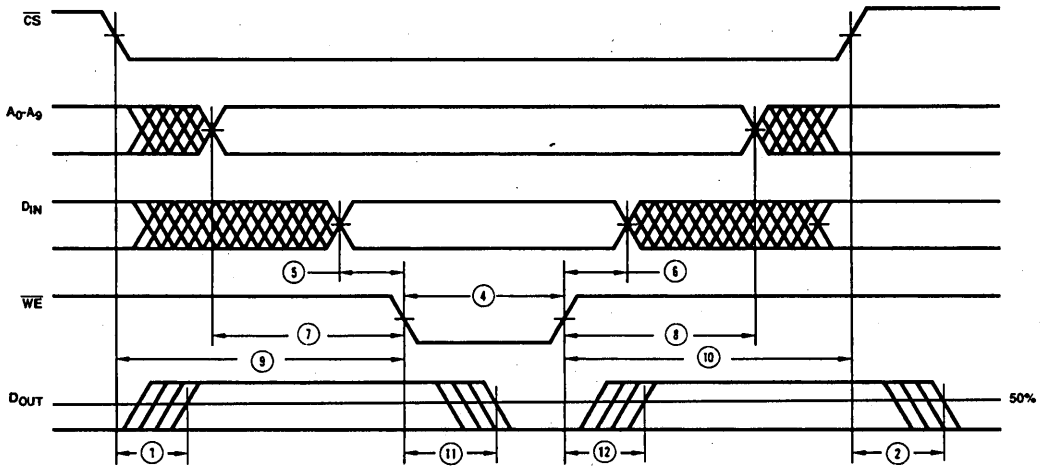
No.	Parameter Symbol	Parameter Description	Test Conditions	Am100415A-10 Min.	Am100415A-10 Typ. (Note 1)	Am100415A-10 Max.	Am100415A Min.	Am100415A Typ. (Note 1)	Am100415A Max.	Am100415 Min.	Am100415 Typ. (Note 1)	Am100415 Max.	Units
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		5	8		5	8		5	8	ns
2	t_{RCS}	Chip Select Recovery Time			5	8		5	8		5	8	
3	t_{AA}	Address Access Time			8	10		10	15		12	20	
WRITE MODE													
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$(Min.)	10	6		10	6		12	9		ns
5	t_{WSD}	Data Setup Time Prior to Write		1	0		2	0		4	0		ns
6	t_{WHD}	Data Hold Time After Write		1	0		2	0		4	0		ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$(Min.)	1	0		3	3		5	3		ns
8	t_{WHA}	Address Hold Time After Write		1	0		2	0		3	0		ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	1	0		2	0		4	0		ns
				1	0		2	0		4	0		ns
					5	10		5	10		5	10	ns
					6	10		6	12		7	15	ns
RISE TIME AND FALL TIME													
	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
	t_f	Output Fall Time			2.5			2.5			2.5		
CAPACITANCE													
	C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5		4	5	pF
	C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

SWITCHING WAVEFORMS



WF001173

Read Mode



WF001163

Write Mode

Am10415

1024 x 1 IMOX™ ECL Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fast access time (8 ns typ.) — improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL — no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

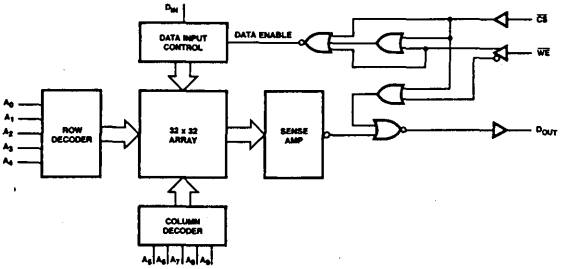
The Am10415 is a fully decoded 1024-bit ECL RAM organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and an unterminated OR-tieable emitter follower output.

An active-LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000640

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH ≅ −0.9 V
L = LOW ≅ −1.7 V
X = Don't Care

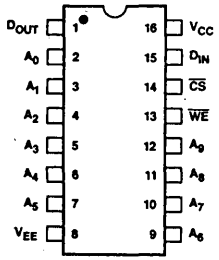
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters

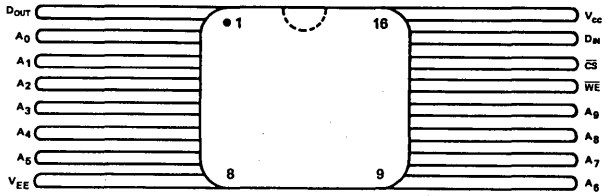
Part Number	Am10415-10	Am10415SA	Am10415A	Am10415-15	Am10415SA	Am10415A
Temperature Range	C	C	C	M	M	M
Address Access Time (t_{AA})	10 ns	15 ns	20 ns	15 ns	20 ns	25 ns
Write Pulse Width (t_W)	10 ns	10 ns	12 ns	11 ns	13 ns	16 ns
Write Recovery (t_{WR})	10 ns	12 ns	15 ns	10 ns	12 ns	15 ns
Chip Select Access/ Recovery (t_{ACS}/t_{RCS})	8 ns	8 ns	8 ns	10 ns	10 ns	12 ns
Write Disable (t_{WS})	10 ns	10 ns	10 ns	10 ns	10 ns	10 ns
Power Supply (I_{EE})	−150 mA	−150 mA	−150 mA	−165 mA	−165 mA	−165 mA

Publication # 01419 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



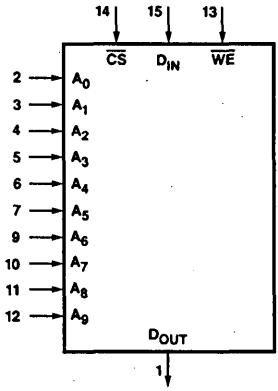
CD000920



CD009800

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

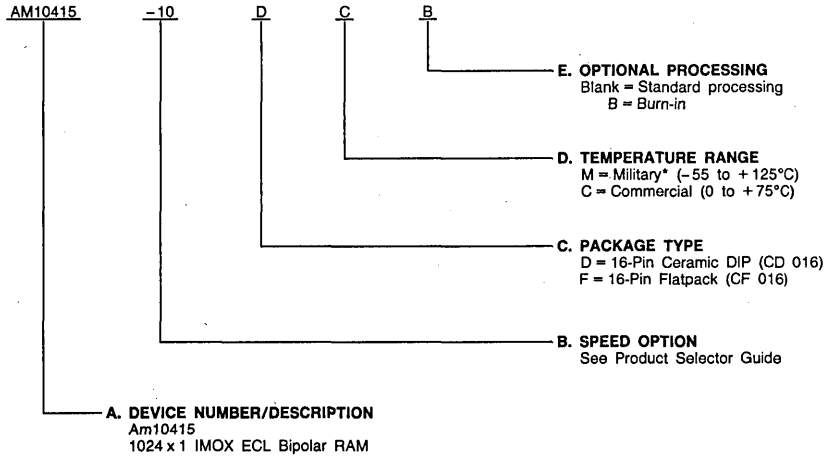


LS000241

V_{CC} = Pin 16
V_{EE} = Pin 8

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM10415-10	DC, DCB, FC, FCB
AM10415-15	DMB, FMB
AM10415SA	DC, DCB, FC,
AM10415A	FCB, DMB, FMB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.46 V to −4.94 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... −5.72 V to −4.68 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (Commercial)* V_{EE} = −5.2 V, V_{CC} = GND (Note 2)

Parameter Symbol	Parameter Description	Test Conditions			B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	T = 0°C	−1000		−840	mV
				T = +25°C	−960		−810	
				T = +75°C	−900		−720	
V_{OL}	Output Voltage LOW			T = 0°C	−1870		−1665	mV
				T = +25°C	−1850		−1650	
				T = +75°C	−1830		−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T = 0°C	−1020			mV
				T = +25°C	−980			
				T = +75°C	−920			
V_{OLC}	Output Voltage LOW			T = 0°C			−1645	mV
				T = +25°C			−1630	
				T = +75°C			−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T = 0°C	−1145		−840	mV
				T = +25°C	−1105		−810	
				T = +75°C	−1045		−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T = 0°C	−1870		−1490	mV
				T = +25°C	−1850		−1475	
				T = +75°C	−1830		−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T = 0 to +75°C			220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		T = +25°C	0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 8)	All Inputs and Outputs Open		T = 0°C	−150	−105		mA
				T = +75°C		−90		

Notes: 1. Typical values are at V_{EE} = −5.2 V, T = 25°C and maximum loading.
2. Output load = 50 Ω and 30 pF to −2.0 V. T = T_A = 0 to +75°C for Commercial DIPs.
Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate thermal resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T = T_C = 0 to + 75°C for Flatpacks and Leadless Chip Carriers
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
5. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T = T_C.
$\theta_{JC} \approx 25°C/W$ (approximately)

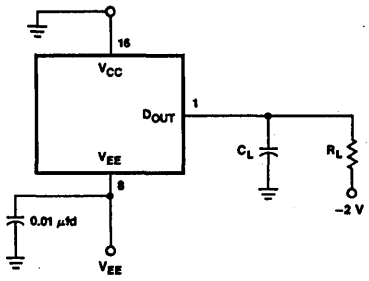
*See the last page of this spec for Group A Subgroup Testing information.

DC CHARACTERISTICS (Military)* $V_{EE} = -5.2$ V, $V_{CC} = GND$ (Note 5)

Parameter Symbol	Parameter Description	Test Conditions			B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	T = −55°C	−1140		−870	mV
				T = +25°C	−1000		−840	
				T = +125°C	−880		−685	
V_{OL}	Output Voltage LOW			T = −55°C	−1910		−1700	
				T = +25°C	−1870		−1665	
				T = +125°C	−1815		−1600	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T = −55°C	−1160			mV
				T = +25°C	−1020			
				T = +125°C	−900			
V_{OLC}	Output Voltage LOW			T = −55°C			−1680	mV
				T = +25°C			−1645	
				T = +125°C			−1580	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T = −55°C	−1285		−870	mV
				T = +25°C	−1145		−840	
				T = +125°C	−1025		−685	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T = −55°C	−1910		−1525	mV
				T = +25°C	−1870		−1490	
				T = +125°C	−1815		−1420	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T = −55°C			220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{ILB}$		T = 55°C	0.5		170	μA
	Chip Select ($\overline{CS}$)							
	All Other Inputs				−50			
I_{EE}	Power Supply Current (Pin 8)	All Inputs and Outputs Open		T = −55°C	−165	−115		mA
				T = +125°C		−80		

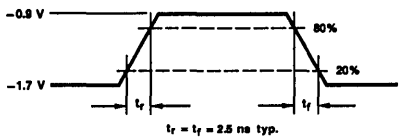
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



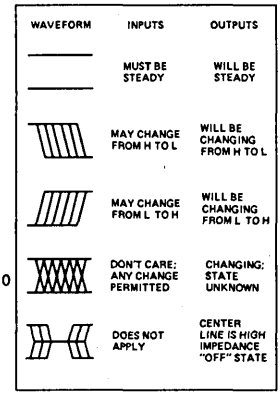
TC003800

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING TEST WAVEFORM



KS000010

R_L = 50 Ω temination of measurement system
C_L = 30 pF(including stray jig capacitance)

SWITCHING CHARACTERISTICS* V_{EE} = −5.46 to −4.94 V (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am10415-10 Min.	Am10415-10 Typ. (Note 1)	Am10415-10 Max.	Am10415SA Min.	Am10415SA Typ. (Note 1)	Am10415SA Max.	Am10415A Min.	Am10415A Typ. (Note 1)	Am10415A Max.	Units
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output		6	8		6	8		6	8	ns
2	t_{RCS}	Chip Select Recovery Time			5	8		5	8		5	8	ns
3	t_{AA}	Address Access Time			8	10		10	15		13	20	ns
WRITE MODE													
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$(Min.)	10	6		10	9		12	9		ns
5	t_{WSD}	Data Setup Time Prior to Write		1	0		2	0		4	0		ns
6	t_{WHD}	Data Hold Time After Write		1	0		2	0		4	0		ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$(Min.)	1	0		3	3		5	3		ns
8	t_{WHA}	Address Hold Time After Write		1	0		2	0		3	1		ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	1	0		2	0		4	0		ns
10	t_{WHCS}	Chip Select Hold Time After Write		1	0		2	0		4	0		ns
11	t_{WS}	Write Disable Time			5	10		5	10		5	10	ns
10	t_{WR}	Write Recovery Time			6	10		6	12		10	15	ns
RISE TIME AND FALL TIME													
	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
	t_f	Output Fall Time			2.5			2.5			2.5		
CAPACITANCE													
	C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5		4	5	pF
	C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	

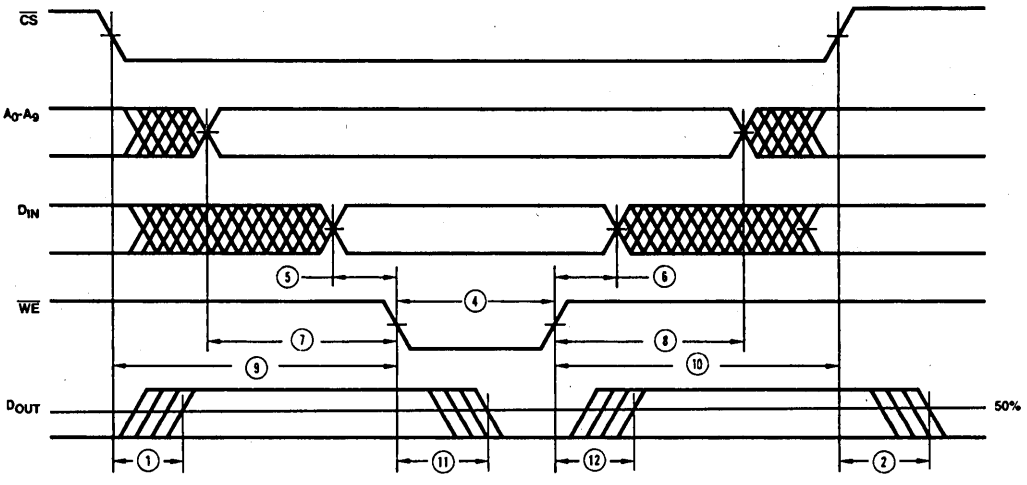
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS (Military)* V_{EE} = −5.72 to −4.68 V (Note 5)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am10415-15			Am10415SA			Am10415A			Units
				Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output		6	10		6	10		6	12	ns
2	t_{RCS}	Chip Select Recovery Time			5	10		5	10		5	12	ns
3	t_{AA}	Address Access Time			10	15		10	20		13	25	ns
WRITE MODE													
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$(Min.)	11	6		16	6		16	9		ns
5	t_{WSD}	Data Setup Time Prior to Write		2	0		4	0		4	0		ns
6	t_{WHD}	Data Hold Time After Write		2	0		4	0		4	0		ns
7	t_{WSA}	Address Setup Time	$t_W = t_W$(Min.)	2	0		5	3		5	3		ns
8	t_{WHA}	Address Hold Time After Write		2	0		4	0		4	0		ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2	0		4	0		4	0		ns
10	t_{WHCS}	Chip Select Hold Time After Write		2	0		4	0		4	0		ns
11	t_{WS}	Write Disable Time			5	10		5	10		5	10	ns
12	t_{WR}	Write Recovery Time			6	10		6	12		10	15	ns
RISE TIME AND FALL TIME													
	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
	t_f	Output Fall Time			2.5			2.5			2.5		ns
CAPACITANCE													
	C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5		4	5	pF
	C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	

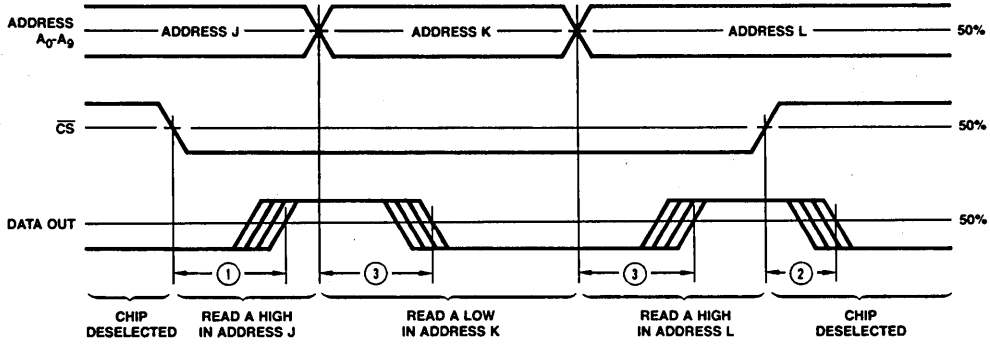
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF001163

Write Mode



WF001173

Read Mode

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OHC}	1, 2, 3
V_{OLC}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{EE}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACS}	9, 10, 11	7	t_{WSA}	9, 10, 11
2	t_{RCS}	9, 10, 11	8	t_{WHA}	9, 10, 11
3	t_{AA}	9, 10, 11	9	t_{WSCS}	9, 10, 11
4	t_{W}	9, 10, 11	10	t_{WHCS}	9, 10, 11
5	t_{WSD}	9, 10, 11	11	t_{WS}	9, 10, 11
6	t_{WHD}	9, 10, 11	12	t_{WR}	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am10469/Am100469

512 x 9 ECL Tag Buffer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast address to comparator output (MISS)
- Replaces six or more integrated circuits with a single device
- On-chip parity generator and checker
- Easy horizontal and vertical expansion
- Fully ECL compatible in 10K and 100K versions
- Integrated reset feature
- 24-pin ceramic DIP (400 Mil) and Flatpak packages

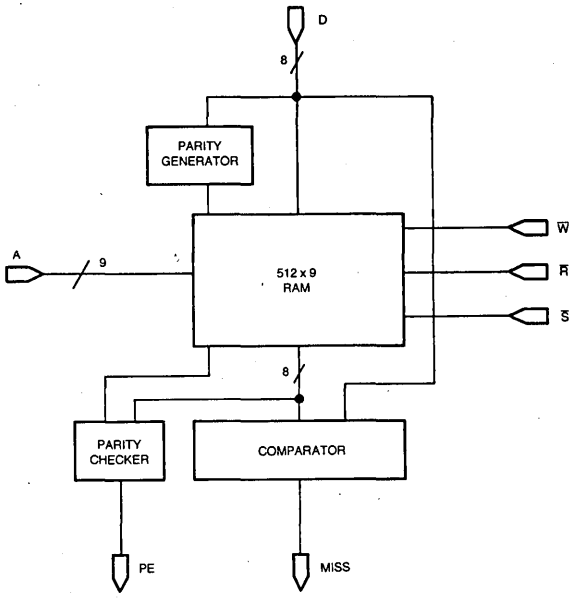
GENERAL DESCRIPTION

The Am10469/Am100469 Tag Buffer combines a 512 x 9 memory with a comparator. An internal parity generator and parity checker guarantee that no misoperation occurs.

The device has three operational modes: Compare, Write, and Reset. In Compare mode, data is compared to the contents of an address location. Write mode is used to store data. Reset mode is used to clear a single "valid bit" stream.

The Tag Buffer is designed to be used in a cache memory system for the translation of virtual addresses to physical addresses. The device can also be used in the directory and data cache. It offers state-of-the-art technology performance, while combining the functions of six or more integrated circuits into a single device.

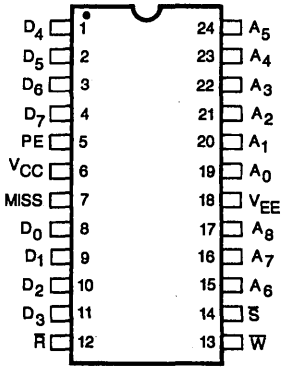
BLOCK DIAGRAM



BD005900

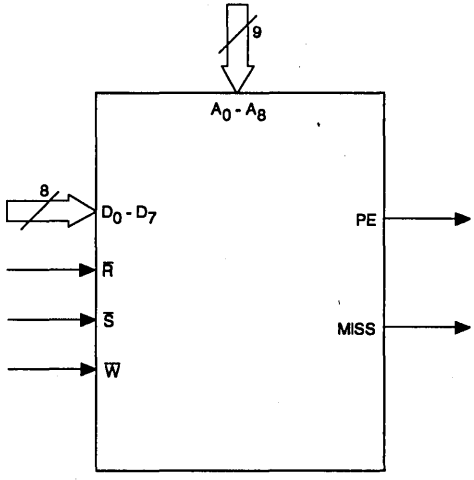
Publication # 07561 | Rev. A | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009161

LOGIC SYMBOL



LS002201

V_{CC} = Positive Supply
= Ground
V_{EE} = Negative Supply

PIN DESCRIPTION

$A_0 - A_8$ Address (Inputs)
Identifies memory locations.

$D_0 - D_7$ Data (Inputs)
During Compare cycle, eight bits of data are compared with address location given by $A_0 - A_8$ for equality. The result is indicated on the Comparator output pin, MISS. When $\overline{W}$ is LOW, data is written into the address location given by $A_0 - A_8$.

$\overline{R}$ $\overline{\text{Reset}}$ (Input, Active LOW)
Resets D_3 to zero.

$\overline{S}$ $\overline{\text{Chip Select}}$ (Input, Active LOW)
When $\overline{S}$ is LOW, the device is activated. A HIGH on this input will disable the chip and force PE and MISS outputs LOW, allowing easy vertical expansion.

$\overline{W}$ $\overline{\text{Write Enable}}$ (Input, Active LOW)
Must be LOW to write Data ($D_0 - D_7$) into location given by $A_0 - A_8$. PE output is LOW and MISS output HIGH during Write cycle.

MISS Comparator Miss (Output, Active HIGH)
LOW when Data ($D_0 - D_7$) equals content of memory location specified by $A_0 - A_8$. HIGH when mismatch occurs.

PE Parity Error (Output, Active HIGH)
HIGH when the nine bits of internal data do not constitute odd parity.

FUNCTIONAL DESCRIPTION

The Am10469/Am100469 Tag Buffer has three modes of operation: Compare, Write, and Reset. These modes are described as follows.

Compare Mode

The eight bits of Data inputs are compared with the content of a given memory location for equality. The nine address inputs define each memory location. In this mode, $\overline{W}$ and $\overline{R}$ inputs are HIGH, and $\overline{S}$ is LOW. If the eight bits of Data inputs are exactly the same as the eight bits of data in the given memory location, the MISS output will be LOW. If not, the MISS output will be HIGH. The parity bit out of the memory array is not compared.

Write Mode

The eight bits of data inputs and the one bit of parity are written into the RAM array when both $\overline{S}$ and $\overline{W}$ are LOW, and $\overline{R}$ is HIGH. The MISS output is forced HIGH (the MISS output is associated with the output enable of the data cache). The Parity Error (PE) output is forced LOW.

Reset Mode

When $\overline{R}$ = LOW, $\overline{S}$ = LOW, and $\overline{W}$ = HIGH, a dedicated section of the entire array, D_3, is reset to LOW. The PE output is forced LOW during reset. The MISS output is forced HIGH. All 512 D_3 data bits are reset to a low state. The other seven bits in each address location may change to an undetermined state (HIGH or LOW).

TABLE 1. FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{S}$	$\overline{W}$	$\overline{R}$	PE	MISS	DESCRIPTION
H	X	X	L	L	Disabled
L	H	H	H = Parity Error L = No Parity Error	H = MISS L = MATCH	Compare
L	H	L	L	H	Reset
L	L	H	L	H	Write
L	L	L	L	H	Illegal

Key: H = HIGH
L = LOW
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −7.0 to +0.5 V
DC Input Voltage ..... V_{EE} to +0.5 V
DC Output HIGH Current ..... −30 to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

10K Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{EE}) ..... −5.46 to −4.94 V

100K Commercial (C) Devices
Temperature (T_A) ..... 0 to +85°C
Supply Voltage (V_{EE}) ..... −5.7 to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameter Symbol	Parameter Description	Test Conditions (Note 3)			B (Note 4) Min.	A (Note 4) Max.	Units
Am10469 10K 512 x 9 ECL TAG BUFFER							
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	$T_A = 0°C$	−1000	−840	mV
				$T_A = +25°C$	−960	−810	
				$T_A = +75°C$	−900	−720	
V_{OL}	Output Voltage LOW			$T_A = 0°C$	−1870	−1665	mV
				$T_A = +25°C$	−1850	−1650	
				$T_A = +75°C$	−1830	−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		$T_A = 0°C$	−1020		mV
				$T_A = +25°C$	−980		
				$T_A = +75°C$	−920		
V_{OLC}	Output Voltage LOW			$T_A = 0°C$		−1645	mV
				$T_A = +25°C$		−1630	
				$T_A = +75°C$		−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 2)		$T_A = 0°C$	−1145	−840	mV
				$T_A = +25°C$	−1105	−810	
				$T_A = +75°C$	−1045	−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 2)		$T_A = 0°C$	−1870	−1490	mV
				$T_A = +25°C$	−1850	−1475	
				$T_A = +75°C$	−1830	−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		$T_A = 0$ to +75°C		220	µA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	$V_{IN} = V_{ILB}$		$T_A = 0$ to +75°C	0.5	170	µA
	All Other Inputs				−50		
I_{EE}	Power Supply Current (Pin 12)	All Inputs and Outputs Open	Am10474-10	$T_A = 0$ to +75°C	−240		mA
Am100469 100K 512 x 9 ECL TAG BUFFER							
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		Loading is 50 Ω to −2.0 V	−1025	−880	mV
V_{OL}	Output LOW Voltage				−1810	−1620	
V_{OHC}	Output HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}			−1035		mV
V_{OLC}	Output LOW Voltage					−1610	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Note 2)			−1165	−880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Note 2)			−1810	−1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$				200	µA
I_{IL}	Input LOW Current Chip Select ($\overline{S}$)	$V_{IN} = V_{ILB}$			0.5	170	µA
	All Other Inputs				−50		
I_{EE}	Power Supply Current (Pin 18)	All Inputs and Outputs Open			−240		mA

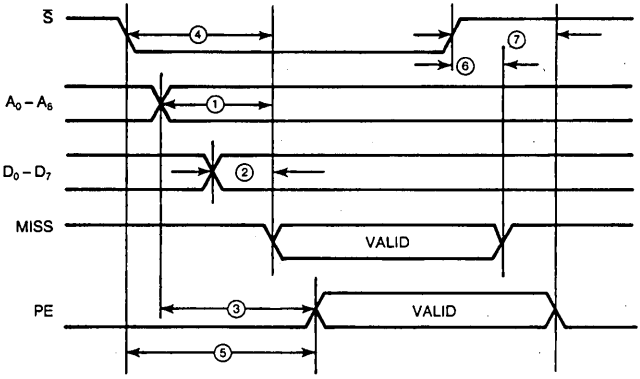
Notes:
1. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two-minute warm-up period. Typical resistance values of the page are:
   θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction-to-Case) = 25°C/Watt
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. $T_A = T_C$ for Flatpacks.
4. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
Compare Mode					
1	t_{AVMV}	Address to MISS		9.5	ns
2	t_{DVMV}	Data to MISS		4.5	ns
3	t_{AVPV}	Address to PE		12.0	ns
4	t_{SLMV}	$\overline{S}$ to MISS		5.0	ns
5	t_{SLPV}	$\overline{S}$ to PE		5.0	ns
6	t_{SHML}	$\overline{S}$ to MISS Recovery		5.0	ns
7	t_{SHPL}	$\overline{S}$ to PE Recovery		5.0	ns
Write Mode					
8	t_{WLWH}	Write Pulse Width	12.5		ns
9	t_{AVWL}	Address Setup	2.0		ns
10	t_{WHAX}	Address to $\overline{W}$ Hold	2.0		ns
11	t_{DVWH}	Data to $\overline{W}$ Setup	14.5		ns
12	t_{WHDX}	Data to $\overline{W}$ Hold	2.0		ns
13	t_{SLWH}	$\overline{S}$ Setup	14.5		ns
14	t_{WHSH}	$\overline{S}$ Hold	2.0		ns
15	t_{WLMH}	$\overline{W}$ to MISS		5.0	ns
16	t_{WHMX}	Write Recovery (MISS)		11.5	ns
17	t_{WLPL}	$\overline{W}$ to PE		5.0	ns
18	t_{WHPX}	Write Recovery (PE)		14.0	ns
Reset Mode					
19	t_{RLRH}	$\overline{R}$ Pulse Width	50.0		ns
20	t_{SLRL}	$\overline{S}$ to $\overline{R}$ Setup	2.0		ns
21	t_{RHSH}	$\overline{S}$ to $\overline{R}$ Hold	10.0		ns
22	t_{WHRL}	$\overline{W}$ to $\overline{R}$ Setup	2.0		ns
23	t_{RHWL}	$\overline{W}$ to $\overline{R}$ Hold	10.0		ns
24	t_{RLMH}	$\overline{R}$ to MISS HIGH		5.0	ns
25	t_{RHMX}	$\overline{R}$ to MISS Recovery		12.0	ns
26	t_{RLPL}	$\overline{R}$ to PE LOW		5.0	ns
27	t_{RHPX}	$\overline{R}$ to PE Recovery		14.0	ns

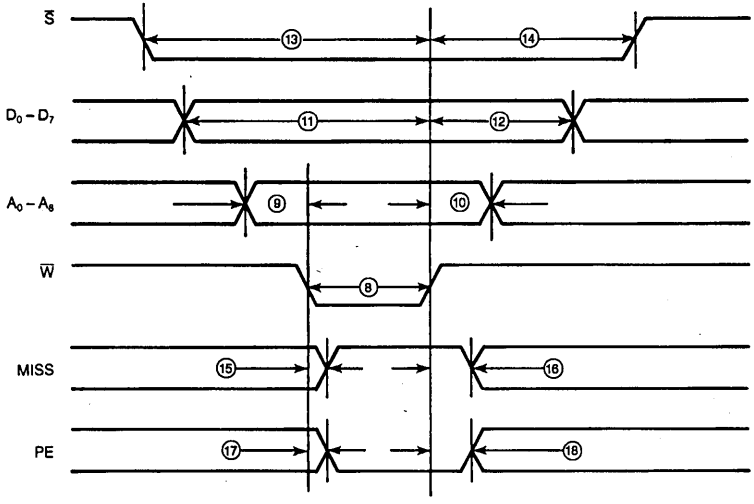
Notes: 1. *All Switching Characteristics are measured at 50% of input to valid output.*

SWITCHING WAVEFORMS



WF021890

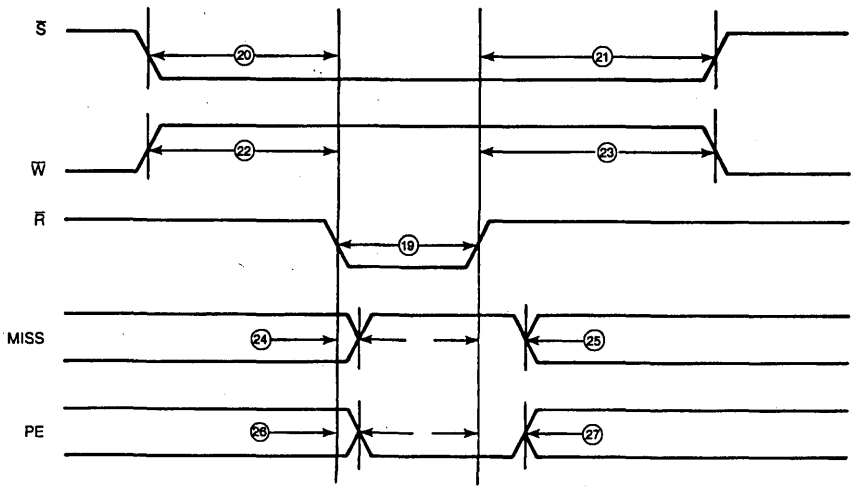
Compare Mode



WF021011

Write Mode

SWITCHING WAVEFORMS (Cont.)



WF021021

Reset Mode

Am100470

4096 x 1 IMOX™ ECL Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fast access time (12 ns typ.) — improves system cycle speeds
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

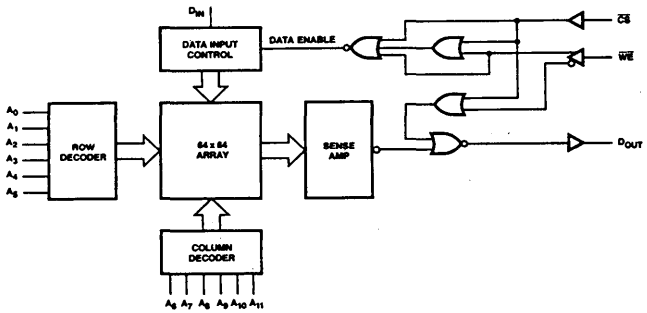
The Am100470 is a fully decoded 4096-bit ECL RAM organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and an unterminated OR-tieable emitter follower output.

An active-LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000660

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH = −0.9 V
L = LOW = −1.7 V
X = Don't Care

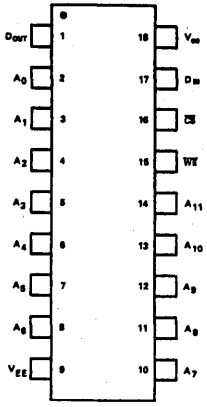
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

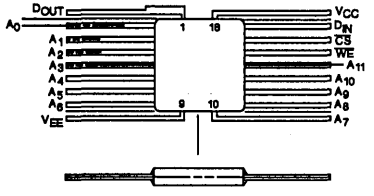
Part Number	Am100470SA	Am100470A
Address Access Time (t_{AA})	15 ns	25 ns
Write Pulse Width (t_W)	15 ns	20 ns
Write Recovery (t_{WR})	8 ns	10 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	10 ns
Power Supply (I_{EE})	230 mA	200 mA

Publication # 03225 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



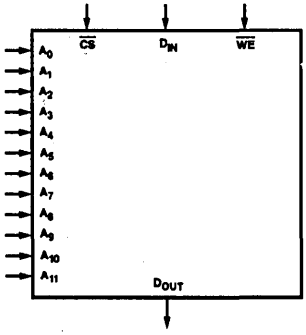
CD005331



CD009790

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



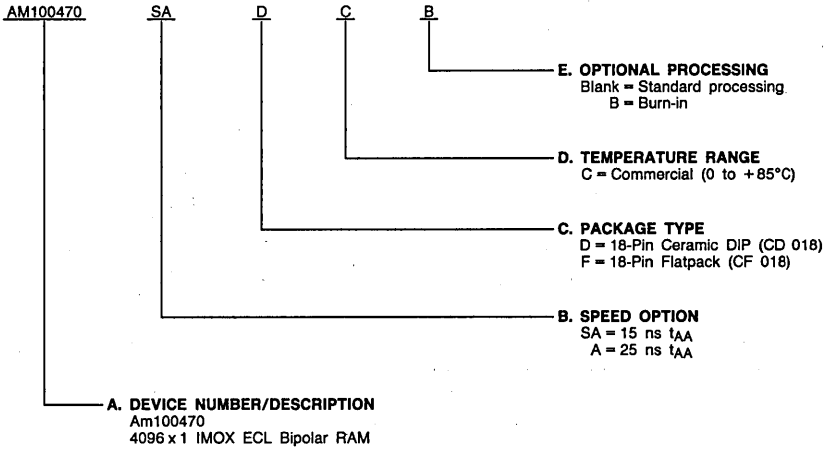
LS002550

V_{CC} = Pin 18
V_{EE} = Pin 9

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM100470SA	DC, DCB,
AM100470A	FC, FCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

3

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

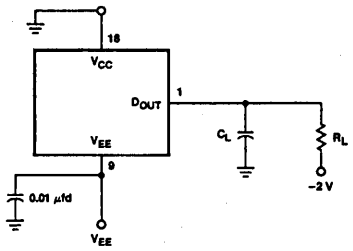
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{EE} = −4.5 V, V_{CC} = GND (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	−1025	−955	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1715	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for all inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for all inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$				220	μA
I_{IL}	Input Current LOW Chip Select($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 9)	All Inputs and Outputs Open	Am100470A	−200	−160		mA
			Am100470SA	−230	−180		

Notes: 1. Typical values are at V_{EE} = −4.5V, T = 25°C and maximum loading.
2. Output Load = 50 Ω and 30 pF to −2.0 V
T = T_A = 0 to +85°C for DIPs.
Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T = T_C = 0 to +85°C for Flatpacks and Leadless Chip Carriers.
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

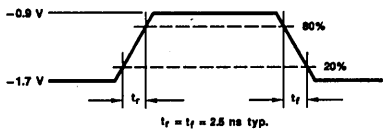
SWITCHING TEST CIRCUIT



TC000231

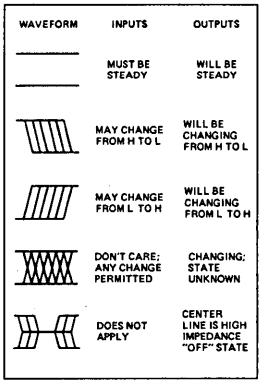
R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)

SWITCHING TEST WAVEFORMS



TW000310

KEY TO SWITCHING WAVEFORMS



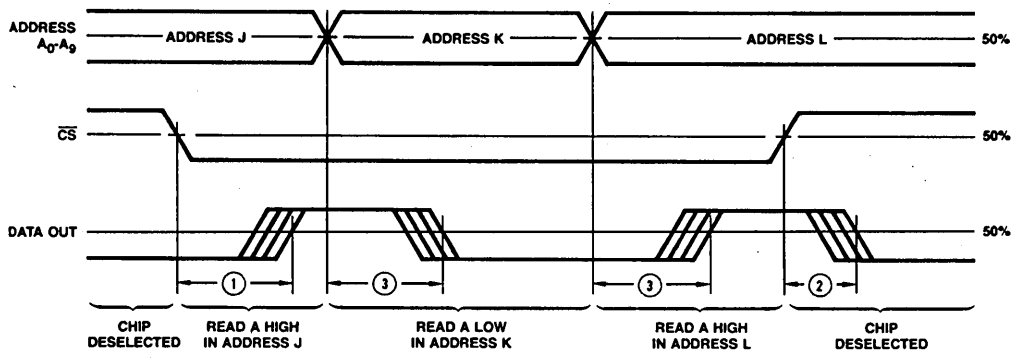
KS000010

3

SWITCHING CHARACTERISTICS V_{EE} = −4.73 to −4.72 V (Note 2)

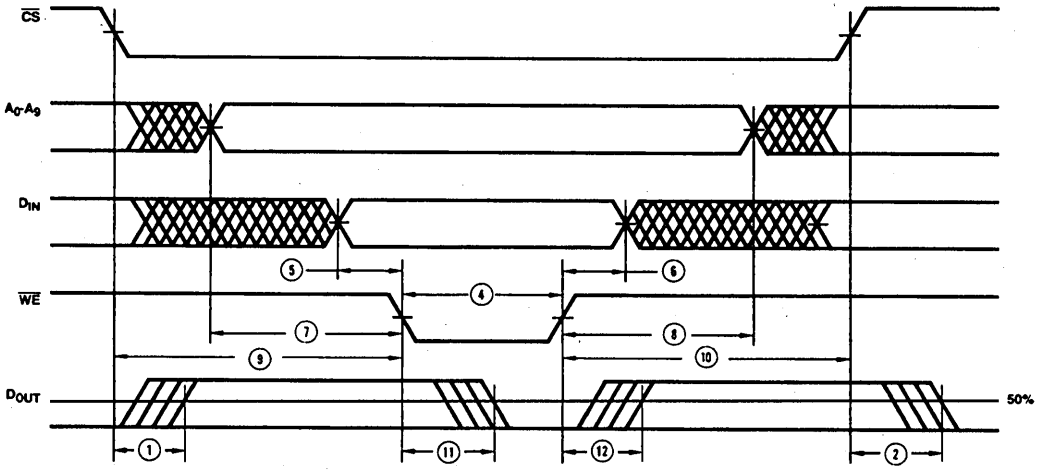
No.	Parameter Symbol	Parameter Description	Test Conditions	Am100470SA Min.	Am100470SA Typ. (Note 1)	Am100470SA Max.	Am100470A Min.	Am100470A Typ. (Note 1)	Am100470A Max.	Units
READ MODE										
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output		6	8		8	10	ns
2	t_{RCS}	Chip Select Recovery Time			6	8		8	10	ns
3	t_{AA}	Address Access Time			12	15		18	25	ns
WRITE MODE										
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$(Min.)	15			20			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			2			ns
6	t_{WHD}	Data Hold Time After Write		2			2			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$(Min.)	3			3			ns
8	t_{WHA}	Address Hold Time After Write		2			2			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			2			ns
10	t_{WHCS}	Chip Select Hold Time After Write		2			2			ns
11	t_{WS}	Write Disable Time			6	8		8	10	ns
12	t_{WR}	Write Recovery Time			6	8		8	10	ns
RISE TIME AND FALL TIME										
	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5		ns
	t_f	Output Fall Time			2.5			2.5		
CAPACITANCE										
	C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique on a Sample Basis.		4	5		4	5	pF
	C_{OUT}	Output Pin Capacitance			7	8		7	8	

SWITCHING WAVEFORMS



WF001173

Read Mode



WF001163

Write Mode

Am10470

4096 x 1 IMOX™ ECL Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fast access time (12 ns typ.) — improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL — no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

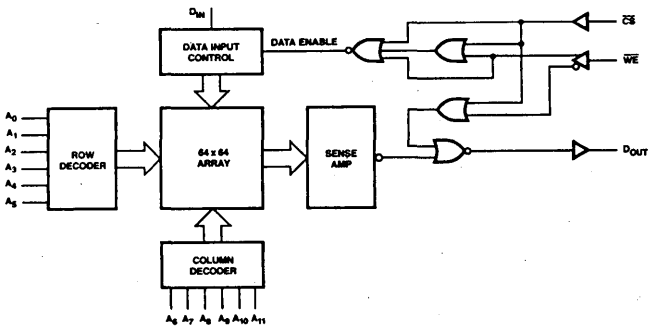
The Am10470 is a fully decoded 4096-bit ECL RAM organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and an unterminated OR-tieable emitter follower output.

An active-LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000660

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH = −0.9 V
L = LOW = −1.7 V
X = Don't Care

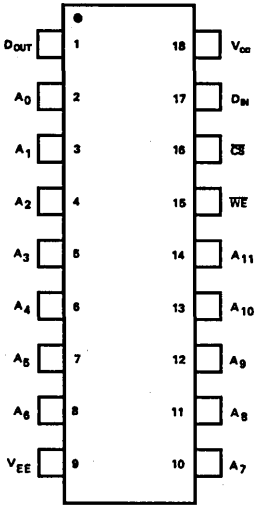
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters

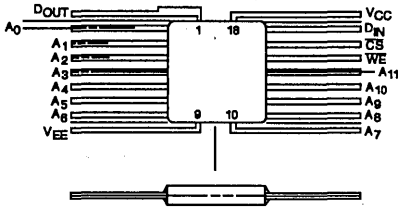
Part Number	Am10470SA	Am10470-15	Am10470SA	Am10470A	Am10470A
Temperature Range	C	M	M	C	M
Address Access Time (t_{AA})	15 ns	15 ns	20 ns	25 ns	30 ns
Write Pulse Width (t_W)	15 ns	15 ns	18 ns	20 ns	22 ns
Write Recovery (t_{WR})	8 ns	10 ns	10 ns	10 ns	12 ns
Chip Select Access/Recovery (t_{ACS}/t_{RCS})	8 ns	10 ns	10 ns	10 ns	15 ns
Write Disable (t_{WS})	8 ns	10 ns	10 ns	10 ns	12 ns
Power Supply (I_{EE})	230 mA	255 mA	255 mA	200 mA	220 mA

Publication # 03224 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



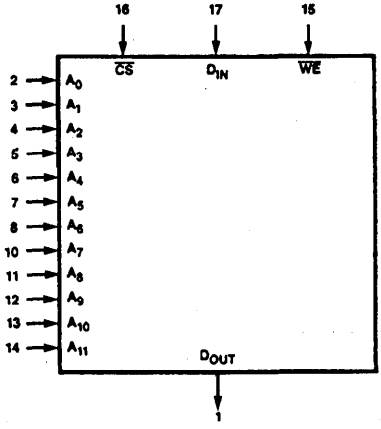
CD009810



CD009790

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



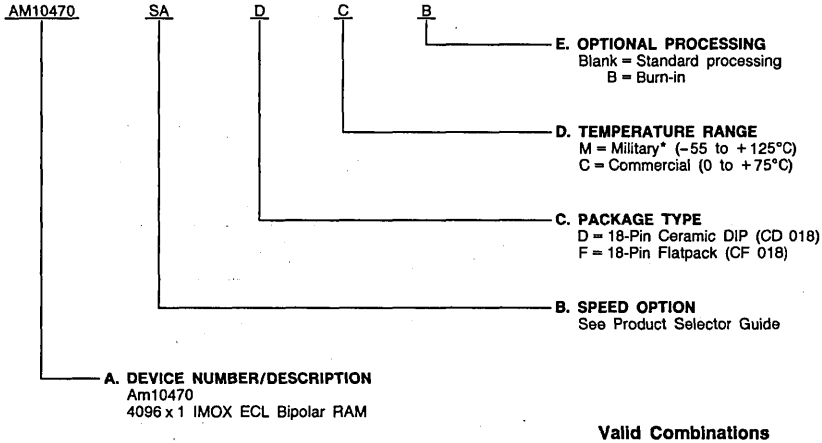
LS000271

V_{CC} = Pin 18
V_{EE} = Pin 9

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM10470SA	DC, DCB, DMB
AM10470A	FC, FCB, FMB
AM10470-15	DMB, FMB

*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

3

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to 150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) ... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.46 V to −4.94 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... −5.72 V to −4.68 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (Commercial)* V_{EE} = −5.2 V, V_{CC}=GND (Note 2)

Parameter Symbol	Parameter Description	Test Conditions			B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	T = 0°C	−1000		−840	mV
				T = +25°C	−960		−810	
				T = +75°C	−900		−720	
V_{OL}	Output Voltage LOW			T = 0°C	−1870		−1665	mV
				T = +25°C	−1850		−1650	
				T = +75°C	−1830		−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T = 0°C	−1020			mV
				T = +25°C	−980			
				T = +75°C	−920			
V_{OLC}	Output Voltage LOW			T = 0°C			−1645	mV
				T = +25°C			−1630	
				T = +75°C			−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Input (Note 4)		T = 0°C	−1145		−840	mV
				T = +25°C	−1105		−810	
				T = +75°C	−1045		−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage Low for All Inputs (Note 4)		T = 0°C	−1870		−1490	mV
				T = +25°C	−1850		−1475	
				T = +75°C	−1830		−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T = 0°C to +75°C			220	µA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		T = +25°C	0.5 −50		170	µA
I_{EE}	Power Supply Current (Pin 9)	All Inputs and Outputs Open	Am10470A and Am10470	T = 0°C	−200	−160		mA
				T = +75°C		−145		
			Am10470SA	T = 0°C	−230	−180		

Notes: 1. Typical values are at V_{EE} = −5.2 V, T_A = 25°C and maximum loading.
2. Output Load = 50 Ω and 30 pF to −2.0 V
T=T_A = 0 to +75°C for Commercial DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate thermal resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T = T_C=0 to +75°C for Flatpacks and Leadless Chip Carriers.
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
5. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T = T_C.
$\theta_{JC} \approx 25°C/W$ (approximately).

*See the last page of this spec for Group A Subgroup Testing information.

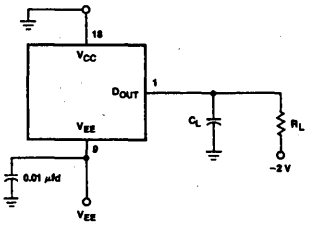
DC CHARACTERISTICS (Military)* $V_{EE} = -5.2$ V, $V_{CC} = GND$ (Note 5)

Parameter Symbol	Parameter Description	Test Conditions			B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	$T_A = -55°C$	−1140		−870	mV
				$T_A = +25°C$	−1000		−840	
				$T_A = +125°C$	−880		−685	
V_{OL}	Output Voltage LOW			$T_A = -55°C$	−1910		−1700	
				$T_A = +25°C$	−1870		−1665	
				$T_A = +125°C$	−1815		−1600	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		$T_A = -55°C$	−1160			mV
				$T_A = +25°C$	−1020			
				$T_A = +125°C$	−900			
V_{OLC}	Output Voltage LOW			$T_A = -55°C$			−1680	mV
				$T_A = +25°C$			−1645	
				$T_A = +125°C$			−1580	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		$T_A = -55°C$	−1285		−870	mV
				$T_A = +25°C$	−1145		−840	
				$T_A = +125°C$	−1025		−685	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		$T_A = -55°C$	−1910		−1525	mV
				$T_A = +25°C$	−1870		−1490	
				$T_A = +125°C$	−1815		−1420	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		$T_A = -55°C$			220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		$T_A = -55°C$	0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 9)	All Inputs and Outputs Open	Am10470A	$T_A = -55°C$	−220	−175		mA
				$T_A = +125°C$		−160		
			Am10470SA Am10470-15	$T_A = -55°C$	−255	−200		

*See the last page of this spec for Group A Subgroup Testing information.

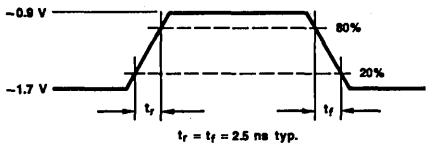
3

SWITCHING TEST CIRCUIT



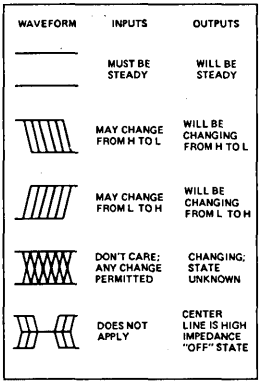
TC000231

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING WAVEFORMS



KS000010

R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)

SWITCHING CHARACTERISTICS (Commercial)* V_{EE} = −5.46 to −4.94 V (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am10470SA Min.	Am10470SA Typ. (Note 1)	Am10470SA Max.	Am10470A Min.	Am10470A Typ. (Note 1)	Am10470A Max.	Units
READ MODE										
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output		6	8		8	10	ns
2	t_{RCS}	Chip Select Recovery Time			6	8		8	10	ns
3	t_{AA}	Address Access Time			12	15		18	25	ns
WRITE MODE										
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	15	8		20	10		ns
5	t_{WSD}	Data Setup Time Prior to Write		2	0		2	0		ns
6	t_{WHD}	Data Hold Time After Write		2	0		2	0		ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2	0		2	0		ns
8	t_{WHA}	Address Hold Time After Write		2	0		2	0		ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			2	0		ns
10	t_{WHCS}	Chip Select Hold Time After Write		2	0		2	0		ns
11	t_{WS}	Write Disable Time			6	8		8	10	ns
12	t_{WR}	Write Recovery Time			6	8		8	10	ns
RISE TIME AND FALL TIME										
	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5		ns
	t_f	Output Fall Time			2.5			2.5		ns
CAPACITANCE										
	C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique on a Sample Basis.		4	5		4	5	pF
	C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

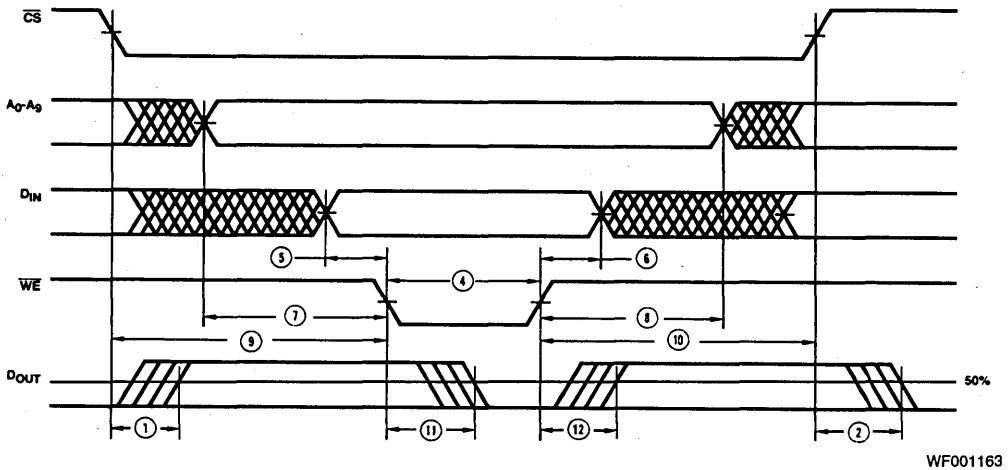
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING CHARACTERISTICS (Military)*

No.	Parameter Symbol	Parameter Description	Test Conditions	Am10470-15			Am10470SA			Am10470A			Units
				Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output		8	10		8	10		10	15	ns
2	t_{RCS}	Chip Select Recovery Time			8	10		8	10		10	15	ns
3	t_{AA}	Address Access Time			12	15		17	20		20	30	ns
WRITE MODE													
4	t_W	Write Pulse Width	$t_{WSA} = t_{WSA}$ (Min.)	15	10		18	14		22	17		ns
5	t_{WSD}	Data Setup Time Prior to Write		3	0		3	0		5	2		ns
6	t_{WHD}	Data Hold Time After Write		3	0		3	0		5	2		ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	3	0		3	0		5	2		ns
8	t_{WHA}	Address Hold Time		3	0		3	0		5	2		ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	3	0		3	0		5	2		ns
10	t_{WHCS}	Chip Select Hold Time After Write		3	0		3	0		5	2		ns
11	t_{WS}	Write Disable Time			8	10		8	10		10	12	ns
12	t_{WR}	Write Recovery Time			8	10		8	10		10	12	ns
RISE TIME AND FALL TIME													
	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
	t_f	Output Fall Time			2.5			2.5			2.5		ns
CAPACITANCE													
	C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique on a Sample Basis.		4	5		4	5		4	5	pF
	C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	

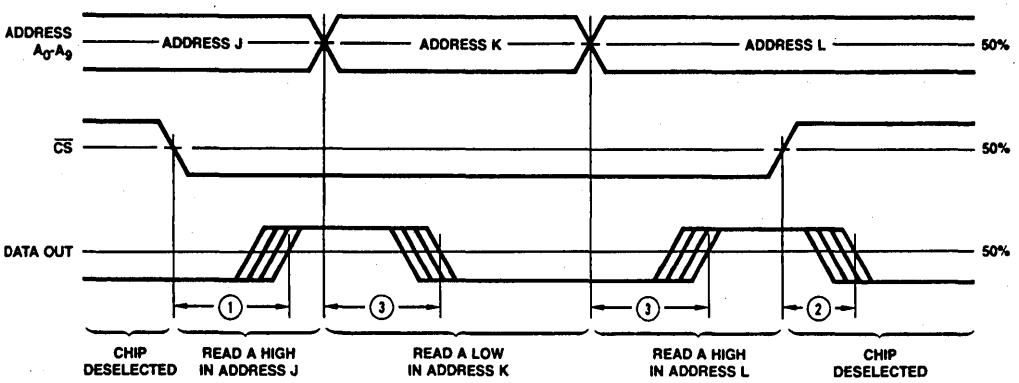
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Cont'd.)



Write Mode

SWITCHING WAVEFORMS



WF001173

Read Mode

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OHC}	1, 2, 3
V_{OLC}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{EE}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACS}	9, 10, 11	7	t_{WSA}	9, 10, 11
2	t_{RCS}	9, 10, 11	8	t_{WHA}	9, 10, 11
3	t_{AA}	9, 10, 11	9	t_{WSCS}	9, 10, 11
4	t_{W}	9, 10, 11	10	t_{WHCS}	9, 10, 11
5	t_{WSD}	9, 10, 11	11	t_{WS}	9, 10, 11
6	t_{WHD}	9, 10, 11	12	t_{WR}	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am100474

1024 x 4 IMOX™ ECL Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (10 ns) — improves system cycle speeds.
- Fully compatible with 100K series ECL logic — no board changes required.
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges.
- Internally voltage-compensated providing flat AC performance.
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature.

GENERAL DESCRIPTION

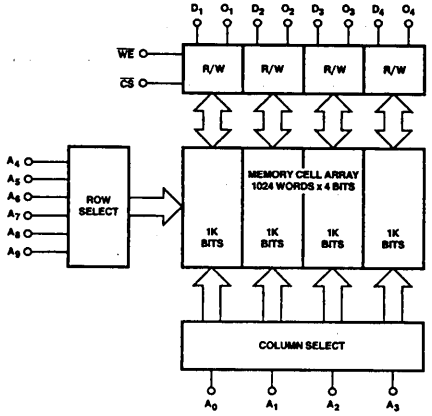
The Am100474-10, Am100474-15 and Am100474-25 are fully decoded 4096-bit ECL RAMs, organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and unterminated OR-tieable emitter follower outputs.

An active LOW write enable ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write enable lines are LOW, the data inputs ($D_1 - D_4$) are written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed word is read out on the noninverting outputs, $O_1 - O_4$.

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000650

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH
L = LOW
X = Don't Care

PRODUCT SELECTOR GUIDE

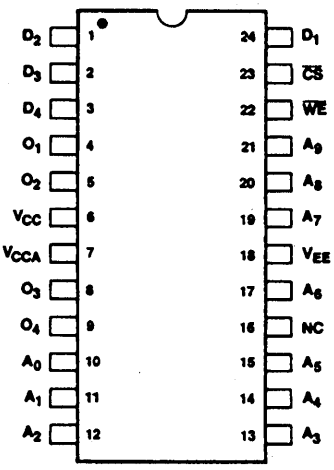
Highlights of Key Performance Parameters (Commercial)

Part Number	Am100474-10	Am100474-15	Am100474-25
Address Access Time (t_{AA})	10 ns	15 ns	25 ns
Write Pulse Width (t_W)	12 ns	15 ns	25 ns
Write Recovery (t_{WR})	14 ns	17 ns	27 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	8 ns	10 ns
Power Supply (I_{EE})	230 mA	200 mA	200 mA

Publication # 03232 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

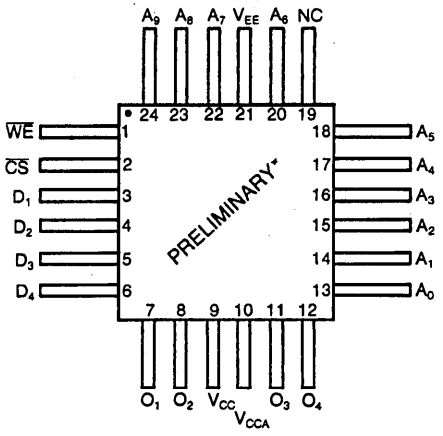
DIP



CD000940

Note: Pin 1 is marked for orientation.

Flatpak

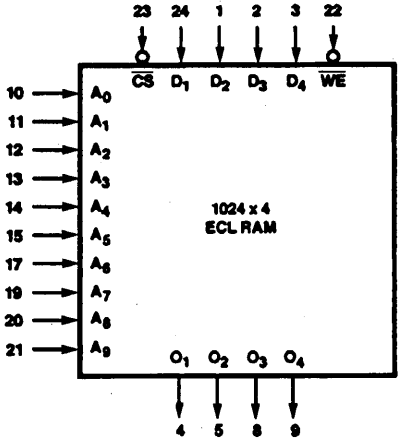


CD006022

*Preliminary. Subject to Change.

3

LOGIC SYMBOL*



LS000262

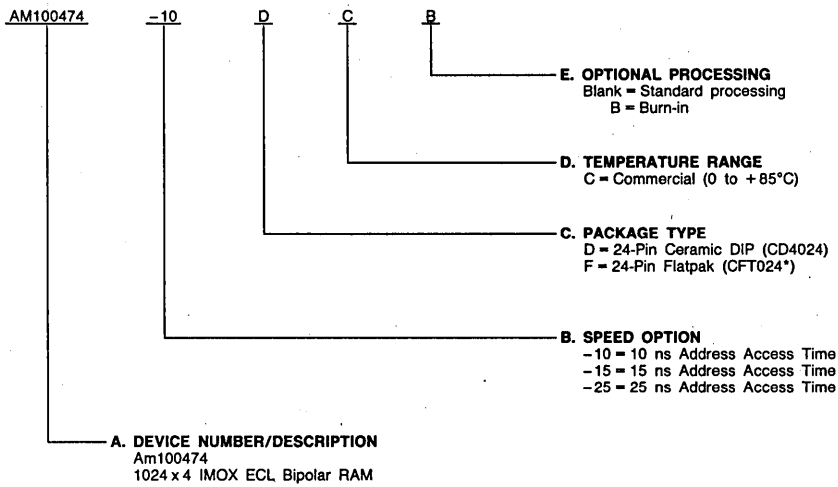
VCC = Pin 6
VCCA = Pin 7
VEE = Pin 18
NC = Pin 16

*Pin numbers apply to DIP.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Preliminary. Subject to Change.

Valid Combinations	
AM100474-10	DC, DCB FC, FCB
AM100474-15	
AM100474-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to
GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (V_{EE} = −4.5 V, V_{CC} = GND (Note 2))

Parameter Symbol	Parameter Description	Test Conditions (Note 2)		B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	−1025		−880	mV
V_{OL}	Output Voltage LOW			−1810		−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$				220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	$V_{IN} = V_{ILB}$		0.5		170	μA
	All Other Inputs			−50			
I_{EE}	Power Supply Current (Pin 18)	All Inputs and Outputs Open	Am100474-10	−230			mA
			Am100474-15/-25	−200			

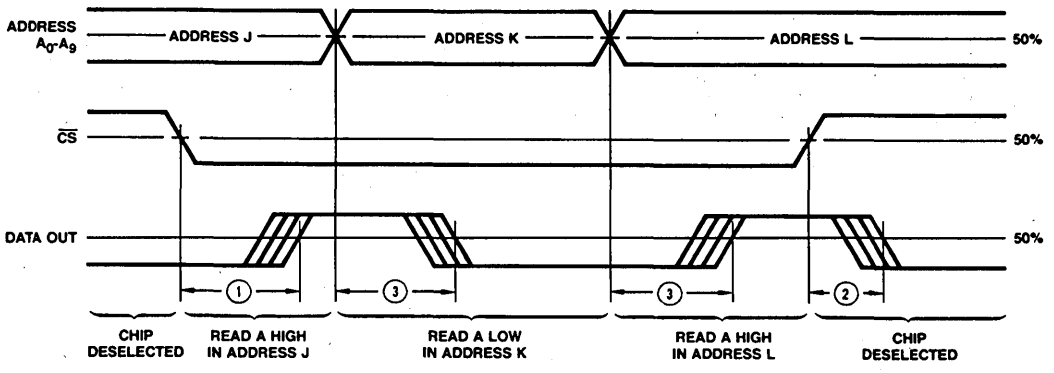
Notes:
1. Typical values are:
   V_{EE} = −4.5 V, $V_{CC} = V_{CCA}$ = GND, T_A = 25°C
2. Output Load = 50 Ω and 30 pF to −2.0 V, T = T_A = 0 to +85°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate resistance values of the package are:
   θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   T = T_C = 0 to +85°C for Flatpak and LCC packages
   θ_{JC} (Junction-to-Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3

SWITCHING CHARACTERISTICS V_{EE} = −4.8 to −4.2 V, V_{CC} = GND (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am100474-10			Am100474-15			Am100474-25			Units
				Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output			8			8			10	ns
2	t_{RCS}	Chip Select Recovery Time				8			8			10	ns
3	t_{AA}	Address Access Time				10			15			25	ns
WRITE MODE													
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	12			15			25			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			2			2			ns
6	t_{WHD}	Data Hold Time After Write		2			2			2			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2			2			2			ns
8	t_{WHA}	Address Hold Time After Write		2			2			2			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			2			2			ns
10	t_{WHCS}	Chip Select Hold Time After Write		2			2			2			ns
11	t_{WS}	Write Disable Time				8			8			10	ns
12	t_{WR}	Write Recovery Time				14			17			27	ns
RISE TIME AND FALL TIME													
13	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
14	t_f	Output Fall Time			2.5			2.5			2.5		
CAPACITANCE													
15	C_{IN}	Input Pin Capacitance	Measured with a pulse technique on sample basis		4			4			4		pF
16	C_{OUT}	Output Pin Capacitance			7			7			7		

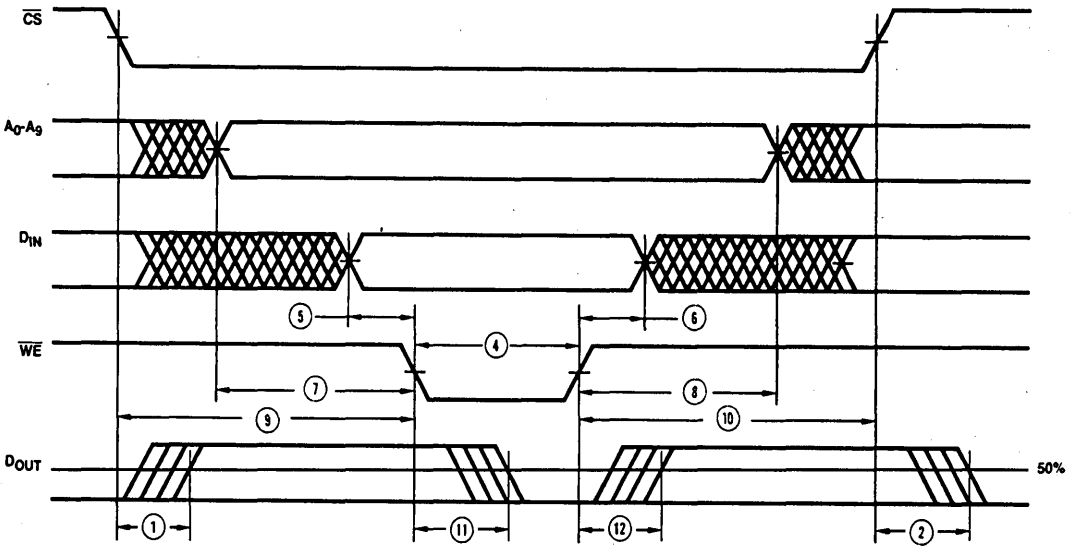
SWITCHING WAVEFORMS (Cont'd.)



WF001173

Read Mode

SWITCHING WAVEFORMS

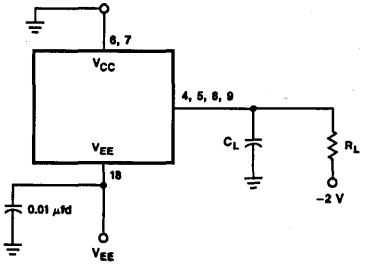


WF001163

Write Mode

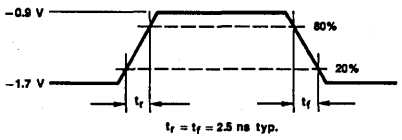
3

SWITCHING TEST CIRCUIT



TC000225

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▨	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)

Am10474

1024 x 4 IMOX™ ECL Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (10 ns) improves system cycle speeds.
- Fully compatible with standard voltage-compensated 10K series ECL — no board changes required.
- Enhanced output voltage level compensation providing 6X improvement in V_{OL} and V_{OH} stability over supply and temperature ranges.
- Internally voltage-compensated providing flat AC performance.
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature.

GENERAL DESCRIPTION

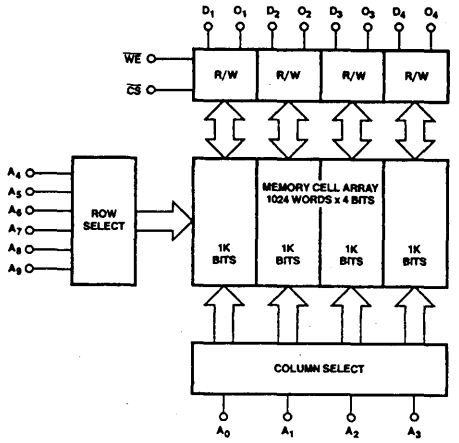
The Am10474-10, Am10474-15 and Am10474-25 are fully decoded 4096-bit ECL RAMs, organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR-tieable emitter follower output.

An active LOW write enable ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write enable lines are LOW, the data inputs ($D_1 - D_4$) are written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed word is read out on the noninverting outputs, $O_1 - O_4$.

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000650

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH
L = LOW
X = Don't Care

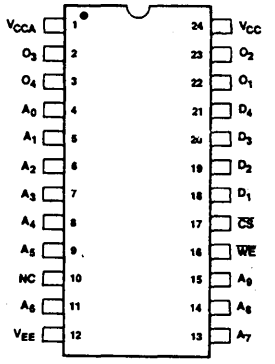
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

Part Number	Am10474-10	Am10474-15	Am10474-25
Address Access Time (t_{AA})	10 ns	15 ns	25 ns
Write Pulse Width (t_W)	12 ns	15 ns	25 ns
Write Recovery (t_{WR})	14 ns	17 ns	27 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	8 ns	10 ns
Power Supply (I_{EE})	230 mA	200 mA	200 mA

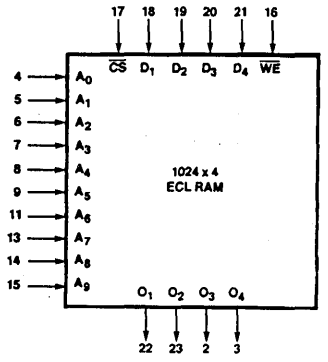
Publication # 03231 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD000931

LOGIC SYMBOL



LS000251

V_{CCA} = Pin 1
V_{CC} = Pin 24
V_{EE} = Pin 12
NC = Pin 10

Note: Pin 1 is marked for orientation.

3

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM10474 -10 D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

C. PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD4024)

B. SPEED OPTION
-10 = 10 ns Address Access Time
-15 = 15 ns Address Access Time
-25 = 25 ns Address Access Time

A. DEVICE NUMBER/DESCRIPTION
Am10474
1024 x 4 IMOX ECL Bipolar RAM

Valid Combinations	
AM10474-10	DC, DCB
AM10474-15	
AM10474-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.46 V to −4.94 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (Commercial) $V_{EE} = -5.2$ V, V_{CC} = GND (Note 2)

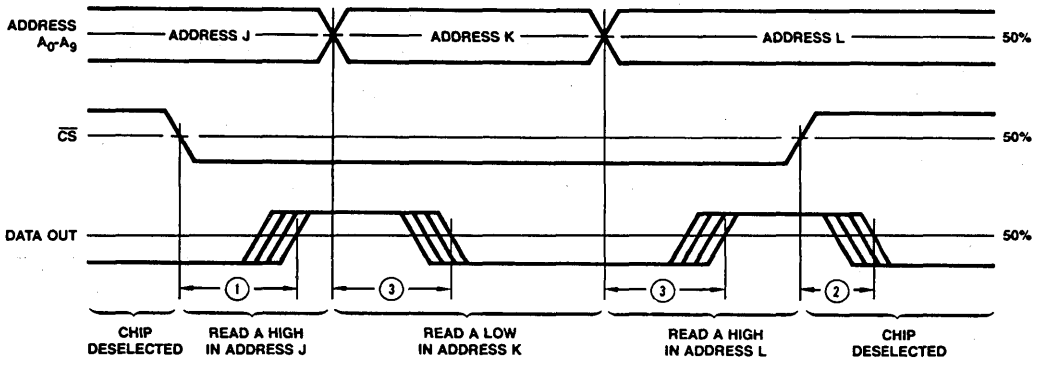
Parameter Symbol	Parameter Description	Test Conditions (Note 2)			B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	T = 0°C	−1000		−840	mV
				T = +25°C	−960		−810	
				T = +75°C	−900		−720	
V_{OL}	Output Voltage LOW			T = 0°C	−1870		−1665	mV
				T = +25°C	−1850		−1650	
				T = +75°C	−1830		−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T = 0°C	−1020			mV
				T = +25°C	−980			
				T = +75°C	−920			
V_{OLC}	Output Voltage LOW			T = 0°C			−1645	mV
				T = +25°C			−1630	
				T = +75°C			−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T = 0°C	−1145		−840	mV
				T = +25°C	−1105		−810	
				T = +75°C	−1045		−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T = 0°C	−1870		−1490	mV
				T = +25°C	−1850		−1475	
				T = +75°C	−1830		−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T = 0 to +75°C			220	µA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	$V_{IN} = V_{ILB}$		T = 0 to +75°C	0.5		170	µA
	All Other Inputs				−50			
I_{EE}	Power Supply Current (Pin 12)	All Inputs and Outputs Open	Am10474-10	T = 0 to +75°C	−230			mA
			Am10474-15/-25		−200			

Notes: 1. Typical values are:
$V_{EE} = -5.2$ V, $V_{CC} = V_{CCA}$ = GND, T_A = 25°C
2. Output Load = 50 Ω and 30 pF to −2.0 V, T = T_A = 0 to +75°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate thermal resistance values of the package are:
θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T = T_C = 0 to +75°C for Flatpak and LCC packages
θ_{JC} (Junction-to-Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
5. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed θ = 25°C/w (approximately)

SWITCHING CHARACTERISTICS (Commercial) V_{EE} = −5.46 V to −4.94 V, V_{CC} = GND (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am10474-10 Min.	Am10474-10 Typ. (Note 1)	Am10474-10 Max.	Am10474-15 Min.	Am10474-15 Typ. (Note 1)	Am10474-15 Max.	Am10474-25 Min.	Am10474-25 Typ. (Note 1)	Am10474-25 Max.	Units
READ MODE													
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output			8			8			10	ns
2	t_{RCS}	Chip Select Recovery Time				8			8			10	ns
3	t_{AA}	Address Access Time				10			15			25	ns
WRITE MODE													
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	12			15			25			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			2			2			ns
6	t_{WHD}	Data Hold Time After Write		2			2			2			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2			2			2			ns
8	t_{WHA}	Address Hold Time After Write		2			2			2			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			2			2			ns
10	t_{WHCS}	Chip Select Hold Time After Write		2			2			2			ns
11	t_{WS}	Write Disable Time				8			8			10	ns
12	t_{WR}	Write Recovery Time				14			17			27	ns
RISE TIME AND FALL TIME													
13	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5			2.5		ns
14	t_f	Output Fall Time			2.5			2.5			2.5		
CAPACITANCE													
15	C_{IN}	Input Pin Capacitance	Measured with a pulse technique on sample basis		4			4			4		pF
16	C_{OUT}	Output Pin Capacitance			7			7			7		

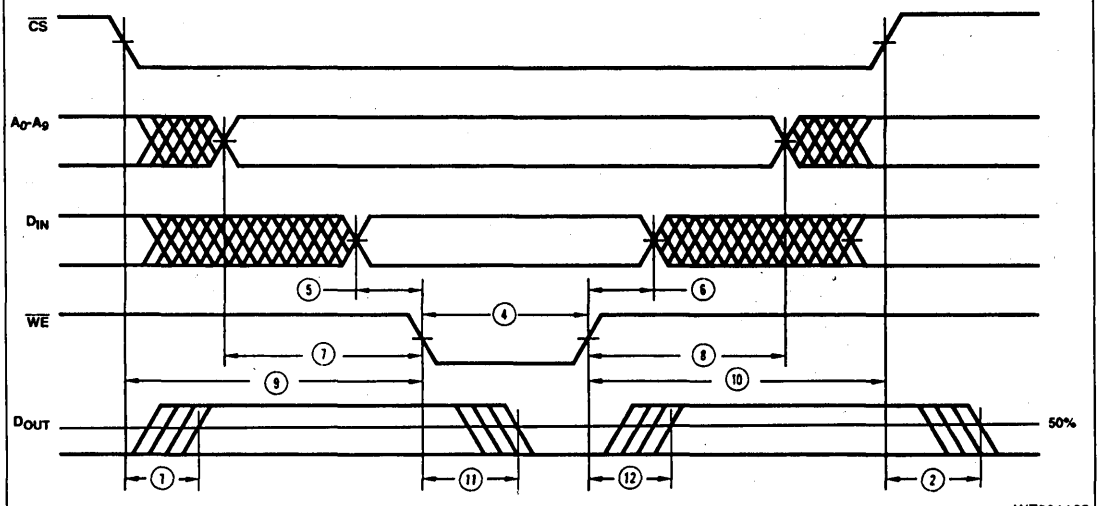
SWITCHING WAVEFORMS (Cont'd.)



WF001173

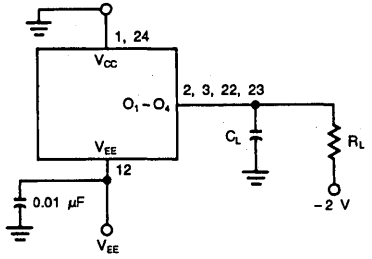
Read Mode

SWITCHING WAVEFORMS

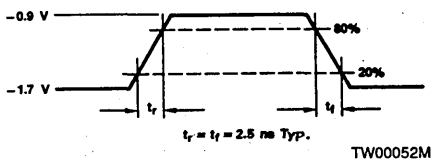


Write Mode

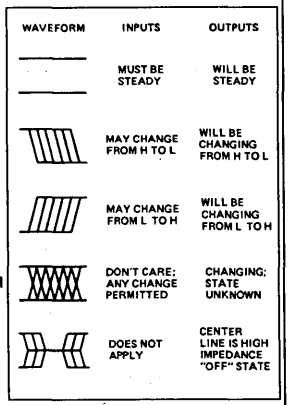
SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORM



KEY TO SWITCHING WAVEFORM



$R_L = 50\ \Omega$ termination of measurement system
$C_L = 30$ pF (including stray jig capacitance)

Am100480

16,384 x 1 IMOX™ ECL Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (15 ns) — improves system cycle speeds.
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges.
- Internally voltage and temperature compensated providing flat AC performance.
- Fully compatible with 100K series ECL logic – no board changes required.
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature.

GENERAL DESCRIPTION

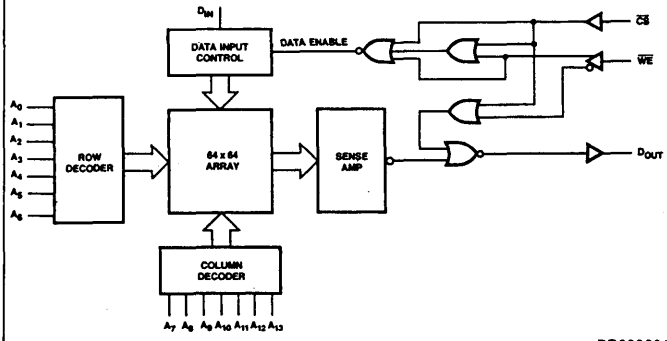
The Am100480-15 and Am100480-25 are fully decoded 16,384-bit ECL RAMs organized 16,384 words by one bit. Bit selection is achieved by means of a 14-bit address, A_0 through A_{13}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write enable ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write enable lines are LOW, the data input (D_{IN}) is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed bit is read out on the noninverting output (D_{OUT}).

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000661

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH
L = LOW
X = Don't Care

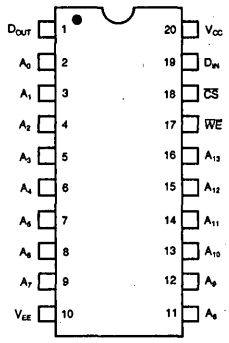
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

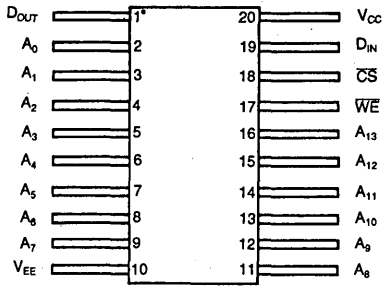
Part Number	Am100480-15	Am100480-25
Address Access Time (t_{AA})	15 ns	25 ns
Write Pulse Width (t_W)	15 ns	25 ns
Write Recovery (t_{WR})	18 ns	20 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	10 ns
Power Supply (I_{EE})	220 mA	200 mA

Publication # 06875 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



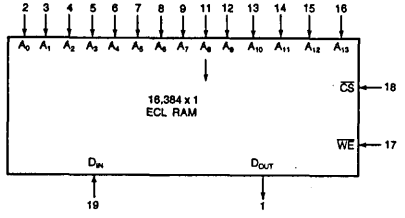
CD006040



CD006050

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS001902

V_{CC} = Pin 20
V_{EE} = Pin 10

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM100480 -15 D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +85°C)

C. PACKAGE TYPE
D = 20-Pin Ceramic DIP (CD 020)
F = 20-Pin Flatpak (CF 020)

B. SPEED OPTION
-15 = 15 ns
-25 = 25 ns

A. DEVICE NUMBER/DESCRIPTION
Am100480
16,384 x 1 IMOX ECL Bipolar RAM

Valid Combinations	
AM100480-15	DC, DCB
AM100480-25	FC, FCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature ..... 0 to +85°C
Supply Voltage ..... −5.7 V to −4.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS V_{EE} = −4.5 V, V_{CC} = GND (Note 2)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)		B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	−1025	−955	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1715	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$				220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	$V_{IN} = V_{ILB}$		0.5		170	μA
	All Other Inputs			−50			
I_{EE}	Power Supply Current (Pin 10)	All Inputs and Outputs Open	Am100480-15	−220			mA
			Am100480-25	−200			

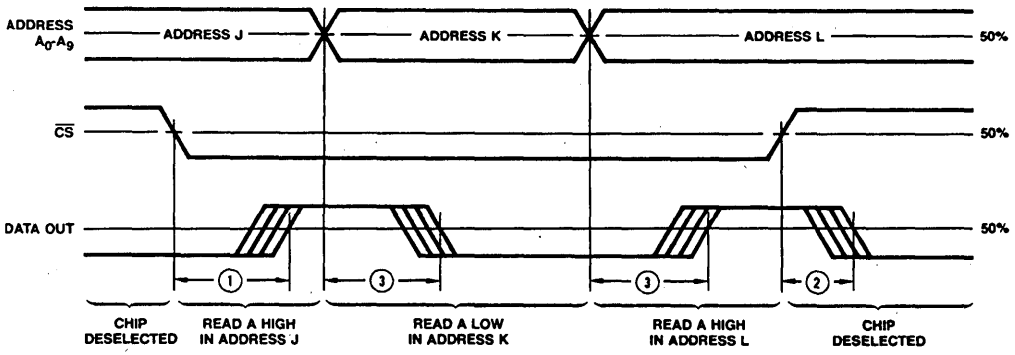
Notes: 1. Typical values are:
V_{EE} = −4.5 V, V_{CC} = GND, T_A = 25°C
2. Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0 to +85°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate resistance values of the package are:
θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
T_C = 0 to +85°C for Flatpak and LCC packages
θ_{JC} (Junction-to-Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3

SWITCHING CHARACTERISTICS V_{EE} = −4.8 V to −4.2 V, V_{CC} = GND (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am100480-15			Am100480-25			Units
				Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
READ MODE										
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output			8			10	ns
2	t_{RCS}	Chip Select Recovery Time				8			10	
3	t_{AA}	Address Access Time				15			25	
WRITE MODE										
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	15			25			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			5			ns
6	t_{WHD}	Data Hold Time After Write		3			5			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2			5			ns
8	t_{WHA}	Address Hold Time After Write		3			5			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			5			ns
10	t_{WHCS}	Chip Select Hold Time After Write		3			5			ns
11	t_{WS}	Write Disable Time				8			10	ns
12	t_{WR}	Write Recovery Time				18			20	ns
RISE TIME AND FALL TIME										
13	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5		ns
14	t_f	Output Fall Time			2.5			2.5		
CAPACITANCE										
15	C_{IN}	Input Pin Capacitance	Measure with a pulse technique on sample basis		4			4		pF
16	C_{OUT}	Output Pin Capacitance			7			7		

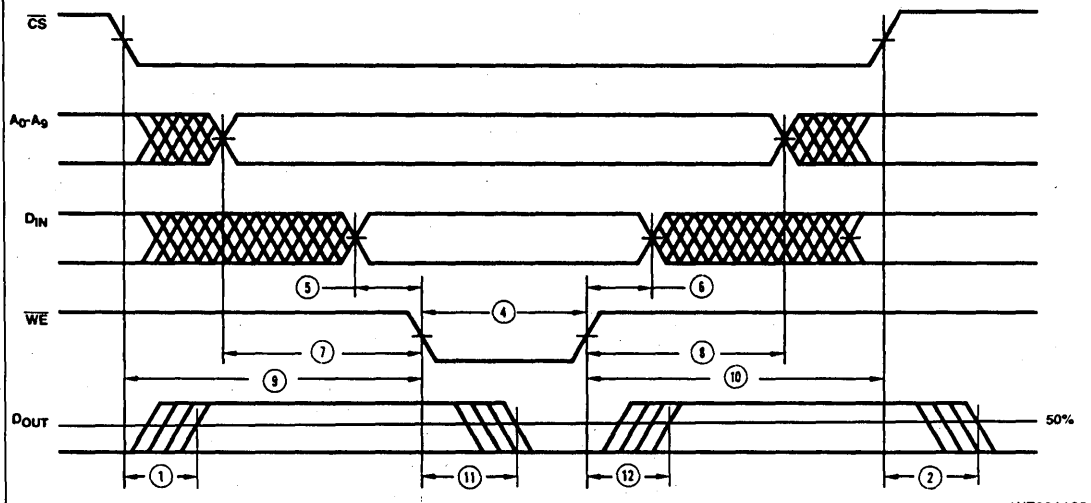
SWITCHING WAVEFORMS (Cont'd.)



WF001173

Read Mode

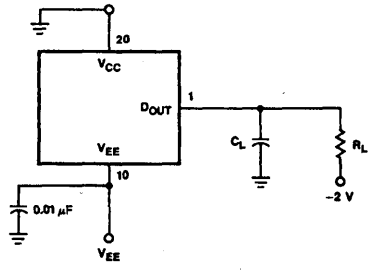
SWITCHING WAVEFORMS



WF001163

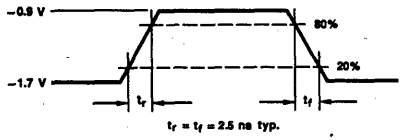
Write Mode

SWITCHING TEST CIRCUIT



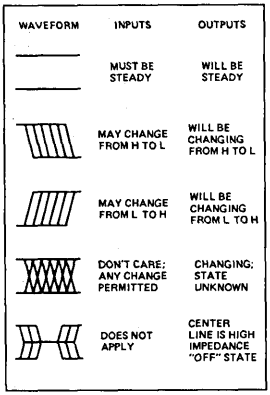
TC000223

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING WAVEFORMS



KS000010

R_L = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)

Am10480

16,384 x 1 IMOX™ ECL Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (15 ns) — improves system cycle speeds.
- Fully compatible with standard voltage compensated 10K series ECL — no board changes required.
- Internally voltage compensated providing flat AC performance.
- Enhanced output voltage level compensation providing 6X improvement in V_{OL} and V_{OH} stability over supply and temperature ranges.
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature.

GENERAL DESCRIPTION

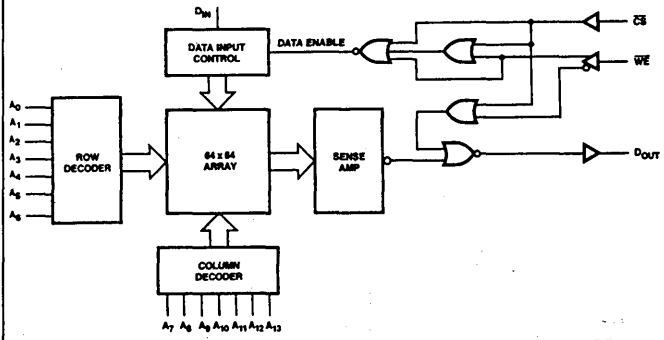
The Am10480-15 and Am10480-25 are fully decoded 16,384-bit ECL RAMs organized 16,384 words by one bit. Bit selection is achieved by means of a 14-bit address, A_0 through A_{13}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write enable ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write enable lines are LOW, the data input (D_{IN}) is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write enable line HIGH. The information stored in the addressed bit is read out on the noninverting output (D_{OUT}).

During the writing operation, or when the chip select line is HIGH, the output of the memory goes to a LOW state.

BLOCK DIAGRAM



BD000661

MODE SELECT TABLE

Input			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH
L = LOW
X = Don't Care

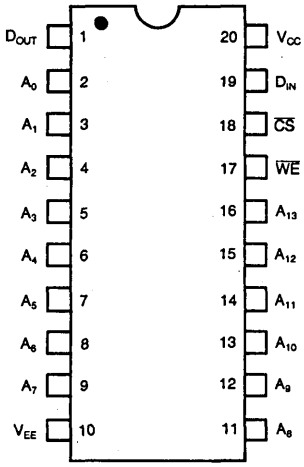
PRODUCT SELECTOR GUIDE

Highlights of Key Performance Parameters (Commercial)

Part Number	Am10480-15	Am10480-25
Address Access Time (t_{AA})	15 ns	25 ns
Write Pulse Width (t_W)	15 ns	25 ns
Write Recovery (t_{WR})	18 ns	20 ns
Chip Select Access/ Recovery and Write Disable Times (t_{ACS}, t_{RCS}, t_{WS})	8 ns	10 ns
Power Supply (I_{EE})	220 mA	200 mA

Publication # 06874 Rev. B Amendment /0
Issue Date: May 1986

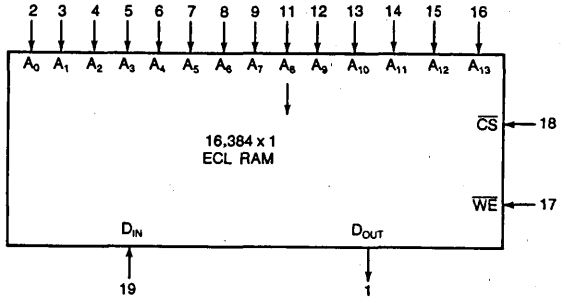
CONNECTION DIAGRAM
Top View



CD006040

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS001902

V_{CC} = Pin 20
V_{EE} = Pin 10

3

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM10480 -15 D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

C. PACKAGE TYPE
D = 20-Pin Ceramic DIP (CD 020)

B. SPEED OPTION
-15 = 15 ns
-25 = 25 ns

A. DEVICE NUMBER/DESCRIPTION
Am10480
16,384 x 1 IMOX ECL Bipolar RAM

Valid Combinations	
AM10480-15	DC, DCB
AM10480-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature ..... 0 to +75°C
Supply Voltage ..... −5.46 V to −4.94 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (Commercial) V_{EE} = −5.2 V, V_{CC} = GND (Note 2)

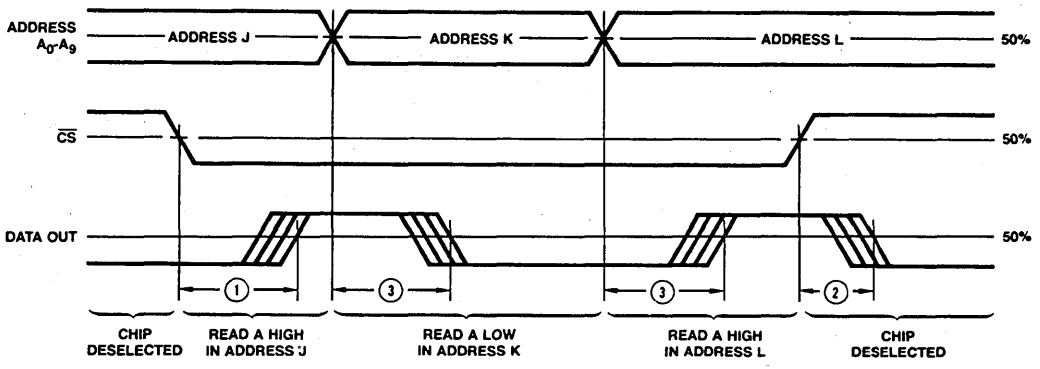
Parameter Symbol	Parameter Description	Test Conditions (Note 2)			B (Note 3)	Typ. (Note 1)	A (Note 3)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V	T = 0°C	−1000		−840	mV
				T = +25°C	−960		−810	
				T = +75°C	−900		−720	
V_{OL}	Output Voltage LOW			T = 0°C	−1870		−1665	mV
				T = +25°C	−1850		−1650	
				T = +75°C	−1830		−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T = 0°C	−1020			mV
				T = +25°C	−980			
				T = +75°C	−920			
V_{OLC}	Output Voltage LOW			T = 0°C			−1645	mV
				T = +25°C			−1630	
				T = +75°C			−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Inputs Voltage HIGH for All Inputs (Note 4)		T = 0°C	−1145		−840	mV
				T = +25°C	−1105		−810	
				T = +75°C	−1045		−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T = 0°C	−1870		−1490	mV
				T = +25°C	−1850		−1475	
				T = +75°C	−1830		−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T = 0 to +75°C			220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$)	$V_{IN} = V_{ILB}$		T = 0 to +75°C	0.5		170	μA
	All Other Inputs				−50			
I_{EE}	Power Supply Current (Pin 10)	All Inputs and Outputs Open	Am10480-15	T = 0 to +75°C	−220			mA
			Am10480-25		−200			

Notes:
1. *Typical values are:* V_{EE} = −5.2 V, V_{CC} = GND, T_A = 25°C
2. Output Load = 50 Ω and 30 pF to −2.0 V, T = T_A = 0 to +75°C for DIPs. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Approximate thermal resistance values of the package are:
   θ_{JA} (Junction-to-Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction-to-Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   T = T_C = 0 to +75°C for Flatpak and LCC packages θ_{JC} (Junction-to-Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS (Commercial) $V_{EE} = -5.46$ to -4.94 V, V_{CC} = GND (Note 2)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am10480-15 Min.	Am10480-15 Typ. (Note 1)	Am10480-15 Max.	Am10480-25 Min.	Am10480-25 Typ. (Note 1)	Am10480-25 Max.	Units
READ MODE										
1	t_{ACS}	Chip Select Access Time	Measured at 50% of input to 50% of output			8			10	ns
2	t_{RCS}	Chip Select Recovery Time				8			10	
3	t_{AA}	Address Access Time				15			25	
WRITE MODE										
4	t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min.)	15			25			ns
5	t_{WSD}	Data Setup Time Prior to Write		2			5			ns
6	t_{WHD}	Data Hold Time After Write		3			5			ns
7	t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min.)	2			5			ns
8	t_{WHA}	Address Hold Time After Write		3			5			ns
9	t_{WSCS}	Chip Select Setup Time Prior to Write	Measured at 50% of input to 50% of output	2			5			ns
10	t_{WHCS}	Chip Select Hold Time After Write		3			5			ns
11	t_{WS}	Write Disable Time				8			10	ns
12	t_{WR}	Write Recovery Time				18			20	ns
RISE TIME AND FALL TIME										
13	t_r	Output Rise Time	Measured between 20% and 80% points		2.5			2.5		ns
14	t_f	Output Fall Time			2.5			2.5		
CAPACITANCE										
15	C_{IN}	Input Pin Capacitance	Measure with a pulse technique on sample basis		4			4		pF
16	C_{OUT}	Output Pin Capacitance			7			7		

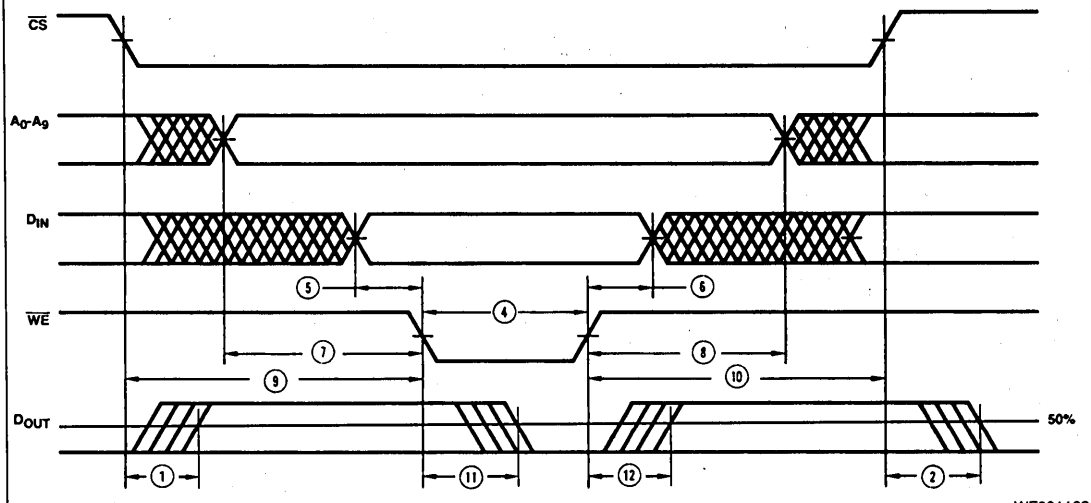
SWITCHING WAVEFORMS (Cont'd.)



WF001173

Read Mode

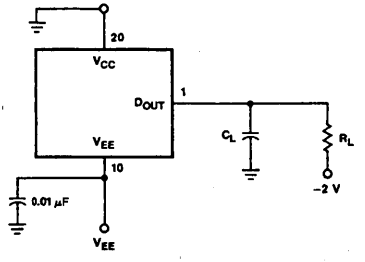
SWITCHING WAVEFORMS



WF001163

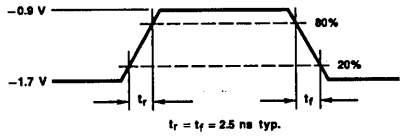
Write Mode

SWITCHING TEST CIRCUIT



TC000223

SWITCHING TEST WAVEFORM



TW000310

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

$R_L = 50\ \Omega$ termination of measurement system
$C_L = 30$ pF (including stray jig capacitance)

Am21L50

512 x 9 TTL Low-Power Tag Buffer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 45-ns address-to-comparator output (MATCH)
- Replaces six or more integrated circuits with a single device
- On-chip parity generator and checker
- One-third power consumption of the Am2150
- Fully TTL compatible
- Integrated reset feature

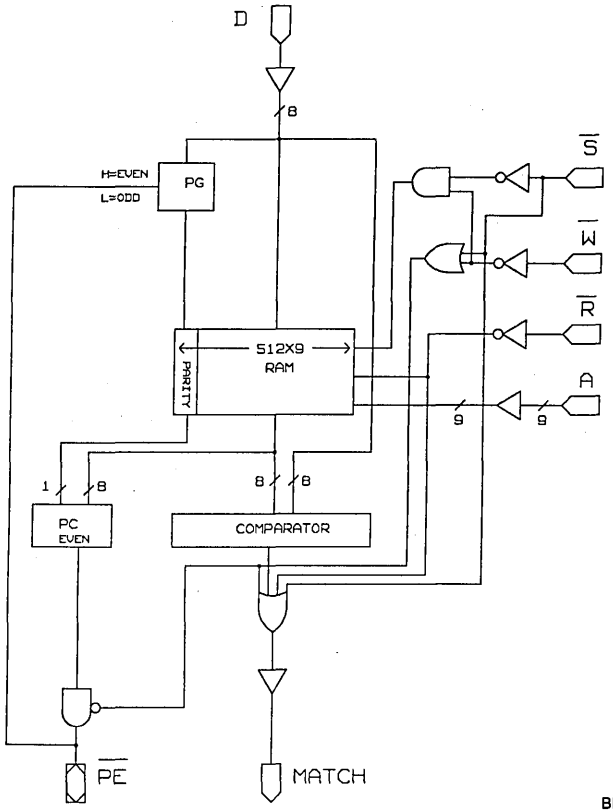
GENERAL DESCRIPTION

The Am21L50 Low-Power Tag Buffer combines a 512 x 9 memory with a comparator. An internal parity generator and parity checker guarantee that no misoperation occurs.

The device has three operational modes: Compare, Write, and Reset. In Compare mode, data is compared to the contents of an address location. Write mode is used to store data. Reset mode is used to clear a single 'valid bit' stream.

The Tag Buffer is designed to be used in a cache memory system for the translation of virtual addresses to physical addresses. The device can also be used in the directory and data cache. It offers state-of-the-art technology performance, while combining the functions of six or more integrated circuits into a single device.

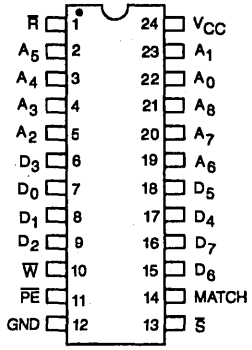
BLOCK DIAGRAM



BD005901

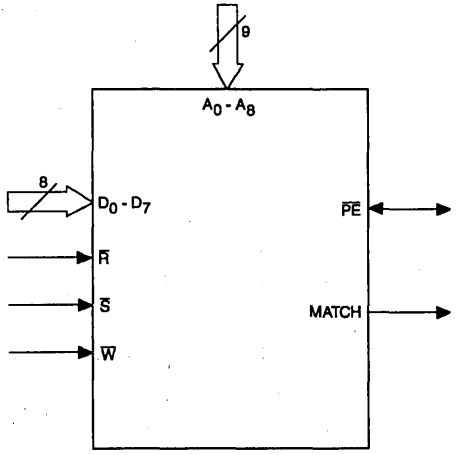
Publication # 08001 | Rev. B | Amendment /0
Issue Date: June 1986

CONNECTION DIAGRAM
Top View



CD009153

LOGIC SYMBOL



LS002202

V_{CC} = Positive Power Supply
GND = Ground

PIN DESCRIPTION

A_0–A_8 Address (Inputs)
Identifies memory locations.

D_0–D_7 Data (Inputs)
During Compare cycle, eight bits of data are compared with address location given by A_0–A_8 for equality. The result is indicated on the Comparator output pin, MATCH. When $\overline{W}$ is LOW, data is written into the address location given by A_0–A_8.

$\overline{R}$ Reset (Input, Active LOW)
Resets D_3 to zero (all 512 locations).

$\overline{S}$ Chip Select (Input, Active LOW)
When $\overline{S}$ is LOW, the device is activated. A HIGH on this input will disable the chip and force $\overline{PE}$ and MATCH outputs LOW, allowing easy vertical expansion.

$\overline{W}$ Write Enable (Input, Active LOW)
Must be LOW to write Data (D_0–D_7) into location given by A_0–A_8. MATCH is output HIGH during Write cycle.

MATCH Comparator Match (Output, Active HIGH)
HIGH when Data (D_0–D_7) equals content of memory location specified by A_0–A_8. LOW when mismatch occurs.

$\overline{PE}$ Parity Error (Input/Output, Active LOW)
LOW when the nine bits of internal data do not constitute even parity. If held LOW during Write Cycle, odd parity will be generated, forcing a parity error for that address upon output.

FUNCTIONAL DESCRIPTION

The Am21L50 Low-Power Tag Buffer has three modes of operation: Compare, Write, and Reset. These modes are described as follows.

Compare Mode

The eight bits of Data inputs are compared with the content of a given memory location for equality. The nine address inputs define each memory location. In this mode, $\overline{W}$ and $\overline{R}$ inputs are HIGH, and $\overline{S}$ is LOW. If the eight bits of Data inputs are exactly the same as the eight bits of data in the given memory location, the MATCH output will be HIGH. If not, the MATCH output will be LOW. The parity bit is not compared.

Write Mode

The eight bits of data inputs and the one bit of parity are written into the RAM array when both $\overline{S}$ and $\overline{W}$ are LOW, and $\overline{R}$ is HIGH. The MATCH output is forced HIGH (the MATCH output is associated with the output enable of the data cache). Holding the Parity Error ($\overline{PE}$) LOW forces a Parity Error to be output during the later compare cycles.

Reset Mode

When $\overline{R}$ = LOW, $\overline{S}$ = LOW, and $\overline{W}$ = HIGH, a dedicated section of the entire array, D_3, is reset to LOW. The $\overline{PE}$ output is forced LOW during reset. The MATCH output is forced HIGH. All 512 D_3 data bits are reset to a low state. The other seven bits in each address location may change to an undetermined state (HIGH or LOW).

3

TABLE 1. FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	
$\overline{S}$	$\overline{W}$	$\overline{R}$	$\overline{PE}$ (Note 1)	MATCH	DESCRIPTION
H	X	X	Input Output Disabled	H (Forced)	Chip Disabled
L	H	H	Output H = No Parity Error L = Parity Error	H = MATCH L = MISS	Compare
L	H	L	Output L	H (Forced)	Reset
L	L	H	Input H = Even Parity L = Odd Parity	H (Forced)	Write
L	L	L	Input Output Disabled	H (Forced)	Illegal

Note: 1. $\overline{PE}$ is an open-collector output, requiring an external Pull-up Resistor.

Key: H = HIGH
L = LOW
X = Don't Care

TABLE 2. COMPARE CYCLE OUTPUT DESCRIPTION

MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error or After Reset
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 to V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH} (MATCH)	Output HIGH Voltage	I_{OH} = −2 mA	2.4		V
V_{OL} (MATCH)	Output LOW Voltage	I_{OL} = 18 mA		0.45	V
V_{OL} ($\overline{PE}$)	Output LOW Voltage	I_{OL} = 12 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
V_{CL}	Input Clamp Voltage	I_{IN} = −10 mA		−1.5	V
I_{IL}	Input LOW Current	V_{IN} = 0 to 5.5 V		100	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V		40	μA
I_{SC} (Note 1)	Output Short-Circuit Current	V_{OUT} =0.0V		−75	mA
I_{CC}	Supply Current			80	mA

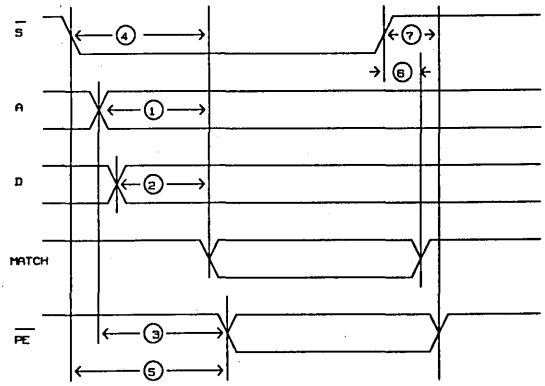
Note: 1. No more than one output should be short circuited at a time. The duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

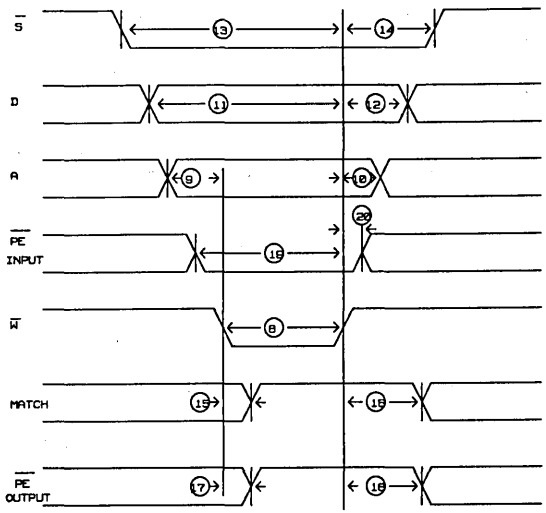
No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
Compare Mode					
1	t_{AVMV}	Address to MATCH		45.0	ns
2	t_{DVMV}	Data to MATCH		25.0	ns
3	t_{AVPV}	Address to $\overline{PE}$		55.0	ns
4	t_{SLMV}	$\overline{S}$ to MATCH		25.0	ns
5	t_{SLPV}	$\overline{S}$ to $\overline{PE}$		25.0	ns
6	t_{SHMH}	$\overline{S}$ to MATCH Recovery		25.0	ns
7	t_{SHPH}	$\overline{S}$ to $\overline{PE}$ Recovery		25.0	ns
Write Mode					
8	t_{WLWH}	Write Pulse Width	45.0		ns
9	t_{AVWL}	Address Setup	5.0		ns
10	t_{WHAX}	Address to $\overline{W}$ Hold	5.0		ns
11	t_{DVWH}	Data to $\overline{W}$ Setup	40.0		ns
12	t_{WHDX}	Data to $\overline{W}$ Hold	5.0		ns
13	t_{SLWH}	$\overline{S}$ to Setup	40.0		ns
14	t_{WHSH}	$\overline{S}$ to Select Hold	5.0		ns
15	t_{WLMH}	$\overline{W}$ to MATCH		20.0	ns
16	t_{WHMV}	Write Recovery (MATCH)		45.0	ns
17	t_{WLPH}	$\overline{W}$ to $\overline{PE}$		20.0	ns
18	t_{WHPV}	Write Recovery ($\overline{PE}$)		45.0	ns
19	t_{PVWH}	$\overline{PE}$ Input to $\overline{W}$ Setup		40.0	ns
20	t_{WHPH}	$\overline{PE}$ Input to $\overline{W}$ Hold		5.0	ns
Reset Mode					
21	t_{RLRH}	$\overline{R}$ Pulse Width	60.0		ns
22	t_{SLRL}	$\overline{S}$ to $\overline{R}$ Setup	5.0		ns
23	t_{RHSH}	$\overline{S}$ to $\overline{R}$ Hold	5.0		ns
24	t_{WHRL}	$\overline{W}$ to $\overline{R}$ Setup	5.0		ns
25	t_{RHWL}	$\overline{W}$ to $\overline{R}$ Hold	5.0		ns
26	t_{RLMH}	$\overline{R}$ to MATCH HIGH		15.0	ns
27	t_{RHMX}	$\overline{R}$ to MATCH Recovery		40.0	ns

Notes: 1. All Switching Characteristics are measured at 50% of input to valid output. Both input and output timings are referenced to 1.5 V.

SWITCHING WAVEFORMS (Cont'd)

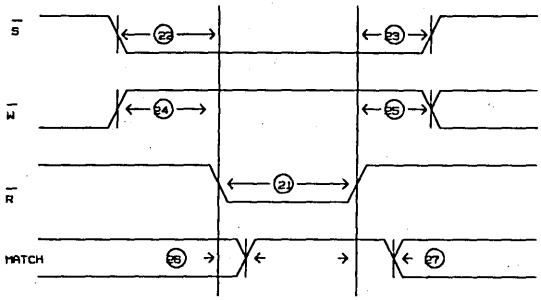


Compare Mode



Write Mode

SWITCHING WAVEFORMS



Reset Mode

Am2150

512 x 9 TTL Tag Buffer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast address to comparator output (MATCH)
- Replaces six or more integrated circuits with a single device
- On-chip parity generator and checker
- Easy horizontal and vertical expansion
- Fully TTL compatible
- Integrated reset feature
- 24-pin Ceramic DIP (300 Mil) and Flatpack packages

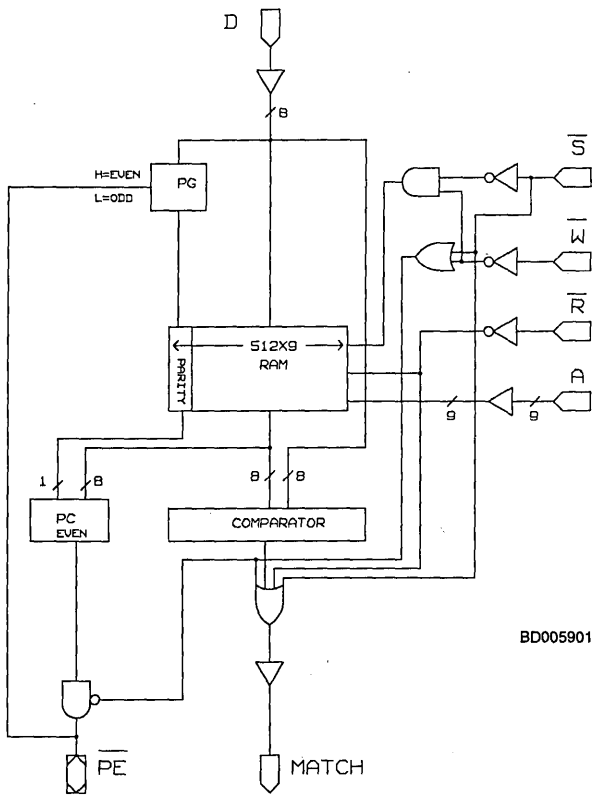
GENERAL DESCRIPTION

The Am2150 Tag Buffer combines a 512 x 9 memory with a comparator. An internal parity generator and parity checker guarantee that no misoperation occurs.

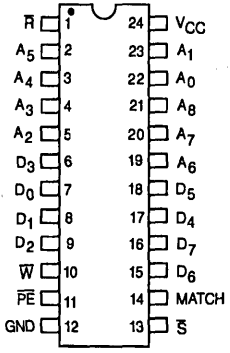
The device has three operational modes: Compare, Write, and Reset. In Compare mode, data is compared to the contents of an address location. Write mode is used to store data. Reset mode is used to clear a single 'valid bit' stream.

The Tag Buffer is designed to be used in a cache memory system for the translation of virtual addresses to physical addresses. The device can also be used in the directory and data cache. It offers state-of-the-art technology performance, while combining the functions of six or more integrated circuits into a single device.

BLOCK DIAGRAM

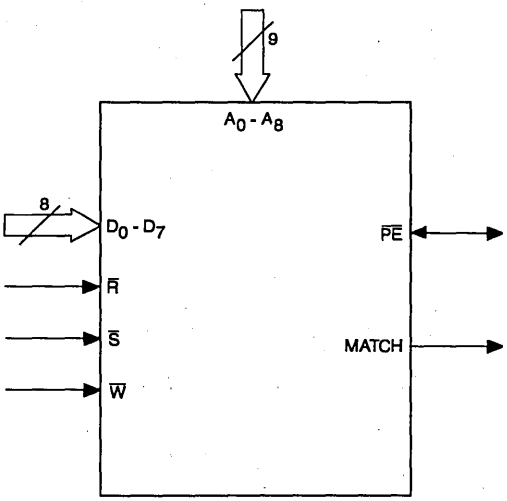


CONNECTION DIAGRAM
Top View



CD009153

LOGIC SYMBOL



LS002202

V_{CC} = Positive Power Supply
GND = Ground

PIN DESCRIPTION

A_0–A_8 Address (Inputs)
Identifies memory locations.

D_0–D_7 Data (Inputs)
During Compare cycle, eight bits of data are compared with address location given by A_0–A_8 for equality. The result is indicated on the Comparator output pin, MATCH. When $\overline{W}$ is LOW, data is written into the address location given by A_0–A_8.

$\overline{R}$ $\overline{\text{Reset}}$ (Input, Active LOW)
Resets D_3 to zero (all 512 locations).

$\overline{S}$ $\overline{\text{Chip Select}}$ (Input, Active LOW)
When $\overline{S}$ is LOW, the device is activated. A HIGH on this input will disable the chip and force $\overline{PE}$ and MATCH outputs HIGH, allowing easy vertical expansion.

$\overline{W}$ $\overline{\text{Write Enable}}$ (Input, Active LOW)
Must be LOW to write Data (D_0–D_7) into location given by A_0–A_8. MATCH is output HIGH during Write cycle.

MATCH Comparator Match (Output, Active HIGH)
HIGH when Data (D_0–D_7) equals content of memory location specified by A_0–A_8. LOW when mismatch occurs.

$\overline{PE}$ $\overline{\text{Parity Error}}$ (Input/Output, Active LOW)
LOW when the nine bits of internal data do not constitute even parity. If held LOW during Write Cycle, odd parity will be generated, forcing a parity error for that address upon output.

FUNCTIONAL DESCRIPTION

The Am2150 Tag Buffer has three modes of operation: Compare, Write, and Reset. These modes are described as follows.

Compare Mode

The eight bits of Data inputs are compared with the content of a given memory location for equality. The nine address inputs define each memory location. In this mode, $\overline{W}$ and $\overline{R}$ inputs are HIGH, and $\overline{S}$ is LOW. If the eight bits of Data inputs are exactly the same as the eight bits of data in the given memory location, the MATCH output will be HIGH. If not, the MATCH output will be LOW. The parity bit is not compared.

Write Mode

The eight bits of data inputs and the one bit of parity are written into the RAM array when both $\overline{S}$ and $\overline{W}$ are LOW, and $\overline{R}$ is HIGH. The MATCH output is forced HIGH (the MATCH output is associated with the output enable of the data cache). Holding the Parity Error ($\overline{PE}$) LOW forces a Parity Error to be output during the later compare cycles.

Reset Mode

When $\overline{R}$ = LOW, $\overline{S}$ = LOW, and $\overline{W}$ = HIGH, a dedicated section of the entire array, D_3, is reset to LOW. The $\overline{PE}$ output is forced LOW during reset. The MATCH output is forced HIGH. All 512 D_3 data bits are reset to a low state. The other seven bits in each address location may change to an undetermined state (HIGH or LOW).

TABLE 1. FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	
$\overline{S}$	$\overline{W}$	$\overline{R}$	$\overline{PE}$ (Note 1)	MATCH	DESCRIPTION
H	X	X	Input Output Disabled	H (Forced)	Chip Disabled
L	H	H	Output H = No Parity Error L = Parity Error	H = MATCH L = MISS	Compare
L	H	L	Output L	H (Forced)	Reset
L	L	H	Input H = Even Parity L = Odd Parity	H (Forced)	Write
L	L	L	Input Output Disabled	H (Forced)	Illegal

Note: 1. $\overline{PE}$ is an open-collector output, requiring an external pull-up resistor.

Key: H = HIGH
L = LOW
X = Don't Care

TABLE 2. COMPARE CYCLE OUTPUT DESCRIPTION

MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error or After Reset
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 to V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH} (MATCH)	Output HIGH Voltage	I_{OH} = −2 mA	2.4		V
V_{OL} (MATCH)	Output LOW Voltage	I_{OL} = 36 mA		0.45	V
V_{OL} ($\overline{PE}$)	Output LOW Voltage	I_{OL} = 24 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
V_{CL}	Input Clamp Voltage	I_{IN} = −10 mA		−1.5	V
I_{IL}	Input LOW Current	V_{IN} = 0 to 5.5 V		−220	µA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V		40	µA
I_{SC} (Note 1)	Output Short-Circuit Current	V_{OUT} =0.0V		−150	mA
I_{CC}	Supply Current			195	mA

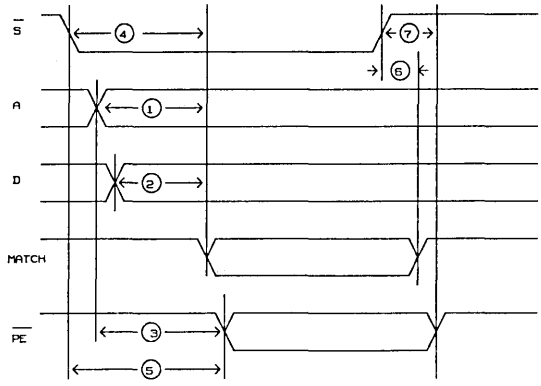
Note: 1. No more than one output should be short circuited at a time. The duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
Compare Mode					
1	t_{AVMV}	Address to MATCH		20.0	ns
2	t_{DVMV}	Data to MATCH		10.0	ns
3	t_{AVPV}	Address to $\overline{PE}$		25.0	ns
4	t_{SLMV}	$\overline{S}$ to MATCH		10.0	ns
5	t_{SLPV}	$\overline{S}$ to $\overline{PE}$		10.0	ns
6	t_{SHMH}	$\overline{S}$ to MATCH Recovery		10.0	ns
7	t_{SHPH}	$\overline{S}$ to $\overline{PE}$ Recovery		10.0	ns
Write Mode					
8	t_{WLWH}	Write Pulse Width	20.0		ns
9	t_{AVWL}	Address Setup	0.0		ns
10	t_{WHAX}	Address to $\overline{W}$ Hold	0.0		ns
11	t_{DVWH}	Data to $\overline{W}$ Setup	20.0		ns
12	t_{WHDX}	Data to $\overline{W}$ Hold	0.0		ns
13	t_{SLWH}	$\overline{S}$ to Setup	20.0		ns
14	t_{WHSH}	$\overline{S}$ to Select Hold	0.0		ns
15	t_{WLMH}	$\overline{W}$ to MATCH		10.0	ns
16	t_{WHMV}	Write Recovery (MATCH)		20.0	ns
17	t_{WLPH}	$\overline{W}$ to $\overline{PE}$		10.0	ns
18	t_{WHPV}	Write Recovery ($\overline{PE}$)		20.0	ns
19	t_{PVWH}	$\overline{PE}$ Input to $\overline{W}$ Setup		20.0	ns
20	t_{WHPH}	$\overline{PE}$ Input to $\overline{W}$ Hold		0.0	ns
Reset Mode					
21	t_{RLRH}	$\overline{R}$ Pulse Width	40.0		ns
22	t_{SLRL}	$\overline{S}$ to $\overline{R}$ Setup	0.0		ns
23	t_{RHSH}	$\overline{S}$ to $\overline{R}$ Hold	0.0		ns
24	t_{WHRL}	$\overline{W}$ to $\overline{R}$ Setup	0.0		ns
25	t_{RHWL}	$\overline{W}$ to $\overline{R}$ Hold	0.0		ns
26	t_{RLMH}	$\overline{R}$ to MATCH HIGH		10.0	ns
27	t_{RHMX}	$\overline{R}$ to MATCH Recovery		20.0	ns

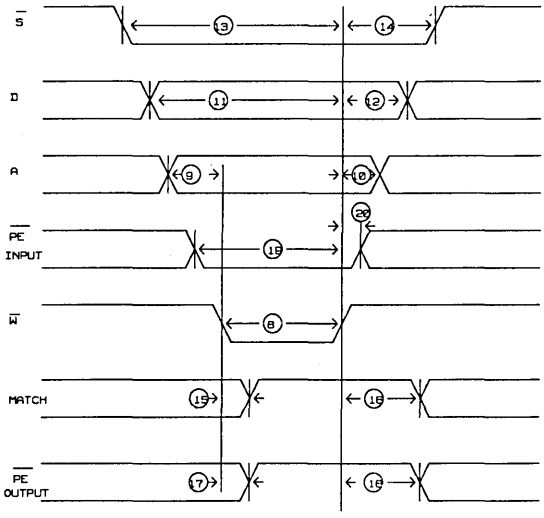
Notes: 1. All Switching Characteristics are measured at 50% of input to valid output. Both input and output timings are referenced to 1.5 V.

SWITCHING WAVEFORMS (Cont'd)



WF021890

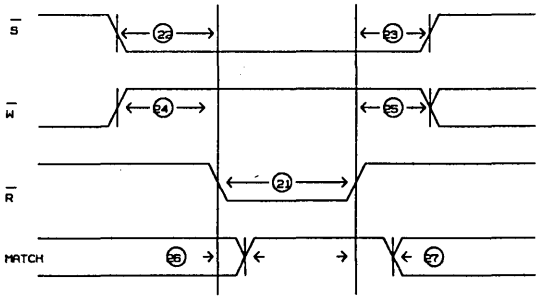
Compare Mode



WF021011

Write Mode

SWITCHING WAVEFORMS



WF021021

Reset Mode

Am27LS00/01 Series

256-Bit Low-Power Schottky Bipolar RAM

DISTINCTIVE CHARACTERISTICS

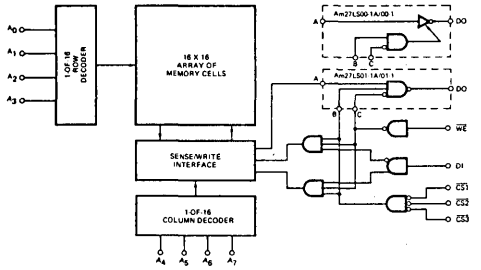
- High speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs or with open-collector outputs

GENERAL DESCRIPTION

The Am27LS00/01 Family is comprised of fully decoded bipolar random-access memories for use in high-speed buffer memories. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00 devices) or open-collector output (Am27LS01 devices). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output of the -1 device is active and inverts the value of DI (Write Transparent Operation). The other devices disable the output during the period $\overline{WE}$ is low. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

BLOCK DIAGRAM



BD000590

MODE SELECT TABLE

Input			Data Output Status $\overline{DO}$ (t_{n+1})	Mode
$\overline{CS}$	$\overline{WE}$	DI		
H	X	X	Output Disabled	No Selection
L	L	L	Inverted/Disabled*	Write '0'
L	L	H	Inverted/Disabled*	Write '1'
L	H	X	Selected Bit (Inverted)	Read

H = HIGH
L = LOW
X = Don't Care

*Inverted = -1 Devices
Disabled = All Other Devices

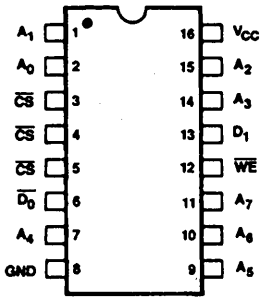
PRODUCT SELECTOR GUIDE

Open Collector Part Number	**STD**	Am27LS01A	Am27LS01	Am27LS01A	Am27LS01
	Write Transparent		Am27LS01-1		Am27LS01-1
Three-State Part Number	**STD**	Am27LS00A	Am27LS00	Am27LS00A	Am27LS00
	Write Transparent		Am27LS00-1		Am27LS00-1
Access Time		35 ns	45 ns		55 ns
Temperature Range		C	C	M	M

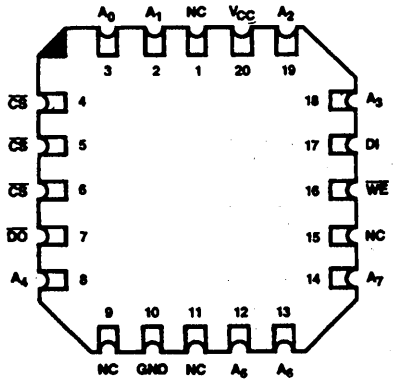
Publication # 03233 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

*



CD000880

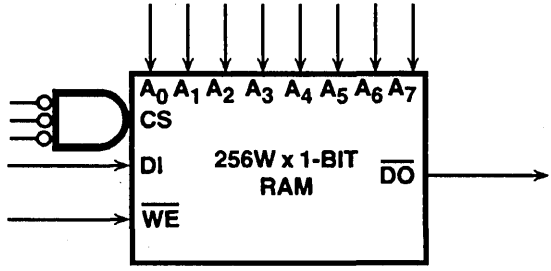


CD000890

*Same pinouts apply to both Ceramic DIP and Flatpack.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



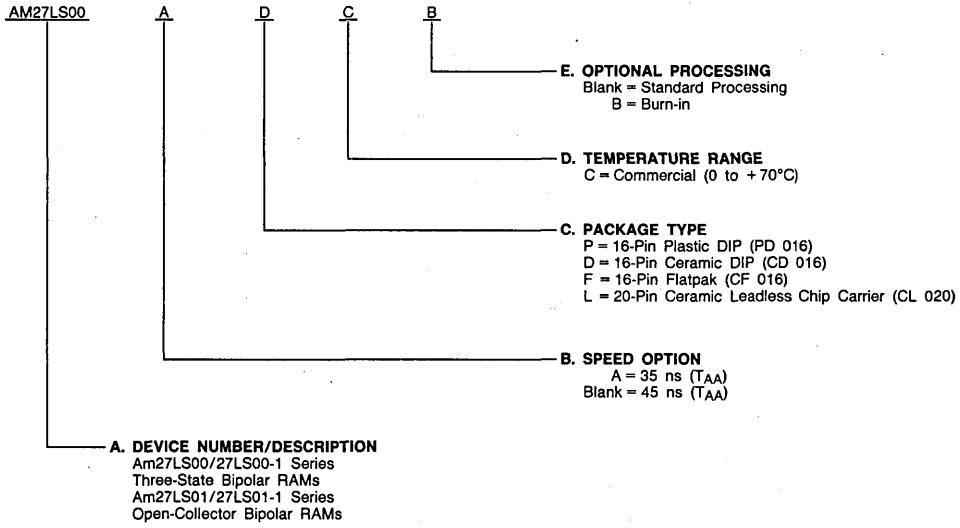
LS000201

V_{CC} = Power Supply
GND = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27LS00	PC, PCB, DC, DCB, FC, FCB, LC, LCB
AM27LS00A	
AM27LS00-1	
AM27LS01	
AM27LS01A	
AM27LS01-1	

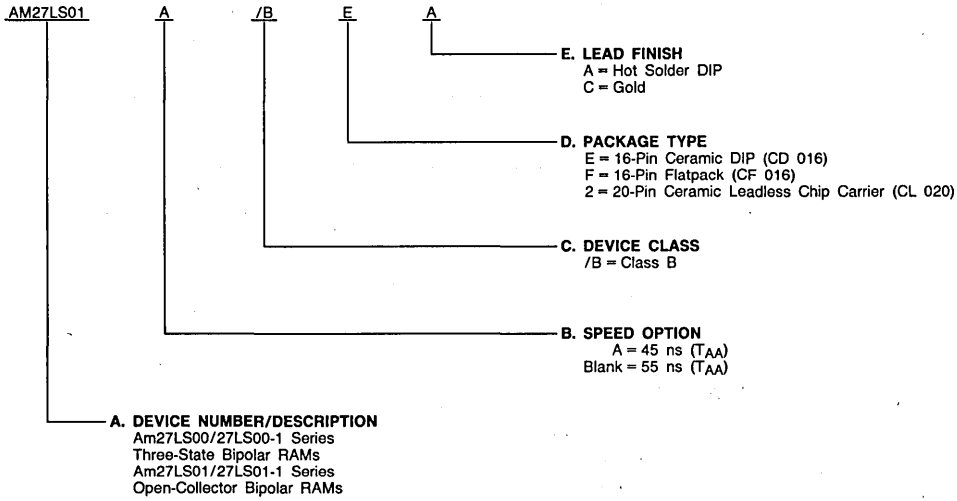
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27LS00	/BEA, /BFA, /B2C
AM27LS00A	
AM27LS00-1	
AM27LS01	
AM27LS01A	
AM27LS01-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to ground potential
(Pin16 to Pin8) continuous ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to+ V_{CC} max
DC Input Voltage ..... −0.5 V to +V_{CC}
Output Current, into Outputs ..... 30 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

See Note 4

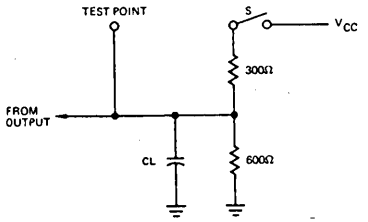
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V				−0.030	−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				< 1	20	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V			−20	−30	−60	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.		"A" version		80	115	mA
				Standard		55	70	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 2.4 V				0	30	μA
		$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−30	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Operating Specification with adequate time for temperatur e stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C=T_J 0_JA = 44 − 59° c/w (with moving air) for ceramic DIPs.0_JC = 10 − 17° c/w for flatpack or leadless chip carriers.

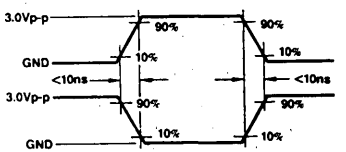
* See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST* CIRCUIT



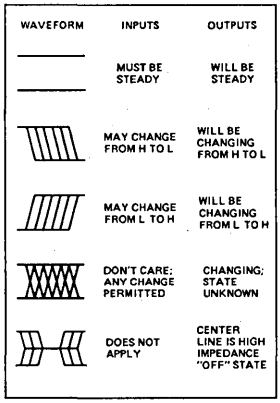
TC000210

SWITCHING TEST WAVEFORM



TW000030

KEY TO SWITCHING WAVEFORMS



KS000010

* See notes 3, 4, and 5 following Switching Characteristics table.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

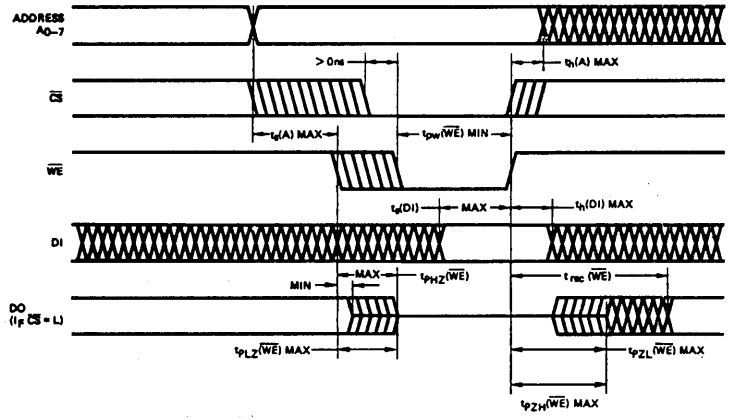
No.	Parameter Symbol	Parameter Description	Am27LS00A/01A Family				Am27S00/01 Family				Units
			C Devices		M Devices		C Devices		M Devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PLH}(A)	Delay from Address to Output		35		45		45		55	ns
2	t_{PHL}(A)										
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to to Active Output and Correct Data		25		25		25		30	ns
4	$t_{PZL}(\overline{CS})$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data		35		45		45		55	ns
6	$t_{PZL}(\overline{WE})$										
7	t_s(A)	Setup Time Address (Prior to Initiation of Write)	0		5		0		5		ns
8	t_h(A)	Hold Time Address (After Termination of Write)	0		5		0		5		ns
9	t_s(DI)	Setup Time Data Input (Prior to Termination of Write)	25		30		30		35		ns
10	t_h(DI)	Hold Time Data Input (After Termination of Write)	0		5		0		5		ns
11	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	25		30		30		35		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)		25		25		25		30	ns
13	$t_{PLZ}(\overline{CS})$										
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z) (Note 6)		30		40		30		40	ns
15	$t_{PHZ}(\overline{WE})$										

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. t_{PLH}(A) and t_{PHL}(A) are tested with S closed an d C_L = 50 pF with both input and output timing referenced to 1.5 V.
4. For open collector, all delays from write Enable($\overline{WE}$) o r Chip Select($\overline{CS}$) inputs to the Data Output(D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed and C_L = 50 pF and with both the input and output timing referenced to 1.5 V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S open, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S open and $C_L \leqslant$ 5 pF and are measured between the 1.5 V level on the input and the V_{OH} – 500 mV level on the output. $T_{PLZ}(\overline{WE})$ and $T_{PLZ}(\overline{CS})$ are measured with S closed and $C_L \leqslant$ 5 pF and are measured between the 1.5 V level on the input and the V_{OL} + 500 mV level on the output.
6. Does not apply to –1 devices.

*See the last page of the spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS

WRITE MODE

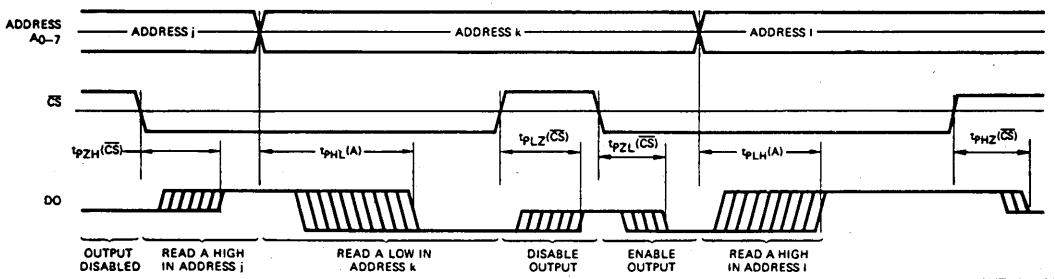


WF001091

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00A/00) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

3

READ MODE



WF001100

Switching delays from address and chip select inputs to the data output. For the Am27LS00A/00, Am27LS00-1A/00-1 disabled output is "OFF," represented by a single center line. For the Am27LS01A/01, Am27LS01-1A/01-1, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups	Parameter Symbol	Subgroups
t_{PLH} (A)	9, 10, 11	t_s (DI)	9, 10, 11
t_{PHL} (A)	9, 10, 11	t_h (DI)	9, 10, 11
t_{PZH} ($\overline{CS}$)	9, 10, 11	t_{pw} ($\overline{WE}$)	9, 10, 11
t_{PZL} ($\overline{CS}$)	9, 10, 11	t_{PHZ} ($\overline{CS}$)	9, 10, 11
t_{PZH} ($\overline{WE}$)	9, 10, 11	t_{PLZ} ($\overline{CS}$)	9, 10, 11
t_{PZL} ($\overline{WE}$)	9, 10, 11	t_{PLZ} ($\overline{WE}$)	9, 10, 11
t_s (A)	9, 10, 11	t_{PHZ} ($\overline{WE}$)	9, 10, 11
t_h (A)	9, 10, 11		

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27LS02/27LS03

64-Bit Low-Power Inverting-Output Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16 word x 4-bit low-power Schottky RAMs
- Low Power
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open-collector outputs (Am27LS02) or with three-state outputs (Am27LS03)
- Pin-compatible replacements for 74LS289, (use Am27LS02); for 74LS189, (use Am27LS03)

GENERAL DESCRIPTION

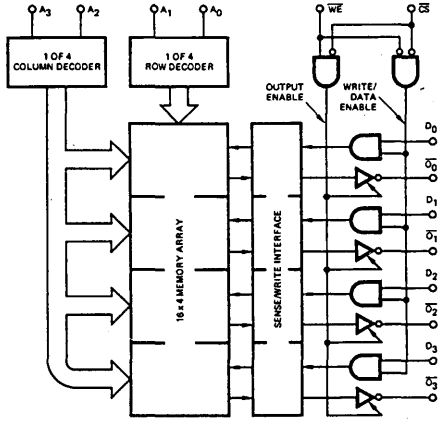
The Am27LS02 and Am27LS03 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open-collector OR tieable outputs (Am27LS02) or three-state outputs (Am27LS03).

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high-impedance state.

BLOCK DIAGRAM



BD000551

MODE SELECT TABLE

Input		Data Output Status $\overline{O_0}-\overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

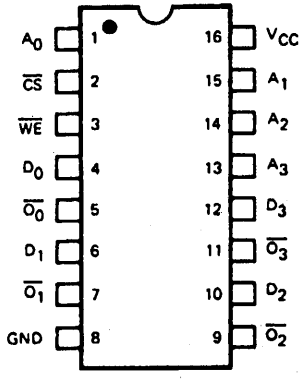
H = HIGH
L = LOW
X = Don't Care

PRODUCT SELECTOR GUIDE

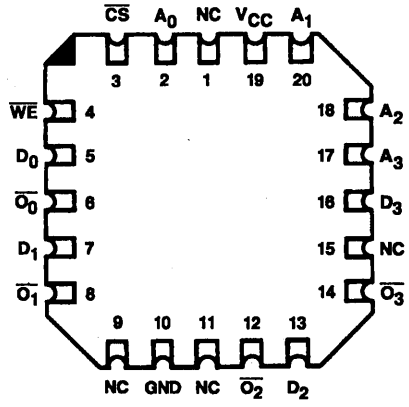
Access Time	55 ns	65 ns
I_{CC}	35 mA	38 mA
Temperature Range	C	M
Open Collector	Am27LS02	
Three-State	Am27LS03	

Publication # 08062 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



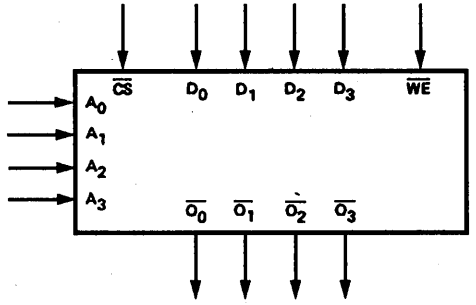
CD000831



CD000891

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



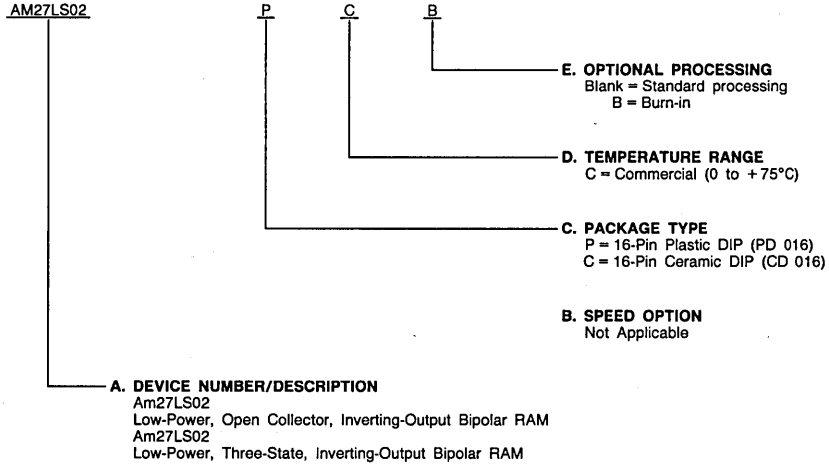
LS000211

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27LS02	PC, PCB, DC, DCB
AM27LS03	

Valid Combinations

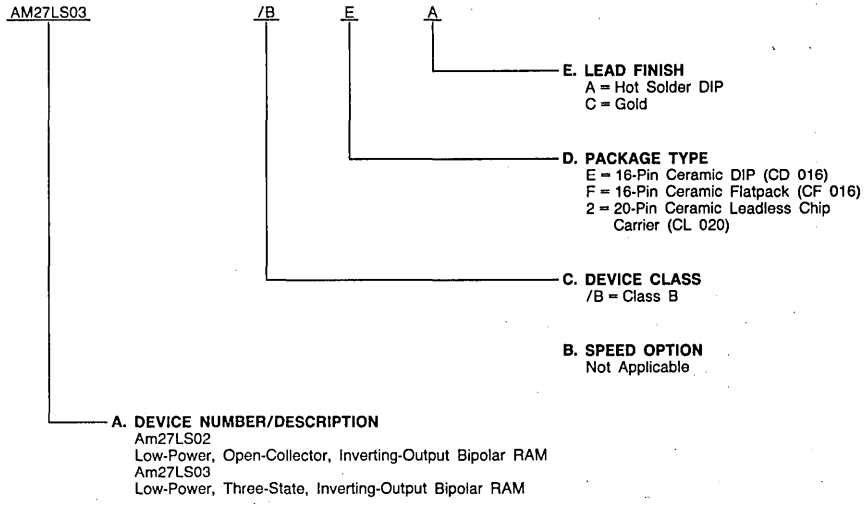
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

3

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
M27LS02	/BEA, /BFA
AM27LS03	/B2C

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

See Note 5

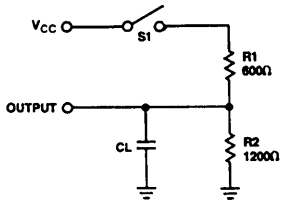
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am27LS02/27LS03 Min.	Typ.	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			350	450	mV
			I_{OL} = 10 mA			380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)		COM'L	2.0			Volts
				MIL	2.1			
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 3)		COM'L			0.8	
				MIL			0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, D_0–D_3, A_0–A_3			−15	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.		COM'L		30	35	
				MIL		30	38	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−40	0		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Operating specifications with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance Testing performed instantaneously where T_A = T_C = T_J.
$\theta_{JA} \approx 50°C/W$ (with moving air) for ceramic DIPs.
$\theta_{JC} \approx 10-17°C/W$ for flatpack and leadless chip carrier.

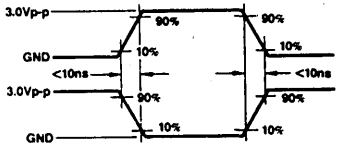
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



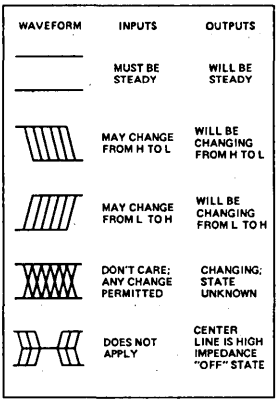
TC000200

SWITCHING TEST WAVEFORM



TW000030

KEY TO THE SWITCHING WAVEFORMS



KS000010

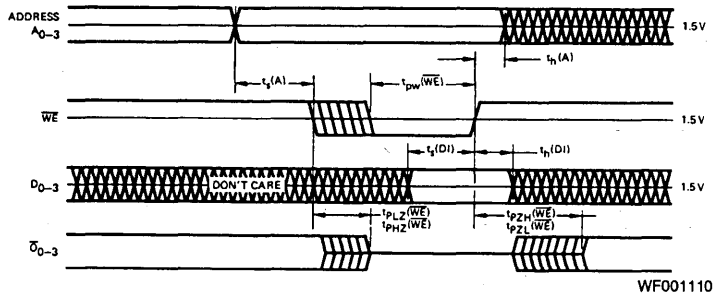
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am27LS02/Am27LS03 C Devices Min.	C Devices Max.	M Devices Min.	M Devices Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output		55		65	ns
2	$t_{PHL}(A)$						
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		30		35	ns
4	$t_{PZL}(\overline{CS})$						
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery - See Note 1)		30		35	ns
6	$t_{PZL}(\overline{WE})$						
7	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	45		55		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		ns
11	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	45		55		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)		30		35	ns
13	$t_{PLZ}(\overline{CS})$						
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)		30		35	ns
15	$t_{PHZ}(\overline{WE})$						

Notes:
1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and C_L = 30 pF with both input and output timing referenced to 1.5 V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30 pF and with both the input and output timing referenced to 1.5 V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30 pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30 pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the V_{OH} – 500 mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the V_{OL} + 500 mV level on the output.

*See the last page of this spec for Group A Subgroup Testing information.

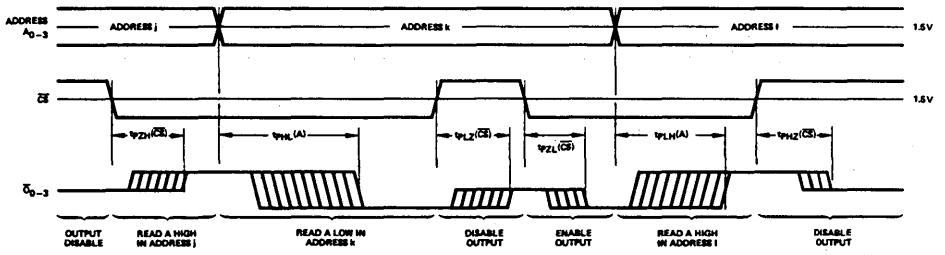
SWITCHING WAVEFORMS



WF001110

Write Mode

Write Cycle Timing. The cycle is initiated by an address change. After t_S(A)min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A)min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS03) while the write enable is ($\overline{WE}$) LOW.



WF001200

Read Mode

Switching delays from address and chip select inputs to the data output. For the Am27LS03 disabled output is "OFF", represented by a single center line. For the Am27LS02, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{PLH}(A)	9, 10, 11	9	t_s(DI)	9, 10, 11
2	t_{PHL}(A)				
3	$t_{PZH}(\overline{CS})$	9, 10, 11	10	t_h(DI)	9, 10, 11
4	$t_{PZL}(\overline{CS})$				
5	$t_{PZH}(\overline{WE})$	9, 10, 11	11	$t_{pw}(\overline{WE})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$				
7	t_s(A)	9, 10, 11	12	$t_{PHZ}(\overline{CS})$	9, 10, 11
			13	$t_{PLZ}(\overline{CS})$	
8	t_h(A)	9, 10, 11	14	$t_{PLZ}(\overline{WE})$	9, 10, 11
			15	$t_{PHZ}(\overline{WE})$	

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S02/27S03

64-Bit Inverting-Output Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16 word x 4-bit low-power Schottky RAMS
- Ultra-Fast "A" Version: Address access time 25ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open-collector outputs (Am27S02/02A) or with three-state outputs (Am27S03/03A)
- Pin-compatible replacements for 3101A, 74S289, (use Am27S02A/02); for 74S189, (use Am27S03A/03)

GENERAL DESCRIPTION

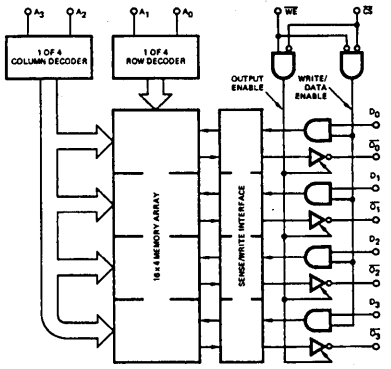
The Am27S02/02A and Am27S03/03A are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27S02/02A) or three-state outputs (Am27S03/03A). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

BLOCK DIAGRAM



BD000551

MODE SELECT TABLE

Input		Data Output Status $\overline{O_0}-\overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

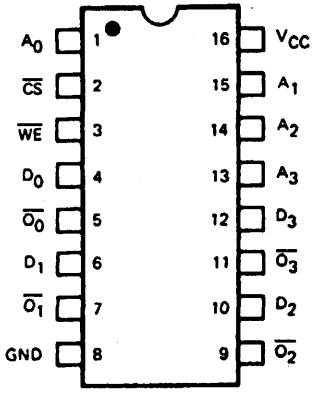
H = HIGH
L = LOW
X = Don't Care

PRODUCT SELECTOR GUIDE

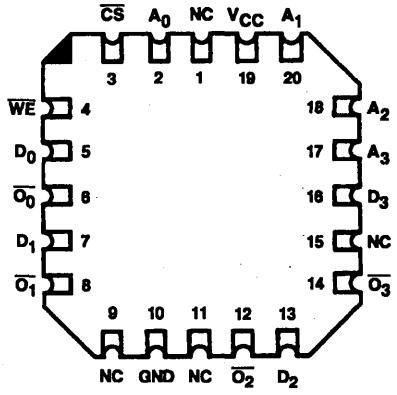
Access Time	25 ns	30 ns	35 ns	50 ns
I_{CC}	100 mA	105 mA	100 mA	105 mA
Temperature Range	C	M	C	M
Open Collector	Am27S02A	Am27S02A	Am27S02	Am27S02
Three-State	Am27S03A	Am27S03A	Am27S03	Am27S03

Publication # 02191 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



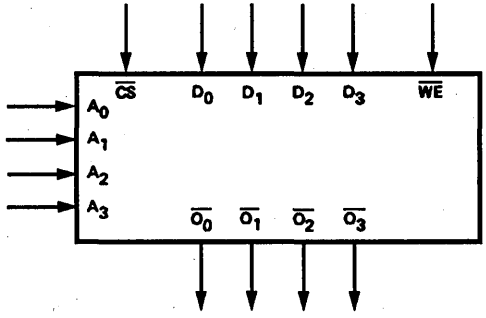
CD000831



CD000891

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



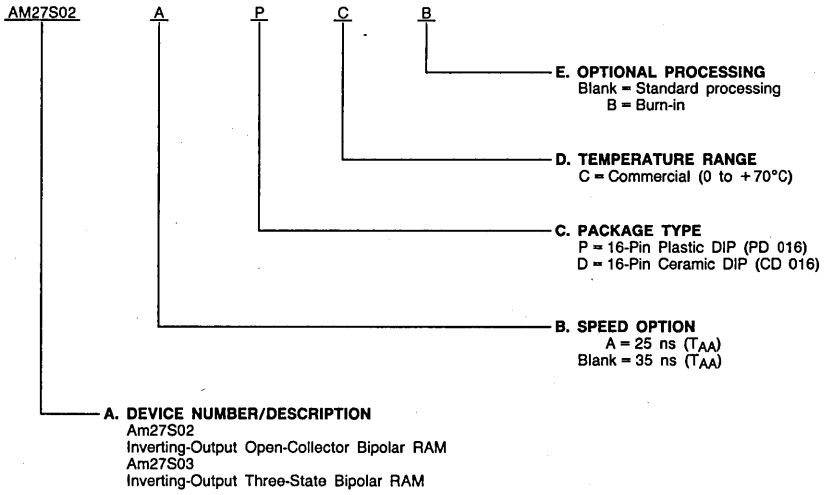
LS000211

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S02	PC, PCB, DC, DCB
AM27S02A	
AM27S03	
AM27S03A	

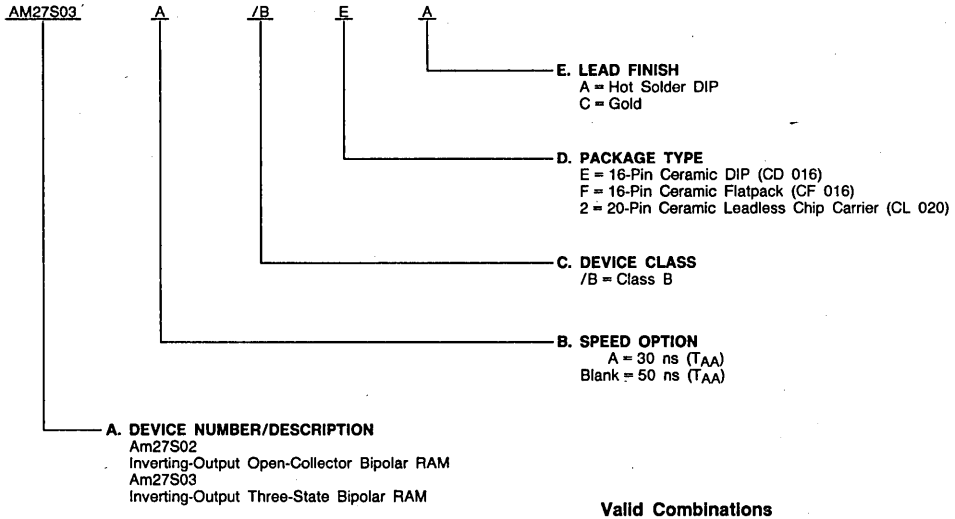
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S02	/BEA, /BFA, /B2C
AM27S02A	
AM27S03	
AM27S03A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (See Note 5)

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +475 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

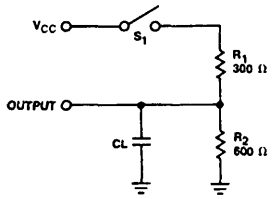
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			27S02/3 Min.	27S02/3 Typ.	27S02/3 Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			350	450	mV
			I_{OL} = 20 mA			380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)		COM'L	2.0			Volts
				MIL	2.1			
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 3)		COM'L			0.8	
				MIL			0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, D_0–D_3, A_0–A_3			−15	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.		COM'L		75	100	
				MIL		75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$=V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−40	0		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Operating specifications with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance Testing performance instantaneously where T_A = T_C = T_J.
$\theta_{JA} \approx$ 50 °C/W (with moving air) for Ceramic DIP.
$\theta_{JA} \approx$ 10-17°C/W for flatpack and leadless chip carrier.

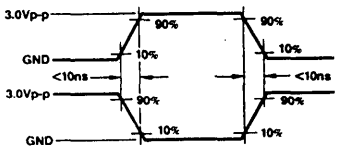
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



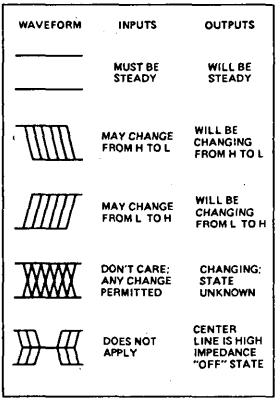
TC000170

SWITCHING TEST WAVEFORM



TW000030

KEY TO THE SWITCHING WAVEFORMS



KS000010

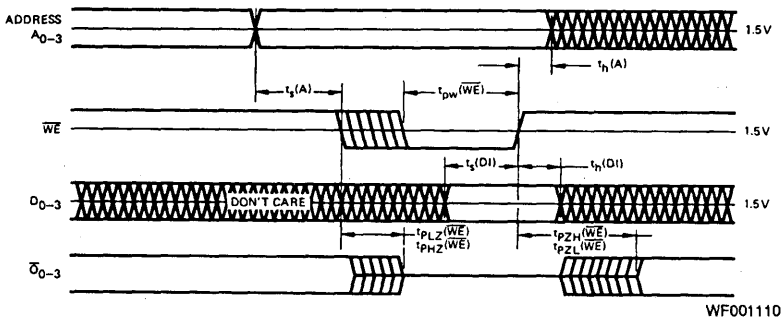
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am27S02A/3A A C Devices Min.	Am27S02A/3A A C Devices Max.	Am27S02A/3A A M Devices Min.	Am27S02A/3A A M Devices Max.	Am27S02/3 STD C Devices Min.	Am27S02/3 STD C Devices Max.	Am27S02/3 STD M Devices Min.	Am27S02/3 STD M Devices Max.	Units
1	t_{PLH}(A)	Delay from Address to Output		25		30		35		50	ns
2	t_{PHL}(A)										
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		15		20		17		25	ns
4	$t_{PZL}(\overline{CS})$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery- See Note 1)		20		25		35		40	ns
6	$t_{PZL}(\overline{WE})$										
7	t_s(A)	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
8	t_h(A)	Hold Time Address (After Termination of Write)	0		0		0		0		ns
9	t_s(DI)	Setup Time Data Input (Prior to Termination of Write)	20		25		25		25		ns
10	t_h(DI)	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
11	$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	20		25		25		25		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to inactive Output (HI-Z)		15		20		17		25	ns
13	$t_{PLZ}(\overline{CS})$										
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)		20		25		25		35	ns
15	$t_{PHZ}(\overline{WE})$										

Notes:
1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and C_L = 30 pF with both input and output timing referenced to 1.5 V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30 pF and with both the input and output timing referenced to 1.5 V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30 pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30 pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the V_{OH} – 500 mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the V_{OL} + 500 mV level on the output.

*See the last page of this spec for Group A Subgroup Testing information.

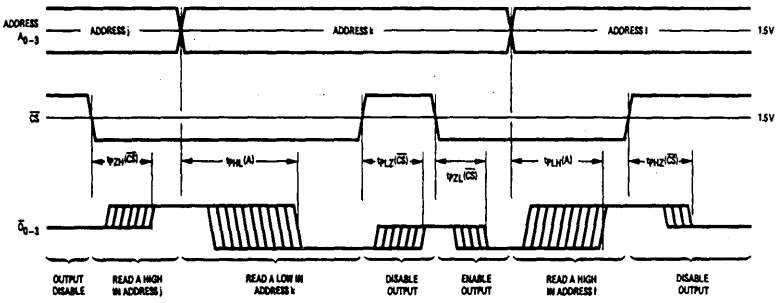
SWITCHING WAVEFORMS



WF001110

Write Mode

Write Cycle Timing. The cycle is initiated by an address change. After t_S(A)min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A)min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03A/03) while the write enable is ($\overline{WE}$) LOW.



WF001200

Read Mode

Switching delays from address and chip select inputs to the data output. For the Am27S03A/03 disabled output is "OFF", represented by a single center line. For the Am27S02A/02, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{PLH}(A)	9, 10, 11	9	t_s(DI)	9, 10, 11
2	t_{PHL}(A)				
3	$t_{PZH}(\overline{CS})$	9, 10, 11	10	t_h(DI)	9, 10, 11
4	$t_{PZL}(\overline{CS})$				
5	$t_{PZH}(\overline{WE})$	9, 10, 11	11	$t_{pw}(\overline{WE})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$				
7	t_s(A)	9, 10, 11	12	$t_{PHZ}(\overline{CS})$	9, 10, 11
			13	$t_{PLZ}(\overline{CS})$	
8	t_h(A)	9, 10, 11	14	$t_{PLZ}(\overline{WE})$	9, 10, 11
			15	$t_{PHZ}(\overline{WE})$	

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27LS06/27LS07

64-Bit Low-Power Noninverting-Output Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low power Schottky RAMs
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS07) or with open collector outputs (Am27LS06)
- Electrically tested and optically inspected die for the assemblers of hybrid products

GENERAL DESCRIPTION

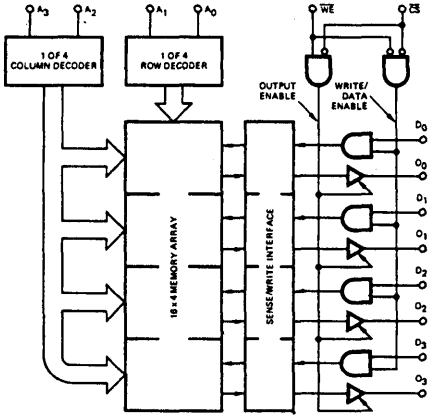
The Am27LS06 and Am27LS07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs or three-state outputs.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

BLOCK DIAGRAM



BD000560

MODE SELECT TABLE

Input		Data Output Status O_{0-3}	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word	Read
H	X	Output Disabled	Deselect

H = HIGH
L = LOW
X = Don't Care

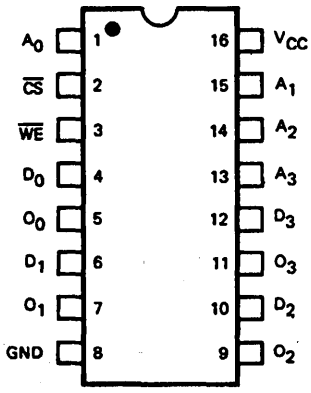
PRODUCT SELECTOR GUIDE

Access Time	55 ns	65 ns
I_{CC}	35 mA	38 mA
Temperature Range	C	M
Open Collector	27LS06	
Three-State	27LS07	

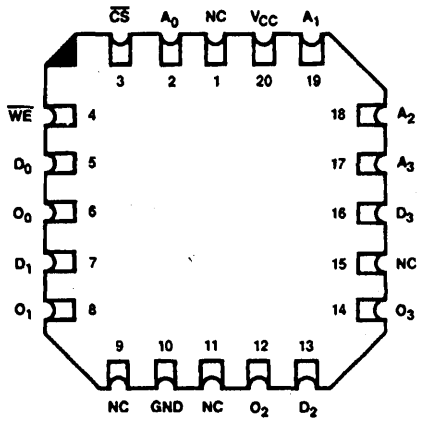
Publication # 08064 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

DIPs*



CD000870

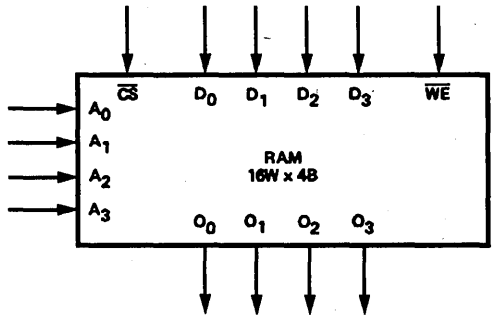


CD000841

*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

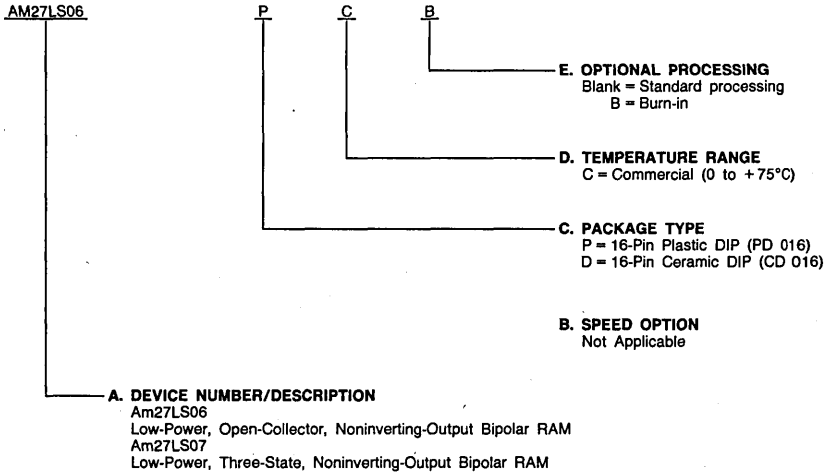


LS000311

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27LS06	PC, PCB, DC, DCB
AM27LS07	

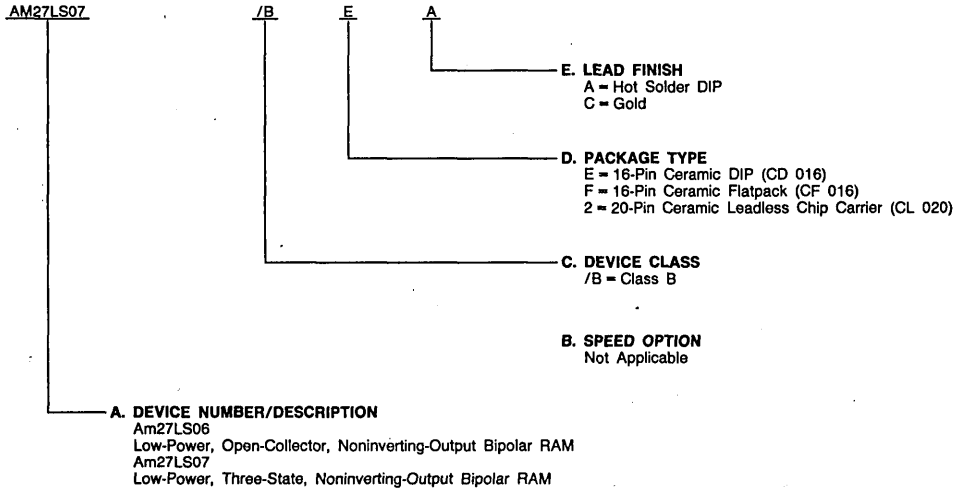
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27LS06	/BEA, /BFA, /B2C
AM27LS07	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

See Note 5

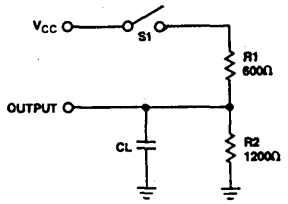
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am27LS06/Am27LS07 Min.	Typ.	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			350	450	mV
			I_{OL} = 10 mA			380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)		COM'L	2.0			Volts
				MIL	2.1			
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 3)		COM'L			0.8	
				MIL			0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, D_0–D_3, A_0–A_3			−15	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.		COM'L		30	35	
				MIL		30	38	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−40	0		

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
   $\theta_{JA} \approx 50°/W$ (with moving air) for Ceramic DIP.
   $\theta_{JC} \approx 10-17°/W$ for flatpack and leadless chip carrier.

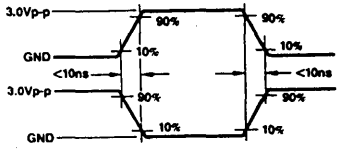
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



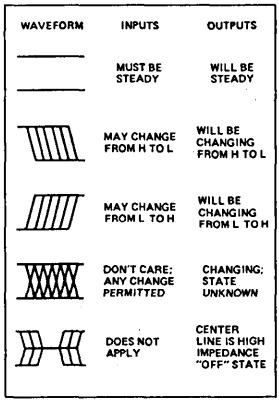
TC000200

SWITCHING TEST WAVEFORM



TW000030

KEY TO SWITCHING WAVEFORMS



KS000010

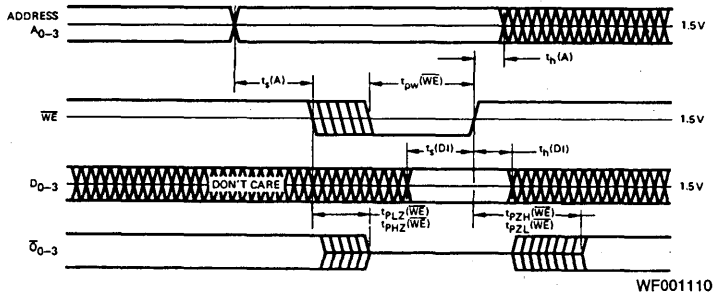
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am27LS06/Am27LS07 C Devices Min.	C Devices Max.	M Devices Min.	M Devices Max.	Units
1	t_{PLH}(A)	Delay from Address to Output		55		65	ns
2	t_{PHL}(A)						
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		30		35	ns
4	$t_{PZL}(\overline{CS})$						
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery-See Note 1)		30		35	ns
6	$t_{PZL}(\overline{WE})$						
7	t_s(A)	Setup Time Address (Prior to Initiation of Write)	0		0		ns
8	t_h(A)	Hold Time Address (After Termination of Write)	0		0		ns
9	t_s(DI)	Setup Time Data Input (Prior to Termination of Write)	45		55		ns
10	t_h(DI)	Hold Time Data Input (After Termination of Write)	0		0		ns
11	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	45		55		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)		30		35	ns
13	$t_{PLZ}(\overline{CS})$						
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)		30		35	ns
15	$t_{PHZ}(\overline{WE})$						

Notes:
1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

*See the last page of this spec for Group A Subgroup Testing information.

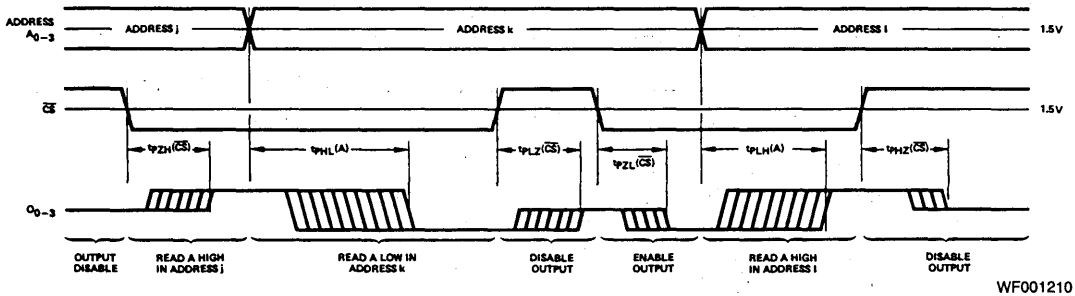
SWITCHING WAVEFORMS



WF001110

Write Mode
($\overline{CS}$ = LOW unless otherwise noted)

Write Cycle Timing. The cycle in initiated by an address change. After t_S(A)min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A)min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS07) while the write enable is LOW.



WF001210

Read Mode

Switching delays from address and chip select inputs to the data output. For the Am27LS07, disabled output is "OFF", represented by a single center line. For the Am27LS06, disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{PLH}(A)	9, 10, 11	9	t_s(DI)	9, 10, 11
2	t_{PHL}(A)				
3	$t_{PZH}(\overline{CS})$	9, 10, 11	10	t_h(DI)	9, 10, 11
4	$t_{PZL}(\overline{CS})$				
5	$t_{PZH}(\overline{WE})$	9, 10, 11	11	$t_{pw}(\overline{WE})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$				
7	t_s(A)	9, 10, 11	12	$t_{PHZ}(\overline{CS})$	9, 10, 11
			13	$t_{PLZ}(\overline{CS})$	
8	t_h(A)	9, 10, 11	14	$t_{PLZ}(\overline{WE})$	9, 10, 11
			15	$t_{PHZ}(\overline{WE})$	

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27S06/27S07

64-Bit Noninverting-Output Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low power Schottky RAMs
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27S07/07A) or with open collector outputs (Am27S06/06A)
- Electrically tested and optically inspected die for the assemblers of hybrid products

GENERAL DESCRIPTION

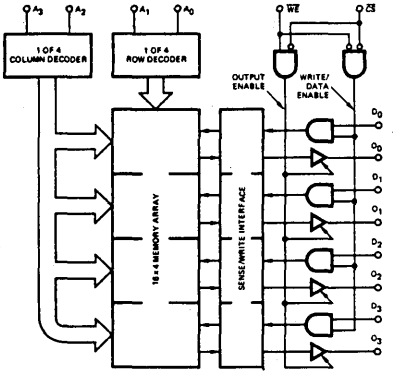
The Am27S06/06A and Am27S07/07A are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs or three-state outputs.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

BLOCK DIAGRAM



BD000560

MODE SELECT TABLE

Input		Data Output Status O_{0-3}	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word	Read
H	X	Output Disabled	Deselect

H = HIGH
L = LOW
X = Don't Care

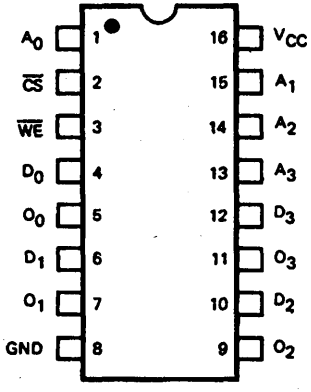
PRODUCT SELECTOR GUIDE

Access Time	25 ns	30 ns	35 ns	50 ns
I_{CC}	100 mA	105 mA	100 mA	105 mA
Temperature Range	C	M	C	M
Open Collector Part Number	27S06A		27S06	
Three-State Part Number	27S07A		27S07	

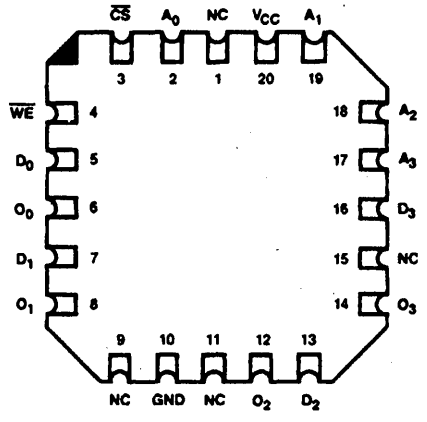
Publication # 03205 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

DIPs*



CD000870

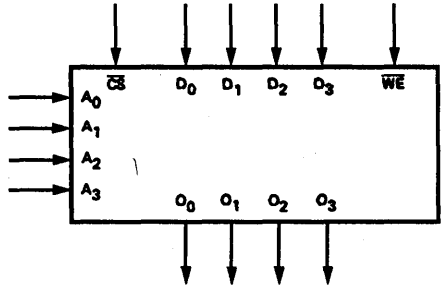


CD000841

*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

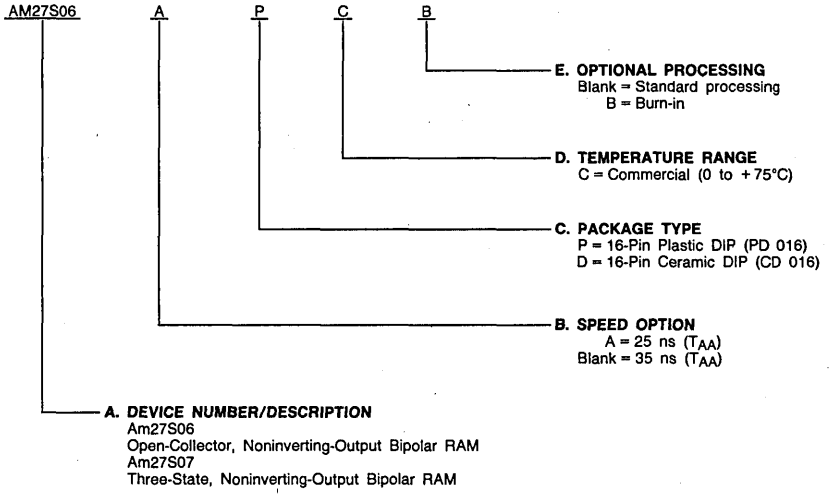


LS000312

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27S06	PC, PCB, DC, DCB
AM27S06A	
AM27S07	
Am27S07A	

Valid Combinations

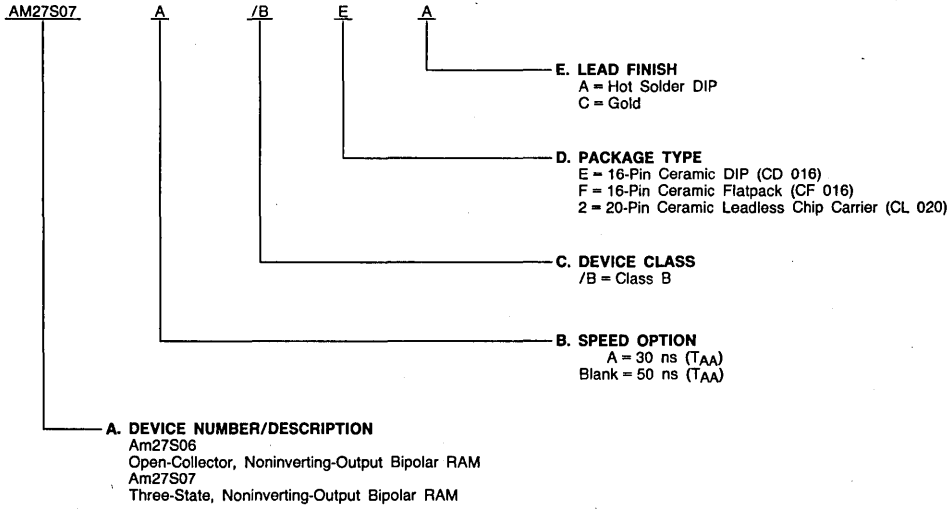
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

3

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S06	/BEA, /BFA, /B2C
AM27S06A	
AM27S07	
AM27S07A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

See Note 5

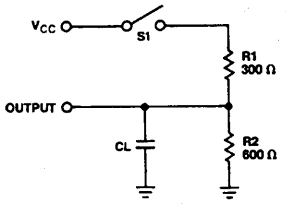
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am27S06/27S07, 27S06A/27S07A Min.	Typ.	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			350	450	mV
			I_{OL} = 20 mA			380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)		COM'L	2.0			Volts
				MIL	2.1			
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 3)		COM'L			0.8	
				MIL			0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, D_0–D_3, A_0–A_3			−15	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.		COM'L		75	100	
				MIL		75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA
		$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−40	0		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
$\theta_{JA} \approx 50°/w$ (with moving air) for Ceramic DIP.
$\theta_{JC} \approx 10-17°/w$ for Flatpack and leadless chip carrier.

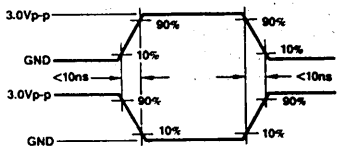
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



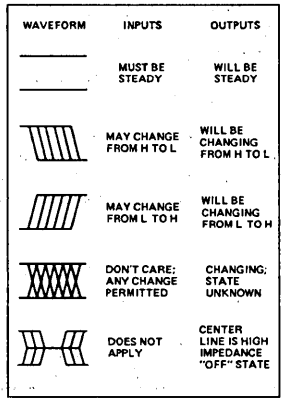
TC000201

SWITCHING TEST WAVEFORM



TW000030

KEY TO SWITCHING WAVEFORMS



KS000010

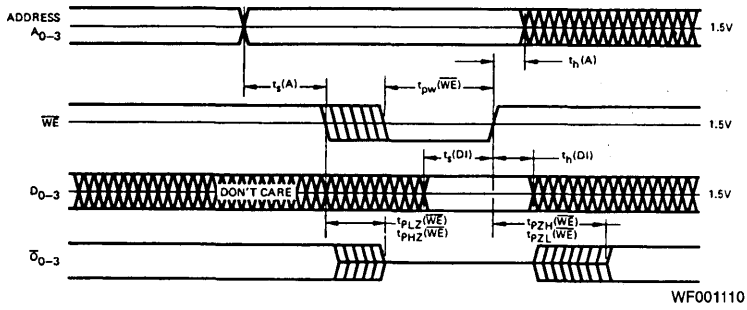
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am27S06A/27S07A C Devices Min.	Am27S06A/27S07A C Devices Max.	Am27S06A/27S07A M Devices Min.	Am27S06A/27S07A M Devices Max.	Am27S06/27S07 C Devices Min.	Am27S06/27S07 C Devices Max.	Am27S06/27S07 M Devices Min.	Am27S06/27S07 M Devices Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output		25		30		35		50	ns
2	$t_{PHL}(A)$										
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		15		20		17		25	ns
4	$t_{PZL}(\overline{CS})$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery-See Note 1)		20		25		35		40	ns
6	$t_{PZL}(\overline{WE})$										
7	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		0		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	20		25		25		25		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
11	$t_{pw}(\overline{WE})$	MIN Write Enable Width Pulse to Insure Write	20		25		25		25		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to inactive Output (HI-Z)		15		20		17		25	ns
13	$t_{PLZ}(\overline{CS})$										
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)		20		25		25		35	ns
15	$t_{PHZ}(\overline{WE})$										

Notes:
1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

*See the last page of this spec for Group A Subgroup Testing information.

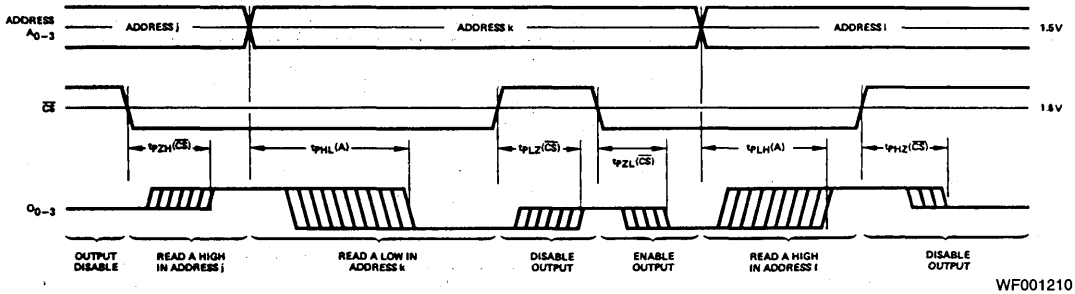
SWITCHING WAVEFORMS



WF001110

Write Mode
($\overline{CS}$ = LOW unless otherwise noted)

Write Cycle Timing. The cycle in initiated by an address change. After t_S(A)min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A)min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S07A/07) while the write enable is LOW.



WF001210

Read Mode

Switching delays from address and chip select inputs to the data output. For the Am27S07/07A disabled output is "OFF", represented by a single center line. For the Am27S06A/06 disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{PLH}(A)	9, 10, 11	9	t_s(DI)	9, 10, 11
2	t_{PHL}(A)				
3	$t_{PZH}(\overline{CS})$	9, 10, 11	10	t_h(DI)	9, 10, 11
4	$t_{PZL}(\overline{CS})$				
5	$t_{PZH}(\overline{WE})$	9, 10, 11	11	$t_{pw}(\overline{WE})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$				
7	t_s(A)	9, 10, 11	12	$t_{PHZ}(\overline{CS})$	9, 10, 11
			13	$t_{PLZ}(\overline{CS})$	
8	t_h(A)	9, 10, 11	14	$t_{PLZ}(\overline{WE})$	9, 10, 11
			15	$t_{PHZ}(\overline{WE})$	

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am31L01/31L01A

64-Bit Low Power Write Transparent, Inverting Output, Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Standard version: Address access time 50 ns
- Low power: I_{CC} typically 75 mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- High speed
- Fully decoded 16-word x 4-bit Schottky RAMs

GENERAL DESCRIPTION

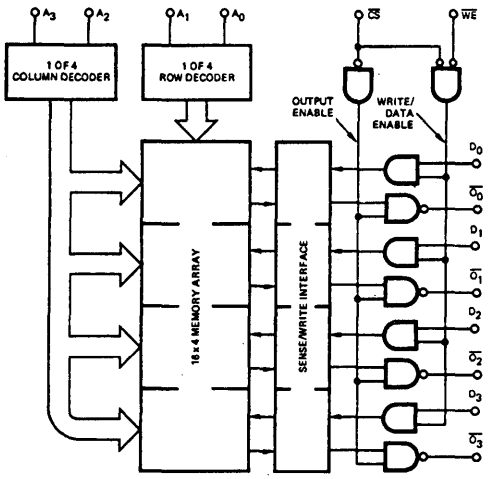
The Am31L01/31L01A is comprised of 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and open-collector OR tieable outputs.

An active-LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the four data inputs, D_0 to D_3, is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs, D_0 to D_3.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high-impedance state.

BLOCK DIAGRAM



BD000761

MODE SELECT TABLE

Input		Data Output Status $\overline{O_0}$–$\overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Data In (Inverted)	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

H = HIGH L = LOW X = Don't Care

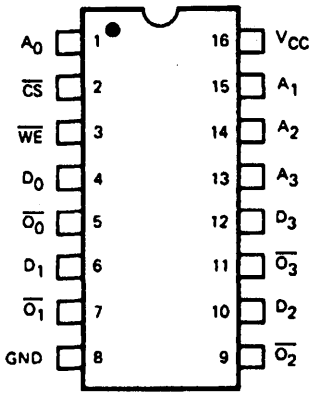
PRODUCT SELECTOR GUIDE

Open Collector (Write Transparent)	Am31L01A	Am31L01A	Am31L01	Am31L01
Access Time	55 ns	65 ns	80 ns	90 ns
I_{CC}	35 mA	38 mA	35 mA	38 mA
Temperature Range	C	M	C	M

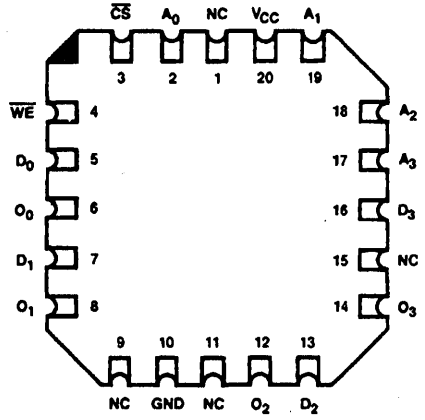
Publication # 08063 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

DIPs*



CD000831

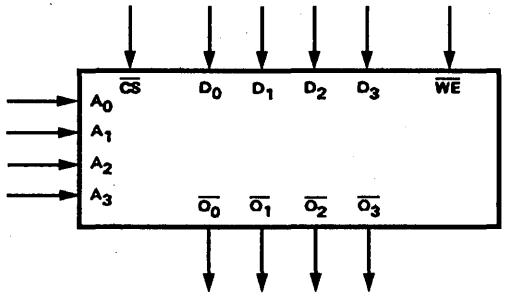


CD000841

*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

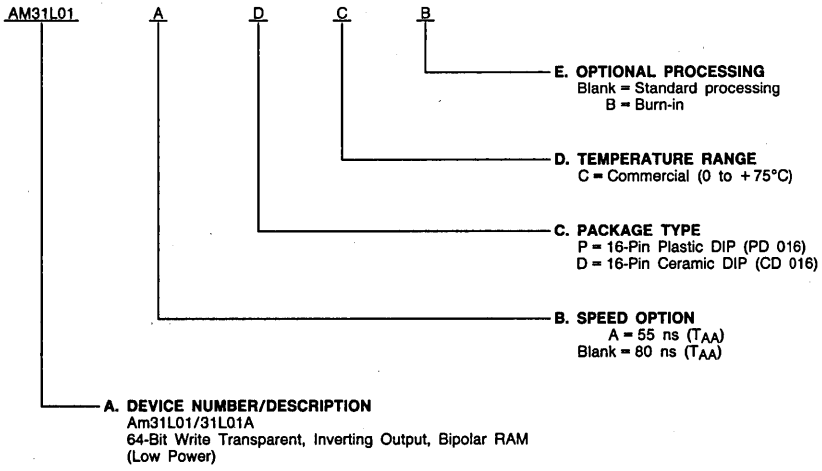


LS000211

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM31L01	PC, PCB, DC, DCB
AM31L01A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

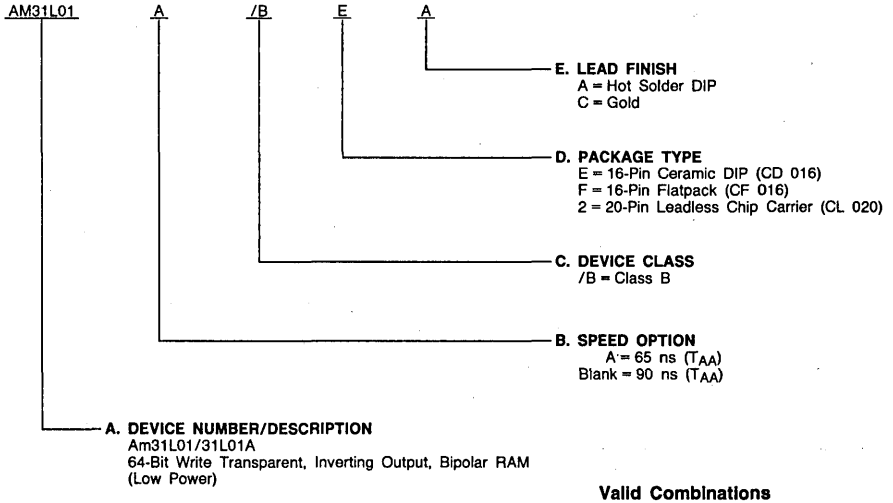
3

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM31L01	/BEA, /BFA, /B2C
AM31L01A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to Ground Potential
(Pin 18 to Pin 8) ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current, into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 3)

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

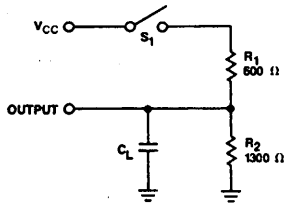
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am31L01/31L01A Min.	Typ.	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			280	450	mV
			I_{OL} = mA			310	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)		COM'L	2.0			Volts
				MIL.	2.1			
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)		COM'L.			0.8	
				MIL.			0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, $D_0 - D_3$, $A_0 - A_3$			−30	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.		COM'L		25	35	mA
				MIL.		25	38	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
$\theta_{JA} \approx 50$ °/w (with moving air) for Ceramic DIP.
$\theta_{JC} \approx 10–17$ °/w for Flatpack and Leadless Chip Carrier.

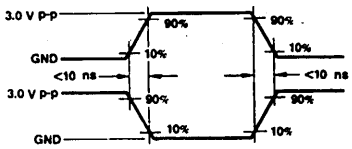
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



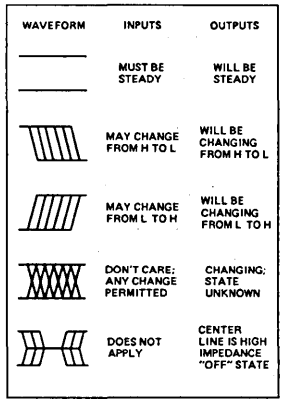
TC000172

SWITCHING TEST WAVEFORM



TW000031

KEY TO SWITCHING WAVEFORMS



KS000010

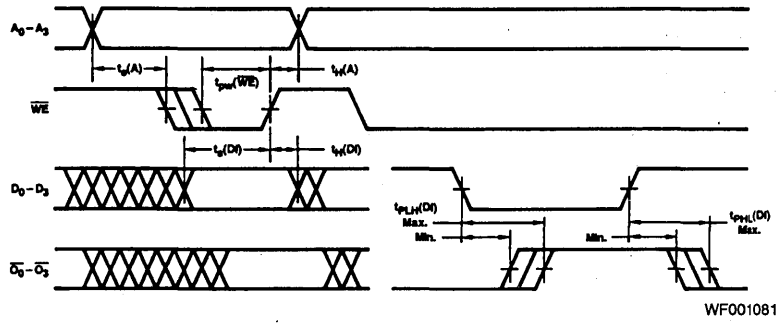
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am31L01A C Devices Min.	Am31L01A C Devices Max.	Am31L01A M Devices Min.	Am31L01A M Devices Max.	AM31L01 C Devices Min.	AM31L01 C Devices Max.	AM31L01 M Devices Min.	AM31L01 M Devices Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output		55		65		80		90	ns
2	$t_{PHL}(A)$										
3	$t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		30		35		60		70	ns
4	$t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 1)		30		35		80		100	ns
5	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
6	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		0		ns
7	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	45		55		60		80		ns
8	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
9	$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	45		55		60		80		ns
10	$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)		30		35		50		60	ns
11	$t_{PLH}(DI)$	Delay from Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)		55		65		80		90	ns
12	$t_{PHL}(DI)$										

Notes: 1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated. (No write recovery glitch).
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. All delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS}$), t_{PZL} ($\overline{WE}$) and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V.

*See the last page of this spec for Group A Subgroup Testing information.

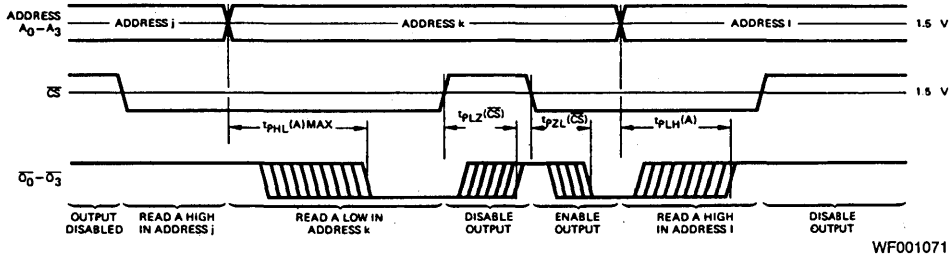
SWITCHING WAVEFORMS



WF001081

Write Mode

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ Min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ Min. must be allowed before the address may be changed again. The output will be the complement of the data input while the write enable ($\overline{WE}$) is LOW.



WF001071

Read Mode

Switching delays from address and chip select inputs to the data output.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{PLH}(A)	9, 10, 11
2	t_{PHL}(A)	9, 10, 11
3	$t_{PZL}(\overline{CS})$	9, 10, 11
4	$t_{PZL}(\overline{WE})$	9, 10, 11
5	t_s(A)	9, 10, 11
6	t_h(A)	9, 10, 11
7	t_s(DI)	9, 10, 11
8	t_h(DI)	9, 10, 11
9	$t_{pw}(\overline{WE})$	9, 10, 11
10	$t_{PLZ}(\overline{CS})$	9, 10, 11
11	t_{PLH}(DI)	9, 10, 11
12	t_{PHL}(DI)	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am3101/3101-1

64-Bit Write Transparent, Inverting Output, Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Standard version: Address access time 50 ns
- Low power: I_{CC} typically 75 mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- High speed
- Fully decoded 16-word x 4-bit Schottky RAMs

GENERAL DESCRIPTION

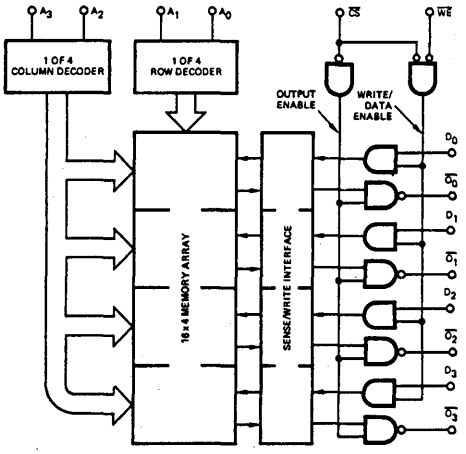
The Am3101/3101-1 is comprised of 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select ($\overline{CS}$) input and open-collector OR tieable outputs. Chip selection for large memory systems can be controlled by active-LOW output decoders such as the Am74S138.

An active-LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the four data inputs, D_0 to D_3, is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs, D_0 to D_3.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high-impedance state.

BLOCK DIAGRAM



BD000761

MODE SELECT TABLE

Input		Data Output Status $\overline{O_0}$ - $\overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output Disabled	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

MODE SELECT TABLE

Input		Data Output Status $\overline{O_0}$ - $\overline{O_3}$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Data in (Inverted)	Write
L	H	Selected Word (Inverted)	Read
H	X	Output Disabled	Deselect

H = HIGH L = LOW X = Don't Care

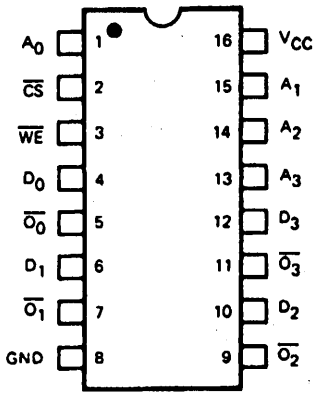
PRODUCT SELECTOR GUIDE

Open Collector (Write Transparent)	Am3101-1	Am3101-1	Am3101	Am3101
I_{CC}	100 mA	105 mA	100 mA	105 mA
Access Time	35 ns	50 ns		60 ns
Temperature Range	C	M	C	M

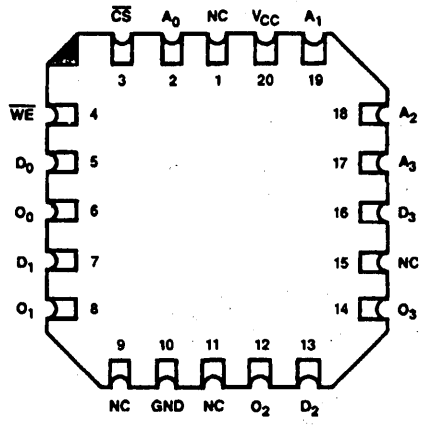
Publication # 03203 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

DIPs*



CD000831

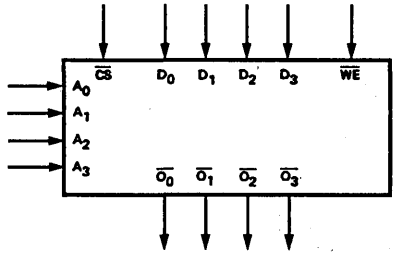


CD000841

*Also available in 16-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

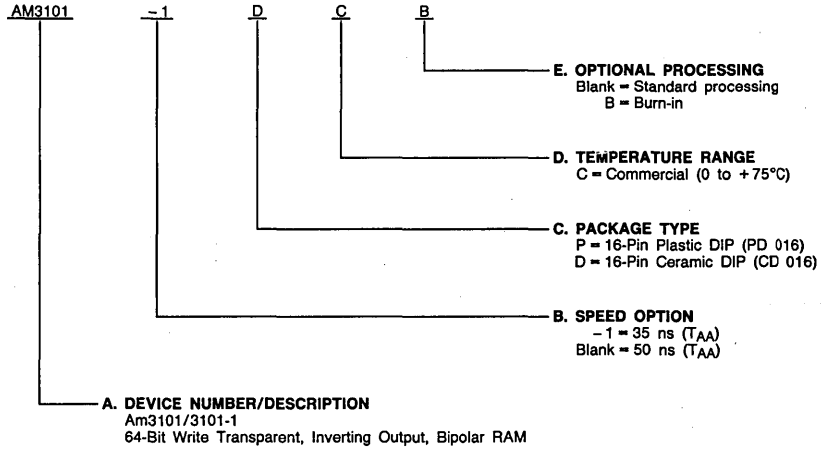


LS000211

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM3101	PC, PCB, DC, DCB
AM3101-1	

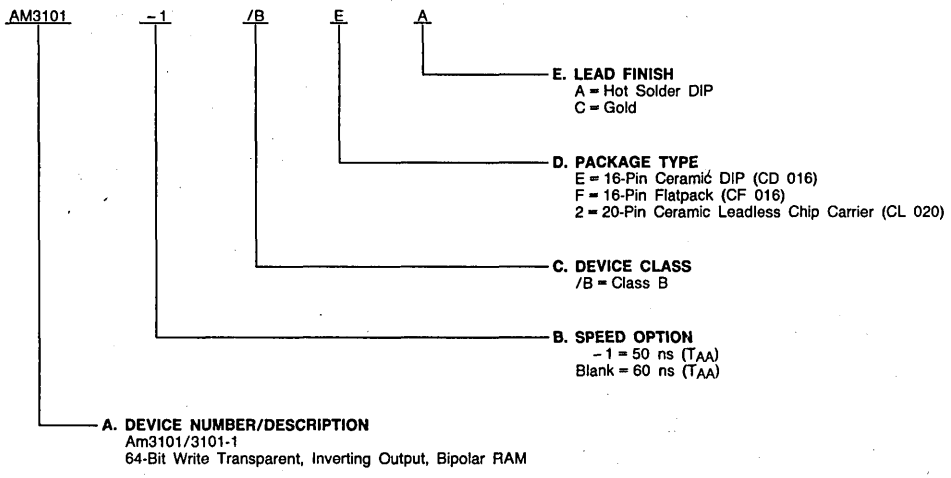
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM3101	/BEA, /BFA, /B2C
AM3101-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to Ground Potential
(Pin 18 to Pin 8) ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
Output Current, into Outputs ..... 20 mA
DC Input Current ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 3)

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified*

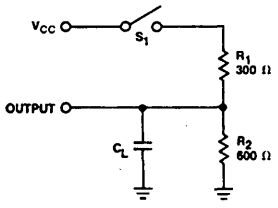
Parameter Symbol	Parameter Description	Test Conditions			Am3101/3101-1 Min.	Typ.	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			350	450	mV
			I_{OL} = 20 mA			380	500	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)		COM'L	2.0			Volts
				MIL.	2.1			
V_{IL}	Input HIGH Level	Guaranteed Input Logical LOW Voltage for all inputs (Note 2)		COM'L.			0.8	
				MIL.			0.8	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V	$\overline{WE}$, $D_0 - D_3$, $A_0 - A_3$			−15	−250	μA
			$\overline{CS}$			−30	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				0	10	μA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.		COM'L		75	100	mA
				MIL.		75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.85	−1.2	Volts
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = 2.4 V, V_{CC} = Max.				0	40	μA

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_C = T_J$.
$\theta_{JA} \approx 50$ °/w (with moving air) for Ceramic DIP.
$\theta_{JC} \approx 10 - 17$ °/w for Flatpack and Leadless Chip Carrier.

*See the last page of this spec for Group A Subgroup Testing information.

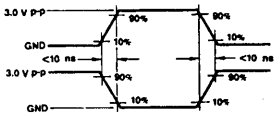
3

SWITCHING TEST CIRCUIT



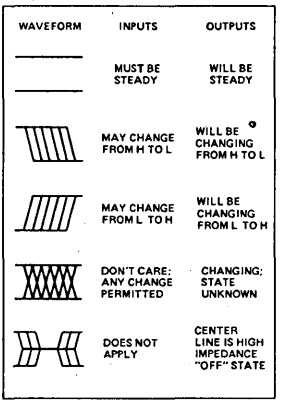
TC000171

SWITCHING TEST WAVEFORM



TW000031

KEY TO SWITCHING WAVEFORMS



KS000010

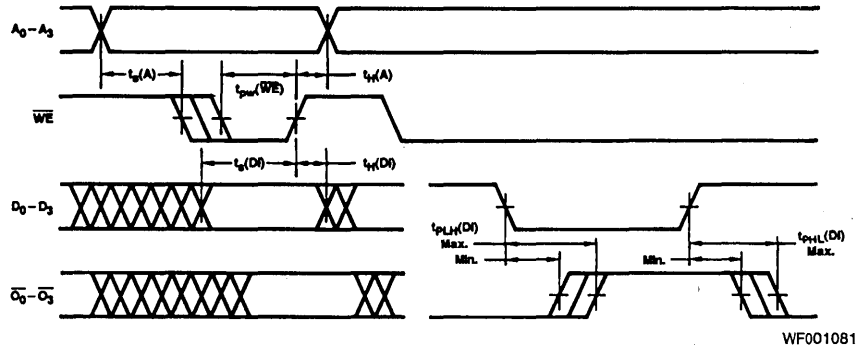
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am3101-1 C Devices Min.	Am3101-1 C Devices Max.	Am3101-1 M Devices Min.	Am3101-1 M Devices Max.	Am3101 C Devices Min.	Am3101 C Devices Max.	Am3101 M Devices Min.	Am3101 M Devices Max.	Units
Standard Power Devices											
1	$t_{PLH}(A)$	Delay from Address to Output		35		50		50		60	ns
2	$t_{PHL}(A)$										
3	$t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data		17		25		30		40	ns
4	$t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 1)		35		50		50		60	ns
5	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
6	$t_h(A)$	Hold Time Address (After Termination of Write)	0		0		0		0		ns
7	$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	25		25		30		30		ns
8	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	0		0		0		0		ns
9	$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	25		25		30		30		ns
10	$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)		17		25		30		40	ns
11	$t_{PLH}(DI)$	Delay from Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)		35		50		50		60	ns
12	$t_{PHL}(DI)$										

Notes:
1. Output is conditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated.
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. All delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS}$), t_{PZL} ($\overline{WE}$) and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.

*See the last page of this spec for Group A Subgroup Testing information.

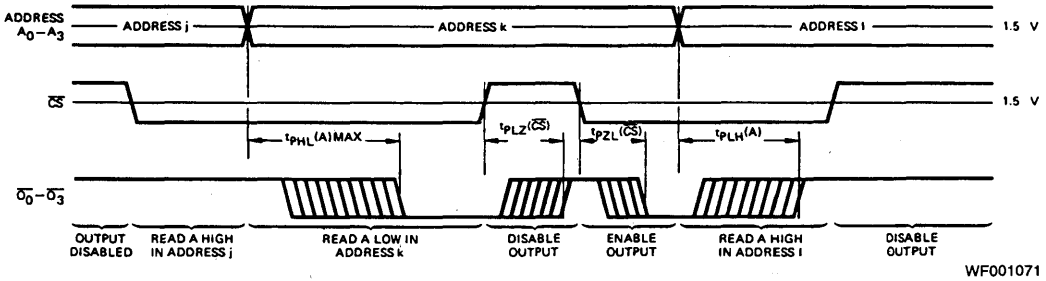
SWITCHING WAVEFORMS



WF001081

Write Mode

Write Cycle Timing. The cycle is initiated by an address change. After t_S(A) Min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) Min. must be allowed before the address may be changed again. The output will be the complement of the data input while the write enable ($\overline{WE}$) is LOW.



WF001071

Read Mode

Switching delays from address and chip select inputs to the data output.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	$t_{PLH}(A)$	9, 10, 11
2	$t_{PHL}(A)$	9, 10, 11
3	$t_{PZL}(\overline{CS})$	9, 10, 11
4	$t_{PZL}(\overline{WE})$	9, 10, 11
5	$t_s(A)$	9, 10, 11
6	$t_h(A)$	9, 10, 11
7	$t_s(DI)$	9, 10, 11
8	$t_h(DI)$	9, 10, 11
9	$t_{pw}(\overline{WE})$	9, 10, 11
10	$t_{PLZ}(\overline{CS})$	9, 10, 11
11	$t_{PLH}(DI)$	9, 10, 11
12	$t_{PHL}(DI)$	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am93L412/93L422

256 x 4-Bit Low-Power TTL Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- High-speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs or with open-collector outputs
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

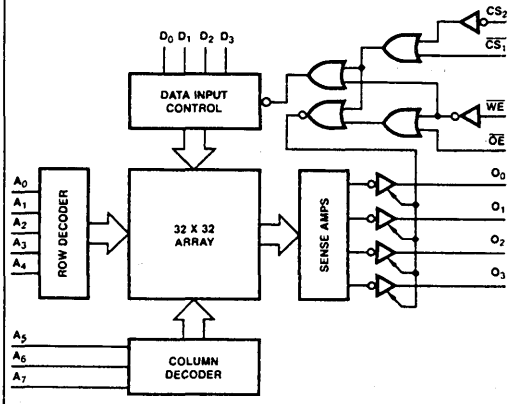
The Am93L412/L422 is comprised of 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 256-word memory of four bits per word. Easy memory expansion is provided by an active-LOW chip select one ($\overline{CS_1}$) and active HIGH chip select two (CS_2) as well as open collector OR tieable outputs (Am93L412) or three-state outputs (Am93L422).

An active-LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write line ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) LOW and the chip select two (CS_2) HIGH and the write line ($\overline{WE}$) HIGH and with the output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3).

The outputs of the memory go to an inactive high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

BLOCK DIAGRAM



BD000600

MODE SELECT TABLE

Input					Output	
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	Mode
L	X	X	X	X	*Hi-Z	Not Select
X	H	X	X	X	*Hi-Z	Not Select
H	L	H	H	X	*Hi-Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*Hi-Z	Write "0"
H	L	L	X	H	*Hi-Z	Write "1"
H	L	L	H	L	Hi-Z	Write "0" Output Disable
H	L	L	H	H	Hi-Z	Write "1" Output Disable

H = HIGH L = LOW X = Don't Care

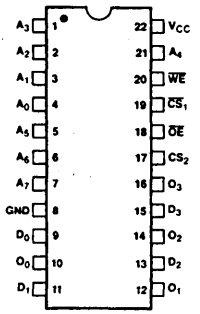
*Hi-Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the Am93L422A/L422 and as output high level for the Am93L412A/L412.

PRODUCT SELECTOR GUIDE

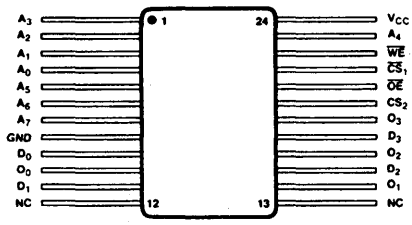
Open-Collector Part Number	Am93L412A	Am93L412A	Am93L412	Am93L412
Three-State Part Number	Am93L422A	Am93L422A	Am93L422	Am93L422
Access Time	45 ns	55 ns	60 ns	75 ns
Temperature Range	C	M	C	M

Publication # 08015 Rev. A Amendment /0
Issue Date: May 1986

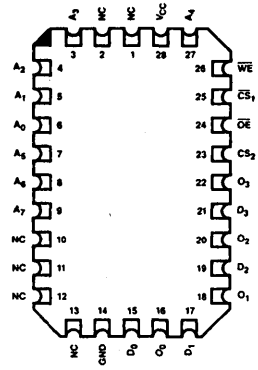
CONNECTION DIAGRAMS
Top View



CD000610



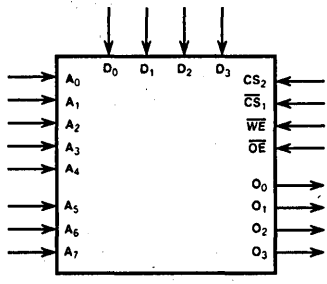
CD001000



CD000620

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

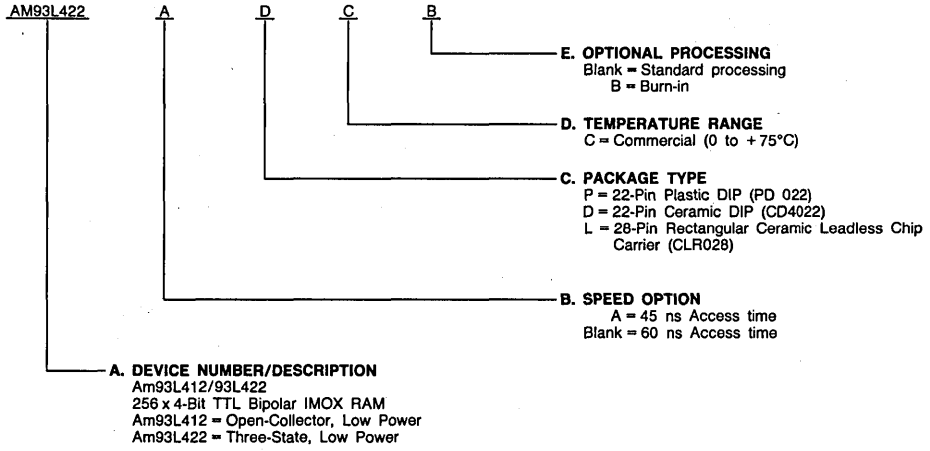


LS000221

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM93L422	PC, PCB, DC, DCB, LC, LCB
AM93L422A	
AM93L412	
AM93L412A	

Valid Combinations

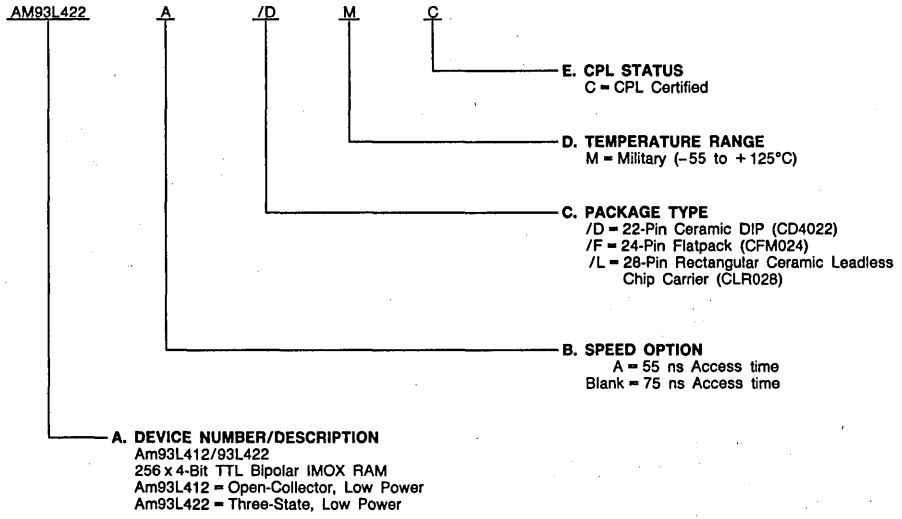
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

3

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for CPL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM93L422	/DMC, /FMC, /LMC
AM93L422A	
AM93L412	
AM93L412A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

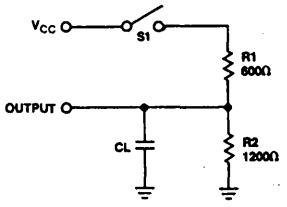
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.350	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs		2.1			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V			−100	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V			1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)		−10		−90	mA
I_{CC}	Power Supply Current	ALL inputs = GND, V_{CC} = Max.	Commercial			80	mA
			Military			90	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −10 mA			−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4 V	Am93L422A/L422		0	50	μA
		V_{OUT} = 0.5 V, V_{CC} = Max.	Am93L422A/L422	−50	0		
		V_{OUT} = 4.5 V	Am93L412A/L412		0	100	
C_{IN}	Input Pin Capacitance	See Note 5			4		pF
C_{OUT}	Output Pin Capacitance	See Note 5			7		pF

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Applies only to devices with three-state outputs (Am93L422 family).
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Input and output capacitance measured on a sample basis @ f = 1.0 MHz at initial characterization.
6. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_j.
$\theta_{jA} \cong 66^{\circ}C/W$ (with moving air) for Ceramic DIP.
$\theta_{jC} \cong 18^{\circ}C/W$ for Flatpack and Leadless Chip Carrier.

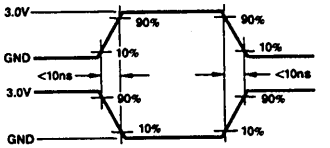
*See the last page of this spec for Group A Subgroup testing information.

SWITCHING TEST CIRCUIT



TC000200

SWITCHING TEST WAVEFORMS



TW000040

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

*See notes after Switching Characteristics.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

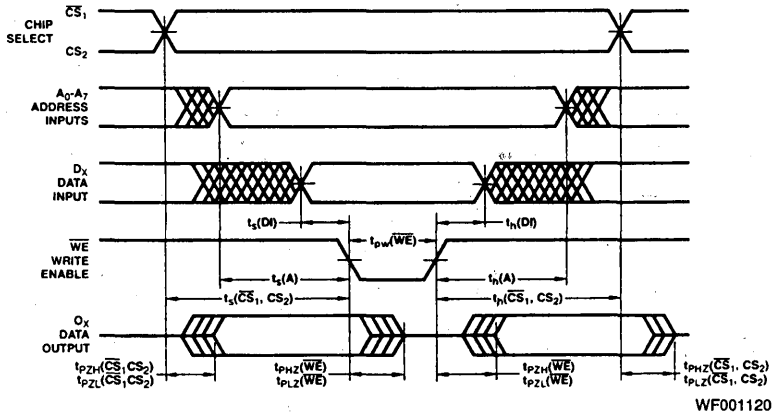
No.	Parameter Symbol	Parameter Description	Am93L412A/L422A				Am93L412/L422				Units
			C devices		M devices		C devices		M devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PLH}(A)(Note 2)	Delay from Address to Output (Address Access Time)		45		55		60		75	ns
2	t_{PHL}(A)(Note 2)										
3	$t_{PZH}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Active Output and Correct Data		30		40		35		45	ns
4	$t_{PZL}(\overline{CS_1}, CS_2)$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		40		45		45		50	ns
6	$t_{PZL}(\overline{WE})$										
7	$t_{PZH}(\overline{OE})$	Delay from Output Enable to Active Output and Correct Data		30		40		35		45	ns
8	$t_{PZL}(\overline{OE})$										
9	t_s(A)	Setup Time Address (Prior to Initiation of Write)	5		10		10		10		ns
10	t_h(A)	Hold Time Address (After Termination of Write)	5		5		5		10		ns
11	t_s(DI)	Setup Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
12	t_h(DI)	Hold Time Data Input (After Termination of Write)	5		5		5		5		ns
13	$t_s(\overline{CS_1}, CS_2)$	Setup Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
14	$t_h(\overline{CS_1}, CS_2)$	Hold Time Chip Select (After Termination of Write)	5		5		5		10		ns
15	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	35		40		45		55		ns
16	$t_{PHZ}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Inactive Output (Hi-Z)		30		40		35		45	ns
17	$t_{PLZ}(\overline{CS_1}, CS_2)$										
18	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		35		40		40		45	ns
19	$t_{PLZ}(\overline{WE})$										
20	$t_{PHZ}(\overline{OE})$	Delay from Output Enable to Inactive Output (Hi-Z)		30		40		35		45	ns
21	$t_{PLZ}(\overline{OE})$										

Notes:
1. For AC and Functional Testing, $V_{IH} = 3.0$ V and $V_{IL} = 0.0$ V.
2. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. For open collector devices, all delays from Write Enable ($\overline{WE}$) or selects ($\overline{CS_1}$, CS_2, $\overline{OE}$) inputs to the Data Output ($O_0 - O_3$) ($t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$, $t_{PLZ}(\overline{OE})$ $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$) are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.
4. For three-state output devices, $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}\ CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with S_1 open and $C_L \leqslant 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with S_1 closed and $C_L \leqslant 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

*See the last page of this spec for Group A Subgroup testing information.

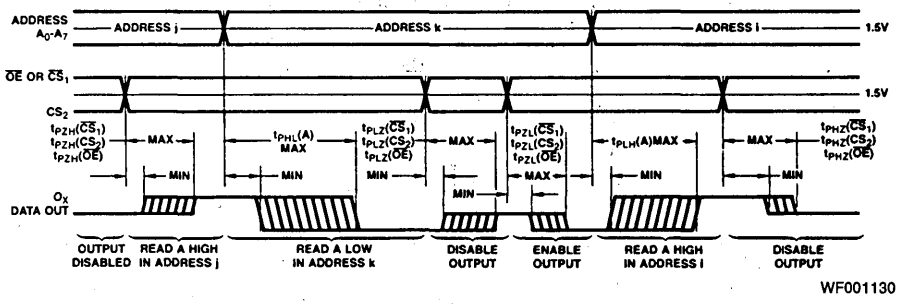
3

SWITCHING WAVEFORMS



WF001120

Diagram A. Write Mode (With $\overline{OE}$ = LOW)



WF001130

Diagram B. Read Mode

Switching delays form address input, output enable input and the chip select inputs to the data output. For the Am93422A/422 disabled output is OFF, represented by a single center line. For the Am93L412A/412, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	$t_{PLH}(A)$	9, 10, 11	12	$t_h(DI)$	9, 10, 11
2	$t_{PHL}(A)$	9, 10, 11	13	$t_s(\overline{CS_1}, CS_2)$	9, 10, 11
3	$t_{PZH}(\overline{CS_1}, CS_2)$	9, 10, 11	14	$t_h(\overline{CS_1}, CS_2)$	9, 10, 11
4	$t_{PZL}(\overline{CS_1}, CS_2)$	9, 10, 11	15	$t_{PW}(\overline{WE1})$	9, 10, 11
5	$t_{PZH}(\overline{WE})$	9, 10, 11	16	$t_{PHZ}(\overline{CS_1}, CS_2)$	9, 10, 11
6	$t_{PZL}(\overline{WE})$	9, 10, 11	17	$t_{PLZ}(\overline{CS_1}, CS_2)$	9, 10, 11
7	$t_{PZH}(\overline{OE})$	9, 10, 11	18	$t_{PHZ}(\overline{WE})$	9, 10, 11
8	$t_{PZL}(\overline{OE})$	9, 10, 11	19	$t_{PLZ}(\overline{WE})$	9, 10, 11
9	$t_S(A)$	9, 10, 11	20	$t_{PHZ}(\overline{OE})$	9, 10, 11
10	$t_h(A)$	9, 10, 11	21	$t_{PLZ}(\overline{OE})$	9, 10, 11
11	$t_s(DI)$	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am93412/93422

256 x 4-Bit TTL Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- High-speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs or with open-collector outputs
- Power dissipation decreases with increasing temperature

GENERAL DESCRIPTION

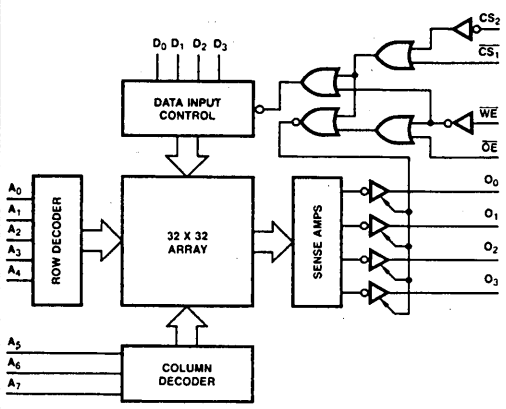
The Am93412/22 is comprised of 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and is ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 256-word memory of four bits per word. Easy memory expansion is provided by an active-LOW chip select one ($\overline{CS_1}$) and active HIGH chip select two (CS_2) as well as open collector OR tieable outputs (Am93412) or three-state outputs (Am93422).

An active-LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write line ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) LOW and the chip select two (CS_2) HIGH and the write line ($\overline{WE}$) HIGH and with the output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3).

The outputs of the memory go to an inactive high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

BLOCK DIAGRAM



BD000600

MODE SELECT TABLE

Input					Output	
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	Mode
L	X	X	X	X	*Hi-Z	Not Select
X	H	X	X	X	*Hi-Z	Not Select
H	L	H	H	X	*Hi-Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*Hi-Z	Write "0"
H	L	L	X	H	*Hi-Z	Write "1"
H	L	L	H	L	*Hi-Z	Write "0" Output Disable
H	L	L	H	H	*Hi-Z	Write "1" Output Disable

H = HIGH L = LOW X = Don't Care

*Hi-Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the Am93422A/422 and as output high level for the Am93412A/412.

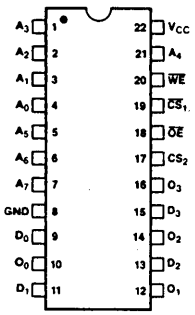
PRODUCT SELECTOR GUIDE

Open-Collector Part Number	Am93412A	Am93412	Am93412A	Am93412
Three-State Part Number	Am93422A	Am93422	Am93422A	Am93422
Access Time	35 ns	45 ns		60 ns
Temperature Range	C	C	M	M

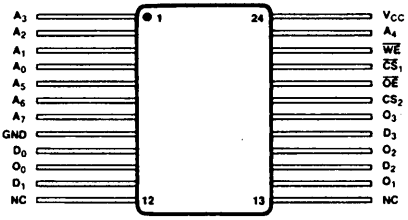
IMOX is a trademark of Advanced Micro Devices, Inc.

Publication # 03080 Rev. C Amendment /0
Issue Date: May 1986

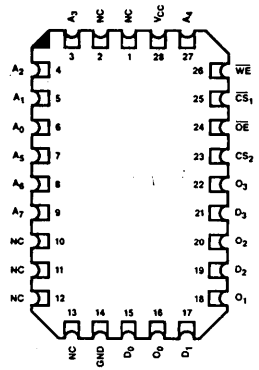
CONNECTION DIAGRAMS
Top View



CD000610



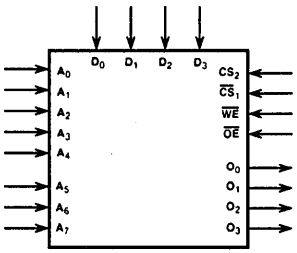
CD001000



CD000620

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

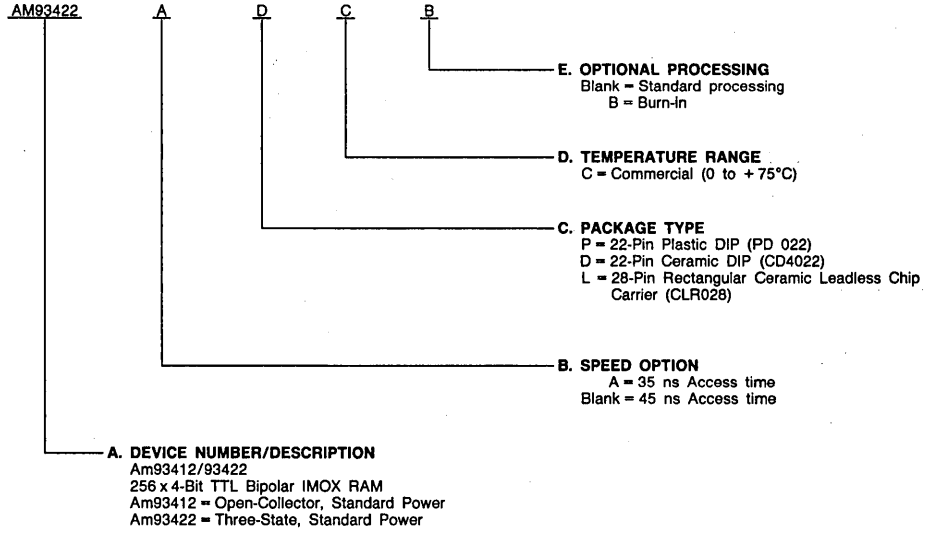


LS000221

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM93422	PC, PCB, DC, DCB, LC, LCB
AM93422A	
AM93412	
AM93412A	

Valid Combinations

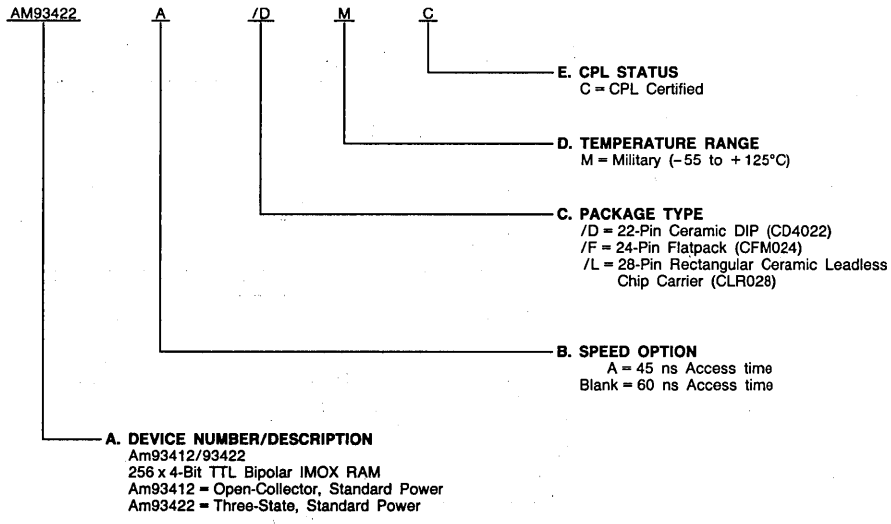
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for CPL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM93422	/DMC, /FMC, /LMC
AM93422A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 6)

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

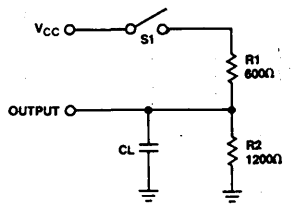
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.350	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs		2.1			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V			−100	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V			1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 4)		−10		−90	mA
I_{CC}	Power Supply Current	ALL inputs = GND, V_{CC} = Max.	Commercial			155	mA
			Military			170	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −10 mA			−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4 V	Am93422A/422		0	50	μA
		V_{OUT} = 0.5 V, V_{CC} = Max.	Am93422A/422	−50	0		
		V_{OUT} = 4.5 V	Am93412A/412		0	100	
C_{IN}	Input Pin Capacitance	See Note 5			4		pF
C_{OUT}	Output Pin Capacitance	See Note 5			7		pF

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Applies only to devices with three-state outputs (Am93422 family).
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Input and output capacitance measured on a sample basis @ f = 1.0 MHz at initial characterization.
6. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
   $\theta_{JA} \cong 60°C/W$ (with moving air) for Ceramic DIP.
   $\theta_{JC} \cong 36°C/W$ for Flatpack and Leadless Chip Carrier.

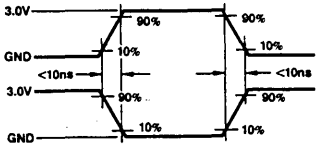
*See the last page of this spec for Group A Subgroup testing information.

SWITCHING TEST CIRCUIT



TC000200

SWITCHING TEST WAVEFORMS



TW000040

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

*See notes after Switching Characteristics.

3

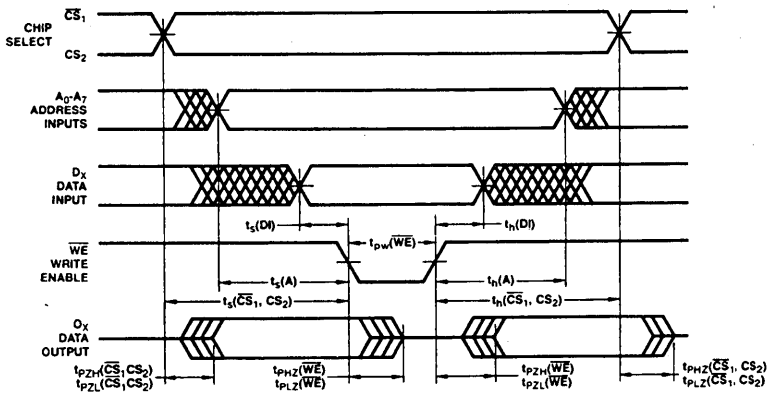
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93412A/93422A				Am93412/93422				Units
			C Devices		M Devices		C Devices		M Devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PLH}(A)(Note 2)	Delay from Address to Output (Address Access Time)		35		45		45		60	ns
2	t_{PHL}(A)(Note 2)										
3	$t_{PZH}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Active Output and Correct Data		25		35		30		45	ns
4	$t_{PZL}(\overline{CS_1}, CS_2)$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		25		40		40		50	ns
6	$t_{PZL}(\overline{WE})$										
7	$t_{PZH}(\overline{OE})$	Delay from Output Enable to Active Output and Correct Data		25		35		30		45	ns
8	$t_{PZL}(\overline{OE})$										
9	t_s(A)	Setup Time Address (Prior to Initiation of Write)	5		5		10		10		ns
10	t_h(A)	Hold Time Address (After Termination of Write)	5		5		5		5		ns
11	t_s(DI)	Setup Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
12	t_h(DI)	Hold Time Data Input (After Termination of Write)	5		5		5		5		ns
13	$t_s(\overline{CS_1}, CS_2)$	Setup Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
14	$t_h(\overline{CS_1}, CS_2)$	Hold Time Chip Select (After Termination of Write)	5		5		5		5		ns
15	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	20		35		30		40		ns
16	$t_{PHZ}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Inactive Output (Hi-Z)		30		35		30		45	ns
17	$t_{PLZ}(\overline{CS_1}, CS_2)$										
18	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		30		40		35		45	ns
19	$t_{PLZ}(\overline{WE})$										
20	$t_{PHZ}(\overline{OE})$	Delay from Output Enable to Inactive Output (Hi-Z)		30		35		30		45	ns
21	$t_{PLZ}(\overline{OE})$										

Notes:
1. For AC and Functional Testing, $V_{IH} = 3.0$ V and $V_{IL} = 0.0$ V.
2. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
3. For open-collector devices, all delays from Write Enable ($\overline{WE}$) or selects ($\overline{CS_1}$, CS_2, $\overline{OE}$) inputs to the Data Output ($O_0 - O_3$) ($t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$, $t_{PLZ}(\overline{OE})$, $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$) are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.
4. For three-state output devices, $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}\ CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with S_1 open and $C_L \leqslant 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with S_1 closed and $C_L \leqslant 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

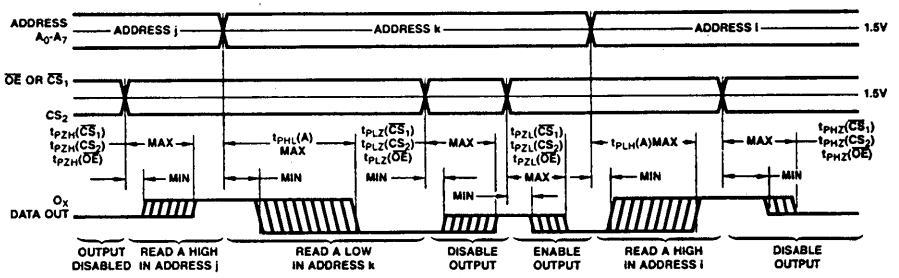
*See the last page of this spec for Group A Subgroup testing information.

SWITCHING WAVEFORMS



WF001120

Write Mode (With $\overline{OE}$ = LOW)



WF001130

Read Mode

Switching delays form address input, output enable input and the chip select inputs to the data output. For the Am93422A/422 disabled output is OFF, represented by a single center line. For the Am93412A/412, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	$t_{PLH}(A)$	9, 10, 11	12	$t_h(DI)$	9, 10, 11
2	$t_{PHL}(A)$	9, 10, 11	13	$t_s(\overline{CS_1}, CS_2)$	9, 10, 11
3	$t_{PZH}(\overline{CS_1}, CS_2)$	9, 10, 11	14	$t_h(\overline{CS_1}, CS_2)$	9, 10, 11
4	$t_{PZL}(\overline{CS_1}, CS_2)$	9, 10, 11	15	$t_{PW}(\overline{WE})$	9, 10, 11
5	$t_{PZH}(\overline{WE})$	9, 10, 11	16	$t_{PHZ}(\overline{CS_1}, CS_2)$	9, 10, 11
6	$t_{PZL}(\overline{WE})$	9, 10, 11	17	$t_{PLZ}(\overline{CS_1}, CS_2)$	9, 10, 11
7	$t_{PZH}(\overline{OE})$	9, 10, 11	18	$t_{PHZ}(\overline{WE})$	9, 10, 11
8	$t_{PZL}(\overline{OE})$	9, 10, 11	19	$t_{PLZ}(\overline{WE})$	9, 10, 11
9	$t_S(A)$	9, 10, 11	20	$t_{PHZ}(\overline{OE})$	9, 10, 11
10	$t_h(A)$	9, 10, 11	21	$t_{PLZ}(\overline{OE})$	9, 10, 11
11	$t_s(DI)$	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am93L415/Am93L425

1024 x 1 Bit TTL Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 1024-word x 1-bit RAMs
- 93L415A/425A has a 35 ns maximum access time, 65 mA I_{CC}
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am93L425 series) or with open-collector outputs (Am93L415 series)
- Plug-in replacement for Fairchild 93L415A/415 and 93L425A/425, and Intel 2115/2125 series

GENERAL DESCRIPTION

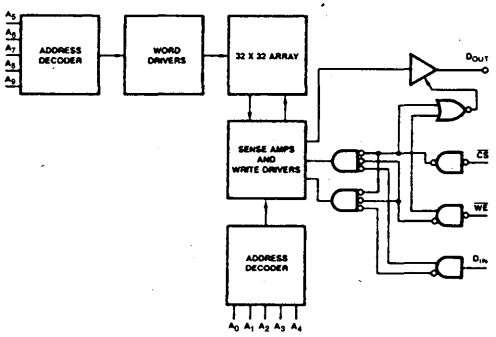
The Am93L415 and Am93L425 are fully decoded 1024 x 1 RAMs built with Schottky diode clamped transistors in conjunction with internal ECL circuitry. They are ideal for use in high-speed control and buffer memory applications. Easy memory expansion is provided by an active LOW chip select input ($\overline{CS}$) and either open-collector (93L415) or three-state (93L425) output. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write lines ($\overline{WE}$) are LOW, the information on the data input (D_{IN}) is written into the addressed memory word and the output circuitry preconditioned so that true data is present at the output when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the reading and writing operation or any time the chip select line is HIGH, the output of the memory goes to an inactive high-impedance state.

BLOCK DIAGRAM



BD000632

MODE SELECT TABLE

Inputs			Output	
CS	WE	D_{IN}	D_{OUT}	Mode
H	X	X	*Hi-Z	Not Selected
L	L	L	*Hi-Z	Write "0"
L	L	H	*Hi-Z	Write "1"
L	H	X	Selected Data	Read

H = HIGH L = LOW X = Don't Care

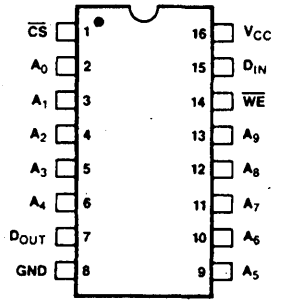
*Hi-Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the Am93L425 series and as an output high level for the Am93L415 series.

PRODUCT SELECTOR GUIDE

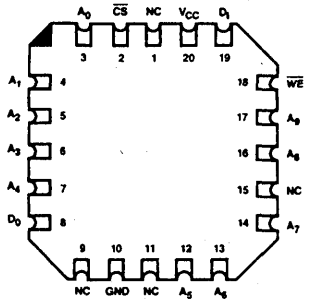
Access Time	35 ns	40 ns	45 ns	55 ns	60 ns
Temperature Range	C	M	C	M	C
Open-Collector	Am93L415SA	Am93L415SA	Am93L415A	Am93L415A	Am93L415
Three-State	Am93L425SA	Am93L425SA	Am93L425A	Am93L425A	Am93L425

Publication # 05850 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD000900



CD000910

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM93L425 SA D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

C. PACKAGE TYPE
P = 16-Pin Plastic DIP (PD 016)
D = 16-Pin Ceramic DIP (CD 016)

B. SPEED OPTION
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
Am93L415/Am93L425
1024 x 1 Bit TTL Bipolar IMOX RAM
Am93L415 = Open-Collector
Am93L425 = Three-State

Valid Combinations	
AM93L415SA	PC, PCB, DC, DCB
AM93L425SA	
AM93L415A	
AM93L425A	
AM93L415	
AM93L425	

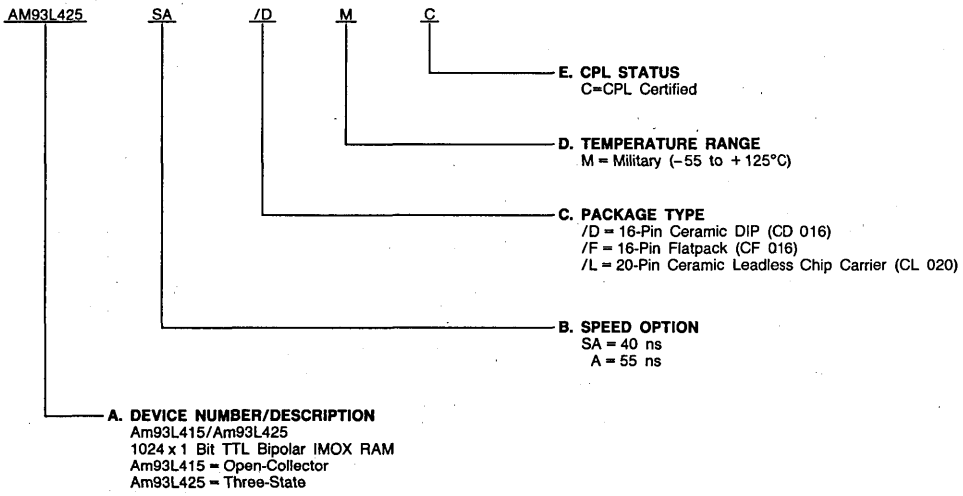
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status



Valid Combinations	
AM93L425SA	/DMC, /FMC, /LMC
AM93L415SA	
AM93L425A	
AM93L415A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

3

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 6)

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

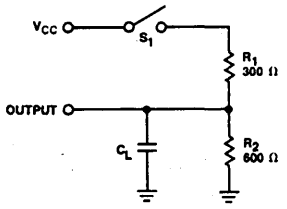
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.33	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs		2.1			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V			−90	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V			1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 5)		−20	−50	−100	mA
I_{CC}	Power Supply Current	All inputs = GND	Commercial			65	mA
		V_{CC} = Max.	Military			75	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −10 mA			−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 2.4 V	Am93L415 Series Only		0	100	μA
			Am93L425 Series Only		0	50	
		$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.5 V, V_{CC} = Max.	Am93L425 Series Only	−50	0		
C_{IN}	Input Pin Capacitance	See Note 4			8		pF
C_{OUT}	Output Pin Capacitance	See Note 4			10		pF

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies only to devices with three-state output. (Am93L425 series)
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Input and output capacitance measured on a sample basis using pulse technique.
5. Duration of the short circuit should not be more than one second.
6. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
   $\theta_{JA} \approx 60°C/W$ (with moving air) for Ceramic DIP.
   $\theta_{JC} \approx 10-17°C/W$ for Flatpack.

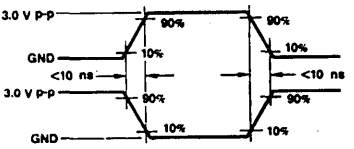
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



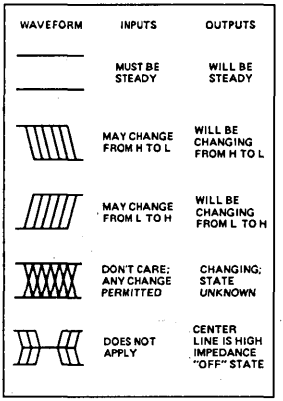
TC000171

SWITCHING TEST WAVEFORM



TW000031

KEY TO SWITCHING WAVEFORMS



KS000010

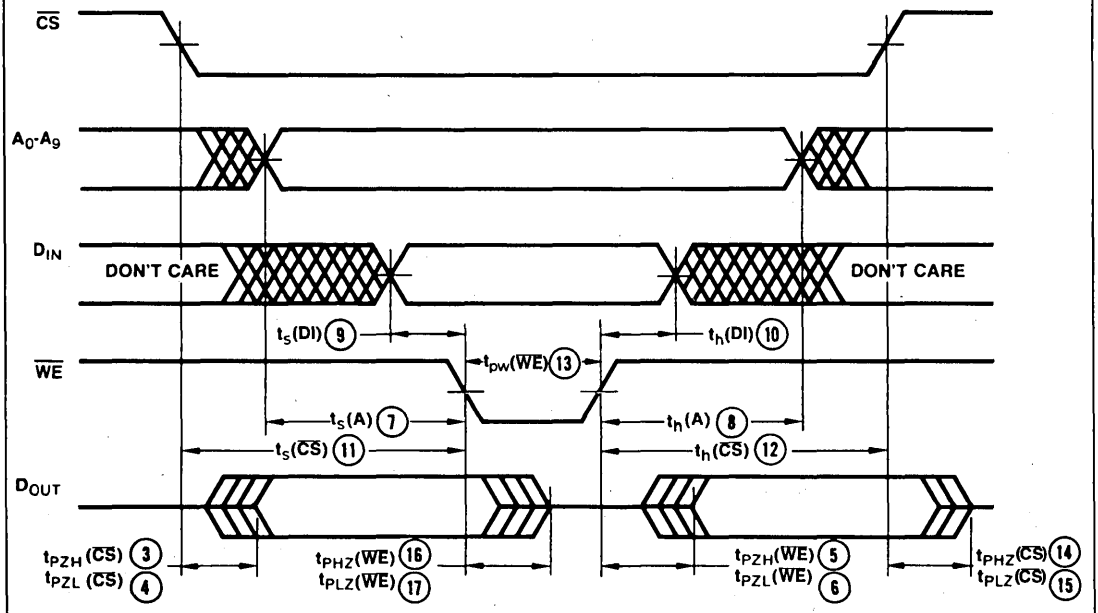
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93L415SA-Am93L425SA COM'L Min.	Am93L415SA-Am93L425SA COM'L Max.	Am93L415SA-Am93L425SA MIL Min.	Am93L415SA-Am93L425SA MIL Max.	Am93L415A-Am93L425A COM'L Min.	Am93L415A-Am93L425A COM'L Max.	Am93L415A-Am93L425A MIL Min.	Am93L415A-Am93L425A MIL Max.	Am93L415/Am93L425 COM'L Min.	Am93L415/Am93L425 COM'L Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output (Note 1)		35		40		45		55		60	ns
2	$t_{PHL}(A)$												
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select to Active Output (Notes 2 and 3)		25		40		30		45		40	ns
4	$t_{PZL}(\overline{CS})$												
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output (Write Recovery) (Note 2 and 3)		20		30		25		35		45	ns
6	$t_{PZL}(\overline{WE})$												
7	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	5		5		5		5		5		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	5		5		5		5		5		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Initiation of Write)	0		5		0		5		5		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	5		5		5		5		5		ns
11	$t_s(\overline{CS})$	Setup Time Chip Select (Prior to Initiation of Write)	5		5		5		5		5		ns
12	$t_h(\overline{CS})$	Hold Time Chip Select (After Termination of Write)	5		5		5		5		5		ns
13	$t_{pw}(\overline{WE})$	Write Enable Pulse Width to Insure Write	25		30		30		45		45		ns
14	$t_{PHZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (Hi-Z) (Notes 2 and 3)		30		35		35		40		40	ns
15	$t_{PLZ}(\overline{CS})$												
16	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z) (Notes 2 and 3)		30		35		35		40		45	ns
17	$t_{PLZ}(\overline{WE})$												

Notes: 1. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
2. For open-collector devices (93L415 series), delays for $\overline{WE}$ and $\overline{CS}$ to either an active or inactive output are measured with S_1 closed and $C_L = 30$ pF; both input and output timing referenced to 1.5 V.
3. For three-state output devices (93L425 series), delays for t_{PZH} and t_{PZL} are measured with $C_L = 30$ pF, S_1 open and S_1 closed, respectively. Both input and output timing are referenced to 1.5 V. Delays for t_{PHZ} with S_1 open and t_{PLZ} with S_1 closed and $C_L \leq 5$ pF are measured between the 1.5 V level on the input and the $V_{OH} - 0.5$ V and $V_{OL} + 0.5$ V level on the output, respectively.

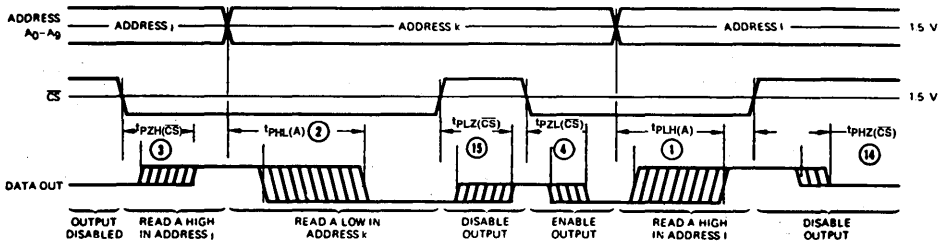
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF001152

Write Mode



WF001742

Read Mode

Switching delays from address and chip select inputs to the data output. For the Am93L425 series, a disabled output is OFF, represented by a single center line. For the Am93L415 series, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	$t_{PLH}(A)$	9, 10, 11	10	$t_h(DI)$	9, 10, 11
2	$t_{PHL}(A)$	9, 10, 11	11	$t_s(\overline{CS})$	9, 10, 11
3	$t_{PZH}(\overline{CS})$	9, 10, 11	12	$t_h(\overline{CS})$	9, 10, 11
4	$t_{PZL}(\overline{CS})$	9, 10, 11	13	$t_{pw}(\overline{WE})$	9, 10, 11
5	$t_{PZH}(\overline{WE})$	9, 10, 11	14	$t_{PHZ}(\overline{CS})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$	9, 10, 11	15	$t_{PLZ}(\overline{CS})$	9, 10, 11
7	$t_s(A)$	9, 10, 11	16	$t_{PLZ}(\overline{WE})$	9, 10, 11
8	$t_h(A)$	9, 10, 11	17	$t_{PHZ}(\overline{WE})$	9, 10, 11
9	$t_s(DI)$	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am93415/Am93425

1024 x 1 Bit TTL Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 1024-word x 1-bit RAMs
- Ultra-high speed (SA) version:
  Address Access time 20 ns
  High Speed (A) version:
  Address Access time 30 ns
  Standard version:
  Address Access time 45 ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am93425 series) or with open-collector outputs (Am93415 series)
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Plug in replacement for Fairchild 93415A/415 and 93425A/425, and Intel 2115/2125 series
- I_{CC} decreases as temperature increases

GENERAL DESCRIPTION

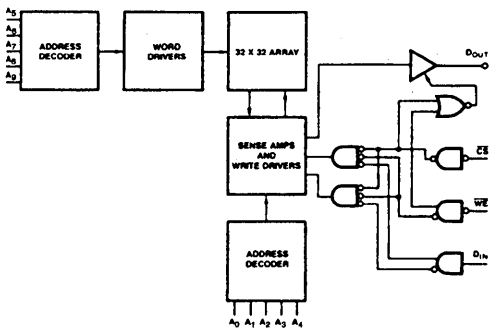
The Am93415 and Am93425 are fully decoded 1024 x 1 RAMs built with Schottky diode clamped transistors in conjunction with internal ECL circuitry. They are ideal for use in high-speed control and buffer memory applications. Easy memory expansion is provided by an active LOW chip select input ($\overline{CS}$) and either open-collector or three-state outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the data input (D_{IN}) is written into the addressed memory word and the output circuitry preconditioned so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or any time the chip select line is HIGH, the output of the memory goes to an inactive high-impedance state.

BLOCK DIAGRAM



BD000632

MODE SELECT TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	*Hi-Z	Not Selected
L	L	L	*Hi-Z	Write "0"
L	L	H	*Hi-Z	Write "1"
L	H	X	Selected Data	Read

H = HIGH L = LOW X = Don't Care

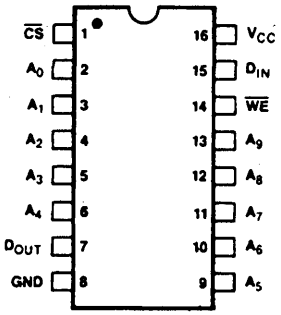
*Hi-Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the Am93425 series and as an output high level for the Am93415 series.

PRODUCT SELECTOR GUIDE

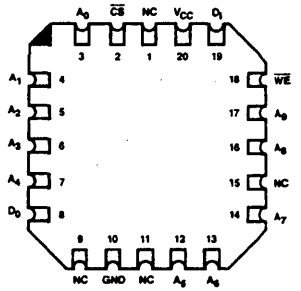
Access Time	20 ns	30 ns		40 ns	45 ns
Temperature Range	C	C	M	M	C
Open-Collector	Am93415SA	Am93415A	Am93415SA	Am93415A	Am93415A
Three-State	Am93425SA	Am93425A	Am93425SA	Am93425A	Am93425

Publication # 03195 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD000900



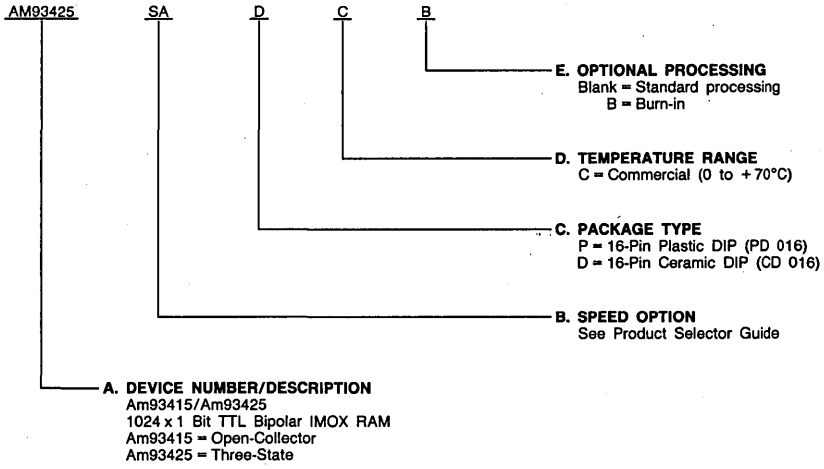
CD000910

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM93415SA	PC, PCB, DC, DCB
AM93425SA	
AM93415A	
AM93425A	
AM93415	
AM93425	

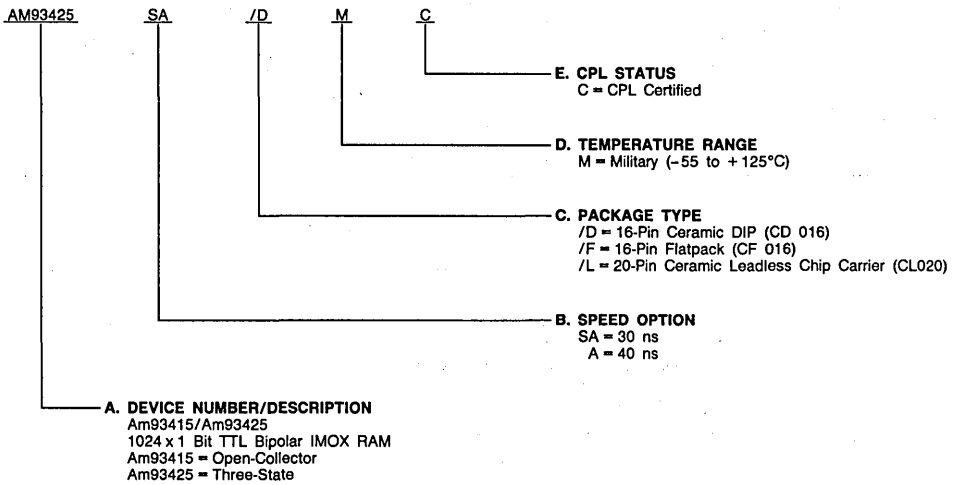
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status



Valid Combinations	
AM93425SA	/DMC, /FMC, /LMC
AM93415SA	
AM93425A	
AM93415A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +V_{CC} Max.
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 6)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

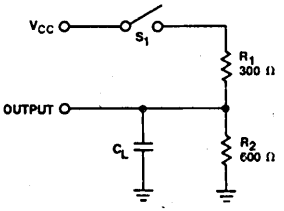
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −10.3 mA	COM'L	2.4	3.4		Volts
			I_{OH} = −5.2 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 16 mA		0.33	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.1			Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V				−90	−400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V				1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 5)			−20	−50	−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.	SA Device				150	mA
			A and STD Devices				125	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −10 mA				−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4 V		Am93415 Series Only		0	100	μA
				Am93425 Series Only		0	50	
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.5 V, V_{CC} = Max.		Am93425 Series Only	−50	0		
C_{IN}	Input Pin Capacitance	See Note 4				8		pF
C_{OUT}	Output Pin Capacitance	See Note 4				10		pF

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. This applies only to devices with three-state output. (Am93L425 series)
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Input and output capacitance measured on a sample basis using pulse technique.
5. Duration of the short circuit test should not be more than one second.
6. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where T_A = T_C = T_J.
$\theta_{JA} \approx 60°/w$ (with moving air) for CeramicDIP.
$\theta_{JC} \approx 10 - 17°/w$ for Flatpack.

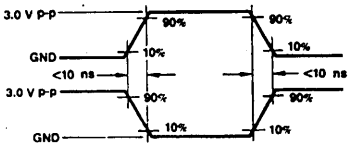
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUIT



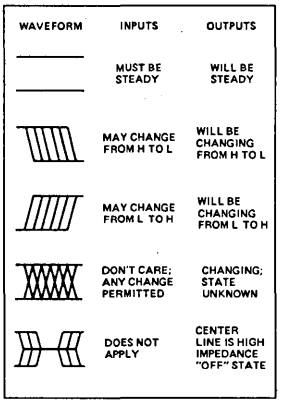
TC000171

SWITCHING TEST WAVEFORM



TW000031

KEY TO SWITCHING WAVEFORMS



KS000010

See notes 1, 2 and 3 of Switching Characteristics.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93415SA/25SA				Am93415A/25A				Units
			C devices		M devices		C devices		M devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PLH}(A)	Delay from Address to Output		20		30		30		40	ns
2	t_{PHL}(A)										
3	$t_{PZH}\overline{CS}$	Delay from Chip Select to Active Output and Correct Data		15		25		20		30	ns
4	$t_{PZL}\overline{CS}$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		15		25		25		35	ns
6	$t_{PZL}(\overline{WE})$										
7	t_s(A)	Setup Time Address (Prior to Initiation of Write)	5		5		5		5		ns
8	t_h(A)	Hold Time Address (After Termination of Write)	0		5		5		5		ns
9	t_s(DI)	Setup Time Data Input (Prior to Initiation of Write)	0		5		5		5		ns
10	t_h(DI)	Hold Time Data Input (After Termination of Write)	0		5		5		5		ns
11	$t_s(\overline{CS})$	Setup Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
12	$t_h(\overline{CS})$	Hold Time Chip Select (After Termination of Write)	0		5		5		5		ns
13	$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	15		25		20		30		ns
14	$t_{PHZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (Hi-Z)		20		30		20		30	ns
15	$t_{PLZ}(\overline{CS})$										
16	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		15		25		20		30	ns
17	$t_{PLZ}(\overline{WE})$										

*See the last page of this spec for Group A Subgroup Testing information.

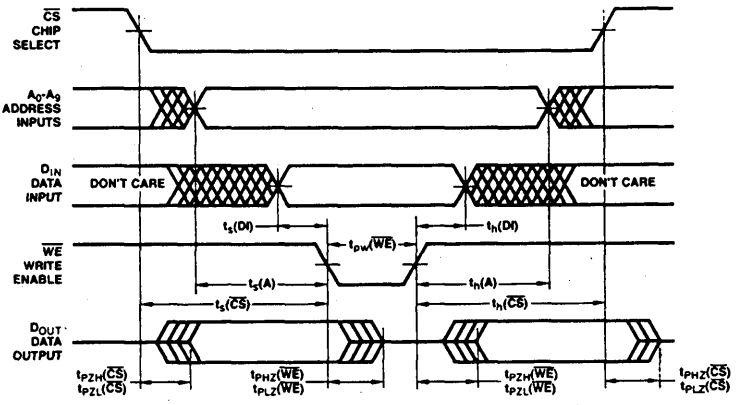
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am93415/25 C devices Min.	Am93415/25 C devices Max.	Units
1	$t_{PLH}(A)$	Delay from Address to Output (Address Access Time)		45	ns
2	$t_{PHL}(A)$				
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data		35	ns
4	$t_{PZL}(\overline{CS})$				
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		40	ns
6	$t_{PZL}(\overline{WE})$				
7	$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	10		ns
8	$t_h(A)$	Hold Time Address (After Termination of Write)	5		ns
9	$t_s(DI)$	Setup Time Data Input (Prior to Initiation of Write)	5		ns
10	$t_h(DI)$	Hold Time Data Input (After Termination of Write)	5		ns
11	$t_s(\overline{CS})$	Setup Time Chip Select (Prior to Initiation of Write)	5		ns
12	$t_h(\overline{CS})$	Hold Time Chip Select (After Termination of Write)	5		ns
13	$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	30		ns
14	$t_{PHZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (Hi-Z)		35	ns
15	$t_{PLZ}(\overline{CS})$				
16	$t_{PHZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (Hi-Z)		35	
17	$t_{PLZ}(\overline{WE})$				

Notes:
1. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30$ pF with both input and output timing referenced to 1.5 V.
2. For open-collector devices (Am93415 series), all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CE}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30$ pF; and with both the input and output timing referenced to 1.5 V.
3. For three-state output devices (Am93425 series), $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, $C_L = 30$ pF and with both the input and output timing referenced to 1.5 V. $t_{HZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leqslant 5$ pF and are measured between the 1.5 V level on the input to the $V_{OH} - 500$ mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leqslant 5$ pF and are measured between the 1.5 V level on the input and the $V_{OL} + 500$ mV level on the output.

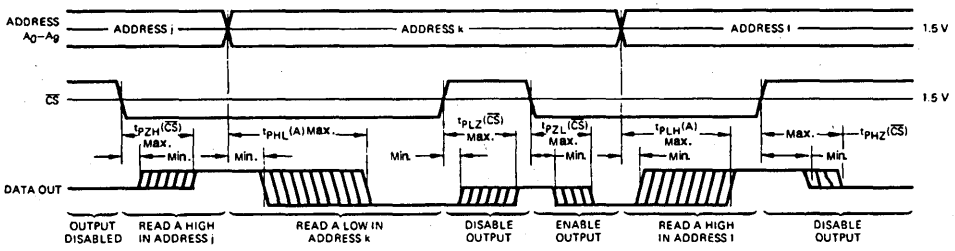
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF001150

Write Mode



WF001141

Switching delays from address and chip select inputs to the data output. For the Am93425SA/A/425, disabled output is OFF, represented by a single center line. For the Am93415SA/A/415, a disabled output is HIGH.

Read Mode

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	$t_{PLH}(A)$	9, 10, 11	10	$t_h(DI)$	9, 10, 11
2	$t_{PHL}(A)$	9, 10, 11	11	$t_s(\overline{CS})$	9, 10, 11
3	$t_{PZH}(\overline{CS})$	9, 10, 11	12	$t_h(\overline{CS})$	9, 10, 11
4	$t_{PZL}(\overline{CS})$	9, 10, 11	13	$t_{pw}(\overline{WE})$	9, 10, 11
5	$t_{PZH}(\overline{WE})$	9, 10, 11	14	$t_{PHZ}(\overline{CS})$	9, 10, 11
6	$t_{PZL}(\overline{WE})$	9, 10, 11	15	$t_{PLZ}(\overline{CS})$	9, 10, 11
7	$t_s(A)$	9, 10, 11	16	$t_{PLZ}(\overline{WE})$	9, 10, 11
8	$t_h(A)$	9, 10, 11	17	$t_{PHZ}(\overline{WE})$	9, 10, 11
9	$t_s(DI)$	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am93L469

512 x 9 TTL Low-Power Tag Buffer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 45-ns address to comparator output (MATCH)
- Replaces six or more integrated circuits with a single device
- On-chip parity generator and checker
- One-third power consumption of the Am93469
- Fully TTL compatible
- Integrated reset feature

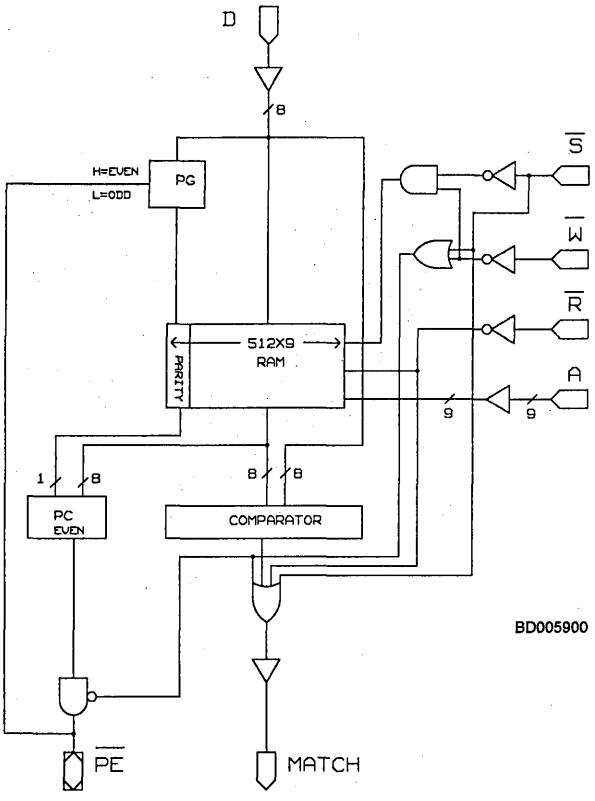
GENERAL DESCRIPTION

The Am93L469 Low-Power Tag Buffer combines a 512 x 9 memory with a comparator. An internal parity generator and parity checker guarantee that no misoperation occurs.

The device has three operational modes: Compare, Write, and Reset. In Compare mode, data is compared to the contents of an address location. Write mode is used to store data. Reset mode is used to clear a single 'valid bit' stream.

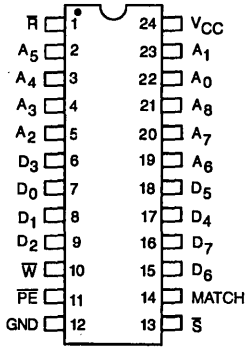
The Tag Buffer is designed to be used in a cache memory system for the translation of virtual addresses to physical addresses. The device can also be used in the directory and data cache. It offers state-of-the-art technology performance, while combining the functions of six or more integrated circuits into a single device.

BLOCK DIAGRAM



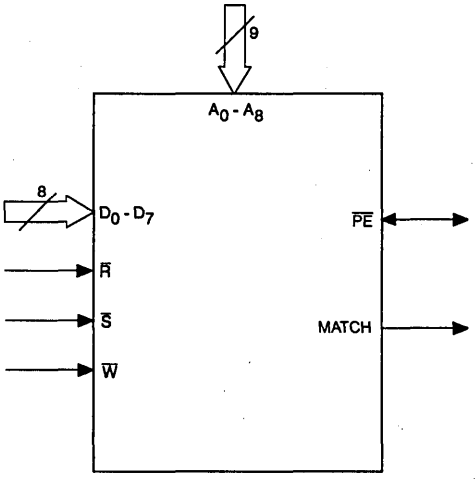
Publication # 08002 | Rev. B | Amendment /0
Issue Date: June 1986

CONNECTION DIAGRAM
Top View



CD009152

LOGIC SYMBOL



LS002201

V_{CC} = Positive Power Supply
GND = Ground

3

PIN DESCRIPTION

A_0–A_8 Address (Inputs)
Identifies memory locations.

D_0–D_7 Data (Inputs)
During Compare cycle, eight bits of data are compared with address location given by A_0–A_8 for equality. The result is indicated on the Comparator output pin, MATCH. When $\overline{W}$ is LOW, data is written into the address location given by A_0–A_8.

$\overline{R}$ Reset (Input, Active LOW)
Resets D_3 to zero (all 512 locations).

$\overline{S}$ Chip Select (Input, Active LOW)
When $\overline{S}$ is LOW, the device is activated. A HIGH on this input will disable the chip and force $\overline{PE}$ and MATCH outputs HIGH, allowing easy vertical expansion.

$\overline{W}$ Write Enable (Input, Active LOW)
Must be LOW to write Data (D_0–D_7) into location given by A_0–A_8. MATCH is output HIGH during Write cycle.

MATCH Comparator Match (Output, Active HIGH)
HIGH when Data (D_0–D_7) equals content of memory location specified by A_0–A_8. LOW when mismatch occurs.

$\overline{PE}$ Parity Error (Input/Output, Active LOW)
LOW when the nine bits of internal data do not constitute even parity. If held LOW during Write Cycle, odd parity will be generated, forcing a parity error for that address upon input.

FUNCTIONAL DESCRIPTION

The Am93L469 Low-Power Tag Buffer has three modes of operation: Compare, Write, and Reset. These modes are described as follows.

Compare Mode

The eight bits of Data inputs are compared with the content of a given memory location for equality. The nine address inputs define each memory location. In this mode, $\overline{W}$ and $\overline{R}$ inputs are HIGH, and $\overline{S}$ is LOW. If the eight bits of Data inputs are exactly the same as the eight bits of data in the given memory location, the MATCH output will be HIGH. If not, the MATCH output will be LOW. The parity bit is not compared.

Write Mode

The eight bits of data inputs and the one bit of parity are written into the RAM array when both $\overline{S}$ and $\overline{W}$ are LOW, and $\overline{R}$ is HIGH. The MATCH output is forced HIGH (the MATCH output is associated with the output enable of the data cache). Holding the Parity Error ($\overline{PE}$) LOW forces a Parity Error to be output during the later compare cycles.

Reset Mode

When $\overline{R}$ = LOW, $\overline{S}$ = LOW, and $\overline{W}$ = HIGH, a dedicated section of the entire array, D_3, is reset to LOW. The $\overline{PE}$ output is forced LOW during reset. The MATCH output is forced HIGH. All 512 D_3 data bits are reset to a low state. The other seven bits in each address location may change to an undetermined state (HIGH or LOW).

TABLE 1. FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	
$\overline{S}$	$\overline{W}$	$\overline{R}$	$\overline{PE}$ (Note 1)	MATCH (Note 2)	DESCRIPTION
H	X	X	Input Output Disabled	H (Forced)	Chip Disabled
L	H	H	Output H = No Parity Error L = Parity Error	H = MATCH L = MISS	Compare
L	H	L	Output L	H (Forced)	Reset
L	L	H	Input H = Even Parity L = Odd Parity	H (Forced)	Write
L	L	L	Input Output Disabled	H (Forced)	Illegal

Note: 1. $\overline{PE}$ is an open-collector output, requiring an external Pull-up Resistor.
2. Match is an open-collector output, requiring an external Pull-up Resistor.

Key: H = HIGH
L = LOW
X = Don't Care

TABLE 2. COMPARE CYCLE OUTPUT DESCRIPTION

MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error or After Reset
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 to V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

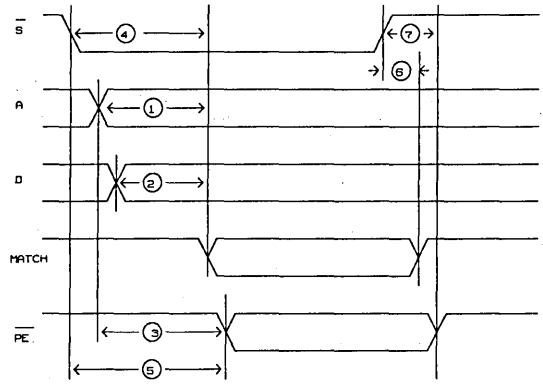
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OL} (MATCH)	Output LOW Voltage	I_{OL} = 18 mA		0.45	V
V_{OL} ($\overline{PE}$)	Output LOW Voltage	I_{OL} =12 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
V_{CL}	Input Clamp Voltage	I_{IN} = −10 mA		−1.5	V
I_{IL}	Input LOW Current	V_{IN} = 0 to 5.5 V		100	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V		40	μA
I_{CC}	Supply Current			80	mA

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

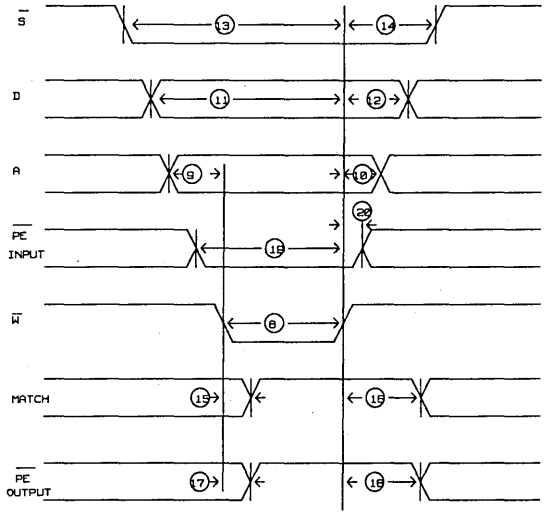
No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
Compare Mode					
1	t_{AVMV}	Address to MATCH		45.0	ns
2	t_{DVMV}	Data to MATCH		25.0	ns
3	t_{AVPV}	Address to $\overline{PE}$		55.0	ns
4	t_{SLMV}	$\overline{S}$ to MATCH		25.0	ns
5	t_{SLPV}	$\overline{S}$ to $\overline{PE}$		25.0	ns
6	t_{SHMH}	$\overline{S}$ to MATCH Recovery		25.0	ns
7	t_{SHPH}	$\overline{S}$ to $\overline{PE}$ Recovery		25.0	ns
Write Mode					
8	t_{WLWH}	Write Pulse Width	45.0		ns
9	t_{AVWL}	Address Setup	5.0		ns
10	t_{WHAX}	Address to $\overline{W}$ Hold	5.0		ns
11	t_{DVWH}	Data to $\overline{W}$ Setup	40.0		ns
12	t_{WHDX}	Data to $\overline{W}$ Hold	5.0		ns
13	t_{SLWH}	$\overline{S}$ to Setup	40.0		ns
14	t_{WHSH}	$\overline{S}$ to Select Hold	5.0		ns
15	t_{WLMH}	$\overline{W}$ to MATCH		20.0	ns
16	t_{WHMV}	Write Recovery (MATCH)		45.0	ns
17	t_{WLPH}	$\overline{W}$ to $\overline{PE}$		20.0	ns
18	t_{WHPV}	Write Recovery ($\overline{PE}$)		45.0	ns
19	t_{PVWH}	$\overline{PE}$ Input to $\overline{W}$ Setup		40.0	ns
20	t_{WHPH}	$\overline{PE}$ Input to $\overline{W}$ Hold		5.0	ns
Reset Mode					
21	t_{RLRH}	$\overline{R}$ Pulse Width	60.0		ns
22	t_{SLRL}	$\overline{S}$ to $\overline{R}$ Setup	5.0		ns
23	t_{RHSH}	$\overline{S}$ to $\overline{R}$ Hold	5.0		ns
24	t_{WHRL}	$\overline{W}$ to $\overline{R}$ Setup	5.0		ns
25	t_{RHWL}	$\overline{W}$ to $\overline{R}$ Hold	5.0		ns
26	t_{RLMH}	$\overline{R}$ to MATCH HIGH		15.0	ns
27	t_{RHMX}	$\overline{R}$ to MATCH Recovery		40.0	ns

Notes: 1. All Switching Characteristics are measured at 50% of input to valid output. Both input and output timings are referenced to 1.5 V.

SWITCHING WAVEFORMS (Cont'd)

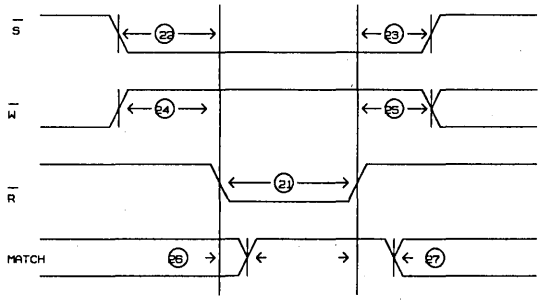


Compare Mode



Write Mode

SWITCHING WAVEFORMS



Reset Mode

Am93469

512 x 9 TTL Tag Buffer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast address to comparator output (MATCH)
- Replaces six or more integrated circuits with a single device
- On-chip parity generator and checker
- Easy horizontal and vertical expansion
- Fully TTI compatible
- Integrated reset feature
- 24-pin Ceramic DIP (300 Mil) and Flatpack packages

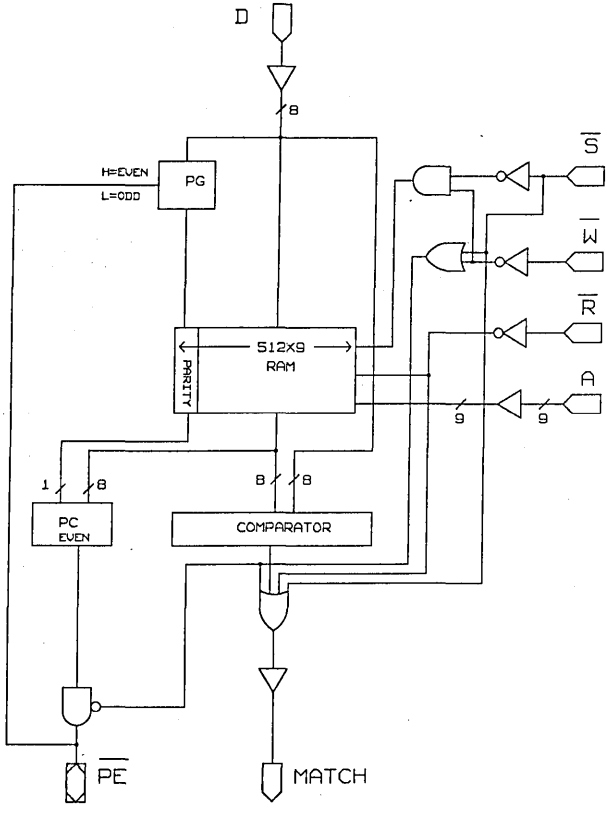
GENERAL DESCRIPTION

The Am93469 Tag Buffer combines a 512 x 9 memory with a comparator. An internal parity generator and parity checker guarantee that no misoperation occurs.

The device has three operational modes: Compare, Write, and Reset. In Compare mode, data is compared to the contents of an address location. Write mode is used to store data. Reset mode is used to clear a single 'valid bit' stream.

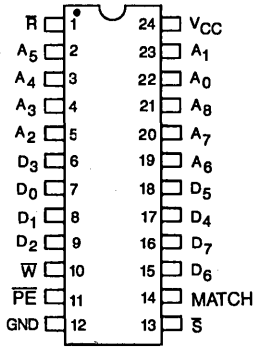
The Tag Buffer is designed to be used in a cache memory system for the translation of virtual addresses to physical addresses. The device can also be used in the directory and data cache. It offers state-of-the-art technology performance, while combining the functions of six or more integrated circuits into a single device.

BLOCK DIAGRAM



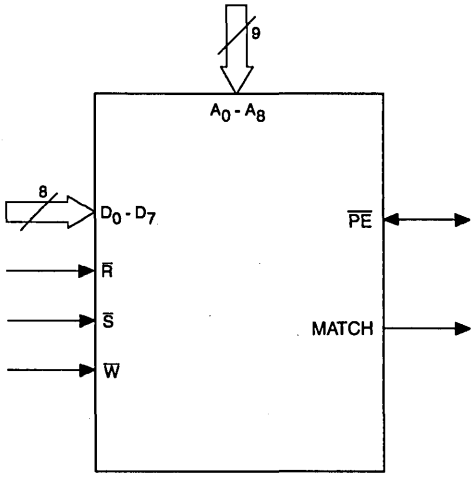
Publication # 07562B | Rev. A | Amendment /0
Issue Date: June 1986

CONNECTION DIAGRAM
Top View



CD009152

LOGIC SYMBOL



LS002201

V_{CC} = Positive Power Supply
GND = Ground

PIN DESCRIPTION

A_0–A_8 Address (Inputs)
Identifies memory locations.

D_0–D_7 Data (Inputs)
During Compare cycle, eight bits of data are compared with address location given by A_0–A_8 for equality. The result is indicated on the Comparator output pin, MATCH. When $\overline{W}$ is LOW, data is written into the address location given by A_0–A_8.

$\overline{R}$ $\overline{\text{Reset}}$ (Input, Active LOW)
Resets D_3 to zero (all 512 locations).

$\overline{S}$ $\overline{\text{Chip Select}}$ (Input, Active LOW)
When $\overline{S}$ is LOW, the device is activated. A HIGH on this input will disable the chip and force $\overline{PE}$ and MATCH outputs HIGH, allowing easy vertical expansion.

$\overline{W}$ $\overline{\text{Write Enable}}$ (Input, Active LOW)
Must be LOW to write Data (D_0–D_7) into location given by A_0–A_8. MATCH is output HIGH during Write cycle.

MATCH Comparator Match (Output, Active HIGH)
HIGH when Data (D_0–D_7) equals content of memory location specified by A_0–A_8. LOW when mismatch occurs.

$\overline{PE}$ $\overline{\text{Parity Error}}$ (Input/Output, Active LOW)
LOW when the nine bits of internal data do not constitute even parity. If held LOW during Write Cycle, odd parity will be generated, forcing a parity error for that address upon output.

FUNCTIONAL DESCRIPTION

The Am93469 Tag Buffer has three modes of operation: Compare, Write, and Reset. These modes are described as follows.

Compare Mode

The eight bits of Data inputs are compared with the content of a given memory location for equality. The nine address inputs define each memory location. In this mode, $\overline{W}$ and $\overline{R}$ inputs are HIGH, and $\overline{S}$ is LOW. If the eight bits of Data inputs are exactly the same as the eight bits of data in the given memory location, the MATCH output will be HIGH. If not, the MATCH output will be LOW. The parity bit is not compared.

Write Mode

The eight bits of data inputs and the one bit of parity are written into the RAM array when both $\overline{S}$ and $\overline{W}$ are LOW, and $\overline{R}$ is HIGH. The MATCH output is forced HIGH (the MATCH output is associated with the output enable of the data cache). Holding the Parity Error ($\overline{PE}$) LOW forces a Parity Error to be output during the later compare cycles.

Reset Mode

When $\overline{R}$ = LOW, $\overline{S}$ = LOW, and $\overline{W}$ = HIGH, a dedicated section of the entire array, D_3, is reset to LOW. The $\overline{PE}$ output is forced LOW during reset. The MATCH output is forced HIGH. All 512 D_3 data bits are reset to a low state. The other seven bits in each address location may change to an undetermined state (HIGH or LOW).

3

TABLE 1. FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	
$\overline{S}$	$\overline{W}$	$\overline{R}$	$\overline{PE}$ (Note 1)	MATCH (Note 2)	DESCRIPTION
H	X	X	Input Output Disabled	H (Forced)	Chip Disabled
L	H	H	Output H = No Parity Error L = Parity Error	H = MATCH L = MISS	Compare
L	H	L	Output L	H (Forced)	Reset
L	L	H	Input H = Even Parity L = Odd Parity	H (Forced)	Write
L	L	L	Input Output Disabled	H (Forced)	Illegal

Notes: 1. $\overline{PE}$ is an open-collector output, requiring an external Pull-up Resistor.
2. MATCH is an open-collector output, requiring an external Pull-up Resistor.

Key: H = HIGH
L = LOW
X = Don't Care

TABLE 2. COMPARE CYCLE OUTPUT DESCRIPTION

MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error or After Reset
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 to V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

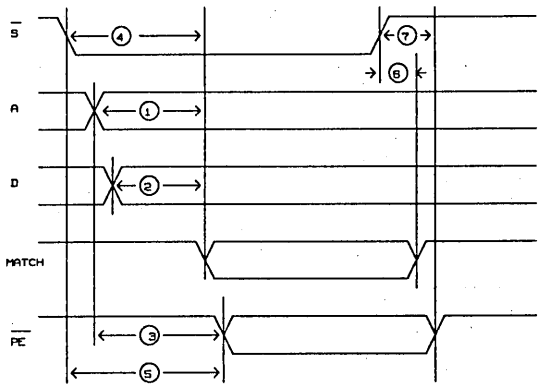
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OL} (MATCH)	Output LOW Voltage	I_{OL} = 36 mA		0.45	V
V_{OL} ($\overline{PE}$)	Output LOW Voltage	I_{OL} = 24 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
V_{CL}	Input Clamp Voltage	I_{IN} = −10 mA		−1.5	V
I_{IL}	Input LOW Current	V_{IN} = 0 to 5.5 V		−220	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V		40	μA
I_{CC}	Supply Current			195	mA

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
Compare Mode					
1	t_{AVMV}	Address to MATCH		20.0	ns
2	t_{DVMV}	Data to MATCH		10.0	ns
3	t_{AVPV}	Address to $\overline{PE}$		25.0	ns
4	t_{SLMV}	$\overline{S}$ to MATCH		10.0	ns
5	t_{SLPV}	$\overline{S}$ to $\overline{PE}$		10.0	ns
6	t_{SHMH}	$\overline{S}$ to MATCH Recovery		10.0	ns
7	t_{SHPH}	$\overline{S}$ to $\overline{PE}$ Recovery		10.0	ns
Write Mode					
8	t_{WLWH}	Write Pulse Width	20.0		ns
9	t_{AVWL}	Address Setup	0.0		ns
10	t_{WHAX}	Address to $\overline{W}$ Hold	0.0		ns
11	t_{DVWH}	Data to $\overline{W}$ Setup	20.0		ns
12	t_{WHDX}	Data to $\overline{W}$ Hold	0.0		ns
13	t_{SLWH}	$\overline{S}$ to Setup	20.0		ns
14	t_{WHSH}	$\overline{S}$ to Select Hold	0.0		ns
15	t_{WLMH}	$\overline{W}$ to MATCH		10.0	ns
16	t_{WHMV}	Write Recovery (MATCH)		20.0	ns
17	t_{WLPH}	$\overline{W}$ to $\overline{PE}$		10.0	ns
18	t_{WHPV}	Write Recovery ($\overline{PE}$)		20.0	ns
19	t_{PVWH}	$\overline{PE}$ Input to $\overline{W}$ Setup		20.0	ns
20	t_{WHPH}	$\overline{PE}$ Input to $\overline{W}$ Hold		0.0	ns
Reset Mode					
21	t_{RLRH}	$\overline{R}$ Pulse Width	40.0		ns
22	t_{SLRL}	$\overline{S}$ to $\overline{R}$ Setup	0.0		ns
23	t_{RHSH}	$\overline{S}$ to $\overline{R}$ Hold	0.0		ns
24	t_{WHRL}	$\overline{W}$ to $\overline{R}$ Setup	0.0		ns
25	t_{RHWL}	$\overline{W}$ to $\overline{R}$ Hold	0.0		ns
26	t_{RLMH}	$\overline{R}$ to MATCH HIGH		10.0	ns
27	t_{RHMX}	$\overline{R}$ to MATCH Recovery		20.0	ns

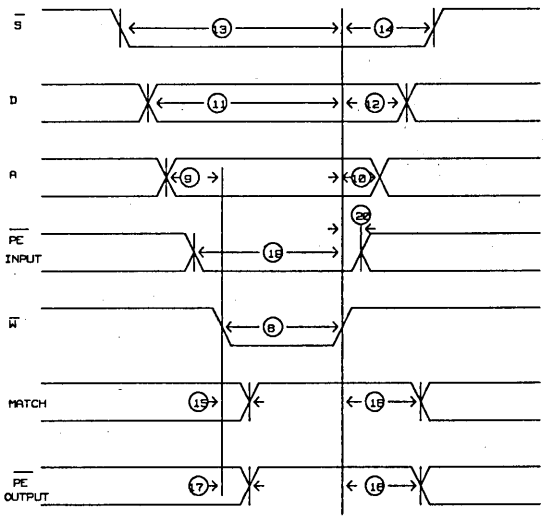
Notes: 1. All Switching Characteristics are measured at 50% of input to valid output. Both input and output timings are referenced to 1.5 V.

SWITCHING WAVEFORMS (Cont'd)



WF021890

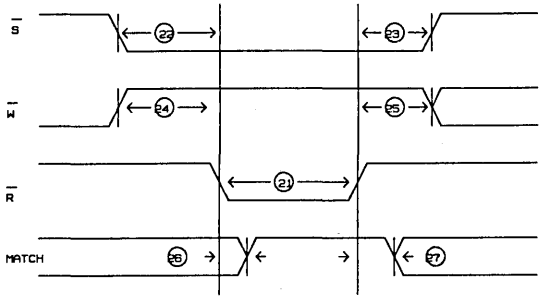
Compare Mode



WF021011

Write Mode

SWITCHING WAVEFORMS



WF021021

Reset Mode

MOS Random-Access Memories (RAM) Index

Am21L41

4096 x 1 Static RAM

DISTINCTIVE CHARACTERISTICS

- Fully static storage and interface circuitry
- Automatic power-down when deselected
- Low power dissipation
  - Am21L41; 220 mW active, 27.5 mW power down
- High output drive
- TTL compatible interface levels
- No power-on current surge

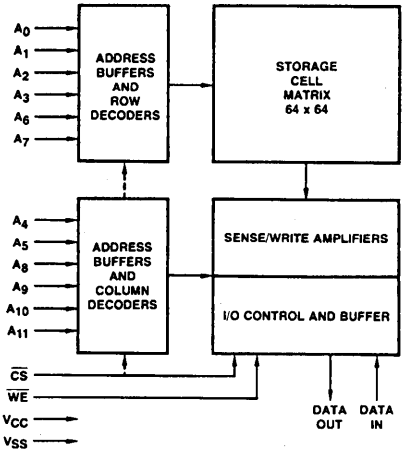
GENERAL DESCRIPTION

The Am21L41 is a high-performance, 4096-bit, static, read/write, random-access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single +5-volt power supply is required. When deselected ($\overline{CS} \geq V_{IH}$), the Am21L41 automatically enters a power-down mode which reduces power dissipation by as much as 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-OR operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



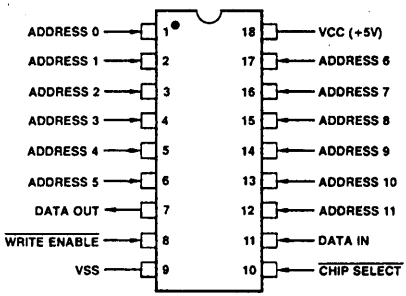
BD000111

PRODUCT SELECTOR GUIDE

Part Number	Am21L41-12	Am21L41-15	Am21L41-20	Am21L41-25
Maximum Access Time (ns)	120	150	200	250
Maximum Active Current (mA)	55	40	40	40
Maximum Standby Current (mA)	10	5	5	5

Publication # 03078 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

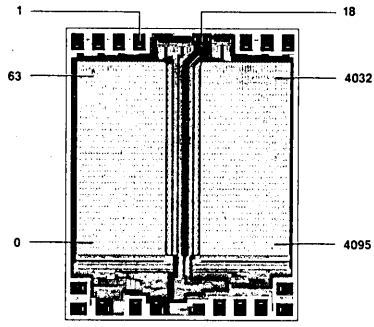


CD000161

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	**Internal**
A_0	A_2
A_1	A_5
A_2	A_4
A_3	A_3
A_4	A_8
A_5	A_7
A_6	A_1
A_7	A_0
A_8	A_{11}
A_9	A_9
A_{10}	A_{10}
A_{11}	A_6

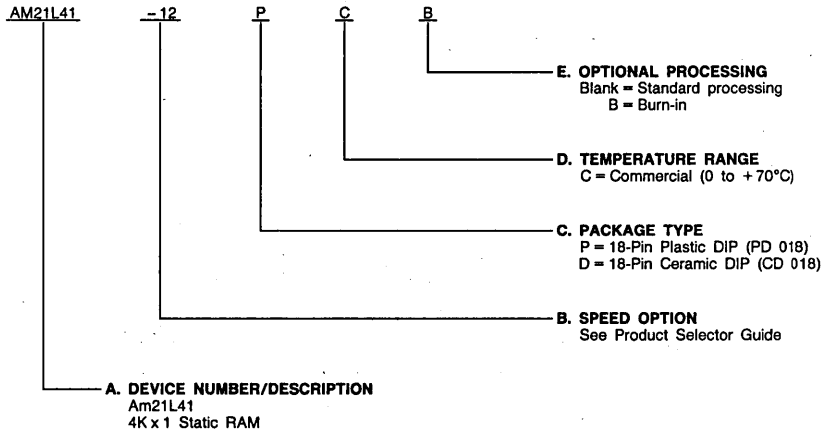


Die Size: 0.130" x 0.106"

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM21L41-12	PC, PCB, DC, DCB
AM21L41-15	
AM21L41-20	
AM21L41-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

PIN DESCRIPTION

$A_0 - A_{11}$ Address (Inputs)
The address input lines select memory location from which to read or write.

$\overline{CS}$ Chip Select (Input, Active LOW)
The Chip Select line selects the memory device for active operation.

$\overline{WE}$ Write Enable (Input, Active LOW)
When both $\overline{CS}$ and $\overline{WE}$ are LOW, data on the input lines is written to the location presented on the address input lines.

D_{IN} Data In (Input)
This pin is used to enter data during write operations.

D_{OUT} Data Out (Output, Three-State)
The content of the selected memory location is presented on the Data Output line during read operations ($\overline{CS}$ LOW, $\overline{WE}$ HIGH). The line goes three-state during write operations.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... 0 to +70°C
Supply Voltage ..... −0.5 V to +7.0 V
All Signal Voltage with
Respect to Ground ..... −1.5 V to +7.0 V
Power Dissipation ..... 1.2 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commcercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

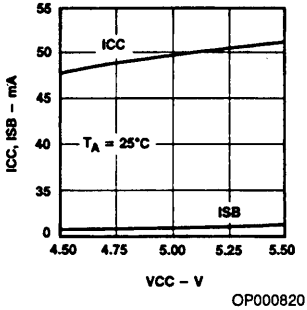
DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Am21L41-12		Am21L41-15, Am21L41-20, Am21L41-25		Units
				Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	T_A = 70°C	8		8		mA
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	Volts
V_{IL}	Input LOW Voltage			−2.5	0.8	−2.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10	µA
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Output Disabled	T_A = 70°C	−10	10	−10	10	µA
I_{OS}	Output Short-Circuit Current	$V_{SS} \leq V_O \leq V_{CC}$ (Note 3)	0 to +70°C	−120	120	−120	120	mA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$	T_A = 0°C		55		40	mA
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, ($\overline{CS} \geq V_{IH}$) (Note 5)			10		5.0	mA
C_I	Input Capacitance (Note 13)	Test Frequency = 1.0 MHz T_A = 25°C, All pins at 0 V			5.0		5.0	pF
C_O	Output Capacitance (Note 13)				6.0		6.0	

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.
4. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.5 V and output loading of the specified I_{OL}/I_{OH} and C_L = 30 pF load capacitance (reference A. under Switching Test Circuit.).
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up, otherwise I_{SB} will exceed values given.
7. Chip deselected greater than 55 ns prior to selection.
8. Chip deselected less than 55 ns prior to selection.
9. Transtion is measured at V_{OH} −500 mV and V_{OL} +500 mV levels on the output from 1.5 V level on the input with load shown in Figure 1 using C_L = 5 pF.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. These parameters are not 100% tested, but are evaluated at initial characterization and at anytime the design is modified where capacitance may be affected.

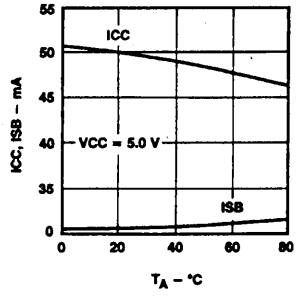
TYPICAL DC and AC CHARACTERISTICS

Supply Current Versus Supply Voltage



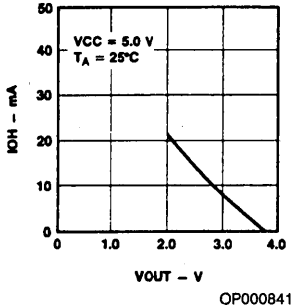
OP000820

Supply Current Versus Ambient Temperature



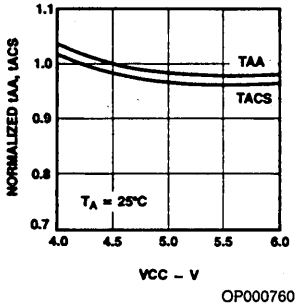
OP000831

Output Source Current Versus Output Voltage



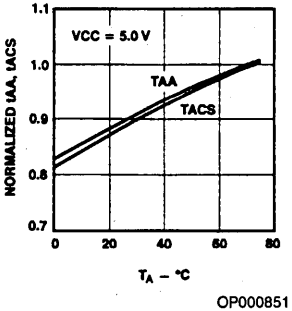
OP000841

Normalized Access Time Versus Supply Voltage



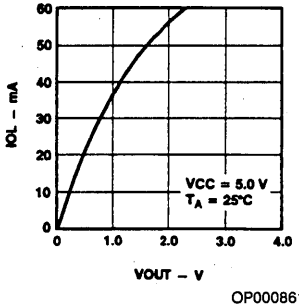
OP000760

Normalized Access Time Versus Ambient Temperature



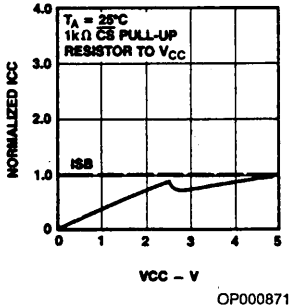
OP000851

Output Sink Current Versus Output Voltage



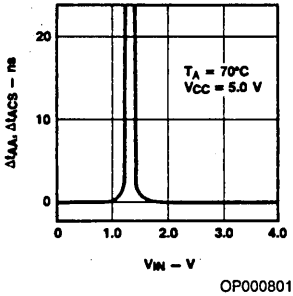
OP000861

Typical Power-On Current Versus Power Supply



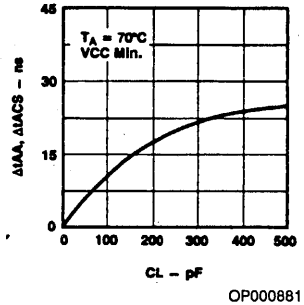
OP000871

Access Time Change Versus Input Voltage



OP000801

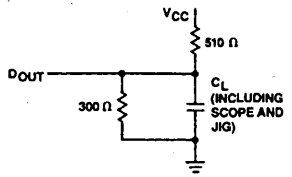
Access Time Change Versus Output Loading



OP000881

4

SWITCHING TEST CIRCUIT



TC000031

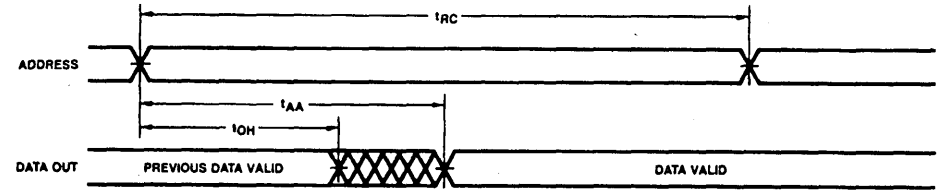
A. Output Load

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Notes 4-12)

No.	Parameter Symbol	Parameter Description		Am21L41-12 Min.	Am21L41-12 Max.	Am21L41-15 Min.	Am21L41-15 Max.	Am21L41-20 Min.	Am21L41-20 Max.	Am21L41-25 Min.	Am21L41-25 Max.	Units
Read Cycle												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		120		150		200		250		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			120		150		200		250	ns
3	t_{ASC1}	Chip Select LOW to Data Out Valid	(Note 7)		120		150		200		250	ns
4	t_{ASC2}		(Note 8)		130		160		200		250	ns
5	t_{LZ}	Chip Select LOW to Data Out On (Note 9, 13)		10		10		10		10		ns
6	t_{HZ}	Chip Select HIGH to Data Out Off (Note 9, 13)		0	60	0	60	0	60	0	60	ns
7	t_{OH}	Address Unknown to Data Out Unknown Time		10		10		10		10		ns
8	t_{PD}	Chip Select HIGH to Power LOW Delay (Note 13)			60		60		60		60	ns
9	t_{PU}	Chip Select LOW to Power HIGH Delay (Note 13)		0		0		0		0		ns
Write Cycle												
10	t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)		120		150		200		250		ns
11	t_{WP}	Write Enable LOW to Write Enable HIGH Time (Note 5)		60		60		60		75		ns
12	t_{WR}	Write Enable HIGH to Address Do Not Care Time		10		15		20		20		ns
13	t_{WZ}	Write Enable LOW to Data Out Off Delay (Notes 9, 13)		0	70	0	80	0	80	0	80	ns
14	t_{DW}	Data in Valid to Write Enable HIGH Time		50		60		60		75		ns
15	t_{DH}	Write Enable HIGH to Data In Do Not Care Time		10		10		10		10		ns
16	t_{AS}	Address Valid to Write Enable LOW Time		0		0		0		0		ns
17	t_{CW}	Chip Select LOW to Write Enable HIGH Time (Note 5)		110		135		180		230		ns
18	t_{OW}	Write Enable HIGH to Output Turn On (Notes 9, 13)		0		0		0		0		ns
19	t_{AW}	Address Valid to End of Write		110		135		180		230		ns

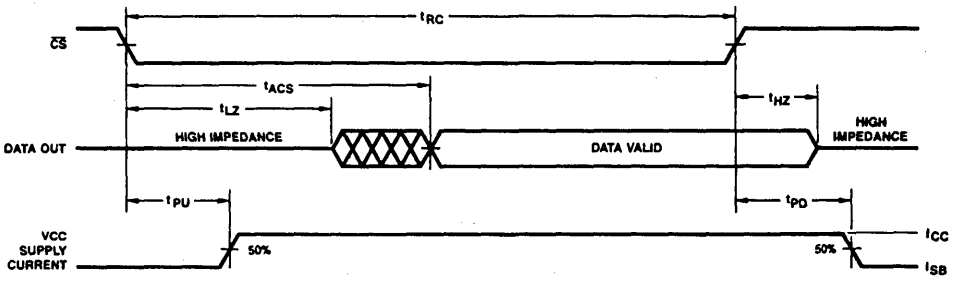
Notes: See notes following DC Characteristics table.

SWITCHING WAVEFORMS (Cont'd.)



WF000231

Read Cycle No. 1 (Notes 10 & 11)

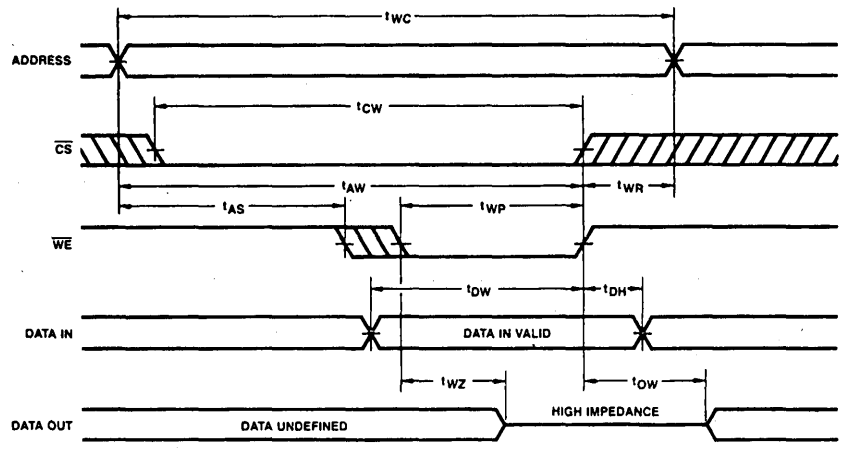


WF000241

Read Cycle No. 2 (Notes 10 & 12)

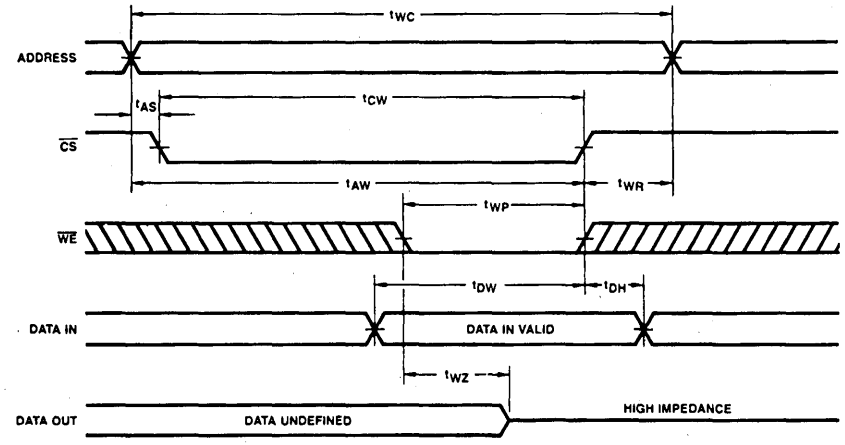
4

SWITCHING WAVEFORMS



WF000211

Write Cycle No. 1 ($\overline{WE}$ Controlled)



WF000221

Write Cycle No. 2 ($\overline{CS}$ Controlled)

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Am2130

1024 x 8 Dual-Port Static Random-Access Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast 70-ns access time
- Fully static operation
- Full TTL compatibility
- Interrupt function ($\overline{INT}$)
  Open drain for OR-tied operation
- Easy microprocessor interface
- $\overline{BUSY}$ function to handle contention
  – Open drain for OR-tied operation
- Automatic power down ($\overline{CE}$)
- Output Enable function ($\overline{OE}$)
- Both ports operate independently
- Each port accesses entire memory

GENERAL DESCRIPTION

The Am2130 is an 8192-Bit Dual-Port Static Random-Access Memory organized 1024 words by 8 bits. It is designed using fully static circuitry requiring no clocks or refresh to operate.

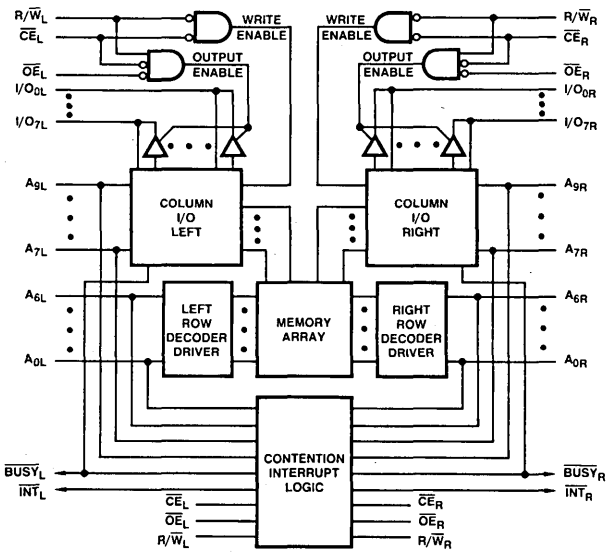
The Am2130 features two separate I/O ports which allow independent access for read or write to any location in the memory. The only situation where contention can occur is when both ports are active and both addresses match. In the event that contention occurs, on-chip control logic arbitrates delaying one port until the other port's operation is completed. A $\overline{BUSY}$ flag is sent to the side whose operation is delayed. $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data.

An interrupt function ($\overline{INT}$) is also provided to allow communication between systems. This function acts like a writable flag. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. The $\overline{INT}$s and $\overline{BUSY}$s have open-drain drivers to allow OR-tied operation.

The Am2130 has an automatic power-down feature which is controlled by the Chip Enable inputs. Each Chip Enable controls automatic power-down circuitry that allows its respective side of the device to remain in a standby power mode.

The Am2130 is packaged in 48-pin DIPs (Plastic or Ceramic Sidebrazed) and 52-pin Chip Carriers (Plastic Leaded or Ceramic Leadless) for highest possible density. The device is fully TTL-compatible and requires a single +5 V power supply.

BLOCK DIAGRAM

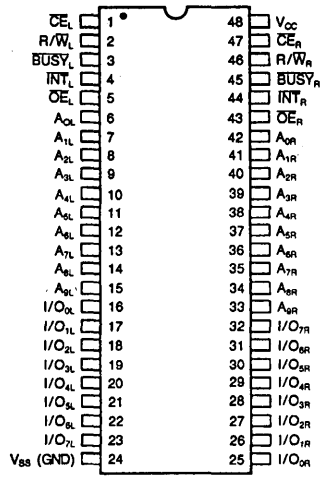


BD005083

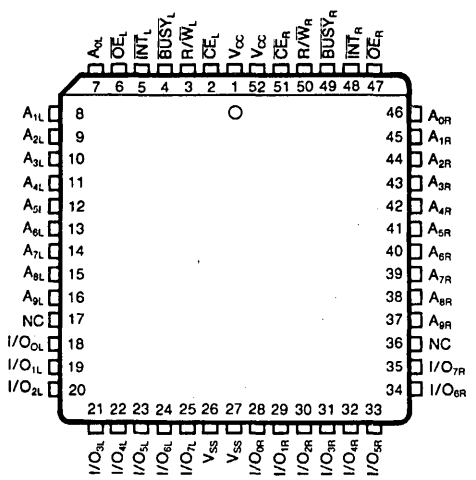
Publication # 05157 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

LCC/PLCC*



CD005812

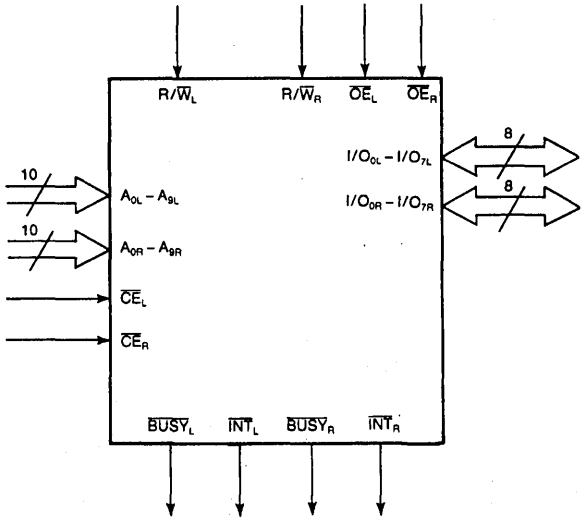


CD009600

* Same Pinouts apply for LCC.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



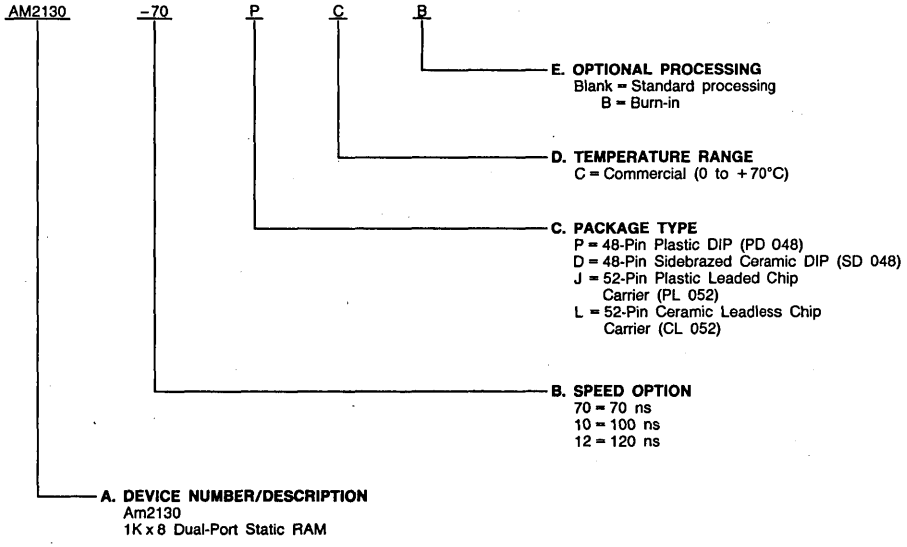
LS002231

V_{CC} = +5-V Power Supply
V_{SS} = Ground

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2130-70	PC, PCB, DC, DCB, JC, LC, LCB
AM2130-10	
AM2130-12	

Valid Combinations

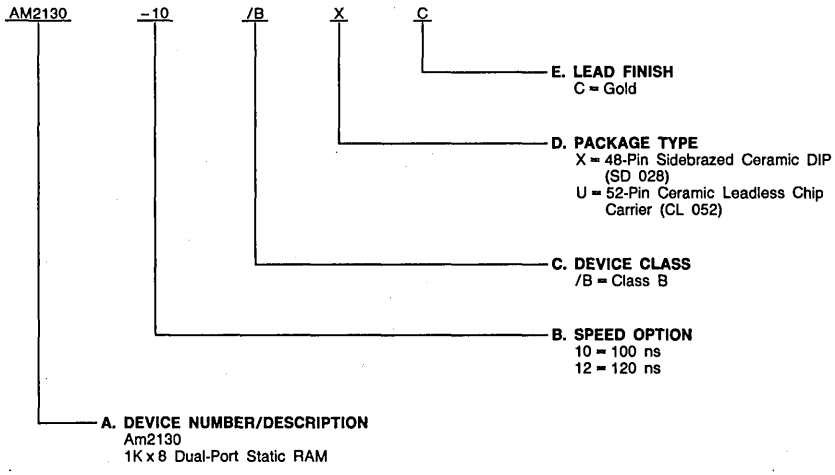
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2130-10	/BXC, /BUC
AM2130-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$\overline{CE}_L$ Left Port $\overline{\text{Chip Enable}}$ (Input)
When $\overline{CE}_L$ goes HIGH, the left port of the RAM is deselected and the left-port control circuitry will automatically power down — excluding $\overline{INT}_L$ — and remain in a standby power mode as long as $\overline{CE}_L$ remains HIGH.

$\overline{CE}_R$ Right Port $\overline{\text{Chip Enable}}$ (Input)
When $\overline{CE}_R$ goes HIGH, the right port of the RAM is deselected and the right-port control circuitry will automatically power down — excluding $\overline{INT}_R$ — and remain in a standby power mode as long as $\overline{CE}_R$ remains HIGH.

$A0_L - A9_L$ Left Port Address (Inputs)
The 10-bit field presented at the Left Port Address Inputs selects one of the 1024 memory locations to be read from — or written into — via the Left Port Data Input/Output Lines.

$A0_R - A9_R$ Right Port Address (Inputs)
The 10-bit field presented at the Right Port Address Inputs selects one of the 1024 memory locations to be read from — or written into — via the Right Port Data Input/Output Lines.

$\overline{OE}_L$ $\overline{\text{Output Enable}}$ for Left Port (Input)
When $\overline{OE}_L$ is HIGH, the left port outputs are disabled — excluding $\overline{BUSY}_L$ and $\overline{INT}_L$. When LOW, the left port outputs are enabled.

$\overline{OE}_R$ $\overline{\text{Output Enable}}$ for Right Port (Input)
When $\overline{OE}_R$ is HIGH, the right port outputs are disabled — excluding $\overline{BUSY}_R$ and $\overline{INT}_R$. When LOW, the right port outputs are enabled.

$I/O_{0L} - I/O_{7L}$ Left Port Data Input/Output Lines (Input/Output)

$I/O_{0R} - I/O_{7R}$ Right Port Data Input/Output Lines (Input/Output)

$R/\overline{W}_L$ Left Port Read/$\overline{\text{Write}}$ Enable (Input)
When $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, data from the RAM location selected by the left address field is present at the Left Port Data I/O Lines. When $R/\overline{W}_L$ is LOW, data present on the Left Port Data I/O Lines is written into the RAM location selected by the left address field regardless of the state of $\overline{OE}_L$. These operations can be affected by contention (see Functional Description).

$R/\overline{W}_R$ Right Port Read/$\overline{\text{Write}}$ Enable (Input)
When $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ HIGH, data from the RAM location selected by the right address field is present at the Right Port Data I/O Lines. When $R/\overline{W}_R$ is LOW, data present on the Right Port Data I/O Lines is written into the RAM location selected by the right address field regardless of the state of $\overline{OE}_R$. These operations can be affected by contention (see Functional Description).

$\overline{BUSY}_L$ Left Port $\overline{\text{Busy}}$ Flag (Output)
$\overline{BUSY}_L$ remains HIGH at all times unless both ports initiate an operation to the same address location and the right port is given priority. When this occurs, $\overline{BUSY}_L$ will go LOW and remain LOW until the right port operation is completed.

$\overline{BUSY}_R$ Right Port $\overline{\text{Busy}}$ Flag (Output)
$\overline{BUSY}_R$ remains HIGH at all times unless both ports initiate an operation to the same address location and the left port is given priority. When this occurs $\overline{BUSY}_R$ will go LOW and remain LOW until the left port operation is completed.

Both $\overline{BUSY}_R$ and $\overline{BUSY}_L$ are open drain, allowing OR-tied operation.

$\overline{INT}_L$ Left Port $\overline{\text{Interrupt}}$ Flag (Output)
If the right port writes to memory location 3FE, then $\overline{INT}_L$ is latched LOW until the left port reads data from memory location 3FE. These operations can be affected by contention (see Functional Description).

$\overline{INT}_R$ Right Port $\overline{\text{Interrupt}}$ Flag (Output)
If the left port writes to memory location 3FF, then $\overline{INT}_R$ is latched LOW until the right port reads data from memory location 3FF. These operations can be affected by contention (see Functional Description).

Both $\overline{INT}_R$ and $\overline{INT}_L$ are open drain, allowing OR-tied operation.

FUNCTIONAL DESCRIPTION

The Am2130 is a 1024-word by 8-bit dual-port RAM that features two separate I/O ports. Each port allows independent access for read or write to any location in the memory.

The Am2130 features separate Left and Right Port Chip Enable controls ($\overline{CE}_L$ and $\overline{CE}_R$). Each Chip Enable activates its respective port when it goes LOW. When a port is active, it is allowed access to the entire memory array. When each Chip Enable goes HIGH, the automatic power-down circuitry returns its respective port to standby power mode.

Each port has an Output Enable control ($\overline{OE}_L$ and $\overline{OE}_R$) that keeps its respective outputs — excluding $\overline{BUSY}$ and $\overline{INT}$ — in a high-impedance mode when HIGH. When $\overline{OE}$ is LOW, that port's output drivers are turned on providing its R/$\overline{W}$ control is HIGH.

Separate Read/Write Enable inputs (R/$\overline{W}_L$ and R/$\overline{W}_R$) control writing of new data into any location in the RAM from either port. When R/$\overline{W}_L$ is LOW, new data is written into the location selected by the left address field. Likewise, when R/$\overline{W}_R$ is LOW, new data is written into the location selected by the right address field. When R/$\overline{W}$ is HIGH, data can be read from that port if its respective $\overline{OE}$ is LOW. When R/$\overline{W}_L$ is HIGH and $\overline{OE}_L$ LOW, data is read from the location selected by the left address field. When R/$\overline{W}_R$ is HIGH and $\overline{OE}_R$ LOW, data is read from the location selected by the right address field.

There is one situation where contention can occur. It is when both left and right ports are active and both addresses match. For this condition, on-chip control logic arbitrates the situation. Priority is given to the first port whose inputs are valid at the address match.

There are two possible ways a port becomes valid at an address match. One is where Address inputs are valid before the respective Chip Enable goes LOW. The other is where Chip Enable is LOW and an address change follows. Priority, then, is given to the first port that has both its Chip Enable LOW, and Address inputs valid, at the address match. The other port will not be allowed access to the memory core in contention until the first port's operation is complete.

Separate Busy Flags ($\overline{BUSY}_L$ and $\overline{BUSY}_R$) are provided to signal when a port's access to the memory core has been delayed. When both ports try to access the same memory location, the on-chip arbitration logic causes the Busy Flag to go LOW on the side that is delayed. The Busy Flag goes HIGH when either port is deselected, or either ports' addresses change to a non-matching location. These flags are provided to allow the user to stop the processor if desired. $\overline{BUSY}$ is driven out fast enough for the processor's address and data to be preserved if needed.

Interrupt logic is included on-chip to provide a means for two processors to communicate to one another. If the left port writes to memory location 3FF, the Right Port Interrupt Flag ($\overline{INT}_R$) is latched LOW until the right port reads data from that same location. If the right port writes to location 3FE, then the Left Port Interrupt Flag ($\overline{INT}_L$) is latched LOW until the left port reads data from that location. If both ports are enabled and contention occurs, only the port with priority may set or clear the Interrupt Flags. The other port may not set or clear the Interrupt Flags until the first port is either deselected or its addresses change to a different location.

TABLE 1. NON-CONTENTION READ/WRITE CONTROL

Left Port Inputs				Right Port Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	H	X	X	X	X	X	X	H	X	H	X	Left port in power-down mode
X	X	X	X	X	H	X	X	H	X	H	X	Right port in power-down mode
L	L	X	X	X	X	X	X	H	X	H	X	Data on left port written to memory location $A_{0L}-A_{9L}$
H	L	L	X	X	X	X	X	H	X	H	X	Data in memory location $A_{0L}-A_{9L}$ output on left port
X	X	X	X	L	L	X	X	H	X	H	X	Data on right port written to memory location $A_{0R}-A_{9R}$
X	X	X	X	H	L	L	X	H	X	H	X	Data in memory location $A_{0R}-A_{9R}$ output on right port
L	L	X	3FF	X	X	X	X	H	X	H	L	Left port flags right port to read memory location 3FF
X	X	X	X	L	L	X	3FE	H	L	H	X	Right port flags left port to read memory location 3FE

TABLE 2. BUSY ARBITRATION OF ADDRESS CONTENTION

Left Port				Right Port				Flags (Note 1)		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
X	L (LIV)	X	Match	X	L	X	Match	L	H	Right-Port operation only is permitted. (Note 3)
X	L	X	Match (LIV)	X	L	X	Match	L	H	
X	L	X	Match	X	L (LIV)	X	Match	H	L	Left-port operation only is permitted. (Note 4)
X	L	X	Match	X	L	X	Match (LIV)	H	L	

TABLE 3. INTERRUPT FLAG

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{INT}_R$	Function
L	L	X	3FF	L	X	X	X	X_1	L	Set $\overline{INT}_R$
X	X	X	X_1	H	H	L	L	3FF	H	Reset $\overline{INT}_R$
X	X	X	X_1	X	L	L	X	3FE	X	Set $\overline{INT}_L$
H	L	L	3FE	X	X	X	X	X_1	X	Reset $\overline{INT}_L$

Key: H = HIGH
L = LOW
LIV = Last Input Valid; meets t_{APS} spec (Note 2)
X = Don't Care
X_1 = No Match, or
Same port deselected, or
Opposite port has priority

Notes: 1. INT Flags = X
2. If LIV violates t_{APS} spec then one of the two ports receives priority, and the remaining port's $\overline{BUSY}$ Flag goes LOW. However, there is an extremely rare metastable event which can occur when the arbitration circuitry cannot determine which port was "first" at the matching address. On this rare occurrence, both ports may momentarily receive $\overline{BUSY}$ = LOW signals until the metastable state is resolved (usually within a few nanoseconds). Thereafter, one port's $\overline{BUSY}$ remains LOW while the other completes its operation and resumes normal operation.
3. A Left-Port Read operation is also permitted if the Right-Port is also reading.
4. A Right-Port Read operation is also permitted if the Left-Port is also reading.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −55 to +125°C
Supply Voltage
with Respect to Ground ..... −0.5 to +7.0 V
All Signal Voltages ..... −3.5 to +7.0 V
Power Dissipation ..... 1.2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 8)
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Military (M) Devices (Note 8)*
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Am2130 Min.	Am2130 Max.	Units
I_{LI}	Input Load Current (All Input Pins)	V_{CC} = Max., V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{CC} = Max., V_{OUT} = GND to 4.5 V			10	µA
I_{CC}	Power Supply Current (Both Ports Active)	V_{CC} = Max., $\overline{CE}$ = V_{IL} Outputs Open	C Devices		170	mA
			M Devices		185	
I_{SB1}	Standby Current (Both Ports Standby)	V_{CC} = Min. to Max., $\overline{CE_L}$ and $\overline{CE_R}$ = V_{IH}	C Devices		30	mA
			M Devices		40	
I_{SB2}	Standby Current (One Port Standby)	V_{CC} = Max., $\overline{CE_L}$ = V_{IL} and $\overline{CE_R}$ = V_{IH} or $\overline{CE_L}$ = V_{IH} and $\overline{CE_R}$ = V_{IL}	C Devices		110	mA
			M Devices		125	
V_{IL1}	Input LOW Voltage (I/O_n)			−0.5	0.8	V
V_{IL2}	Input LOW Voltage (All Addresses & Clocks)			−2.0	0.8	V
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{OL1}	Output LOW Voltage (I/O_0 − I/O_7)	I_{OL} = 3.2 mA (Note 7)			0.4	V
V_{OL2}	Open-Drain Output LOW Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 4 mA			0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA (Note 7)		2.4		V

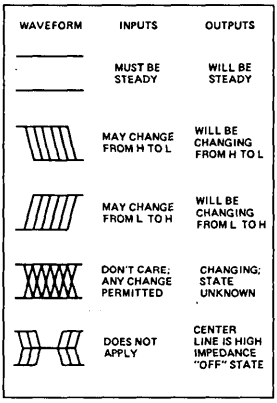
*See the last page of this spec for Group A Subgroup Testing information.

CAPACITANCE (Note 9)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_{OUT}	Output Capacitance			10	pF
C_{IN}	Input Capacitance			10	

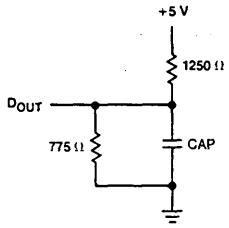
Notes: See notes following Switching Waveforms.

KEY TO SWITCHING WAVEFORMS



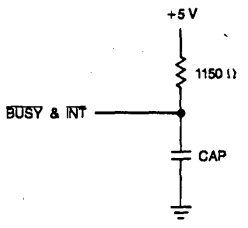
KS000010

SWITCHING TEST CIRCUITS



TC002201

Test Loads A and B



TC002222

Test Loads C and D

TEST OUTPUT LOADS	
Test Load	**CAP**
A	5 pF (Note 1)
B	100 pF
C	50 pF
D	5 pF (Note 1)

Notes: 1. Includes Scope and Jig Capacitance.

SWITCHING TEST WAVEFORM

AC Test Conditions	
Input Levels	GND to 3.0 V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Test Output Load	See Test Output Loads Table

4

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

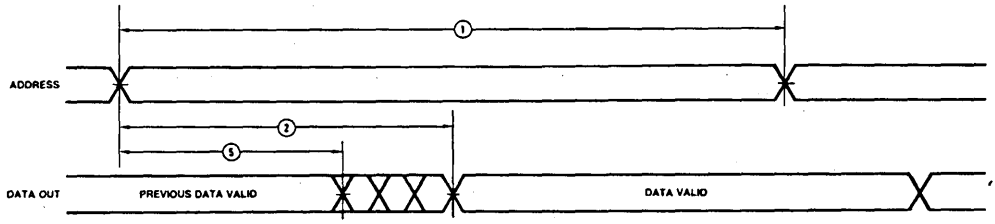
No.	Parameter Symbol	Parameter Description	Test Conditions	Am2130-70		Am2130-10		Am2130-12		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE (Note 10)										
1	t_{RC}	Read Cycle Time		70		100		120		ns
2	t_{AA}	Address Access Time			70		100		120	ns
3	t_{ACE}	Chip Enable Access Time			70		100		120	ns
4	t_{AOE}	Output Enable Access Time			35		40		60	ns
5	t_{OH}	Output Hold from Address Change		5		5		5		ns
6	t_{LZ}	Output Low Z Time	(Notes 5 & 9)	5		5		5		ns
7	t_{HZ}	Output High Z Time	(Notes 5 & 9)	0	30	0	40	0	40	ns
8	t_{PU}	Chip Enable to Power Up Time		0		0		0		ns
9	t_{PD}	Chip Disable to Power Down Time			35		50		60	ns
WRITE CYCLE (Note 10)										
10	t_{WC}	Write Cycle Time		70		100		120		ns
11	t_{EW}	Chip Enable to End of Write		65		90		100		ns
12	t_{AW}	Address Valid to End of Write		65		90		100		ns
13	t_{AS}	Address Setup Time		0		0		0		ns
14	t_{WP}	Write Pulse Width		50		60		70		ns
15	t_{WR}	Write Recovery Time		0		0		0		ns
16	t_{DW}	Data Valid to End of Write		35		40		40		ns
17	t_{DH}	Data Hold Time		0		0		0		ns
18	t_{WZ}	Write Enabled to Output in High Z	(Note 9)	0	30	0	40	0	50	ns
19	t_{OW}	Output Active from End of Write	(Note 9)	0		0		0		ns
$\overline{\text{BUSY}}$ FLAG TIMING (Note 7)										
20	t_{RC}	Read Cycle Time		70		100		120		ns
21	t_{WC}	Write Cycle Time		70		100		120		ns
22	t_{BAA}	$\overline{\text{BUSY}}$ Access Time to Address			45		50		60	ns
23	t_{BDA}	$\overline{\text{BUSY}}$ Disable Time to Address	(Note 9)		45		50		60	ns
24	t_{BAC}	$\overline{\text{BUSY}}$ Access Time to Chip Enable or Chip Select			45		50		60	ns
25	t_{BDC}	$\overline{\text{BUSY}}$ Disable Time to Chip Enable or Chip Select	(Note 9)		45		50		60	ns
26	t_{APS}	Arbitration Priority Setup Time		10		10		10		ns
INTERRUPT TIMING (Note 7)										
27	t_{WINS}	$\overline{\text{WE}}$ to Interrupt Set Time			30		35		45	ns
28	t_{EINS}	$\overline{\text{CE}}$ to Interrupt Set Time			55		60		70	ns
29	t_{INS}	Address to Interrupt Set Time			55		60		70	ns
30	t_{OINR}	Output Enable to Interrupt Reset Time	(Note 9)		30		35		45	ns
31	t_{INR}	Address to Interrupt Reset Time	(Note 9)		55		60		70	ns
32	t_{EINR}	Chip Enable to Interrupt Reset Time	(Note 9)		55		60		70	ns

Notes: See notes following Switching Waveforms.

*See the last page of this spec for Group A Subgroup Testing information.

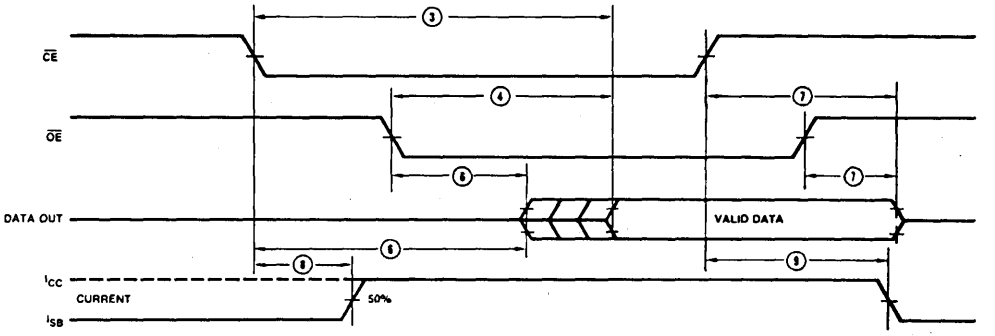
SWITCHING WAVEFORMS

READ CYCLE
(Either Side)



WF009391

Address Access
(Notes 1 & 2)

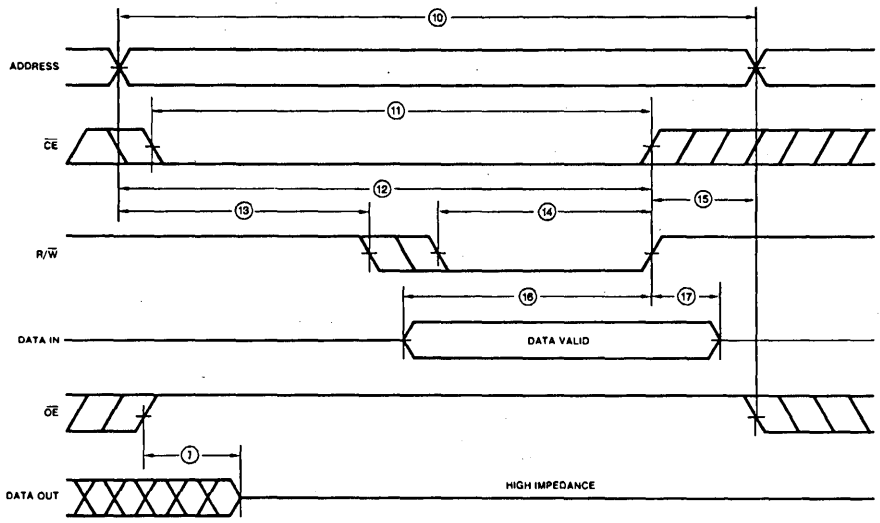


WF009401

$\overline{CE}$ and $\overline{OE}$-Controlled Access
(Notes 1 & 3)

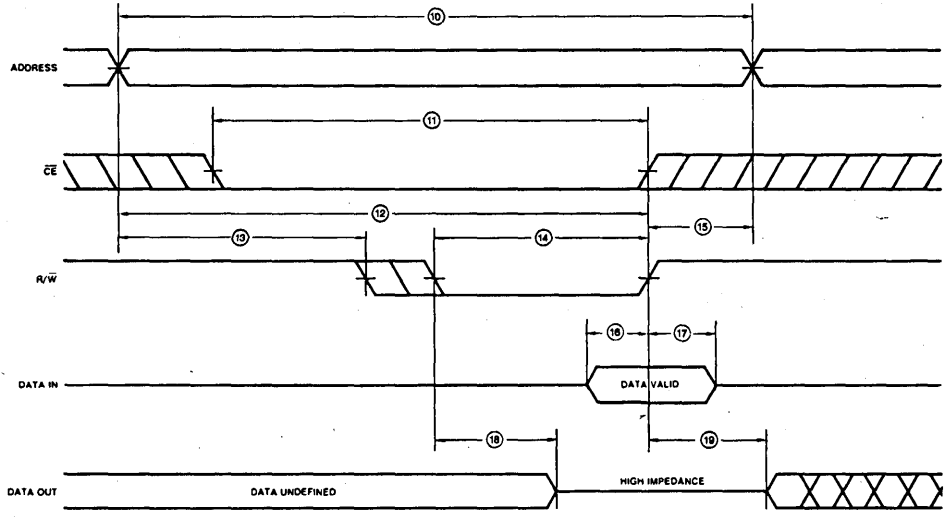
SWITCHING WAVEFORMS (Cont.)

WRITE CYCLE
(Either Side — Note 4)



WF009411

OE-Controlled Data Out

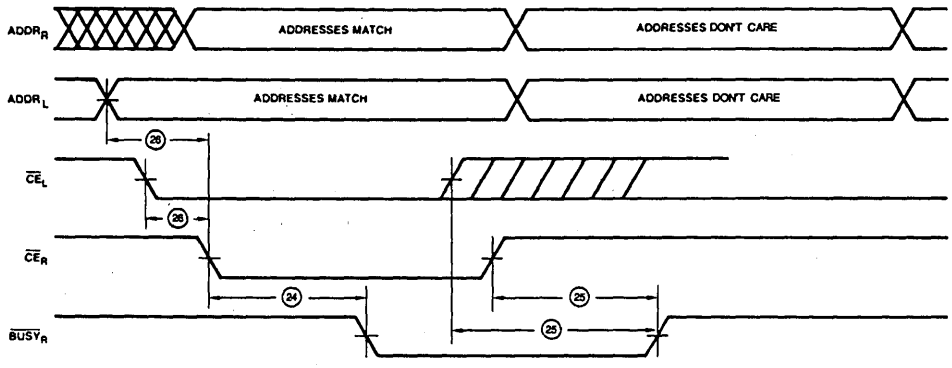


WF009421

WE-Controlled Data Out
($\overline{OE}$ = V_{IL})

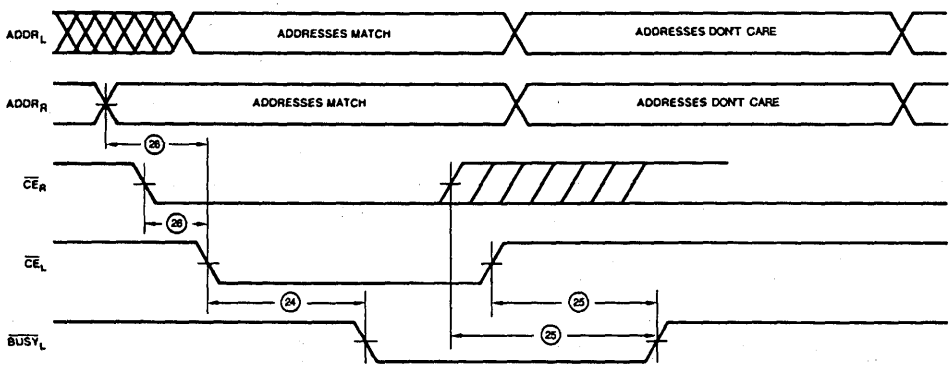
SWITCHING WAVEFORMS (Cont.)

$\overline{BUSY}$ FLAG TIMING (1 of 2) (Note 12)
(Chip Enable Arbitration)



WF009431

$\overline{CE}_R$ Valid Last



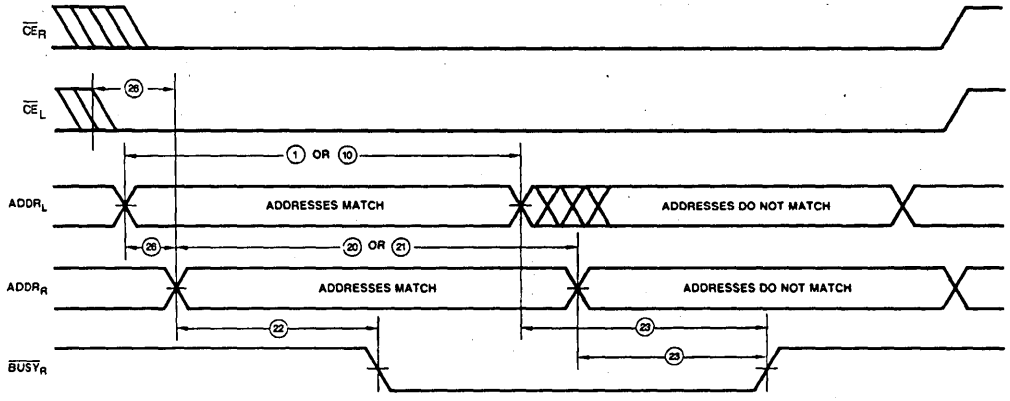
WF009432

$\overline{CE}_L$ Valid Last

4

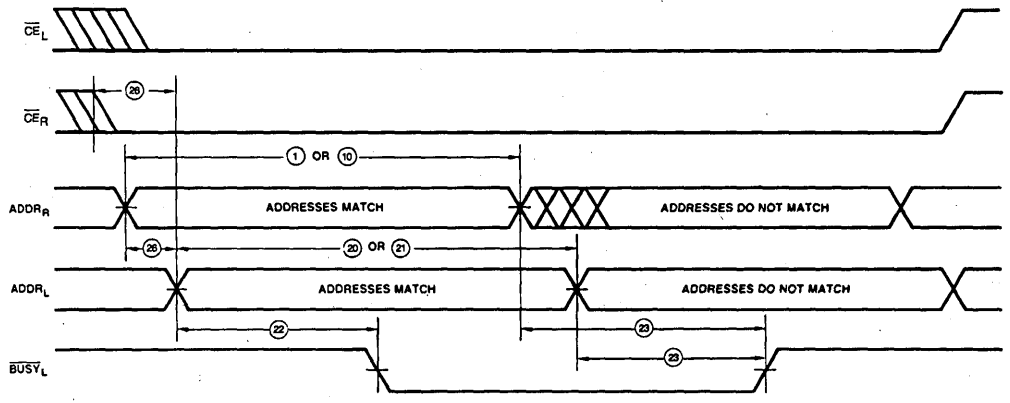
SWITCHING WAVEFORMS (Cont.)

$\overline{BUSY}$ FLAG TIMING (2 of 2)
(Address Arbitration)



WF009441

$ADDR_R$ Valid Last

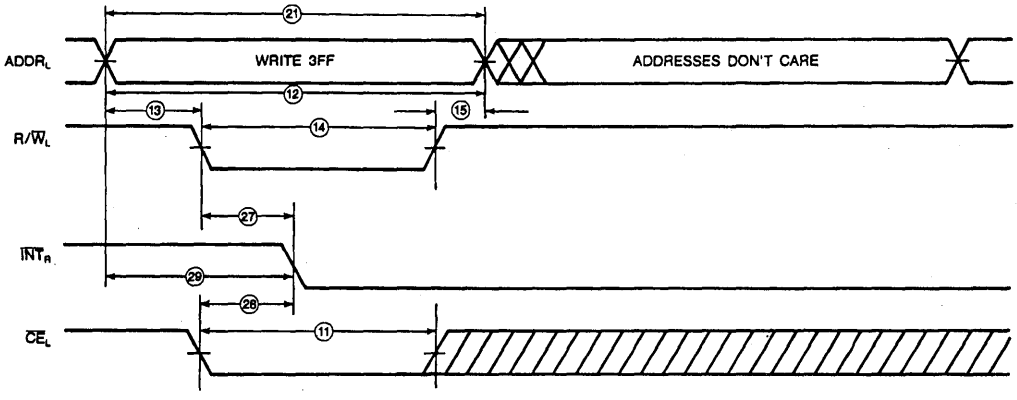


WF009442

$ADDR_L$ Valid Last

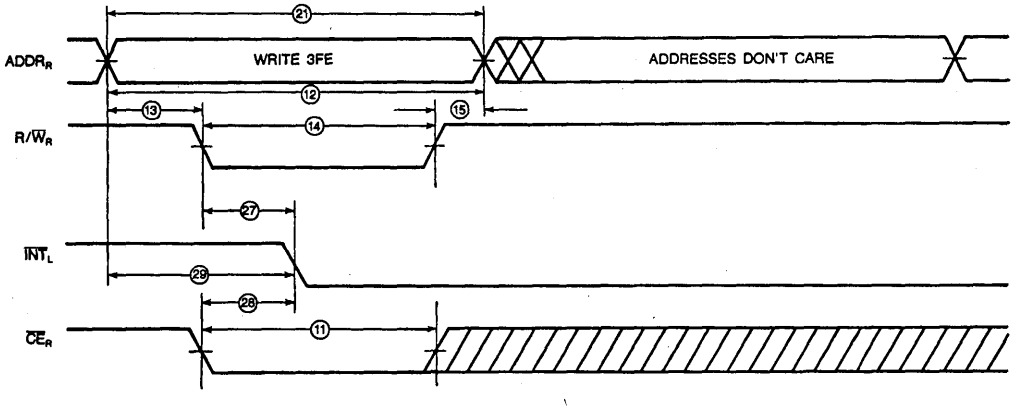
SWITCHING WAVEFORMS (Cont.)

INTERRUPT TIMING (1 of 2)
(Set $\overline{INT}$ Flag — Note 11)



WF009481

Left Side Flags Right Side



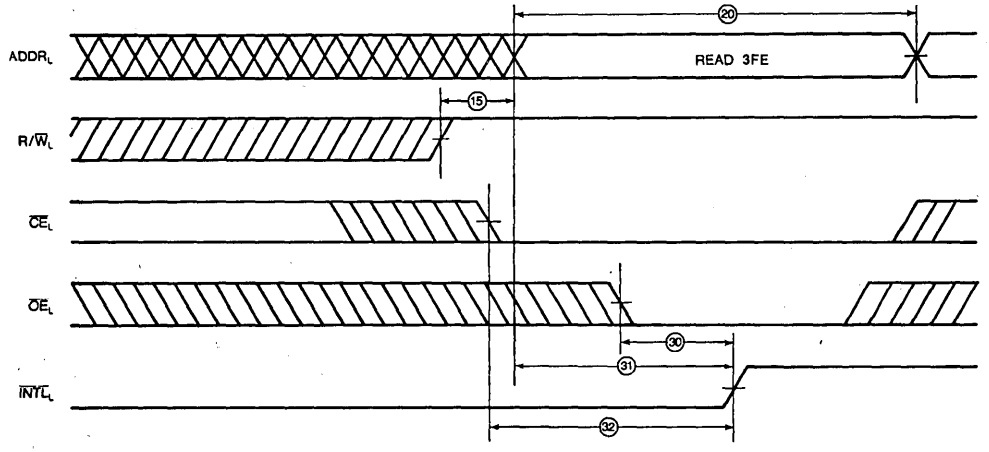
WF009482

Right Side Flags Left Side

4

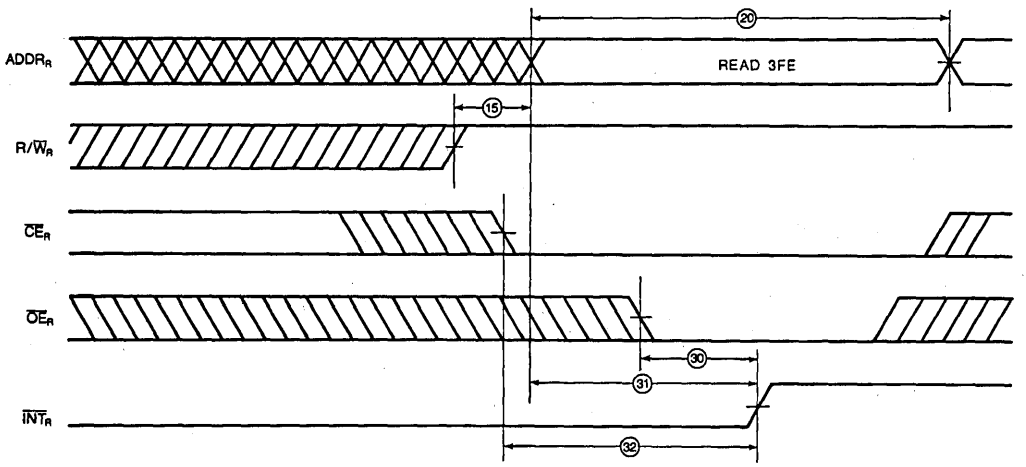
SWITCHING WAVEFORMS

INTERRUPT TIMING (2 of 2)
(Clear $\overline{INT}$ Flag)



WF009485

Left Side Clears $\overline{INT}_L$



WF009484

Right Side Clears $\overline{INT}_R$

Notes*

1. R/$\overline{W}$ is HIGH for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.
4. If $\overline{CE}$ and R/$\overline{W}$ go HIGH simultaneously, the outputs remain in the high-impedance state.
5. Output transition is measured at ±500 mV from the low- or high- impedance voltage levels using Load A.
6. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
7. The $\overline{BUSY}$ and $\overline{INT}$ outputs are open drain. A pull-up resistor is required for system operation. For measurement purposes, Load C is used for HIGH-to-LOW transitions; output reference level is 1.5 V. Load D is used for LOW-to-HIGH transitions; output reference level is +500 mV from the output LOW voltage level.
8. For test and correlation purposes, temperature is defined as stabilized case temperature.
9. This parameter is guaranteed by design but is not 100% tested.
10. Except where indicated, I/O pins use Load B.
11. For a given port to Set or Clear an Interrupt Flag, 1) that port must have priority if addresses match and both $\overline{CE}_L = \overline{CE}_R$ = LOW; or 2) Addresses do not match; or 3) opposite port's $\overline{CE}$ is HIGH.
12. If the last input valid transition, which would ordinarily cause a match, occurs at the same time that the opposite port address or $\overline{CE}$ changes to a no-match condition, then $\overline{BUSY}$ will remain HIGH (i.e., if there is never a match, then $\overline{BUSY}$ remains HIGH).

* Notes listed correspond to reference made in the following sections:
- Operating Ranges
- DC Characteristics table
- Switching Characteristics table
- Switching Waveforms

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
V_{IL1}	1, 2, 3
V_{IL2}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL1}	1, 2, 3
V_{OL2}	1, 2, 3
V_{OH}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11	15	t_{WR}	7, 8, 9, 10, 11
2	t_{AA}	7, 8, 9, 10, 11	16	t_{DW}	7, 8, 9, 10, 11
3	t_{ACE}	7, 8, 9, 10, 11	17	t_{DH}	7, 8, 9, 10, 11
4	t_{AOE}	7, 8, 9, 10, 11	20	t_{RC}	7, 8, 9, 10, 11
5	t_{OH}	7, 8, 9, 10, 11	21	t_{WC}	7, 8, 9, 10, 11
8	t_{PU}	7, 8, 9, 10, 11	22	t_{BAA}	7, 8, 9, 10, 11
9	t_{PD}	7, 8, 9, 10, 11	24	t_{BAC}	7, 8, 9, 10, 11
10	t_{WC}	7, 8, 9, 10, 11	26	t_{APS}	7, 8, 9, 10, 11
11	t_{EW}	7, 8, 9, 10, 11	27	t_{WINS}	7, 8, 9, 10, 11
12	t_{AW}	7, 8, 9, 10, 11	28	t_{EINS}	7, 8, 9, 10, 11
13	t_{AS}	7, 8, 9, 10, 11	29	t_{INS}	7, 8, 9, 10, 11
14	t_{WP}	7, 8, 9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am2147

4096 x 1 Static RAM

DISTINCTIVE CHARACTERISTICS

- High speed — access times down to 35 ns maximum
- Automatic power-down when deselected
- Low power dissipation
- High output drive
- TTL compatible interface levels
- No power-on current surge

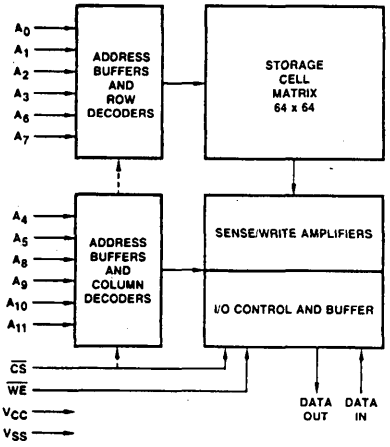
GENERAL DESCRIPTION

The Am2147 is a high- performance, 4096 x 1-bit, static, read/write, random-access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard TTL loads or up to six Schottky TTL loads.

Only a single +5-volt power supply is required. When deselected ($\overline{CS} \geq V_{IH}$), the Am2147 automatically enters a power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



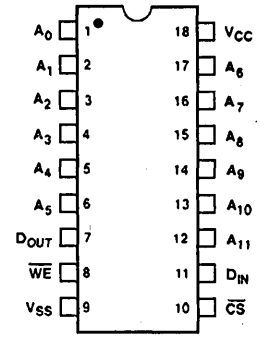
BD000051

PRODUCT SELECTOR GUIDE

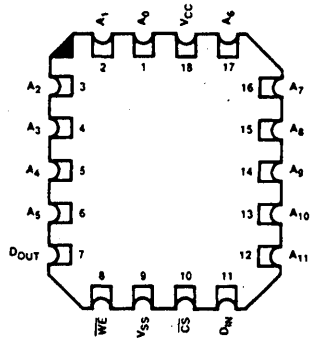
Part Number	Am2147-35	Am2147-45	Am21L47-45	Am2147-55	Am21L47-55	Am2147-70	Am21L47-70
Maximum Access time (ns)	35	45	45	55	55	70	70
Maximum Active Current (mA)	180	180	125	180	125	160 (180 mil)	125
Maximum Standby Current (mA)	30	30	15	30	15	20 (30 mil)	15
Full Military Operating Range Version		Yes		Yes		Yes	

Publication # 01940 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD000091

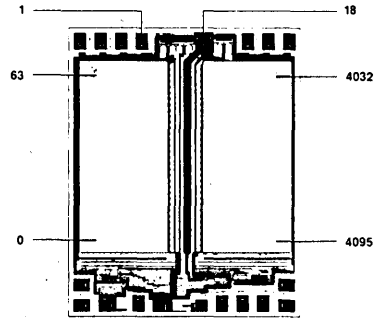


CD000100

Note: Pin 1 is marked for orientation.

BIT MAP

Address Designators	
External	**Internal**
A_0	A_2
A_1	A_5
A_2	A_4
A_3	A_3
A_4	A_8
A_5	A_7
A_6	A_1
A_7	A_0
A_8	A_{11}
A_9	A_9
A_{10}	A_{10}
A_{11}	A_6



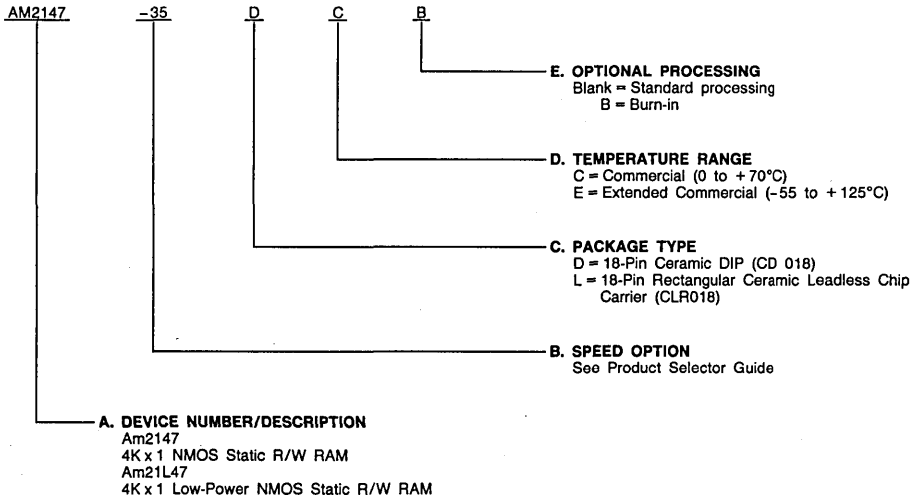
Die Size: 0.130 x 0.106

Figure 2. Bit Mapping Information

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2147-35	DC, DCB, LC, LCB
AM21L47-45	
AM21L47-55	
AM21L47-70	
AM21L47-45	DC, DCB, DE, DEB, LC, LCB, LE, LEB,
AM2147-55	
AM2147-70	

* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

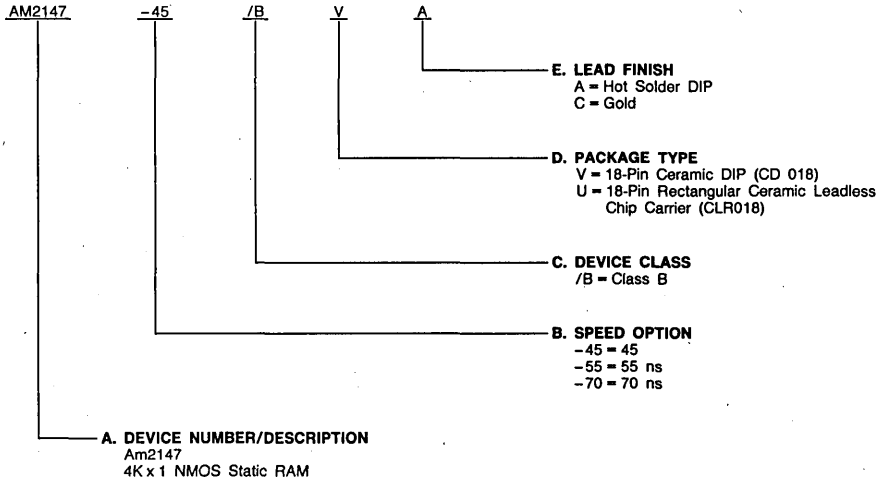
4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2147-45 AM2147-55 AM2147-70	/BVA
AM2147-45 AM2147-55 AM2147-70	/BUC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs
The address input lines select the RAM location to be read or written.

$\overline{CS}$ Chip Select (Input, Active LOW)
The Chip Select selects the memory device.

$\overline{WE}$ Write Enable (Input, Active LOW)
When $\overline{WE}$ is LOW and $\overline{CS}$ is also LOW, data is written into the location specified on the address pins.

D_{IN} Data In (Input)
This pin is used for entering data during write operations.

D_{OUT} Data Out (Output, Three-State)
This pin is three state during write operations. It becomes active when $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
Signal Voltages with
respect to ground ..... −3.5 V to +7.0 V
Power Dissipation ..... 1.2 W
DC Output Current ..... 20. mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings are for system-design reference; parameters given are not 100% tested.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A)* ..... −55 to +125°C
Supply Voltage V_{CC} ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*T_A is defined as the instant-on case temperature.

DC CHARACTERISTICS over operating range unless otherwise specified**

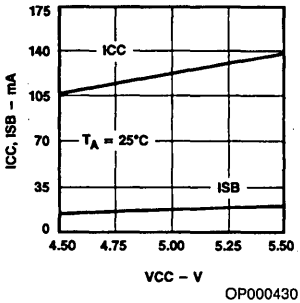
Parameter Symbol	Parameter Description	Test Conditions		Am2147-35 Am2147-45 Am2147-55 Min.	Max.	Am21L47-45 Am21L47-55 Am21L47-70 Min.	Max.	Am2147-70 Min.	Max.	Units
I_{OH}	Output High Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	T_A = 70°C	12		12		12		mA
			T_A = 125°C	8		N/A		8		
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	2.0	6.0	Volts
V_{IL}	Input Low Voltage			−2.5	0.8	−2.5	0.8	−2.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	10	−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disables	T_A = −55 to+ 125°C	−50	50	−50	50	−50	50	µA
C_I	Input Capacitance	Test Frequency = 1.0 MHz (Note 4) T_A = 25°C, All pins at 0 V, V_{CC} = 5 V			5		5		5	pF
C_O	Output Capacitance				6		6		6	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC} $\overline{CS} \leq V_{IL}$ Output Open	T_A = 0 to 70°C		180		125		160	mA
			T_A = −55 to 125°C		180		N/A		180	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, ($\overline{CS} \geq V_{IH}$) (Note 3)	T_A = 0 to 70°C		30		15		20	mA
			T_A = −55 to +125°C		30		N/A		30	

Notes:
1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V for 2147-35 and 0.8/2.0 V for −45, −55 and −70 parts.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{SB} will exceed values given.
4. These parameters are not 100% tested, but guaranteed b y characterization.
5. Chip deselected greater than 55 ns prior to selection.
6. Chip deselected less than 55 ns prior to selection.
7. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

**See the last page of this spec for Group A Subgroup Testing information.

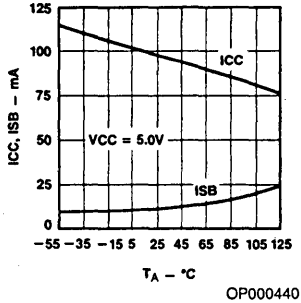
TYPICAL DC and AC CHARACTERISTICS

Supply Current Versus Supply Voltage



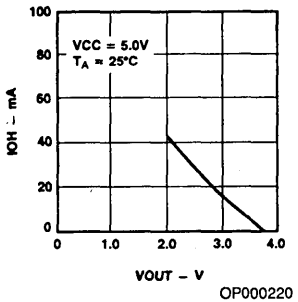
OP000430

Supply Current Versus Ambient Temperature



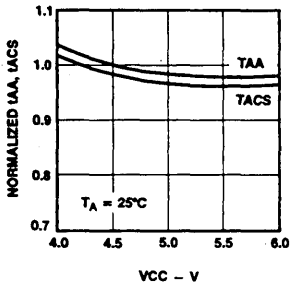
OP000440

Output Source Current Versus Output Voltage



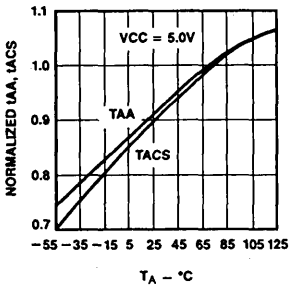
OP000220

Normalized Access Time Versus Supply Voltage



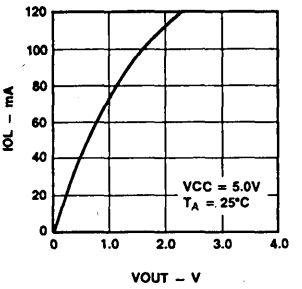
OP000760

Normalized Access Time Versus Ambient Temperature



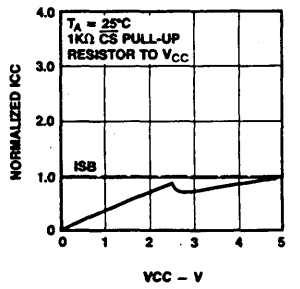
OP000230

Output Sink Current Versus Output Voltage



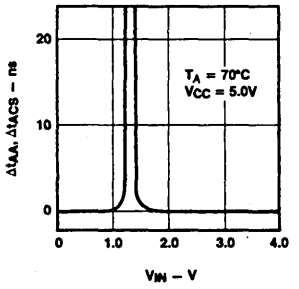
OP000240

Typical Power-On Current Versus Power Supply



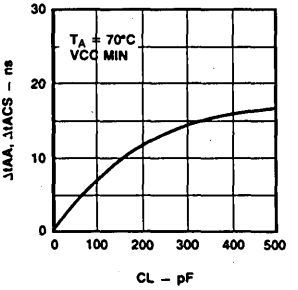
OP000870

Access Time Change Versus Input Voltage



OP000800

Access Time Change Versus Output Loading



OP000270

SWITCHING TEST CIRCUITS

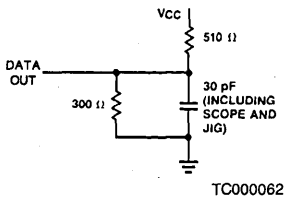


Figure 1. Output Load

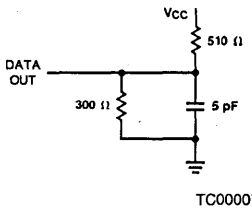


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)**

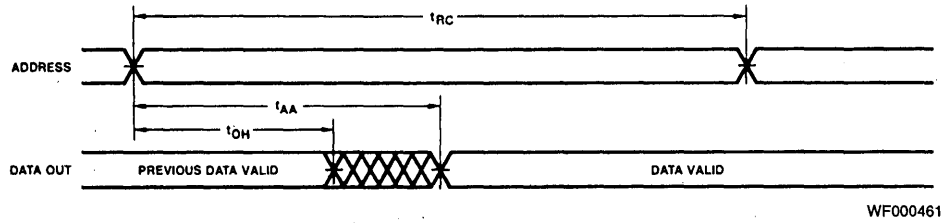
No.	Parameter Symbol	Parameter Description		Am2147-35 Min.	Am2147-35 Max.	Am2147-45 Am21L47-45 Min.	Am2147-45 Am21L47-45 Max.	Am2147-55 Am21L47-55 Min.	Am2147-55 Am21L47-55 Max.	Am2147-70 Am21L47-70 Min.	Am2147-70 Am21L47-70 Max.	Units
Read Cycle												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		70		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55		70	ns
3	t_{ACS1}	Chip Select LOW to Data Out Valid	(Note 5)		35		45		55		70	ns
4	t_{ACS2}		(Note 6)		35		45		65		80	
5	t_{LZ}	Chip Select LOW to Data Out On (Notes 4 & 7)		5		5(10*)		10		10		ns
6	t_{HZ}	Chip Select HIGH to Data Out Off (Notes 4 & 7)		0	30	0	30	0	30	0	40	ns
7	t_{OH}	Address Unknown to Data Out Unknown Time		5		5		5		5		ns
8	t_{PD}	Chip Select HIGH Power Down Delay (Note 4)			20		20		20		30	ns
9	t_{PU}	Chip Select LOW to Power Up Delay (Note 4)		0		0		0		0		ns
Write Cycle												
10	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		70		ns
11	t_{WP}	Write Enable LOW to Write Enable High (Note 2)		20		25		25		40		ns
12	t_{WR}	Write Enable HIGH to Address		0		0		10		15		ns
13	t_{WZ}	Write Enable LOW to Output in Hi Z (Notes 4 & 7)		0	20	0	25	0	25	0	35	ns
14	t_{DW}	Data In Valid to Write Enable HIGH		20		25		25		30		ns
15	t_{DH}	Data Hold Time		10		10		10		10		ns
16	t_{AS}	Address Valid to Write Enable LOW		0		0		0		0		ns
17	t_{CW}	Chip Select LOW to Write Enable HIGH (Note 2)		35		45		45		55		ns
18	t_{OW}	Write Enable HIGH to Output in Low Z (Notes 4 & 7)		0		0		0		0		ns
19	t_{AW}	Address Valid to End of Write		35		45		45		55		ns

*Military version only.
**Notes: See notes following DC Characteristics table.

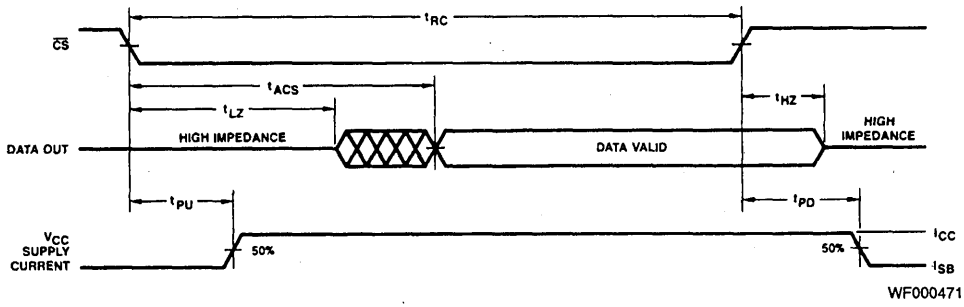
*See the last page of this spec for Group A Subgroup Testing information.

4

SWITCHING WAVEFORMS (Cont'd.)

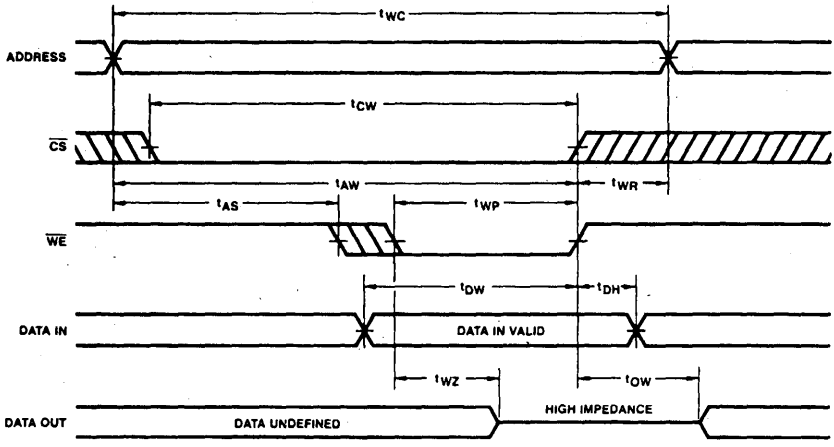


Read Cycle No. 1 (Notes 8, 9)



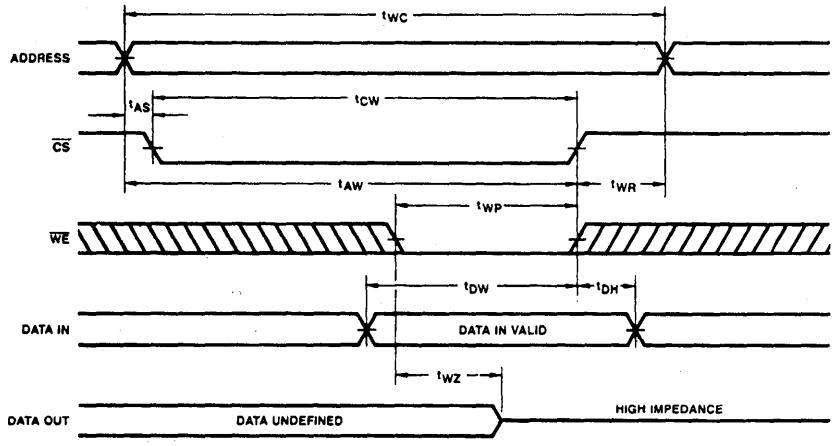
Read Cycle No. 2 (Notes 8, 10)

SWITCHING WAVEFORMS



WF000211

Write Cycle No. 1 ($\overline{WE}$ Controlled)



WF000221

Write Cycle No. 2 ($\overline{CS}$ Controlled)

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups	Parameter Symbol	Subgroups
t_{RC}	7, 8, 9, 10, 11	t_{WP}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11	t_{WR}	7, 8, 9, 10, 11
t_{ACS1}	7, 8, 9, 10, 11	t_{DW}	7, 8, 9, 10, 11
t_{ACS2}	7, 8, 9, 10, 11	t_{DH}	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11	t_{AS}	7, 8, 9, 10, 11
t_{WC}	7, 8, 9, 10, 11	t_{CW}	7, 8, 9, 10, 11
		t_{AW}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am2148/2149

1024 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35 ns
- Fully static storage and interface circuitry
- Automatic power-down when deselected (Am2148)
- TTL-compatible interface levels
- Low power dissipation
  - Am2148: 990 mW active, 165 mW power down
  - Am21L48: 688 mW active, 110 mW power down
- High output drive
  - Up to seven standard TTL loads

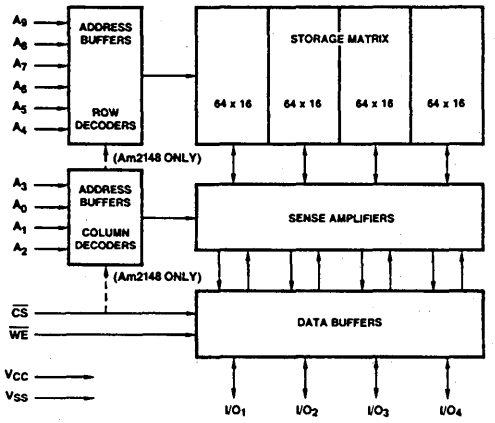
GENERAL DESCRIPTION

The Am2148 and Am2149 are high-performance, static, N-Channel, read/write, random-access memories, organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. The Am2148 and Am2149 are the same except that the Am2148 offers an automatic $\overline{CS}$ power-down feature.

The Am2148 remains in a low-power standby mode as long as $\overline{CS}$ remains HIGH, thus reducing its power requirements. The Am2148 power decreases from 990 mW to 165 mW in the standby mode. The $\overline{CS}$ input does not affect the power dissipation of the Am2149.

Data readout is not destructive and has the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied.

BLOCK DIAGRAM



BD000270

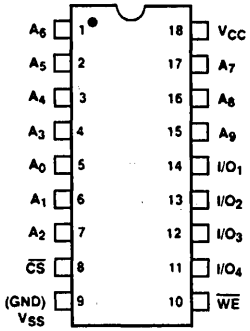
PRODUCT SELECTOR GUIDE

Part Number		Am2148/9 -35	Am2148/9 -45	Am21L48/9 -45	Am2148/9 -55	Am21L48/9 -55	Am2148/9 -70	Am21L48/9 -70
Maximum Access Time (ns)		35	45	45	55	55	70	70
I_{CC} Max. (mA)	0 to +70°C	180	180	125	180	125	180	125
I_{SB}* Max. (mA)	0 to +70°C	30	30	20	30	20	30	20
I_{CC} Max. (mA)	-55 to +125°C	N/A	180	N/A	180	N/A	180	N/A
I_{SB}* Max. (mA)	-55 to +125°C	N/A	30	N/A	30	N/A	30	N/A

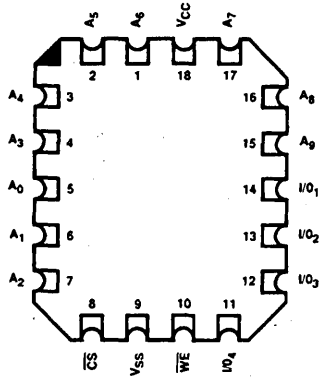
*Am2148 and Am21L48 only.

Publication # 03210 | Rev. E | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD000171

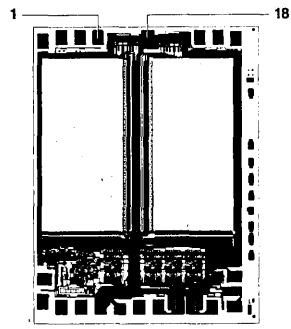


CD000350

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	**Internal**
A_0	A_7
A_1	A_8
A_2	A_9
A_3	A_6
A_4	A_5
A_5	A_4
A_6	A_3
A_7	A_2
A_8	A_1
A_9	A_0

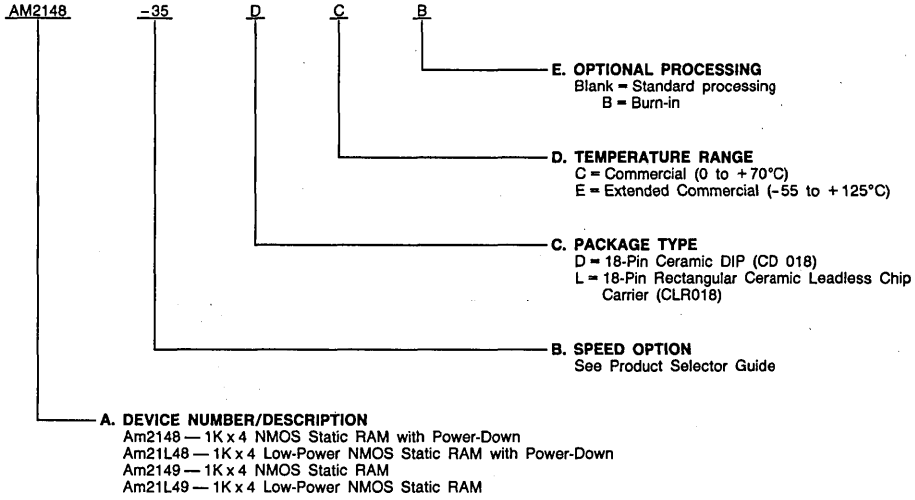


Die Size: 0.107″ x 0.145″

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM2148-35	DC, DCB, LC, LCB
AM2149-35	
AM21L48-45	
AM21L49-45	
AM21L48-55	
AM21L49-55	
AM21L48-70	
AM21L49-70	
AM2148-45	DC, DCB, DE, DEB, LC, LCB, LE, LEB,
AM2149-45	
AM2148-55	
AM2149-55	
AM2148-70	
AM2149-70	

Valid Combinations

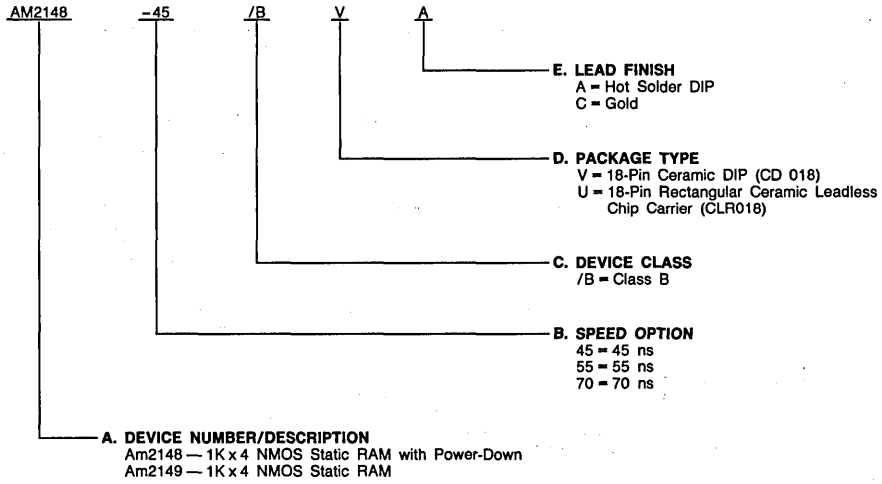
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

4

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2148-45 AM2149-45 AM2148-55 AM2149-55 AM2148-70 AM2149-70	/BVA
AM2148-45 AM2149-45 AM2148-55 AM2149-55 AM2148-70 AM2149-70	/BUC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The address input lines select the RAM location to be read or written.

$\overline{CS}$ Chip Select (Input, Active LOW)
The Chip Select selects the memory device.

$\overline{WE}$ Write Enable (Input, Active LOW)
When $\overline{WE}$ is LOW and $\overline{CS}$ is also LOW, data is written into the location specified on the address pins.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional, Active HIGH)
These I/O lines provide the path for data to be read from or written to the selected memory location.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
Signal Voltages with
Respect to Ground ..... −3.5 V to +7.0 V
Power Description ..... 1.2 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings are for system-design reference; parameters given are not 100% tested.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A*) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*T_A is defined as the "instant-ON" case temperature.

DC CHARACTERISTICS over operating range unless otherwise specified*

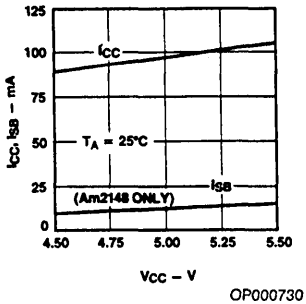
Parameter Symbol	Parameter Description	Test Conditions		Standard		Low Power		Units
				Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	T_A = 70°C	8		8		mA
			T_A = 125°C	8		N/A		
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	10		10	μA
I_{OZ}	Output Leakage Current	GND ≤ $V_O \leq V_{CC}$ Output Disabled	T_A = −55 to +125°C	−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 12)			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ Output Open	T_A = 0 to+ 70°C		180		125	mA
			T_A = −55 to+125°C		180		N/A	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, ($\overline{CS} \geq V_{IH}$)	T_A = 0 to+70°C		30		20	mA
			T_A = −55 to+125°C		30		N/A	
I_{PO}	Peak Power-On Current	Max. V_{CC}, ($\overline{CS} \geq V_{IH}$) (Notes 3 & 12)	T_A = 0 to+70°C		50		30	mA
			T_A = −55 to+125°C		50		N/A	
I_{OS}	Output Short-Circuit Current	GND ≤ $V_O \leq V_{CC}$ (Notes 11, 12)	T_A = 0 to+70°C		±275		±275	mA
			T_A = −55 to+125°C		±350		±350	

Notes:
1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pullup resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{PO} will exceed values given (Am2148 only).
4. The operating ambient temperature is defined as the "instant-ON" case temperature.
5. Chip deselected greater than 55 ns prior to selection.
6. Chip deselected less than 55 ns prior to selection.
7. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2. These parameters are sampled and not 100% tested.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
12. This parameter is sampled and not 100% tested, but guaranteed by characterization.

*See the last page of this spec for Group A Subgroup Testing information.

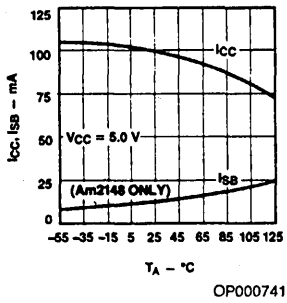
TYPICAL DC and AC CHARACTERISTICS

Supply Current Versus Supply Voltage



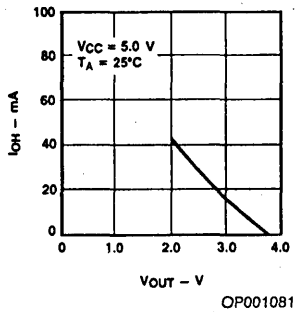
OP000730

Supply Current Versus Ambient Temperature



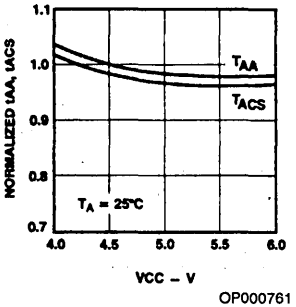
OP000741

Output Source Current Versus Output Voltage



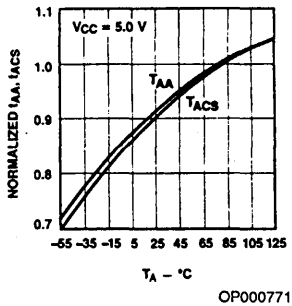
OP001081

Normalized Access Time Versus Supply Voltage



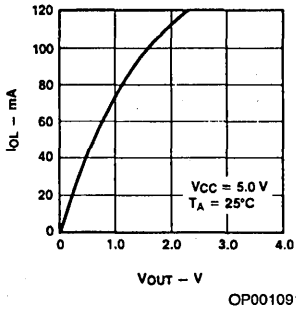
OP000761

Normalized Access Time Versus Ambient Temperature



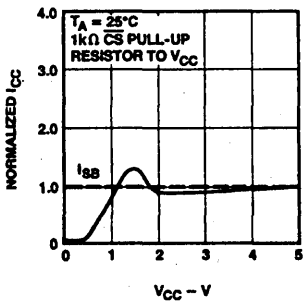
OP000771

Output Sink Current Versus Output Voltage



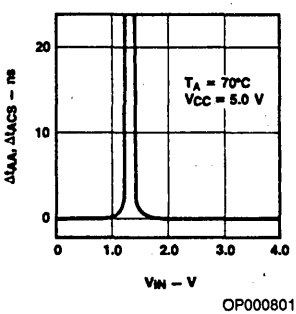
OP001091

Typical Power-On Current Versus Power Supply



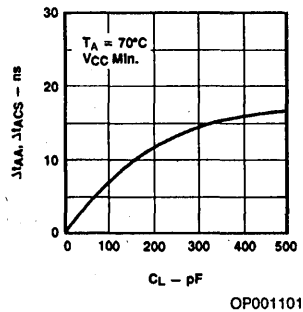
OP000791

Access Time Change Versus Input Voltage



OP000801

Access Time Change Versus Output Loading



OP001101

SWITCHING TEST CIRCUITS

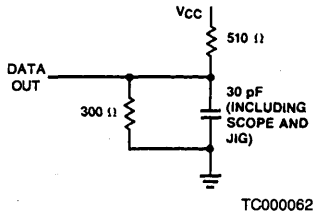
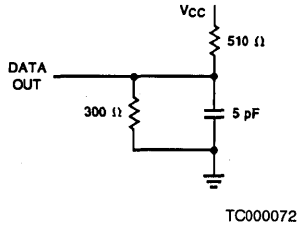


Figure 1. Output Load



Figue 2. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Note 1)**

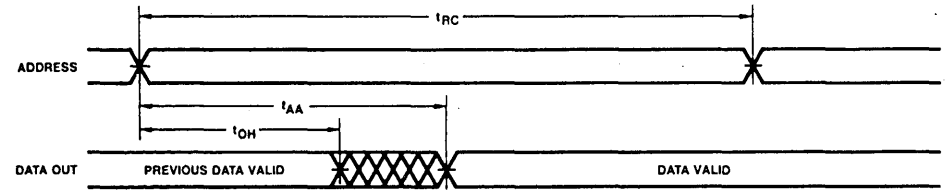
No.	Parameter Symbol	Parameter Description		Am2148/9-35 Min.	Am2148/9-35 Max.	Am2148/9-45 Am21L48/9-45 Min.	Am2148/9-45 Am21L48/9-45 Max.	Am2148/9-55 Am21L48/9-55 Min.	Am2148/9-55 Am21L48/9-55 Max.	Am2148/9-70 Am21L48/9-70 Min.	Am2148/9-70 Am21L48/9-70 Max.	Units
Read Cycle												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		70		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55		70	ns
3	t_{ACS1}	Chip Select LOW to Data Out Valid (Am2148 only)	(Note 5)		35		45		55		70	ns
4	t_{ACS2}		(Note 6)		45		55		65		80	
5	t_{ACS}	Chip Select LOW to Data Out Valid (Am2149 only)			15		20		25		30	ns
6	t_{LZ}	Chip Select LOW to Data Out On (Notes 7 & 12)	Am2148	10		10		10		10		ns
			Am2149	5		5		5		5		
7	t_{HZ}	Chip Select HIGH to Data Out Off (Notes 7 & 12)		0	20	0	20	0	20	0	20	ns
8	t_{OH}	Address Unknown to Data Out Unknown Time		0		5		5		5		ns
9	t_{PD}	Chip Select HIGH to Power Down Delay (Note 12)	Am2148		30		30		30		30	ns
10	t_{PU}	Chip Select LOW to Power Up Delay (Note 12)	Am2148	0		0		0		0		ns
Write Cycle												
11	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		70		ns
12	t_{WP}	Write Enable LOW to Write Enable HIGH (Note 2)		30		35		40		50		ns
13	t_{WR}	Write Enable HIGH to Address		5		5		5		5		ns
14	t_{WZ}	Write Enable LOW to Output in High Z (Notes 7 & 12)		0	10	0	15	0	20	0	25	ns
15	t_{DW}	Data In Valid to Write Enable HIGH		20		20		20		25		ns
16	t_{DH}	Data Hold Time		0		0		0		0		ns
17	t_{AS}	Address Valid to Write Enable LOW		0		0		0		0		ns
18	t_{CW}	Chip Select LOW to Write Enable HIGH (Note 2)		30		40		50		65		ns
19	t_{OW}	Write Enable HIGH to Output in Low Z (Notes 7 & 12)		0		0		0		0		ns
20	t_{AW}	Address Valid to End of Write		30		40		50		65		ns

**Notes: See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

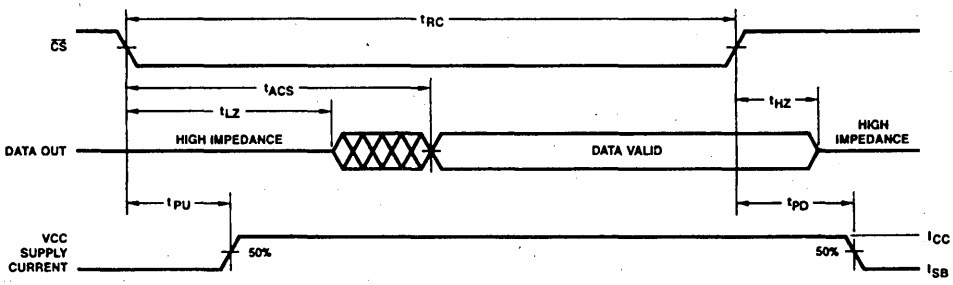
4

SWITCHING WAVEFORMS (Cont'd.)



WF000461

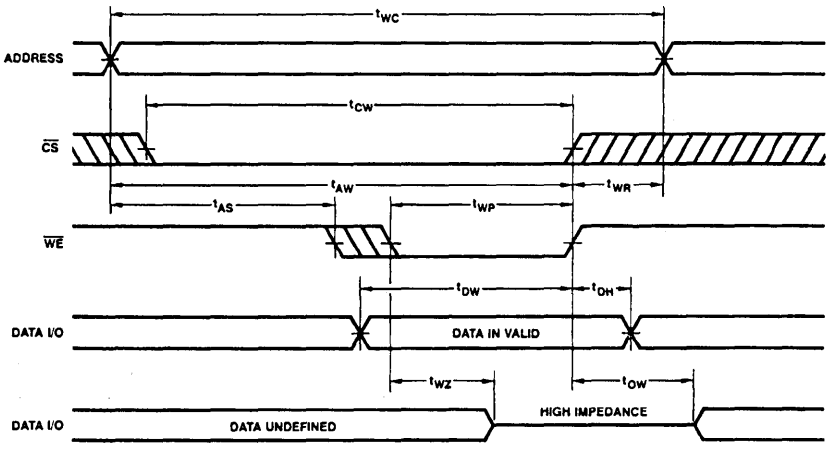
Read Cycle No. 1 (Notes 8, 9)



WF000241

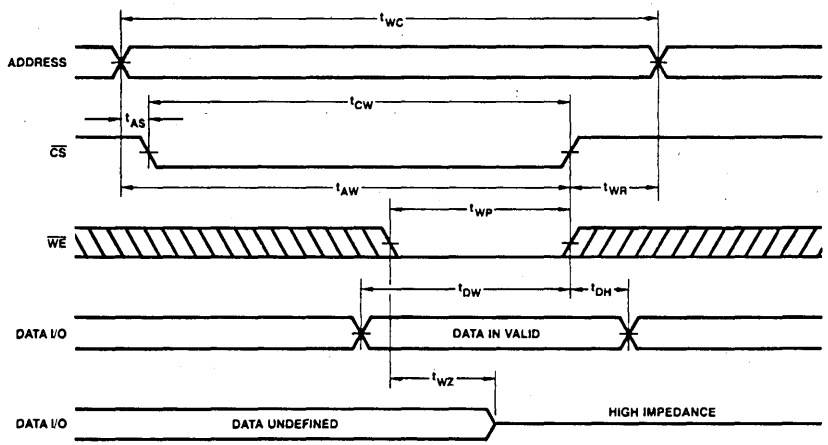
Read Cycle No. 2 (Notes 8, 10)

SWITCHING WAVEFORMS



WF000711

Write Cycle No. 1 ($\overline{WE}$ Controlled)



WF000721

Write Cycle No. 2 ($\overline{CS}$ Controlled)

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB} (Am2148 only)	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11	12	t_{WP}	7, 8, 9, 10, 11
2	t_{AA}	7, 8, 9, 10, 11	13	t_{WR}	7, 8, 9, 10, 11
3	t_{ACS1} (Am2148 only)	7, 8, 9, 10, 11	15	t_{DW}	7, 8, 9, 10, 11
4	t_{ACS2} (Am2148 only)	7, 8, 9, 10, 11	16	t_{DH}	7, 8, 9, 10, 11
5	t_{ACS} (Am2149 only)	7, 8, 9, 10, 11	17	t_{AS}	7, 8, 9, 10, 11
8	t_{OH}	7, 8, 9, 10, 11	18	t_{CW}	7, 8, 9, 10, 11
11	t_{WC}	7, 8, 9, 10, 11	20	t_{AW}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am2167

16,384 x 1 Static RAM

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35 ns maximum
- Automatic power down when deselected
- Low power dissipation
  - Am2167: 660 mW active, 110 mW power down
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL-compatible interface levels
- No power-on current surge

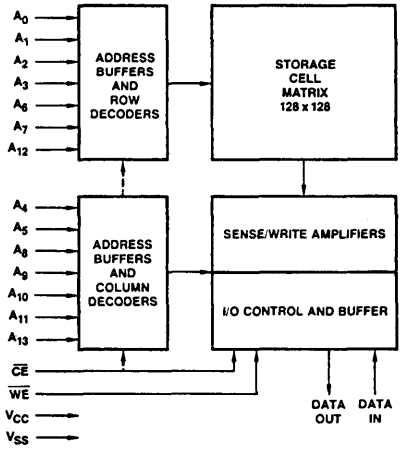
GENERAL DESCRIPTION

The Am2167 is a high-performance, 16,384-bit, static, read/write, random-access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

Only a single +5-volt power supply is required. When deselected ($\overline{CE} \geq V_{IH}$), the Am2167 automatically enters a power-down mode which reduces power dissipation by 80%.

Data In and Data Out use separate pins and are the same polarity allowing them to be connected together for operation in a common data bus environment. Data Out is a three-state output allowing similar devices to be wire-OR'd together.

BLOCK DIAGRAM



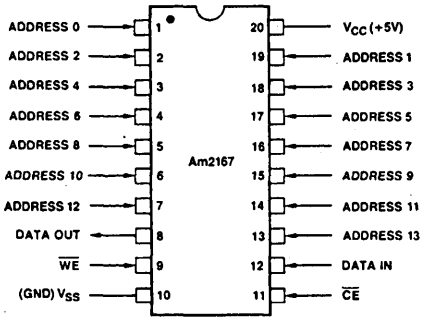
BD000170

PRODUCT SELECTOR GUIDE

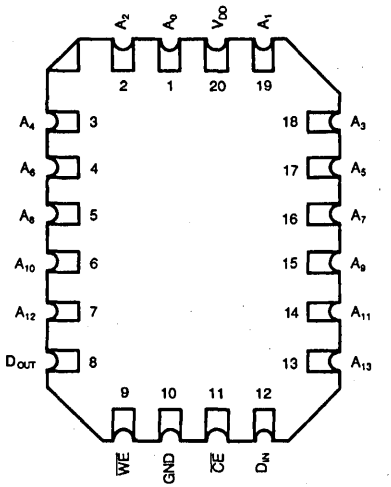
Part Number	Am2167-35	Am2167-45	Am2167-55	Am2167-70
Maximum Access Time (ns)	35	45	55	70
Maximum Active Current (mA)	120	120 (160 mil)	120 (160 mil)	120 (160 mil)
Maximum Standby Current (mA)	20	20 (30 mil)	20 (30 mil)	20 (30 mil)
Full Military Operating Range Version	No	Yes	Yes	Yes

Publication # 03211 Rev. E Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD009680

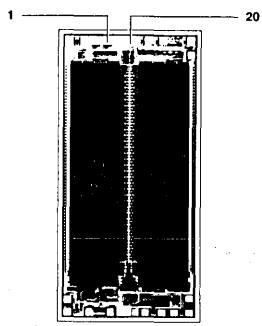


CD009690

Note: Pin 1 is marked for orientation.

BIT MAP

Address Designators	
External	**Internal**
A_0	A_1
A_1	A_6
A_2	A_2
A_3	A_5
A_4	A_3
A_5	A_0
A_6	A_4
A_7	A_{13}
A_8	A_{10}
A_9	A_6
A_{10}	A_{11}
A_{11}	A_9
A_{12}	A_{12}
A_{13}	A_7



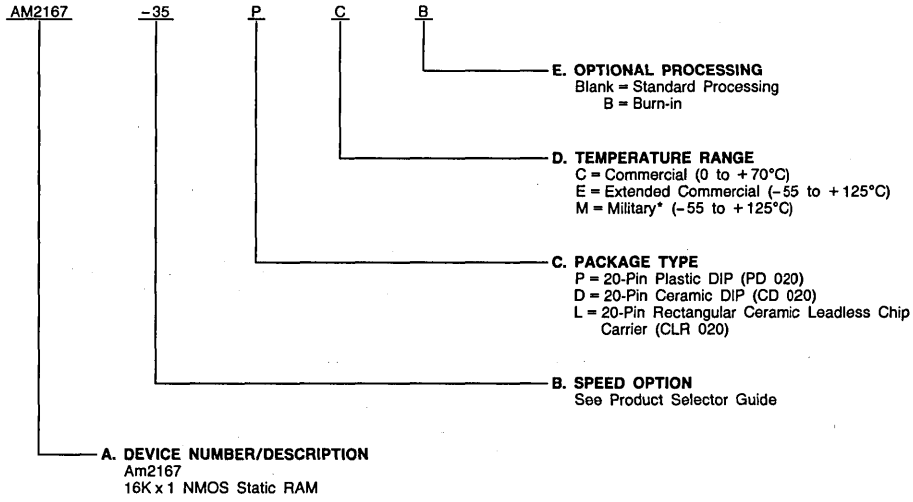
Die Size: 0.121 x 0.249

Figure 3. Bit Mapping Information

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM2167-35	PC, PCB, DC, DCB, LC, LCB
AM2167-45	PC, PCB, DC, DCB, DE, DEB,
AM2167-55	
AM2167-70	

Valid Combinations

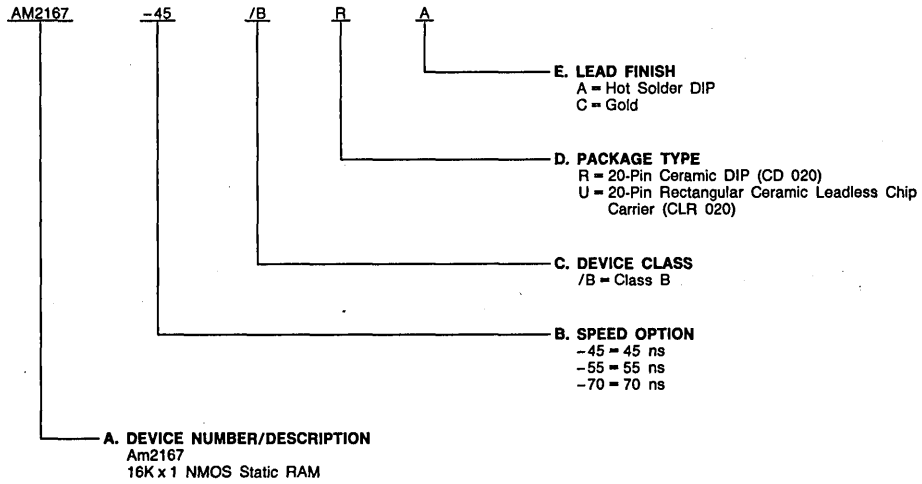
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2167-45	/BRA /BUC
AM2167-55	
AM2167-70	
AM2167-45	
AM2167-55	
AM2167-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{13}$ Address (Inputs)
The address input lines select the RAM location to be read or written.

$\overline{CE}$ Chip Enable (Input, Active LOW)
The Chip Enable selects the memory device.

$\overline{WE}$ Write Enable (Input, Active LOW)
When Write Enable is LOW and Chip Enable is also LOW, data is written into the location specified on the address pins.

D_{IN} Data (Input)
This pin issued for entering data during write operation.

D_{OUT} Data (Output, Three State)
This pin is three state during write operation. It becomes active when $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH.

V_{CC} Power Supply

V_{SS} Ground

4

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
Signal Voltages with
Respect to Ground ..... −3.5 V to +7.0 V
Power Description ..... 1.2 W
DC Output Current ..... 50 mA

Maximum rating are to be for system design reference, parameters given may not be 100% tested by AMD.

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_C for M — T_A for E Devices) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*T_A, Ambient temperature is defined to be the "instant on" case temperature

DC CHARACTERISTICS over operating range unless otherwise specified (Note 4)*

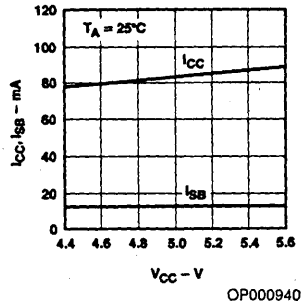
Parameter Symbol	Parameter Description	Test Conditions		Am2167-35 Min.	Am2167-35 Max.	Am2167-45, Am2167-55, Am2167-70 Min.	Am2167-45, Am2167-55, Am2167-70 Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	COM'L	16		16		mA
			MIL	12		12		
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	Volts
V_{IL}	Input LOW Voltage			−2.5	0.8	−2.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All pins at 0 V, V_{CC} = 5 V (Note 9)			5		5	pF
C_O	Output Capacitance				6		6	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC}, CE ≤ V_{IL} Output Open	COM'L		120		120	mA
			MIL		N/A		160	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	MAX V_{CC}, (CE ≥ V_{IH}) (Note 3)	COM'L		20		20	mA
			MIL		N/A		30	

Notes:
1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{SB} will exceed values given.
4. The operating ambient temperature range is guaranteed at the "instant-on" case temperature.
5. The device must be selected during the previous cycle. Otherwise t_{AA} and t_{RC} are equivalent to t_{ACS}.
6. Transition is measured ±500 mV from steady state voltage with load specified in Figure 2 for t_{HZ}, t_{LZ}, t_{OW} and t_{WZ}.
7. $\overline{WE}$ is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9. Parameter not 100% tested. Guaranteed by characterization.

*See last page of Spec for Group A Subgroup Testing Information.

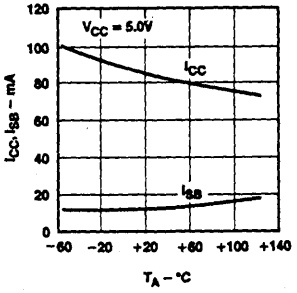
TYPICAL DC and AC OPERATING CHARACTERISTICS

Supply Current
versus Supply Voltage



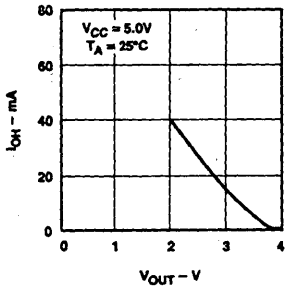
OP000940

Supply Current
versus Ambient Temperature



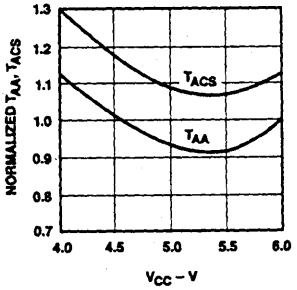
OP000950

Output Source Current
versus Output Voltage



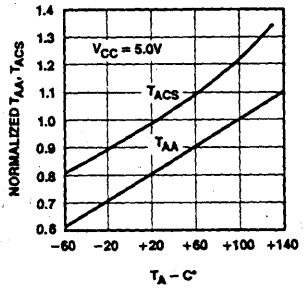
OP000960

Normalized Access Time
versus Supply Voltage



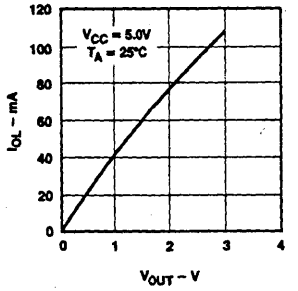
OP000970

Normalized Access Time
versus Ambient Temperature



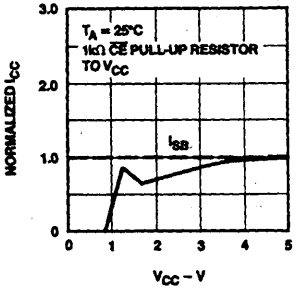
OP000980

Output Sink Current
versus Output Voltage



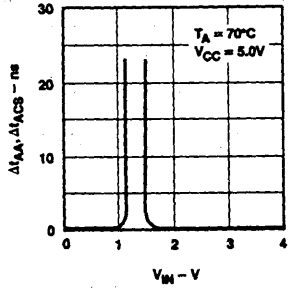
OP000990

Typical Power-On Current
versus Power Supply



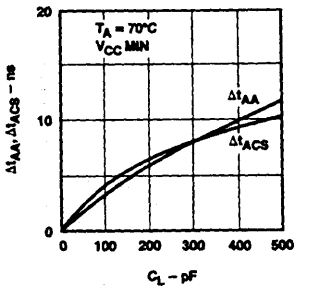
OP001000

Access Time Change
versus Input Voltage



OP001010

Access Time Change
versus Output Loading



OP001020

4

SWITCHING TEST CIRCUITS

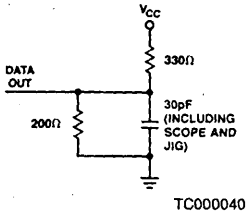


Figure 1. Output Load

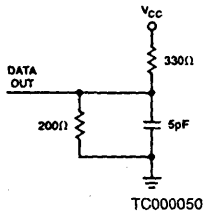


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

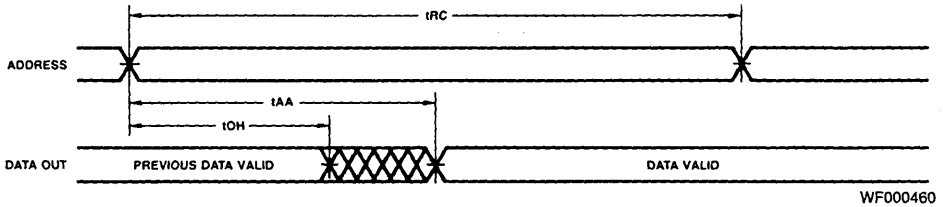
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)*

No.	Parameter Symbol	Parameter Description		Am2167-35 Min.	Am2167-35 Max.	Am2167-45 Min.	Am2167-45 Max.	Am2167-55 Min.	Am2167-55 Max.	Am2167-70 Min.	Am2167-70 Max.	Units
Read Cycle												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time) (Note 5)		30		40		50		70		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time) (Note 5)			30		40		50		70	ns
3	t_{ACS}	Chip Enable LOW to Data Out Valid (Chip Enable Access Time)			35		45		55		70	ns
4	t_{LZ}	Chip Enable LOW to Data Out On (Notes 6, 9)		5		5		5		5		ns
5	t_{HZ}	Chip Enable HIGH to Data Out Off (Notes 6, 9)		0	20	0	25	0	30	0	40	ns
6	t_{OH}	Address Unknown to Data Out Unknown Time	COM'L	3		3		3		3		ns
			MIL	1		1		1		1		ns
7	t_{PD}	Chip Enable HIGH to Power Down Delay (Note 9)			25		30		30		55	ns
8	t_{PU}	Chip Enable LOW to Power Up Delay (Note 9)		0		0		0		0		ns
Write Cycle												
9	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		30		40		50		70		ns
10	t_{WP}	Write Enable LOW to Write Enable HIGH (Note 2)		20		20		25		40		ns
11	t_{WR}	Write Enable HIGH to Address		0		0		0		0		ns
12	t_{WZ}	Write Enable LOW to Output in HIGH Z (Notes 6 & 9)		0	20	0	20	0	25	0	35	ns
13	t_{DW}	Data In Valid to Write Enable HIGH		15		15		20		30		ns
14	t_{DH}	Data Hold Time		5		5		5		5		ns
15	t_{AS1}	Address Valid to Write Enable LOW ($\overline{WE}$ Controlled Write)		5		5		5		5		ns
	t_{AS2}	Address Valid to Write Enable LOW ($\overline{CE}$ Controlled Write)		0		0		0		0		ns
16	t_{CW}	Chip Enable LOW to Write Enable HIGH (Note 2)		30		40		50		55		ns
17	t_{OW}	Write Enable HIGH to Output in LOW Z (Notes 6 & 9)		0		0		0		0		ns
18	t_{AW}	Address Valid to End of Write		30		40		50		70		ns

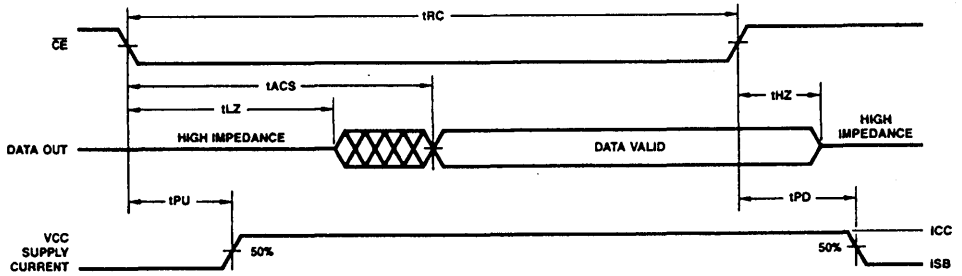
*See last page of specification for Group A Subgroup B Testing Information.

SWITCHING WAVEFORMS

READ CYCLE NO. 1 (Notes 5, 7)

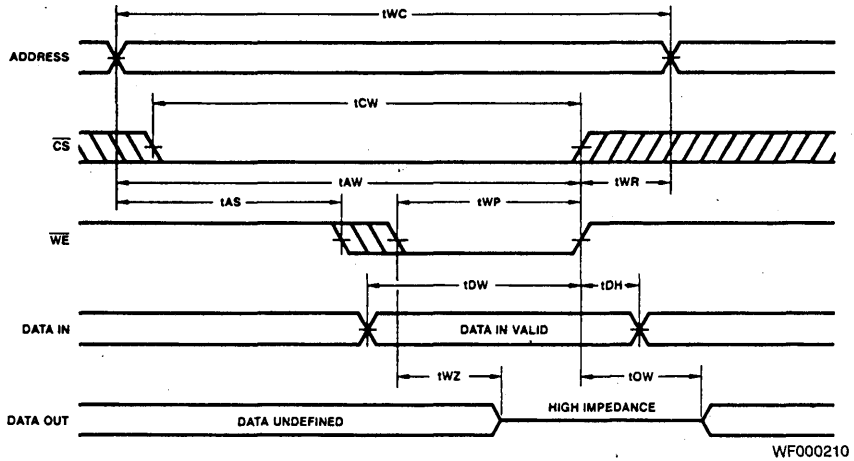


READ CYCLE NO. 2 (Notes 7, 8)



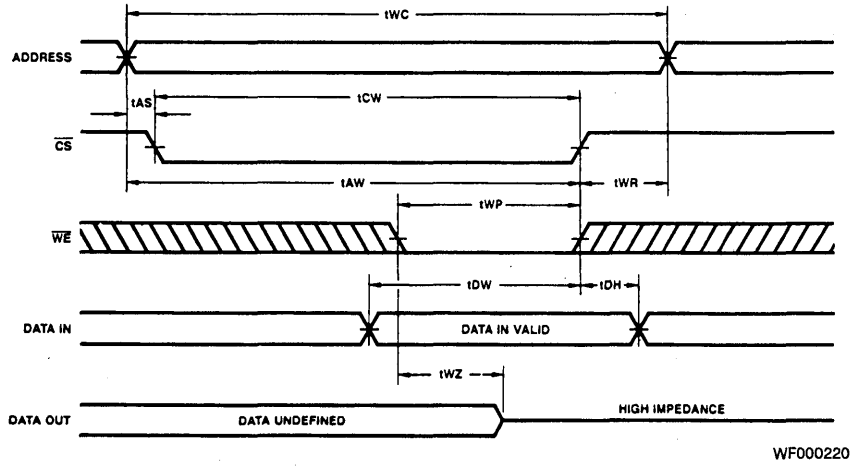
WF000280

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



WF000210

WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)



WF000220

Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbols	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbols	Subgroups	Parameter Symbols	Subgroups
t_{RC}	7, 8, 9, 10, 11	t_{DW}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11	t_{DH}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11	t_{CW}	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11	t_{AW}	7, 8, 9, 10, 11
t_{WC}	7, 8, 9, 10, 11	t_{AS1}	7, 8, 9, 10, 11
t_{WP}	7, 8, 9, 10, 11	t_{AS2}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11		

MILITARY BURN-IN

Military burn-in is in accordance with the current revisions of MIL-STD-883, Test Method 1015, Conditions A through E. Test Conditions are selected at AMD's option.

Am2168/Am2169

4096 x 4 Static R/W Random-Access Memory

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 40 ns
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected (Am2168)
- Power dissipation
  - Am2168: 660 mW active, 165 mW standby
    Am2169: 660 mW
- Standard 20-pin, .300 inch dual-in-line package
- Standard 20-pin rectangular ceramic leadless chip carrier
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL-compatible interface levels

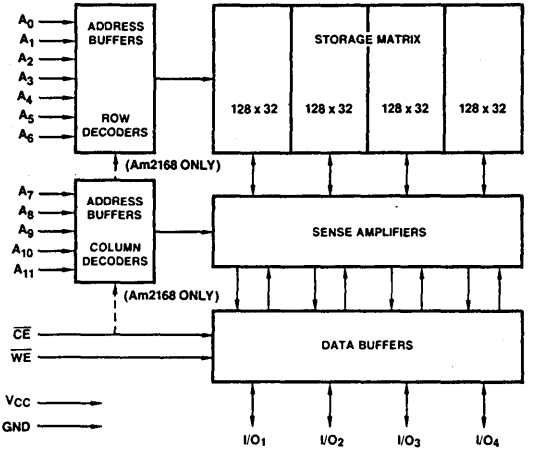
GENERAL DESCRIPTION

The Am2168 and Am2169 are high-performance, static, N-channel, read/write, random-access memories organized as 4096 words of 4 bits. Operation is from a single 5 V supply, and all input/output levels are identical to standard TTL specifications. The Am2168 and Am2169 are the same except that the Am2168 offers an automatic Chip Enable ($\overline{CE}$) power-down feature.

The Am2168 remains in a low-power standby mode as long as $\overline{CE}$ remains HIGH, thus reducing its power requirements from 660 mW to 165 mW maximum.

The data read out is not destructive and has the same polarity as the input data. The device is packaged in either a .300 slim DIP or 20-pin leadless chip carrier. The outputs of similar devices can be OR-tied and easy selection obtained by use of the $\overline{CE}$.

BLOCK DIAGRAM

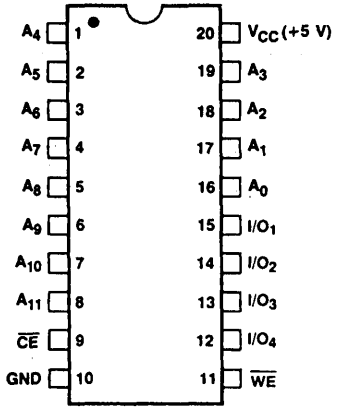


PRODUCT SELECTOR GUIDE

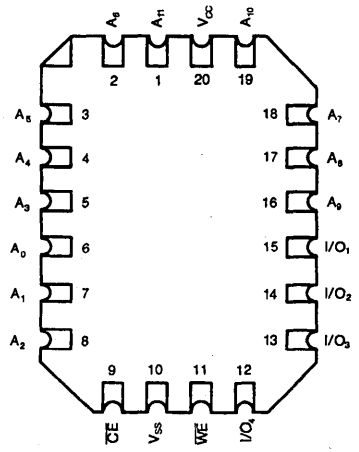
'68-35	Am2168-45	Am2169-40	Am2168-55	Am2169-50	Am2168-70	Am2169-70
5	45	40	55	50	70	70
)	120	120	120	120	120	120
	30	N/A	30	N/A	30	N/A
	160	N/A	160	160	160	160
	30	N/A	30	N/A	30	N/A

Publication # 04588 | Rev. B | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009450

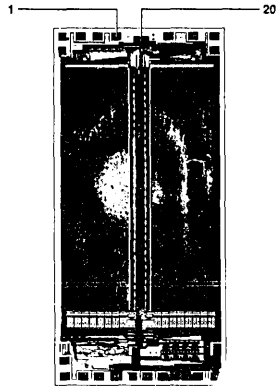


CD009282

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A_0	A_0
A_1	A_1
A_2	A_2
A_3	A_3
A_4	A_4
A_5	A_5
A_6	A_6
A_7	A_7
A_8	A_8
A_9	A_{11}
A_{10}	A_{10}
A_{11}	A_9

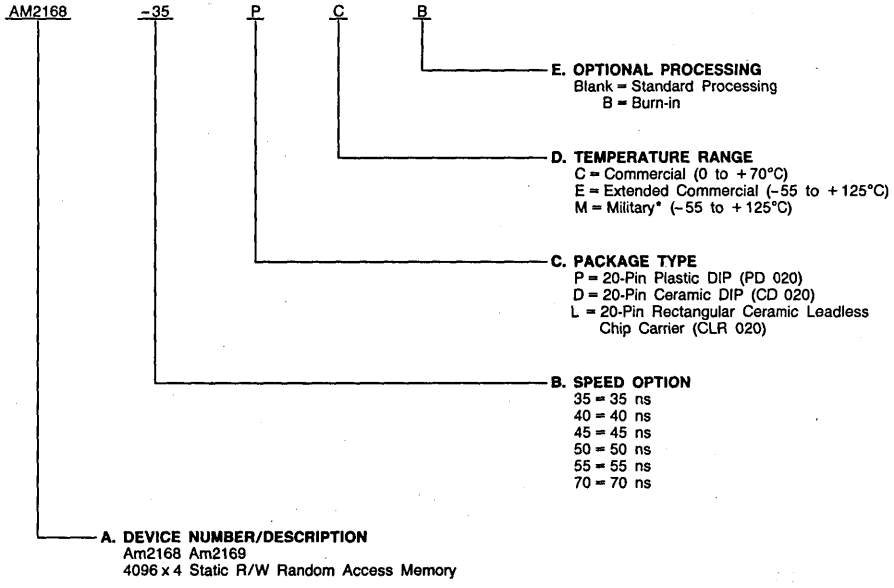


Die Size: 0.12″

ORDERING INFORMATION (Cont'd)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM2168-35	PC, PCB, DC, DCB, LC, LCB
AM2169-40	
AM2168-45	PC, PCB, DC, DCB, DE, DEB, LE, LEB
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	

Valid Combinations

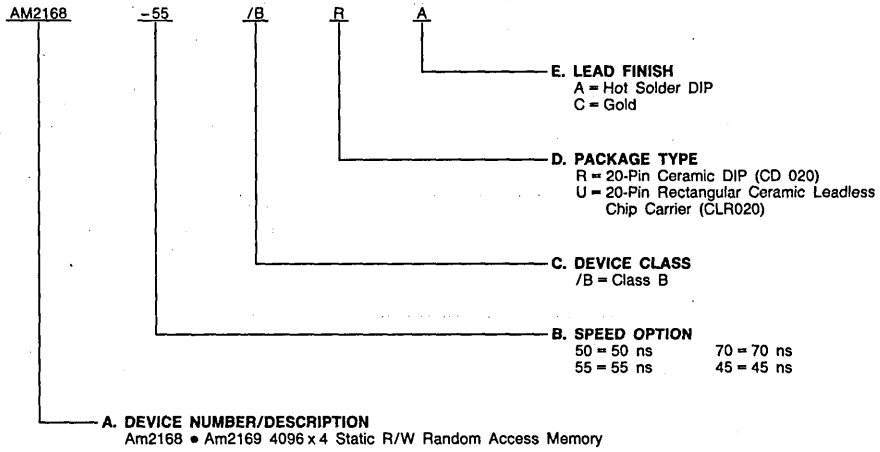
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2168-45	/BRA
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	
AM2168-45	
AM2168-55	
AM2169-50	
AM2168-70	
AM2169-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs (Inputs)
The address input lines select the RAM location to be read or written.

$\overline{CE}$ Chip Enable (Input, Active LOW)
The Chip Enable selects the memory device.

$\overline{WE}$ Write Enable (Input, Active LOW)
When Write Enable is LOW and Chip Enable is also LOW, data is written into the location specified on the address pins.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional Active HIGH)
These I/O lines provide the path for data to be read from or written to the selected memory location.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... −0.5 V to +7.0 V
All Signal Voltages ..... −3.5 V to +7.0 V
DC Output Current ..... 20 mA
Power Dissipation
  Cerdip & Leadless Packages ..... 1.2 W
  Plastic Packages ..... 0.7 W
Ambient Temperature with Power Applied
  Cerdip & Leadless Packages ..... −55 to +125°C
  Plastic Packages ..... −10 to +85°C
Storage Temperature
  Cerdip & Leadless Packages ..... −65 to +150°C
  Plastic Packages ..... −55 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

*Maximum ratings are for system design reference; parameters given may not be 100% tested.

OPERATING RANGES

Commercial (C) Devices
  Temperature (T_A)* ..... 0 to +70°C
  Supply Voltage (V_{CC}) ..... 4.5 V to +5.5 V

Extended Commercial (E) and Military (M) Devices
  Temperature
  (T_A −E Devices) (T_C −M Devices) ..... −55 to +125°C
  Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*T_A, ambient temperature, is defined as the "instant-on" case temperature.

DC CHARACTERISTICS over operating range unless otherwise specified*

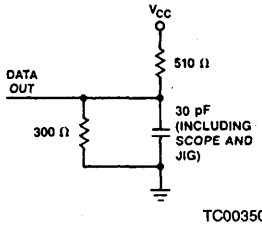
Parameter Symbol	Parameter Description	Test Conditions		Am2168-35, -45, & -40 Min.	Am2168-35, -45, & -40 Max.	Am2168-55 & -70 Am2169-50 & -70 Min.	Am2168-55 & -70 Am2169-50 & -70 Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	COM'L	8		8		mA
			MIL	8		8		
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	Volts
V_{IL}	Input LOW Voltage	Note 3		−0.5	0.8	−0.5	0.8	Volts
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disabled		−50	50	−50	50	µA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 5)			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $CE \leq V_{IL}$ Output Open	COM'L		120		120	mA
			MIL		N/A		160	
I_{SB}	Automatic $\overline{CE}$ Power Down Current (Am2168 Only)	Max. V_{CC}, ($CE \geq V_{IH}$)	COM'L		30		30	mA
			MIL		N/A		30	

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. V_{IL} voltages of less than −0.5 V on the I/O pins will cause the output current to exceed the maximum rating and thus should not exceed 30 seconds in duration.
4. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} and t_{WZ} is less than t_{OW} for all devices. Transition is measured at 1.5 V on the input to V_{OH} −500 mV and V_{OL} +500 mV on the outputs using the load shown in B. under Switching Test Circuits. C_L = 5 pF.
5. Not 100% tested parameter; parameter guaranteed by characterization.

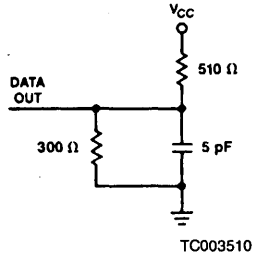
*See the last page of this spec for Group A Subgroup Testing information.

4

SWITCHING TEST CIRCUITS



A. Output Load



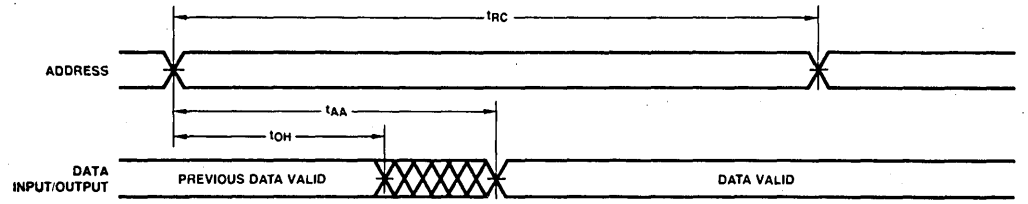
B. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)*

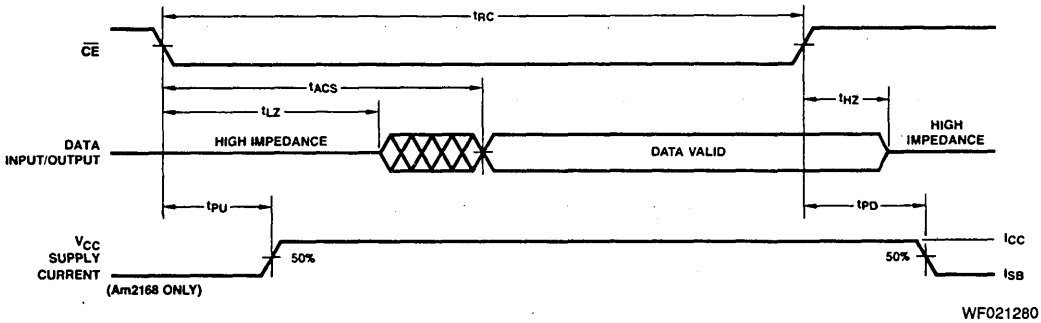
No.	Parameter Symbol	Parameter Description			Am2168-35 Min.	Am2168-35 Max.	Am2168-45, Am2169-40 Min.	Am2168-45, Am2169-40 Max.	Am2168-55, Am2169-50 Min.	Am2168-55, Am2169-50 Max.	Am2168-70, Am2169-70 Min.	Am2168-70, Am2169-70 Max.	Units
Read Cycle													
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)			35		40		50		70		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)				35		40		50		70	ns
3	t_{ACS}	Chip Enable LOW to Data Out Valid (Chip Enable Access Time)	Am2168			35		45		55		70	ns
			Am2169			35		20		25		30	
4	t_{LZ}	Chip Enable LOW to Data Out On	Am2168	Notes 4, 5	5		5		5		5		
			Am2169		2		2		2		2		
5	t_{HZ}	Chip Enable HIGH to Data Out Off		Notes 4, 5	0	20	0	20	0	25	0	30	ns
6	t_{OH}	Address Unknown to Data Out Unknown Time	COM'L		3		3		3		3		
			MIL				1		1		1		
7	t_{PD}	Chip Enable HIGH to Power-Down Delay	Am2168			35		45		55		70	ns
8	t_{PU}	Chip Enable LOW to Power-Up Delay	Am2168		0		0		0		0		ns
Write Cycle													
9	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)			35		40		50		70		ns
10	t_{WP}	Write Enable LOW to Write Enable HIGH		Note 2	30		35		45		65		ns
11	t_{WR}	Write Enable HIGH to Address Do Not Care			0		0		0		0		ns
12	t_{WZ}	Write Enable LOW to Output in Hi-Z		Notes 4, 5	0	15	0	15	0	20	0	25	ns
13	t_{DW}	Data In Valid to Write Enable HIGH			20		20		25		35		ns
14	t_{DH}	Data Hold Time			5		5		5		5		ns
15	t_{AS}	Address Valid to Write Enable LOW			0		0		0		0		ns
16	t_{CW}	Chip Enable LOW to Write Enable HIGH		Note 2	30		35		45		65		ns
17	t_{OW}	Write Enable HIGH to Output in Low-Z		Notes 4, 5	0		0		0		0		ns
18	t_{AW}	Address Valid to End of Write			30		35		45		65		ns

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Cont'd.)



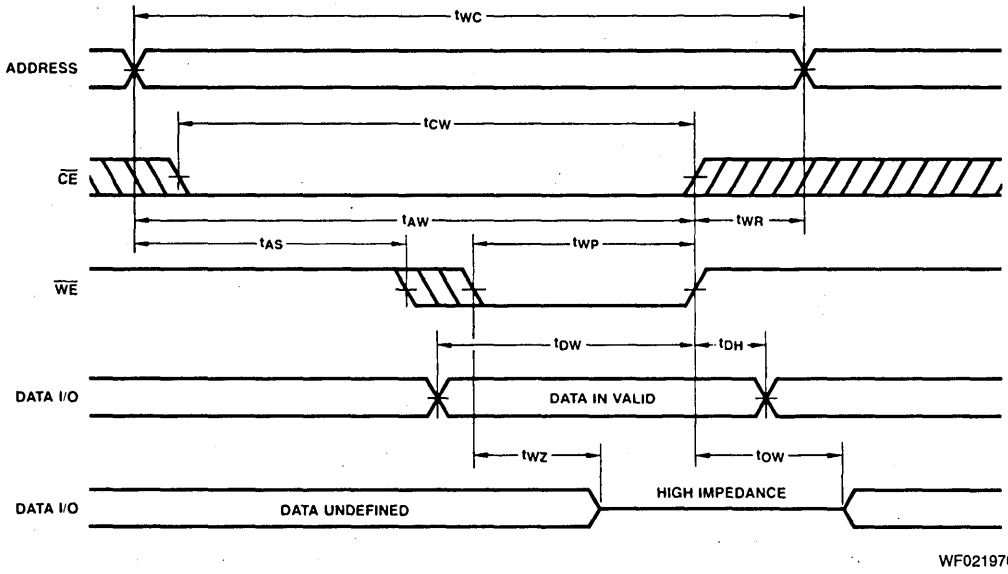
Read Cycle No. 1 ($\overline{WE}$ HIGH, $\overline{CE}$ LOW)



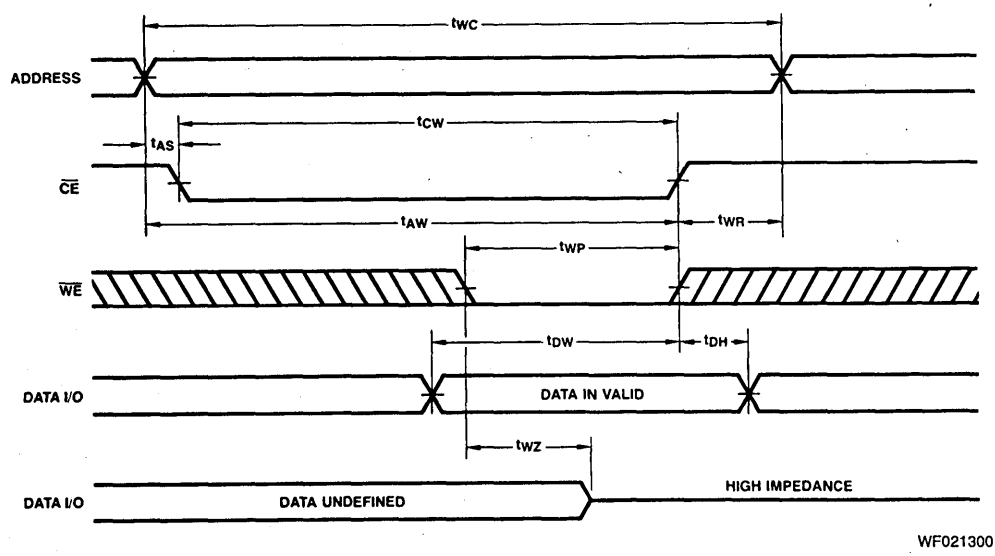
Read Cycle No. 2 ($\overline{WE}$ HIGH, Address Valid Prior to $\overline{CE}$ Transition to LOW)

4

SWITCHING WAVEFORMS



Write Cycle No. 1 ($\overline{WE}$ Controlled)

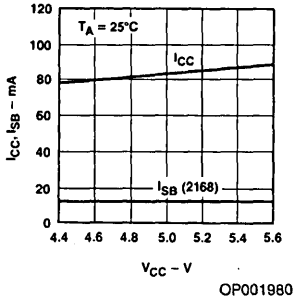


Write Cycle No. 2 ($\overline{CE}$ Controlled)

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

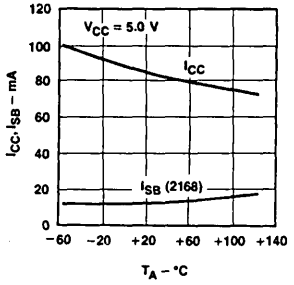
TYPICAL PERFORMANCE CURVES

Supply Current versus Supply Voltage



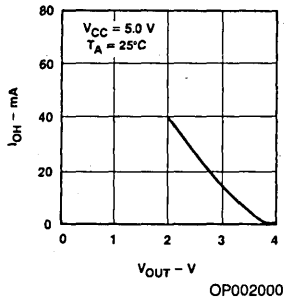
OP001980

Supply Current versus Ambient Temperature



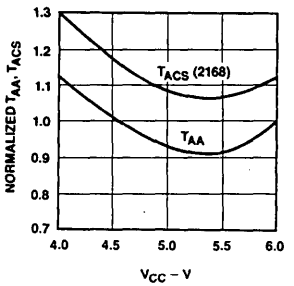
OP001990

Output Source Current versus Output Voltage



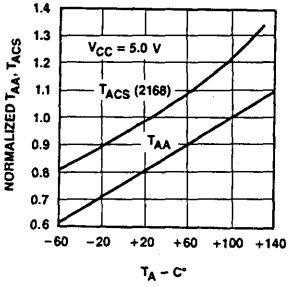
OP002000

Normalized Access Time versus Supply Voltage



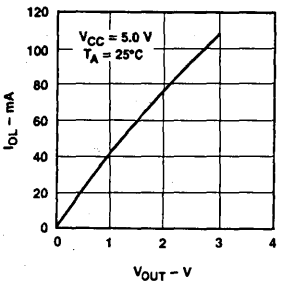
OP002010

Normalized Access Time versus Ambient Temperature



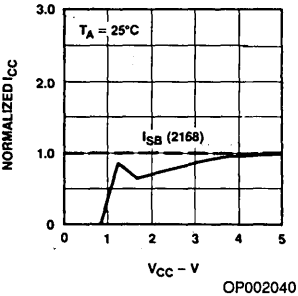
OP002020

Output Sink Current versus Output Voltage



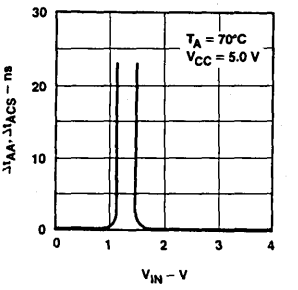
OP002030

Typical Power-On Current versus Power Supply



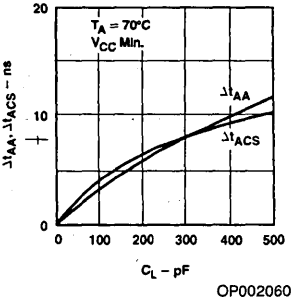
OP002040

Access Time Change versus Input Voltage



OP002050

Access Time Change versus Output Loading



OP002060

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB} (2168 only)	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11
2	t_{AA}	7, 8, 9, 10, 11
3	t_{ACS}	7, 8, 9, 10, 11
6	t_{OH}	7, 8, 9, 10, 11
9	t_{WC}	7, 8, 9, 10, 11
10	t_{WP}	7, 8, 9, 10, 11
11	t_{WR}	7, 8, 9, 10, 11
13	t_{DW}	7, 8, 9, 10, 11
14	t_{DH}	7, 8, 9, 10, 11
15	t_{AS}	7, 8, 9, 10, 11
16	t_{CW}	7, 8, 9, 10, 11
18	t_{AW}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

256K x 1 CMOS Dynamic RAM Family

Introduction

This document presents preliminary specifications on the 256K x 1 CMOS Dynamic RAM Family of products. The family consists of three device types, each with its own distinct addressing scheme. The Am90C255 features Nibble Mode addressing which allows high-speed serial access of up to 4 bits of data, resulting in significant bandwidth improvement over conventional Page Mode addressing. The Am90C256 supports Enhanced Page Mode which permits random or serial access of up to 512 bits within a row. The Static Column Mode DRAM, the Am90C257, offers a new addressing scheme which significantly reduces access times. In this method, $\overline{RAS}$ latches the row addresses are read directly from the address bus as in a static RAM. $\overline{CAS}$ can either be tied to ground or used as a chip select. Access time of 80 ns, 100 ns and 120 ns are offered on all three device types.

All three devices types have corresponding low-power versions which offer very low CMOS standby power of 0.5 mW (Max.), ideal for battery-operated or battery back-up applications. During standby (Refresh-only cycles), the refresh period can be extended to 32 ms to reduce the total current required for data retension to less than 230 μA (Max.). All three low standby power versions are screened for 100-ns, 120-ns and 150-ns access times. The low-power versions share the same AC and DC characteristics with the standard CMOS versions, except for one addition to the DC characteristics, viz CMOS standby current specified at 100 μA (Max.). These additions are presented in the Low-Power DRAM overview. All other data is supplied in the respective standard DRAM data sheet. The three low-power devices are identified as the Am90CL255 (Nibble Mode DRAM), the Am90CL256 (Enhanced Page Mode DRAM) and the AM90CL257 (Static Column Mode DRAM).

The three addressing schemes, along with the low-power options, support a wide range of applications requiring superior speed-power characteristics, such as mini-computers, professional computers, workstations, CAD/CAM systems, buffer memories, peripheral storage, etc. Besides low standby power, the CMOS process permits significantly improved soft-error immunity (<100 FITS*), thus significantly improving system reliability.

Both families are available in a 16-Pin Plastic DIP or 18-Pin Plastic Leaded Chip Carrier. Physical dimensions for these packages are provided in Section 7 of this book.

* 1 FIT (Failure in Time) = 1 Failure in 10^9 device-hours.

Am90C255

256K x 1 CMOS Nibble Mode Dynamic RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High density 256K x 1
- Low-power dissipation — 358 mW active
- High-speed operation — 80-ns access, 130-ns cycle times
- High-speed Nibble Mode
  - 15-ns access, 35-ns cycle times
- Fast Read-Modify-Write Cycle time
- Single 5-V supply
- Fast $\overline{CAS}$ output control
- Back biased substrate for high performance
- $\overline{RAS}$-only refresh

GENERAL DESCRIPTION

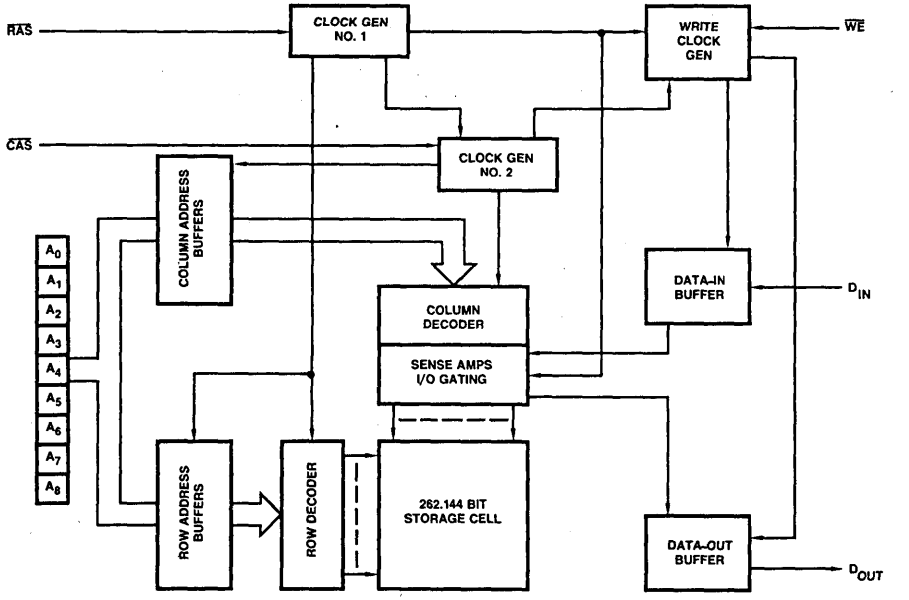
The Am90C255 is a fully decoded, CMOS Dynamic Random-Access Memory organized as 262,144 one-bit words. The design is optimized for high-speed, high-performance applications such as mainframe memory, graphics, buffer memory and peripheral storage, and battery operated applications.

The Am90C255 features "nibble mode" which allows high-speed serial access of up to four bits of data. This results in significant bandwidth improvement over conventional page mode, while simplifying system design.

The Am90C255 is fabricated using silicon gate CMOS process which permits significant improvements in speed-power characteristics. It has an on-chip fully regulated substrate bias generator which significantly improves transistor performance, and also functions as a power-up clamp which serves to protect the device from latch-ups.

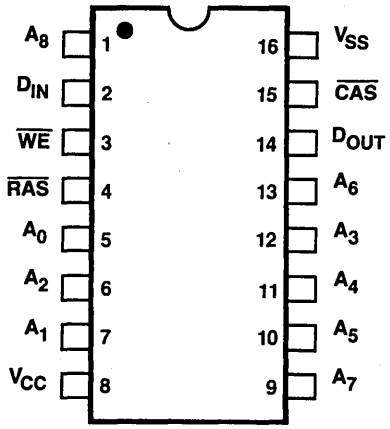
The device operates on a single 5-V supply and is stable over a wide range. All inputs and outputs are TTL-compatible. The Am90C255 is housed in a standard 16-pin, 0.3-inch wide plastic DIP.

BLOCK DIAGRAM

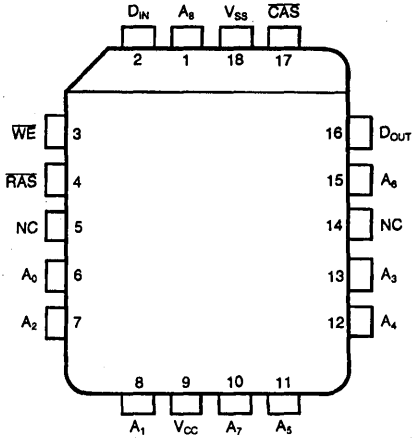


Publication # 06084 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

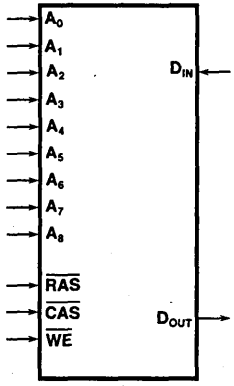


CD005843



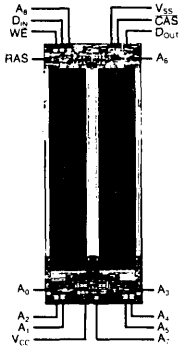
CD007080

LOGIC SYMBOL



LS001812

METALLIZATION AND PAD LAYOUT

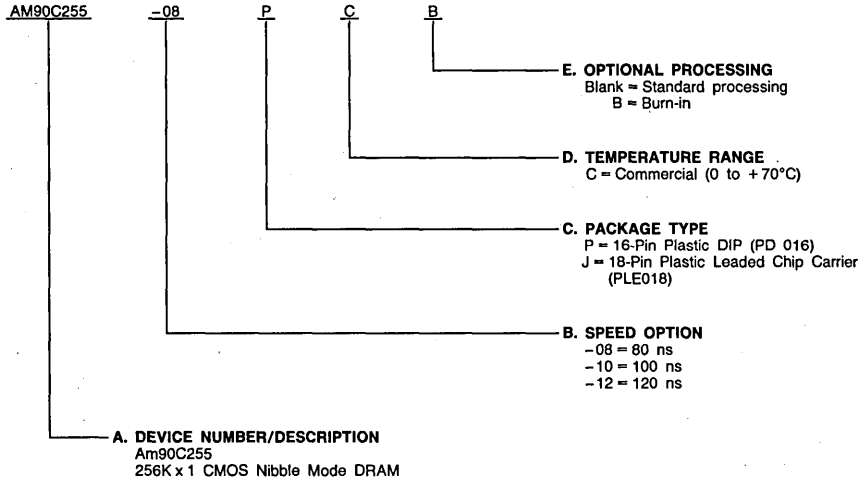


4

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

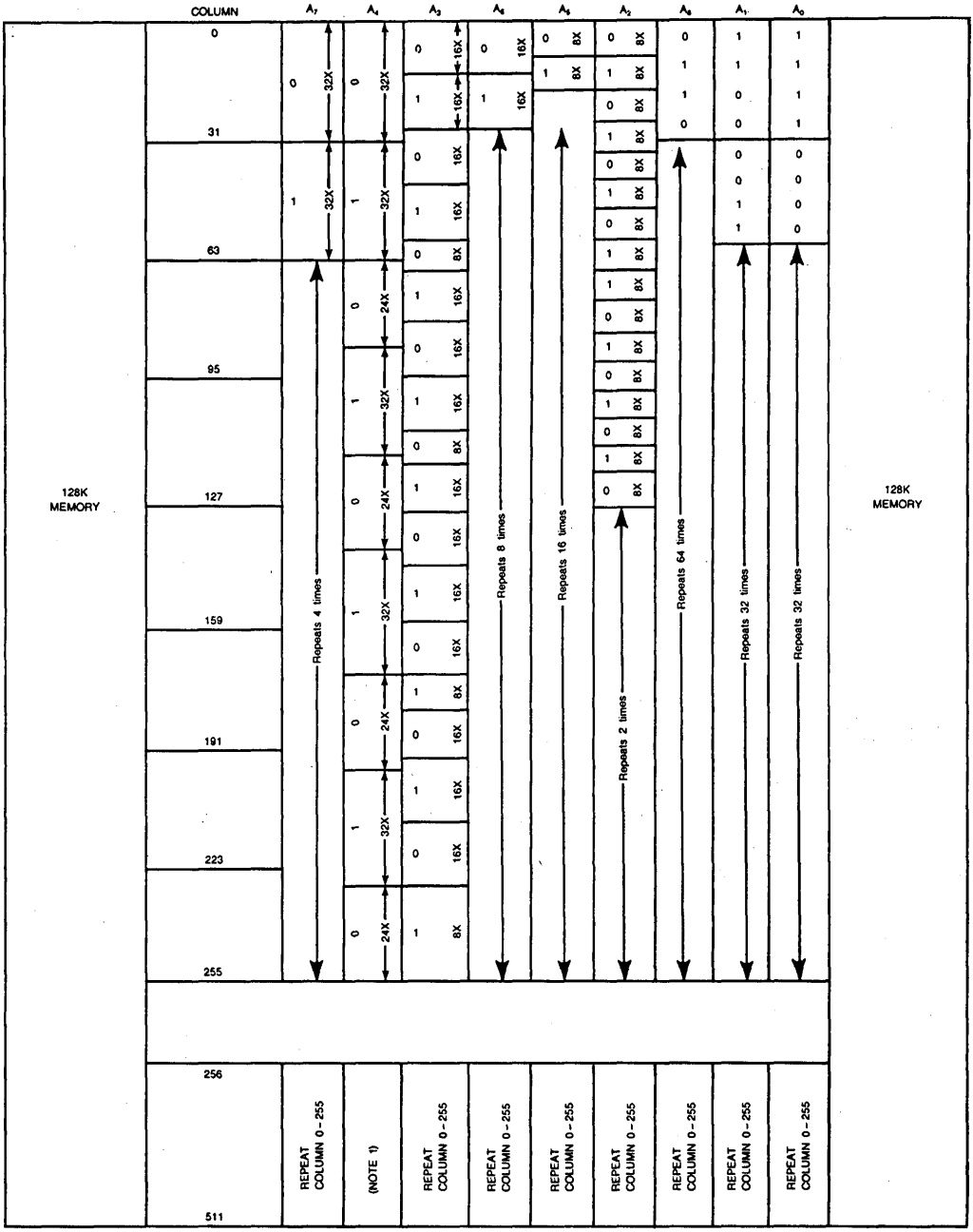


Valid Combinations	
AM90C255-08	PC, PCB JC, JCB
AM90C255-10	
AM90C255-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

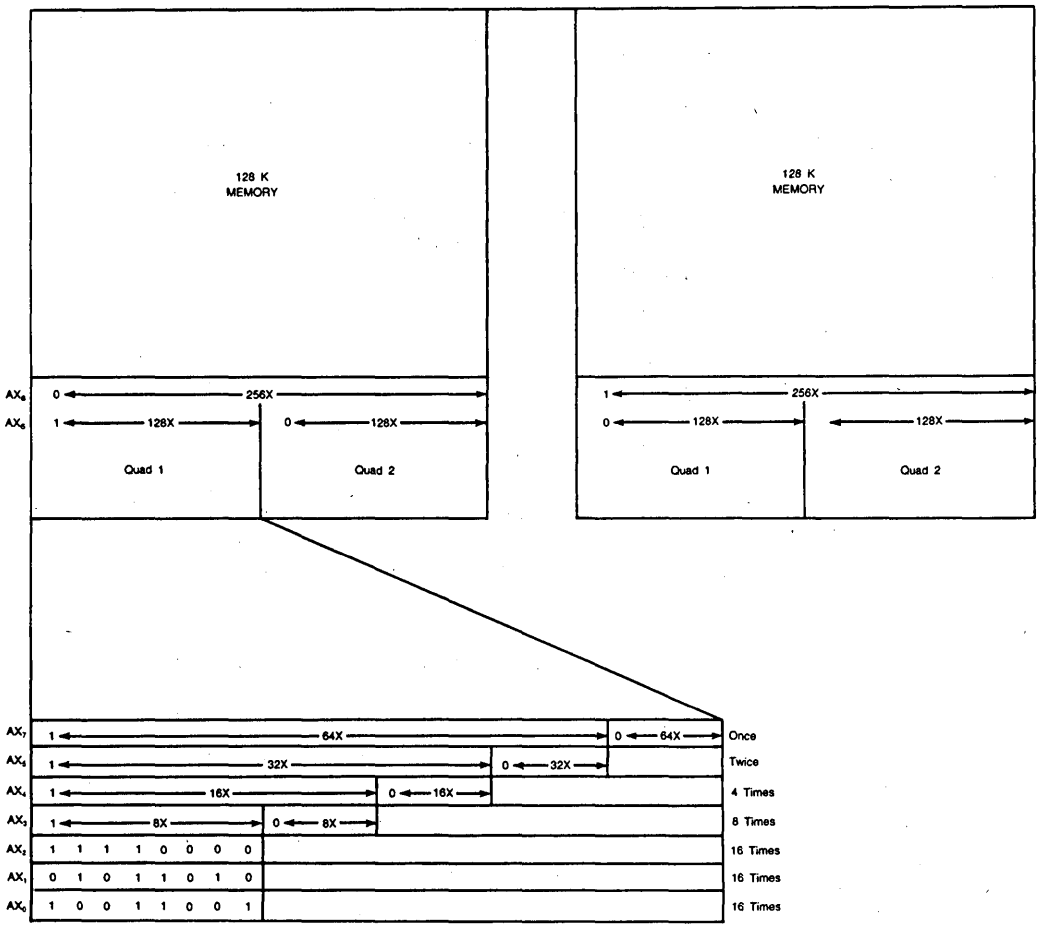
COLUMN ADDRESS TOPOLOGICAL BIT MAP



AF003960

Note: 1. Address A_4 from 256 to 511 is the inverse of address 0 to 255.

ROW ADDRESS TOPOLOGICAL BIT MAP



AF003970

Note: Quad 2 is a mirror image of AX_2 thru AX_7 in Quad 1. AX_0 and AX_1 are repeated in both quads.

PIN DESCRIPTION

$A_0 - A_8$ Nine multiplexed inputs, initially provides nine row address inputs and then nine column address inputs, all within one normal cycle. The nine row address inputs (meeting the set-up and hold times, t_{ASR} and t_{RAH}) are latched in by $\overline{RAS}$ ↓. The nine column address inputs (meeting the set-up and hold times, t_{ASC} and t_{CAH}) are latched in by $\overline{CAS}$ ↓. The combined row and column address inputs (18 total) will select one of 262,144 memory bits for Read, Write or Read-Modify-Write operation. During Nibble Mode operation, A_8 determines the starting point of the circular 4-bit nibble. Row A_8 and Column A_8 provide two binary bits needed to select one of four bits (see Section on Nibble Mode Cycles).

D_{IN} The Data Input (meeting set-up and hold times, t_{DS} and t_{DH}) is latched in by either $\overline{WE}$ ↓ or $\overline{CAS}$ ↓, whichever comes later, while $\overline{RAS}$ is LOW.

$\overline{RAS}$ The Row Address Strobe control clock. $\overline{RAS}$ ↓ latches the row address on $A_0 - A_8$ and activates a memory cycle and precharges the memory's dynamic circuits. Memory cycle time, as defined by the $\overline{RAS}$ clock, has a very large operating range. However, $\overline{RAS}$ LOW pulse width (t_{RAS}) and $\overline{RAS}$ HIGH pulse width (t_{RP}) must satisfy the specified minimum and maximum values in order to maintain continuous memory operation and data retention. $\overline{RAS}$ alone controls memory refresh function.

$\overline{CAS}$ The Column Address Strobe control clock. With $\overline{RAS}$ LOW, $\overline{CAS}$ ↓ latches the column address and activates the memory input and output operations. With $\overline{WE}$ LOW, $\overline{CAS}$ controls the input timing; with $\overline{WE}$ HIGH, $\overline{CAS}$ controls the timing of valid output. $\overline{CAS}$ HIGH turns off D_{OUT} (D_{OUT} = high impedance). In the Nibble Mode, $\overline{CAS}$ is toggled to sequentially access the three nibble bits after the first bit of the nibble is accessed in the usual manner.

$\overline{WE}$ The Write Enable control clock. $\overline{WE}$ timing, relative to $\overline{CAS}$ and $\overline{RAS}$, will define one of three memory cycles. $\overline{RAS}$ and $\overline{CAS}$, both LOW, and 1) $\overline{WE}$ HIGH, will define a Read Cycle; 2) $\overline{WE}$ LOW (meeting the set-up and hold time t_{WCS}), will define an Early Write Cycle; 3) $\overline{WE}$, first HIGH and then LOW (meeting the t_{CWD} delay time), will define a Read-Write/Read-Modify-Write Cycle.

D_{OUT} The three-state output. D_{OUT} is controlled by $\overline{CAS}$. Valid output appears on D_{OUT} in a Read Cycle after access time has elapsed (t_{CAC} or t_{RAC}, whichever applies). Last valid D_{OUT} remains valid as long as $\overline{CAS}$ is LOW. D_{OUT} can be turned off only with $\overline{CAS}$.

FUNCTIONAL DESCRIPTION

Device Initialization

Since the Am90C255 dynamic RAM is a single supply 5 V-only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up, an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 ms with device powered up), the wake-up sequence (8 active cycles) will be necessary to assure proper device operation.

Addressing The RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative), the row address strobe and the column address strobe. A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row-to-column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the Am90C255. One is called the $\overline{RAS}$-only refresh cycle (described later), where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on row address A_8 (pin 1) is not required for refresh. The other variation, which is called Nibble Mode allows the user to address 4 bits of data (serially) at a very high data rate.

Operating Cycles

Read Cycle

A Read Cycle is referred to as a Normal Read Cycle to differentiate it from a Nibble Mode Read Cycle, a Read-Write Cycle, and Read-Modify-Write Cycle which are covered in later sections.

The Memory Read Cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from HIGH to LOW. The $\overline{CAS}$ clock must also make a transition from HIGH to LOW, at the specified t_{RCD} timing limits, when the column addresses are latched. These clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. However, the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum for an access (data valid) from the $\overline{RAS}$ clock edge to be valid (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as shown in the block diagram. This gating feature on the $\overline{CAS}$ clock allows the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met, and thus defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row-to-column addresses to generate the $\overline{CAS}$ clock.

Once the clocks have become active they must stay active for certain minimums (t_{RAS} for $\overline{RAS}$ clock, t_{CAS} for the $\overline{CAS}$ clock), and the $\overline{RAS}$ clock must stay inactive for a minimum time (t_{RP}). The former is for the completion of the cycle in progress and the latter allows the device internal circuitry to be precharged for the next active cycle.

4

D_{OUT} is not latched and is valid as long as the $\overline{CAS}$ clock is active. The output will switch to the high impedance mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active before the start of the next cycle. To perform a Read Cycle, the Write Enable ($\overline{WE}$) input must be held HIGH from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}), to the time when it transitions into the inactive mode (t_{RCH}).

Write Cycle

A Write Cycle is similar to a Read Cycle except that the Write Enable ($\overline{WE}$) clock must go active LOW at or before the time the $\overline{CAS}$ clock goes active. In this case the cycle in progress is referred to as an early Write Cycle. In an early Write Cycle, the Write Clock and D_{IN} are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the Write Cycle: the column-strobe-to-write lead time (t_{CWL}) and the row-strobe-to-write lead time (t_{RWL}). These are the minimum times that the $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{WE}$ clock LOW).

It is also possible to perform a late Write Cycle. For this cycle, the Write Clock is activated after $\overline{CAS}$ goes LOW, which is beyond t_{WCS} minimum time so the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early Write Cycle and late Write Cycle is that in a late Write Cycle the Write Enable clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock.

At the start of an Early Write Cycle, D_{OUT} is in a Hi-Z condition and remains so throughout the cycle. It remains Hi-Z because the active transition of the Write Enable clock prevents the $\overline{CAS}$ clock from enabling the output buffers, as shown in the Block Diagram. This characteristic can be effectively utilized in a system that has a common input/output bus, with the only stipulation being the system must use only the early write mode.

Read-Modify-Write And Read-Write Cycles

As the name implies, both a Read and a Write Cycle are accomplished at the same cell location during a single access. The Read-Modify-Write Cycle is similar to the late Write Cycle discussed above.

For the Read-Modify-Write Cycle, a normal Read Cycle is initiated with the $\overline{WE}$ clock HIGH. After the data is read, $\overline{WE}$ is transitioned to LOW and D_{IN} is set up and held with respect to the active edge of $\overline{WE}$. This cycle assumes a zero modify time between read and write.

Another variation of the Read-Modify-Write Cycle is the Read-Write Cycle, in which the one parameter (t_{CWD}) plays an important role. A Read-Write Cycle starts as a normal Read Cycle with the $\overline{WE}$ clock being transitioned at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before D_{OUT} occurs. In this case, D_{IN} is set up with respect to the $\overline{WE}$ clock active edge.

Refresh Cycles

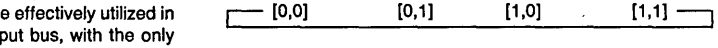
The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 ms. This is accomplished by sequentially cycling through the 256 row address locations every 4 ms. A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with that particular row decoded.

$\overline{RAS}$-Only Refresh

One method to ensure data retention is to employ the $\overline{RAS}$-only refresh scheme. In this refresh method, the system must perform a $\overline{RAS}$-only cycle on all 256 row addresses every 4 ms. The row addresses are latched with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. The $\overline{CAS}$ clock is not required and must be inactive or HIGH to conserve power.

Nibble Mode Cycles

Nibble Mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ LOW, $\overline{CAS}$ can be cycled up and then down, to read or write the next three bits at a high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycle. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A_8) determines the starting point of the circular 4-bit nibble. Row A_8 and Column A_8 provide the two binary bits needed to select one of four bits. The user can start the Nibble Mode at any one of the four bits. From then on, successive bits come out in a binary fashion (i.e., 00→01→10→11) with Row A_8 being the least significant address.

If more than 4 bits are accessed during Nibble Mode, the address will begin to repeat. If any bit is written during Nibble Mode, the new data will be written to the memory cells selected, but the new data will not be read during the same nibble sequence.

In Nibble Mode, the three-state control of D_{OUT} is determined by the first normal access cycle.

The data output is controlled only by the $\overline{WE}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle [first nibble bit]. That is, when $t_{WCS} > t_{WCS}$ minimum is met, the data output will remain open circuit throughout the succeeding Nibble Cycle regardless of the $\overline{WE}$ state. The write operation is done during the period in which the $\overline{WE}$ and $\overline{CAS}$ clock are LOW. This is demonstrated in Figures 1, 2 and 3.

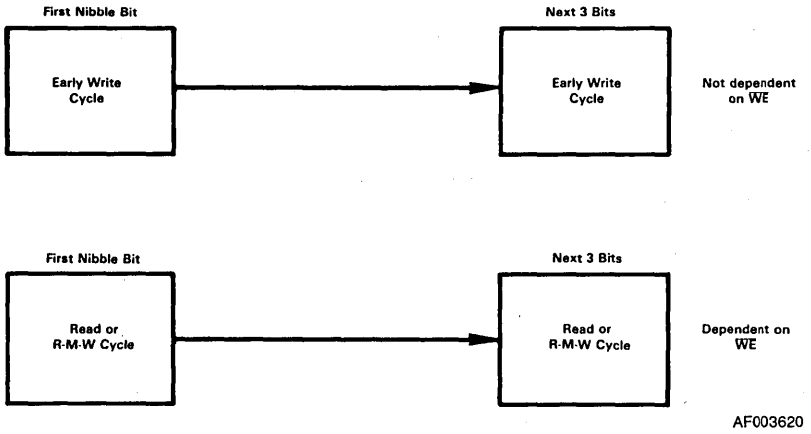


Figure 1.

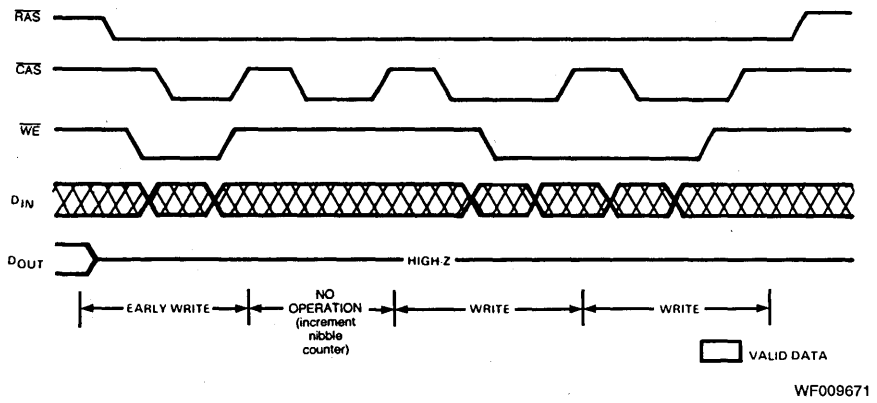


Figure 2. Case One (Nibble Cycle is an Early-Write Cycle)

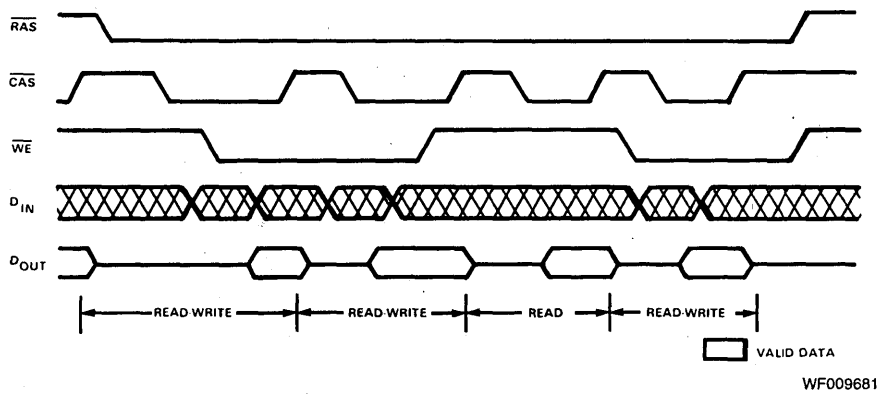


Figure 3. Case Two (Nibble Cycle is a delayed Write, Read-Write Cycle)

4

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −10 to +80°C
Voltage on Any Pin Relative to V_{SS} (Except V_{CC}) ..... −2 to +7.5 V
Voltage on V_{CC} Supply Relative to V_{SS} ..... −1 to +7.5 V
Short Circuit Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Input High Voltage (V_{IH}) ..... 2.4 V to V_{CC} +1.0 V
Input Low Voltage (V_{IL}) ..... −1.0 V to 0.8 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Part No.	Min.	Max.	Unit
V_{OH}	Output Levels	Output HIGH Voltage (I_{OH} = −5.0 mA)		2.4		V
V_{OL}		Output LOW Voltage (I_{OL} = 4.2 mA)			0.4	
V_{IH}	Input HIGH Voltage	0°C ≤ T_A ≤ + 70°C		2.4	V_{CC} +1.0 V	V
V_{IL}	Input LOW Voltage			−1.0	0.8	V
$I_{I(L)}$	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.5 V, V_{SS} = 0 V All Other Pins Not Under Test = 0 V		−10	10	μA
$I_{O(L)}$	Output Leakage Current	Data-Out Disabled, 0 V < V_{OUT} < 5.5 V		−10	10	μA
I_{CC1}	Operating Current	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	Am90C255-08		85	mA
			Am90C255-10		65	
			Am90C255-12		60	
I_{CC2}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} (TTL Level)			4	mA
I_{CC3}	V_{CC} Supply Current $\overline{RAS}$-Only Refresh	$\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} t_{RC} = Min.	Am90C255-08		85	mA
			Am90C255-10		60	
			Am90C255-12		55	
I_{CC4}	Nibble Mode Operating Current	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling t_{NC} = Min.	Am90C255-8		25	mA
			Am90C255-10		20	
			Am90C255-12		18	

Notes: 1. All voltages referenced to V_{SS}.
2. Specified I_{CC} (Max.) is measured with output open.
3. Test Conditions apply for DC Characteristics only.

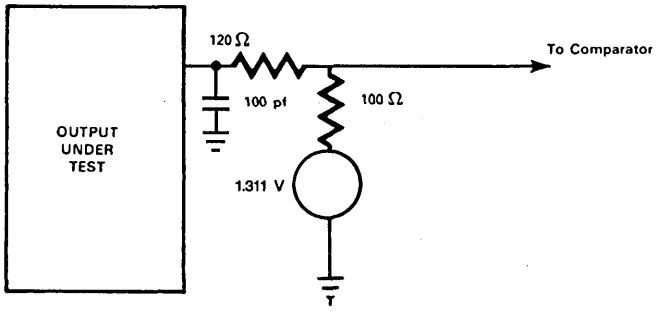
CAPACITANCE*

(T_A = +25°C, V_{CC} = 5 V, f = 1.0 MHz)

Parameter Symbol	Parameter Description	Max.	Units
C_{IN1}	Input Capacitance A_0 to A_8, D_{IN}	5	pF
C_{IN2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF
C_{OUT}	Output Capacitance D_{OUT}	6	pF

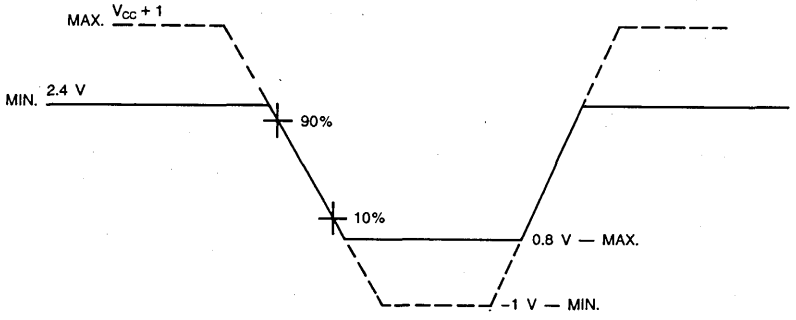
*Measured with a Booton Meter or calculated from the equation $C = I\Delta t/\Delta V$.

SWITCHING TEST CIRCUIT



TC002323

SWITCHING TEST WAVEFORM



WF010380

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

4

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90C255-08		Am90C255-10		Am90C255-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ/WRITE/READ-MODIFY-WRITE CYCLE									
1	t_{RAC}	Access Time from $\overline{RAS}$ (Note 10)		80		100		120	ns
2	t_{CAC}	Access Time from $\overline{CAS}$ (Note 10)		35		40		50	ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		65		70		ns
4	t_{RC}	R/W Cycle Time (Note 3)	130		175		200		ns
5	t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	120	10,000	ns
6	t_{CAS}	$\overline{CAS}$ Pulse Width	35	10,000	40	10,000	50	10,000	ns
7	t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	0		0		0		ns
8	t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time (Note 4)	20	45	22	60	25	70	ns
9	t_{RSH}	$\overline{RAS}$ Hold Time	35		40		50		ns
10	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		ns
11	t_{ASR}	Row Address Setup Time	3		0		0		ns
12	t_{RAH}	Row Address Hold Time	10		12		15		ns
13	t_{ASC}	Column Address Setup Time	0		0		0		ns
14	t_{CAH}	Column Address Hold Time	12		15		20		ns
15	t_{AR}	Column Address Hold Time to $\overline{RAS}$ (Note 12)							ns
16	t_T	Transition Time	3	50	3	50	3	50	ns
17	t_{OFF}	Output Disable Time	0	20	0	20	0	25	ns
18	t_{REF}	Time Between Refresh		4		4		4	ms
READ CYCLE									
19	t_{RCS}	Read Command Setup Time	0		0		0		ns
20	t_{RCH}	Read Command Hold to $\overline{CAS}$	0		0		0		ns
21	t_{RRH}	Read Command Hold to $\overline{RAS}$	20		20		20		ns
WRITE CYCLE									
22	t_{WCS}	Write Command Setup	0		0		0		ns
23	t_{WCH}	Write Command Hold Time	12		15		20		ns
24	t_{WP}	Write Command Pulse Width	12		15		20		ns
25	t_{RWL}	Write Command to $\overline{RAS}$	15		20		25		ns
26	t_{CWL}	Write Command to $\overline{CAS}$ Setup Time	15		20		25		ns
27	t_{DS}	Data-In Setup Time	0		0		0		ns
28	t_{DH}	Data-In Hold Time	12		15		20		ns
READ-MODIFY-WRITE CYCLE									
29	t_{RWC}	RMW Cycle Time (Note 5)	130		175		200		ns
30	t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time	12		15		20		ns
31	t_{RRW}	RMW $\overline{RAS}$ Pulse Width (Note 6)	80	10,000	100	10,000	120	10,000	ns
32	t_{CRW}	RMW $\overline{CAS}$ Pulse Width (Note 7)	32		40		50		ns
NIBBLE MODE READ CYCLE									
33	t_{NC}	Nibble R/W Cycle Time (Note 8)	35		40		50		ns
34	t_{NCAC}	Nibble $\overline{CAS}$ Access Time		15		20		25	ns
35	t_{NCAS}	Nibble $\overline{CAS}$ Pulse Width	15		20		25		ns
36	t_{NCP}	Nibble $\overline{CAS}$ Precharge Time	10		10		15		ns
37	t_{NRSH}	Nibble $\overline{RAS}$ Hold Time	15		20		25		ns

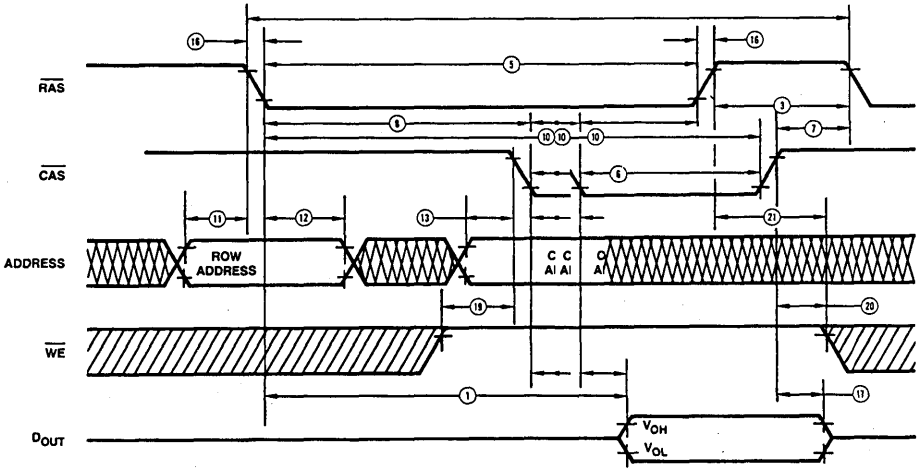
Notes: See next page for notes.

SWITCHING CHARACTERISTICS (Cont.) (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90C255-08 Min.	Am90C255-08 Max.	Am90C255-10 Min.	Am90C255-10 Max.	Am90C255-12 Min.	Am90C255-12 Max.	Unit
NIBBLE MODE WRITE CYCLE									
38	t_{NCWL}	Nibble Mode Write-to-$\overline{CAS}$ Lead Time	15		20		25		ns
39	t_{NCWD}	Nibble $\overline{CAS}$-to-$\overline{WE}$ Delay Time (Note 11)	0		0		0		ns
40	t_{NCRW}	Nibble Mode RMW $\overline{CAS}$ Pulse Width	15		20		25		ns
41	t_{NWRH}	Nibble $\overline{RAS}$ Hold Time	25		30		35		ns
42	t_{NRWC}	Nibble RMW Cycle Time (Note 9)	40		45		55		ns

Notes:
1. An initial pause of 100 µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.
2. Switching characteristics assume t_T = 5 ns. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
3. $t_{RC} = t_{RAS} + t_T + t_{RP} + t_T$.
4. $t_{RCD} = t_{RAH} + t_T + t_{ASC} + t_T$.
5. $t_{RWC} = t_{RRW} + t_{RP} + t_T + t_T$.
6. $t_{RRW} = t_{RCD}(Max) + t_{CWD} + t_T + t_{RWL}$.
7. $t_{CRW} = t_{CWD} + t_T + t_{CWL}$.
8. $t_{NC} = t_{NCAS} + t_T + t_{NCP} + t_T$.
9. $t_{NRWC} = t_{NCWD} + t_T + t_{NCWL} + t_T + t_{NCP} + t_T$.
10. All switching characteristic parameters are measured with a load equivalent of two TTL loads and 100 pF.
11. If the first Nibble Cycle is a Read-Modify-Write, the same cycle can be performed on the next three bits if $\overline{WE}$ stays LOW, or Read Cycle if $\overline{WE}$ is pulled HIGH prior to start of Nibble Cycle.
12. Timing requirements referenced to $\overline{RAS}$ are non-restrictive and are deleted from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. The hold times of the Column Address, D_{IN} and $\overline{WE}$, as well as t_{CWD} ($\overline{CAS}$-to-$\overline{WE}$ delay) are not restricted by t_{RCD}.

SWITCHING WAVEFORMS (Cont'd.)

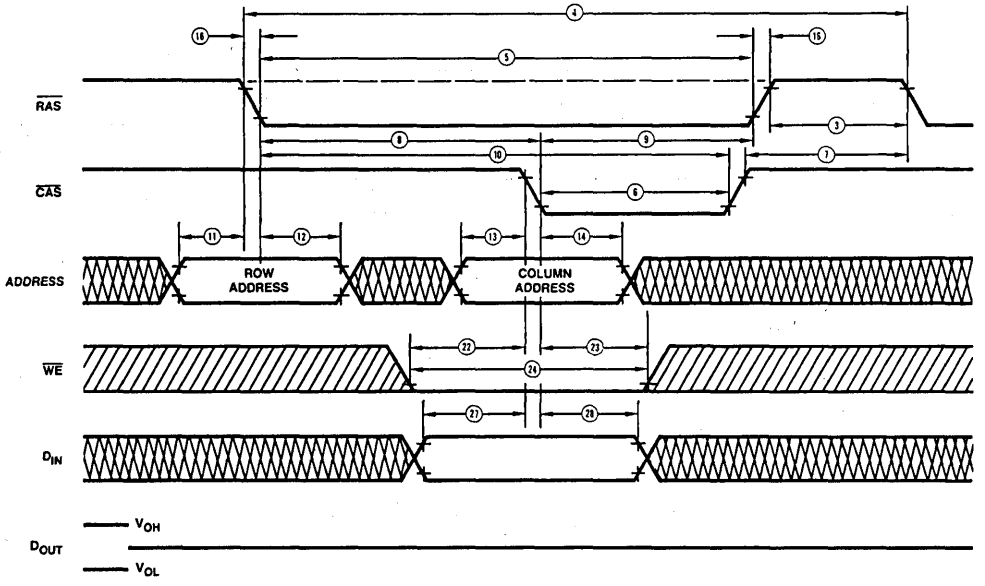


WF009692

Read Cycle

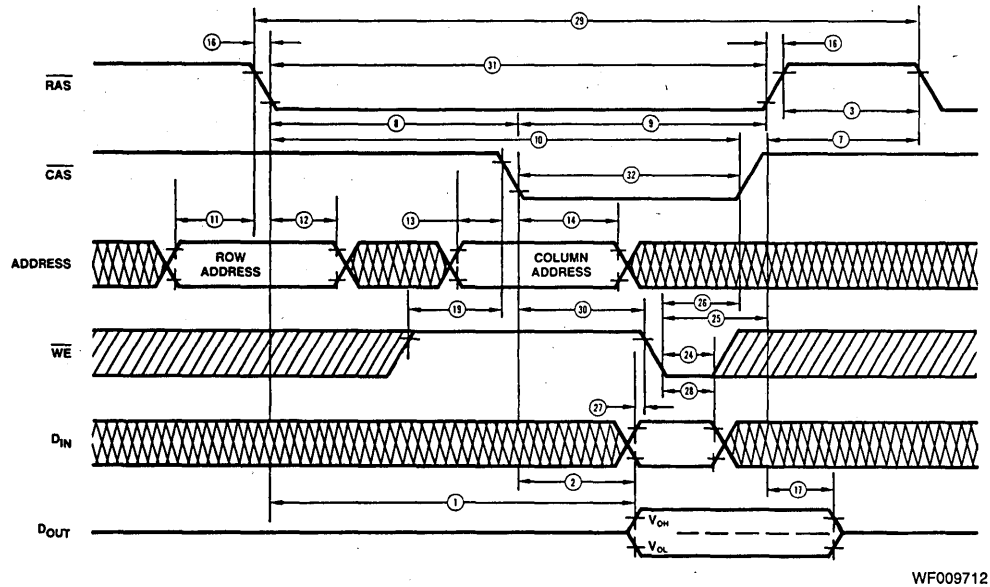
SWITCHING WAVEFORMS (Cont'd.)

WRITE CYCLE



WF009702

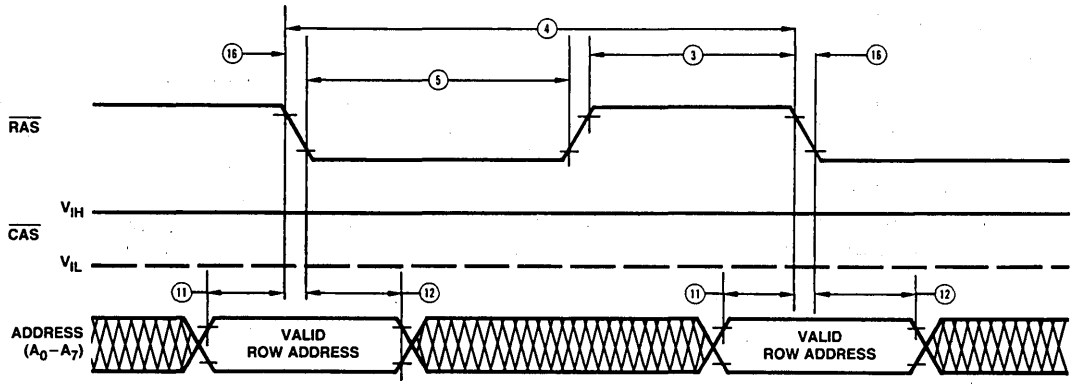
READ-MODIFY-WRITE CYCLE



WF009712

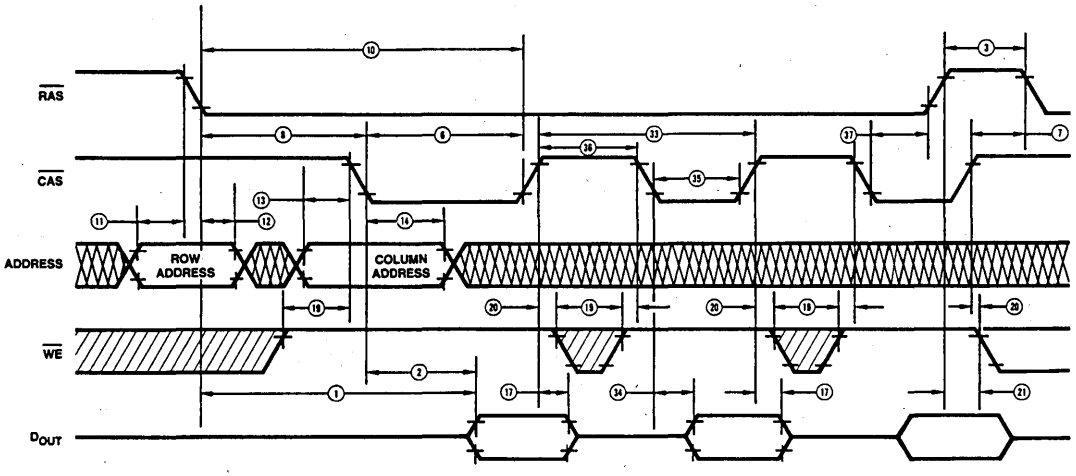
SWITCHING WAVEFORMS (Cont'd.)

$\overline{RAS}$-ONLY REFRESH



WF009721

NIBBLE MODE READ CYCLE

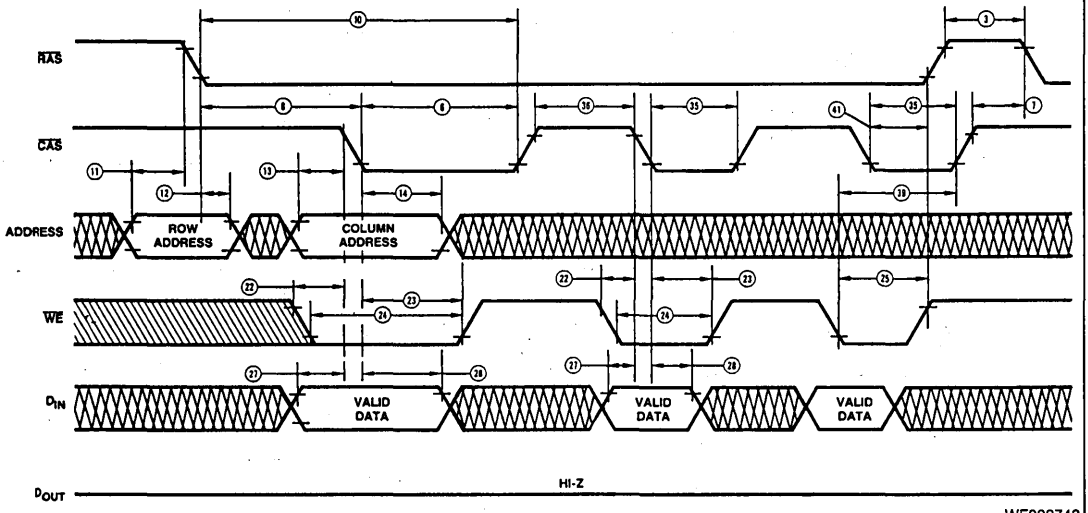


WF009731

4

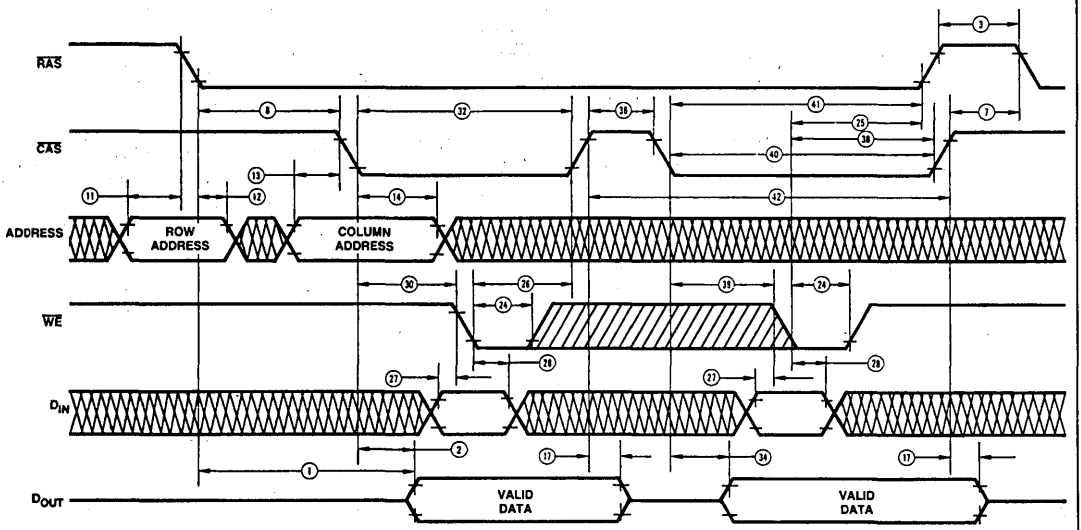
SWITCHING WAVEFORMS (Cont'd.)

NIBBLE MODE WRITE CYCLE



WF009742

NIBBLE MODE READ-MODIFY-WRITE CYCLE



WF009752

Am90CL255

Low-Power 256K x 1 CMOS Nibble Mode DRAM

OVERVIEW

The 256K x 1 CMOS Low-Power ('L') DRAM versions share common functional descriptions, DC and AC characteristics with the corresponding standard CMOS (non-'L') versions. The only additions to these sections are:

DISTINCTIVE CHARACTERISTICS

- Extended refresh period
  — 32 ms (Max.) during standby
- Low data retention current
  — 230 μA (Max.)
- Low-power dissipation
  — 0.55 mW (Max.)

ORDERING INFORMATION

The Ordering Information for the Low-Power DRAM versions are the same as for the Standard CMOS DRAMs, with the exception of an 'L' inserted within the device number to denote 'Low-Power.' For example, the Am90CL255 is = a 256K x 1 CMOS "Low-Power" Nibble Mode DRAM. All temperature ranges, speed and package options remain the same as those listed in Ordering Information sections for the respective Standard CMOS DRAMs.

DC CHARACTERISTICS

The low-power version DRAMs are screened for one additional parameter, viz, CMOS standby current. All other DC characteristics remain the same for both families.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{CC5}	V_{CC} Supply Current CMOS Standby	$\overline{RAS} \geq V_{CC} - 0.5$ V and $\overline{CAS}$ at V_{IH}, all other inputs and outputs $\geq V_{SS}$	Am90CL255		0.1	mA

The Am90CL255-15 is screened for I_{CC1} = 55 mA, I_{CC3} = 50 mA, and I_{CC4} = 16 mA.

AC CHARACTERISTICS

AC Characteristics remain unchanged on the low-power 100 ns and 120 ns versions. The AC characteristics corresponding to the 150 ns speed are on the following pages.

FUNCTIONAL DESCRIPTION

The Functional Descriptions for low-power versions are the same as the corresponding standard versions. The low-power devices, however, support Extended Refresh cycles described below:

Extended Refresh Cycle

All low-power versions extend the Refresh Cycle period to 32 ms for $\overline{RAS}$-Only Refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA for data retention. The low-standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})\ (I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{T_{RI}}$$

where t_{RC} = Refresh Cycle Time

and t_{RI} = Refresh Interval Time or $t_{REF}/256$

Before entering or leaving an Extended Refresh period, the entire array must be refreshed at the normal interval of 4 ms. This can be accomplished by either a burst or distributed refresh.

Publication # 07412 | Rev. A | Amendment /0
Issue Date: May 1986

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL255-15 Min.	Am90CL255-15 Max.	Units
READ/WRITE/READ-MODIFY-WRITE CYCLE					
1	t_{RAC}	Access Time from $\overline{RAS}$ (Note 10)		150	ns
2	t_{CAC}	Access Time from $\overline{CAS}$ (Note 10)		60	ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	85		ns
4	t_{RC}	R/W Cycle Time (Note 3)	245		ns
5	t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	ns
6	t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	ns
7	t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	0		ns
8	t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time (Note 4)	30	90	ns
9	t_{RSH}	$\overline{RAS}$ Hold Time	60		ns
10	t_{CSH}	$\overline{CAS}$ Hold Time	150		ns
11	t_{ASR}	Row Address Setup Time	0		ns
12	t_{RAH}	Row Address Hold Time	20		ns
13	t_{ASC}	Column Address Setup Time	0		ns
14	t_{CAH}	Column Address Hold Time	25		ns
15	t_{AR}	Column Address Hold Time to $\overline{RAS}$ (Note 12)			ns
16	t_T	Transition Time	3	50	ns
17	t_{OFF}	Output Disable Time	0	30	ns
18	t_{REF}	Time Between Refresh		4	ms
READ CYCLE					
19	t_{RCS}	Read Command Setup Time	0		ns
20	t_{RCH}	Read Command Hold to $\overline{CAS}$	0		ns
21	t_{RRH}	Read Command Hold to $\overline{RAS}$	20		ns
WRITE CYCLE					
22	t_{WCS}	Write Command Setup	0		ns
23	t_{WCH}	Write Command Hold Time	25		ns
24	t_{WP}	Write Command Pulse Width	25		ns
25	t_{RWL}	Write Command to $\overline{RAS}$	30		ns
26	t_{CWL}	Write Command to $\overline{CAS}$ Setup Time	30		ns
27	t_{DS}	Data-In Setup Time	0		ns
28	t_{DH}	Data-In Hold Time	25		ns
READ-MODIFY-WRITE CYCLE					
29	t_{RWC}	RMW Cycle Time (Note 5)	245		ns
30	t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time	25		ns
31	t_{RRW}	RMW $\overline{RAS}$ Pulse Width (Note 6)	150	10,000	ns
32	t_{CRW}	RMW $\overline{CAS}$ Pulse Width (Note 7)	60		ns
NIBBLE MODE READ CYCLE					
33	t_{NC}	Nibble R/W Cycle Time (Note 8)	60		ns
34	t_{NCAC}	Nibble $\overline{CAS}$ Access Time	30		ns
35	t_{NCAS}	Nibble $\overline{CAS}$ Pulse Width	30		ns
36	t_{NCP}	Nibble $\overline{CAS}$ Precharge Time	20		ns
37	t_{NRSH}	Nibble $\overline{RAS}$ Hold Time	30		ns

Notes: See next page for notes.

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL255-15 Min.	Am90CL255-15 Max.	Units
NIBBLE MODE WRITE CYCLE					
38	t_{NCWL}	Nibble Mode Write-to-$\overline{CAS}$ Lead Time	30		ns
39	t_{NCWD}	Nibble $\overline{CAS}$-to-$\overline{WE}$ Delay Time (Note 11)	0		ns
40	t_{NCRW}	Nibble Mode RMW $\overline{CAS}$ Pulse Width	30		ns
41	t_{NWRH}	Nibble $\overline{RAS}$ Hold Time	40		ns
42	t_{NRWC}	Nibble RMW Cycle Time (Note 9)	65		ns

Notes:
1. An initial pause of 100 µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.
2. Switching characteristics assume t_T = 5 ns. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
3. $t_{RC} = t_{RAS} + t_T + t_{RP} + t_T$.
4. $t_{RCD} = t_{RAH} + t_T + t_{ASC} + t_T$.
5. $t_{RWC} = t_{RRW} + t_{RP} + t_T + t_T$.
6. $t_{RRW} = t_{RCD}(Max) + t_{CWD} + t_T + t_{RWL}$.
7. $t_{CRW} = t_{CWD} + t_T + t_{CWL}$.
8. $t_{NC} = t_{NCAS} + t_T + t_{NCP} + t_T$.
9. $t_{NRWC} = t_{NCWD} + t_T + t_{NCWL} + t_T + t_{NCP} + t_T$.
10. All switching characteristic parameters are measured with a load equivalent of two TTL loads and 100 pF.
11. If the first Nibble Cycle is a Read-Modify-Write, the same cycle can be performed on the next three bits if $\overline{WE}$ stays LOW, or Read Cycle if $\overline{WE}$ is pulled HIGH prior to start of Nibble Cycle.
12. Timing requirements referenced to $\overline{RAS}$ are non-restrictive and are deleted from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. The hold times of the Column Address, D_{IN} and $\overline{WE}$, as well as t_{CWD} ($\overline{CAS}$-to-$\overline{WE}$ delay) are not restricted by t_{RCD}.

4

Am90C256

256K x 1 CMOS Enhanced Page Mode Dynamic RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Continuous data rate over 25 MHz
- Random access within a row
- Flow-through column latch for pipelining
- Low operating current – 70 mA
- High-speed operation – 80-ns $\overline{RAS}$ access, 130-ns $\overline{RAS}$ cycle time, – 20-ns $\overline{CAS}$ access
- Fully TTL compatible

GENERAL DESCRIPTION

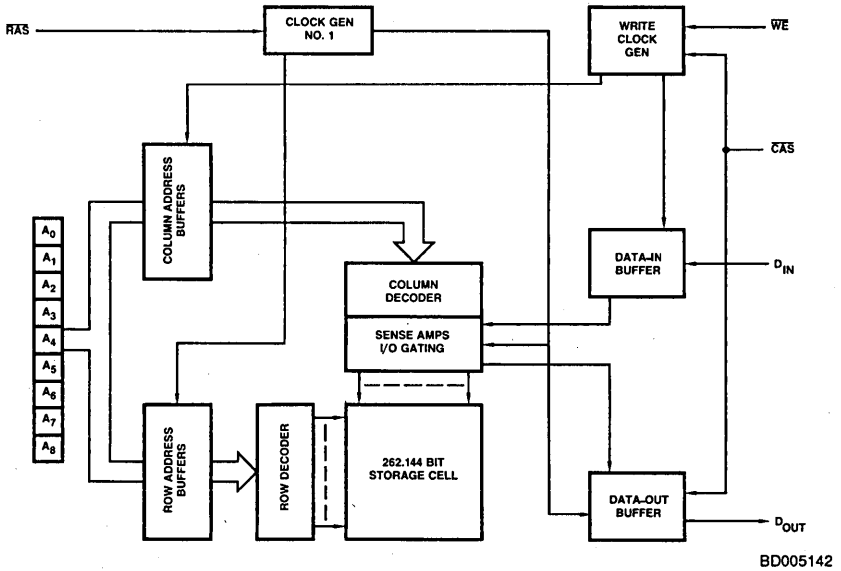
The Am90C256 is a fully decoded, CMOS Dynamic Random-Access Memory organized as 262,144 one-bit words. The device offers an Enhanced Page Mode Feature which permits very high-speed accesses ideal for graphics, digital signal processing and cache applications.

The Enhanced Page Mode allows random or sequential access of up to 512 bits within a row, with cycle times as fast as 45 ns. Because of static column circuitry, the $\overline{CAS}$ clock is no longer in the critical timing path. The flow-through column latch allows address pipelining while relaxing many critical system requirements.

The Am90C256 is fabricated using silicon gate CMOS process which permits significant improvements in speed-power characteristics.

The device operates on a single 5-V supply and is stable over a wide range. All inputs and outputs are TTL-compatible. The Am90C256 is housed in a standard 16-pin, 0.3-inch wide plastic DIP.

BLOCK DIAGRAM

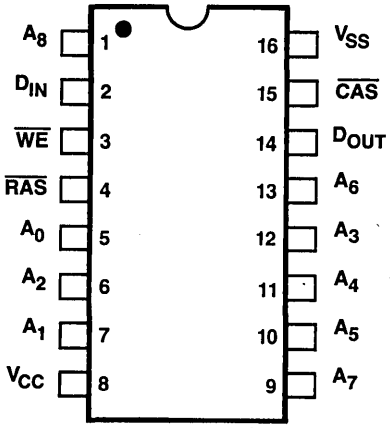


PRODUCT SELECTOR GUIDE

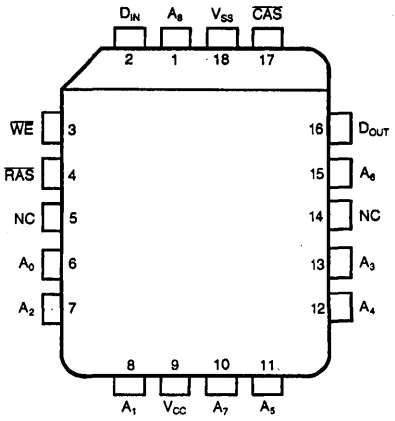
Part Number	Am90C256-08	Am90C256-10	Am90C256-12
$\overline{RAS}$ Access Time	80 ns	100 ns	120 ns
Temperature Range	Commercial	Commercial	Commercial

Publication # 06954 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

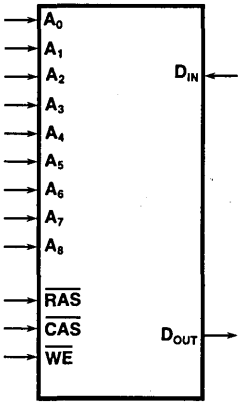


CD005843



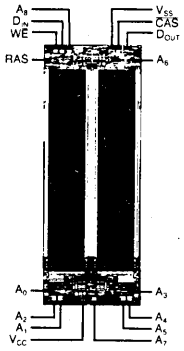
CD007080

LOGIC SYMBOL



LS001812

METALLIZATION AND PAD LAYOUT

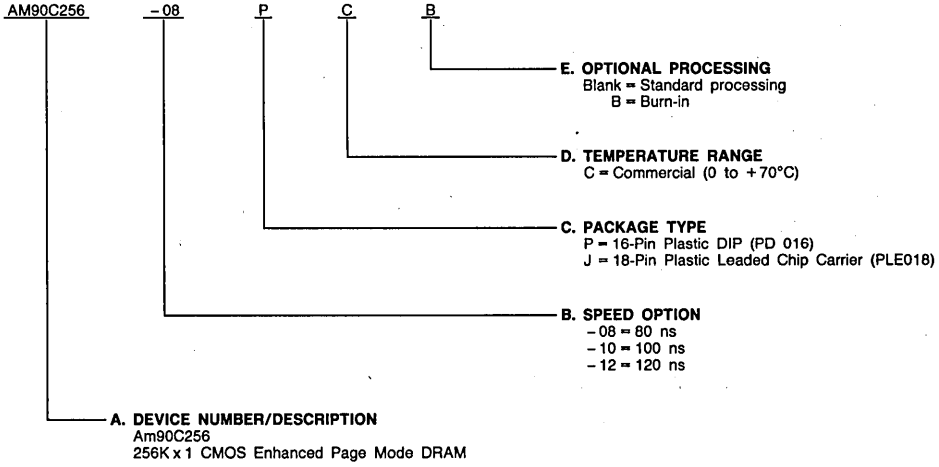


4

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

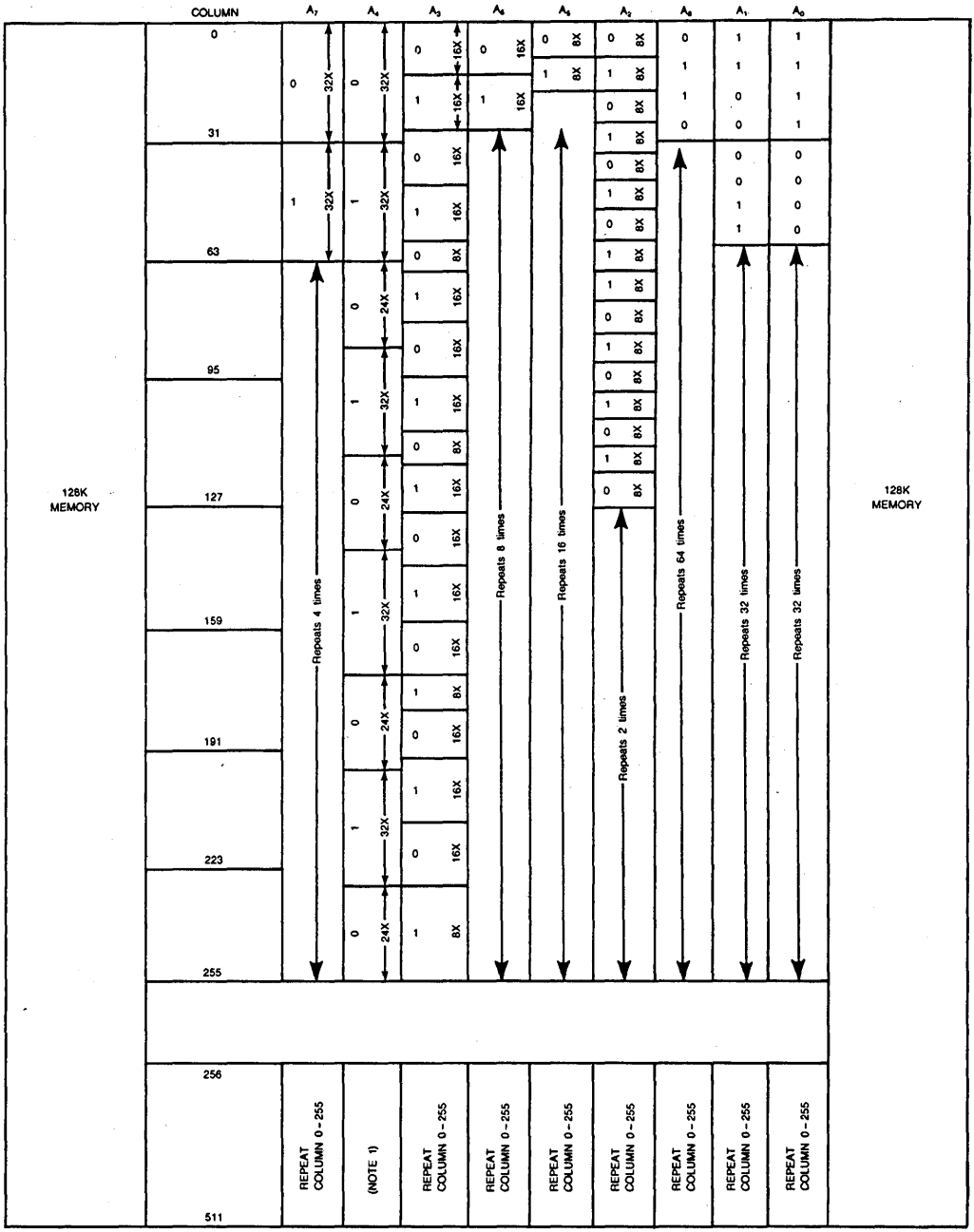


Valid Combinations	
AM90C256-08	PC, PCB, JC, JCB
AM90C256-10	
AM90C256-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

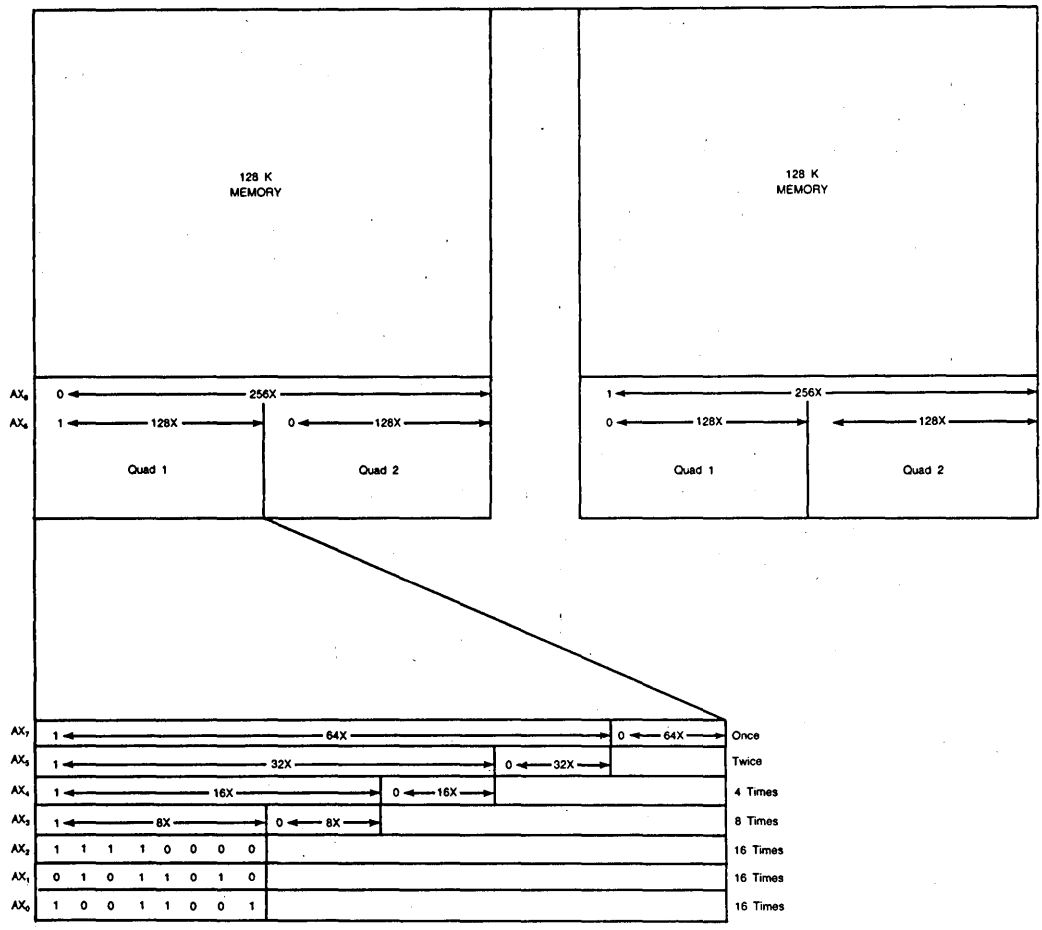
COLUMN ADDRESS TOPOLOGICAL BIT MAP



AF003960

Note: 1. Address A_4 from 256 to 511 is the inverse of address 0 to 255.

ROW ADDRESS TOPOLOGICAL BIT MAP



AF003970

Note: Quad 2 is a mirror image of AX_2 thru AX_7 in Quad 1. AX_0 and AX_1 are repeated in both quads.

PIN DESCRIPTION

$A_0 - A_8$ Nine multiplexed address inputs, initially provides nine row address inputs and then nine column address inputs, all within one normal cycle. The nine row address inputs (meeting the set-up and hold times, t_{ASR} and t_{RAH}) are latched in by $\overline{RAS}$ ↓. The nine column address inputs (meeting the set-up and hold times, t_{ASC}, t_{CAH} and t_{AR}) are latched in by $\overline{CAS}$ ↓. The combined row and column address inputs (18 total) will select one of 262,144 memory bits for Read, Write or Read-Modify-Write operation.

D_{IN} The Data Input (meeting set-up and hold times, t_{DS} and t_{DH}) is latched in by either $\overline{WE}$ ↓ or $\overline{CAS}$ ↓, whichever comes later, while $\overline{RAS}$ is LOW.

$\overline{RAS}$ The Row Address Strobe control clock. $\overline{RAS}$ ↓ latches the row address on $A_0 - A_8$ and activates a memory cycle and precharges the memory's dynamic circuits. Memory cycle time, as defined by the $\overline{RAS}$ clock, has a very large operating range. However, $\overline{RAS}$ LOW pulse width (t_{RAS}) and $\overline{RAS}$ HIGH pulse width (t_{RP}) must satisfy the specified minimum and maximum values in order to maintain continuous memory operation and data retention. $\overline{RAS}$ alone controls memory refresh function.

$\overline{CAS}$ The Column Address Strobe control clock. With $\overline{RAS}$ LOW, $\overline{CAS}$ ↓ latches the column address and activates the memory input and output operations. With $\overline{WE}$ LOW, $\overline{CAS}$ controls the input timing; with $\overline{WE}$ HIGH, $\overline{CAS}$ controls the timing of valid output. $\overline{CAS}$ HIGH turns off D_{OUT} (D_{OUT} = high impedance). In Page Mode, $\overline{CAS}$ and t_{CAA} define the Page Mode Cycle time. In Enhanced Page Mode operation, $\overline{CAS}$ is cycled while maintaining $\overline{RAS}$ LOW. The column address buffer acts as a flow-through latch while $\overline{CAS}$ is HIGH.

$\overline{WE}$ The Write Enable control clock. $\overline{WE}$ timing, relative to $\overline{CAS}$ and $\overline{RAS}$, will define one of three memory cycles. $\overline{RAS}$ and $\overline{CAS}$, both LOW, and 1) $\overline{WE}$ HIGH, will define a Read Cycle; 2) $\overline{WE}$ LOW (meeting the set-up and hold time t_{WCS}), will define an Early Write Cycle; 3) $\overline{WE}$, first HIGH and then LOW (meeting the t_{CWD} delay time), will define a Read-Write/Read-Modify-Write Cycle.

D_{OUT} The three-state output. D_{OUT} is controlled by $\overline{CAS}$. Valid output appears on D_{OUT} in a Read Cycle after access time has elapsed (t_{CAC} or t_{RAC}, whichever applies). Last valid D_{OUT} remains valid as long as $\overline{CAS}$ is LOW. D_{OUT} can be turned off only with $\overline{CAS}$.

FUNCTIONAL DESCRIPTION

Device Initialization

An initial pause of 100 μs is required after V_{CC} power-up. This time delay is needed for the on-chip substrate-bias generator to pump enough negative charge into the substrate to establish the operating back-bias voltage. This is followed by a wake-up sequence of eight $\overline{RAS}$ cycles to initialize the internal dynamic circuits. If the device remains in standby mode for more than 4 ms while V_{CC} is on, the wake-up sequence of any eight $\overline{RAS}$ cycles will be necessary prior to normal operation. On-chip circuits prevent current surges during initial system power-up.

Operating Cycles

Memory Cycle

The Memory Cycle begins with $\overline{RAS}$ being pulled LOW. Once started, the Memory Cycle must not be aborted prior to fulfilling the minimum t_{RAS} timing specification to ensure data integrity. Furthermore, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP}, has elapsed.

Read Cycle

A Read Cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal HIGH during the $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data-out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ LOW during a $\overline{RAS}$ operation. The column address is latched in by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$-controlled or $\overline{CAS}$-controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ LOW transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-Controlled Write Cycle (the leading edge of $\overline{WE}$ occurs prior to, or coincident with, the $\overline{CAS}$ LOW transition), the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state.

The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the Write Cycle.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses ($A_0 - A_7$) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only Cycle will perform refresh.

Data Output

The Am90C256 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ HIGH state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Enhanced Page Mode Operation

Enhanced Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ LOW while successive $\overline{CAS}$ cycles are performed, retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is HIGH. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the addresses into the column address buffer and acts as an output enable.

During this operation, Read, Write, Read-Modify-Write, or Read-Write-Read Cycles are possible at random or sequential addresses within a row. Following the entry cycle into Enhanced Page Mode operation, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to, or coincident with, the rising edge of $\overline{CAS}$, then the access time is

determined by the rising edge of $\overline{CAS}$ specified by t_{CAP}, as shown in Figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Enhanced Page Mode operation provides a sustained data rate over 18 MHz for applications that require high data rate such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511\ t_{PC}}$$

Read-Modify-Write And Read-Write Cycles

As the name implies, both a Read and a Write Cycle are accomplished at the same cell location during a single access. The Read-Modify-Write Cycle is similar to the late Write Cycle discussed above.

For the Read-Modify-Write Cycle, a normal Read Cycle is initiated with the $\overline{WE}$ clock HIGH. After the data is read, $\overline{WE}$ is transitioned to LOW and D_{IN} is set up and held with respect to the active edge of $\overline{WE}$. This cycle assumes a zero modify time between read and write.

Another variation of the Read-Modify-Write Cycle is the Read-Write Cycle, in which the two parameters (t_{RWD} and t_{CWD}) play an important role. A Read-Write Cycle starts as a normal Read Cycle with the $\overline{WE}$ clock being transitioned at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before D_{OUT} occurs. In this case, D_{IN} is set up with respect to the $\overline{WE}$ clock active edge.

TABLE 1. Am90C256 DATA OUTPUT OPERATION FOR VARIOUS TYPES OF CYCLES

Cycle	Data Out of State
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{CAS}$ Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{WE}$ Controlled)	Data from Addressed Memory Cell and Active, Not Valid
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Only Cycle	High Impedance

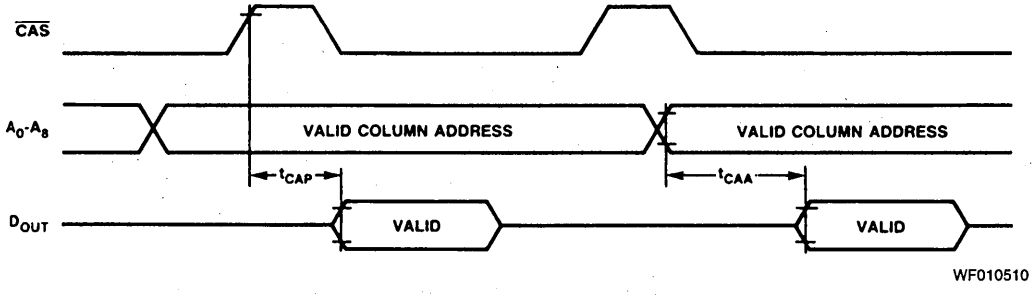


Figure 1. Enhanced Page Mode Access Time Determination

APPLICATIONS

Device Description

The Am90C256 is a state-of-the-art, high-performance CMOS 256K DRAM which combines the fastest DRAM speed available (80 ns access time) with low power (standby current < 4 mA). It is designed to operate with a single +5-V power supply, and all input/output voltage levels are TTL-compatible, making the Am90C256 easy to integrate into a wide range of systems. The Am90C256 features the static column access method which is ideal for high data bandwidth applications. Eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the Am90C256. Nine row address bits are established on the input pins ($A_0 - A_8$) and latched with $\overline{RAS}$. After a minimum t_{RAH} timing specification has been fulfilled, the column address flows through the internal address buffer and is latched by a column address strobe.

The Am90C256 improves system reliability by means of the following on-chip features:

- Allows V_{CC} power-up with floating input levels without causing excess I_{CC} surges (see Device Initialization).
- Tolerates real-time V_{CC} fluctuation between 4.5 V and 5.5 V while memory chip is in operation.
- Accepts input voltage transition overshoot (V_{CC} + 1 V) and undershoot (−1 V).
- Fabricated with a CMOS technology that is optimized to provide very high device latch-up voltage in excess of 10 volts.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −10 to +80°C
Voltage on Any Pin Relative to V_{SS} (Except V_{CC}) ..... −2 to +7.5 V
Voltage on V_{CC} Supply Relative to V_{SS} ..... −1 to +7.5 V
Short Circuit Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Input High Voltage (V_{IH}) ..... 2.4 V to V_{CC} +1.0 V
Input Low Voltage (V_{IL}) ..... −1.0 V to 0.8 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Part No.	Min.	Max.	Unit
V_{OH}	Output Levels	Output HIGH Voltage (I_{OH} = −5.0 mA)		2.4		V
V_{OL}		Output LOW Voltage (I_{OL} = 4.2 mA)			0.4	
V_{IH}	Input HIGH Voltage	0°C ≤ T_A ≤ +70°C		2.4	V_{CC} + 1.0 V	V
V_{IL}	Input LOW Voltage			−1.0	0.8	
$I_{I(L)}$	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.0 V, V_{SS} = 0 V All Other Pins Not Under Test = 0 V		−10	10	µA
$I_{O(L)}$	Output Leakage Current	Data-Out Disabled, 0 V < V_{OUT} < 5.5 V		−10	10	µA
I_{CC1}	Operating Current Average Power Supply Current	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min.	Am90C256-08		85	mA
			Am90C256-10		70	
			Am90C256-12		65	
I_{CC2}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} (TTL Level)			4	mA
I_{CC3}	V_{CC} Supply Current $\overline{RAS}$-Only Refresh	t_{RC} = Min.	Am90C256-08		85	mA
			Am90C256-10		70	
			Am90C256-12		65	
I_{CC4}	V_{CC} Supply Current Enhanced Page Mode	t_{PC} = Min.	Am90C256-08		85	mA
			Am90C256-10		70	
			Am90C256-12		65	
I_{CC5}	V_{CC} Supply Current Standby, Output Enabled	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}			6	mA

Notes: 1. All voltages referenced to V_{SS}.
2. Specified I_{CC} (Max.) is measured with output open.
3. Test conditions apply for DC Characteristics only.

CAPACITANCE*

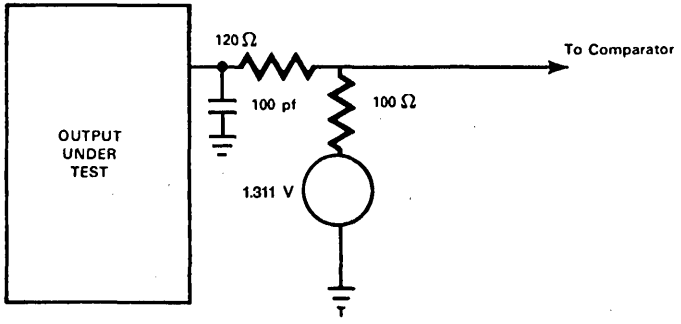
(T_A = +25°C, V_{CC} = 5 V, f = 1.0 MHz)

Symbol	Parameter	Max.	Units
C_{IN1}	Input Capacitance A_0 to A_8, D_{IN}	5	pF
C_{IN2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF
C_{OUT}	Output Capacitance D_{OUT}	6	pF

*Measured with a Booton Meter or calculated from the equation C = I∆t/∆V.

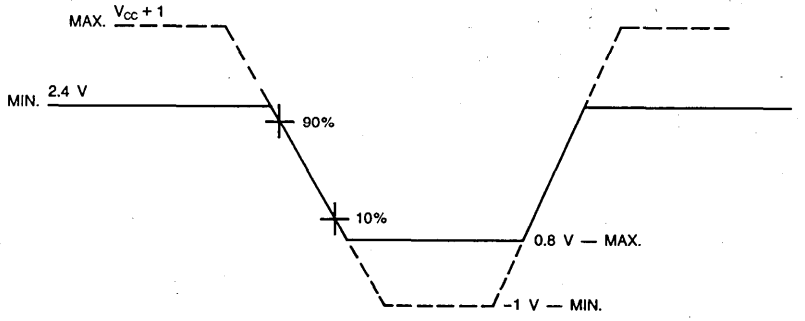
4

SWITCHING TEST CIRCUIT



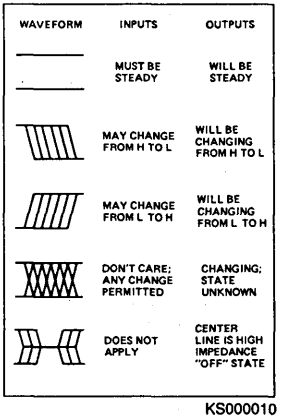
TC002323

SWITCHING TEST WAVEFORM



WF010380

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90C256-08		Am90C256-10		Am90C256-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ/WRITE/READ-MODIFY-WRITE AND REFRESH CYCLES									
1	t_{RAS}	$\overline{RAS}$ Pulse Width	80	75,000	100	75,000	120	75,000	ns
2	t_{RC}	Random R/W Cycle Time	130		170		200		ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		60		70		ns
4	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		ns
5	t_{CAS}	$\overline{CAS}$ Pulse Width	20	75,000	25	75,000	30	75,000	ns
6	t_{WRP}	Write-to-$\overline{RAS}$ Precharge Time (Note 10)	–		–		–		ns
7	t_{RWH}	$\overline{RAS}$-to-Write Hold Time (Note 10)	–		–		–		ns
8	t_{ASR}	Row Address Setup Time	3		0		0		ns
9	t_{RAH}	Row Address Hold Time	10		20		20		ns
10	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns
11	t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	0		10		10		ns
12	t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time (Note 1)	20	60	30	75	30	90	ns
13	t_{ASC}	Column Address Setup Time	0		0		0		ns
14	t_{CAH}	Column Address Hold Time	12		15		20		ns
15	t_{AR}	Column Address Hold Time from $\overline{RAS}$	32		45		60		ns
16	t_{REF}	Time Between Refresh		4		4		4	ms
17	t_T	Transition Time (Rise and Fall) (Note 2)	3	25	3	25	3	25	ns
18	t_{ON}	Output Buffer Turn-On Delay	0		0		0		ns
19	t_{OFF}	Output Buffer Turn-Off Delay		20		20		25	ns
READ CYCLE									
20	t_{RAC}	Access Time From $\overline{RAS}$ (Notes 3 & 5)		80		100		120	ns
21	t_{CAC}	Access Time From $\overline{CAS}$ (Notes 4 & 5)		20		25		25	ns
22	t_{CAA}	Access Time from Column Address (Note 5)		35		40		55	ns
23	t_{RSH} (R)	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		30		ns
24	t_{RCS}	Read Command Setup Time	0		0		0		ns
25	t_{CAR}	Column Address-to-$\overline{RAS}$ Setup Time	35		40		55		ns
26	t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$ (Note 6)	5		5		5		ns
27	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$ (Note 6)	10		10		10		ns
WRITE CYCLE									
28	t_{RSH} (W)	$\overline{RAS}$ Hold Time (Write Cycle)	20		25		30		ns
29	t_{RWL}	Write Command to $\overline{RAS}$ Setup Time	20		25		30		ns
30	t_{CWL}	Write Command to $\overline{CAS}$ Setup Time	20		25		30		ns
31	t_{WP}	Write Command Pulse Width	12		15		20		ns
32	t_{WCS}	Write Command Setup Time (Note 7)	0		0		0		ns
33	t_{WCH}	Write Command Hold Time	15		20		25		ns
34	t_{DS}	Data-In Setup Time	0		0		0		ns
35	t_{DH}	Data-In Hold Time	12		20		25		ns

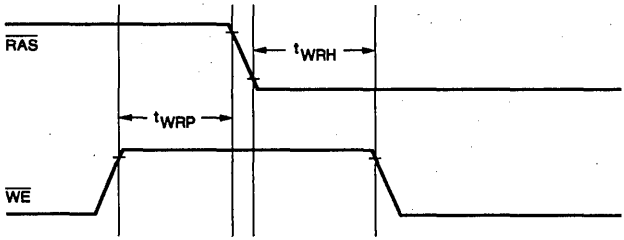
Notes: See next page for notes.

SWITCHING CHARACTERISTICS (Cont'd.)

(T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90C256-08		Am90C256-10		Am90C256-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ-MODIFY-WRITE (RMW) CYCLE									
36	t_{RWC}	RMW Cycle Time	155		200		235		ns
37	t_{RRW}	RMW $\overline{RAS}$ Pulse Width	105	75,000	130	75,000	155	75,000	ns
38	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	45	75,000	55	75,000	65	75,000	ns
39	t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time (Note 7)	80		100		120		ns
40	t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time (Note 7)	20		25		30		ns
41	t_{AWD}	Column Address-to-$\overline{WE}$ Delay Time (Note 7)	35		40		50		ns
ENHANCED PAGE MODE CYCLE									
42	t_{CAP}	Access Time from Column Precharge Time (Note 8)		40		45		55	ns
43	t_{PC}	Enhanced Page Mode Read/Write Cycle Time (Note 8)	45		50		60		ns
44	t_{PCM}	Enhanced Page Mode RMW Cycle Time	65		75		95		ns

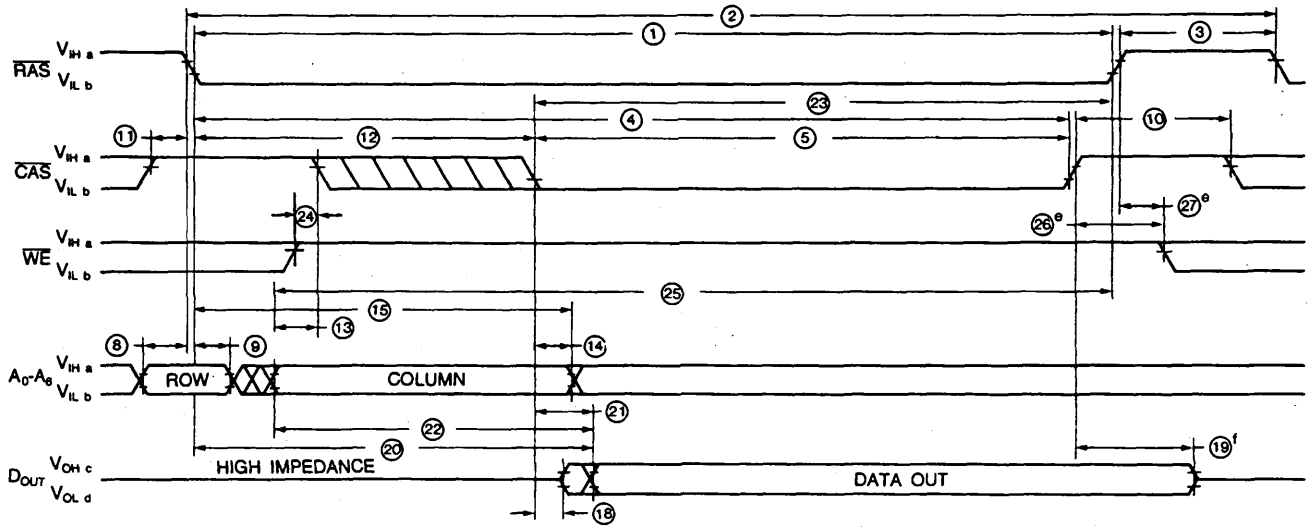
Notes:
1. t_{RCD} (Max.) is specified for reference only.
2. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
3. Assumes that $t_{RCD} \leq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), then t_{RAC} will increase by an amount that t_{RCD} exceeds t_{RCD} (Max.).
4. Assumes $t_{RCD} \geq t_{RCD}$ (Max.).
5. If $t_{ASC} < (t_{CAA}$ (Max.) $- t_{CAC}$ (Max.) $- t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
6. Either t_{RCH} or t_{RRH} must be satisfied.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is a $\overline{CAS}$-controlled write cycle (early write cycle) and D_{OUT} pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a RMW cycle and the data-out will contain the data read from the selected address. If any of these conditions are not satisfied, the condition of data-out is indeterminate.
8. Access time and cycle time are determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.
9. All AC parameters are measured with a load equivalent to two TTL loads and 100-pF capacitive load.
10. Timing parameters t_{WRP} and t_{RWH} (see below), referenced to $\overline{RAS}$, are redundant on the Am90C256, and hence, not specified in the data sheet.



WF010790

SWITCHING WAVEFORMS

READ CYCLE

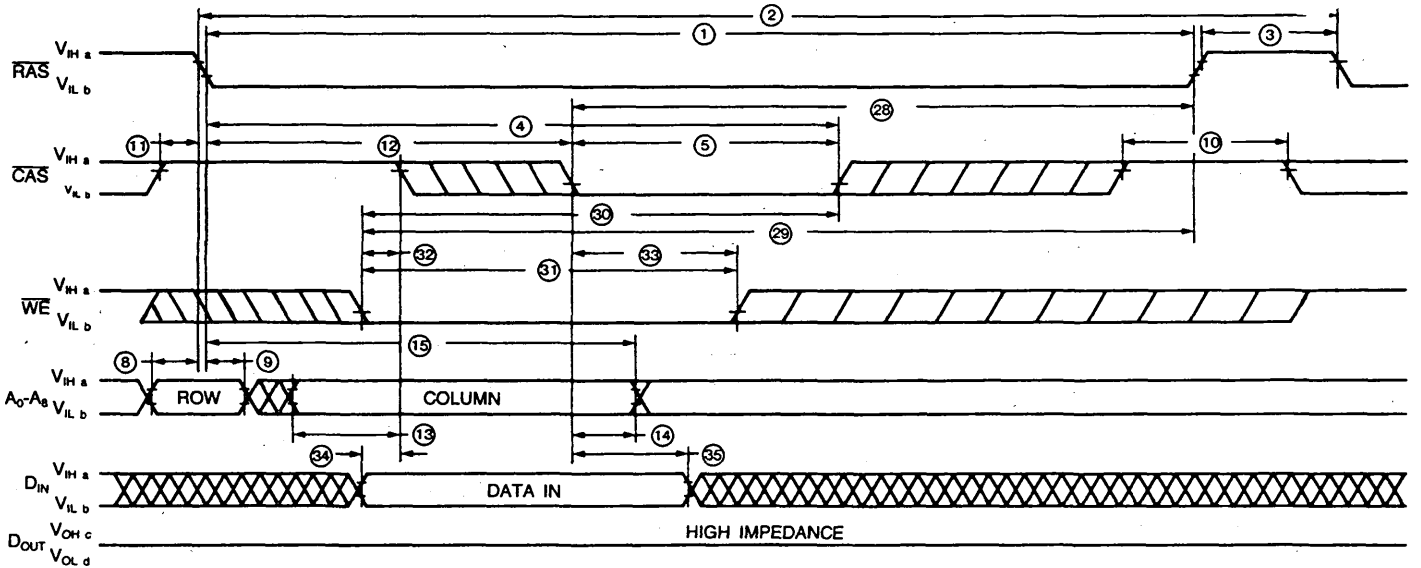


WF010391

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Either t_{RCH} or t_{RRH} must be satisfied.
f. t_{OFF} is measured to $|I_{OUT}| \leq |I_{O(L)}|$.

SWITCHING WAVEFORMS (Cont'd.)

WRITE CYCLE ($\overline{CAS}$ Controlled)

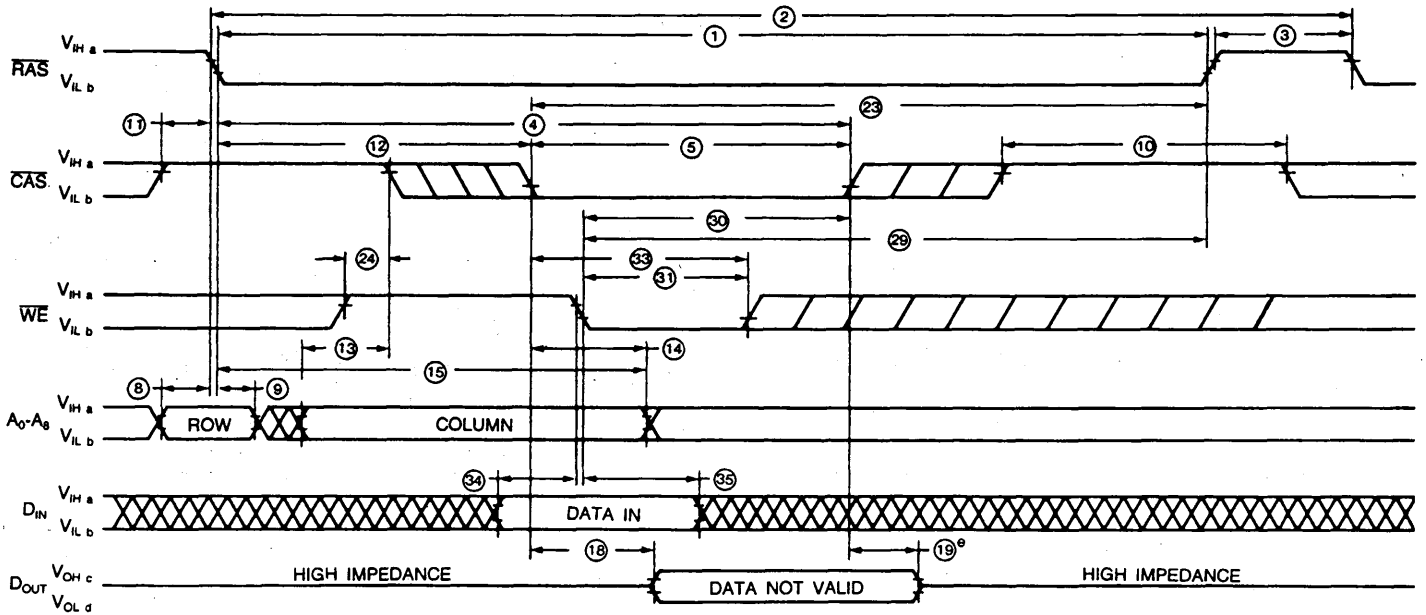


WF010401

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition, $\overline{CAS}$ latches column address and data-in.

SWITCHING WAVEFORMS (Cont'd.)

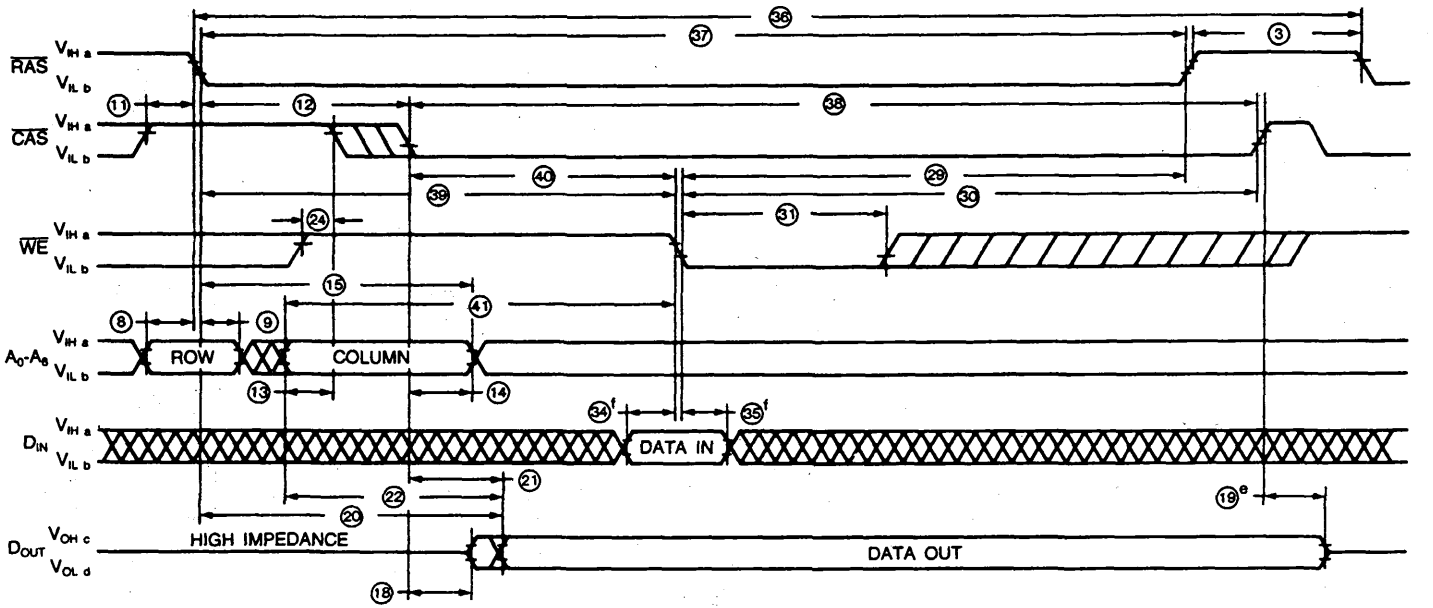
WRITE CYCLE ($\overline{WE}$ Controlled)



Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{O(L)}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

SWITCHING WAVEFORMS (Cont'd.)

READ/MODIFY/WRITE CYCLE

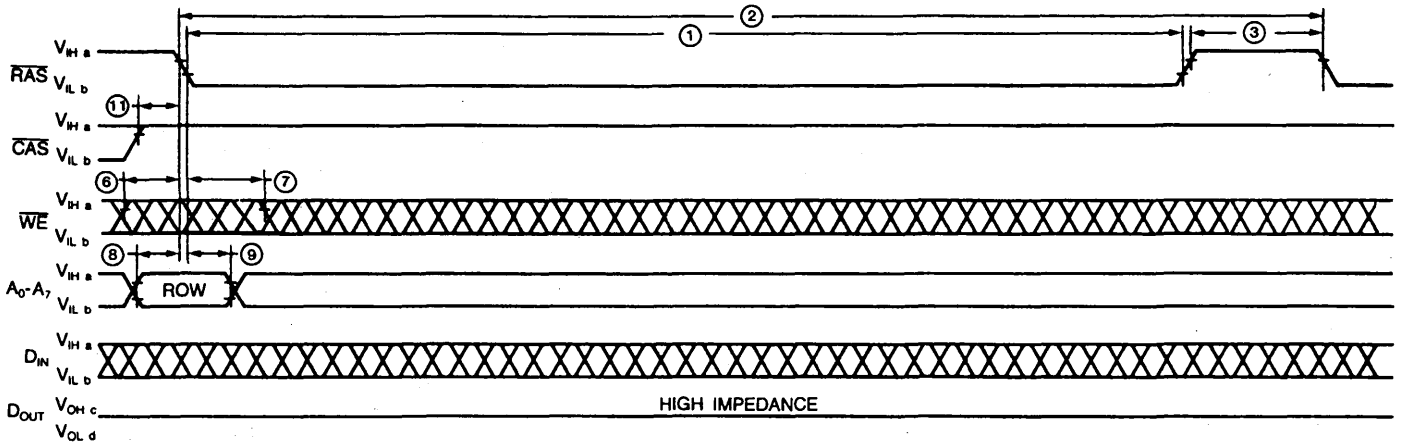


WF010421

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT} \leq |I_{O(L)}|$.
f. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

SWITCHING WAVEFORMS (Cont'd.)

$\overline{RAS}$-ONLY REFRESH CYCLE

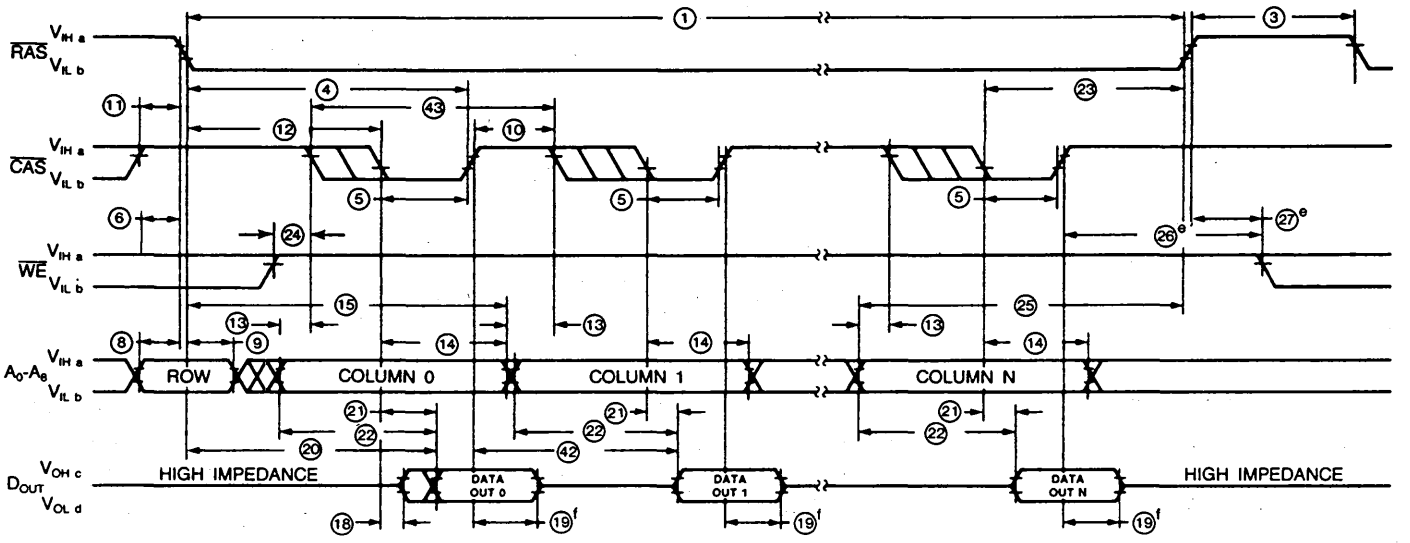


WF010431

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

SWITCHING WAVEFORMS (Cont'd.)

ENHANCED PAGE MODE READ CYCLE

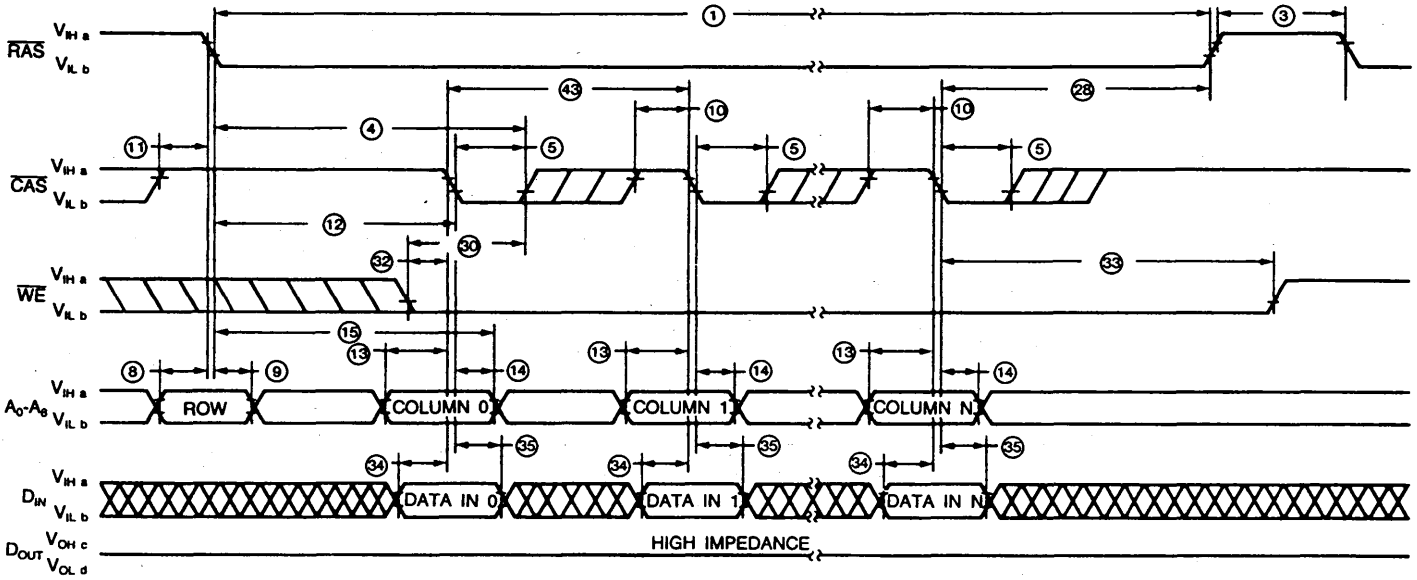


WF010441

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. either t_{RCH} or t_{RRH} must be satisfied.
f. t_{OFF} is measured to $I_{OUT} \leq |I_{O(L)}|$.

SWITCHING WAVEFORMS (Cont'd.)

ENHANCED PAGE MODE WRITE CYCLE ($\overline{CAS}$ Controlled)

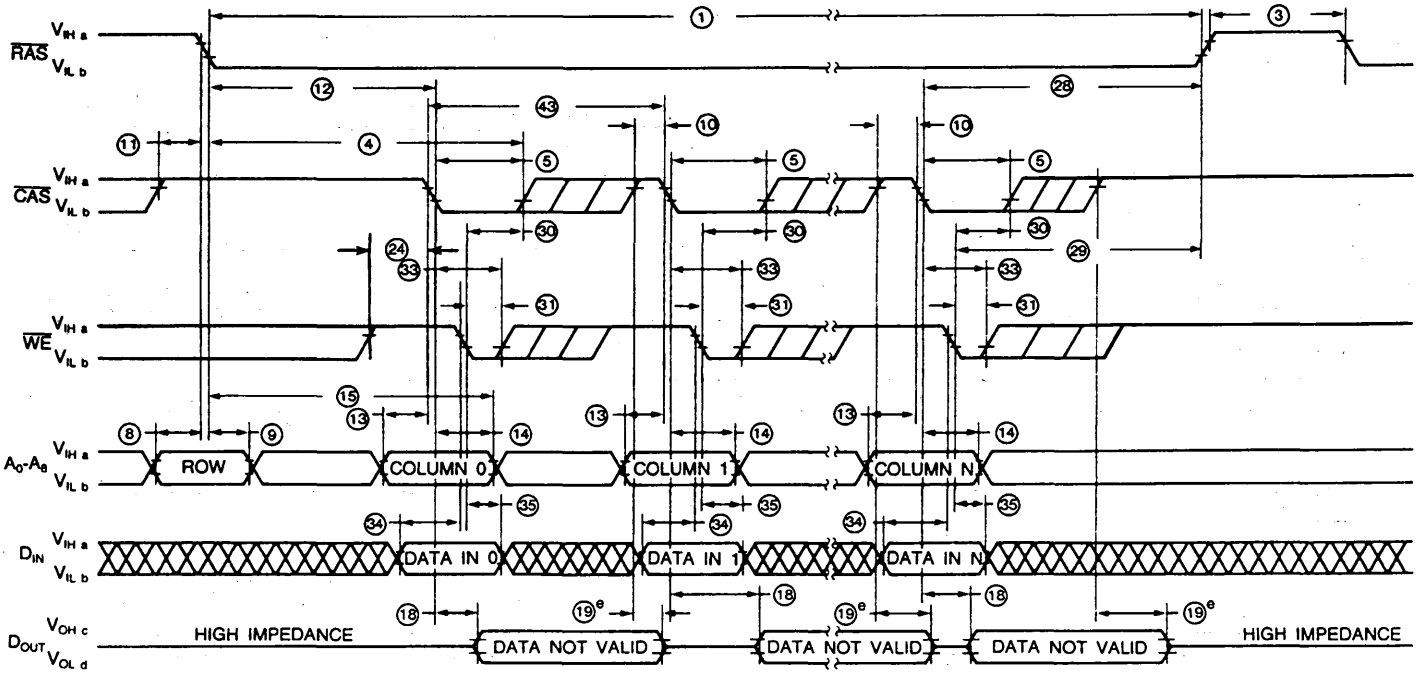


WF010461

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column addresses and data-in.

SWITCHING WAVEFORMS (Cont'd.)

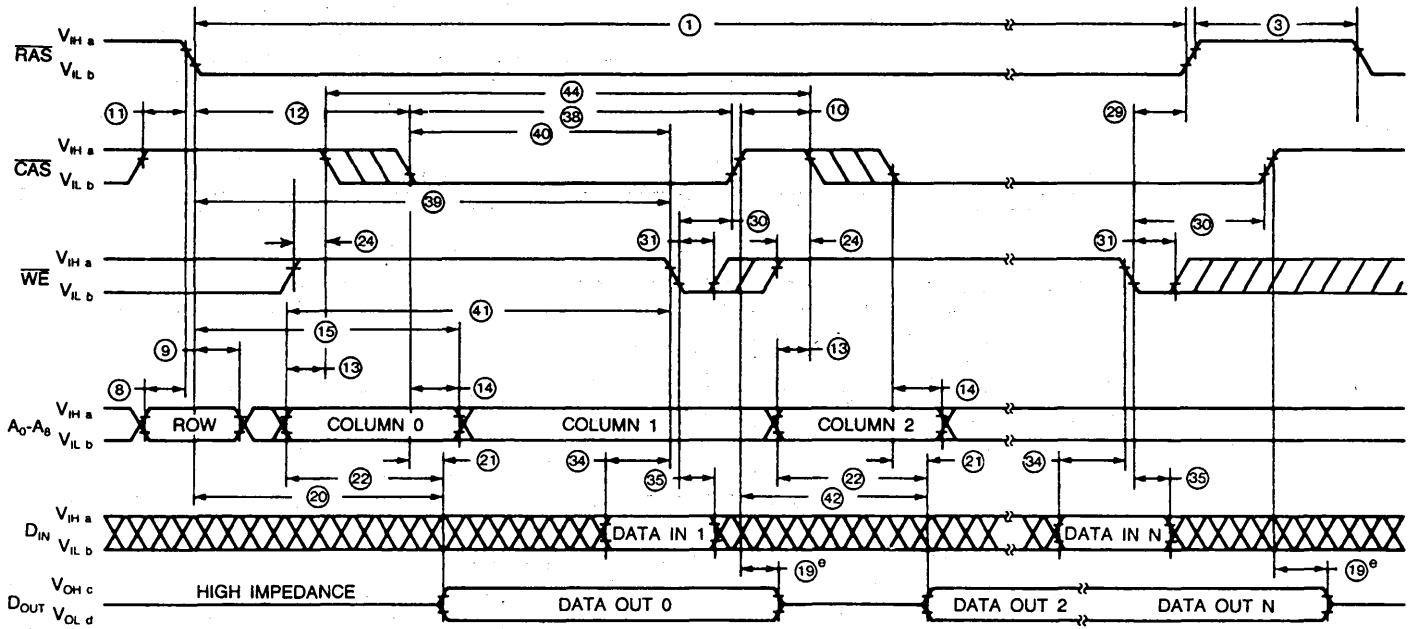
ENHANCED PAGE MODE WRITE CYCLE ($\overline{WE}$ CONTROLLED)



Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{O(L)}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

SWITCHING WAVEFORMS (Cont'd.)

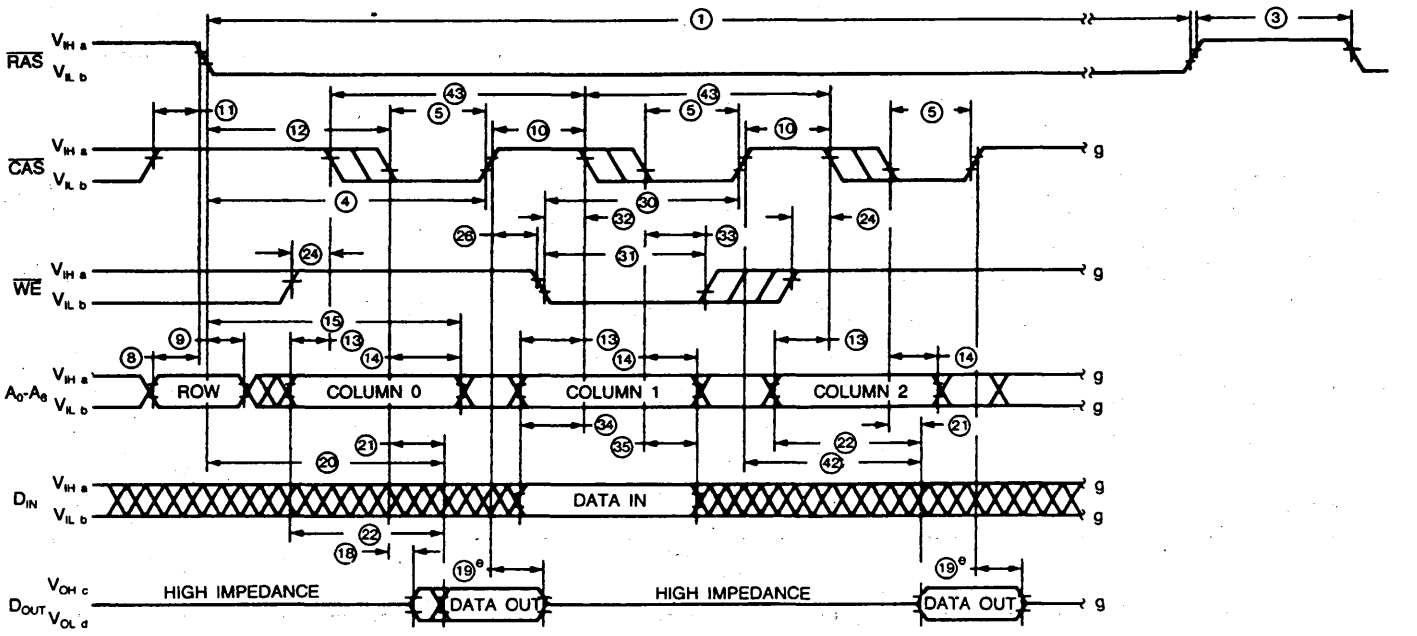
ENHANCED PAGE MODE READ-MODIFY-WRITE CYCLE



Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OEF} is measured to $|I_{OUT}| \leq |I_{O(L)}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

SWITCHING WAVEFORMS (Cont'd.)

ENHANCED PAGE MODE READ-WRITE-READ ... CYCLE ($\overline{CAS}$ CONTROLLED)

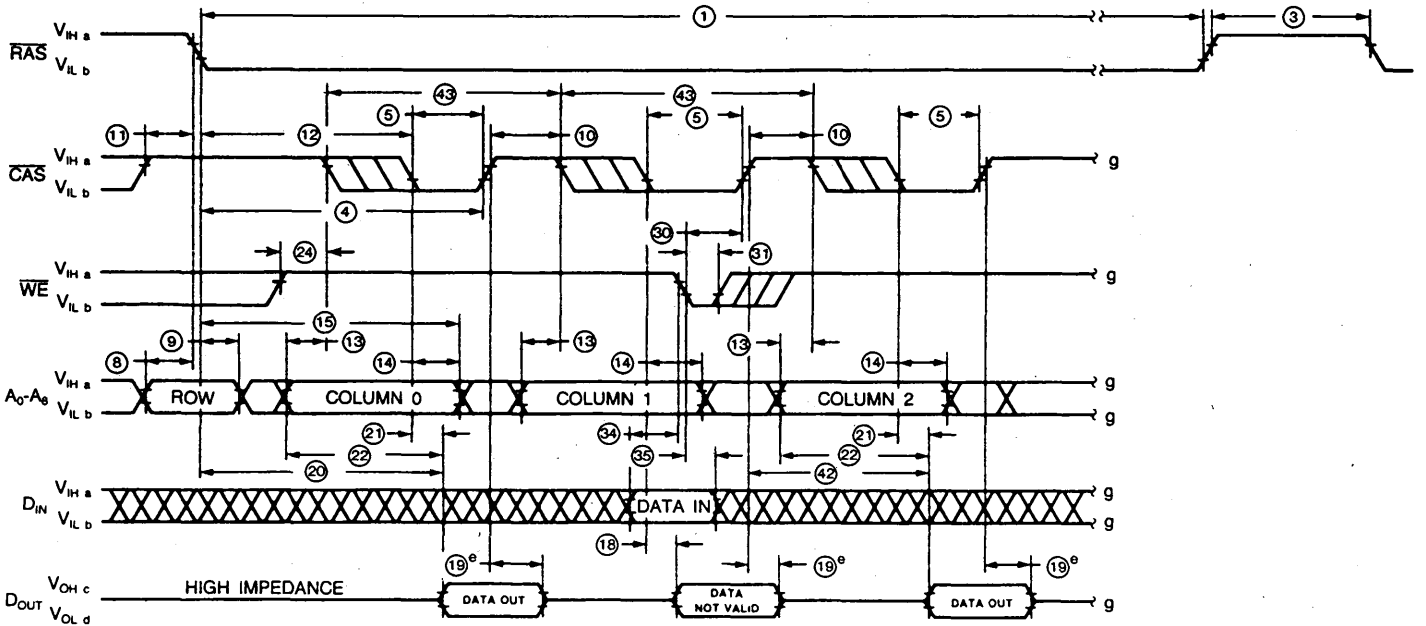


WF010491

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{O(L)}|$.
f. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column address and data-in.
g. The cycle can be terminated either by a read or a write operation followed by a $\overline{RAS}$ high transition.

SWITCHING WAVEFORMS (Cont'd.)

ENHANCED PAGE MODE READ-WRITE-READ ... CYCLE ($\overline{WE}$ CONTROLLED)



WF010501

Notes: a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{O(L)}|$.
f. $\overline{CAS}$ is low prior to $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches data-in.
g. The cycle can be terminated either by a read or a write operation followed by a $\overline{RAS}$ high transition.

Am90CL256

Low-Power 256K x 1 CMOS Enhanced Page Mode DRAM

OVERVIEW

The 256K x 1 CMOS Low-Power ('L') DRAM versions share common functional descriptions, DC and AC characteristics with the corresponding standard CMOS (non-'L') versions. The only additions to these sections are:

DISTINCTIVE CHARACTERISTICS

- Extended refresh period
  — 32 ms (Max.) during standby
- Low data retention current
  — 230 μA (Max.)
- Low-power dissipation
  — 0.55 mW (Max.)

ORDERING INFORMATION

The Ordering Information for the Low-Power DRAM versions are the same as for the Standard CMOS DRAMs, with the exception of an 'L' inserted within the device number to denote 'Low-Power.' For example, the Am90CL255 is = a 256K x 1 CMOS "Low-Power" Nibble Mode DRAM. All temperature ranges, speed and package options remain the same as those listed in Ordering Information sections for the respective Standard CMOS DRAMs.

DC CHARACTERISTICS

The low-power version DRAMs are screened for one additional parameter, viz, CMOS standby current. All other DC characteristics remain the same for both families.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{CC6}	V_{CC} Supply Current CMOS Standby	$\overline{RAS} \geq V_{CC} - 0.5$ V and $\overline{CAS}$ at V_{IH}, all other inputs and outputs $\geq V_{SS}$	Am90CL256		0.1	mA

The Am90CL256-15 is screened for I_{CC1} = 60 mA, I_{CC3} = 60 mA, and I_{CC4} = 60 mA

AC CHARACTERISTICS

AC Characteristics remain unchanged on the low-power 100 ns and 120 ns versions. The AC characteristics corresponding to the 150 ns speed are on the following page.

FUNCTIONAL DESCRIPTION

The Functional Descriptions for low-power versions are the same as the corresponding standard versions. The low-power devices, however, support Extended Refresh cycles described below:

Extended Refresh Cycle

All low-power versions extend the Refresh Cycle period to 32 ms for $\overline{RAS}$-Only Refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA for data retention. The low-standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})\ (I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{T_{RI}}$$

where t_{RC} = Refresh Cycle Time

and t_{RI} = Refresh Interval Time or $t_{REF}/256$

Before entering or leaving an Extended Refresh period, the entire array must be refreshed at the normal interval of 4 ms. This can be accomplished by either a burst or distributed refresh.

Publication #	Rev.	Amendment
07412	A	/0

Issue Date: May 1986

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL256-15 Min.	Am90CL256-15 Max.	Units
READ/WRITE/READ-MODIFY-WRITE AND REFRESH CYCLES					
1	t_{RAS}	$\overline{RAS}$ Pulse Width	150	75,000	ns
2	t_{RC}	Random R/W Cycle Time	245		ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	85		ns
4	t_{CSH}	$\overline{CAS}$ Hold Time	150		ns
5	t_{CAS}	$\overline{CAS}$ Pulse Width	35	75,000	ns
6	t_{WRP}	Write-to-$\overline{RAS}$ Precharge Time (Note 10)	–		ns
7	t_{RWH}	$\overline{RAS}$-to-Write Hold Time (Note 10)	–		ns
8	t_{ASR}	Row Address Setup Time	0		ns
9	t_{RAH}	Row Address Hold Time	20		ns
10	t_{CP}	$\overline{CAS}$ Precharge Time	10		ns
11	t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	10		ns
12	t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time (Note 1)	30	120	ns
13	t_{ASC}	Column Address Setup Time	0		ns
14	t_{CAH}	Column Address Hold Time	20		ns
15	t_{AR}	Column Address Hold Time from $\overline{RAS}$	65		ns
16	t_{REF}	Time Between Refresh		4	ms
17	t_T	Transition Time (Rise and Fall) (Note 2)	1	25	ns
18	t_{ON}	Output Buffer Turn-On Delay	0		ns
19	t_{OFF}	Output Buffer Turn-Off Delay		25	ns
READ CYCLE					
20	t_{RAC}	Access Time From $\overline{RAS}$ (Notes 3 & 5)		150	ns
21	t_{CAC}	Access Time From $\overline{CAS}$ (Notes 4 & 5)		30	ns
22	t_{CAA}	Access Time from Column Address (Note 5)		70	ns
23	t_{RSH} (R)	$\overline{RAS}$ Hold Time (Read Cycle)	30		ns
24	t_{RCS}	Read Command Setup Time	0		ns
25	t_{CAR}	Column Address-to-$\overline{RAS}$ Setup Time	70		ns
26	t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$ (Note 6)	5		ns
27	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$ (Note 6)	10		ns
WRITE CYCLE					
28	t_{RSH} (W)	$\overline{RAS}$ Hold Time (Write Cycle)	30		ns
29	t_{RWL}	Write Command to $\overline{RAS}$ Setup Time	30		ns
30	t_{CWL}	Write Command to $\overline{CAS}$ Setup Time	30		ns
31	t_{WP}	Write Command Pulse Width	25		ns
32	t_{WCS}	Write Command Setup Time (Note 7)	0		ns
33	t_{WCH}	Write Command Hold Time	30		ns
34	t_{DS}	Data-In Setup Time	0		ns
35	t_{DH}	Data-In Hold Time	25		ns
READ-MODIFY-WRITE (RMW) CYCLE					
36	t_{RWC}	RMW Cycle Time	280		ns
37	t_{RRW}	RMW $\overline{RAS}$ Pulse Width	185	75,000	ns
38	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	65	75,000	ns
39	t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time (Note 7)	150		ns
40	t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time (Note 7)	30		ns
41	t_{AWD}	Column Address-to-$\overline{WE}$ Delay Time (Note 7)	65		ns

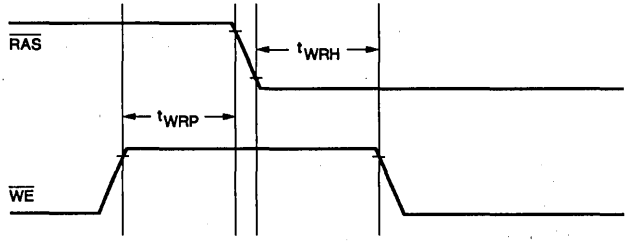
Notes: See next page for notes.

SWITCHING CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL256-15 Min.	Am90CL256-15 Max.	Units
ENHANCED PAGE MODE CYCLE					
42	t_{CAP}	Access Time from Column Precharge Time (Note 8)		70	ns
43	t_{PC}	Enhanced Page Mode Read/Write Cycle Time (Note 8)	75		ns
44	t_{PCM}	Enhanced Page Mode RMW Cycle Time	110		ns

Notes:
1. t_{RCD} (Max.) is specified for reference only.
2. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
3. Assumes that $t_{RCD} \leq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), then t_{RAC} will increase by an amount that t_{RCD} exceeds t_{RCD} (Max.).
4. Assumes $t_{RCD} \geq t_{RCD}$ (Max.).
5. If $t_{ASC} < (t_{CAA}$ (Max.) $- t_{CAC}$ (Max.) $- t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
6. Either t_{RCH} or t_{RRH} must be satisfied.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is a $\overline{CAS}$-controlled write cycle (early write cycle) and D_{OUT} pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a RMW cycle and the data-out will contain the data read from the selected address. If any of these conditions are not satisfied, the condition of data-out is indeterminate.
8. Access time and cycle time are determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.
9. All AC parameters are measured with a load equivalent to two TTL loads and 100-pF capacitive load.
10. Timing parameters t_{WRP} and t_{RWH} (see below), referenced to $\overline{RAS}$, are redundant on the Am90CL256, and hence, not specified in the data sheet.



WF010790

Am90C257

256K x 1 CMOS Static Column Dynamic RAM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Continuous data rate over 25 MHz
- Lower power dissipation via CMOS process – 20-mW standby mode
  – 300-mW operating mode
- High-speed operation – 80-ns $\overline{RAS}$ access times
  130-ns $\overline{RAS}$ cycle times
  – 35-ns $\overline{CAS}$ access times
- Fully TTL compatible
- Fast $\overline{CS}$ output control

GENERAL DESCRIPTION

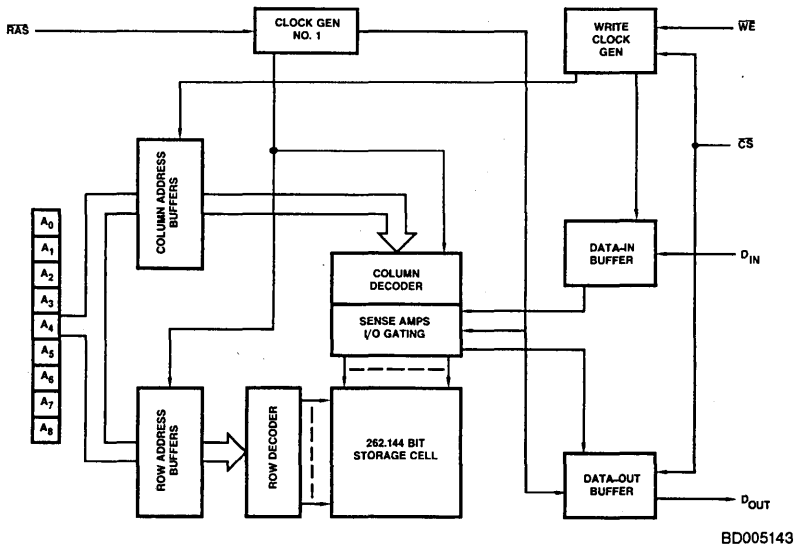
The Am90C257 is a fully decoded, CMOS static column random-access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high-performance applications such as main frame memory, graphics, buffer memory and peripheral storage digital signal processing, and battery-operated applications.

The device offers a new addressing technique – static column addressing which significantly reduces access times. In the static column technique, the $\overline{RAS}$ latches the row address, and column addresses are read directly from the address bus. By changing the column address, all 512 bits in a row can be randomly or sequentially accessed. A continuous data rate of over 18 million bits per second can be achieved by this method, which is ideal for high-data bandwidth applications.

The Am90C257 is fabricated using silicon gate CMOS process which permits significant improvements in speed-power characteristics.

The device operates on a single 5-V supply and is stable over a wide range. All inputs and outputs are TTL-compatible. The Am90C257 is housed in a standard 16-pin, 0.3-inch wide DIP.

BLOCK DIAGRAM



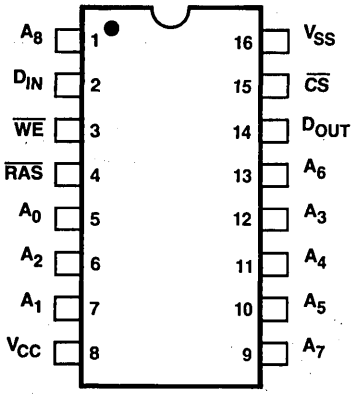
BD005143

PRODUCT SELECTOR GUIDE

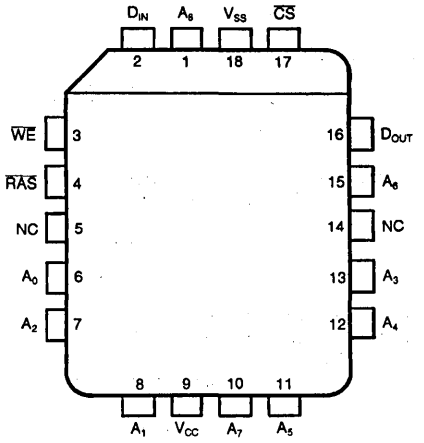
Part Number	Am90C257-08	Am90C257-10	Am90C257-12
$\overline{RAS}$ Access Time	80 ns	100 ns	120 ns
Temperature Range	Commercial	Commercial	Commercial

Publication # 07086 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View

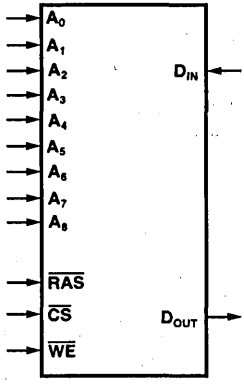


CD005844



CD007081

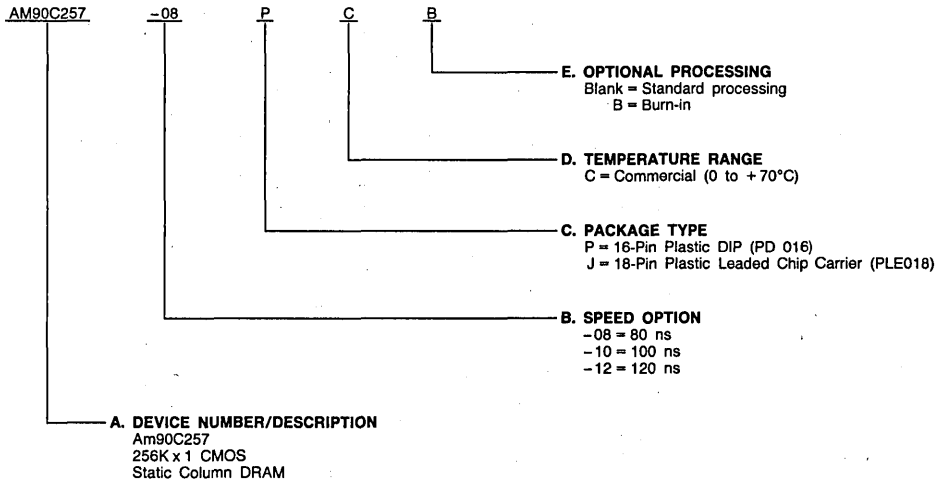
LOGIC SYMBOL



LS001813

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



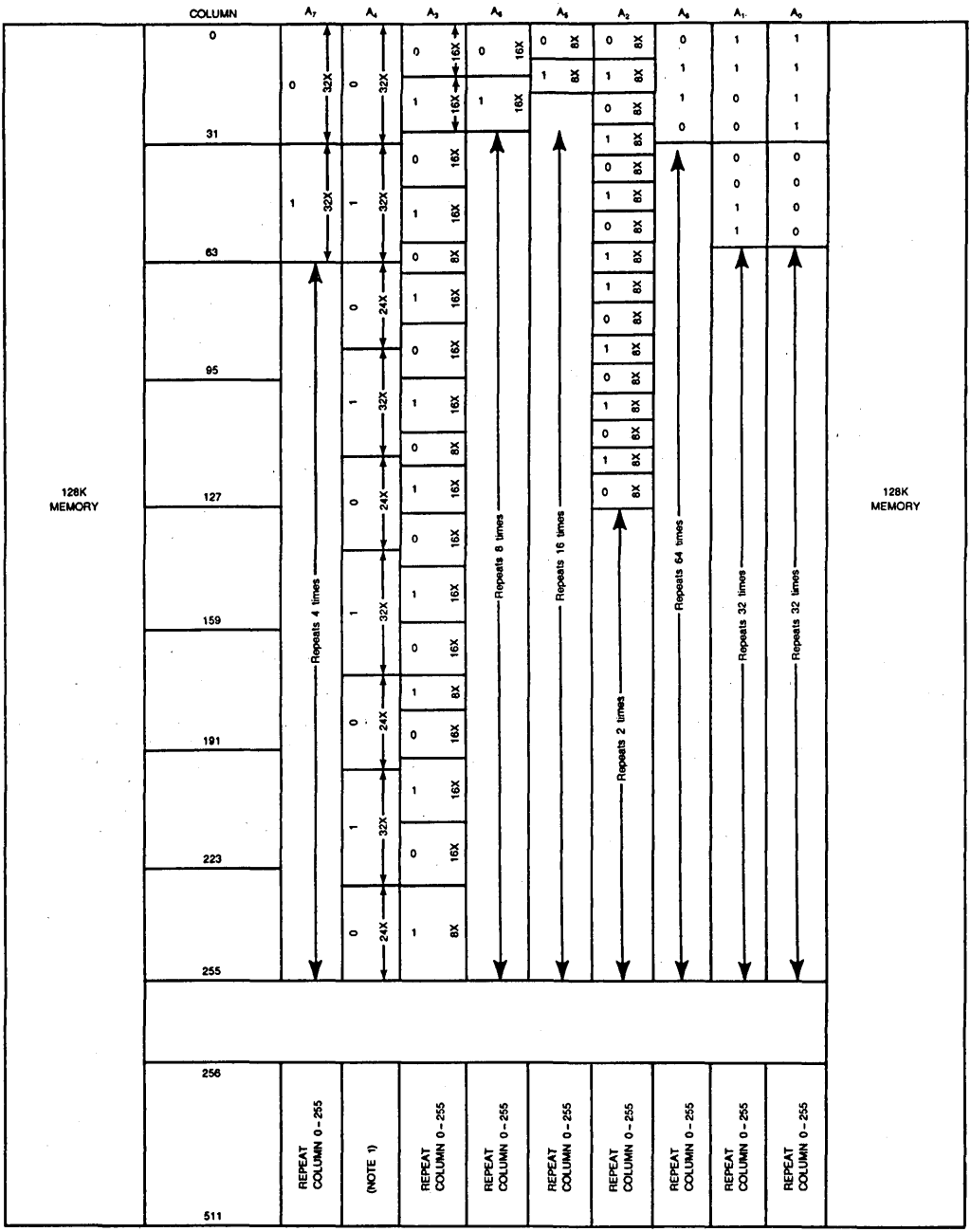
Valid Combinations	
AM90C257-08 AM90C257-10 AM90C257-12	PC, PCB, JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

4

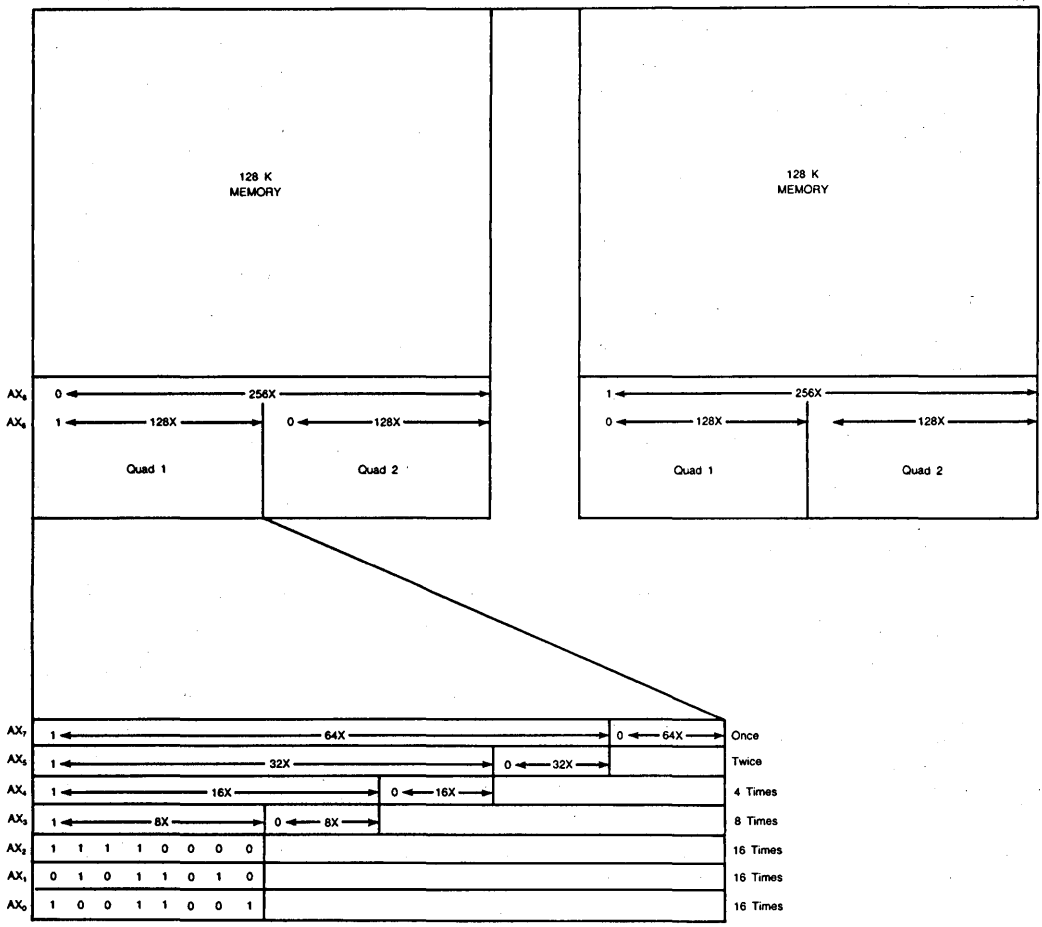
COLUMN ADDRESS TOPOLOGICAL BIT MAP



AF003960

Note: 1. Address A_4 from 256 to 511 is the inverse of address 0 to 255.

ROW ADDRESS TOPOLOGICAL BIT MAP



AF003970

Note: 1. Quad 2 is a mirror image of AX_2 thru AX_7 in Quad 1. AX_0 and AX_1 are repeated in both quads.

PIN DESCRIPTION

$A_0 - A_8$ Nine multiplexed address inputs, initially provides the nine row address inputs and then the nine column address inputs, all within one normal cycle. The nine row address inputs (meeting the set-up and hold times, t_{ASR} and t_{RAH}) are latched in by $\overline{RAS}$ ↓. The nine column address inputs flow through the column address buffer during a Read cycle. In a Write cycle the column addresses are latched by the latter of $\overline{WE}$ and $\overline{CS}$. The combined row and column address inputs (18 total) will select one of 262,144 memory bits for Read, Write or Read-Modify-Write operation.

D_{IN} The Data Input (meeting set-up and hold times, t_{DS} and t_{DH}) is latched in by either $\overline{WE}$ ↓ or $\overline{CS}$ ↓, whichever comes later, while $\overline{RAS}$ is LOW.

$\overline{RAS}$ The $\overline{\text{Row Address Strobe}}$ control clock. $\overline{RAS}$ ↓ latches the row address on $A_0 - A_8$ and activates a memory cycle and precharges the memory's dynamic circuits. Memory cycle time, as defined by the $\overline{RAS}$ clock, has a very large operating range. However, $\overline{RAS}$ LOW pulse width (t_{RAS}) and $\overline{RAS}$ HIGH pulse width (t_{RP}) must satisfy the specified minimum and maximum values in order to maintain continuous memory operation and data retention. $\overline{RAS}$ alone controls memory refresh function.

$\overline{CS}$ The $\overline{\text{Chip Select}}$ signal. With $\overline{RAS}$ LOW, $\overline{CS}$ ↓ enables the column address and activates the memory input and output operations. With $\overline{WE}$ LOW, $\overline{CS}$ controls the input timing; with $\overline{WE}$ HIGH, $\overline{CS}$ controls the timing of valid output. $\overline{CS}$ HIGH turns off D_{OUT} (D_{OUT} = high impedance). $\overline{CS}$ may be held LOW or pulsed.

$\overline{WE}$ The $\overline{\text{Write Enable}}$ control clock. $\overline{WE}$ timing, relative to $\overline{CS}$ and $\overline{RAS}$, will define one of three memory cycles. $\overline{RAS}$ and $\overline{CS}$, both LOW, and 1) $\overline{WE}$ HIGH, will define a Read Cycle; 2) $\overline{WE}$ LOW (meeting the set-up and hold time t_{WCS}), will define an Early Write Cycle; 3) $\overline{WE}$, first HIGH and then LOW (meeting the t_{CWD} delay time), will define a Read-Write/Read-Modify-Write Cycle. During a Write Cycle, $\overline{WE}$ ↓ strobes D_{IN} and nine column addresses.

D_{OUT} The three-state output. D_{OUT} is controlled primarily by $\overline{CS}$. Valid output appears on D_{OUT} in a Read Cycle after access time has elapsed (t_{CAC} or t_{RAC}, whichever applies). Last valid D_{OUT} remains valid as long as $\overline{CS}$ is LOW. D_{OUT} can be turned off with $\overline{CS}$. D_{OUT} is not controlled by $\overline{CS}$ during a memory cycle initialization.

FUNCTIONAL DESCRIPTION

Device Initialization

An initial pause of 100 μs is required after V_{CC} power-up. This time delay is needed for the on-chip substrate-bias generator to pump enough negative charge into the substrate to establish the operating back-bias voltage. This is followed by a wake-up sequence of eight $\overline{RAS}$ cycles to initialize the internal dynamic circuits. If the device remains in standby mode for more than 4 ms while V_{CC} is on, the wake-up sequence of any eight $\overline{RAS}$ cycles will be necessary prior to normal operation. On-chip circuits prevent current surges during initial system power-up.

Operating Cycles

Memory Cycle

The Memory Cycle begins with $\overline{RAS}$ being pulled LOW. Once started, the Memory Cycle must not be aborted prior to meeting the minimum t_{RAS} timing specification to ensure data integrity. Furthermore, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, has elapsed. D_{OUT} will always switch into the high impedance state when a memory cycle is initiated and remain in that state for a minimum period specified by t_{RLZ}, after which the output can change impedance states.

Read Cycle

The $\overline{WE}$ control input is used to select read and write modes. A logic HIGH initiates a Read Cycle. The row address must be held for a minimum time, specified by t_{RAH}, while the column address must meet the t_{AR} specification. $\overline{CS}$ may be held LOW or pulsed.

In applications where $\overline{CS}$ is held LOW, D_{OUT} is in a low impedance state except when the cycle is initiated. D_{OUT} becomes valid when t_{RAC} and t_{CAA} are both satisfied.

In applications where $\overline{CS}$ is pulsed, D_{OUT} will remain in a high impedance state until both t_{RLZ} and t_{LZ} are satisfied. D_{OUT} becomes valid only when t_{CAC}, t_{CAA} and t_{RAC} are satisfied. Consequently, the access time is dependent upon the timing relationship between t_{CAC}, t_{CAA} and t_{RAC}. For example, when t_{RAC} and t_{CAC} are satisfied, access time is limited to t_{CAA}.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ LOW during an $\overline{RAS}$ operation. It begins with the last falling edge of $\overline{CS}$ or $\overline{WE}$. As in the read cycle, $\overline{CS}$ may be either held LOW or pulsed.

In applications where $\overline{CS}$ is held LOW, D_{IN} must be valid at or before the falling edge of $\overline{WE}$. D_{OUT} is in a low impedance state except when the cycle is initiated.

In applications where $\overline{CS}$ is pulsed, D_{IN} must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CS}$, whichever occurs last. In an Early Write Cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with $\overline{CS}$ LOW transition), D_{OUT} will be in a high impedance state at the beginning of the Write Cycle. Terminating the Write Cycle with $\overline{CS}$ will maintain D_{OUT} in the high impedance state, while terminating with $\overline{WE}$ allows D_{OUT} to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses ($A_0 - A_7$) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only Cycle will perform refresh. $\overline{CS}$ is not required.

Data Output

The Am90C257 Data Output (D_{OUT}), is controlled by $\overline{CS}$ and secondarily by $\overline{RAS}$ and $\overline{WE}$. $\overline{CS}$ acts only as an output enable. By bringing $\overline{CS}$ HIGH, D_{OUT} switches to the high impedance state within the time specified by t_{HZ}. By taking $\overline{CS}$ LOW, D_{OUT} switches to a low impedance state after the time specified by t_{LZ}.

D_{OUT} is not controlled by $\overline{CS}$ during memory cycle initialization. By bringing $\overline{RAS}$ LOW to initiate a memory cycle, D_{OUT} automatically switches to the high impedance state within the

time specified by t_{RHZ} and will remain in that state for at least the period specified by t_{RLZ}. In an Early Write Cycle, when $\overline{WE}$ is asserted before $\overline{CS}$, D_{OUT} will remain in the high impedance state until the end of write.

Static Column Mode Operation

Static Column Mode Operation permits all 512 columns within a selected row to be randomly accessed at a high data rate. Read, Write and Read–Modify–Write Cycles can be performed during Static Column Mode Operation. The row address is latched by $\overline{RAS}$. Following the entry cycle into Static Column Mode Operation, the data is accessed simply by changing the column address. The column address buffer acts as a transparent or flow-through buffer. Therefore, access begins from a valid column address. Thus, the Am90C257 behaves like a static RAM permitting multiple accesses within the same row.

In a Static Column Read Cycle, $\overline{CS}$ serves only as an output enable. Once $\overline{RAS}$ has been strobed to latch in the row address, and $\overline{CS}$ is pulled LOW to enable the outputs, the column addresses can simply be cycled, with data appearing t_{CAA} after each new column address. $\overline{CS}$ can remain LOW during this entire cycle, simplifying the circuitry needed to implement the Static Column Mode. $\overline{CS}$ can also be tied to ground as long as active data outputs do not cause bus contention.

In Static Column Mode Write Cycles, the addresses are latched internally to avoid disrupting valid data. The latter of $\overline{WE}$ and $\overline{CS}$ will latch in both addresses and data.

APPLICATIONS

Device Description

The Am90C257 is a state-of-the-art, high-performance CMOS 256K DRAM which combines the fastest DRAM speed available (100-ns access time) with low power (standby current < 4 mA). It is designed to operate with a single +5-V power supply, and all input/output voltage levels are TTL-compatible, making the Am90C257 easy to integrate into a wide range of systems. The Am90C257 features the static column access method which is ideal for high-data bandwidth applications. Eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the Am90C257. Nine row address bits are established on the input pins ($A_0 - A_8$) and latched with $\overline{RAS}$. After a minimum t_{RAH} timing specification has been met, the column address flows through the internal address buffer and is not latched by a column address strobe.

The Am90C257 improves system reliability by means of the following on-chip features:

- Allows V_{CC} power-up with floating input levels without causing excess I_{CC} surges (see Device Initialization).
- Tolerates real-time V_{CC} fluctuation between 4.5 V and 5.5 V while memory chip is in operation.
- Accepts input voltage transition overshoot (V_{CC} + 1 V) and undershoot (–1 V).
- Fabricated with a CMOS technology that is optimized to provide very high device latch-up voltage in excess of 10 volts.

4

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −10 to +80°C
Voltage on Any Pin Relative to V_{SS} (Except V_{CC}) ..... −2 to +7.5 V
Voltage on V_{CC} Supply Relative to V_{SS} ..... −1 to +7.5 V
Short Circuit Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Input High Voltage (V_{IH}) ..... 2.4 V to V_{CC} +1.0 V
Input Low Voltage (V_{IL}) ..... −1.0 V to 0.8 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Part No.	Min.	Max.	Unit
V_{OH}	Output Levels	Output HIGH Voltage (I_{OH} = 5.0 mA)		2.4		V
V_{OL}		Output LOW Voltage (I_{OL} = 4.2 mA)			0.4	
V_{IH}	Input HIGH Voltage	0°C ≤ T_A ≤ +70°C		2.4	V_{CC} + 1.0 V	V
V_{IL}	Input LOW Voltage			−1.0	0.8	V
$I_{I(L)}$	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.0 V, V_{SS} = 0 V All Other Pins Not Under Test = 0 V		−10	10	μA
$I_{O(L)}$	Output Leakage Current	Data-Out Disabled, 0 V < V_{OUT} < 5.5 V		−10	10	μA
I_{CC1}	Operating Current	$\overline{RAS}$, $\overline{CS}$ Cycling t_{RC} = Min.	Am90C257-08		85	mA
			Am90C257-10		65	
			Am90C257-12		60	
I_{CC2}	Standby Current	$\overline{RAS}$ = $\overline{CS}$ = V_{IH} (TTL Level)			4	mA
I_{CC3}	V_{CC} Supply Current $\overline{RAS}$-Only Refresh	$\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH} t_{RC} = Min.	Am90C257-08		85	mA
			Am90C257-10		65	
			Am90C257-12		60	
I_{CC4}	Static Column Mode Operating Current	$\overline{RAS}$ = V_{IL} t_{RC} = Min.	Am90C257-08		85	mA
			Am90C257-10		65	
			Am90C257-12		60	
I_{CC5}	V_{CC} Supply Current Standby Output Enabled	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}			6	mA

Notes: 1. All voltages referenced to V_{SS}.
2. Specified I_{CC} (Max.) is measured with output open.
3. Test conditions apply for DC Characteristics only.

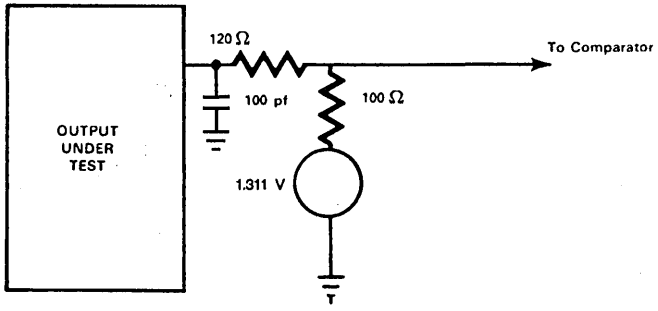
CAPACITANCE*

(T_A = +25°C, V_{CC} = 5 V, f = 1.0 MHz)

Symbol	Parameter	Max.	Units
C_{IN1}	Input Capacitance A_0 to A_8, D_{IN}	5	pF
C_{IN2}	Input Capacitance $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$	6	pF
C_{OUT}	Output Capacitance D_{OUT}	6	pF

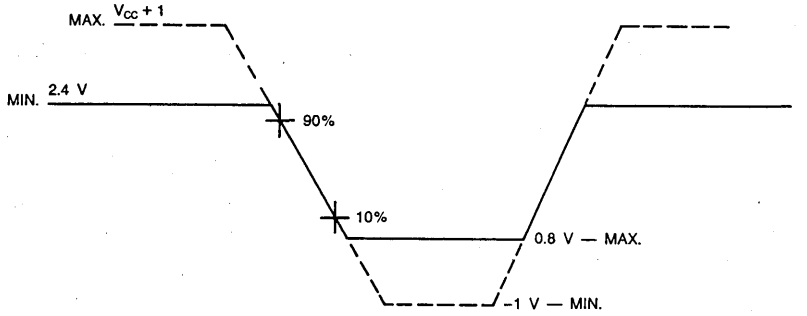
*Measured with a Boonton Meter or calculated from the equation C = IΔt/ΔV.

SWITCHING TEST CIRCUIT



TC002323

SWITCHING TEST WAVEFORM



WF010380

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

4

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

(Table continued on next page)

No.	Parameter Symbol	Parameter Description	Am90C257-08		Am90C257-10		Am90C257-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ, REFRESH and WRITE CYCLES									
1	t_{RAS}	$\overline{RAS}$ Pulse Width	80	75,000	100	75,000	120	75,000	ns
2	t_{RC}	Random R/W Cycle Time	130		170		200		ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		60		70		ns
4	t_{CSH}*	$\overline{CS}$ Hold Time	80		100		120		ns
5	t_{WRP}	Write-to-$\overline{RAS}$ Precharge Time	0		0		0		ns
6	t_{ASR}	Row Address Setup Time	3		3		3		ns
7	t_{RAH}	Row Address Hold Time	12		15		15		ns
8	t_{AR}	Column Address Hold Time from $\overline{RAS}$	80		100		120		ns
9	t_{RHZ}	$\overline{RAS}$-to-Output High Impedance (Note 1)		15		20		20	ns
10	t_{RLZ}	$\overline{RAS}$-to-Output Low Impedance (Note 1)	30		30		30		ns
11	t_{HZ}*	$\overline{CS}$-to-Output High Impedance (Notes 1 & 2)		15		20		25	ns
12	t_{LZ}*	$\overline{CS}$-to-Output Low Impedance (Notes 1 & 2)							
13	t_{REF}	Time Between Refresh		4		4		4	ms
14	t_T	Transition Time (Rise and Fall) (Note 3)	3	50	3	50	3	50	ns
READ CYCLE									
15	t_{RAC}	Access Time From $\overline{RAS}$ (Notes 4 & 5)		80		100		120	ns
16	t_{CAC}*	Access Time From $\overline{CS}$ (Note 5)		15		20		25	ns
17	t_{CAA}	Access Time from Column Address (Note 5)		30		35		40	ns
18	$t_{CS\ (R)}$*	$\overline{CS}$ Pulse Width (Read Cycle)	15		20		25		ns
19	$t_{RSH\ (R)}$*	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		10		ns
20	t_{RCS}*	Read Command Setup Time	0		0		0		ns
21	t_{CAR}	Column Address-to-$\overline{RAS}$ Setup Time	30		35		40		ns
22	t_{RCH}*	Read Command Hold Time Referenced to $\overline{CS}$	0		0		0		ns
23	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	10		10		10		ns
24	t_{ARH}	Column Address Hold Time Referenced to $\overline{RAS}$	10		10		10		ns
25	t_{RAD}	$\overline{RAS}$-to-Column Address Delay Time (Note 6)	17	50	20	65	20	80	ns
26	$t_{CS\ (W)}$*	$\overline{CS}$ Pulse Width (Write Cycle)	15		20		25		ns
27	$t_{RSH\ (W)}$*	$\overline{RAS}$ Hold Time (Write Cycle)	15		20		25		ns
WRITE CYCLE									
28	t_{WDR}	$\overline{RAS}$-to-Write Command Delay Time	20		25		25		ns
29	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		25		ns
30	t_{CWL}*	Write Command to $\overline{CS}$ Lead Time	15		20		25		ns
31	t_{WP}	Write Command Pulse Width	15		20		25		ns
32	t_{WCP}	Write Command Precharge Time	10		10		10		ns
33	t_{WCS}*	Write Command Setup Time	0		0		0		ns
34	t_{WCH}*	Write Command Hold Time	15		20		25		ns
35	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	80		100		120		ns
36	t_{AWS}	Column Address-to-Write Command Setup Time	5		5		5		ns
37	t_{AWH}	Column Address-to-Write Command Hold Time	12		15		20		ns
38	t_{DS}	Data-In Setup Time	5		5		5		ns
39	t_{DH}	Data-In Hold Time	12		15		20		ns
40	t_{OW}	Output Active from End of Write	0		0		0		ns

*This parameter not applicable if operated with $\overline{CS}$ grounded.

Notes: See next page for notes.

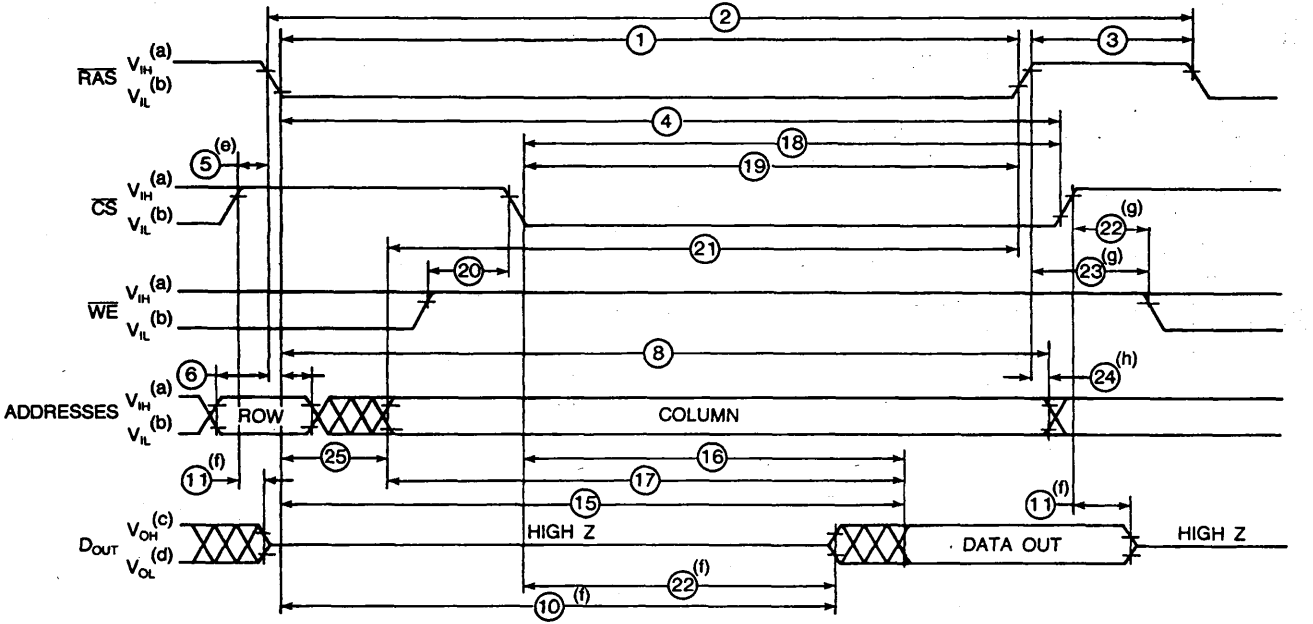
SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90C257-08		Am90C257-10		Am90C257-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ-MODIFY-WRITE (RMW) CYCLE									
41	t_{RWC}	RMW Cycle Time	150		195		230		ns
42	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	100	75,000	125	75,000	150	75,000	ns
43	t_{CRW}*	RMW Cycle $\overline{CS}$ Pulse Width	35		45		55		ns
44	t_{WRH}	$\overline{WE}$-to-$\overline{RAS}$ Hold Time	5		5		5		ns
45	t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time (Note 7)	80		100		120		ns
46	t_{AWD}	Column Address-to-$\overline{WE}$ Delay Time (Note 7)	30		35		40		ns
47	t_{CWD}	$\overline{CS}$-to-$\overline{WE}$ Delay Time (Note 7)	15		20		25		ns
STATIC COLUMN MODE CYCLE									
48	t_{OHA}	Output Hold Time from Address Change	0		0		0		ns
49	t_{OHW}	Output Hold Time from End of Write	0		0		0		ns
50	t_{WPA}	RMW Write Precharge Access Time		40		45		50	ns
51	t_{WRA}	RMW Write-Read Access Time		60		70		80	ns
52	t_{WPS}	RMW Write Command Precharge Time	40		45		50		ns

*This parameter not applicable if operated with $\overline{CS}$ grounded.

Notes:
1. Assumes three-state test load (5 pF and a 380 Ω Thevenin equivalent).
2. At any given temperature and voltage combination, t_{HZ} (Max.) is less than t_{LZ} (Min.) from device to device.
3. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
4. Assumes that $t_{RAD} \leq t_{RAD}$ (Max.). If $t_{RAD} > t_{RAD}$ (Max.), then t_{RAC} will increase by the amount that t_{RAD} exceeds to t_{RAD} (Max.).
5. Load = 2 TTL loads and 100 pF.
6. t_{RAD} specified for reference only.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an Early Write Cycle and the data-out pin will remain in high impedance for the duration of $\overline{WE}$. If $t_{WCD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a Read-Modify-Write Cycle and the data-out will contain the data read from the selected address. If any of the above conditions are not satisfied, data-out is indeterminate.
8. Access time from a write command to a read command is determined by the latter of t_{CAA} or t_{WPA} or t_{WRA}.

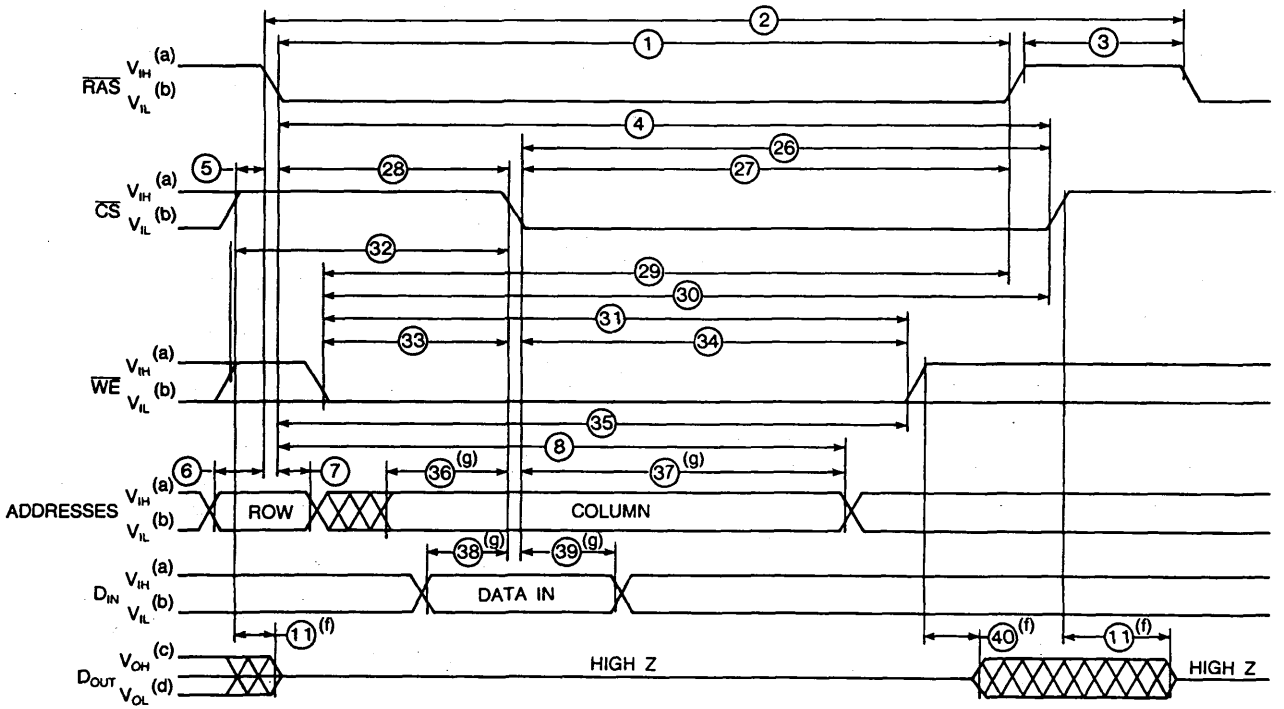
SWITCHING WAVEFORMS



Read Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) *are reference levels for measuring timing of input signals.*
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CS}$ or $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).
g. Either t_{RCH} or t_{RRH} must be satisfied.
h. If $t_{ARH} \geq t_{ARH}$ (Min.), then data from the last address will be latched on D_{OUT}, as long as D_{OUT} is held in low impedance by $\overline{CS}$.

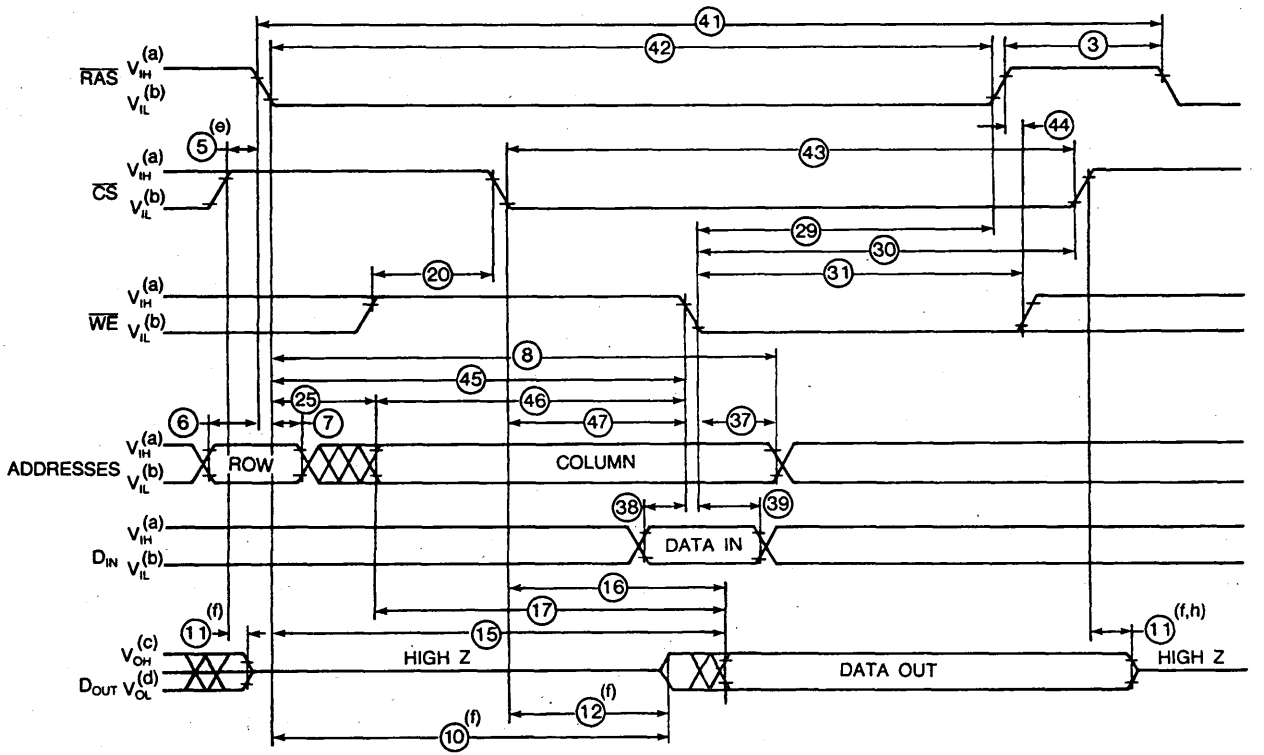
SWITCHING WAVEFORMS (Cont.)



Write Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CS}$ or $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).
g. t_{AWS}, t_{AWH}, t_{DS}, t_{DH} and t_{WDR} are referenced to $\overline{CS}$ or $\overline{WE}$ low transition, whichever occurs last.
h. t_{WCP} (Min.) is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ high transition to the later of $\overline{CS}$ or $\overline{WE}$ low transition.
i. If $\overline{CS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance.

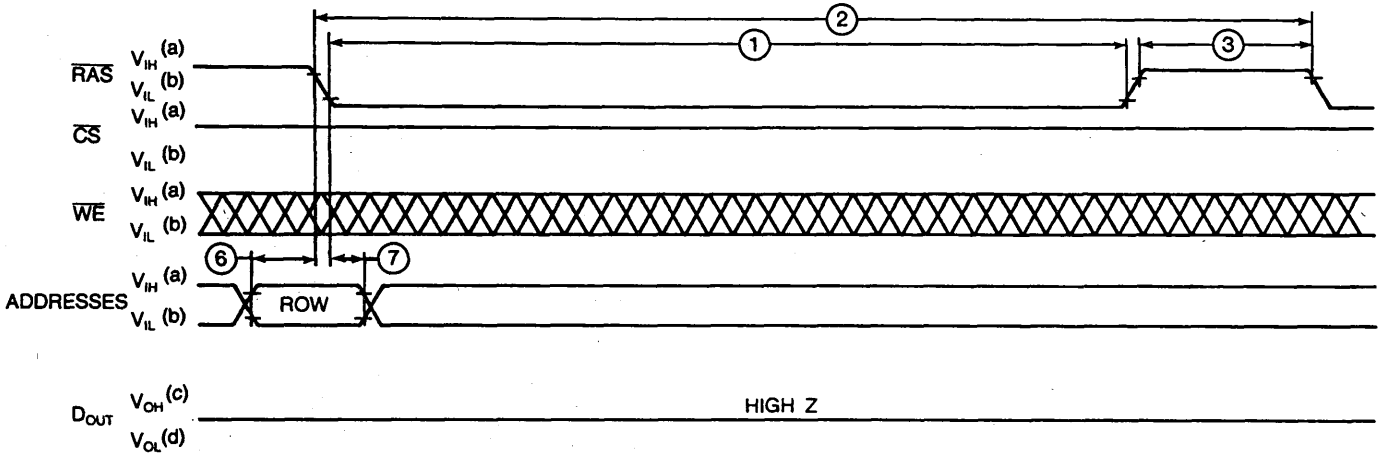
SWITCHING WAVEFORMS (Cont.)



Read – Modify – Write Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT} signals.
e. t_{WRP} is referenced to $\overline{CS}$ or $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 MV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).
g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CS}$ or $\overline{WE}$ low transition, whichever occurs last.
h. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{WRH} \geq t_{WRH}$ (Min.).

SWITCHING WAVEFORMS (Cont.)

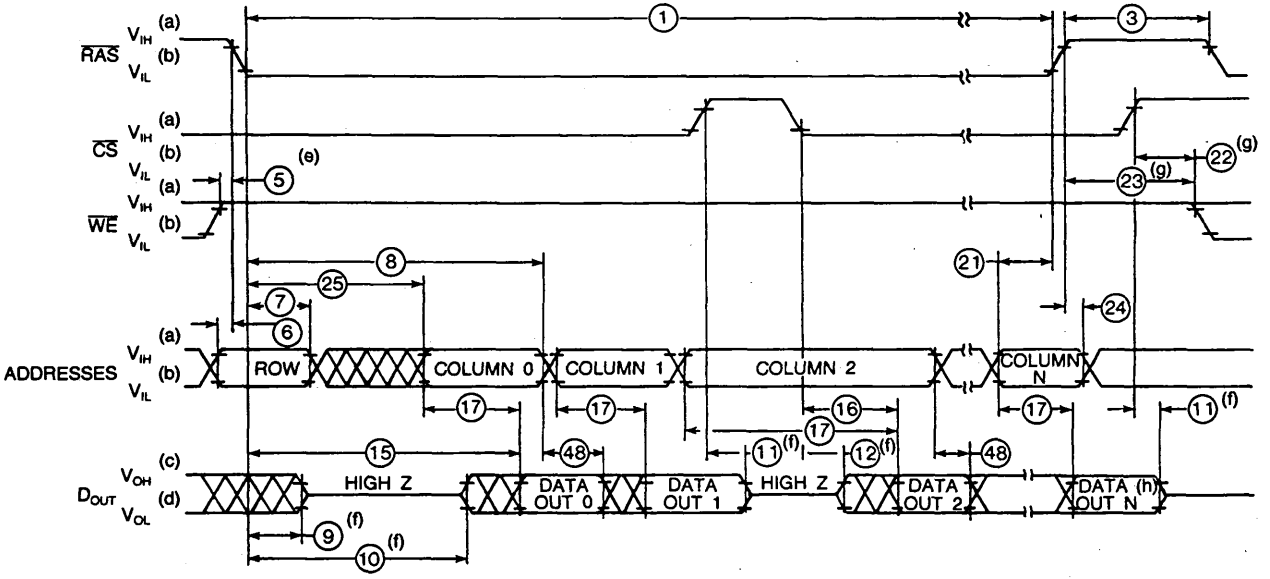


WF010830

$\overline{RAS}$ – Only Refresh Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.

SWITCHING WAVEFORMS (Cont.)

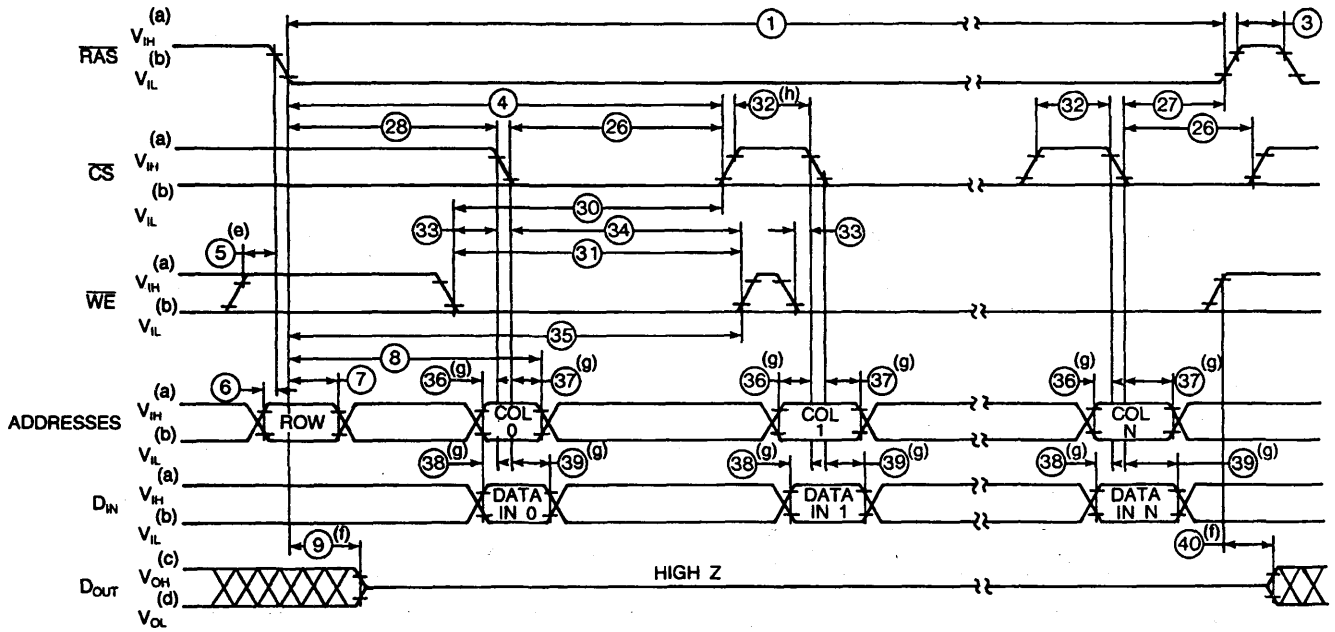


WF010840

Static Column Mode Read Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CS}$ or $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).
g. Either t_{RCH} or t_{RRH} must be satisfied.
h. D_{OUT} is valid as shown if and only if $t_{ARH} \geq t_{ARH}$ (Min.).
i. $\overline{CS}$ pulse is shown for reference in this case. D_{OUT} will go to high impedance.

SWITCHING WAVEFORMS (Cont.)

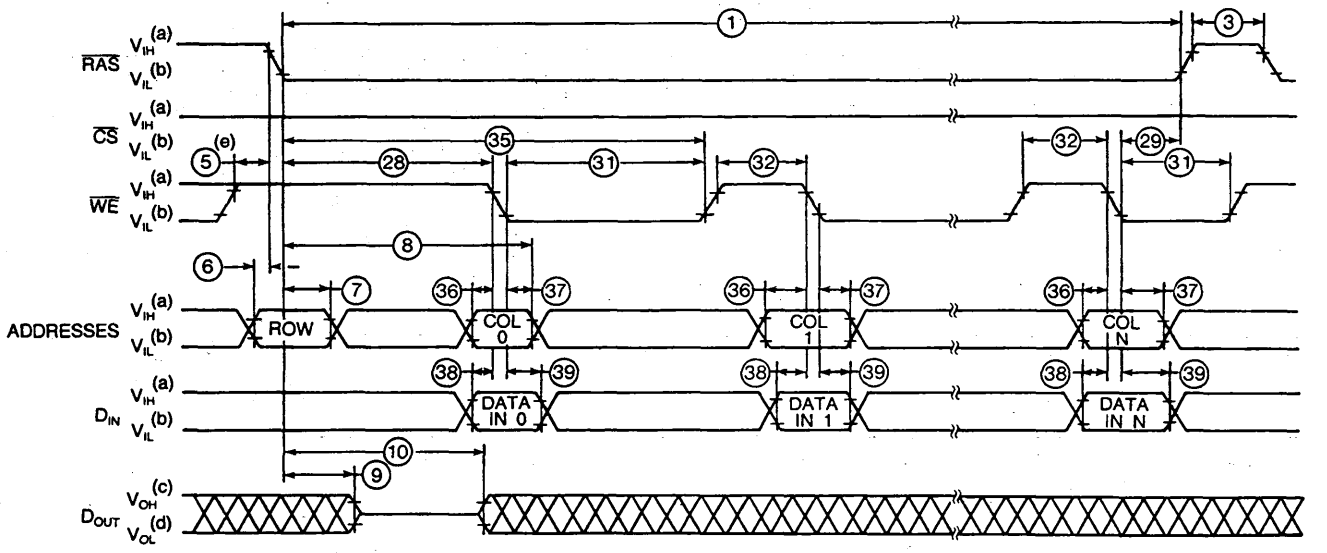


WF010850

Static Column Mode Write Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CS}$ or $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).
g. t_{AWS}, t_{AWH}, t_{DS}, t_{DH} and t_{WDR} are referenced to $\overline{CS}$ or $\overline{WE}$ low transition, whichever occurs last.
h. t_{WCP} (Min.) is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ high transition to the later of $\overline{CS}$ or $\overline{WE}$ low transition.
i. If $\overline{CS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance.

SWITCHING WAVEFORMS (Cont.)

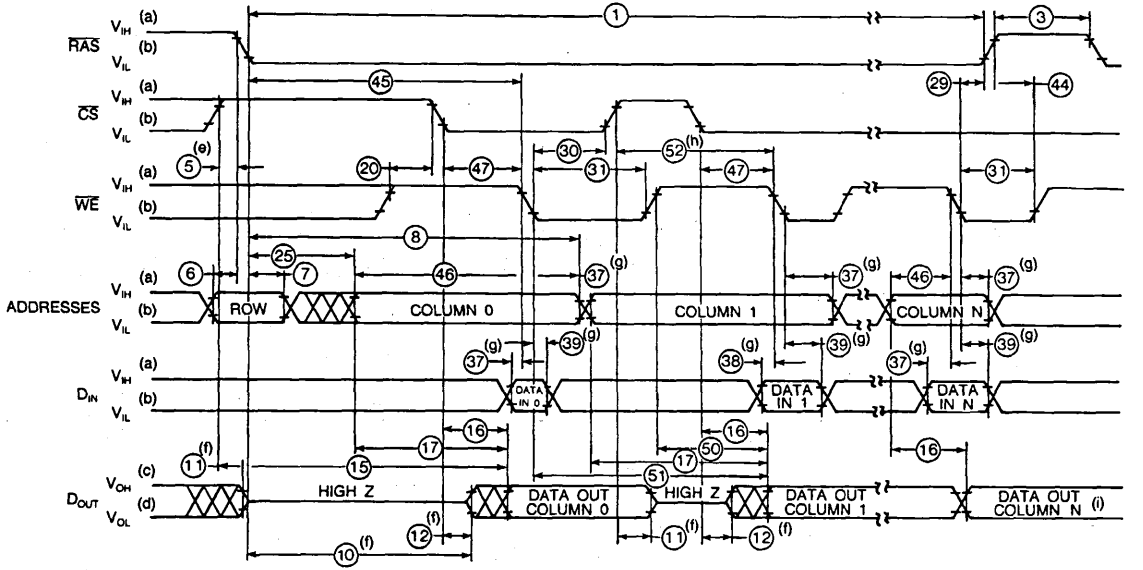


WF010860

Static Column Mode Write Cycle ($\overline{CS}$ Low)

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).

SWITCHING WAVEFORMS (Cont.)

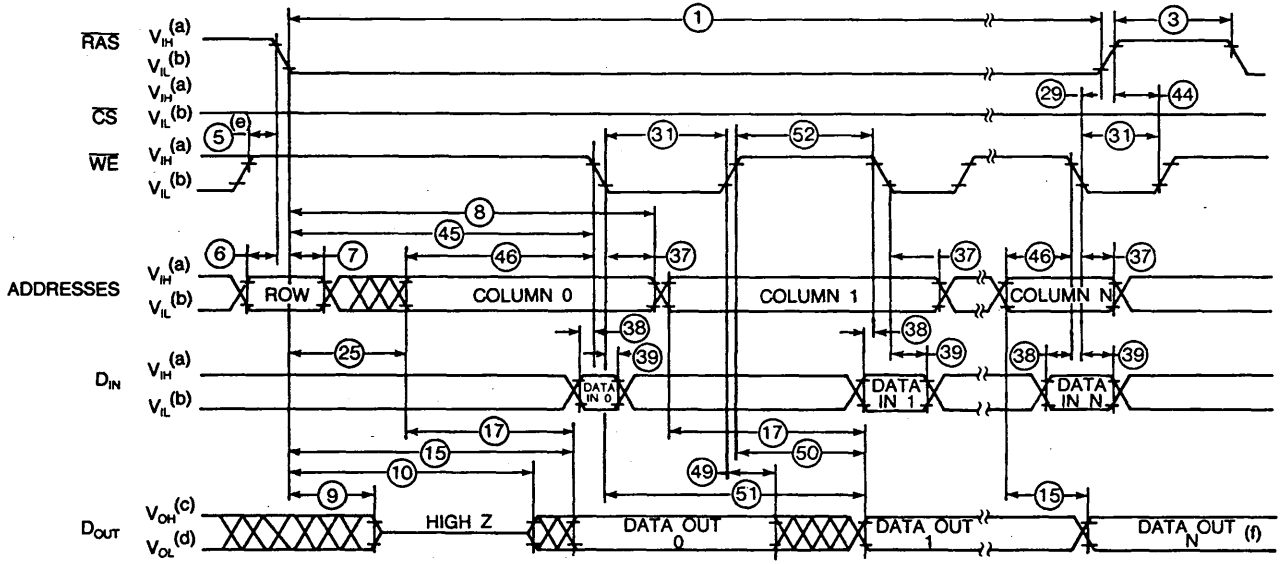


WF010871

Static Column Mode Read – Modify – Write Cycle

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CS}$ or $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and a 380 Ω Thevenin equivalent).
g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CS}$ or $\overline{WE}$ low transition, whichever occurs last.
h. t_{WPS} (Min.) is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ high transition to the later of $\overline{CS}$ or $\overline{WE}$ low transition.
i. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{WRH} \geq t_{WRH}$ (Min.).

SWITCHING WAVEFORMS (Cont.)



Static Column Mode Read – Modify – Write Cycle ($\overline{CS}$ Low)

Notes: a & b. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals.
c & d. V_{OH} (Min.) and V_{OL} (Max.) are reference levels for measuring timing of D_{OUT}.
e. *Transition is measured ±500 mV from steady state voltage with specified three-state load (5 pF and 380 Ω Thevenin equivalent).*
f. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{WRH} \geq t_{WRH}$ (Min.).

Am90CL257

Low-Power 256K x 1 CMOS Static Column Mode DRAM

OVERVIEW

The 256K x 1 CMOS Low-Power ('L') DRAM versions share common functional descriptions, DC and AC characteristics with the corresponding standard CMOS (non-'L') versions. The only additions to these sections are:

DISTINCTIVE CHARACTERISTICS

- Extended refresh period
  — 32 ms (Max.) during standby
- Low data retention current
  — 230 μA (Max.)
- Low-power dissipation
  — 0.55 mW (Max.)

ORDERING INFORMATION

The Ordering Information for the Low-Power DRAM versions are the same as for the Standard CMOS DRAMs, with the exception of an 'L' inserted within the device number to denote 'Low-Power.' For example, the Am90CL255 is = a 256K x 1 CMOS "Low-Power" Nibble Mode DRAM. All temperature ranges, speed and package options remain the same as those listed in Ordering Information sections for the respective Standard CMOS DRAMs.

DC CHARACTERISTICS

The low-power version DRAMs are screened for one additional parameter, viz, CMOS standby current. All other DC characteristics remain the same for both families.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{CC6}	V_{CC} Supply Current CMOS Standby	$\overline{RAS} \geq V_{CC} - 0.5$ V and $\overline{CAS}$ at V_{IH}, all other inputs and outputs $\geq V_{SS}$	Am90CL257		0.1	mA

The Am90CL257-15 is screened for I_{CC1} = 55 mA, I_{CC3} = 55 mA, and I_{CC4} = 55 mA.

AC CHARACTERISTICS

AC Characteristics remain unchanged on the low-power 100 ns and 120 ns versions. The AC characteristics corresponding to the 150 ns speed are on the following page.

FUNCTIONAL DESCRIPTION

The Functional Descriptions for low-power versions are the same as the corresponding standard versions. The low-power devices, however, support Extended Refresh cycles described below:

Extended Refresh Cycle

All low-power versions extend the Refresh Cycle period to 32 ms for $\overline{RAS}$-Only Refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA for data retention. The low-standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})\ (I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{T_{RI}}$$

where t_{RC} = Refresh Cycle Time

and t_{RI} = Refresh Interval Time or $t_{REF}/256$

Before entering or leaving an Extended Refresh period, the entire array must be refreshed at the normal interval of 4 ms. This can be accomplished by either a burst or distributed refresh.

Publication # 07412 Rev. A Amendment /0
Issue Date: May 1986

SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL257-15 Min.	Am90CL257-15 Max.	Units
READ/WRITE/READ-MODIFY-WRITE AND REFRESH CYCLES					
1	t_{RAS}	$\overline{RAS}$ Pulse Width	150	75,000	ns
2	t_{RC}	Random R/W Cycle Time	245		ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	85		ns
4	t_{CSH}*	$\overline{CS}$ Hold Time	150		ns
5	t_{WRP}	Write-to-$\overline{RAS}$ Precharge Time	0		ns
6	t_{ASR}	Row Address Setup Time	0		ns
7	t_{RAH}	Row Address Hold Time	15		ns
8	t_{AR}	Column Address Hold Time from $\overline{RAS}$	130		ns
9	t_{RHZ}	$\overline{RAS}$-to-Output High Impedance (Note 1)		20	ns
10	t_{RLZ}	$\overline{RAS}$-to-Output Low Impedance (Note 1)	30		ns
11	t_{HZ}*	$\overline{CS}$-to-Output High Impedance (Notes 1 & 2)		25	ns
12	t_{LZ}*	$\overline{CS}$-to-Output Low Impedance (Notes 1 & 2)			
13	t_{REF}	Time Between Refresh		4	ms
14	t_T	Transition Time (Rise and Fall) (Note 3)	3	50	ns
READ CYCLE					
15	t_{RAC}	Access Time From $\overline{RAS}$ (Notes 4 & 5)		150	ns
16	t_{CAC}*	Access Time From $\overline{CS}$ (Note 5)		30	ns
17	t_{CAA}	Access Time from Column Address (Note 5)		65	ns
18	t_{CS} (R)*	$\overline{CS}$ Pulse Width (Read Cycle)	30		ns
19	t_{RSH} (R)*	$\overline{RAS}$ Hold Time (Read Cycle)	10		ns
20	t_{RCS}*	Read Command Setup Time	0		ns
21	t_{CAR}	Column Address-to-$\overline{RAS}$ Setup Time	65		ns
22	t_{RCH}*	Read Command Hold Time Referenced to $\overline{CS}$	0		ns
23	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	10		ns
24	t_{ARH}	Column Address Hold Time Referenced to $\overline{RAS}$	0		ns
25	t_{RAD}	$\overline{RAS}$-to-Column Address Delay Time (Note 6)	20	85	ns
26	t_{CS} (W)*	$\overline{CS}$ Pulse Width (Write Cycle)	30		ns
27	t_{RSH} (W)*	$\overline{RAS}$ Hold Time (Write Cycle)	30		ns
WRITE CYCLE					
28	t_{WDR}	$\overline{RAS}$-to-Write Command Delay Time	20		ns
29	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		ns
30	t_{CWL}*	Write Command to $\overline{CS}$ Lead Time	30		ns
31	t_{WP}	Write Command Pulse Width	30		ns
32	t_{WCP}	Write Command Precharge Time	10		ns
33	t_{WCS}*	Write Command Setup Time	0		ns
34	t_{WCH}*	Write Command Hold Time	30		ns
35	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	120		ns
36	t_{AWS}	Column Address-to-Write Command Setup Time	0		ns
37	t_{AWH}	Column Address-to-Write Command Hold Time	25		ns
38	t_{DS}	Data-In Setup Time	0		ns
39	t_{DH}	Data-In Hold Time	25		ns
40	t_{OW}	Output Active from End of Write	0		ns

*This parameter not applicable if operated with $\overline{CS}$ grounded.
Notes: See next page for notes.

SWITCHING CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL257-15 Min.	Am90CL257-15 Max.	Units
READ-MODIFY-WRITE (RMW) CYCLE					
41	t_{RWC}	RMW Cycle Time	280		ns
42	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	185	75,000	ns
43	t_{CRW}*	RMW Cycle $\overline{CS}$ Pulse Width	65		ns
44	t_{WRH}	$\overline{WE}$-to-$\overline{RAS}$ Hold Time	5		ns
45	t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time (Note 7)	150		ns
46	t_{AWD}	Column Address-to-$\overline{WE}$ Delay Time (Note 7)	75		ns
47	t_{CWD}	$\overline{CS}$-to-$\overline{WE}$ Delay Time (Note 7)	30		ns
STATIC COLUMN MODE CYCLE					
48	t_{OHA}	Output Hold Time from Address Change	10		ns
49	t_{OHW}	Output Hold Time from End of Write	0		ns
50	t_{WPA}	RMW Write Precharge Access Time		75	ns
51	t_{WRA}	RMW Write-Read Access Time		110	ns
52	t_{WPS}	RMW Write Command Precharge Time	75		ns

*This parameter not applicable if operated with $\overline{CS}$ grounded.

Notes:
1. Assumes three-state test load (5 pF and a 380 Ω Thevenin equivalent).
2. At any given temperature and voltage combination, t_{HZ} (Max.) is less than t_{LZ} (Min.) from device to device.
3. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
4. Assumes that $t_{RAD} \leq t_{RAD}$ (Max.). If $t_{RAD} > t_{RAD}$ (Max.), then t_{RAC} will increase by the amount that t_{RAD} exceeds to t_{RAD} (Max.).
5. Load = 2 TTL loads and 100 pF.
6. t_{RAD} specified for reference only.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an Early Write Cycle and the data-out pin will remain in high impedance for the duration of $\overline{WE}$. If $t_{WCD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a Read-Modify-Write Cycle and the data-out will contain the data read from the selected address. If any of the above conditions are not satisfied, data-out is indeterminate.
8. Access time from a write command to a determined by the latter of t_{CAA} or t_{WPA} or t_{WRA}.

Am9044/9244

4096 x 1 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating and standby power
- Access times down to 200 ns
- Am9044 is a direct plug-in replacement for 4044
- Am9244 pin and function compatible with Am9044 and 4044 plus $\overline{CS}$ power-down feature
- High output drive — 4.0 mA sink current @ 0.4 V
- TTL identical interface logic levels

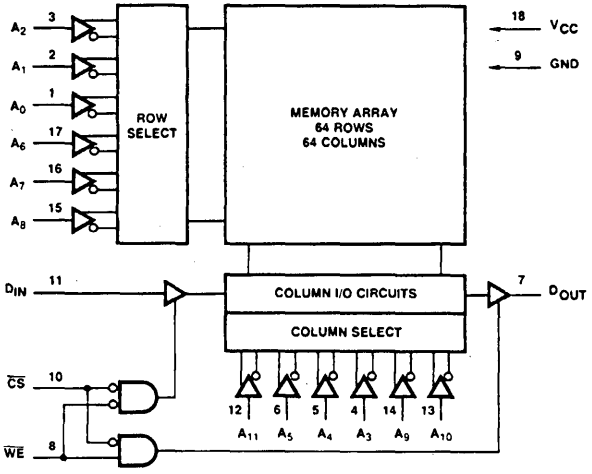
GENERAL DESCRIPTION

The Am9044 and Am9244 are high-performance, static, N-Channel, read/write, random-access memories organized as 4096 x 1. Operation is from a single 5 V supply, and all input/output levels are identical to standard TTL specifications. Low-power versions of both devices are available with power savings of about 30%. The Am9044 and Am9244 are the same except that the Am9244 offers an automatic $\overline{CS}$ power-down feature.

The Am9244 remains in a low-power standby mode as long as $\overline{CS}$ remains HIGH, thus reducing its power requirements. The Am9244 power decreases from 385 mW to 165 mW in the standby mode, and the Am92L44 from 275 mW to 110 mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9044.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0 mA for Am9244 and Am9044 provide increased short-circuit current for improved drive.

BLOCK DIAGRAM



BD000091

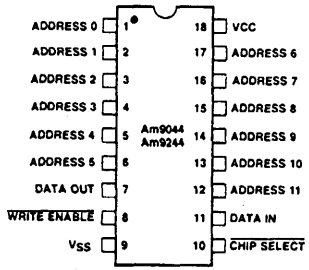
Publication # 03254 | Rev. D | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

Part Number			Am9044/90L44 and Am9244/92L44			
Speed Indicator			B	C	D	E
Maximum Access Time (ns)			450	300	250	200
0 to +70°C	I_{CC} (mA)	Standard	70	70	70	70
		Low-Power	50	50	50	–
	I_{PD} (mA) (Note 1)	Standard	30	30	30	30
		Low-Power	20	20	20	–
−55 to +125°C	I_{CC} (mA)	Standard	80	80	80	–
		Low-Power	60	60	–	–
	I_{PD} (mA) (Note 1)	Standard	33	33	33	–
		Low-Power	22	22	–	–

Notes: 1. Am9244/92L44 only.

CONNECTION DIAGRAM
Top View

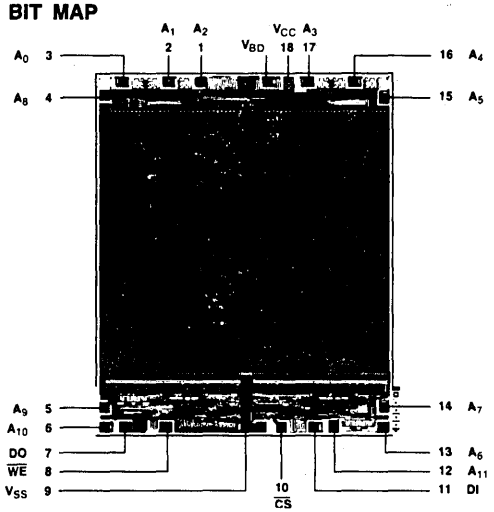


CD000141

Note: Pin 1 is marked for orientation.

Address Designators	
External	Internal
A_0	A_2
A_1	A_1
A_2	A_0
A_3	A_8
A_4	A_9
A_5	A_{10}
A_6	A_3
A_7	A_4
A_8	A_5
A_9	A_7
A_{10}	A_6
A_{11}	A_{11}

BIT MAP

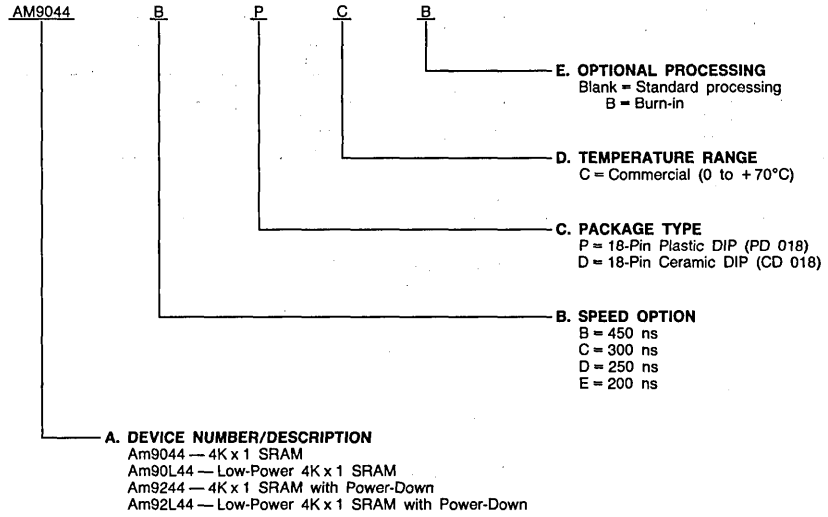


Die Size 0.137" x 0.167"

ORDERING INFORMATION (Con't.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9044B	PC, PCB, DC, DCB
AM90L44B	
AM9244B	
AM92L44B	
AM9044C	
AM90L44C	
AM9244C	
AM92L44C	
AM9044D	
AM90L44D	
AM9244D	
AM92L44D	
AM9044E	
AM90L44E	
AM9244E	
AM92L44E	

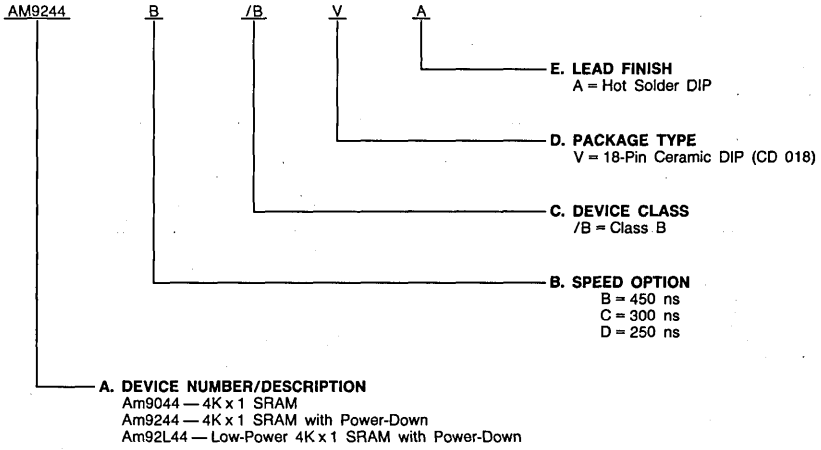
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9044B	/BVA
AM9244B	
AM92L44B	
AM9044C	
AM9244C	
AM92L44C	
AM9044D	
Am90L44D	
AM9244D	
AM92L44D	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

PIN DESCRIPTION

$A_0 - A_{11}$ Address Inputs (Inputs)
The address input lines select the memory location from which to read or write.

$\overline{CS}$ Chip Select (Input, Active LOW)
The $\overline{CS}$ line selects the memory device for active operation.

$\overline{WE}$ Write Enable (Input, Active LOW)
When both $\overline{CS}$ and $\overline{WE}$ are LOW, data on the input lines is written to the location presented on the address input lines.

D_{IN} Data In (Input)
This pin is used to enter data during write operations.

D_{OUT} Data Out (Output, Three-State)
The content of the selected memory location is presented on the Data Output line during read operations ($\overline{CS}$ LOW, $\overline{WE}$ HIGH). The line goes three-state during write operations.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
All Signal Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military products 100% tested at T_C = +75°C, +125°C and −55°C

DC CHARACTERISTICS over operating range unless otherwise specified*

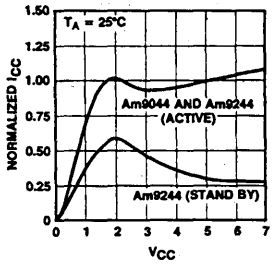
Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	T_A = 70°C		−1.0		mA
			T_A = 125°C		−0.4		
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	T_A = 70°C		4.0		mA
			T_A = 125°C		3.2		
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10	μA
I_{OZ}	Output Leakage Current	0.4V ≤ V_O ≤ V_{CC}, Output Disabled	T_A = +70°C		−50	50	μA
			T_A = +125°C		−10	10	
I_{CC}	Operating Supply Current	V_{CC} = Max. $\overline{CS} \leq V_{IL}$ (9244/92L44 only)	T_A = 0°C	Standard devices		70	mA
				L devices		50	
			T_A = −55°C	Standard devices		80	
				L devices		60	
I_{PD}	Automatic $\overline{CS}$ Power-Down Current (9244/92L44 only)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$	T_A = 0°C	9244		30	mA
				92L44		20	
			T_A = −55°C	9244		33	
				92L44		22	
C_I	Input Capacitance (Note 6)	Test Frequency = 1.0 MHz, T_A = 25°C, All pins at 0 V				7.0	pF
C_O	Output Capacitance (Note 6)					7.0	

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V and output loading of one standard TTL gate plus 100 pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9244 than for the Am9044. The specified address access time will be valid only when $\overline{CS}$ is LOW soon enough for t_{CO} to elapse.
6. *These parameters are not* 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

*See last page of this spec for Group A Subgroup Testing information.

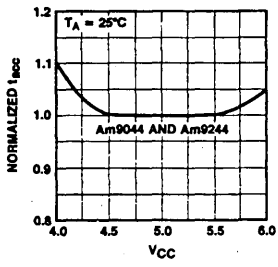
TYPICAL DC and AC CHARACTERISTICS

Normalized Suplly Current Versus Supply Voltage



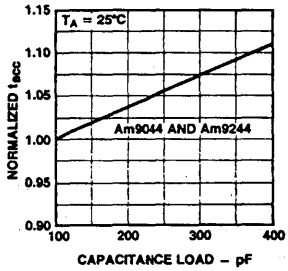
OP000891

Normalized Access Time Versus Supply Voltage



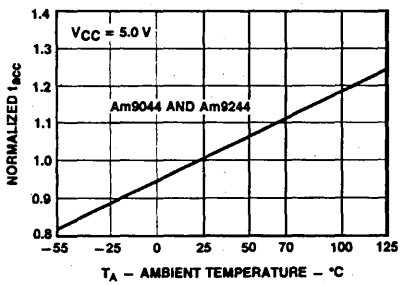
OP000901

Normalized Access Time Versus Output Loading



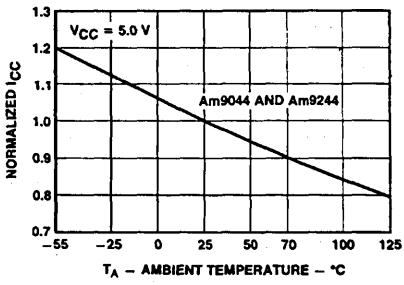
OP000911

Normalized Access Time Versus Ambient Temperature



OP000921

Normalized Supply Current Versus Ambient Temperature



OP000931

4

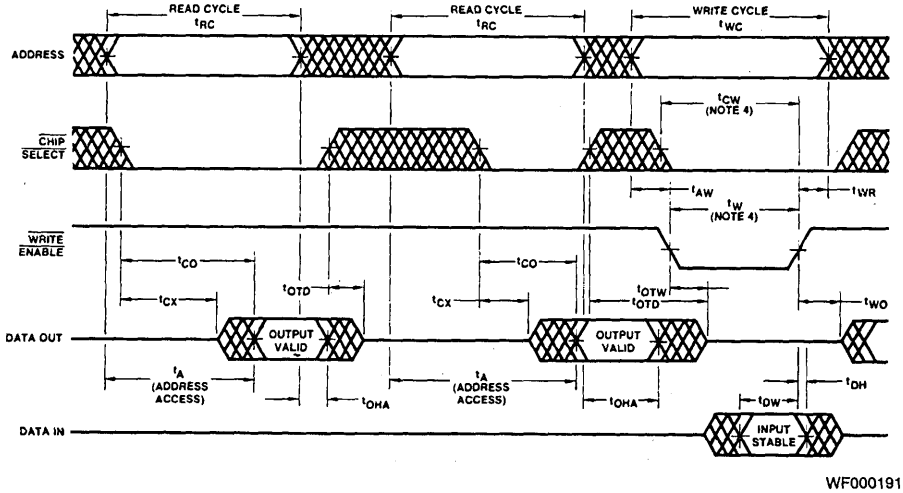
SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Notes 3 – 6)

No.	Parameter Symbol	Parameter Description		B devices		C devices		D devices		E devices		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		250		200		
2	t_A	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		250		200	
3	t_{CO}	Chip Select LOW to Data Out Valid (Note 5)	Am9044		100		100		70		70	
			Am9244		450		300		250		200	ns
4	t_{CX}	Chip Select LOW to Data Out On (Note 6)		10		10		10		10		
5	t_{OTD}	Chip Select HIGH to Data Out Off (Note 6)			100		80		60		60	
6	t_{OHA}	Address Unknown to Data Out Unknown Time		20		20		20		20		
Write Cycle												
7	t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		250		200		
8	t_W	Write Enable LOW to Write Enable HIGH Time (Note 4)	Am9044	200		150		100		100		
			Am9244	250		200		150		150		
9	t_{WR}	Write Enable HIGH to Address Do Not Care Time		0		0		0		0		
10	t_{OTW}	Write Enable LOW to Data Out Off Delay (Note 6)			100		80		60		60	
11	t_{DW}	Data In Valid to Write Enable HIGH Time		200		150		100		100		
12	t_{DH}	Write Enable HIGH to Data In Do Not Care Time		0		0		0		0		ns
13	t_{AW}	Address Valid to Write Enable LOW Time		0		0		0		0		
14	t_{PD}	Chip Select HIGH to Power LOW Delay (Am9244 only Note 6)			200		150		100		100	
15	t_{PU}	Chip Select LOW to Power HIGH Delay (Am9244 only Note 6)		0		0		0		0		
16	t_{CW}	Chip Select LOW to Write Enable HIGH Time (Note 4)	Am9044	200		150		100		100		
			Am9244	250		200		150		150		
17	t_{WO}	Write Enable HIGH To Output Turn On (Note 6)			100		100		70		70	

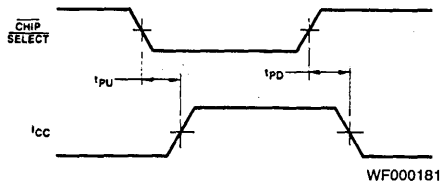
Notes: See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF000191



WF000181

Power-Down Waveform (Am9244 only)

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups	Parameter Symbol	Subgroups
t_{RC}	7, 8, 9, 10, 11	t_{OTW}	7, 8, 9, 10, 11
t_A	7, 8, 9, 10, 11	t_{DW}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11	t_{DH}	7, 8, 9, 10, 11
t_{CX}	7, 8, 9, 10, 11	t_{AW}	7, 8, 9, 10, 11
t_{OTD}	7, 8, 9, 10, 11	t_{PD}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11	t_{PU}	7, 8, 9, 10, 11
t_{WC}	7, 8, 9, 10, 11	t_{CW}	7, 8, 9, 10, 11
t_W	7, 8, 9, 10, 11	t_{WO}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11		

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test Conditions are selected at AMD's option.

Am90C644

64K x 4 CMOS DUAL-ARRAY MEMORY

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 64K x 4 organization
- High-speed access: t_{RAC} – 100 ns
- Write-per-Bit mask allows separate write controls for each of the four DRAM input bits
- On-chip video shifter with up to 100 Megapixel/sec. bandwidth
- Dual-port access permits shifter operation independent of DRAM
- Bi-directional interface between DRAM and shifter
- Shifter port can serve as a serial input port
- Single cycle reset of shifter on command
- CMOS technology

GENERAL DESCRIPTION

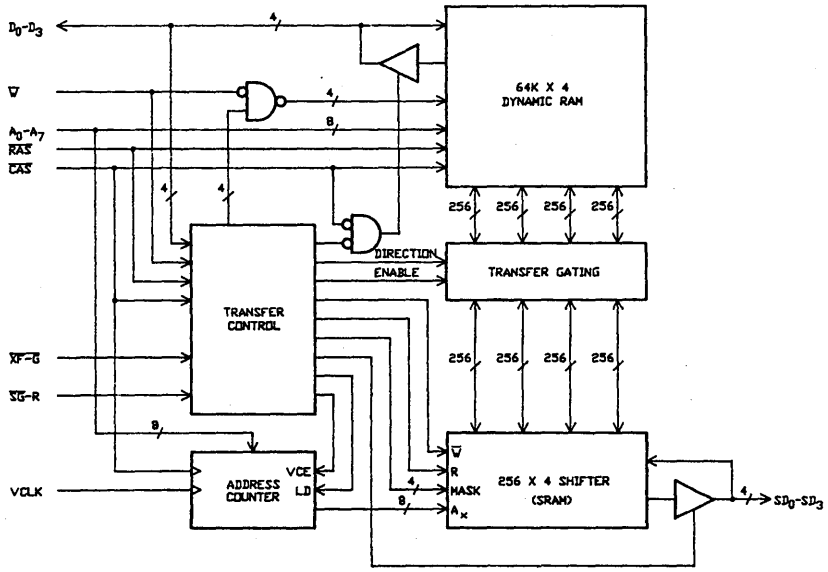
The Am90C644 is a fully decoded, high-speed, dual access 262,144-bit dynamic random-access memory fabricated on CMOS technology. The random-access port comprises a 64K x 4 DRAM array which operates independently from the sequential access port. The sequential access port has four 256-bit shift registers which can be accessed serially and independently from the DRAM. The interface between the DRAM array and the shifter is bi-directional, permitting transfers between the two.

The 64K x 4 DRAM array has an Enhanced Page Mode feature which permits cycle times as short as 70 ns. The Shifter is organized as a 256 x 4 static RAM with an 8-bit programmable Address Counter. This permits pixel-by-pixel resolution in graphics applications, thereby supporting smooth panning and windowing. The Shifter has a 25-MHz shift rate (equivalent to 100 Megapixel/second video rate) which is ideal for high-resolution screens.

The Am90C644 reduces device count in graphics applications and improves bus bandwidth while significantly increasing system performance. Although several of its features are well suited for video applications, the Am90C644 can also be used as a general-purpose memory in mainframes and minicomputers, as well as in peripherals such as printers.

All inputs and outputs are TTL-compatible. The device is assembled in a 24-pin, 400-mil wide Plastic DIP and operates from a single +5 V power supply.

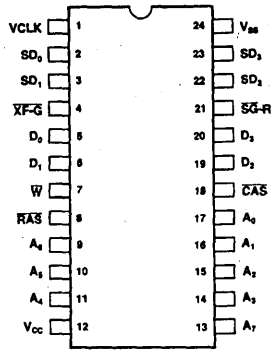
BLOCK DIAGRAM



BD005601

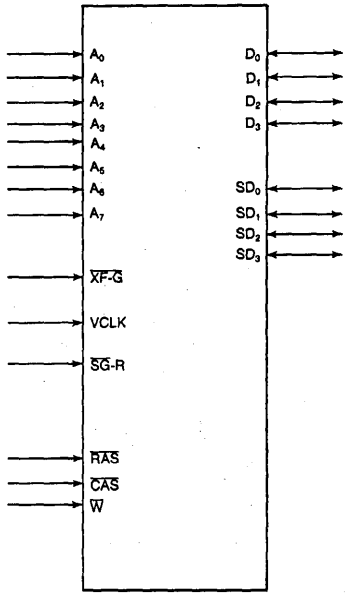
Publication # 07001 | Rev. B | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD008001

LOGIC SYMBOL



LS001981

PIN DESCRIPTION

$A_0 - A_7$ Addresses (Inputs, TTL)

The address pins are used to reference the desired location inside the DRAM. This 64K x 4 array requires sixteen address lines to access 65,536 locations, each of which contains four bits. Thus, the address inputs are time-multiplexed two ways. During the row address interval, as determined by the Row Address Strobe ($\overline{RAS}$), the eight address lines are interpreted by the device as a row address which selects one of 256 rows inside the device. The address lines are latched internally and then allowed to change to a column address. They are strobed (latched) into the device by the Column Address Strobe ($\overline{CAS}$), selecting one of 256 sets of four columns to be connected to the output circuitry. During a Transfer cycle, when data is transferred from the DRAM to the Shifter, or vice versa, the Shifter start address is loaded from the DRAM address lines into the internal Address Counters at the time of the falling edge of $\overline{CAS}$.

$\overline{RAS}$ Row Address Strobe (Input, TTL)

The Row Address Strobe serves three major functions. First, $\overline{RAS}$ performs the major chip enable function. On a HIGH-to-LOW transition of $\overline{RAS}$, the device changes from the standby power mode to the active mode. $\overline{RAS}$ must be LOW for at least the minimum specified interval, t_{RAS}, and must be HIGH for at least the minimum specified precharge time, t_{RP}. The precharge time is required to initialize the dynamic circuitry in the RAM. The second function that $\overline{RAS}$ performs is the latching of the row address from $A_0 - A_7$, the Reset or Write mask from $D_0 - D_3$, and the Transfer Control signals $\overline{W}$, $\overline{SG}$-R and $\overline{XF\text{-}G}$. $\overline{RAS}$ is used to initiate all DRAM memory cycles — Read/Write, Read-Modify-Write, Page Mode, Enhanced Page Mode, Transfer and Refresh. Thirdly, $\overline{RAS}$ terminates those control functions used only during a Transfer cycle on its LOW-to-HIGH transition at the end of the Transfer cycle.

$\overline{CAS}$ Column Address Strobe (Input, TTL)

The Column Address Strobe serves three major purposes. First, during a regular DRAM cycle, when $\overline{CAS}$ makes a HIGH-to-LOW transition, the column addresses that are present at the $A_0 - A_7$ inputs are latched into the chip. Secondly, during a Transfer cycle when data is transferred between the DRAM and the Shifter, $\overline{CAS}$ serves as the strobe to load the Shifter counter with the address on the $A_0 - A_7$ inputs. The Shifter Reset command and Read/Write command are also presented to the device on the falling edge of $\overline{CAS}$. Thirdly, $\overline{CAS}$ activates the outputs, serving as an Output Enable. Thus, cycles that are initiated by $\overline{RAS}$ and do not assert $\overline{CAS}$ leave the outputs in the high-impedance state. Further, following a specified period of time after $\overline{CAS}$ goes HIGH, the $D_0 - D_3$ outputs assume the high-impedance state.

$\overline{XF\text{-}G}$ Transfer/Output Enable (Input, TTL)

The Transfer/Output Enable input is a multifunction pin. When $\overline{XF\text{-}G}$ is LOW prior to the HIGH-to-LOW transition of $\overline{RAS}$, the execution of a Transfer cycle commences on that edge. $\overline{XF\text{-}G}$ behaves as an Output Enable except just before and just after the falling edge of $\overline{RAS}$. During a Read cycle when the $\overline{XF\text{-}G}$ line is LOW, the $D_0 - D_3$ output buffers are enabled (assuming $\overline{CAS}$ is LOW). If the $\overline{XF\text{-}G}$ line is HIGH at this time, then the $D_0 - D_3$ output buffers will be in their high-impedance state. If $\overline{XF\text{-}G}$ is HIGH at the HIGH-to-LOW transition of $\overline{RAS}$, a regular DRAM cycle is performed. In such a case, the $\overline{XF\text{-}G}$ line must go LOW, enabling the $D_0 - D_3$ outputs to perform a Read cycle.

$\overline{W}$ Write Enable (Input, TTL)

The Write Enable input is active-LOW. For regular DRAM cycles, $\overline{W}$ behaves in the same manner as for standard address-multiplexed DRAMs, except at the beginning of a Write cycle when the Write-per-Bit function is desired. $\overline{W}$ must be LOW prior to $\overline{RAS}$ going LOW to latch the Write mask on the falling edge of $\overline{RAS}$. When $\overline{W}$ is LOW prior to the HIGH-to-LOW transition of $\overline{CAS}$, an Early-Write cycle is performed. When $\overline{W}$ remains HIGH during that transition, a Read or Read-Modify-Write cycle is performed. $\overline{W}$ is time-multiplexed during Transfer cycles. When $\overline{RAS}$ makes a HIGH-to-LOW transition in a Transfer cycle, $\overline{W}$ determines the direction of data transfer between the DRAM and Shifter. When $\overline{W}$ is LOW during that transition, the data is transferred from the Shifter to the DRAM. When $\overline{W}$ is HIGH, data is transferred from the DRAM to the Shifter. When $\overline{CAS}$ makes a HIGH-to-LOW transition during a Transfer cycle, $\overline{W}$ is used to provide the Read or Write command for the Shifter. If $\overline{W}$ is HIGH during that transition, the Shifter will execute Read cycles until the next Transfer cycle where $\overline{W}$ is LOW during $\overline{CAS}$'s falling edge. If $\overline{W}$ is LOW during that transition, the Shifter will execute Write cycles until the next Transfer cycle where $\overline{W}$ is HIGH during $\overline{CAS}$'s falling edge.

$D_0 - D_3$ Bi-directional Data Lines (Input/Output, TTL, Three-state)

$D_0 - D_3$ are the data lines which data is read from or written to the DRAM. There is no binary significance to the four data lines. During normal DRAM Read cycles, data from the addressed location in the memory is available at the appropriate I/O pin as outputs, after sufficient response time has elapsed from the start of the cycle. Data is written into the DRAM on data lines where the Write mask contains a logic '1.' Writing is inhibited on data lines where the mask contains a logic '0.' During normal DRAM Write cycles, the Write mask is latched from the $D_0 - D_3$ lines on the falling edge of $\overline{RAS}$; the data to be written is then supplied on the $D_0 - D_3$ lines and is latched by the falling edge of $\overline{CAS}$ (for Early-Write cycles) or the falling edge of $\overline{W}$ (for Read/Write or Read-Modify-Write cycles). During Transfer cycles the $D_0 - D_3$ lines are used to input a data pattern that is to be written into the Shifter in a Reset cycle. This Reset mask is latched by the falling edge of $\overline{RAC}$ and remains valid until $\overline{RAC}$ goes HIGH at the end of a Reset cycle. For example, if D_1 is LOW in the Reset mask, all 256 locations of SD_1 in the Shifter will be reset to a LOW level when the Reset operation is performed.

The three-state condition of the $D_0 - D_3$ lines is controlled by various combinations of $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$ and $\overline{XF\text{-}G}$. For normal DRAM cycles ($\overline{XF\text{-}G}$ is HIGH when $\overline{RAS}$ goes LOW) the output buffers driving the $D_0 - D_3$ lines are in the high-impedance state except during a Read or Read-Modify-Write cycle. The output buffers are in the high-impedance state during a Transfer cycle and during an Early-Write cycle.

VCLK Video Clock (Input, TTL)

The Video Clock is a high-speed clock input used to increment the Address Counter and to synchronize the Shifter Write and Read operations. The minimum cycle time is the propagation delay through the Address Counter plus the Shifter SRAM access time. The Address Counter is incremented on the LOW-to-HIGH transition of VCLK. The initiation of a Transfer cycle must not occur at the same time as the rising edge of VCLK.

$\overline{SG}$-R Shifter Output Enable and Reset Control (Input, TTL)

The $\overline{SG}$-R pin accepts the buffer-enable signal for the Shifter outputs except when $\overline{CAS}$ goes LOW during a Transfer cycle. When LOW, $\overline{SG}$-R causes the buffers to assume a low-impedance state. When $\overline{SG}$-R is HIGH, the Shifter outputs are in the high-impedance state. The $\overline{SG}$-R line is used as the Shifter select line when Shifters are cascaded in a system.

During a Transfer cycle the signal on the $\overline{SG}$-R pin is interpreted as a Shifter Reset (active-HIGH). Thus, when $\overline{SG}$-R is HIGH, meeting the specified set-up and hold times, during the falling edge of $\overline{CAS}$, the SRAM is reset to a background state. That background state is defined by the Reset mask of four bits which is entered into the Reset mask latch via the $D_0 - D_3$ lines when $\overline{RAS}$ goes LOW during a DRAM-to-Shifter Transfer cycle.

$SD_0 - SD_3$ Bi-directional Shifter Data Lines (Input/Output, Three-state)

These four common I/O data lines are used to write and read data to and from the Shifter. Read or Write cycles are specified by the state of $\overline{W}$ when $\overline{CAS}$ makes a HIGH-to-LOW transition during a Transfer cycle. Changing from Read cycles to Write cycles or vice versa requires the execution of a Transfer cycle with $\overline{W}$ in the appropriate state when $\overline{CAS}$ makes that transition. The three-state condition of the output buffers is controlled by the $\overline{SG}$-R pin except during Transfer cycles when $SD_0 - SD_3$ are in the high-impedance state.

V_{CC} and V_{SS} Positive Power Supply and Ground

The V_{CC} supply is nominally +5 volts with respect to the V_{SS} pin which is connected to the system ground.

FUNCTIONAL DESCRIPTION

The Am90C644 is a composite read/write memory consisting of two arrays (see Block Diagram). The first is a 262,144-bit Dynamic Random-Access Memory (DRAM) configured as 65,536 four-bit words. The second is a high-speed serial Shifter consisting of a 256 x 4-bit static read/write memory with an on-chip, presettable Address Counter. These two memory arrays can operate independently to perform, screen refresh and display update, the two necessary memory functions of a bit-mapped graphics memory. Information is transferred between the two memory elements on command utilizing a Transfer cycle.

The DRAM element features a standard interface consisting of two control signals ($\overline{RAS}$ and $\overline{CAS}$), four common I/O data lines ($D_0 - D_3$), a write enable ($\overline{W}$) and eight time-multiplexed address lines ($A_0 - A_7$), all of which are TTL-compatible. The DRAM requires periodic refreshing of the data by accessing all 256 rows through the use of any $\overline{RAS}$ initiated cycle within 4 milliseconds.

The data to be loaded into the DRAM may be masked to select which memory bits are updated in a memory Write cycle. The Write mask is latched from the $D_0 - D_3$ lines on the falling edge of $\overline{RAS}$ while $\overline{W}$ is LOW. The mask is only updated on $\overline{RAS}$-initiated non-Transfer cycles.

The serial Shifter outputs four new data bits on each rising edge of the Video Clock (VCLK) except during Transfer cycles. The data rate of the Shifter is 25 MHz which permits a single-bit rate of 100 MHz, consistent with the needs of high-performance bit-mapped graphics and other scanning systems. Higher rates can be achieved by paralleling Shifters. Data is loaded into the Shifter from the DRAM when a Transfer cycle is performed. At the same time, the presettable Address Counter is parallel-loaded from the DRAM address lines at the falling edge of $\overline{CAS}$. The address loaded into the Address Counter serves as the start address for the shifting operation. Therefore, shifting can start at any arbitrary Shifter location, which provides support for smooth panning features, such as those in bit-mapped graphics systems. The Shifter can also be reset to a selectable background state to facilitate the clearing of a screen.

Functional descriptions of the key arrays in the Block Diagram are detailed as follows:

64K x 4 DRAM

The DRAM consists of a standard dynamic RAM with time-multiplexed addresses ($A_0 - A_7$), two address strokes ($\overline{RAS}$ and $\overline{CAS}$), a Write Enable ($\overline{W}$) and four bi-directional data lines ($D_0 - D_3$). A Write mask latch is provided that allows selected bits to be written from the $D_0 - D_3$ lines by gating the individual Write-Enable inputs to the DRAM via NAND gates. This latch is loaded from the $D_0 - D_3$ on the falling edge of $\overline{RAS}$ at the beginning of a Write cycle, while $\overline{W}$ is LOW. If $\overline{W}$ is HIGH as $\overline{RAS}$ falls, the Write mask is ignored and all four data bits are written during the Write cycle. Thus, the $D_0 - D_3$ lines are time-multiplexed during a Write cycle, carrying the Write mask on the falling edge of $\overline{RAS}$ and the data to be written on the falling edge of $\overline{CAS}$, or on the falling edge of $\overline{W}$ in a Read-Modify-Write cycle.

The DRAM array consists of 256 rows of 1024 bits per row. Refresh is done on a row-at-a-time basis where all 256 rows are refreshed in a single interval of 4 ms. The output buffers for the data lines are controlled by a combination of $\overline{RAS}$, $\overline{CAS}$ and $\overline{XF\text{-}G}$. If $\overline{XF\text{-}G}$ is LOW when $\overline{RAS}$ makes a HIGH-to-LOW transition, a Transfer cycle is initiated and the output buffers are disabled. If the converse is true, the Transfer Control logic allows $\overline{XF\text{-}G}$ to act as the enable signal for the output buffers. The buffers are enabled if $\overline{XF\text{-}G}$ is LOW and $\overline{CAS}$ is LOW.

Transfer Gating Logic

Each of the DRAM's bit lines is connected to the Transfer Gating logic. Data flows through the Transfer Gating logic between the DRAM and the Shifter when a Transfer cycle occurs. The direction of the data flow is determined by the state of the $\overline{W}$ line when $\overline{RAS}$ makes a HIGH-to-LOW transition during a Transfer cycle. When $\overline{W}$ is HIGH during that transition, the data flows from the DRAM to the Shifter. Data flows from the Shifter to the DRAM when $\overline{W}$ is LOW. The Transfer Gating logic is only enabled when $\overline{RAS}$ is LOW during a Transfer cycle.

Transfer Control Logic

The Transfer Control logic in the Am90C644 is used to modify the definitions of some of the pins and operations during a Transfer cycle. The pins that are affected are the $\overline{W}$, $\overline{SG}$-R, $\overline{XF\text{-}G}$, $D_0 - D_3$ and $A_0 - A_7$ pins. The $\overline{W}$ pin is time-multiplexed both during a Transfer cycle and a regular DRAM cycle. The $\overline{W}$ pin indicates the direction of transfer when $\overline{RAS}$ goes LOW during a Transfer cycle. When $\overline{CAS}$ goes LOW, the $\overline{W}$ pin indicates whether Read cycles ($\overline{W}$ = HIGH) or Write cycles ($\overline{W}$ = LOW) will be executed by the Shifter after completion of the Transfer cycle. A subsequent Transfer cycle is required to change the type of Shifter cycle to be performed.

The $\overline{SG}$-R signal determines whether a Reset cycle is to be executed during the DRAM-to-Shifter Transfer cycle. If $\overline{SG}$-R is HIGH when $\overline{CAS}$ goes LOW during the Transfer cycle, the Shifter will be reset to the background state specified by the data on the $D_0 - D_3$ lines (the Reset mask) when $\overline{RAS}$ went

LOW during that same Transfer cycle. The Reset mask is latched into the Transfer Control logic by the falling edge of $\overline{RAS}$ during a DRAM-to-Shifter Transfer cycle. If $\overline{SG}$-R is LOW, a Reset cycle will not be executed. Except during Transfer cycles, the $\overline{XF}$-$\overline{G}$ pin is used as the DRAM Output Enable. When $\overline{XF}$-$\overline{G}$ is LOW during regular cycles, the DRAM output buffers are enabled. When $\overline{XF}$-$\overline{G}$ is HIGH, the buffers are in the high-impedance state.

The Transfer Control logic provides the Video Clock Enable (VCE) signal. During Transfer cycles, the Video Clock (VCLK) is prevented from incrementing the Address Counter. The Transfer Control logic also provides the Address Counter Load command (LD) causing the data on the $A_0 - A_7$ lines to be loaded into the Address Counter in parallel on the falling edge of $\overline{CAS}$. Control signals for the transfer direction and transfer enable operations are also provided by the Transfer Control logic.

Shifter

The Shifter consists of a resettable 256 x 4 SRAM array, a parallel-loadable Address Counter, and four three-state, bi-directional output buffers. The output buffers are enabled when $\overline{SG}$-R is LOW during normal Shifter cycles and disabled (high-impedance state) when $\overline{SG}$-R is HIGH. The address inputs for the SRAM are supplied by the Address Counter. The SRAM inputs are connected to the Transfer Gating logic as described in the preceding section. The four data channels in the SRAM array are connected to the DRAM array such that picture elements (pixels), written to $D_0 - D_3$ in the DRAM array, appear at one SRAM address on $SD_0 - SD_3$. In other words, data written into the DRAM array on D_0, for example, will appear on SD_0 at the Shifter output (see Figure 1).

The Address Counter is a synchronous binary counter eight bits in length, parallel-loadable from the $A_0 - A_7$ inputs during a Transfer cycle on the falling edge of $\overline{CAS}$, and incremented by the rising edge of the Video Clock (VCLK). The data, at the address initially contained in the Address Counter, that is transferred from the DRAM to the Shifter in a Transfer cycle appears on the Shifter outputs, $SD_0 - SD_3$, prior to the first VCLK rising edge. One new 4-bit output occurs after each subsequent rising edge of VCLK. The Address Counter continues to count in a wraparound manner after reaching the all-1's state. This fall-through read feature allows data to be moved from the Shifter on one device to that on another without external logic.

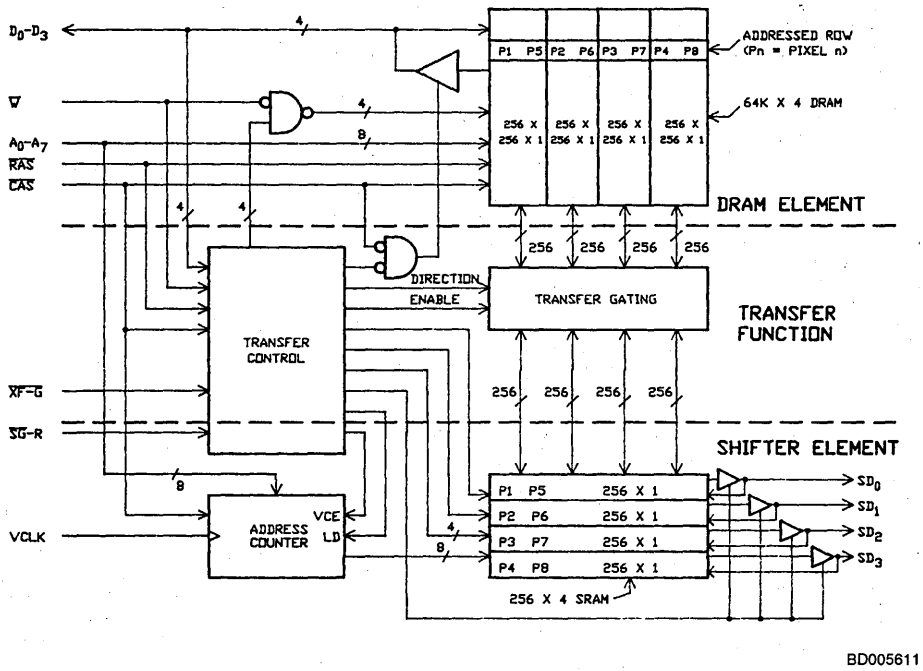


Figure 1. Pixel Address Mapping

APPLICATIONS

Operational Modes

The Am90C644 can be used in high-speed bit-mapped graphics systems where the graphics memory has two major functions: 1) screen refresh at nominal video rates and 2) display update where the memory interfaces to the graphics processor. The following description of the operating modes of the Am90C644 revolves around these two functions. The Transfer function permits communication between these two functions, which otherwise operate separately and independently.

Display Update

Operating the display update function resembles the normal use of any other dynamic RAM, with the exception of the Write-per-Bit function. The $\overline{XF}$-$\overline{G}$ input is HIGH during the

HIGH-to-LOW transition of $\overline{RAS}$ to allow display update access to the Video DRAM. In this case, the DRAM is organized with 65,536 4-bit words. Data can be written to the DRAM up to four bits at a time using an Early-Write cycle, a Read/Write or Read-Modify-Write cycle, or a Page-Mode Write or Enhanced-Page-Mode Write cycle. At the beginning of the Write cycle the Write mask is latched from the input lines. The Write mask determines which of the four data inputs, $D_0 - D_3$, are written to the DRAM during that cycle. For Write cycles not initiated by the falling edge of $\overline{RAS}$ (e.g., Page-Mode or Enhanced-Page Mode cycles), the Write mask cannot be changed from the previous value set on the last falling edge of $\overline{RAS}$ when $\overline{W}$ was LOW. All DRAM cycles are initiated by the falling edge of $\overline{RAS}$. The row addresses are latched at this time. Also, during a Write cycle the Write mask is read from the data input lines if $\overline{W}$ is LOW at the time $\overline{RAS}$ goes LOW. Following the row-address-hold interval, the system is permitted to change the addresses to a valid column address which is read from the address inputs and latched by the falling edge of $\overline{CAS}$. Following the column-address-hold interval, the addresses are again free to change. This sequence is followed for all DRAM cycles except the chip Refresh cycle (not to be confused with the screen refresh discussed later), which requires no column address or $\overline{CAS}$ signals. In Page Mode and Enhanced Page Mode cycles, multiple column addresses can be entered and the corresponding data read or written by asserting multiple $\overline{CAS}$ pulses while $\overline{RAS}$ is still LOW. An Early-Write cycle occurs when the Write Enable ($\overline{W}$) signal goes LOW prior to the falling edge of $\overline{CAS}$. In this mode the DRAM produces an internal Write signal corresponding to the $\overline{CAS}$ signal. The output buffers remain in the high-impedance state, and the data on the input lines ($D_0 - D_3$) is loaded into the chip on the falling edge (HIGH-to-LOW transition) of $\overline{CAS}$.

In a Read/Write cycle, data is read from the currently addressed location in the DRAM after which new data is written into the same location. In a Read-Modify-Write cycle, data is first read from the currently addressed location, modified and rewritten into the same location. Read/Write and Read-Modify-Write take place within a single memory cycle. The data is set up and held with respect to the falling edge of $\overline{W}$. The $\overline{XF\text{-}G}$ signal, in its output enable mode, can assist in the timing of the Read/Write cycle by disabling the output buffers at the appropriate time. External latches will be needed to execute a Read-Modify-Write cycle since the Data Lines ($D_0 - D_3$) are used for both inputs and outputs. The various types of Write cycles are terminated in the same fashion as all other cycles when $\overline{RAS}$ goes HIGH. A minimum specified precharge interval is required before a new cycle can be initiated.

Data is retrieved from the DRAM by using a Read cycle which is initiated by the falling edge of $\overline{RAS}$. The same sequence of signals occurs for the Read cycle as for the Write cycles, except that the $\overline{W}$ signal remains HIGH throughout the cycle and $\overline{XF\text{-}G}$ is used to enable the output. Data appears at the output pins ($D_0 - D_3$) no later than the specified $\overline{RAS}$ access time or the $\overline{CAS}$ access time, whichever is later. The Read cycle terminates in the same manner as the Write cycle, (ie., when $\overline{RAS}$ goes HIGH). Page-Mode and Enhanced-Page-Mode Read cycles are also permitted, as shown in the Switching Characteristics section.

The data in the DRAM element needs periodic refreshing to prevent data loss. Refreshing is accomplished by using any $\overline{RAS}$-initiated cycle, including a $\overline{RAS}$-Only Refresh cycle, for each of the 256 rows of cells in the DRAM array within the specified refresh interval (4 ms). If refreshing is the only object of a given cycle, column addresses need not be valid. The refresh operation requires about 3% or less of the display update bandwidth and is usually controlled by the graphics processor.

Screen Refresh

The Shifter element is used for the screen refresh function. Data from the DRAM element is transferred to and from the Shifter element during a Transfer cycle as explained in the Transfer function description. The Shifter presents data to the four output buffers and to the off-chip environment on the Shifter Data pins ($SD_0 - SD_3$) during a Shifter Read cycle. Read cycles are specified if the $\overline{W}$ line is HIGH when $\overline{CAS}$ goes LOW during a Transfer cycle. Following a a Transfer cycle, the data presented during the subsequent Shifter Read cycles is stored in the SRAM at the location pointed to by the Address Counter. A new Shifter Read cycle is initiated when the Address Counter is incremented by a LOW-to-HIGH transition of VCLK. The maximum specified frequency of the VCLK input is 25 MHz. Since four bits are presented in parallel, the pixel rate out is up to 100 MHz for stripe mapping. Stripe mapping is so called because one memory location holds a number of bits each representing one attribute of a number of adjacent pixels which map to a stripe on the screen. External serialization of the data is then required to supply data for refreshing the screen. In point mapping, each of the four bits is an attribute of a single pixel, thus requiring no external serialization. The dot clock in this case would be limited to 25 MHz. The first Read cycle occurs without the need for a VCLK transition. The data stored at the address initially loaded into the Address Counter is passed directly through to the $SD_0 - SD_3$ as part of the Transfer cycle operation. This feature allows data to be transferred from the Shifter on one device to that on another without external logic.

Data can also be loaded into the Shifter from the outside environment through the use of a Shifter Write cycle. The writing operation is specified if $\overline{W}$ is LOW when $\overline{CAS}$ goes LOW during a Transfer cycle. The data on $SD_0 - SD_3$ is written into the Shifter at the address contained in the Address Counter on the rising edges of VCLK until the Write command is cancelled by a subsequent Transfer cycle. Note that when cascading Shifters and transferring data from one Shifter to another, the source Shifter is in the Read mode, and the destination Shifter is in the Write mode. Two Transfer cycles are required to set up this configuration with only the appropriate $\overline{RAS}$ active for each. Since data falls directly through to the Shifter outputs for the Read operation and is not written into the destination Shifter until the first VCLK transition, the Shifters can be directly cascaded. Data must meet specified set-up and hold times with respect to the VCLK transition.

A parallel Reset function allows the SRAM to be cleared to a background state to facilitate the rapid resetting of the entire display. If $\overline{SG}$-R is HIGH when $\overline{CAS}$ goes LOW during a DRAM-to-Shifter Transfer cycle, the Shifter is reset according to the Reset mask which is stored in the Reset mask latch. The Reset cycle ends on the rising edge of $\overline{RAS}$ at the end of the DRAM-to-Shifter Transfer cycle. The screen is then reset by simply executing Shifter Read cycles. Once the Reset mask latch has been loaded, the entire display memory can be rapidly reset by executing a sufficient number of Transfer cycles with $\overline{W}$ in the LOW state during the falling edge of $\overline{RAS}$.

Transfer Function

Data moves between the DRAM element and the Shifter through the use of a Transfer cycle. A Transfer cycle is initiated when $\overline{RAS}$ makes a HIGH-to-LOW transition and $\overline{XF\text{-}G}$ is LOW. During a Transfer cycle the Row addresses are interpreted on the falling edge of $\overline{RAS}$ as the Row address to or from which the data transfers take place. During the Transfer cycle the column addresses are interpreted as the data to be loaded into the Address Counter on the falling edge

of $\overline{CAS}$. The $D_0 - D_3$ lines are used to input data to the Reset mask latch in preparation for resetting the Shifter. This data is loaded on the falling edge of $\overline{RAS}$, during a DRAM-to-Shifter Transfer cycle, whether or not a Reset cycle is desired. As discussed above, the Reset command is given by the $\overline{SG}$-R input when $\overline{CAS}$ goes LOW. The output buffers connected to the $D_0 - D_3$ remain in the high-impedance state during the entire Transfer cycle.

The direction in which the data moves between the DRAM element and the Shifter element is determined by the $\overline{W}$ line when $\overline{RAS}$ goes LOW during a Transfer cycle. If the $\overline{W}$ line is LOW during that transition the data moves from the Shifter to the DRAM. If $\overline{W}$ is HIGH, the data moves from the DRAM to the Shifter.

When data is written to the DRAM, each of the Data Input lines is connected to a 64K x 1 section (see example in Figure 1). Thus, at a given row and column address, four data bits are written into four sections of the 64K x 4 DRAM element. When data is transferred to the Shifter, only a row address is specified. The 256 bits (one per column) in each section are loaded into the 256 locations in each of the corresponding sections of the SRAM. Thus, for a given SRAM address (contained in the Address Counter), one bit from each of the four DRAM sections is presented at the four Shifter Data lines ($SD_0 - SD_3$) in parallel. In other words, a pixel written into the DRAM on Data Input D_1 will appear on SD_1 of the Shifter at the SRAM address which corresponds to the DRAM column address at which the data was written. This mapping structure allows the video data to be serialized externally and presented to the screen such that adjacent pixels on the graphics-processor data bus are also adjacent pixels on the screen.

Bit-Map Graphics Application

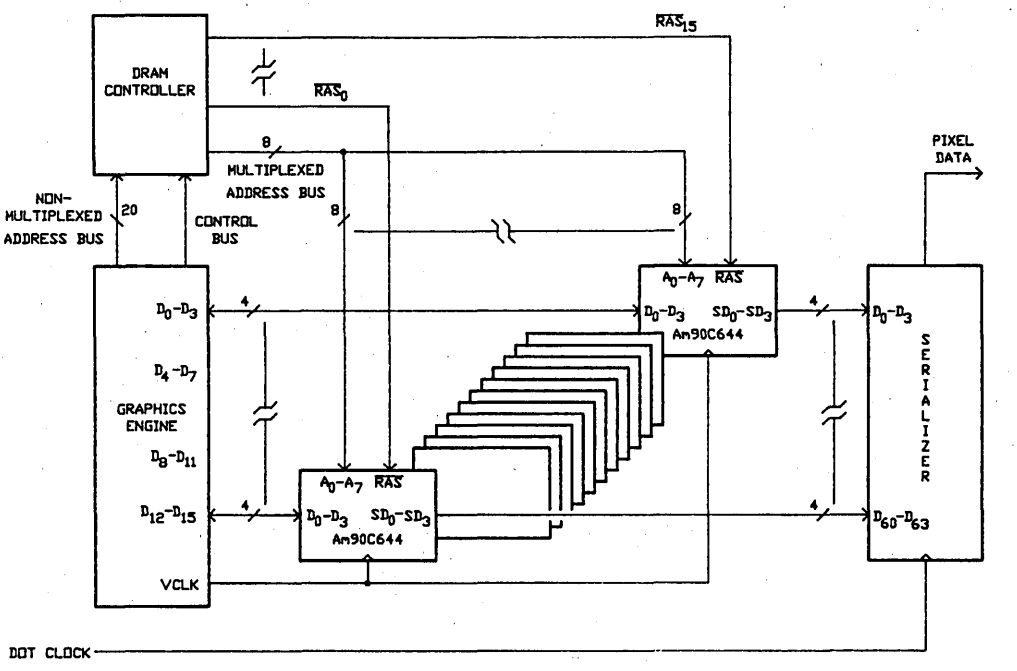
The following applications discussion centers around the use of the Am90C644 in bit-mapped graphics terminal.

For the following example, assume that the graphics subsystem is controlled by a Graphics Engine. The screen is 1024 x 1024 pixels, the display memory is 2048 x 2048, and the screen display is composed of stripes with a width of 64 pixels and a height of one scan line (linear architecture). In this simplified example, the aspect ratio of the screen is assumed to be square. More realistically, the aspect ratio is four-to-three. Figure 2 is a simplified block diagram of an Am90C644-based graphics display memory architecture. In this example, no hardware windows are supported. The Graphics Engine is used to compute the pertinent addresses for the start of the screen display. This system supports horizontal panning on a pixel-by-pixel basis in point mapping architecture because the Shifter consists of a RAM and an Address Counter rather than a shift register. In stripe mapped applications, a similar structure may also be required for the external serializer to support pixel-by-pixel panning. Generally the Transfer cycles will be timed to occur during the horizontal blanking interval of the display.

The Shifter Read operation will be interrupted to permit the Transfer cycle which loads the configuration of the next screen scan line into the dual-port, Video DRAM. The Graphics Engine selects the nature of the Shifter cycle (whether the Shifter is to be reset to a background pattern) and the type of pattern. The DRAM Controller block shown in Figure 2 performs the address multiplexing, DRAM refresh, DRAM clock driving and timing functions for the Graphics Engine. This interface is a standard DRAM interface, similar to that of the Am9064, 64K x 1 DRAM. The Am90C644 supports an Enhanced Page Mode not found on the the 64K DRAM. This access method is similar to Page Mode with considerably higher performance. The Graphics Engine also supplies the data for the display memory and the necessary control functions for the DRAM Controller, such as the latch enable, the mode controls and the cycle start signals (see Figure 3). In our current example, suppose that a Shifter Read function is desired. The screen start address will be loaded into the Address Counter from the Am90C644 Address inputs by the falling edge of $\overline{CAS}$. When the VCLK signal resumes the scanning process, the SRAM will present sequential nibbles of the scan line pixels for external serialization on the $SD_0 - SD_3$ lines starting at the address initially in the Address Counter. The first VCLK rising edge upon resuming the scanning operation will increment the Address Counter to START + 1, and the second nibble will follow. The subsystem of Figure 2 uses sixteen Am90C644s in parallel, supplying 64 pixels at a time. As a result, four scan lines of 1024 pixels each can be transferred in one Transfer cycle. If the required dot rate is 100 MHz, the VCLK signal rate is about 1.56 MHz, well within the specified upper limit of 25 MHz. Since several microseconds are allotted for horizontal blanking, the Graphics Engine has sufficient time to execute one or more Transfer cycles of 190 ns each.

If hardware windows are desired, the Am90C644 can be easily configured to support this feature. If the display needs to start a window at another arbitrary address (refer again to Figure 2), the Graphics Engine merely executes a Transfer cycle at that time to reconfigure the Video DRAM. The mid-line Transfer cycle reloads the Address Counter with an initial value corresponding to the window offset from the start of the scan line. The SRAM is also loaded with the window data at the appropriate address. The external serializer will need to contain some elastic buffering (FIFO) to smooth out the timing anomaly caused by the mid-line Transfer cycle. In multi-bank systems the selection between the banks for the scanning operation is done by using the $\overline{SG}$-R signal, which is supplied by the Graphics Engine as a high-order address. More than one hardware window is generally not required since, even in multi-window systems, usually only one is active at any given time.

Display update operations are handled in the same manner as for any other DRAM. After the Am90C644 is initiated, the Graphics Engine may begin loading the display memory for subsequent scanning for screen display. The Dynamic Memory Controller, the Am2968 in this example, controls the refresh address, but the Graphics Engine or a separate Timing Controller is required to handle the timing control along with the Am2971 Programmable Event Generator, used here as a timing reference.



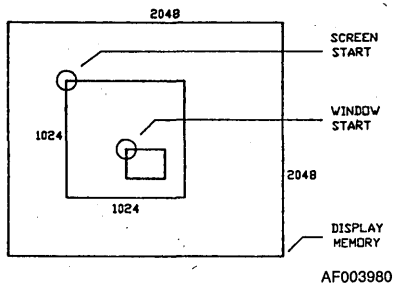
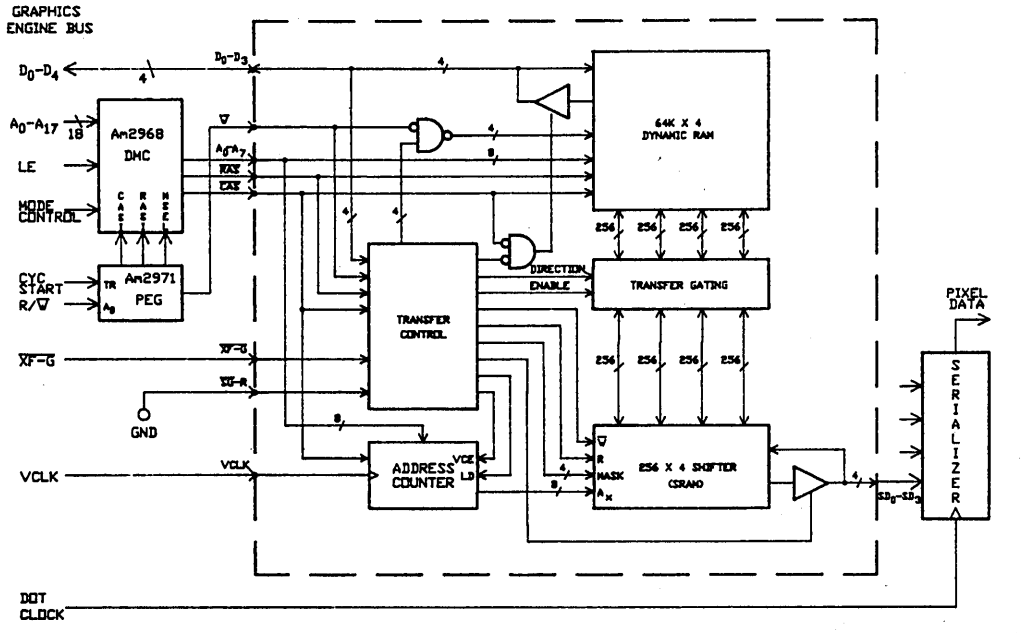


Figure 2. Graphics Display Memory Architecture



BD005631

Figure 3. Interface Detail

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ...−10 to +80°C
Voltage on Any Pin Relative to Ground
(except Vcc) .....−2 to +7.5 V
Voltage on Vcc Supply Relative to Ground ..−1 to +7.5 V
DC Output Short Circuit Current.....50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A).....0 to +70°C
Supply Voltage (V_{CC}) .....+4.5 to +5.5 V
Input HIGH Voltage (V_{IH}) .....+2.4 to V_{CC} + 1 V
Input LOW Voltage (V_{IL}) .....−2.0 to +0.8 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

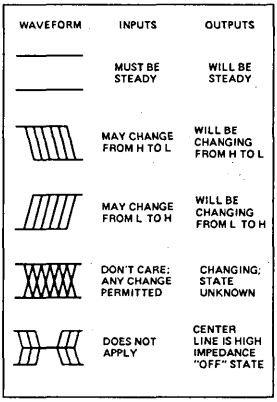
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −5.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.2 mA	0.4		V
V_{IH}	Input HIGH Voltage	0°C ≤ T_A ≤ 70°C	2.4	V_{CC} + 1	V
V_{IL}	Input LOW Voltage		−2.0	+0.8	V
I_{CC1}	Average Operating Power Supply Current w/o Shifter (Note 1)	$\overline{RAS}$, $\overline{CAS}$ cycling at Min. cycle time		70	mA
I_{CC2}	Average Operating Power Supply Current with Shifter Operating (Note 1)	$\overline{RAS}$, $\overline{CAS}$, VCLK cycling at Min. cycle time		90	mA
I_{CC3}	Standby Power Supply Current w/o Shifter	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} VCLK = V_{IL}		12	mA
I_{CC4}	Standby Power Supply Current with Shifter (Note 1)	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} VCLK cycling at Min. cycle time		32	mA
I_{CC5}	Average Power Supply Current during Refresh w/o Shifter (Note 1)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}		60	mA
I_{CC6}	Average Power Supply Current during Refresh with Shifter (Note 1)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, VCLK cycling		80	mA
I_{CC7}	Average Power Supply Current in Page Mode w/o Shifter (Note 1)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling		50	mA
I_{CC8}	Average Power Supply Current in Page Mode with Shifter (Note 1)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, VCLK cycling		70	mA
I_{CC9}	Average Power Supply Current in Enhanced Page Mode with Shifter (Note 1)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, VCLK cycling		110	mA
I_{CC10}	Average Power Supply Current in Enhanced Page Mode w/o Shifter (Note 1)	$\overline{RAS}$, VCLK = V_{IL} $\overline{CAS}$ cycling		90	mA
I_{CC11}	Average Power Supply Current in Data Transfer cycle w/o Shifter (Note 1)	$\overline{RAS}$, $\overline{CAS}$ cycling at Min. cycle time VCLK = V_{IL}		90	mA
I_{CC12}	Average Power Supply Current in Data Transfer cycle with Shifter (Note 1)	$\overline{RAS}$, $\overline{CAS}$, VCLK cycling at Min. cycle time		110	mA
$I_{I(L)}$	Input Leakage Current	All inputs except D_n, SD_n, V_{SS} ≤ V_{IN} ≤ V_{CC}	−10	+10	uA
I_{BLK}	Data Line Leakage Current	Outputs disabled V_{SS} ≤ V_{IN} ≤ V_{CC}	−10	+10	uA

CAPACITANCE: (Note 2)

Parameter Symbol	Parameter Description	Max.	Units
C_{IN1}	Input Capacitance, Except Clocks, $\overline{W}$	5	pF
C_{IN2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, VCLK	8	pF
C_D	Data Line Capacitance (D_n, SD_n)	7	pF

Notes: See notes following Switching Characteristics table.

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, & 5)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
READ OR WRITE CYCLES					
01	t_{RAC}	Access Time from $\overline{RAS}$ (Notes 5 & 6)		100	ns
02	t_{CAC}	Access Time from $\overline{CAS}$ (Notes 5 & 6)		30	ns
03	t_{REF}	Refresh Interval		4	ms
04	t_{RP}	$\overline{RAS}$ Precharge Time	80		ns
05	t_{CPN}	$\overline{CAS}$ Precharge Time (non-Page Mode)	25		ns
06	t_{CRP}	$\overline{CAS}$–$\overline{RAS}$ Precharge Time	20		ns
07	t_{RCD}	$\overline{RAS}$–to–$\overline{CAS}$ Delay Time (Notes 5, 6 & 7)	25	70	ns
08	t_{RSH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$	55		ns
09	t_{CSH}	$\overline{CAS}$ Hold Time from $\overline{RAS}$	100		ns
10	t_{ASR}	Row Address Setup Time	0		ns
11	t_{RAH}	Row Address Hold Time	15		ns
12	t_{ASC}	Column Address Setup Time	0		ns
13	t_{CAH}	Column Address Hold Time	20		ns
14	t_T	Rise or Fall Times	3	50	ns
15	t_{OFF}	D_n Buffer Turn-off ($\overline{CAS}$) (Note 8)	0	20	ns
16	t_{OEZ}	D_n Buffer Turn-off ($\overline{XF}$-$\overline{G}$)	0	15	ns
17	t_{OE}	D_n Buffer Turn-on ($\overline{XF}$-$\overline{G}$)		30	ns
READ AND REFRESH CYCLES					
18	t_{RC}	Random Read or Write Cycle	190		ns
19	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75,000	ns
20	t_{CAS}	$\overline{CAS}$ Pulse Width	30	75,000	ns
21	t_{RCS}	Read Command Setup Time	0		ns
22	t_{RCH}	Read Command Hold ($\overline{CAS}$) (Note 9)	0		ns
23	t_{RRH}	Read Command Hold ($\overline{RAS}$) (Note 9)	0		ns
24	t_{OEP}	$\overline{XF}$-$\overline{G}$ Pulse Width	30		ns

SWITCHING CHARACTERISTICS (Cont.)

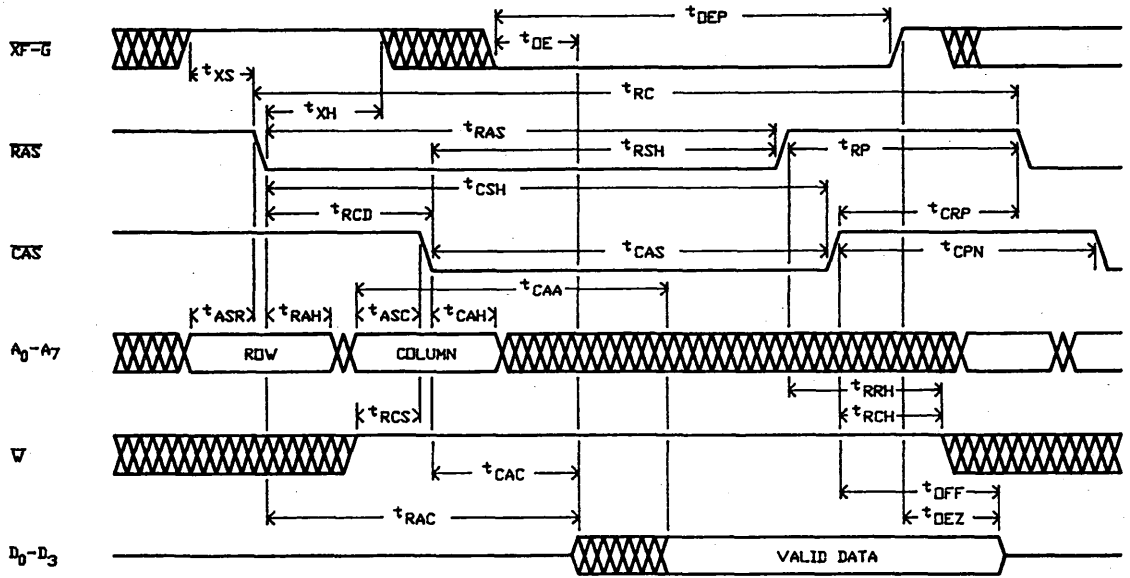
No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
WRITE CYCLE					
25	t_{WCS}	Write Command Setup Time (Note 10)	0		ns
26	t_{WCH}	Write Command Hold Time	20		ns
27	t_{WP}	Write Pulse Width	20		ns
28	t_{DS}	Data Setup Time (Note 11)	0		ns
29	t_{DH}	Data Hold Time (Note 11)	20		ns
30	t_{OEH}	$\overline{XF\text{-}G}$ HIGH Hold from $\overline{W}$ LOW	30		ns
31	t_{WBS}	Write-per-Bit Command Setup Time	0		ns
32	t_{WBH}	Write-per-Bit Command Hold Time	20		ns
33	t_{WMS}	Write Mask Setup Time	0		ns
34	t_{WMH}	Write Mask Hold Time	15		ns
READ-MODIFY-WRITE CYCLE					
35	t_{RWC}	Read-Modify-Write (RMW) Cycle	240		ns
36	t_{RWL}	Write-to-$\overline{RAS}$ Lead Time	30		ns
37	t_{CWL}	Write-to-$\overline{CAS}$ Lead Time	30		ns
38	t_{RWD}	$\overline{RAS}$-to-Write Enable Delay (Note 10)	115		ns
39	t_{CWD}	$\overline{CAS}$-to-Write Enable Delay (Note 10)	45		ns
40	t_{XDD}	$\overline{XF\text{-}G}$ HIGH-to-Data Setup	15		ns
41	t_{XWS}	$\overline{XF\text{-}G}$ HIGH-to-$\overline{W}$ Setup	15		ns
42	t_{AWD}	Column Address-to-$\overline{W}$ Delay Time (Note 10)	65		ns
ENHANCED PAGE MODE					
43	t_{PC}	Enhanced Page Mode Cycle Time	70		ns
44	t_{PRWM}	Enhanced Page Mode RMW Cycle	100		ns
45	t_{CP}	$\overline{CAS}$ Precharge Time (Enhanced Page Mode)	10		ns
46	t_{CAA}	Address-to-Data-Out Valid		50	ns
47	t_{WCS}	$\overline{CAS}$-to-$\overline{W}$ Setup Time	0		ns
TRANSFER CYCLE					
48	t_{XH}	Transfer Hold Time	20		ns
49	t_{XS}	Transfer Setup Time	0		ns
50	t_{CS}	Command Setup Time	0		ns
51	t_{CH}	Command Hold Time	15		ns
52	t_{WS}	Transfer Direction Setup	0		ns
53	t_{WH}	Transfer Direction Hold	15		ns
54	t_{XC}	Transfer Cycle Time	190		ns
55	t_{VCS}	Video Clock Set-up Time to $\overline{RAS}$	0		ns
56	t_{RQZ}	$\overline{RAS}$-to-Serial Out High-Z	10	40	ns
57	t_{RS}	Reset Setup-to-$\overline{CAS}$	0		ns
58	t_{RH}	Reset Hold-from-$\overline{CAS}$	15		ns
59	t_{RSAC}	$\overline{RAS}$-to-Serial Data Access	115	140	ns
60	t_{CSAC}	$\overline{CAS}$-to-Serial Data Access	70	95	ns
61	t_{XR}	Transfer Recovery Time	10	40	ns
62	t_{VHR}	Video Clock Hold-from-$\overline{RAS}$	60		ns

SWITCHING CHARACTERISTICS (Cont.)

No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
SHIFTER CYCLES					
63	t_{VCYC}	Video Clock Cycle Time	40		ns
64	t_{VCLKH}	Video Clock HIGH Time	10		ns
65	t_{VCLKL}	Video Clock LOW Time	10		ns
66	t_{KQ}	Video Clock-to-Data Out Delay	5	35	ns
67	t_{SOE}	$\overline{SG}$ LOW-to-Output Low-Z	0	15	ns
68	t_{SOZ}	$\overline{SG}$ HIGH-to-Output High-Z		15	ns
69	t_{SDS}	Shifter Data Setup Time	10		ns
70	t_{SDH}	Shifter Data Hold Time	20		ns
71	t_{VOH}	Serial Output Hold after Video Clock High	3		ns
72	t_{SEP}	$\overline{SG}$-R Pulse Width	10		ns
73	t_{SOP}	$\overline{SG}$-R Precharge Time	10		ns

Notes:
1. I_{CC} is dependent on output loading and cycle times. Specified values are with outputs open.
2. Capacitance is measured with a Boonton Meter or calculated from the equation $C = I\ (\Delta t)/(\Delta V)$, at $T_A = +25°C$, $V_{CC} = 5.0$ V, $f = 1$ MHz.
3. An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring the timing of input signals. Also, transition times are measured between these two levels. Timing Parameters assume $t_T = 5$ ns.
5. Maximum t_{RCD} is specified as a reference level only. If $t_{RCD} \leq$ Max. allowed, access time is t_{RAC}. If $t_{RCD} > t_{RCD}$(Max.), either access time is controlled exclusively by t_{CAC} or t_{RAC} and will increase by the amount that t_{RCD} exceeds the specified maximum.
6. Output load is equivalent to two standard TTL loads and 100 pF.
7. $t_{RCD}(Min.) = t_{RAH} + t_{ASC} + 2t_T$.
8. t_{OFF}(Max.) defines the time at which the outputs assume the open-circuit condition and is not referenced to output voltage levels.
9. Either t_{RRH} or t_{RCH} and t_{AWD} must be satisfied for a Read cycle.
10. t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are specified as reference points and are not restrictive operating parameters.
11. These parameters are referenced to the leading edge of $\overline{CAS}$ in Early-Write cycles and to the leading edge of W in Delayed-Write or Read-Modify-Write cycles.
12. Positive, non-zero setup time permits a shorter t_{RAH}.

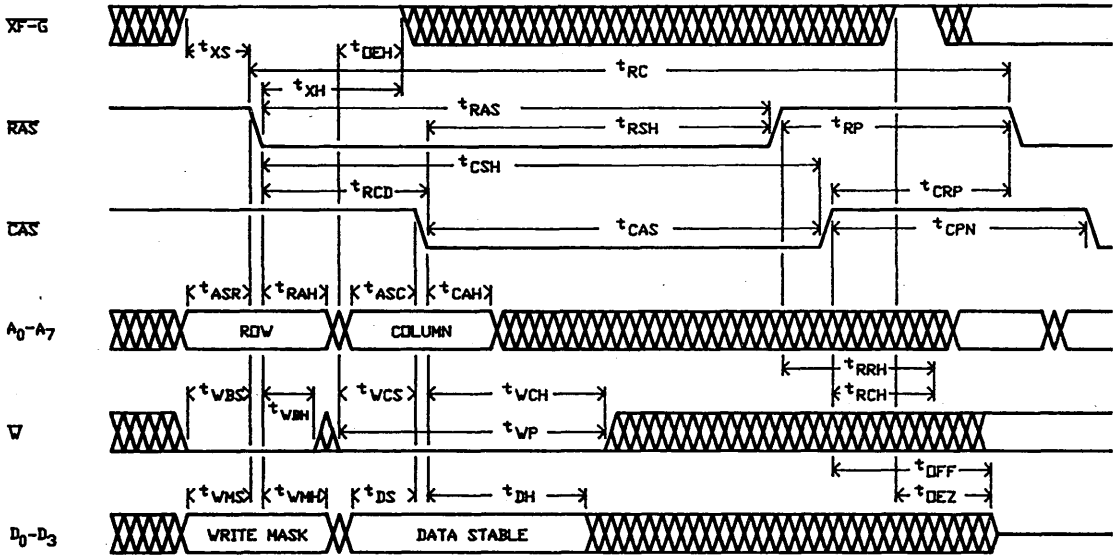
SWITCHING WAVEFORMS (Cont'd.)



WF010892

Read Cycle

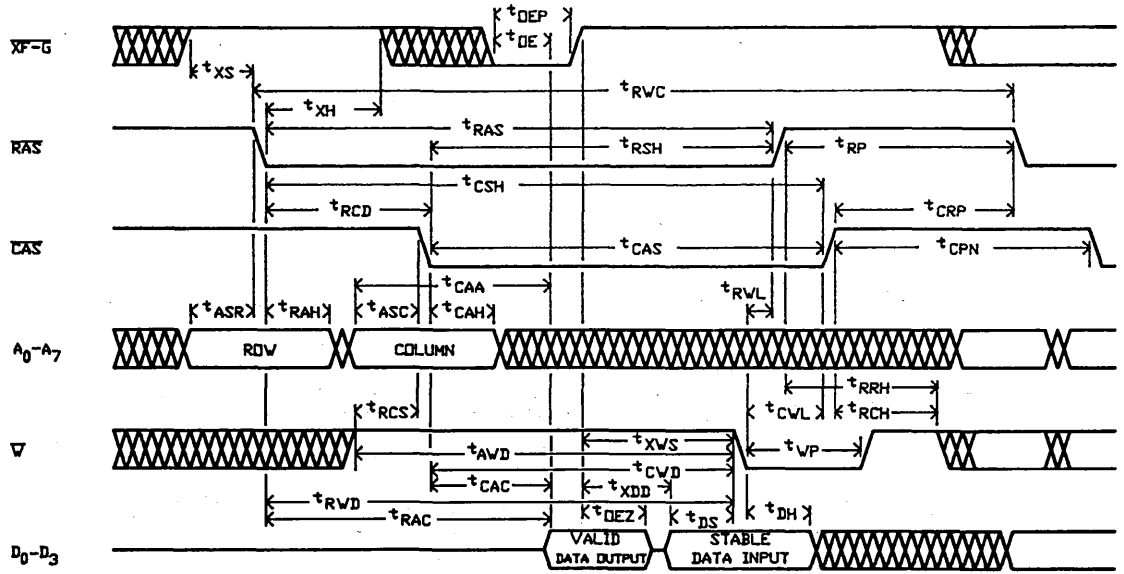
SWITCHING WAVEFORMS



WF010902

Write Cycle

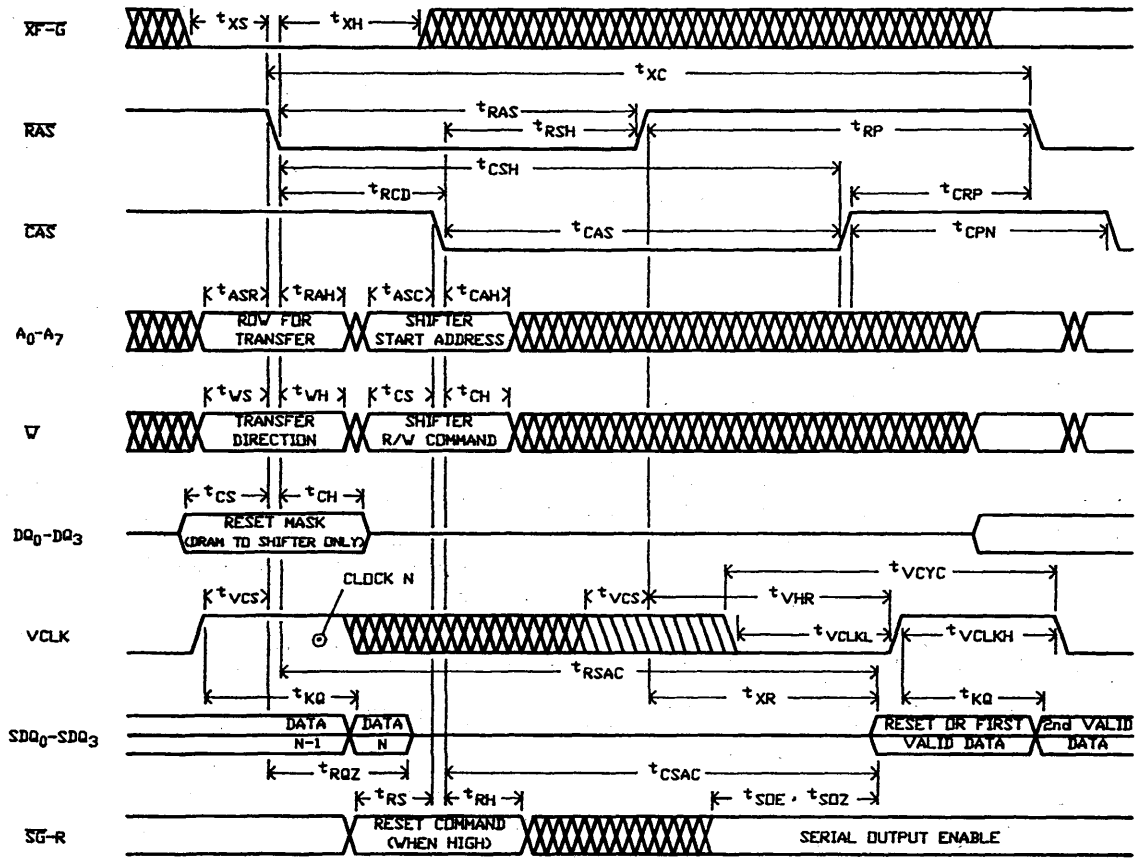
SWITCHING WAVEFORMS (Cont'd.)



WF022030

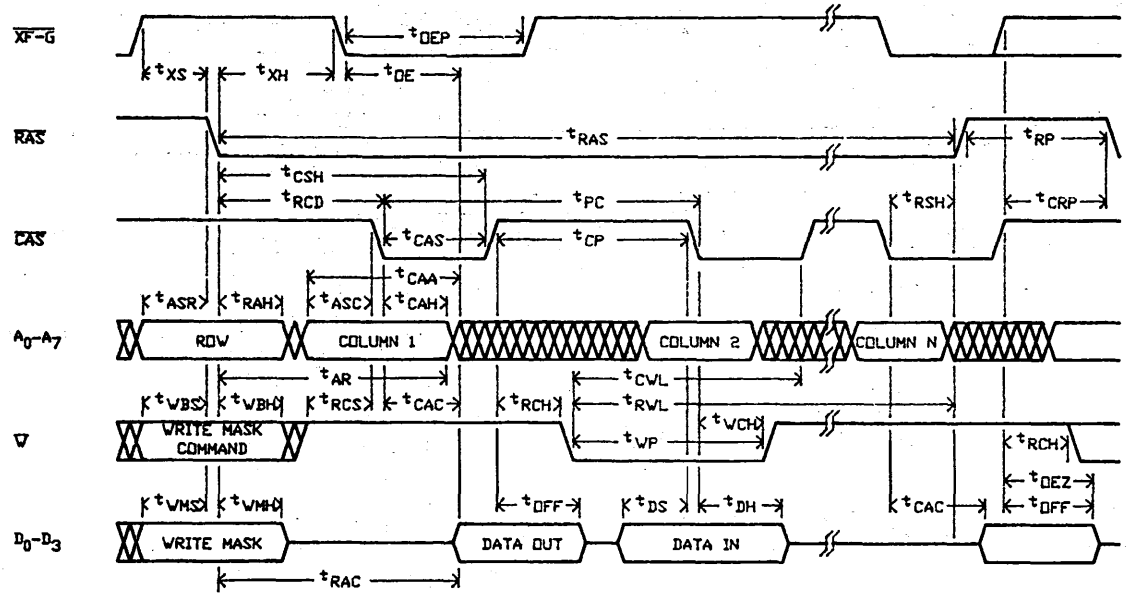
Read-Modify-Write Cycle

SWITCHING WAVEFORMS



WF010922

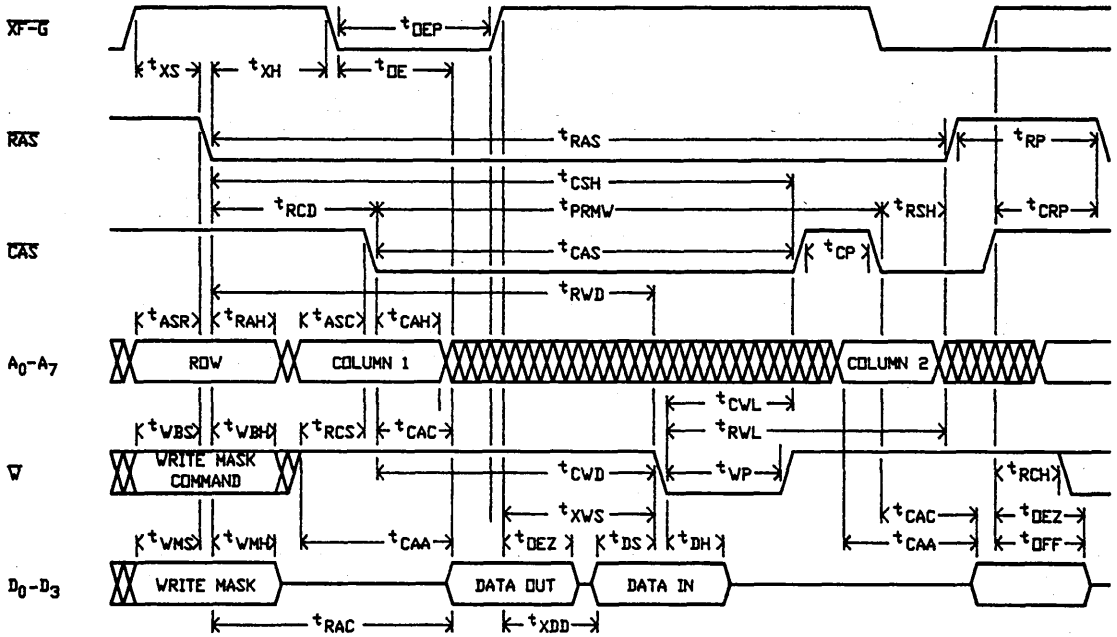
Transfer Cycle



WF010932

Enhanced Page Mode — Read and $\overline{CAS}$-Controlled Write Cycles

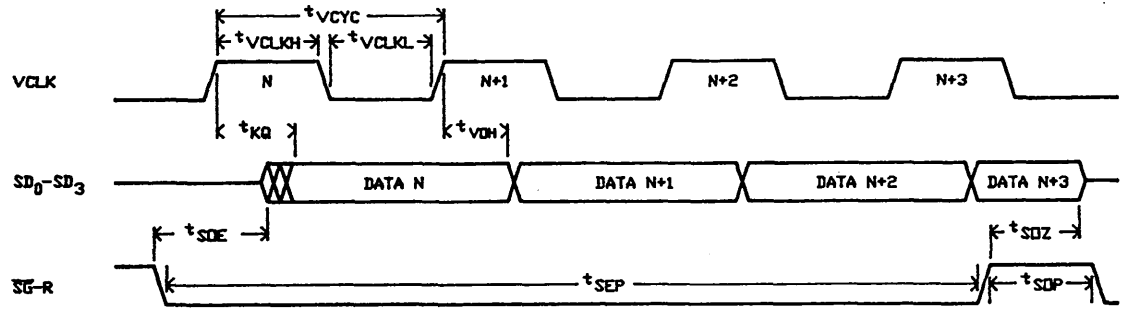
SWITCHING WAVEFORMS



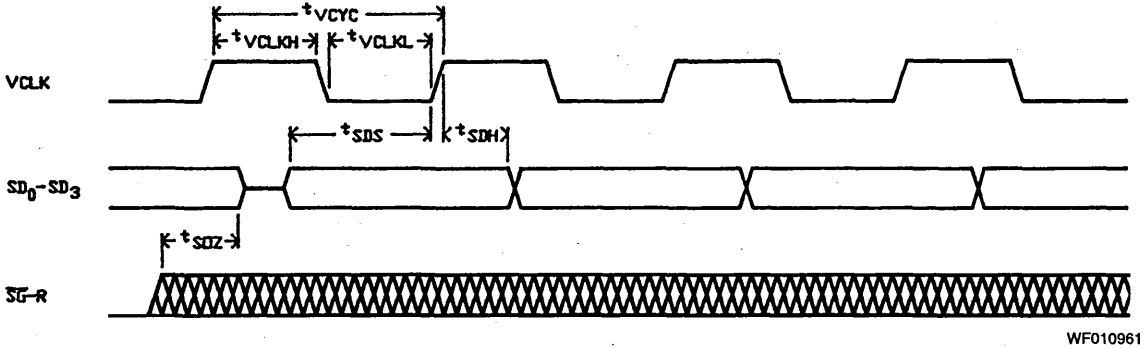
WF022041

Enhanced Page Mode — Read-Modify-Write Cycles

SWITCHING WAVEFORMS (Cont'd.)

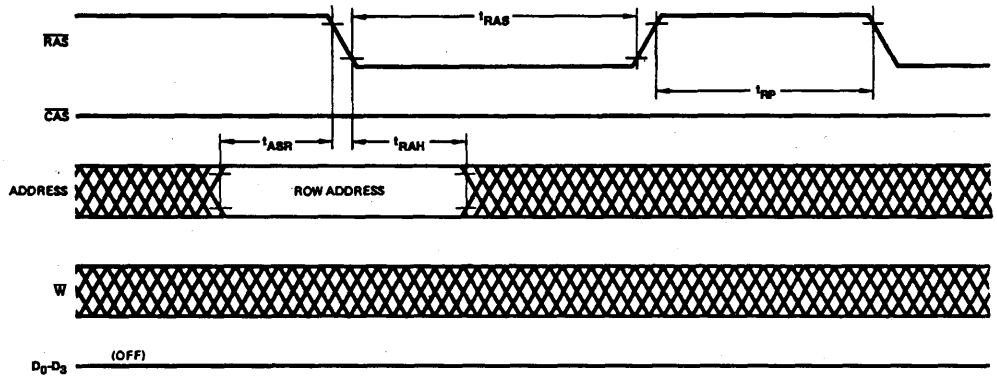


Shifter Read Cycle



Shifter Write Cycle

SWITCHING WAVEFORMS



WF000372

$\overline{\text{RAS}}$-Only Refresh

Am9101 Family

256 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating power
  125 mW typ.; 290 mW maximum — standard power
  100 mW typ.; 175 mW maximum — low power
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400 mV
- Two chip enable inputs
- Output disable control

GENERAL DESCRIPTION

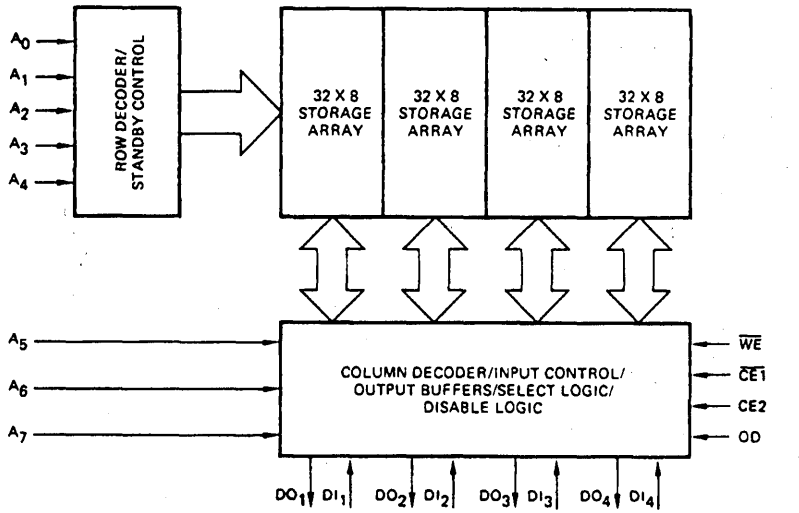
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, Static, Read/Write Random Access Memories. They offer a wide range of access times including versions as fast as 200 ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

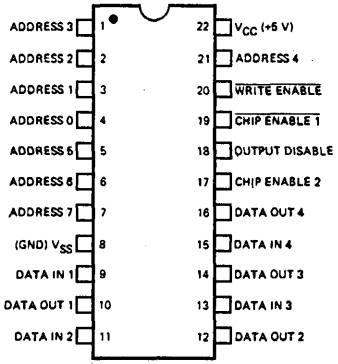
BLOCK DIAGRAM



BD000100

Publication # 03255 | Rev. D | Amendment /0
Issue Date: May 1986

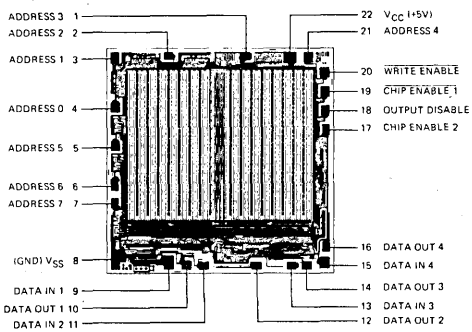
CONNECTION DIAGRAM
Top View



CD000151

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

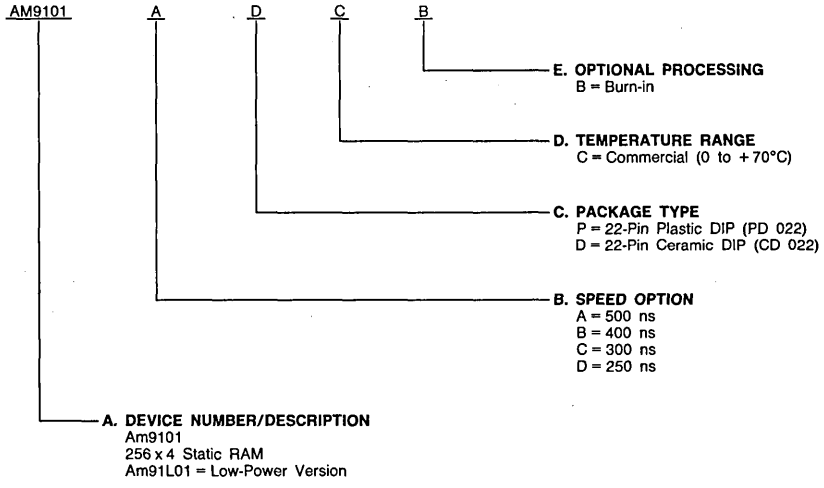


Die Size 0.132″ x 0.131″

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9101A	PC, PCB, DC, DCB
AM9101B	
AM9101C	
AM9101D	
AM91L01A	
AM91L01B	
Am91L01C	

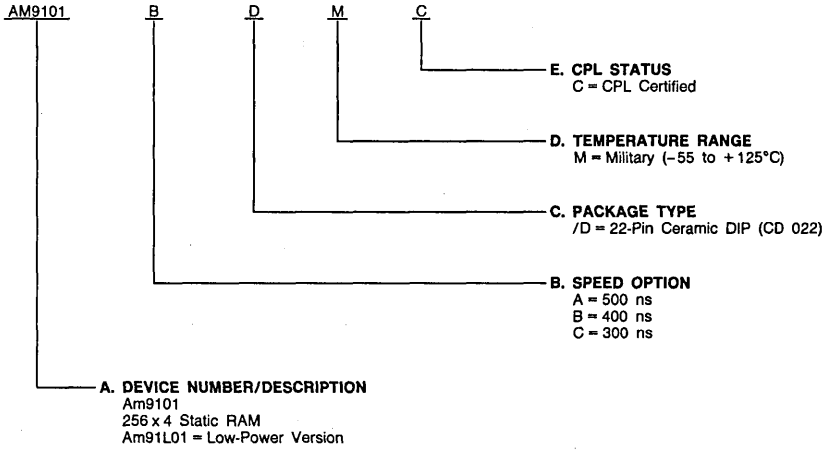
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for CPL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status



Valid Combinations	
AM9101A	/DMC
AM9101B	
AM9101C	
AM91L01A	
AM91L01B	
AM91L01C	

Valid Combinations

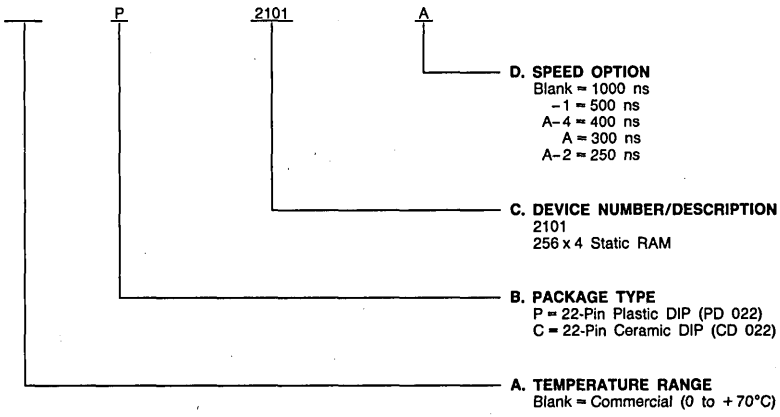
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Temperature Range**
B. Package Type
C. Device Number
D. Speed Option



Valid Combinations		
P, C	2101	-1, A-4, A, A-2

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_7$ Addresses (Input)
The 8-bit field presented at the address inputs selects one of the 256 memory locations to be read from — or written into — via the Data Input/Output lines.

$DI_1 - DI_4$ Data In Lines (Input)
The inputs whose states represent the data to be stored in memory.

$DO_1 - DO_4$ Data In Lines (Output)
The outputs whose states represent the data to be stored in memory.

$\overline{CE1}$, CE2 Chip Enable Signals (Input)
Read and Write cycles can be executed only when $\overline{CE1}$ is LOW and CE2 is HIGH.

$\overline{WE}$ Write Enable (Input, Active LOW)
Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

OD Output Disable (Input)
Read cycles can be executed only when OD is LOW.

FUNCTIONAL DESCRIPTION

Applications

Refer to Figure 1 for Memory System information.

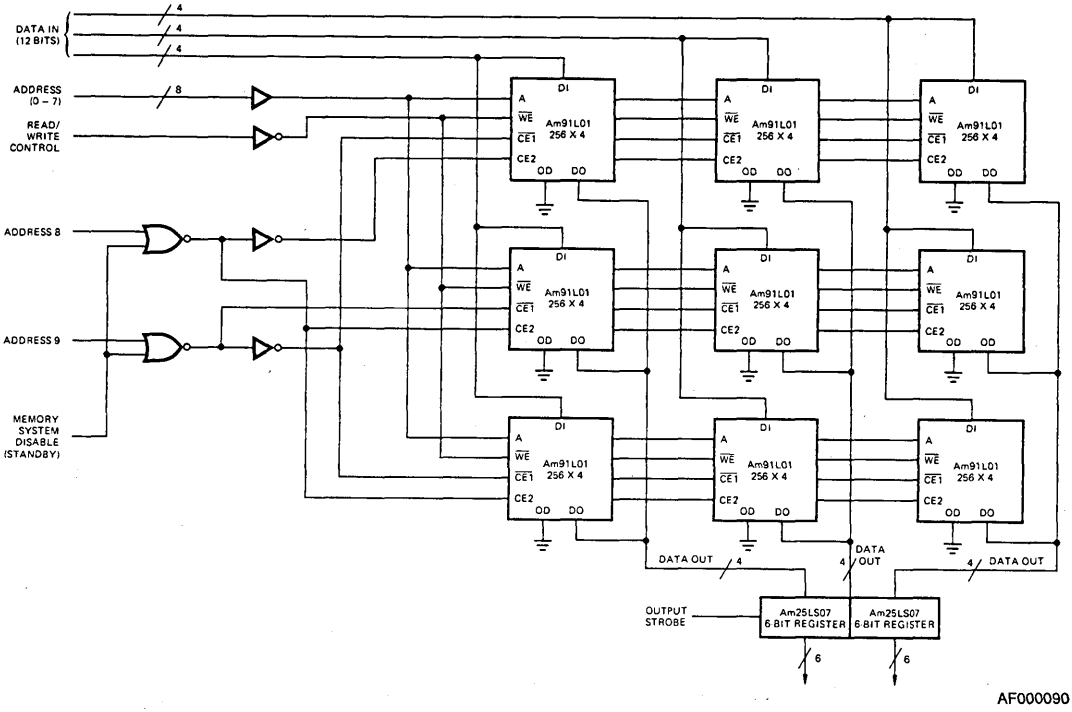


Figure 1. Memory System 768 Words by 12 Bits Per Word

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +7.0 V
DC Layout Voltage ..... −0.5 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am9101/ Am91L01 Min.	Am9101/ Am91L01 Max.	Am2101 Min.	Am2101 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −200 μA		2.4				V
			I_{OH} = −150 μA				2.2		
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 3.2 mA			0.4			V
			I_{OL} = 2.0 mA					0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	V
I_{LI}	Input Load Current	V_{CC} = Max., $0 \leq V_{IN} \leq V_{CC}$				10		10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_O = V_{CC}$	C devices		5.0		15	μA
				M devices		10			
			V_O = 0.4 V			−10		−50	
I_{CC_1}	Power Supply Center	Data Out Open V_{CC} = Max. $V_{IN} = V_{CC}$	T_A = 25°C (Note 3)	Am9101A/B		50			mA
				Am9101/C/D/E		55			
				Am91L01A/B		31			
				Am91L01C/D/E		34			
				Am2101				60	
			T_A = 0°C (C devices only)	Am9101A/B		55			
				Am9101C/D/E		60			
				Am91L01A/B		33			
				Am91L01C/D/E		36			
				Am2101				70	
			T_A = −55°C (M devices only)	Am9101A/B		60			
				Am9101C/D/E		65			
				Am91L01A/B		37			
				Am91L01C/D/E		40			
				Am2101					
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{IN} = 0 V (Note 3)				9		9	pF
C_O	Output Capacitance	T_A = 25°C, f = 1 MHz, V_O = 0 V (Note 3)				12		12	

Notes: 1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Guaranteed by characterization data. Data will be updated upon any process or design change which affects this parameter.
4. Test conditions assume signal transition times of 10 ns or less. Output load equals 1 TTL gate + 100 pF. Input signal timing reference level = 1.5 V, with input pulse levels of 0 to 3.0 V. Data output timing reference levels = 0.8 and 2.0 V.
5. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

*See the last page of this spec for Group A Subgroup Testing information.

STANDBY OPERATING CONDITIONS over temperature range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$ All Inputs = V_{PD}	$V_{PD} = 1.5$ V	Am91L01		11	25	mA
				Am9101		13	31	
			$V_{PD} = 2.0$ V	Am91L01		13	31	
				Am9101		17	41	
		$T_A = -55°C$ All Inputs = V_{PD}	$V_{PD} = 1.5$ V	Am91L01		11	28	mA
				Am9101		13	34	
			$V_{PD} = 2.0$ V	Am91L01		13	34	
				Am9101		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts

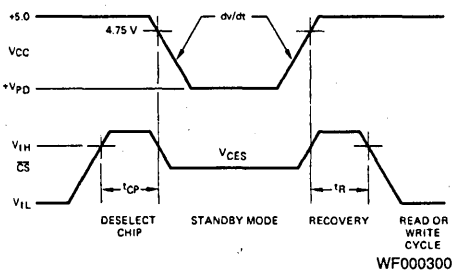
Power-Down Standby Operation

The Am9101/AM91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5 – 2.0 volts (see table and graph). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high-impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

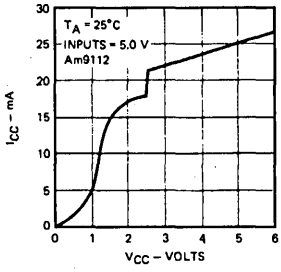
4

TYPICAL DC AND AC CHARACTERISTICS



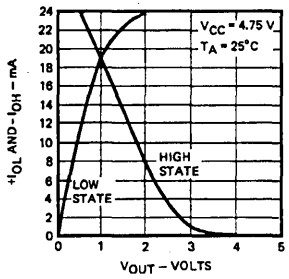
WF000300

Typical Power Supply Current Versus Voltage



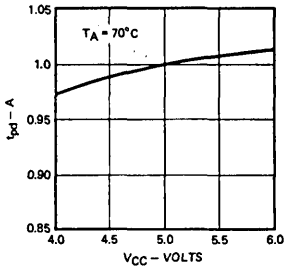
OP000460

Typical Output Current Versus Voltage



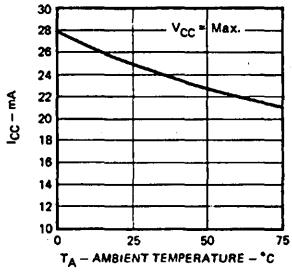
OP001060

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



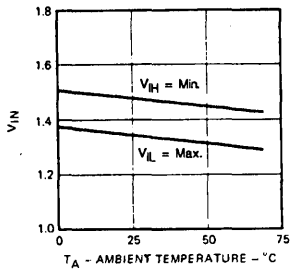
OP000100

Typical Power Supply Current Versus Ambient Temperature



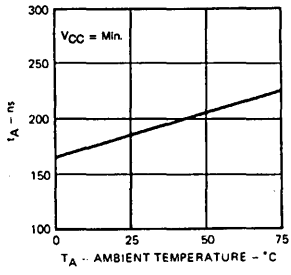
OP001070

Typical V_{IN} Limits Versus Ambient Temperature



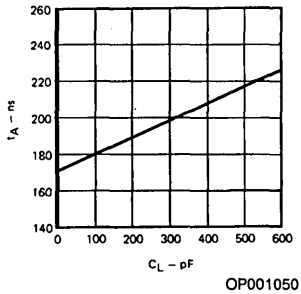
OP001030

Typical t_A Versus Ambient Temperature



OP001040

Typical t_A Versus C_L



OP001050

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 4)*

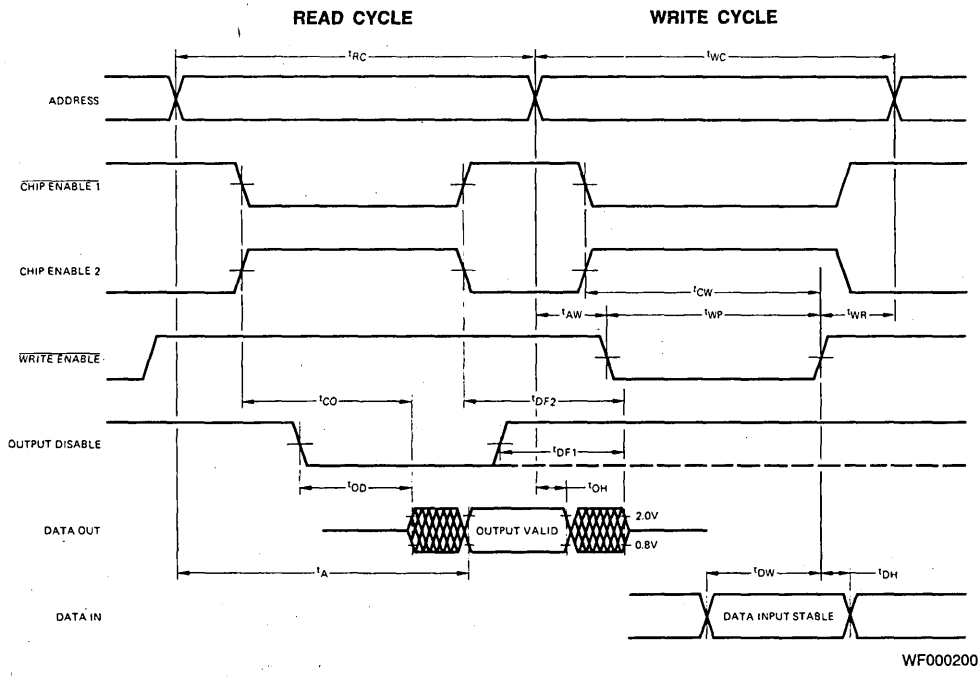
No.	Parameter Symbol	Parameter Description	Am2101		Am2101-2		Am2101-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	1000		650		500		ns
2	t_A	Access Time		1000		650		500	ns
3	t_{CO}	Chip Enable to Output ON Delay (Note 5)		800		400		350	ns
4	t_{OD}	Output Disable to Output ON Delay		700		350		300	ns
5	t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		ns
6	t_{DF1}	Output Disable to Output OFF Delay (Note 3)	0	200	0	150	0	150	ns
7	t_{DF2}	Chip Enable to Output OFF Delay (Note 3)	0	200	0	150	0	150	ns
8	t_{WC}	Write Cycle Time	1000		650		500		ns
9	t_{AW}	Address Set-up Time	150		150		100		ns
10	t_{WP}	Write Pulse Width	750		400		300		ns
11	t_{CW}	Chip Enable Set-up Time (Note 5)	900		550		400		ns
12	t_{WR}	Address Hold Time	50		50		50		ns
13	t_{DW}	Input Data Set-up Time	700		400		280		ns
14	t_{DH}	Input Data Hold Time	100		100		100		ns

No.	Parameter Symbol	Parameter Description	Am9101A Am91L01A		Am9101B Am91L01B		Am9101C Am91L01C		Am9101D		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	500		400		300		250		ns
2	t_A	Access Time		500		400		300		250	ns
3	t_{CO}	Chip Enable to Output ON Delay (Note 5)		200		175		150		125	ns
4	t_{OD}	Output Disable to Output ON Delay		175		150		125		100	ns
5	t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
6	t_{DF1}	Output Disable to Output OFF Delay	5.0	125	5.0	100	5.0	100	5.0	75	ns
7	t_{DF2}	Chip Enable to Output OFF Delay	10	125	10	125	10	100	10	100	ns
8	t_{WC}	Write Cycle Time	500		400		300		250		ns
9	t_{AW}	Address Set-up Time	20		20		20		20		ns
10	t_{WP}	Write Pulse Width	225		200		175		150		ns
11	t_{CW}	Chip Enable Set-up Time (Note 5)	175		150		125		100		ns
12	t_{WR}	Address Hold Time	0		0		0		0		ns
13	t_{DW}	Input Data Set-up Time	150		125		100		85		ns
14	t_{DH}	Input Data Hold Time	15		15		15		15		ns

See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF000200

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
V_{PD}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11
2	t_{A}	7, 8, 9, 10, 11
3	t_{CO}	7, 8, 9, 10, 11
4	t_{OD}	7, 8, 9, 10, 11
5	t_{OH}	7, 8, 9, 10, 11
8	t_{WC}	7, 8, 9, 10, 11
9	t_{AW}	7, 8, 9, 10, 11
10	t_{WP}	7, 8, 9, 10, 11
11	t_{CW}	7, 8, 9, 10, 11
12	t_{WR}	7, 8, 9, 10, 11
13	t_{DW}	7, 8, 9, 10, 11
14	t_{DH}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9111 Family

256 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating power dissipation
  125 mW typ.; 290 mW maximum — standard power
  100 mW typ.; 175 mW maximum — low power
- DC standby mode reduces power up to 84%
- High noise immunity — full 400 mV
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Output disable control
- Zero address setup and hold times for simplified timing

GENERAL DESCRIPTION

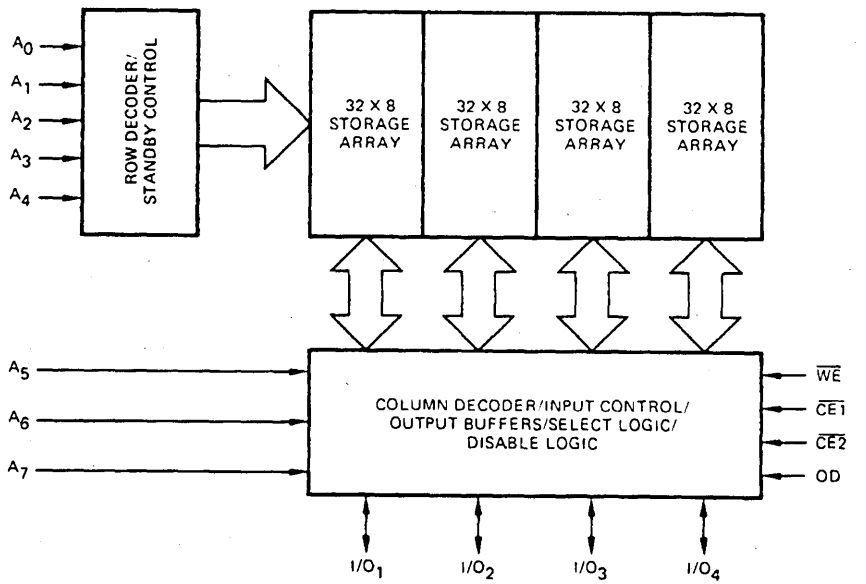
The Am9111/Am91L11 series of devices are high-performance, low-power, 1024-bit, Static, Read/Write Random Access Memories. They offer a wide range of access times including versions as fast as 200 ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but also helps eliminate external logic in bus-oriented memory systems

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

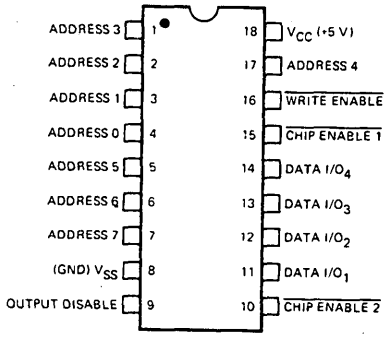
BLOCK DIAGRAM



BD000220

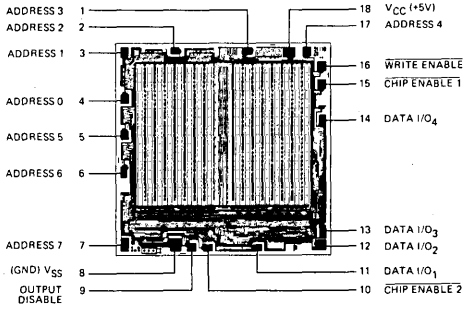
Publication # 03256 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD000320

METALLIZATION AND PAD LAYOUT



Die Size: 0.132" x 0.131"

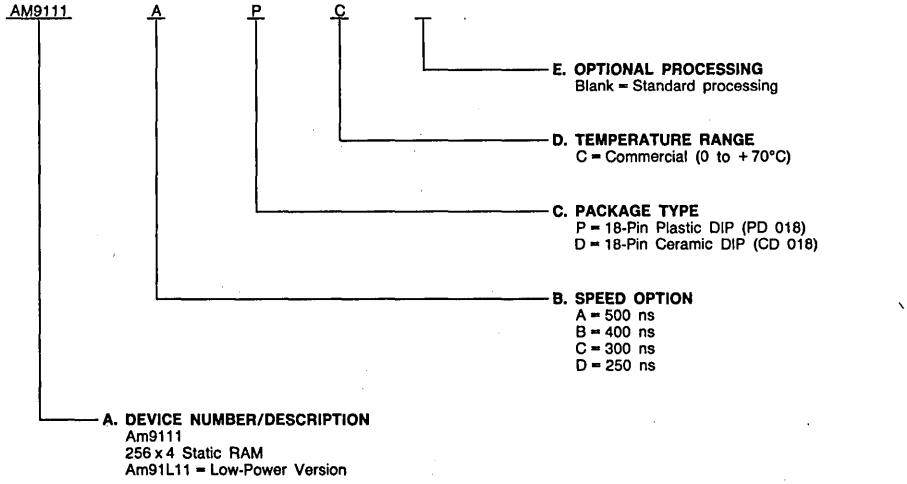
4

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9111A	PC, DC
AM9111B	
AM9111C	
AM9111D	
AM91L11A	
AM91L11B	
AM91L11C	

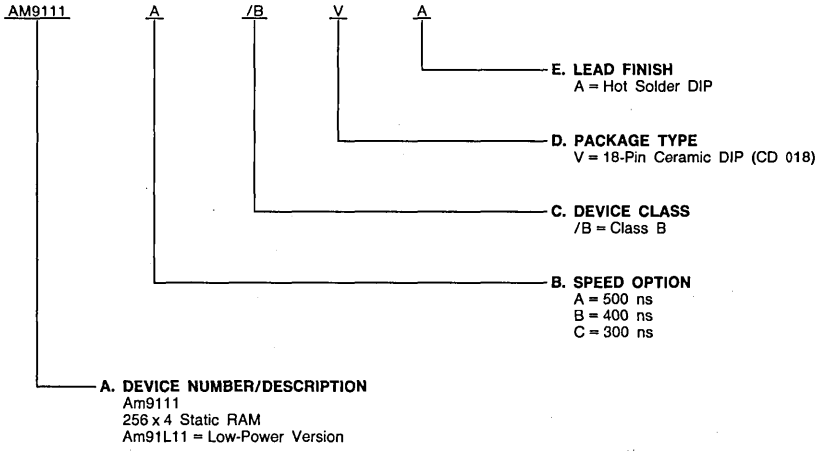
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9111A	/BVA
AM9111B	
AM9111C	
AM91L11A	
AM91L11B	
AM91L11C	

Valid Combinations

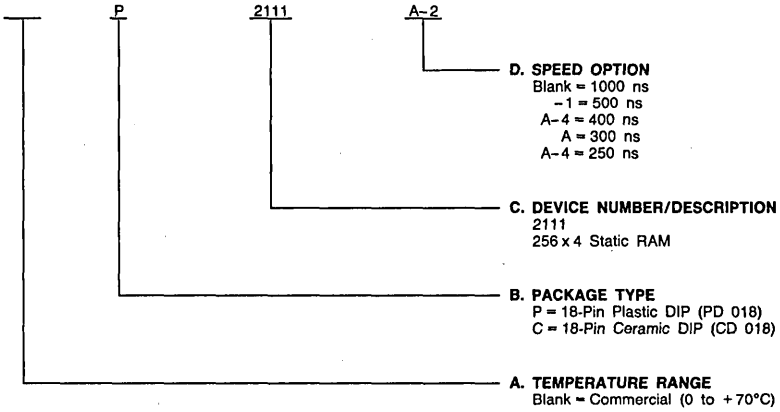
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Temperature Range**
B. Package Type
C. Device Number
D. Speed Option



Valid Combinations		
P, C	2111	-1, A-4, A, A-2

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_7$ Addresses (Input)
The 8-bit field presented at the address inputs selects one of the 256 memory locations to be read from — or written into — via the Data Input/Output lines.

$I/O_1 - I/O_4$ Data Input/Output Lines (Input/Output)
If $\overline{WE}$ is LOW, the data represented on the Data I/O lines can be written into the selected memory location. If $\overline{WE}$ is HIGH, the Data I/O lines represent the data read from the selected memory location.

$\overline{CE1}$, $\overline{CE2}$ Chip Enable Signals (Input)
Read and Write cycles can be executed only when both $\overline{CE1}$ and $\overline{CE2}$ are LOW.

$\overline{WE}$ Write Enable (Input, Active LOW)
Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

OD Output Disable (Input)
Read cycles can be executed only when OD is LOW.

FUNCTIONAL DESCRIPTION

Applications

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low-power versions available, high speed, high output drive, etc. In addition, the Am9111 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

This bussed I/O approach cuts down the package pin count allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9111 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

The Output Disable control signal is provided to prevent signal contention for the bus lines, and to simplify tri-state bus control in the external circuitry. If the chip is enabled and the output is enabled and the memory is in the Read state, then the output buffers will be impressing data on the bus lines. At that point, if the external system tries to drive the bus with data, in preparation for a write operation, there will be conflict for domination of the bus lines. The Output Disable signal allows the user direct control over the output buffers, independent of the state of the memory. Although there are alternative ways to resolve the conflict, normally Output Disable will be held HIGH during a write operation.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +7.0 V
DC Layout Voltage ..... −0.5 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Am9111/ Am91L11 Min.	Am9111/ Am91L11 Max.	Am2111 Min.	Am2111 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −200 μA		2.4				V
			I_{OH} = −150 μA				2.2		
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 3.2 mA			0.4			V
			I_{OL} = 2.0 mA					0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	V
I_{LI}	Input Load Current	V_{CC} = Max., $0 \leq V_{IN} \leq V_{CC}$				10		10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_O = V_{CC}$	C devices		5.0		15	μA
				M devices		10			
			V_O = 0.4 V			−10		−50	
I_{CC1}	Power Supply Center	Data Out Open V_{CC} = Max. $V_{IN} = V_{CC}$	T_A = 25°C (Note 3)	Am9111A/B		50			mA
				Am9111		55			
				Am9111		31			
				Am91L11C/D/E		34			
				Am2111				60	
			T_A = 0°C (C devices only)	Am9111		55			
				Am9111		60			
				Am91L11A/B		33			
				Am91L11C/D/E		36			
				Am2111				70	
			T_A = −55°C (M devices only)	Am9111A/B		60			
				Am9111C/D/E		65			
				Am9111		37			
				Am9111		40			
				Am2111					
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{IN} = 0 V (Note 3)				9		9	pF
C_O	Output Capacitance	T_A = 25°C, f = 1 MHz, V_O = 0 V (Note 3)				12		15	

Notes: 1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Guaranteed by characterization data. Data will be updated upon any process or design change which affects this parameter.
4. Test conditions assume signal transition times of 10 ns or less. Output load equals 1 TTL gate + 100 pF. Input signal timing reference level = 1.5 V, with input pulse levels of 0 to 3.0 V. Data output timing reference levels = 0.8 and 2.0 V.
5. Both $\overline{CE1}$ and $\overline{CE2}$ must be true to enable the chip.

*See the last page of this spec for Group A Subgroup Testing information.

STANDBY OPERATING CONDITIONS over temperature range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	T_A = 0°C, All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L11		11	25	mA
				Am9111		13	31	
			V_{PD} = 2.0 V	Am91L11		13	31	
				Am9111		17	41	
		T_A = −55°C, All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L11		11	28	mA
				Am9111		13	34	
			V_{PD} = 2.0 V	Am91L11		13	34	
				Am9111		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/µs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts

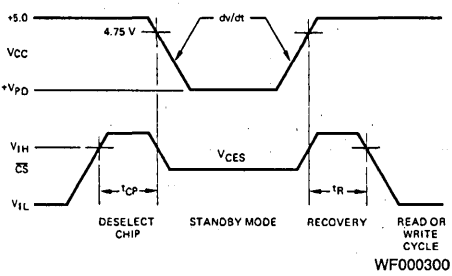
Power-Down Standby Operation

The Am9111/Am91L11 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high-impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

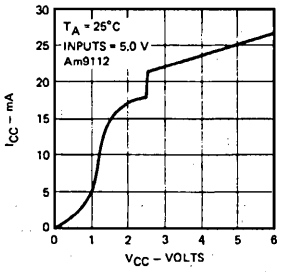
4

TYPICAL DC AND AC CHARACTERISTICS



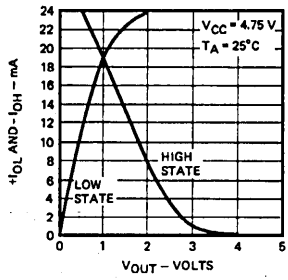
WF000300

Typical Power Supply Current Versus Voltage



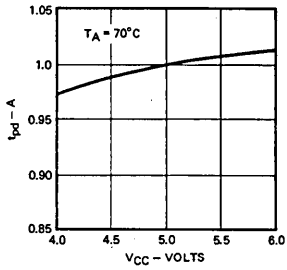
OP000460

Typical Output Current Versus Voltage



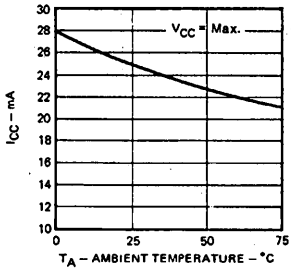
OP001060

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



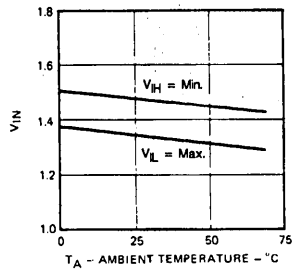
OP000100

Typical Power Supply Current Versus Ambient Temperature



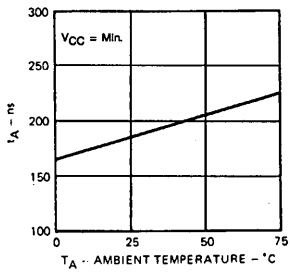
OP001070

Typical V_{IN} Limits Versus Ambient Temperature



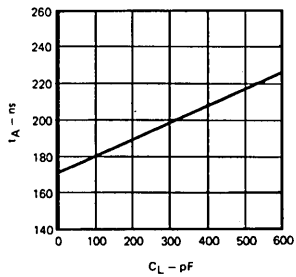
OP001030

Typical t_A Versus Ambient Temperature



OP001040

Typical t_A Versus C_L



OP001050

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 4)*

No.	Parameter Symbol	Parameter Description	Am2111		Am2111-2		Am2111-1		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	1000		650		500		ns
2	t_A	Access Time		1000		650		500	ns
3	t_{CO}	Chip Enable to Output ON Delay (Note 5)		800		400		350	ns
4	t_{OD}	Output Disable to Output ON Delay		700		350		300	ns
5	t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		ns
6	t_{DF1}	Output Disable to Output OFF Delay (Note 3)	0	200	0	150	0	150	ns
7	t_{DF2}	Chip Enable to Output OFF Delay (Note 3)	0	200	0	150	0	150	ns
8	t_{WC}	Write Cycle Time	1000		650		500		ns
9	t_{AW}	Address Set-up Time	150		150		100		ns
10	t_{WP}	Write Pulse Width	750		400		300		ns
11	t_{CW}	Chip Enable Set-up Time (Note 1)	900		550		400		ns
12	t_{WR}	Address Hold Time	50		50		50		ns
13	t_{DW}	Input Data Set-up Time	700		400		280		ns
14	t_{DH}	Input Data Hold Time	100		100		100		ns

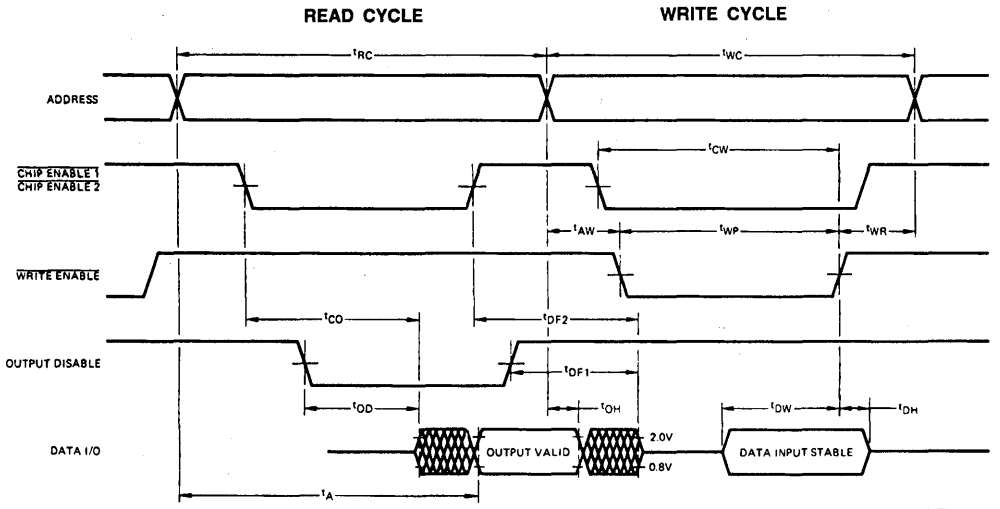
No.	Parameter Symbol	Parameter Description	Am9111A Am91L11A		Am9111B Am91L11B		Am9111C Am91L11C		Am9111D		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	500		400		300		250		ns
2	t_A	Access Time		500		400		300		250	ns
3	t_{CO}	Chip Enable to Output ON Delay (Note 5)		200		175		150		125	ns
4	t_{OD}	Output Disable to Output ON Delay		175		150		125		100	ns
5	t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
6	t_{DF1}	Output Disable to Output OFF Delay	5.0	125	5.0	100	5.0	100	5.0	75	ns
7	t_{DF2}	Chip Enable to Output OFF Delay	10	150	10	125	10	125	10	100	ns
8	t_{WC}	Write Cycle Time	500		400		300		250		ns
9	t_{AW}	Address Set-up Time	20		20		20		20		ns
10	t_{WP}	Write Pulse Width	225		200		175		150		ns
11	t_{CW}	Chip Enable Set-up Time (Note 5)	175		150		125		100		ns
12	t_{WR}	Address Hold Time	0		0		0		0		ns
13	t_{DW}	Input Data Set-up Time	150		125		100		85		ns
14	t_{DH}	Input Data Hold Time	15		15		15		15		ns

See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

4

SWITCHING WAVEFORMS



WF000591

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
V_{PD}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11
2	t_{A}	7, 8, 9, 10, 11
3	t_{CO}	7, 8, 9, 10, 11
4	t_{OD}	7, 8, 9, 10, 11
5	t_{OH}	7, 8, 9, 10, 11
8	t_{WC}	7, 8, 9, 10, 11
9	t_{AW}	7, 8, 9, 10, 11
10	t_{WP}	7, 8, 9, 10, 11
11	t_{CW}	7, 8, 9, 10, 11
12	t_{WR}	7, 8, 9, 10, 11
13	t_{DW}	7, 8, 9, 10, 11
14	t_{DH}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9112

256 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating power dissipation
  125 mW typ.; 290 mW maximum — standard power
  100 mW typ.; 175 mW maximum — low power
- High noise immunity — full 400 mV
- Uniform switching characteristics — access times insensitive to supply variations, address patterns and data patterns
- Bus-oriented I/O data
- Zero address, setup and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices

GENERAL DESCRIPTION

The Am9112/Am91L12 series of products are high-performance, low-power, 1024-bit, static read/write random-access memories. They offer a range of speeds and power dissipations including versions as fast as 200 ns and as low as 100 mW typical.

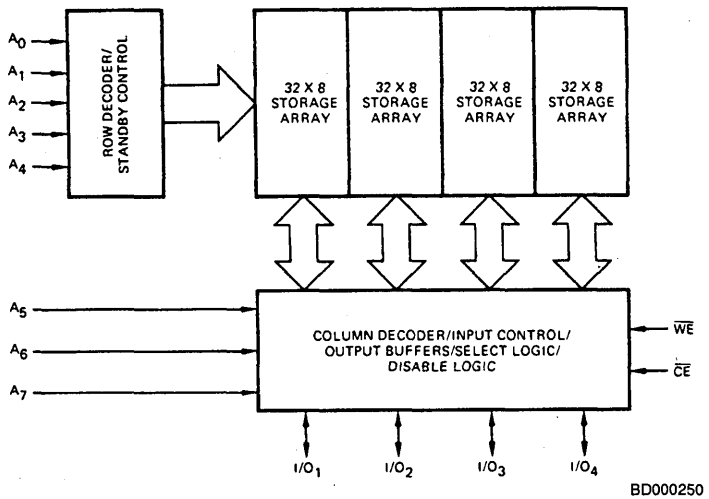
Each memory is implemented as 256 words by 4 bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1 of 256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, the write amplifiers are disabled, the output buffers are enabled, and the memory will execute a read cycle. When $\overline{CE}$ is LOW and $\overline{WE}$ is LOW, the write amplifiers are enabled, the output buffers are disabled, and the memory will execute a write cycle. When $\overline{CE}$ is HIGH, both the write amplifiers and the output buffers are disabled.

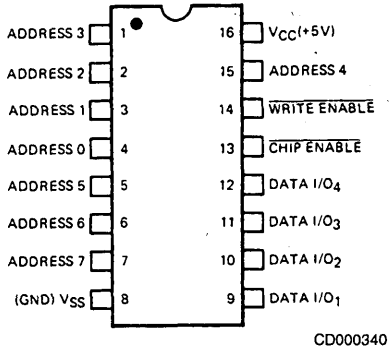
These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

BLOCK DIAGRAM



Publication # 03257 Rev. D Amendment /0
Issue Date: May 1986

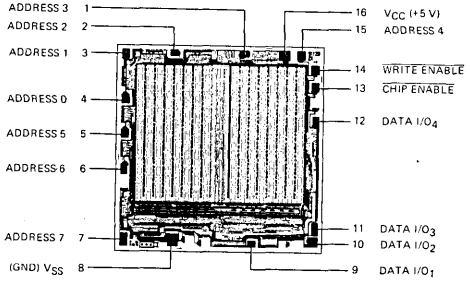
CONNECTION DIAGRAM
Top View



CD000340

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT



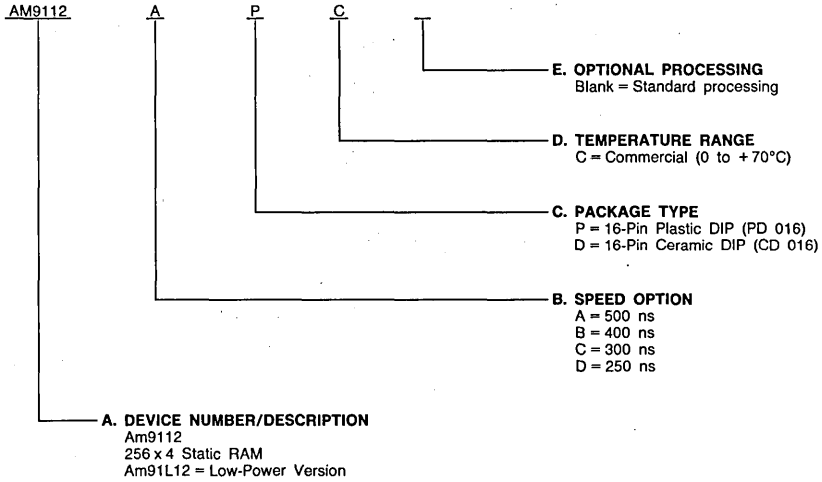
Die Size 0.132" x 0.131"

4

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9112A	PC, DC
AM9112B	
AM9112C	
AM9112D	
AM91L12A	
AM91L12B	
AM91L12C	

Valid Combinations

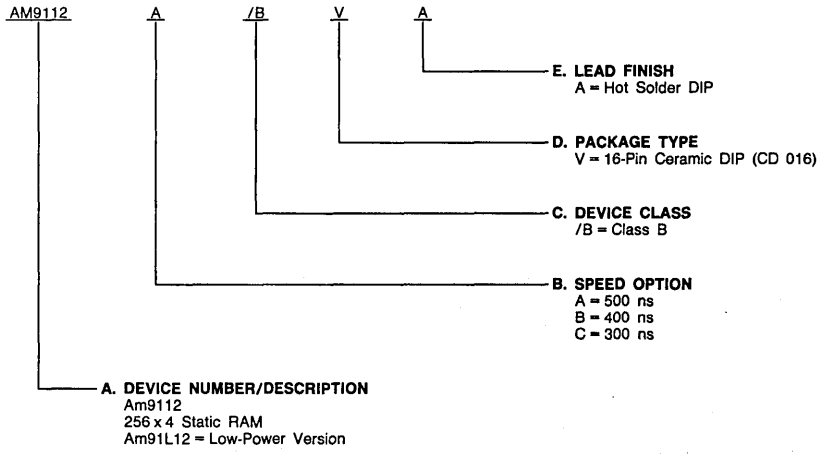
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9112A	/BVA
AM9112B	
AM9112C	
AM91L12A	
AM91L12B	
AM91L12C	

Valid Combinations

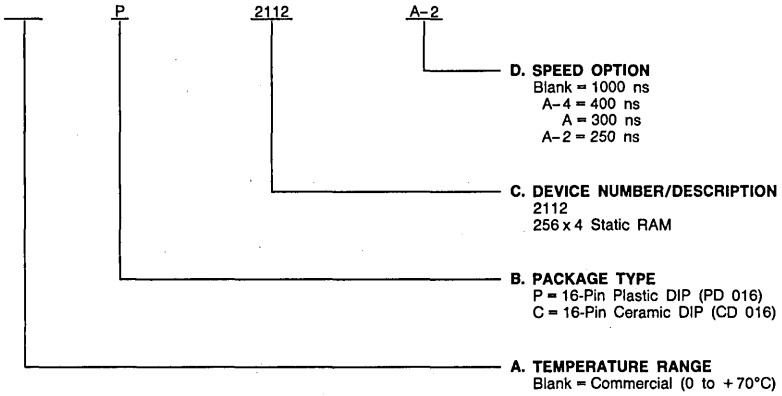
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Temperature Range**
B. Package Type
C. Device Number
D. Speed Option



Valid Combinations		
P, C	2112	A-4, A, A-2

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_7$ Addresses (Input)
The 8-bit field presented at the address inputs selects one of the 256 memory locations to be read from — or written into — via the Data Input/Output lines.

$I/O_1 - I/O_4$ Data Input/Output Lines (Input/Output)
If $\overline{WE}$ is LOW, the data represented on the Data I/O lines can be written into the selected memory location. If $\overline{WE}$ is HIGH, the Data I/O lines represent the data read from the selected memory location.

$\overline{CE}$ Chip Enable (Input, Active LOW)
Read and Write cycles can be executed only when $\overline{CE}$ is LOW.

$\overline{WE}$ Write Enable (Input, Active LOW)
Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

FUNCTIONAL DESCRIPTION

Applications

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low-power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

This bussed I/O approach keeps the package pin count low, allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ LOW) and the memory is in the Read state ($\overline{WE}$ HIGH), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always LOW or is derived directly from addresses and so is LOW for the whole cycle, make sure t_{WP} is at least $t_{DW} + t_{DF}$ and delay the input data until t_{DF} following the falling edge of $\overline{WE}$. With zero address set-up and hold times, it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.

2. For systems where $\overline{CE}$ is HIGH for at least t_{DF} preceeding the falling edge of $\overline{WE}$, t_{WP} may assume the minimum specified value. When $\overline{CE}$ is HIGH for t_{DF} before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.

3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be LOW to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25 ns.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +7.0 V
DC Layout Voltage ..... −0.5 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			C Devices Min.	C Devices Max.	M Devices Min.	M Devices Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −200 μA			2.4		2.2		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 3.2 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.8	V
I_{LI}	Input Load Current	V_{CC} = Max., 0 V ≤ V_{IN} ≤ V_{CC}				10		10	μA
I_{IO}	I/O Leakage Current	V=CE = V_{IH}	V_O = V_{CC}			5		10	μA
			V_O = 0.4 V			−10		−10	
I_{CC}	Power Supply Current	Data Out Open V_{CC} = Max. V_{IN} = V_{CC}	T_A = 25°C	9112A/B		50		50	mA
				9112C/D/E		55		55	
				91L12A/B		31		31	
				91L12C/D/E		34		34	
			T_A = 0°C (Note 3)	9112A/B		55			
				9112C/D/E		60			
				91L12A/B		33			
				91L12C/D/E		36			
			T_A = −55°C	9112A/B				60	
				9112C/D/E				65	
				91L12A/B				37	
				91L12C/D/E				40	
C_{IN}	Input Capacitance	V_{IN} = 0 V, T_A = 25°C, f = 1 MHz (Note 3)				9		9	pF
C_O	Output Capacitance	V_O = 0 V, T_A = 25°C, f = 1 MHz (Note 3)				12		11	

Notes: See notes following Switching Characteristics table.

STANDBY OPERATING CONDITIONS over temperature range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	T_A = 0°C All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L12		11	25	mA
				Am9112		13	31	
			V_{PD} = 2.0 V	Am91L12		13	31	
				Am9112		17	41	
		T_A = −55°C All Inputs = V_{PD}	V_{PD} = 1.5 V	Am91L12		11	28	mA
				Am9112		13	34	
			V_{PD} = 2.0 V	Am91L12		13	34	
				Am9112		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts

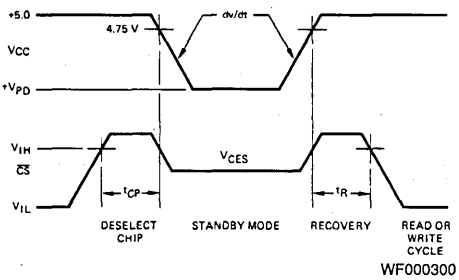
*See the last page of this spec for Group A Subgroup Testing information.

Power-Down Standby Operation

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5 – 2.0 volts (see table and graph). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

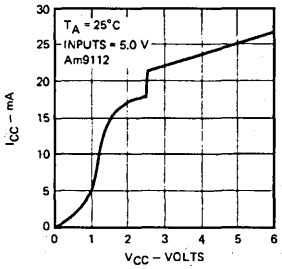
To ensure that the output of the device is in a high-impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

TYPICAL DC and AC CHARACTERISTICS



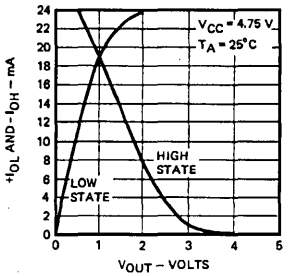
WF000300

Typical Power Supply Current Versus Voltage



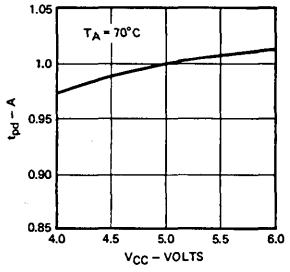
OP000460

Typical Output Current Versus Voltage



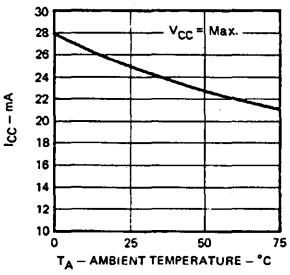
OP001060

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



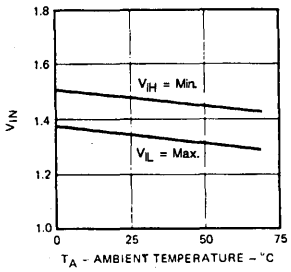
OP000100

Typical Power Supply Current Versus Ambient Temperature



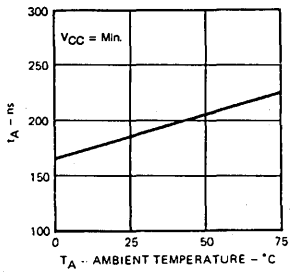
OP001070

Typical V_{IN} Limits Versus Ambient Temperature



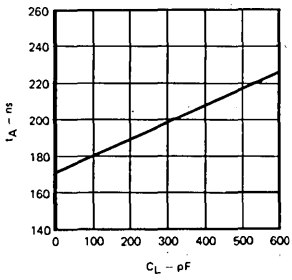
OP001030

Typical t_A Versus Ambient Temperature



OP001040

Typical t_A Versus C_L



OP001050

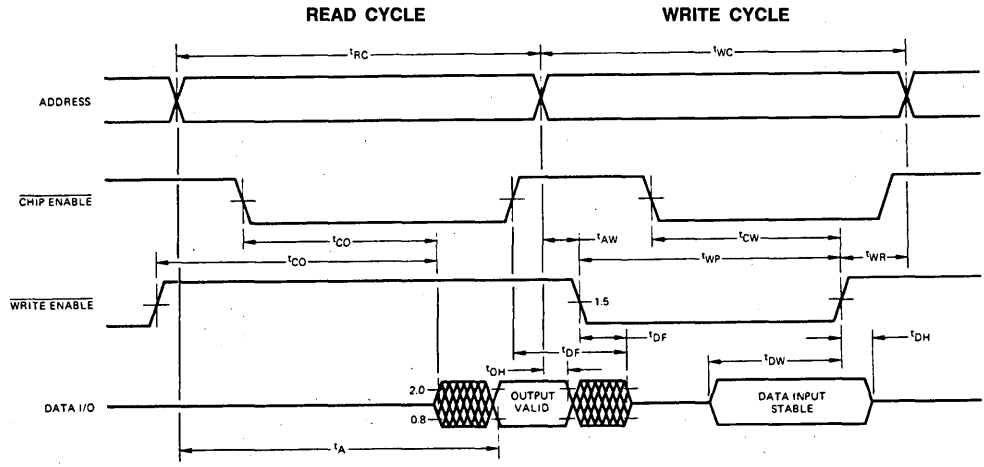
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 4)*

No.	Parameter Symbol	Parameter Description	Am9112A Am91L12A		Am9112B Am91L12B		Am9112C Am91L12C		Am9112D		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	500		400		300		250		ns
2	t_A	Access Time		500		400		300		250	ns
3	t_{CO}	Output Enabled to Output ON Delay (Note 5)	5.0	175	5.0	150	5.0	125	5.0	100	ns
4	t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
5	t_{DF}	Output Disabled to Output OFF Delay (Note 6)	5.0	125	5.0	100	5.0	100	5.0	75	ns
6	t_{WC}	Write Cycle Time	500		400		300		250		ns
7	t_{AW}	Address Setup Time	20		20		20		20		ns
8	t_{WR}	Address Hold Time	0		0		0		0		ns
9	t_{WP}	Write Pulse Width (Note 7)	225		200		175		150		ns
10	t_{CW}	Chip Enable Setup Time	175		150		125		100		ns
11	t_{DW}	Input Data Setup Time	150		125		100		85		ns
12	t_{DH}	Input Data Hold Time (Note 8)	15		15		15		15		ns

Notes:
1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Guaranteed by characterization data. Data will be updated upon any process or design change which affects this parameter.
4. Test conditions assume signal transition times of 10 ns or less. Output load equals 1 TTL gate + 100 pF. Input signal timing reference level = 1.5 V, with input pulse levels of 0 to 3.0 V. Data output timing reference levels = 0.8 and 2.0 V.
5. Output is enabled and t_{CO} commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
6. Output is disabled and t_{DF} defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
7. Minimum t_{WP} is valid when $\overline{CE}$ has been HIGH at least t_{DF} before $\overline{WE}$ goes LOW. Otherwise $t_{WP(Min.)} = t_{DW(Min.)} + t_{DF(Min.)}$.
8. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
9. See Functional Description section of this specification.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Note 9)



WF000610

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC}	1, 2, 3
V_{PD}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11
2	t_{A}	7, 8, 9, 10, 11
3	t_{CO}	7, 8, 9, 10, 11
4	t_{OH}	7, 8, 9, 10, 11
5	t_{DF}	7, 8, 9, 10, 11
6	t_{WC}	7, 8, 9, 10, 11
7	t_{AW}	7, 8, 9, 10, 11
8	t_{WR}	7, 8, 9, 10, 11
9	t_{WP}	7, 8, 9, 10, 11
10	t_{CW}	7, 8, 9, 10, 11
11	t_{DW}	7, 8, 9, 10, 11
12	t_{DH}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9114/9124

1024 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

- Low operating and standby power
- Access times down to 200 ns
- Am9114 is a direct plug-in replacement for 2114
- Am9124 pin and function compatible with Am9114 and 2114, plus $\overline{CS}$ power-down feature
- High output drive — 4.0-mA sink current @ 0.4 V —Am9124, 3.2-mA sink current @ 0.4 V—Am9114
- TTL-identical input/output levels

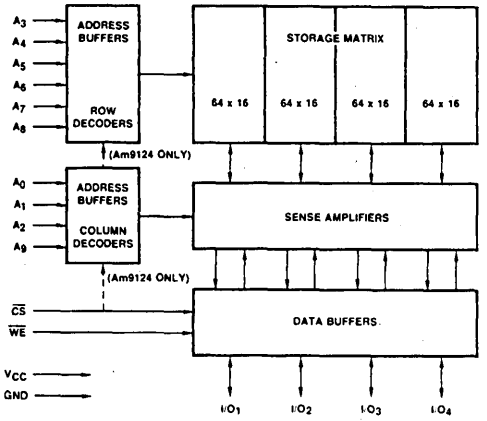
GENERAL DESCRIPTION

The Am9114 and Am9124 are high-performance, static, N-Channel, read/write, random-access memories organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. Low-power versions of both devices are available with power savings of over 30%. The Am9114 and Am9124 are the same except that the Am9124 offers an automatic $\overline{CS}$ power-down feature.

The Am9124 remains in a low-power standby mode as long as $\overline{CS}$ remains HIGH, thus reducing its power requirements. The Am9124 power decreases from 368 mW to 158 mW in the standby mode, and the Am91L24 from 262 mW to 105 mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9114.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0 mA for Am9124 and 3.2 mA for Am9114 provides increased short-circuit current for improved capacitive drive.

BLOCK DIAGRAM



BD000081

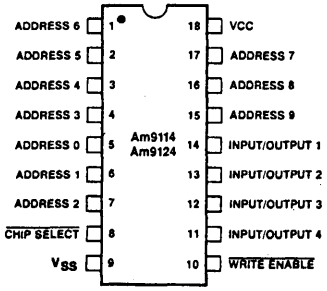
Publication # 01454 | Rev. E | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

Part Number			Am9114/91L14 & Am9124/91L24		Am9114/91L14
Speed Indicator			B	C	E
Maximum Access Time (ns)			450	300	200
0 to +70°C	I_{CC} (mA)	Standard	70	70	70
		Low-Power	50	50	50
	I_{PD} (mA) (Note 1)	Standard	30	30	–
		Low-Power	20	20	–
−55 to +125°C	I_{CC} (mA)	Standard	80	80	80
		Low-Power	60	60	60
	I_{PD} (mA) (Note 1)	Standard	33	33	–
		Low-Power	22	22	–

Notes: 1. Am9124/91L24 only.

CONNECTION DIAGRAM
Top View

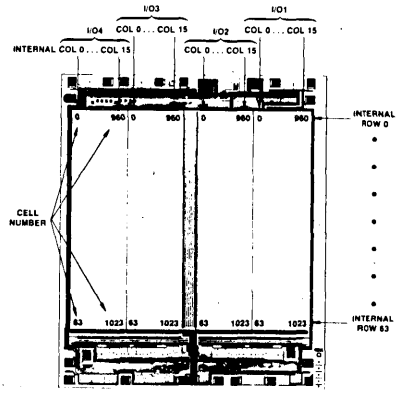


CD000131

Note: Pin 1 is marked for orientation.

BIT MAP

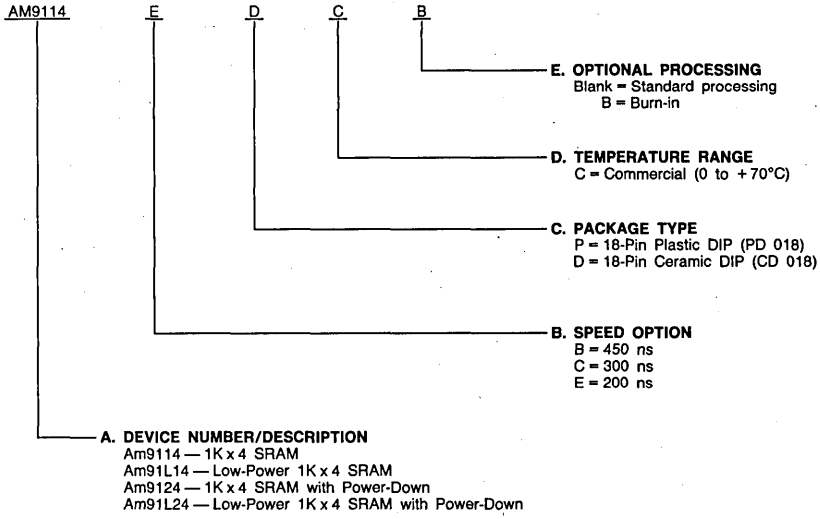
Address Designators	
External	Internal
A_0	A_9
A_1	A_8
A_2	A_7
A_3	A_0
A_4	A_1
A_5	A_2
A_6	A_3
A_7	A_4
A_8	A_5
A_9	A_6



ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9114B	PC, PCB, DC, DCB
AM91L14B	
AM9124B	
AM91L24B	
AM9114C	
AM91L14C	
AM9124C	
AM91L24C	
AM9114E	
AM91L14E	

Valid Combinations

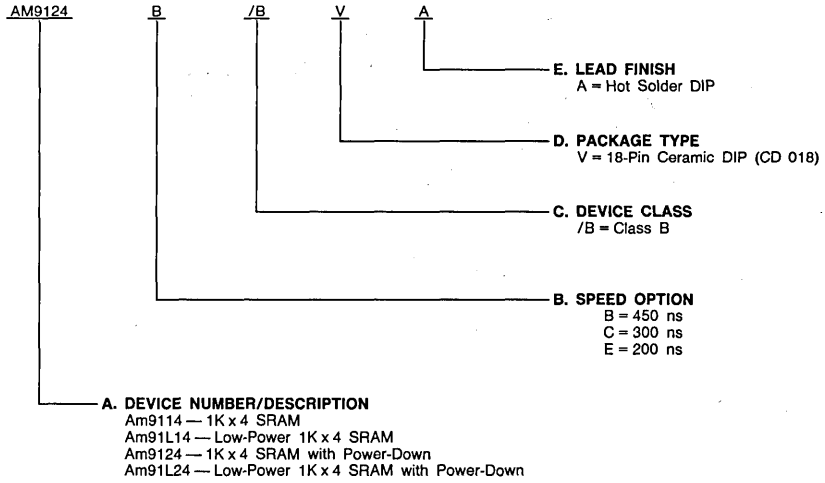
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9114B	/BVA
AM91L14B	
AM9124B	
AM91L24B	
AM9114C	
AM91L14C	
AM9124C	
AM91L24C	
AM9114E	
AM91L14E	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The address input lines select the memory location from which to read or write.

$\overline{CS}$ Chip Select (Input, Active LOW)
The $\overline{CS}$ line selects the memory device for active operation.

$\overline{WE}$ Write Enable (Input, Active LOW)
When both $\overline{CS}$ and $\overline{WE}$ are LOW, data on the input lines is written to the location presented on the address input lines.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional)
These lines provide the path for data to be written to or read from the selected memory location.

V_{CC} Power Supply

V_{SS} Ground

TABLE 1. SUPPLY CURRENT ADVANTAGE OF Am9124

		Worst Case Current (mA at 0°C)	
Configuration	**Part Number**	**100% Duty Cycle**	**50% Duty Cycle**
2K x 8	9114	280	280
	91L14	200	200
	9124	200	160
	91L24	140	110
4K x 12	9114	840	840
	91L14	600	600
	9124	480	420
	91L24	330	285
8K x 16	9114	2240	2240
	91L14	1600	1600
	9124	1120	1040
	91L24	760	700

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
Signal Voltages with
Respect to Ground ..... −0.5 V to +7.0 V
Power Dissipation ..... 1.0 W
DC Output Current ..... 10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5 V

Military (M) Devices*
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at T_C = +25°C, +125°C and −55°C

DC CHARACTERISTICS over operating range unless otherwise specified*

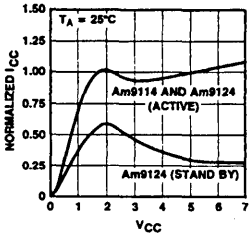
Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Units
I_{OH}	Output HIGH Current	V_{CC} = +4.5V, V_{OH} = 2.4V	91(L)14		−1.0		mA
			91(L)24		−1.4		
I_{OL}	Output LOW Current	V_{OL} = 0.4V	T_A = 70°C	91(L)14	3.2		
				91(L)24	4.0		
			T_A = +125°C	91(L)14	2.4		
				91(L)24	3.2		
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−0.5	0.8	
I_{IX}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10	μA
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$, Output Disabled	T_A = 0 to +70°C		−10	10	
			T_A = −55 to +125°C		−50	50	
I_{OS}	Output Short Circuit Current	(Note 3)	91(L)14C			75	mA
			91(L)24C			95	
			91(L)14M			75	
			91(L)24M			115	
I_{CC}	Operating Supply Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$	T_A = 0°C	Standard devices		70	mA
				L devices		50	
			T_A = −55°C	Standard devices		80	
				L devices		60	
I_{PD}	Automatic $\overline{CS}$ Power Down Current (9124/L24 only)	V_{CC} = Max., $\overline{CS} \geq V_{IH}$	T_A = 0°C	9124		30	
				91L24		20	
			T_A = −55°C	9124		33	
				91L24		22	
C_{IN}	Input Capacitance	(Note 7)	f = 1.0 MHz, T_A = 25°C, All pins at 0 V			7	pF
$C_{I/O}$	I/O Capacitance					7	

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. For test purposes, not more than one output at a time should be shorted. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.
4. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V and output loading of one standard TTL gate plus 100 pF.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. Chip Select access time (t_{CO}) is longer for the Am9124 than for the Am9114. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.
7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

*See the last page of this spec for Group A Subgroup Testing information.

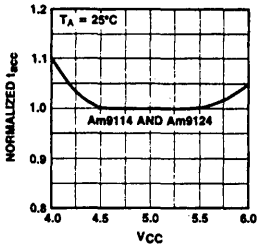
TYPICAL DC and AC CHARACTERISTICS

Normalized Supply Current Versus Supply Voltage



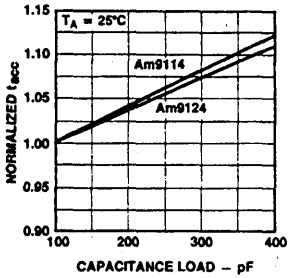
OP000531

Normalized Access Time Versus Supply Voltage



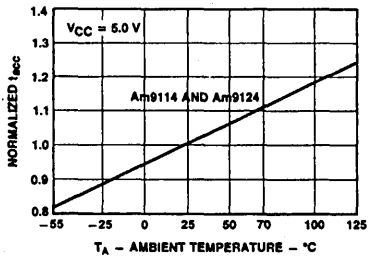
OP000541

Normalized Access Time Versus Output Loading



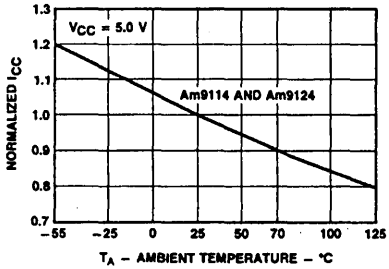
OP000551

Normalized Access Time Versus Ambient Temperature



OP000201

Normalized Supply Current Versus Ambient Temperature



OP000211

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 4-6)*

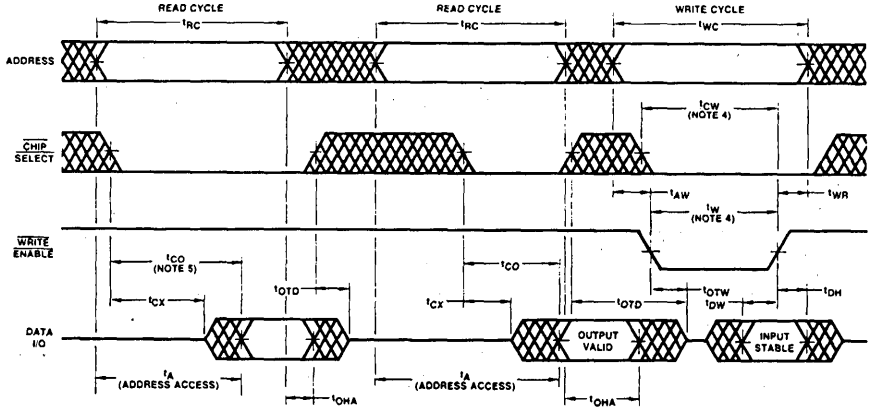
No.	Parameter Symbol	Parameter Description		B Devices Min.	B Devices Max.	C Devices Min.	C Devices Max.	E Devices Min.	E Devices Max.	Units
Read Cycle										
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		200		ns
2	t_A	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		200	ns
3	t_{CO}	Chip Select LOW to Data Out Valid (Note 6)	Am9114		120		100		70	ns
			Am9124		420		280		185	ns
4	t_{CX}	Chip Select LOW to Data Out On		10		10		10		ns
5	t_{OTD}	Chip Select HIGH to Data Out Off			100		80		60	ns
6	t_{OHA}	Address Unknown to Data Out Unknown Time		50		50		50		ns
Write Cycle										
7	t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		200		ns
8	t_W	Write Enable LOW to Write Enable HIGH Time (Note 5)	Am9114	200		150		120		ns
			Am9124	250		200		150		ns
9	t_{WR}	Write Enable HIGH to Address Do Not Care Time		0		0		0		ns
10	t_{OTW}	Write Enable LOW to Data Out Off Delay			100		80		60	ns
11	t_{DW}	Data In Valid to Write Enable HIGH Time		200		150		120		ns
12	t_{DH}	Write Enable HIGH to Data In Do Not Care Time		0		0		0		ns
13	t_{AW}	Address Valid to Write Enable LOW Time		0		0		0		ns
14	t_{PD}	Chip Select HIGH to Power LOW Delay (Am9124 only) (Note 7)			200		150		100	ns
15	t_{PU}	Chip Select LOW to Power HIGH Delay (Am9124 only) (Note 7)		0		0		0		ns
16	t_{CW}	Chip Select LOW to Write Enable HIGH Time (Note 5)	Am9114	200		150		120		90
			Am9124	250		200		150		ns

Notes: See notes following DC Characteristics table

*See the last page of this spec for Group A Subgroup Testing information.

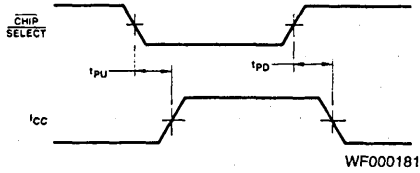
4

SWITCHING WAVEFORMS



WF000171

Power-Down Waveform (Am9124 Only)



WF000181

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{PD}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups	Parameter Symbol	Subgroups
t_{RC}	7, 8, 9, 10, 11	t_{WR}	7, 8, 9, 10, 11
t_A	7, 8, 9, 10, 11	t_{OTW}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11	t_{DW}	7, 8, 9, 10, 11
t_{CX}	7, 8, 9, 10, 11	t_{DH}	7, 8, 9, 10, 11
t_{OTD}	7, 8, 9, 10, 11	t_{AW}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11	t_{PD}	7, 8, 9, 10, 11
t_{WC}	7, 8, 9, 10, 11	t_{PU}	7, 8, 9, 10, 11
t_W	7, 8, 9, 10, 11	t_{CW}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test Conditions are selected at AMD's option.

Am9122

256 x 4 Static RAM

DISTINCTIVE CHARACTERISTICS

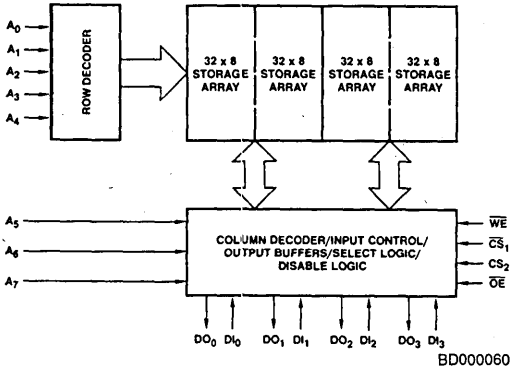
- High-performance replacement for 93422/93L422
- Fast access times — as low as 25 ns
- Low-power dissipation
  - Low power: 440 mW (Commercial)
    495 mW (Military)
- Single 5-volt power supply — ±10% tolerance both Commercial and Military

GENERAL DESCRIPTION

The Am9122/Am91L22 series is a MOS pin-for-pin and functional replacement for the 93422/93L422 bipolar memories. These devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 25 ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

The Am9122/91L22 employs an output enable and two chip enable inputs to give the user better data control. High noise immunity, high output drive (4 TTL loads) and TTL logic voltage levels allow easy conversion from bipolar to MOS. 10% power supply tolerances give better margins in the memory system.

BLOCK DIAGRAM



BD000060

MODE SELECT TABLE

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	D_0–D_3		
X	H	X	X	X	Hi-Z	Not Selected
X	X	L	X	X	Hi-Z	Not Selected
L	L	H	H	X	O_0–O_3	Read Stored Data
X	L	H	L	L	Hi-Z	Write "0"
X	L	H	L	H	Hi-Z	Write "1"
H	L	H	H	X	Hi-Z	Output Disabled
H	L	H	L	L	Hi-Z	Write "0" (Output Disabled)
H	L	H	L	H	Hi-Z	Write "1" (Output Disabled)

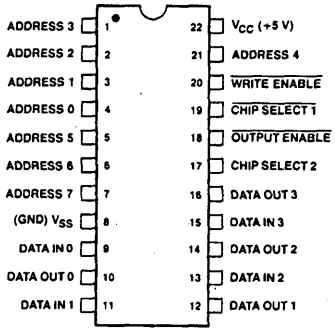
H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)
Hi-Z = High Impedance

PRODUCT SELECTOR GUIDE

Part Number		Am9122-25	Am9122-35	Am91L22-35	Am91L22-45
Maximum Access Time (ns)		25	35	35	45
Maximum Operating Current (mA)	0° to +70°C	120	120	80	80
	−55° to +125°C	N/A	135	N/A	90

Publication # 01547 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

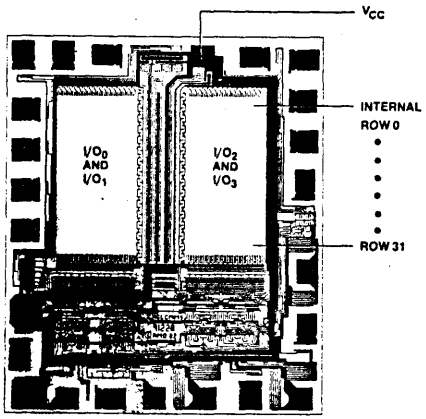


CD000111

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A_0	A_0
A_1	A_1
A_2	A_2
A_3	A_3
A_4	A_4
A_5	A_5
A_6	A_6
A_7	A_7



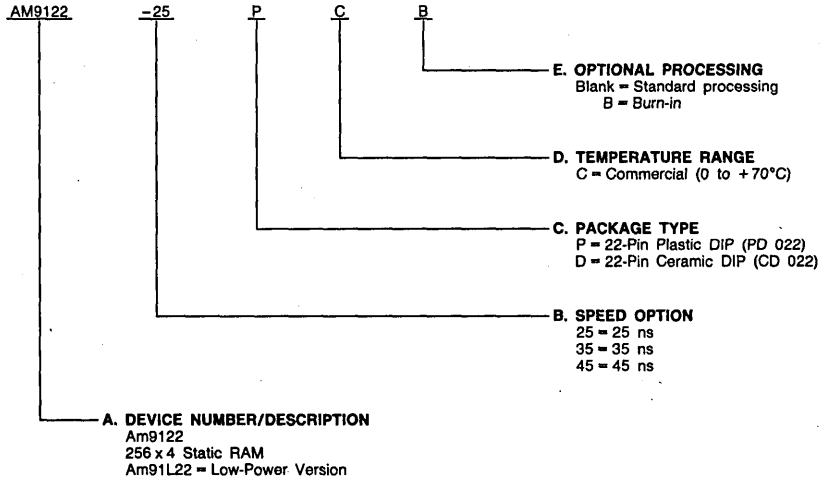
4

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9122-25	DC, DCB, PC, PCB
AM91L22-35	
AM9122-35	
AM91L22-45	

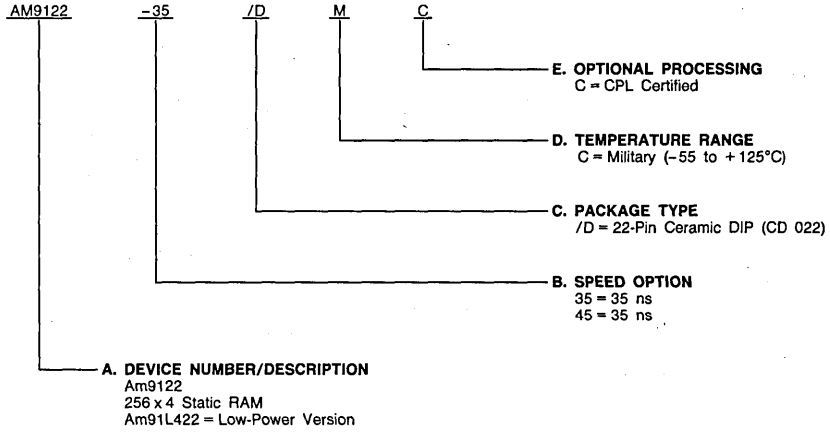
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of packages, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for CPL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9122-35	/DMC
AM91L22-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations.

4

PIN DESCRIPTION

$A_0 - A_7$ Address (Input)
The 8 address inputs select one of the 256 4-bit words in the RAM.

$\overline{CS_1}$ Chip Select 1 (Input)

CS_2 Chip Select 2 (Input)
$\overline{CS_1}$ is active LOW and CS_2 is active HIGH. The device can be accessed only when both Chip Selects are active. If either Chip Select is not active, the device is deselected and the outputs will be in a high-impedance state.

$\overline{WE}$ Write Enable Input
$\overline{WE}$ controls read and write operations. When $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, data will be present at the data outputs. When $\overline{WE}$ is LOW, data present on the data inputs will be written into the selected memory location. The data outputs will be in a high-impedance state.

$\overline{OE}$ Output Enable (Input)
$\overline{OE}$ controls the state of the data outputs in conjunction with Chip Select and $\overline{WE}$.

$DI_0 - DI_3$ Data IN (Input)
Data inputs to the RAM.

$DO_0 - DO_3$ Data Out (Output)
Data output from the RAM. The data output will be in a high-impedance state when either Chip Select is not active or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

V_{CC} Power Supply +5 Volts

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 V to +7.0 V
DC Input Voltage ..... −0.5 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

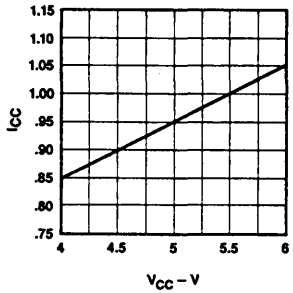
Parameter Symbol	Parameter Description	Test Conditions		Am91L22-35 Am91L22-45 Min.	Typ.	Max.	Am9122-25 Am9122-35 Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −5.2 mA	2.4			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA			0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.1		V_{CC}	2.1		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−2.5		0.8	−2.5		0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		−10			−10			μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				10			10	μA
V_{CD}	Input Diode Clamp Voltage					Note 3			Note 3	Volts
I_{OFF}	Output Current (Hi-Z)	$V_{OL} \leq V_{OUT} \leq V_{OH}$ Output Disabled	T_A = Max.	−10		10	−10		10	μA
I_{OS}	Output Short Circuit Current (Note 4)	V_{CC} = Max., V_{OUT} = GND	Commercial			−85			−85	mA
			Military			−100			−100	
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	T_A = 0°C			80			120	mA
			T_A = −55°C			90			135	
C_{IN}	Input Capacitance V_{IN} = O V	T_A = 25°C, f=1 MHz V_{CC} = 4.5 V (Note 5)			3	5		3	5	pF
C_{OUT}	Output Capacitance V_{OUT} = 0 V				5	8		5	8	

Notes:
1. Absolute Maximum Rating are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the "instant-ON" case temperature.
3. The NMOS process does not provide a clamp diode. However, the Am9122/91L22 is insensitive to −3 V DC input levels and −5 V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
6. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in A. under Switching Test Circuits.
7. Transition is measured at V_{OH} −500 mV or V_{OL} +500 mV levels on the output from 1.5 V level on the input with load shown in B. under Switching Test Circuits.
8. T_w measured at t_{wsa} = Min.; t_{wsa} measured at t_w = Min.

*See the last page of this spec for Group A Subgroup Testing information.

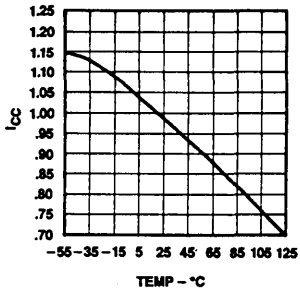
TYPICAL AND AC CHARACTERISTICS

Normalized I_{CC} versus Supply Voltage



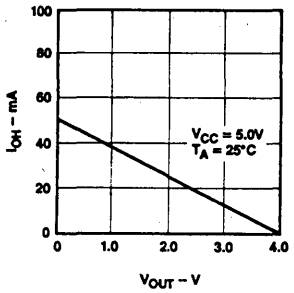
OP000120

Normalized I_{CC} versus Ambient Temperature



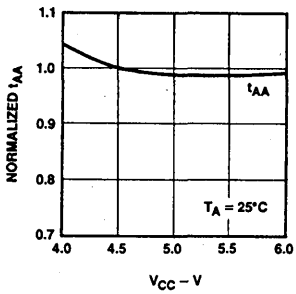
OP000130

Output Source Current versus Output Voltage



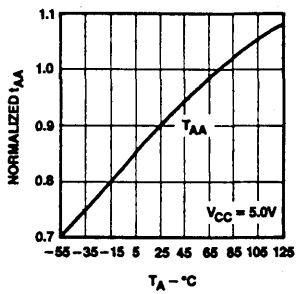
OP000140

Normalized Access Time versus Supply Voltage



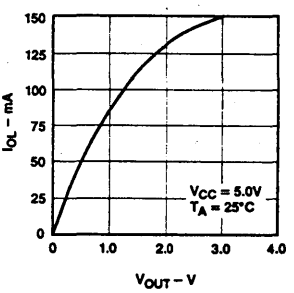
OP000150

Normalized Access Time versus Ambient Temperature



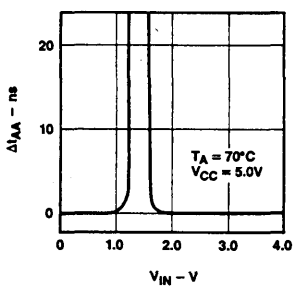
OP000160

Output Sink Current versus Output Voltage



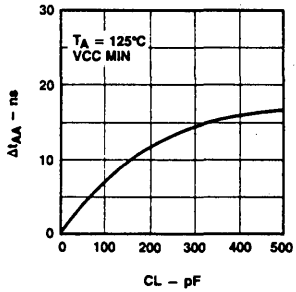
OP000170

Access Time Change versus Input Voltage



OP000180

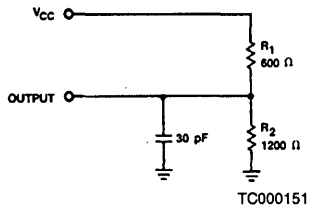
Access Time Change versus Output Loading



OP000190

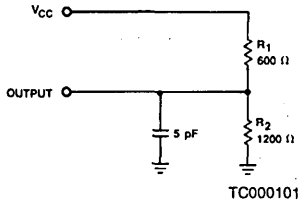
4

SWITCHING TEST CIRCUITS



TC000151

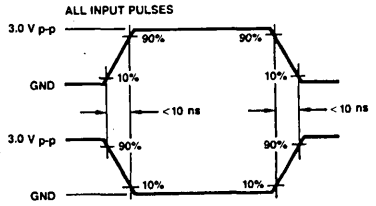
A.



TC000101

B.

SWITCHING TEST WAVEFORM



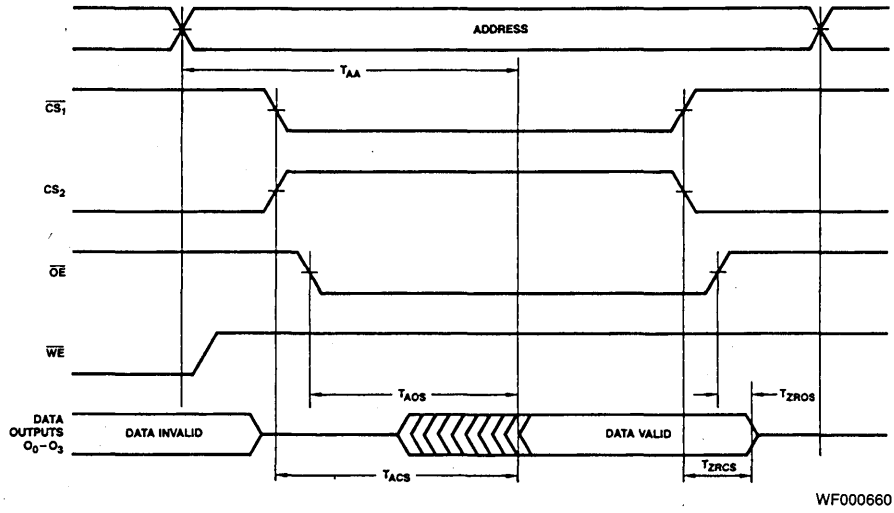
TW000021

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 6, 7, 8)*

No.	Parameter Symbol	Parameter Description	Am9122-25		Am91L22-35 Am9122-35		Am91L22-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACS}	Chip Select Time		15		25		30	ns
2	t_{ZRCS}	Chip Select to Hi-Z (Note 7)		20		30		30	ns
3	t_{AOS}	Output Enable Time		15		25		30	ns
4	t_{ZROS}	Output Enable to Hi-Z (Note 7)		20		30		30	ns
5	t_{AA}	Address Access Time		25		35		45	ns
6	t_{ZWS}	Write Disable to Hi-Z (Note 7)		20		30		35	ns
7	t_{WR}	Write Recovery Time		20		25		40	ns
8	t_W	Write Pulse Width (Note 8)	15		25		30		ns
9	t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns
10	t_{WHD}	Data Hold Time After Write	5		5		5		ns
11	t_{WSA}	Address Setup Time (Note 8)	5		5		10		ns
12	t_{WHA}	Address Hold Time	5		5		5		ns
13	t_{WSCS}	Chip Select Setup Time	5		5		5		ns
14	t_{WHCS}	Chip Select Hold Time	5		5		5		ns

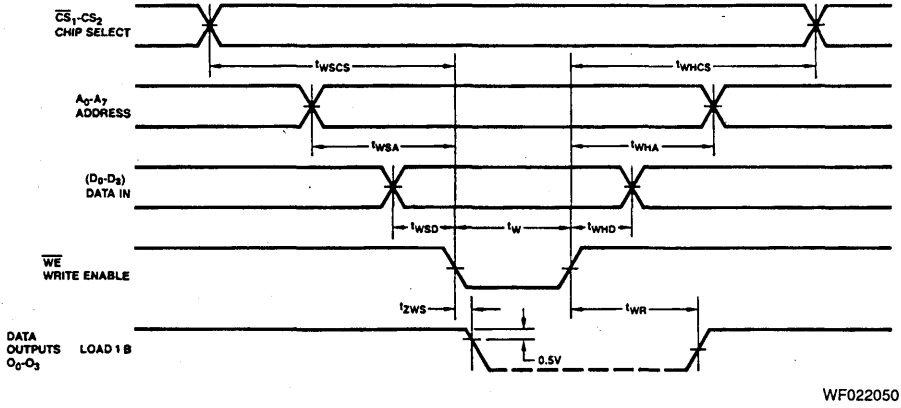
Notes: See notes following DC CHaracteristics table.
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF000660

Read Mode



WF022050

Write Mode

(All above measurements implemented to 1.5 V unless otherwise stated.)

Note: Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst-case limits are not violated.

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{OFF}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACS}	7, 8, 9, 10, 11	8	t_W	7, 8, 9, 10, 11
2	t_{ZRCS}	7, 8, 9, 10, 11	9	t_{WSD}	7, 8, 9, 10, 11
3	t_{AOS}	7, 8, 9, 10, 11	10	t_{WHD}	7, 8, 9, 10, 11
4	t_{ZROS}	7, 8, 9, 10, 11	11	t_{WSA}	7, 8, 9, 10, 11
5	t_{AA}	7, 8, 9, 10, 11	12	t_{WHA}	7, 8, 9, 10, 11
6	t_{ZWS}	7, 8, 9, 10, 11	13	t_{WSCS}	7, 8, 9, 10, 11
7	t_{WR}	7, 8, 9, 10, 11	14	t_{WHCS}	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9128

2048 x 8 Static RAM

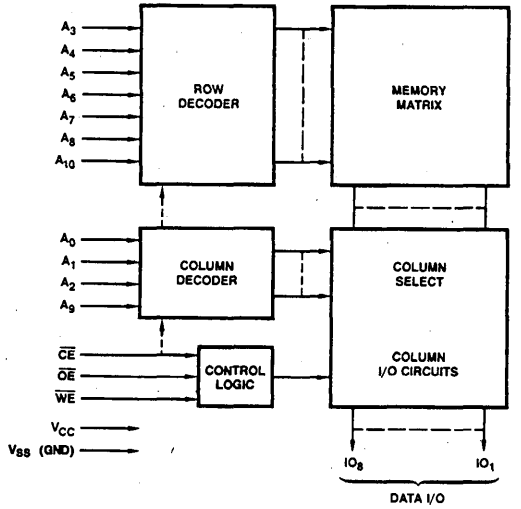
DISTINCTIVE CHARACTERISTICS

- Logic voltage levels compatible with TTL
- Three-state output buffers and common I/O
- I_{CC} Max., as low as 100 mA
- T_{AA}/T_{ACS} as low as 70 ns
- Power-Down mode (I_{SB} as low as 15 mA)

GENERAL DESCRIPTION

The Am9128 is a 16,384-bit Static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5 V supply simplify system designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROMs).

BLOCK DIAGRAM



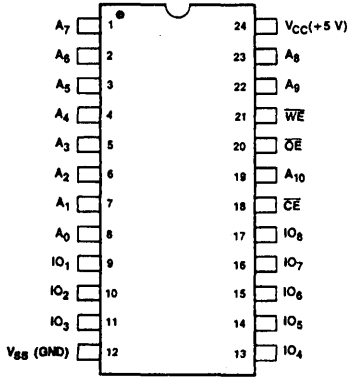
BD000281

PRODUCT SELECTOR GUIDE

Part Number		Am9128-70	Am9128-90	Am9128-10	Am9128-12	Am9128-15	Am9128-20
Maximum Access Time (ns)		70	90	100	120	150	200
Maximum Operating Current (mA)	0 to 70°C	140	N/A	120	N/A	100	140
	−55° to 125°C	N/A	180	N/A	150	150	150
Maximum Standby Current (mA)	0° to 70°C	30	N/A	15	N/A	15	30
	−55° to 125°C	N/A	30	N/A	30	30	30

Publication # 02050 | Rev. D | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

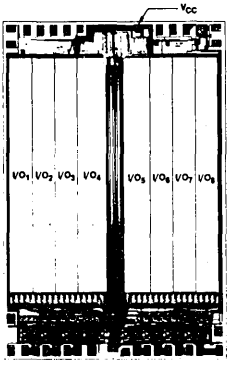


CD000121

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

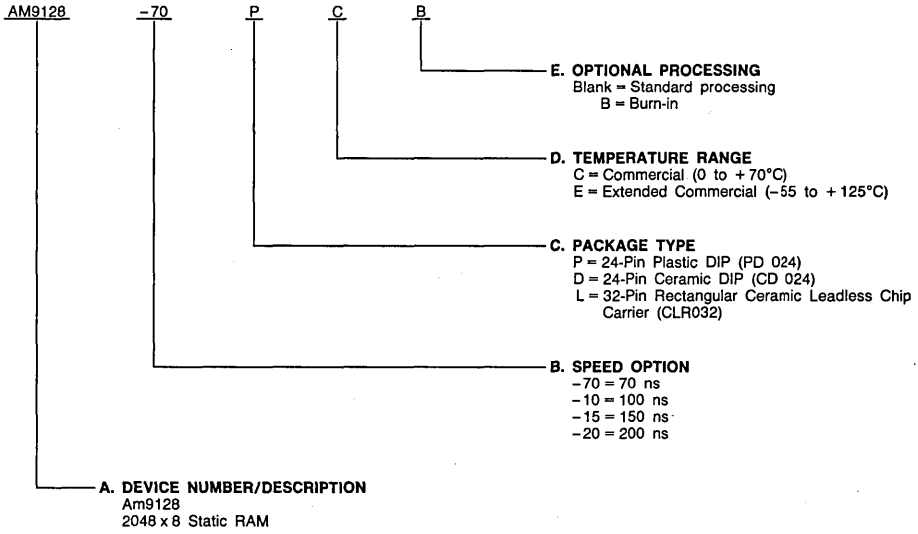
Address Designators	
External	**Internal**
A_3	AX_0
A_4	AX_1
A_5	AX_2
A_6	AX_3
A_7	AX_4
A_8	AX_5
A_{10}	AX_6
A_0	AY_0
A_1	AY_1
A_2	AY_2
A_9	AY_3



ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
9128-70	PC, DC, DCB, DE, DEB, LC, LCB
9128-10	
9128-15	
9128-20	

Valid Combinations

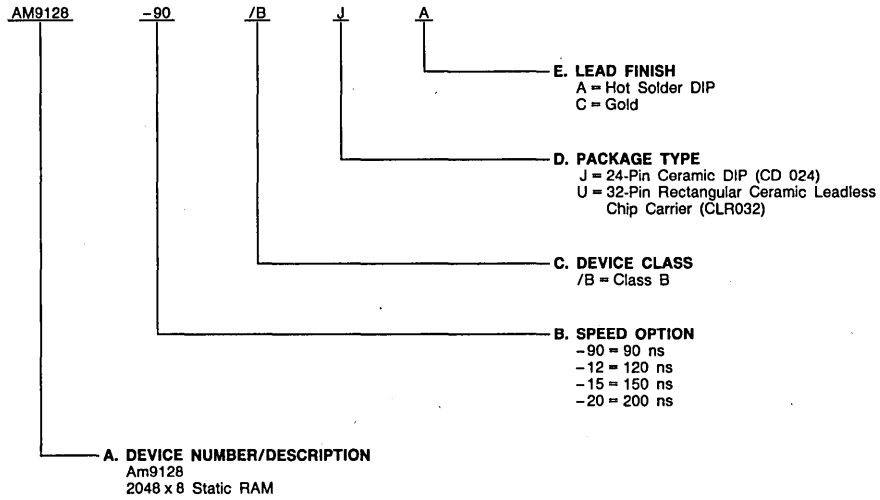
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
9128-90	/BJA, /BUC
9128-12	
9128-15	
9128-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{10}$ Addresses (Input)
The 10-bit field presented at the address inputs selects one of the 2048 memory locations to be read from — or written into — via the data lines.

$I/O_1 - I/O_8$ Data In/Out Port (Input/Output)
If $\overline{WE}$ is LOW, the data represented on the I/O lines can be written into the selected memory location. If $\overline{WE}$ is HIGH, the I/O lines represent the data read from the selected memory location.

$\overline{CE}$ Chip Enable (Input, Active LOW)
Read and Write cycles can be executed only when $\overline{CE}$ is LOW.

$\overline{WE}$ Write Enable (Input, Active LOW)
Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

$\overline{OE}$ Output Enable (Input, Active LOW)
Read cycles can be executed only when $\overline{OE}$ is LOW.

ABSOLUTE MAXIMUM RATINGS (Note 11)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
Signal Voltage with
Respect to Ground ..... −3.0 V to +7.0 V
Power Description ..... 1.0 W
DC Output Current ..... 10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.5 V to +5.5 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 3)*

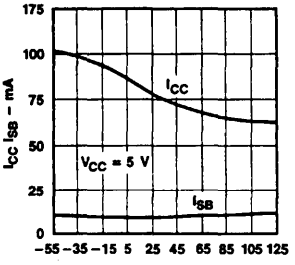
Parameter Symbol	Parameter Description	Test Conditions		Am9128-90 Am9128-10 Min.	Am9128-90 Am9128-10 Max.	Am9128-15 Min.	Am9128-15 Max.	Am9128-70 Am9128-12 Am9128-20 Min.	Am9128-70 Am9128-12 Am9128-20 Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	−2		−2		−2		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V		4		4		4		mA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1.0	2.0	V_{CC} + 1.0	2.0	V_{CC} + 1.0	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	−0.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10		10	μA
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Output Disabled			10		10		10	μA
C_{IN}	Input Capacitance (Note 12)	Test Frequency = 1.0 MHz, T_A = 25°C, All pins at 0	V_{CC} = 5.0 V		6		6		6	pF
$C_{I/O}$	Input/Output Capacitance (Note 12)				7		7		7	pF
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CE} \leq V_{IL}$ Outputs Open	COM'L		120		100		140	mA
			MIL		180		150		150	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	COM'L		15		15		30	mA
			MIL		30		30		30	
I_{PO}	Peak Power On Current (Note 12)	V_{CC} = GND to V_{CC} Max. $\overline{CE} \geq V_{IH}$ (Note 2)	COM'L		15		15		30	mA
			MIL		30		30		30	

Notes:
1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. A pull up resistor to V_{CC} on the $\overline{CE}$ input is required during power up to keep the device deselected, otherwise I_{PO} will exceed values given.
3. Ambient temperature is defined as the case temperature.
4. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ}.
5. $\overline{WE}$ is HIGH for read cycle.
6. Device is continuously selected, $\overline{CE} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
8. $\overline{OE} = V_{IL}$.
9. C_L = 30 pF.
10. Transition is measured from 1.4 V on the input to 0.9 V and 1.9 V on the output using the load shown under Switching Test Circuit.
11. The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling, and use to avoid exposure to excessive voltages.
12. The parameter is guaranteed by characterization, but is not tested.

*See the last page of this spec for Group A Subgroup Testing information.

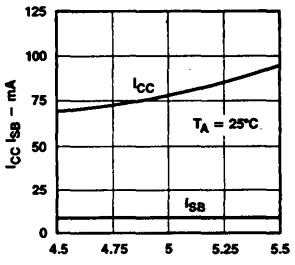
TYPICAL DC and AC CHARACTERISTICS

Supply Current Versus Ambient Temperature



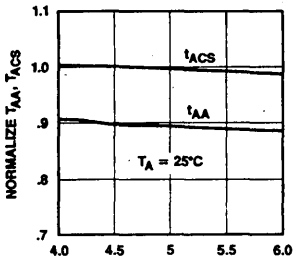
OP000640

Supply Current Versus Supply Voltage



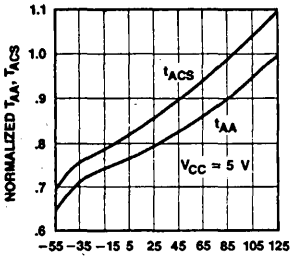
OP000650

Normalized Access Time Versus Supply Voltage



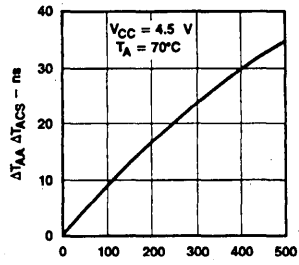
OP000660

Normalized Access Time Versus Ambient Temperature



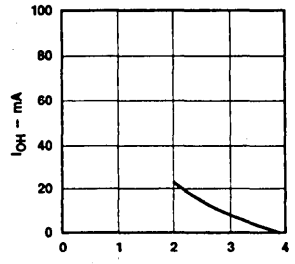
OP000670

Access Time Change Versus Output Loading



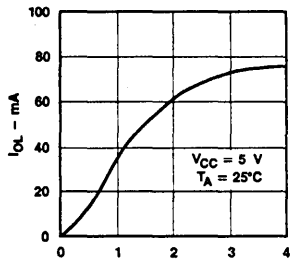
OP000680

Output Source Current Versus Output Voltage



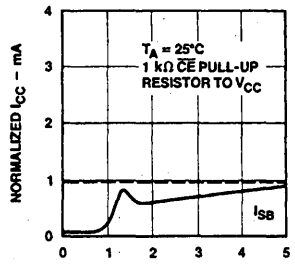
OP000690

Output Sink Current Versus Output Voltage



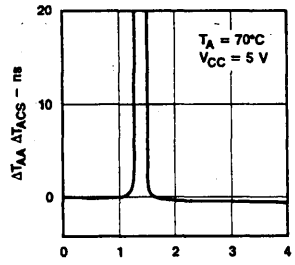
OP000700

Typical Power-On Current Versus Power Supply



OP000710

Access Time Change Versus Input Voltage

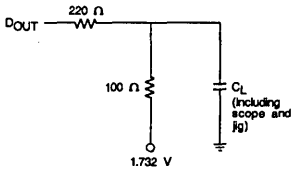


OP000720

SWITCHING TEST CONDITIONS

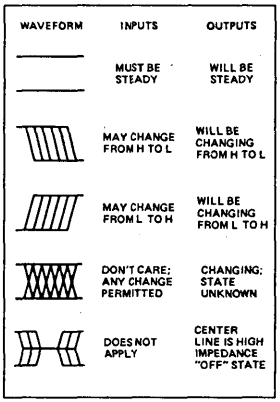
Input Pulse Levels	.4 to 2.4 V
Input Rise and Fall Times	10 ns
Input Timing Reference Levels	1.4 V
Output Timing Reference Levels	1.4 V

SWITCHING TEST CIRCUIT



TC003700

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Cont'd.)

No.	Parameter Symbol	Parameter Description		Am9128-70 Min.	Am9128-70 Max.	Am9128-90 Min.	Am9128-90 Max.	Am9128-10 Min.	Am9128-10 Max.	Units
Read Cycle										
1	t_{RC}	Read Cycle Time		70		90		100		ns
2	t_{ACC}	Address Access Time (Note 9)			70		90		100	ns
3	t_{ACS}	Chip Select Access Time (Note 9)			70		90		100	ns
4	t_{OE}	Output Enable Time (Note 9)	COM'L		40		N/A		50	ns
			MIL		N/A		50		N/A	
5	t_{OH}	Output Hold Time from Address Change		5		5		5		ns
6	t_{CLZ}	Output in Low-Z from $\overline{CE}$ (Notes 4, 10)		5		5		5		ns
7	t_{CHZ}	Output in Hi-Z from $\overline{CE}$ (Notes 4, 10)			35		40		40	ns
8	t_{OLZ}	Output in Low-Z from $\overline{OE}$ (Notes 4, 10)		5		5		5		ns
9	t_{OHZ}	Output in Hi-Z from $\overline{OE}$ (Notes 4, 10)			30		35		35	ns
10	t_{PU}	Chip Selection to Power-Up Time (Note 12)		0		0		0		ns
11	t_{PD}	Chip Deselection to Power-Down Time (Note 12)			40		45		50	ns
Write Cycle										
12	t_{WC}	Write Cycle Time		70		90		100		ns
13	t_{CW}	Chip Selection to End of Write (Note 1)	0 to +70°C	60		N/A		90		ns
			−55 to −125°C	N/A		80		N/A		
14	t_{AS}	Address Setup Time		5		10		10		ns
15	t_{WP}	Write Pulse Width (Note 1)		40		55		60		ns
16	t_{WR}	Write Recovery Time		5		5		5		ns
17	t_{DS}	Data Setup Time		30		35		40		ns
18	t_{DH}	Data Hold Time		5		5		5		ns
19	t_{WLZ}	Output in Low-Z from $\overline{WE}$ (Notes 4, 10)		5		5		5		ns
20	t_{WHZ}	Output in Hi-Z from $\overline{WE}$ (Notes 4, 10)			30		35		35	ns
21	t_{AW}	Address to End of Write		65		80		80		ns

Notes: See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

4

SWITCHING CHARACTERISTICS*

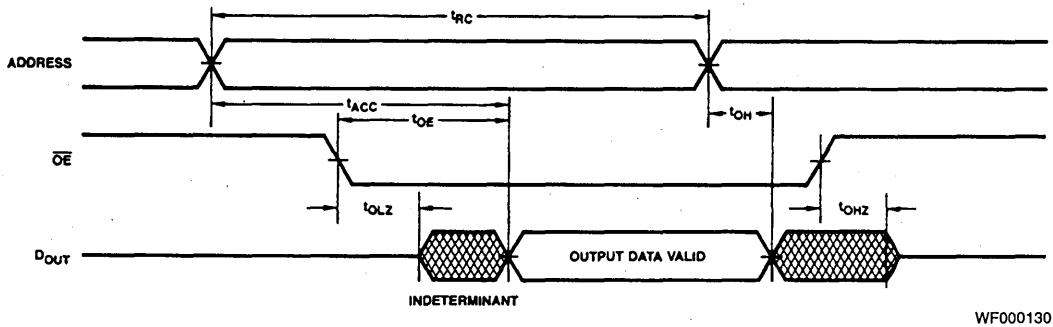
No.	Parameter Symbol	Parameter Description		Am9128-12 Min.	Am9128-12 Max.	Am9128-15 Min.	Am9128-15 Max.	Am9128-20 Min.	Am9128-20 Max.	Units
Read Cycle										
1	t_{RC}	Read Cycle Time		120		150		200		ns
2	t_{ACC}	Address Access Time (Note 9)			120		150		200	ns
3	t_{ACS}	Chip Select Access Time (Note 9)			120		150		200	ns
4	t_{OE}	Output Enable Time (Note 9)	COM'L		N/A		60		70	ns
			MIL		70		70		80	
5	t_{OH}	Output Hold Time from Address Change		5		5		5		ns
6	t_{CLZ}	Output in Low-Z from $\overline{CE}$ (Notes 4, 10)		5		5		5		ns
7	t_{CHZ}	Output in Hi-Z from $\overline{CE}$ (Notes 4, 10)			50		55		55	ns
8	t_{OLZ}	Output in Low-Z from $\overline{OE}$ (Notes 4, 10)		5		5		5		ns
9	t_{OHZ}	Output in Hi-Z from $\overline{OE}$ (Notes 4, 10)			45		50		50	ns
10	t_{PU}	Chip Selection to Power-Up Time (Note 12)		0		0		0		ns
11	t_{PD}	Chip Deselection to Power-Down Time (Note 12)			55		60		60	ns
Write Cycle										
12	t_{WC}	Write Cycle Time		120		150		200		ns
13	t_{CW}	Chip Selection to End of Write (Note 1)	COM'L	N/A		120		150		ns
			MIL	105		130		160		
14	t_{AS}	Address Setup Time		10		20		20		ns
15	t_{WP}	Write Pulse Width (Note 1)		70		85		100		ns
16	t_{WR}	Write Recovery Time		5		5		5		ns
17	t_{DS}	Data Setup Time		45		50		60		ns
18	t_{DH}	Data Hold Time		5		5		5		ns
19	t_{WLZ}	Output in Low-Z from $\overline{WE}$ (Notes 4, 10)		5		5		5		ns
20	t_{WHZ}	Output in Hi-Z from $\overline{WE}$ (Notes 4, 10)			50		50		50	ns
21	t_{AW}	Address to End of Write		105		120		120		ns

Notes: See notes following DC Characteristics table.

*See the last page of this spec for Group A Subgroup Testing information.

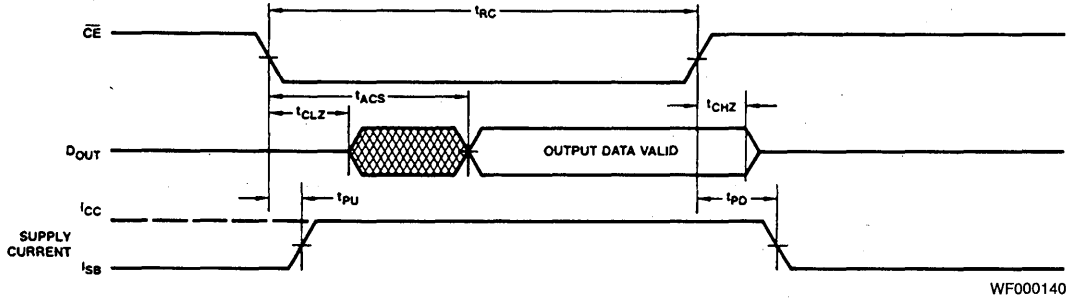
SWITCHING WAVEFORMS (Cont'd.)

READ CYCLE NO. 1 (Notes 5, 6)



WF000130

READ CYCLE 2 (Notes 5, 7, 8)



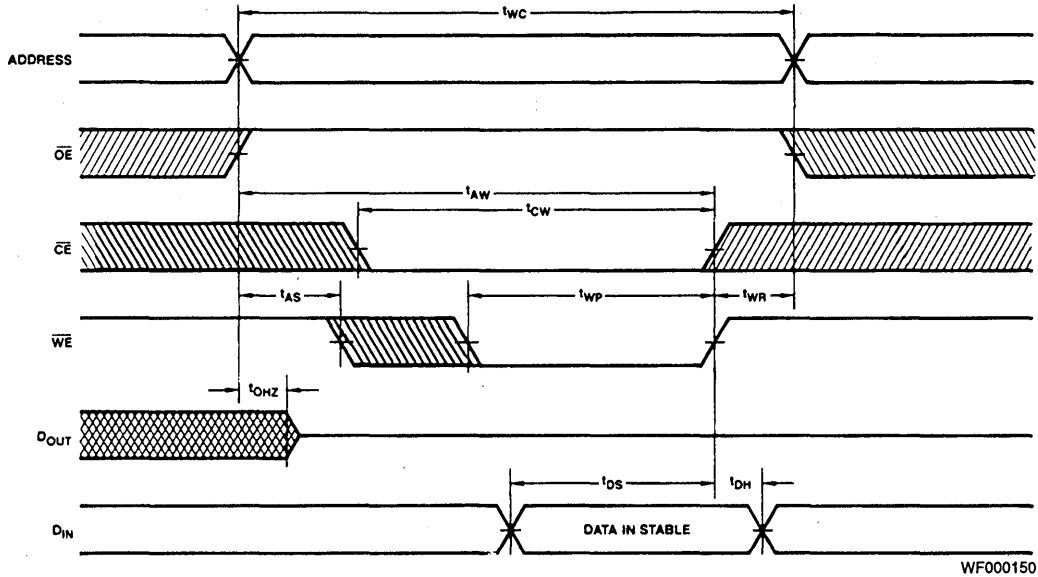
WF000140

Notes: See notes following DC Characteristics table.

4

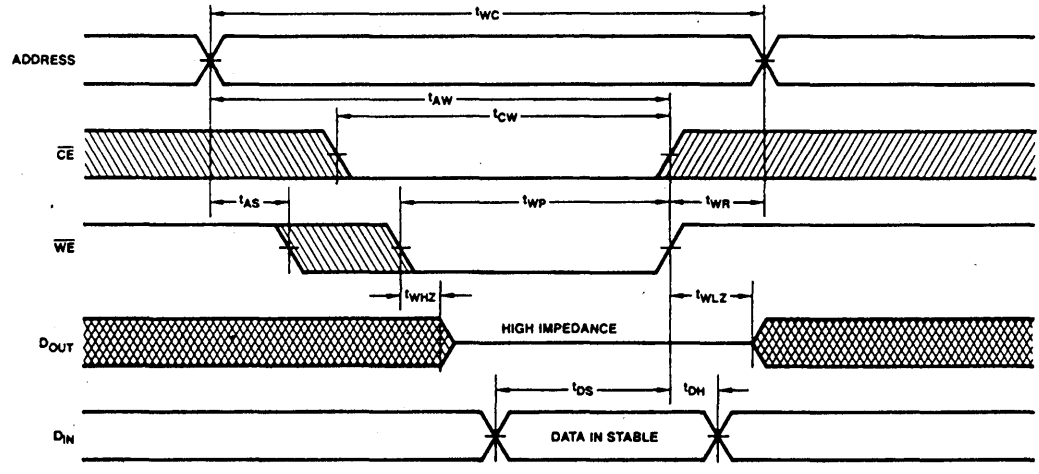
SWITCHING WAVEFORMS

WRITE CYCLE 1



WF000150

WRITE CYCLE NO. 2 (Notes 7, 8)



WF000160

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{RC}	7, 8, 9, 10, 11	13	t_{CW}	7, 8, 9, 10, 11
2	t_{ACC}	7, 8, 9, 10, 11	14	t_{AS}	7, 8, 9, 10, 11
3	t_{ACS}	7, 8, 9, 10, 11	15	t_{WP}	7, 8, 9, 10, 11
4	t_{OE}	7, 8, 9, 10, 11	16	t_{WR}	7, 8, 9, 10, 11
5	t_{OH}	7, 8, 9, 10, 11	17	t_{DS}	7, 8, 9, 10, 11
6	t_{CLZ}	7, 8, 9, 10, 11	18	t_{DH}	7, 8, 9, 10, 11
7	t_{CHZ}	7, 8, 9, 10, 11	19	t_{WLZ}	7, 8, 9, 10, 11
8	t_{OLZ}	7, 8, 9, 10, 11	20	t_{WHZ}	7, 8, 9, 10, 11
9	t_{OHZ}	7, 8, 9, 10, 11	21	t_{AW}	7, 8, 9, 10, 11
12	t_{WC}	7, 8, 9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9150/Am91L50

1024 x 4 High-Speed Static R/W RAM

DISTINCTIVE CHARACTERISTICS

- 1024 x 4 organization
- High speed – 20 ns Max. access time
- Separate data inputs and outputs
- Memory reset function
- High density SLIM 24-pin 300-MIL package
- Three-state output buffers
- Single +5 V power supply ±10%
- Low-power version

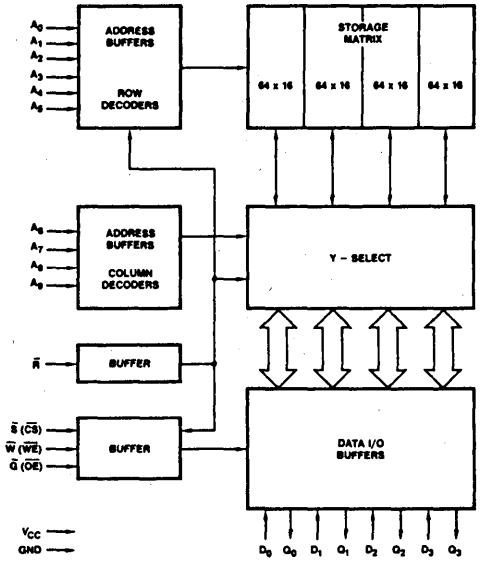
GENERAL DESCRIPTION

The Am9150 is a high-performance, static, n-channel, read/write, random-access memory organized as 1024 x 4. It features single 5 V supply operation, TTL-compatible input and output levels, and separate input and output pins for improved system performance and ease of use.

The Am9150 also incorporates a reset feature which will reset the entire contents of the memory to logical LOW in two cycle times by controlling $\overline{R}$ ($\overline{RESET}$) and $\overline{S}$ ($\overline{CS}$).

The Am9150 has four control signals $\overline{R}$, $\overline{S}$, $\overline{W}$ and $\overline{G}$. The $\overline{S}$ input controls read, write and reset operations of the device and provides for easy selection of an individual device when the outputs are tied together. The $\overline{W}$ ($\overline{WE}$) input controls the normal read and write operations, and the $\overline{G}$ ($\overline{OE}$) controls the state of the outputs.

BLOCK DIAGRAM



BD005261

MODE SELECT TABLE

Inputs				Outputs	Mode
$\overline{S}$	$\overline{W}$	$\overline{G}$	$\overline{R}$		
H	X	X	X	Hi-Z	Not Selected
L	H	X	L	Hi-Z	Reset*
L	L	X	H	Hi-Z	Write
L	H	L	H	$Q_0 - Q_3$	Read
L	X	H	H	Hi-Z	Output Disable

H = High
L = Low
X = Don't Care

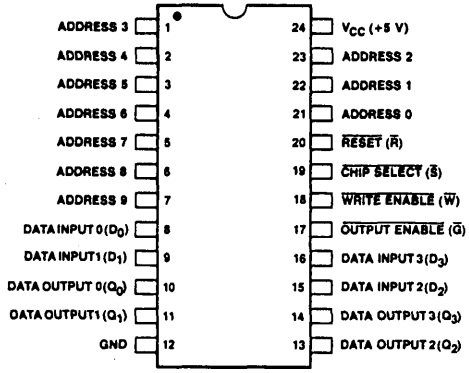
*See Reset cycle description.

PRODUCT SELECTOR GUIDE

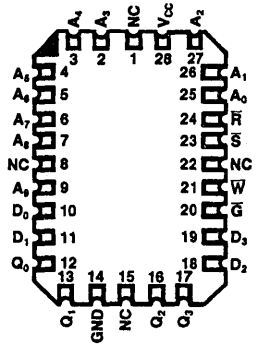
Part Number		Am9150-20	Am9150-25	Am9150-35	Am9150-45	Am91L50-25	Am91L50-35	Am91L50-45
Maximum Access Time (ns)		20	25	35	45	25	35	45
I_{CC} Max. (mA)	0°C to +70°C	180	180	180	180	130	130	130
	−55°C to +125°C	N/A	180	180	180	N/A	N/A	N/A

Publication # 04444 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



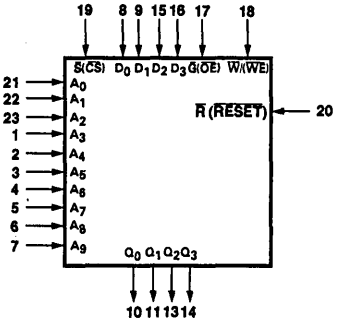
CD005963



CD005931

Note: Pin 1 is marked for orientation.

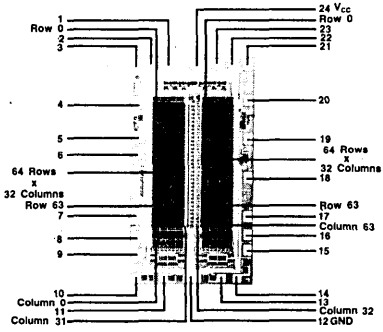
LOGIC SYMBOL
(DIP ONLY)



LS001821

Address Designators	
External	Internal
A_0	AX_0
A_1	AX_1
A_2	AX_2
A_3	AX_3
A_4	AX_4
A_5	AX_5
A_6	AY_0
A_7	AY_1
A_8	AY_2
A_9	AY_3

METALLIZATION AND PAD LAYOUT



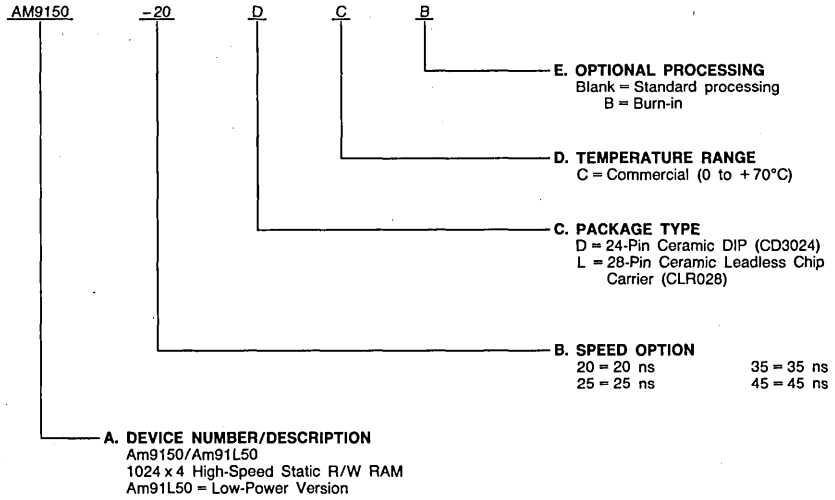
Die Size: 0.93″ x 0.163″

4

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM9150-20	DC, DCB, LC, LCB
AM9150-25	
AM9150-35	
AM9150-45	
AM91L50-25	
AM91L50-35	
AM91L50-45	

Valid Combinations

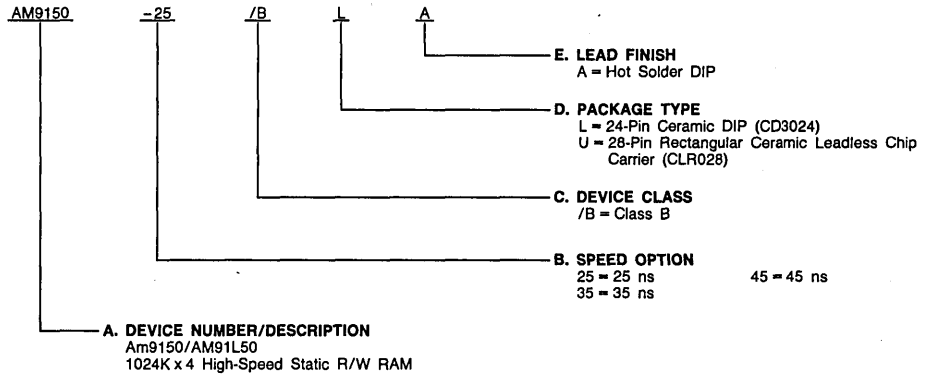
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **APL Products: A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

APL Products



Valid Combinations	
AM9150-25	/BLA
AM9150-35	/BUC
AM9150-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

PIN DESCRIPTION

$A_0 - A_9$ Address (Inputs)
The 10 address inputs select one of the 1024 4-bit words in the RAM.

$\overline{S}$ $\overline{\text{Chip Select}}$ (Input)
An active-LOW input which selects the device for operation. When $\overline{S}$ is HIGH, the device is deselected and the outputs will be in a high-impedance state.

$\overline{W}$ $\overline{\text{Write Enable}}$ (Input)
$\overline{W}$ controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, data will be present at the data outputs. When $\overline{W}$ is LOW, data present on the data inputs will be written into the selected memory location. The data outputs will be in a high-impedance state.

$\overline{G}$ $\overline{\text{Output Enable}}$ (Input)
$\overline{G}$ controls the state of the data outputs in conjunction with $\overline{S}$ and $\overline{W}$.

$D_0 - D_3$ Data Input
Data inputs to the RAM.

$Q_0 - Q_3$ Data Output
Data outputs from the RAM. The data outputs will be in a high-impedance state when either $\overline{S}$ or $\overline{G}$ are HIGH or $\overline{W}$ is LOW.

V_{CC} Power Supply +5 Volts

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage with
Respect to Ground ..... −0.5 V to +7.0 V
Signal Voltages with
Respect to Ground ..... −3.5 V to +7.0 V
Power Dissipation (Package Limitation) ..... 1.2 W
DC Output Current ..... 20 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +5.0 V ±10%

Military (M) Devices*
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +5.0 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Am9150 Min.	Am9150 Max.	Am91L50 Min.	Am91L50 Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V		−4		−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V		12		12		mA
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage			−2.5	0.8	−2.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disabled		−10	10	−10	10	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 8)			5		5	pF
C_O	Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC} $\overline{S} \leq V_{IL}$ Output Open	COM'L.		180		130	mA
			MIL.		180		N/A	
I_{OS}	Output Short Circuit Current	$GND \leq V_O \leq V_{CC}$ (Notes 7, 8)			±300		±300	mA

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, operating temperature is defined as the "instant-ON" case temperature.
3. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.
4. The internal write time of the memory is defined by the overlap of $\overline{S}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing is referenced to the rising edge of the signal that terminates the write. $\overline{R}$ must be HIGH.
5. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 1b under Switching Test Circuits.
6. $\overline{W}$ and $\overline{R}$ are HIGH for read cycle.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. This parameter is not tested, but guaranteed by characterization.

*See the last page of this spec for Group A Subgroup Testing information.

4

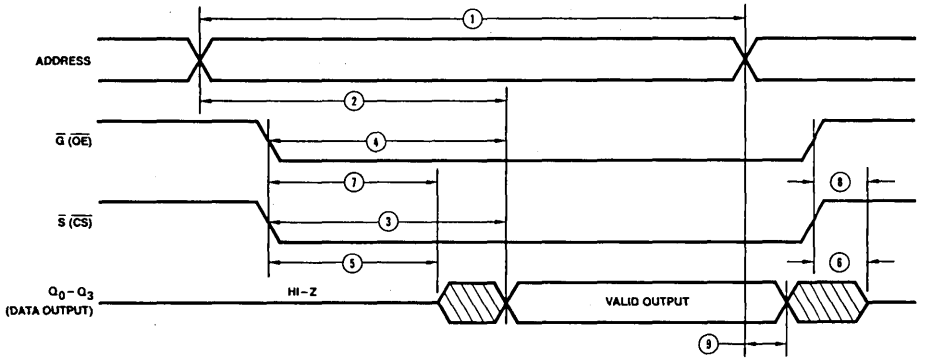
SWITCHING CHARACTERISTICS over operating range unless otherwise specified SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 3)*

No.	Parameter Symbol Standard	Parameter Symbol Alternate	Parameter Description		Am9150-20 Min.	Am9150-20 Max.	Am9150-25 Am91L50-25 Min.	Am9150-25 Am91L50-25 Max.	Am9150-35 Am91L50-35 Min.	Am9150-35 Am91L50-35 Max.	Am9150-45 Am91L50-45 Min.	Am9150-45 Am91L50-45 Max.	Units
READ CYCLE													
1	TAVAV	t_{RC}	Read Cycle Time (Note 6)		20		25		35		45		ns
2	TAVQV	t_{AA}	Address Access Time			20		25		35		45	ns
3	TSLQV	t_{ACS}	Chip Select Access Time			10		15		20		25	ns
4	TGLQV	t_{OE}	Output Enable Access Time			10		15		20		25	ns
5	TSLQX	t_{CLZ}	Chip Select LOW to Output in Low-Z (Notes 5, 8)		0		0		0		0		ns
6	TSHQZ	t_{CHZ}	Chip Select HIGH to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	30	ns
7	TGLQX	t_{OLZ}	Output Enable LOW to Output in Low-Z (Note 5, 8)		0		0		0		0		ns
8	TGHQZ	t_{OHZ}	Output Enable HIGH to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	30	ns
9	TAXQX	t_{OHA}	Output Hold after Address Change	COM'L.	3		3		3		3		ns
				MIL.	1		1		1		1		
WRITE CYCLE													
10	TAVAV	t_{WC}	Write Cycle Time (Note 4)		20		25		35		45		ns
11	TSLWH	t_{CW}	Chip Select LOW to Write Enable HIGH		10		15		20		30		ns
12	TAVWH	t_{AW}	Address Valid to End of Write		15		20		30		40		ns
13	TAVWL	t_{AS}	Address Valid to Beginning of Write		5		5		5		5		ns
14	TWLWH	t_{WP}	Write Pulse Width		10		15		20		30		ns
15	TWHAX	t_{WR}	Address Hold after End of Write		5		5		5		5		ns
16	TDVWH	t_{DW}	Data in Valid to Write Enable HIGH		10		15		20		30		ns
17	TWHDX	t_{DH}	Data Hold after End of Write		5		5		5		5		ns
18	TWLQZ	t_{WZ}	Write Enable LOW to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	30	ns
19	TWHQX	t_{OW}	Write Enable HIGH to Output in Low-Z (Notes 5, 8)		0		0		0		0		ns
RESET CYCLE													
20	TAVAV	t_{RRC}	Reset Cycle Time		40		50		70		90		ns
21	TAVRL	t_{RSA}	Address Valid to Beginning of Reset		0		0		0		0		ns
22	TWHRL	t_{RSW}	Write Enable HIGH to Beginning of Reset		0		0		0		0		ns
23	TSLRL	t_{RSCS}	Chip Select LOW to Beginning of Reset		0		0		0		0		ns
24	TRLRH	t_{RP}	Reset Pulse Width		20		20		30		40		ns
25	TRHSX	t_{RHCS}	Chip Select Hold after End of Reset		0		0		0		0		ns
26	TRHWL	t_{RHW}	Write Enable Hold after End of Reset		20		30		40		50		ns
27	TRHAX	t_{RHA}	Address Hold after End of Reset		20		30		40		50		ns
28	TRLQZ	t_{RHZ}	Reset LOW to Output in Hi-Z (Notes 5, 8)		0	15	0	20	0	25	0	35	ns
29	TRHQX	t_{RLZ}	Reset HIGH to Output in Low-Z (Notes 5, 8)		0	15	0	20	0	25	0	35	ns

Notes: See notes following DC Characteristics table.

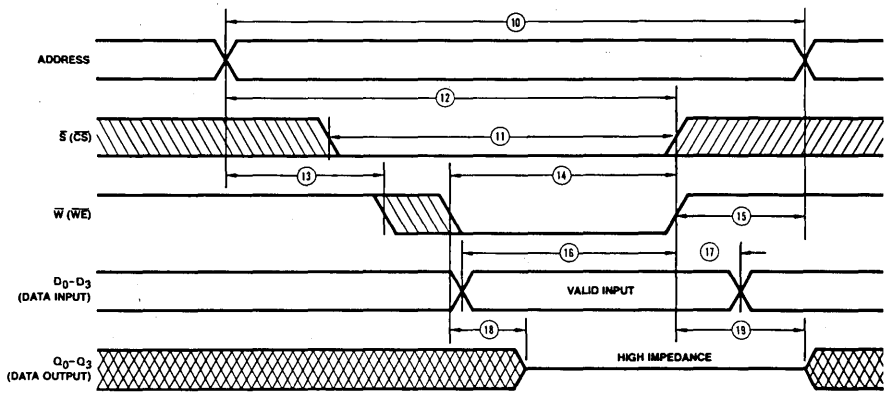
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



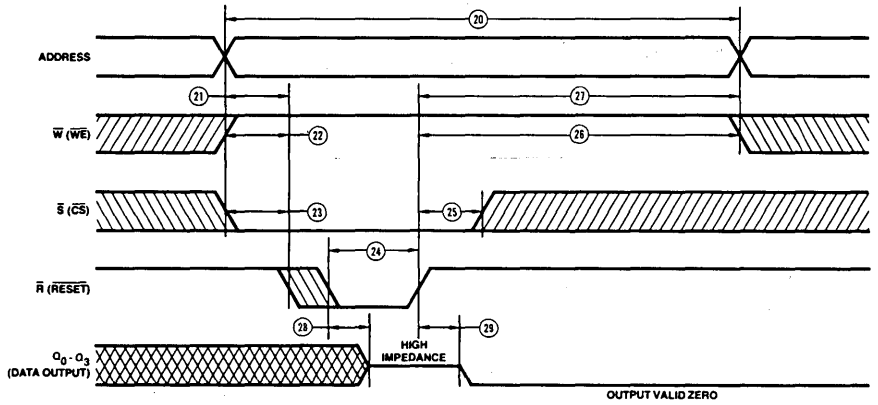
WF009890

READ CYCLE



WF009900

WRITE CYCLE



WF009910

RESET CYCLE

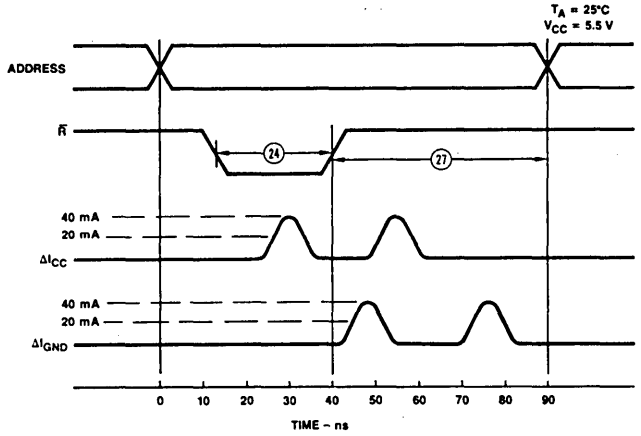
4

RESET CYCLE

The reset cycle is initiated by $\overline{R}$ going LOW for a time $\geq t_{RP}$, and is terminated by holding $\overline{R}$ HIGH for a time $\geq t_{RHA}$. The addresses to the device must be stable during the RESET cycle time. The entire contents of the RAM will be reset to ZERO regardless of the address chosen during the cycle. The control $\overline{S}$ must be $\leq V_{IL}$ maximum, and $\overline{W}$ must be $\geq V_{IH}$ minimum and it is recommended that $\overline{G}$ be $\geq V_{IH}$ minimum.

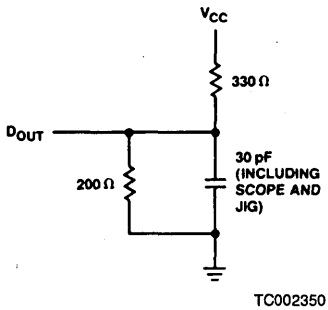
The reset cycle is normally associated with current spikes, both at V_{CC} and GND as shown in the graph. To attenuate the current spikes, an external bypass capacitor (high frequency, 0.1 μF) for each Am9150 socket is recommended.

Typical I_{CC} and I_{GND} During a Reset Cycle



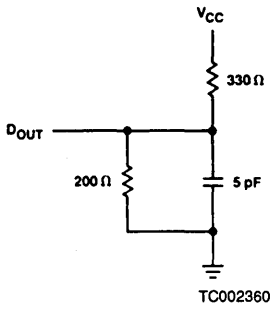
WF009920

SWITCHING TEST CIRCUITS



TC002350

Figure 1a.



TC002360

Figure 1b.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVAV (t_{RC})	7, 8, 9, 10, 11	16	TDVWH (t_{DW})	7, 8, 9, 10, 11
2	TAVQV (t_{AA})	7, 8, 9, 10, 11	17	TWHDX (t_{DH})	7, 8, 9, 10, 11
3	TSLQV (t_{ACS})	7, 8, 9, 10, 11	20	TAVAV (t_{RRC})	7, 8, 9, 10, 11
4	TGLQV (t_{OE})	7, 8, 9, 10, 11	21	TAVRL (t_{RSA})	7, 8, 9, 10, 11
9	TAXQX (t_{OHA})	7, 8, 9, 10, 11	22	TWHRL (t_{RSW})	7, 8, 9, 10, 11
10	TAVAV (t_{WC})	7, 8, 9, 10, 11	23	TSLRL (t_{RSCS})	7, 8, 9, 10, 11
11	TSLWH (t_{CW})	7, 8, 9, 10, 11	24	TRLRH (t_{RP})	7, 8, 9, 10, 11
12	TAVWH (t_{AW})	7, 8, 9, 10, 11	25	TRHSX (t_{RHCS})	7, 8, 9, 10, 11
13	TAVWL (t_{AS})	7, 8, 9, 10, 11	26	TRHWL (t_{RHW})	7, 8, 9, 10, 11
14	TWLWH (t_{WP})	7, 8, 9, 10, 11	27	TRHAX (t_{RHA})	7, 8, 9, 10, 11
15	TWHAX (t_{WR})	7, 8, 9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9151

1024 x 4 Registered Static RAM with SSR™
— On-Chip Diagnostics Capability

DISTINCTIVE CHARACTERISTICS

- High Speed – 40 ns cycle time (25 ns Max. setup and 15 ns Max. clock-to-output)
- On-chip high-speed parallel register for pipelined systems
- On-chip high-speed "Shadow" register with serial shift mode for Serial Shadow Register (SSR) Diagnostics and for loading writable control stores
- Writable Initialize register for system interrupt or reset
- Synchronous or asynchronous output enable
- 24 mA output drive capability

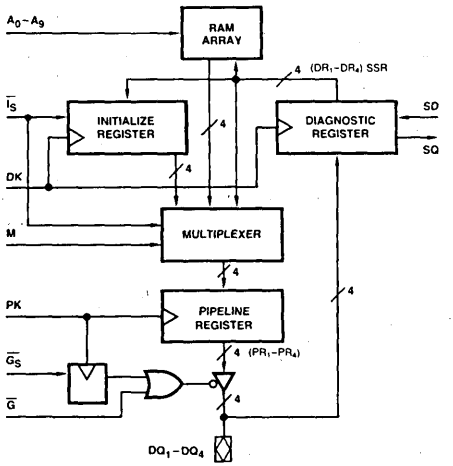
GENERAL DESCRIPTION

The Am9151 is a high-performance 1K x 4, n-channel, Registered Static RAM. The on-board registers are used for pipelined microprogrammed systems operation and for performing Serial Shadow Register (SSR) Diagnostics and Writable Control Store (WCS) loading.

The Am9151 contains three high-speed, 4-bit registers. The Pipeline register is a parallel data register in the memory array-to-output path intended for normal registered data operations. The Diagnostics register, also called a Serial Shadow Register (SSR), is used in a systematic way to control and observe the Pipeline register in order to exercise any desired system function during a diagnostic test mode. WCS loading can be accomplished by serially shifting an instruction word into the Shadow register and then clocking the data in parallel into memory. The Initialize register is used to generate any arbitrary microinstruction for system interrupt or reset.

The Am9151 operates from a single 5-volt supply and is fully TTL-compatible. The device is packaged in a slim 24-pin, 300-mil-wide DIP for the highest possible density.

BLOCK DIAGRAM



BD006270

PRODUCT SELECTOR GUIDE

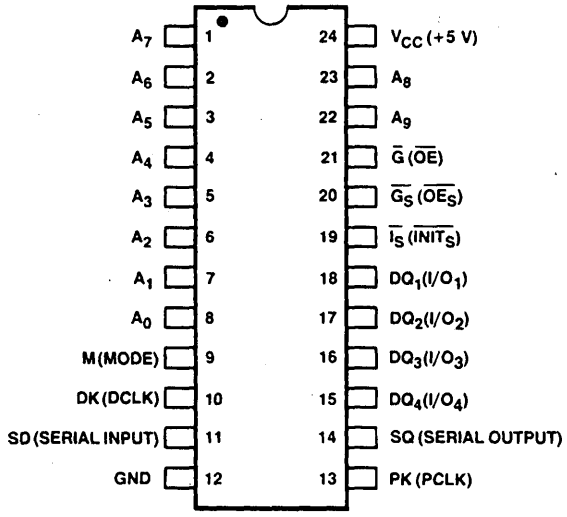
Part Number		Am9151-40	Am9151-50	Am9151-60
Minimum Cycle Time (ns)[1]		40	50	60
I_{CC} Max. (mA)	0°C to +70°C	180	180	180
	−55°C to +125°C	N/A	180	180

1. Cycle time = Address setup time plus clock to output time, including transition times.

SSR is a trademark of Advanced Micro Devices, Inc.

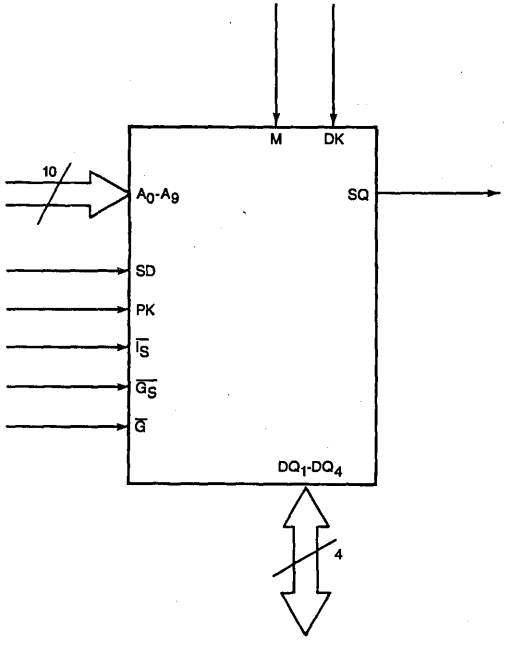
Publication # 05385 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009481

LOGIC SYMBOL



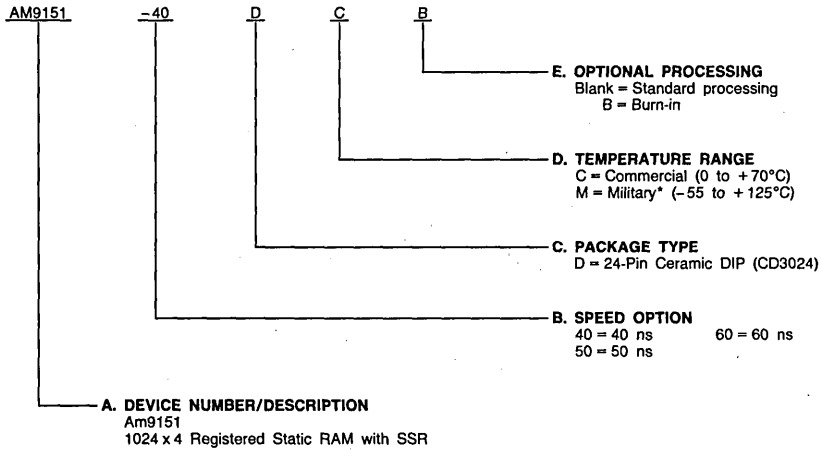
LS002440

4

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM9151-40	DC, DCB
AM9151-50	DC, DCB, DMB
AM9151-60	

Valid Combinations

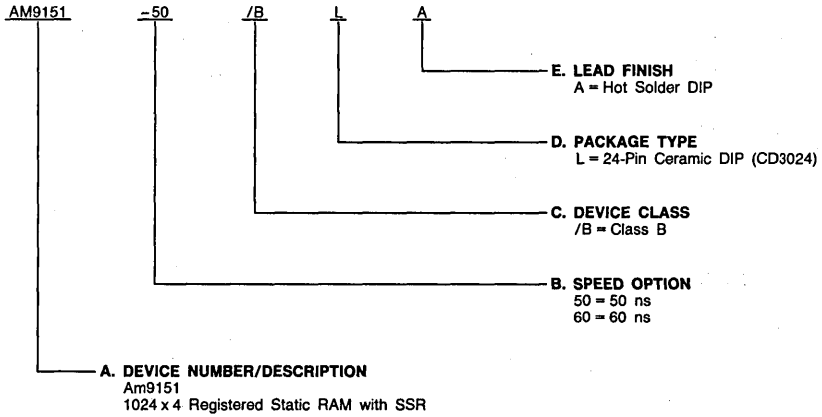
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9151-50	/BLA
AM9151-60	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

PIN DESCRIPTION

$A_0 - A_9$ Address (Inputs)
The 10-bit field presented at the address inputs selects one of the 1024 memory locations to be read from or written into.

M Mode (Input)
Control input for the pipeline register, multiplexer, shadow register, shadow register multiplexer, and initialize register.

DK Diagnostic Clock (Input)
The diagnostic clock is used to load or shift data into the shadow register. Also used to load data into the initialize register and the memory array. Transfer occurs on the LOW-to-HIGH transition of DK.

SD Serial Data Input (Input)
The input to the least significant bit of the shadow register when operating in the shift mode. SD is also a control input when it is not in the shift mode.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the pipeline register from the initialize register, shadow register, or the memory array.

SQ Serial Data Output (Output)
The output from the most significant bit of the shadow register. When mode is LOW SD feeds through to SQ.

$DQ_1 - DQ_4$ Data I/O Port (Input/Output)
Parallel data output from the pipeline register or parallel data input to the shadow register.

$\overline{IS}$ Synchronous Initialize (Input)
Control input for the initialize register. Used to load the pipeline register from the initialize register or load the initialize register from the shadow register. The initialize function can be used to generate any arbitrary microinstruction for system interrupt or reset.

$\overline{GS}$ Synchronous Output Enable (Input)
Controls the state of the DQ outputs in conjunction with PK.

$\overline{G}$ Asynchronous Output Enable (Input)
Controls the state of the DQ outputs independent of clock.

FUNCTIONAL DESCRIPTION

See the following function tables (Tables 1 and 2) for PK and DK operations.

TABLE 1. FUNCTION TABLE for PK OPERATIONS

PK transitions LOW-to-HIGH. DK stable at least 65 ns before PK transition, SD = Don't Care.

Inputs					Outputs	
PK	$\overline{IS}$	M	$\overline{GS}$	$\overline{G}$	$DQ_1 - DQ_4$	Operation
↑	L	L	L	L	$PR_1 - PR_4$	IREG → PREG
			H	X	Hi-Z	
			X	H	Hi-Z	
↑	H	L	L	L	$PR_1 - PR_4$	MEM → PREG
			H	X	Hi-Z	
			X	H	Hi-Z	
↑	X	H	L	L	$PR_1 - PR_4$	DREG → PREG
			H	X	Hi-Z	
			X	H	Hi-Z	

TABLE 2. FUNCTION TABLE for DK OPERATIONS

DK transitions LOW-to-HIGH, PK stable at least 65 ns before DK transition, $\overline{G}$ controls output impedance, otherwise Don't Care.

Inputs						Outputs	
DK	$\overline{IS}$	M	SD	$\overline{GS}$*	$\overline{G}$	$DQ_1 - DQ_4$	Operation
↑	L	H	H	L	L	$PR_1 - PR_4$	DREG → IREG
				H	X	Hi-Z	
				X	H	Hi-Z	
↑	X	L	X	L	L	$PR_1 - PR_4$	SHIFT DREG
				H	X	Hi-Z	
				X	H	Hi-Z	SD = DR_1, DR_4 = SQ
↑	X	H	L	L	L	$PR_1 - PR_4$	PDREG → DREG
				H	X	Hi-Z	DQ → DREG
				X	H	Hi-Z	$DQ_1 = DR_1$, $DQ_4 = DR_4$
↑	H	H	H	L	L	$PR_1 = PR_4$	
				H	X	Hi-Z	DREG → MEM
				X	H	Hi-Z	

*Set in a previous cycle by PK.

Note: If DK and PK transitions are within 65 ns of each other, the device will assume an unknown state.

APPLICATIONS

Applying Serial Shadow Register (SSR) Diagnostics In Sequential Logic Systems

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals — address, data, control, and status — to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

Serial Shadow Register Diagnostics

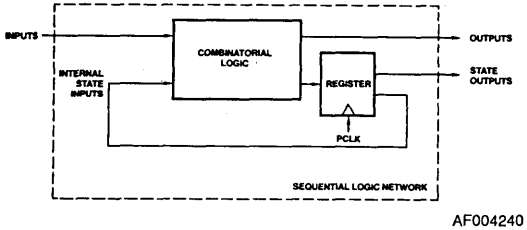
Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PCLK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

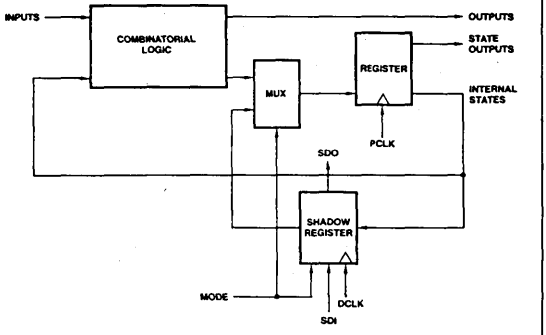
In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

4



AF004240

Figure 1. Sequential Network



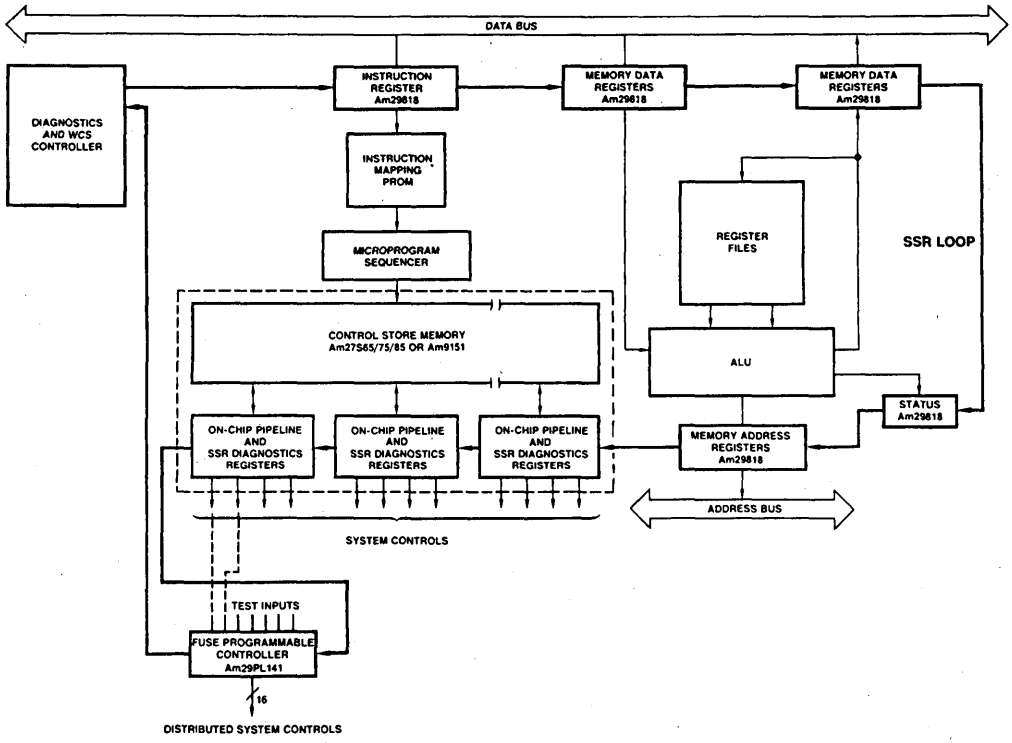
AF004250

Figure 2. Combinational Network

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 3 shows a typical computer system using Am29818's and Am9151's.

Serial paths have been added to all the important state registers (macroinstruction, data, status, address, and microinstruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the microinstruction register with the necessary microinstruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 3 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug. The Am9151s' SSR format and functionality are identical to the Am29818.



BD006280

Figure 3. Typical System Configuration

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
V_{CC} with Respect to GND ..... −0.5 to +7.0 V
All Signal Voltages with
Respect to GND ..... −3.5 to +7.0 V
Power Dissipation
(Package Limitation) ..... 1.2 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.5 to +5.5 V

Military (M) Devices*
Temperature ..... 55 to +125°C
Supply Voltage ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

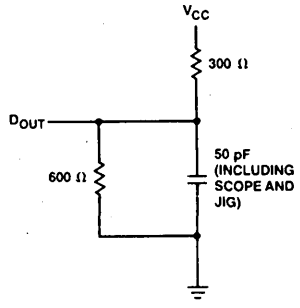
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{OH} (DQ)	Parallel Output HIGH Current	V_{OH} = 2.4 V		−2		mA
I_{OL} (DQ)	Parallel Output LOW Current	V_{OL} = 0.4 V	T_A = +70°C	24		mA
			T_A = +125°C	18		
I_{OH} (SQ)	Serial Output HIGH Current	V_{OH} = 2.4 V		−0.5		mA
I_{OL} (SQ)	Serial Output LOW Current	V_{OL} = 0.5 V		4		mA
V_{IH}	Input HIGH Voltage			2.2	6.0	Volts
V_{IL}	Input LOW Voltage	(Note 6)		−0.5	0.8	Volts
I_{IX}	Input Load Corrent	$GND \leq V_I \leq V_{CC}$		−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$		−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 8)			5	pF
$C_{I/O}$	Parallel Input/Output Capacitance				7	pF
C_O	Serial Output Capacitance				7	pF
I_{CC}	V_{CC} Operating Supply Current				180	mA
I_{OS} (DQ)	Parallel Output Short Circuit Current	V_O = 0 V (Notes 7, 8)			−225	mA
I_{OS} (SQ)	Serial Output Short Circuit Current	V_O = 0 V (Notes 7, 8)			−85	mA

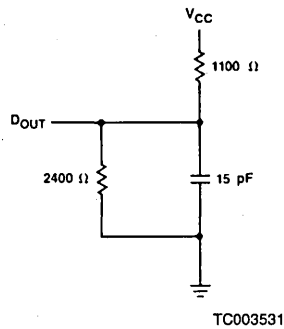
Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, operating temperature is defined as the "instant-ON" case temperature.
3. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 50 pF load capacitance for $DQ_1 - DQ_4$ and 15 pF for SQ output; output timing reference is 1.5 V.
4. TGHDQZ and TPKHDQZ are measured to the V_{OH} −0.5 V and V_{OL} +0.5 V output levels using the load in C. under Switching Test Circuits.
5. All device test loads should be located within 2" of device outputs.
6. V_{IL} voltages of less than −0.5 V on $DQ_1 - DQ_4$ pins will cause the output current to exceed the maximum rating and thus should not exceed 30 seconds in duration.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. This parameter is not tested, but guaranteed by characterization.

*See the last page of this spec for Group A Subgroup Testing information.

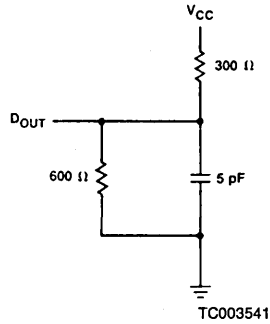
SWITCHING TEST CIRCUITS



A. Output Load for $DQ_1 - DQ_4$



B. Output Load for SQ



C. Output Load for TGHDQZ and TPKHDQZ (Note 4)

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Cont'd.)

No.	Parameter Symbol	Parameter Description	Am9151-40		Am9151-50		Am9151-60		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PK-Controlled Operations									
1	TAVPKH	Address to PK HIGH Setup Time	25		30		35		ns
2	TPKHAX	Address from PK HIGH Hold Time	0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, if Outputs Were Not Hi-Z Initially		12		15		20	ns
4	TPKHDQV2	Delay from PK HIGH to Output Valid, if Outputs Were Hi-Z Initially		15		20		25	ns
5	TPKHPKL TPKLPKH	PK Pulse Width (LOW or HIGH)	15		20		25		ns
6	TGLDQV	Asynchronous Output Enable LOW to Output Valid		15		20		25	ns
7	TGHDQZ	Asynchronous Output Enable HIGH to Output Hi-Z (Note 4)		15		20		25	ns
8	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time	15		15		20		ns
9	TPKHGSX	$\overline{GS}$ from PK HIGH Hold Time	0		0		0		ns
10	TPKHDQZ	Delay from PK HIGH to Output in Hi-Z (Note 4)		15		20		25	ns
11	TMVPKH	Mode to PK HIGH Setup Time	35		35		40		ns
12	TPKHMX	Mode from PK HIGH Hold Time	5		5		5		ns
13	TIVPKH	Synchronous $\overline{I}$ to PK HIGH Setup Time	20		25		30		ns
14	TPKHIX	Synchronous $\overline{I}$ from PK HIGH Hold Time	5		5		5		ns
15	TDKSPKH	DK Stable to PK HIGH Setup Time	65		65		65		ns
16	TPKHDKX	DK from PK HIGH Hold Time	65		65		65		ns
		Address Input Rise and Fall Times		1		1		1	ns

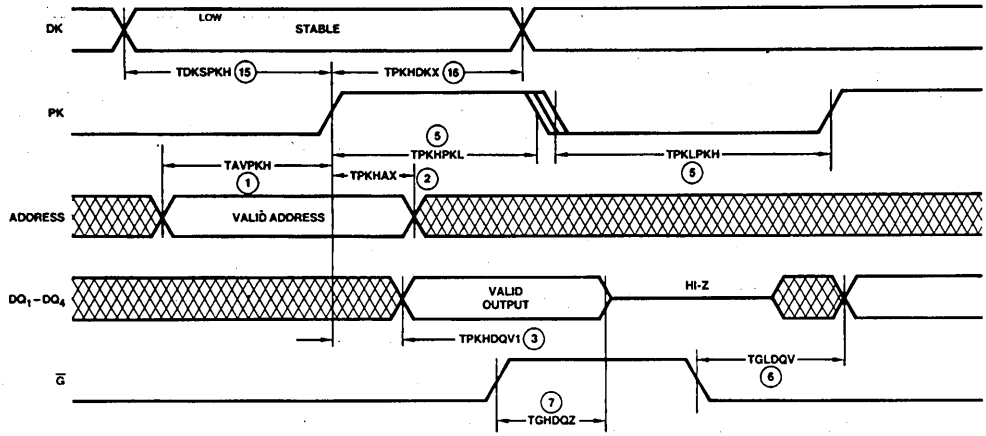
SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am9151-40		Am9151-50		Am9151-60		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
DK-Controlled Operations									
17	TPKSDKH	PK Stable to DK HIGH Setup Time	65		65		65		ns
18	TDKHPKX	PK from DK HIGH Hold Time	65		65		65		ns
19	TSDVDKH	Serial Data in to DK HIGH Setup Time	20		25		30		ns
20	TDKHSDX	Serial Data in from DK HIGH Hold Time	5		5		5		ns
21	TMVDKH	Mode to DK HIGH Setup Time	35		35		40		ns
22	TDKHMX	Mode from DK HIGH Hold Time	5		5		5		ns
23	TDQVDKH	Data in to DK HIGH Setup Time	20		25		30		ns
24	TDKHDQX	Data in from DK HIGH Hold Time	5		5		5		ns
25	TIVDKH	$\overline{IS}$ to DK HIGH Setup Time	20		25		30		ns
26	TDKHIX	$\overline{IS}$ from DK HIGH Hold Time	5		5		5		ns
27	TDKHSQV	Delay from DK HIGH to Serial Data Out Valid (Shifting)		35		35		40	ns
28	TDKHDKL TDKLDKH	DK Pulse Width (LOW or HIGH)	25		30		35		ns
29	TAVDKH	Address Valid to DK HIGH Setup Time for Memory Write	0		0		0		ns
30	TDKHAX	Address Hold from DK HIGH (Write)	40		50		60		ns
Non DK- or PK-Controlled Operations (DK = Stable, PK = Stable)									
31	TSDVSQV	Delay from Serial Data in Valid to Serial Data Out Valid (Mode HIGH)		25		30		35	ns
32	TMHSQV	Delay from Mode HIGH to Serial Data Out Valid		35		40		45	ns
33	TSDVMH	Serial Data in Valid to Mode HIGH Setup Time	0		0		0		ns
34	TMLSQV	Delay from Mode LOW to Serial Data Valid (SQ = DR4)		35		40		45	ns

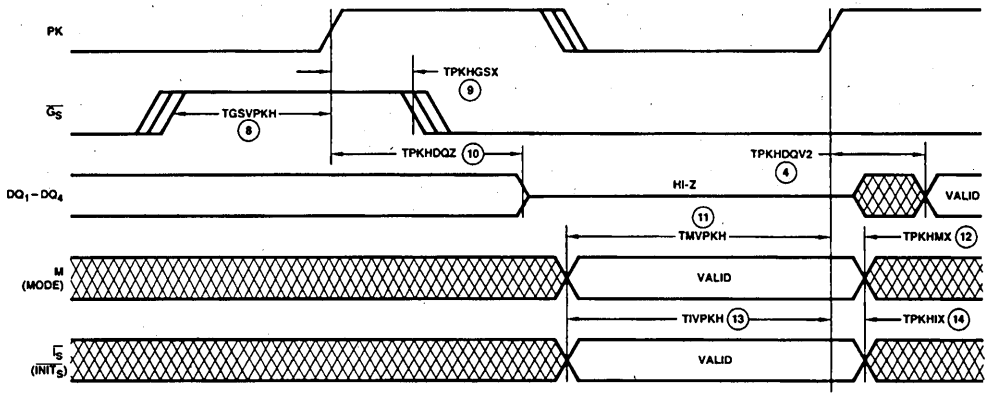
*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS (Cont'd.)

TIMING SET 1 NOTE ($\overline{GS}$ LOW - IF DK HELD STABLE PK CAN HAVE MINIMUM CYCLE TIME)



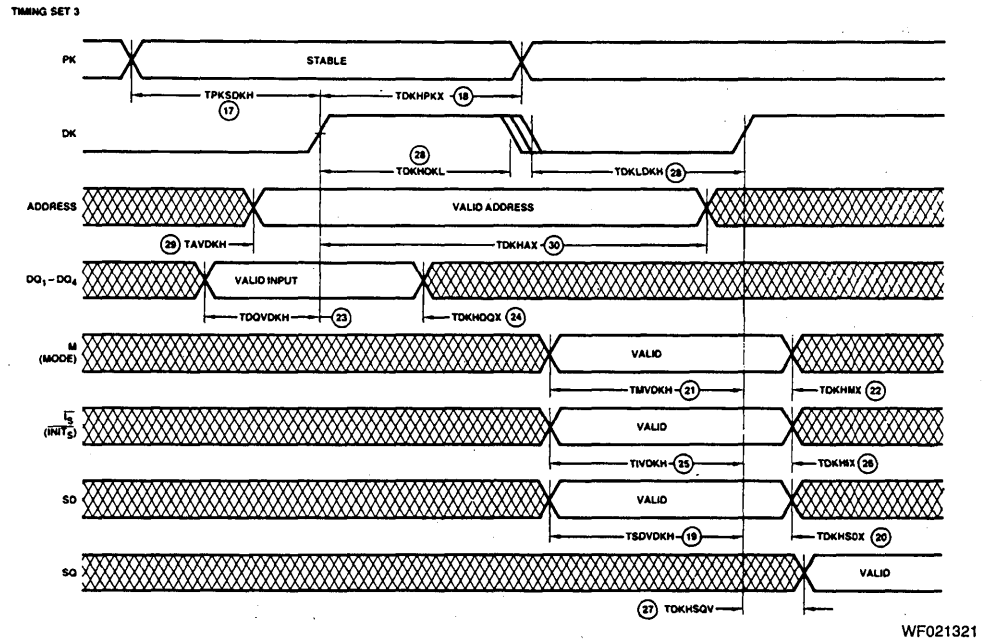
TIMING SET 2 ($\overline{G}$ LOW)



WF021312

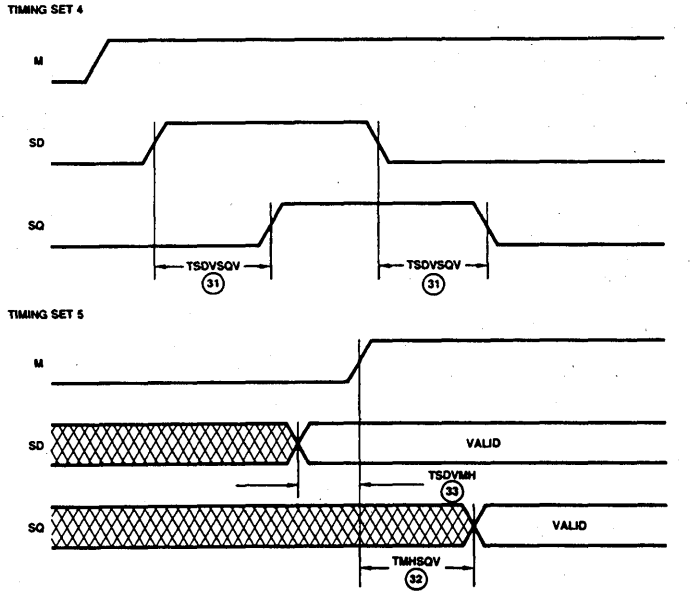
PK-Related

SWITCHING WAVEFORMS



WF021321

DK-Related



WF021330

Non DK- or PK-Related

4

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH} (DQ)	1, 2, 3
I_{OL}(DQ)	1, 2, 3
I_{OH} (SQ)	1, 2, 3
I_{OL}(SQ)	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVPKH	7, 8, 9, 10, 11	19	TSDVDKH	7, 8, 9, 10, 11
2	TPKHAX	7, 8, 9, 10, 11	20	TDKHSDX	7, 8, 9, 10, 11
3	TPKHDQV1	7, 8, 9, 10, 11	21	TMVDKH	7, 8, 9, 10, 11
4	TPKHDQV2	7, 8, 9, 10, 11	22	TDKHMX	7, 8, 9, 10, 11
5	TPKHPKL TPKHPKH	7, 8, 9, 10, 11	23	TDQVDKH	7, 8, 9, 10, 11
6	TGLDQV	7, 8, 9, 10, 11	24	TDKHDQX	7, 8, 9, 10, 11
8	TGSVPKH	7, 8, 9, 10, 11	25	TIVDKH	7, 8, 9, 10, 11
9	TPKHGSX	7, 8, 9, 10, 11	26	TDKHIX	7, 8, 9, 10, 11
11	TMVPKH	7, 8, 9, 10, 11	27	TDKHSQV	7, 8, 9, 10, 11
12	TPKHMX	7, 8, 9, 10, 11	28	TDKHDKL TDKLDKH	7, 8, 9, 10, 11
13	TIVPKH	7, 8, 9, 10, 11	29	TAVDKH	7, 8, 9, 10, 11
14	TPKHIX	7, 8, 9, 10, 11	30	TDKHAX	7, 8, 9, 10, 11
15	TDKSPKH	7, 8, 9, 10, 11	31	TSDVSQV	7, 8, 9, 10, 11
16	TPKHDKX	7, 8, 9, 10, 11	32	TMHSQV	7, 8, 9, 10, 11
17	TPKSDKH	7, 8, 9, 10, 11	33	TSDVMH	7, 8, 9, 10, 11
18	TDKHPKX	7, 8, 9, 10, 11	34	TMLSQV	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am99C10

256 x 48 Content Addressable Memory (CAM)

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast-compare time — 50 ns data to match output
- Maskable-bits and maskable-words
- Word-parallel search
- Multiple-match capabilities
- On-chip address decoder
- Time-multiplexed data input
- TTL-compatible inputs and outputs
- Low power dissipation via CMOS

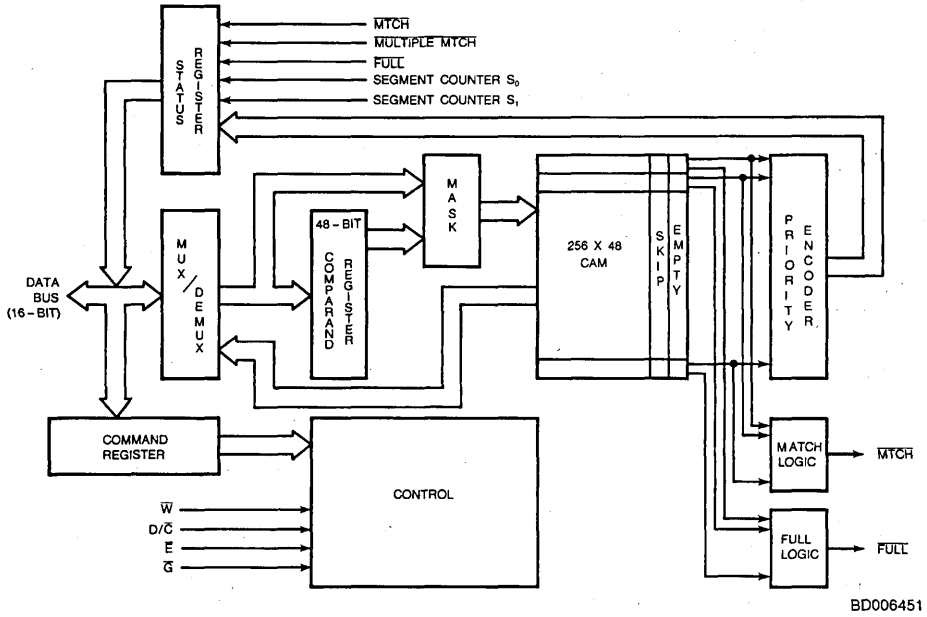
GENERAL DESCRIPTION

The Am99C10 is a high-speed Content Addressable Memory (CAM) with a capacity of 256 words of 48 bits each. The 256 x 48 organization is ideal in Ethernet network applications where it can function as an address filter and perform the network address look-up function in bridges. It can also find use in database machines, temporary storage, decoding, and scratch pad memory applications. Unlike standard memories that associate data with an address, the CAM associates an address with data. The data (comparand) is presented to the CAM which performs simultaneous compare operations on all data (256 words). When the comparand and a word in the CAM are matched, the on-chip priority encoder generates a match word address identifying the location of the data in the CAM. If multiple matches occur, the encoder generates the lowest matched address.

The Am99C10 features a 16-bit bidirectional data bus and three control signals: $\overline{W}$, $\overline{G}$ and $\overline{E}$. $\overline{W}$ controls the writing of the internal registers, latches, and the CAM. $\overline{G}$ controls the reading of the output data and status, while $\overline{E}$ controls the selection/deselection of the device.

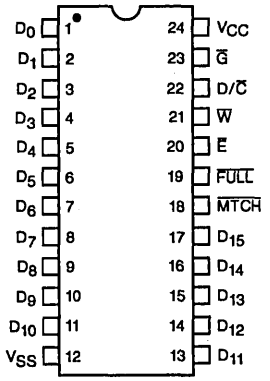
The Am99C10 CAM is manufactured with state-of-the-art CMOS processing techniques. It is assembled in a 24-pin, 400-mil wide DIP.

BLOCK DIAGRAM



Publication # 08125 | Rev. A | Amendment /0
Issue Date: Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009610

Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

D/$\overline{C}$ Data/Command Mode Selection (Input, TTL, Active HIGH)
A LOW on this input selects the command mode. A HIGH on this input selects the data mode.

$\overline{W}$ Write Enable (Input, TTL, Active LOW)
This pin controls the writing of the internal registers and latches. New data may be written into a register by forcing the appropriate state of D/$\overline{C}$, $\overline{E}$ and $\overline{W}$.

$\overline{G}$ Output Enable (Input, TTL, Active LOW)
This pin controls the reading of the output data and status register. The status register can be accessed by forcing the appropriate state of D/$\overline{C}$ and pulling $\overline{G}$ LOW. $D_0 - D_{15}$ is in the high-impedance state when $\overline{G}$ is pulled HIGH.

$\overline{E}$ Chip Enable (Input, TTL, Active LOW)
A LOW on this input enables chip operations as specified by the state of D/$\overline{C}$, $\overline{W}$, $\overline{G}$ and the command word.

$D_0 - D_{15}$ Data Bus (Bidirectional, Three-State)
The 16-bit bidirectional data bus performs data transfers. The data bus is in a high-impedance state when $\overline{G}$ is HIGH and/or $\overline{E}$ is HIGH.

$\overline{FULL}$ Address Full (Output, TTL, Active LOW)
A LOW on this output indicates that all the words in the 256 address locations in CAM are used. A HIGH on this output indicates that certain locations are still available for storage or that the $\overline{FULL}$ output is disabled. The $\overline{FULL}$ output is in the logic HIGH state when $\overline{E}$ is HIGH.

$\overline{MTCH}$ Match (Output, TTL, Active LOW)
A LOW on this output indicates that the data present in the comparand register and word(s) already stored in the CAM are matched. A HIGH on this output indicates that a mismatch has taken place or the match output is disabled. The match output is in the logic HIGH state when $\overline{E}$ is HIGH.

V_{CC} Power Supply (Input) +5 V

V_{SS} Power Supply (Input) Ground

FUNCTIONAL DESCRIPTION

The following functional description briefly describes the Am99C10 Block Diagram as well as the architecture of the device.

Organized 256 x 48, the Am99C10 has an internal 16-bit bidirectional data bus, while the internal data bus is organized 48 bits wide. The demultiplexer and Comparand Register assemble 48-bit wide data from the external 16-bit data. The Segment Counter controls the multiplexer/demultiplexer operations. The Comparand Register is organized as three 16-bit registers. The source of data to the Comparand Register is selected from the CAM, Mask Register, or I/O. The Segment Counter output is used to select a 16-bit field in the 48-bit bus. The Mask Register is 48 bits wide and is loaded from the Comparand Register by issuing a "move" command. The command latch holds a 16-bit command word, providing global control of the Am99C10.

The state information memory indicates the state of the 48-bit word in the CAM and is organized 256 words by 2 bits. Each 48-bit word has a skip-bit and an empty-bit associated with it. The skip-bit enables/disables a word in the CAM in situations where there are multiple matches. The priority encoder generates the lowest match address when multiple matches occur. The skip-bit gives the user the ability to detect other matched addresses. The match address is accessed by reading the status register. The empty-bit indicates available or empty addresses in the CAM into which data can be written. If multiple empty addresses exist, the priority encoder generates the lowest empty address. The empty address is accessed by reading the status register.

Am99C164/Am99C165

16,384 x 4 STATIC R/W RANDOM-ACCESS MEMORY

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time – Am99C164 – 35/45/55/70 ns maximum
  Am99C165 – 35/45/55/70 ns maximum
- 16K x 4 organization
- Output Enable ($\overline{G}$) control to alleviate bus contention conditions (Am99C165)
- Single 5 V ±10% power supply operation
- Fully static storage and interface circuitry
- Automatic power down when deselected
- Low power dissipation
  - 330 mW average operating power
  - 85 mW maximum standby power for TTL interface levels
- 2 V data retention capability
- 22-pin 0.300-inch DIP (Am99C164)
- 24-pin 0.300-inch DIP (Am99C165)

GENERAL DESCRIPTION

The Am99C164 and Am99C165 are high-performance 16,384 x 4 bit static read/write random-access memory manufactured with state-of-the-art CMOS processing techniques.

The Am99C164 device features common input/output pins and two control signals ($\overline{E}$) and ($\overline{W}$). While $\overline{E}$ controls read, write and selection/deselection of the device, $\overline{W}$ controls the write operation and output buffers only.

The Am99C165 device features three control signals ($\overline{E}$), ($\overline{W}$) and ($\overline{G}$) to facilitate not only memory expansion but also alleviate any bus contention conditions which might limit high performance read/write operation. While $\overline{W}$ activates only the input buffers during a write cycle, $\overline{G}$ activates only the output buffers during a read cycle. $\overline{E}$ controls the selection/deselection of the entire device irrespective of read or write and powers down the device when $\overline{E}$ is inactive. All input/output interface levels are fully TTL compatible for both the Am99C164 and Am99C165.

The Am99C164 and Am99C165 require a single 5 V power supply while operating but can hold the data when power supply level is maintained at a voltage as low as 2 V.

The Am99C164 is available in a 22-pin 0.300 inch wide dual in-line ceramic or plastic package.

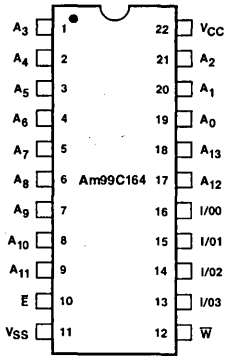
The Am99C165 is available in a 24-pin 0.300 inch wide dual in-line ceramic or plastic package.

PRODUCT SELECTOR GUIDE

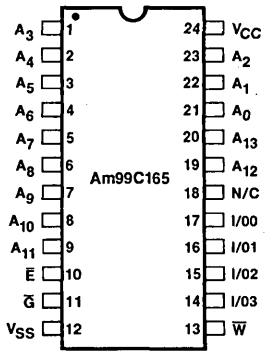
Part Number		99C164-35 99C165-35	99C164-45 99C165-45	99C164-55 99C165-55	99C164-70 99C165-70
Maximum Access Time (ns)		35	45	55	70
I_{CC}Max (mA)	0 to +70°C	110	90	90	90
I_{CC}Max (mA)	−55 to +125°C	NA	110	110	110

Publication # 07437 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



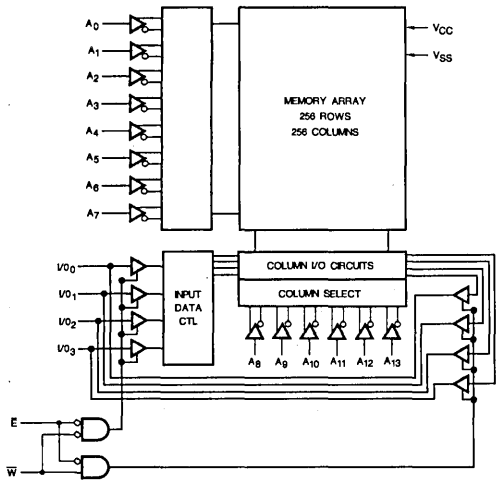
CD009000



CD009010

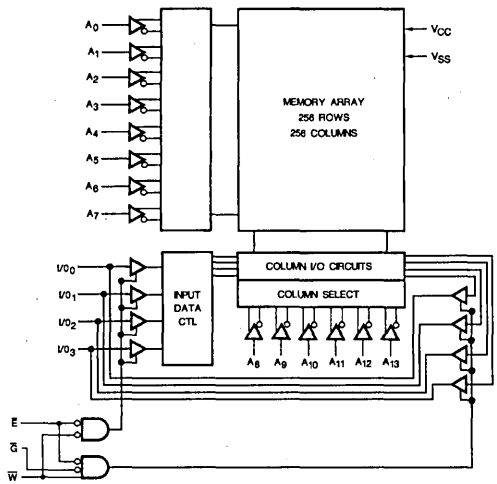
BLOCK DIAGRAMS

Am99C164



BD005700

Am99C165



BD005710

Am99C19

1024 x 9 First-In/First-Out (FIFO)

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- First-In/First-Out dual-port memory
- 1024 x 9 organization
- Fast cycle time
  - 45 ns typical
- Fast throughput time > 20 MHz
- Expandable by both word depth and/or bit width
- Empty, half-full, and full warning flags
- Asynchronous and simultaneous read and write
- Auto re-transmit capabilities
- Low-power dissipation
  - 440 mW (0 to +70°C)
  - 550 mW (−55 to +125°C)
- Single 5-volt ±10% power-supply operation
- 28-pin (0.600-inch) DIP

GENERAL DESCRIPTION

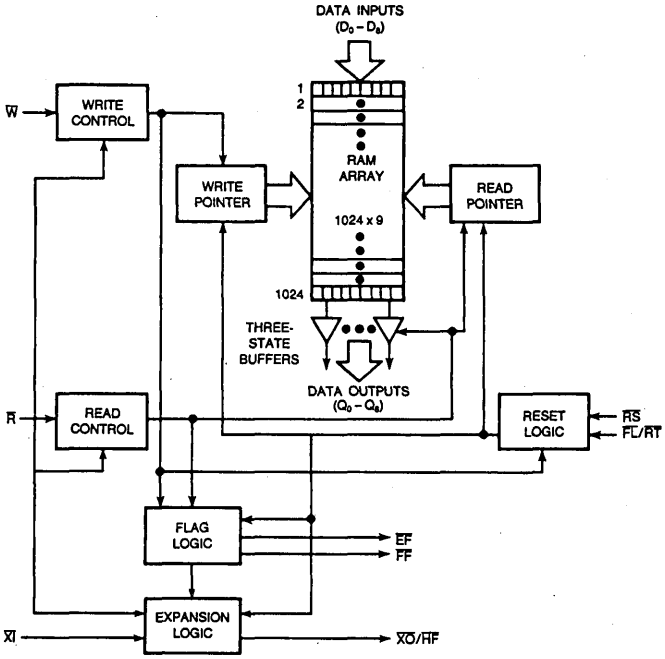
The Am99C19 is a dual-port FIFO memory that offers parallel loading capability. Full and empty flags are provided to prevent overflow or underflow of data. Expansion logic is incorporated into the device for easy expansion in both word size and depth.

The read and write cycles are internally sequential through the use of ring pointers without address information present to load and unload data. Write and Read signals are used to toggle data in and out of the device. The Am99C19 has a typical read/write cycle time of 45 ns (> 20 MHz).

The AM99C19 FIFO offers a 9-bit wide data array for control and parity bits at the user's choice. This feature is ideally suited for data communications where a parity bit for transmission/reception error checking is necessary. The Am99C19 device offers the user a choice to re-transmit from the beginning of data by incorporating a "re-transmit" capability.

The Am99C19 is available in a 28-pin (0.600-inch) dual-in-line package.

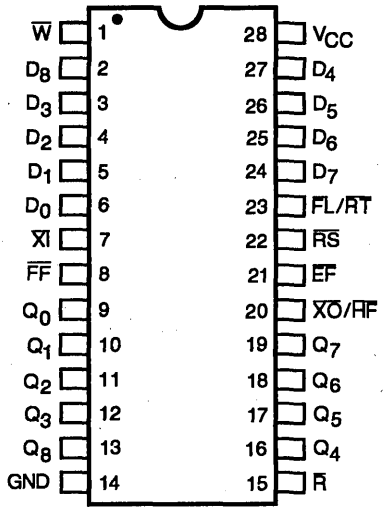
BLOCK DIAGRAM



BD006120

Publication # 08010 | Rev. A | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009410

Note: Pin 1 is marked for orientation.

Am99C328

32,768 x 8 Static R/W Random-Access Memory

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time — 45/55/70/100 ns Maximum
- 32K x 8 organization
- Output Enable $\overline{G}$ ($\overline{OE}$) control to alleviate bus contention
- Single 5 V ±10% power supply operation
- Fully static storage and interface circuitry
- Automatic Power-Down when deselected
- Low power dissipation
  - 400 mW typical operating power
  - 125 mW maximum standby power for TTL interface levels
- 2 V data retention capability
- 28-pin, 0.6-inch DIP

GENERAL DESCRIPTION

The Am99C328 is a high-performance, 32,768 x 8-Bit Static Read/Write Random-Access Memory manufactured with state-of-the-art CMOS processing techniques.

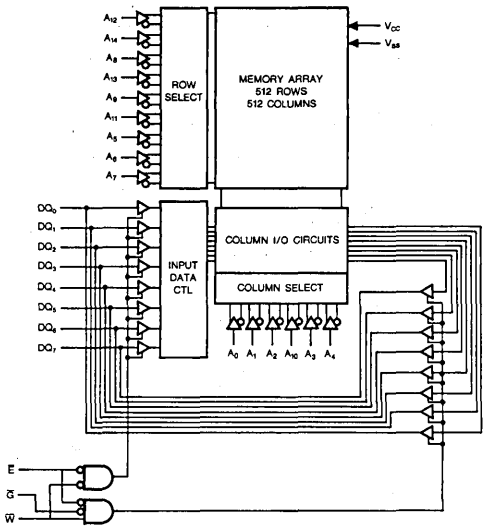
The Am99C328 features three control signals, $\overline{E}$ ($\overline{CE}$), $\overline{W}$ ($\overline{WE}$), and $\overline{G}$ ($\overline{OE}$), to facilitate not only memory expansion, but also alleviate any bus contention conditions which might limit high-performance Read/Write operation. While $\overline{W}$ ($\overline{WE}$) activates only the input buffers during a write cycle, $\overline{G}$ ($\overline{OE}$) activates only the output buffers during a read cycle.

$\overline{E}$ ($\overline{CE}$) controls the selection/deselection of the entire device irrespective of read or write and powers down the device when $\overline{E}$ ($\overline{CE}$) is inactive. All input/output interface levels are fully TTL compatible for the Am99C328.

The Am99C328 requires a single 5 V power supply while operating, but will hold the data when the power-supply level is maintained at voltages as low as 2 V.

The Am99C328 is available in a 28-pin, 0.6-inch wide, dual-in-line, side/brazed package.

BLOCK DIAGRAM



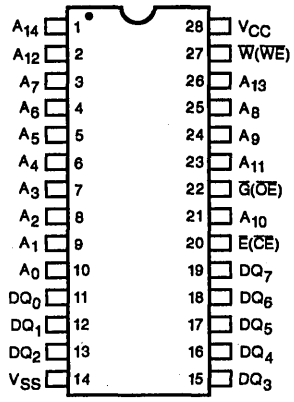
BD006531

PRODUCT SELECTOR GUIDE

Part Number	Am99C328-45	Am99C328-55	Am99C328-70	Am99C328-10
Access Time Max. (ns)	45	55	70	100
I_{CC} Max. (mA) 0 to +70°C	120	120	120	120
I_{CC} Max. (mA) −55 to +125°C	NA	140	140	140

Publication # 08137 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009700

ADDRESS DESIGNATORS

External	Internal	Pin Number
A_{14}	AY_5	1
A_{12}	AX_6	2
A_7	AX_5	3
A_6	AX_4	4
A_5	AX_3	5
A_4	AX_2	6
A_3	AY_4	7
A_2	AY_3	8
A_1	AY_2	9
A_0	AY_1	10
A_{10}	AY_0	21
A_{11}	AX_1	23
A_9	AX_0	24
A_8	AX_8	25
A_{13}	AX_7	26

Am99C416

4096 x 16 Static Read/Write Random-Access Memory

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- High Speed
  - Access time as fast as 45 ns
- Low-power consumption
  - 605 mW Maximum (Active)
  - 140 mW Maximum (Standby)
- Output Enable ($\overline{G}$) control to minimize bus contention
- 2-V data retention for battery back-up operation
- Single 5-V ±10% power supply operation
- Fully static — no clocks or timing signals required
- 40-pin, 0.600-inch DIP

GENERAL DESCRIPTION

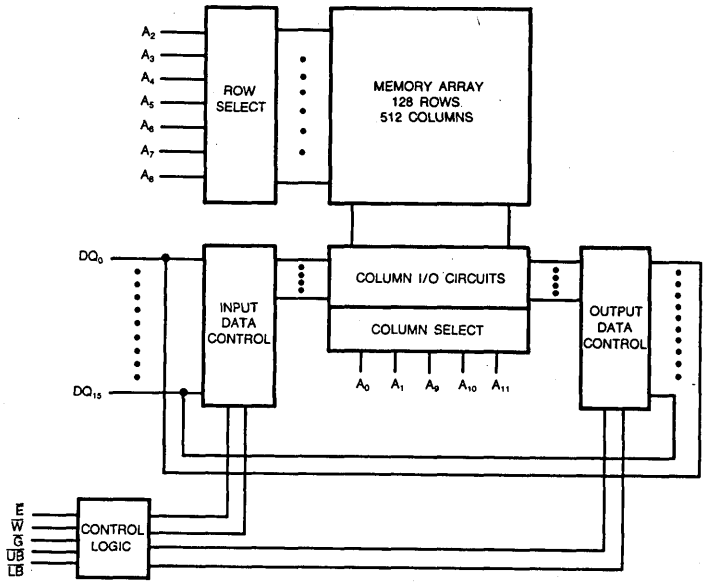
The Am99C416 is a 65,536-bit, static, high-speed, Read/Write Random-Access Memory organized as 4096 words with 16 bits per word. Manufactured with advanced CMOS processing techniques, the Am99C416 combines fast access time with low-power consumption and increased reliability.

Features include common input/output pins and three control signals to facilitate read/write operations, simplify memory expansion, and minimize any bus contention that may limit device performance. $\overline{W}$ activates only the input buffers during a write cycle while $\overline{G}$ activates only the output buffers during a read cycle. $\overline{E}$ controls the selection/deselection of the entire device and powers down the device when $\overline{E}$ goes HIGH. Two memory-array partition signals, $\overline{UB}$ and $\overline{LB}$, allow independent access to either the upper or lower eight bits of the 16-bit word.

The wide word length and 4K depth make the Am99C416 useful as writable control store memory in mini and super-mini computers in addition to applications using 16-bit and 32-bit microprocessors.

The Am99C416 requires a single 5-V power supply while operating, but can retain data with supply voltages as low as 2 V. All input/output levels are TTL-compatible.

BLOCK DIAGRAM



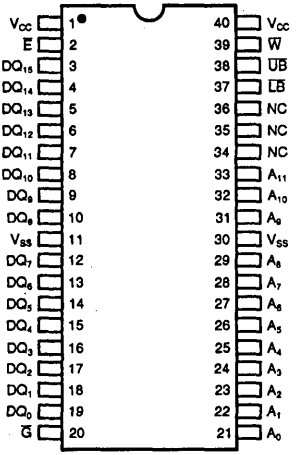
BD006480

Publication # 08119 | Rev. A | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

Part Number	Am99C416-45	Am99C416-55	Am99C416-70
Maximum Access Time (ns)	45	55	70
I_{CC} Maximum (mA)	110	110	110
I_{SB} Maximum (mA)	25	25	25

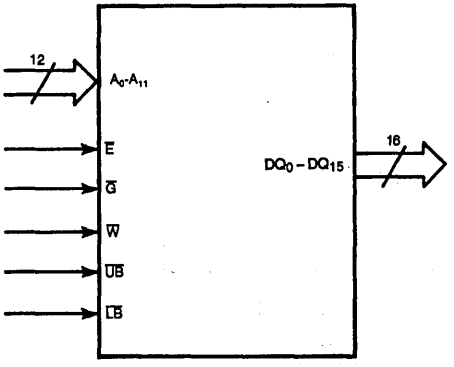
CONNECTION DIAGRAM
Top View



CD009650

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002461

Pin Names

$DQ_0 - DQ_{15}$ = Data I/O
$A_0 - A_{11}$ = Address Inputs
$\overline{E}$ = Chip Enable
$\overline{W}$ = Write Enable
$\overline{G}$ = Output Enable
$\overline{UB}$ = Upper Byte Control
$\overline{LB}$ = Lower Byte Control
V_{CC} = +5-V Power Supply
V_{SS} = Ground

FUNCTIONAL DESCRIPTION

Please refer to Table 1 for Mode Selection for the Am99C416.

TABLE 1. MODE SELECT

Inputs					Outputs		
$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{UB}$	$\overline{LB}$	$DQ_{15}-DQ_8$	DQ_7-DQ_0	Mode
H	X	X	X	X	Hi-Z	Hi-Z	Deselected, Power Down
L	L	X	H	H	Hi-Z	Hi-Z	Deselected
L	L	X	L	H	Data In	Hi-Z	Byte-Write
L	L	X	H	L	Hi-Z	Data In	Byte-Write
L	L	X	L	L	Data In	Data In	Word-Write
L	H	L	H	H	Hi-Z	Hi-Z	Deselected
L	H	L	L	H	Data Out	Hi-Z	Byte-Read
L	H	L	H	L	Hi-Z	Data Out	Byte-Read
L	H	L	L	L	Data Out	Data Out	Word-Read
L	H	H	X	X	Hi-Z	Hi-Z	Output Not Enabled

H = HIGH
L = LOW
X = Don't Care

4

Am99C58/Am99C59

4096 x 4 CMOS Static Random-Access Memory

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 4096 x 4 organization
- High Speed
  - 25 ns t_{AA} Maximum
  - 15 ns t_{ACS} Maximum (Am99C59)
- Separate data inputs and outputs
- Automatic power-down when deselected (Am99C58)
- Maximum power dissipation: 990 mW
- Maximum standby power dissipation: 220 mW (Am99C58)
- TTL-compatible inputs and outputs
- Single +5-V ±10% power supply
- Slim 24-pin, 300-mil DIP and 28-pin ceramic leadless carrier

GENERAL DESCRIPTION

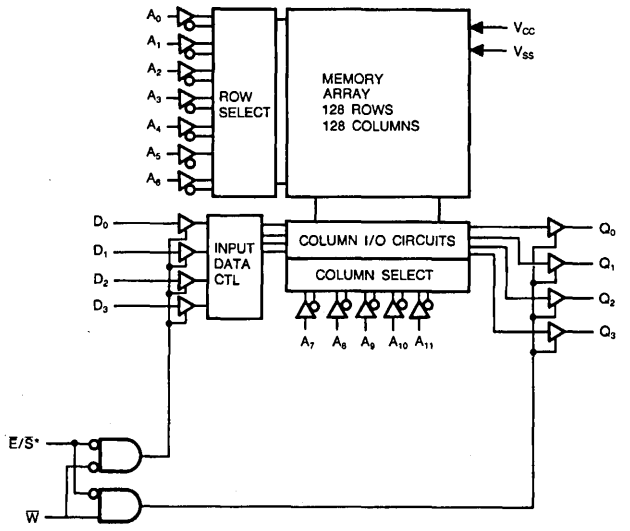
The Am99C58 and Am99C59 are high-performance CMOS Static RAMs organized as 4096 words by 4 bits. They are manufactured using an advanced high-performance CMOS process that combines high speed with low-power consumption and increased reliability.

Both devices feature access times as fast as 25 ns and separate data inputs and outputs. The Am99C58 and Am99C59 operate from a single 5-V supply and all inputs and outputs are fully TTL-compatible. The Am99C58 provides a Chip Enable ($\overline{E}$) function that automatically powers down the device when deselected. The Am99C59 provides a Chip Select ($\overline{S}$) function that offers a chip select access time of 15 ns.

Two inputs, $\overline{E}/\overline{S}$* and $\overline{W}$, are used to control the device. Chip Enable/Select ($\overline{E}/\overline{S}$)* selects the device for operation and provides for easy memory expansion. Write Enable ($\overline{W}$) controls write and read operations. The data outputs will be in a high-impedance state when $\overline{E}/\overline{S}$* is HIGH, or $\overline{W}$ is LOW.

The Am99C58 and Am99C59 are packaged in a slim 24-pin, 300-mil DIP or 28-pin ceramic leadless chip carrier.

BLOCK DIAGRAM



BD006491

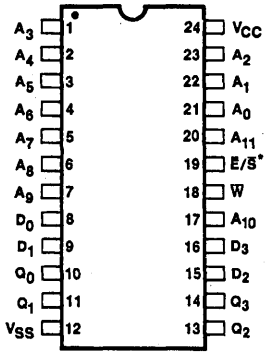
*$\overline{E}$=Am99C58
$\overline{S}$=Am99C59

Publication # 08116 | Rev. A | Amendment /0
Issue Date: May 1986

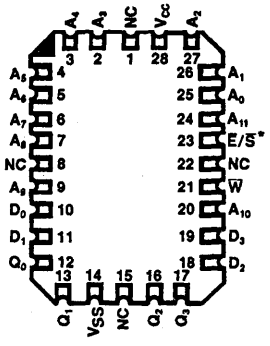
PRODUCT SELECTOR GUIDE

Part Number		Am99C58			Am99C59		
		-25	-35	-45	-25	-35	-45
Access Time Max. (ns)		25	35	45	25	35	45
0 to +70°C	I_{CC} Max. (mA)	180	180	180	180	180	180
	I_{SB} Max. (mA)	40	40	40	—	—	—
−55 to +125°C	I_{CC} Max. (mA)	—	180	180	—	180	180
	I_{SB} Max. (mA)	—	40	40	—	—	—

CONNECTION DIAGRAMS
Top View



CD009012

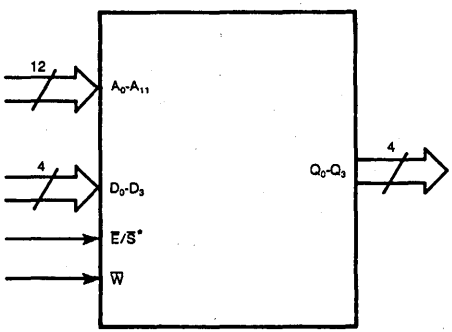


CD005933

*$\overline{E}$ = Am99C58
$\overline{S}$ = Am99C59

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS009651

*$\overline{E}$ = Am99C58
$\overline{S}$ = Am99C59

Am99C60

4096 x 4 CMOS Static Random-Access Memory with Reset

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- 4096 x 4 organization
- High Speed
  - 25 ns t_{AA} Maximum (Commercial)
  - 35 ns t_{AA} Maximum (Military)
- Memory reset function per bit
- Common data inputs and outputs
- Automatic power-down when deselected
- Maximum power dissipation: 990 mW
- Maximum standby power dissipation: 220 mW
- TTL-compatible inputs and outputs
- Single +5-V ±10% power supply
- Slim 24-pin, 300-mil DIP and 28-pin ceramic leadless carrier

GENERAL DESCRIPTION

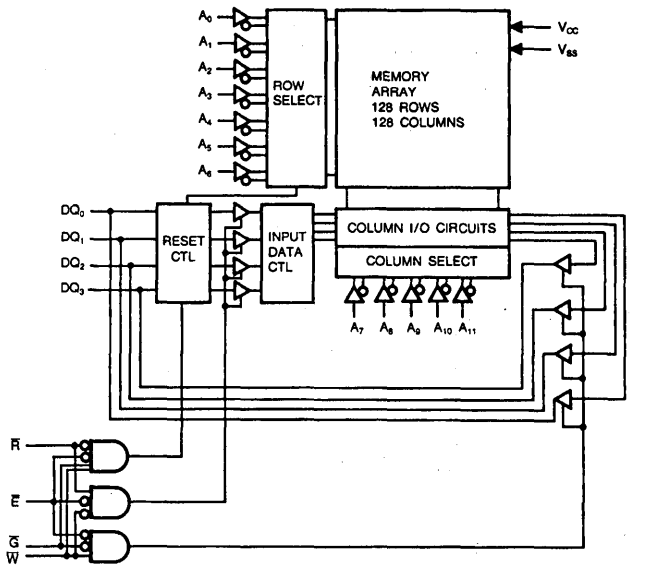
The Am99C60 is a high-performance CMOS Static RAM organized as 4096 words by 4 bits. It is manufactured using an advanced high-performance CMOS process that combines high speed with low-power consumption and increased reliability.

The Am99C60 offers access times as fast as 25 ns and features a memory reset function which allows individual, combination of individual, or all sections of the memory array to be reset to a logic LOW.

The Am99C60 operates from a single 5-V supply and all inputs and outputs are fully TTL-compatible. Four inputs, $\overline{E}$, $\overline{W}$, $\overline{G}$, and $\overline{R}$ are used to control the device. Chip Enable ($\overline{E}$) selects the device for operation and automatically powers down the device when deselected. Write Enable ($\overline{W}$) controls write and read operations. Output Enable ($\overline{G}$) controls the three-state output buffers on the four common data inputs and outputs. Reset ($\overline{R}$) controls the reset function.

The Am99C60 is packaged in a slim 24-pin, 300-mil DIP or 28-pin ceramic leadless chip carrier.

BLOCK DIAGRAM



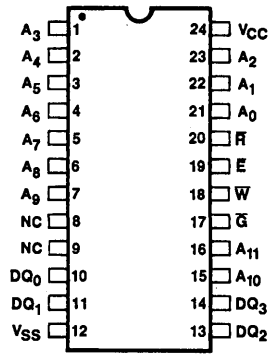
BD006500

Publication # 08117 | Rev. A | Amendment /0
Issue Date: May 1986

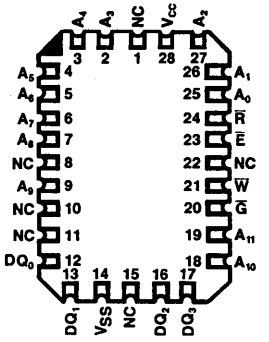
PRODUCT SELECTOR GUIDE

Part Number		Am99C60		
		-25	-35	-45
Access Time Max. (ns)		25	35	45
0 to +70°C	I_{CC} Max. (mA)	180	180	180
	I_{SB} Max. (mA)	40	40	40
-55 to +125°C	I_{CC} Max. (mA)	—	180	180
	I_{SB} Max. (mA)	—	40	40

CONNECTION DIAGRAMS
Top View



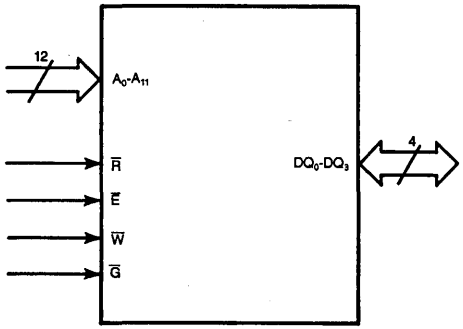
CD009011



CD005932

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002590

FUNCTIONAL DESCRIPTION

Please refer to Table 1 for Mode Selection for the Am99C60.

TABLE 1. MODE SELECT

Inputs					Data Outputs	Mode
$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{R}$	Data Inputs		
H	X	X	X	X	Hi-Z	Not Enabled
L	H	H	L	L	Hi-Z	Reset for any DQ that is LOW
L	H	H	L	H	Hi-Z	No Reset for any DQ that is HIGH
L	L	X	H	Data	Hi-Z	Write
L	H	L	H	N/A	Data Out	Read
L	H	H	H	N/A	Hi-Z	Output Not Enabled

H = HIGH
L = LOW
X = Don't Care
NA = Not Applicable
Z = High Impedance

Am99C641

65,536 x 1 Static Read/Write Random-Access Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

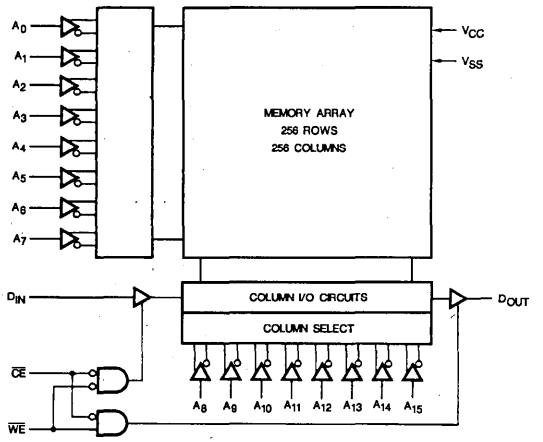
- High-performance CMOS circuit design and process
- High Speed – access times as fast as 25 ns
- Single 5-V ±10% power-supply operation
- Low power – 715 mW active
  110 mW TTL – Standby
- 2 V data retention for battery back up applications
- Fully static — no clocks or timing signals required
- Standard 22-pin slim (0.300 inch) DIP, (plastic and ceramic), and 22-pin rectangular ceramic leadless chip carriers.

GENERAL DESCRIPTION

The Am99C641 is a high-performance, Static CMOS, read/write random-access memory organized as 65,536 words with 1 bit per word. The Am99C641 features single 5-V operation with automatic power-down capability. All inputs and outputs are fully TTL-compatible. There are separate data input and output pins which, along with the two control signals $\overline{CE}$ and $\overline{WE}$, provide ease of expansion in large memory-array applications.

In addition to low TTL-level standby power, this device offers a low CMOS-level standby power of 77 mW and a low data retention current of 4 mA with V_{CC} at 2 V.

BLOCK DIAGRAM



BD005691

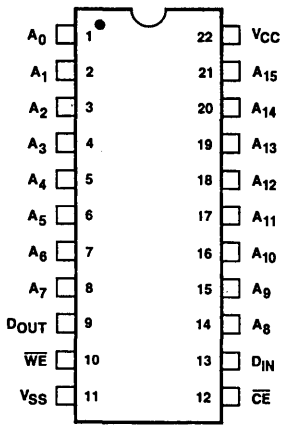
PRODUCT SELECTOR GUIDE

Part Number	Am99C641-25		Am99C641-35		Am99C641-45		Am99C641-55		Am99C641-70	
Maximum Access Time (ns)	25		35		45		55		70	
Temperature Range (Note 1)	C	M	C	M	C	M	C	M	C	M
Supply Voltage Tolerance (mA):										
I_{DD1} Max.	130	—	110	—	90	90	90	90	90	90
I_{SB} Max.	20	—	20	—	20	20	20	20	20	20
I_{SBC} Max.	14	—	14	—	14	16	14	16	14	16
I_{DDR} Max.	4	—	4	—	4	4	4	4	4	4

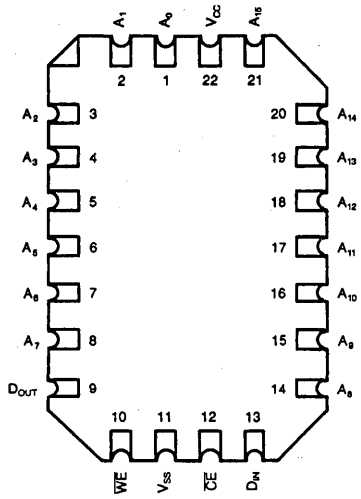
Notes: 1. C = Commercial (0 to +70°C)
2. M = Military (−55 to +125°C)

Publication # 07438 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



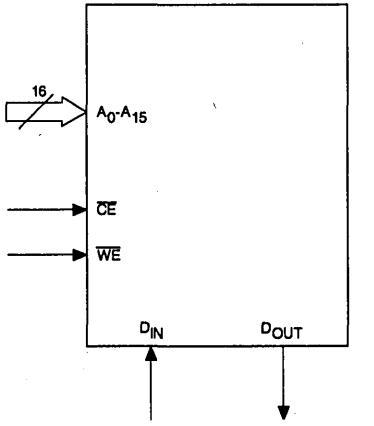
CD008091



CD009283

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



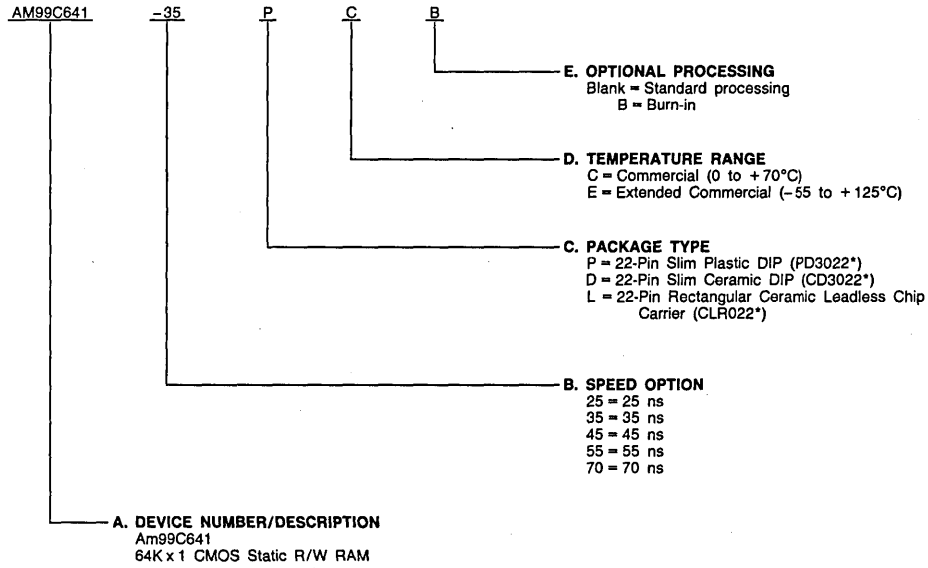
LS002620

V_{CC} = Power Supply
V_{SS} = Ground

Address Designators	
External	**Internal**
A_0	A_2
A_1	A_3
A_2	A_5
A_3	A_6
A_4	A_7
A_5	A_{12}
A_6	A_{10}
A_7	A_{11}
A_8	A_9
A_9	A_8
A_{10}	A_{14}
A_{11}	A_{13}
A_{12}	A_0
A_{13}	A_1
A_{14}	A_4
A_{15}	A_{15}

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM99C641-25, AM99C641-35	PC, PCB, DC, DCB, LC, LCB
AM99C641-45, AM99C641-55, AM99C641-70	PC, PCB, DC, DCB, DE, DEB, LC, LCB, LE, LEB

*Preliminary. Subject to Change.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

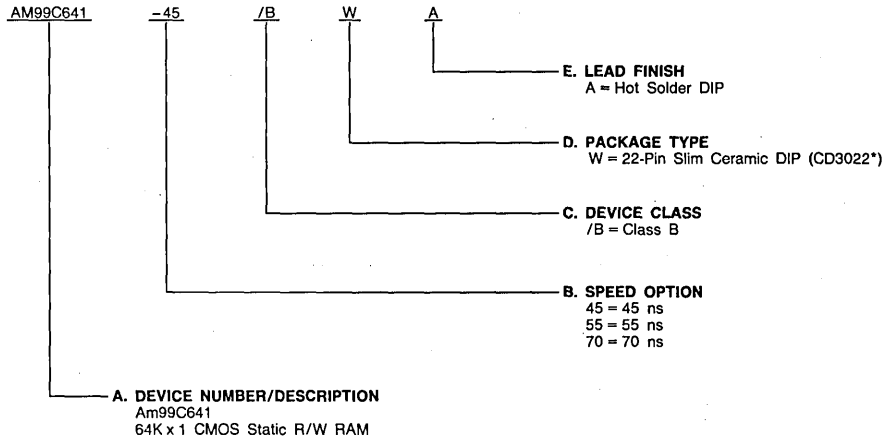
ORDERING INFORMATION
APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

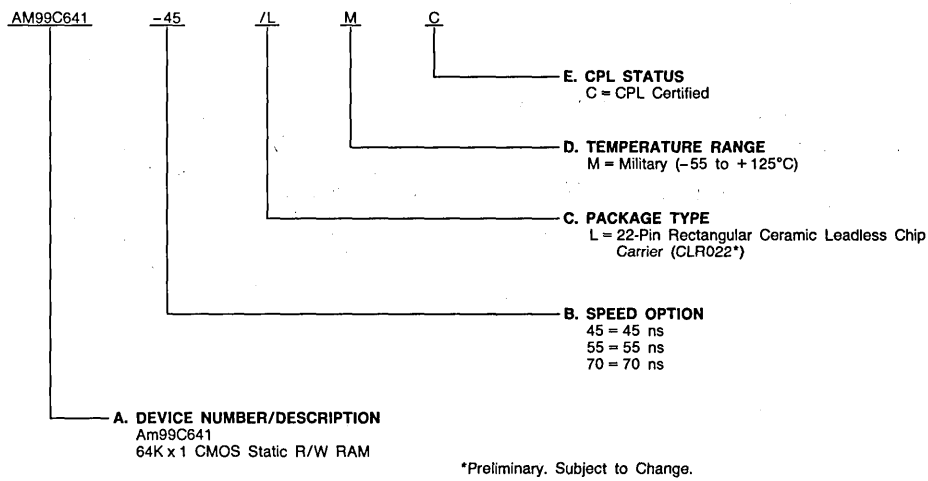
APL Products:
A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

CPL Products:
A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status

APL Products



CPL Products



*Preliminary. Subject to Change.

	Valid Combinations	
APL	AM99C641-45, AM99C641-55, AM99C641-70,	/BWA
CPL	AM99C641-45, AM99C641-55, AM99C641-70	/LMC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

A_0-A_{15} Address (Inputs)
The Address input lines select the RAM location to be read or written.

$\overline{CE}$ Chip Enable (Input, Active LOW)
The Chip Enable selects the memory device. $\overline{WE}$ is ignored when $\overline{CE}$ is HIGH.

$\overline{WE}$ Write Enable (Input, Active LOW)
When $\overline{WE}$ is LOW and $\overline{CE}$ is LOW, data will be written into the location specified on the Address pins. When $\overline{WE}$ is HIGH and $\overline{CE}$ is LOW, data will be read out and placed on the D_{OUT} pin.

D_{IN} Data Input
This pin is used for entering data during write operations.

D_{OUT} Data Output (Three-State)
This pin is three-state during write operations. It becomes active when $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1*)

Storage Temperature
- Ceramic Packages ..... −65 to +150°C
- Plastic Packages ..... −55 to +125°C

Ambient Temperature with Power Applied
- Ceramic Packages ..... −55 to +125°C
- Plastic Packages ..... −10 to +85°C

DC Supply Voltage to Ground Potential Continuous ..... −0.5 to +7.0 V

All Signal Voltages ..... −0.5 to +7.0 V

DC Output Current ..... 20 mA

Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2*)

Commercial (C) Devices
- Temperature (T_A) ..... 0 to +70°C
- Supply Voltage (V_{CC}) ..... 4.5 to +5.5 V

Extended Commercial (E) and Military (M) Devices
- Temperature (T_A − E Devices) (T_C − M Devices) ..... −55 to +125°C
- Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

* See notes following Switching Characteristics table.

DC CHARACTERISTICS over operating range unless otherwise specified

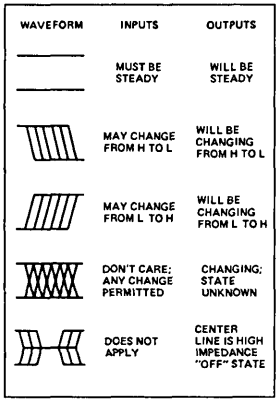
Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 1.0	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_{IN} \leq V_{CC}$			2.0	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, $\overline{CE} \geq V_{IH}$			2.0	μA
I_{DD}	Static Operating Supply Current	$\overline{CE} \leq V_{IL}$; I/O = 0 mA	T_{AA} = 25/35 ns		60.0	mA
			T_{AA} = 45 ns		50.0	
			T_{AA} = 55/70 ns		50.0	
I_{DD1}	Dynamic Operating Supply Current	Cycle = Min.; Duty = 100%; $\overline{CE} \leq V_{IL}$; I/O = 0 mA	T_{AA} = 25 ns		130.0	mA
			T_{AA} = 35 ns		110.0	
			T_{AA} = 45 ns		90.0	
			T_{AA} = 55/70 ns		90.0	
I_{SB}		$\overline{CE} = V_{IH}$			20.0	mA
I_{SBC}	Standby Power Supply Current	$\overline{CE} \geq V_{CC}$ − 0.2 V	Com'l.		14.0	mA
		$V_{IN} \geq V_{CC}$ − 0.2 V or ≤ 0.2 V	Mil.		16.0	

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_I	Input Capacitance	f = 1 MHz, V_{IN} = 0 V		6.0	pF
C_O	Output Capacitance	V_{OUT} = 0 V		7.0	

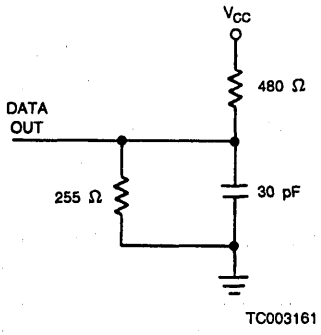
* These capacitances are not 100% tested, but are evaluated at initial characterization and at any time the product is modified where capacitance may be affected.

KEY TO SWITCHING WAVEFORMS



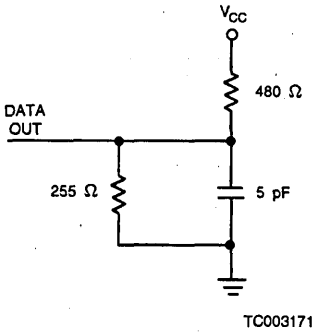
KS000010

SWITCHING TEST CIRCUITS



TC003161

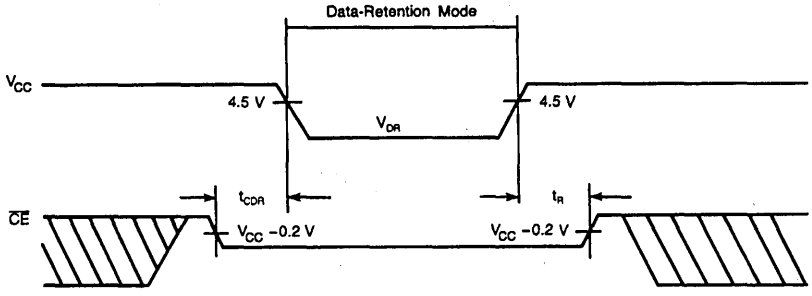
Test Load A



TC003171

Test Load B

SWITCHING TEST WAVEFORM



WF021431

Low V_{CC} Data Retention Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CE} \geq V_{CC}$ -0.2 V	2.0		V
I_{DDDR}	Data Retention Current	V_{CC} = 2.0 V		4.0	mA
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	See waveform (Note 2)	0		ns
t_R	Operating Recovery Time (Note 1)		t_{RC}		ns

Notes: 1. Parameter not tested, guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)
(Table continued on next page)

No.	Parameter Symbol STD	Parameter Symbol ALT	Parameter Description	Device Number	Min.	Max.	Units
Read Cycles One and Two							
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time	Am99C641-25		25	ns
				Am99C641-35		35	
				Am99C641-45		45	
				Am99C641-55		55	
				Am99C641-70		70	
2	t_{AVAV}	t_{RC}	Read Cycle Time	Am99C641-25	25		ns
				Am99C641-35	35		
				Am99C641-45	45		
				Am99C641-55	55		
				Am99C641-70	70		
3	t_{AVQV}	t_{AA}	Address Access Time	Am99C641-25		25	ns
				Am99C641-35		35	
				Am99C641-45		45	
				Am99C641-55		55	
				Am99C641-70		70	
4	t_{AXQX}	t_{OH}	Output Hold After Address	Am99C641-25	3		ns
				All others	5		

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1) (Cont'd.)

No.	Parameter Symbol		Parameter Description	Device Number	Min.	Max.	Units
	STD	ALT					
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active (Note 7)	Am99C641-25	3		ns
				All others	5		
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable (Note 7)	Am99C641-25	0	15	ns
				Am99C641-35	0	15	
				Am99C641-45	0	15	
				Am99C641-55	0	20	
				Am99C641-70	0	20	
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up (Note 3)	All versions	0		ns
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down (Note 3)	Am99C641-25	0	25	ns
				Am99C641-35	0	35	
				Am99C641-45	0	45	
				Am99C641-55	0	55	
				Am99C641-70	0	70	
Write Cycle 1							
9	t_{AVAV}	T_{WC}	Write Cycle Time	Am99C641-25	25		ns
				Am99C641-35	35		
				Am99C641-45	45		
				Am99C641-55	55		
				Am99C641-70	70		
10	t_{WLWH}	t_{WP}	Write Pulse Width (Note 5)	Am99C641-25	20		ns
				Am99C641-35	25		
				Am99C641-45	25		
				Am99C641-55	30		
				Am99C641-70	40		
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write (Note 5)	Am99C641-25	25		ns
				Am99C641-35	35		
				Am99C641-45	40		
				Am99C641-55	50		
				Am99C641-70	65		
12	t_{DVWH}	t_{DW}	Data Setup to End of Write	Am99C641-25	20		ns
				Am99C641-35	25		
				Am99C641-45	25		
				Am99C641-55	30		
				Am99C641-70	30		
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	All Versions	0		ns
14	t_{AVWH}	t_{AW}	Address Setup to End of Write (Note 5)	Am99C641-25	20		ns
				Am99C641-35	30		
				Am99C641-45	40		
				Am99C641-55	50		
				Am99C641-70	65		
15	t_{AVWL}	t_{AS}	Address Setup to Beginning of Write	All Versions	0		ns
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	All Versions	0		ns
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable (Notes 6 & 7)	Am99C641-25	0	10	ns
				Am99C641-35	0	15	
				Am99C641-45	0	20	
				Am99C641-55	0	25	
				Am99C641-70	0	30	

4

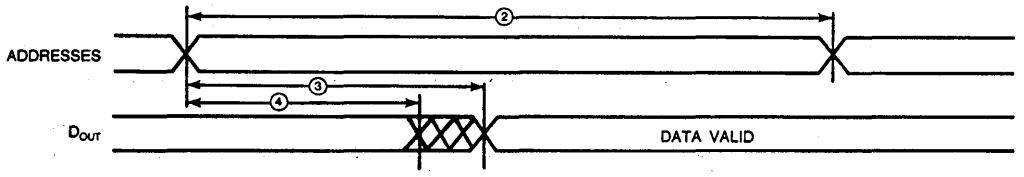
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1) (Cont'd.)

No.	Parameter Symbol		Parameter Description	Device Number	Min.	Max.	Units
	STD	ALT					
18	t_{WHQX}	t_{OW}	Output Active After End of Write (Notes 6 & 7)	Am99C641-25	0	20	ns
				Am99C641-35	0	20	
				Am99C641-45	0	25	
				Am99C641-55	0	30	
				Am99C641-70	0	40	
Write Cycle Two							
19	t_{AVAV}	t_{WC}	Write Cycle Time	Am99C641-25	25		ns
				Am99C641-35	35		
				Am99C641-45	45		
				Am99C641-55	55		
				Am99C641-70	70		
20	t_{WLEH}	t_{WP}	Write Pulse Width (Note 5)	Am99C641-25	20		ns
				Am99C641-35	25		
				Am99C641-45	25		
				Am99C641-55	30		
				Am99C641-70	30		
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write (Note 5)	Am99C641-25	25		ns
				Am99C641-35	35		
				Am99C641-45	40		
				Am99C641-55	50		
				Am99C641-70	65		
22	t_{DVEH}	t_{DW}	Data Setup to End of Write	Am99C641-25	20		ns
				Am99C641-35	25		
				Am99C641-45	25		
				Am99C641-55	30		
				Am99C641-70	30		
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	All Versions	0		ns
24	t_{AVEH}	t_{AW}	Address Setup to End of Write (Note 5)	Am99C641-25	20		ns
				Am99C641-35	30		
				Am99C641-45	40		
				Am99C641-55	50		
				Am99C641-70	60		
25	t_{AVEL}	t_{AS}	Address Setup to Beginning of Write	All Versions	0		ns
26	t_{EHAX}	t_{WR}	Address Hold After End of Write	All Versions	0		ns
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable (Notes 6 & 7)	Am99C641-25	0	10	ns
				Am99C641-35	0	15	
				Am99C641-45	0	20	
				Am99C641-55	0	25	
				Am99C641-70	0	30	
28		t_T	Input Rise and Fall Times	All Versions	3	50	ns

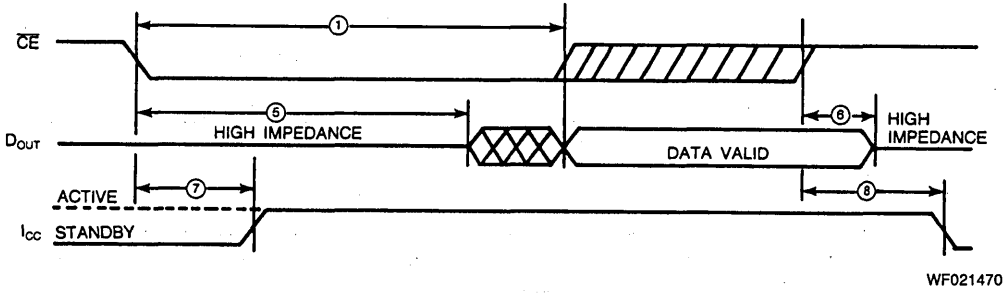
Notes*:

1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Parameter not tested—guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input-pulse levels of 0 to 3.0 V, and output loading of specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V (see Test Load A in Switching Test Circuits section).
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ LOW. Both signals must be active to initiate a write and either signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in Test Load B—Switching Test Circuits. Transition is measured ±500 mV from steady state voltage.

SWITCHING WAVEFORMS (Cont'd.)



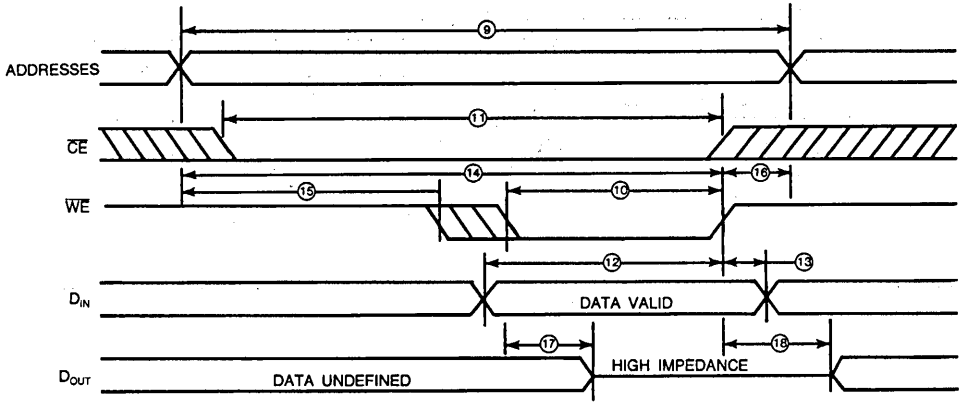
Read Cycle One



Read Cycle Two

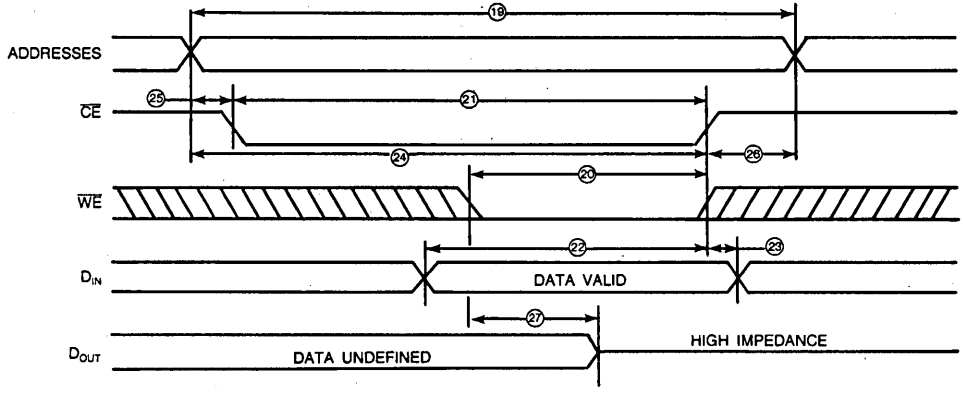
4

SWITCHING WAVEFORMS



WF021440

Write Cycle One



WF021451

Write Cycle Two

Am99C68/Am99CL68

4096 x 4 CMOS Static R/W Random-Access Memory

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 45 ns
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected
- Low power dissipation:
  - Active: 660 mW Max.
  - Standby: 11 mW Max. (Am99C68)
    275 µW Max. (Am99CL68)
- Standard 20-pin, .300-inch dual-in-line package
- TTL-compatible interface levels
- 2-V data retention

GENERAL DESCRIPTION

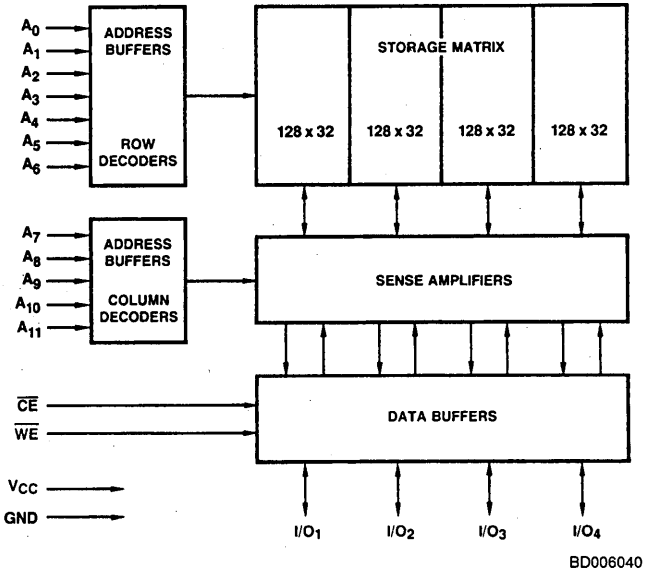
The Am99C68 and Am99CL68 are high-performance CMOS static random- access memories. Organized as 4096 words of 4 bits, the device operation is from a single +5-volt supply and all input/output levels are TTL compatible.

Both devices enter the standby power mode when $\overline{CE}$ is taken HIGH. They go into a full standby mode when, in addition to $\overline{CE}$ being HIGH, V_{IN} is either greater than (V_{CC} −0.2 V) or less than 0.2 V. In the full standby power mode, the Am99C68 draws 2 mA and the Am99CL68 draws only 50 µA.

Both devices have a data retention mode which allows them to maintain memory when V_{CC} is as low as 2.0 V.

Data readout is not destructive and has the same polarity as data input.

BLOCK DIAGRAM



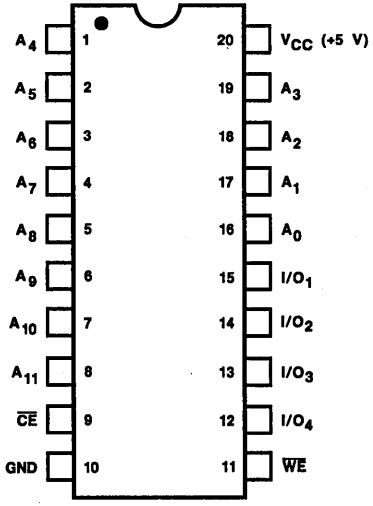
BD006040

PRODUCT SELECTOR GUIDE

Family Part Number		Am99C68/Am99CL68							
Ordering Part Number		99C68-35	99CL68-35	99C68-45	99CL68-45	99C68-55	99CL68-55	99C68-70	99CL68-70
Maximum Access Time (ns)		TBD*		45		55		70	
I_{CC} Max. (mA)	C Devices	TBD		100		100		100	
	M Devices	TBD		120		120		120	
I_{SB} Max. (mA)		TBD		20		20		20	
I_{SBI} Max. (μA)		TBD	TBD	2000	50	2000	50	2000	50
I_{CCDR} Max. (μA)		TBD	TBD	1600	40	1600	40	1600	40

*TBD = To Be Determined.

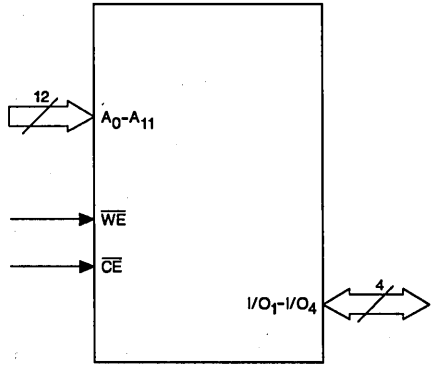
CONNECTION DIAGRAM
Top View



CD009350

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



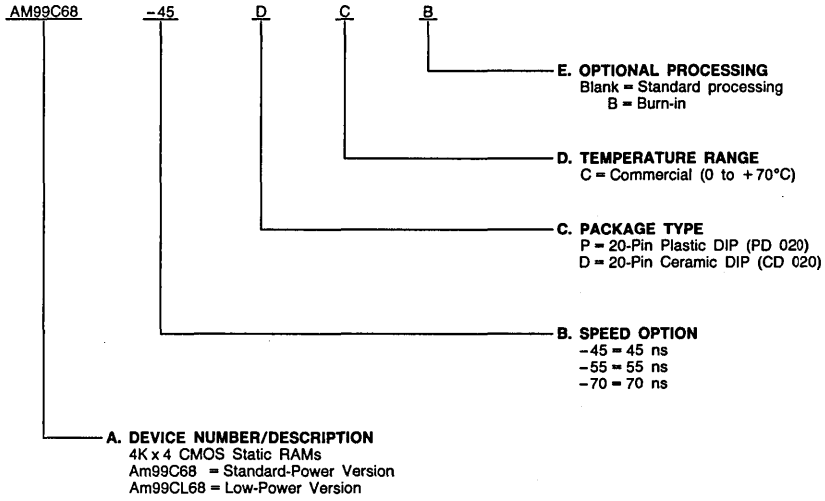
LS002320

V_{CC} = +5-V Power Supply
GND = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM99C68-45	DC, DCB, PC, PCB
AM99CL68-45	
AM99C68-55	
AM99CL68-55	
AM99C68-70	
AM99CL68-70	

Valid Combinations

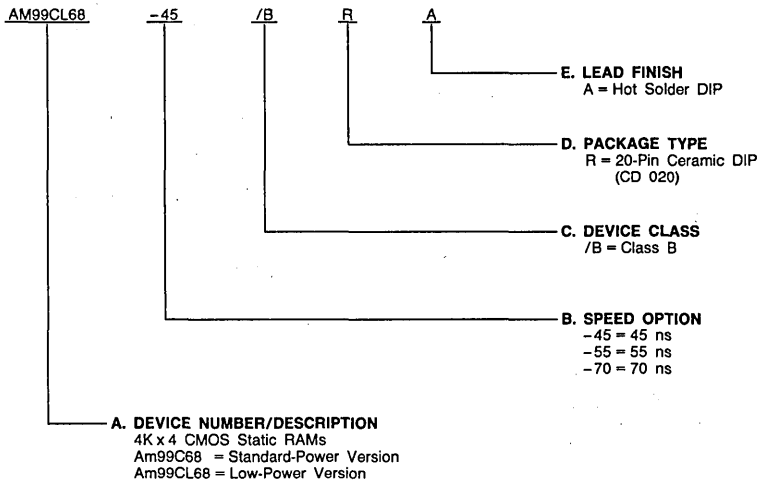
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM99C68-45	/BRA
AM99CL68-45	
AM99C68-55	
AM99CL68-55	
AM99C68-70	
AM99CL68-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Line (Inputs)
These inputs select the desired location (memory cell) that data is read from or written to.

$\overline{WE}$ Write Enable (Input, Active LOW)
This input enables data to be written into the memory location selected by the address when $\overline{CE}$ is active.

$\overline{CE}$ Chip Enable (Input, Active LOW)
$\overline{CE}$ acts as a general enable for the part. When $\overline{CE}$ is active LOW and $\overline{WE}$ is HIGH, data will be read. When $\overline{CE}$ is active HIGH and $\overline{WE}$ is LOW, data will be written.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional, active HIGH)
These I/O lines provide the path for data to be read from or written to the selected memory cell.

V_{CC} +5-Volt Power Supply

GND 0-Volt Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- Ceramic DIPs ..... −65 to +150°C
- Plastic DIPs ..... −55 to +150°C

Ambient Temperature with Power Applied
- Ceramic DIPs ..... −55 to +125°C
- Plastic DIPs ..... −10 to +85°C

Supply Voltage with Respect to Ground ..... −0.5 to +7.0 V

All Signal Voltages with Respect to Ground ..... −0.5 to +7.0 V

DC Output Short-Circuit Current, into Outputs (Note 1) ..... 25 mA

Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Temperature (T_A) ..... 0 to +70°C
- Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military (M) Devices
- Temperature (T_A) ..... −55 to +125°C
- Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 4)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V		−4.0		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	C Devices	8.0		mA
			M Devices	8.0		
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{IL}	Input LOW Voltage	(Note 3)		−0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		−5.0	5.0	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		−5.0	5.0	μA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CE} \leq V_{IL}$ Output Open, Max. Frequency	C Devices		100.0	mA
			M Devices		120.0	
I_{SB}	Automatic Power-Down Current	Max. V_{CC}, ($\overline{CE} \geq V_{IH}$)			20.0	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CE} \geq V_{IH}$, $V_{IN} \geq (V_{CC} - 0.2\ V)$ or ≤ 0.2 V	Am99C68		2,000	μA
			Am99CL68		50.0	

4

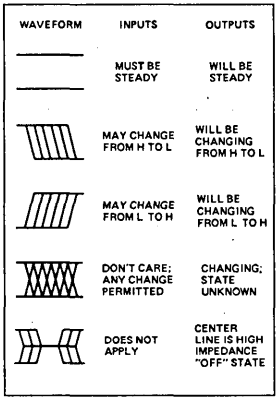
CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_I	Input Capacitance	Test Frequency = 1.0 MHz, T_A = 25°C, All pins at 0 V, V_{CC} = 5 V (Note 7)		6.0	pF
$C_{I/O}$	Input/Output Capacitance			7.0	

Notes*: 1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. V_{IL} voltages of less than −0.5 V on the I/O pins will cause the output current to exceed the maximun rating. −0.1-V and −3.0-V pulses can be tolerated for up to 50 ns and 10 ns respectively.
4. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} and t_{WZ} is less than t_{OW} for all devices. Transition is measured from the inputs at 1.5 V to the outputs at 1.0 V, and 0.9 V using the load shown in Test Circuit B (see Switching Test Circuits). C_L = 5 pF.
6. The minimum limit is not tested and is included as user-guidelines only.
7. These parameters are not tested, but are guaranteed by characterization.

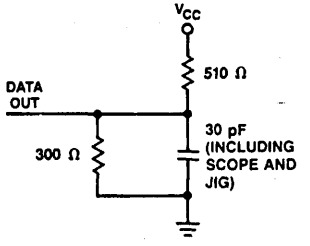
*Notes listed also correspond to references made in Switching Characteristics table.

KEY TO SWITCHING WAVEFORMS



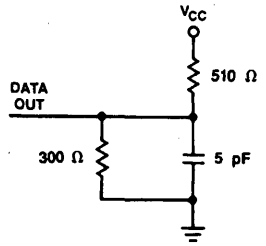
KS000010

SWITCHING TEST CIRCUITS



TC003360

A. Output Load

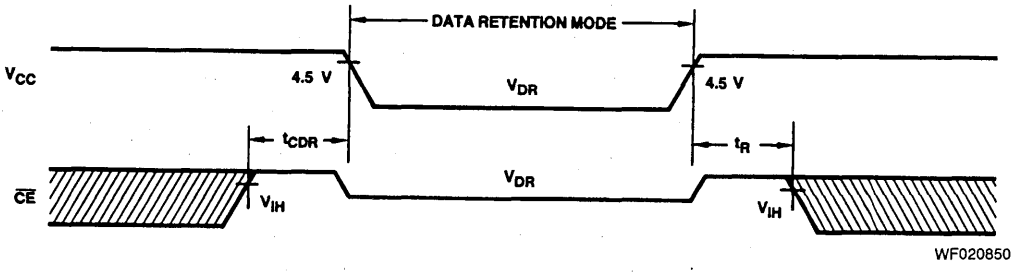


TC003370

B. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

Data Retention Characteristics

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2$ V	Am99C68		1600	µA
			Am99CL68		40	
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	$V_{IN} \geq (V_{CC} - 0.2\ V)$ or ≤ 0.2 V		0		ns
t_R	Operation Recovery Time (Note 1)			t_{RC}		ns



Data Retention Waveform (Note 2)

Notes: 1. Parameter is not tested, but is guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

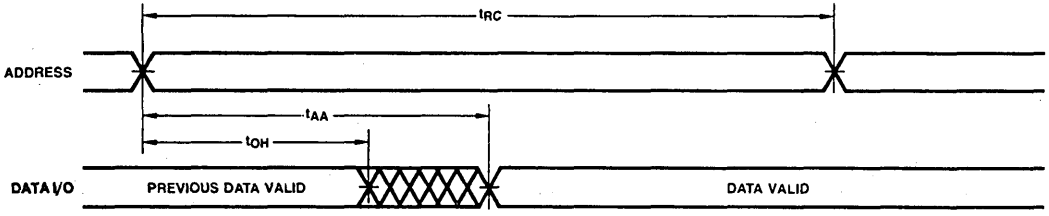
4

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameter No.	Parameter Symbol	Parameter Description	Am99C68-35 Am99CL68-35		Am99C68-45 Am99CL68-45		Am99C68-55 Am99CL68-55		Am99C68-70 Am99CL68-70		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	TBD*		45		55		70		ns
2	t_{AA}	Address Valid to Data-Out Valid Delay (Address Access Time)		TBD		45		55		70	ns
3	t_{ACS}	Chip Enable LOW to Data-Out Valid (Chip Enable Access Time)		TBD		45		55		70	ns
4	t_{LZ}	Chip Enable LOW to Data-Out On (Note 5)	TBD		5		5		5		ns
5	t_{HZ}	Chip Enable HIGH to Data-Out Off (Notes 5 & 6)		TBD	0	20	0	25	0	30	ns
6	t_{OH}	Address Unknown to Data-Out Unknown Time	TBD		5		5		5		ns
7	t_{PD}	Chip Enable HIGH to Power-Down Delay (Note 7)		TBD		45		55		70	ns
8	t_{PU}	Chip Enable LOW to Power-On Delay (Note 7)	TBD		0		0		0		ns
WRITE CYCLE											
9	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)	TBD		40		50		60		ns
10	t_{WP}	Write Enable LOW to Write Enable HIGH (Note 2)	TBD		35		45		60		ns
11	t_{WR}	Write Enable HIGH to Address Do Not Care			0		0		0		ns
12	t_{WZ}	Write Enable LOW to Output in High Z (Notes 5 & 6)		TBD	0	20	0	25	0	30	ns
13	t_{DW}	Data In Valid to Write Enable HIGH	TBD		15		20		30		ns
14	t_{DH}	Data Hold Time	TBD		3		3		3		ns
15	t_{AS}	Address Valid to Write Enable LOW			0		0		0		ns
16	t_{CW}	Chip Enable LOW to Write Enable HIGH (Note 2)	TBD		35		45		60		ns
17	t_{OW}	Write Enable HIGH to Output In Low Z (Note 5)	TBD		5		5		5		ns
18	t_{AW}	Address Valid to End of Write	TBD		35		45		60		ns

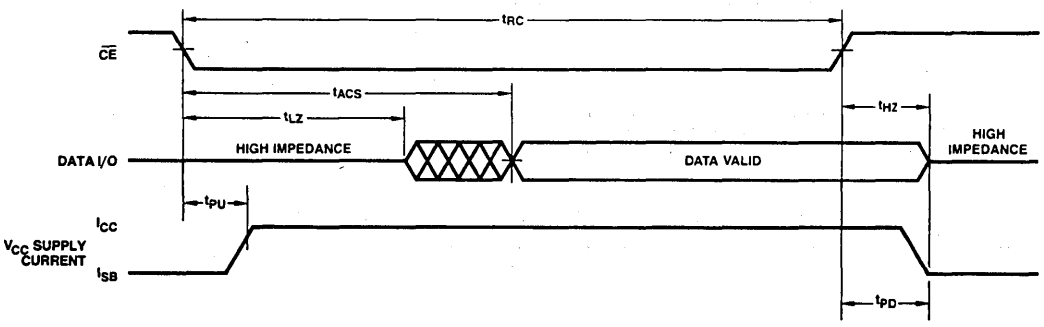
Notes: See notes following DC Characteristics table.
*TBD = To Be Determined.

SWITCHING WAVEFORMS (Cont'd.)



WF020860

Read Cycle No. 1 — $\overline{WE}$ HIGH, $\overline{CE}$ LOW

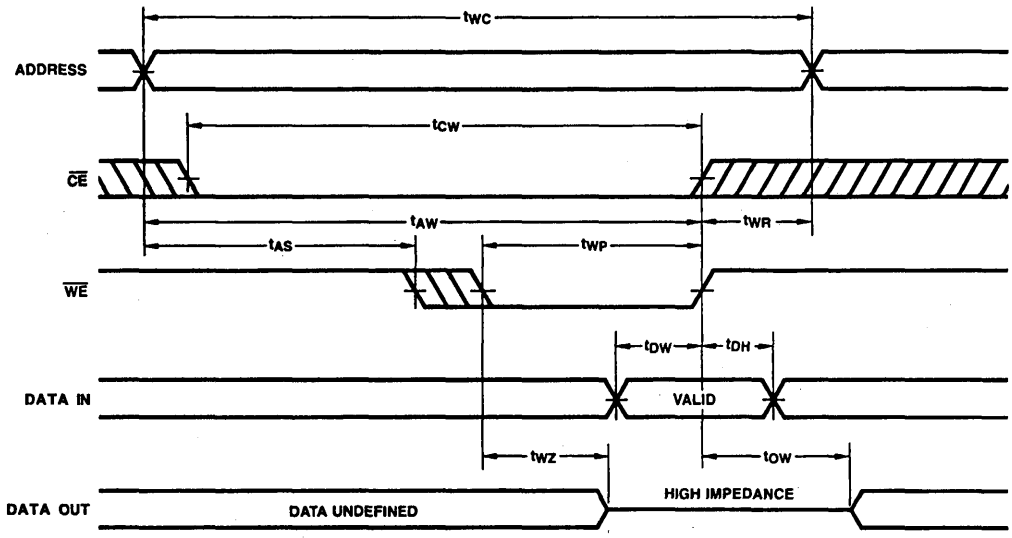


WF020870

Read Cycle No. 2 — $\overline{WE}$ HIGH, Address Valid Prior to $\overline{CE}$ Transition to LOW

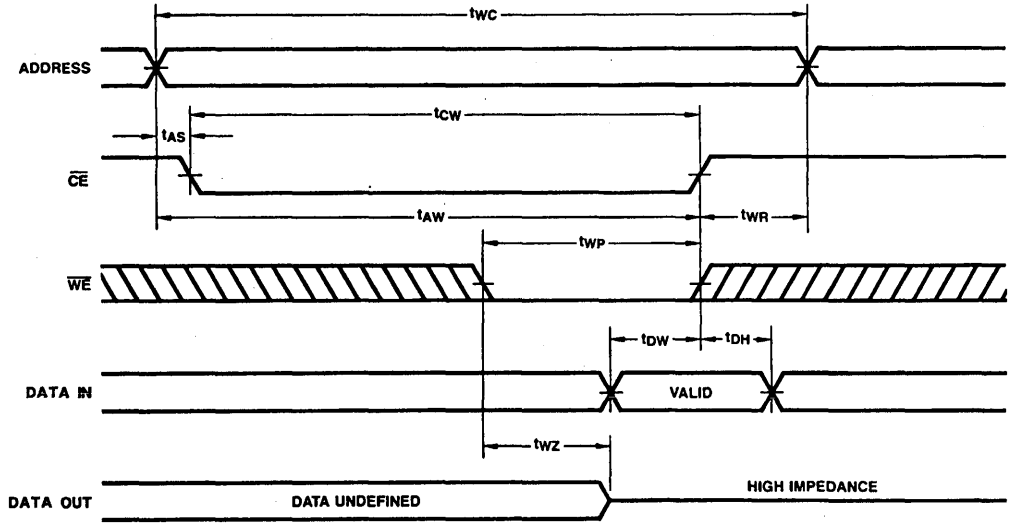
4

SWITCHING WAVEFORMS



WF020881

Write Cycle No. 1 — $\overline{WE}$ Controlled, $\overline{CE}$ Active Prior to $\overline{WE}$



WF020891

Write Cycle No. 2 — $\overline{CE}$ Controlled

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Am99C88/Am99CL88

8K x 8 CMOS Static Random-Access Memory

DISTINCTIVE CHARACTERISTICS

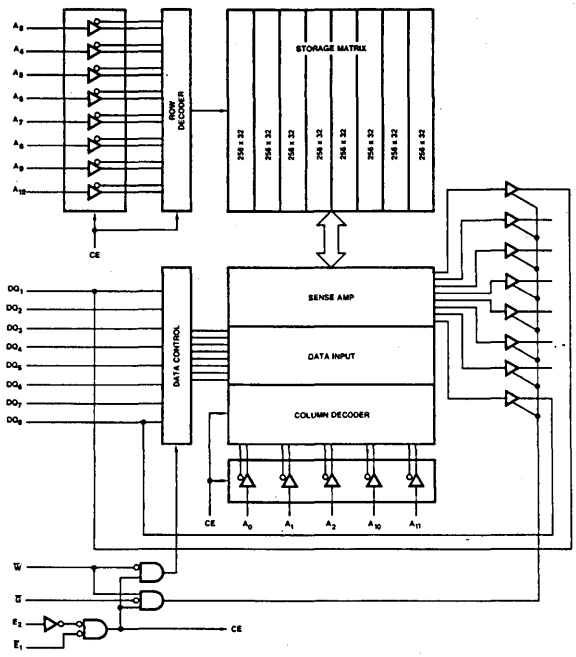
- High speed – access times 70/100/120/150 ns
- Low-power requirements:
  - Am99C88
    - Operating: 330 mW Max.
    - Standy: 16.5 mW Max.
  - Am99CL88
    - Operating: 220 mW Max.
    - Standby: 550 μW Max.
- Battery backed-up operation (2 V data retention)
- Fully static storage and interface (no clocks or timing signals required)
- TTL compatible interface levels
- Industry standard package (28-pin 0.6 in dual-in-line)
- Two chip enables ($\overline{E_1}$ and E_2) for ease of expansion and automatic power down
- Pin compatible with 2764 type programmable ROM

GENERAL DESCRIPTION

The Am99C88/Am99CL88 is a high-performance, low power CMOS static RAM organized as 8192 words of 8 bits each. In addition to 13 address inputs and 8 common data inputs and outputs, the device utilizes 4 control pins. Two of them, $\overline{E_1}$ and E_2, perform chip enable functions and automatically power down the device when proper polarity of logic levels are applied. The other control pins, $\overline{G}$ and $\overline{W}$, facilitate read and write operations, respectively. These control inputs, along with three-state data inputs/outputs, allow similar devices to be connected to a common bus.

The data read out is non-destructive and has the same polarity as the data stored. The data is retained by the device even at V_{DD} as low as 2 V. Am99C88/Am99CL88 requires a single 5 V power supply and dissipates 330 mW/220 mW maximum in operating mode and 16.5 mW/550 μW maximum in standby mode. The devices are packaged in industry-standard, 28-pin, 0.6-inch wide dual-in-line packages.

BLOCK DIAGRAM



BD005871

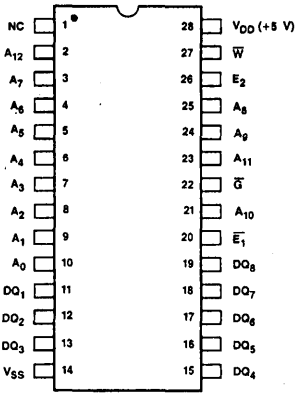
Publication # 06036 | Rev. C | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

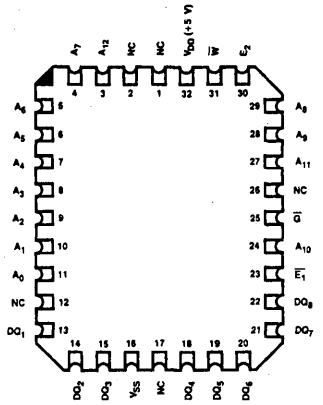
		Am99CS88					Am99C88					Am99CL88			
		-70	-10	-12	-15	-20	-70	-10	-12	-15	-20	-70	-10	-12	-15
Access Time Max (ns)		70	100	120	150	200	70	100	120	150	200	70	100	120	150
0 to 70°C	I_{DD1} Max (mA)	–	–	–	–	–	60	60	60	60	–	40	40	40	40
	I_{SB} Max (mA)	–	–	–	–	–	5	5	5	5	–	1	1	1	1
	$I_{SB1,2}$ Max (μA)	–	–	–	–	–	3000	3000	3000	3000	–	100	100	100	100
	I_{DDR} 2 V (μA)	–	–	–	–	–	1000	1000	1000	1000	–	50	50	50	50
−55 to +125°C	I_{DD1} Max. (mA)	60	60	60	60	60	60	60	60	60	60	–	–	–	–
	I_{SB} Max. (mA)	10	10	10	10	10	5	5	5	5	5	–	–	–	–
	$I_{SB1,2}$ Max. (μA)	10000	10000	10000	10000	10000	5000	5000	5000	5000	5000	–	–	–	–
	I_{DDR} 2 V (μA)	5000	5000	5000	5000	5000	1000	1000	1000	1000	1000	–	–	–	–

CONNECTION DIAGRAMS

Top View



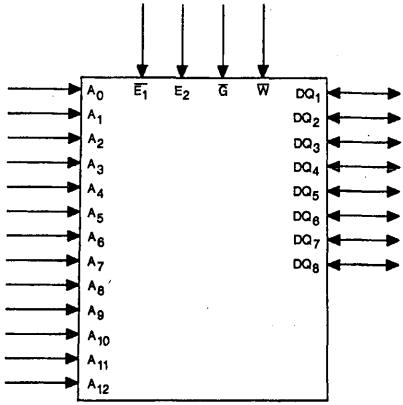
CD009132



CD009124

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002181

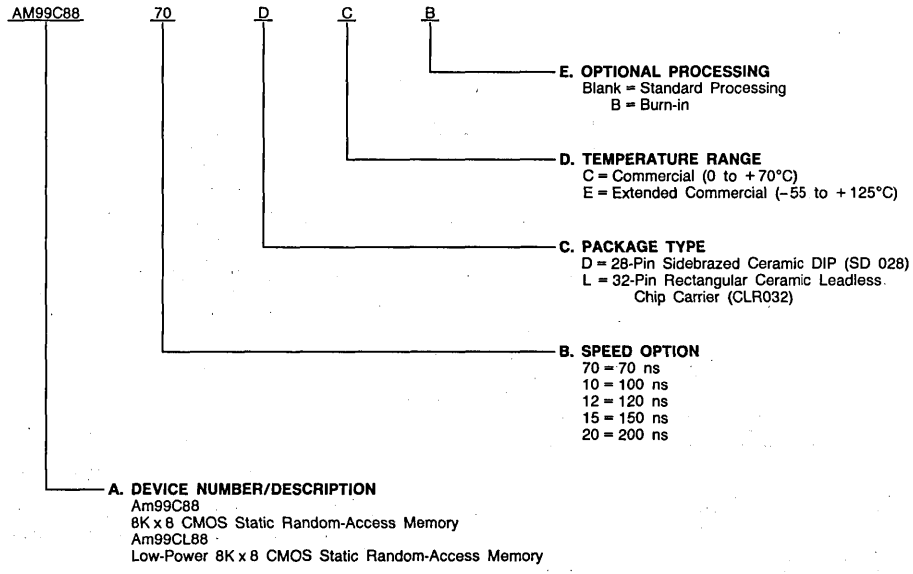
ADDRESS DESIGNATORS

External	Internal	Pin Number DIP Package
A_9	AX_0	24
A_3	AX_1	7
A_4	AX_2	6
A_5	AX_3	5
A_6	AX_4	4
A_7	AX_5	3
A_{12}	AX_6	2
A_8	AX_7	25
A_{11}	AY_0	23
A_{10}	AY_1	21
A_0	AY_2	10
A_1	AY_3	9
A_2	AY_4	8

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



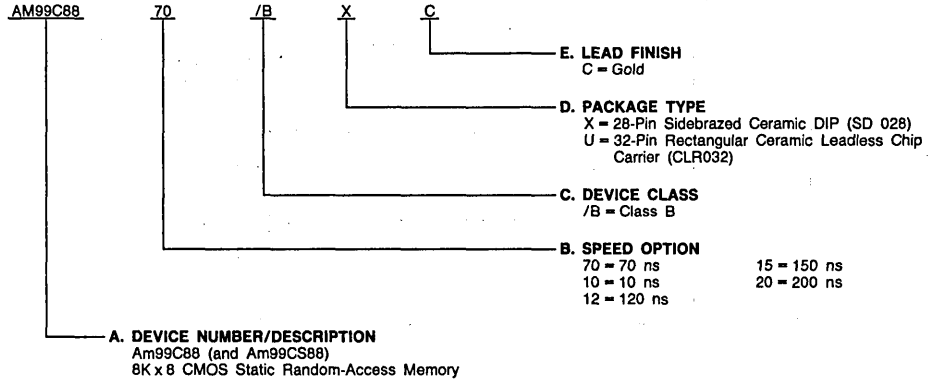
Valid Combinations	
AM99C88-70 AM99C88-10 AM99C88-12 AM99C88-15	DC, DCB, LC, LCB DE, DEB, LE, LEB
AM99C88-20	DE, DEB, LE, LEB
AM99CL88-70 AM99CL88-10 AM99CL88-12 AM99CL88-15	DC, DCB, LC, LCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM99CS88-70	/BXC, /BUC
AM99CS88-10	
AM99CS88-12	
AM99CS88-15	
AM99CS88-20	
AM99C88-70	/BXC, /BUC
AM99C88-10	
AM99C88-12	
AM99C88-15	
Am99C88-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{12}$ Address (Inputs)
The 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E_1}$ Chip Enable1 (Input)

E_2 Chip Enable2 (Input)
$\overline{E_1}$ is active LOW and E_2 is active HIGH. The device can be accessed only when both Chip Enables are active. If either Chip Enable is not active, the device is deselected and will be in a standby power mode. The DQ port will be in a high-impedance state.

$\overline{W}$ Write Enable (Input)
$\overline{W}$ controls read and write operations. When $\overline{W}$ is HIGH and $\overline{G}$ is LOW, data will be output at the DQ port. When $\overline{W}$ is LOW, data present on the DQ port will be written into the selected memory location.

$\overline{G}$ Output Enable (Input)
$\overline{G}$ controls the state of the outputs in conjunction with Chip Enable and $\overline{W}$.

$DQ_1 - DQ_8$ Data Input/Data Output Ports
Eight bidirectional ports used to write into or read data from the RAM.

V_{DD} Power Supply +5 Volts

V_{SS} Ground

FUNCTIONAL DESCRIPTION

Please refer to Table 1 for summary of Mode Select.

TABLE 1. MODE SELECT

$\overline{E_1}$	E_2	$\overline{W}$	$\overline{G}$	Output	Supply Current	Mode
H	X	X	X	Hi-Z	I_{SB}, I_{SB1}	Not Selected
X	L	X	X	Hi-Z	I_{SB}, I_{SB2}	Not Selected
L	H	H	H	Hi-Z	I_{DD}, I_{DD1}	Output Disabled
L	H	H	L	D_{OUT}	I_{DD}, I_{DD1}	Read
L	H	L	X	Hi-Z	I_{DD}, I_{DD1}	Write

H = HIGH
L = LOW
X = Don't Care

4

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... −0.5 to +7.0 V
All Signal Voltages ..... −0.5 to +7.0 V
DC Output Current ..... 20 mA
Power Dissipation
  Cerdip Packages ..... 1.0 W
  Plastic Packages ..... 1.0 W
Ambient Temperature with Power Applied
  Cerdip Packages ..... −55 to +125°C
  Plastic Packages ..... −10 to +85°C
Storage Temperature
  Cerdip Packages ..... −65 to +150°C
  Plastic Packages ..... −55 to +125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Supply Voltage ..... +4.5 to +5.5 V
Temperature ..... 0 to +70°C

Military (M) Devices*
Supply Voltage ..... +4.5 to +5.5 V
Temperature ..... −55 to +125°C

Operating ranges define those limits between which the functionality and parameters of the device are guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Am99CS88 Min.	Am99CS88 Max.	Am99C88 Min.	Am99C88 Max.	Am99CL88 Min.	Am99CL88 Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V V_{DD} = 4.5 V		−2		−2		−2		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V		4		4		4		mA
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 1.0	2.2	V_{DD} + 1.0	2.2	V_{DD} + 1.0	V
V_{IL}	Input LOW Voltage			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_{IN} \leq V_{DD}$			2		2		2	µA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{DD}$ $\overline{E_1} \geq V_{IH}$ or $E_2 \leq V_{IL}$ or $\overline{G} \geq V_{IH}$			2		2		2	µA
I_{DD}	Operating Supply Current	$\overline{E_1} \leq V_{IL}$ $E_2 \geq V_{IH}$ $I_{I/O}$ = 0 mA			60		60		40	mA
I_{DD1}	Average Operating Supply Current	Cycle = Min., Duty = 100% $\overline{E_1} \leq V_{IL}$, $E_2 \geq V_{IH}$, $I_{I/O}$ = 0 mA			60		60		40	mA
I_{SB}	Standby Power Supply Current	$\overline{E_1} = V_{IH}$ or $E_2 = V_{IL}$			10		5		1	mA
I_{SB1}		$\overline{E_1} \geq V_{DD}$ − 0.2 V, $E_2 \geq V_{DD}$ − 0.2 V or $E_2 \leq$ 0.2 V	COM'L		–		3000		100	µA
			MIL		10000		5000		–	
I_{SB2}		$E_2 \leq$ 0.2 V	COM'L		–		3000		100	µA
			MIL		10000		5000		–	

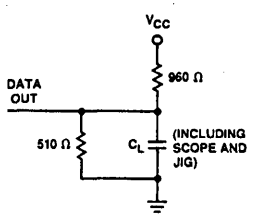
*See the last page of this spec for Group A Subgroup Testing information.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions		Am99CS88 Min.	Am99CS88 Max.	Am99C88 Min.	Am99C88 Max.	Am99CL88 Min.	Am99CL88 Max.	Units
C_I	Input Capacitance	f = 1 MHz	V_{IN} = 0 V		8		8		8	pF
$C_{I/O}$	Input/Output Capacitance		$V_{I/O}$ = 0 V		8		8		8	pF

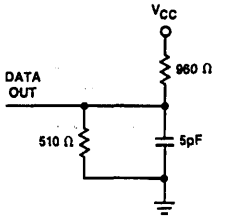
Notes: These parameters are not 100% tested, but are evaluated at initial characterisation and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUITS



TC002971

A.



TC002981

B.

C_L = 100 pF

SWITCHING CHARACTERISTICS (Notes 3-7)*

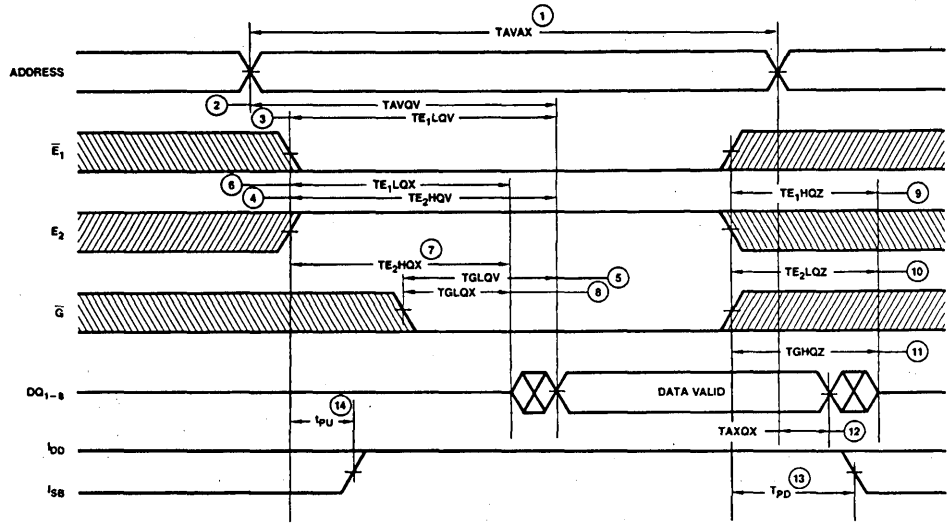
No.	Parameter Symbols		Parameter Description		Am99CS88/ Am99C88/ Am99CL88-70		Am99CS88/ Am99C88/ Am99CL88-10		Am99CS88/ Am99C88/ Am99CL88-12		Am99CS88/ Am99C88/ Am99CL88-15		AM99CS88/ Am99C88-20		Units
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE															
1	TAVAX	t_{RC}	Read Cycle Time (Address Valid to Address Don't Care)		70		100		120		150		200		ns
2	TAVQV	t_{AA}	Address Access Time (Address Valid to Data Out Valid)			70		100		120		150		200	ns
3	TE_1LQV	t_{CE1}	Chip Enable Access Time(Chip Enable Valid to Data Out Valid)	$\overline{E_1}$		70		100		120		150		200	ns
4	TE_2HQV	t_{CE2}		E_2		70		100		120		150		200	
5	TGLQV	t_{OE}	Output Enable Valid to Data Out Valid			40		50		60		70		90	ns
6	TE_1LQX	t_{LZ1}	Chip Enable Valid to Data Out On (Note 7)	$\overline{E_1}$	10		10		10		10		10		ns
7	TE_2HQX	t_{LZ2}		E_2	10		10		10		10		10		
8	TGLQX	t_{OLZ}	Output Enable Valid to Data Out On (Note 7)		5		5		5		5		5		ns
9	TE_1HQZ	t_{HZ1}	Chip Enable Not Valid to Data Out Off (Notes 6 & 7)	$\overline{E_1}$	0	35	0	35	0	40	0	50	0	60	ns
10	TE_2LQZ	t_{HZ2}		E_2	0	35	0	35	0	40	0	50	0	60	
11	TGHQZ	t_{OHZ}	Output Enable Not Valid to Data Out Off (Notes 6 & 7)		0	30	0	35	0	40	0	50	0	60	ns
12	TAXQX	t_{OH}	Output Hold from Address Change		3		3		3		3		3		ns
13		t_{PD}	Chip Disable to Power-Down Delay (Note 3)			40		50		60		70		90	ns
14		t_{PU}	Chip Enable to Power Up (Note 3)		0		0		0		0		0		
WRITE CYCLE															
15	TAVAX	t_{WC}	Write Cycle Time (Address Valid to Addres Don't Care)		70		100		120		150		200		ns
16	TE_1LWH	t_{CW}	Chip Enable to End of Write (Note 5)	$\overline{E_1}$	65		80		85		100		140		ns
17	TE_2HWH	t_{CW}		E_2	65		80		85		100		140		ns
18	TAVWL	t_{AS}	Address Setup Time		0		0		0		0		0		ns
19	TAVWH	t_{AW}	Address Valid to End of Write		65		80		85		100		140		ns
20	TWLWH	t_{WP}	Write Pulse Width (Note 5)		60		60		70		90		120		ns
21	TWHAX	t_{WR1}	End of Write to Address Don't Care	$\overline{E_1}, \overline{W}$	5		5		5		10		15		ns
22	TE_2LAX	t_{WR2}		E_2	15		15		15		15		20		
23	TWHQX	t_{OW}	Write Enable LOW to Data Out Off (Notes 6,7)		0	30	0	35	0	40	0	50	0	60	ns
24	TWLQZ	t_{WHZ}	Data in Valid to Write Enable HIGH		30		40		50		60		70		ns
25	TWHDX	t_{DH}	Write Enable HIGH to Data Don't Care		0		0		0		0		0		ns
26	TWHQX	t_{OW}	Write Enable HIGH to Data Out Active (Note 7)		10		10		10		10		10		ns

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
3. Parameter not tested, guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 100 pF load capacitance. Output timing reference is 1.5 V.
5. The internal write time of the memory is defined by the overlap of $\overline{E_1}$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in B. under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

4

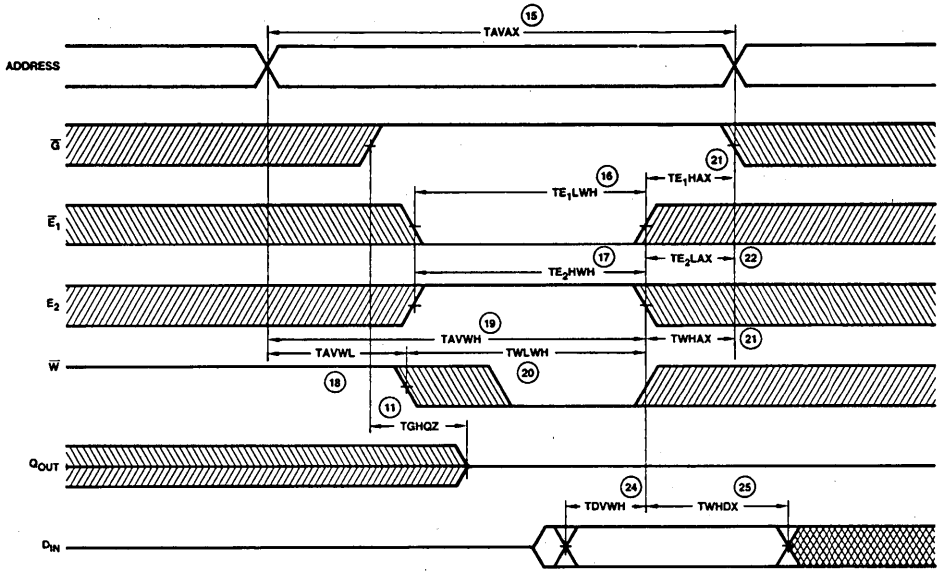
SWITCHING WAVEFORMS (Cont'd.)



WF021790

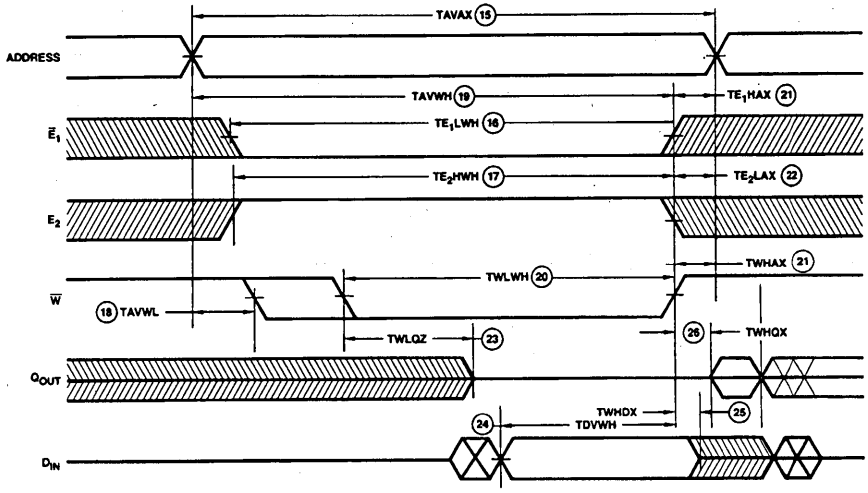
Read Cycle ($\overline{W}$ HIGH)

SWITCHING WAVEFORMS



WF021770

Write Cycle 1

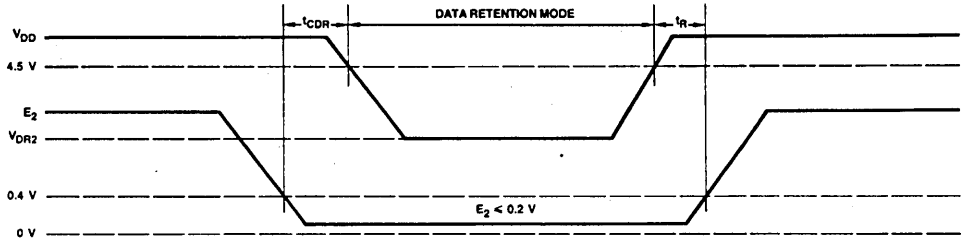


WF021780

Write Cycle 2 ($\overline{G}$ LOW)

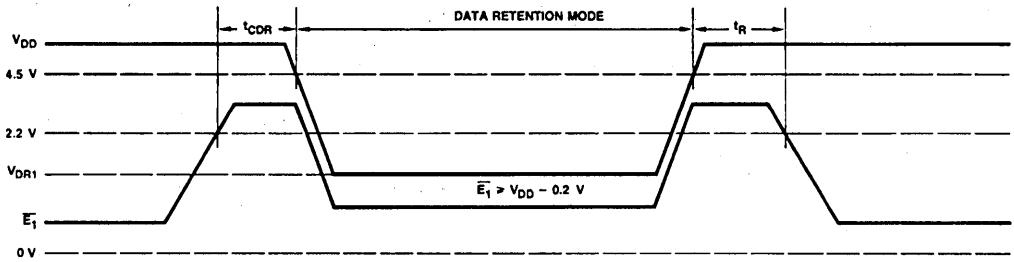
LOW V_{DD} DATA RETENTION CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Am99CS88		Am99C88		Am99CL88		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DR1}	V_{DD} for Data Retention	$\overline{E_1} \geq V_{DD}-0.2$, $E_2 \geq V_{DD}-0.2$ V or $E_2 \leq 0.2$ V	2.0		2.0		2.0		V
V_{DR2}		$E_2 \leq 0.2$ V							
I_{DDR1}	Data Retention Current	V_{DD} = 0.2 V, $\overline{E_1} \geq V_{DD}-0.2$ V, $E_2 \geq 0.2$ V or $E_2 \leq 0.2$ V		5000		1000		50	µA
I_{DDR2}		V_{DD} = 2.0 V, $E_2 \leq 0.2$ V		5000		1000		50	µA
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	See Waveform (Note 2)	0		0		0		ns
t_R	Operating Recovery Time (Note 1)		t_{RC}		t_{RC}		t_{RC}		ns



WF021800

Low V_{DD} Data Retention Waveform 1 (E_2 Controlled)



WF021811

Low V_{DD} Data Retention Waveform 2 ($\overline{E_1}$ Controlled, $E_2 \geq V_{DD}-0.2$ V or $E_2 \leq 0.2$ V)

Notes: 1. Parameter not tested, guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{DD}	1, 2, 3
I_{DD1}	1, 2, 3
I_{SB}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVAX (t_{RC})	7, 8, 9, 10, 11	17	TE_2HWH (t_{CW})	7, 8, 9, 10, 11
2	TAVQV (t_{AA})	7, 8, 9, 10, 11	18	TAVWL (t_{AS})	7, 8, 9, 10, 11
3	TE_1LQV (t_{CE1})	7, 8, 9, 10, 11	19	TAVWH (t_{AW})	7, 8, 9, 10, 11
4	TE_2HQV (t_{CE2})	7, 8, 9, 10, 11	20	TWLWH (t_{WP})	7, 8, 9, 10, 11
5	TGLQV (t_{OE})	7, 8, 9, 10, 11	21	TWHAX (t_{WR1})	7, 8, 9, 10, 11
8	TGLQX (t_{OLZ})	7, 8, 9, 10, 11	22	TE_2LAX (t_{WR2})	7, 8, 9, 10, 11
12	TAXQX (t_{OH})	7, 8, 9, 10, 11	24	TWLQZ (t_{WHZ})	7, 8, 9, 10, 11
15	TAVAX (t_{WC})	7, 8, 9, 10, 11	25	TWHDX (t_{DH})	7, 8, 9, 10, 11
16	TE_1LWH (t_{CW})	7, 8, 9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am99C88H

8192 x 8 CMOS Static Random-Access Memory

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- High Speed
  - 35 ns Commercial
  - 45 ns Military
- Low active power dissipation
  - 605 mW Maximum
- Low standby power dissipation
  - 138 mW Maximum
- Battery backup operation
  - 2-V data retention
- Single 5-V ±10% power-supply operation
- Common data inputs and outputs
- Fully static operation and interface
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Standard 28-pin, 600-mil DIP, and 32-pin ceramic leadless and plastic leaded chip carriers

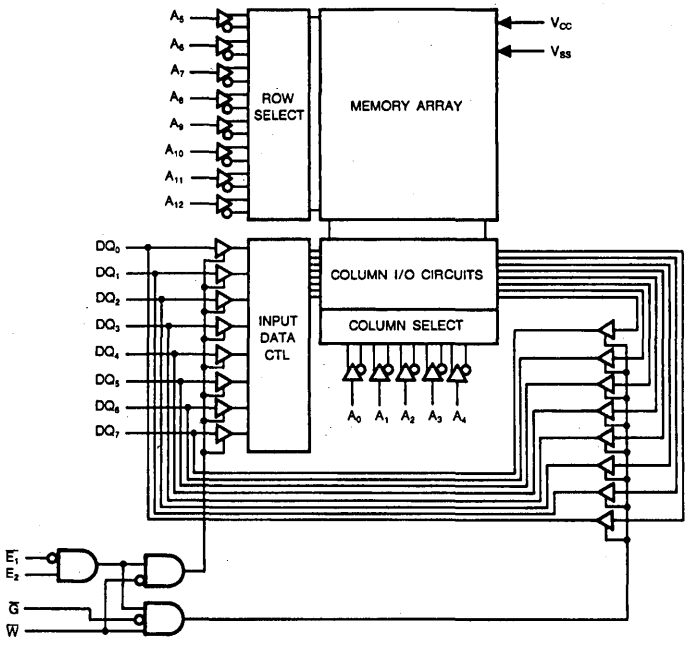
GENERAL DESCRIPTION

The Am99C88H is a high-performance CMOS Static RAM organized as 8192 words by 8 bits. It is manufactured using an advanced high-performance CMOS process that combines high speed with low-power consumption and increased reliability.

The Am99C88H operates from a single 5-V supply and is fully TTL-compatible. Four inputs, $\overline{E_1}$, E_2, $\overline{W}$, and $\overline{G}$ are used to control the device. Two Chip Enables ($\overline{E_1}$ and E_2) select the device for operation, control the automatic power-down feature, and provide for easy memory expansion. Write Enable ($\overline{W}$) controls write and read operations. Output Enable ($\overline{G}$) controls the three-state output buffers on the eight common data inputs and outputs. Data is retained by the device with V_{CC} as low as 2 V.

The Am99C88H is available in a 28-pin, 600-mil DIP, a 32-pin ceramic leadless chip carrier, and a 32-pin plastic leaded chip carrier.

BLOCK DIAGRAM



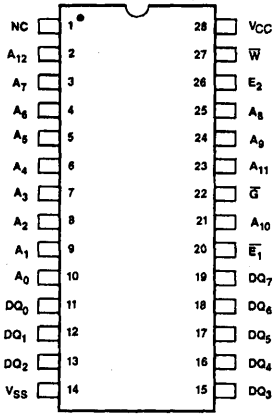
BD006470

Publication # 08118 | Rev. A | Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

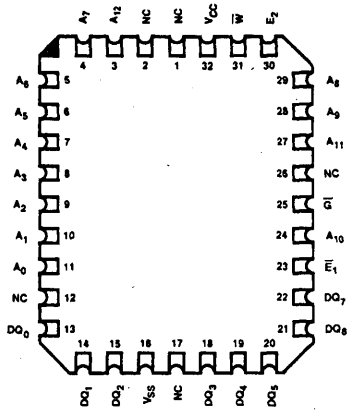
Part Number		Am99C88H			
		-35	-45	-55	-70
Access Time Max. (ns)		35	45	55	70
0 to +70°C	I_{CC} Max. (mA)	110	110	110	110
	I_{SB} Max. (mA)	25	25	25	25
	I_{SBC} Max. (mA)	5	5	5	5
-55 to +125°C	I_{CC} Max. (mA)	—	125	125	125
	I_{SB} Max. (mA)	—	30	30	30
	I_{SBC} Max. (mA)	—	10	10	10

CONNECTION DIAGRAMS
Top View



CD009133

LCC*

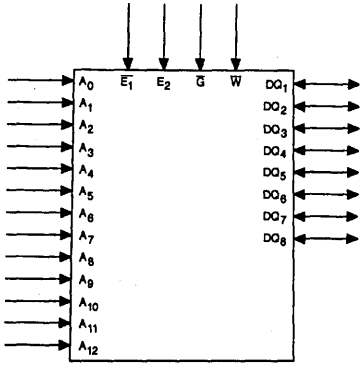


CD009125

*Same pinouts apply for PLCC.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002181

Am99C89

8192 x 9 Static R/W Random-Access Memory

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- High Speed
  - Access time as fast as 45 ns
- Low power consumption
  - 660 mW Maximum (Active)
  - 140 mW Maximum (Standby)
- Output Enable ($\overline{G}$) control to minimize bus contention
- Dual Chip Enable for increased design flexibility
- Automatic power-down when deselected
- Single 5-V ±10% power supply operation
- Fully static — no clocks or timing signals required
- Standard 28-pin, 300-mil DIP

GENERAL DESCRIPTION

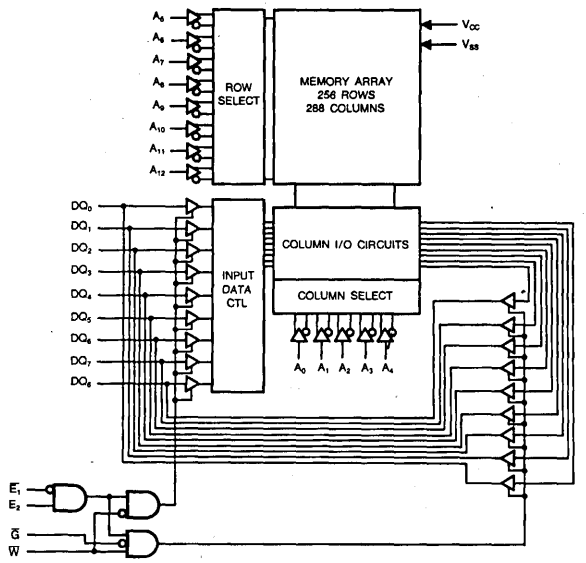
The Am99C89 is a high-performance, 8192 x 9-bit, static, Read/Write, Random-Access Memory. Fabricated with advanced CMOS processing techniques, the Am99C89 combines fast access time with low power consumption and increased reliability.

Features include common input/output pins and four control signals ($\overline{W}$, $\overline{G}$, $\overline{E_1}$, and E_2) to facilitate read/write operations, simplify memory expansion, and minimize any bus contention that may limit device performance. The availability of two Chip Enable pins provides further system design flexibility.

The Am99C89 offers enhanced system reliability in writable control store applications by providing an extra bit for parity checks. This device is ideal for use in high-performance EDP equipment, disk controllers, workstations, and automatic test equipment systems.

The Am99C89 features single 5-V operation with automatic power-down capability. All input/output levels are TTL-compatible.

BLOCK DIAGRAM



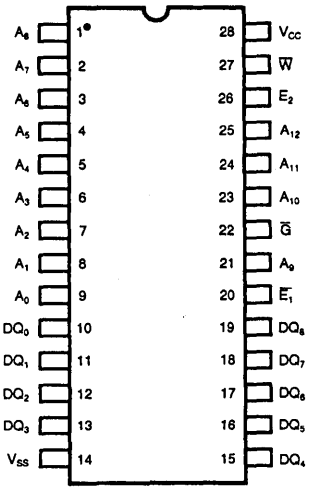
BD006461

Publication # 08110 Rev. A Amendment /0
Issue Date: May 1986

PRODUCT SELECTOR GUIDE

Part Number	Am99C89-45	Am99C89-55	Am99C89-70
Maximum Access Time (ns)	45	55	70
I_{CC} Maximum (mA)	120	120	120
I_{SB} Maximum (mA)	25	25	25

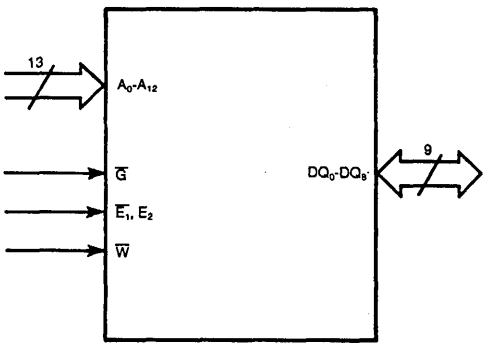
CONNECTION DIAGRAMS
Top View



CD009641

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002471

Pin Names

$A_0 - A_{12}$ = Address Inputs
$DQ_0 - DQ_8$ = Data I/O
$\overline{G}$ = Output Enable
$\overline{E_1}$, E_2 = Chip Enable
$\overline{W}$ = Write Enable
V_{CC} = +5-V Power Supply
V_{SS} = Ground

4

MOS Electrically Erasable Programmable ROM (EEPROM) Index

Am2817A

2048 x 8-Bit Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

- 5-Volt-only operation
- Write-protect circuitry to preserve data on power up and power down
- Ready/$\overline{\text{Busy}}$ pin for end-of-write indication
- Self-timed write cycle with on-chip latches
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the Am9864 Reliability Report (PID #06891A)

GENERAL DESCRIPTION

The Am2817A is a 16,384-bit Electrically Erasable Programmable Read-Only Memory (EEPROM). It is organized as 2048 words by 8 bits per word and offers a fast 200 ns read access time.

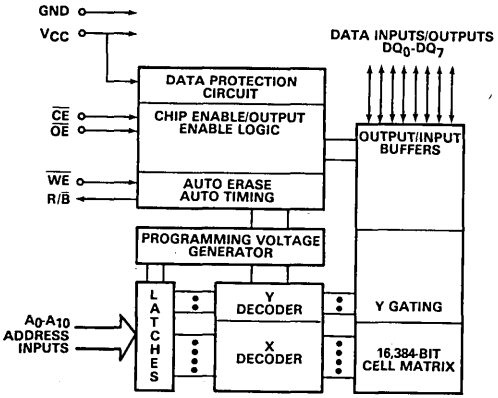
The 2817A has a fully self-timed write cycle with address, data, and control lines latched during the write operation.

The latched inputs and self-timed write cycle free the microprocessor to perform other processes during write. A transparent automatic erase before write enhances system performance.

To eliminate bus contention in a microprocessor system, this device offers separate Output Enable ($\overline{\text{OE}}$) and Chip Enable ($\overline{\text{CE}}$) controls.

The Am2817A is fabricated on AMD's highly manufacturable N-Channel silicon gate process and uses AMD's proprietary EEPROM technology to achieve electrically alterable, non-volatile storage.

BLOCK DIAGRAM



BD003532

MODE SELECT TABLE

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Outputs	R/$\overline{\text{B}}$	Mode
L	L	H	D_{OUT}	Hi-Z	Read
L	H	H	Hi-Z	Hi-Z	Read Inhibit
H	X	X	Hi-Z	Hi-Z	Standby
L	H	⊓	D_{IN}	⊓	Byte Write
Automatic before each "Write"					Byte Erase
X	L	X	–	–	Write Inhibit

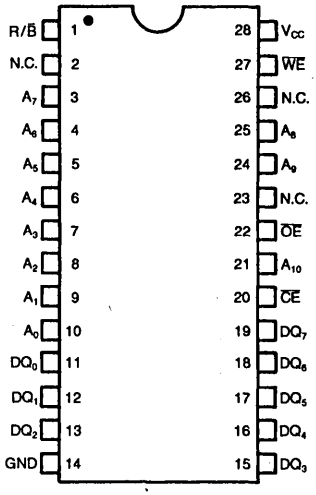
H = HIGH
L = LOW
X = Don't Care
⊓ = Pulse

PRODUCT SELECTOR GUIDE

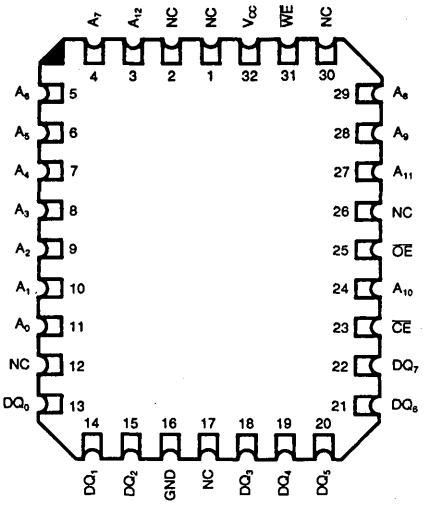
Part Number	Am2817A-2	Am2817A-20	Am2817A	Am2817A-25	Am2817A-3	Am2817A-35
Access Time	200 ns		250 ns		350 ns	
Supply Tolerance	±5%	±10%	±5%	±10%	±5%	±10%

Publication # 06153 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



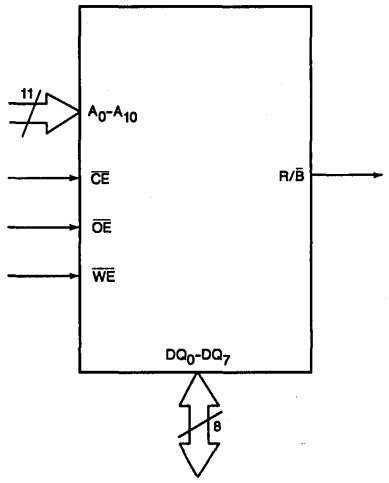
CD005372



CD006001

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



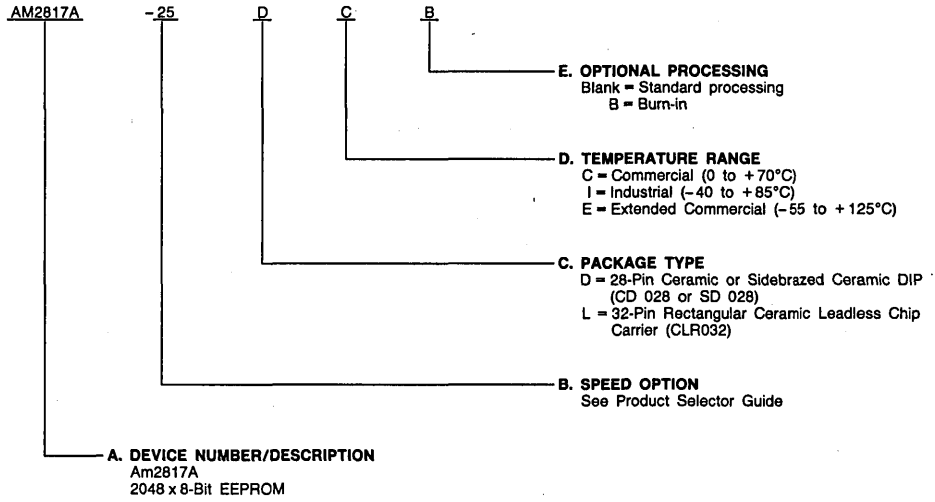
LS002273

V_{CC} = Power Supply
GND = Ground

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2817A-2	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2817A-20	
AM2817A	
AM2817A-25	
AM2817A-3	
AM2817A-35	

Valid Combinations

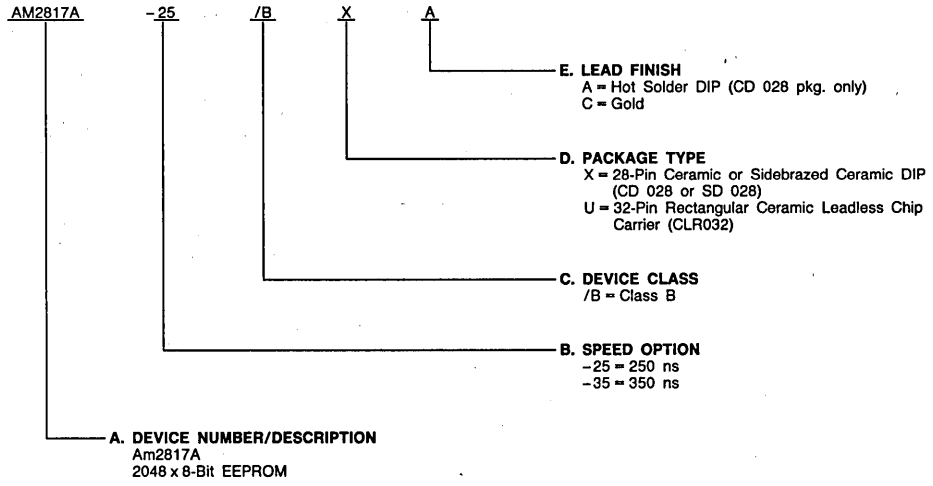
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

5

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2817A-25	/BXA, /BXC, /BUC
AM2817A-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am2817A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am2817A has a standby mode which reduces the active power dissipation by 60% from 500 mW to 200 mW (values for 0 to 70°C). The Am2817A is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am2817A incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.8 volts. It is the user's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.8 volts.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less than 10 ns* duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Write Mode

The Am2817A has a write cycle that is similar to that of a static RAM. The write cycle is completely self timed, and initiated by a LOW-going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ (R/$\overline{B}$) pin goes to a logic-LOW level indicating that the Am2817A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When R/$\overline{B}$ goes back to a HIGH, the Am2817A has completed writing and is ready to accept another cycle.

Output OR-Tieing

To accommodate mulitiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Ready/$\overline{Busy}$ Pin

The Ready/$\overline{Busy}$ (R/$\overline{B}$) pin is an open-drain output which allows two or more R/$\overline{B}$ signals to be OR-tied together. The value of the pullup resistor required is as follows:

$$R_{pu} = \frac{4.6\ V}{2.1\ mA - I_{IL}}$$

I_{IL} = total V_{IL} input current of devices connected to R/$\overline{B}$.

A typical pullup resistor value for R/$\overline{B}$ is 3 kΩ, assuming I_{IL} is less than 0.5 mA.

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

* This parameter is sampled and not 100% tested.

5

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

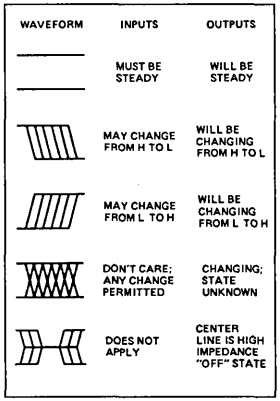
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	μA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ ⊓, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			100	mA
V_{IL}	Input LOW Voltage		−0.1		.8	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 1	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA	2.4			Volts
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts
V_{RB}	R/$\overline{B}$ Output LOW	I_{RB} = 2.1 mA			.45	Volts
C_{IN}	Input Capacitance (Notes 1, 2 & 3)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Notes 1, 2 & 3)	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, V_{OUT} = 0 V		8	12	pF

Notes 1. This parameter is sampled on a periodic basis and not 100% tested.
2. Freq. = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.

KEY TO SWITCHING WAVEFORMS



KS000010

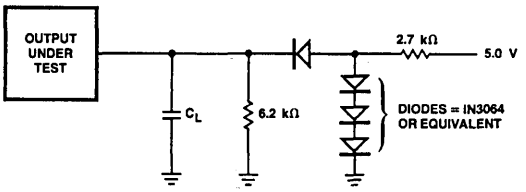
Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurements Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



TC002491

C_L = 100 pF, including jig capacitance.

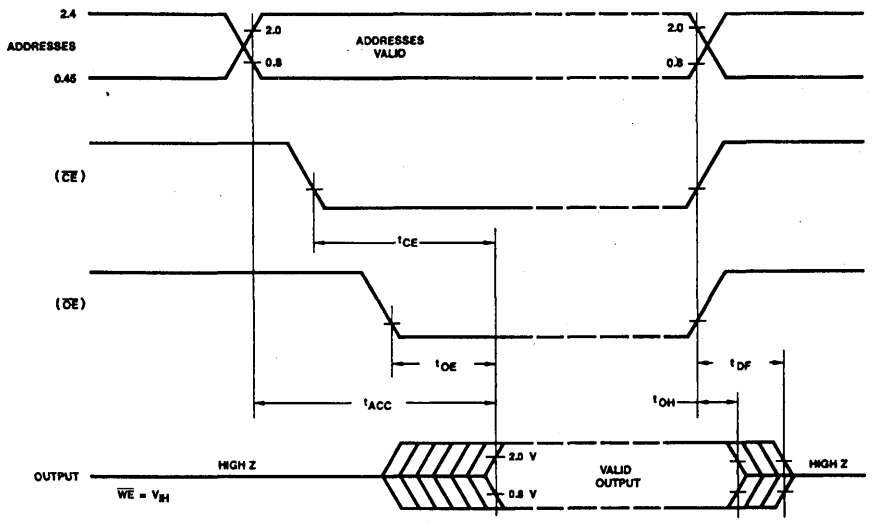
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	Test Conditions		Am2817A-2, Am2817A-20 Min.	Am2817A-2, Am2817A-20 Max.	Am2817A, Am2817A-25 Min.	Am2817A, Am2817A-25 Max.	Am2817A-3, Am2817A-35 Min.	Am2817A-3, Am2817A-35 Max.	Units
READ											
1	t_{ACC} (Note 3)	Address to Output Delay	$\overline{WE}$ = V_{IH} Output Load: 1 TTL gate and C_L = 100 pF Input Rise and Fall Times: ≤ 20 ns Input Pulse Levels: 0.45 to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2 V Outputs: 0.8 V and 2 V	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200		250		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE}$ = V_{IL}		200		250		350	ns
3	t_{OE} (Note 3)	Output Enable to Output Delay		$\overline{CE}$ = V_{IL}		75		100		120	ns
4	t_{DF} (Notes 1 & 4)	Output Enable HIGH to Output Float		$\overline{CE}$ = V_{IL}	0	60	0	60	0	80	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First		$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		ns
WRITE											
6	t_{AS}	Address to Write Setup Time			20		20		20		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time			30		30		30		ns
8	t_{WP}	Write Pulse Width			100		100		100		ns
9	t_{AH}	Address Hold Time			50		50		50		ns
10	t_{DS}	Data Setup Time			50		50		50		ns
11	t_{DH}	Data Hold Time			20		20		20		ns
12	t_{CH}	$\overline{CE}$ Hold Time			0		0		0		ns
13	t_{OES}	$\overline{OE}$ Setup Time			20		20		20		ns
14	t_{OEH}	$\overline{OE}$ Hold Time			35		35		35		ns
15	t_{DB}	Time to Device Busy				100		100		100	ns
16	t_{WR}	Bytes Write Cycle				10		10		10	ms
17	t_{WPH}	Write Control Recovery			50		50		50		ns
18	t_{RE}	Write Recovery Time (Note 6)			0		0		0		ns
19	t_{RBO}	R/$\overline{B}$ to Output Time (Notes 2 & 6)				50		50		50	ns
20	t_{WEH} (Note 6)	$\overline{WE}$ HIGH Recovery from R/$\overline{B}$			10		10		10		μs
	(Notes 1 & 5)	Number of Writes per Byte			10		10		10		x1000

Notes: 1. This parameter is sampled on a periodic basis to worst-case test conditions and not 100% tested.
2. If $\overline{CE}$ and $\overline{OE}$ = V_{IL} when R/$\overline{B}$ is going to V_{OH}, then DQ_{0-7} becomes valid after $t_{RBO} + t_{ACC}$ ns.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, which ever occurs first.
5. See Am9864 Reliability Report (PID #06891A).
6. This parameter is for information only. It is not tested nor characterized.

5

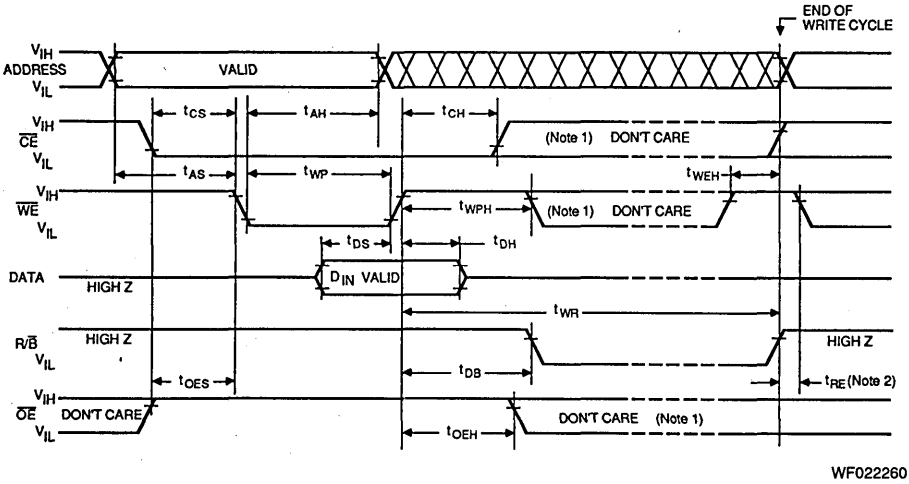
SWITCHING WAVEFORMS



WF001292

Read

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.



WF022260

Write

Notes: 1. After t_{WPH} and before the end of the Write cycle (R/$\overline{B}$ goes HIGH), $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ are Don't Cares. However, in order to prevent an accidental write when R/$\overline{B}$ returns HIGH, it is recommended that at least one of the following conditions after t_{WPH}: $\overline{WE}$ HIGH, $\overline{CE}$ HIGH, or $\overline{OE}$ LOW.
2. After the Write cycle is completed (R/$\overline{B}$ HIGH), the user must meet one of the following conditions: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{IL}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
V_{WI}	7, 8
V_{RB}	1, 2, 3
C_{IN}	4
C_{OUT}	4

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	9	t_{AH}	9, 10, 11
2	t_{CE}	9, 10, 11	10	t_{DS}	9, 10, 11
3	t_{OE}	9, 10, 11	11	t_{DH}	9, 10, 11
4	t_{DF}	9, 10, 11	12	t_{CH}	9, 10, 11
5	t_{OH}	9, 10, 11	13	t_{OES}	9, 10, 11
6	t_{AS}	9, 10, 11	14	t_{OEH}	9, 10, 11
7	t_{CS}	9, 10, 11	15	t_{DB}	9, 10, 11
8	t_{WP}	9, 10, 11	16	t_{WR}	9, 10, 11
			17	t_{WPH}	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am9864

8192 x 8-Bit Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

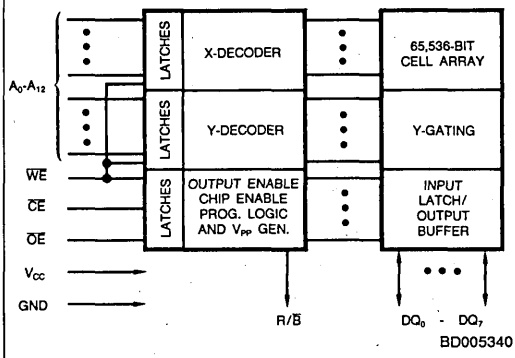
- 5 V only operation
- Self Timed Write Cycle with on chip latches
- Ready/$\overline{\text{Busy}}$ Pin for end of write indication
- Data Protection Features to prevent writes from occurring during V_{CC} power up/down
- Fast Read Access Time
  - Am9864-2/-20 : 200 ns
  - Am9864 /-25 : 250 ns
  - Am9864-30 : 300 ns
  - Am9864-3/-35 : 350 ns
- Minimum endurance of 10,000 write cycles per byte with a 10 year data retention (See 9864 Reliability Report Order #06891A for detailed information).

GENERAL DESCRIPTION

The Am9864 is a 65,536 bit Electrically Erasable Programmable Read Only Memory (EEPROM), organized as 8192 words by 8 bits per word. It operates from a single 5 volt supply and has a fully self timed write cycle with address, data and control lines latched during the write operation. The Am9864 is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve the Electrically Alterable Nonvolatile Storage. This technology employs the industry accepted Fowler-Nordheim tunneling across a thin oxide.

The Am9864 provides on chip the logic necessary to interface with most microprocessors. The latched inputs and self timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

BLOCK DIAGRAM



MODE SELECTION

Inputs			Outputs		Mode
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	R/$\overline{B}$	I/O	
L	L	H	H	Data Out	Read
L	H	⊓	⊓	Data In	Write
H	X	X	H	Hi Z	Standby
L	H	H	H	Hi Z	Read Inhibit
X	L	X	–	–	Write Inhibit

H = High
L = Low
X = Don't Care
⊓ = Pulse

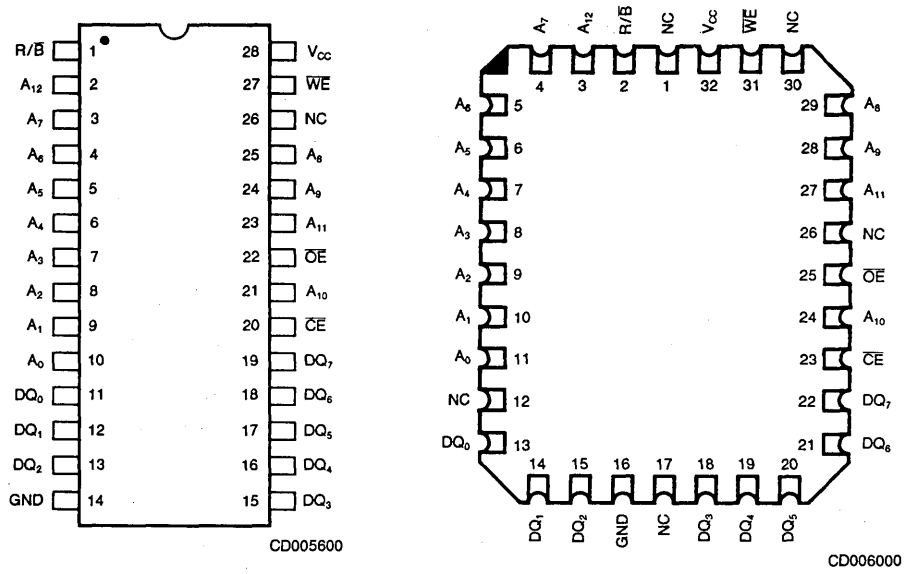
PRODUCT SELECTOR GUIDE

Part Number	Am9864-2	Am9864-20	Am9864	Am9864-25	Am9864-30	Am9864-3	Am9864-35
V_{CC} Supply tolerance	±5%	±10%	±5%	±10%	±10%	±5%	±10%
Access Time	200 ns		250 ns		300 ns	350 ns	
Chip Select Delay	200 ns		250 ns		300 ns	350 ns	
Output Enable Delay	75 ns		100 ns		120 ns	120 ns	

Publication # 05003 Rev. D Amendment /0
Issue Date: May 1986

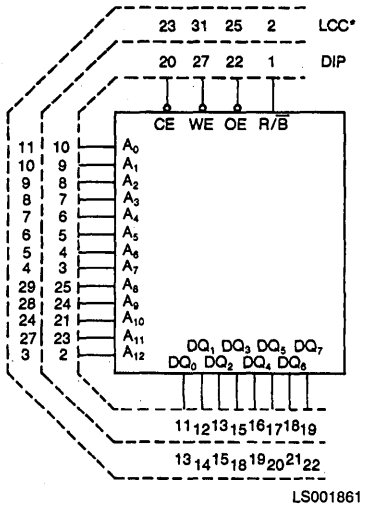
CONNECTION DIAGRAMS
Top View

LCC*



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



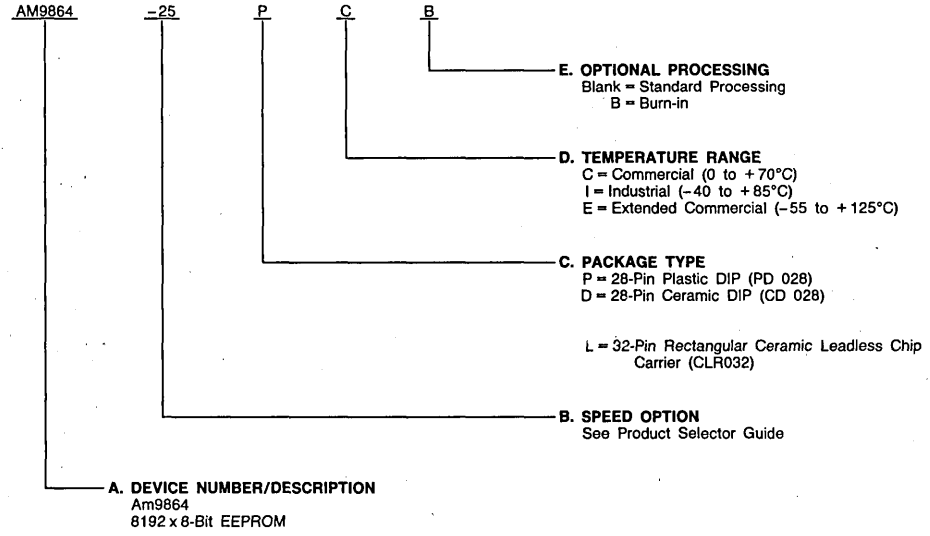
*Same pinouts apply to PLCC.

5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9864-2	PC, PCB, DC, DCB, DI, DIB, LI, LIB
AM9864-20	
AM9864	
AM9864-3	
AM9864-25	PC, PCB, DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM9864-35	

Valid Combinations

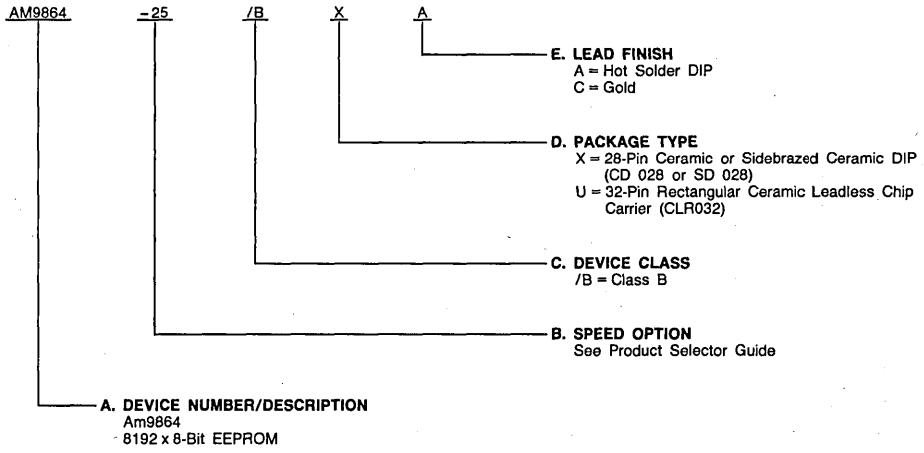
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*To be announced.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9864-25	/BXA, /BXC, /BUC
AM9864-30	
AM9864-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

5

FUNCTIONAL DESCRIPTION

Read Mode

The Am9864 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The Am9864 has a standby mode which reduces the active power dissipation by 60%, from 525 mW to 210 mW (V_{CC} ±5% values for 0 to 70°C). The Am9864 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am9864 incorporates several features that prevent unwanted write cycles during V_{CC} power up and power down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for V_{CC} less than 3.3 volts (typical 3.8 V). It is the users's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.3 volts.

There is a $\overline{WE}$ lockout circuit that prevents WE pulses of less than 10 ns duration from initiating a write cycle.*

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Write Mode

The Am9864 has a write cycle that is similar to that of a Static RAM. The write cycle is completely self timed, and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the Am9864 is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high the Am9864 has completed writing, and is ready to accept another cycle.

Output OR-Tieing

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OEW}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Ready/$\overline{Busy}$ Pin

The Ready/$\overline{Busy}$ is a totem-pole output. It can be tied to a system interrupt to allow a writing operation to be defined by one microprocessor cycle time. The state of this output is determined by the Am9864 and must not be externally forced. When not used this pin must be kept floating. This output cannot be or-tied.

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Endurance

Since endurance testing is a destructive test it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point, when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant mortality failures to be screened out. For the next 10,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above 12,000 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write 10,000 times. Those devices that fail will have one single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained please refer to the Am9864 reliability report.

*This parameter is sampled and is not 100% tested.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.25 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Supply Voltage* (V_{CC} ±5%) ..... +4.75 to +5.25 V
Supply Voltage** (V_{CC} ±10%) ..... +4.5 to +5.5 V
*9864-2, 9864, 9864-3
**9864-20, 9864-25, 9864-35

Commercial (C) Device
Case Temperature ..... 0 to +70°C
Industrial (I) Device
Case Temperature ..... −40 to +85°C
Limited (L) Device
Case Temperature ..... −55 to +100°C
Extended Commercial (E) Device
Case Temperature ..... −55 to +125°C
Military (M) Device
Case Temperature ..... −55 to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

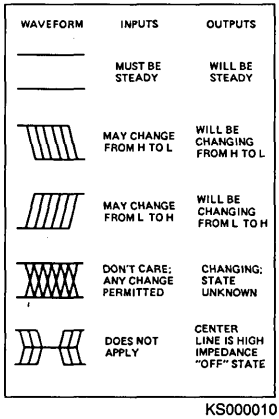
DC CHARACTERISTICS over operating range unless otherwise specified *

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	µA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ = ⊓⊔, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			120	mA
V_{IL}	Input Low Voltage		−0.1		.8	Volts
V_{IH}	Input High Voltage		2.0		V_{CC}+1	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4			Volts
C_{IN}	Input Capacitance (Notes 1, 2)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Notes 1, 2)	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, V_{OUT} = 0V		8	12	pF
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts
V_{RB}	R/$\overline{B}$ Output Low	I_{RB} = 2.1 mA			.45	Volts

Note 1. This parameter is sampled on a periodic basis and not 100% tested.
2. freq = 1 MHz @ 25°C.
3.Typical values are for nominal supply voltages.

*See the last page of this spec for Group A Subgroup Testing Information.

KEY TO SWITCHING WAVEFORMS



KS000010

5

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Test Conditions		Am9864-2, -20 Min.	Am9864-2, -20 Max.	Am9864, -25 Min.	Am9864, -25 Max.	Am9864-30 Min.	Am9864-30 Max.	Am9864-3, -35 Min.	Am9864-3, -35 Max.	Units
READ													
1	t_{ACC}	Address to Output Delay	$\overline{WE} = V_{IH}$ Output Load: 1 TTL gate and $C_L = 100$ pF Input Rise and Fall Times: ≤20 ns Input Pulse Levels: 0.45 to 2.4 V Timing Measurement Reference Level Inputs: 0.8 V and 2 V Outputs: 0.8 V and 2 V	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE} = V_{IL}$		200		250		300		350	ns
3	t_{OE}	Output Enable to Output Delay		$\overline{CE} = V_{IL}$		75		100		120		120	ns
4	t_{DF} (Note 1)	Output Enable High to Output Float		$\overline{CE} = V_{IL}$	0	60	0	60	0	80	0	80	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First		$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns
WRITE													
6	t_{AS}	Address to Write Setup Time			20		20		20		60		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time			20		20		20		20		ns
8	t_{WP}	Write Pulse Width			100		100		100		150		ns
9	t_{AH}	Address Hold Time			80		80		80		100		ns
10	t_{DS}	Data Setup Time			50		50		50		70		ns
11	t_{DH}	Data Hold Time			20		20		20		20		ns
12	t_{CH}	$\overline{CE}$ Hold Time			50		50		50		50		ns
13	t_{OES}	$\overline{OE}$ Setup Time			20		20		20		20		ns
14	t_{OEH}	$\overline{OE}$ Hold Time			35		35		35		35		ns
15	t_{DB}	Time to Device Busy				100		100		100		100	ns
16	t_{WR}	Bytes Write Cycle				10		10		10		20	ms
17	t_{WPH}	Write Control Recovery			50		50		50		50		ns
18	t_{RE} (Note 4)	Write Recovery Time			0		0		0		0		ns
19	t_{RBO} (Notes 2, 4)	R/$\overline{B}$ to Output Time				50		50		50		50	ns
20	t_{WEH} (Note 4)	$\overline{WE}$ HIGH Recovery from R/$\overline{B}$			10		10		10		10		μs
	(Notes 1, 3)	Number of Writes per Byte			10		10		10		10		x1000

Notes: 1. This parameter is sampled on a periodic basis and is not 100% tested.
2. If $\overline{CE}$ and $\overline{OE} = V_{IL}$ when R/$\overline{B}$ is going to V_{OH}, then $DQ_0 - DQ_7$ becomes valid after $t_{RBO} + t_{ACC}$.
3. See 9864 reliability report.
4. This parameter is for information only. It is not tested or characterized.

*See the last page of this spec for Group A Subgroup Testing Information.

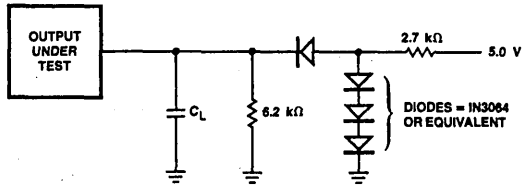
SWITCHING TEST CONDITIONS

Output load: 1 TTL gate and $C_L = 100$ pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT

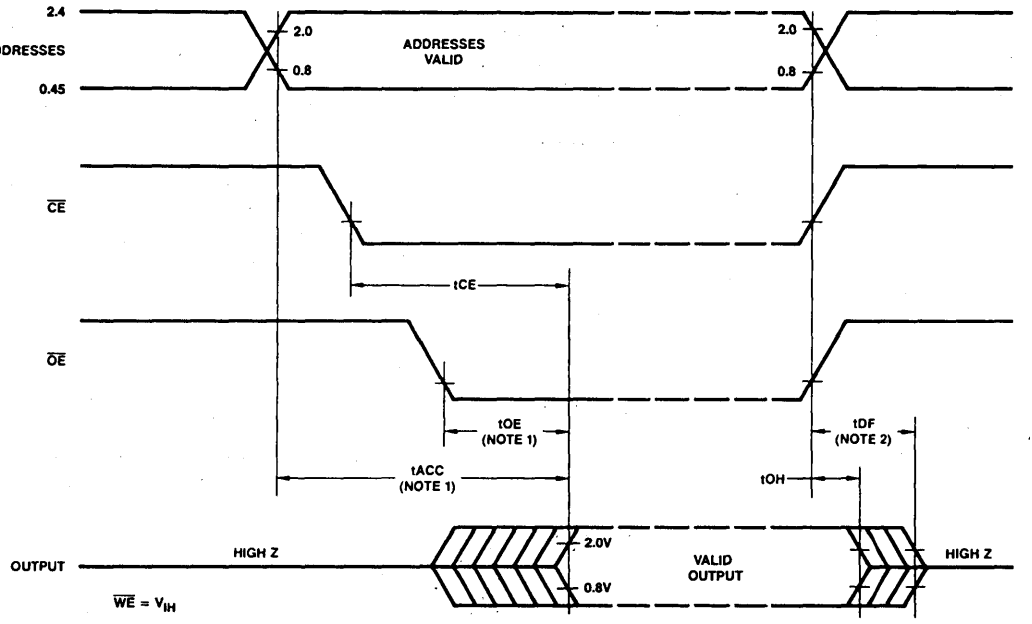


TC002491

$C_L = 100$pF, including jig capacitance.

SWITCHING WAVEFORMS

READ

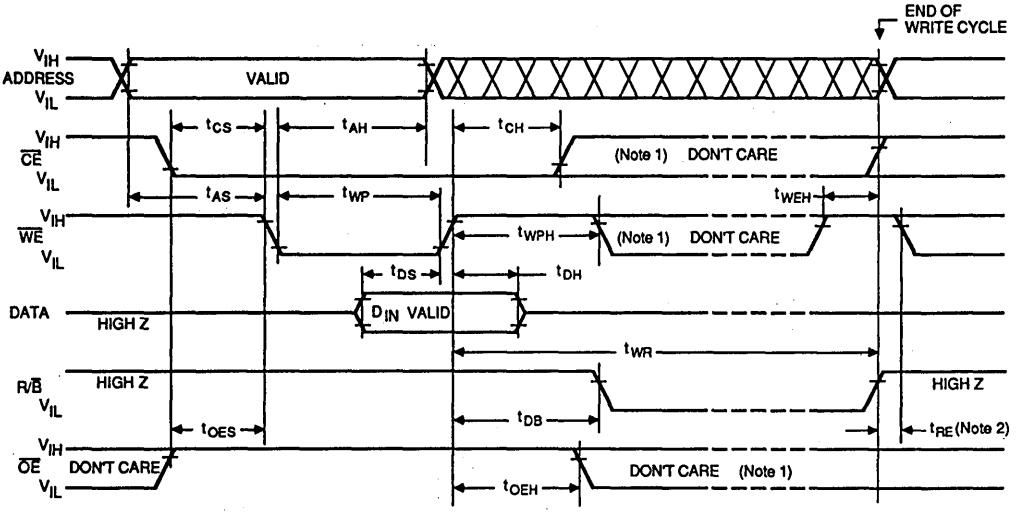


WF010280

Notes: 1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

5

WRITE



WF022260

Notes: 1. After t_{wph} and before the end of write cycle (R/$\overline{B}$ goes high), $\overline{WE}$, $\overline{CE}$ and $\overline{OE}$ are don't cares. However, in order to prevent an accidental write when R/$\overline{B}$ returns high, it is recommended that at least one of the following conditions are met after t_{wph}: $\overline{WE}$ high, $\overline{CE}$ high or an $\overline{OE}$ low.

2. After the write cycle is completed (R/$\overline{B}$ is high) the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
C_{IN}	4
C_{OUT}	4
V_{WI}	7, 8
V_{RB}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	9	t_{AH}	9, 10, 11
2	t_{CE}	9, 10, 11	10	t_{DS}	9, 10, 11
3	t_{OE}	9, 10, 11	11	t_{DH}	9, 10, 11
4	t_{DF}	9, 10, 11	12	t_{CH}	9, 10, 11
5	t_{OH}	9, 10, 11	13	t_{OES}	9, 10, 11
6	t_{AS}	9, 10, 11	14	t_{OEH}	9, 10, 11
7	t_{CS}	9, 10, 11	15	t_{DB}	9, 10, 11
8	t_{WP}	9, 10, 11	16	t_{WR}	9, 10, 11
			17	t_{wph}	9, 10, 11

5

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am2864A

8192 x 8 Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

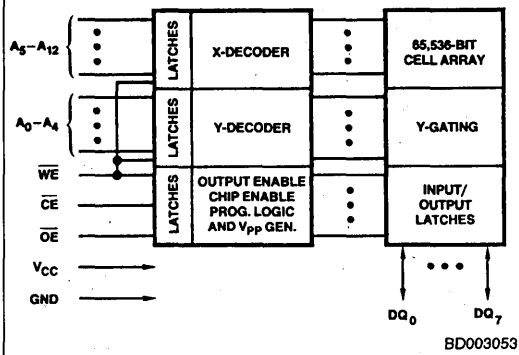
- 5-V only operation
- Military temperature range available
- Self-timed Write Cycle with on-chip latches
- $\overline{\text{Data}}$ Polling for end-of-write indication
- Data protection features to prevent writes from occurring during V_{CC} power-up/down
- 32-byte page write mode
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the Am9864 Reliability Report (PID #06891A).

GENERAL DESCRIPTION

The Am2864A is a 65,536-bit Electrically Erasable Programmable Read-Only Memory (EEPROM), organized as 8192 words by 8 bits per word. It operates from a single 5-volt supply and has a fully self timed write cycle with address, data and control lines latched during the write operation. The 32-byte page write mode allows programming in as little as 2.8 seconds. The Am2864A is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve the electrically alterable nonvolatile storage. This technology employs the industry-accepted accepted Fowler-Nordheim tunneling across a thin oxide.

The Am2864A provides on-chip the logic necessary to interface with most microprocessors. The latched inputs and self-timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

BLOCK DIAGRAM



MODE SELECT TABLE

Inputs			Outputs		
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	A_9	Mode
L	L	H	Data Out	X	Read
L	H	⊓	Data In	X	Write
H	X	X	Hi-Z	X	Standby
L	H	H	Hi-Z	X	Read Inhibit
X	L	X	–	X	Write Inhibit
L	L	H	Code	V_H	Auto Select
L	L	H	$\overline{D_{IN}}$	X	$\overline{\text{Data}}$ Polling

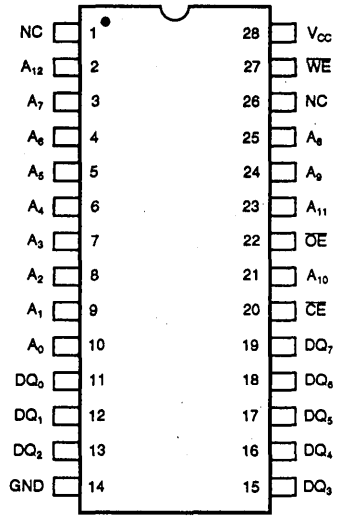
V_H = 12.0 V ± .5 V
H = HIGH
L = LOW
X = Don't Care
⊓ = Pulse

PRODUCT SELECTOR GUIDE

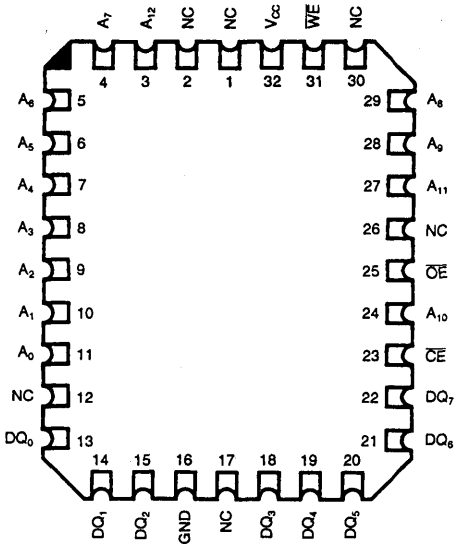
Part Number	Am2864A-2	Am2864A-20	Am2864A	Am2864A-25	Am2864A-3	Am2864A-30	Am2864A-355	Am2864A-35
Maximum Access Time	200 ns		250 ns		300 ns		350 ns	
V_{CC} Supply Tolerance	±5%	±10%	±5%	±10%	±5%	±10%	±5%	±10%

Publication # 08085 | Rev. A | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



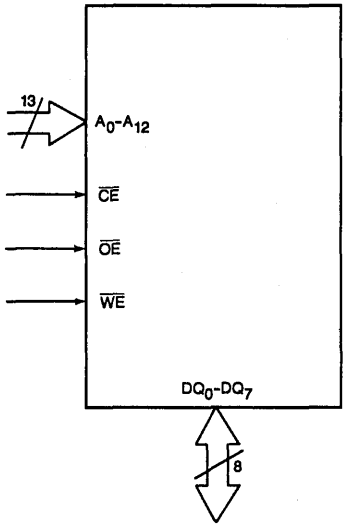
CD005601



CD006001

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002272

VCC = Power Supply
GND = Ground

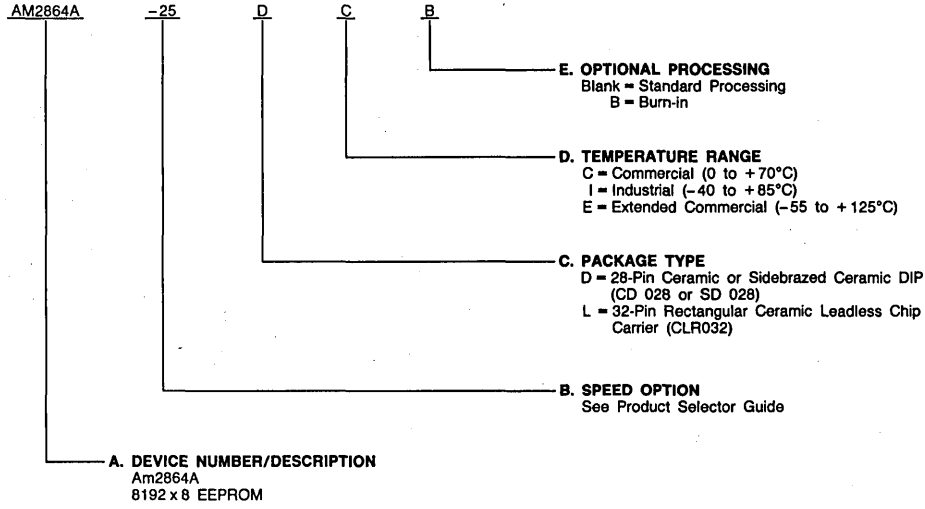
5

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2864A-2	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2864A-20	
AM2864A	
AM2864A-25	
AM2864A-3	
AM2864A-30	
AM2864A-355	
AM2864A-35	

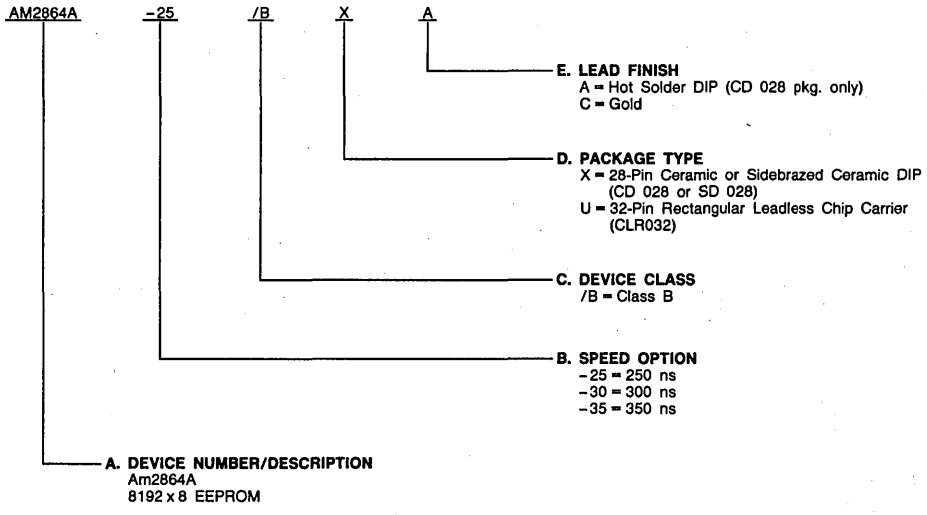
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2864A-25	/BXA, /BXC, /BUC
AM2864A-30	
AM2864A-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

5

FUNCTIONAL DESCRIPTION

Read Mode

The Am2864A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The Am2864A has a standby mode which reduces the active power dissipation by 60%, from 525 mW to 210 mW (V_{CC} ±5% values for 0 to 70°C). The Am2864A is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am2864A incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.3 volts (typical 3.8 V). It is the users's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.3 volts.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less than 20 ns duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Page Write Mode

The page write allows from 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. The page write mode consists of a load sequence followed by an automatic write sequence.

During the load portion, sequential $\overline{WE}$ pulses load the byte address and the byte data into a 32-byte register. The bytes can be loaded into this register in any order. On each $\overline{WE}$ pulse, the "Y" address is latched on the falling edge of the $\overline{WE}$, the data input is latched on the rising edge of $\overline{WE}$, and the page address (A_5-A_{12}) is latched on the falling edge of the last $\overline{WE}$. Note that for a write to occur, $\overline{CE}$ and $\overline{WE}$ must be LOW and $\overline{OE}$ must be HIGH. The load portion of the page write is complete when all the data (up to 32 bytes) is loaded into the register.

The automatic write portion starts t_{WW} after each transition of $\overline{WE}$ from LOW-to-HIGH. If $\overline{WE}$ transitions from HIGH-to-LOW before t_{WW} minimum (100 µs), the timer is reset and the automatic write portion does not start. This is how the bytes are loaded into the register. If $\overline{WE}$ is held LOW, this t_{WW} timer never starts and the write cycle is held indefinitely.

If $\overline{WE}$ transitions from LOW-to-HIGH and stays HIGH for at least t_{WW} maximum, then the automatic write sequence is initiated. Note that the load sequence can also be terminated if $\overline{OE}$ goes LOW. Once $\overline{OE}$ is LOW, further attempts to load will be ignored and the part will time out (t_{WW}) and enter the automatic write sequence.

The automatic write sequence consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which puts data back into the erased cells. Note that a page write will only write data to the locations being addressed and will not rewrite the entire page.

Byte Mode Write

When $\overline{WE}$ is toggled once, the Am2864A operates in the byte mode. A single byte is loaded into the register and after $\overline{WE}$ goes HIGH and t_{WW} is satisfied, the automatic write cycle starts. It is in this mode that the Am2864A is identical to the Am2864B and Am9864.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C ±5°C ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line A_9 of the Am2864A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am2864A, these two identifier bytes are given in Table 1. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit. The auto select code for the Am2864A is identical to the Am2864B.

Output OR-Tieing

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

$\overline{\text{Data}}$ Polling

This feature makes the Am2864A highly flexible. It allows the designer the option of a software polling technique for end of write indication. $\overline{\text{Data}}$ Polling requires a simple software routine that performs a read operation when the chip is in the automatic write mode. The data that becomes valid during this $\overline{\text{Data}}$ Polling read is the inverse of all 8 bits, last written to the outputs. The true data ($DQ_0 - DQ_7$) will become valid when the automatic write has been completed. Note that all 8 bits invert during $\overline{\text{Data}}$ Polling, thereby giving the user more flexibility during design and layout.

Chip Clear Mode (Military only)

Another feature included on AMD's Am2864A for military applications is a single-pulse chip erase. This optional mode allows the user to program all bits to a logic ONE with a single 10-ms write pulse. Additional information is available from AMD regarding this test mode — consult the local AMD sales office.

Endurance

Since endurance testing is a destructive test it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point, when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant-mortality failures to be screened out. For the next 20,000 to 30,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of 10^4 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained please refer to the Am9864 Reliability Report (PID#06891A).

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

PROGRAMMING

TABLE 1. IDENTIFIER BYTES (Notes 1, 2 & 3)

Identifier	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Device Code	V_{IH}	1	0	0	0	1	0	1	0	8A

Legend: 1 = HIGH
0 = LOW

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. $A_1 - A_8$, $A_{10} - A_{12}$, $\overline{CE}$, $\overline{OE} = V_{IL}$
3. $\overline{WE} = V_{IH}$

5

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.50 to −0.6 V
Voltage on A_9 with Respect to GND ..... +13.5 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

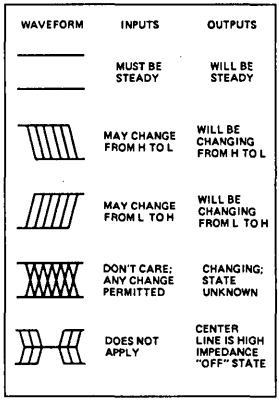
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	µA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ = ⌐⌐, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			100	mA
V_{IL}	Input LOW Voltage		−0.1		.8	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC}+1	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA	2.4			Volts
C_{IN}	Input Capacitance (Note 1, 2)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Note 1, 2)	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, V_{OUT} = 0 V		8	12	pF
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts

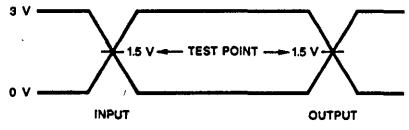
Notes: 1. This parameter is sampled on a periodic basis and not 100% tested.
2. Freq. = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.
*See the last page of this spec for Group A Subgroup Testing information.

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING TEST WAVEFORM



WF009501

AC Testing: Input are driven at 3 V for logic "1" and 0 V for logic "0." Timing measurements are made at 1.5 V . Input pulse rise and fall times are 10 ns.

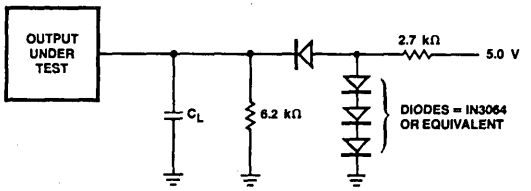
SWITCHING TEST CIRCUIT

Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0 V to 3.0 V

Timing Measurement Reference Levels

Input: 1.5 V
Output: 1.5 V



TC002491

C_L = 100 pF, including jig capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

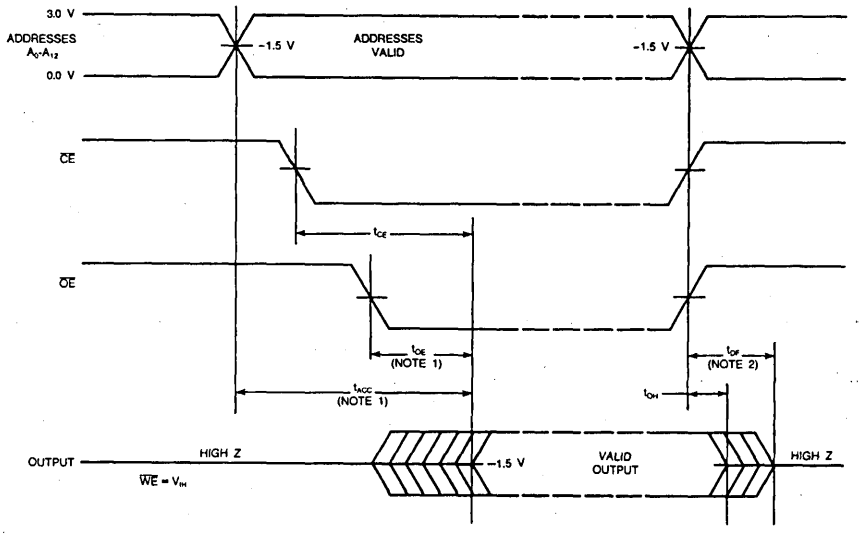
No.	Parameter Symbol	Parameter Description	Test Conditions	Am2864A-2, Am2864A-20		Am2864A, Am2864A-25		Am2864A-3, Am2864A-30		Am2864A-355, Am2864A-35		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ												
1	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200		250		300		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		200		250		300		350	ns
3	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}		100		100		110		120	ns
4	t_{DF} (Note 1)	Output Enable HIGH to Output Float	$\overline{CE}$ = V_{IL}	0	60	0	60		80	0	80	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		0		ns
WRITE												
6	t_{AS}	Address to Write Setup Time		20		20		20		60		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time		0		0		0		0		ns
8	t_{WP}	Write Pulse Width		100		100		120		150		ns
9	t_{AH}	Address Hold Time		80		80		80		100		ns
10	t_{DS}	Data Setup Time		50		50		50		70		ns
11	t_{DH}	Data Hold Time		30		30		30		30		ns
12	t_{CH}	$\overline{CE}$ Hold Time		0		0		0		0		ns
13	t_{OES}	$\overline{OE}$ Setup Time		0		0		0		0		ns
14	t_{OEH}	$\overline{OE}$ Hold Time		0		0		0		0		ns
15	t_{WC}	$\overline{WE}$ Cycle Time		1		1		1		1		μs
16	t_{WW}	Page Write Window (Note 3)		100	500	100	500	100	500	100	1000	μs
17	t_{WH}	$\overline{WE}$ Hold Time		250		250		250		300		ns
18	t_{WB}	Byte Write Cycle			10		10		10		12	ms
19	t_{RED}	Write Recovery from $\overline{Data}$ Polling Time		20		20		20		20		μs
	(Notes 1 & 2)	Number of Writes per Byte		10		10		10		10		x1000

Notes: 1. This parameter is sampled and is not 100% tested.
2. See Am9864 Reliability Report.
3. A timer of t_{WW} duration starts at every LOW-to-HIGH transition of $\overline{WE}$. If it is allowed to time out, a page load will start. A transition of $\overline{WE}$ from HIGH-to-LOW will stop the timer.

*See the last page of this spec for Group A Subgroup Testing information.

5

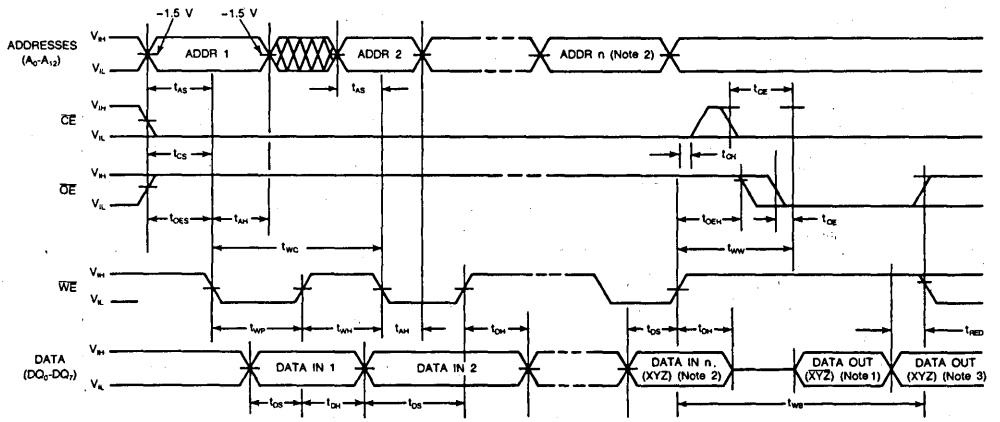
SWITCHING WAVEFORMS (Cont'd.)



WF010287

Read

Notes: 1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

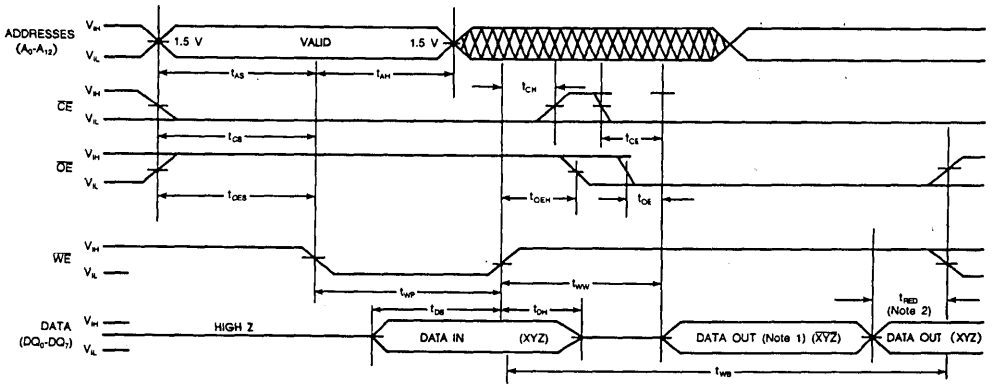


WF020037

Page Write With $\overline{Data}$ Polling

Notes: 1. This is where $\overline{Data}$ Polling is available (if a write operation is performed).
2. $n \leqslant 32$.
3. After the write cycle is completed (Data Out True), the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

SWITCHING WAVEFORMS



WF020046

Byte Write With $\overline{\text{Data}}$ Polling

Notes: 1. This is where $\overline{\text{Data}}$ Polling is available (if a read operation is performed).
2. After the write cycle is completed (Data Out True), the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

5

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
C_{IN}	4
C_{OUT}	4
V_{WI}	7, 8

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	11	t_{DH}	9, 10, 11
2	t_{CE}	9, 10, 11	12	t_{CH}	9, 10, 11
3	t_{OE}	9, 10, 11	13	t_{OES}	9, 10, 11
4	t_{DF}	9, 10, 11	14	t_{OEH}	9, 10, 11
5	t_{OH}	9, 10, 11	15	t_{WC}	9, 10, 11
6	t_{AS}	9, 10, 11	16	t_{WW}	9, 10, 11
7	t_{CS}	9, 10, 11	17	t_{WH}	9, 10, 11
8	t_{WP}	9, 10, 11	18	t_{WB}	9, 10, 11
9	t_{AH}	9, 10, 11	19	t_{RED}	9, 10, 11
10	t_{DS}	9, 10, 11			

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am2864B

8192 x 8 Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

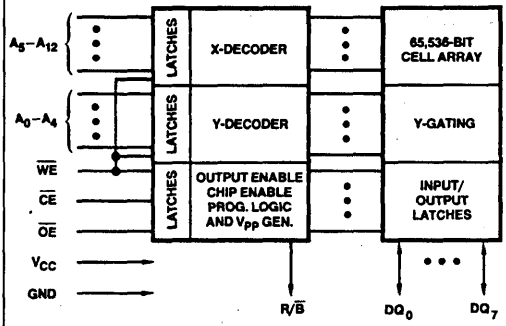
- 5-V only operation
- Military temperature range available
- Self-timed Write Cycle with on-chip latches
- Ready/$\overline{\text{Busy}}$ pin and $\overline{\text{Data}}$ Polling for end-of-write indication
- Data protection features to prevent writes from occurring during V_{CC} power-up/down
- 32-byte page write mode
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the Am9864 Reliability Report (PID #06891A).

GENERAL DESCRIPTION

The Am2864B is a 65,536-bit Electrically Erasable Programmable Read-Only Memory (EEPROM), organized as 8192 words by 8 bits per word. It operates from a single 5-volt supply and has a fully self timed write cycle with address, data and control lines latched during the write operation. The 32-byte page write mode allows programming in as little as 2.8 seconds. The Am2864B is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve the electrically alterable nonvolatile storage. This technology employs the industry-accepted accepted Fowler-Nordheim tunneling across a thin oxide.

The Am2864B provides on-chip the logic necessary to interface with most microprocessors. The latched inputs and self-timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

BLOCK DIAGRAM



MODE SELECT TABLE

Inputs			Outputs			
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	R/$\overline{B}$	I/O	A_9	Mode
L	L	H	Hi Z	Data Out	X	Read
L	H	⊓	⊓	Data In	X	Write
H	X	X	Hi Z	Hi Z	X	Standby
L	H	H	Hi Z	Hi Z	X	Read Inhibit
X	L	X	–	–	X	Write Inhibit
L	L	H	Hi Z	Code	V_H	Auto Select
L	L	H	L	$\overline{D_{in}}$	X	$\overline{Data}$ Polling

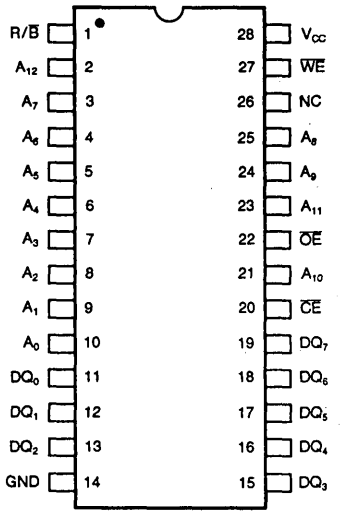
V_H = 12.0 V ± .5 V
H = HIGH
L = LOW
X = Don't Care
⊓ = Pulse

PRODUCT SELECTOR GUIDE

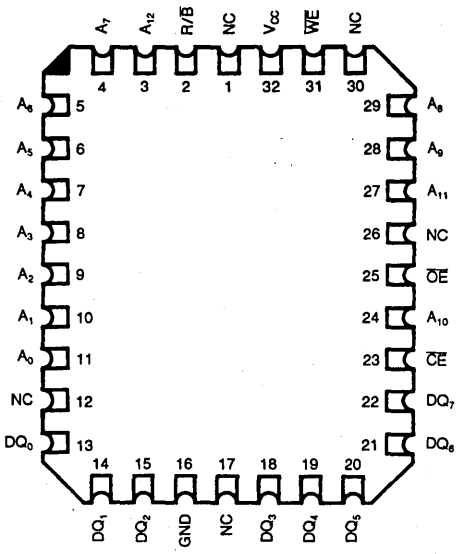
Part Number	Am2864B-2	Am2864B-20	Am2864B	Am2864B-25	Am2864B-3	Am2864B-30	Am2864B355	Am2864B-35
Maximum Access Time	200 ns		250 ns		300 ns		350 ns	
V_{CC} Supply Tolerance	±5%	±10%	±5%	±10%	±5%	±10%	±5%	±10%

Publication # 05571 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



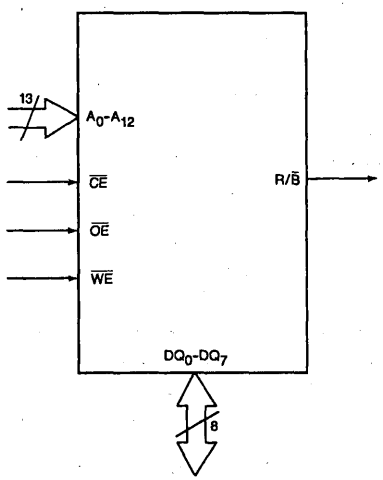
CD005600



CD006000

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002271

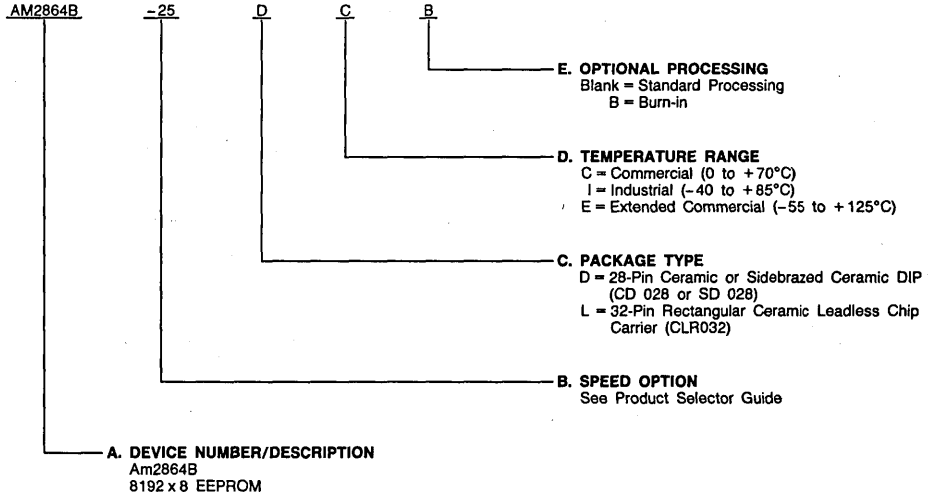
VCC = Power Supply
GND = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2864B-2	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2864B-20	
AM2864B	
AM2864B-25	
AM2864B-3	
AM2864B-30	
AM2864B-355	
AM2864B-35	

Valid Combinations

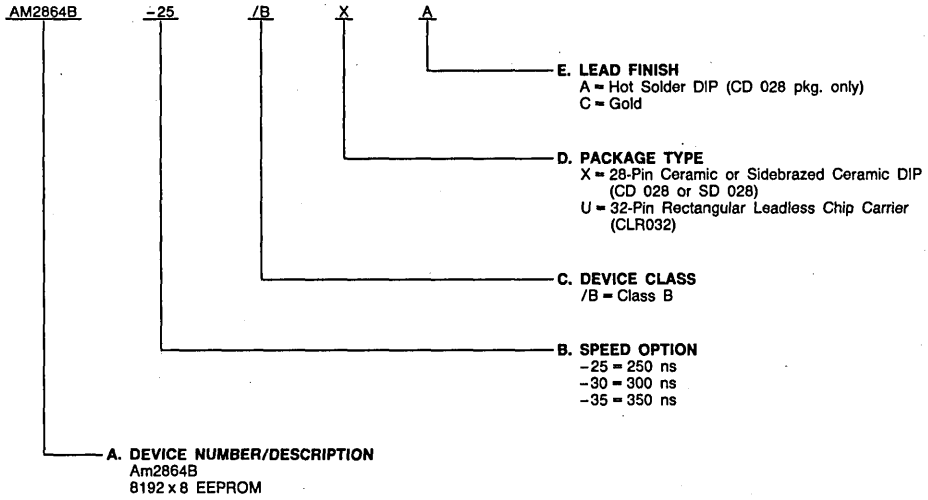
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

5

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2864B-25	/BXA, /BXC, /BUC
AM2864B-30	
AM2864B-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am2864B has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The Am2864B has a standby mode which reduces the active power dissipation by 60%, from 525 mW to 210 mW (V_{CC} ±5% values for 0 to 70°C). The Am2864B is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am2864B incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.3 volts (typical 3.8 V). It is the users's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.3 volts.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less than 20 ns duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Page Write Mode

The page write allows from 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. The page write mode consists of a load sequence followed by an automatic write sequence.

During the load portion, sequential $\overline{WE}$ pulses load the byte address and the byte data into a 32-byte register. The bytes can be loaded into this register in any order. On each $\overline{WE}$ pulse, the "Y" address is latched on the falling edge of the $\overline{WE}$, the data input is latched on the rising edge of $\overline{WE}$, and the page address (A_5-A_{12}) is latched on the falling edge of the last $\overline{WE}$. Note that for a write to occur, $\overline{CE}$ and $\overline{WE}$ must be LOW and $\overline{OE}$ must be HIGH. The load portion of the page write is complete when all the data (up to 32 bytes) is loaded into the register.

The automatic write portion starts t_{WW} after each transition of $\overline{WE}$ from LOW-to-HIGH. If $\overline{WE}$ transitions from HIGH-to-LOW before t_{WW} minimum (100 µs), the timer is reset and the automatic write portion does not start. This is how the bytes are loaded into the register. If $\overline{WE}$ is held LOW, this t_{WW} timer never starts and the write cycle is held indefinitely.

If $\overline{WE}$ transitions from LOW-to-HIGH and stays HIGH for at least t_{WW} maximum, then the automatic write sequence is initiated. Note that the load sequence can also be terminated if $\overline{OE}$ goes LOW. Once $\overline{OE}$ is LOW, further attempts to load will be ignored and the part will time out (t_{WW}) and enter the automatic write sequence.

The automatic write sequence consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which puts data back into the erased cells. Note that a page write will only write data to the locations being addressed and will not rewrite the entire page. The Ready/$\overline{Busy}$ pin (R/$\overline{B}$) goes to a logic LOW level during the automatic write sequence. This could signal a microprocessor host that the system bus is free for other activity. When R/$\overline{B}$ transitions to a HIGH state, the Am2864B has completed writing and is ready to accept another cycle.

Byte Mode Write

When $\overline{WE}$ is toggled once, the Am2864B operates in the byte mode. A single byte is loaded into the register and after $\overline{WE}$ goes HIGH and t_{WW} is satisfied, the automatic write cycle starts. It is in this mode that the Am2864B is similar to the Am9864 and the Am2817A.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C ±5°C ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line A_9 of the Am2864B. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am2864B, these two identifier bytes are given in Table 1. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

Output OR-Tieing

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Ready/$\overline{Busy}$ Pin

The Ready/$\overline{Busy}$ (R/$\overline{B}$) pin is an open-drain output which allows two or more R/$\overline{B}$ signals to be OR-tied together. The value of the pullup resistor required is as follows:

$$R_{pu} = \frac{4.6 \text{ volts}}{2.1 \text{ mA} - I_{IL}}$$

I_{IL} = total V_{IL} input current of devices connected to R/$\overline{B}$.

A typical pullup resistor value for R/$\overline{B}$ is 3 kΩ, assuming I_{IL} is less than 0.5 mA.

$\overline{Data}$ Polling

This feature makes the Am2864B highly flexible. It allows the designer the option of a software polling technique as well as the hardware interrupt Ready/$\overline{Busy}$ technique for end of write indication. $\overline{Data}$ Polling requires a simple software routine that performs a read operation when the chip is in the automatic write mode. The data that becomes valid during this $\overline{Data}$ Polling read is the inverse of all 8 bits, last written to the outputs. The true data ($DQ_0 - DQ_7$) will become valid when the automatic write has been completed. Note that all 8 bits

5

invert during $\overline{\text{Data}}$ Polling, thereby giving the user more flexibility during design and layout.

Chip Clear Mode (Military only)

Another feature included on AMD's Am2864B for military applications is a single-pulse chip erase. This optional mode allows the user to program all bits to a logic ONE with a single 10-ms write pulse. Additional information is available from AMD regarding this test mode — consult the local AMD sales office.

Endurance

Since endurance testing is a destructive test it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point, when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant-mortality failures to be screened out. For the next 20,000 to 30,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of 10^4 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained please refer to the Am9864 Reliability Report (PID#06891A).

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

PROGRAMMING

TABLE 1. IDENTIFIER BYTES (Notes 1, 2 & 3)

Identifier	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Device Code	V_{IH}	1	0	0	0	1	0	1	0	8A

Legend: 1 = HIGH
0 = LOW

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. $A_1 - A_8$, $A_{10} - A_{12}$, $\overline{CE}$, $\overline{OE} = V_{IL}$
3. $\overline{WE} = V_{IH}$

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.50 to −0.6 V
Voltage on A_9 with Respect to GND ..... +13.5 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V
Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V
Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V
Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

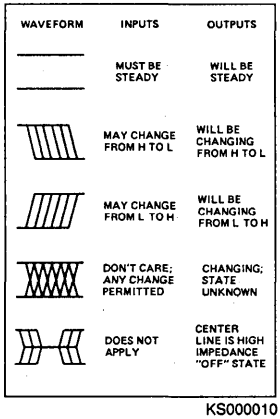
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	µA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ = ⌐¬, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$			100	mA
V_{IL}	Input LOW Voltage		−0.1		.8	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC}+1	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA	2.4			Volts
V_{RB}	R/$\overline{B}$ Output LOW	I_{RB} = 2.1 mA			.45	Volts
C_{IN}	Input Capacitance (Note 1, 2)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Note 1, 2)	$\overline{OE} = \overline{CE} = V_{IH}$, V_{OUT} = 0 V		8	12	pF
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts

Notes: 1. This parameter is sampled on a periodic basis and not 100% tested.
2. Freq. = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.

KEY TO SWITCHING WAVEFORMS



KS000010

5

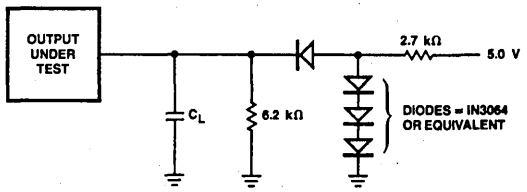
SWITCHING TEST CIRCUIT

Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V



TC002491

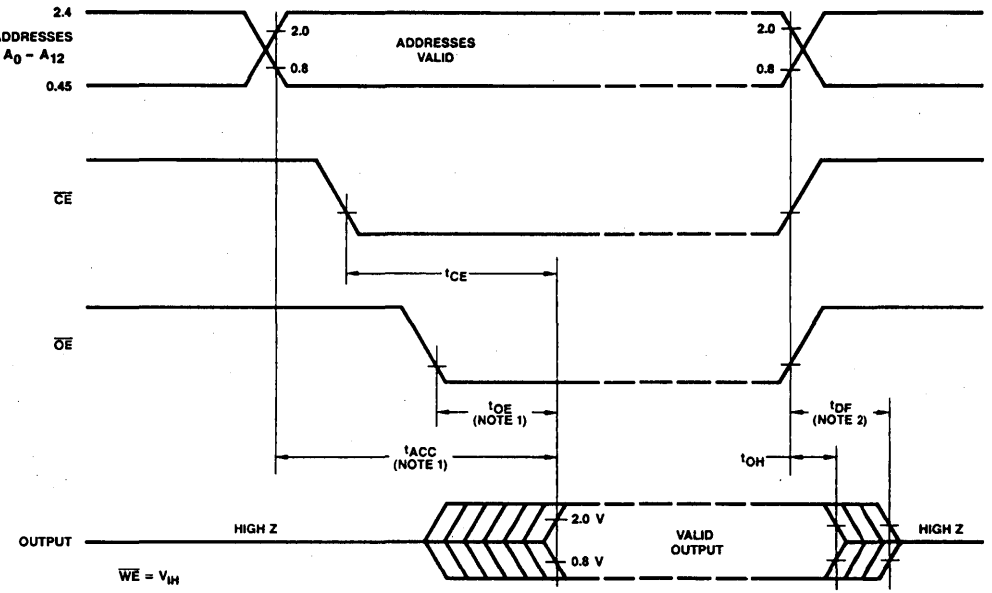
C_L = 100 pF, including jig capacitance.

SWITCHING CHARACTERISTICS over operating ranges

No.	Parameter Symbol	Parameter Description	Test Conditions	Am2864B-2, Am2864B-20		Am2864B, Am2864B-25		Am2864B-3, Am2864B-30		Am2864B355, Am2864B-35		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ												
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		350	ns
3	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		75		100		110		120	ns
4	t_{DF} (Note 1)	Output Enable HIGH to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60		70	0	80	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns
WRITE												
6	t_{AS}	Address to Write Setup Time		20		20		20		60		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time		0		0		0		0		ns
8	t_{WP}	Write Pulse Width		100		100		120		150		ns
9	t_{AH}	Address Hold Time		80		80		80		100		ns
10	t_{DS}	Data Setup Time		50		50		50		70		ns
11	t_{DH}	Data Hold Time		30		30		30		30		ns
12	t_{CH}	$\overline{CE}$ Hold Time		0		0		0		0		ns
13	t_{OES}	$\overline{OE}$ Setup Time		0		0		0		0		ns
14	t_{OEH}	$\overline{OE}$ Hold Time		0		0		0		0		ns
15	t_{DB}	Time to Device Busy			100		100		100		100	ns
16	t_{WC}	$\overline{WE}$ Cycle Time		1		1		1		1		μs
17	t_{WW}	Page Write Window (Note 4)		100	500	100	500	100	500	100	1000	μs
18	t_{WH}	$\overline{WE}$ Hold Time		250		250		250		300		ns
19	t_{WB}	Byte Write Cycle			10		10		10		12	ms
20	t_{RED}	Write Recovery from $\overline{Data}$ Polling Time		20		20		20		20		μs
21	t_{RE}	Write Recovery from R/$\overline{B}$ Time (Note 5)		0		0		0		0		ns
	t_{RBO}	R/$\overline{B}$ to Output Time (Notes 2, 5)			50		50		50		50	ns
	(Notes 1 & 3)	Number of Writes per Byte		10		10		10		10		x1000

Notes: 1. This parameter is sampled on a periodic basis to worst-case test conditions and is not 100% tested.
2. If $\overline{CE}$ and $\overline{OE} = V_{IL}$ when R/$\overline{B}$ is going to V_{OH}, then $DQ_0 - DQ_7$ becomes valid after $t_{RBO} + t_{ACC}$.
3. See Am9864 Reliability Report.
4. A timer of t_{WW} duration starts at every LOW-to-HIGH transition of $\overline{WE}$. If it is allowed to time out, a page load will start. A transition of $\overline{WE}$ from HIGH-to-LOW will stop the timer.
5. This parameter is for information only. It is not tested or characterized.

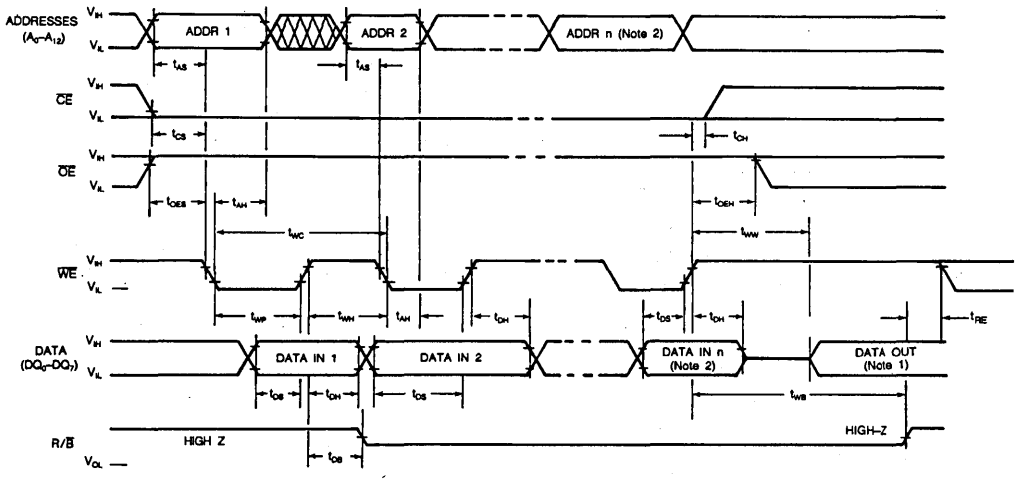
SWITCHING WAVEFORMS (Cont'd.)



WF010282

Read

Notes: 1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.



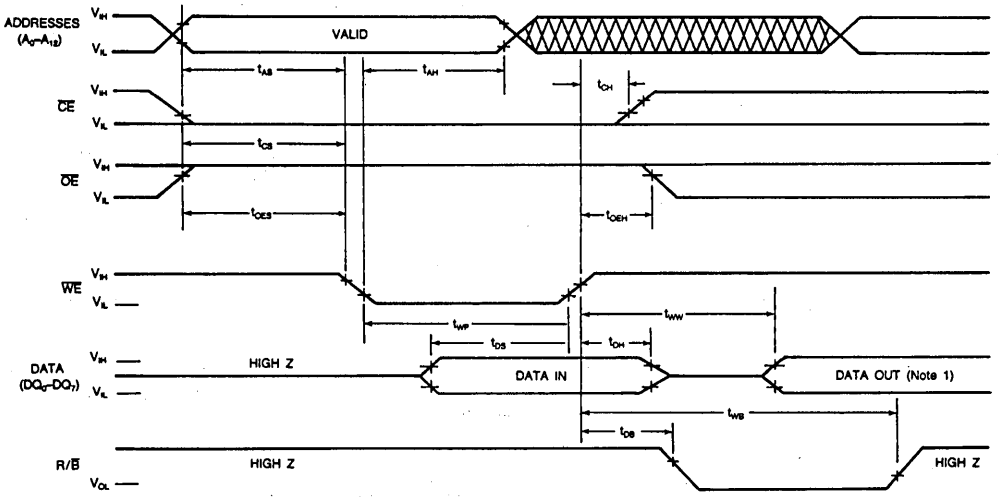
WF020032

Page Write

Notes: 1. This is where $\overline{Data}$ Polling is available. See $\overline{Data}$ Polling timing for setups.
2. $n \leqslant 32$.

5

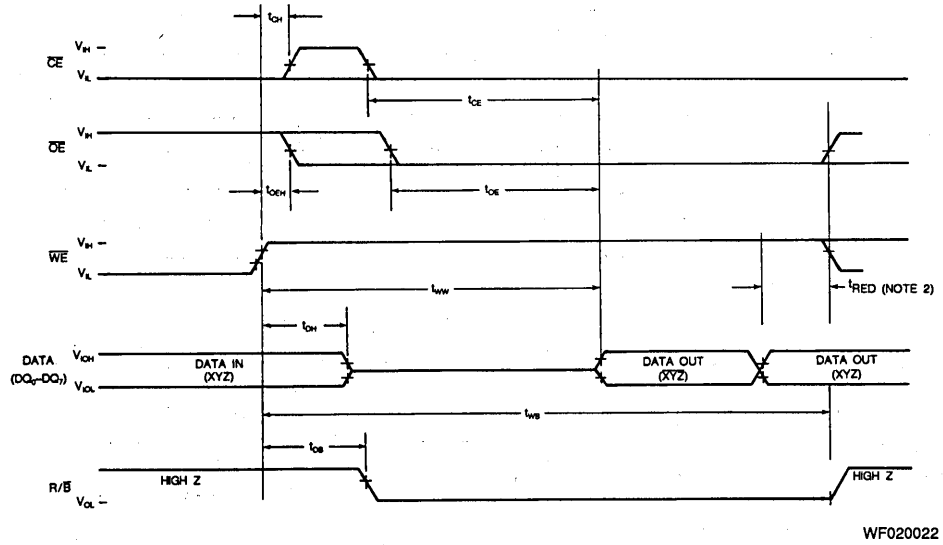
SWITCHING WAVEFORMS



WF020041

Byte Write

Notes: 1. This is where $\overline{\text{Data}}$ Polling is available. See $\overline{\text{Data}}$ Polling timing for setups.



WF020022

$\overline{\text{Data}}$ Polling

Notes: 1. This is shown for single byte write. In page write, R/$\overline{B}$ goes LOW on first LOW-to-HIGH transition of $\overline{WE}$.

2. After the Write cycle is completed (R/$\overline{B}$ is HIGH or data out TRUE), the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
V_{RB}	1, 2, 3
C_{IN}	4
C_{OUT}	4
V_{WI}	7, 8

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	11	t_{DH}	9, 10, 11
2	t_{CE}	9, 10, 11	12	t_{CH}	9, 10, 11
3	t_{OE}	9, 10, 11	13	t_{OES}	9, 10, 11
4	t_{DF}	9, 10, 11	14	t_{OEH}	9, 10, 11
5	t_{OH}	9, 10, 11	15	t_{DB}	9, 10, 11
6	t_{AS}	9, 10, 11	16	t_{WC}	9, 10, 11
7	t_{CS}	9, 10, 11	17	t_{WW}	9, 10, 11
8	t_{WP}	9, 10, 11	18	t_{WH}	9, 10, 11
9	t_{AH}	9, 10, 11	19	t_{WB}	9, 10, 11
10	t_{DS}	9, 10, 11	20	t_{RED}	9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am28C256

32K x 8 Electrically Erasable PROM

ADVANCE INFORMATION

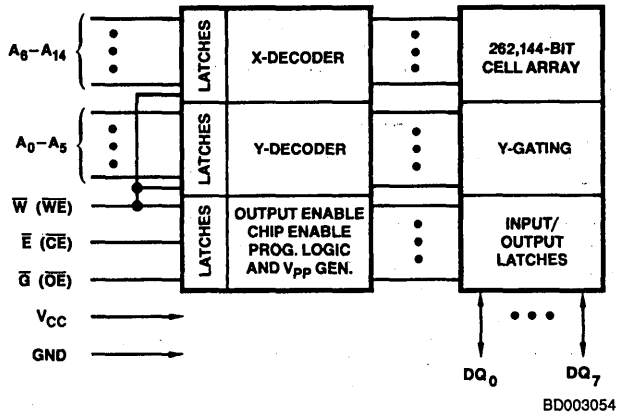
DISTINCTIVE CHARACTERISTICS

- 5-V only operation
- Military temperature range available
- Low-power CMOS
  - 60 mA active current
  - 1 mA standby current
  - 100 μA power-down current
- 64-byte page write
- Software-write protection
- Minimum endurance of 10,000 write cycles per byte with a ten year data retention

GENERAL DESCRIPTION

The Am28C256 is a 32,768 x 8-bit Electrically Erasable Programmable Read-Only Memory (EEPROM). It operates from a single 5-volt supply and has a fully self-timed write cycle with address, data, and control lines latched during the write operation. The 64-byte page-write mode allows full chip programming in as little as five seconds. The Am28C256, in the JEDEC-approved pinout, also features Status-Bit Polling, and a software-write protect that enhances the hardware-write protect. The Am28C256 is an upward-compatible part from the Am2864A and Am2864B. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



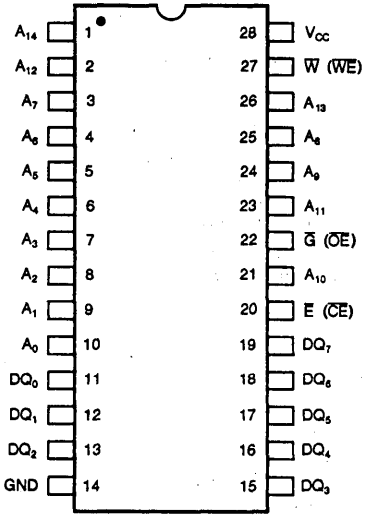
BD003054

PRODUCT SELECTOR GUIDE

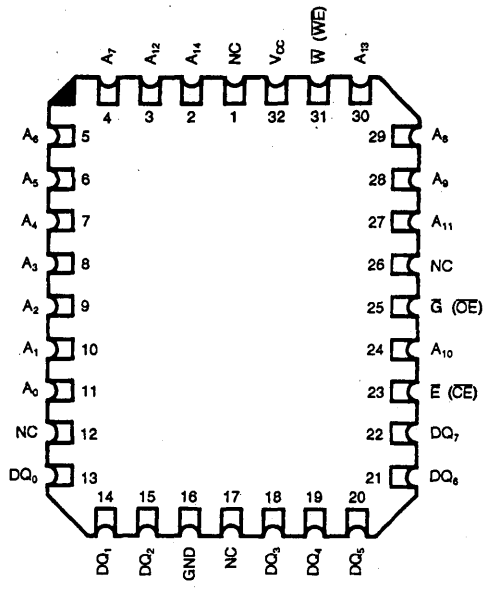
Family Part No.				
Ordering Part No.: ±5% V_{CC} Tolerance	28C256-205	28C256	28C256-305	28C256-355
±10% V_{CC} Tolerance	28C256-200	28C256-250	28C256-300	28C256-350
t_{ACC} (ns)	200	250	300	350
t_{CE} (ns)	200	250	300	350
t_{OE} (ns)	75	100	110	120

Publication # 08124 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



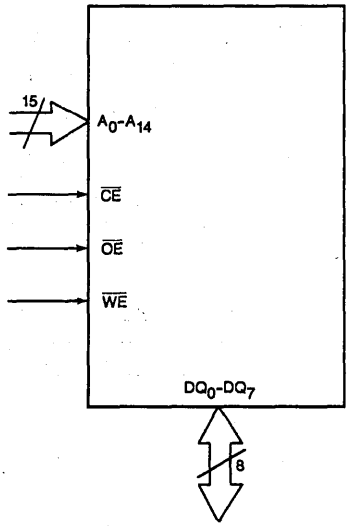
CD009821



CD009831

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002570

VCC = Power Supply
GND = Ground

FUNCTIONAL DESCRIPTION

Read Mode

The Am28C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable, $\overline{E}$ ($\overline{CE}$), is the power control and should be used for device selection. Output Enable, $\overline{G}$ ($\overline{OE}$), is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{E}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am28C256 has a standby mode which reduces the active power dissipation by 98%, from 300 mW to 5 mW (values for 0 to +70°C). The Am28C256 is placed in the standby mode by applying a TTL-HIGH signal to the $\overline{E}$ ($\overline{CE}$) input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{G}$ ($\overline{OE}$) input.

Power-Down Mode

The Am28C256 also has a power-down mode which reduces the power dissipation by 99.8% — from 300 mW to .5 mW (values for 0 to +70°C). The Am28C256 is placed in power down by raising $\overline{E}$ ($\overline{CE}$) to V_{CC} ±0.3 V.

Data Protection — Hardware

The Am28C256 incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.5 volts. It is the user's responsibility to ensure that the control levels are logically correct when V_{CC} is above 3.5 volts.

There is a $\overline{W}$ ($\overline{WE}$) lockout circuit that prevents $\overline{W}$ pulses of less than 20 ns duration from initiating a write cycle.

When the $\overline{G}$ ($\overline{OE}$) control is LOW (logic ZERO), a write cycle cannot be initiated.

Data Protection — Software

In addition to the hardware-protected write features provided on the Am28C256, the user may choose to implement software-write protect and minimize the chances of inadvertent writes.

The software-write protection has three modes of operation: set protection, write operation under protection, and disable protection.

Set Protection

The default power-up mode of the Am28C256 is with the protection disabled. The software-write protection is set by performing a three-byte write operation (with page-mode timing) using specific addresses and data.

TABLE 1. SET-PROTECTION MODE

Step	Mode	$A_{14} - A_0$	$I/O_7 - I/O_0$	Comment
1	Write	5555 Hex	AA Hex	Dummy Write
2	Write	2AAA Hex	55 Hex	Dummy Write
3	Write	5555 Hex	A0 Hex	Dummy Write

A violation of this sequence or the timeout of a 100-μs timer ($\overline{WE}$ transition LOW-to-HIGH starts the timer) aborts the set-protection operation.

The first time this sequence is applied to the part, a non-volatile bit is set. This reconfigures the part so that both software and hardware-protection are implemented. Once this bit is set, the software algorithm must be used every time a write cycle occurs.

Write Operation Under Protection

The write operation uses the same three steps to unlock the write protection for each byte-write, or page-write operation. Note that while under software write protection, a write can only be performed using page mode timing. Thus, a "byte write" is actually a four byte page write. The first three bytes unlock write protection (and are not written), while the fourth byte is the single byte to be written into the device.

TABLE 2. WRITE OPERATION UNDER PROTECTION MODE

Step	Mode	$A_{14} - A_0$	$I/O_7 - I/O_0$	Comment
1	Write	5555 Hex	AA Hex	Dummy Write
2	Write	2AAA Hex	55 Hex	Dummy Write
3	Write	5555 Hex	A0 Hex	Dummy Write
4 – 67	Write	Address	Data	Page-Load Writes

At the conclusion of the write cycle, the write operations to the Am28C256 are disabled. The page addresses ($A_6 - A_{14}$) should be held constant throughout the page-load operation (steps 4 – 67).

Disable Protection

The software protection can be disabled, and the part reconfigured to hardware-only protection, by using the operations shown in Table 3. Again, page mode timing must be used for all six bytes.

TABLE 3. DISABLE-PROTECTION MODE

Step	Mode	$A_{14} - A_0$	$I/O_7 - I/O_0$	Comment
1	Write	5555 Hex	AA Hex	Dummy Write
2	Write	2AAA Hex	55 Hex	Dummy Write
3	Write	5555 Hex	80 Hex	Dummy Write
4	Write	5555 Hex	AA Hex	Dummy Write
5	Write	2AAA Hex	55 Hex	Dummy Write
6	Write	5555 Hex	20 Hex	Dummy Write

The software-write protection is now disabled and the user has unrestricted write access to the Am28C256 — like on the Am2864B EEPROM.

Byte-Write Mode

To write into a particular location, addresses must be valid and a TTL LOW applied to the Write Enable ($\overline{W}$) pin of a selected ($\overline{E}$ LOW) device. This combined with Output Enable ($\overline{G}$) being HIGH, initiates a write cycle. During a byte-write cycle, all inputs except data are latched on the falling edge of $\overline{W}$ or $\overline{E}$, whichever occurred last. Data is latched on the rising edge of $\overline{W}$ or $\overline{E}$, whichever occurred first. An automatic erase is performed before data is written.

For system-design simplification, the Am28C256 is designed in such a way that either the $\overline{E}$ or $\overline{W}$ pin can be used to initiate a write cycle. The device uses the second HIGH-to-LOW transition of either $\overline{E}$ or $\overline{W}$ to latch addresses and the first LOW-to-HIGH transition to latch the data. For example, if $\overline{W}$ is used to initiate and terminate the write cycle, then $\overline{W}$ must go LOW after $\overline{E}$ goes LOW, and $\overline{W}$ must return HIGH before $\overline{E}$ goes HIGH. It is also permissible to mix control pins. As a second example, if $\overline{E}$ is used to initiate the write cycle and $\overline{W}$ is used to end the cycle, then $\overline{E}$ must go LOW after $\overline{W}$ goes LOW, and $\overline{W}$ must return HIGH before $\overline{E}$ goes HIGH. All address setup and hold times are with respect to the HIGH-to-LOW transition of the lagging control pin, and all data setup and hold times are with respect to the LOW-to-HIGH transition of the leading control pin.

To simplify the following discussion, the $\overline{W}$ pin is used as the write-cycle control pin throughout the rest of this data sheet.

Page-Write Mode

The page write allows from 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. The page-write mode consists of a load sequence, followed by an automatic write sequence.

During the load portion, sequential $\overline{W}$ ($\overline{WE}$) pulses load the byte address and the byte data into a 64-byte register; the bytes can be loaded into this register in any order. On each $\overline{W}$ pulse, the "Y" address is latched on the falling edge of $\overline{W}$, the data input is latched on the rising edge of $\overline{W}$, and the page address ($A_6 - A_{14}$) is latched on the falling edge of the last $\overline{W}$. Note that for a write to occur, $\overline{E}$ ($\overline{CE}$) and $\overline{W}$ ($\overline{WE}$) must be LOW, and $\overline{G}$ ($\overline{OE}$) must be HIGH. Although the page address ($A_6 - A_{14}$) is latched on the final $\overline{W}$ HIGH-to-LOW pulse (before t_{WW}), it is recommended that the page address be held steady during the entire page load. This is to ensure that an accidental software write protect sequence is not seen by the device. If the user chooses to change addresses during the page load, it is then the user's responsibility to make sure the three byte software algorithm is not accidentally sent to the device.

The automatic-write portion starts t_{WW} after the last transition of $\overline{W}$ from LOW-to-HIGH. If $\overline{W}$ transitions from HIGH-to-LOW before t_{WW} minimum (100 μs), the timer is reset and the automatic-write portion does not start. This is how the bytes are loaded into the register. If $\overline{W}$ is held LOW, this t_{WW} timer never starts and the write cycle is held indefinitely.

If $\overline{W}$ transitions from LOW-to-HIGH and stays HIGH for at least t_{WW} maximum, then the automatic-write sequence is initiated. Note that the load sequence can also be disabled if $\overline{G}$ ($\overline{OE}$) goes LOW. If $\overline{G}$ is LOW, attempts to load will be ignored. The part will time out if $\overline{G}$ ($\overline{OE}$) is held LOW longer than t_{WW} Max. and enter the automatic-write sequence.

The automatic-write sequence consists of an erase cycle — which erases any data that existed in each addressed cell, and a write cycle — which puts data back into the erased cells. Note that a page write will only write data to the locations selected during the page load and will not rewrite the entire page.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C ±5% ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line A_9 of the Am28C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28C256, these two identifier bytes are given in Table 5. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (O_7) defined as the parity bit.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation.
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{E}$ ($\overline{CE}$) be decoded and used as the primary device-selecting function, while $\overline{G}$ ($\overline{OE}$) be made a common connection to all devices in the array and connected to the Read line from the system-control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Write-Operation Status Register

The Am28C256 features a Status-Bit register which can be used to poll the present state of the part. During a write cycle, a read to the Status register can be performed. Out of this register the toggle bit, the page-load timer, and $\overline{DATA}$ polling can be read.

5

Toggle Bit (DQ_6)

The toggle bit is used to tell if the Am28C256 is still writing. The toggle bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device, as is required when using $\overline{DATA}$ polling. With each consecutive read, I/O_6 toggles. Therefore, two read operations must be performed to get the status.

Page-Load Timer (DQ_5)

The page-load timer tells the user if the page-write window (t_{WW}) has timed out, and the write cycle has commenced, or if it's still available to load data into. If I/O_5 is HIGH, the write cycle has begun; if it's LOW, t_{WW} has not timed out.

$\overline{DATA}$ Polling (DQ_7)

$\overline{DATA}$ polling requires a simple software routine that performs a read operation when the chip is in the automatic-write mode. The data that becomes valid during this $\overline{DATA}$ polling read is the inverse of DQ_7, last written to DQ_7. The true data (DQ_7) will become valid when the automatic write has been completed.

Endurance

Since endurance testing is a destructive test, it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data-retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point — when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide — the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant mortality failures to be screened out. For the next 20,000 to 30,000 write cycles, the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of 10^4 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD-test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability mechanisms are measured.

TABLE 4. Am28C256 MODE SELECT

MODE \ PINS	$\overline{E}$ ($\overline{CE}$)	$\overline{G}$ ($\overline{OE}$)	$\overline{W}$ ($\overline{WE}$)	A_9	OUTPUTS
Read	L	L	H	X	D_{OUT}
Write	L	H	L	X	D_{IN}
Standby/Write Inhibit	H	X	X	X	Hi-Z
Write Inhibit	X	L	X	X	
Write Inhibit	X	X	H	X	
Auto Select	L	L	H	V_H	CODE
$\overline{DATA}$ Polling	L	L	H	X	$DQ_7 - \overline{D_{IN7}}$

Key: L = LOW (V_L)
H = HIGH (V_H)
X = Don't Care
V_H = 12.0 V ±0.5 V

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed-circuit-board traces on EEPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −65 to +135°C
Voltage on All Inputs
with Respect to Ground, except A_9 ..+6.50 V to −0.6 V
Voltage on A_9
with Respect to Ground ..... +13.50 V to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −205, blank, −305, and −355 versions, V_{CC} = +4.75 to +5.25 V.
2. For −200, −250, −300, and −350 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V, $\overline{G}$ ($\overline{OE}$) = V_{IH}		10	μA
I_{CC3}	V_{CC} Current (Power Down)	$\overline{E}$ ($\overline{CE}$) = V_{CC} ±0.3 V		100	μA
I_{CC2}	V_{CC} Current (Standby)	$\overline{E}$ ($\overline{CE}$) = V_{IH}, $\overline{G}$ ($\overline{OE}$) = V_{IL}		1	mA
I_{CC1}	V_{CC} Current (Active)	$\overline{E}$ ($\overline{CE}$) = V_{IL}, $\overline{W}$ ($\overline{WE}$) = V_{IH}, f = 5 MHz, I_{OUT} = 0 mA (Note 3)		60	mA
I_{CC}	V_{CC} Current (Write)	$\overline{E}$ ($\overline{CE}$) = V_{IL}, $\overline{G}$ ($\overline{OE}$) = V_{IH}, $\overline{W}$ ($\overline{WE}$) = V_{IL}		60	mA
V_{IL}	Input LOW Voltage		−0.1	.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +1	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = 400 μA	2.4		V
V_{WI}	Write-Inhibit Voltage		3.5		V

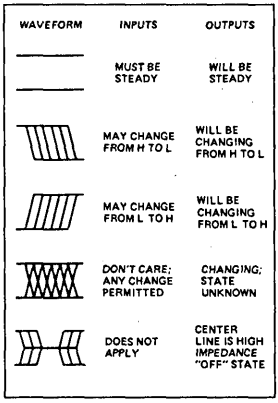
CAPACITANCE (Notes 1 & 2)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4	10	pF
C_{OUT}	Output Capacitance	$\overline{G}$ ($\overline{OE}$) = $\overline{E}$ ($\overline{CE}$) = V_{IH}, V_{OUT} = 0 V	8	12	pF

Notes: 1. T_A = 25°C, f = 1 MHz
2. This parameter is sampled and not 100% tested.
3. This parameter is tested with $\overline{G}$ ($\overline{OE}$) = V_{IH} to simulate open outputs.

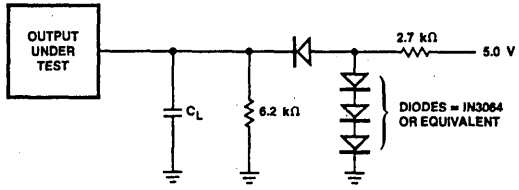
5

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING TEST CIRCUITS



TC002491

C_L = 100pF, including jig capacitance.

Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

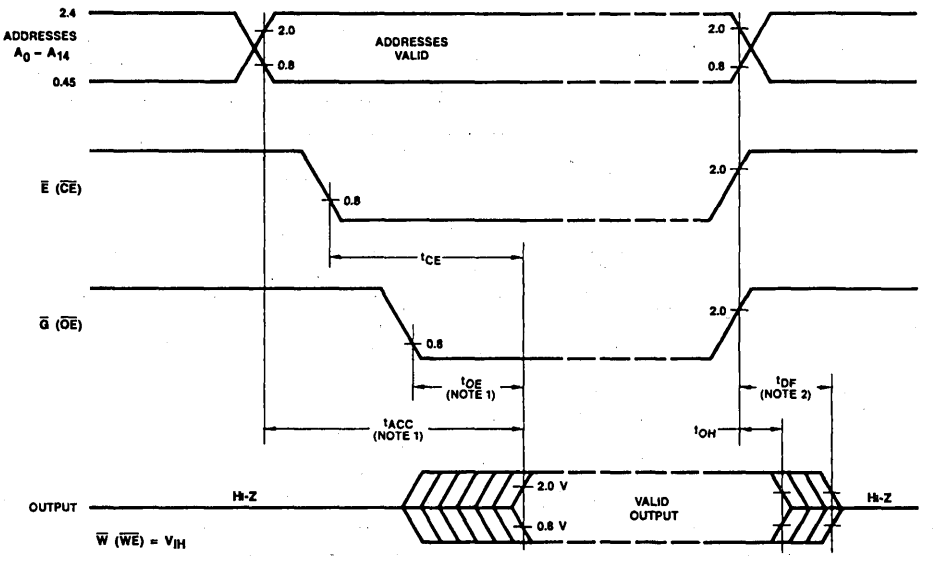
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol JEDEC	Parameter Symbol Std.	Parameter Description	Test Conditions	28C256-205, -200 Min.	28C256-205, -200 Max.	28C256, -250 Min.	28C256, -250 Max.	28C256-305, -300 Min.	28C256-305, -300 Max.	28C256-355, -350 Min.	28C256-355, -350 Max.	Units
READ													
1	t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{E}$ ($\overline{CE}$) = $\overline{G}$ ($\overline{OE}$) = V_{IL}		200		250		300		350	ns
2	t_{ELQV}	t_{CE}	$\overline{E}$ to Output Delay	$\overline{G}$ ($\overline{OE}$) = V_{IL}		200		250		300		350	ns
3	t_{GLQV1}	t_{OE}	Output Enable to Output Delay	$\overline{E}$ ($\overline{CE}$) = V_{IL}		75		100		110		120	ns
4	t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 1)	Output Enable HIGH to Output Float	$\overline{E}$ ($\overline{CE}$) = V_{IL}	0	60	0	60		70	0	80	ns
5	t_{AXQX}	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{E}$ or $\overline{G}$ Whichever Occurred First	$\overline{E}$ ($\overline{CE}$) = $\overline{G}$ ($\overline{OE}$) = V_{IL}	0		0		0		0		ns
WRITE													
6		t_{AS}	Address to Write Setup Time		10		10		20		40		ns
7		t_{AH}	Address Hold Time		100		100		100		100		ns
8		t_{DS}	Data Setup Time		50		50		50		70		ns
9		t_{DH}	Data Hold Time		20		20		25		40		ns
10		t_{CS}	$\overline{E}$ to Write Setup Time		0		0		0		0		ns
11		t_{CH}	$\overline{E}$ Hold Time		0		0		0		0		ns
12		t_{OES}	$\overline{G}$ Setup Time		0		0		0		0		ns
13		t_{OEH}	$\overline{G}$ Hold Time		0		0		0		0		ns
14		t_{WP}	Write Pulse Width		100		100		120		150		ns
15		t_{WC}	$\overline{W}$ Cycle Time		1		1		1		1		μs
16		t_{WW}	Page Write Window (Note 2)		100	250	100	250	100	250	100	500	μs
17		t_{WH}	$\overline{W}$ Hold Time		100		100		120		150		ns
18		t_{WB}	Byte Write Cycle			10		10		10		10	ms
19		t_{RED}	Write Recovery from $\overline{DATA}$ Polling Time (Note 3)		0		0		0		0		μs
20		t_{SB}	$\overline{G}$ ($\overline{OE}$) LOW to Status Bit		150		150		150		150		ns
21		t_{OEW}	Write Control Recovery		50		50		50		50		ns
		(Note 1)	Number of Writes per Byte		10		10		10		10		x 1000

Notes: 1. This parameter is sampled and not 100% tested.
2. A timer of t_{WW} duration starts at every LOW-to-HIGH transition of $\overline{W}$ ($\overline{WE}$). If it is allowed to time out, a page write will start. A transition of $\overline{W}$ from HIGH to LOW will stop the timer.
3. This parameter is for information only. It is not tested or characterized.

5

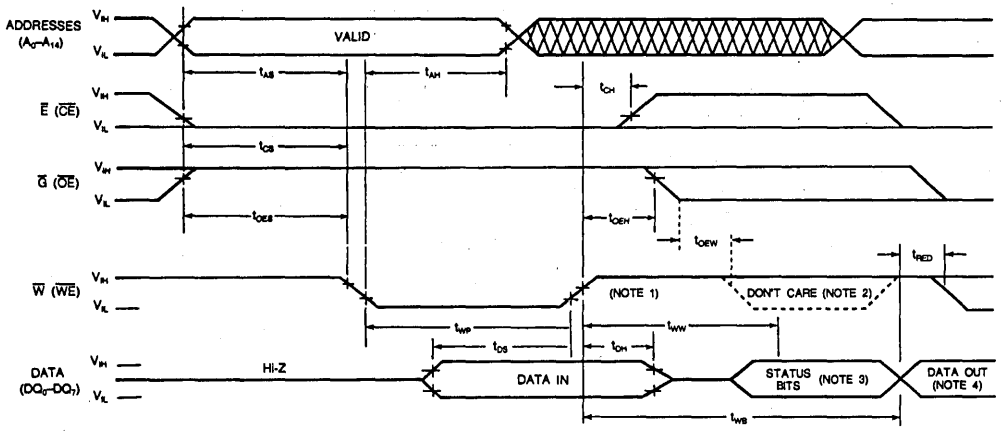
SWITCHING WAVEFORMS (Cont'd.)



WF010286

Read

Notes: 1. $\overline{G}$ ($\overline{OE}$) may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ ($\overline{CE}$) without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{G}$ ($\overline{OE}$) or $\overline{E}$ ($\overline{CE}$) whichever occurs first.

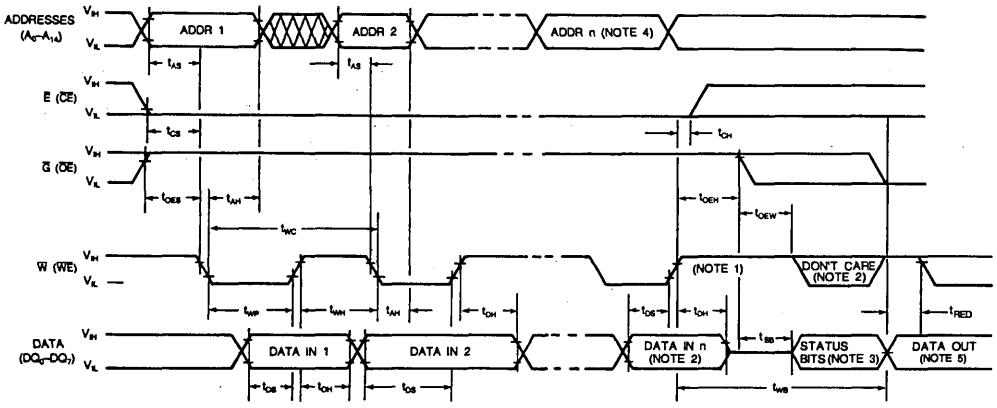


WF020045

Byte — Write Timing

Notes: 1. To initiate the write cycle, one of the following write controls must be held for at least t_{WW} maximum: $\overline{W}$ ($\overline{WE}$) HIGH, $\overline{E}$ ($\overline{CE}$) HIGH, or $\overline{G}$ ($\overline{OE}$) LOW.
2. After being held HIGH for a minimum of $t_{OEW} + t_{OEH}$, $\overline{W}$ can be toggled LOW during the write cycle as long as one of the following conditions are met: $\overline{E}$ HIGH or $\overline{G}$ LOW.
3. This is where STATUS Bits are available. STATUS Bits are only available with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW.
4. Data is available only with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW.

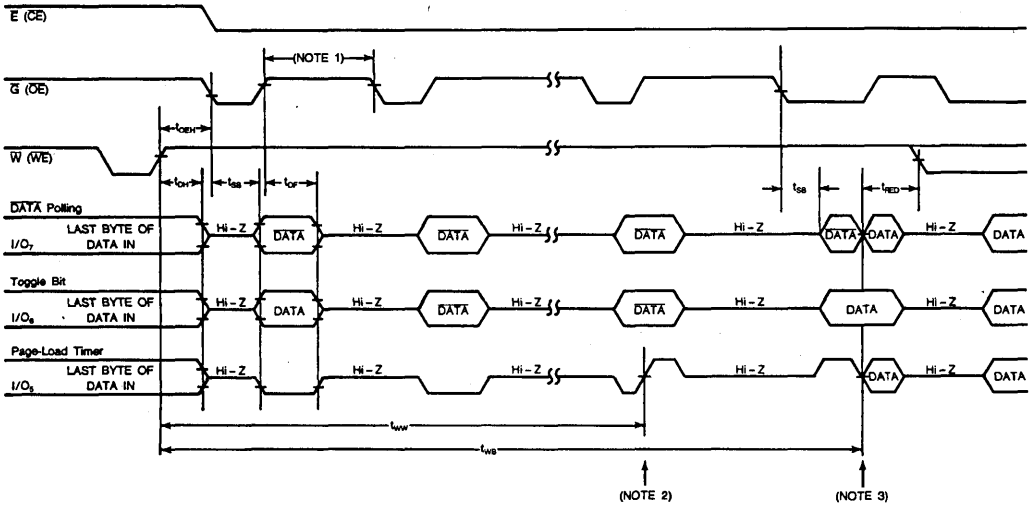
SWITCHING WAVEFORMS



WF020036

Page-Write Timing

Notes: 1. To initiate the page-write cycle, one of the following write controls must be held for at least t_{WW} maximum: $\overline{W}$ HIGH, $\overline{E}$ HIGH, or $\overline{G}$ LOW.
2. After being held HIGH for a minimum of t_{OEW}, $\overline{W}$ can be toggled LOW during the write cycle as long as one of the following conditions are met: $\overline{E}$ HIGH or $\overline{G}$ LOW.
3. This is where STATUS Bits are available. STATUS Bits are only available with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW. (See STATUS Bits Timing for setups.)
4. $n \leqslant 64$
5. Data is available only with $\overline{W}$ HIGH, $\overline{E}$ LOW, and $\overline{G}$ LOW.



WF022251

Write Operation STATUS Bit Timing

Notes: 1. $\overline{G}$ ($\overline{OE}$) HIGH Minimum 50 ns
2. Page load ends and internal write cycle starts here.
3. Internal write cycle ends and a fresh page load may be initiated here.

5

PROGRAMMING

Please refer to Table 5 for a summary of identifier bytes.

TABLE 5. IDENTIFIER BYTERS (Notes 1 & 2)

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am28C256 Device Code	V_{IH}	0	0	1	0	0	0	0	0	20

Key: 1 = Logic HIGH
0 = Logic LOW

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{E}$ ($\overline{CE}$), $\overline{G}$ ($\overline{OE}$) = V_{IL}
3. $\overline{W}$ ($\overline{WE}$) = V_{IH}

MOS UV Erasable Programmable ROM (EPROM) Index

Am2716B/Am2732B

2048 x 8-Bit/4096 x 8-Bit EPROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access times — as low as 100 ns
- Low-power dissipation
- Programming voltage — 12.5 V
- Single +5-V power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available

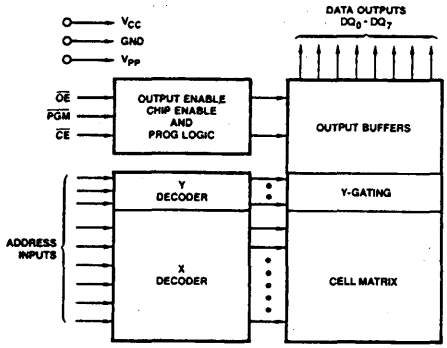
GENERAL DESCRIPTION

The Am2716B and Am2732B are ultraviolet Erasable Programmable Read-Only Memories (EPROMs) and are organized as 2048 x 8 bits, and 4096 x 8 bits, respectively. All standard EPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any Wait states. Some of AMD's EPROMs have access times of as fast as 100 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD EPROMs offer separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's EPROMs may be programmed using 1-ms pulses.

BLOCK DIAGRAM



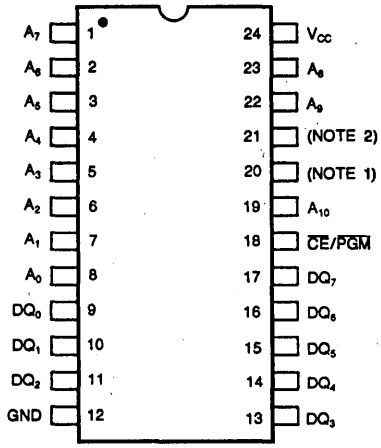
BD000231

PRODUCT SELECTOR GUIDE

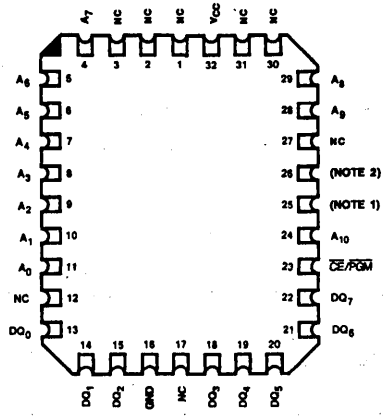
Family Part No.	Am2716B/Am2732B					
Ordering Part No.:						
±5% V_{CC} Tolerance	2716B-105 2732B-105	2716B-155 2732B-155	2716B-205 2732B-205	2716B 2732B	2716B-305 2732B-305	2716B-455 2732B-455
±10% V_{CC} Tolerance	2716B-100 2732B-100	2716B-150 2732B-150	2716B-200 2732B-200	2716B-250 2732B-250	2716B-300 2732B-300	2716B-455 2732B-455
t_{ACC} (ns)	100	150	200	250	300	450
t_{CE} (ns)	100	150	200	250	300	450
t_{OE} (ns)	75	75	75	100	110	150

Publication # 08160 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD009781



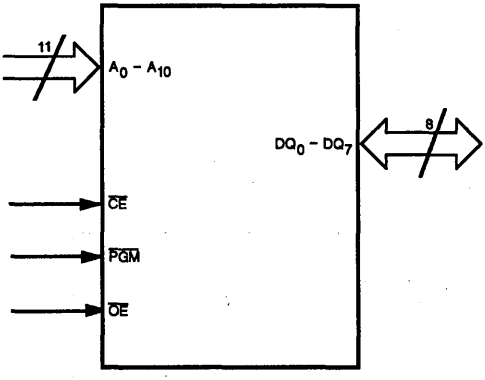
CD009431

Notes:

	Am2716B	Am2732B
1	$\overline{OE}$	$\overline{OE}/V_{PP}$
2	V_{PP}	A_{11}

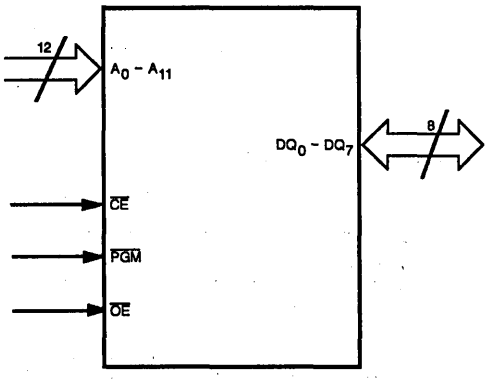
LOGIC SYMBOLS

Am2716B



LS002361

Am2764B

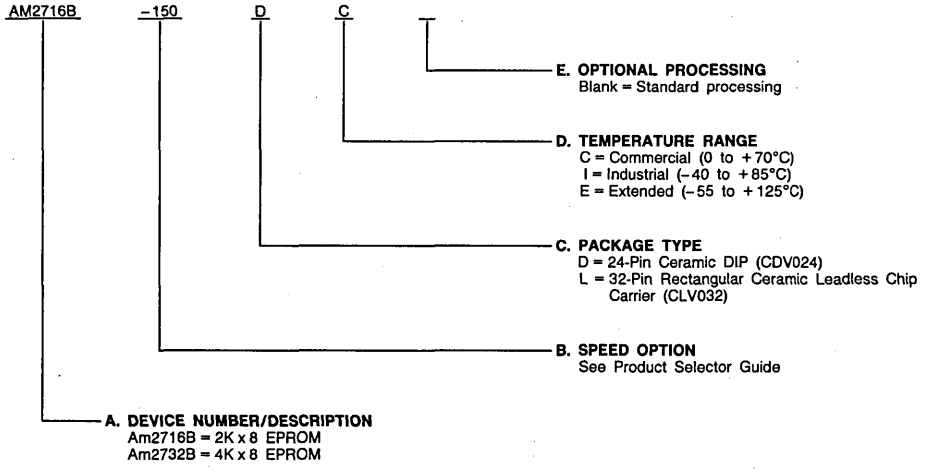


LS002371

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
±5% V_{CC} Tolerance	
AM2716B-105	DC, DI, LC, LI
AM2716B-155	
AM2716B-205	
AM2716B	
AM2716B-305	
AM2716B-455	
AM2732B-105	
AM2732B-155	
AM2732B-205	
AM2732B	
AM2732B-305	
AM2732B-455	
±10% V_{CC} Tolerance	
AM2716B-100	DC, DI, LC, LI
AM2716B-150	
AM2732B-100	
AM2732B-150	
AM2716B-200	DC, DI, DE, LC, LI, LE
AM2716B-250	
AM2716B-300	
AM2716B-450	
AM2732B-200	
AM2732B-250	
AM2732B-300	
AM2732B-450	

Valid Combinations

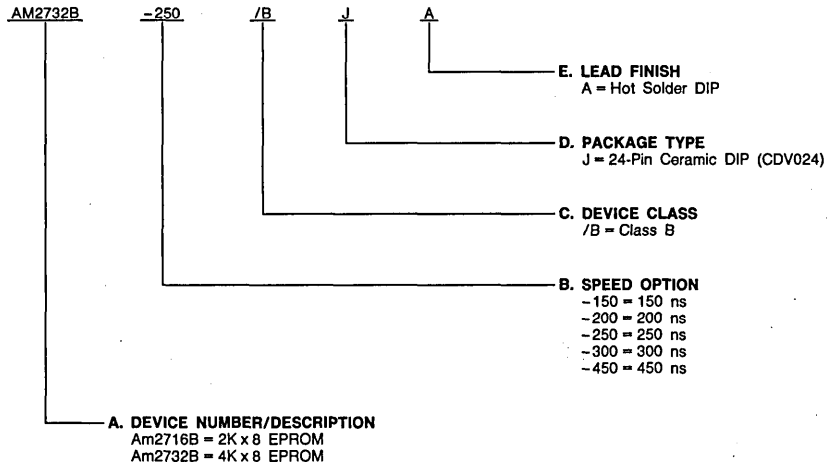
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

6

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
±10% V_{CC} Tolerance	
AM2716B-150	/BJA
AM2716B-200	
AM2716B-250	
AM2716B-300	
AM2716B-450	
AM2732B-150	
AM2732B-200	
AM2732B-250	
AM2732B-300	
AM2732B-450	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

FUNCTIONAL DESCRIPTION

Erasing the EPROMs

In order to clear all locations of their programmed contents, it is necessary to expose the EPROMs to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 $\mu W/cm^2$ for fifteen to twenty minutes. The EPROM should be about directly under and about one inch from the source and all filters should be removed from the ultraviolet light source prior to erasure.

It is important to note that the EPROMs will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with ultraviolet sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the EPROMs and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the EPROMs

Upon delivery, or after each erasure, the EPROM has all bits in the "1", or HIGH state. Zeros ("0s") are loaded into the EPROM through the procedure of programming.

The programming mode is entered when a voltage greater than 12.0, but less than 13.3 V is applied to the V_{PP} pin ($\overline{OE}/V_{PP}$ for 32K) and $\overline{CE}/\overline{PGM}$ is given a TTL-LOW pulse. The data to be programmed is applied 8 bits in parallel to the Data I/O (DQ_n) pins.

The flowchart (Figure 1) in the Programming section of this document shows the AMD-preferred interactive programming algorithm. Interactive algorithms requires less programming time than most other algorithms. This does not preclude the use of other algorithms, including the conventional 50-ms pulse, as long as the maximum specifications are not violated.

The AMD-preferred algorithm reduces programming time by using short (1 ms) program pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 15 pulses. This process is repeated while sequencing through each address of the EPROM. The interactive section of the algorithm is programmed and verified at $V_{CC} = 6.0$ V, ±5%.

The overprogram section of the algorithm programs the entire array by cycling through each address and applying an additional 2-ms program pulse. This section is done at $V_{CC} = 5.0$ V, ±5%.

After the final address is completed, the entire EPROM is verified to the data-sheet specifications of $V_{CC} = 5.0$ V, ±5%.

Auto Select Mode

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient-temperature range required when programming the EPROMs.

To activate this mode, the programming equipment must force 12.0 V ±0.5 V on address line A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select mode.

Byte 0 ($A_0 = V_{IL}$, $DQ_0 - DQ_7$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$, $DQ_0 - DQ_7$), the device identifier code. These identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the most significant bit (MSB), DQ_7, defined as the parity bit.

Read Mode

AMD EPROMs have two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

AMD EPROMs have a standby mode which reduces the active power dissipation up to 80%. The EPROM is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for: 1) low-memory power dissipation, and 2) assurance that output-bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array, and connected to the Read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs (including $\overline{OE}$ and V_{PP}) of the parallel EPROMs may be common. For the Am2716B, a LOW-level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed. For the Am2732B, a HIGH-level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed.

Data for all the EPROMs should be verified t_{OE} after the falling edge of $\overline{OE}$, V_{PP} may remain at 12.5 V for the 2716B during program verify, but for the 2732B, $\overline{OE}/V_{PP}$ must be a TTL low level.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capaci-

tance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit-board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

FUNCTION TABLES

TABLE 1. Am2716B MODE SELECT

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	V_{PP}	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output Disable	L	H	X	V_{CC}	Hi-Z
Standby	H	X	X	V_{CC}	Hi-Z
Program	L	H	X	V_{PP}	D_{IN}
Program Verify	L	L	X	V_{PP}	D_{OUT}
Program Inhibit	L	H	X	V_{PP}	Hi-Z
Auto Select	L	L	V_H	V_{CC}	Code

TABLE 2. Am2732B MODE SELECT

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	A_9	OUTPUTS
Read	L	L	X	D_{OUT}
Output Disable	L	H	X	Hi-Z
Standby	H	X	X	Hi-Z
Program	L	V_{PP}	X	D_{IN}
Program Verify	L	L	X	D_{OUT}
Program Inhibit	H	V_{PP}	X	Hi-Z
Auto Select	L	L	V_H	Code

Key: L = LOW
H = HIGH
X = Can be either LOW or HIGH
V_H = 12.0 V ±0.5 V

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Supply Voltage
with respect to Ground
on all Inputs except A_9 and V_{PP} ..... +6.25 to −0.6 V
on A_9 ..... +13.50 to −0.6 V
on V_{PP} ..... +13.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −105, −155, −205, blank, −305, and −455 versions, V_{CC} = +4.75 to +5.25 V.
2. For −100, −150, −200, −250, −300, and −450 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, & 4)*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1	V
V_{IL}	Input LOW Voltage			−0.1	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 to +5.5 V			10.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to −5.5 V			10.0	μA
I_{CC1}	V_{CC} Standby Current for Am2716B (Note 6)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		25	mA
			E/M Devices		40	
	V_{CC} Standby Current for Am2732B		C, I, E, & M Devices		40	
I_{CC2}	V_{CC} Active Current for Am2716B and Am2732B	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	C, I, E & M Devices		100	mA
I_{PP1}	V_{PP} Program Current (Note 5)	V_{PP} = 5.5 V	C, I, E, & M Devices		30	mA
I_{PP2}	V_{PP} Read Current	V_{PP} = 5.5 V	C, I, E, & M Devices		5	mA

Notes: See notes following the Capacitance table on next page.

*See the last page of this spec for Group A Subgroup Testing information.

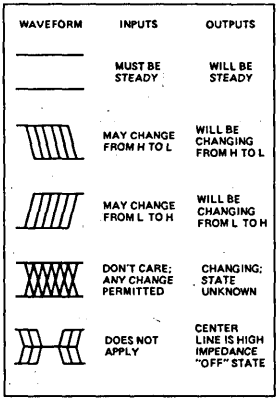
6

CAPACITANCE (Notes 2 & 3)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0$ V	4	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$ V	8	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0$ V	12	20	pF
C_{IN3}	$\overline{CE}/\overline{PGM}$ Input Capacitance		9	12	

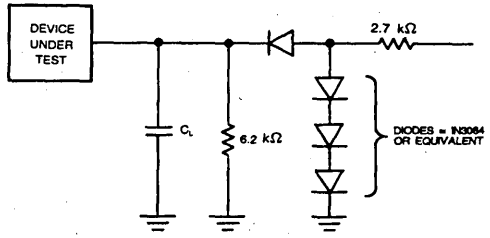
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The EPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. V_{PP} may be connected to V_{CC} directly except during programming. The supply would then be the sum of I_{CC} and I_{PP}.
6. I_{CC1} Max. is 40 mA for −4XX devices.

KEY TO SWITCHING WAVEFORMS



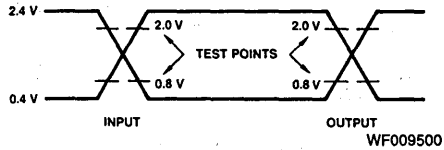
KS000010

SWITCHING TEST CIRCUITS



TC003191

SWITCHING TEST WAVEFORMS



WF009500

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "0". Input pulse rise and fall times are 5 ns.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Notes 1 & 3)

(Table 1 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	-105, -100		-155, -150		-205, -200		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		100		150		200	ns
2	t_{CE}	Chip Enable to Output Delay			100		150		200	ns
3	t_{OE}	Output Enable to Output Delay			75		75		75	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	60	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

(Table 2 of 2)

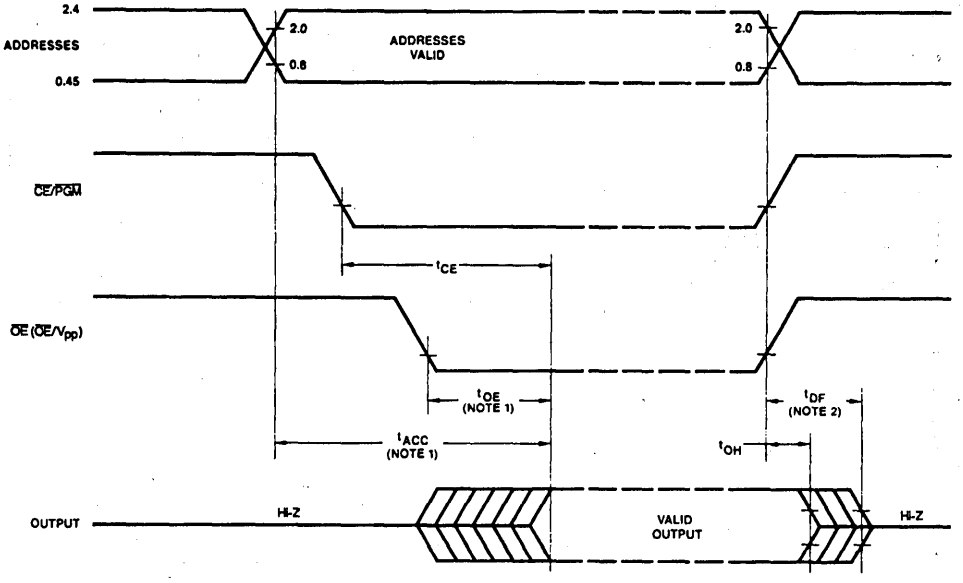
No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	Blank, -250		-305, -300		-455, -450		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		250		300		450	ns
2	t_{CE}	Chip Enable to Output Delay			250		300		450	ns
3	t_{OE}	Output Enable to Output Delay			100		110		150	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	80	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. Caution: The EPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C_L = 100$ pF,
Input Rise and Fall Times: ≤ 20 ns,
Input Pulse Levels: 0.45 to 2.4 V,
Timing Measurement Reference Level — Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V.

*See the last page of this spec for Group A Subgroup Testing information.

6

SWITCHING WAVEFORMS



WF021981

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING

This section covers Identifier bytes, Interactive Flowcharts, and Interactive Programming Algorithms for DC Programming and Switching Programming Characteristics.

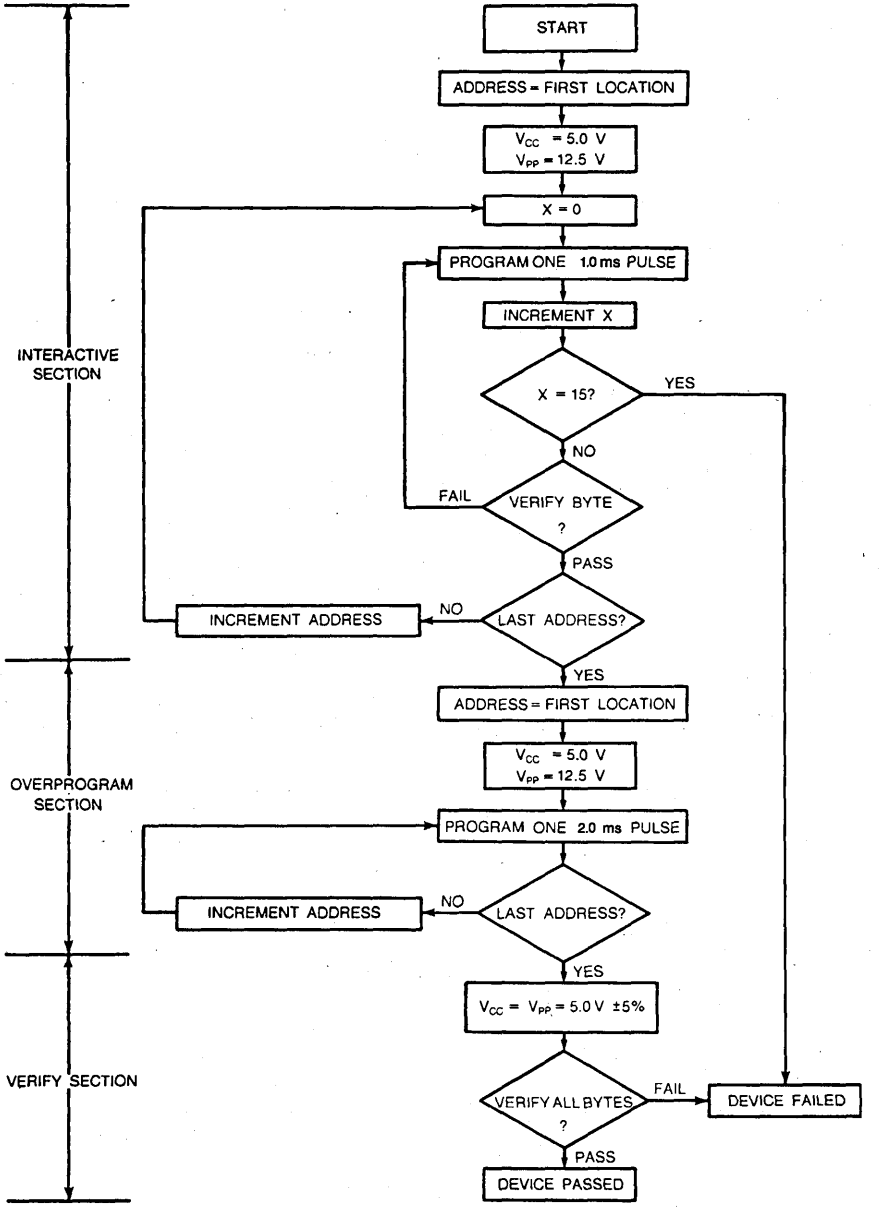


Figure 1. Interactive Programming Flow Chart

TABLE 4. IDENTIFIER BYTES

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am2716B Device Code	V_{IH}	1	0	0	0	0	1	1	0	86
Am2732B Device Code	V_{IH}	0	0	0	0	0	1	1	1	07

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. All other Address Lines = $\overline{CE} = \overline{OE} = V_{IL}$

INTERACTIVE PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

(Notes 1, 2, and 4)

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Units
I_{LI}	Input Current (All Inputs)		$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)			−0.1	0.8	V
V_{IH}	Input HIGH Level			2.0	$V_{CC} + 1$	V
V_{OL}	Output LOW Voltage during Verify		$I_{OL} = 2.1$ mA		.45	V
V_{OH}	Output LOW Voltage during Verify		$I_{OH} = -400$ μA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)	For Am2716B and Am2732B			100	mA
I_{PP1}	V_{PP} Supply Current (Program)		$V_{PP} = 5.5$ V		30	mA
V_{ID}	A_9 Auto-Select Voltage			11.5	12.5	V

Notes: See notes following the Interactive Programming Algorithm Switching Programming Characteristics table.

INTERACTIVE PROGRAMMING ALGORITHM SWITCHING PROGRAMMING CHARACTERISTICS

(Notes 1, 2, 3, and 4)

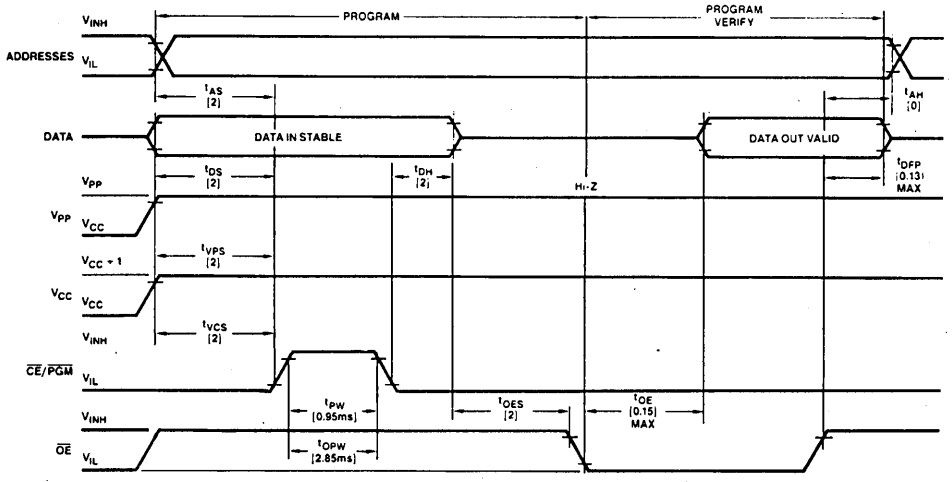
No.	Parameter Symbols	Parameter Description	Min.	Max.	Units
1	t_{AS}	Address Setup Time	2		μs
2	t_{OES}	$\overline{OE}$ Setup Time	2		μs
3	t_{DS}	Data Setup Time	2		μs
4	t_{AH}	Address Hold Time	2		μs
5	t_{DH}	Data Hold Time	2		μs
6	t_{DF}	Chip Enable to Output Float Delay	0	130	μs
7	t_{VPS}	V_{PP} Setup Time	2.0		μs
8	t_{VCS}	V_{CC} Setup Time	2		μs
9	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	.95	1.05	ms
10	t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width (Note 3)	1.9	55	ms
11	t_{CES}	$\overline{CE}$ Setup Time	2		μs
12	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes: 1. $T_A = +25°C \pm 5°C$; $V_{CC} = 6.0\ V \pm 0.25\ V$; $V_{PP} = 12.0$ to 13.3 V.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming the EPROMs, a 0.1-μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are guidelines which must be followed. They are not 100% tested to worst-case limits.

INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

AM2716B

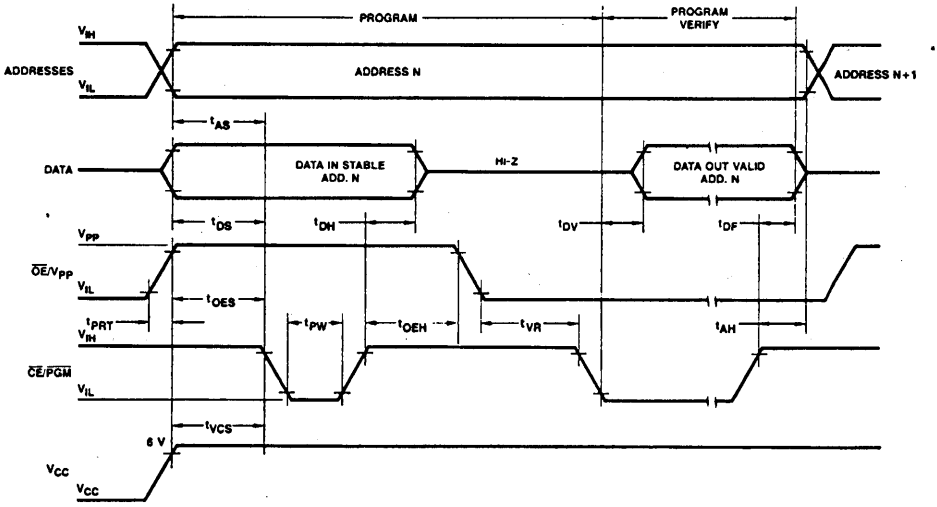
(Notes 1 and 3)



WF000583

Am2732B

(Notes 1 and 2)



WF001331

Notes: 1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DF} are characteristics of the device, but must be accommodated by the programmer.
3. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

6

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups*
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{PP1}	1, 2, 3
I_{PP2}	1, 2, 3
C_{IN}	4
C_{OUT}	4
C_{IN2}	4
C_{IN3}	4

*For DC Programming Characteristics, only Subgroup 1 applies.

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11
2	t_{CE}	9, 10, 11
3	t_{OE}	9, 10, 11
4	t_{DF}	9
5	t_{OH}	9

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

8-BIT EPROM FAMILY

(Am2764A, Am27128A, Am27256, Am27512)

DISTINCTIVE CHARACTERISTICS

- Fast access times — as low as 150 ns
- Low-power dissipation
- Programming voltage — 12.5 V
- Single +5-V power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available

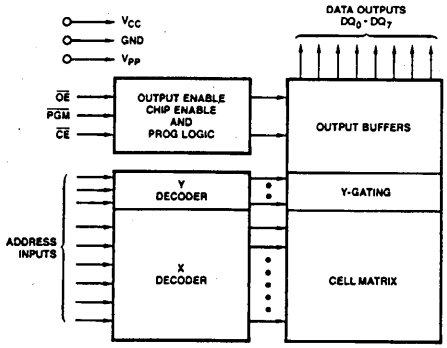
GENERAL DESCRIPTION

The Am2764A, Am27128A, Am27256, and the Am27512 are ultraviolet Erasable Programmable Read-Only Memories (EPROMs) and are organized as 8 bits per word. All standard EPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any Wait states. Some of AMD's EPROMs have access times of as fast as 150 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD EPROMs offer separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's EPROMs may be programmed using 1-ms pulses.

BLOCK DIAGRAM



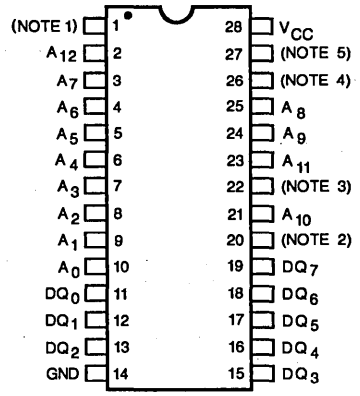
BD000231

PRODUCT SELECTOR GUIDE

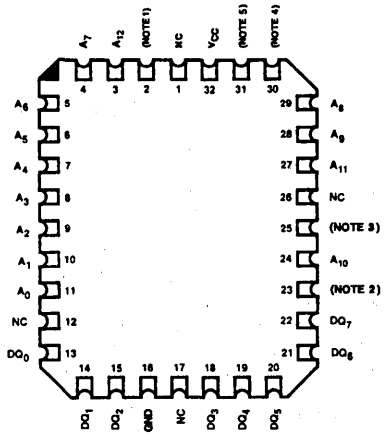
Family Part No.	Am2764A, Am27128A, Am27256, Am27512					
Ordering Part No.:						
±5% V_{CC} Tolerance	2764A-1 27128A-1 — —	— — 27256-1 —	2764A-2 27128A-2 27256-2 —	2764A 27128A 27256 27512	2764A-3 27128A-3 27256-3 27512-3	2764A-4 27128A-4 27256-4 27512-4
±10% V_{CC} Tolerance	2764A-15 27128A-15 — —	— — 27256-17 —	2764A-20 27128A-20 27256-20 —	2764A-25 27128A-25 27256-25 27512-25	2764A-30 27128A-30 27256-30 27512-30	2764A-45 27128A-45 27256-45 27512-45
t_{ACC} (ns)	150	170	200	250	300	450
t_{CE} (ns)	150	170	200	250	300	450
t_{OE} (ns)	75	75	75	100	110	150

Publication # 08005 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD009420

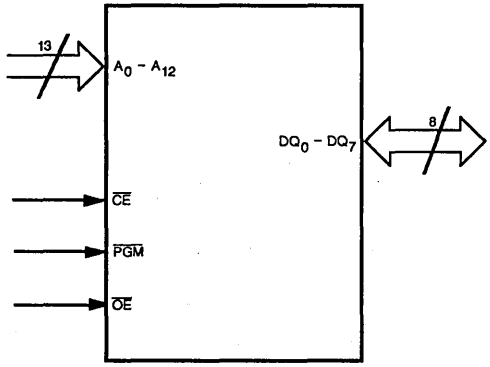


CD009710

Notes:		AM2764A	AM27128A	AM27256	AM27512
	1	V_{PP}	V_{PP}	V_{PP}	A_{15}
	2	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
	3	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
	4	NC	A_{13}	A_{13}	A_{13}
	5	$\overline{PGM}$	$\overline{PGM}$	A_{14}	A_{14}

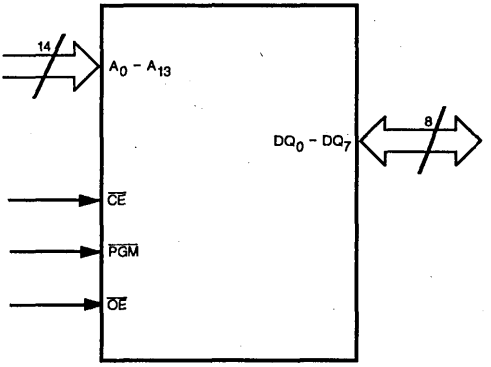
LOGIC SYMBOL

Am2764A



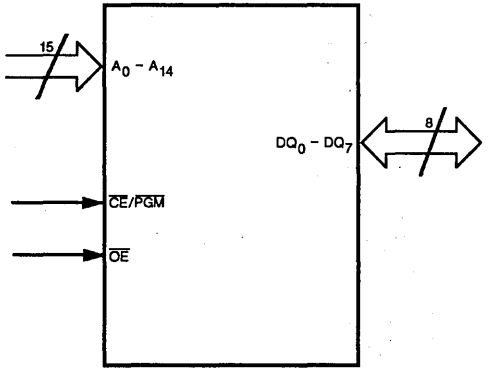
LS002360

Am27128A



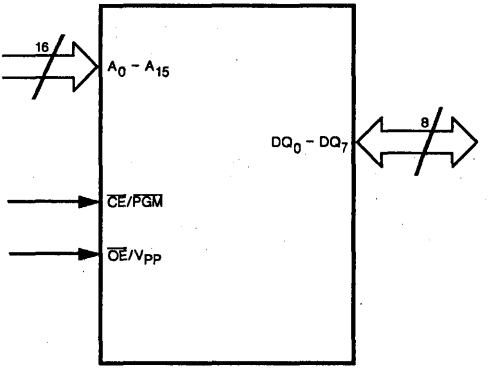
LS002370

Am27256



LS002520

Am27512

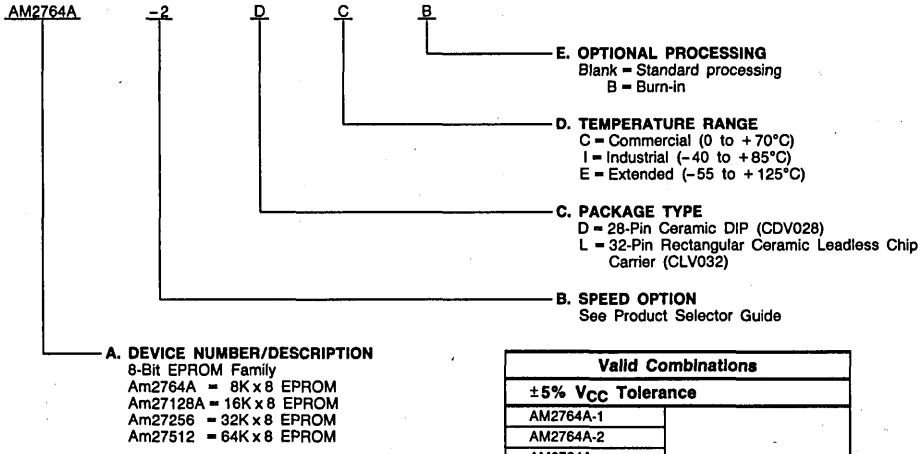


LS002530

ORDERING INFORMATION (Cont'd.)
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations

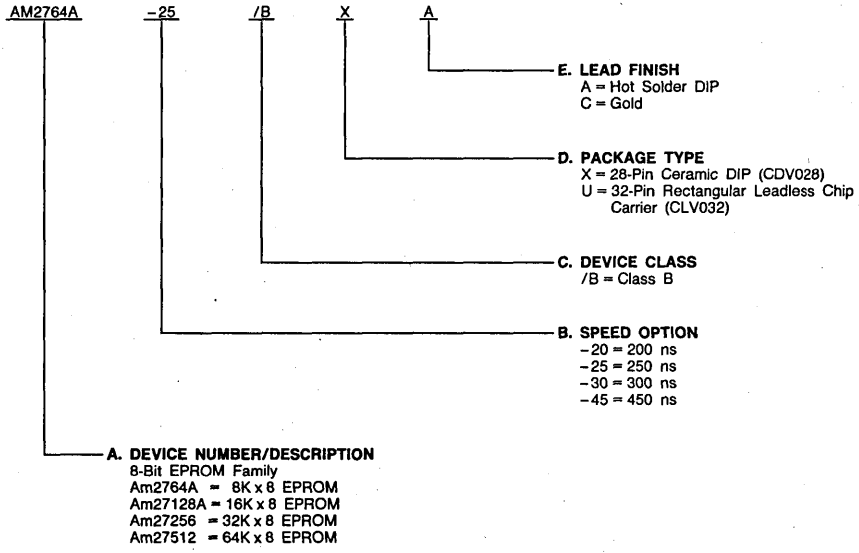
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
±5% V_{CC} Tolerance	
AM2764A-1	DC, DCB, DI, DIB, LC, LCB, LE, LEB
AM2764A-2	
AM2764A	
AM2764A-3	
AM2764A-4	
AM27128A-1	
AM27128A-2	
AM27128A	
AM27128A-3	
AM27128A-4	
AM27256-1	
AM27256-2	
AM27256	
AM27256-3	
AM27256-4	
AM27512	
AM27512-3	
AM27512-4	
±10% V_{CC} Tolerance	
AM2764A-15	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2764A-20	
AM2764A-25	
AM2764A-30	
AM2764A-45	
AM27128A-15	
AM27128A-20	
AM27128A-25	
AM27128A-30	
AM27128A-45	
AM27256-17	
AM27256-20	
AM27256-25	
AM27256-30	
AM27256-45	
AM27512-25	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB
AM27512-30	
AM27512-45	

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
±10% V_{CC} Tolerance	
AM2764A-20	/BXA, /BUA /BUC
AM2764A-25	
AM2764A-30	
AM2764A-45	
AM27128A-20	
AM27128A-25	
AM27128A-30	
AM27128A-45	
AM27256-20	
AM27256-25	
AM27256-30	
AM27256-45	
AM27512-30	/BXA
AM27512-45	

6

FUNCTIONAL DESCRIPTION

Erasing the 8-Bit EPROMs

In order to clear all locations of their programmed contents, it is necessary to expose the EPROMs to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for fifteen to twenty minutes. The EPROM should be about directly under and about one inch from the source and all filters should be removed from the ultraviolet light source prior to erasure.

It is important to note that the EPROMs will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with ultraviolet sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the EPROMs and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the 8-Bit EPROMs

Upon delivery, or after each erasure, the EPROM has all bits in the "1", or HIGH state. Zeros ("0s") are loaded into the EPROM through the procedure of programming.

The programming mode is entered when a voltage greater than 12.0, but less than 13.3 V is applied to the V_{PP} pin ($\overline{OE}/V_{PP}$ for 512K) and $\overline{PGM}$ ($\overline{CE}/\overline{PGM}$ for 256K and 512K) is LOW. The data to be programmed is applied 8 bits in parallel to the Data I/O (DQ_n) pins.

The flowchart (Figure 1) in the Programming section of this document shows the AMD-preferred interactive programming algorithm. Interactive algorithms requires less programming time than most other algorithms. This does not preclude the use of other algorithms, including the conventional 50-ms pulse, as long as the maximum specifications are not violated.

The AMD-preferred algorithm reduces programming time by using short (1 ms) program pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 15 pulses. This process is repeated while sequencing through each address of the EPROM. The interactive section of the algorithm is programmed and verified at V_{CC} = 6.0 V, ±5%.

The overprogram section of the algorithm programs the entire array by cycling through each address and applying an additional 2-ms program pulse. This section is done at V_{CC} = 5.0 V, ±5%.

After the final address is completed, the entire EPROM is verified to the data-sheet specifications of V_{CC} = 5.0 V, ±5%.

Auto Select Mode

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient-temperature range required when programming the EPROMs.

To activate this mode, the programming equipment must force 12.0 V ±0.5 V on address line A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select mode.

Byte 0 ($A_0 = V_{IL}$, $DQ_0 - DQ_7$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$, $DQ_0 - DQ_7$), the device identifier code. These identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the most significant bit (MSB), DQ_7, defined as the parity bit.

Read Mode

AMD EPROMs have two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

AMD EPROMs have a standby mode which reduces the active power dissipation up to 80%. The EPROM is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for: 1) low-memory power dissipation, and 2) assurance that output-bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array, and connected to the Read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ or $\overline{PGM}$, all like inputs (including $\overline{OE}$ and V_{PP}) of the parallel EPROMs may be common. A TTL LOW-level program pulse applied to the $\overline{PGM}$ ($\overline{CE}/\overline{PGM}$ for 256K and 512K) input with V_{PP} between 12.0 and 13.3 V and $\overline{CE}$ LOW, will program that EPROM. A HIGH-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed.

Data for all the EPROMs should be verified t_{OE} after the falling edge of $\overline{OE}$, V_{PP} must be between 12.0 V and 13.3 V for all EPROMs except the Am27512 which requires $\overline{OE}/V_{PP}$ to be at V_{IL}.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these

transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit-board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

FUNCTION TABLES

TABLE 1. Am2764A and 27128A MODE SELECT

PINS / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	V_{PP}	OUTPUTS
Read	L	L	H	X	V_{CC}	D_{OUT}
Output Disable	L	H	H	X	V_{CC}	Hi-Z
Standby	H	X	X	X	V_{CC}	Hi-Z
Program	L	X	L	X	V_{PP}	D_{IN}
Program Verify	L	L	H	X	V_{PP}	D_{OUT}
Program Inhibit	H	X	X	X	V_{PP}	Hi-Z
Auto Select	L	L	H	V_H	V_{CC}	Code

TABLE 2. Am27256 MODE SELECT

PINS / MODE	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$	A_9	V_{PP}	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output Disable	L	H	X	V_{CC}	Hi-Z
Standby	H	X	X	V_{CC}	Hi-Z
Program	L	H	X	V_{PP}	D_{IN}
Program Verify	H	L	X	V_{PP}	D_{OUT}
Program Inhibit	H	H	X	V_{PP}	Hi-Z
Auto Select	L	L	V_H	V_{CC}	Code

TABLE 3. Am27512 MODE SELECT

PINS / MODE	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$/V_{PP}	A_9	OUTPUTS
Read	L	L	X	D_{OUT}
Output Disable	L	H	X	Hi-Z
Standby	H	X	X	Hi-Z
Program	L	V_{PP}	X	D_{IN}
Program Verify	L	L	X	D_{OUT}
Program Inhibit	H	V_{PP}	X	Hi-Z
Auto Select	L	L	V_H	Code

Key: L = LOW
H = HIGH
X = Can be either LOW or HIGH
V_H = 12.0 V ±0.5 V

6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Supply Voltage
with respect to Ground
on all Inputs except A_9 and V_{PP} .....+6.25 to −0.6 V
on A_9 ..... +13.50 to −0.6 V
on V_{PP} ..... +13.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −1, −2, blank, −3, and −4 versions, V_{CC} = +4.75 to +5.25 V.
2. For −15, −17, −20, −25, −30, and −45 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, & 4)*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1	V
V_{IL}	Input LOW Voltage			−0.1	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 to +5.5 V			10.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to −5.5 V			10.0	μA
I_{CC1}	V_{CC} Standby Current (Note 6)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		25	mA
			E/M Devices		40	
I_{CC2}	V_{CC} Active Current for Am2764A	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	C/I Devices		75	mA
			E/M Devices		100	
	V_{CC} Active Current for Am27128A and Am27256		C, I, E & M Devices		100	
	V_{CC} Active Current for Am27512		C/I Devices		100	
			E/M Devices		120	
I_{PP1}	V_{PP} Read Current (except Am27512) (Notes 1 & 5)	V_{PP} = 5.5 V	C, I, E, & M Devices		5	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Read Current for Am27512 (Note 5)	$\overline{OE}/V_{PP}$ = 5.5 V	C, I, E, & M Devices		10	mA

Notes: See notes following the Capacitance table on next page.

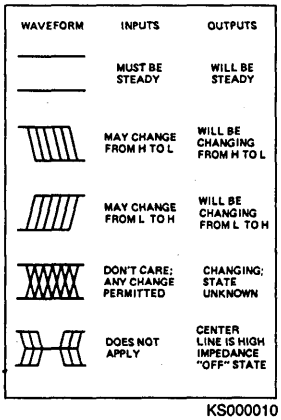
*See the last page of this spec for Group A Subgroup Testing information.

CAPACITANCE (Notes 2 & 3)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF
C_{IN2}	Am27512 $\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0 V	12	20	pF
C_{IN3}	Am27512 $\overline{CE}/\overline{PGM}$ Input Capacitance		9	12	

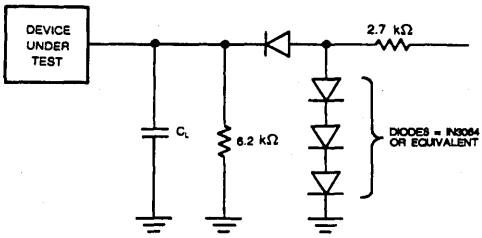
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The EPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. V_{PP} may be connected to V_{CC} directly except during programming. The supply would then be the sum of I_{CC} and I_{PP}.
6. I_{CC1} Max. is 40 mA for −4 and −45 devices.

KEY TO SWITCHING WAVEFORMS



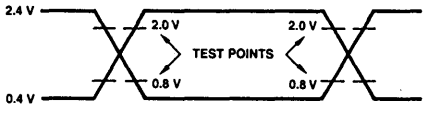
KS000010

SWITCHING TEST CIRCUITS



TC003191

SWITCHING TEST WAVEFORMS



WF009500

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤20 ns.

6

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Notes 1 & 3)

(Table 1 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	-1, -15		-1, -17**		-2, -20		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		170		200	ns
2	t_{CE}	Chip Enable to Output Delay			150		170		200	ns
3	t_{OE}	Output Enable to Output Delay			75		75		75	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	60	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

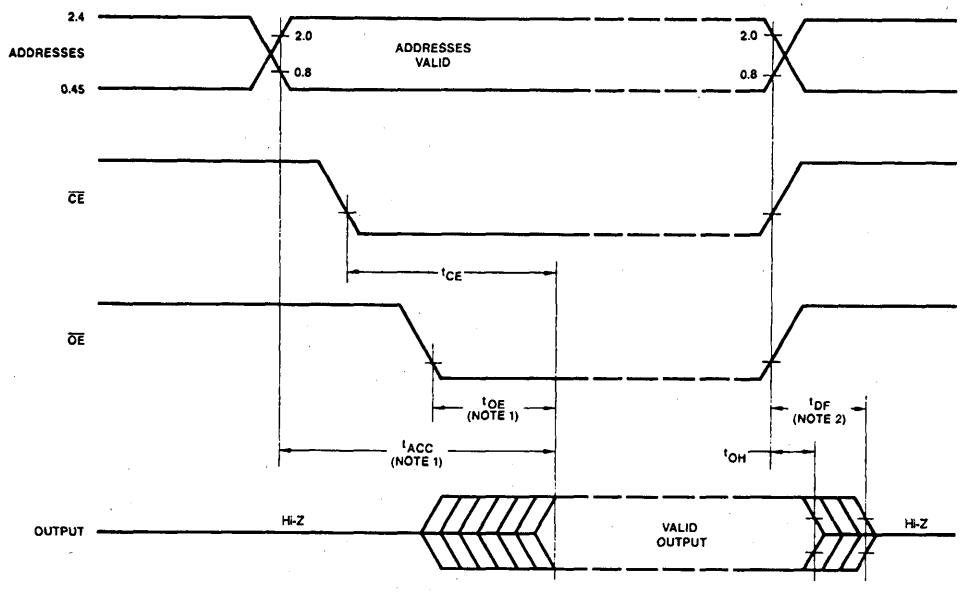
(Table 2 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	Blank, -25		-3, -30		-4, -45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		250		300		450	ns
2	t_{CE}	Chip Enable to Output Delay			250		300		450	ns
3	t_{OE}	Output Enable to Output Delay			100		120		150	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	80	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. Caution: The AMD 8-bit EPROM Family must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C_L = 100$ pF,
Input Rise and Fall Times: ≤ 20 ns,
Input Pulse Levels: 0.45 to 2.4 V,
Timing Measurement Reference Level — Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V.

*See the last page of this spec for Group A Subgroup Testing information.
**for Am27256 only.

SWITCHING WAVEFORMS



WF021980

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

6

PROGRAMMING

This section covers Identifier bytes, Interactive Programming Flowchart, and Interactive Programming DC and AC Switching Programming Characteristics.

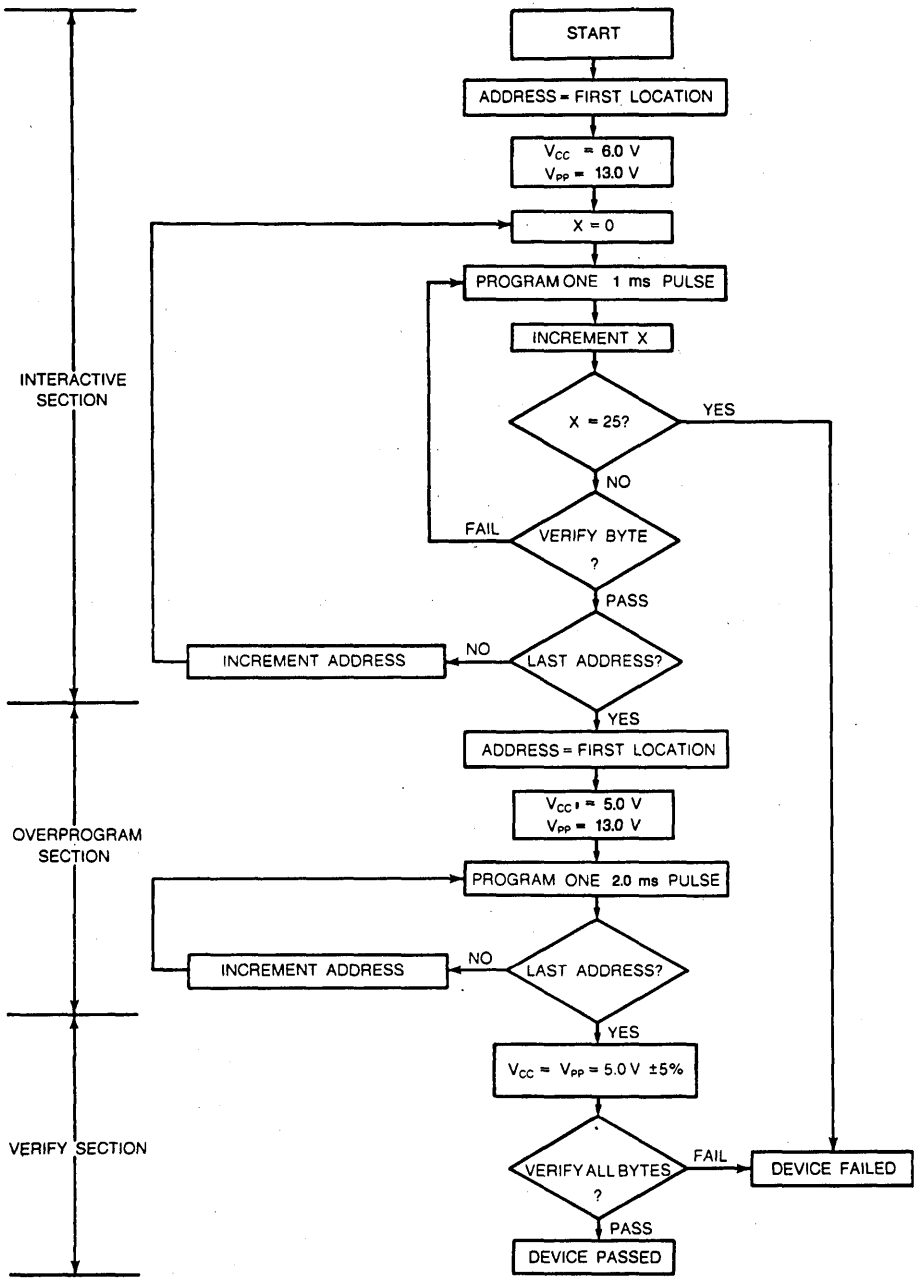


Figure 1. Interactive Programming Flow Chart

TABLE 4. IDENTIFIER BYTES

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am2764A Device Code	V_{IH}	0	0	0	0	1	0	0	0	08
Am27128A Device Code	V_{IH}	1	0	0	0	1	0	0	1	89
Am27256 Device Code	V_{IH}	0	0	0	0	0	1	0	0	04
Am27512 Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. All other Address Lines = $\overline{CE} = \overline{OE} = V_{IL}$
3. For Am2764A, $\overline{PGM} = V_{IH}$
4. For Am27256 and Am27512, A_{14} = Don't Care

INTERACTIVE PROGRAMMING ALGORITHM DC CHARACTERISTICS

(Notes 1, 2, and 4)

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Units
I_{LI}	Input Current (All Inputs)		$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)			−0.1	0.8	V
V_{IH}	Input HIGH Level			2.0	$V_{CC} + 1$	V
V_{OL}	Output LOW Voltage during Verify		$I_{OL} = 2.1$ mA		.45	V
V_{OH}	Output LOW Voltage during Verify		$I_{OH} = -400$ μA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)	For Am2764A			75	mA
		For Am27128A and Am27256			100	
		For Am27512			150	
I_{PP3}	V_{PP} Supply Current (Program)		$\overline{CE} = V_{IL} = \overline{PGM} = \overline{CE}/\overline{PGM}$		30	mA
V_{ID}	A_9 Auto-Select Voltage			11.5	12.5	V

Notes: See notes following the Interactive Programming Algorithm Switching Programming Characteristics table on next page.

INTERACTIVE PROGRAMMING ALGORITHM AC SWITCHING PROGRAMMING CHARACTERISTICS

(Notes 1, 2, 3, and 4)

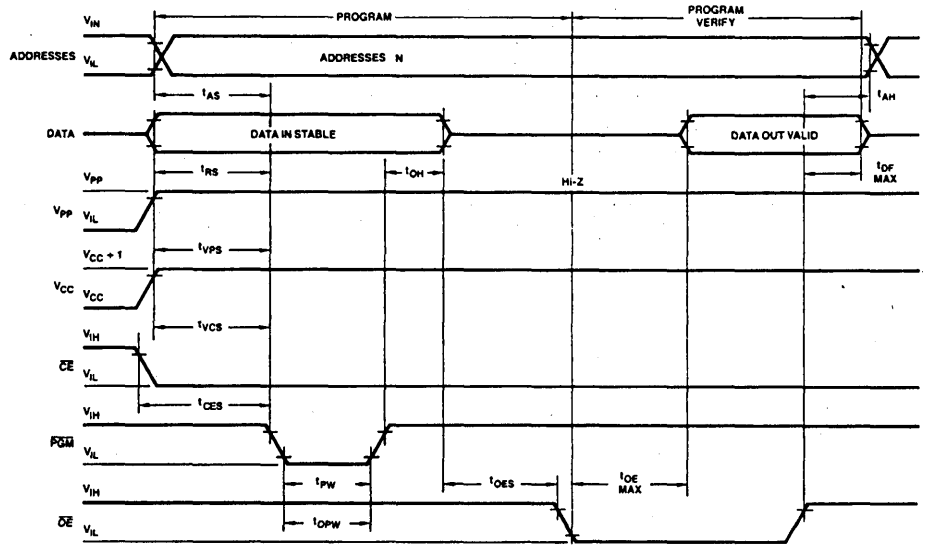
No.	Parameter Symbols	Parameter Description	Min.	Max.	Units
1	t_{AS}	Address Setup Time	2		μs
2	t_{OES}	$\overline{OE}$ Setup Time	2		μs
3	t_{DS}	Data Setup Time	2		μs
4	t_{AH}	Address Hold Time	2		μs
5	t_{DH}	Data Hold Time	2		μs
6	t_{DF}	Chip Enable to Output Float Delay	0	130	μs
7	t_{VPS}	V_{PP} Setup Time	2.0		μs
8	t_{VCS}	V_{CC} Setup Time	2		μs
9	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	.95	1.05	ms
10	t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width (Note 3)	1.95	78.75	ms
11	t_{CES}	$\overline{CE}$ Setup Time	2		μs
12	t_{OE}	Data Valid from $\overline{OE}$		150	ns
13	t_{DV}	Am27512 Data Valid from $\overline{CE}$		450	ns

Notes: 1. $T_A = +25°C \pm 5°C$; $V_{CC} = 6.0\ V \pm 0.25\ V$; $V_{PP} = 12.0$ to $13.3\ V$.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming the EPROM family, a 0.1-μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are guidelines which must be followed. They are not 100% tested to worst-case limits.

INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS (Cont'd.)

Am2764A and Am27128A

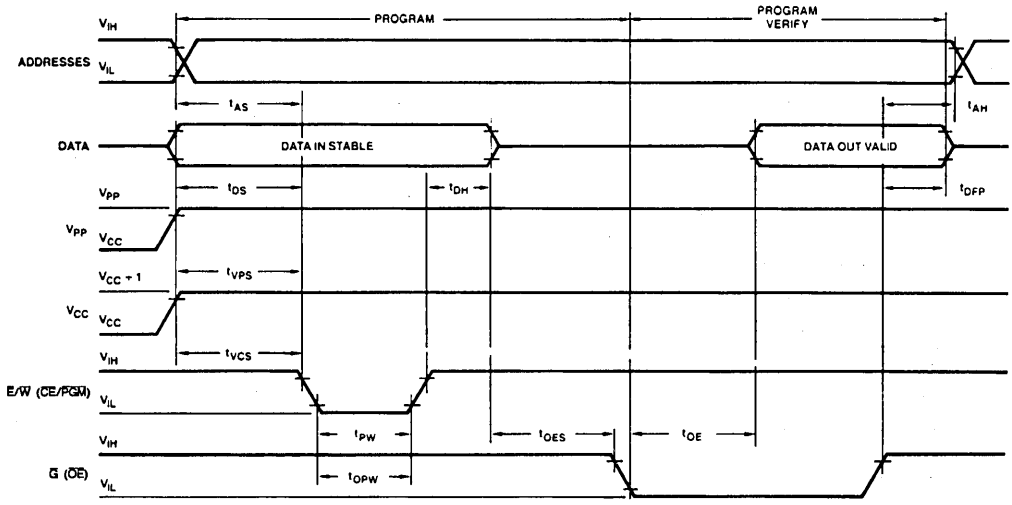
(Notes 1 and 2)



WF000552

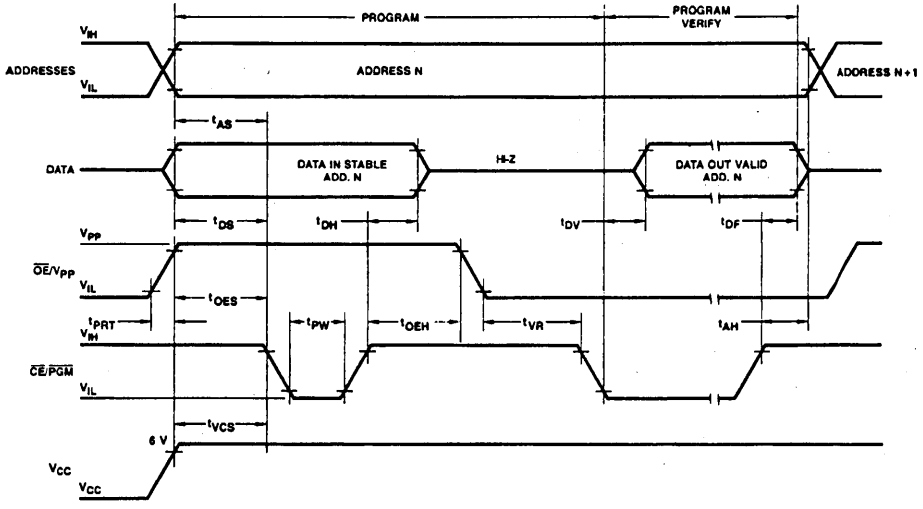
Notes: See notes following the Am27512 Waveform on next page.

Am27256
(Notes 1 and 3)



WF000582

Am27512
(Notes 1 and 2)



WF021990

Notes: 1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DF} are characteristics of the device, but must be accommodated by the programmer.
3. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

6

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups*
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{PP1}	1, 2, 3
I_{PP2}	1, 2, 3
C_{IN}	4
C_{OUT}	4
C_{IN2}	4
C_{IN3}	4

*For DC Programming Characteristics, only Subgroup 1 applies.

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11
2	t_{CE}	9, 10, 11
3	t_{OE}	9, 10, 11
4	t_{DF}	9
5	t_{OH}	9

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

8-BIT OTPROM FAMILY

(Am2764A, Am27128A, Am27256)

DISTINCTIVE CHARACTERISTICS

- Fast access times — as low as 200 ns
- Low-power dissipation
- Both interactive and new Flashrite* programming algorithms available
- Single +5-V power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available
- Programming voltage—12.5 V

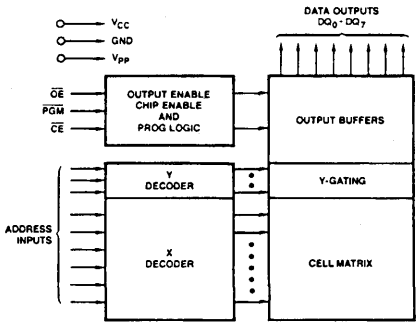
GENERAL DESCRIPTION

The Am2764A, Am27128A, and the Am27256 are One-Time Programmable Read-Only Memories (OTPROMs) and are organized as 8 bits per word. The plastic OTPROMs are ideal for volume production. First, because they can be inventoried unprogrammed and used with current-level software revisions; second, there is no window to be covered to prevent light from changing data —this could eliminate a manufacturing step and increase the reliability of the system; and third, they are compatible with auto insertion equipment. All standard OTPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any Wait states. Some of AMD's OTPROMs have access times of as fast as 200 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD OTPROMs offer separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's OTPROMs may be programmed using the Flashrite programming algorithm, which offers several fold improvement in programming time.

BLOCK DIAGRAM



BD000231

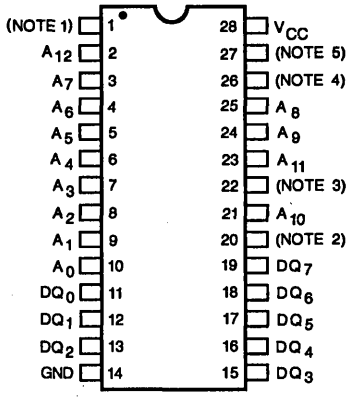
PRODUCT SELECTOR GUIDE

Family Part No.	Am2764A, Am27128A, Am27256		
Ordering Part No.:			
±5% V_{CC} Tolerance	2764A-2 27128A-2 27256-2	2764A 27128A 27256	2764A-4 27128A-4 27256-4
±10% V_{CC} Tolerance	2764A-20 27128A-20 27256-20	2764A-25 27128A-25 27256-25	— — —
t_{ACC} (ns)	200	250	450
t_{CE} (ns)	200	250	450
t_{OE} (ns)	75	100	150

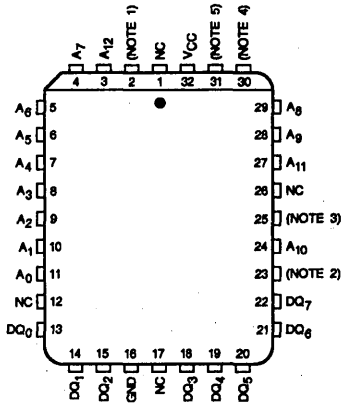
*Flashrite is a trademark of Advanced Micro Devices, Inc.

Publication # 08159 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



CD009420



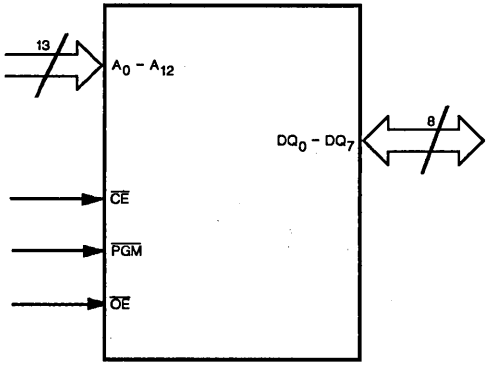
CD009770

Notes:

	Am2764A	Am27128A	Am27256
1	V_{PP}	V_{PP}	V_{PP}
2	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$
3	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
4	NC	A_{13}	A_{13}
5	$\overline{PGM}$	$\overline{PGM}$	A_{14}

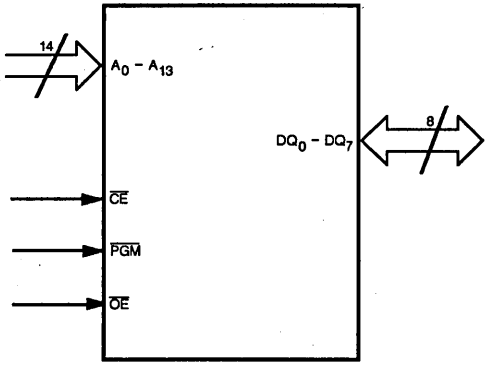
LOGIC SYMBOLS

Am2764A



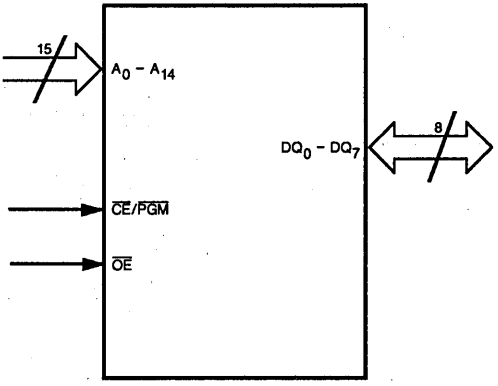
LS002360

Am27128A



LS002370

Am27256



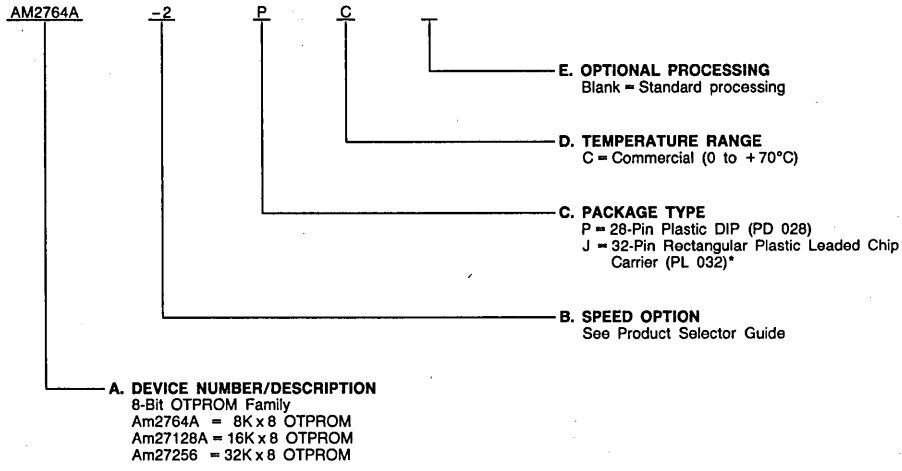
LS002380

6

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*Preliminary. Subject to Change.

Valid Combinations	
±5% V_{CC} Tolerance	
AM2764A-2	PC, JC
AM2764A	
AM2764A-4	
AM27128A-2	
AM27128A	
AM27128A-4	
AM27256-2	
AM27256	
AM27256-4	
±10% V_{CC} Tolerance	
AM2764A-20	PC, JC
AM2764A-25	
AM27128A-20	
AM27128A-25	
AM27256-20	
AM27256-25	

FUNCTIONAL DESCRIPTION

Programming the 8-Bit OTPROMs

Upon delivery, or after each erasure, the OTPROM has all bits in the "1", or HIGH state. Zeros ("0s") are loaded into the OTPROM through the procedure of programming.

The programming mode is entered when a voltage greater than 12.0, but less than 13.3 V, is applied to the V_{PP} pin and $\overline{PGM}$ ($\overline{CE}/\overline{PGM}$ for 256K) is low. The data to be programmed is applied 8 bits in parallel to the Data I/O (DQ_n) pins.

The flowcharts (Figures 1 and 2) show AMD's Flashrite programming and interactive programming algorithms. The Flashrite programming algorithm improves the programming time by several folds as compared to the interactive algorithm.

The AMD Flashrite programming algorithm reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTPROM.

The Flashrite programming algorithm is programmed and verified at V_{CC} = 6.25 V and V_{PP} = 13.0 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

In addition to the Flashrite programming algorithm, OTPROMs are also compatible with AMD's interactive programming algorithm (see Figure 1).

The programming mode is entered when a voltage greater than 12.0 V but less than 13.3 V is applied to the V_{PP} pin.

The AMD interactive algorithm uses short (1 ms) program pulses by giving each address only as many pulses as necessary to program the data. After each pulse is applied to a given address, data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTPROM. Programming and verification are done at V_{CC} = 6.0 V ±5%.

The overprogram section of the algorithm programs the entire array by cycling through each address and applying an additional 2-ms program pulse. This section is done at V_{CC} = 5.0 V ±5%.

After the final address is completed, the entire OTPROM is verified at V_{CC} = 5.0 V ±5%.

Auto Select Mode

The Auto Select mode allows the reading out of a binary code from an OTPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient-temperature range required when programming the OTPROMs.

To activate this mode, the programming equipment must force 12.0 V to ±0.5 V on address line A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select mode.

Byte 0 ($A_0 = V_{IL}$, $DQ_0 - DQ_7$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$, $DQ_0 - DQ_7$), the device identifier code. These identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the most significant bit (MSB), DQ_7, defined as the parity bit.

Read Mode

AMD OTPROMs have two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

AMD OTPROMs have a standby mode which reduces the active power dissipation up to 80%. The OTPROM is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for: 1) low-memory power dissipation, and 2) assurance that output-bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array, and connected to the Read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Program Inhibit

Programming of multiple OTPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ or $\overline{PGM}$, all like inputs (including $\overline{OE}$ and V_{PP}) of the parallel OTPROMs may be common. A TTL LOW-level program pulse applied to the $\overline{PGM}$ ($\overline{CE}/\overline{PGM}$ for 256K) input with V_{PP} between 12.75 V and 13.25 V and $\overline{CE}$ LOW, will program that OTPROM. A HIGH-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other OTPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed.

Data for all the OTPROMs should be verified t_{OE} after the falling edge of $\overline{OE}$, V_{PP} must be between 12.75 V and 13.25 V for all OTPROMs.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit-board traces on OTPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

FUNCTION TABLES

TABLE 1. Am2764A and 27128A MODE SELECT

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	V_{PP}	OUTPUTS
Read	L	L	H	X	V_{CC}	D_{OUT}
Output Disable	L	H	H	X	V_{CC}	Hi-Z
Standby	H	X	X	X	V_{CC}	Hi-Z
Program	L	X	L	X	V_{PP}	D_{IN}
Program Verify	L	L	H	X	V_{PP}	D_{OUT}
Program Inhibit	H	X	X	X	V_{PP}	Hi-Z
Auto Select	L	L	H	V_H	V_{CC}	Code

TABLE 2. Am27256 MODE SELECT

MODE \ PINS	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$	A_9	V_{PP}	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output Disable	L	H	X	V_{CC}	Hi-Z
Standby	H	X	X	V_{CC}	Hi-Z
Program	L	H	X	V_{PP}	D_{IN}
Program Verify	H	L	X	V_{PP}	D_{OUT}
Program Inhibit	H	H	X	V_{PP}	Hi-Z
Auto Select	L	L	V_H	V_{CC}	Code

Key: L = LOW
H = HIGH
X = Can be either LOW or HIGH
V_H = 12.0 V ±0.5 V

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Supply Voltage
with respect to Ground
on all Inputs except A_9 and V_{PP} ..... +6.50 to −0.6 V
on A_9 ..... +13.50 to −0.6 V
on V_{PP} ..... +13.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −2, blank, and −4 versions, V_{CC} = +4.75 to +5.25 V.
2. For −20 and −25 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, & 4)*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 1	V
V_{IL}	Input LOW Voltage		−0.1	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 to +5.5 V		10.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to −5.5 V		10.0	μA
I_{CC1}	V_{CC} Standby Current (Note 6)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}		25	mA
I_{CC2}	V_{CC} Active Current for Am2764A	$\overline{OE}$ = $\overline{CE}$ = V_{IL}		75	mA
	V_{CC} Active Current for Am27128A and Am27256			100	
I_{PP1}	V_{PP} Read Current (Notes 1 & 5)	V_{PP} = 5.5 V		5	mA

Notes: See notes following the Capacitance table on next page.

*See the last page of this spec for Group A Subgroup Testing information.

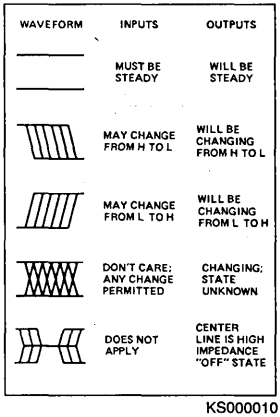
6

CAPACITANCE (Notes 2 & 3)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0$ V	4	7	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$ V	8	12	pF

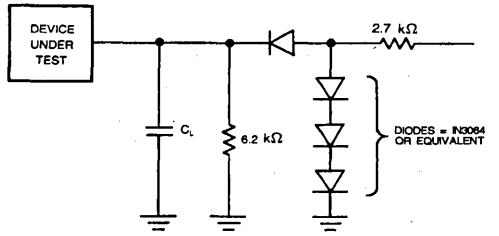
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The OTPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. V_{PP} may be connected to V_{CC} directly except during programming. The supply would then be the sum of I_{CC} and I_{PP}.
6. I_{CC1} Max. is 40 mA for −4 devices.

KEY TO SWITCHING WAVEFORMS



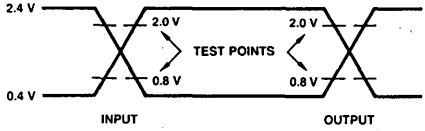
KS000010

SWITCHING TEST CIRCUITS



TC003191

SWITCHING TEST WAVEFORMS



WF009500

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤20 ns.

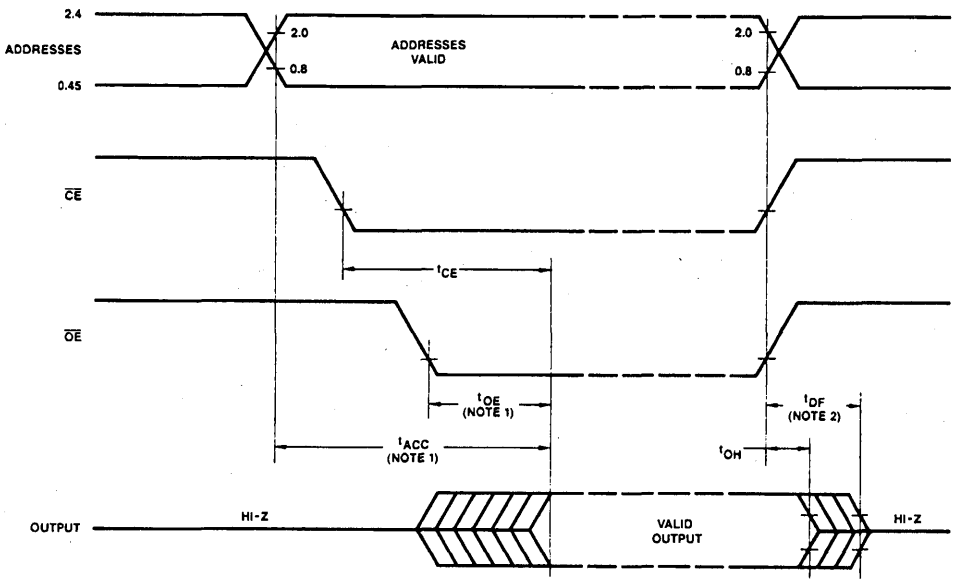
SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Notes 1 & 3)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	-2, -20		Blank, -25		-4		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		450	ns
2	t_{CE}	Chip Enable to Output Delay			200		250		450	ns
3	t_{OE}	Output Enable to Output Delay			75		100		150	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	80	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. Caution: The AMD 8-bit OTPROM Family must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C_L = 100$ pF,
Input Rise and Fall Times: ≤ 20 ns,
Input Pulse Levels: 0.45 to 2.4 V,
Timing Measurement Reference Level — Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



WF001321

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

6

PROGRAMMING

This section covers Identifier bytes, Interactive Programming Flowchart, and Programming DC and AC Switching Programming Characteristics.

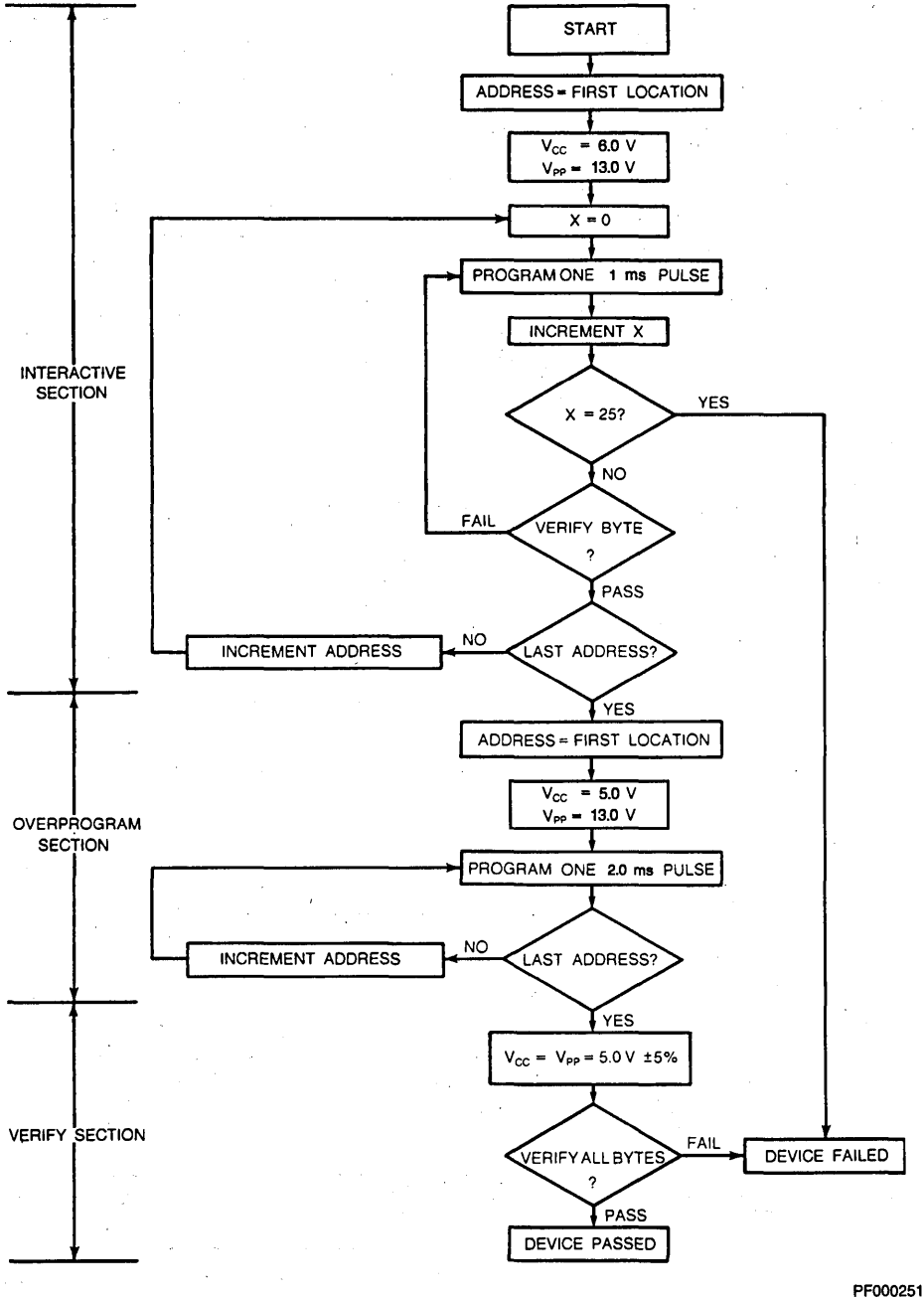


Figure 1. Interactive Programming Flow Chart

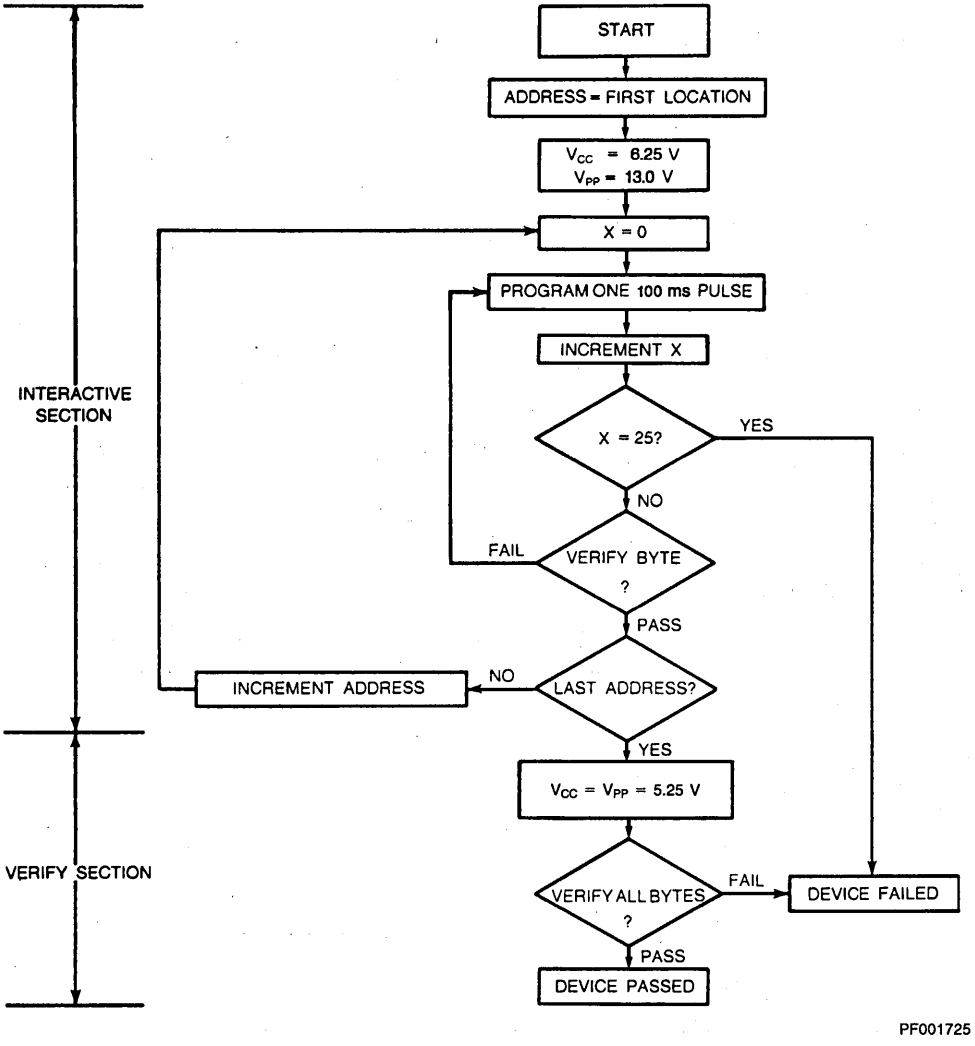


Figure 2. Flashrite Programming Flow Chart

TABLE 3. IDENTIFIER BYTES

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am2764A Device Code	V_{IH}	0	0	0	0	1	0	0	0	08
Am27128A Device Code	V_{IH}	1	0	0	0	1	0	0	1	89
Am27256 Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. All other Address Lines = $\overline{CE} = \overline{OE} = V_{IL}$
3. For Am2764A, $\overline{PGM} = V_{IH}$
4. For Am27256, A_{14} = Don't Care

INTERACTIVE PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Units
I_{LI}	Input Current (All Inputs)		$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)			−0.1	0.8	V
V_{IH}	Input HIGH Level			2.0	$V_{CC} + 1$	V
V_{OL}	Output LOW Voltage during Verify		$I_{OL} = 2.1$ mA		.45	V
V_{OH}	Output LOW Voltage during Verify		$I_{OH} = -400$ μA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)	For Am2764A			75	mA
		For Am27128A and Am27256			100	
I_{PP3}	V_{PP} Supply Current (Program)		$\overline{CE} = V_{IL} = \overline{PGM} = \overline{CE}/\overline{PGM}$		30	mA
V_{ID}	A_9 Auto-Select Voltage			11.5	12.5	V
V_{PP}	Interactive Programming Algorithm			12.0	13.3	V
	Flashrite Programming Algorithm			12.75	13.25	V
V_{CC}	Interactive Programming Algorithm			5.75	6.25	V
	Flashrite Programming Algorithm			6.0	6.5	V

PROGRAMMING AC CHARACTERISTICS

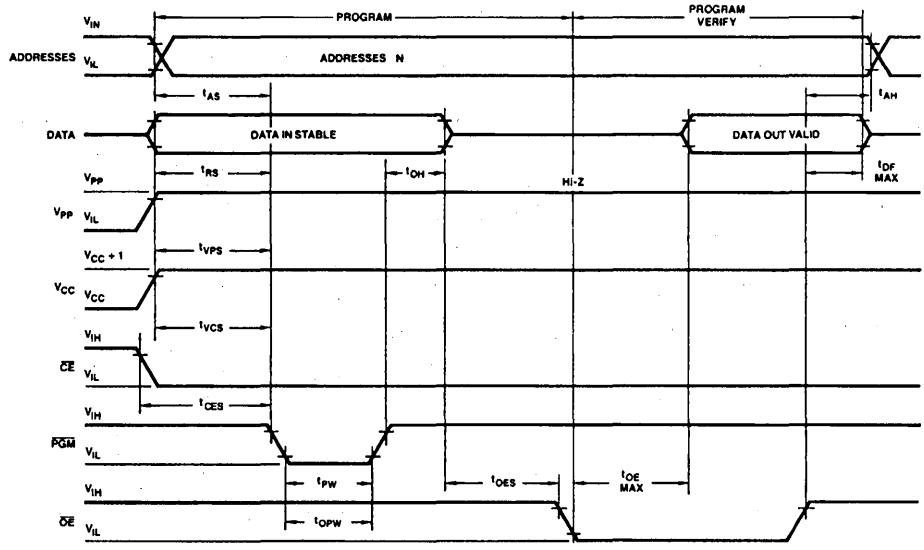
(Notes 1, 2, 3, and 4)

No.	Parameter Symbols	Parameter Description	Min.	Max.	Units
1	t_{AS}	Address Setup Time	2		μs
2	t_{OES}	$\overline{OE}$ Setup Time	2		μs
3	t_{DS}	Data Setup Time	2		μs
4	t_{AH}	Address Hold Time	2		μs
5	t_{DH}	Data Hold Time	2		μs
6	t_{DF}	Chip Enable to Output Float Delay	0	130	μs
7	t_{VPS}	V_{PP} Setup Time	2.0		μs
8	t_{VCS}	V_{CC} Setup Time	2		μs
9	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width (Interactive)	.95	1.05	ms
		$\overline{PGM}$ Initial Program Pulse Width (Flashrite)	95	105	μs
10	t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width (Note 3,5)	1.95	2.05	ms
11	t_{CES}	$\overline{CE}$ Setup Time	2		μs
12	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes: 1. $T_A = +25°C \pm 5°C$; see DC Programming Characteristics for V_{CC} and V_{PP} voltages.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming the OTPROM family, a 0.1-μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are guidelines which must be followed. They are not 100% tested to worst-case limits.
5. Interactive programming algorithm only.

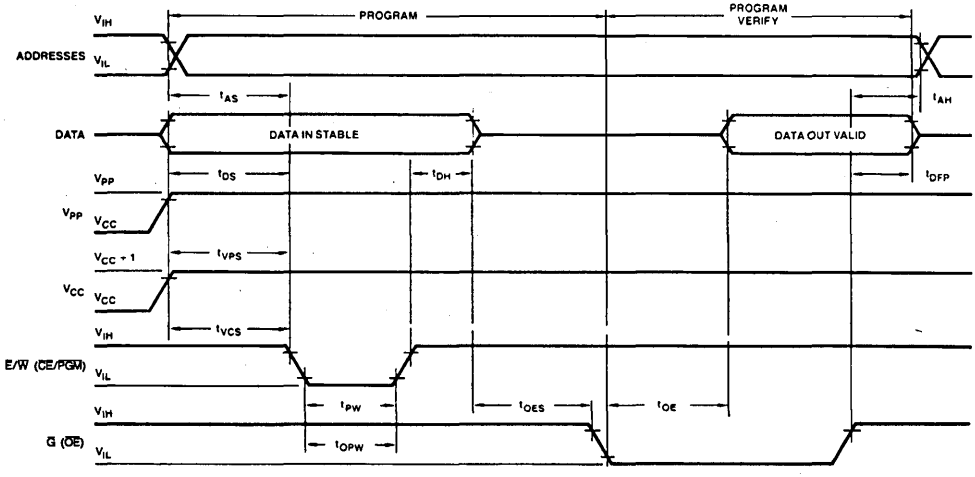
INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS

Am2764A and Am27128A
(Notes 1 and 2)



WF000552

Am27256
(Notes 1 and 3)



WF000582

Notes: 1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DF} are characteristics of the device, but must be accommodated by the programmer.
3. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups*
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{PP1}	1, 2, 3
I_{PP2}	1, 2, 3
C_{IN}	4
C_{OUT}	4
C_{IN2}	4
C_{IN3}	4

*For DC Programming Characteristics, only Subgroup 1 applies.

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11
2	t_{CE}	9, 10, 11
3	t_{OE}	9, 10, 11
4	t_{DF}	9
5	t_{OH}	9

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Am27C256

32,768 x 8-Bit CMOS EPROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time — 150 ns
- Low-power dissipation
- Both interactive and new Flashrite* programming algorithms available
- Single 5-volt power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available
- Programming voltage—12.5 V

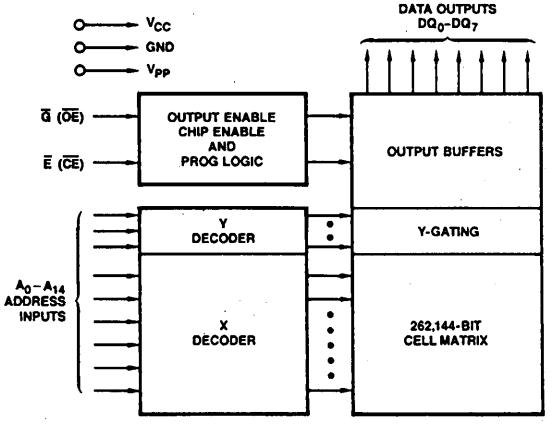
GENERAL DESCRIPTION

The Am27C256 is a CMOS ultraviolet Erasable Programmable Read-Only Memory (EPROM). It is organized as 32,768 x 8 bits per word. All AMD CMOS EPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any wait state. Some of AMD's EPROMs have access times of as fast as 150 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD EPROMs offer separate output enable—$\overline{G}$ ($\overline{OE}$)—and chip enable—$\overline{E}$ ($\overline{CE}$)—controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's EPROMs may be programmed using the Flashrite programming algorithm, which offers several fold improvement in programming time. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



BD000211

*Does not include redundant row and column bits.

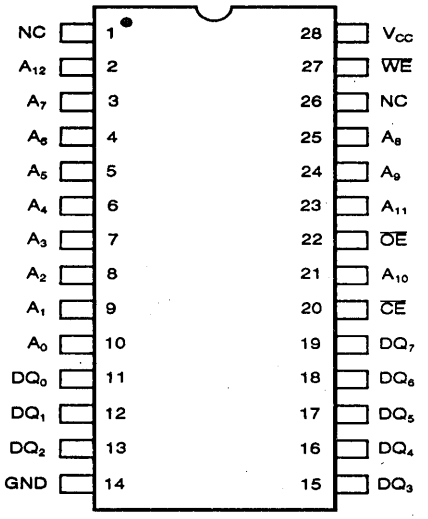
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C256				
Ordering Part No.:					
±5% V_{CC} Tolerance	27C256-155	27C256-205	27C256-255	27C256-305	27C256-455
±10% V_{CC} Tolerance	27C256-150	27C256-200	27C256-250	27C256-300	27C256-450
Max. Access Time (ns)	150	200	250	300	450
$\overline{E}$ ($\overline{CE}$) Access (ns)	150	200	250	300	450
$\overline{G}$ ($\overline{OE}$) Access (ns)	75	75	100	120	150

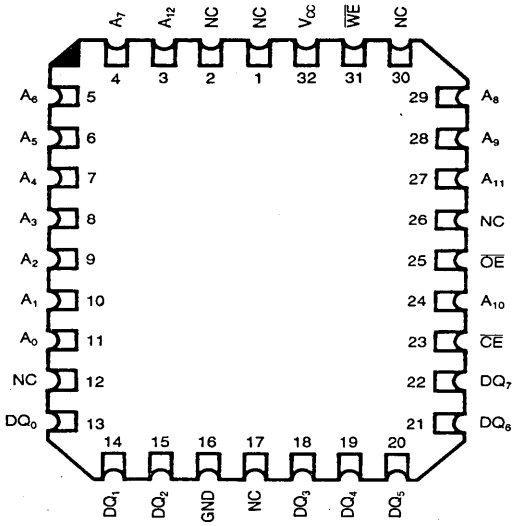
*Flashrite is a trademark of Advanced Micro Devices, Inc.

Publication # 08007 | Rev. A | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



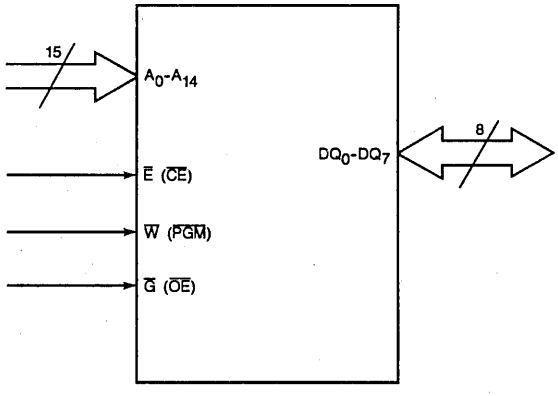
CD005601



CD006001

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002292

V_{CC} = 5.0-V Power Supply
V_{SS} = 0-V Power Supply
V_{PP} = 12.5-V Power Supply

6

Am27C256 OTP

32,768 x 8-Bit CMOS One-Time Programmable ROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time — 200 ns
- Low-power dissipation
- Both interactive and new Flashrite* programming algorithms available
- Single 5-volt power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available
- Programming voltage—12.5 V

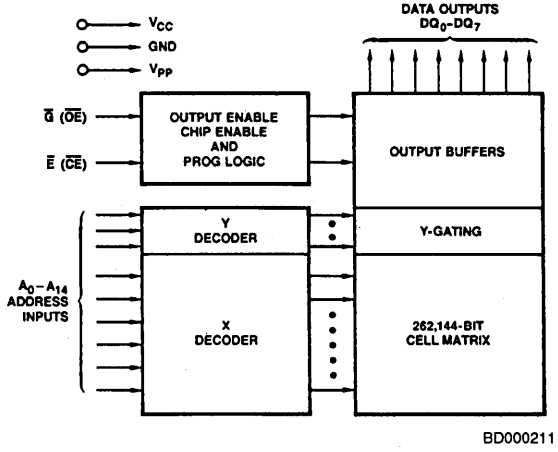
GENERAL DESCRIPTION

The Am27C256 is a CMOS One-Time Programmable Read-Only Memory (OTPROM) in a plastic package. It is organized as 32,768 x 8 bits per word. The plastic OTPROMs are ideal for volume production. First, because they can be inventoried unprogrammed and used with current-level software revisions; second, there is no window to be covered to prevent light from changing data —this could eliminate a manufacturing step and increase the reliability of the system; and third, they are compatible with auto insertion equipment. All AMD CMOS OTPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any wait state. Some of AMD's OTPROMs have access times of as fast as 200 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD OTPROMs offer separate output enable—$\overline{G}$ ($\overline{OE}$)—and chip enable—$\overline{E}$ ($\overline{CE}$)—controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's OTPROMs may be programmed using the Flashrite programming algorithm, which offers several fold improvement in programming time. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



BD000211

*Does not include redundant row and column bits.

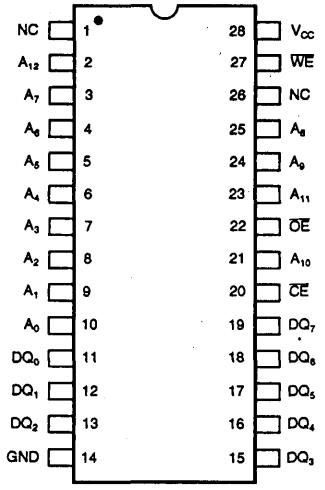
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C256 OTP	
Ordering Part No.:		
±5% V_{CC} Tolerance	27C256-205	27C256
±10% V_{CC} Tolerance	27C256-200	27C256-250
Max. Access Time (ns)	200	250
$\overline{E}$ ($\overline{CE}$) Access (ns)	200	250
$\overline{G}$ ($\overline{OE}$) Access (ns)	75	100

*Flashrite is a trademark of Advanced Micro Devices, Inc.

Publication # 08139 Rev. A Amendment /0
Issue Date: May 1986

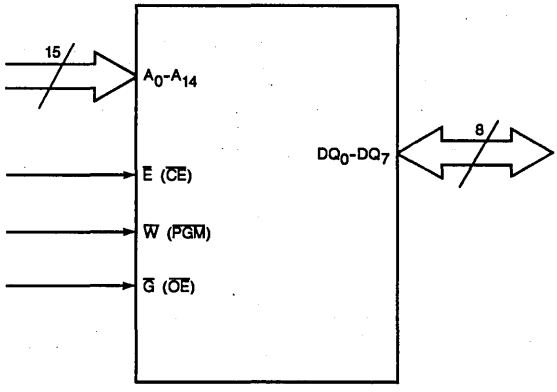
CONNECTION DIAGRAM
Top View



CD005601

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002292

V_{CC} = 5.0-V Power Supply
V_{SS} = 0-V Power Supply
V_{PP} = 12.5-V Power Supply

6

Am27C512

65,536 x 8-Bit CMOS EPROM

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time — 150 ns
- Low-power dissipation
- Both interactive and new Flashrite* programming algorithms available
- Single 5-volt power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available
- Programming voltage—12.5 V

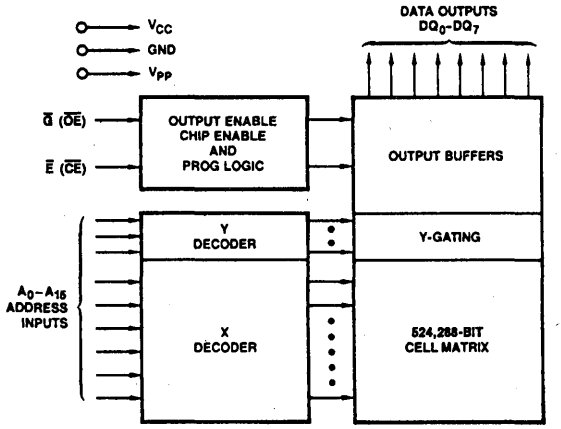
GENERAL DESCRIPTION

The Am27C512 is a CMOS ultraviolet erasable, programmable read-only memory. It is organized as 65,536 x 8 bits per word. All AMD CMOS EPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any wait state. Some of AMD's EPROMs have access times of as fast as 150 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD EPROMs offer separate output enable—$\overline{G}$ ($\overline{OE}$)—and chip enable—$\overline{E}$ ($\overline{CE}$)—controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's EPROMs may be programmed using the Flashrite programming algorithm, which offers several fold improvement in programming time. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



BD000212

*Does not include redundant row and column bits.

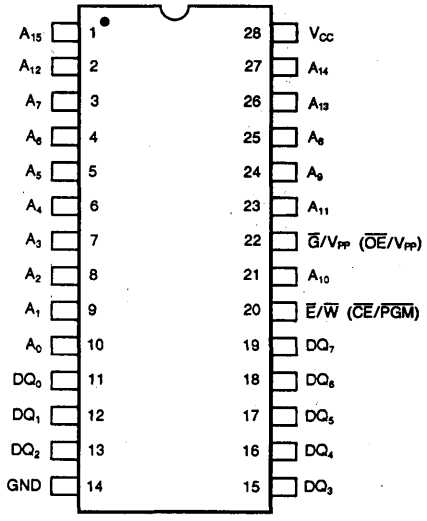
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C512				
Ordering Part No.:					
±5% V_{CC} Tolerance	27C512-155	27C512-205	27C512	27C512-305	27C512-455
±10% V_{CC} Tolerance	27C512-150	27C512-200	27C512-250	27C512-300	27C512-450
Max. Access Time (ns)	150	200	250	300	450
$\overline{E}$ ($\overline{CE}$) Access (ns)	150	200	250	300	450
$\overline{G}$ ($\overline{OE}$) Access (ns)	75	75	100	120	150

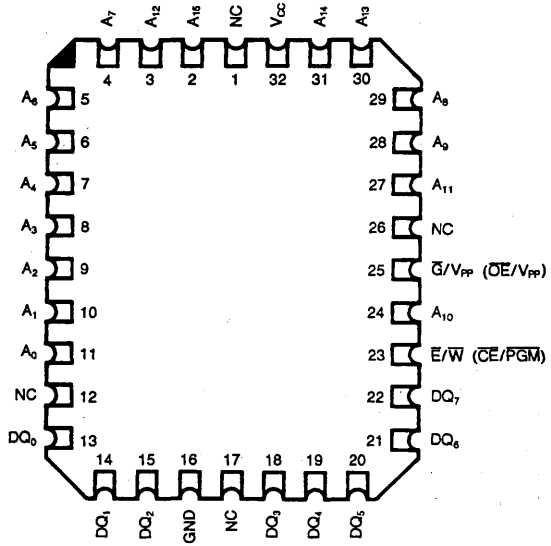
*Flashrite is a trademark of Advanced Micro Devices, Inc.

Publication # 08140 Rev. A Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



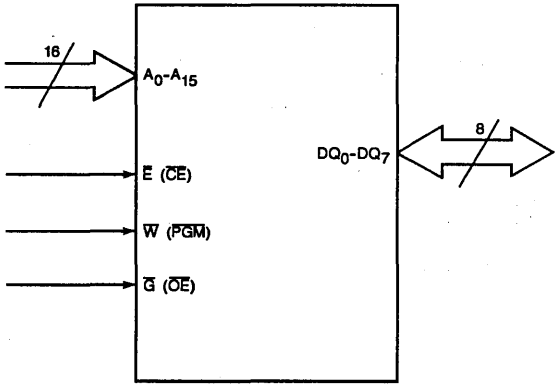
CD005602



CD006002

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002293

V_{CC} = 5.0-V Power Supply
V_{SS} = 0-V Power Supply
V_{PP} = 12.5-V Power Supply

6

Am27C512 OTP

65,536 x 8-Bit CMOS One-Time Programmable ROM (OTPROM)

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time — 200 ns
- Low-power dissipation
- Both interactive and new Flashrite* programming algorithms available
- Single 5-volt power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available
- Programming voltage—12.5 V

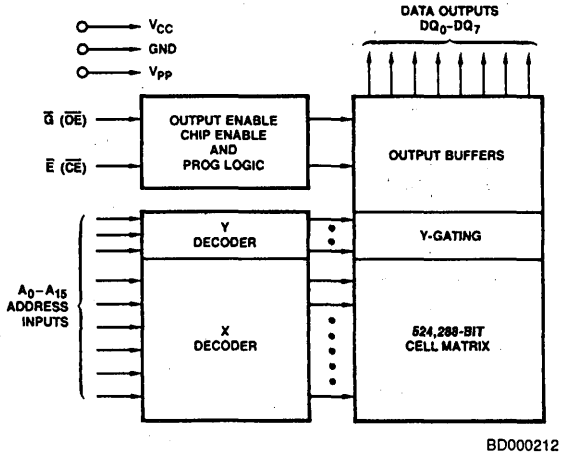
GENERAL DESCRIPTION

The Am27C512 is a CMOS One-Time Programmable Read-Only Memory (OTPROM). It is organized as 65,536 x 8 bits per word. The plastic OTPROMs are ideal for volume production. First, because they can be inventoried unprogrammed and used with current-level software revisions; second, there is no window to be covered to prevent light from changing data—this could eliminate a manufacturing step and increase the reliability of the system; and third, they are compatible with auto insertion equipment. All AMD CMOS OTPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any wait state. Some of AMD's OTPROMs have access times of as fast as 200 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD OTPROMs offer separate output enable—$\overline{G}$ ($\overline{OE}$)—and chip enable—$\overline{E}$ ($\overline{CE}$)—controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's OTPROMs may be programmed using the Flashrite programming algorithm, which offers several fold improvement in programming time. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



BD000212

*Does not include redundant row and column bits.

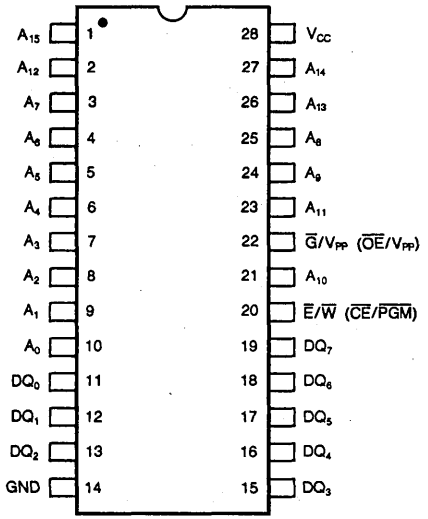
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C512 OTP	
Ordering Part No.:		
±5% V_{CC} Tolerance	27C512-205	27C512
±10% V_{CC} Tolerance	27C512-200	27C512-250
Max. Access Time (ns)	200	250
$\overline{E}$ ($\overline{CE}$) Access (ns)	200	250
$\overline{G}$ ($\overline{OE}$) Access (ns)	75	100

*Flashrite is a trademark of Advanced Micro Devices, Inc.

Publication # 08138 Rev. A Amendment /0
Issue Date: May 1986

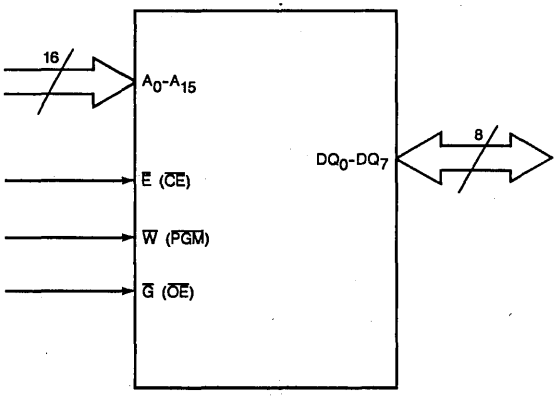
CONNECTION DIAGRAM
Top View



CD005602

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002293

V_{CC} = 5.0-V Power Supply
V_{SS} = 0-V Power Supply
V_{PP} = 12.5-V Power Supply

6

Am27C1024

65,536 x 16-Bit CMOS EPROM

PRELIMINARY

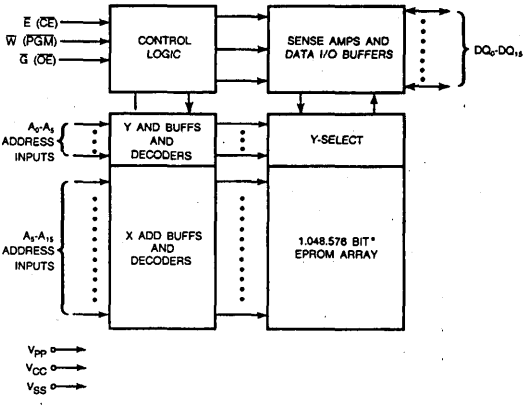
DISTINCTIVE CHARACTERISTICS

- Fast access time — 200 ns
- Low-power dissipation
  - 250 mW at 5 MHz
  - 1 mW at $\overline{E}$ ($\overline{CE}$) = V_{CC} ±0.3
- Programming voltage—12.5 ±0.3 V
- First EPROM offering 16-bit inputs and outputs
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available

GENERAL DESCRIPTION

The Am27C1024 is a 1-megabit, ultraviolet erasable, programmable read-only memory. It is organized as 65,536 words by 16 bits per word, operates from a single +5-volt supply, has a static standby mode, and features fast single address location programming. Because the Am27C1024 operates from a single +5-volt supply, it is ideal for use in 16-bit microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. The Am27C1024 supports a high-speed interactive programming algorithm which can result in programming times of less than two minutes. For convenience, both JEDEC and industry-standard notation is used throughout this document.

BLOCK DIAGRAM



BD005991

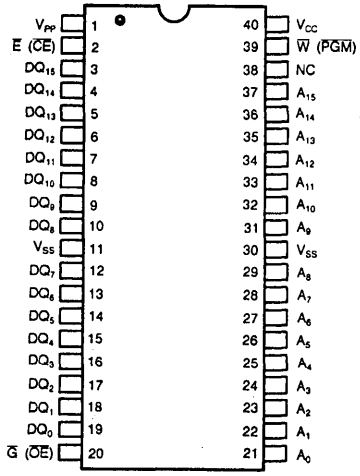
*Does not include redundant row and column bits.

PRODUCT SELECTOR GUIDE

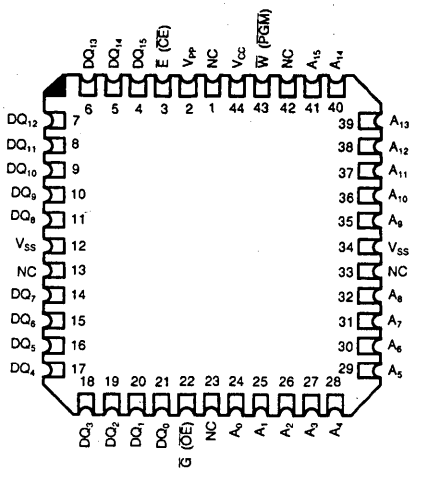
Family Part No.	Am27C1024			
Ordering Part No.:				
±5% V_{CC} Tolerance	27C1024-205	27C1024	27C1024-305	27C1024-455
±10% V_{CC} Tolerance	27C1024-200	27C1024-250	27C1024-300	–
Max. Access Time (ns)	200	250	300	450
$\overline{E}$ ($\overline{CE}$) Access (ns)	200	250	300	450
$\overline{G}$ ($\overline{OE}$) Access (ns)	75	100	120	150

Publication # 06780 Rev. B Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAMS
Top View



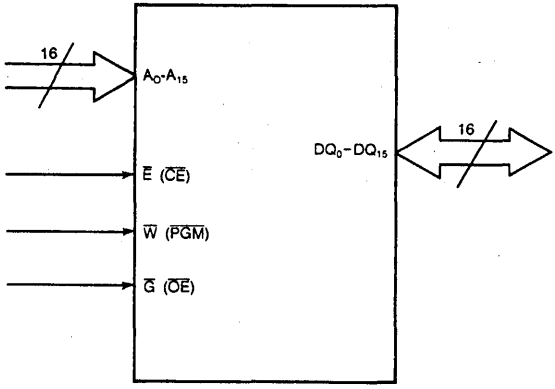
CD009301



CD009310

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002291

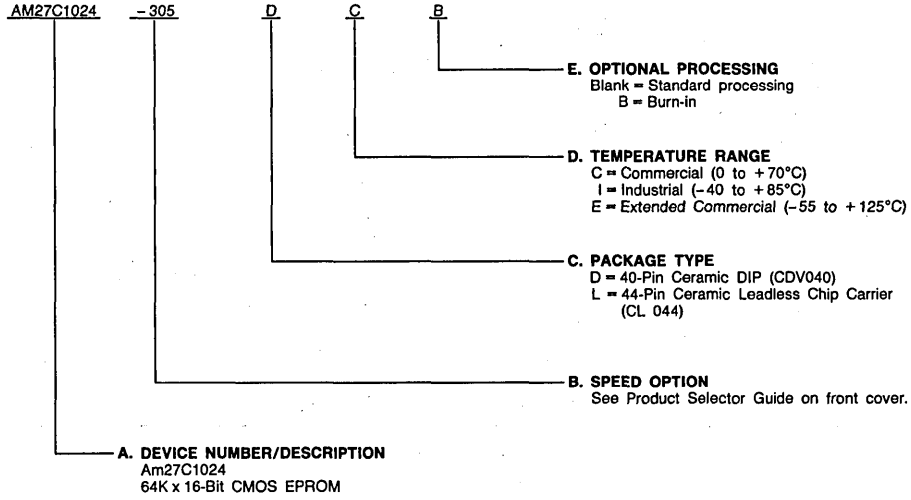
V_{CC} = 5.0-V Power Supply
V_{SS} = 0-V Power Supply
V_{PP} = 12.5 V Power Supply

6

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option *(if applicable)*
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27C1024-200, AM27C1024-205, AM27C1024-455	DC, DCB
AM27C1024, AM27C1024-250 AM27C1024-300 AM27C1024-305	DC, DCB, DI, DIB, DE, DEB, LE, LEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

Erasing the Am27C1024

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C1024 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C1024. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for fifteen to twenty minutes. The Am27C1024 should be about one inch from the source and all filters should be removed from the ultraviolet light source prior to erasure.

It is important to note that the Am27C1024, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with ultraviolet sources at 2537A, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the Am27C1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C1024

Upon delivery, or after each erasure, the Am27C1024 has all 1,048,576 bits in the "1," or HIGH state. "0s" (LOW state) are loaded into the Am27C1024 through the procedure of programming.

The programming mode is entered when 12.5 ±0.3 V is applied to the V_{PP} pin, $\overline{W}$ ($\overline{PGM}$) is at V_{IL}, and $\overline{E}$ ($\overline{CE}$) is at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the DQ_n pins.

The flowchart (Figure 1) in the Programming section of this document shows AMD's interactive algorithm. Interactive algorithms reduce programming time by using short programming pulses and giving each address only as many pulses as is necessary to reliably program the data. After each pulse is applied to a given address, data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C1024. After interactive programming is complete, an overprogram pulse is given to each memory location; this ensures that all bits have sufficient margin. After the final address is completed, the entire EPROM memory is verified at V_{CC} = 5 V ±5%. Conventional (fixed pulse) programming can be performed with a pulse of 10 ms at every address. This method is sampled and not 100% tested.

Program Inhibit

Programming of multiple Am27C1024s in parallel with different data is also easily accomplished. Except for $\overline{W}$ ($\overline{PGM}$) or $\overline{E}$ ($\overline{CE}$), all like inputs of the parallel Am27C1024 — including $\overline{G}$ ($\overline{OE}$) — may be common. A TTL LOW-level program pulse applied to an Am27C1024 $\overline{W}$ input with V_{PP} = 12.5 ±0.3 V and $\overline{E}$ LOW will program that Am27C1024. A HIGH-level $\overline{E}$ or $\overline{W}$ input inhibits the other Am27C1024s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{G}$ ($\overline{OE}$) at V_{IL}, $\overline{E}$ ($\overline{CE}$) at V_{IL}, $\overline{W}$ ($\overline{PGM}$) at V_{IH}, and V_{PP} at 12.5 ±0.3 V.

Auto Select Mode

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient-temperature range required when programming the Am27C1024.

To activate this mode, the programming equipment must force 12.0 ±0.5 V on address line A_9 of the Am27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select mode.

Byte 0 ($A_0 = V_{IL}$, DQ_0-DQ_7) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$, DQ_0-DQ_7), the device identifier code. For the Am27C1024, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the most significant bit (MSB), DQ_7, defined as the parity bit. The state of the higher order outputs (DQ_8-DQ_{15}) is undefined during Auto Select.

Read Mode

The Am27C1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$ ($\overline{CE}$)) is the power control and should be used for device selection. Output Enable ($\overline{G}$ ($\overline{OE}$)) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{E}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been LOW and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The Am27C1024 has a standby mode which reduces the active power dissipation by 98% from 250 mW to 5 mW (values for 0 to +70°C). The Am27C1024 is placed in the standby mode by applying a TTL HIGH signal to the $\overline{E}$ ($\overline{CE}$) input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{G}$ ($\overline{OE}$) input.

Power-down Mode

The Am27C1024 also has a power-down mode which reduces the power dissipation by 99.8% — from 250 mW to 1 mW (values for 0 to +70°C). The Am27C1024 is placed in power down by raising $\overline{E}$ to V_{CC} ±0.3 V.

Output Or-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1) low-memory power dissipation, and
2) assurance that output-bus contention will not occur.

It is recommended that $\overline{E}$ ($\overline{CE}$) be decoded and used as the primary device selecting function, while $\overline{G}$ ($\overline{OE}$) be made a common connection to all devices in the array, and connected to the Read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit-board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

TABLE 1. FUNCTION TABLE

MODE \ PINS	$\overline{E}$ ($\overline{CE}$)	$\overline{G}$ ($\overline{OE}$)	$\overline{W}$ ($\overline{PGM}$)	A_9	V_{PP}	OUTPUTS
Read	L	L	H	X	V_{CC}	D_{OUT}
Output Disable	L	H	H	X	V_{CC}	High Z
Standby	H	X	X	X	V_{CC}	High Z
Program	L	X	L	X	V_{PP}	D_{IN}
Program Verify	L	L	H	X	V_{PP}	D_{OUT}
Program Inhibit	H	X	X	X	V_{PP}	High Z
Auto Select	L	L	H	V_H	V_{CC}	Code

Notes: H = HIGH
L = LOW
X = Don't Care
V_H = 12.0 ±0.5 V

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature
with Power Applied ..... −55 to +125°C
Supply Voltage
with Respect to Ground
on All Inputs Except A_9 and V_{PP} ..... +6.25 to −0.6 V
on A_9 ..... +13.00 to −0.6 V
on V_{PP} ..... +13.00 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)
(V_{PP}) ..... +12.20 to +12.80 V

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)
(V_{PP}) ..... +12.20 to +12.80 V

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)
(V_{PP}) ..... +12.20 to +12.80 V

Notes: 1. For the Am27C1024, 27C1024-205, 27C1024-305, and 27C1024-455, V_{CC} = +4.75 to +5.25 V.
2. For the Am27C1024-200, 27C1024-250, and 27C1024-300, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1	V
V_{IL}	Input LOW Voltage			−0.1	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 to +5.5 V			10.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to +5.5 V			10.0	µA
I_{CC3}	V_{CC} Power-down Current (Note 7)	$\overline{E}$ ($\overline{CE}$) = V_{CC} ±0.3 V	C/I Devices:		200.0	µA
			E Devices:		240.0	
I_{CC2}	V_{CC} Standby Current (Note 7)	$\overline{E}$ = V_{IH}, $\overline{G}$ ($\overline{OE}$) = V_{IL}	C/I Devices:		1.0	mA
			E Devices:		1.5	
I_{CC1}	V_{CC} Active Current (Notes 5 & 7)	$\overline{E}$ = V_{IL}, f = 5 MHz; I_{OUT} = 0 mA (open outputs)	C/I Devices:		50.0	mA
			E Devices:		60.0	
I_{PP}	V_{PP} Supply Current (Read) (Notes 6 & 7)	$\overline{E}$ = V_{IL} = $\overline{G}$, V_{PP} = 5.5 V			5.0	mA

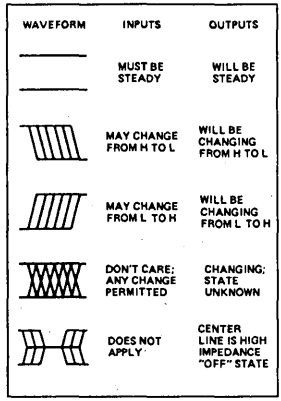
CAPACITANCE (Notes 2, 3 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	18.0	25.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	18.0	25.0	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The Am27C1024 must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{G}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. For Am27C1024-455, I_{PP} = 10 mA, I_{CC1} = 5 mA, and I_{CC3} = 1 mA maximum.
8. T_A = +25°C, f = 1 MHz.

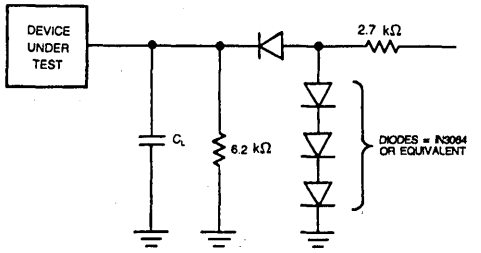
6

KEY TO SWITCHING WAVEFORMS



KS000010

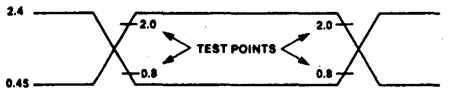
SWITCHING TEST CIRCUITS



TC003191

C_L = 100 pF including jig capacitance.

SWITCHING TEST WAVEFORMS



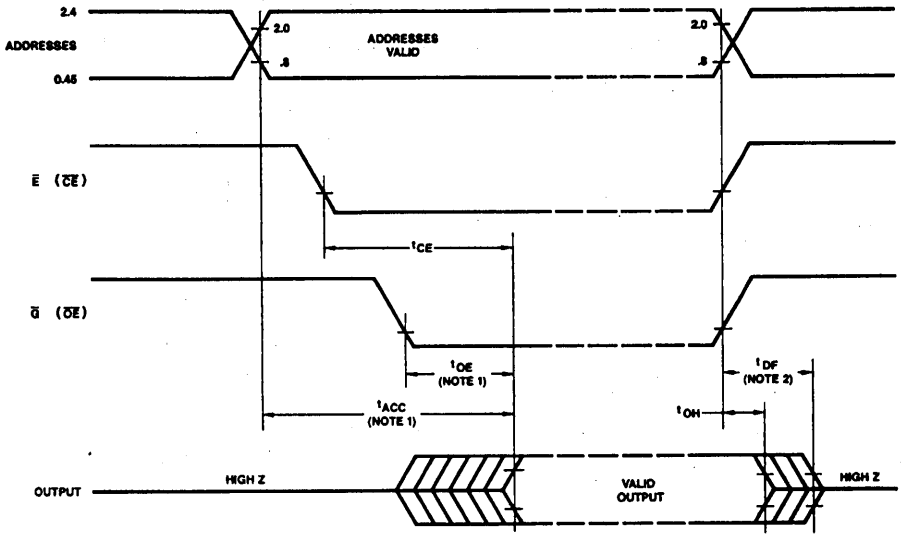
WF009540

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, 4, 5)

No.	Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description	Test Conditions	27C1024-200, 27C1024-205 Min.	27C1024-200, 27C1024-205 Max.	27C1024 27C1024-250 Min.	27C1024 27C1024-250 Max.	27C1024-300, 27C1024-305 Min.	27C1024-300, 27C1024-305 Max.	27C1024-455 Min.	27C1024-455 Max.	Units
1	t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{E}$ ($\overline{CE}$) = $\overline{G}$ ($\overline{OE}$) = V_{IL}		200		250		300		450	ns
2	t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{G}$ = V_{IL}		200		250		300		450	ns
3	t_{GLQV1}	t_{OE}	Output Enable to Output Delay	$\overline{E}$ = V_{IL}		75		100		120		150	ns
4	t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 3)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float			60		60		60		80	ns
5	t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{E}$, or whichever occurred first			0		0		0		0	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The Am27C1024 must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. Output Load: 1 TTL gate and C_L = 100 pF
Input Rise & Fall Times: ≤ 20 ns
Input Pulse Levels: 0.45 to 2.4 V
Timing Measurement
Reference Level — Inputs: 0.8 V and 2 V
— Outputs: 0.8 V and 2 V

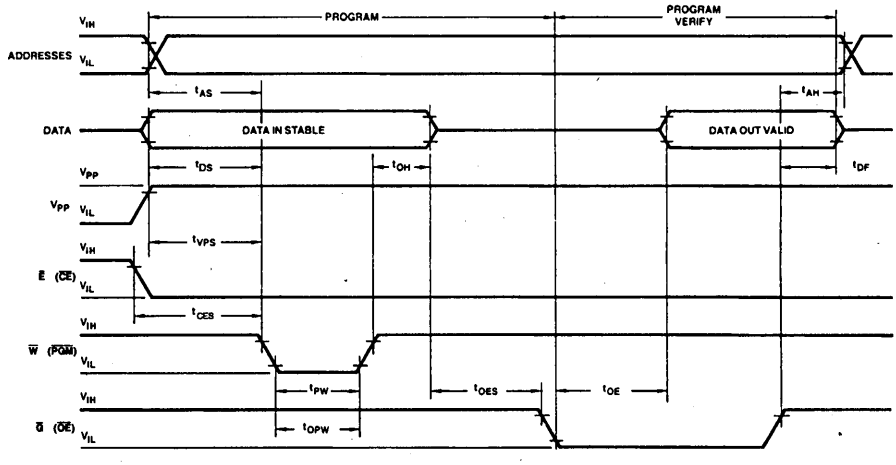
SWITCHING WAVEFORMS



WF001291

Read Cycle

Notes: 1. $\overline{G}$ ($\overline{OE}$) may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{E}$ ($\overline{CE}$) without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.



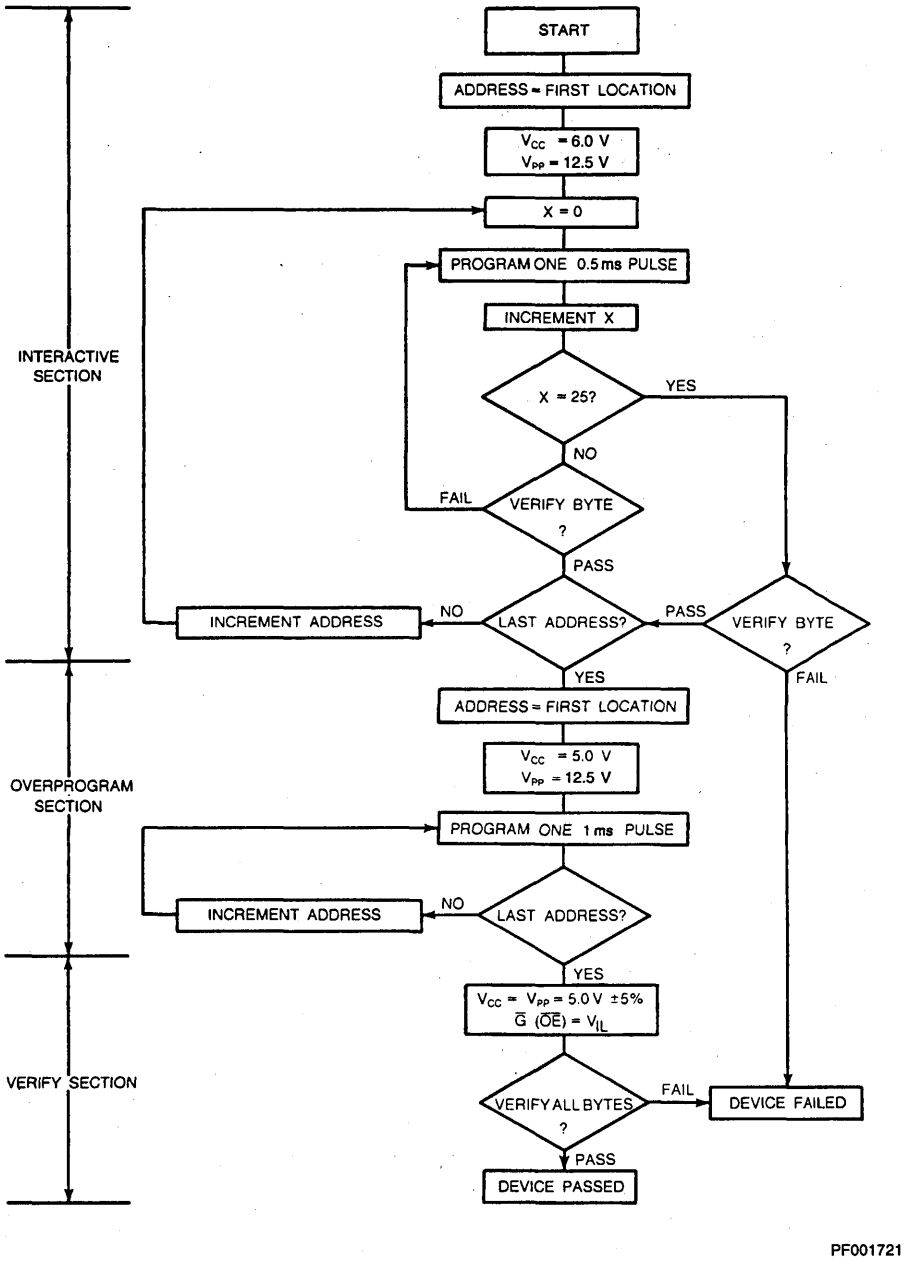
WF000551

Interactive Programming Algorithm Waveforms (Notes 1 and 2)

Notes: 1. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
2. t_{OE} and t_{DF} are characteristics of the device but must be accommodated by the programmer.

PROGRAMMING

This section covers identifier bytes, Interactive Programming Flowchart, and Interactive Programming DC and AC Switching Programming Characteristics.



PF001721

Figure 1. Interactive Programming Flowchart

6

TABLE 2. IDENTIFIER BYTES

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8C

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. A_1-$A_8 = A_{10}$-$A_{15} = \overline{E}\ (\overline{CE}) = \overline{G}\ (\overline{OE}) = V_{IL}$
3. $\overline{W}\ (\overline{PGM}) = V_{IH}$

INTERACTIVE PROGRAMMING ALGORITHM DC CHARACTERISTICS

(Notes 1-4)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)		−0.1	0.8	V
V_{IH}	Input HIGH Level		2.0	$V_{CC} + 1$	V
V_{OL}	Output LOW Voltage during Verify	$I_{OL} = 2.1$ mA		.45	V
V_{OH}	Output HIGH Voltage during Verify	$I_{OH} = -400$ μA	2.4		V
V_{A9}	A_9 Auto-Select Voltage		11.5	12.5	V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50.0	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{E}\ (\overline{CE}) = V_{IL} = \overline{W}\ (\overline{PGM})$		30.0	mA

INTERACTIVE PROGRAMMING ALGORITHM AC SWITCHING PROGRAMMING CHARACTERISTICS

(Notes 1-4)

No.	Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description	Min.	Max.	Units
1	t_{AVWL}	t_{AS}	Address Setup Time	2.0		μs
2	t_{DZGL}	t_{OES}	$\overline{G}\ (\overline{OE})$ Setup Time	2.0		μs
3	t_{DVWL}	t_{DS}	Data Setup Time	2.0		μs
4	t_{GHAX}	t_{AH}	Address Hold Time	2.0		μs
5	t_{WHDX}	t_{DH}	Data Hold Time	2.0		μs
6	t_{EHQZ}	t_{DF}	Chip Enable to Output Float Delay	0	130.0	μs
7	t_{VPS}	t_{VPS}	V_{PP} Setup Time	2.0		μs
8	t_{WLWH1}	t_{PW}	$\overline{W}\ (\overline{PGM})$ Initial Program Pulse Width	.45	.55	ms
9	t_{WLWH2}	t_{OPW}	$\overline{W}$ Overprogram Pulse	0.95	1.05	ms
10	t_{ELWL}	t_{CES}	$\overline{E}\ (\overline{CE})$ Setup Time	2.0		μs
11	t_{GLQV2}	t_{OE}	Data Valid from $\overline{G}$		150.0	ns

Notes: 1. $T_A = +25°C \pm 5°C$; $V_{CC} = 5.0\ V \pm 0.25\ V$; $V_{PP} = 12.5 \pm 0.3\ V$.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming the Am27C1024, a 9.1-μF capacitor is required between V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are sampled but not 100% tested to worst-case conditions.
5. Conventional (fixed pulse) programming can be performed with a 10-ms pulse at every address. This method is sampled and is not 100% tested.

Packaging

TECHNICAL REPORT

No. TR202

THERMAL CHARACTERIZATION OF PACKAGE DEVICES

BY James. D. Hayward

7

Publication #	Rev.	Amendment
08127	A	/0

Issue Date: **May 1986**

ABSTRACT

Determination of the Thermal Resistance of Packaged Devices is of concern to the designer of new devices and to AMD customers. The Advanced Package and Material Development group has undertaken the task of characterizing current AMD products and quantifying package-related influences on Thermal Resistance. This report describes some of these effects and the technique used to measure Thermal Resistance.

1.0 DEFINITION OF THERMAL RESISTANCE

The reliability of an integrated circuit is largely dependent on the maximum temperature which the device will attain during operation. Because the stability of a semiconductor junction declines with increasing temperature, knowledge of the thermal properties of the packaged device becomes an important factor during device design. In order to increase the operating lifetime of a given device, the junction temperatures must be minimized. This demands knowledge of the thermal resistance of the completed assembly and specification of the conditions in which the device will function properly. As devices become both smaller and more complex and the requirement for high speed operation becomes more important, heat dissipation will become an ever more critical parameter.

Thermal resistance is defined as the temperature rise per unit power dissipation above some referenced condition. The unit of measure is typically °C/watt. The relationship between junction temperature and thermal resistance is given by:

$$T_j = T_X + P_d \theta_{jx} \qquad (1)$$

where: T_j = junction temperature
T_X = reference temperature
P_d = power dissipation
θ_{jx} = thermal resistance
X = some defined test condition

In general, one of three conditions is defined for measurement of thermal resistance:

θ_{jc} – thermal resistance measured with reference to the temperature at some specified point on the package surface.

θ_{ja} (still air) – thermal resistance measured with respect to the temperature of a specified volume of still air.

θ_{ja} (moving air) – thermal resistance measured with respect to the temperature of air moving at a specified velocity.

The relationship between θ_{jc} and θ_{ja} is

$$\theta_{ja} = \theta_{jc} + \theta_{ca}$$

where θ_{ca} is a measure of the heat dissipation due to natural convection (still air) or forced convection (moving air) and the effect of heat radiation and mounting techniques. θ_{jc} is dependent solely on material properties and package geometry; θ_{ja} includes the influence of the surface area of the package and environmental conditions. Each of these definitions of thermal resistance is an attempt to simulate some manner in which the package device may be used.

The thermal resistance of a packaged device, however measured, is a summation of the thermal resistances of the individual components of the assembly. These in turn are functions of the thermal conductivity of the component materials and the geometry of the heat flow paths. Like other material properties, thermal conductivity is usually temperature dependent. For alumina and silicon, two common package materials, this dependence can amount to a 30% variation in thermal conductivity over the operating temperature range of the device. The thermal resistance of a component is given by

$$\theta = \frac{L}{K(T)A} \qquad (2)$$

where: L = length of the heat flow path
A = cross sectional area of the heat flow path
K(T) = thermal conductivity as a function of temperature

and the overall thermal resistance of the assembly (discounting convective effects) will be:

$$\theta = \Sigma\theta_n = \Sigma\frac{L_n}{K_n A_n}$$

But since the heat flow path through a component is influenced by the materials surrounding it, determination of L and A is not always straightforward.

A second factor that affects the thermal resistance of a packaged device is the power dissipation level and, more particularly, the relationship between power level and die geometry, i.e., power distribution and power density. By rearrangement of equation 1 to

$$P_d = \frac{1}{\theta_{jx}}(T_j - T_X) = \frac{1}{\Sigma\theta_n}(T_j - T_X) \qquad (3)$$

the relationship between P_d and T_j can be more clearly seen. Thus, to dissipate a greater quantity of heat for a given geometry, T_j must increase and, since the individual θ_n will also increase with temperature, the increase in T_j will not be a linear function of increasing power levels.

A third factor of concern is the quality of the material interfaces. In terms of package construction, this relates specifically to the die attach bond, and for those packages having a heatsink, the heatsink attach bond. The quality of the die attach bond will most severely influence the package thermal resistance as this is the area which first impedes the transfer of heat out of the silicon die. Indeed, it seems likely that the initial thermal response of a powered device can be directly related to the quality of the die attach bond.

2.0 EXPERIMENTAL METHOD

The technique for measurement of thermal resistance involves the identification of a temperature-sensitive parameter on the device and monitoring this parameter while the device is powered. For bipolar integrated circuits the forward voltage of the substrate isolation diode provides a convenient parameter to measure and has the advantage of a linear dependence on temperature. MOS devices which do not have an accessible substrate diode present greater measurement difficulties and may require simulation through use of a specially designed thermal test die. Choice of the parameter to be measured must be made with some care to insure that the results of the measurement are truly representative of the thermal state of the device being investigated. Thus measurement of the substrate isolation diode which is generally diffused across the area of the die yields a weighted average of the condition of

the individual junctions across the die surface. Measurement of a more local source would yield a less generalized result.

For MOS devices, simulation is accomplished using the thermal test die. The basis for this test die is a 25 mil square cell containing an isolated diode and a 1KΩ resistor. The resistors are interconnected from cell to cell on the wafer before it is cut into multiple arrays of the basic unit cell. In use the device is powered via the resistors with voltage or current adjusted for the proper level and the voltage drop of the individual diodes is monitored as in the case of actual devices.

Prior to the thermal resistance test, the diode voltage/temperature calibration must be determined. This is done by measuring the forward voltage at 1mA current level at two different temperatures. The diode calibration factor is then:

$$K_f = \frac{T_2 - T_1}{V_2 - V_1} = \frac{\Delta T}{\Delta V} \qquad (4)$$

in units of °C/mV. For most diodes used for this test the voltage/temperature relationship is linear and these two measurement points are sufficient to determine the calibration.

The actual thermal resistance measurement has two alternating phases: measurement and power on. The device under test is pulse powered with an ON duty cycle of 99% and a repetition rate of < 100Hz. During the brief OFF states the device is reverse-biased with a 1mA current and the voltage drop is measured. The series of voltage readings are averaged over short periods and compared to the voltage reading obtained before the device was first powered ON. The thermal resistance is then computed as:

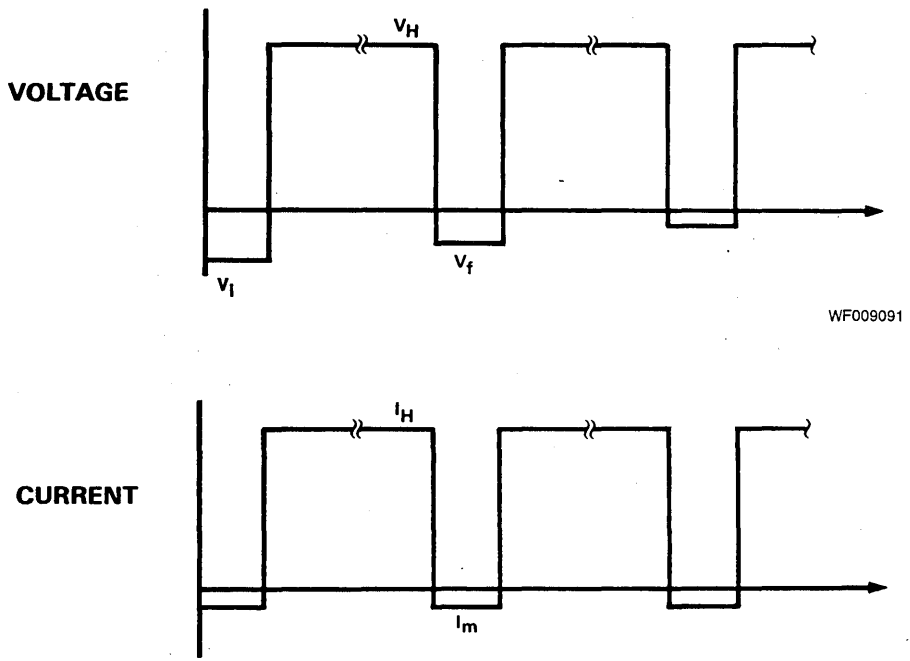
$$\theta_{jx} = \frac{K_f(V_f - V_i)}{V_H I_H} = \frac{K_f \Delta V}{P_d} \qquad (5)$$

where: K_f = calibration factor
V_i = initial forward voltage value
V_f = current forward voltage value
V_H = heating voltage
I_H = heating current

The pulsing measurement is continued until the device has reached thermal equilibrium and the final value measured is the equilibrium thermal resistance of the device under test.

When the end result desired is θ_{ja} (still air), the device and the test fixture (typically a standard burn-in socket) are enclosed in a box containing approximately 1 cubic foot of air. For θ_{jc} measurements the device is attached to a large metal heatsink. This insures that the reference point on the device surface is maintained at a constant temperature. The requirements for measurement of θ_{ja} (moving air) are rather more complex and involve the use of a small wind tunnel with capability for monitoring air pressure, temperature and velocity in the area immediately surrounding the device tested. Standardization of this last test requires much careful attention.

WAVEFORMS FOR PULSED THERMAL RESISTANCE TEST



3.0 Experimental Results

The thermal resistance data included in Table 1 is representative of the output of tests on representative samples of AMD products. This data has resulted from an on-going program undertaken by members of the Advanced Package and Material Development group.

The data represents what can be expected from a device in the specified package. Specific device types may differ; these numbers are for example only.

TABLE 1. THERMAL RESISTANCE OF AMD PRODUCTS
(Notes 1 & 2)

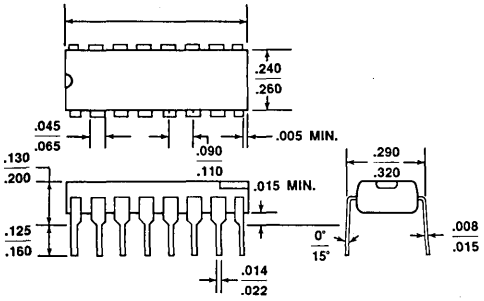
Pin Count	Package Type (Note 3)	θ_{ja}	θ_{jc}
16	Ceramic DIP	80	20
	Plastic DIP	110	35
	Ceramic Flatpack	120	10
18	Ceramic DIP	65	15
20	Ceramic DIP	65	15
	Plastic DIP	90	35
	Ceramic Flatpack	120	10
	Ceramic LCC	70	12
	Plastic LCC*	75	35
22	Plastic DIP	90	20
24	Ceramic DIP	50	15
	Plastic DIP	70	30
	Ceramic Flatpack	100	10
28	Ceramic DIP	40	12
	Plastic DIP	85	25
	Ceramic Flatpack	70	
	Ceramic LCC	70	15
	Plastic LCC*	55	30

Notes: 1. Representative values for each package type — for information only.
2. Any given device may differ from these values. Consult your local AMD sales office for specific-device information.
3. DIP = Dual-In-Line Package
LCC = Leadless Chip Carrier
LCC* = Leaded Chip Carrier

Package Outlines

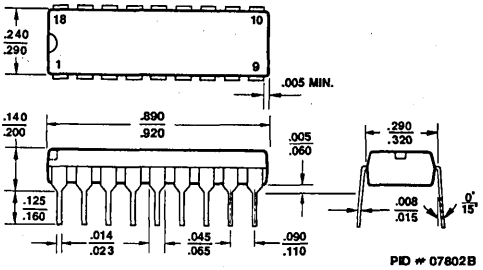
Plastic Dual-In-Line Packages (PD) (Cont'd.)

PD 016



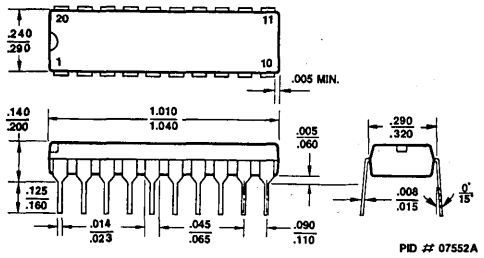
PID# 06957A

PD 018



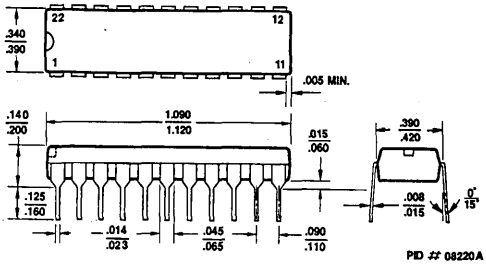
PID # 07802B

PD 020



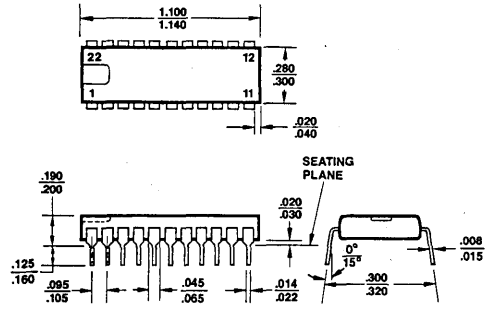
PID # 07552A

PD 022



PID # 08220A

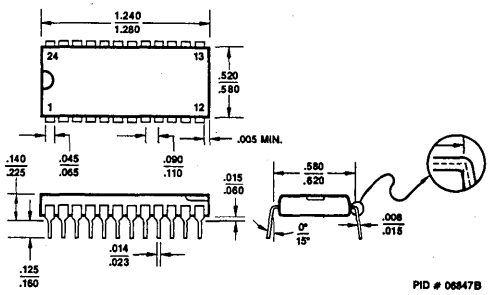
PD3022*



PID # 07813A

*Preliminary. Subject to Change

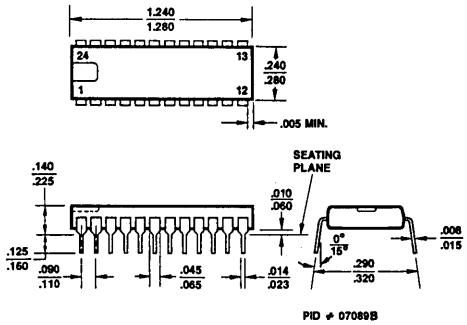
PD 024



PID # 06847B

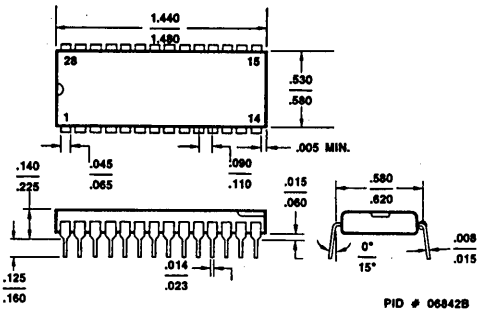
7

PD3024



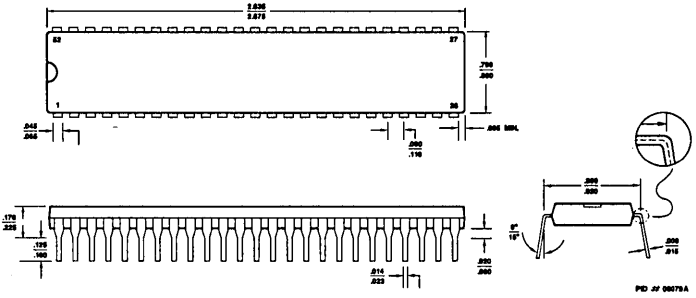
PID # 07089B

PD 028



PID # 06842B

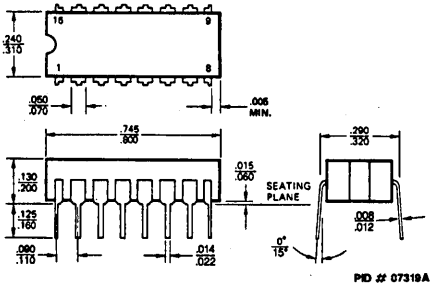
PD 052



PID # 06879A

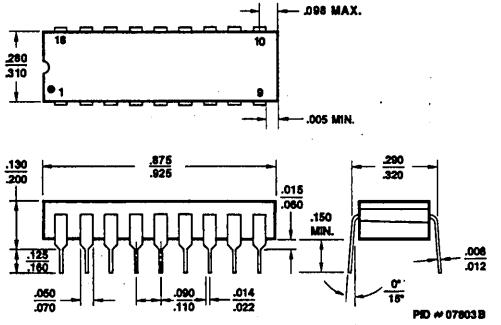
Ceramic Hermetic Dual-In-Line Packages (CD) (Cont'd.)

CD 016



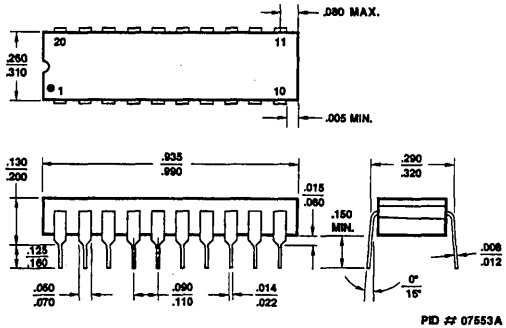
PID # 07319A

CD 018



PID # 07803B

CD 020

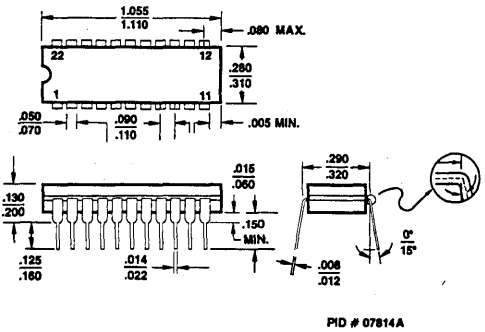


PID # 07553A

CD 020

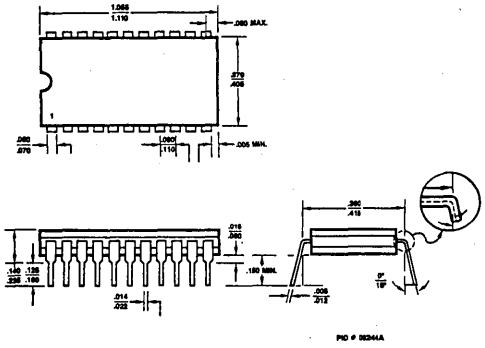
IN DEVELOPMENT

CD3022*



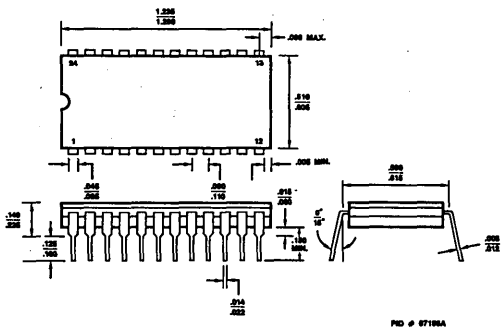
PID # 07814A

CD4022

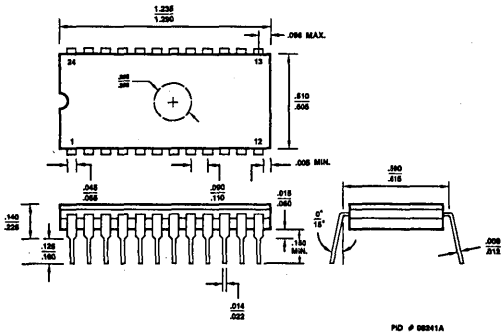


*Preliminary. Subject to Change

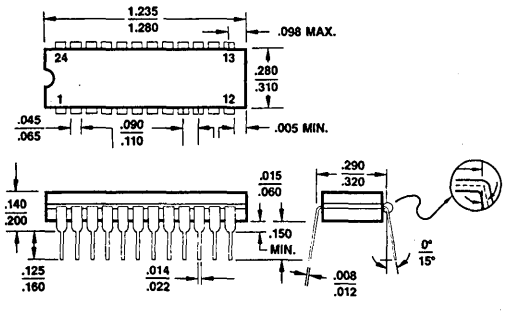
CD 024



CDV024

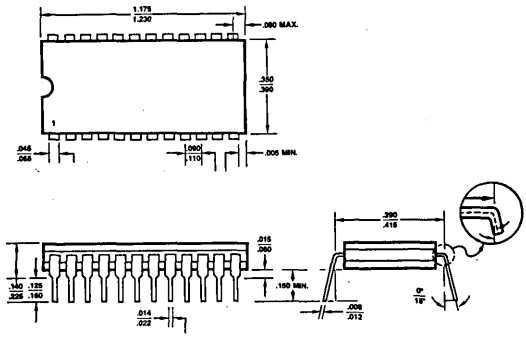


CD3024



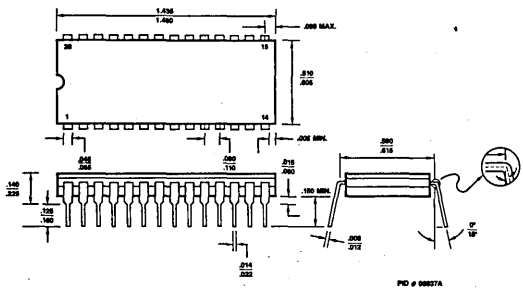
PID # 06850B

CD4024



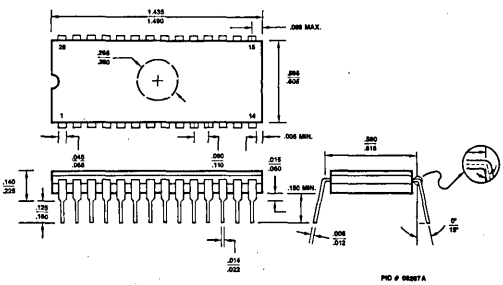
PID # 06701A

CD 028



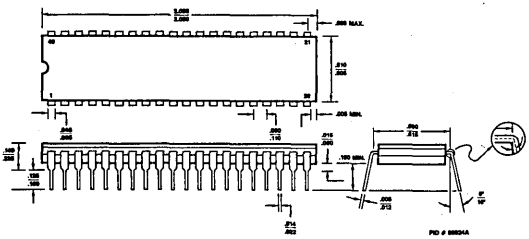
PID # 06837A

CDV028



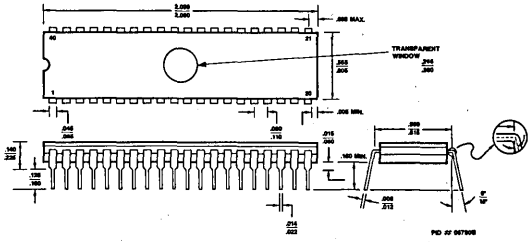
PID # 06267A

CD 040



PID # 06834A

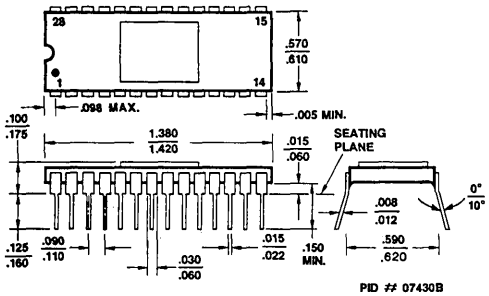
CDV040



PID # 06790B

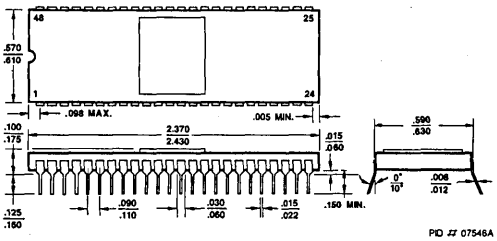
Sidebrazed Hermetic Dual-In-Line Packages (SD)

SD 028



PID # 07430B

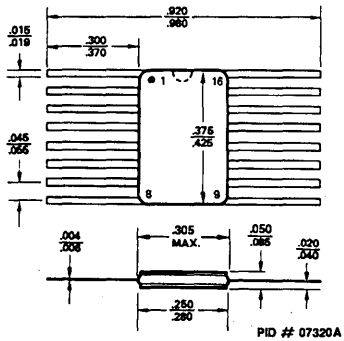
SD 048



PID # 07546A

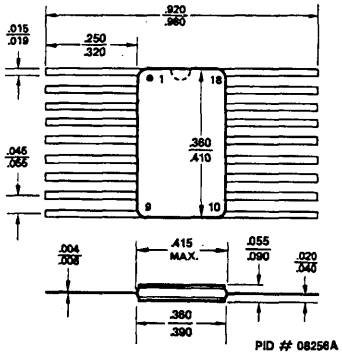
Ceramic Faltpacks (CF)

CF 016



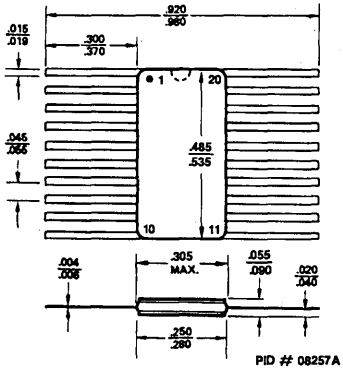
PID # 07320A

CF 018



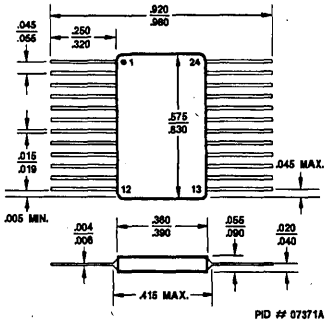
PID # 08256A

CF 020



PID # 08257A

CFM024



PID # 07371A

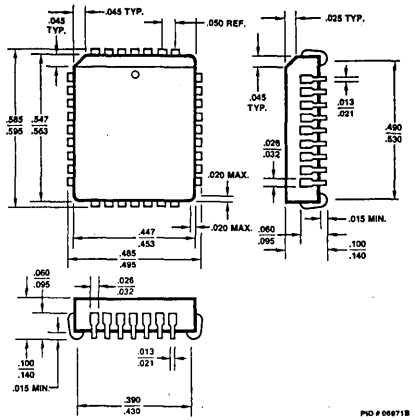
7

Plastic Leaded Chip Carriers (PL)

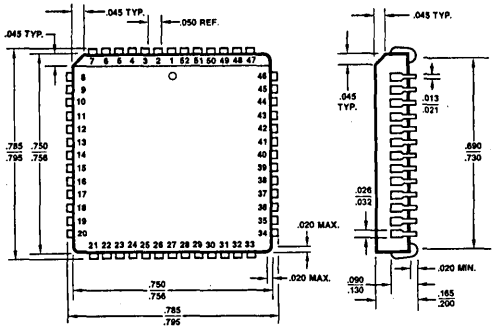
PLE018

IN DEVELOPMENT

PL 032*



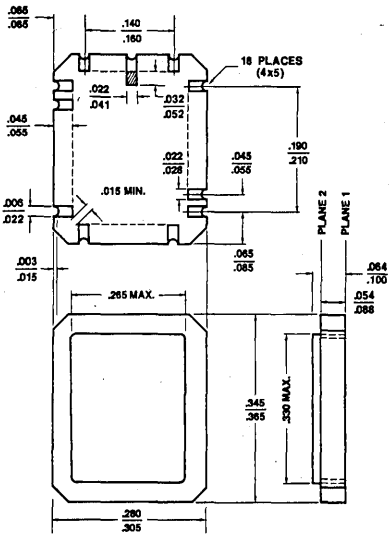
PL 052*



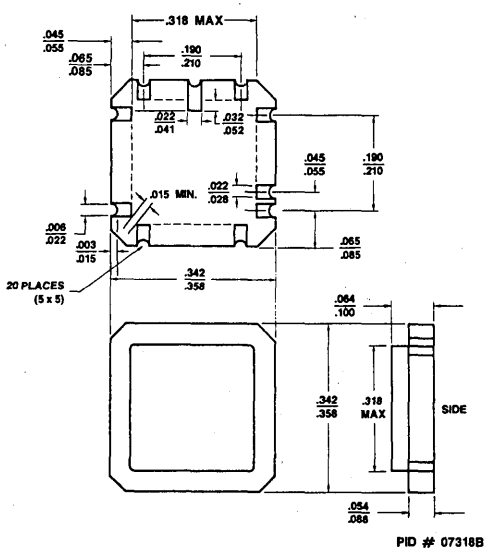
*Preliminary. Subject to Change.

Ceramic Leadless Chip Carriers (CL)

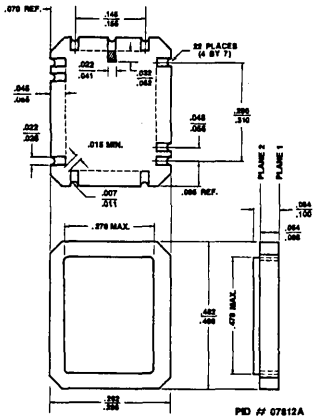
CLR018



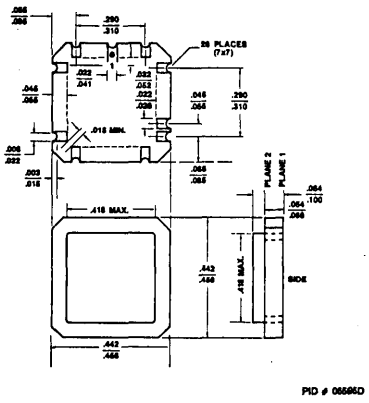
CL 020



CLR022*

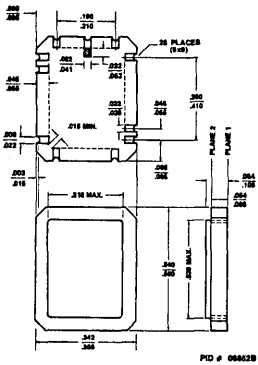


CL 028

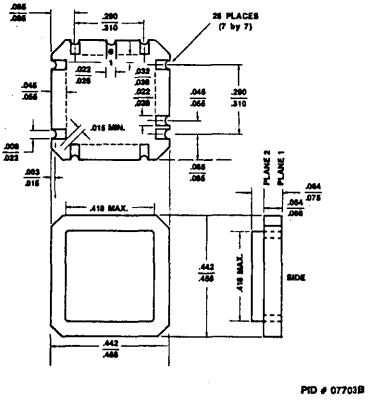


*Preliminary. Subject to Change.

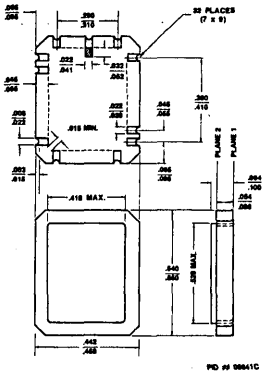
CLR028



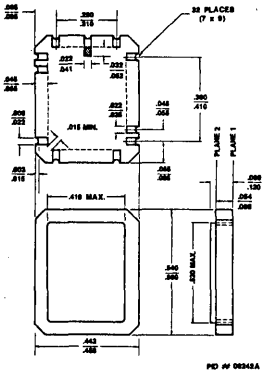
CLT028



CLR032



CLV032

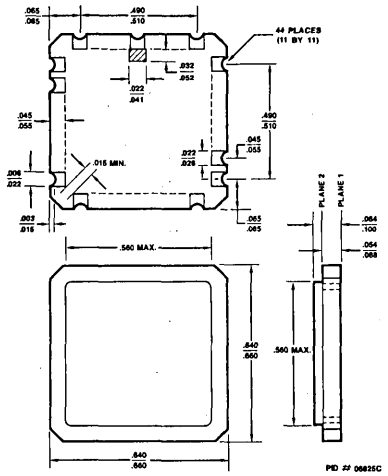


7

CLX032

IN DEVELOPMENT

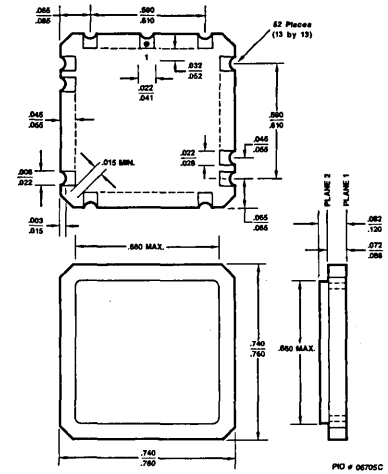
CL 044



CLV044

IN DEVELOPMENT

CL 052



Testing High-Performance Bipolar Memory

INTRODUCTION

During the last several years, the state-of-the art of TTL compatible bipolar memory integrated circuits has advanced very rapidly. Device complexity has increased dramatically not only in terms of the memory storage capacity but also by the addition of new on-chip functions such as the inclusion of output data registers. Simultaneously, advances in bipolar LSI design and manufacturing technology have generated significant improvements in the performance levels of bipolar memory. Similarly, the complexity and performance levels of systems which employ these devices have grown. The concomitant growth of system complexity has placed additional demands on both the device manufacturer and the user's incoming inspection area to assure the performance capabilities of each component before it is assembled into the system.

Several test equipment manufacturers now supply sophisticated, computer controlled testers for these inspection tasks. Most of this equipment is inherently capable of the millivolt and nanosecond accuracies which are required; most memory testers can generate the complex waveforms and test patterns needed. However, the details of applying this equipment to a specific test problem, including the problem of interfacing the tester to the device-under-test, are usually left to the user. The purpose of this application note is to discuss several problems which are frequently encountered when testing high performance bipolar memory devices, and to acquaint the user with how such problems may be identified, measured and corrected.

WHAT MAKES A MEMORY GOOD?

Before discussing the specifics of bipolar memory testing problems, it is important to understand the basic characteristics which these devices should exhibit. Clearly each device must meet all product specification parameters but, first and foremost, a bipolar memory should be fast! Address access time (delay from address input to data output), enable access time and enable recovery time should be as small as possible. High performance is often the primary reason for using bipolar memory. Similarly, the performance of the ideal bipolar memory should remain relatively constant with changes in supply voltage, ambient temperature and output load capacitance. Fast devices, offering stable performance over a broad range of conditions, permit the user to qualify a smaller number of part types; one fast device can accommodate many standard as well as high performance applications. Such devices provide added safety margin for the system design, permit simplification of system test and debug and assure trouble-free system performance in the field. Hence the "best" memory is a fast, stable device which not only meets a given user specification, but also offers the extra performance needed for a broad range of applications.

Advanced Micro Devices offers a family of bipolar Random Access Memories (RAMs) and Programmable Read Only Memories (PROMs) which are designed to meet this idealized definition as closely as possible. First, each AMD device is designed to meet a "military design goal." This means AMD bipolar memories are designed to provide the extra margins and higher output drive capabilities needed to assure proper performance over the extended miliary supply voltage and operating temperature ranges. This often necessitates the use of more advanced design techniques such as on-chip regulators, temperature and voltages compensation networks and feedback circuits. Second, AMD has conceived and developed an advanced, oxide separated, ion implanted manufacturing process called IMOX™. Developed specifically for the production of high density bipolar memories, this technology provides both high density and excellent performance in a truly reliable and manufacturable process. This combination of advanced design and fabrication technologies assures the military user of receiving components which are intended for his application while providing the commercial user with the extra margins, performance advantages and procurement benefits mentioned above.

THE SYSTEM ENVIRONMENT

To understand the problems of high-performance memory testing, it is helpful to understand the electrical environment in which the memory devices will actually operate, i.e., the typical system environment. The system designer must address and resolve several critically important questions if the system is to consistently perform to its design specifications. These questions include:

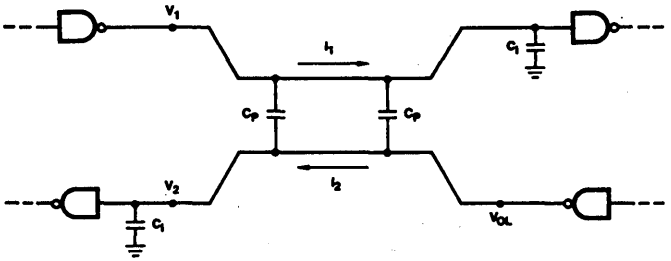
1. What noise voltages can the system's logic and memory devices tolerate?
2. What are the sources of system noise?
3. What can be done to control and minimize this noise?

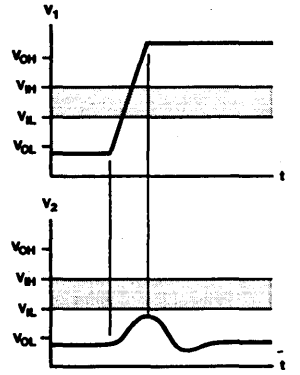
The first question is answered relatively easily. The magnitude of noise which can be tolerated relates directly to the worst case noise immunity specified for the logic family. Noise immunity is simply the difference between the worst case output levels (V_{OH} and V_{OL}) of the driving circuit and the worst case input voltage requirements (V_{IH} and V_{IL}, respectively) of the receiving circuit. For TTL devices the worst case noise immunity is typically 400mV for both the high and low logic levels.

If "system noise" is defined as the sum of things which subtract from this noise immunity, several sources can be identified. A few of the most important sources found in a digital, TTL system are listed below:

- Cross-Talk: The desire to pack system components as tightly as possible inevitably causes signal wires or PC board traces to be placed in close proximity. The lead-to-lead capacitance and mutual inductance thus created (see Figure 1) causes "noise" voltages to appear when adjacent signal paths switch.
- Transmission Line Reflections: Like it or not, every signal path in the system has transmission line characteristics. TTL signal paths are usually not designed as transmission lines, with predictable and uniform characteristic impedances. This is partly because of the higher costs implied for multilayer PC boards with internal ground planes, termination resistors, etc. It is also the result of TTL logic's limited ability to drive the low impedance lines provided by current PC board technologies. Hence, TTL signal paths do exhibit the ringing and reflection problems associated with improperly terminated transmission lines. These reflections subtract from the available noise immunity as shown in Figure 2.

Publication # 08190 Rev. A Amendment /0
Issue Date: May 1986

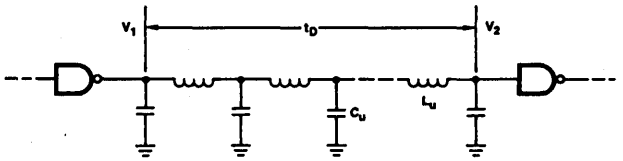


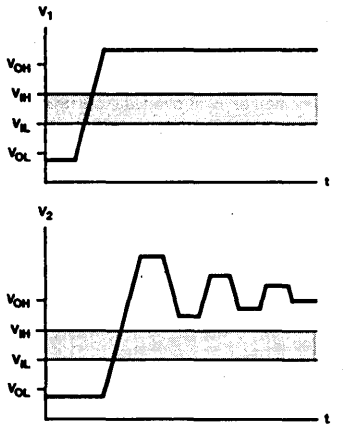


DG000010

As V_1 switches, I_1 flows to charge the input capacitance C_i. I_2 flows as a result of mutual inductance. The V_1 voltage change is also coupled directly to V_2 through the parasitic line-to-line capacitances, C_P.

Figure 1. An Example of Cross-Talk

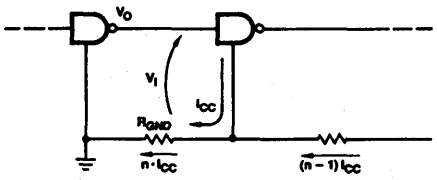




DG000020

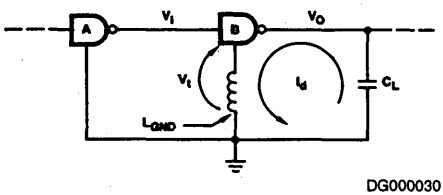
The unit length capacitance and inductance (C_u and L_u) give each system connection transmission line characteristics. Without a matched termination, switching at V_1 causes reflection voltages to appear at V_2, reducing noise immunity.

Figure 2. Line Reflections



$V_i = V_O - (n \cdot I_{CC})\ R_{GND}$

a) DC Ground "Noise"



DG000030

When V_i goes HIGH, V_O goes LOW discharging C_L. The discharge current I_d flows through the ground inductance L_{GND}, creating a transient voltage V_t. The input voltage seen by gate B is actually $V_i - V_t$.

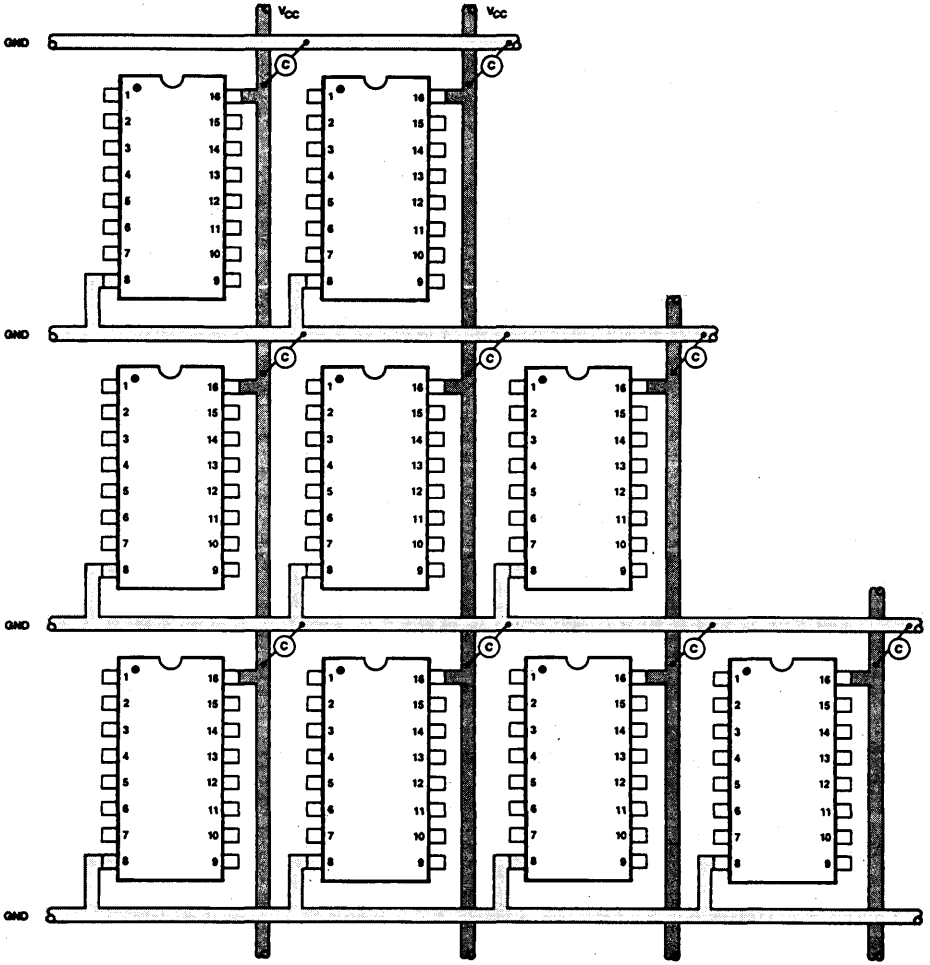
b) Transient Ground Noise

Figure 3.

- Ground Network Noise: Most high-performance systems employ large numbers of high-performance ICs. These devices typically draw large I_{CC} currents from the power supply. Cumulatively, these currents can reach several amperes per board. Such currents, flowing in the ground network, cause non-negligible DC voltage drops to occur; not all device ground pins are at zero volts. Since the output levels and the input thresholds of each TTL device reference the local ground (Figure 3a), these drops also subtract from the available noise immunity. Additional noise margin losses occur each time the device outputs switch. This occurs because large currents must flow to rapidly charge and discharge the interconnect and input capacitances which load each output. These charging currents flow in a loop

(Figure 3b) through the ground network which is normally a simple interconnection of wires, each with some value of resistance and inductance per unit length. Some additional resistive drops occur. But, the rapid changes in these currents (large di/dt), occurring as charging starts and stops, mean a transient ground noise voltage is also generated. This voltage obeys the law of $v = L(di/dt)$ where L is the ground circuit inductance and di/dt is the rate of change of the charging currents. Notice that adding local bypass capacitors can only reduce this voltage by paralleling the ground inductance with the V_{CC} network inductance. Bypassing cannot eliminate this problem because these capacitors shunt the devices and not the ground and V_{CC} network inductances where the noise is generated.

Controlling and minimizing noise in a digital system becomes more challenging as the system performance requirements increase. These requirements demand devices capable of short propagation delays, e.g., ultra-fast memories with excellent drive characteristics to minimize fully loaded access times.



Note: Transient ground current flow in four directions from each device ground: right and left on the ground bus; up and down the V_{CC} bus after passing through the local bypass capacitor, C. Equivalent ground inductance is very low.

Figure 4. Example of an AC Ground Mesh

Since noise margin violations result in system malfunctions, the system designer must define a set of rules governing the physical construction techniques to be used within the system. These rules address a host of considerations including power distribution, AC grounding, lead placement, line termination requirements, logic loading (fan in and fan out) and interconnect delays. Specifying these rules is a complex process of making appropriate cost-performance tradeoffs.

For a medium to high performance system, these rules might specify arranging devices in an array with V_{CC} power traces running vertically up the columns while ground metal running horizontally between the rows. Inserting bypass capacitors at each grid intersection forms an AC ground mesh (Figure 4), limiting the amount of ground inductance at each array site. If limits are also placed on the total capacitance each device may drive (cumulative interconnect and input capacitance on

all outputs), the total charging currents may be controlled thus limiting the noise immunity eroded by ground circuit noise. Similarly, the distance between adjacent traces and the maximum length of unterminated lines may be specified to control noise immunity losses caused by cross-talk and termination mismatches. Ultra-high performance systems may require additional measures; e.g., multilayer boards with true ground planes or increased usage of line drivers and receivers. Though the preceding descriptions have been simplified, it should be clear that distances between driving and receiving devices, the quantity and distribution of load capacitance, as well as the AC ground network integrity are all essential elements of the system design.

THE MEMORY TEST ENVIRONMENT

Ideally the test system hardware and fixtures would be designed to even more stringent rules than those used for the system. This is reasonable as the tester is the standard employed for accepting or rejecting components used in the system. Because a collection of additional objectives constrain the test environment, designing test hardware to equally or more stringent rules is usually impractical.

Memory testers must test many types of components under a variety of conditions. Tests performed include DC parametric tests, functional and AC tests with complex test patterns and margin tests to assure device operation at the extremes of applied conditions and supply voltage. To accomplish this, connections to sets of programmable input drivers and output receivers (comparators), multiple device bias and power supplies, relays to permit connection of the DC parametric test unit, and special load circuits must all converge at the test site.

To provide flexibility and facilitate repair, test hardware must be modular. This requirement dictates placing the hardware (drivers, receivers, etc.) on many small PC boards which then must talk to the DUT (device under test) through additional wiring and connectors.

Frequently the quantity of parts tested necessitates mating an automatic device handler to the tester. Handlers also provide capabilities for testing at temperature extremes when needed. The DUT must be tested inside this equipment, requiring still more wiring between the test head and the actual test site.

Ideally, all test hardware would be located immediately adjacent to the test site to minimize cross-talk, reflections and ground noise. However, this objective must be compromised to address the other objectives and constraints outlined above. Techniques commonly employed in making this compromise are illustrated in Figure 5. Notice that DUT drivers are remote from the test site, driving signal to the DUT through "series terminated" transmission lines. Similarly the receivers are some distance from the test site, receiving signals from the DUT through a series of connectors and wires which can degrade the signal. Most annoying of all, the test site ground connection has been compromised. This signal path must carry heavy transient and DC currents during test and should provide a very solid, low impedance reference against which all AC and DC tests are made. Accumulating resistance and inductance in this path jeopardizes the integrity of all test results.

Hence, the electrical environment provided at the test site is generally inferior to the actual system environment where the memory component will be used.

TEST RELATED PROBLEMS AND SOLUTIONS

Accurately measuring or verifying memory performance in the test system environment requires a recognition of its inherent limitations. Outlined below are five problem areas commonly encountered when testing high-performance bipolar memories. Methods of identifying and alleviating these problems are indicated.

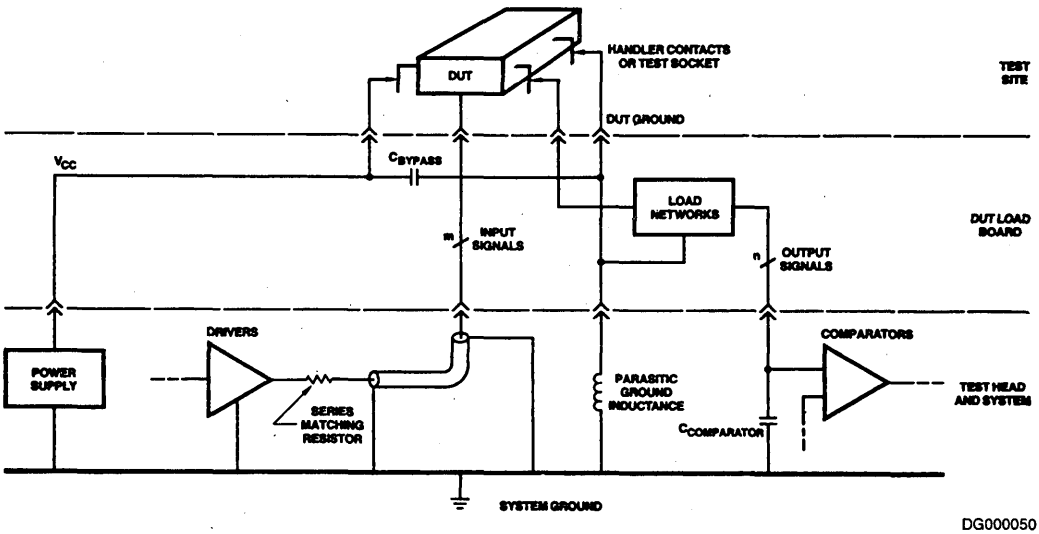


Figure 5. The Test System Environment

- Contending with Ground Noise: Ground noise is one of the most common and troublesome test problems. As defined above, ground noise is caused by switching currents flowing through the ground network impedance. Whereas the system environment (Figure 4) may provide multiple low inductance ground paths into a ground mesh or plane, the tester provides one long, higher inductance path back to the test system ground (Figure 5). This path includes handler con-

tacts, connectors and the DUT load board, all of which increase ground inductance and resistance. Transient currents which result when the DUT switches can be enormous. Consider the case of a byte wide (8 output) memory functional test. At some point in the test sequence, all memory outputs will switch from high to low (V_{OH} to V_{OL}) at the same instant, discharging all eight load capacitances simultaneously. If the input capacitance of the receiver is 40pF and the interconnect capacitance of the test fixture is 10pF, the total load capacitance driven by all device outputs would be 400pF. A fast memory device could discharge this load at a 1V/ns rate. The relationship i = C(dv/dt) implies peak charging currents of 400mA must flow through ground. As Figure 6 illustrates, this charging current does not build to its full value instantaneously. For a fast device the time required to go from zero to full charging current would approximate 2ns. A resultant ground current di/dt of 200mA/ns is implied. If the ground inductance is 1 nanohenry (approximate inductance of 1 inch of straight, small gauge wire), then v = L(di/dt) predicts AC ground noise of 200mV. As you have probably guessed, the typical test site ground inductance exceeds 1nh. The path is longer and it is usually not a straight line connection. Actual tester ground noise of up to 800mV is common when testing high-performance byte wide memories. This noise can be measured easily with a high bandwidth oscilloscope by attaching the scope ground to the actual test system ground and monitoring the DUT ground pin with one channel.

Excessive ground noise creates several problems: First, this noise is capacitively coupled to the input drive signals through the DUT input capacitances; if large enough, DC coupling through the DUT input clamp diodes can occur (Figure 7). The DUT output levels are, of course, referenced to the DUT ground potential whereas the receiver board is referenced to test system ground, introducing inaccuracy in access time measurements, etc.

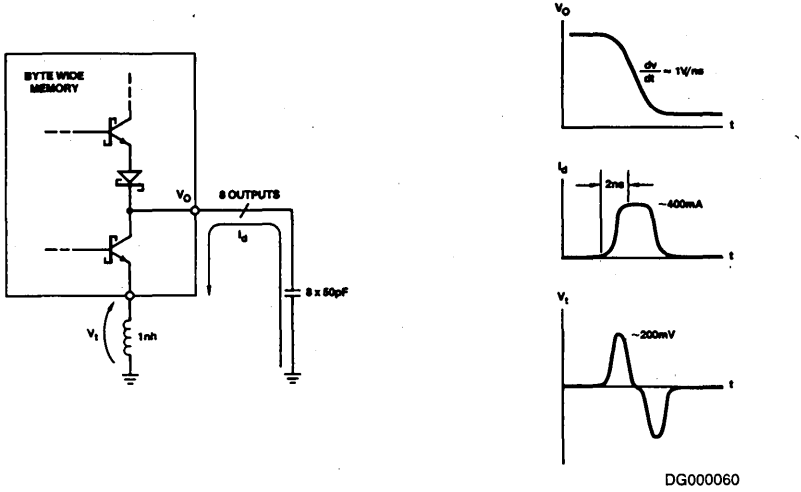
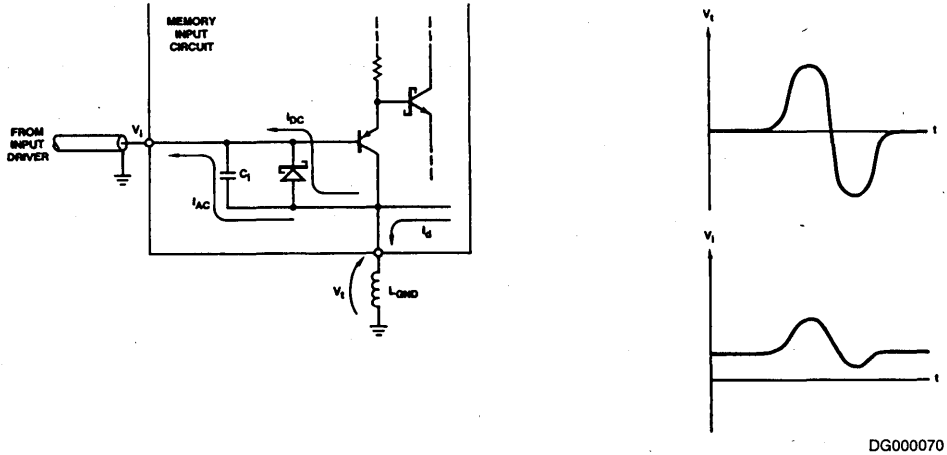


Figure 6. Byte Wide Memory Ground Transients



For small magnitudes of noise, V_t, noise is AC coupled to the inputs through the input capacitance, C_i. If V_i is low, large positive values of V_t may momentarily forward bias the input clamp diode, creating a DC coupling.

Figure 7. Ground Noise Coupling to the Inputs

7

Worst of all, severe ground noise can make functional testing at or near the guaranteed input levels (V_{IH} and V_{IL}) impossible. To demonstrate, assume the device ground noise reaches a positive 0.8V with respect to test system ground during output switching. Assume the input driver high level is programmed to 2.0V, minimum V_{IH} for most TTL devices. The actual voltage between a "high" DUT input and its ground is only 1.2V. The typical room temperature threshold voltage of a TTL device is 1.5V, and the device interprets 1.2V as a logic "low." This causes the memory to access a new memory location momentarily. The resultant momentary change in output data interferes with access time measurements. In severe cases, this momentary switching of output data creates additional ground noise which also feeds back to the inputs resulting in sustained oscillations. This noise interaction can also be viewed with a dual trace oscilloscope as shown in Figure 8. Channel A of the scope is connected to the address input while channel B monitors the DUT ground pin. The input voltage, as seen by the DUT, can be viewed directly by putting the scope in "A – B," algebraic subtract mode. Note the scope ground is connected to test system ground as before. Attaching scope ground to the DUT pin ground should be avoided as this creates a "ground loop." If connected this way, large noise currents flow in the alternate ground path provided by the scope back to earth ground; this interferes with the scope's ability to measure high-speed events and modifies the condition which is to be observed.

Several techniques can be employed to reduce ground noise problems:

- Keep the ground path as short as possible; use large diameter wire and "straight line" wiring techniques.
- Minimize the number of series connections in the DUT ground path; provide as many parallel ground connections as possible through each remaining connector.
- If the system uses a Kelvin (force – sense) ground system, terminate the system by shorting force to sense on the DUT load board. Kelvin systems provide DC accuracy, but their response times are much too slow to aid in the suppression of ground noise at the test site. Terminating Kelvin early sacrifices a little DC accuracy, but the ability to use the previous sense line as second, low impedance ground path usually improves the overall test accuracy.
- Provide multiple high frequency bypass capacitors as close as possible to the DUT, and again on the DUT load board. This allows the V_{CC} wiring to serve as an extra AC ground path for high frequency ground noise.
- Reduce the DUT load capacitance (receiver and interconnect capacitance) as much as possible; avoid using low values of load resistors. Both techniques reduce the transient currents, thus improving test accuracy. When necessary, DUT output drive capability can usually be verified with DC tests.
- If V_{IL} and V_{IH} tests are necessary, measure the maximum amount of ground noise that the specific device type to be tested generates in the actual test site. Set the input drive levels no tighter than "V_{IH} plus the maximum noise" and "V_{IL} minus the maximum noise." Using tighter limits over tests the device!
- Alternatively, use DC bench tests on a sample basis to verify that input margins are acceptable. This is a sound practice as the input thresholds of bipolar devices are extremely insensitive to fabrication process variations. Virtually any process variation or defect which would result in a threshold failure would also result in the catastrophic failure of other tests.

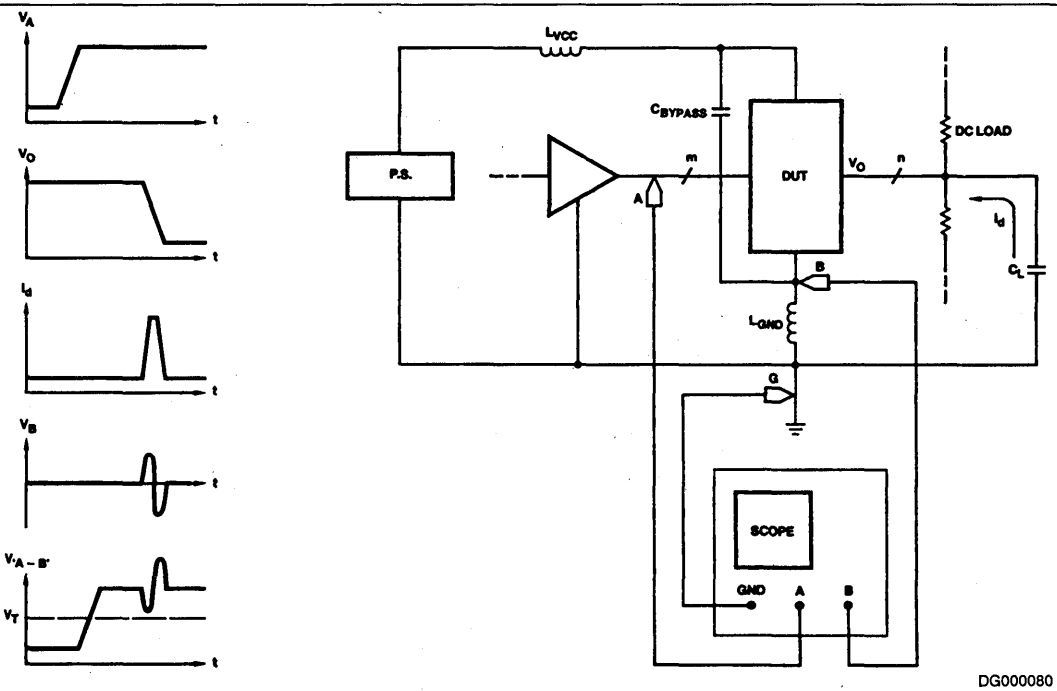


Figure 8. Monitoring Ground Noise

- DC verification of V_{IL} and V_{IH} can also be performed on the test system, but care must be exercised to insure that input voltages NEVER cross through the 0.8V to 2.0V window; voltages residing in this window can cause the DUT to switch, triggering sustained oscillations.

- The Output "Tank Circuit": A second common problem encountered is resonance in the circuitry which connects the DUT outputs to the output comparators or receivers. This resonance occurs because the wire connecting the DUT outputs to the receivers is actually an inductor connected in series with the comparator input capacitance, forming a series resonant tank circuit (Figure 9). This load circuit is quite different from the typical loading situation found in a system environment. Notice that the capacitance in the tester tends to be a single large value of capacitance, lumped at the end of the DUT output drive line. The load capacitance in the system is generally smaller and it is distributed along the drive line; this configuration looks much more like a transmission line, with per unit length values of inductance and capacitance, than it does a resonant tank. The resonant frequencies found at the test site vary with wire length and capacitive load, but tend to be in the 100 - 500MHz range. The input voltage sensed by the receiver is actually the voltage at the center connection within the tank circuit, which can ring violently when the outputs switch; measurement errors of 5ns or more can occur. A good evaluation technique for this problem is to compare the waveforms observed at the output of the device with a "shmoo plot" of the output. Assuming a simple pattern is used, differences in these results may indicate a resonance problem.

Corrective action for this problem includes:

- Use short, low inductance connections from the DUT output to the receiver; minimize comparator and interconnect capacitance. Both techniques raise the resonant frequency of the tank circuit which limits the time measurement error and reduces the DUT's ability to stimulate ringing in the tank.

- Use twisted pair wiring techniques to connect DUT outputs to the receivers. Though this raises the capacitance slightly, it reduces the purely inductive character of the interconnect, usually tending to reduce ringing.

- Minimizing Cross-Talk: Cross-talk between the input and output lines of the DUT is also a common problem. Obviously, the greater the number of paths which must be packed into a given area, the greater the problem. The signal coupling that occurs adds noise to both the input lines, making V_{IH} and V_{IL} testing difficult, and output lines, reducing the accuracy of timing measurements. Techniques which tend to reduce cross-talk include the following:

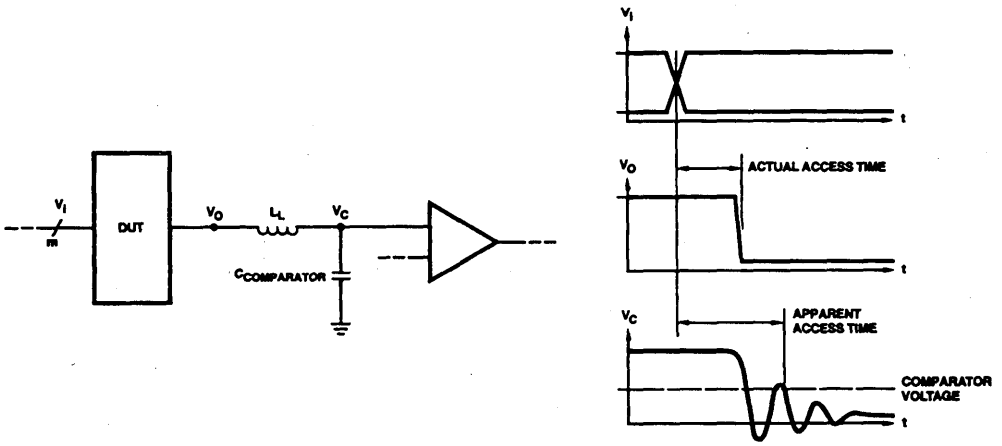
  - Keep wires as short as possible and avoid laying wires on top of each other.

  - Reduce output loading to minimize the magnitude of current transients which could be coupled into adjacent lines.

  - Use twisted pair or coaxial cable wherever possible; take care to tie all grounds from these transmission lines together at both ends.

  - Use ground plane or ground mesh techniques in the load board and the handler interface if possible. A true ground plane permits the use "strip" transmission lines which not only minimize cross-talk, but also reduce ground noise.

Though expensive, ground plane techniques offer the test engineer a consistent reference voltage which can be used to identify and segregate the various components and sources of noise.



L_L, the interconnect inductance and $C_{COMPARATOR}$ form a series resonant tank circuit which can cause time measurement errors.

Figure 9. Resonance of the Outputs

Conclusion

Advanced Micro Devices has invested significantly in the development of advanced, high-performance bipolar memory technologies and products. As the preceding discussion demonstrates, the memory tester presents a very different environment to the memory device than does the system. The additional constraints placed on the tester virtually guarantee that devices which function in this "worst case" environment will perform satisfactorily in the system. However, this worst case environment may also selectively reject the best performing devices; i.e., those with the fastest access times and best drive characteristics. This occurs because high-perfor-

mance devices magnify the problems found in the tester environment. The information presented here should aid the component engineer in recognizing and resolving these special test environment problems. Attention to these details will reward the bipolar memory user by assuring acceptance of the best and broadest range of bipolar memories currently available.

SUMMARY

The Advanced Micro Devices' bipolar memory process has been described with particular emphasis on programmable-read-only memories. An advanced form of the low-power Schottky process is used in conjunction with a highly reliable and stable platinum silicide fuse. Extensive testing and screening have been used to assure that the products will meet all specification after the user has placed his program into the device and that the circuit reliability will be outstanding.

ADVANCED MICRO DEVICES BIPOLAR PROMS

This report describes the technology used to manufacture AMD's family of Bipolar PROMs. This includes Standard PROMs from the 256 bit through the 128K level, Registered PROMs, and AMD's newest family — Diagnostic PROMs with Serial Shadow Register. Included is a discussion of the wafer fabrication in which an advanced, highly reliable platinum silicide fuse is utilized. A description of the major circuit elements and their testing is discussed as well as reliability testing and results.

AMD's families of Bipolar PROMs are manufactured in two highly advanced wafer fabrication areas located in San Antonio, Texas. One area manufactures PROMs on 5 inch diameter wafers which is very advanced for the industry. The other area is the world's first 6 inch bipolar wafer line. These two wafer fabrication areas will provide for the growing demand for Bipolar PROMs at very competitive costs for many years. In fact, AMD's commitment is to continue to be the leading supplier of Bipolar PROMs in both technology and service. Two distinct wafer fabrication processes are used — IMOX II and IMOX III. IMOX II is an advanced junction isolated process utilizing walled emitter transistors for very high speed circuits. Most circuits currently in production use the IMOX II process and it provides extremely high performance circuits with good yields. The IMOX III or "Slot" process utilizes a very narrow and deep silicon etch to create a slot in the silicon to isolate active component areas. This is the most advanced bipolar process available and will provide density and performance advantages unmatched by any other semiconductor technology available today or in the near future. depending on density and performance requirements, most new Bipolar PROM products will be designed using the IMOX III process. The circuit design concepts are similar on each of the PROM products with the result that the products can be programmed using the same hardware. Only the socket adaptor required for the PROM configuration and pin count is different. The same programming algorithm is used for all devices. The programming algorithm is also chosen to minimize programming time. The PROMs utilize a platinum Schottky diode structure with barrier metal. Dual layer metal is employed to maximize speed and minimize chip area. This applies to both the IMOX II and IMOX III process. All Advanced Micro Devices' circuits are screened to MIL-STD-883, Method 5004 class B or better, with burn-in as an option. Nearly all PROM products are on AMD's APL (approved product list) which means they meet all standard military requirements including package dimensions. AMD has also announced a new quality program called INTERNATIONAL STANDARD 500. While it is the objective to build quality into all PROM products toward an objective of zero defects, INT-STD-500 guarantees that lots shipped will not exceed a defect level of 500 parts per million.

The Process Technology

The IMOX™ II Process

THE IMOX II process is the next evolutionary step beyond the conventional bipolar Schottky process. This process utilizes platinum silicide fuses, ion implanted bases and emitters, oxide walled emitter structures, and dual layer metal. Platinum silicide continues to be the fuse material for several reasons. First, it has been demonstrated to be an extremely reliable fuse material. It does not exhibit the growback phenomenon common to nichrome technologies; it is not moisture sensitive in freeze-out tests; it is less fragile than nichrome and it does not have mass transport problems associated with moderate current densities. Second, the manufacturing process is easily controlled with regard to reliability factors and fusing currents. Third, the fuses are quite easy to form during the manufacturing process without a substantial number of additional processing steps.

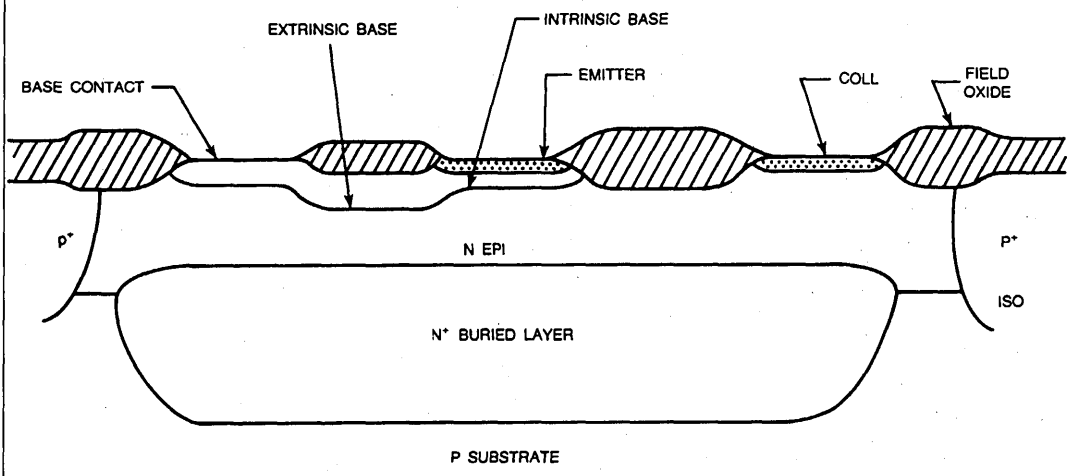


Figure 1

IMOX-II TECHNOLOGY

*IMOX is a trademark of Advanced Micro Devices, Inc.

Figure 1 is a cross section of an IMOX II transistor. A heavily doped buried layer diffusion is first performed to allow for the fabrication of NPN transistors with low saturation resistances. A thin epitaxial layer is grown. The isolation and base regions are effectively self-aligned using a composite masking approach. The combined use of localized oxidations and ion implanting result in a transistor structure where the vertical side of the emitter is walled by oxide and does not come in contact with the base. This feature greatly reduces the emitter base capacitance and significantly improves the switching speed of the transistor. A short series of steps results in the definition of polycrystalline silicon in the shape of the fuse.

Following the formation of the emitter, platinum is sputtered over the entire wafer. Since all contacts, Schottkies, and fuses are exposed at this point, an alloying operation allows platinum silicide to form. The residual platinum is etched off the wafer leaving the silicide contacts, Schottkies, and fuses. After this step, the semiconductor elements of the circuit have been completely formed, and all that remains is the interconnect metalization. To form the interconnects, aluminum is used as the primary conducting element. Aluminum has a very strong affinity for silicon, including that in platinum silicide. To retain the advantages of the very stable platinum silicide Schottky devices, it is necessary to sputter an inactive metal — tungsten — with a small amount of titanium as a bonding agent over the surface of the wafers to serve as a barrier to the diffusion or microalloying of the aluminum. Aluminum is now evaporated over the surface of the wafers and the aluminum interconnections are defined. Figure 3 shows the structure of the metal layer.

To complete the dual layer metalization structure, silicon dioxide is deposited on the wafer and etched with interlayer metal connect openings (vias). A second layer of aluminum is then placed on top of the dielectric. This layer has a thickness greater than the first one and is especially suited for power busses and output lines. To complete the circuit, a layer of nitride is deposited over the top of the wafers and etched at the appropriate locations to allow for bonding pads (see figure 2).

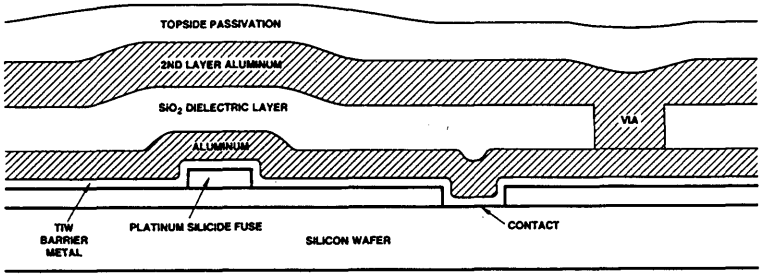


Figure 2
2-Layer Metallization Structure

The IMOX™ III (Slot) Process

Figure 3 shows a cross section of the IMOX III process. This process will be used on most new and advanced bipolar PROM products. It will provide performance and manufacturing advantages unmatched by any other semiconductor technology. The method of isolating active component areas is what makes this process different from the IMOX II process previously discussed. A reactive ion etch creates deep vertical slots in the silicon surface. These slots extend through the epi region into the substrate. A P+ channel stopping implant is placed at the bottom of the slot. An oxide is thermally grown and the slot is filled with insulating polysilicon. The surface is then planerized to provide superior metal step coverage. The remaining processing steps are very similar to the IMOX II process. This technique of isolation reduces substantially the collector to isolation spacing compared to conventional junction isolation techniques. The result is a much smaller chip size for a given memory size and greatly improved switching speeds. The lateral platinum silicide fuse design is retained because of its proven reliability and ease of manufacturing.

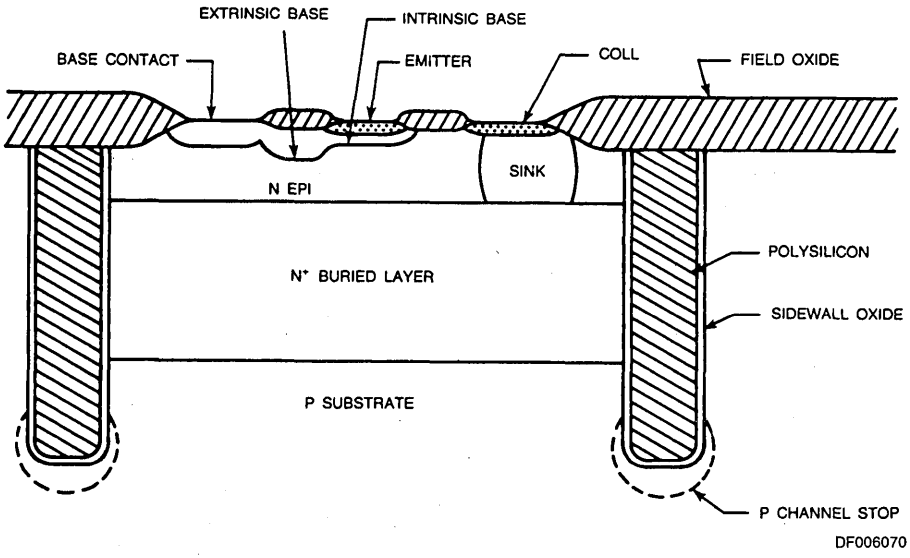


Figure 3

IMOX™ III (SLOT) TECHNOLOGY

PROGRAMMABLE READ-ONLY MEMORY CIRCUITRY

Advanced Micro Devices' bipolar PROM designs have the general configuration shown in Figure 4. Although the figure is for that of the Am27S20, the circuit techniques are the same for the entire generic family of PROMs.

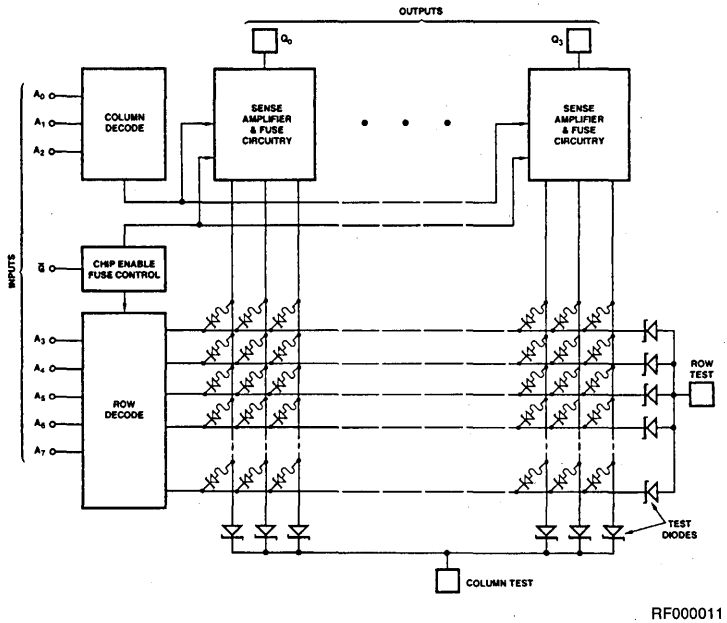


Figure 4. PROM Circuitry Block Diagram

Input, Memory & Output Circuitry

Two groups of input buffers and decoders called "X" and "Y" are used to drive word lines and columns respectively. The X-decode addresses ($A_3 - A_7$) have Schottky clamp diode protected, PNP inputs for minimum loading. (Figure 5). The X-input buffers ($A_3 - A_7$) provide A and $\overline{A}$ outputs to a Schottky decode matrix which selects one of 64 word drivers. The word line drivers are very fast high current, high voltage, non-saturating buffers providing voltage pull down to the selected word line.

The Y-decode address buffers ($A_0 - A_2$) are also Schottky diode clamped, PNP inputs driving a Schottky diode matrix. However, this diode matrix selects one of eight columns on each of the four output bits. The selected column line drives the sense amplifier input to a high level in the case of a blown fuse, or current is shunted through an unblown fuse through the selected word driver to ground resulting in a "low" input to the sense amplifier.

The sense amplifier is a proprietary fast level shifter-inverter with temperature and voltage threshold sensitivities compensated for the driving circuitry. Each of the four sense amplifiers in this circuit provides active drive to an output buffer.

Each output buffer also contains a disable input, which is driven from the chip-enable buffer. The chip-enable buffer input is a Schottky diode clamped PNP buffered design with an active pull up and pull down to drive the output buffer. Additionally, the chip-enable gate contains circuitry to provide fuse control as described below.

Fusing Circuitry

Platinum silicide fuses as implemented in Advanced Micro Devices' PROMs have extremely high fuse current to sense current ratios. Sensing normally requires that only a few hundred microamps flow through the fuse, whereas absolute minimum requirements for opening the fuse are approximately 100 times that amount. This provides a significant safety margin for transient protection and long-term reliability.

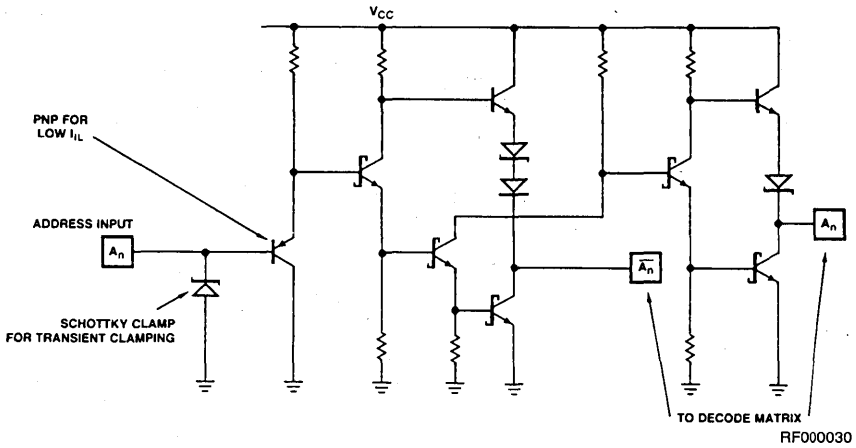


Figure 5. Input Buffer Schematic

7

High-yield fusing of platinum silicide fuses requires that a substantial current be delivered to each fuse. This current is sourced from the output terminals through darlingtons which can drive the column lines when enabled. These darlingtons are driven directly from the output and are selected by the Y-decode column select circuitry. Current during fusing flows from the output through the darlington directly to the fuse through the selected array Schottky and finally through the row-driver output transistor to ground. This path is designed for a very large fusing current safety margin.

The control circuitry works as follows: After V_{CC} is applied, the appropriate address is selected and the $\overline{G}$ input is taken to a logic high, the programmer applies 20 volts to the bit output to be programmed. The application of the 20 volts simultaneously deselects the output buffer to prevent destructive current flow, and powers down internal circuitry unneeded during fusing to minimize chip heating.

It also enables the darlington base drive circuitry, makes power available to the darlington from the output and enables the fusing control circuitry. At this point, the PROM is ready for the control line at the chip-enable pin to release the selected row driver to allow current flow through the fuse. This technique is particularly advantageous because the control signal does not supply the large fusing currents. They are supplied through the darlington from the output power supply. Some care must be taken to avoid excessive line inductance on the output line. Reasonable and normal amounts of care will reward the user with high-programming yields.

Special Test Circuitry

All Advanced Micro Devices PROMs include high-threshold voltage gates paralleling several address lines to allow the selection of special test words and the deselection of the columns to allow for more complete testing of the devices. Additionally, special test pads accessible prior to assembly allow for testing of some key attributes of the devices. The function of these special circuits will be described in more detail in the section, "Testing", later in this report.

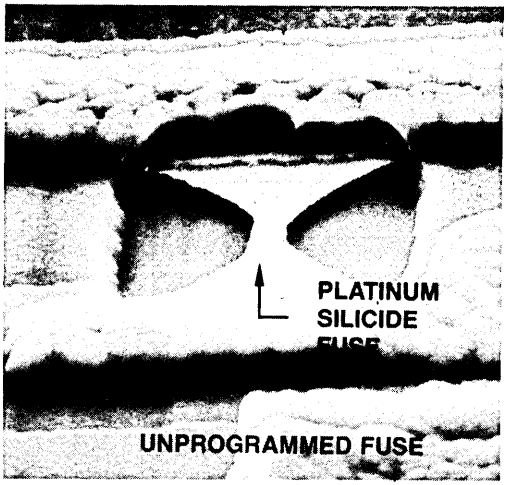
There are several advantages to this technique. First, the two high current power sources, V_{CC} and the voltage applied to the output do not have critical timing requirements. The low current chip select pin gates the fusing current into the circuit. Since it is generally desirable to gate the fusing current into the chip at relatively fast rates, the use of the chip select for this purpose avoids the speed trade-off which would exist using the output voltage as the control. The output voltage must not be raised too quickly to avoid breakdown and latchback conditions which might occur with sub-microsecond rise times on the output.

The second major advantage of this technique is that in the event that the fuse does not open during the first attempt to blow it, a near DC condition may be safely applied to it with no danger of developing a reliability problem such as that which occurs with nichrome fuses. This will be discussed in more detail later. The algorithm can therefore be designed first to minimize the time required to program the PROM, i.e. with a fast first pulse, and second, to maximize the probability that any circuit will program. Most PROMs do, of course, fuse satisfactorily with all short pulses. However, it is impossible for any manufacturer to guarantee absolutely that all fuses in all circuits receive 100 percent of the rated fusing current during programming.

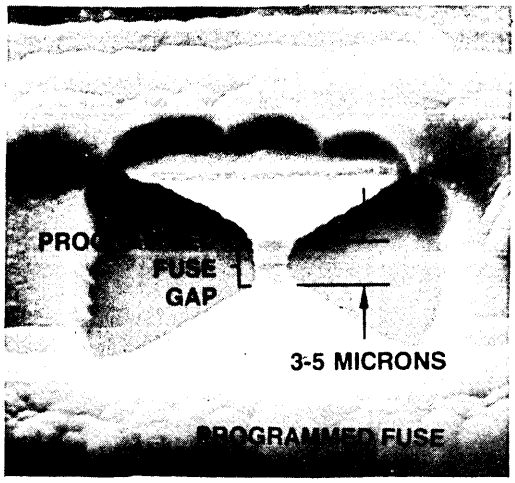
Circuit defects which may be resistant to pre-programming testing prevent such a guarantee. It is, therefore, quite important to have a fuse material insensitive to marginal conditions. Even the application of single, short pulses does not guarantee that no fuse received marginal amounts of current during fusing. The silicide fuse provides this safety margin and allows the programmer to maximize the possibility of fusing by applying near DC condition to the fuses.

Fuse Characteristics

When a fast (less than 500ns rise time) current pulse is applied to a fuse, the fuse voltage rises abruptly to a value approaching the level anticipated from calculations of the room temperature resistance. However, it quickly falls to a value of approximately two volts. This value is nearly independent of the applied current. During this period of time, typically, the fuse is molten. Very abruptly, the fuse current drops to zero indicating the separation of the platinum silicide into two distinct sections. Scanning Electron Microscope photographs of the resulting fuses (see Figure 6) indicate that the typical case is a sharp, clean separation in excess of a micron. This separation occurs in the center of the fuse because the bow-tie structure (see Figure 7) concentrates the energy density in the center away from the aluminum lines. The energy density in the center of the fuse is capable of creating temperatures substantially greater than required to melt the silicide. The very abrupt, high power applied to the fuse melts the fuse center and results in a wicking of material on either side due to surface tension.



Unprogrammed Fuse



Programmed Fuse

Figure 6.

FINAL TESTING OF ADVANCED MICRO DEVICES' MEMORIES

Wafer Level Tests

In addition to all the standard DC tests, Advanced Micro Devices performs a series of special tests to conform to the screening of criteria of MIL-STD-883, Method 5004 3.3 and the 0.05% AQL INT-STD-500. Also, AMD performs special tests to increase the confidence level of unique address selection and to demonstrate fusing capability on all columns and word drivers. To accomplish this, diodes are connected from the column lines and the word lines to special test pads which are accessible only during wafer probing. (See Figure 4). Using these diodes, Advanced Micro Devices confirms that each word driver is capable of sinking sufficient current to blow fuses, has appropriate saturation characteristics for AC performance, and has sufficient voltage breakdown to withstand fusing voltages. In addition, using special software, a sequence of tests dramatically increases the confidence of unique address selection on the address decoding. All darlingtons are checked to confirm that sufficient current drive is available to blow fuses from any column. Schottky diode array leakage is also checked to affirm that it is sufficiently low so as not to overload the pull down circuitry during the high-voltage application of fusing. Finally, high voltages are applied to the inputs and outputs to remove potentially weak devices before the PROM's are assembled.

Test Fusing

Each PROM has two additional word drivers connected to special test fuses. These test words are valuable in demonstrating beyond reasonable doubt that the device is capable of opening fuses in all columns. They also increase the confidence level in unique addressing. Furthermore, the test words serve as correlatable measures of the access times that the user can expect from his devices after he has placed his own program in the memory. These test words are not visible to the user unless he applies special voltages to certain address pins. Figure 8 is a diagram of this input circuit. One hundred percent of the PROM devices shipped from Advanced Micro Devices have had AC testing for access and enable times at high-and low-power supply voltages to affirm their AC characteristics.

The result of this extensive testing at both the wafer and finished device level is a product with very high-programming yields and virtually guaranteed AC performance after the user places his program in the parts. Additionally, the high voltage tests provide an additional level of confidence that the oxide and junction integrity is excellent in each circuit and that the devices will be relatively insensitive to small transients common to programming equipment.

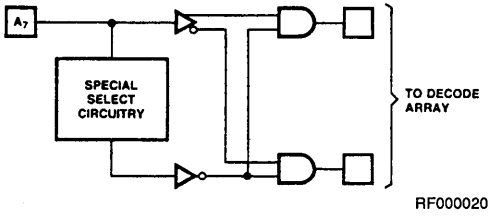


Figure 8. Special Input Circuit Used for Array Deselection and Test Word Check.

7

Reliability Testing

All new AMD products must pass strict reliability requirements prior to production release. Following qualification, the long term reliability of AMD's products is routinely assessed in AMD's Reliability Monitor Program (AMD 15-015). The monitor program in effect ensures monthly requalification of product to AMD's reliability standards & goals. Product is tested by generic groupings, all key elements of the qualification test matrix are repeated monthly, and performance to standards is reviewed by the Executive Quality Board For Bipolar PROMs, over fifty billion fuse hours have been completed with no fuse related failures.

RELIABILITY MONITOR PROGRAM FOR DEVICES IN MOLDED PACKAGES

TEST	CONDITIONS	TEST METHOD	SAMPLE SIZE	TARGET MAX FAIL RATE	ALERT LEVEL FAIL RATE
1. Infant Mortality	160 hours at 125°C or 85°C ambient(Tj < 150°C nominal) Initial and end-point electrical-QA tape	06-108	300	0.15% @ 85°C 0.20% @ 125°C	0.4% @ 85°C 0.6% @ 125°C
2. Operating Life	1000 hrs (1160 total) @ 125°C or 85°C ambient (Tj < 150°C, nominal) Initial & end-point Electrical - QA tape	06-108	120	0.2%/1k hr at 85°C 0.3%/1k hr at 125°C	1.0%/1k hr at 85°C 1.0%/1k hr at 125°C
3. Long Term Life	5,000 hrs cum @ 125°C or 85°C (Tj < 150°C, nominal) Selected from Test 2 above. Test Tape Interim point at 2k hours	06-108	120	0.2%/1k hr at 85°C 0.3%/1k hr at 125°C	1.0%/1k hr at 85°C 1.0%/1k hr at 125°C
4. Temperature and Humidity	85°C/85% RH/low power bias, 500 hours and 1000 hrs Initial, Intermin and end-point electrical QA tape	06-119	50	0.5% at 500 hrs 1.0% at 1000 hrs	2% at 500 hrs 4.0% at 1000 hrs
5. Temperature Cycle	A. 1000 cycles: −65°C to 150°C, 30 minutes/ cycle. High temperature (75°C min) Functional End-point Electrical Test	06-109	50	1.3%	4.0%
6. Pressure Cooker	121°C 15psi, 160 hours, unbiased. Initial end-point electrical	06-120	50	1.0	4.0%

RELIABILITY MONITOR PROGRAM FOR DEVICES IN HERMETIC PACKAGES

TEST	CONDITIONS	TEST METHOD	SAMPLE SIZE	TARGET MAX FAIL RATE	ALERT LEVEL FAIL RATE
1. Infant Mortality	160 hours at 125°C ambient Initial and end-point electrical test – QA tape	06 – 108	300	0.2%	0.4%
2. Operating Life	1000 hrs (1160 total) at 125°C ambient Initial and end-point electrical test – QA tape	06 – 108	120	0.2%/1k hr	1.0%/1k hr
3. Long Term Life	5,000 hrs cum, Selected Test 2 groups, same conditions and test tapes Interim point at 2k hours	06 – 108	120	0.2%/1k hr	1.0%/1k hr
4. Temperature Cycle	1000 cycles, (–65° to 150°C), 30 min/cycle end-point-hermeticity and electrical test QA tape	06 – 109	50	0.7%	2%
5. 150°C Operating Life	1000 hours at 150°C ambient Initial and end-point electrical – QA tape	06 – 108	50	0.6%/1k hr	3.0%/1k hr

Bipolar PROMs as Programmable Logic Products

Selection Guide

PART NUMBER	INPUTS	OUTPUTS	PRODUCT TERMS	REGISTERED OUTPUTS	t_{PD}/I_{CC} $t_{SU}/t_{CP-Q}/I_{CC}$ COM'L (MAX)
Am27S19A	5	8	32		25ns/115mA
Am27S19SA	5	8	32		15ns/115mA
Am27S21A	8	4	256		30ns/130mA
Am27S13A	9	4	512		30ns/130mA
Am27S29A	9	8	512		35ns/160mA
Am27S25A	9	8	512	8	30ns/20ns/185mA
Am27S25SA	9	8	512	8	25ns/12ns/185mA
Am27S33A	10	4	1024		35ns/140mA
Am27S65*	10	4	1024	4	30ns/15ns/165mA
Am27S65A*	10	4	1024	4	23ns/10ns/165mA
Am27S281A	10	8	1024		35ns/185mA
Am27S35A	10	8	1024	8	35ns/20ns/185mA
Am27S37A	10	8	1024	8	35ns/20ns/185mA
Am27S185A	11	4	2048		35ns/150mA
Am27S75*	11	4	2048	4	30ns/15ns/175mA
Am27S75A*	11	4	2048	4	25ns/12ns/175mA
Am27S291A	11	8	2048		35ns/185mA
Am27LS291	11	8	2048		30ns/90mA
Am27S291SA	11	8	2048		20ns/185mA
Am27S45A	11	8	1024	8	40ns/20ns/185mA
Am27S45SA	11	8	1024	8	25ns/10ns/185mA
Am27S47A	11	8	1024	8	40ns/20ns/185mA
Am27S47SA	11	8	1024	8	25ns/10ns/185mA
Am27S41A	12	4	4096		35ns/185mA
Am27S85*	12	4	4096	4	35ns/15ns/185mA
Am27S85A*	12	4	4096	4	27ns/12ns/185mA

*These devices contain SSR™ on chip diagnotics

GENERIC PROGRAMMING INFORMATION

Advanced Micro Devices Bipolar PROMs are members of a generic series incorporating common programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable platinum-silicide fuse technology. Utilizing an easily implemented programming algorithum, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-silicide was selected as the fuse link material to achieve a well-controlled melt rate resulting in large non-conductive gaps that ensure very stable long term high reliability. Extensive operating testing has proven that this low-field, large gap technology offers the best reliability for fusible link PROMs.

High-yield fusing of the platinum-silicide fuses require that a substantial current be delivered to the decoded and selected fuse. The fusing current path has been designed to provide a large fusing current safety margin. This, however, generates large current transients at the time the fuse enable input goes to V_{IHH}, and a proportional current decrease at the time the fuse opens. The magnitude of this current change may be between 50 and 150 mA with rise and fall times of 2 – 10 ns. Some care must be taken to avoid excessive line inductance in the output lines of the device (V_{CCO} for ECL devices) as well as the ground line to the device in order to maximize fusing yields.

The PROMs may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device for more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip, including V_{CC}, should be removed for a period of 5 seconds after which programming may be resumed.

PROM Programming Equipment Guide*

Advanced Micro Devices has an ongoing program of evaluation and qualification of PROM programming equipment from various hardware manufacturers. Qualification by AMD implies that the equipment has been evaluated for proper implementation of the programming algorithm presented at the device socket pins. Programming yield analysis on a limited sample size is also evaluated to meet expected, results of AMD.
Manufacturers listed below have been qualified on the particular equipment listed only. Not all manufacturers have implemented AMD's complete product line. Please contact your local AMD sales representative for up-to-date information regarding manufacturers implementation status.

DATA I/O 10525 Willows Road N.E. Redmond, Wa. 98052 (206) 881-6444	Systems 19, 29, & 100 Model 22	UniPak UniPak II UniPak IIB
Digilec, Inc. 1602 Lawrence Avenue Ocean, N.J. 07712 (201) 493-2420	Model UPP-803	FAM-12
Kontron Electronics 630 Price Avenue Redwood City, Ca. 94063 (415) 361-1012	Model EPP-80 Model MPP-80S	MOD 14
Oliver Advanced Engineering 320 W. Arden, Suite 220. Glendale, Ca. 91203 (818) 240-0080	OMNI 64	
Stag Systems, Inc. 528-5 Weddell Drive Sunnyvale, Ca. 94086 (408) 745-1991	Model PPX Model PP17	PM 2000
Valley Data Sciences, Inc. 2426 Charleston Road Mt. View, Ca. 94043 (415) 968-2900	Series 160	

Software support for PROMs as programmable logic products is available from the following companies, please contact the indicated company for the status of their particular product:

Assisted Technology, Inc. (CUPL)
2381 Zanker Road, Suite 150
San Jose, Ca. 9513
(408) 942-8787

DATA I/O (ABEL) (PROMLINK)
10525 Willows Road N.E.
Redmond, Wa. 98052
(206) 881-6444

7

Publication # 05065 Rev. B Amendment /0
Issue Date: May 1986

TTL PROM Programming Procedure

Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1. V_{CC} power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to one output;
5. The fuse enable voltage is raised to enable a high-threshold voltage gate. This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The output voltage is lowered (the programming voltage removed);
7. The device is enabled and the bit sensed to verify that the fuse has blown. In the unusual event that the fuse does not verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse verifies as open;
8. The sequence of 2 through 7 must be repeated for each fuse which must be opened.
9. At the conclusion of programming, the device should be verified for correct data at all addresses with two (2) V_{CC} supply voltages (V_{CC} = 5.7 V & V_{CC} = 4.4 V.).

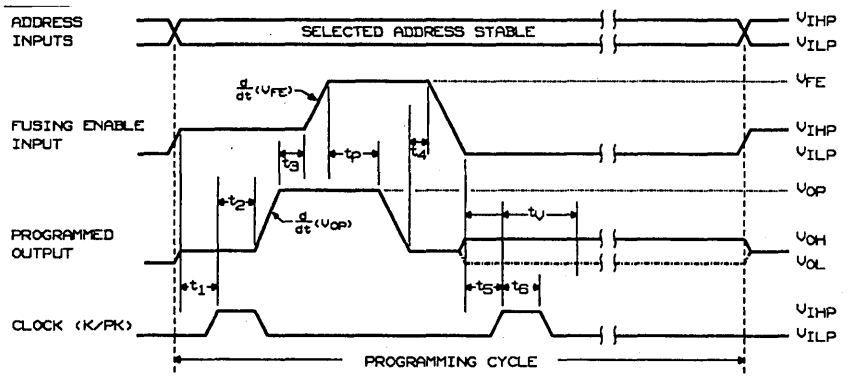
NOTES ON PROGRAMMING

1. All delays between edges are specified from the completion of the first edge to the beginning of the second edge, not the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1.5 μS are recommended to minimize heating during programming.
3. During t_V, the output being programmed is switched to the load R and read to determine if additional programming pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.
5. All output enable pins, except the output enable used as the Fusing Enable Input, should be held at V_{ILP} for $\overline{G}_n$ inputs and V_{IHP} for G_n inputs.

PROGRAMMING PARAMETERS T_A = 25°C

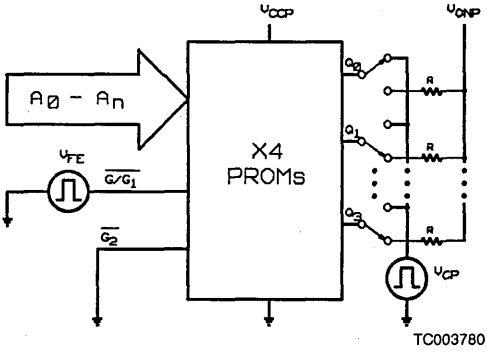
Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{IHH}	Control Pin Extra High Level @ 10 – 40 mA	14.5	15	15.5	Volts
V_{FE}	Fusing Enable Voltage @ 10 – 40 mA	14.5	15	15.5	Volts
V_{OP}	Program Voltage @ 15 – 200 mA	19.5	20	20.5	Volts
V_{IHP}	Input High Level During Programming and Verify	2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify	0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50 – 200 mA	5	5.2	5.5	Volts
dV_{OP}/dt	Rate of Output Voltage Change	20		250	V/μs
dV_{FE}/dt	Rate of Fusing Enable Voltage Change	20		1000	V/μs
t_p	Fusing Time First Attempt	10	50	100	μs
	Fusing Time Subsequent Attempts	1	5	10	ms
$t_1 - t_6$	Delays Between Various Level Changes	100		1500	ns
t_V	Period During which Output is Sensed for V_{Blown} Level		500		ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed	V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed	0.2	2	5.1	KΩ

PROGRAMMING WAVEFORMS



WF022020

PROGRAMMING 4 Bit WIDE TTL PROMs

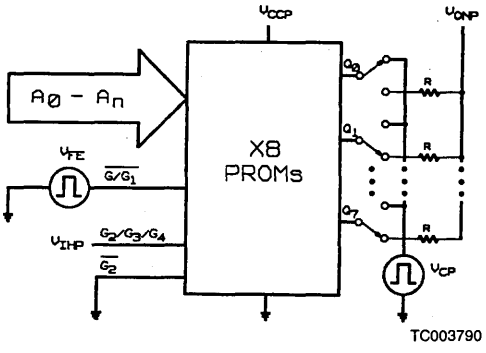


TC003780

SIMPLIFIED PROGRAMMING DIAGRAM

Part Number	Fuse Enable Pin
Am27S20/21	$\overline{G_1}$
Am27S12/13	$\overline{G}$
Am27S32/33	$\overline{G_1}$
Am27S184/185	$\overline{G}$
Am27S40/41	$\overline{G_1}$

PROGRAMMING 8 Bit WIDE TTL PROMs



TC003790

SIMPLIFIED PROGRAMMING DIAGRAM

Part Number	Fuse Enable Pin
Am27S15	$\overline{G_1}$
Am27S18/19	$\overline{G}$
Am27S28/29	$\overline{G}$
Am27S280/281	$\overline{G_1}$
Am27S290/291	$\overline{G_1}$
Am27S31	$\overline{G_1}$
Am27S180/181	$\overline{G_1}$
Am27S190/191	$\overline{G_1}$
Am27S43	$\overline{G_1}$
Am27S49	$\overline{G_1}$
Am27S51	$\overline{G_1}$

7

PROGRAMMING 4-WIDE REGISTERED PROMs

The 4-bit wide Registered PROMs are programmed according to the generic TTL programming algorithm. This algorithm specifies a clock at the beginning of the programming cycle to establish output data states & enable register state. A second clock occurs prior to verification to bring programmed data to the outputs. The fuse enable input is the MODE (M) input. The DK input and all enable inputs ($\overline{G}$ & $\overline{G}/\overline{GS}$) should be held at a logic LOW throughout programming and verification. On the Am27S95 the G_2 input should be held at a logic HIGH.

In addition to the programmable fusible link array these devices contain two (2) architecture fuses to program the $\overline{\text{Enable}}$ and the $\overline{\text{Initialize}}$ input functionality. Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification. This verification circuitry is enabled by holding the SD input at V_{IHH} throughout programming and verification. The two-bit architecture word will then program the functionality of the respective inputs according to Table 1.

Table 1

Architecture Data Word (Hex)	Am27S65, Am27S75, and Am27S95 Input Function		Am27S85 Input Function
	$\overline{G}/\overline{GS}$ Input	$\overline{I}/\overline{IS}$ Input	$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ Input
0	Asynchronous $\overline{\text{Enable}}$ ($\overline{G}$)	Asynchronous $\overline{\text{Initialize}}$ ($\overline{I}$)	Asynchronous $\overline{\text{Enable}}$ ($\overline{G}$)
4	Asynchronous $\overline{\text{Enable}}$ ($\overline{G}$)	Synchronous $\overline{\text{Initialize}}$ ($\overline{IS}$)	Asynchronous $\overline{\text{Initialize}}$ ($\overline{I}$)
8	Synchronous $\overline{\text{Enable}}$ ($\overline{GS}$)	Asynchronous $\overline{\text{Initialize}}$ ($\overline{I}$)	Synchronous $\overline{\text{Enable}}$ ($\overline{GS}$)
C	Synchronous $\overline{\text{Enable}}$ ($\overline{GS}$)	Synchronous $\overline{\text{Initialize}}$ ($\overline{IS}$)	Synchronous $\overline{\text{Initialize}}$ ($\overline{IS}$)

These Registered PROMs all have an additional 4-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

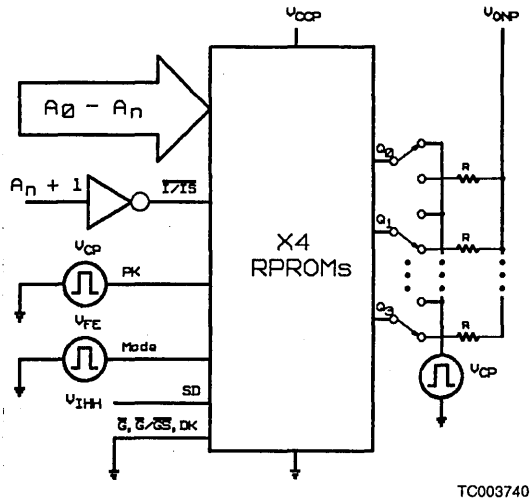
These parts use the initialize ($\overline{I}/\overline{IS}$) pin as a select control between the array and the architecture & initialize words. Initialize ($\overline{I}/\overline{IS}$) HIGH enables the array for programming and disables the architecture & initialize words. Initialize ($\overline{I}/\overline{IS}$) LOW enables the architecture & initialize words for programming and disables the array.

An easy implementation for programming the architecture & initialize words would be to invert the next higher address input ($A_n + 1$) from the PROM programmer and apply this signal to the initialize ($\overline{I}/\overline{IS}$) input pin. The array, architecture, and initialize words could then be programmed over a continuous address field according to Table 2.

Table 2

Device	$\overline{I}/\overline{IS}$ Pin	Array Programming Address Field (Hex)	Architecture Word Address (Hex)	Initialize Word Address (Hex)
Am27S65	$\overline{A_{10}}$	000 thru 3FF	400	401
Am27S75	$\overline{A_{11}}$	000 thru 7FF	800	801
Am27S85	$\overline{A_{12}}$	0000 thru 0FFF	1000	1001
Am27S95	$\overline{A_{13}}$	0000 thru 1FFF	2000	2001

PROGRAMMING 4 Bit WIDE Registered PROMs



TC003740

SIMPLIFIED PROGRAMMING DIAGRAM

Part Number	Fuse Enable Pin
Am27S65	(M) MODE
Am27S75	(M) MODE
Am27S85	(M) MODE
Am27S95	(M) MODE

PROGRAMMING 8 - WIDE REGISTERED PROMs

The 8-bit wide registered PROMs, with the exception of the Am27S55, are programmed according to the generic TTL programming algorithm. This algorithm specifies a clock at the beginning of the programming cycle to establish output data states & enable register state. A second clock occurs prior to verification to bring programmed data to the outputs. The fuse enable input is the asynchronous enable ($\overline{G}$) input. The synchronous enable input ($\overline{GS}$) on all parts is held at a logic LOW.

The Am27S35, Am27S37, Am27S45, & Am27S47 all have an additional 8-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

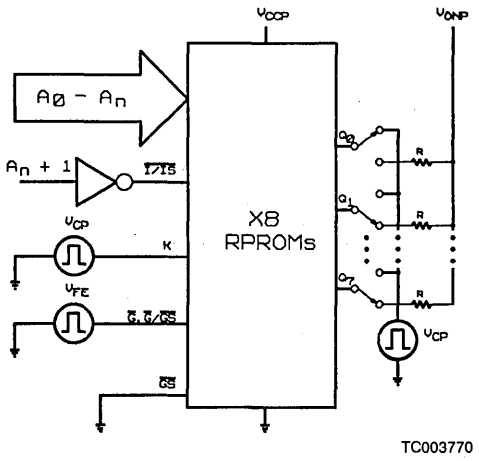
These parts use the initialize ($\overline{I}/\overline{IS}$) pin as a select control between the array and the initialize word. Initialize ($\overline{I}/\overline{IS}$) HIGH enables the array for programming and disables the initialize word. Initialize ($\overline{I}/\overline{IS}$) LOW enables the initialize word for programming and disables the array.

An easy implementation for programming the initialize word would be to invert the next higher address input ($A_n + 1$) from the PROM programmer and apply this signal to the initialize ($\overline{I}/\overline{IS}$) input. The array and initialize word could then be programmed over a continuous address field according to Table 1.

TABLE 1

Device	$\overline{I}/\overline{IS}$	Array Programming Address Field (Hex)	Initialize Word Address (Hex)	$\overline{G}/\overline{GS}$ Word Address (Hex)
Am27S35-Am27S37	$\overline{A_{10}}$	000 thru 3FF	400	N/A
Am27S45-Am27S47	$\overline{A_{11}}$	000 thru 7FF	800	801

PROGRAMMING 8 Bit WIDE Registered PROMs



TC003770

SIMPLIFIED PROGRAMMING DIAGRAM

Part Number	Fuse Enable Pin
Am27S27	$\overline{G}$
Am27S25	$\overline{G}$
Am27S35	$\overline{G}$
Am27S45	$\overline{G}/\overline{GS}$

PROGRAMMING the Am27S55 8-WIDE REGISTERED PROM

The Am27S55 is programmed according to a modified TTL programming algorithm. This algorithm specifies a clock at the beginning of the programming cycle which transitions between a TTL LOW level and V_{IHH} to establish output data states & enable register state. A second clock, at normal TTL levels, occurs prior to verification to bring programmed data to the outputs. The fuse enable input is the multifunctional ($\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$) input.

In addition to the programmable fusible link array this device contains two (2) architecture fuses to program the $\overline{Enable}$ or the $\overline{Initialize}$ input functionality. Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification. This verification circuitry is enabled by holding the A_1 input at V_{IHH} throughout programming and verification of the architecture & initialization fuses. The two-bit architecture word will then program the functionality of the $\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ pin to one of the input functions according to Table 1.

Table 1

Architecture Data Word (Hex)	Input Function
	$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$ Input
00	Asynchronous $\overline{Enable}$ ($\overline{G}$)
01	Synchronous $\overline{Enable}$ ($\overline{GS}$)
02	Asynchronous $\overline{Initialize}$ ($\overline{I}$)
03	Synchronous $\overline{Initialize}$ ($\overline{IS}$)

This product has an additional 8-bit word which may be programmed to provide any arbitrary microinstruction for system initialization. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

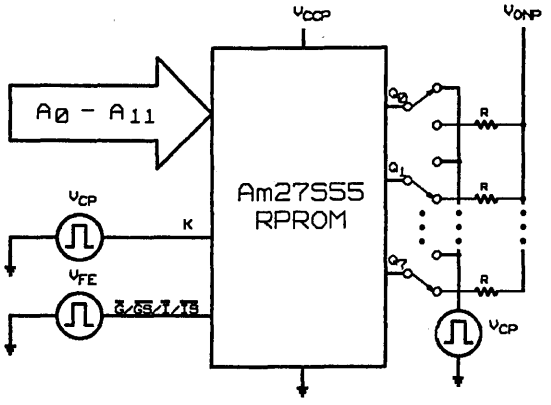
This part uses the address input (A_1) as a select control between the array and the architecture & initialize words. A_1 at either a TTL LOW or HIGH enables the array for programming and disables the architecture & initialize words. A_1 when taken to a V_{IHH} level enables the architecture & initialize words for programming and disables the array.

An easy implementation for programming the architecture & initialize words would be to have the next higher address input ($A_n + 1$). A_{12} in this case, from the PROM programmer used to enable a V_{IHH} HIGH level for the A_1 input pin. The array, architecture, and initialize words could then be programmed over a continuous address field according to Table 2.

Table 2

Device	A_1 (V_{IHH}) Enable Control Pin	Array Programming Address Field (Hex)	Architecture Word Address (Hex)	Initialize Word Address (Hex)
Am27S55	A_{12}	0000 thru 0FFF	1000	1001

PROGRAMMING the Am27S55

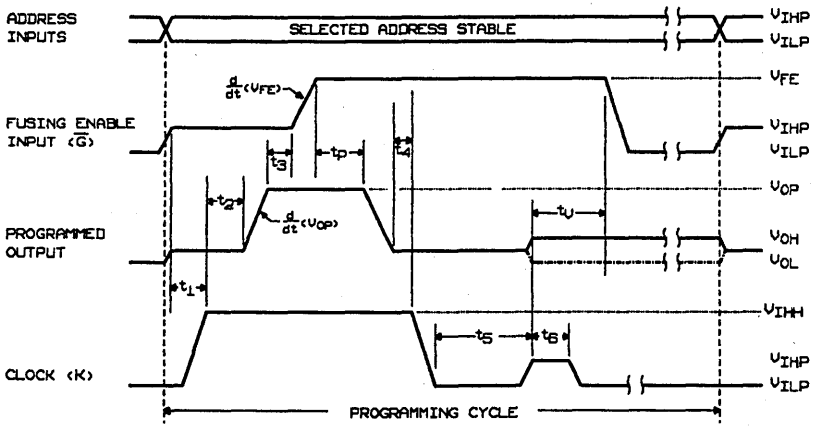


TC003760

Part Number	Fuse Enable Pin
Am27S55	$\overline{G}/\overline{GS}/\overline{I}/\overline{IS}$

SIMPLIFIED PROGRAMMING DIAGRAM

Am27S55 PROGRAMMING WAVEFORMS



WF022010

7

ECL PROM Programming Procedure

Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1. V_{CC} power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to V_{CCO};
5. The output to be programmed is raised to V_{FE}. This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The programming voltage (V_{CP}) is lowered and the fuse enable voltage (V_{FE}) is removed from the output.
7. The device is enabled and the bit sensed to verify that the fuse has blown. In the unusual event that the fuse does not verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse verifies as open;
8. The sequence of 2 through 7 must be repeated for each fuse which must be opened.
9. At the conclusion of programming, the device should be verified for correct data at all addresses with two (2) V_{EE} supply voltages ($V_{EE} = -4.2$ V, & $V_{EE} = -5.7$ V.).

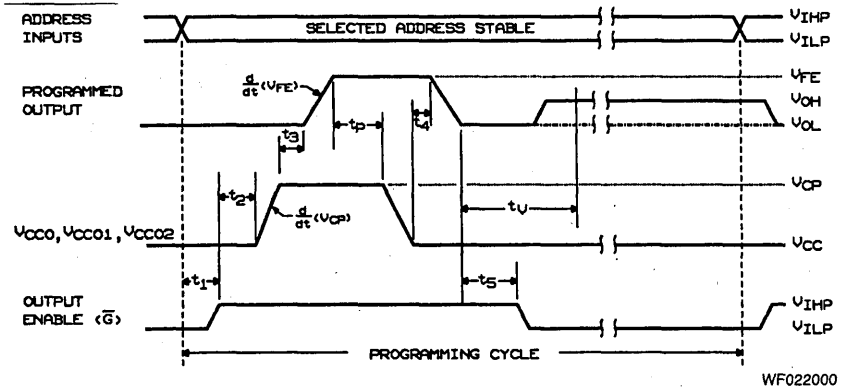
NOTES ON PROGRAMMING

1. All delays between edges are specified from the completion of the first edge to the beginning of the second edge, i.e., not the midpoints.
2. Delays t_1 through t_5 must be greater than 100 ns; maximum delays of 1.5 μs are recommended to minimize heating during programming.
3. During t_V, the output being programmed is switched to the load R and read to determine if additional programming pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING PARAMETERS $T_A = 25°C$

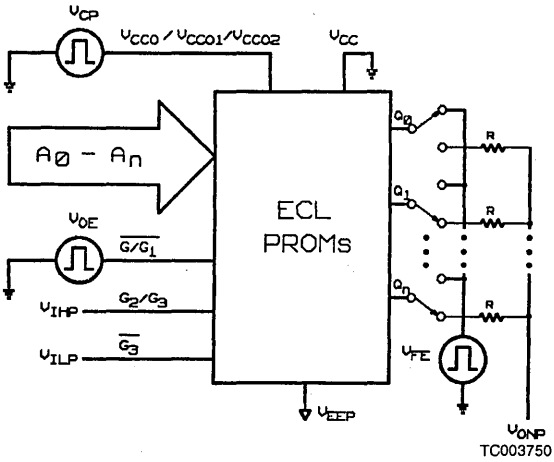
Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{FE}	Fusing Enable Voltage (Applied to Outputs) @ 10 mA	1.60	1.80	2.00	Volts
V_{CP}	Program Voltage @ 15 – 200 mA	14.5	15	15.5	Volts
V_{IHP}	Input High Level During Programming and Verify	–1.2	–1.0	–0.8	Volts
V_{ILP}	Input Low Level During Programming and Verify	–1.85	–1.65	–1.45	Volts
V_{EEP}	V_{EE} During Programming @ $I_{EE} = 50 – 400$ mA	–5.4	–5.2	–5.0	Volts
dV_{OP}/dt	Rate of Program Voltage Change	20		250	V/μs
dV_{FE}/dt	Rate of Fusing Enable Voltage Change	20		1000	V/μs
t_p	Fusing Time First Attempt	40	50	100	μs
	Fusing Time Subsequent Attempts	4	5	10	ms
$t_1 – t_5$	Delays Between Various Level Changes	100		1500	ns
t_V	Period During Which Output is Sensed for V_{Blown} Level		500		ns
V_{ONP}	Pull-Down Voltage for Outputs (During Programming)	0.0	0.0	0.0	Volts
	Pull-Down Voltage for Outputs (During Verification)	–2.1	–2.0	–1.8	Volts
R	Pull-Down Resistor On Outputs Not Being Programmed	1.8	2.0	2.2	KΩ

PROGRAMMING WAVEFORMS



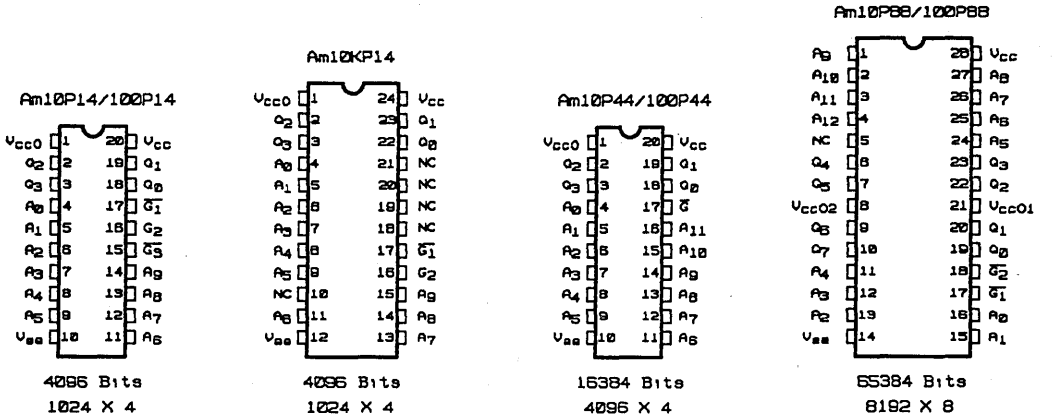
WF022000

PROGRAMMING ECL PROMs



TC003750

SIMPLIFIED PROGRAMMING DIAGRAM



CD00986O

Guide to the Analysis of Programming Problems

Application Note
by
AMD Bipolar Memory Product Engineering

INTRODUCTION

Advanced Micro Devices' Generic Series of Programmable Read Only Memory (PROM) circuits have been designed to provide extremely high programming yields. Available programming currents are over designed by a factor of four and special circuitry accessible only during testing is incorporated into each product to eliminate ordinarily difficult to detect shorts and opens in the array and decoders. As a result, unique decoding and very large fusing currents are virtually assured to the user. AMD PROMs have test fuses programmed prior to shipment as a further guarantee. The results of such extensive testing and design considerations are programming yields consistently in the 98% to 99.5% range.

Key to the achievement of such yields is a programmer properly calibrated to the AMD specification with good contactors, "clean" electrical wave forms and properly functioning subcircuits. In the event that your programming yields fall below 98%, you should investigate the characteristics of the failed devices to find a prominent failure mode, then use the attached information as a guide to resolving the problem. Simple problems can be very costly if not detected and corrected.

Should you continue to have trouble optimizing your programming yield, contact your AMD representative or local programmer manufacturer representative.

Guide to the Analysis of Programming Problems

Primary Symptom	Secondary Symptom	Possible Causes
I) Units fail to program all desired bits	A) Binary blocks of missing data	1) Address driver output which remains continuously low or continuously high. 2) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V. 3) Poor, intermittent or no electrical contact to one or more address input pins. Any of the above may result in over programming half the array and not programming the other half.
	B) Random bits of missing data	1) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V. 2) Poor electrical contact to address, chip enable and output pins. 3) Excessive transient noise on V_{CC}, output pin (> 20.5V), or ground pins. Check with a high speed storage oscilloscope for peak values during programming. Use transient suppression networks where appropriate. 4) Programmer does not comply with AMD Programming Specification. (See Programming Parameters.) Examples: — Output voltage during programming less than 19.5V — V_{CC} during programming less than 5.0V — $\overline{G}$ voltage during programming less than 14.5V
	C) All data associated with a single output missing	1) Poor or no electrical contact to that output pin. 2) Defective current switch in programmer.
	D) No data change	1) Wrong device or programming socket. 2) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.) Examples: — Output voltage during programming less than 19.5V — V_{CC} during programming less than 5.0V — $\overline{G}$ voltage during programming less than 14.5V

Publication # 03305 | Rev. C | Amendment /0
Issue Date: May 1986

Primary Symptom	Secondary Symptom	Possible Causes
II) Over-Programmed Devices	A) One output continuously at a Logic "1"	1) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.) Examples: — Output voltage during programming greater than 20.5V — Programmer timing incorrect
		2) Open outputs can appear to be programmed to Logic "1" with the presence of a pullup resistor even though the device has not actually been programmed.
		3) Excessive voltage transients on output lines during programming. Be sure appropriate transient suppression networks are placed on the outputs.
	B) All outputs continuously at a Logic "1"	1) No V_{CC} applied to device.
		2) No ground applied to device.
		3) Incorrect device type.
		4) Incorrect programming socket.
		5) Excessive voltage transients on output lines. Use transient suppression network shown in Figure 1.

DEFINITIONS

Fuse

— Conductive Platinum-Silicide link used as a memory element in Advanced Micro Devices' PROM circuits.

Unprogrammed Bit

— A conductive fuse.

Programmed Bit

— A nonconductive fuse, that is one which has been opened.

Output Low (Logic "0")

— An output condition created by an unprogrammed bit.

Output High (Logic "1")

— An output condition created by a programmed bit.

Failure to Program

— A device failure in which a fuse selected to be opened failed to open during the fusing operation.

Over Programmed

— A device failure in which a fuse which was not selected to open nevertheless opened during the fusing operation.

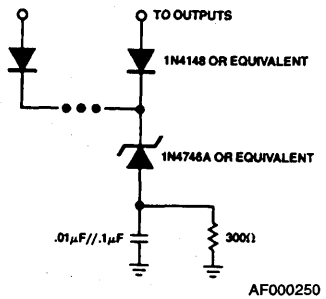
Address Driver

— The voltage source which drives an individual address pin in the PROM. This source is part of the programmer and drives the address pin with "0"s (0V to .45V) and "1"s (2.4V to 5.5V) depending on instructions from the programmer control circuitry. There is a separate address driver for every PROM address pin.

Programmer

— A system capable of providing the appropriate array of signals to a PROM circuit to cause certain user controlled bits to be programmed (i.e., fuses opened) in the device. As a minimum it consists of a memory containing the pattern to be programmed, control circuitry to sequence the addressing and fusing control pulses, power supplies, and address drivers.

TRANSIENT SUPPRESSION NETWORK



AF000250

Notes: 1. Clamp diodes should be connected to each output as close as physically possible to the device pin.
2. V_{CC} should be decoupled at the device pin using .01μF//.1μF capacitors.
3. AMD recommends that all address pins be decoupled using .001μF capacitors.

7

03305B

ADVANCED MICRO DEVICES
DOMESTIC SALES OFFICES

ALABAMA	(205) 882-9122
ARIZONA,	
Tempe	(602) 242-4400
Tucson	(602) 792-1200
CALIFORNIA,	
El Segundo	(213) 640-3210
Newport Beach	(714) 752-6262
San Diego	(619) 560-7030
Sunnyvale	(408) 720-8811
Woodland Hills	(818) 992-4155
COLORADO	(303) 741-2900
CONNECTICUT	(203) 264-7800
FLORIDA,	
Altamonte Springs	(305) 339-5022
Clearwater	(813) 530-9971
Ft Lauderdale	(305) 484-8600
Melbourne	(305) 729-0496
GEORGIA	(404) 449-7920
ILLINOIS	(312) 773-4422
INDIANA	(317) 244-7207
KANSAS	(913) 451-3115
MARYLAND	(301) 796-9310
MASSACHUSETTS	(617) 273-3970
MINNESOTA	(612) 938-0001
NEW JERSEY	(201) 299-0002
NEW YORK,	
Liverpool	(315) 457-5400
Poughkeepsie (IBM only)	(914) 471-8180
Woodbury	(516) 364-8020
NORTH CAROLINA	(919) 847-8471
OREGON	(503) 245-0080
OHIO,	
Columbus	(614) 891-6455
PENNSYLVANIA,	
Allentown (AT&T only)	(215) 398-8006
Willow Grove	(215) 657-3101
PUERTO RICO	(809) 764-4524
TEXAS,	
Austin	(512) 346-7830
Dallas	(214) 934-9099
Houston	(713) 785-9001
WASHINGTON	(206) 455-3600
WISCONSIN	(414) 782-7748

INTERNATIONAL SALES OFFICES

BELGIUM,		
Bruxelles	TEL:	(02) 771 99 93
	FAX:	(02) 762-3716
	TLX:	61028
CANADA, Ontario,		
Kanata	TEL:	(613) 592-0090
Willowdale	TEL:	(416) 224-5193
	FAX:	(416) 224-0056
FRANCE,		
Paris	TEL:	(01) 45 60 00 55
	FAX:	(01) 46 86 21 85
	TLX:	202053F
GERMANY,		
Hannover area	TEL:	(05143) 50 55
	FAX:	(05143) 55 53
	TLX:	925287
München	TEL:	(089) 41 14-0
	FAX:	(089) 406490
	TLX:	523883
Stuttgart	TEL:	(0711) 62 33 77
	FAX:	(0711) 625187
	TLX:	721882
HONG KONG,		
Kowloon	TEL:	3-695377
	FAX:	1234276
	TLX:	50426
ITALY, Milano	TEL:	(02) 3390541
	FAX:	(02) 3498000
	TLX:	315286
JAPAN, Tokyo	TEL:	(03) 345-8241
	FAX:	3425196
	TLX:	J24064AMDTKOJ
LATIN AMERICA,		
Ft. Lauderdale	TEL:	(305) 484-8600
	FAX:	(305) 485-9736
	TLX:	5109554261 AMDFTL
SWEDEN, Stockholm	TEL:	(08) 733 03 50
	FAX:	(08) 733 22 85
	TLX:	11602
UNITED KINGDOM,		
Manchester area	TEL:	(0925) 828008
	FAX:	(0925) 827693
	TLX:	628524
London area	TEL:	(04862) 22121
	FAX:	(04862) 22179
	TLX:	859103

NORTH AMERICAN REPRESENTATIVES

CALIFORNIA	
I^2 INC	OEM (408) 988-3400 DISTI (408) 496-6868
IDAHO	
INTERMOUNTAIN TECH MKGT	(208) 888-6071
INDIANA	
SAI MARKETING CORP	(317) 241-9276
IOWA	
LORENZ SALES	(319) 377-4666
MICHIGAN	
SAI MARKETING CORP	(313) 227-1786
NEBRASKA	
LORENZ SALES	(402) 475-4660
NEW MEXICO	
THORSON DESERT STATES	(505) 293-8555
NEW YORK	
NYCOM, INC	(315) 437-8343
OHIO	
Dayton	
DOLFUSS ROOT & CO	(513) 433-6776
Strongsville	
DOLFUSS ROOT & CO	(216) 238-0300
PENNSYLVANIA	
DOLFUSS ROOT & CO	(412) 221-4420
UTAH	
R^2 MARKETING	(801) 595-0631

ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA
TEL: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 5388450

ADVANCED MICRO DEVICES

To keep you informed of new product developments, we would like to add you to our mailing list. If you are already on our list, please pass this card along to a colleague.

I am interested in receiving Advanced Micro Devices information on a regular basis.

Last Name | Initials | Title

Company | Division

Street Address | Mail Stop

City | State | Zip

1. The principle end products manufactured at this location are aimed at the following markets:
(Check one only)

1.1 ☐ Industrial/Commercial
1.2 ☐ Computer/Business Machine
1.3 ☐ Data Communications
1.4 ☐ Government/Military/ Aerospace
1.5 ☐ Consumer
1.6 ☐ Telephony
1.7 ☐ Other or N/A

2. My principle job function is:
(Check one only)

2.1 ☐ General Management (Non-Engineering)
2.2 ☐ Engineering Management
2.3 ☐ Design Engineering
2.4 ☐ Reliability/Quality Assurance
2.5 ☐ Manufacturing/Production
2.6 ☐ Purchasing/Procurement
2.7 ☐ University
2.8 ☐ Other _____

Products of interest to me:
(Check all that apply)

DD ☐ ISDN
MM ☐ Modem
NN ☐ Bipolar RAMs
OO ☐ Bipolar PROMs
PP ☐ EPROMs/EEPROMs
QQ ☐ CMOS/MOS RAMs (Static and Dynamic)
RR ☐ Bipolar Gate Arrays
SS ☐ CMOS Gate Arrays/Standard Cells
II ☐ Bipolar/CMOS PAL® Products
CC ☐ MOS Microprocessors and Peripherals
AA ☐ Bipolar Microprocessors and Controllers
BB ☐ Digital Signal Processing
EE ☐ Office Automation/Networking
GG ☐ Interface/Logic/Transceivers
JJ ☐ Mass Storage
LL ☐ Display and Graphics

For AMD use only
Sales Code _____
Salesman _____

Order #[illegible]518E

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 465 SUNNYVALE, CA

POSTAGE WILL BE PAID BY ADDRESSEE

ADVANCED MICRO DEVICES, INC.

P.O. Box 3453
901 Thompson Place
Sunnyvale, California 94088

ADVANCED MICRO DEVICES, INC.
901 Thompson Place
P.O. Box 3453
Sunnyvale,
California 94088
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306
TOLL FREE
(800) 538-8450

ISSN 0888-4714

07606A

AIS-RRD-80M-6/86-0