ExpressROM™ Memory

1989 Data Book

Advanced Micro Devices

Advanced Micro Devices

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1989 Databook

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For over ten years Advanced Micro Devices has been an industry leader in EPROM technology. We were the first to introduce the 512K EPROM and the 1 Megabit EPROM, we offer the most complete selection of high speed (<100ns) CMOS EPROMs, and we are the first company to convert our entire commercial product line to advanced CMOS technology. Now, in order to help our customers get more bytes-for-the-buck, AMD has created a new concept — ExpressROM memories. These wafer-programmed EPROMs offer users a low cost alternative for EPROMs without the long time-to-market associated with ROMs.

If you're looking for EPROM cost savings and your codes aren't changing, consider ExpressROM devices, the ROMs without the wait.

Walid Magribi
Product Line Director
Non-Volatile Memory Division

Rich Forte
Division Vice President
Non-Volatile Memory Division

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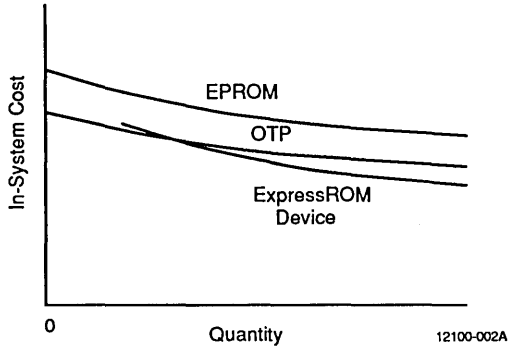
Introduction to ExpressROM Memory

Advanced Micro Devices

ExpressROM memories are an exciting new product family created by Advanced Micro Devices to offer the system manufacturer a cost savings over standard EPROMs while eliminating many of the disadvantages associated with traditional ROMs. These new memory products provide a lower cost alternative for volume production with stable codes.

ExpressROM devices are delivered pre-programmed in a low cost plastic package and are 100% compatible with the EPROMs they replace. They address two critical needs of system manufacturers which are vital in today's marketplace: reduced cost and time-to-market. Typically ExpressROM devices become cost-effective at volumes of 5000 units and offer leadtimes as short as 3-4 weeks.



Pricing Relationships Between ExpressROM Device/EPROM/OTP

ExpressROM wafers are manufactured with the same process as standard AMD EPROMs with one important exception. Since the devices will be pre-programmed with a single code they do not need the transparent topside passivation used on OTP (One Time Programmable) EPROMs. Instead the wafers are coated with a cost-effective nitride topside. This passivation is acknowledged industry-wide as the highest quality protection for plastic encapsulated CMOS devices not requiring UV erasure. Since a standard EPROM die is used, you are assured that the ExpressROM family is identical in architecture, density, and pinout to both AMD's current and future generations of high performance CMOS EPROMs.

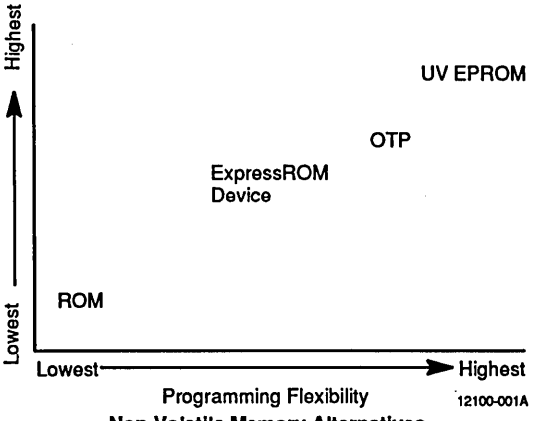
Prior to receipt of a custom code ExpressROM wafers are inventoried untested and unprogrammed. Upon verification of your code the wafers are sorted, packaged and tested. Since your ExpressROM devices are programmed at wafer sort, every device can be rigorously tested with your code under both AC and DC operating conditions prior to shipment. Also, because ExpressROM memories are shipped board-ready with factory guaranteed quality your ship-to-stock or Just-In-Time programs can be easily implemented. At Advanced Micro Devices, we ship them the way you want them — ready for your system. And, there are none of the delays, costs or risks normally associated with custom ROM masks and wafer production.

Non-Volatile Memory Alternatives

	UV EPROM	OTP	ExpressROM Device	ROM
Leadtime	Manufactures Leadtime	Manufactures Leadtime	4 Weeks	8 - 12 Weeks
Set-up Charge	No	No	No	Yes
Minimum Quantity	0	0	5K to 10K	25K
Fully Tested Custom Pattern	No	No	Yes	Yes
User Programming Required	Yes	Yes	No	No
Auto Insertion	No	Yes	Yes	Yes
Flexibility	Total	Can Not Reprogram	Fixed 4 Weeks Prior To Use	Fixed 8 - 12 Weeks Prior to Use

Plastic packaging inherently provides a cost savings over standard EPROMs packaged in expensive windowed ceramic DIPs. Due to simplified test requirements, ExpressROM devices can even cost less than unprogrammed OTP EPROMs. However component price is only a small part of your true in-system cost. ExpressROM devices allow you to eliminate or reduce costs in several other areas: programming, testing and production. Since ExpressROM memories are delivered with your code, you will reap savings by eliminating programming costs and associated yield losses. Incoming inspection may often be eliminated since your ExpressROM devices have been thoroughly tested and are guaranteed to operate to full specifications with your code! Additional in-house cost savings can be attained by using automatic insertion equipment in lieu of manual placement into sockets.

ExpressROM devices were designed to provide a low cost alternative for EPROM users without the liabilities of other non-volatile memory alternatives. Although ROMs have a lower component cost, they are economically feasible only at high volume and have the risks of long leadtimes and limited manufacturing flexibility. While OTP EPROMs offer the systems manufacturer the ability to respond to varying codes during production, they force the user to incur additional and sometimes hidden costs.



Non-Volatile Memory Alternatives

Our mission at AMD is to deliver you the service and products you demand to build the cost competitive systems that are needed to win in your markets. The ExpressROM memory provides this opportunity. As one of the world's five largest IC manufacturers and the first to market with a 1 megabit EPROM, we appreciate the value of efficient manufacturing. Compressing time-to-market cycles, improving yields and providing high levels of quality are invaluable strategies for today's manufacturer. At Advanced Micro Devices we are proud to offer another tool to give our customers this strategic advantage, the ExpressROM memory: the ROM without the wait!

ORDERING ExpressROM DEVICES

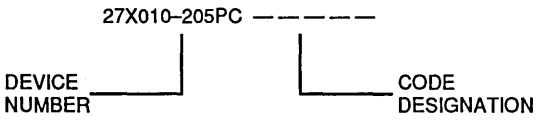
The following are guidelines for ordering an ExpressROM device. For more information, contact your local AMD sales representative.

1) SEND IN THE CODE

Please send your sales representative two EPROMs containing identical copies of the code. To minimize the verification turnaround process, use EPROMs with JEDEC-approved pinouts identical in architecture and density as the ExpressROM device being ordered.

2) AMD CHECKS THE CODE

We check that both EPROMs contain the same code to make certain there was not a mix-up in shipping your codes to the factory as well as ensuring that the integrity of your code has been preserved. After confirming this, a unique 5-digit code designation is assigned. The ordering part number is formed by adding the 5-digit code designation as a suffix to the ExpressROM device number. See below:



3) AMD GENERATES A VERIFICATION EPROM

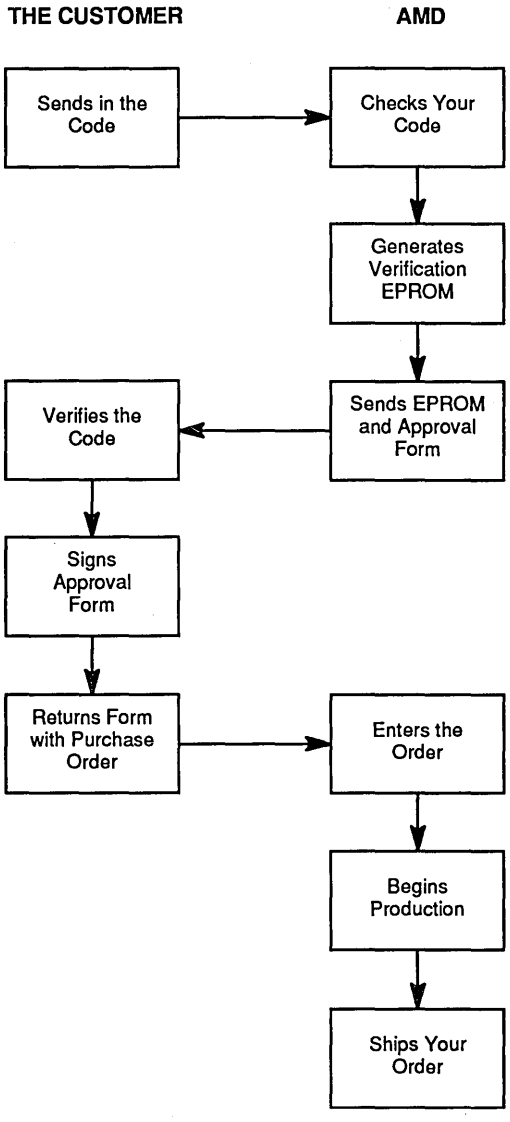
After the check is completed, we duplicate the code and return it to you for verification.

4) CONFIRM THE CODE

The verification EPROM and the code approval form should be back in your hands for final approval before production within 3 days. Sign the approval form and return it to AMD.

5) THE ORDER IS ENTERED

Upon receipt of the authorized code approval form and a purchase order, the order is entered and production is initiated. Delivery is scheduled per the negotiated leadtime.



TERMS AND CONDITIONS

You should be aware of the following guidelines when order ExpressROM devices. Please note that the exact terms and conditions can be found on the code approval form available from your local sales representative.

1) AMD will maintain customer code confidentiality.
2) AMD will absorb all initial set-up cost.
3) All orders are subject to minimum quantities.
4) AMD requires 8 weeks notification for code changes. The customer is liable for all work-in-process.
5) No schedule chages may be made within 30 days of current schedule date. Otherwise any line item may be rescheduled ±30 days from the original schedule date.
6) The customer will accept shipments of line items ±5.

Final

Am27X64

8,192 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **OTP EPROM alternative:**
  - Factory programmed
  - Fully tested and guaranteed
  - Low cost
- **Mask ROM alternative**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High performance CMOS technology**
  - Fast access time — 100 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier**

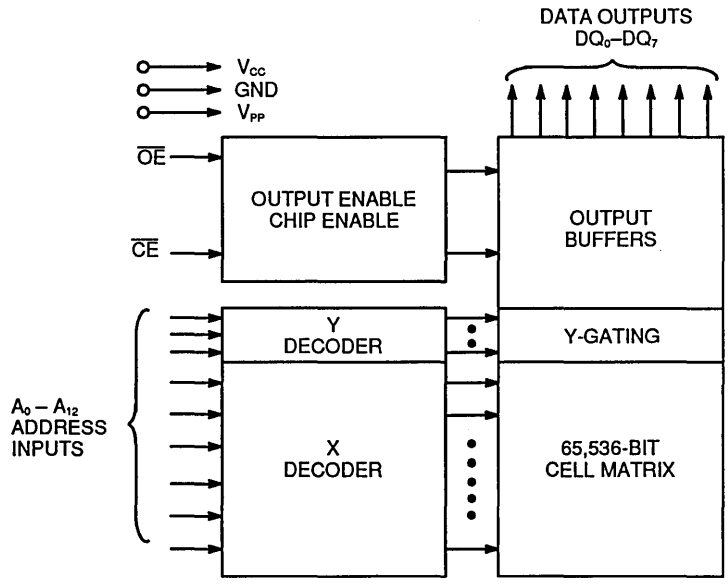
GENERAL DESCRIPTION

The Am27X64 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 8,192 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X64 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

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Publication # 12084 Rev. B Amendment/0
Issue Date: April 1989

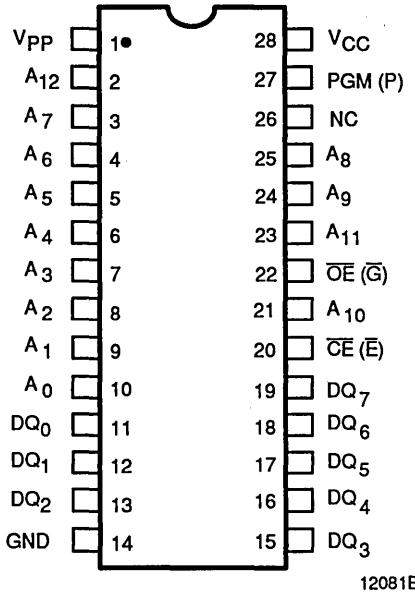
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X64					
Ordering part No:						
±5% VCC Tolerance	-105	-125	-155	-205	-255	-305
±10% VCC Tolerance	—	-120	150	-200	-250	-300
Max Access Time (ns)	100	120	150	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75	100	120

CONNECTION DIAGRAMS

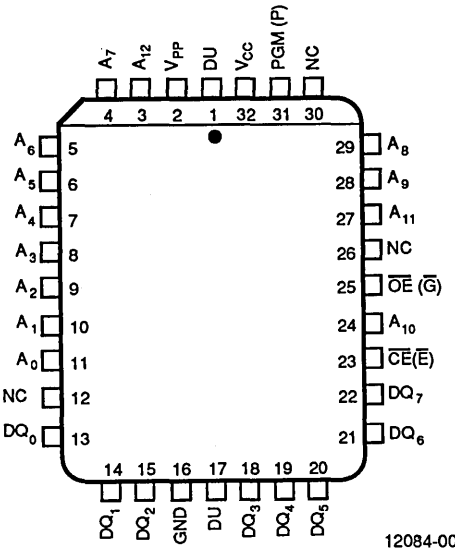
Top View

PLASTIC DIP



12081B-002

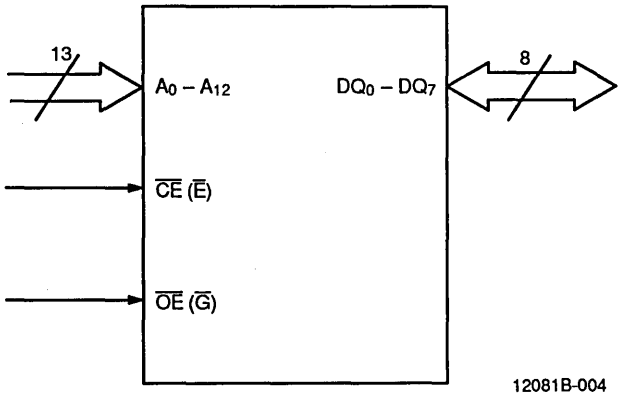
PLCC



12084-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

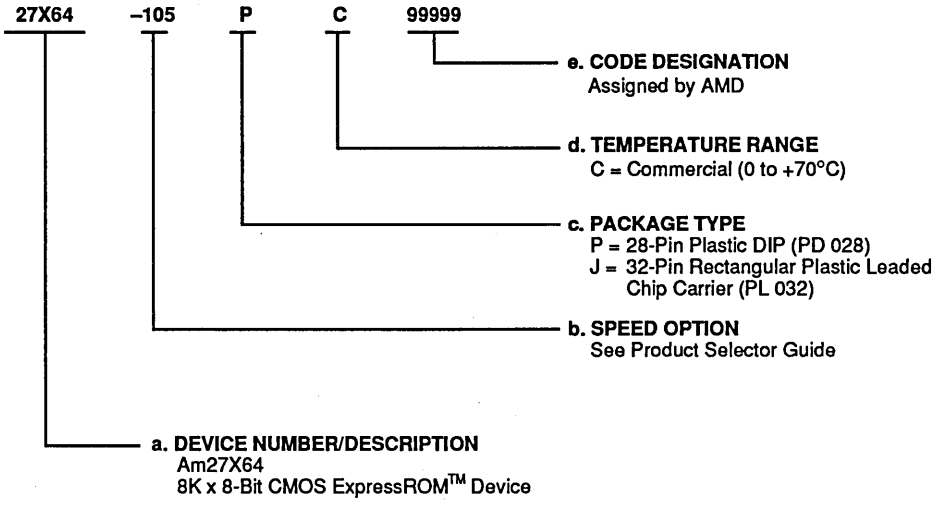
PIN DESCRIPTION

$A_0 - A_{12}$	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
$DQ_0 - DQ_7$	= Data Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
PGM (P)	= Enable Input
V_{PP}	= V_{PP} Supply Voltage
V_{CC}	= V_{CC} Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
27X64-105 27X64-120 27X64-125 27X64-150 27X64-155 27X64-200 27X64-205 27X64-250 27X64-255 27X64-300 27X64-305	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X64 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X64 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM™ device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	PGM	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	V_{CC}	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	V_{CC}	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to 125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC} and V_{PP}	–0.6 to V_{CC} +0.5 V
V_{CC} and V_{PP}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

Minimum DC voltage on input or output is –0.5 V. During transitions, the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T)	0 to +70°C

Supply Read Voltages:

V_{CC} /V_{PP} for Am27X64–XX5	+4.75 to +5.25 V
V_{CC} /V_{PP} for Am27X64–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, 6 and 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CCPP}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$		100	µA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 1, 2 and 5)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	20	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X64 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
7. Maximum active power usage is the sum of I_{CC} and I_{PP}.
8. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

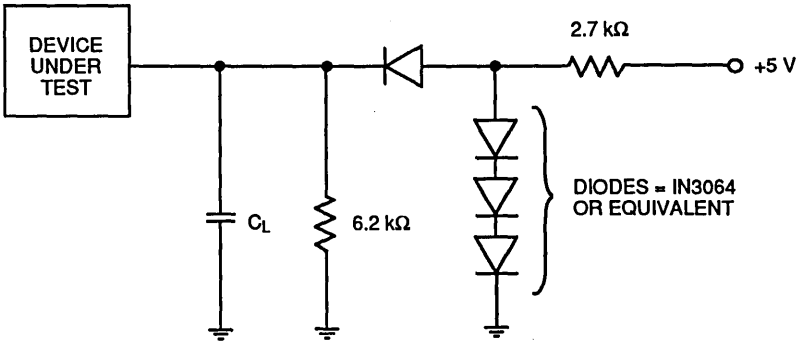
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbol		Parameter Description	Test Conditions			–120	–150	–200	–250	–300	
JEDEC	Standard				–105	–125	–155	–205	–255	–305	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.							ns
				Max.	100	120	150	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.							ns
				Max.	100	120	150	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.							ns
				Max.	40	50	65	75	100	120	ns
t_{EHQZ} t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 1)		Min.							ns
				Max.	30	35	50	55	60	75	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first		Min.	0	0	0	0	0	0	ns
				Max.							ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X64 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

SWITCHING TEST CIRCUIT



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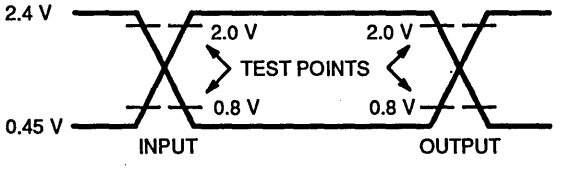
C_L = 100 pF including jig capacitance

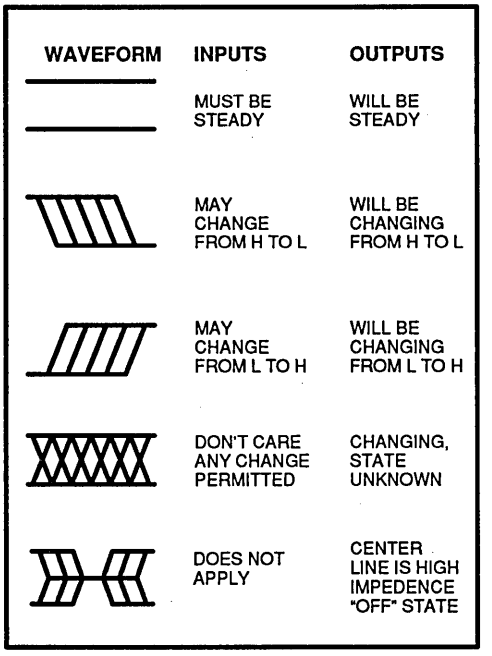
SWITCHING TEST WAVEFORM



12081B-006

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS



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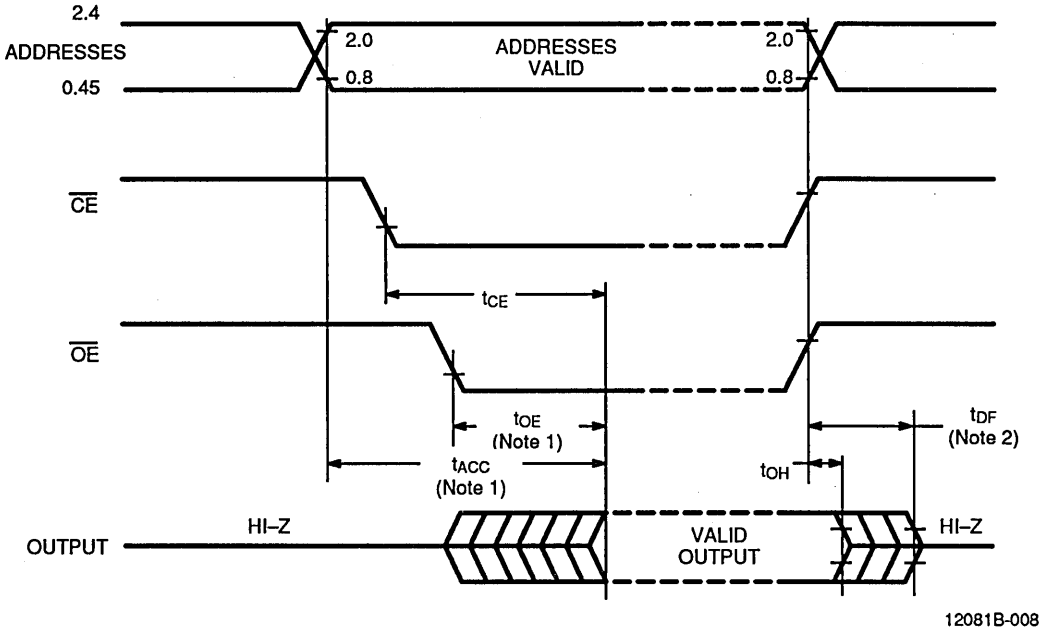
SWITCHING WAVEFORMS



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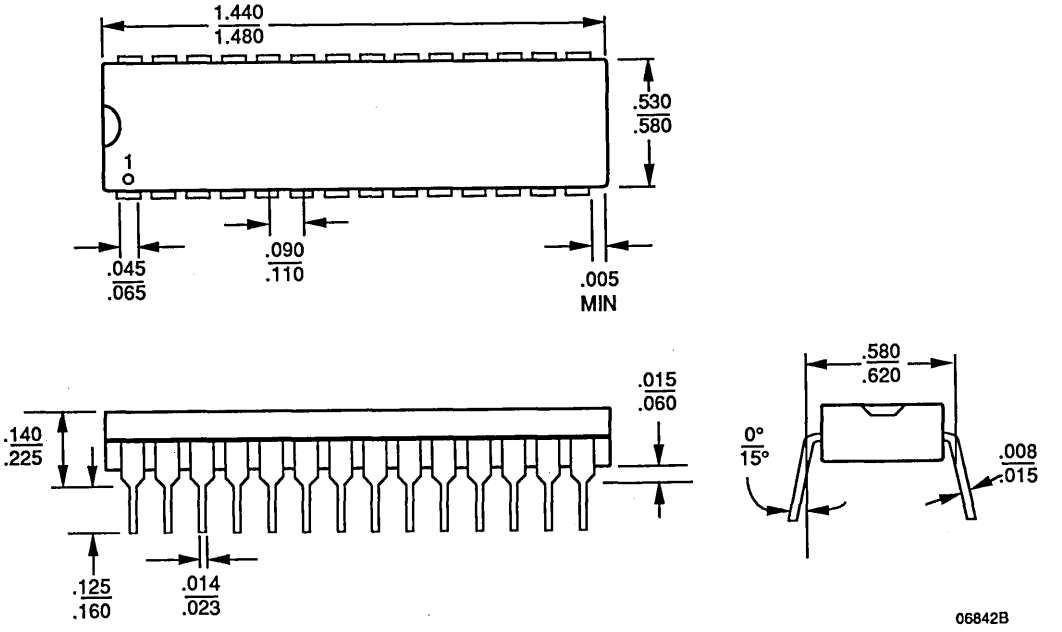
Note:

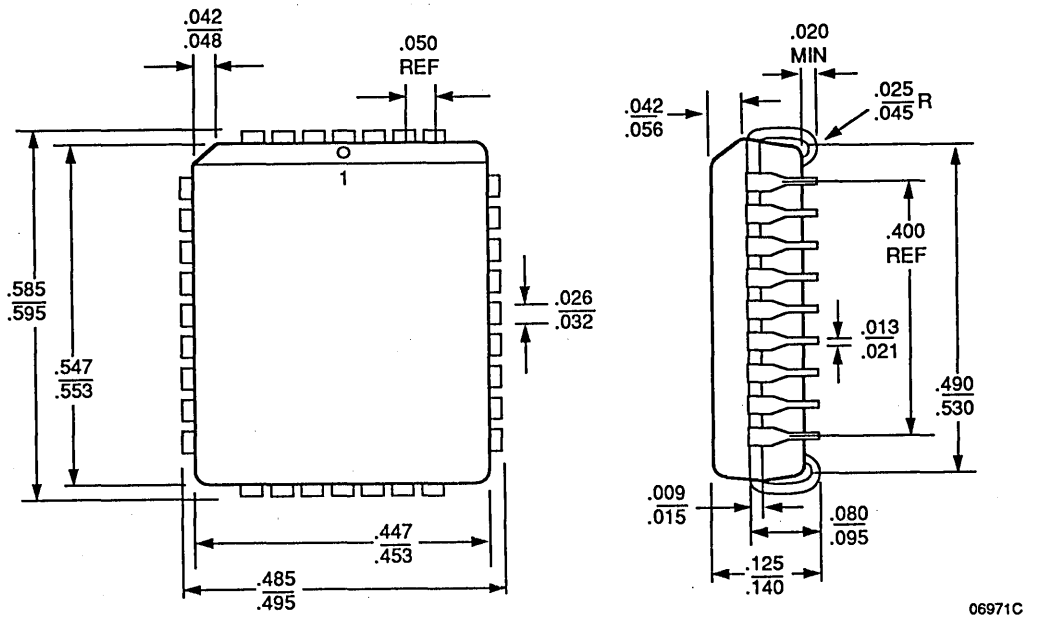
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PHYSICAL DIMENSIONS

PD 028



PL 032



Final

Am27X128

16,384 x 8-Bit ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **OTP EPROM alternative:**
  - Factory programmed
  - Fully tested and guaranteed
  - Low cost
- **Mask ROM alternative**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High performance CMOS technology**
  - Fast access time — 100 ns
  - Low power dissipation
    100 μA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier**

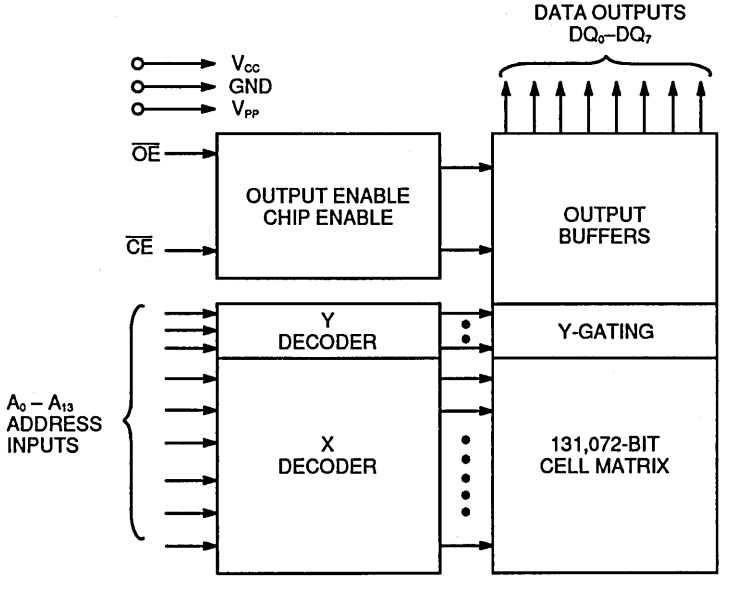
GENERAL DESCRIPTION

The Am27X128 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 16,384 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X128 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 μW in standby mode.

BLOCK DIAGRAM



12081B-001

ExpressROM is a trademark of Advanced Micro Devices Inc.

Publication # 12083 Rev. B Amendment/0
Issue Date: April 1989

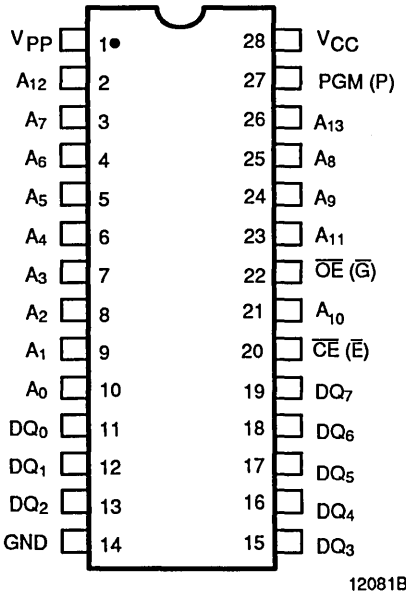
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X128					
Ordering part No:						
±5% VCC Tolerance	-105	-125	-155	-205	-255	-305
±10% VCC Tolerance	—	-120	-150	-200	-250	-300
Max Access Time (ns)	100	120	150	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75	100	120

CONNECTION DIAGRAMS

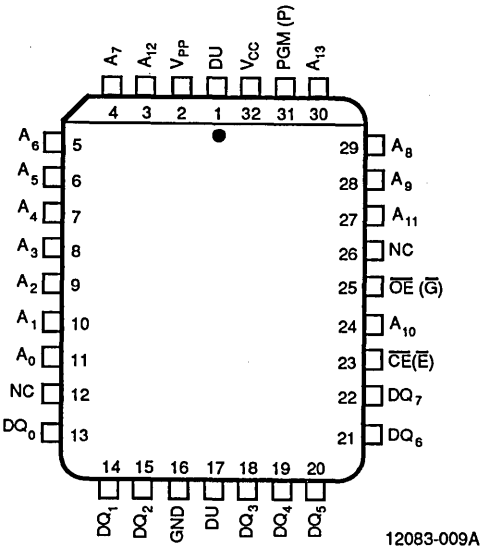
Top View

PLASTIC DIP



12081B-002

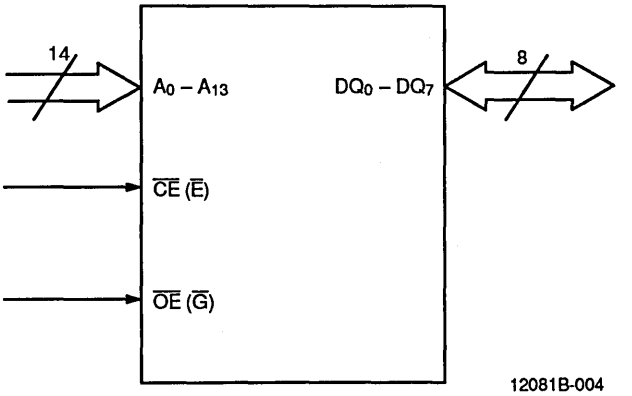
PLCC



12083-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

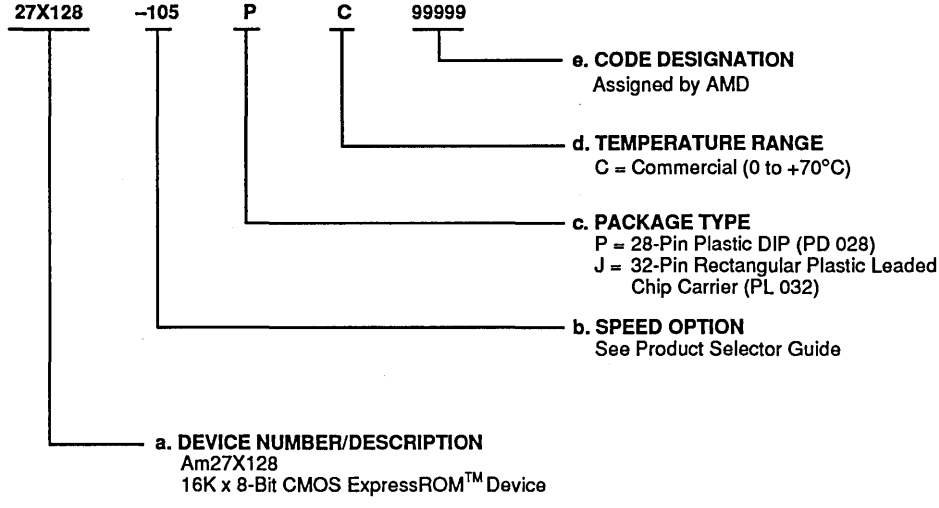
PIN DESCRIPTION

$A_0 - A_{13}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
PGM (P)	=	Enable Input
V_{PP}	=	V_{PP} Supply Voltage
V_{CC}	=	V_{CC} Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
27X128-105 27X128-120 27X128-125 27X128-150 27X128-155 27X128-200 27X128-205 27X128-250 27X128-255 27X128-300 27X128-305	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X128 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X128 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM™ device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	PGM	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	V_{CC}	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	V_{CC}	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to 125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC} and V_{PP}	–0.6 to V_{CC} +0.5 V
V_{CC} and V_{PP}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

Minimum DC voltage on input or output is –0.5 V. During transitions, the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T)	0 to +70°C

Supply Read Voltages:

V_{CC}/V_{PP} for Am27X128–XX5	+4.75 to +5.25 V
V_{CC} /V_{PP} for Am27X128–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, 6 and 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CCPP}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$		100	µA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 1, 2 and 5)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	20	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X128 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
7. Maximum active power usage is the sum of I_{CC} and I_{PP}.
8. V_{cc} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

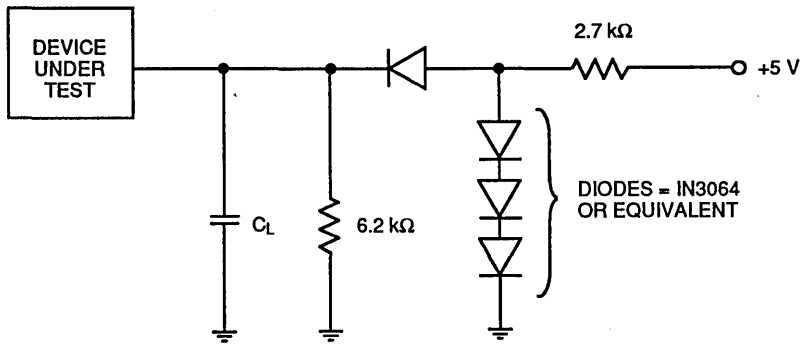
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbol		Parameter Description	Test Conditions		–105	–120 –125	–150 –155	–200 –205	–250 –255	–300 –305	Unit
JEDEC	Standard										
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.							ns
				Max.	100	120	150	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.							ns
				Max.	100	120	150	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.							ns
				Max.	40	50	65	75	100	120	ns
t_{EHQZ} t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 1)		Min.							ns
				Max.	30	35	50	55	60	75	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first		Min.	0	0	0	0	0	0	ns
				Max.							ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X128 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

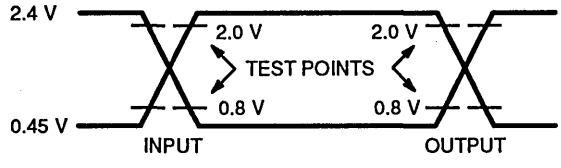
SWITCHING TEST CIRCUIT



12081B-005

C_L = 100 pF including jig capacitance

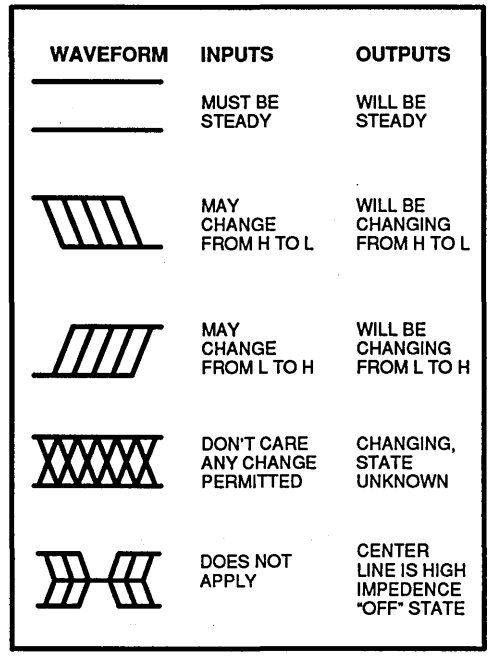
SWITCHING TEST WAVEFORM



12081B-006

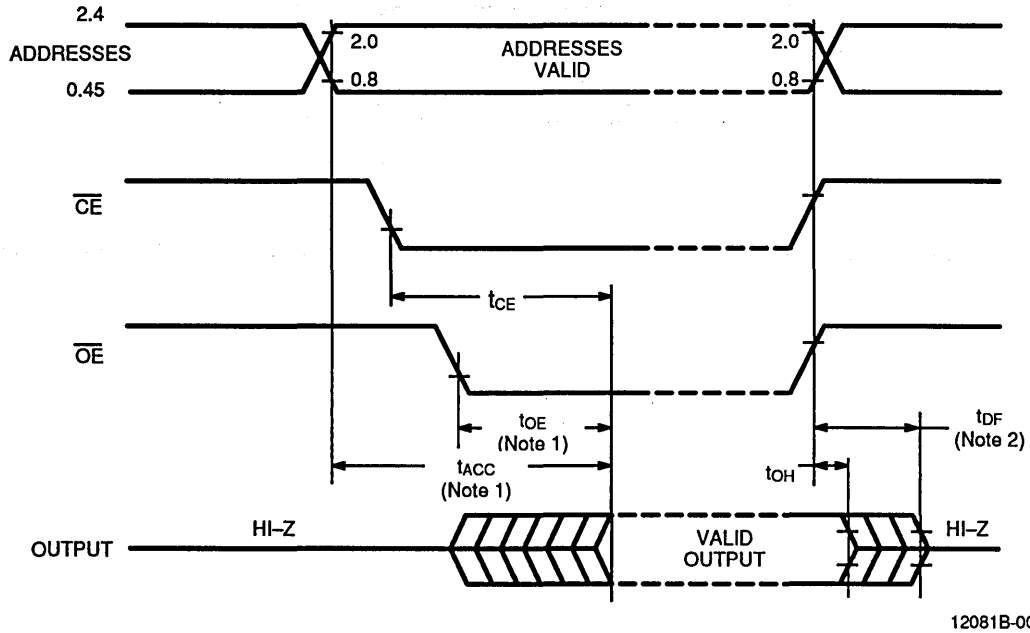
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING WAVEFORMS



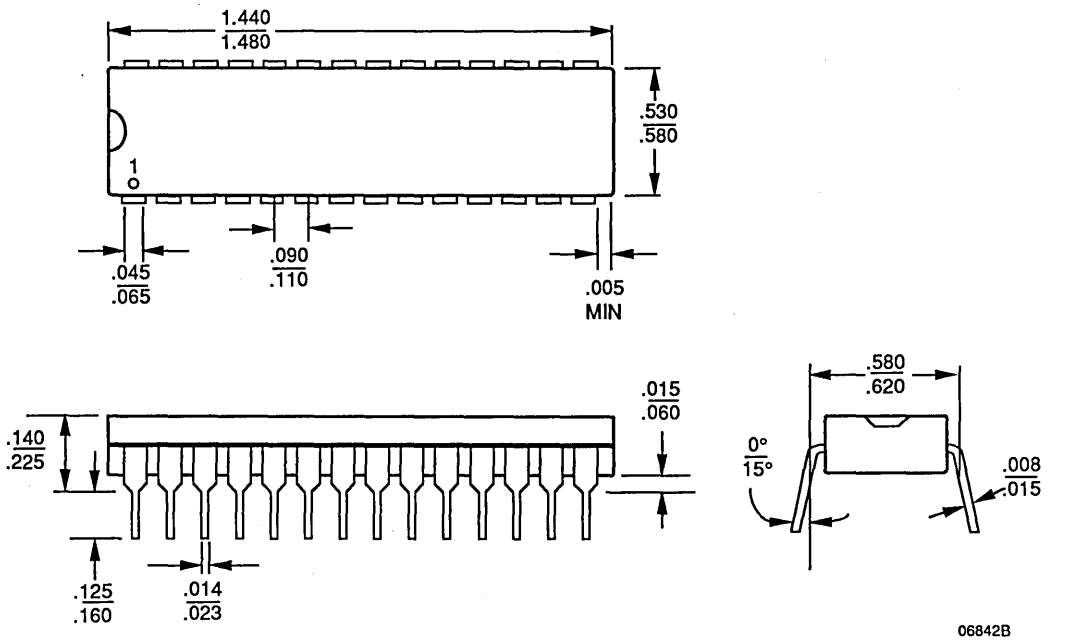
12081B-008

Note:

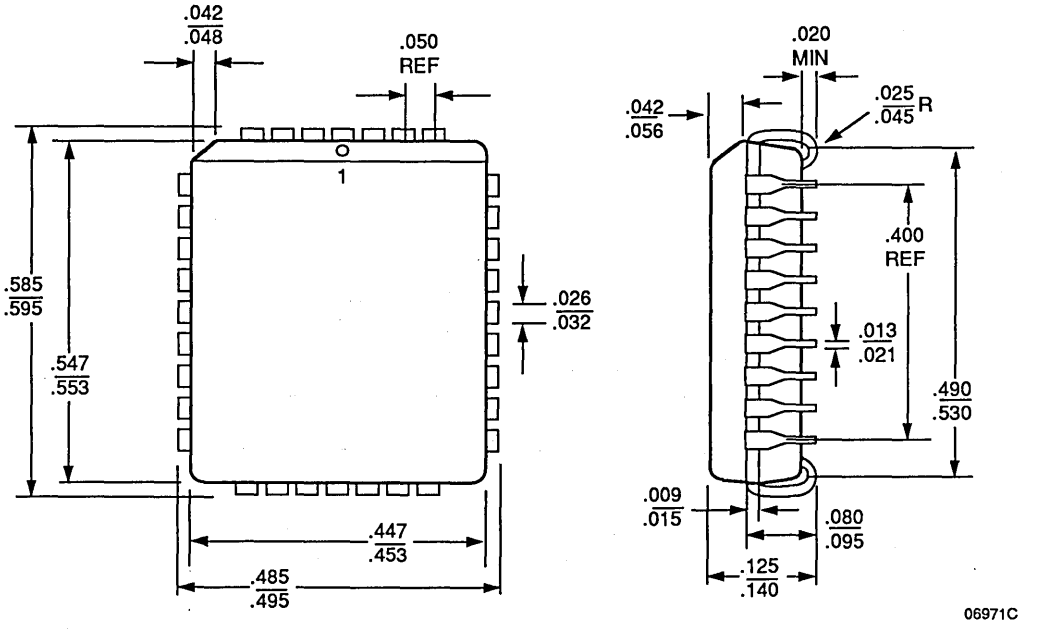
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PHYSICAL DIMENSIONS

PD 028



PL 032



Final

Am27X256

32,768 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **OTP EPROM alternative:**
  - Factory programmed
  - Fully tested and guaranteed
  - Low cost
- **Mask ROM alternative**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High performance CMOS technology**
  - Fast access time — 100 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier**

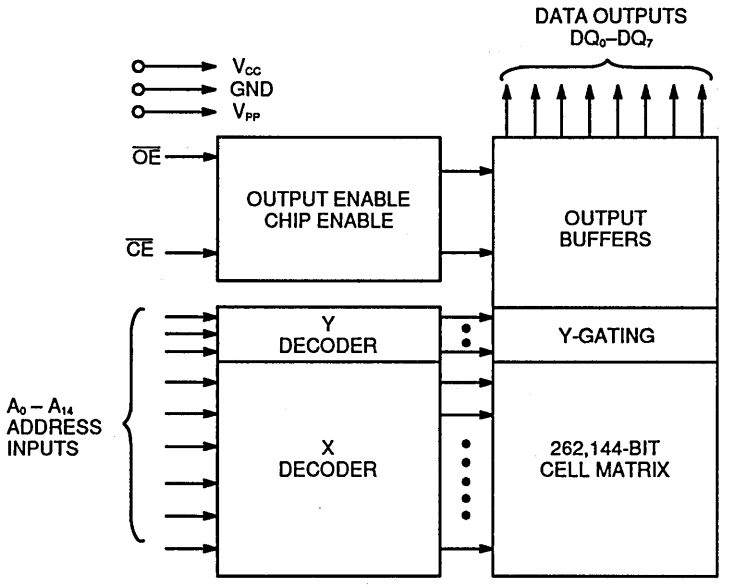
GENERAL DESCRIPTION

The Am27X256 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 32,768 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

ExpressROM is a trademark of Advanced Micro Devices Inc.

Publication # 12082 Rev. B Amendment/0
Issue Date: April 1989

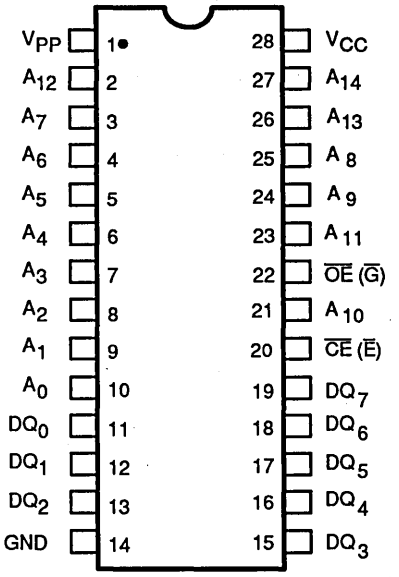
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X256						
Ordering part No: ±5% VCC Tolerance	-105	-125	-155	-175	-205	-255	-305
±10% VCC Tolerance	—	-120	-150	-170	-200	-250	-300
Max Access Time (ns)	100	120	150	170	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	170	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	70	75	100	120

CONNECTION DIAGRAMS

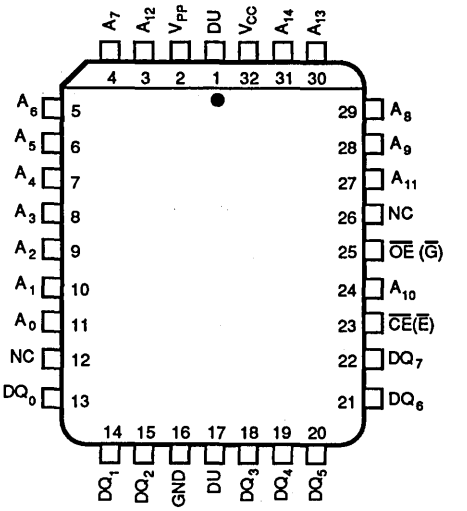
Top View

PLASTIC DIP



12081B-002

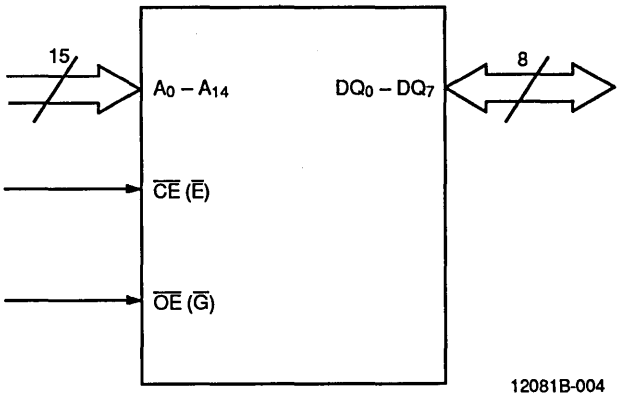
PLCC



12082-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

PIN DESCRIPTION

$A_0 - A_{14}$	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
$DQ_0 - DQ_7$	= Data Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
V_{CC}	= V_{CC} Supply Voltage
V_{PP}	= V_{PP} Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
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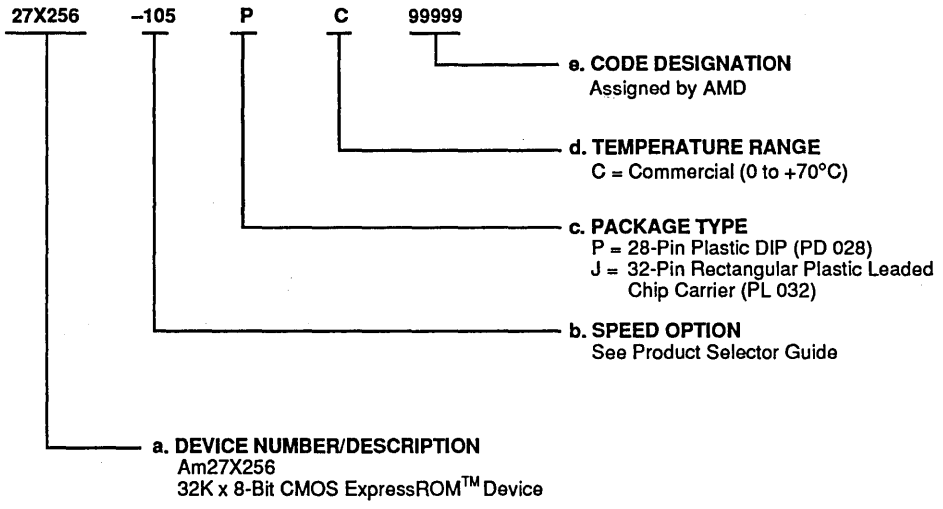


Valid Combinations	
27X256-105 27X256-120 27X256-125 27X256-150 27X256-155 27X256-170 27X256-175 27X256-200 27X256-205 27X256-250 27X256-255 27X256-300 27X256-305	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X256 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X256 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM™ device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	V_{CC}	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	V_{CC}	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to 125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC} and V_{PP}	–0.6 to V_{CC} +0.5 V
V_{CC} and V_{PP}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
Minimum DC voltage on input or output is –0.5 V. During transitions, the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T)	0 to +70°C

Supply Read Voltages:

V_{CC} /V_{PP} for Am27X256–XX5	+4.75 to +5.25 V
V_{CC} /V_{PP} for Am27X256–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, 6 and 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	V_{PP} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		25	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$		100	µA
I_{PP}	V_{PP} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 1, 2 and 5)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	20	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X256 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
7. Maximum active power usage is the sum of I_{CC} and I_{PP}.
8. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbol		Parameter Description	Test Conditions		–105	–120 –125	–150 –155	–170 –175	–200 –205	–250 –255	–300 –305	Unit
JEDEC	Standard											
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.								ns
				Max.	100	120	150	170	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.								ns
				Max.	100	120	150	170	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.								ns
				Max.	40	50	65	70	75	100	120	ns
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 1)		Min.								ns
				Max.	30	35	50	50	55	60	75	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first		Min.	0	0	0	0	0	0	0	ns
				Max.								ns

Notes:

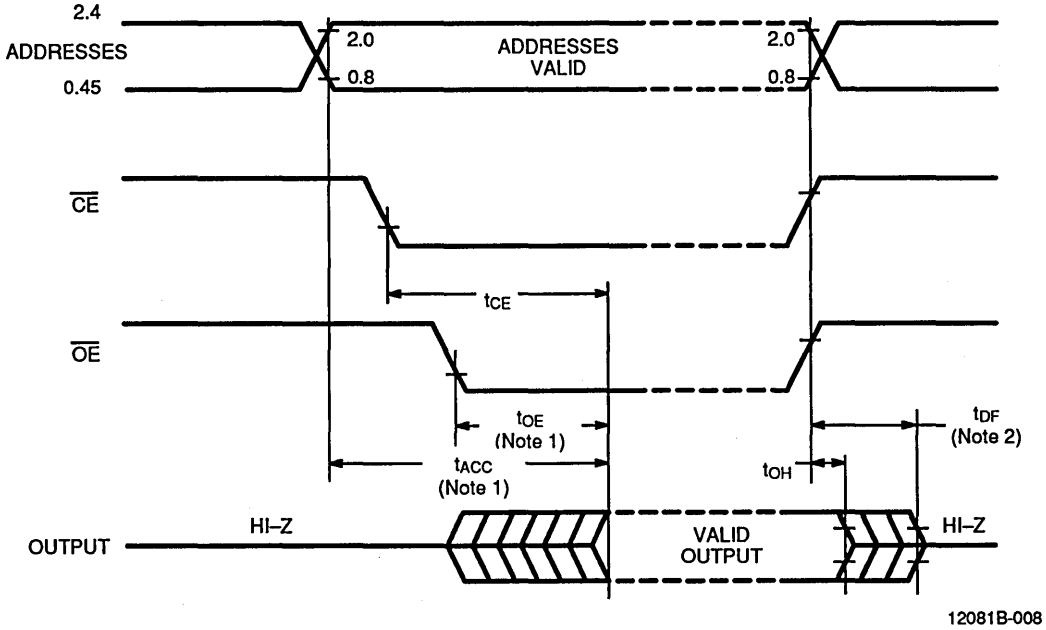
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X256 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDENCE "OFF" STATE

KS000010

SWITCHING WAVEFORMS

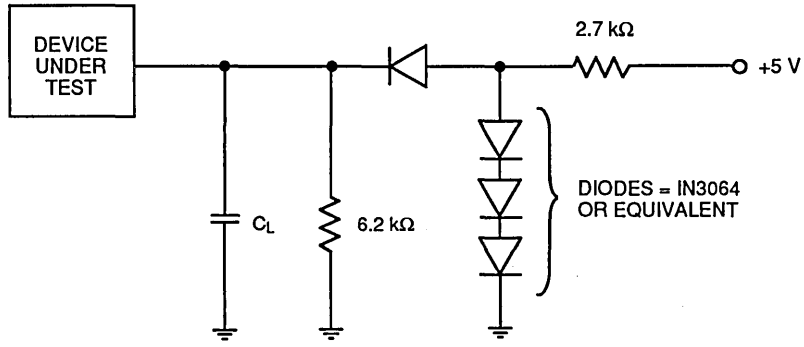


12081B-008

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

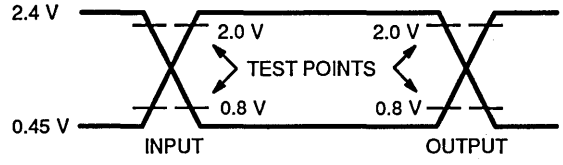
SWITCHING TEST CIRCUIT



12081B-005

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM

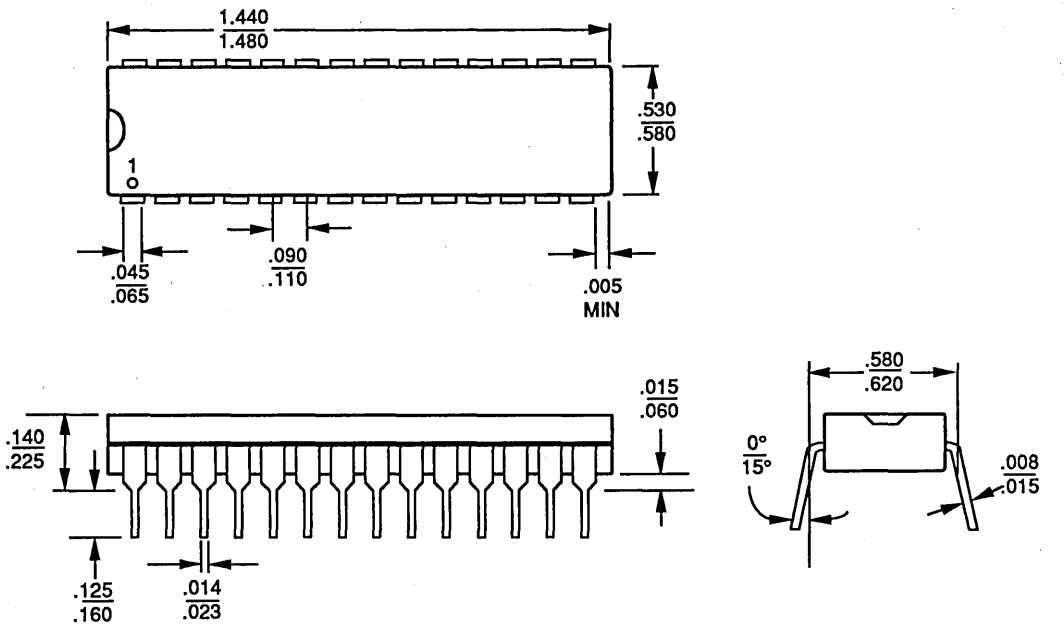


12081B-006

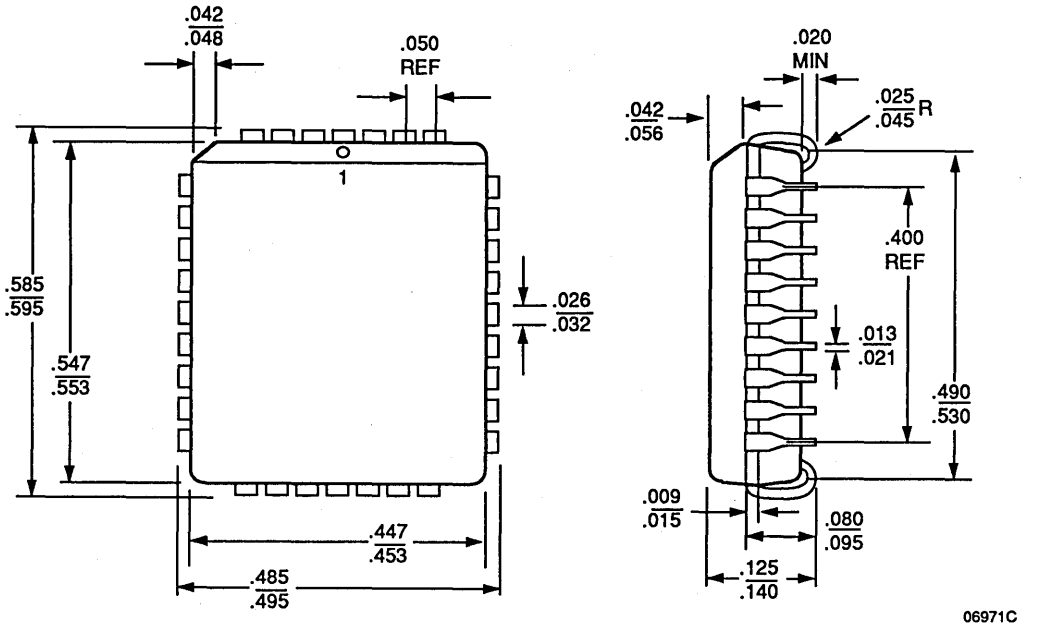
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20ns.

PHYSICAL DIMENSIONS

PD 028



PL 032



Final

Am27X512

65,536 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **OTP EPROM alternative:**
  - Factory programmed
  - Fully tested and guaranteed
  - Low cost
- **Mask ROM alternative**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High performance CMOS technology**
  - Fast access time — 150 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier**

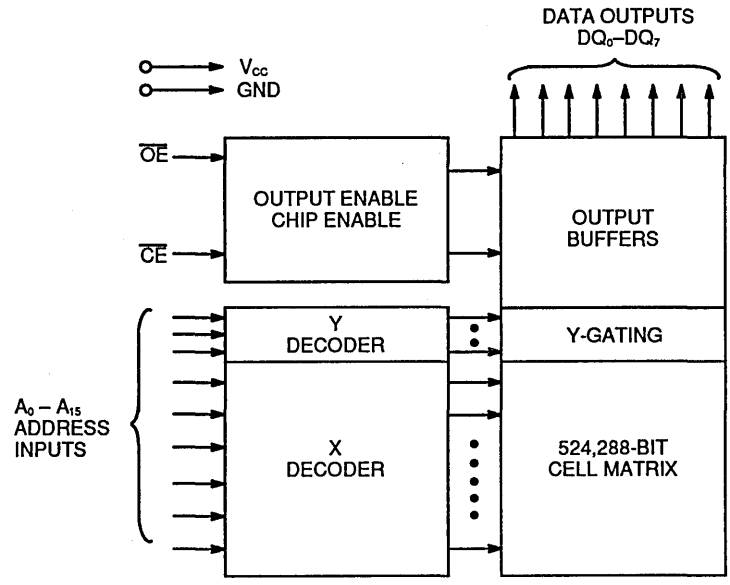
GENERAL DESCRIPTION

The Am27X512 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 150 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

ExpressROM is a trademark of Advanced Micro Devices Inc.

Publication # 12081 Rev. B Amendment/0
Issue Date: April 1989

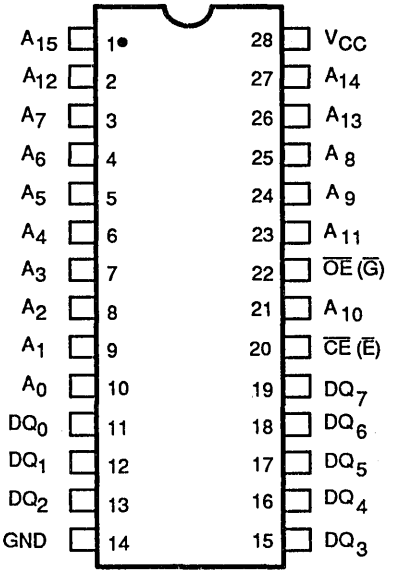
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X512				
Ordering part No:					
±5% VCC Tolerance	-155	-175	-205	-255	-305
±10% VCC Tolerance	–	-170	-200	-250	-300
Max Access Time (ns)	150	170	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	150	170	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	75	100	100

CONNECTION DIAGRAMS

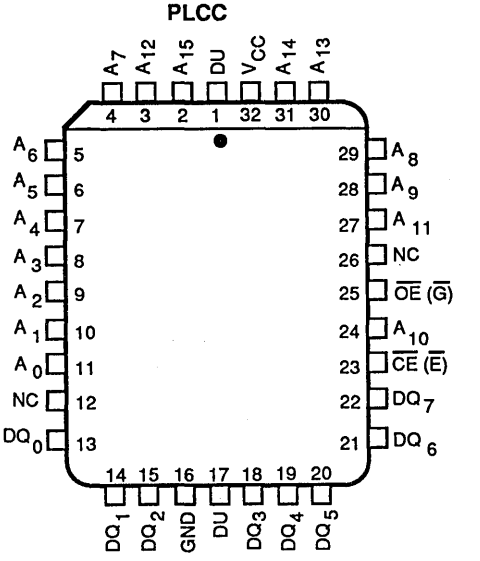
Top View

PLASTIC DIP



12081B-002

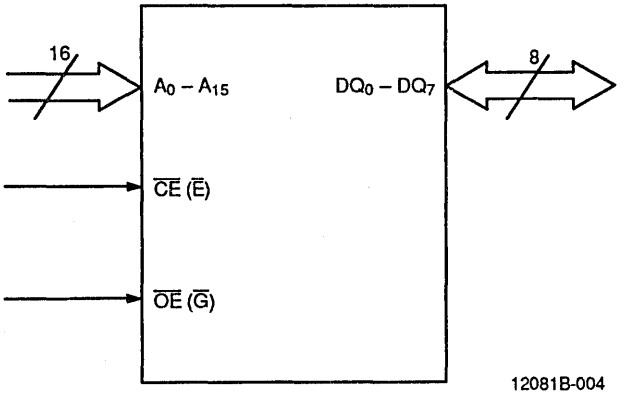
PLCC



11557-003A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

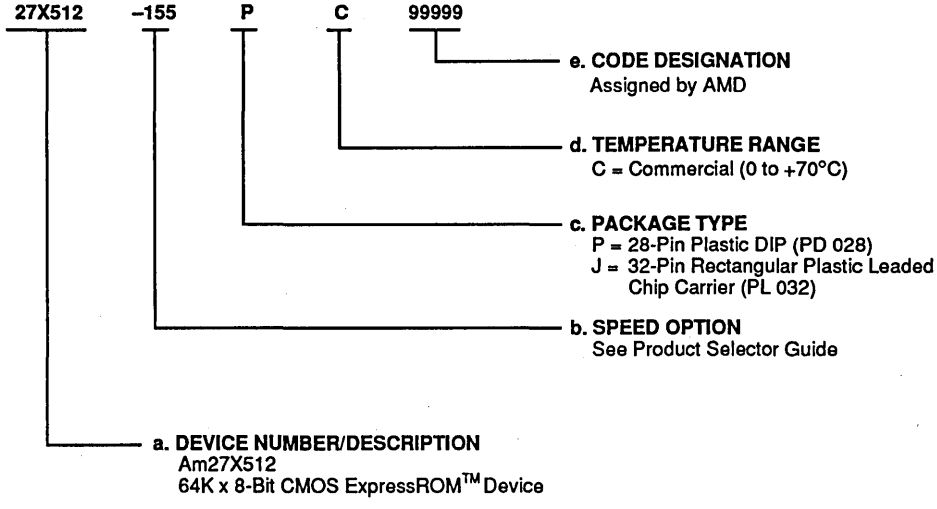
PIN DESCRIPTION

$A_0 - A_{15}$	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
$DQ_0 - DQ_7$	= Data Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
V_{CC}	= V_{CC} Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
27X512-155 27X512-170 27X512-175 27X512-200 27X512-205 27X512-250 27X512-255 27X512-300 27X512-305	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X512 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X512 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM™ device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	Outputs
Read	V_{IL}	V_{IL}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	High Z
Standby (TTL)	V_{IH}	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to 125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} +0.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Note: *Minimum DC voltage on input or output is –0.5 V. During transitions, the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.*

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T)	0 to +70°C

Supply Read Voltages:

V_{CC} for Am27X512–XX5	+4.75 to +5.25 V
V_{CC} for Am27X512–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, and 6)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		–0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		1	mA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		–0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$		100	µA

CAPACITANCE (Notes 1, 2 and 5)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	20	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X512 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

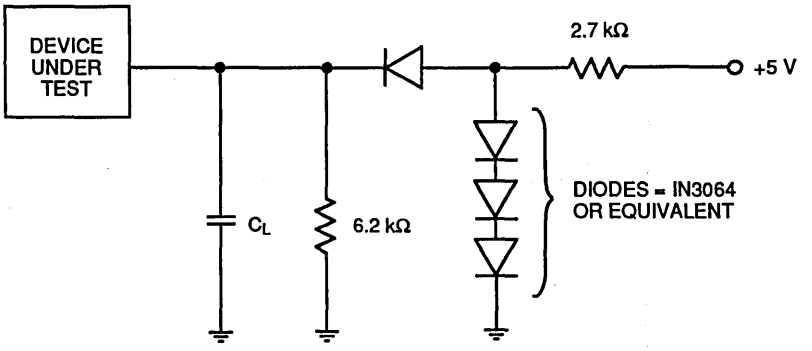
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 2 and 3)

Parameter Symbol		Parameter Description	Test Conditions		-155	-170 -175	-200 -205	-250 -255	-300 -305	Unit
JEDEC	Standard									
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.						ns
				Max.	150	170	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.						ns
				Max.	150	170	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.						ns
				Max.	50	50	75	100	100	ns
t_{EHQZ} t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 1)		Min.						ns
				Max.	30	30	60	60	60	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						ns

Notes:

1. This parameter is only sampled and not 100% tested.
2. **Caution:** The Am27X512 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
3. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

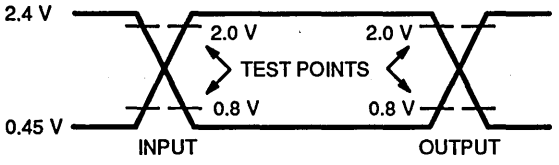
SWITCHING TEST CIRCUIT



12081B-005

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



12081B-006

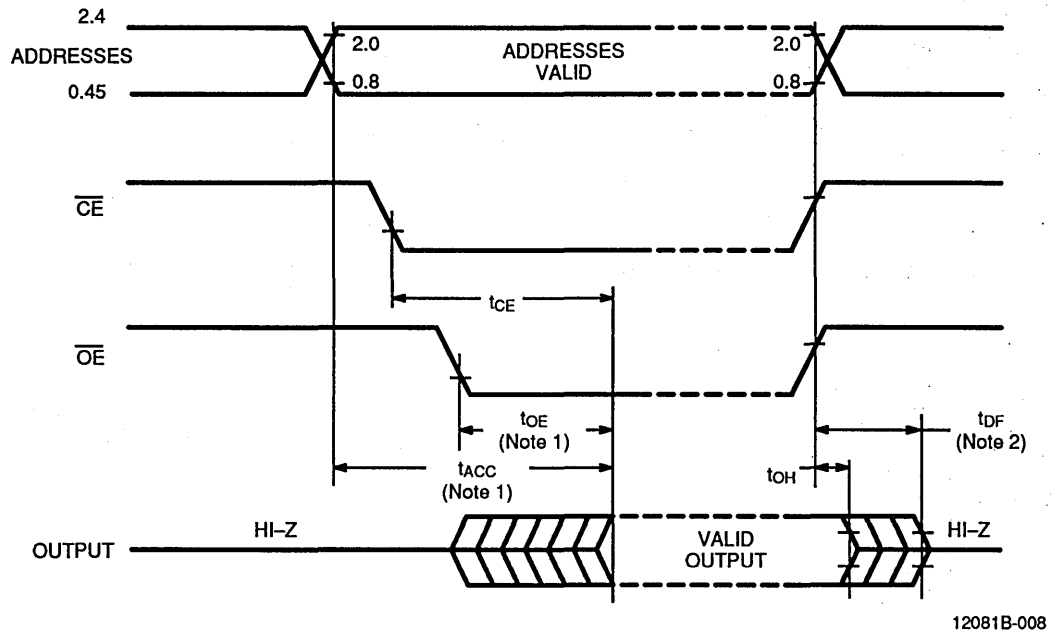
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDENCE "OFF" STATE

KS000010

SWITCHING WAVEFORMS



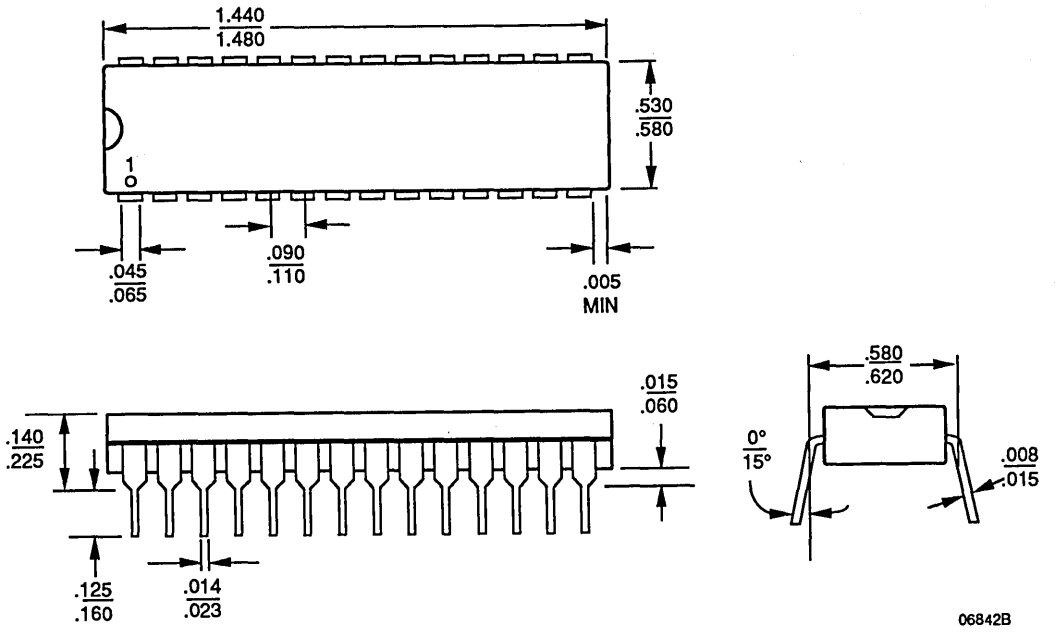
12081B-008

Note:

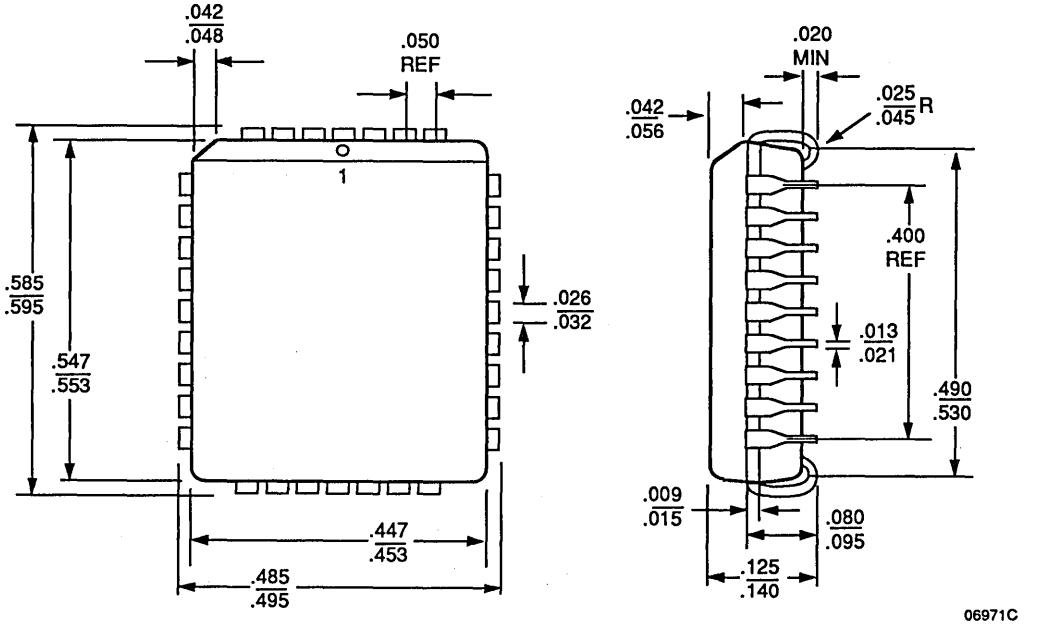
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PHYSICAL DIMENSIONS

PD 028



PL 032



Final

Am27X010

1 Megabit (131,072 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **OTP EPROM alternative:**
  - Factory programmed
  - Fully tested and guaranteed
  - Low cost
- **Mask ROM alternative**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High performance CMOS technology**
  - Fast access time — 200 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier**

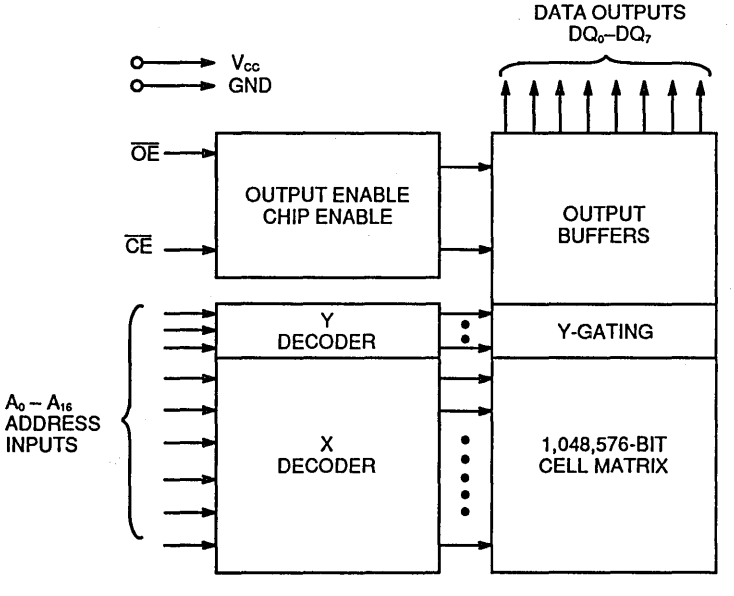
GENERAL DESCRIPTION

The Am27X010 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 131,072 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 200 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

ExpressROM is a trademark of Advanced Micro Devices Inc.

Publication # 12080 Rev. B Amendment/0
Issue Date: April 1989

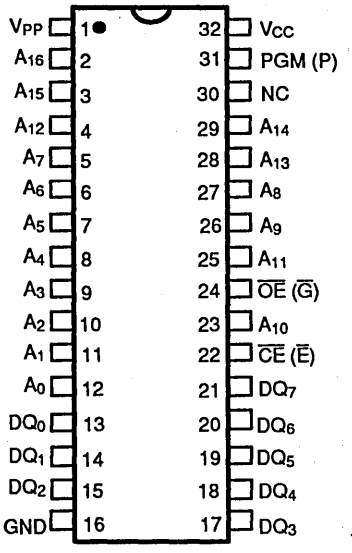
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X010		
Ordering part No:			
±5% VCC Tolerance	-205	-255	-305
±10% VCC Tolerance	-200	-250	-300
Max Access Time (ns)	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	75	100	120

CONNECTION DIAGRAMS

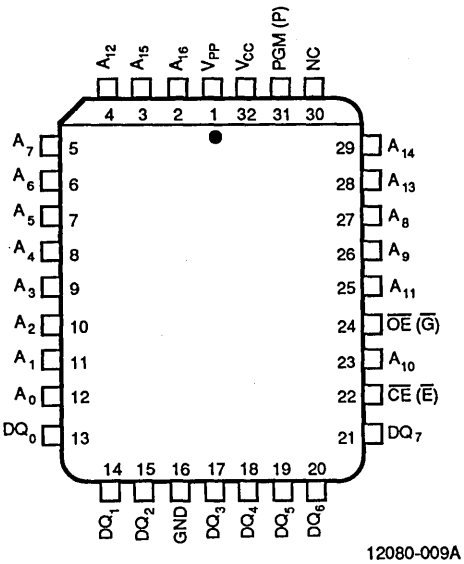
Top View

PLASTIC DIP



12081-002A

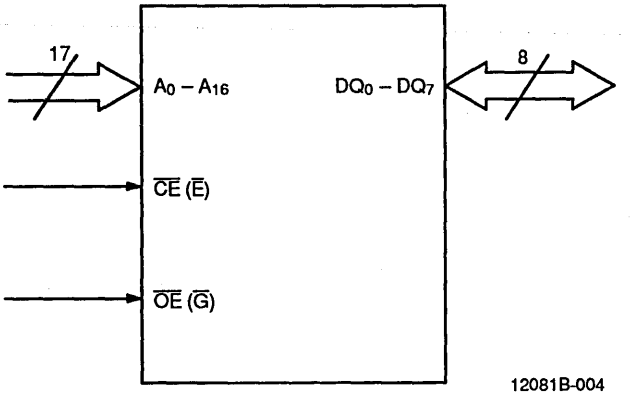
PLCC



12080-009A

Note: 1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin PLCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin PLCC configuration.

LOGIC SYMBOL



12081B-004

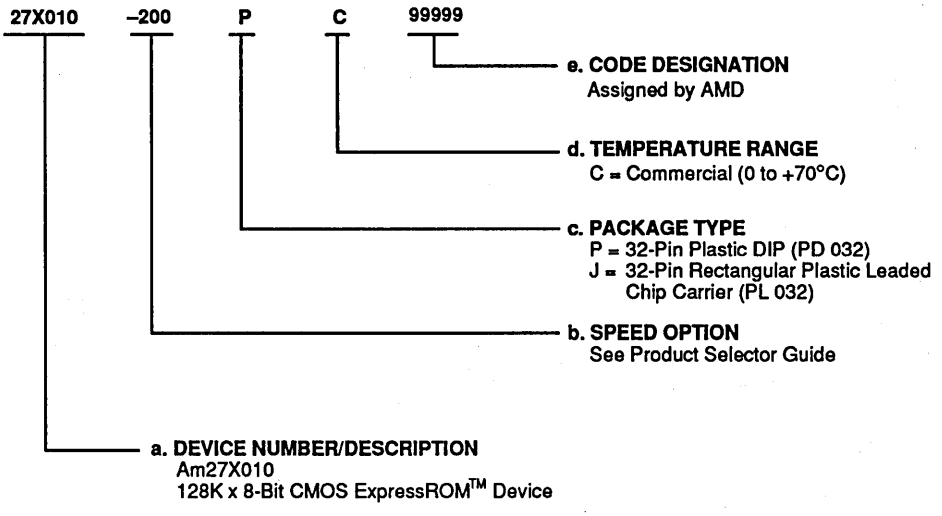
PIN DESCRIPTION

$A_0 - A_{16}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
PGM (P)	=	Enable Input
V_{PP}	=	V_{PP} Supply Voltage
V_{CC}	=	V_{CC} Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
27X010-200 27X010-205 27X010-250 27X010-255 27X010-300 27X010-305	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X010 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM™ device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Pins / Mode	$\overline{CE}$	$\overline{OE}$	PGM	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to 125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC} and V_{PP}	–0.6 to V_{CC} +0.5 V
V_{CC} and V_{PP}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

Minimum DC voltage on input or output is –0.5 V. During transitions, the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T)	0 to +70°C

Supply Read Voltages:

V_{CC} for Am27X010–XX5	+4.75 to +5.25 V
V_{CC} for Am27X010–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, 6 and 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CCPP}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$		100	µA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 1, 2 and 5)

Parameter Symbol	Parameter Description	Test Conditions	PD 032		PL 032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Input Capacitance	V_{IN} = 0 V	8	12	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	20	9	15	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	6	9	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X010 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
7. Maximum active power usage is the sum of I_{CC} and I_{PP}.
8. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

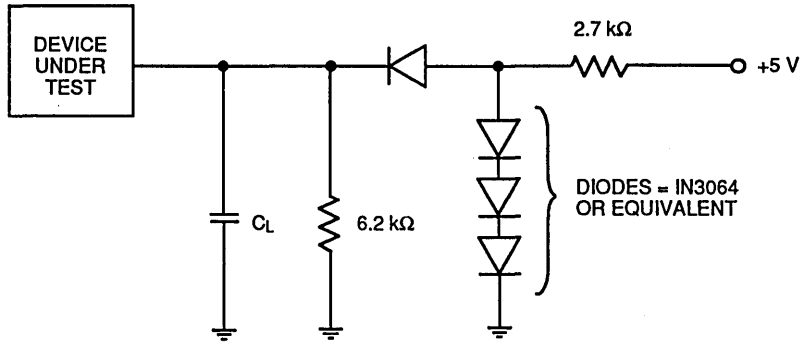
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbol		Parameter Description	Test Conditions		–200 –205	–250 –255	–300 –305	Unit
JEDEC	Standard							
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.				ns
				Max.	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.				ns
				Max.	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.				ns
				Max.	75	100	100	ns
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 1)		Min.				ns
				Max.	60	60	60	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first		Min.	0	0	0	ns
				Max.				ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X010 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

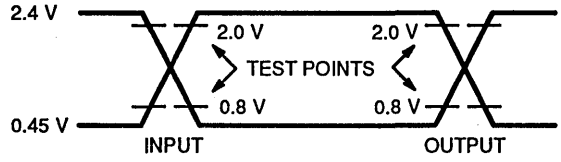
SWITCHING TEST CIRCUIT



12081B-005

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



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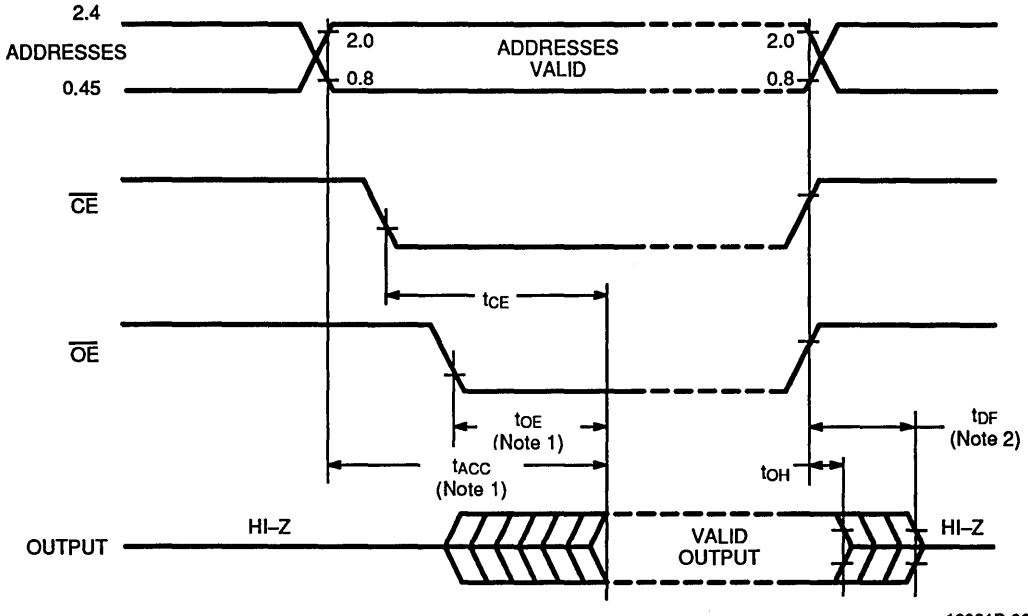
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDENCE "OFF" STATE

KS000010

SWITCHING WAVEFORMS



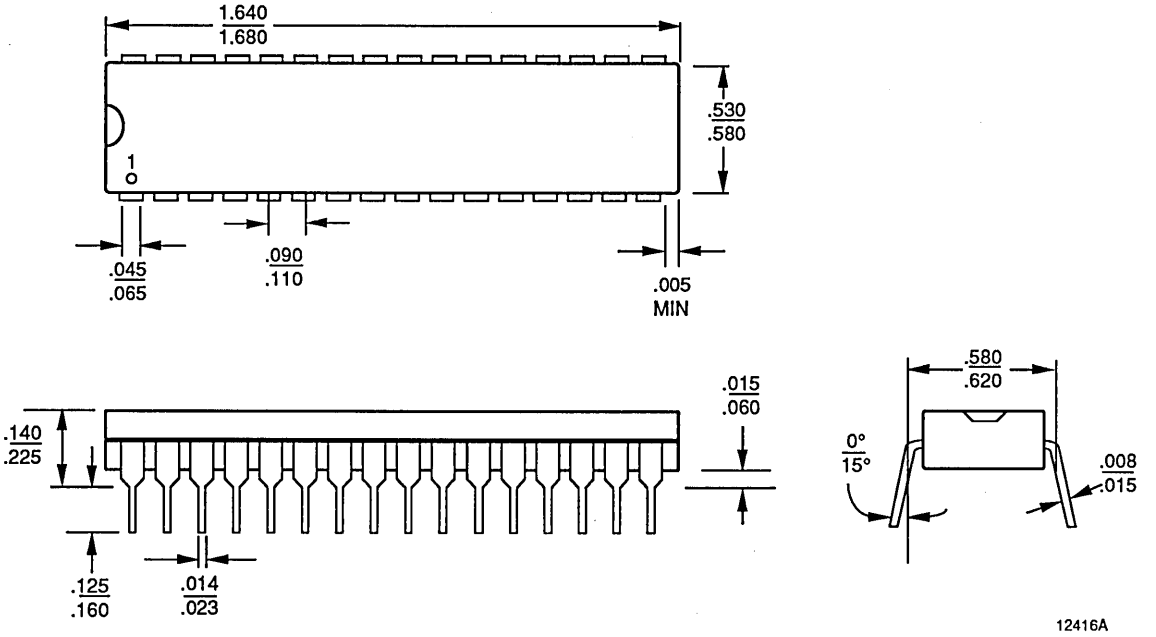
12081B-008

Note:

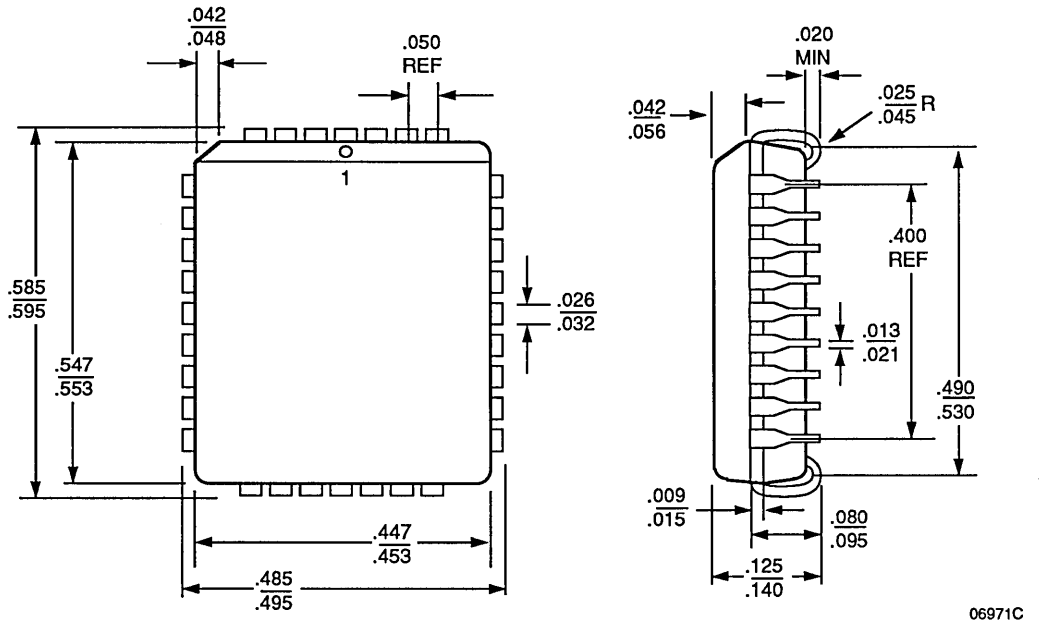
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PHYSICAL DIMENSIONS

PD 032



PL 032



Final

Am27X1024

1 Megabit (65,536 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **OTP EPROM alternative:**
  - Factory programmed
  - Fully tested and guaranteed
  - Low cost
- **Mask ROM alternative**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High performance CMOS technology**
  - Fast access time — 170 ns
  - Low power dissipation
    200 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier**

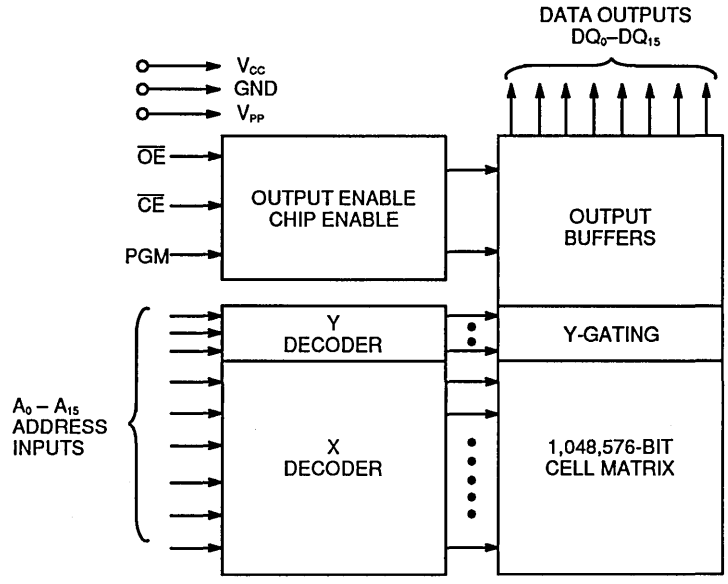
GENERAL DESCRIPTION

The Am27X1024 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 16 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM™ devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 170 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X1024 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 350 µW in standby mode.

BLOCK DIAGRAM



12081B-001

ExpressROM is a trademark of Advanced Micro Devices Inc.

Publication # 12079 Rev. B Amendment/0
Issue Date: April 1989

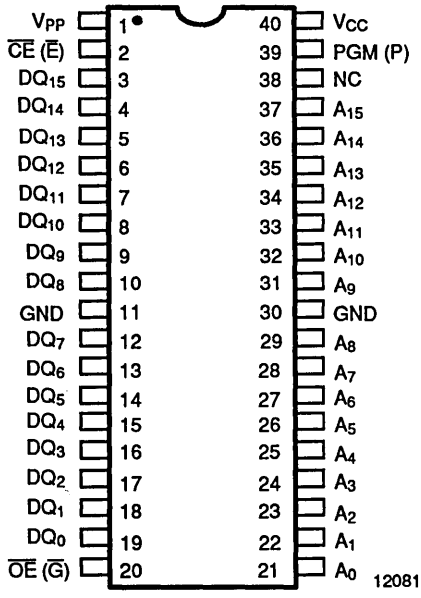
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X1024			
Ordering part No:				
±5% VCC Tolerance	-175	-205	-255	-305
±10% VCC Tolerance	—	-200	-250	-300
Max Access Time (ns)	170	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	170	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	65	75	100	120

CONNECTION DIAGRAMS

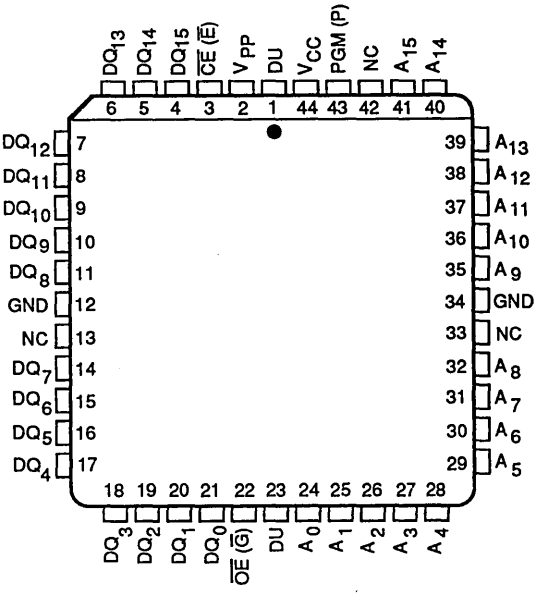
Top View

PLASTIC DIP



12081-002A

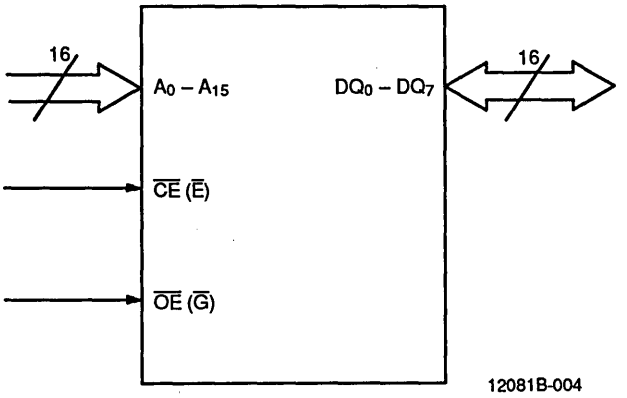
PLCC



12079-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

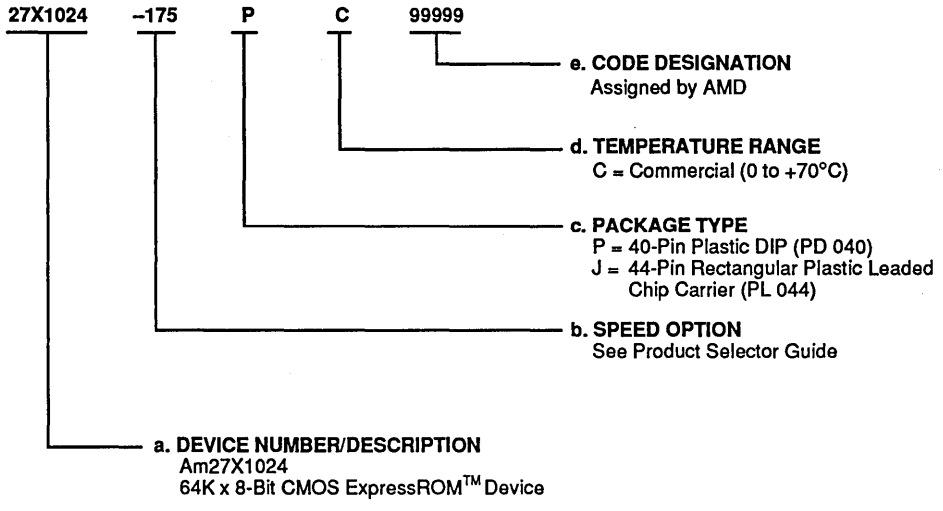
PIN DESCRIPTION

$A_0 - A_{15}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_{16}$	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
PGM	=	Enable Input
V_{PP}	=	V_{PP} Supply Voltage
V_{CC}	=	V_{CC} Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
27X1024-175 27X1024-200 27X1024-205 27X1024-250 27X1024-255 27X1024-300 27X1024-305	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X1024 has a CMOS standby mode which reduces the maximum V_{CC} current to 200 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X1024 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM™ device arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	PGM	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	V_{CC}	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to 125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC} and V_{PP}	–0.6 to V_{CC} +0.5 V
V_{CC} and V_{PP}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

Minimum DC voltage on input or output is –0.5 V. During transitions, the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T)	0 to +70°C

Supply Read Voltages:

V_{CC} /V_{PP} for Am27X1024–XX5	+4.75 to +5.25 V
V_{CC} /V_{PP} for Am27X1024–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4, 6 and 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		50	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		1	mA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.3	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}		10	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		50	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$		200	µA
I_{PP}	V_{CC} Supply Current (Note 7)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 1, 2 and 5)

Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Input Capacitance	V_{IN} = 0 V	8	12	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	20	9	15	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	6	9	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X1024 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
7. Maximum active power usage is the sum of I_{CC} and I_{PP}.
8. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

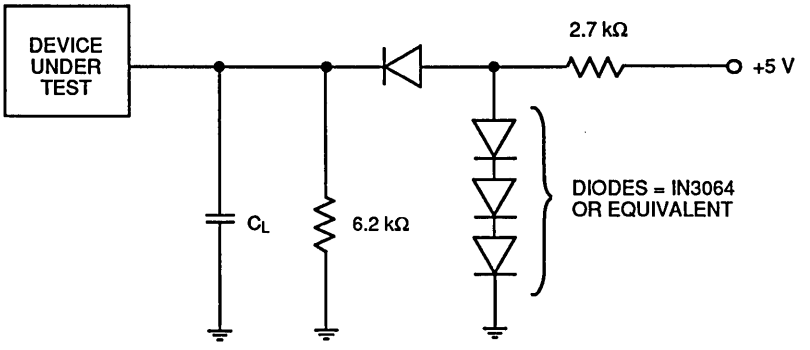
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4)

Parameter Symbol		Parameter Description	Test Conditions		–175	–200 –205	–250 –255	–300 –305	Unit
JEDEC	Standard								
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.					ns
				Max.	170	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.					ns
				Max.	170	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.					ns
				Max.	65	75	100	120	ns
t_{EHQZ} t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 1)		Min.					ns
				Max.	50	60	60	60	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first		Min.	0	0	0	0	ns
				Max.					ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X1024 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

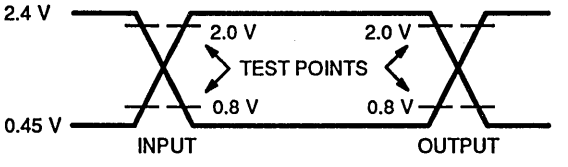
SWITCHING TEST CIRCUIT



12081B-005

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



12081B-006

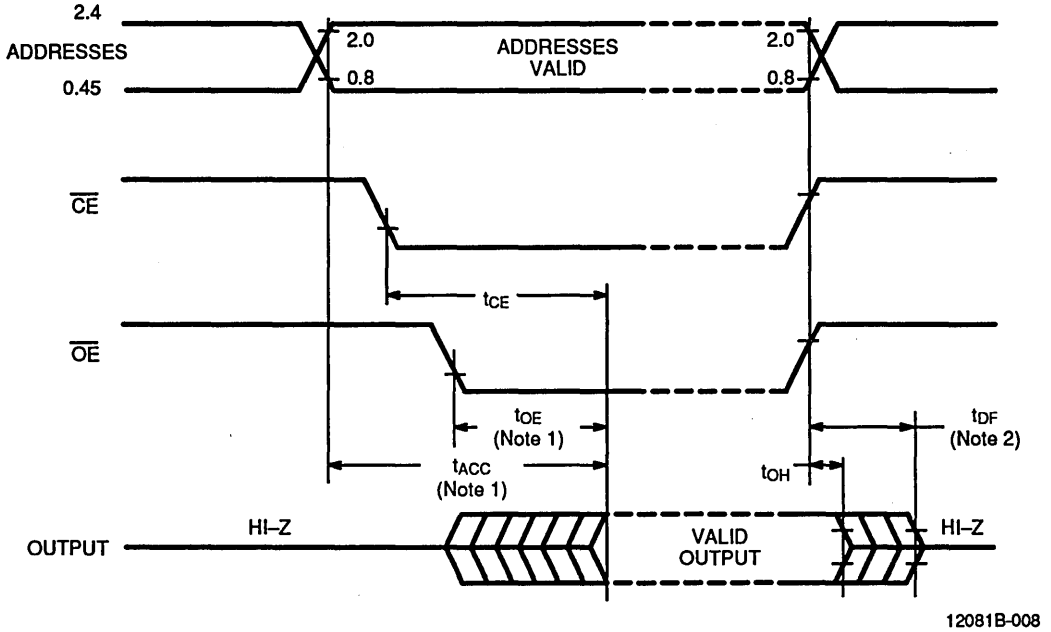
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDENCE "OFF" STATE

KS000010

SWITCHING WAVEFORMS



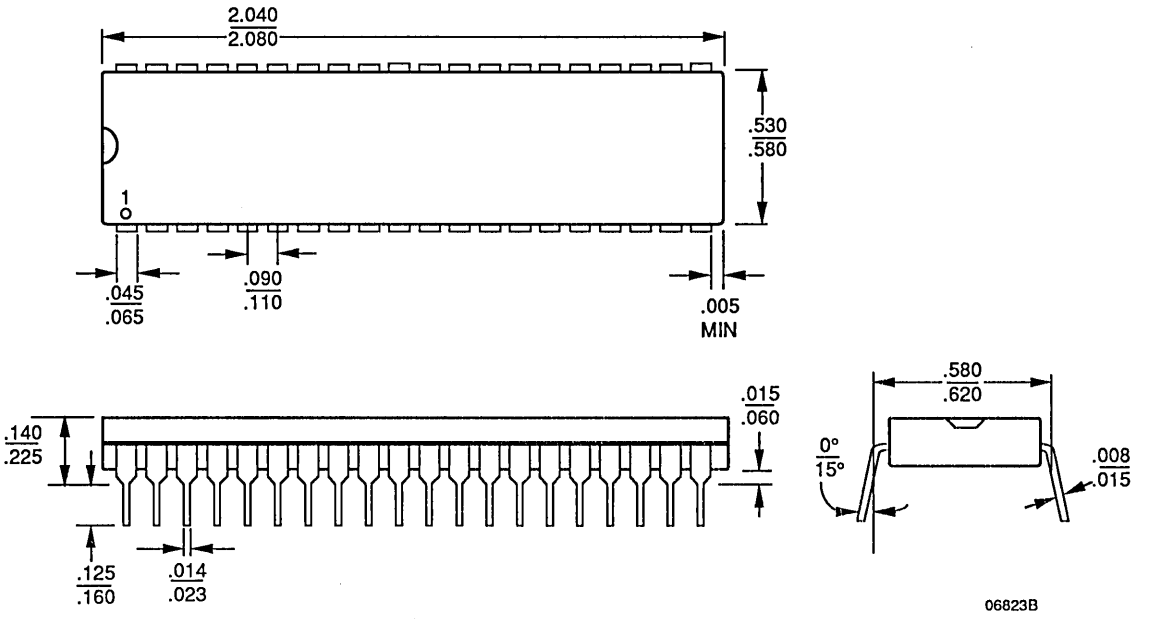
12081B-008

Note:

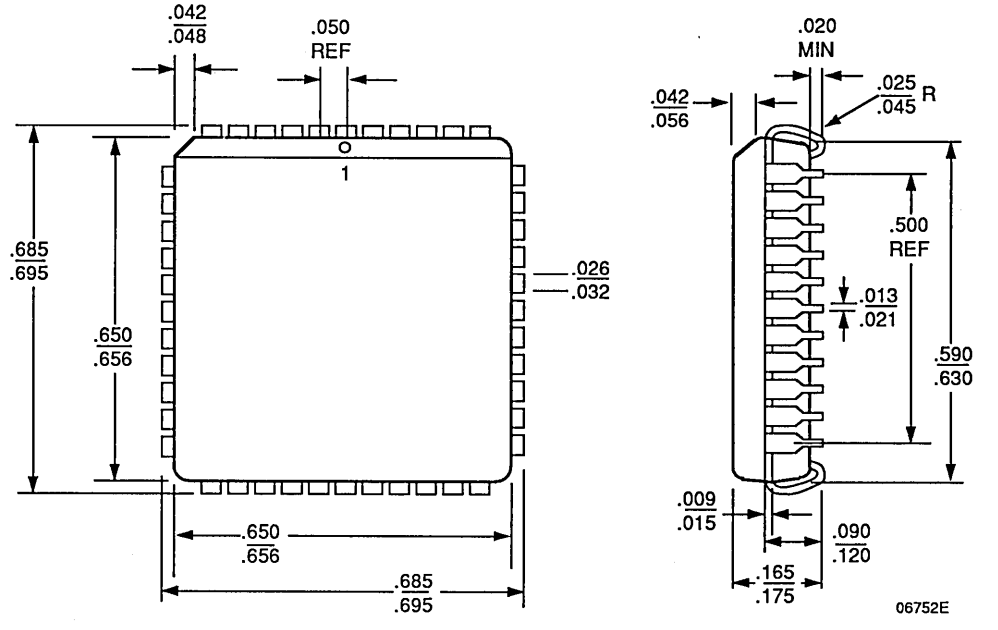
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PHYSICAL DIMENSIONS

PD 040



PL 044



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