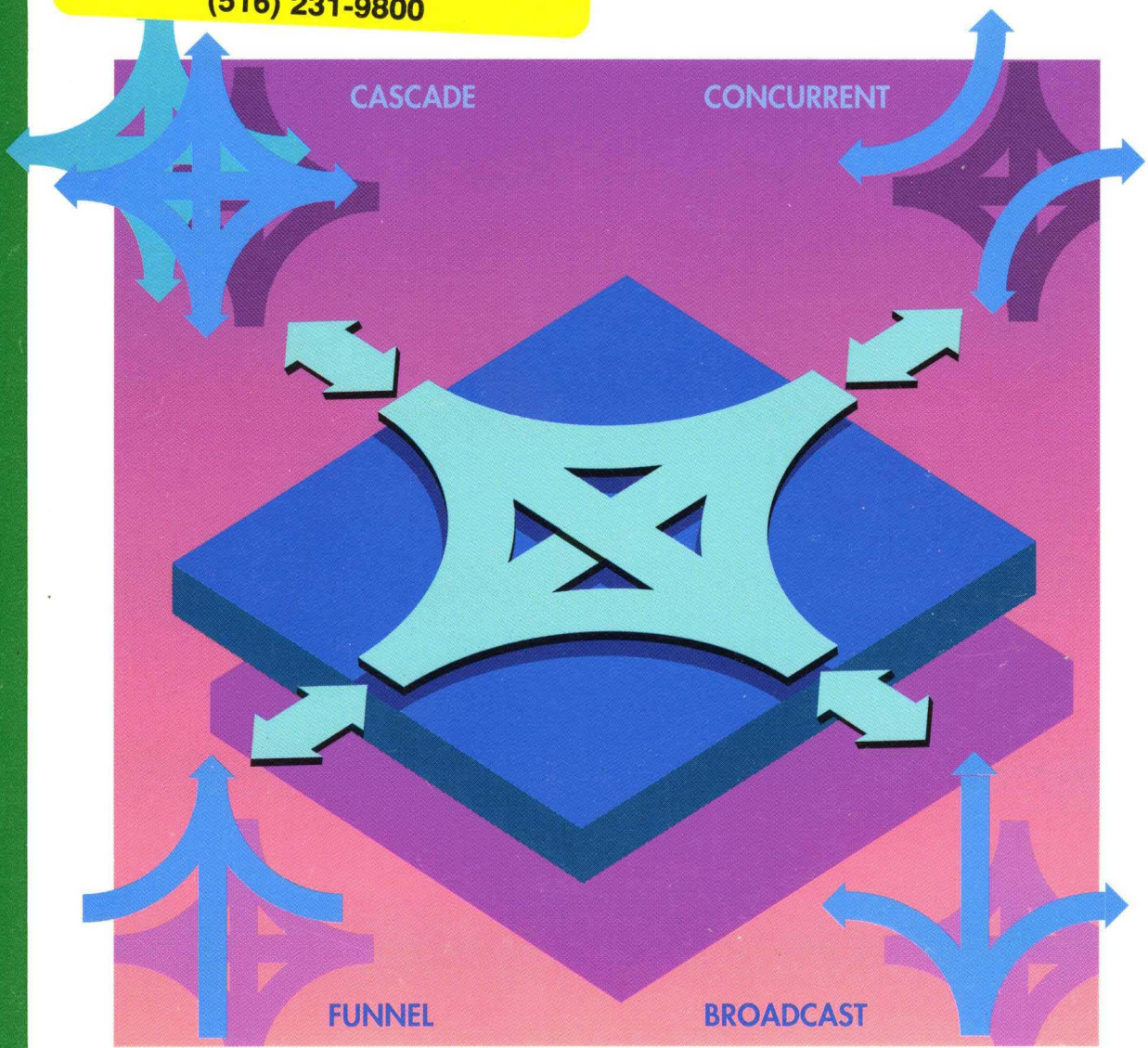
Multiple Bus Exchange

1991 Handbook/Data Book

Advanced
Micro
Devices



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As part of AMD's continued commitment to provide high-performance, innovative bus interface products, we have developed the Multiple Bus Exchange Family. Each MBE device efficiently implements a high-speed digital cross-point switch with high output drive on all ports. These devices provide a level of flexibility and integration superior to alternative inter-bus solutions. We encourage you to evaluate these products for your multiple bus and multiprocessing communication requirements.

Fred J. Roeder
Vice President
Standard Products Division
Advanced Micro Devices, Inc.

PREFACE

An innovative designer of high-performance bus interface devices, AMD offers an integrated solution for sophisticated multiple bus and multiprocessing designs—the Multiple Bus Exchange family:

Am29C982	4-bit x 4-port Multiple Bus Exchange
Am29C983A	9-bit x 4-port Multiple Bus Exchange with input/out latches
Am29C985	9-bit x 4-port Multiple Bus Exchange with Parity Generate/Check

This Handbook/Data Book provides descriptions of AMD's Multiple Bus Exchange devices, including specifications, and gives examples of how to design multiple bus and multiprocessing systems, using these high-speed CMOS bus interface devices.

Chapter 1 gives an overview of the Multiple Bus Exchange family.

Chapter 2 presents application notes and an article reprint describing different multiple bus and multiprocessing communication designs using the MBE devices. The applications are divided into three functional areas:

- funneling
- interleaving
- data routing

Chapter 3 reviews output edge-rate control design methodology used to minimize ground bounce.

Chapter 4 provides general information on AMD's design and testing methodologies.

Chapter 5 contains the MBE data sheets as listed in the table of contents.

Chapter 6 shows packaging and physical dimensions.

Appendix A is a brief discussion of the electronic design automation tools from OrCAD Systems Corporation.

Appendix B is a brief discussion of the behavioral simulation models from Logic Automation, Inc.

Appendix C provides device packaging and process data, useful for qualification purposes.

TABLE OF CONTENTS

CHAPTER 1
Multiple Bus Exchange Overview

Multiple Bus Exchange Overview

MULTIPLE BUS EXCHANGE

Multiple Bus Exchange (MBE) devices are general purpose, digital crosspoint switches that provide both efficient interbus communication and high bus drive capability. A crosspoint switch provides multi-directional communication between 4 ports, such that any port can, with no restrictions, send data to, or receive data from, any other port. This allows data to be broadcast to all other ports, to be funneled from multiple ports to one port, or for data to be concurrently sent between two sets of ports. In addition, any port which is an input, may simultaneously be an output; i.e., a port may write to itself.

Applications for this flexible architecture include parallel and array processing, memory-system interfaces, fault-tolerant environments, and other digital systems that require management of the flow and routing of data between buses.

MBE FAMILY OVERVIEW

Three MBE architectures are presently available—the Am29C982, Am29C983/983A, and the Am29C985.

Am29C982

The Am29C982 is a 4-port, 4-bit/port device with no internal storage. The '982 offers a small (28-pin PLCC), low-cost solution for nibble-divisible applications that require data routing.

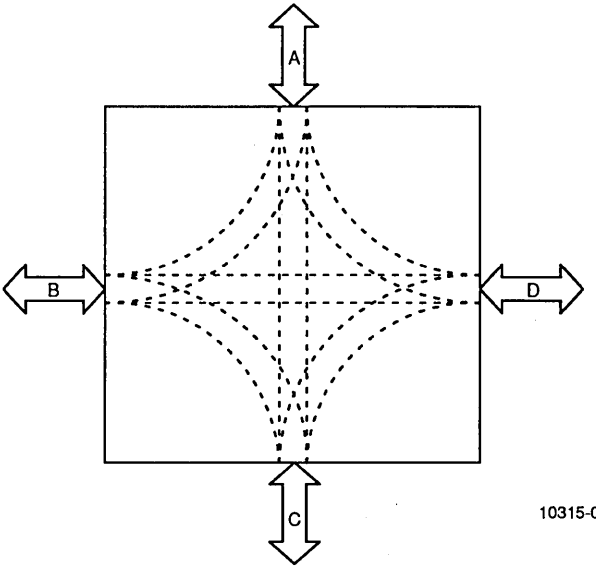


Figure 1-1. Multiple Bus Exchange— Digital Crosspoint Switch

Am29C983/Am29C983A

The Am29C983 is a wider (9-bit), faster (Am29C983A) version of the four-port crosspoint switch. Each I/O port has an input latch and an output latch; thus, data can be latched before and after the switching matrix. All input and output latches are independently controlled by active-HIGH Latch Enable inputs. The integration of these flexible storage and enable features into the bus switch saves board space and improves performance over discrete-based data routing solutions.

The 9-bit port width is an additional boon to the system designer, transmitting a data byte and its (system supplied) parity bit without having to break the byte across multiple devices. The ability to route entire parity protected bytes in one package saves board space and reduces skew problems.

Am29C985

For those systems which require parity generation and checking, AMD integrates this generation and check capability into a 4-port, 9-bit/port crosspoint switch.

The Am29C985 incorporates parity check and generation capabilities on all four output ports. Each output port is capable of generating odd parity on byte-wide input data. Accordingly, parity check is accomplished at each output on the incoming 9-bit data + parity word. Data integrity is further ensured by a proprietary comparison scheme that compares the state of the bus with the data driven onto it. Stuck-at faults and system interconnect problems, which would escape a simple internal parity check, are also detected.

Each I/O port has an output latch to capture outgoing data. All output latches are independently controlled by active-HIGH Output Latch Enable inputs.

MBE FAMILY FEATURES

High-Drive, Low Ground Bounce Outputs

Every MBE device has 48-mA I_{OL} outputs for high capacitance bus driving. AMD's proprietary output edge-rate control minimizes ground bounce and reduces the severity of crosstalk (See Application Note, chapter 3). The MBE not only routes and stores data, but can also drive heavily loaded system buses too. Ample power and ground pins are included to further reduce noise and ground bounce.

Glitch-Free Power-Up/Down

Every MBE device has a power up/down circuit for maintaining a high-impedance state on the bus during power supply sequencing. Each MBE output structure uses n-channel pull-up transistors that withstand an external bus voltage when supply voltage is off. These features guarantee glitch-free operation, an important concern for large systems with separately powered sub-units. For additional power-up/down information, see Chapter 4.

Matched Port Decoding

The MBE has matched port decoding. Each port uses a common coding rule, with a 2-bit port-select code determining the source of data for output. This scheme simplifies external decode logic because all four ports are controlled in an identical manner. This avoids decoding delays and permits independent operation of the routing at each port. As a result, multiple MBEs can be cascaded to effectively construct wider-bus (16-, 32-,...-bit) interface structures.

THE MULTIPLE BUS EXCHANGE—AN INTEGRATED SOLUTION

The MBE provides an integrated interface solution which logically replaces a large number of latches, multiplexers and buffers. This highly integrated solution provides two main advantages: design simplicity and real-estate savings.

Design Simplicity

The advantage of design simplicity is most apparent during the timing and logic control design phases. Since fewer devices are now required in the bus interface design, fewer delays and skews must be factored into the timing equations. Likewise, since the MBE not only integrates multiple components, but also has matched-port decoding, the logic necessary to control the interface device is much less complex. Fewer devices and matched-port decoding result in a simpler timing controller.

Real-Estate Savings

One does not have to look far to realize the importance of real-estate savings. Each computer generation has not only become quite a bit more powerful than its predecessor, but also quite a bit smaller! This decrease in space not only satisfies the end-customer's desire for a compact solution, but also represents significant cost savings for the manufacturer.

Each integrated circuit used on a board costs a certain amount of money to install, house, power and cool, regardless of what it is or what it does. If one adds up the cost of all the physical hardware (cabinets, boards, power supplies, fans, etc.) which support the integrated circuits in the system, minus the cost of the circuits themselves, but including the assembly cost of mounting them onto the board, and divides this cost by the total number of integrated circuits, one would get some sort of "overhead factor"—the cost of having one integrated circuit.

It may seem arbitrary to allocate a specific charge per integrated circuit without regard to the circuit's function; however, any human or automated handling costs are probably similar for any size package. Additionally, since packages cannot touch one another on a circuit board without shorting each other out, a border must be allocated around each package. The corresponding "footprint" around the package tends to decrease the relative difference in board space consumed by smaller and larger packaged parts. Thus, the additional space required for a smaller package footprint increases at a higher percentage than that of a larger package. This also means that being capable of removing any package, large or small, from the design can drastically reduce the overall real-estate and cost requirements.

The following tables demonstrate average real-estate savings of the 68-pin PLCC Am29C983A versus 20-pin PDIP or SOIC octal buffers and latches and 24-pin PDIP or SOIC octal transceiver/registers. Modern component mounting technologies require a minimum of 100 mils (0.1") between the ends and sides of each device.

The minimum area of each component footprint, as shown in Table 1–1, is calculated by adding 0.1" to both the length and width of the device features. The device feature measurements are representative of the package length and pin width of 74F245 buffers, 74F373 latches and 74F646 transceiver/registers.

The real-estate requirements for a typical 8-bit multiple bus interface design with storage, comparing one Am29C983A with four latches and two buffers, is shown in Table 1–2. The real-estate requirements for a typical 32-bit interface design, comparing four Am29C983As with eight buffers and eight transceiver/registers, is shown in Table 1–3. These comparisons are based on systems which do not use parity. The real-estate savings resulting from using Am29C983As is drastically higher in data + parity designs, as demonstrated in tables 1–4 and 1–5.

Table 1–1. Calculated Component Footprints, In Inches

Type	Package		Footprint		Area (In^2)
	Length	Width	Length	Width	
20-Pin PDIP	1.057	0.322	1.157	0.422	0.488
20-Pin SOIC	0.512	0.419	0.612	0.519	0.318
24-Pin PDIP	1.280	0.322	1.380	0.422	0.582
24-Pin SOIC	0.614	0.419	0.714	0.519	0.371
68-Pin PLCC	0.995	0.995	1.095	1.095	1.199

Table 1–2. Typical 8-bit Footprint Comparison, In Square Inches

Design	Pkg	Units	Area/Unit	Total Area
Buffer/Latch	PDIP	6	0.488	2.928
	SOIC	6	0.318	1.908
Am29C983A	PLCC	1	1.199	1.199

Table 1–3. Typical 32-bit footprint comparison, In Square Inches

Design	Pkg	Units	Area/Unit	Total Area
Buffer	PDIP	8	0.488	3.904
Xceiver/Reg	PDIP	8	0.582	+4.656
				8.560
Buffer	SOIC	8	0.318	2.544
Xceiver/Reg	SOIC	8	0.371	+2.968
				5.512
Am29C983A	PLCC	4	1.199	4.796

Table 1–4. Typical 8-bit Data + Parity Footprint Comparison, In Square Inches

Design	Pkg	Units	Area/Unit	Total Area
Buffer/Latch	PDIP	8	0.488	3.904
	SOIC	8	0.318	2.544
Am29C983A	PLCC	1	1.199	1.199

Table 1–5. Typical 32-bit Data + Parity Footprint Comparison, In Square Inches

Design	Pkg	Units	Area/Unit	Total Area
Buffer	PDIP	10	0.488	4.880
Xceiver/Reg	PDIP	10	0.582	+5.820
				10.700
Buffer	SOIC	10	0.318	3.180
Xceiver/Reg	SOIC	10	0.371	+3.710
				6.890
Am29C983A	PLCC	4	1.199	4.796

CHAPTER 2
Applications and Article Reprint

INTRODUCTION

This chapter includes application notes and an article reprint utilizing the Multiple Bus Exchange in various system solutions. The applications are categorized into three general purpose functional groups—funneling, interleaving and data routing.

Diverse applications have been included in each functional group so that the user may understand the broad application base which the MBE serves. Each application is written as general as possible so that the user may tailor his implementation as required.

The article reprint, which was originally printed in Electronic Design, discusses the advantages a silicon digital crosspoint switch in silicon offers to interbus communications.

Applications and Article Reprint

FUNNELING APPLICATIONS

Many applications require data communications between subsystems of differing bus-widths. In these applications, the processor or controller uses byte-word compression and expansion techniques to communicate between the varying bus-widths. This communication between larger and smaller bus sizes is generically called "funneling."

For example, if a 32-bit processor communicates with an 8-bit peripheral, the data must be "funneled" from 32-bits to 8-bits. When byte-word expansion techniques are used, such that an 8-bit peripheral is communicating to a 32-bit processor, the technique is often called "bus expansion."

Another funneling application occurs when a microprocessor communicates to buses of differing widths. For example, a 32-bit processor may have 8-, 16- or 32-bit peripherals. In this application, the processor uses byte-word compression and expansion and then latches the bytes into 8-,16- or 32-bit words, respectively. These words are then communicated to the peripheral device. This intelligent funneling application is often called "dynamic bus sizing."

Maintaining Software Compatibility with Established Bus Standards

Bus standards have traditionally not kept pace with the microprocessors that they are supposed to serve. While microprocessors have evolved from 8-bit to 16-bit, and now 32-bit data buses, the most popular buses (in terms of sales volume and installed base) are either 8-bit (PC, PC-XT) or 16-bit (PC-AT®). This mismatch in bus width places an additional constraint on the hardware designer, that of providing downward compatibility with an installed base of peripheral cards and software, while improving system performance and reducing cost.

Some aspects of the compatibility issue, such as the assignment of memory and peripheral addresses, pose no real design problems. However, ensuring that peripherals behave properly when the source of data is wider than the bus to which it is connected requires a basic understanding of the system code.

For example, the iAPX8088 is a processor with 16-bit internal data paths, but only an 8-bit external data bus. Data is funneled from the external 8-bit to the internal 16-bit data bus. For instruction fetches, code is read a byte at a time and assembled into words internally. Similarly, word-data accesses are converted into two byte-Read operations or two byte-Write operations. It is possible to write iAPX8088 code that performs two byte-writes to a peripheral by using a one-word Write instruction.

Unfortunately, this code is hardware dependent. When using a 16-bit processor, executing a word Write on a 16-bit bus, all 16 bits are transferred at once. However, if the peripheral is an 8-bit device, only the lower byte is read; the upper byte is lost and the peripheral is programmed incorrectly.

To successfully design systems using differing bus-widths, instructions dependent on bus width must not be used. Byte-wide peripherals require byte-oriented instructions to ensure proper operation. Unfortunately, constraining the system to use only byte operations increases code size and slows the system down. Wider data buses and microprocessors are used to increase bus bandwidth and improve system performance. Forcing data transfers to always be byte wide is like using only one lane of a four-lane highway—it's slow and doesn't make much sense.

The only real choice for system designers who wish to maintain compatibility with old software is to incorporate extra hardware which emulates byte Reads and Writes. For example, the IBM PC-AT supports several types of bus access, including word Read or Write to byte memory or to byte I/O. Two bus signals, MEM16 and IOCS16, inform the microprocessor of the data size of the memory or peripheral being accessed. These signals are generated by any word-wide device, but not by any byte-wide devices. If a word access is performed by a 16-bit microprocessor and either MEM16 or IOCS16 is valid, both the high and low bytes of the word are read or written simultaneously. If MEM16 or IOCS16 is not valid, two actions must be taken, depending on the type of access.

For word Write operations, data is valid on the microprocessor data pins for the duration of the access. The microprocessor starts the Write operation on the lower byte, but does not complete it. Instead, the microprocessor is placed in a Wait state and the Write operation to the lower byte is completed by external hardware. The address is then incremented by one, and the high-order data byte is then routed (funneled) to the low-order byte position. A Write strobe is performed, writing the second byte of data, and the microprocessor is then released from the Wait state.

Word Read accesses from an 8-bit device are performed in a similar manner. In this case, the microprocessor is held in the Wait state until a word has been assembled from two byte-Reads. A latch holds the low-order byte until the high-order byte is accessed. Both bytes are then read simultaneously by the microprocessor.

The external hardware required to perform this byte/word funneling without an MBE consists of three bidirectional buffers and a latch, plus some control logic, as shown in Figure 2–1. The control logic can be implemented in a PAL device, but implementing the bidirectional buffers with discrete logic presents some problems. Board space, the cumulative propagation delay of two or more bidirectional buffers in series, and the need for low noise, high drive capability weigh heavily against using discrete devices in funneling applications.

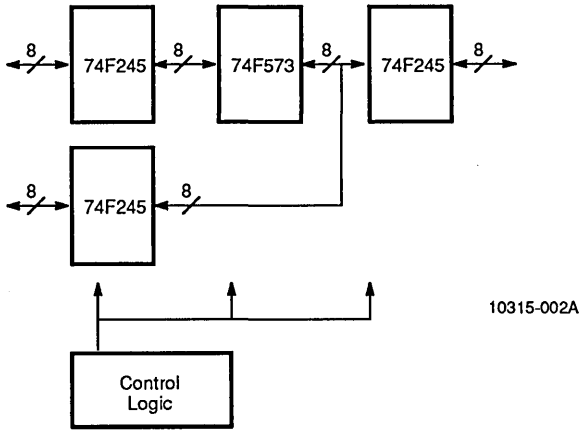


Figure 2-1. 8/16-bit Bus Funnel Using 3 Bidirectional Buffers and a Latch

These problems are solved by using the Am29C983 MBE device, as shown in the completed circuit in Figure 2–2. The four 9-bit I/O ports can be configured as either inputs or outputs. Both input and output latches are available on all ports. The 9-bit data path supports the transmission of byte-wide parity through the system, while the non-blocking crosspoint switch can connect any input port to any output port or ports. Maximum propagation delay from any port to any other port or ports is 14 ns worst case with a 50-pF load. The Am29C983A improves the port-to-port delay to 10 ns worst case. Both parts are specified with an I_{OL} of 48 mA.

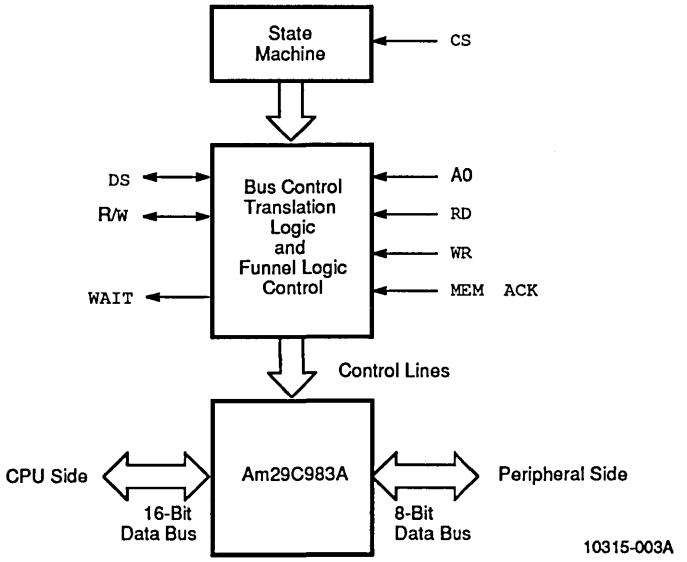


Figure 2–2. 8/16-bit Bus Funnel Using Am29C983A with Control Logic

As shown in the figure, the MBE connects directly onto the microprocessor data pins with two ports, and onto the system backplane (PC-XT bus, in this case) with one of the other two ports. Two PAL® devices are used, one to control MBE data paths, and one to generate Read and Write strobes and increment the address for the byte-oriented device.

Dynamic Bus Sizing with the 80386 Microprocessor

As shown in the previous application, newer system designs are continually increasing data bus-widths. However, many peripheral devices do not require, or have not yet designed-in, these wider data buses. In most cases, the 32-bit microprocessor is forced to run with the smaller 8- or 16-bit bus. The capability of a microprocessor to fetch 8-, 16- and 32-bit words from an 8-bit bus is called *dynamic bus sizing*. The 68020 and 68030 microprocessors support this mode of operation; however, many other microprocessors do not. For example, the 80386 microprocessor can handle a 16-bit bus, but cannot operate in an 8-bit environment.

Full byte-level dynamic bus sizing can be added to an 80386 microprocessor by using one MACH™ device and one Am29C983A MBE, as shown in Figure 2–3. The function of the Am29C983A in this application is made clear by analyzing the conversion of a 32-bit Read or Write cycle to byte accesses on the system bus.

In the case of a 32-bit Read, data must be expanded from 8 bits up to 32 bits. This expansion is done by translating the single 32-bit Read request from the 80386 into four single-byte accesses. Three of the four bytes are input through port A and are latched in ports D, C and B, respectively. On the fourth byte access, the three stored bytes, plus the fourth byte, are presented to the 80386 simultaneously. The MACH110 handles all control signals from the 80386 and controls the Latch Enables and Port Select lines on the MBE.

To transfer 32-bit Writes to the 8-bit bus, data must be funneled down so that a single 32-bit Write is translated into four byte-level transactions. When the 80386 writes the 32-bit data, the lowest-order byte is written directly to the memory or peripheral, while the other three bytes are latched in ports B, C and D. The MACH110 then sends a /Ready signal to the 80386 to indicate completion of the Write cycle, along with the Hold signal to keep the 80386 off the bus until the other three bytes are sent, from their respective latches, to the 8-bit memory or peripheral.

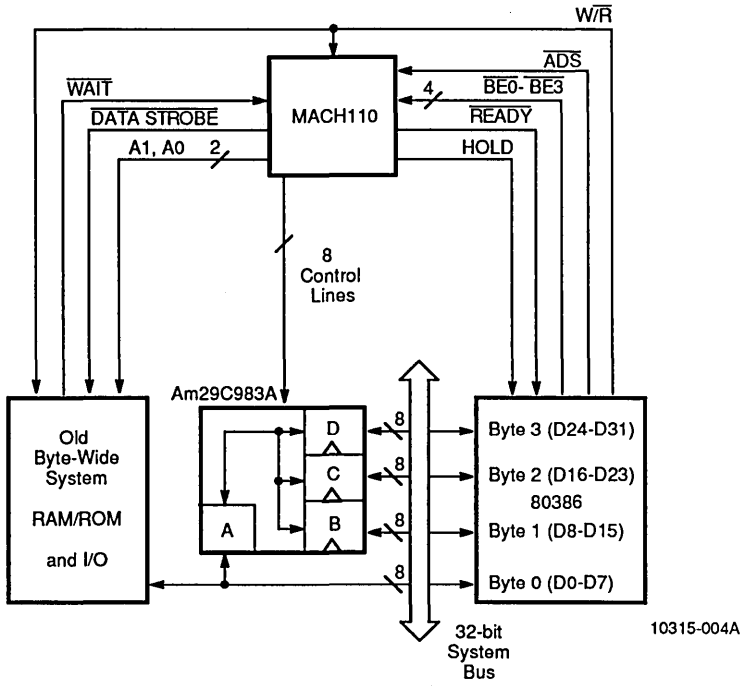


Figure 2–3. 8/32-bit Dynamic Bus Sizing

Expanding the Apparent Width of Various Devices and Systems

Another type of funneling application trades width for depth by using the MBE to expand the width of a data stream. The idea here is to use the MBE to create a "virtual device" that is much wider than the real device on which it is based. This is done by interleaving addresses and running the real device at a multiple of the system clock, which is equal to the expansion factor. Some examples of this technique follow.

Expansion of a ROM-Based Finite-State Machine

A finite state machine (FSM) can be built using an EPROM, as shown in Figure 2–4. The number of user-available outputs in this direct implementation of an FSM is limited by the need to use some of the EPROM outputs for next-state information. One solution to this limitation would be to use more EPROMs in parallel, with their address lines connected. Another, more cost effective solution, uses an MBE to double the number of outputs. Since the wide word is stored as a series of contiguous locations in the narrower EPROM, the system clock must be increased by the expansion factor to maintain overall system performance. For this example, where the apparent width is doubled, the EPROM must be accessed twice as often as usual to maintain the same system speed as the unexpanded EPROM. Proper ordering of two EPROM words into one wide word is easily done with an ordinary flip-flop, alternating between odd and even addresses. In the general case, ordering of n contiguous EPROM words into a single wide word requires a modulo-n counter.

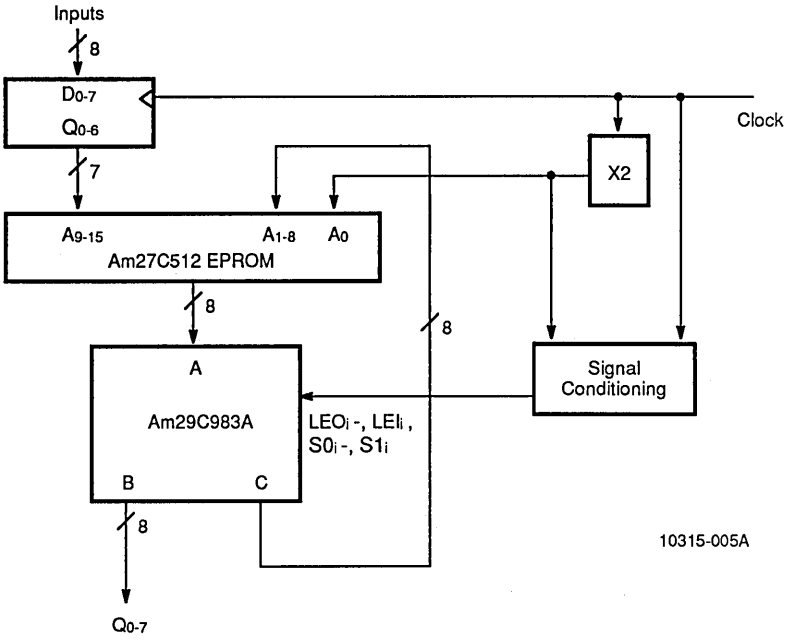


Figure 2–4. Expansion of a ROM-Based Finite-State Machine

Expansion of FIFOs

The same arguments that apply to expanding finite state-machine word width apply to FIFOs as well. A variation of the basic architecture uses two FIFOs and two MBEs to create a wide bidirectional FIFO module.

Expansion of Peripheral Ports

The MBE makes an ideal port expander for many microcontroller applications. With the overhead of just a few control pins, the MBE expands the port from one byte to three. Each expanded byte can be an input or output. The separate input and output latches at each port can add a layer of buffering in both directions between the microcontroller and real-world I/O if desired.

Adaptation of Peripheral Ports

The MBE provides a convenient interface between multiple 8-bit peripherals and buses of various widths. A good example of the power of this type of connectivity is an 80386 to TAXIchip™ device interface. The TAXIchip set consists of a byte-wide parallel-to-serial converter with multiplying phase locked loop (TAXI™ TX) and a companion serial-to-parallel converter with tracking phase locked loop (TAXI RX). The TAXI TX and RX comprise a simple point-to-point serial link which looks to the user like a 10-MByte/s parallel transfer. Since the 80386 can handle 16-bit transfers, the MBE provides a single-chip datapath interface between the microprocessor and the TAXI TX and RX. The separate input and output latches at each port buffer incoming and outgoing bytes.

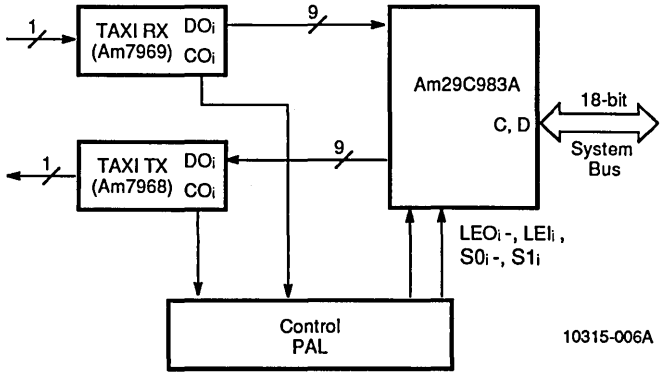


Figure 2–5. TAXI System Interface - 9/18-bit Bus Expansion

Bus Expansion for Graphics – Controlling 24-Bit Planes with an 8-Bit Bus

Display memory for graphics applications is arranged as a bit map, where each picture element (pixel) on the screen corresponds to a particular location in memory. A bit map of m x n x 1 memory locations is referred to as a plane of memory. A single memory plane can indicate if a pixel is on or off. Adding memory planes increases the number of attributes of any particular pixel, such as gray scale, or a pixel blink attribute.

Monochrome images are adequately represented by 256 levels of gray, or 8 bits per pixel. Palette based color graphic systems, which display only 256 selected colors at a time, also require only 8 bits per pixel. True color graphic systems represent the next step up in the display of realistic images. There are no restrictions on the number of simultaneously displayable colors; thus, requiring 8 bits per pixel for each of the primary colors, red green and blue, for a total of 24 bits per pixel. The MBE can provide an easy upgrade path from monochrome or palette based color to true color display by allowing the original 8-bit data bus to support 24 planes of display memory.

The basic system architecture is just a simple bus funnel, transforming an 8-bit graphics processor data bus to the 24-bit width of the bit map. Many variations of this architecture are possible, including modifications for stripe, matrix, and packed-pixel organized bit maps.

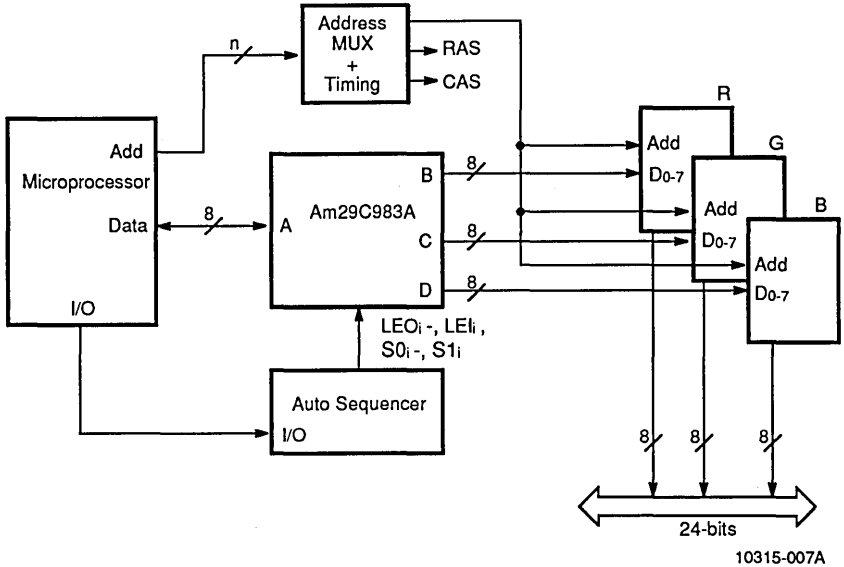


Figure 2–6. Graphics Display – 8/24-bit Bus Expansion

INTERLEAVING APPLICATIONS

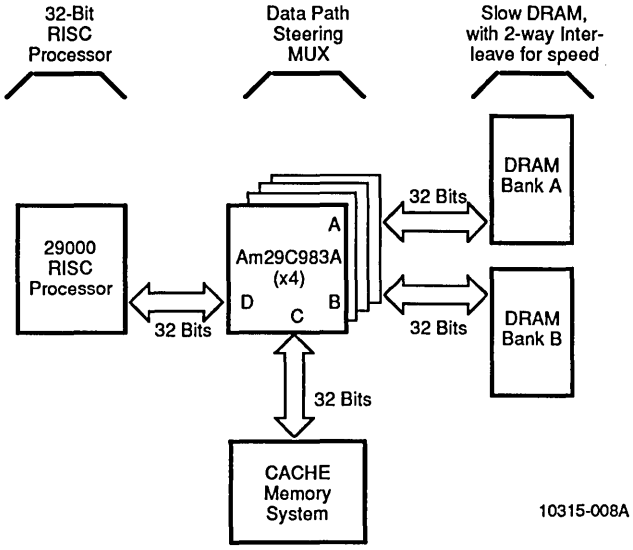
Interleaving is similar to funneling, in that byte-word compression is used to subdivide a wide word into a multitude of smaller words. However, the accessing of these smaller words is done independently. Further, different operations are performed on the smaller words simultaneously.

An additional method of interleaving is to transfer sequential words to two parallel systems, such as memory. This architecture allows the odd and even words to be simultaneously transferred to memory. During memory accesses, the overhead of odd and even word accesses can be overlapped; thus, substantially reducing the average transfer time in comparison to standard sequential accesses.

2-Way Interleaved Memory System

In a 2-way interleaved memory system the DRAMs are arranged into two physically separate memories - odd addresses in one and even addresses in the other. Because they are physically separate memories, both banks are accessed in parallel, starting the read of the next word while the previous word is being processed (see Figure 2–7).

Many microproprocessors require high speed cache, in addition to interleaved main memory, to avoid wait states and maintain high performance. The MBE is ideally suited to this application, providing the odd-even data path switching for bank interleaving, as well as a port for cache accesses. Additional performance is gained by using the MBE's internal latches for posted or deferred writes. In posted writes, the processor completes a write cycle with no wait states to what it thinks is the DRAM main memory. In reality, the data is written to the Am29C983A, which then completes the slow write to DRAM. The latches and data routing capability of the MBE allow the processor to run out of cache concurrently with writing data back to DRAM.



Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data. The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

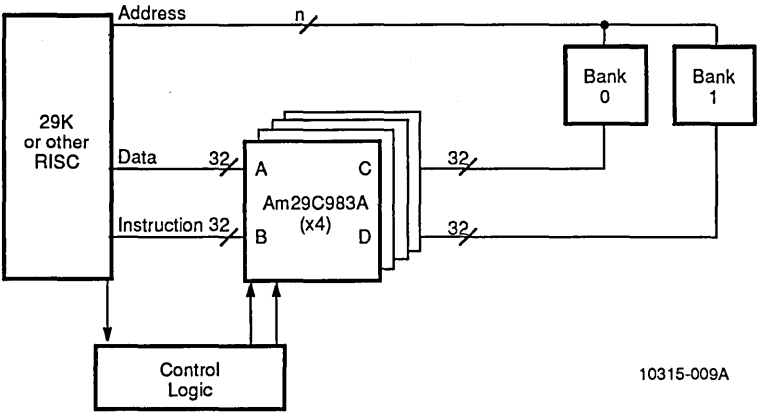
Figure 2–7. 2-Way Interleaved Memory System with Cache

Interleaved Data/Instruction Memory (RISC Memory System)

The key feature to the Harvard Architecture, on which the Am29000™ device and many other RISC microprocessors are based, is the utilization of separate data and instruction buses. Since parallel data and instruction routing is desired, the system designer will also prefer or require separate memory banks. However, some circumstances will require the data bus to have access to either memory bank. The Am29C983A enables such an access to occur with minimal logical overhead.

Figure 2–8 demonstrates the Am29C983A providing the data flow path between the Am29000 or other Harvard Architecture processor and interleaved data and instruction memory banks. Posted-write operations can be performed by latching in the data then sending a /Ready signal to the processor. The processor can then proceed to its next operation without waiting for the write cycle to be completed.

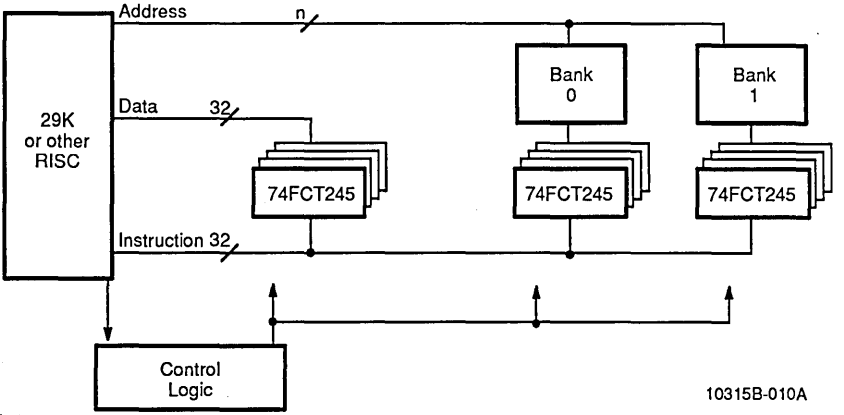
The MBE also allows access to the Instruction Bus via the Data Bus. This is desirable on systems which have the instruction code stored in volatile memory, as the code may need to be loaded into the data memory at power-up.



Note:
The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.
The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–8. Interleaved Data/Instruction Memory (RISC Memory System)

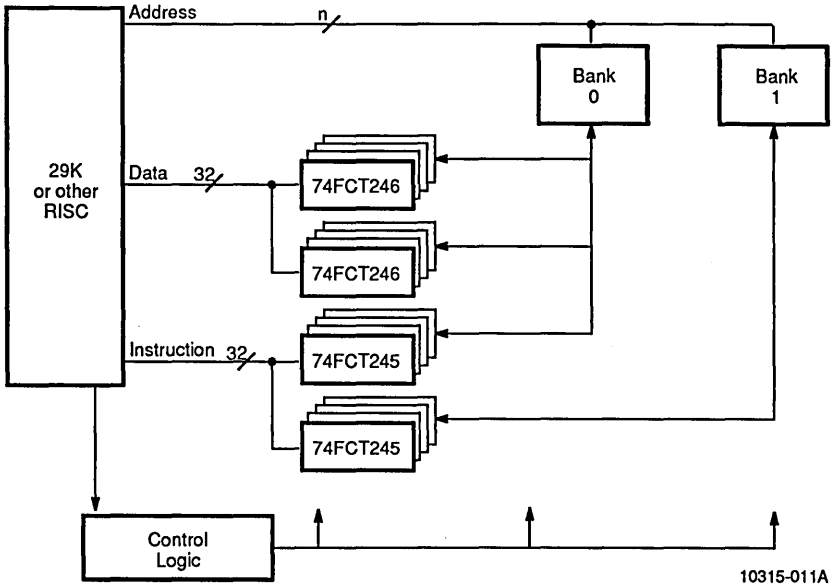
Bank interleaving can also be performed by using buffers, as demonstrated in Figure 2–9. The buffer design adds additional delay while data propagates through the buffers connecting the Data and Instruction buses. This forces the user to add one wait state to all data accesses, as invariably, the speed of the memory is chosen to match the instruction path and not the data path. Posted-write operations cannot be performed with this application; therefore, system performance will be limited.



Note:
This application cannot perform posted-write operations.

Figure 2–9. Interleaved Data/Instruction Memory using 7ns Buffers (RISC Memory System)

If posted-write operations are required, one could use buffers and transceiver/registers to complete the design, as shown if Figure 2–10. The data path will now incorporate 11 ns transceiver/registers in order to latch the data to be written to memory. Once again, a /Ready signal will inform the processor that it can proceed to its next operation. The propagation delay of accessing the Instruction bus via the Data bus will now climb to 18ns. Additional board space will be lost due to the 16 discrete devices and additional logic control requirements.



Note:
This application requires 19 ns delay time (Buffer + Transceiver/Register) to access the instruction via the data bus.

Figure 2–10. Interleaved Data/Instruction Memory using 7ns Buffers and 9ns Transceiver/Registers (RISC Memory System)

Tables 2–1 thru 2–6 calculate the memory access times allotted for the Am29C983A, 7 ns buffer and 7 ns buffer with 11 ns transceiver/register designs. This data is duplicated for 7.5 ns and 5 ns PAL control logic. The Am29C983A propagation delay (11 ns) is calculated from Select In to Port. Two buffer propagation delays (14 ns total) must be used in the buffer application in order not to add an extra wait state on data accesses. Only the transceiver/register propagation delay (11 ns) is used for the third design because data access times are being measured. Note that the buffer with transceiver/register design will require an additional 7 nanoseconds when accessing the Instruction bus via the Data bus.

All accesses are based on the following equation:

$$t_{acc} = 2t_{cyc} - t_{add} - t_{pd} - t_{su}$$

where t_{acc} = Allotted memory access time
t_{cyc} = Processor cycle time
t_{add} = Address valid delay (PAL t_{co})
t_{pd} = Buffer propagation delay
t_{su} = Am29000 Processor Data/Instr setup

Table 2–1. Am29C983As and 7.5ns PALs

Parameter	33MHz	25MHz	20MHz	16MHz
t_{cyc}	30	40	50	62.5
t_{add}	6.5	6.5	6.5	6.5
t_{pd}	11	11	11	11
t_{su}	4	6	8	8
t_{acc}	38.5	56.5	74.5	99.5

Table 2–2. 7 ns Buffers and 7.5 ns PALs

Parameter	33MHz	25MHz	20MHz	16MHz
t_{cyc}	30	40	50	62.5
t_{add}	6.5	6.5	6.5	6.5
t_{pd}	14	14	14	14
t_{su}	4	6	8	8
t_{acc}	35.5	53.5	71.5	96.5

Table 2–3. 7 ns Buffers, 9 ns Transceiver/Registers and 7.5 ns PALs

Parameter	33MHz	25MHz	20MHz	16MHz
t_{cyc}	30	40	50	62.5
t_{add}	6.5	6.5	6.5	6.5
t_{pd}	11	11	11	11
t_{su}	4	6	8	8
t_{acc}	38.5	56.5	74.5	99.5

Table 2–4. Am29C983As and 5 ns PALs

Parameter	33MHz	25MHz	20MHz	16MHz
t_{cyc}	30	40	50	62.5
t_{add}	4	4	4	4
t_{pd}	11	11	11	11
t_{su}	4	6	8	8
t_{acc}	41	59	77	102

Table 2–5. 7 ns Buffers and 5ns PALs

Parameter	33MHz	25MHz	20MHz	16MHz
t_{cyc}	30	40	50	62.5
t_{add}	4	4	4	4
t_{pd}	14	14	14	14
t_{su}	4	6	8	8
t_{acc}	38	56	74	99

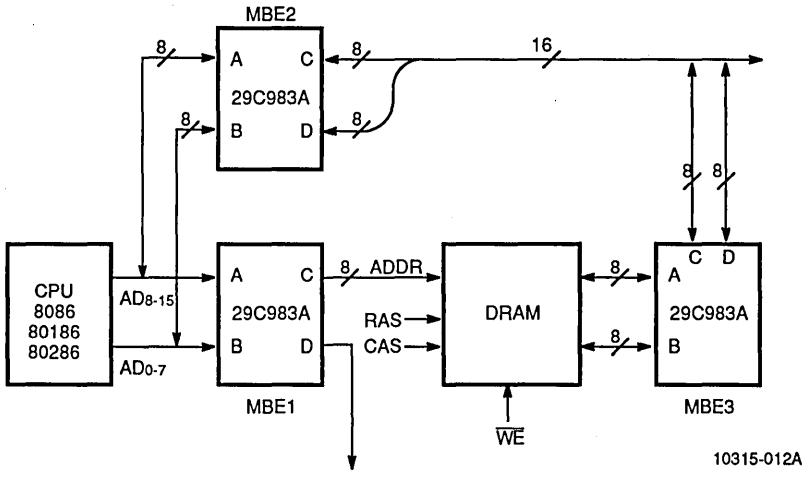
Table 2–6. 7 ns Buffers, 9 ns Transceiver/Registers and 5 ns PALs

Parameter	33MHz	25MHz	20MHz	16MHz
t_{cyc}	30	40	50	62.5
t_{add}	4	4	4	4
t_{pd}	11	11	11	11
t_{su}	4	6	8	8
t_{acc}	41	59	77	102

DATA ROUTING APPLICATIONS

This application illustrates the use of matched port decoding and Input/Output latches of the Am29C983A Multiple Bus Exchange in a simple yet powerful microprocessor-to-DRAM interface (see Figure 2–11).

MBE1 is used as an address latch to capture the 16-bit address into the A and B port input latches from the multiplexed address/data bus. It multiplexes upper and lower bytes of the address to directly drive the DRAM array. MBE2 is configured as an 18-bit wide bidirectional latch to drive the Am29C983A (MBE3) configured as another bidirectional latch for isolation from data bus activity.



Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.

The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–11. Microprocessor-Memory Interface

Microprocessor-Memory with EDC Interface

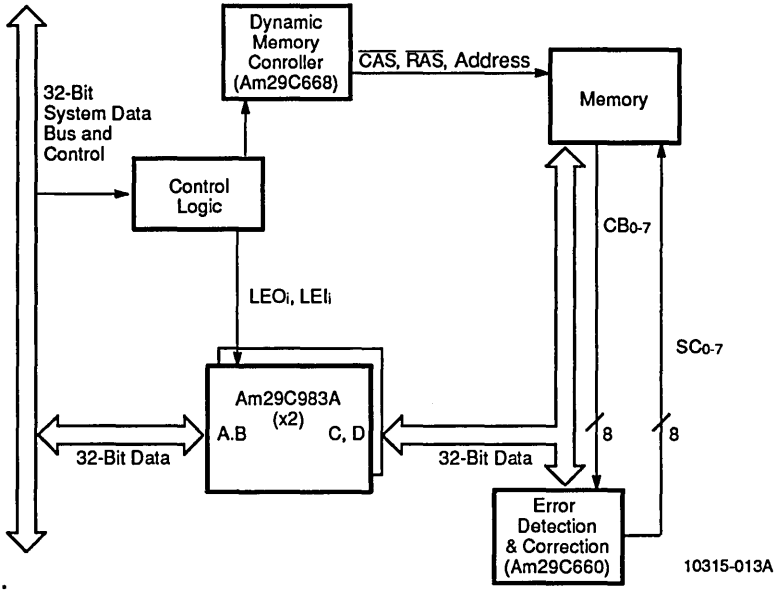
As memory size and density increase, protecting your memory from soft errors becomes more and more important. Error Detection and Correction (EDC) circuitry can correct random single-bit soft errors and detect all double-bit and some triple-bit errors. When a word is accessed from memory, it is checked for errors and if an error is found, the corrected data is written back to memory as well as to the data bus. Memory "scrubbing," which is the detection and correction of single-bit errors during normal refresh cycles, allows the system to maintain memory integrity without interrupting the microprocessor.

One complication associated with Error Detection and Correction is the increased data routing necessary to communicate between the microprocessor, dynamic memory controller, EDC and memory. This function can be simplified by using the Am29C983A to latch and drive data between the devices.

During write sequences, data is latched into the Am29C983As then driven to the EDC and memory. The EDC then generates checkbits and sends them directly to memory.

During a memory read, data is sent to the EDC and MBE simultaneously. The MBE routes the data to the system bus. If an error occurs, a Read/Modify/Write cycle is enacted. The EDC detects the error and sends an error message to the control logic. The EDC corrects the data, which is then rerouted to the system bus via the MBE. The control logic delays sending the READY signal to the microprocessor until the corrected data has been sent.

During memory scrub routines, the EDC performs a Read/Modify/Write cycle and writes directly to the memory.



Note:

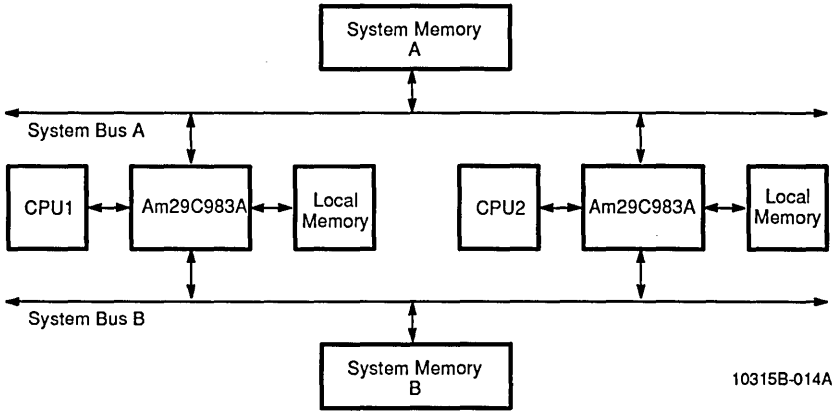
The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.

The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–12. Microprocessor-Memory with EDC Interface

Multiprocessing

The logical cross-point interconnect provided by the Am29C983A is ideal for many types of multiprocessor systems. The ability of any port to drive any other port or combination of ports permits the simultaneous updating of both system (global) and cache (local) memories. Alternatively, data from one system bus can be driven onto the other system bus while the CPU communicates with its local memory. Since the Multiple Bus Exchange cascades directly bit-wise, data paths of any width are easily accommodated, with no performance degradation, by merely tying corresponding port-select pins together. The 48-mA drive (I_{OL}) capability permits driving the system buses directly, saving board area and reducing system cost.

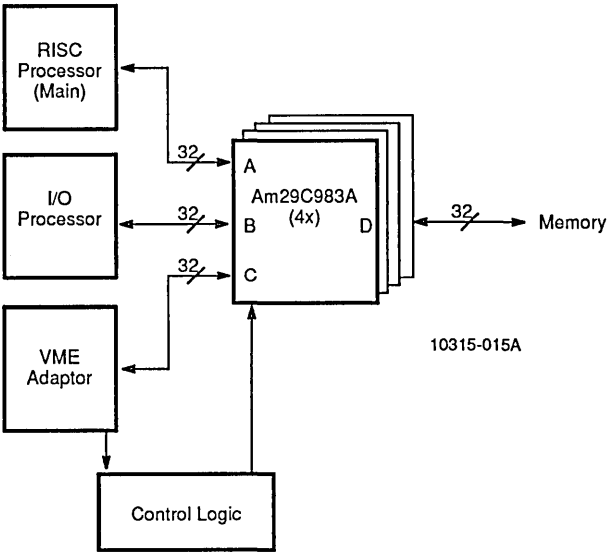


Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data. The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–13. Multiprocessing Application

Many applications have evolved to the point that multiprocessing has become the status quo. Workstation motherboard designs, as in Figure 2–14, are one such example. This application divides the processing workload across three microprocessors. The RISC processor operates as the central processing unit, the I/O processor manipulates and distributes data to and from the peripherals and the VME Adaptor controller manages all data distributed to and from the network.



Note:
The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.
The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–14. Workstation Design Using Multiple Processors

Byte Data Swapping

The Am29C982 can be used to shuffle, swap, or align data paths for a variety of computational and interface applications. For example, upper and lower bytes can be swapped, bidirectionally, to interface systems with different data format requirements. Bidirectional bit-order reversal is easily handled by wiring up the bits in proper order.

Computational applications include FFTs and other forms of array processing. The 14-ns maximum port-to-port propagation delay allows stacking of parts to achieve more complex forms of interconnect at reasonable performance levels. The port-to-port and control-to-port delays are closely matched, further easing the task of dynamic datapath switching.

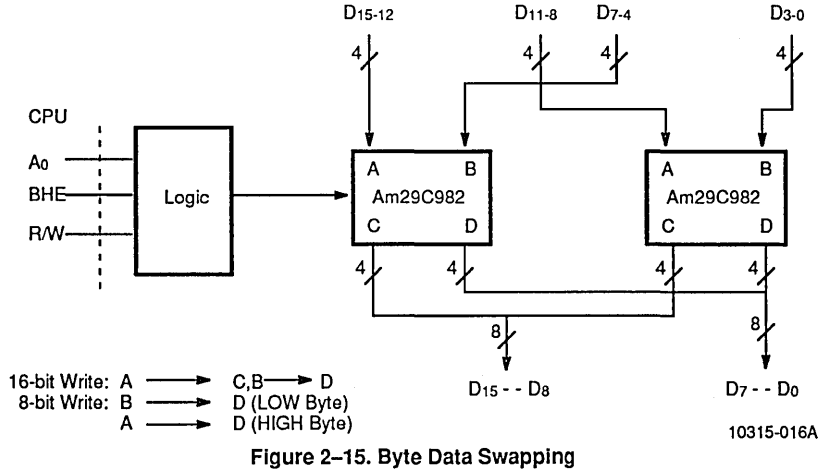


Figure 2–15. Byte Data Swapping

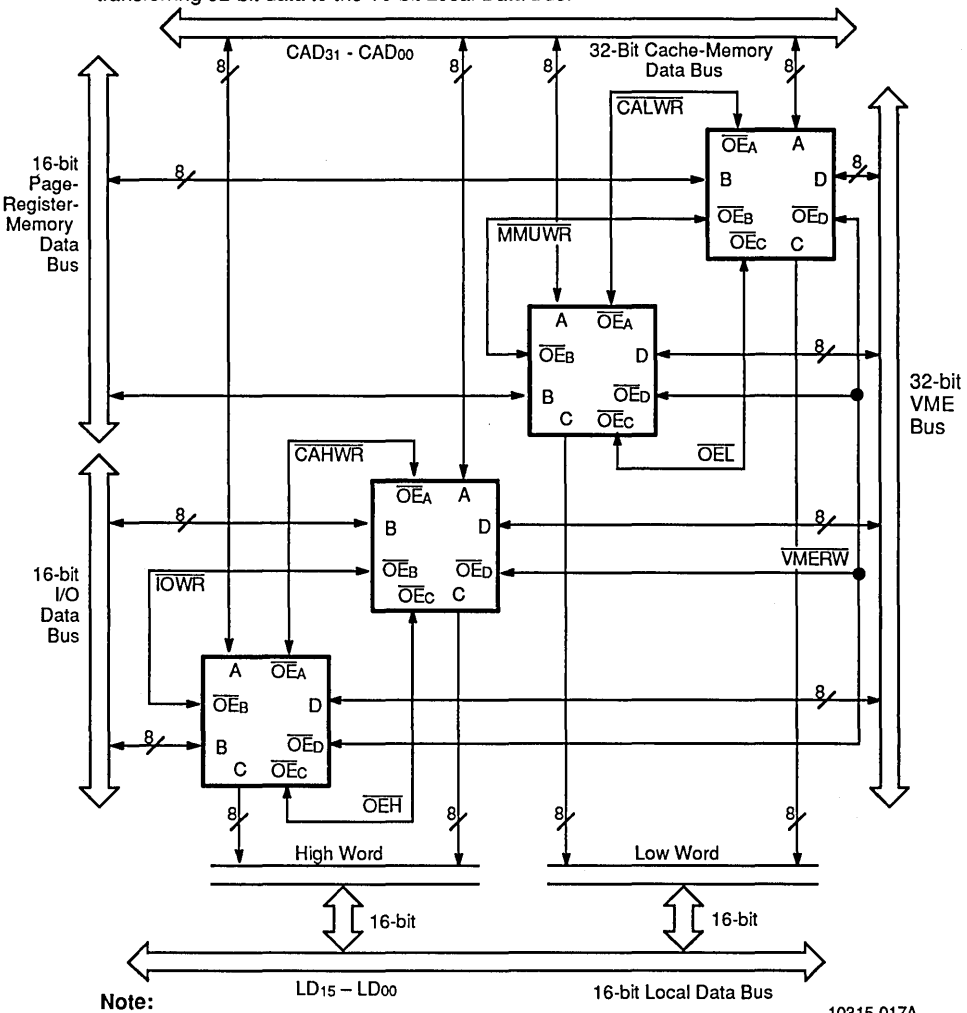
VME System Interface

The VMEbus™ was developed by Motorola, in association with other companies, to provide an open architecture. The VMEbus offers 8-, 16-, or 32-bit data and 16-, 24-, or 32-bit addressing and a 40 MByte/s bandwidth. Numerous products are offered for use with the VMEbus, including almost all processors, memories and memory boards, controllers, error-detection and correction circuits, and other support products.

The following application connects a 32-bit VME data bus to other 32- and 16-bit buses.

In this application, four Am29C983As provide data routing between the 32-bit VME Data Bus, the 32-bit Cache-Memory Data Bus, the 16-bit I/O Data Bus, the 16-bit Page-Register-Memory Data Bus and the 16-bit Local Data Bus.

The MBEs' input and output latches support the VME address pipeline mode. The Am29C983As' 48mA drive and voltage clamps allow direct drive of the VME and interconnected data buses. The MBEs also provide data funneling capabilities necessary for transferring 32-bit data to the 16-bit Local Data Bus.



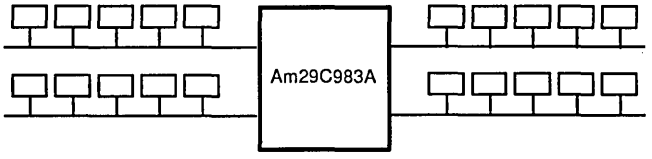
Note:
The Am29C983A has 9-bit wide data paths, so parity can be carried along with data. 10315-017A
The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2-16. VME Inter-bus Data Routing

Networking Applications

Non-Blocking Digital PBX or Matrix Switching Applications

Figures 2-17, 2-18 and 2-19 demonstrate 4-, 6- and 8-bus matrix switching techniques useful in non-blocking PBX or other network applications. This architecture greatly simplifies the PBX design by not only integrating the latches and buffers at each crosspoint switch function, but also by reducing overall control logic requirements.

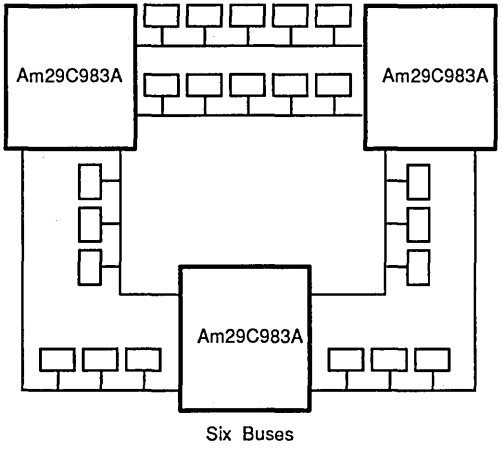


Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.

The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–17. Four-Bus Non-Blocking Digital PBX or Matrix Switch

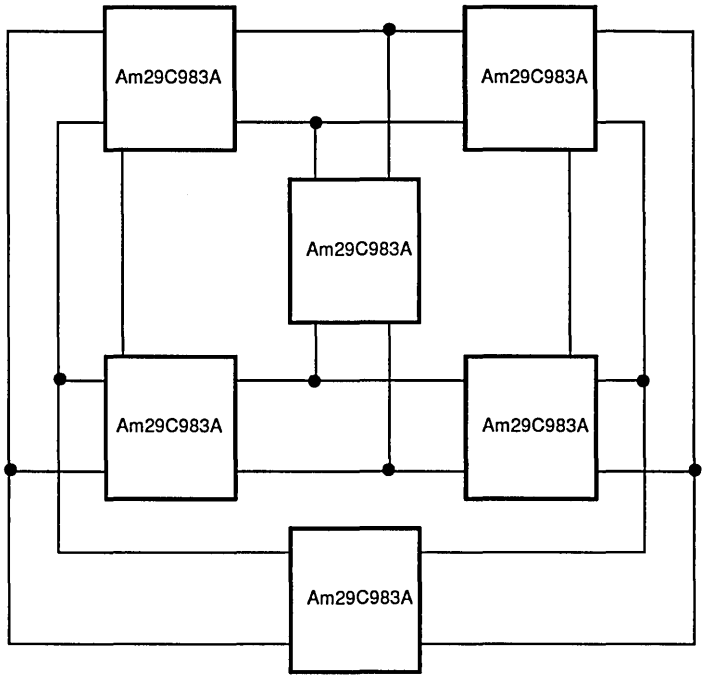


Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.

The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–18. Six-Bus Non-Blocking Digital PBX or Matrix Switch



Eight Buses (devices not shown)

10315B-020A

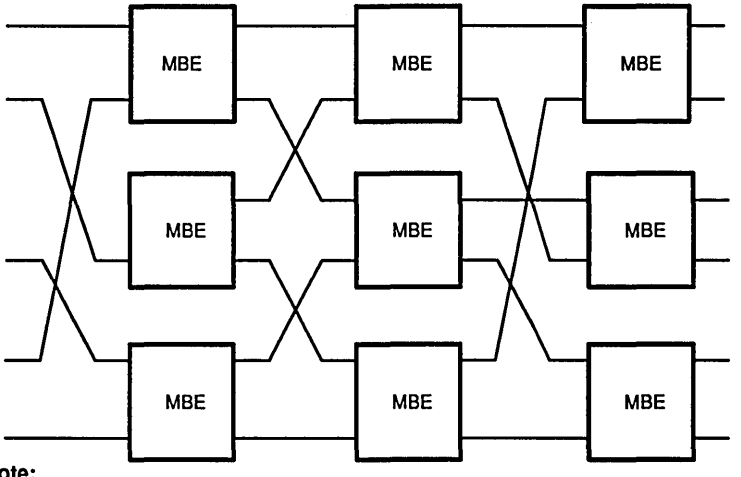
Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data. The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–19. 8-Bus Non-Blocking Digital PBX or Matrix Switch

Bidirectional Wideband Network Switching Applications

Figure 2–20 presents a bidirectional wideband network switching application in which the six 9-bit input channels can communicate with any of six output channels, or any one of six input channels can broadcast to from one to all six output channels, or any combination of the above using both selective channel and broadcast communication techniques.



10315B-021A

Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.

Figure 2–20. Bidirectional Switching Network

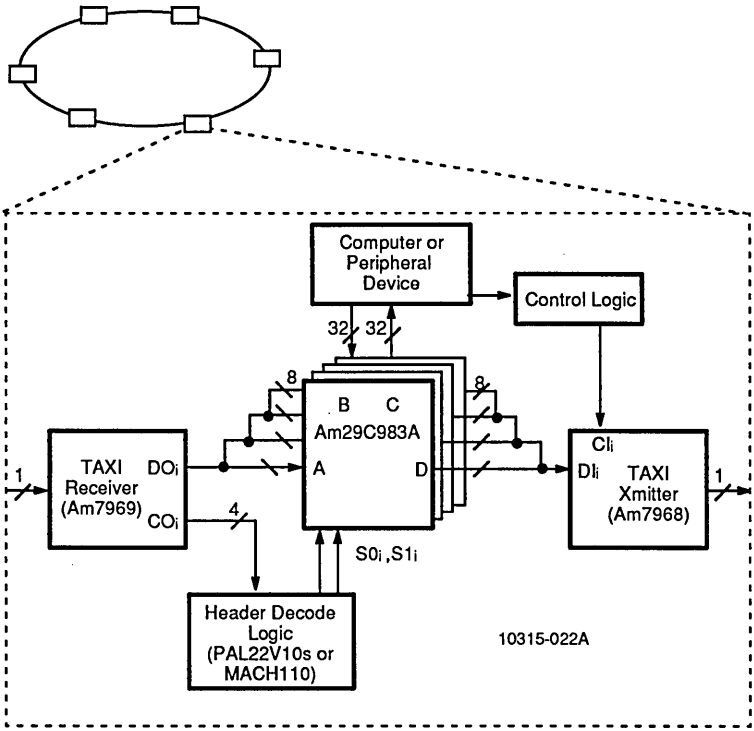
Packet Switching Ring Network Node

A packet switching ring network allows data to be shared among any computer or peripheral connected to the network. The ring network sends serial data in "packets" which consist of header information and data. The header information informs each node whether it should receive the data or allow the data to pass to the next node.

One can design a high-speed ring network by implementing AMD's TAXI chipset, the Am29C983A MBEs and header decode logic (see Figure 2–21). The TAXI chipset performs high-speed (125-175 MHz) node-to-node transfers, the Header Decode Logic controls the Am29C983A data paths, and the MBE is used as the network node switch and driver.

Data packets designated for the node are routed from Port A to Port C. Empty packets loaded at the node for other nodal destinations are routed from Port B to Port D. Information not intended for this node is passed through from Port A to Port D.

The header information is decoded by a state machine and is then address matched to the node address. If no match occurs, the data is passed onto the next node. The state machine can be implemented with AmPAL22V10s, or one high density MACH110. The addresses can be easily compared by using a content addressable memory, such as the Am99C10.



Note:

The Am29C983A has 9-bit wide data paths, so parity can be carried along with data.

The Am29C985 can be substituted for the Am29C983A if parity generation and checking is desired.

Figure 2–21. Packet Switching Ring Network Node

Ethernet Bridge

In this communications application, the Am29C983A serves as the link between two networks, accommodating simultaneous bidirectional data transfers: network to network, network to buffer memory, CPU to network, or CPU to buffer memory. The true logical crosspoint interconnect permits any two operations to occur simultaneously, or permits the broadcast of data from any one port to any or all of the other three ports.

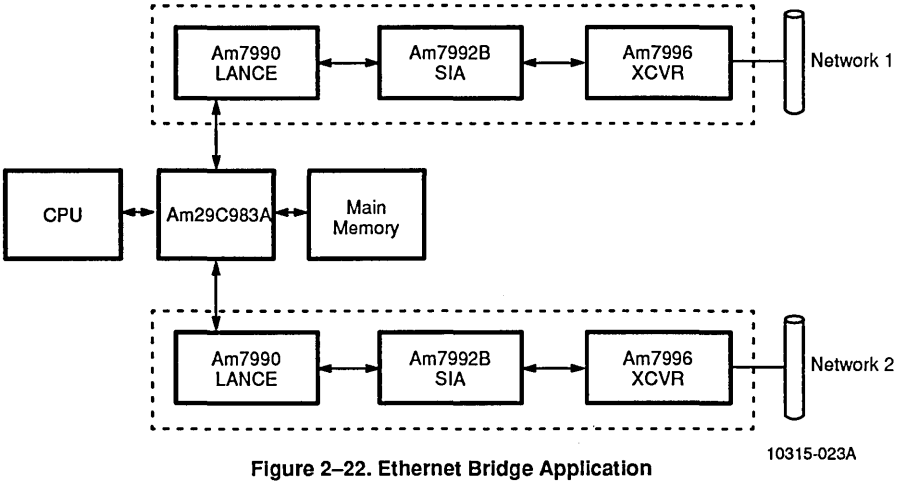


Figure 2–22. Ethernet Bridge Application

Digital Boxcar Integrator

This application illustrates use of the Am29C983A Multiple Bus Exchange (MBE) in a digital "boxcar" integrator. The integrator uses repetitive sampling and a background subtraction scheme to obtain accurate readings of periodic signals in the presence of noise (see Figure 2–23).

The Am29C983A MBEs are used to route and store a running sum of digitized data, signal as well as background. B port input latches can be used for signal, and A port input latches for background. Successive summation is performed by routing A port or latch data to the D port. Background subtraction is performed by connecting the A port to the C port, and the B port to the D port, and routing C port data to the ALU via the 2-to-1 multiplexer. The result is then routed via the C port of the Am29C983A MBE to the barrel shifter for integer division to convert running sums to averages. The output of the barrel shifter can be used to drive an output device, such as a pen plotter, after D/A conversion.

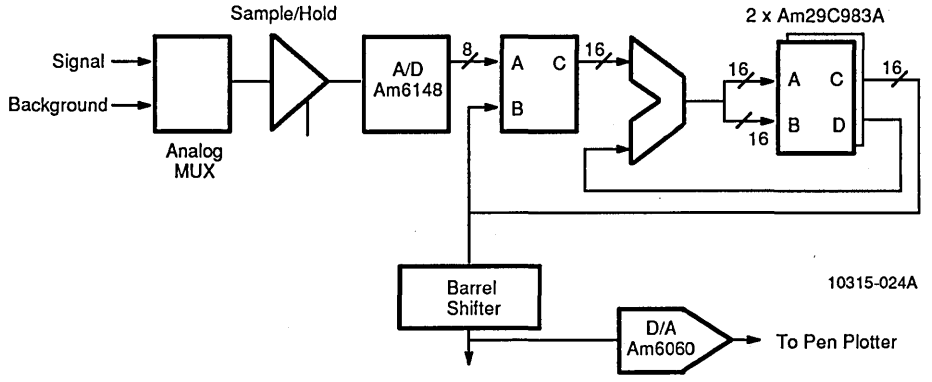


Figure 2–23. Digital Boxcar Integrator

Multiple-bus exchange ICs speed interbus communications

Two chips replace 28 discrete components to build a four-port crosspoint switch, 4 or 9 bits wide, for transferring data between four buses.

NICOLAS MOKHOFF

To link various system elements, traditional interface devices typically deal only with such circuit parameters as volts, milliamps, and nanoseconds. But this scenario overlooks managing interconnections efficiently. Now that picture has changed: With a couple of crosspoint IC switches, a system designer can dynamically manage the interconnection of system elements in multiprocessor, shared-resource, and computational applications.

The Am29C982 and Am29C983 multiple bus exchange (MBE) ICs replace 14 and 28 discrete devices, respectively. Each constructs a four-port crosspoint switch 4 or 9 bits wide. The switching function is a logical one instead of a direct physical connection between input and output ports. The two ICs can be applied to any bus-based digital system to switch data between up to four buses.

Most current digital systems are organized by bus, with data shuttling between sources and sinks over a common data highway. Such systems, though managing connectors and the number of wires efficiently, still are time-division multiplexed under strict rules. Such rules govern bus arbitration to determine which data source wins the right to talk and the length of time that source may occupy the bus. As long as one source transmits data over the bus, no others can. Because only one transfer can take place at time, interconnection efficiency comes at the expense of throughput.

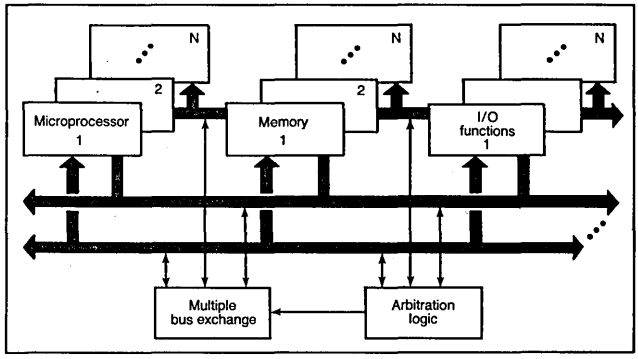
For its part, throughput can be improved by adding more buses to allow more than one transfer to occur at one time. Without communication between buses, however, the result is essentially separate processing of different tasks, rather than coherent shared processing of one overall task. To achieve coherency, the task of the multiple bus exchange chips is to tie all buses together *(Fig. 1)*.

One way to improve coherency is to rely on discrete components such as several bus interface devices and the required SSI/MSI glue logic. The number of discrete elements depends upon the number of buses to be switched, the number of ports, and the width of each port. This solution, though, consumes much board space and hampers throughput.

Or designers can opt for a custom gate array, which is costly and detracts from flexibility. On top of this, a typical gate-array scheme cannot drive high-capacitance loads.

"The Am29C982 and the Am29C983 offer a superior alternative to the discrete as well as gate array implementations of a bus multiplexing scheme," says Roy Sellinger, manager of directorate marketing. "By using AMD's state-of-the-art CMOS technology and a clever bus-selection coding scheme, the discrete functional blocks are integrated to offer a flexible and high-speed solution at very low standby power dissipation for a board space-saving of up to 80%."

The ICs share a similar structure. The input for each port (either 4 or 9



1. For bus multiplexing, a multiple bus exchange (MBE) can go to work in any scheme having several buses. In a typical multiprocessor system, the bus exchange chip gives designers needed flexibility not only to process different tasks separately but also to share coherent processing.

bits wide) is buffered and distributed along an internal bus to multiplexers at each of the other ports on the Am29C982 or at all the ports on the Am29C983. Port selection is independent for each port.

A common coding rule for all ports specifies that the 2-bit port select code asserted at each port must always refer to the source of data. This independent matched-port selection simplifies using the buses and avoids the decoding delays inherent in a centralized, encoded port-selection scheme.

On one hand, if the D port has 00 asserted, then the source data is the "A" port. On the other hand, if the A port has 00 asserted, then the A port is the source of data. For the Am29C982, a port selecting itself means that the port is an input and that the drivers are internally gated to a high-impedance state.

For the Am29C983, the Output Enable signal for each port is brought out to the user so that a port may select itself and store data in the port's output latch, for later transmission back out on the same bus. This readback facility is useful for diagnostics, in which a bus connected to one port can send data to any or all of the other ports and read back from its own port the data that was sent.

The two CMOS devices can drive 48 mA and exhibit typical propagation delays of 9 ns from port to port and 10 ns from control to port. Bus Disable times are shorter than Bus Enable times to avoid contention and minimize system noise. The Am29C982 chip has two power and two ground pins to support a maximum of 12 outputs switching simultaneously from the 16 inputs available. In comparison, the Am29C983 IC has four power and eight ground pins, resulting in one power and two ground pins per port. The drivers in both devices use AMD's proprietary edge-rate control circuitry to minimize the effects of ground balance.

MANY APPLICATIONS

The logical crosspoint interconnection supplied by the multiple bus exchange chip fits many multiprocessor configurations. In one such system either of the two chips serves to update simultaneously both system (global) and cache (local) memories.

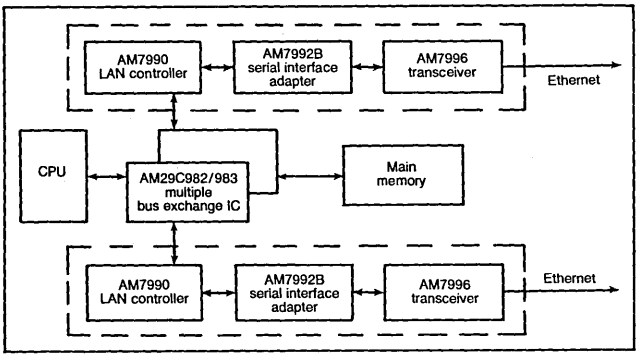
Or data from one system bus can be driven onto the other system bus while the CPU communicates with the local memory. Because multiple bus exchange chips can be cascaded directly in terms of bits, data paths of any width are easily accommodated without sacrificing performance by simply tying the corresponding port select pins together. The 48-mA output capability allows driving the system buses directly, saving board area and reducing system cost.

In a multiprocessing system with multiple access memories, for instance, two Am29C983s can latch up to three sources of addresses while also performing the address multiplexing necessary for row address and column address selection. On the data side, the two chips can deliver bidirectional multiplexing between dynamic RAM memory and any or all of the available processor buses.

In a communication task, the multiple bus exchange chip links two networks, accommodating simultaneous bidirectional data transfers in one of many configurations: network-to-network, network-to-buffer memory, CPU-to-network, or CPU-to-buffer memory *(Fig. 2)*. The true logical crosspoint interconnection allows any two operations to occur simultaneously; or data can be broadcast from any one port to any or all the other three ports.

The chip can also help shuffle, swap, or align data paths for various interface and computational applications. For example, upper and lower bytes can be swapped bidirectionally to link systems with different data format requirements. Bidirectional bit-order reversal is easily handled by wiring up the bits in proper order.

Some computational applications that can be handled by the multiple



2. In a typical communication task, the multiple bus exchange links two Ethernets, for example. With the bus exchange's true logical crosspoint interconnection, two operations can occur simultaneously, or data can be broadcast from any one port to any or all of the other three ports.

bus exchange include fast Fourier transforms (FFTs) and other forms of array processing that require dynamic switching of data paths. With the 14-ns port-to-port propagation delay, parts can be stacked for more complex interconnections while maintaining reasonable system performance.

Although originally intended to take on multiprocessor applications, the multiple bus exchange chip can also stand in for more conventional interface parts. For example, by hard-wiring the Port Select pins so that each port receives data from the complement of that port (A-D, D-A, B-C, and C-B) and connecting A and B as well as C and D Output Enables, the Am29C983 functions as an 18-bit-wide bus transceiver.

And by using the output Latch Enable pins, the chip works as an 18-bit-wide bidirectional register. As a result, two chips, occupying 2 $in.^2$ of board space, along with just two inverters, constitute a 36-bit-wide bidirectional register that can drive a bus and meet the data-path requirements of 32-bit buses with byte parity.□

CHAPTER 3
Design Methodology

INTRODUCTION

This chapter includes an application note describing AMD's proprietary output structure which minimizes ground-bounce by controlling output edge-rates. The application note assesses ideal drivers and recommends real world solutions to reduce ground bounce and system noise. All members of the Multiple Bus Exchange Family incorporate these system friendly output structures.

Minimization of Ground Bounce Through Output Edge-Rate Control

The development of fast, high-current integrated circuits has brought about a phenomenon known as ground bounce. This is especially noticeable in bus-driving applications, where individual devices can have multiple outputs switching very high currents simultaneously.

There are three symptoms associated with the phenomenon:

- Outputs switching from HIGH-to-LOW exhibit excessive ringing, which may cause multiple transitions at inputs connected to that output.
- The ringing also appears at non-switching outputs which are in the LOW state. This may also cause unwanted transitions at inputs connected to those outputs.
- If the device contains storage elements, the ringing may corrupt the data stored in these elements.

Ground bounce is associated with parasitic inductance and resistance in the power-supply connections. These parasitic effects exist within all integrated circuits and may not totally be eliminated. Poor board design will also contribute to the problem. The following discussion covers the cause of ground bounce in CMOS circuits, and describes AMD's output-driver circuit design that minimizes the problem. Accompanying photographs show an example of the driver in operation.

THE IDEAL DRIVER

Figure 1 shows an ideal totem-pole output driver. The two transistors are switched on alternately, the upper one for a logic '1', and the lower one for a logic '0'. Apart from a brief period of overlap during switching, the two transistors are never on together. For the high-impedance state of 3-state outputs, both transistors are turned off. The load connected to the totem-pole output is adequately modeled as a parallel R-C circuit.

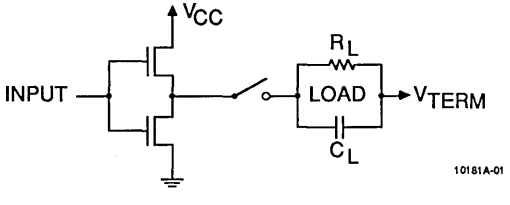


Figure 1. Ideal Driver

While this is an ideal driver, it is not constructed with ideal transistors. Each transistor has a finite impedance when in the 'on' state. This impedance manifests itself in three ways; it affects the slew rate of the output, the dc level of the output,and it limits the short-circuit current.

Before a transition, the load capacitor is charged according to the current output state ('0' or '1'). When the output transistors switch, they charge or discharge the load capacitor, and their impedance is part of the R-C time constant, which determines the slew rate of the output. In this respect, lower impedance is better. With a lower impedance, the load capacitance can be charged or discharged to the required output level faster, thus permitting higher operating speeds.

When the output voltage has stabilized at the desired logic level, the dc current flowing through the transistor impedance creates a residual voltage across the transistor (I-R drop). The output voltage specifications require that this residual voltage be kept below maximum values (V_{OL}). Again, a lower impedance is better, allowing higher output currents at any given V_{OL}.

However, even in the ideal case, the impedances should not be arbitrarily small, since they also control short-circuit current. If an output is inadvertently connected to one of the power supplies, or to a second output in a different state, these impedances will limit the power dissipation in the device and prevent potential destruction.

It would appear that the optimum design would be to make the impedance just large enough to protect the device under short-circuit conditions, while maximizing slew-rate and drive capability. This assumes that die area is not a consideration, since low impedance transistors are physically large. However, in the real world, parasitic effects cause this choice to lead to far from optimum results.

THE REAL WORLD

The practical problems that arise concern parasitic effects in the connections to the transistors. Between the output of the driver and the load, there is a small bond wire and a trace from the package bonding pad to the external pin. These connections are both resistive and inductive.

Publication #	Rev.	Amendment	Issue Date
10181	A	/0	3/88

A similar parasitic impedance is also found in the ground pin of the device. Additionally, it is not possible to locate all outputs physically close to the ground connection on the die. The deposited metal trace that connects the output driver to the ground pad also contributes parasitic resistance and inductance.

In the circuit of Figure 2, only effects in the ground connections are shown. Similar parasitics must exist in the V_{CC} connections but, since requirements for V_{OH} are less demanding, higher-impedance pull-up transistors can be used. This reduces the effect of the parasitic impedance. Experience has shown the problem to be associated with the HIGH-to-LOW transition and outputs in the LOW state, hence the name ground bounce.

Before a HIGH-to-LOW transition, the load capacitor is charged to the HIGH state. During the transition, the pull-up transistor turns 'off' and the pull-down transistor turns 'on' to discharge the load capacitor. The very low impedance of the pull-down transistor causes the parasitic impedances to interact with the load to form a step-excited L-C-R network. This results in ringing on the output.

While the output might quickly reach V_{OL}, it will not remain there due to the ringing. The output may not be considered a LOW until the output has stabilized to the point that it remains below V_{OL}. During the ringing, the output could exceed the actual threshold (as opposed to V_{IH}, the guaranteed input HIGH level) of an input to which it is connected, causing multiple transitions.

Other outputs in the same device may also be affected because the output voltages are referred to the internal device ground. The ringing causes this internal ground to move away from external ground. The other LOW outputs are connected to the internal ground through a low-impedance transistor, and movement in this ground will therefore be reflected at these outputs. Again, this may lead to erroneous transitions in devices connected to these outputs. In addition, the movement of the internal ground may corrupt data stored in the registers.

At this point it is worth noting a different effect also caused by parasitic impedances in the power connections. In accordance with industry practice, the output delays of AMD parts are measured with only one output switching. When more than one output switches, the impedance in the common power-supply connections reduces the current available to each output, thus increasing the delay. This effect occurs in any integrated circuit.

THE SOLUTION

The effects of the load capacitance and the interconnection parasitics are inescapable, although the latter may be minimized by good chip design. The solution must lie in modifying the pull-down transistor.

The AMD solution structures the pull-down transistor so it limits the initial current minimizing the transient; then, after a delay, its strength increases to provide sufficient current to maintain the LOW logic level. This is achieved by using two transistors contained in parallel output buffers. These buffers are designed to have different drive capabilities. One has small transistors with low drive which is used to initiate the transition without causing the shock excitation. After a short delay, a second larger driver turns on. This driver completes the transition, and is capable of sinking the necessary dc current to maintain V_{OL}. Additionally, a similar parallel structure is used in the pull-up circuit to moderate the LOW-to-HIGH transition.

While introducing delay into a high-speed circuit may appear counter productive, that is not the case. The primary objective must be to achieve a stable output

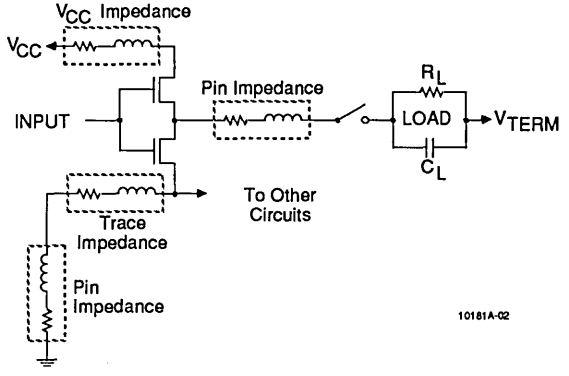


Figure 2. Real Driver and Parasitics

voltage level less than V_{IL} as quickly as possible. The non-controlled output signal may reach V_{IL} sooner, but it will not remain there until the ringing has subsided. This may require more time than the specified output delay, and a good design must allow for this. The modified AMD output will provide a stable, usable voltage level in less time in spite of the added delay.

A secondary effect of limiting the current during transition is that the slew rate is controlled by the driver rather than power-supply parasitics. This generally leads to less delay variations (skew) caused by a different number of switching outputs.

TEST RESULTS

The output driver described above has been incorporated into the Am29C982 4-bit x 4-port Multiple Bus Exchange. This product was mounted in a test jig and its output characteristics photographed. For comparison, a similar test jig was used to test an Am29C821 10-bit register, with traditional 24 mA totem-pole outputs, and a competitive 48 mA output version.

The jigs were designed to eliminate, as far as possible, electrical effects due to the mounting and probing so that intrinsic characteristics of the IC could be observed. It should be noted that the layout and dc loading found on a carefully designed pc board could lower the current transient and its effects. In that respect the following results should be considered worst case.

The test jigs were constructed of double-sided copper-clad board. The two copper planes were used for V_{CC} and GND. Holes were drilled to accept the ICs, and only sufficient copper was cut away to allow clearance of active pins. The ICs were soldered directly into this board. Decoupling was provided by a tantalum capacitor, and a .01 µF ceramic capacitor mounted close to the V_{CC} pin.

Each output was loaded with 47 pF to GND. The leads of this capacitor were cropped short, and the capacitor was soldered directly to the IC pin and the ground plane. Outputs to be observed were connected to SMB sockets through 453 Ω resistors. Each series resistor, together with a 50 Ω oscilloscope input impedance, creates a standard 500 Ω load. The leads of each resistor were cropped short and soldered directly to the IC pin and the socket. The socket body was soldered to the ground plane.

These SMB sockets were connected by coax to the 50 Ω oscilloscope input (Tektronix 7854 with 7S14 sampling input plug-in). The series resistance creates an attenuation of 10:1. The vertical scale is 2 V/div, and the horizontal scale is 20 ns/div.

On the Am29C821, input D_0 was grounded to provide a "quiet" output Y_0. Y_0 was chosen, because it is farthest from the ground pin, and therefore, most susceptible to noise in the supply. Inputs $D_{1\text{-}9}$ were all connected to output Y_8 through a single inverter. The device was then clocked, such that the nine outputs ($Y_{1\text{-}9}$) toggled simultaneously.

Photograph 1 shows the outputs Y_0 and Y_1 during a HIGH-to-LOW transition. The quiet output (Y_0) "bounces" approximately 2.2 V. The maximum positive ringing in Y_1 is approximately 1.5 V. Observation of the transition on the Y_8 output, which is closer to the GND pin, revealed slightly less ringing.

It should be noted that the capacitive loading of the quiet output reduces the initial transient slope and slightly reduces the positive excursion. Since an actual application will present capacitive loading, this test is representative. Without the capacitor, the positive excursion was approximately 0.2 V greater.

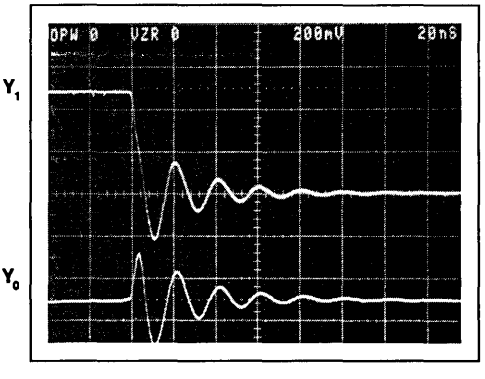


Photo 1. Am29C821

Note
Vertical Scale: 2.0 V/div.
Horizontal Scale: 20 ns/div.

Photograph 2 shows the same outputs during a LOW-to-HIGH transition. Here the effect is much less; the excursion of Y_0 is approximately 0.9 V. In this case, Y_9, which is farther from V_{CC}, exhibited slightly more ringing.

The same tests were performed on a competitor's version of the Am29C821. The results are shown in photographs 3 and 4. As expected, the 48 mA outputs of this part create considerably more noise than the 24 mA outputs of the AMD part.

To test the Am29C982 Multiple Bus Exchange, the A-port was configured as an input that was directed to the B-, C- and D-Ports which were outputs. A_0 was grounded, and a square wave was applied to A_{1-3}. This again gave nine switching outputs and three quiet outputs.

The outputs on D_0 and D_3 are shown in photographs 5 and 6 for HIGH-to-LOW and LOW-to-HIGH transitions respectively. The effect of the modified output driver is quite clear. Both ringing and ground bounce have been reduced dramatically.

The maximum ground bounce during the negative transition is approximately 1.1 V, while the positive ringing is limited to approximately 0.8 V. When compared to Am29C800, this represents a 50% reduction in noise, while increasing the output current from 24 mA to 48 mA.

The tests on the Am29C982 were repeated with the load capacitors increased to 470 pF. The results are shown in photographs 7 and 8. The amplitude of the ringing and ground bounce are the same or less than with the 47 pF load. The ringing frequency is predictably lower due to the larger capacitor.

The improved output structure is also used in the Am29C983 9-Bit x 4-Port Multiple Bus Exchange. A more comprehensive analysis of this output transition control technique, including results from additional package options and the AM29C983, are being prepared for future release.

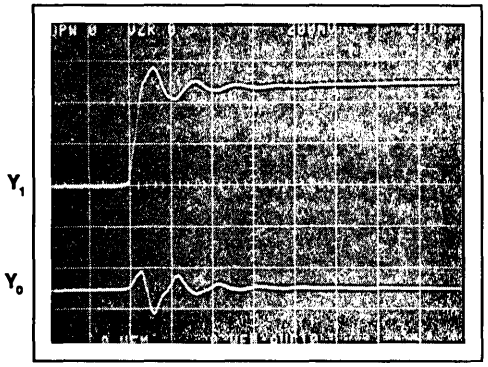


Photo 2. Am29C821

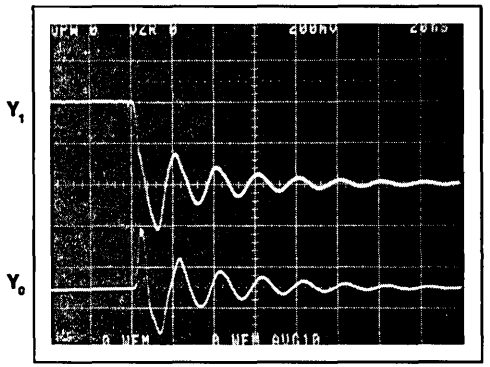
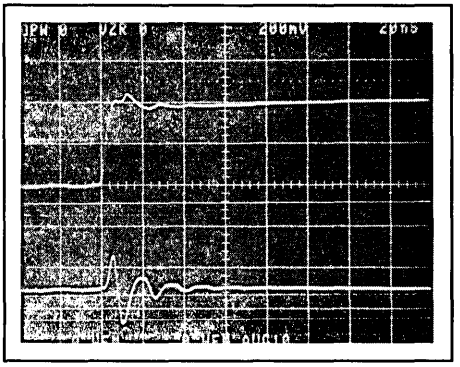


Photo 3. Competitor's C821



Note
Vertical Scale: 2.0 V/div.
Horizontal Scale: 20 ns/div.

Photo 4. Competitor's C821

While these tests were performed on individual, randomly selected parts, and cannot therefore be considered definitive, they do indicate the effectiveness of the new output structure. It is AMD's intent to incorporate outputs with this improved current characteristic into future bus interface devices.

GOOD DESIGN PRACTICE

Ground bounce cannot be eliminated through good design practice alone. However, the situation can be aggravated considerably by failure to follow good practices. The following guidelines are suggested:

- Ensure good power supply connection. Power supply planes are essential, and wire wrap should be avoided. Provide good wide-band decoupling. The ringing occurs at very high frequency, in the gigahertz region. Therefore, a comprehensive decoupling scheme should be designed, including chip capacitors very close to the high-drive devices.
- In general, the layout rules followed should be similar to those for ECL. Branching traces should not be used for signals that are to be routed to more than one input. Traces should pass from one input to the next without Ys or Ts. If possible, the traces should have controlled impedance, and should be terminated.

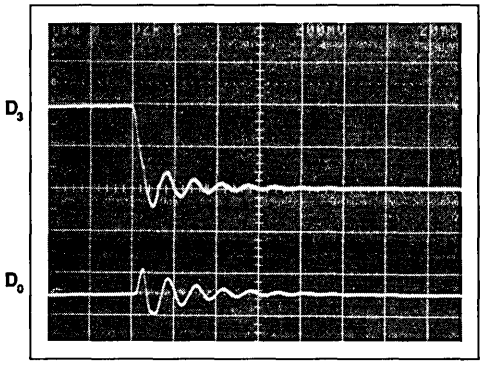


Photo 5. Am29C982

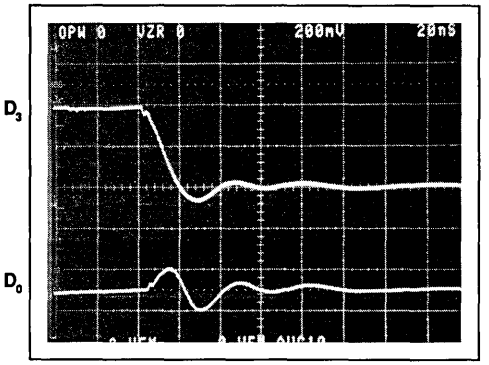


Photo 7. Am29C982 (470 pF)

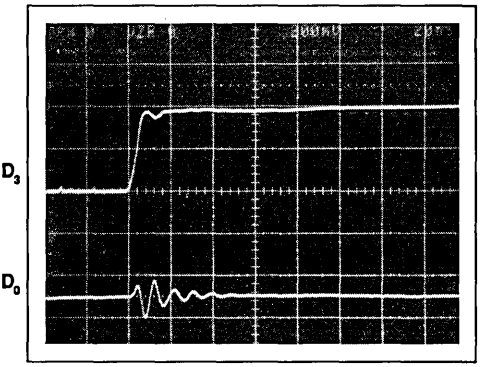


Photo 6. Am29C982

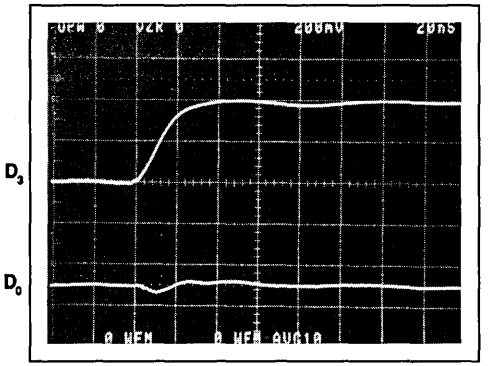


Photo 8. Am29C982 (470 pF)

Note
Vertical Scale: 2.0 V/div.
Horizontal Scale: 20 ns/div.

CHAPTER 4
General Product Information

INTRODUCTION

This chapter includes AMD's testing methodology used to guarantee the highest caliber Multiple Bus Exchanges, testing considerations, power dissipation considerations and typical device operation and description data.

General Product Information

TEST PHILOSOPHY AND METHODS

The following points give the general philosophy that is applied to properly engineered tests to be implemented in an automated test environment. The specifics of what philosophies are applied to which test are shown in the data sheets.

ATE Loads

AC loads specified in the data sheet are used for bench testing. Programmable automatic tester loads, which simulate the data sheet loads, may be used during production testing.

Automatic test equipment (ATE) and its associated hardware has stray capacitance that varies from one type of tester to another, but is generally around 50pF. This makes it impossible to make direct measurements of parameters that require smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float-delays" that measure the propagation delays into the high-impedence state, and are usually specified at a load capacitance of 5pF. In these cases, the ATE test is performed at the higher load capacitance (typically 50pF), and engineering correlations based on data taken with a bench set-up are used to determine the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical ATE is not capable of switching loads in mid test, it is impractical to make measurements at both capacitances, even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is determined from engineering correlations based on data taken with a bench set-up and the knowledge that certain DC tests are performed in order to facilitate this correlation.

Threshold Testing

The noise associated with automatic testing, the long inductive cables and the high gain of devices near threshold frequency give rise to oscillations when testing high-speed circuits. These noise-associated problems are not indicative of a reject device, but instead, of an overtaxed system. To overcome this tester limitation, thresholds are tested at least once during associated DC parametric tests, thus assuring the proper logic-recognition levels. Thereafter, "hard" HIGH and LOW levels are used for other tests. Generally, this means that function and AC testing are performed at "hard" input levels.

AC Testing

Some AC parameters cannot be measured accurately on automatic testers because of tester limitations. In these cases, the parameter in question is tested by correlating the tester data to bench data. Certain AC tests are guaranteed by correlating to other tests that have already been performed. In these cases, the redundant tests are not performed.

Output Short-Circuit Current Testing

When performing I_{SC} tests on devices containing latches or registers, great care must be taken to ensure that undershoot caused by grounding the high-state output does not cause the internal latch to change state. To avoid this effect, it is common to make the measurement at a voltage (V_{OUT}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result is identical to the V_{OUT}=0, V_{CC}= Max. case.

TYPICAL CAPACITIVE VALUES

The following table shows typical input and output capacitance values for MBEs in plastic packages.

Device	C_{OUT}	C_{IN}
Am29C982	10 pF	5 pF
Am29C983A	11 pF	6 pF
Am29C985	11 pF	6 pF

DEVICE GATE COUNT

Part Number	Equivalent Number of Gates
Am29C982	113
Am29C983A	117
Am29C985	217

DIE DIMENSIONS

Part Number	Dimensions (In Mils)
Am29C982	151 x 155
Am29C983A	178 x 183
Am29C985	178 x 183

PACKAGE INFORMATION

	Parameter	LCC	PLCC	PDIP	Unit
Am29C982	Θ_{JA}	54	57	56	°C/W
	Θ_{JC}	10	11	11	°C/W
Am29C983A	Θ_{JA}	–	34	–	°C/W
	Θ_{JC}	–	8	–	°C/W
Am29C985	Θ_{JA}	–	34	–	°C/W
	Θ_{JC}	–	8	–	°C/W

TYPICAL SWITCHING SPEEDS VS. LOAD CAPACITANCE

AC delays in the MBE data sheets are specified for a fixed, given capacitive load. The following graph shows the typical effects of increased capacitive loads on propagation delays. Note that this graph displays typical derating, over the entire V_{CC} and temperature range.

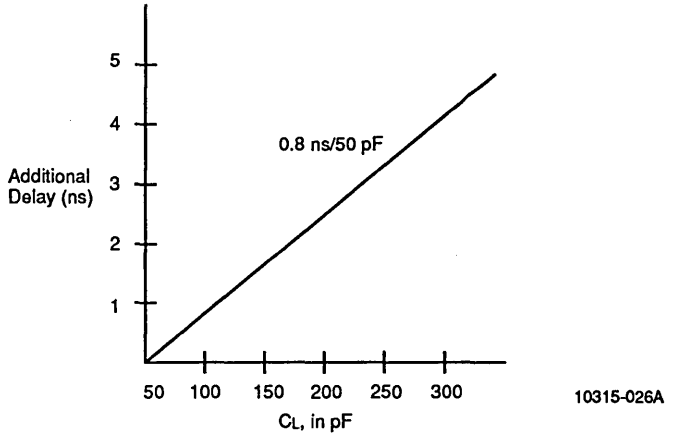


Figure 4–1. Typical Propagation Delay vs. Load Capacitance

ESD PROTECTION

The Multiple Bus Exchanges are protected from ESD damage up to 2000V.

POWER DISSIPATION CONSIDERATIONS FOR CMOS DEVICES

CMOS bus interface devices are rapidly invading the arena previously dominated by bipolar devices, because CMOS technology has made sufficient progress to provide an alternative to bipolar in terms of both high-speed and high-drive. In addition, at low data rates, CMOS devices offer much lower power dissipation when compared with their bipolar counterparts. However, there are some claims made with regard to this "power advantage." Statements such as "CMOS consumes negligible power when driving high-speed buses" are too general and can be misleading. This section explains the basics of switching in CMOS circuits and provides guidelines for calculating power dissipation in CMOS parallel interface circuits.

Definition of Terms

$I_{CC(Q)}$	–	Quiescent power supply current
$I_{CC(T)}$	–	Power supply current component per input at TTL HIGH level
$I_{CC(D)}$	–	Dynamic power supply current expressed in μA/MHz/bit
f	–	Equivalent toggle frequency at the output
C_L	–	Load capacitance per output
C_i	–	Lumped equivalent circuit capacitance per bit

Power Supply Current Components

A CMOS circuit operating in a TTL environment has three power supply current (I_{CC}) components. The total I_{CC}, when multiplied by V_{CC}, will determine the total power dissipated in the device.

The first component is the quiescent current $I_{CC(Q)}$. This is the leakage current through the device when all inputs are tied to either V_{CC} rail or GND, and all outputs are open (no load). This current is typically in the microamps region, and represents STAND-BY (or quiescent) power dissipation. In addition, the MBE devices contain power-up/down disable circuitry. This unique circuit contributes to total $I_{CC(Q)}$ and is the dominant contributor to total $I_{CC(Q)}$ for these devices. However, $I_{CC(Q)}$'s contribution to the total power dissipation is insignificant at high data rates.

The second component is $I_{CC(T)}$, the current in TTL-compatible input stages. Because of the difference in threshold for N-channel and P-channel devices, each input stage offers a DC path from V_{CC} to GND. This I_{CC} component is a function of input voltage applied. Figure 4–2 shows a typical $I_{CC(T)}$ characteristic as a function of VIN.

Considering "realistic" worst-cast conditions, $I_{CC(T)}$ is normally specified at $V_{IN} = 3.4V$. Its value is given on a per input basis. To determined the total $I_{CC(T)}$ per device, one needs to know the number of inputs and the duty cycle for those inputs in HIGH state.

Note that the $I_{CC(T)}$ component applies to CMOS circuits operating in a TTL environment and driven by bipolar TTL circuits. In an all-CMOS environment, the driving signals (input signals) to such interface circuits will be close to V_{CC} rail or GND. In such cases $I_{CC(T)}$ is not applicable.

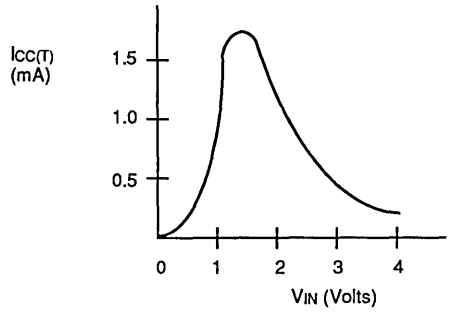


Figure 4–2. Power Supply Current vs. Input Voltage

The third component is the dynamic power supply current, $I_{CC(D)}$. This current represents the power dissipated in the device in order to charge and discharge internal node capacitances in the device as well as any external load connected to the outputs. This component is a function of operating frequency and load capacitance, and dominates the total I_{CC} at high data rates. Therefore, $I_{CC(D)}$ is discussed in further detail in the following sections.

Back to Basics

Consider a simple buffer gate. Figure 4–3 shows the lumped equivalent capacitance of the circuit internal to the device. This capacitance C_i is charged rail-to-rail at frequency f. When the gate has load C_L at the output as shown in Figure 4–4, this load is also charged rail-to-rail.

Basic theory leads us to the equation $P = f\,CV_{CC2}$ where P is the dynamic power dissipation in the gate. Since $P = IV_{CC}$ where I is the average current in the V_{CC} line, we get:

$$I = f\,CV_{CC} \text{ ---------- (1)}$$

Equation (1) shows that there is a linear relationship between I and frequency. By obtaining values of I for different values of f, one can derive a normalized expression for current I per MHz. For the unloaded case, this equation is:

$$I_{CC(D)} = C_i\,V_{CC}\,\mu A/MHz/bit \text{ ----- (2)}$$

where V_{CC} is in volts and C_i is in pF. Equation (2) enables us to obtain the value of C_i per bit if $I_{CC(D)} = 200\ \mu A/MHz/bit$ at $V_{CC} = 5$ V, then:

$$C_i = 200/5 = 40\ pF/bit$$

If the output has a load C_L, it is effectively added to C_i, and $I_{CC(D)}$ will be higher as a result (see equation 2). If C_i is estimated, $I_{CC(D)}$ for a loaded case can be computed by using the formula:

$$I_{CC(D)} @ C_L = I_{CC(D)} \quad \frac{C_L + C_i}{C_i}$$

For the example just given,

$$I_{CC(D)} @ 50\ pF = 400 \quad \frac{50 + 80}{80} = 650\ \mu A/MHz/bit$$

$$I_{CC(D)} @ 300\ pF = 200 \quad \frac{300 + 80}{80} = 1.9\ mA/MHz/bit$$

To get a good feel for the numbers, consider a 10–bit buffer, with a 300 pF load on each output, running at an "average" 5 MHz rate. The dynamic I_{CC} component will be:

$I_{CC(D)}$ = 10 bits x 1.9 mA/bit x 5 MHz = 95 mA

The term "average" rate used in the example above needs some explanation. Since the dynamic I_{CC} is attributed to signal transitions, its value is highest when all outputs have a 1010... pattern at the data rate. However, such a pattern on a continuous basis is not realistic because it does not contain any information, except, of course, in a clock driver application. Therefore, to obtain a "realistic" worst-case $I_{CC(D)}$, one needs to estimate an average rate based on expected number of transitions. This average rate is lower than the data rate.

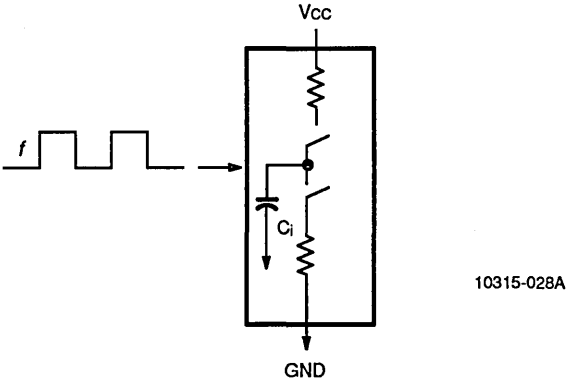


Figure 4–3. Lumped Equivalent Circuit Capacitance

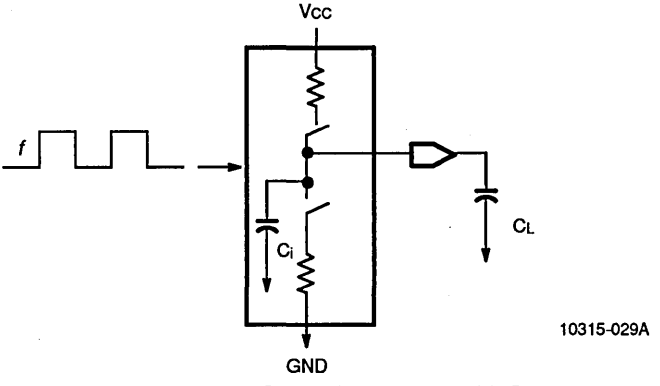


Figure 4–4. Lumped Equivalent Circuit Capacitance with Output Load

Total Power Supply Current (An Example)

For any given condition, the total I_{CC} is given by:

$$I_{CC\,(TOTAL)} = I_{CC(Q)} + I_{CC(T)} + I_{CC(D)}$$

Consider the following specification for the 10-bit buffer used in the last example:

$I_{CC(Q)}$ = 150 µA

$I_{CC(T)}$ – Data Inputs = 1.5 mA/input @ 3.4 V

– Control Inputs = 3.0 mA/input @ 3.4 V

$I_{CC(D)}$ – Unloaded = 0.2 mA/MHz/bit

To find the total I_{CC} at a data rate of 10 MHz (50% duty cycle) when all outputs have 50 pF load:

1. $I_{CC(Q)}$ = 0.15 mA

2. $I_{CC(T)}$ = 10 bits x 1.5 mA per bit x 0.5 = 7.5 mA*

* Control inputs (such as $\overline{OE}$) are assumed to be at logic LOW; therefore their contribution to $I_{CC(T)}$ is ignored.

3. $I_{CC(D)}$ @ 50 pF = 0.2 $\frac{50 + 40}{40}$ = 0.45 mA/MHz
(see example shown earlier)

Therefore:
$I_{CC(D)}$ for the device = 10 bits x 0.45 per bit x 10 MHz = 45 mA

Total I_{CC} = 0.15 + 7.5 + 45 = 52.65 mA

Summary

A system designer needs to consider all components of power supply current, and calculate the total I_{CC} based on the frequency of operation and loading. This is particularly important if CMOS parallel interface devices are used in high-speed bus applications.

TYPICAL ICCD vs. FREQUENCY PLOTS

For CMOS devices, I_{CC} is dependent upon the frequency of operation. The graphs in Figures 4–5 and 4–6 show the increase in dynamic I_{CC} as frequency increased. These graphs represent typical performance over the V_{CC} and temperature operating ranges and are not included in production testing.

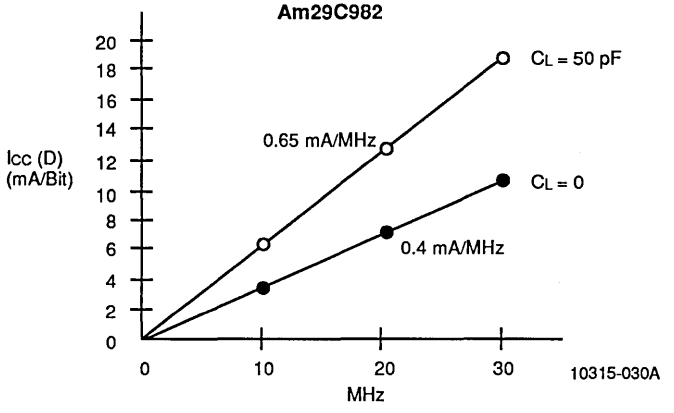


Figure 4–5. The Am29C982 Dynamic Power Supply Current vs. Frequency

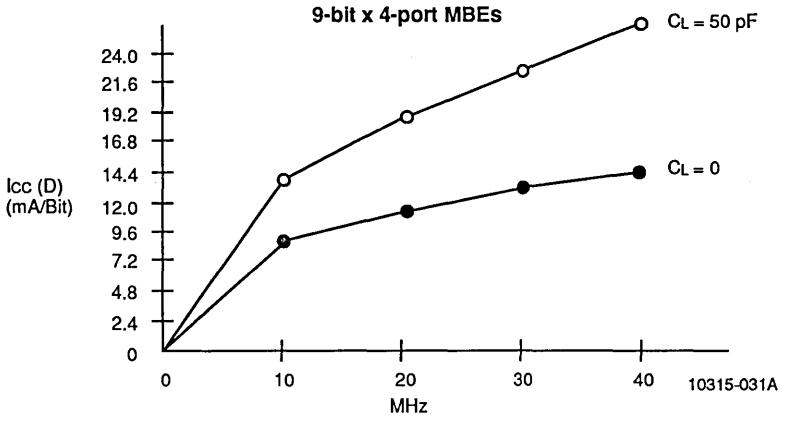


Figure 4–6. Am29C983, 983A, 985 Dynamic Power Supply Current vs. Frequency

POWER-UP/DOWN DISABLE

The Multiple Bus Exchange devices contain a unique power-up/down circuit to provide glitch-free outputs during power-supply sequencing. This power-up circuitry ensures that at low V_{CC} values (typically 0-2.0 V), the outputs are disabled and in 3-state. At V_{CC} values above this threshold, the outputs will remain disabled until the appropriate output-enable inputs are conditioned active (outputs enabled), at which time the output will respond to the steady-state input value. Additionally, the outputs will exhibit high-impedance characteristics under power-off conditions.

This power-up/down circuitry is a distinctive design feature of the Multiple Bus Exchange devices. This is particularly useful in card-edge applications.

The threshold values stated above are typical and are not tested as a part of the production process. The presence of this feature is verified during product characterization.

INPUT/OUTPUT STRUCTURES

Typical CMOS devices on the market today have absolute maximum dc I/O voltage ratings that prevent some card-edge applications, due to the uncertainty of the I/O voltage with respect to V_{CC}. This uncertainty occurs when extracting or replacing a card to a powered-on connector or when a powered-off device is sitting on an active bus. Under these conditions, the maximum rating of –0.5 V to V_{CC} +0.5 V may be violated. This rating is derived from the presence of a parasitic diode from the input or output to V_{CC}. To prevent forward biasing the diode with an active signal, the 0.5 V limit above V_{CC} was adopted.

The MBEs have input and output structures for addressing these concerns (Figures 4–7 and 4–8). In both cases, the diode to V_{CC} has been eliminated. This was accomplished in the output with the use of an n-channel pull-up transistor, as opposed to a p-channel device contained in a typical CMOS output. An ESD structure in the input circuit eliminated the input diodes by using active 3-terminal devices, i.e. lateral bipolar and thick-oxide field effect-transistors, to give protection to V_{CC}. The end result is that the maximum dc I/O voltage ratings become –0.5 v to +7.0 V. The structures can tolerate active signals on a powered-down device, thus eliminating the two problem scenarios described above.

The output n-channel pull-up has another effect. A lightly loaded output will no longer swing rail-to-rail. A typical low load swing is approximately +0.1 v to +4.0 V (V_{CC} = +5.0 V), approximately a 20% reduction over a comparable p-channel output structure. This is beneficial for designs sensitive to switching noise and cross-talk associated with typical CMOS rail-to-rail travel.

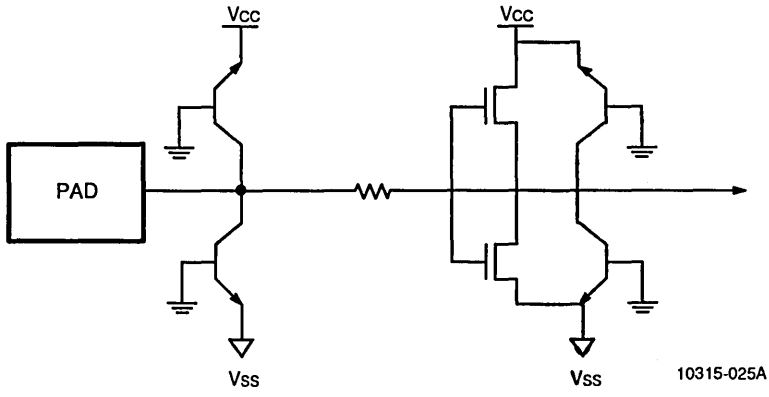


Figure 4–7. Equivalent MBE Input with ESD Structure

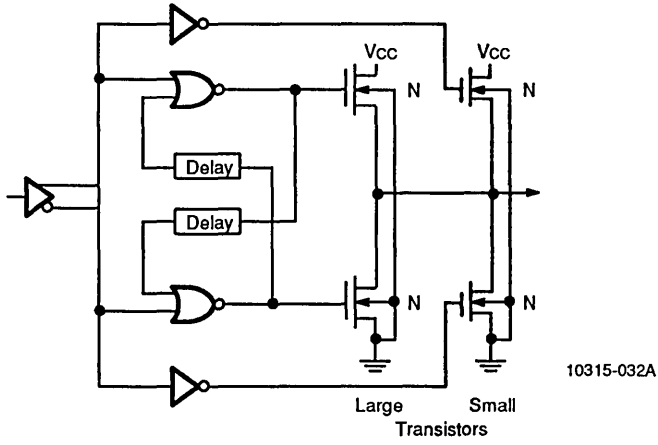


Figure 4–8. Equivalent MBE Output Structure

CHAPTER 5
Product Specifications

Am29C982

4-Bit x 4-Port Multiple Bus Exchange

Advanced Micro Devices

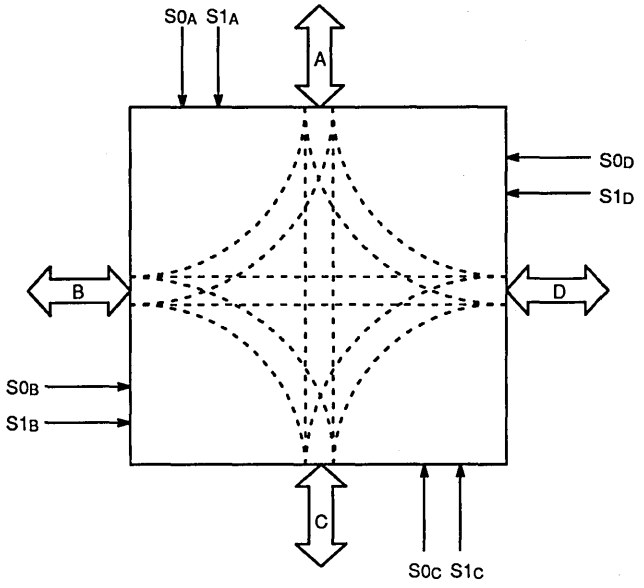
DISTINCTIVE CHARACTERISTICS

- **Four bidirectional I/O ports**
  - Replaces several LS245-type devices
  - TTL Compatibility
  - Permits multiple bus communication
- **Two selection inputs per port**
  - Port-independent interconnect control
- **Matched port decoding**
  - Increased flexibility
  - Simplifies external decode logic
  - Easily cascadable for wider buses
- **Outputs glitch-free during power-up/down**
  - No power-up sequencing needed
  - Ideal for card-edge interface
- **48 mA output drive**
  - High-capacitance bus driving
- **High-performance CMOS**
  - Low power consumption
  - 7 ns (typ.) port-to-port delay
  - 9 ns (typ.) select-to-port delay
- **Available in 400 mil, 28-pin DIP and 28-pin LCC and PLCC packages**

GENERAL DESCRIPTION

The Am29C982 is a high-speed Multiple Bus Exchange device. It is organized as four 4-bit bidirectional I/O ports. Each port can be used either as a source or a destination under independent control to implement a digital cross-point switch. This organization adds data routing flexibility and is ideally suited for multiple bus communication in a multiprocessing environment.

SIMPLIFIED BLOCK DIAGRAM



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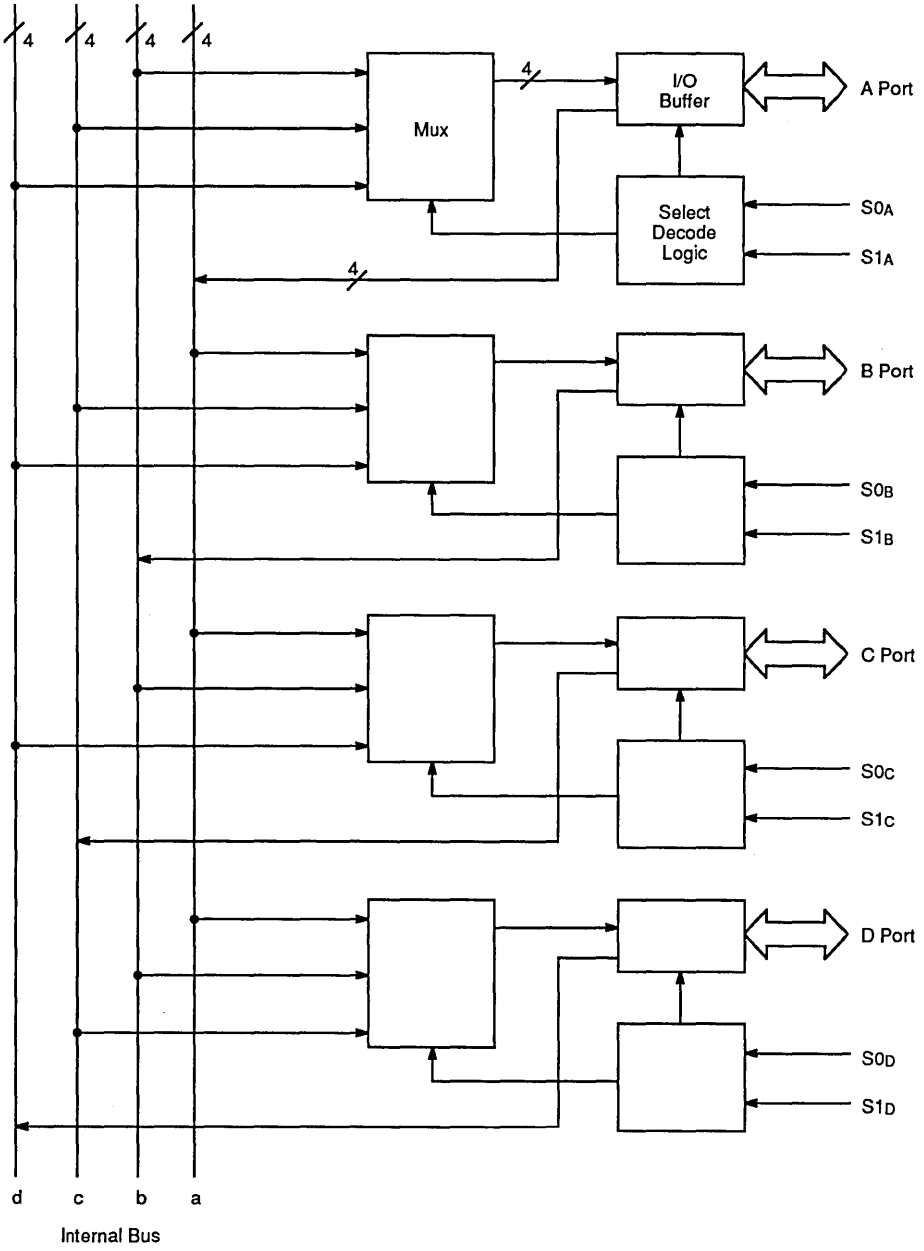
DETAILED BLOCK DIAGRAM



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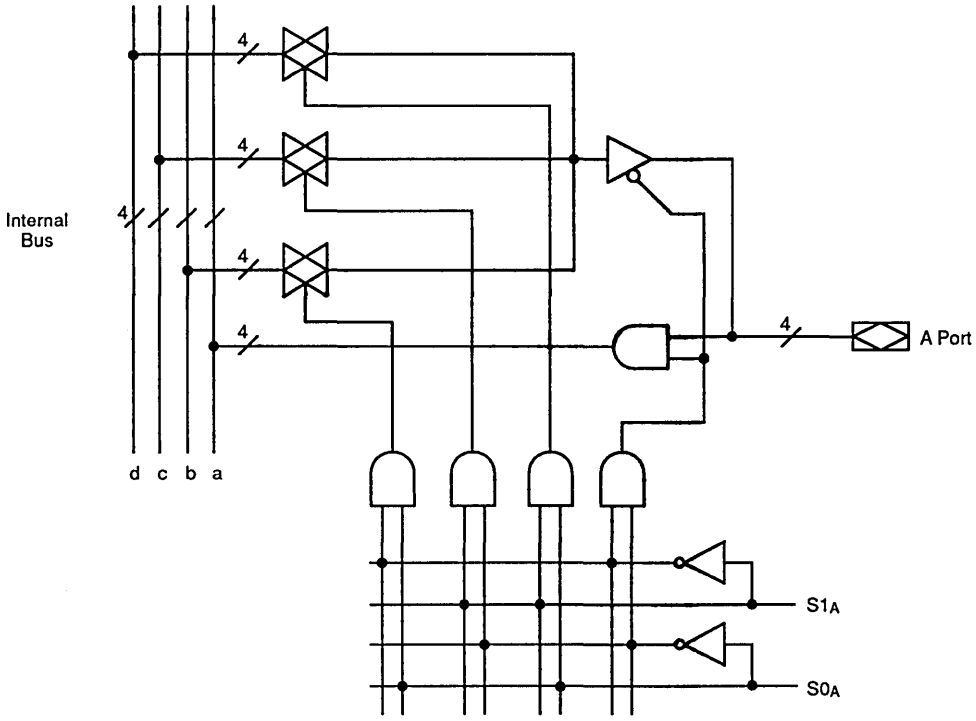
PORT A — DETAILED DIAGRAM



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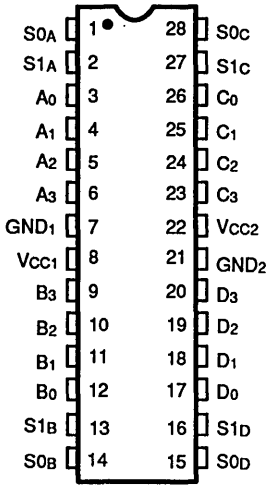
CONNECTION DIAGRAMS
Top View

DIP



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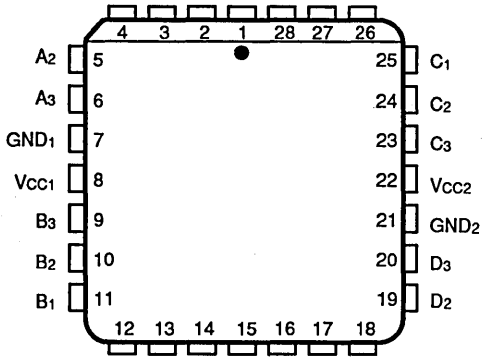
LCC*



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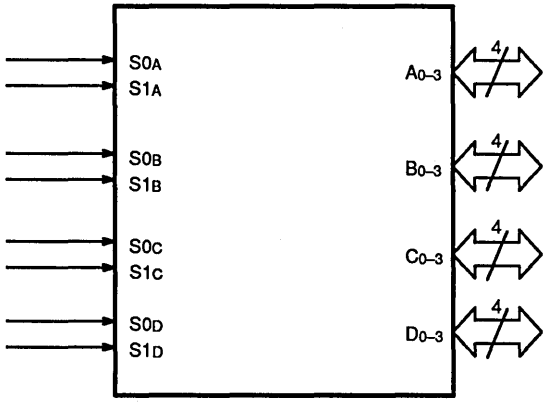
Notes:
Pin 1 is marked for orientation.
*Also available in 28-Pin PLCC; pinout is identical to LCC.

LOGIC SYMBOL



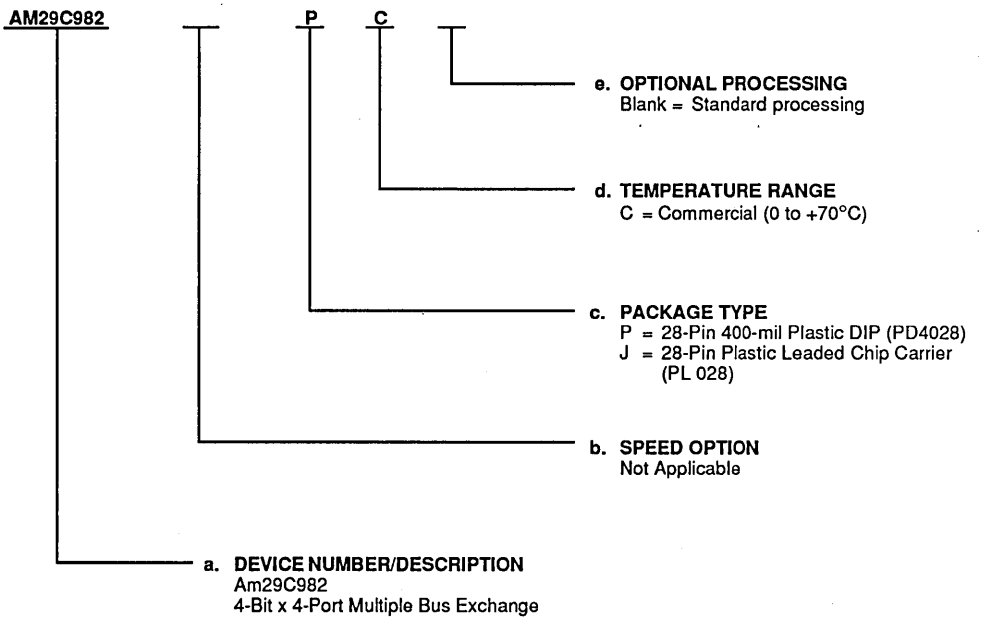
VCC = Power Supply (2)
GND = Ground (2)

09484-006A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C982	PC, JC

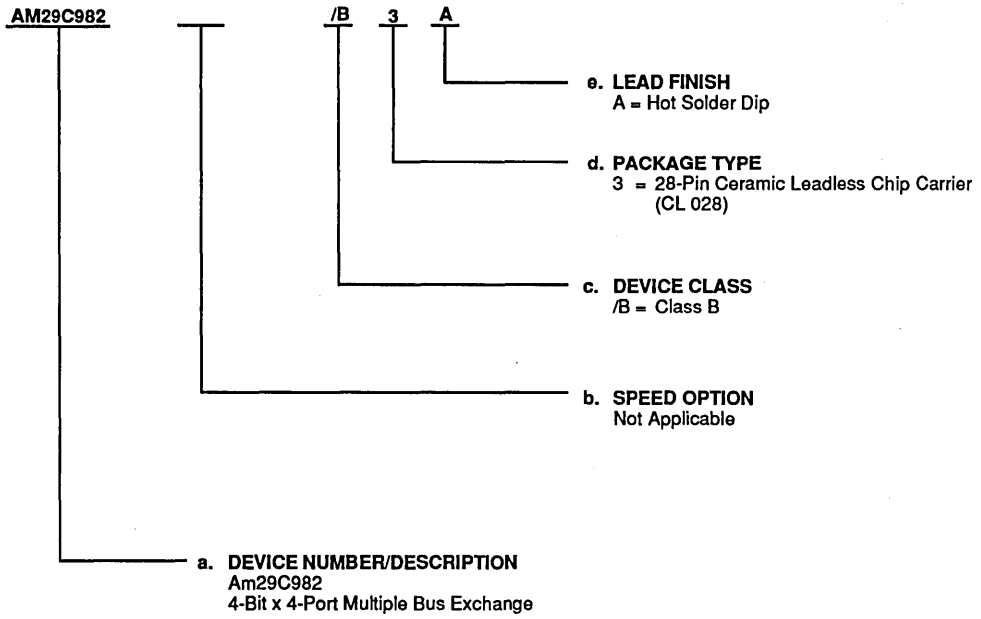
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C982	/B3A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_i, B_i, C_i, & D_i (i = 0-3)

Data Bus I/O Ports (Input/Output)

These four groups of four I/O pins are defined as A, B, C, and D ports respectively. Each port serves as a source (input) or a destination (output). When selected as a source, the output drivers of the port are in the high-impedance state.

Si_A, Si_B, Si_C, & Si_D (i = 0, 1)

Port Select (Inputs)

Each pair of inputs determines the status of its corresponding I/O port as a source (input) or a destination (output). When selected as a destination, the selection inputs determine which port is the source of data.

FUNCTIONAL DESCRIPTION

The Am29C982 Multiple Bus Exchange consists of four 4-bit I/O ports. Each I/O port can either be a source (input) port, or a destination (output) port that accepts data from any one of the three other ports. When the port is an input, its output drivers are in the high-impedance state. The ports that are not intended to be destination ports should be selected as source ports to disable the port.

Independent selection inputs for each port offer flexibility in data routing. Data from one input port can be routed to one or more of the other ports. Two independent channels can also be established by specifying any two ports as sources, and any combination of the other two as destinations.

FUNCTION TABLE

$S1_A$	$S0_A$	A Port Status
L	L	Source
L	H	Destination (B → A)
H	L	Destination (C → A)
H	H	Destination (D → A)
$S1_B$	**$S0_B$**	**B Port Status**
L	L	Destination (A → B)
L	H	Source
H	L	Destination (C → B)
H	H	Destination (D → B)
$S1_C$	**$S0_C$**	**C Port Status**
L	L	Destination (A → C)
L	H	Destination (B → C)
H	L	Source
H	H	Destination (D → C)
$S1_D$	**$S0_D$**	**D Port Status**
L	L	Destination (A → D)
L	H	Destination (B → D)
H	L	Destination (C → D)
H	H	Source

Key:

L = Low

H = High

Destination = Output

Source = Input

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	−0.5 to 7.0 V
DC Input Diode Current	
(I_{IK}) (V_{IN} < 0 V)	−20 mA
(V_{IN} > V_{CC} if applicable)	+20 mA
DC Input Voltage (V_{IN})	−0.5 V to +7.0 V
DC Output Diode Current	
(I_{OK}) (V_{OUT} < 0 V)	−50 mA
(V_{OUT} > V_{CC} if applicable)	+50 mA
DC Output Current Per Output Pin	
I_{SINK}	+70 mA
I_{SOURCE}	−30 mA
DC Output Voltage (V_{OUT})	−0.5 to +7.0 V
Total DC Ground Current (I_{GND})	600 mA
Total DC V_{CC} Current (I_{CC})	220 mA
Storage Temperature	−65 to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to 70°C
Supply Voltage (V_{CC})	4.5 V to 5.5 V

Military (M) Devices

Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OH} = −15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input CLAMP Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} 5.5 V, V_{IN} = 0 V			−10	µA
	(Select Inputs)	V_{CC} 5.5 V, V_{IN} = 0.4 V			−5	µA
I_{IH}	Input HIGH Current	V_{CC} 5.5 V, V_{IN} = 2.7 V			5	µA
	(Select Inputs)	V_{CC} 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current	V_{CC} = 5.5 V, V_{OUT} = 0.4 V			−15	µA
	(I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			−20	µA
I_{OZH}	Off-State Leakage Current	V_{CC} = 5.5 V, V_{OUT} = 2.7 V			15	µA
	(I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−60		mA
$I_{CC(Q)}$	Quiescent Power Supply	V_{CC} = 5.5 V, V_{IN} = 5.5 V or	MIL		1.5	mA
	(Note 4)	GND Outputs Open	COM'L		1.2	mA

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
$I_{CC}(T)$	Power Supply Current TTL	V_{CC} = 5.5 V, V_{IN} = 3.4 V	MIL		1.5	mA/ Input
	Input HIGH (Note 4)	Other Inputs at V_{CC} or GND	COM'L		1.3	
$I_{CC}(D)$ (Note 5)	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)			400	µA/ MHz/Bit

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 milliseconds.
3. Measured at a frequency of <10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC}:

$$I_{CC} = I_{CC}(Q) + I_{CC}(T) \times M_T \times D_H + I_{CC}(D) \times ((C_L + 72) + 72) \times f \times N$$

Where C_L = Load Capacitance in pF per output
f = Frequency in MHz
N = Average number of outputs switching
M_T = Number of inputs at logic HIGH
D_H = Duty cycle for each input HIGH

5. Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
1	t_{PLH}	Propagation Delay Data	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		14		16	ns
2	t_{PHL}	Input to Data Output			14		16	ns
3	t_{PLH}	Propagation Delay Select			15		17	ns
4	t_{PHL}	Input to Data Output			15		17	ns
5	t_{PZH}	Output Enable Time Select			15		17	ns
6	t_{PZL}	Input to Data Output			15		17	ns
7	t_{PHZ}	Output Disable Time Select			14		16	ns
8	t_{PLZ}	Input to Data Output			14		16	ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

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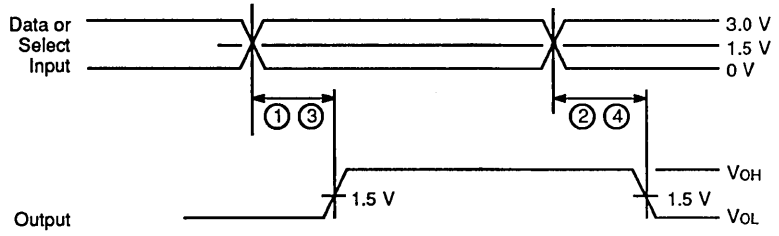
SWITCHING TEST WAVEFORMS



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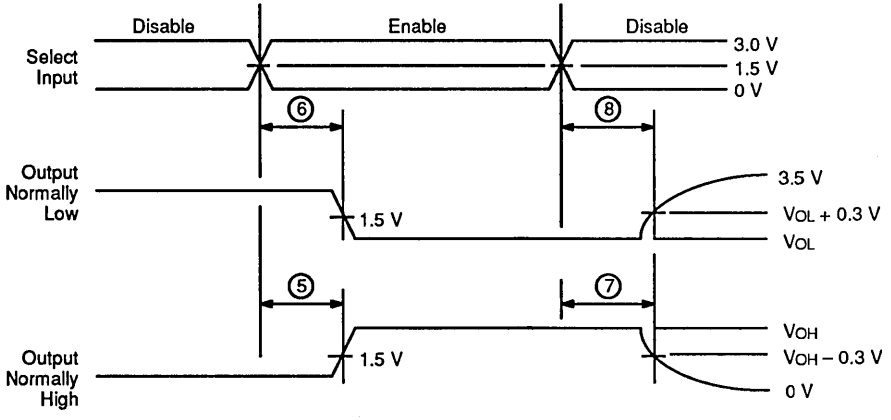
Propagation Delay



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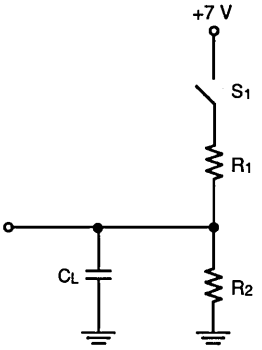
Enable and Disable Times

SWITCHING TEST CIRCUIT



S_1 = Open Normally
S_1 = Closed for t_{PZL} and t_{PLZ}

09485-007A

Am29C983/Am29C983A

9-Bit x 4-Port Multiple Bus Exchange

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Four bidirectional I/O ports with latches**
  - Replaces several bidirectional latches and transceivers
  - Permits multiple bus communication
  - Allows two independent communication channels
  - TTL compatibility
- **9 bit-wide ports to handle byte parity**
- **Two selection inputs per port**
  - Independent port interconnect control
  - Increased flexibility in data routing
- **Matched port decoding**
  - Simplifies external decode logic
  - Easily cascadable for wider buses
- **Latches for incoming and outgoing data**
  - Independent controls permit selective data capture
  - Ideal for stored operation
  - Readback feature for system diagnostics
- **Glitch-free outputs during power-up/down**
  - No power-up sequencing needed
  - Ideal for card-edge interface
- **48 mA output drive**
  - High-capacitance bus driving
- **High-performance CMOS**
  - Low stand-by power consumption
- **Two speeds available**
  Am29C983
  - 9 ns (typ) port-to-port delay
  - 10 ns (typ) select-to-port delay
  Am29C983A
  - 6 ns (typ) port-to-port delay
  - 7 ns (typ) select-to-port delay
- **Available in 68-pin PLCC package**
  - Significant savings in board space

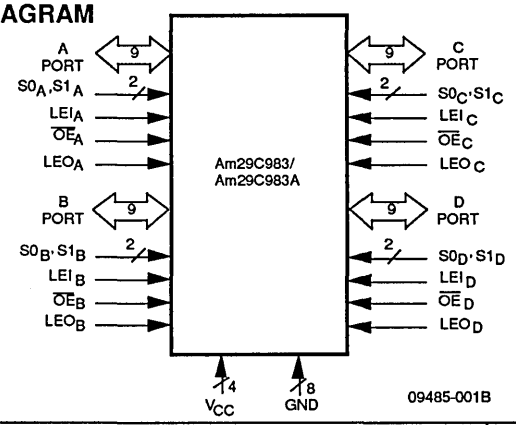
GENERAL DESCRIPTION

The Am29C983/A is a high-speed Multiple Bus Exchange device. It is organized as four 9-bit wide TTL-compatible I/O ports with Output Enable control for each port. Any port can serve either as a source (Input) port or as a destination (Output) port. When the output drivers of a port are disabled (high-impedance state), the port serves as a source port. When the drivers are enabled, the port serves as a destination port. Source port selection is made by two independent Select inputs at each port. This organization offers flexibility in implementing the Am29C983/A as a digital cross-point switch for multiple bus communication in a multiprocessing environment.

Each I/O port has an input latch to capture incoming data and an output latch to capture outgoing data. All input and output latches are independently controlled by active-HIGH Latch Enable inputs. This feature can be used to perform stored operation for byte-word compression and expansion to communicate between buses of different widths.

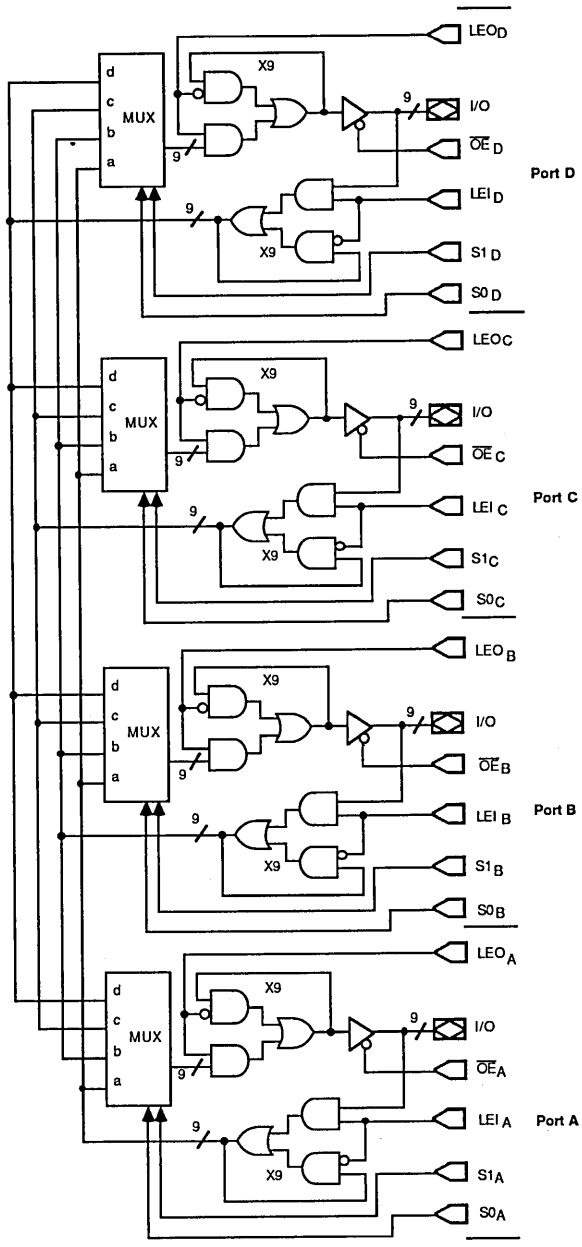
Independent port control permits cascading of Am29C983/As for wider buses. All I/O ports go into high-impedance state upon power-down. This feature makes the device ideally suited for card-edge applications.

SIMPLIFIED BLOCK DIAGRAM



Publication# 09485 Rev. D Amendment /0
Issue Date: October 1990

DETAILED BLOCK DIAGRAM



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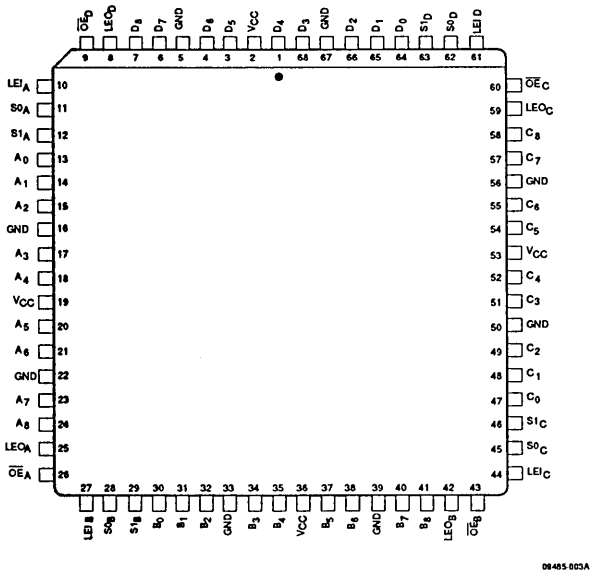
CONNECTION DIAGRAM
PLCC
(Top View)



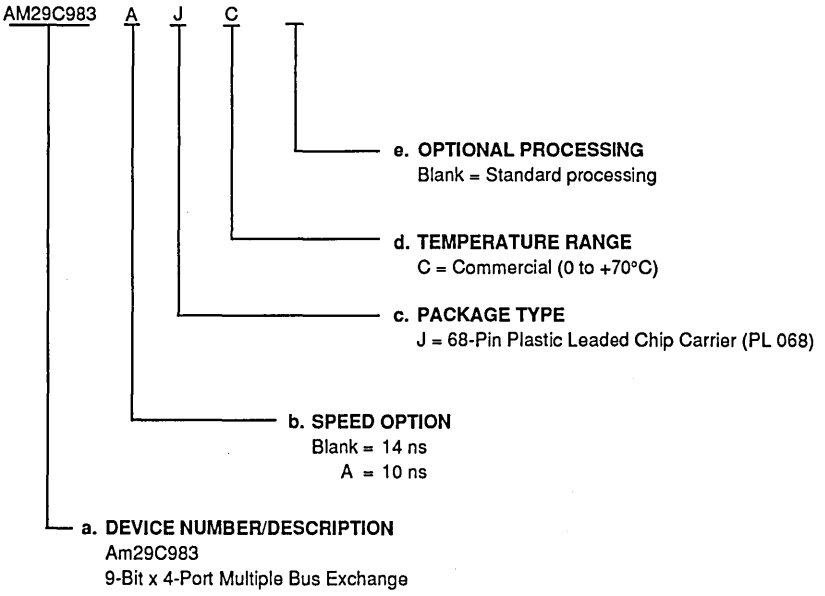
Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM29C983	JC
AM29C983A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A_I, B_I, C_I, AND D_I (I = 0 THROUGH 8)
DATA BUS I/O PORTS (INPUT/OUTPUT)

These four groups of nine I/O pins are defined as the A, B, C, and D ports respectively. Each port serves as a source (Input) or as a destination (Output).

SI_A, SI_B, SI_C, AND SI_D (I = 0, 1)
SOURCE PORT SELECT (INPUTS)

Each pair of inputs determines the source of data for the corresponding I/O port when used as a destination port.

LEI_A, LEI_B, LEI_C, AND LEI_D
INPUT LATCH ENABLE (INPUTS; ACTIVE HIGH)

Each LEI input controls a 9-bit wide latch on the input side of the corresponding I/O port. The latches are transparent when LEI is HIGH and are latched when LEI is LOW.

LEO_A, LEO_B, LEO_C, AND LEO_D
OUTPUT LATCH ENABLE (INPUTS; ACTIVE HIGH)

Each LEO input controls a 9-bit wide latch on the output side of the corresponding I/O port. The latches are transparent when LEO is HIGH and are latched when LEO is LOW.

$\overline{OE}_A$, $\overline{OE}_B$, $\overline{OE}_C$, AND $\overline{OE}_D$
OUTPUT ENABLE (INPUTS; ACTIVE LOW)

Each $\overline{OE}$ input controls the bus drivers of the corresponding I/O port. When $\overline{OE}$ is LOW, data at the output of the Output latches is passed to the bus. When $\overline{OE}$ is HIGH, the bus outputs are in high-impedance state.

FUNCTIONAL DESCRIPTION

The Am29C983/A Multiple Bus Exchange consists of four 9-bit I/O ports. Each port has a 9-bit Input latch to capture incoming data and a 9-bit Output latch to capture outgoing data. There are five control inputs associated with each port: two Select inputs for source port selection, two Latch Enable inputs (active HIGH) to control Input and Output latches, and an active LOW Output Enable line to control the bus driver at the I/O port.

Port Selection and Control

Each port is independently controlled by means of these five control inputs. If the output drivers of a port are disabled (high-impedance state), that port is an input and can be used as a source port. Incoming data can be captured in the Input latch. At the same time, the data at one of the four internal buses can be transferred to the Output latch under the control of the appropriate Select inputs. If the output drivers are enabled, the port serves as a destination port, transporting the data at the output of its Output latch to the external bus connected to the I/O port. Independent control of Input and Output latches and output drivers permits stored operation at any port.

Multiple Bus Communication

Four internal buses serve as pathways for port-to-port connection. By proper choice of source select codes for the ports, the Am29C983 can be configured in different modes for multiple bus communication. In one mode of operation, two ports can be selected as source ports and the other two as destination ports; thus, two independent bidirectional communication channels are established. In another mode, one port can be selected as the source, and one or more of the other ports can serve as destination ports. Any port not intended as a destination port can be disabled (high-impedance state) by means of its Output Enable control.

Input and Output Latches

The presence of Input and Output latches offers significant flexibility in using the Am29C983. Any port can be chosen as the source port to store incoming data in its Input latch. This can then be connected to one or more destination ports. The outgoing data can be further stored in the Output latches for later use; thus there are two stages of data storage between any two ports. This feature can be used in simple store and forward applications, as well as in more sophisticated applications for byte-word compression and expansion. Moreover, the data stored in the Input latch of a port can be "read back" to the same port by choosing it as the destination (its Output latch is transparent). This feature can be used for diagnostics in multiple bus communication.

TRUTH TABLES

A. Port Source Selection

$S1_n$	$S0_n$	Source
L	L	A Bus
L	H	B Bus
H	L	C Bus
H	H	D Bus

B. Latch Operation

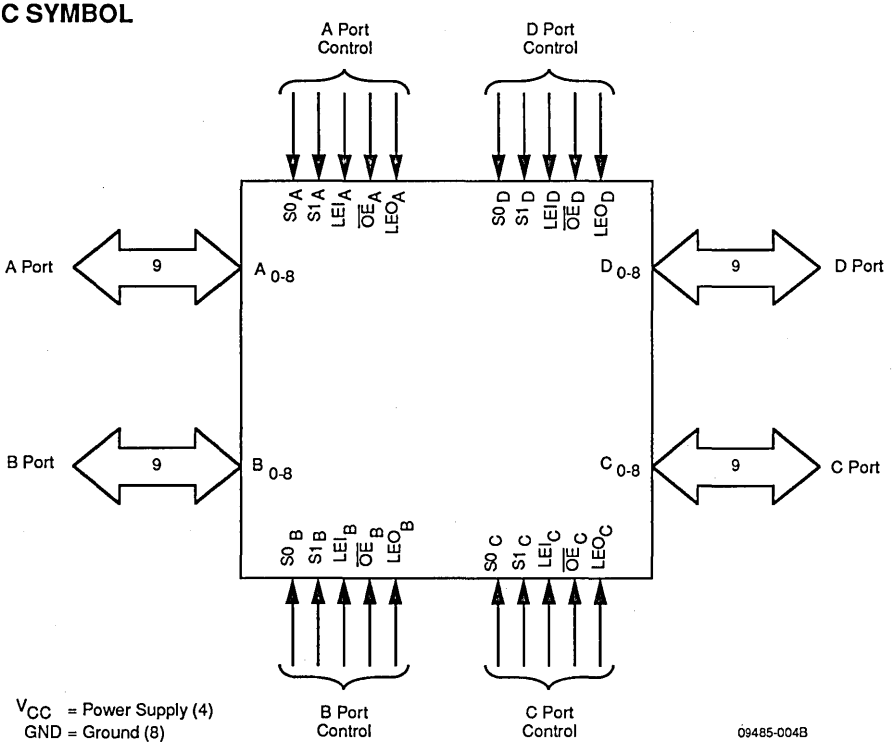
LEI_n or LEO_n	Mode
H	Transparent
L	Latched

C. I/O Port Controls

LEO_n	$\overline{OE}_n$	I/O	Source of Data
L	L	Out	Contents of Output Latch
H	L	Out	Selected Source Port
X	H	In	

Key: n = A, B, C, or D
L = LOW
H = HIGH
X = Don't Care

LOGIC SYMBOL



V_{CC} = Power Supply (4)
GND = Ground (8)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	−0.5 to 7.0 V
DC Input Diode Current	
(I_{IK}) (V_{IN} < 0 V)	−20 mA
(V_{IN} > V_{CC} if applicable)	+20 mA
DC Input Voltage (V_{IN})	−0.5 to V_{CC} +0.5 V
DC Output Diode Current	
(I_{OK}) (V_{OUT} < 0 V)	−50 mA
(V_{OUT} > V_{CC} if applicable)	+50 mA
DC Output Current per Output Pin:	
I_{SINK}	+70 mA
I_{SOURCE}	−30 mA
DC Output Voltage (V_{OUT})	−0.5 to 0.7 V
Total DC Ground Current (I_{GND})	1750 mA
Total DC V_{CC} Current (I_{CC})	575 mA
Storage Temperature	−65 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

AM29C983

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OH} = −15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 0 V			−10	µA
I_{IH}	Input HIGH Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			−20	µA
I_{OZH}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−60		mA
I_{CCQ}	Quiescent Power Supply Current (Note 4)	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND Outputs Open			1.5	mA

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter DescriptionTest Conditions		Min.	Max.	Unit
I_{CCT}	Power Supply Current TTL Input HIGH (Note 4)	V_{CC} = 5.5 V, V_{IN} = 2.4 V Other Inputs at V_{CC} or GND		3.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)		500	µA/ MHz/Bit

AM29C983A

Parameter Symbol	ParameterDescription	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OH} = –15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = –18 mA			–1.2	V
I_{IL}	Input LOW Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 0 V			–10	µA
I_{IH}	Input HIGH Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			–20	µA
I_{OZH}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		–60		mA
I_{CCQ}	Quiescent Power Supply Current (Note 4)	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND Outputs Open			1.5	mA
I_{CCT}	Power Supply Current TTL Input HIGH (Note 4)	V_{CC} = 5.5 V, V_{IN} = 2.4 V Other Inputs at V_{CC} or GND			3.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)			500	µA/ MHz/Bit

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 milliseconds.
3. Measured at a frequency of < 10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC}: $I_{CC} = I_{CCQ} + I_{CCT} \times M_T \times D_H + I_{CCD} \times ((C_L + 91) + 91) \times f \times N$

   Where C_L = Load Capacitance in pF per output
   f = Frequency in MHz
   N = Average number of outputs switching
   M_T = Number of inputs at logic HIGH
   D_H = Duty cycle for each input HIGH

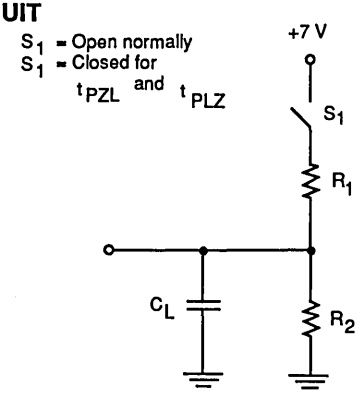
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AM29C983						
No.	**Parameter Symbol**	**Parameter Description**	**Test Conditions**	**Min**	**Max**	**Unit**
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	1.5	14	ns
2	t_{PHL}	LEI = HIGH, LEO = HIGH		1.5	14	ns
3	t_{PLH}	Propagation Delay Select Input to Port LEO = HIGH		1.5	18	ns
4	t_{PHL}			1.5	18	ns
5	t_{PLH}	Propagation Delay LEI to Port		1.5	18	ns
6	t_{PHL}	LEO = HIGH		1.5	18	ns
7	t_{PLH}	Propagation Delay		1.5	14	ns
8	t_{PHL}	LEO to Port		1.5	14	ns
9	t_{PZH}	Output Enable Time		1	14	ns
10	t_{PZL}	$\overline{OE}$ to Port		1	14	ns
11	t_{PHZ}	Output Disable Time		0	12	ns
12	t_{PLZ}	$\overline{OE}$ to Port		0	12	ns
13	t_s	Port to LEI Setup		2		ns
14	t_h	Port to LEI Hold		3		ns
15	t_s	Port to LEO Setup		4.5		ns
16	t_h	Port to LEO Hold		1.5		ns
17	t_s	Select to LEO Setup		6		ns
18	t_h	Select to LEO Hold		0		ns
19	t_s	LEI to LEO Setup		6		ns
20	t_h	LEI to LEO Hold		0		ns
21	t_{PWH}	LEI, LEO Pulse Width HIGH		6		ns

SWITCHING CHARACTERISTICS (Continued)

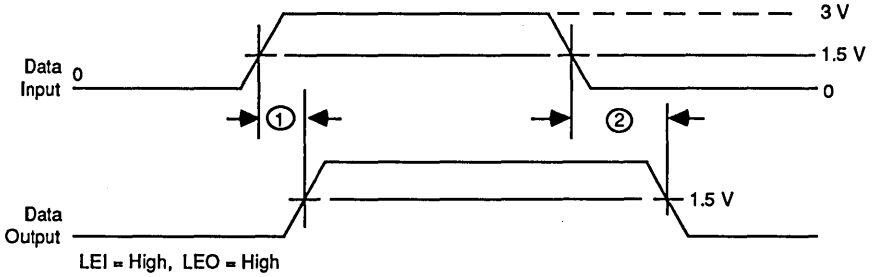
AM29C983A						
No.	**Parameter Symbol**	**Parameter Description**	**Test Conditions**	**Min**	**Max**	**Unit**
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	1.5	10	ns
2	t_{PHL}	LEI = HIGH, LEO = HIGH		1.5	10	ns
3	t_{PLH}	Propagation Delay Select Input to Port LEO = HIGH		1.5	11	ns
4	t_{PHL}			1.5	11	ns
5	t_{PLH}	Propagation Delay LEI to Port LEO = HIGH		1.5	12	ns
6	t_{PHL}			1.5	12	ns
7	t_{PLH}	Propagation Delay LEO to Port		2	10	ns
8	t_{PHL}			1.5	10	ns
9	t_{PZH}	Output Enable Time $\overline{OE}$ to Port		1	10	ns
10	t_{PZL}			1	10	ns
11	t_{PHZ}	Output Disable Time $\overline{OE}$ to Port		0	9	ns
12	t_{PLZ}			0	9	ns
13	t_s	Port to LEI Setup		2		ns
14	t_h	Port to LEI Hold		3		ns
15	t_s	Port to LEO Setup		4.5		ns
16	t_h	Port to LEO Hold		1.5		ns
17	t_s	Select to LEO Setup		6		ns
18	t_h	Select to LEO Hold		0		ns
19	t_s	LEI to LEO Setup		6		ns
20	t_h	LEI to LEO Hold		0		ns
21	t_{PWH}	LEI, LEO Pulse Width HIGH		6		ns

SWITCHING TEST CIRCUIT

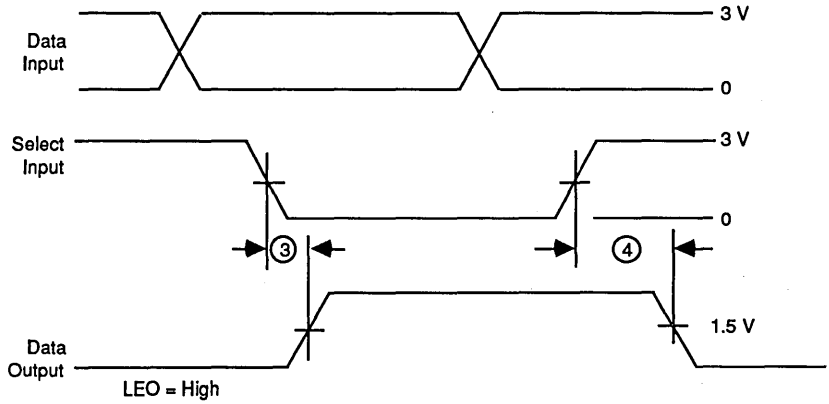


09485-007A

SWITCHING TEST WAVEFORMS



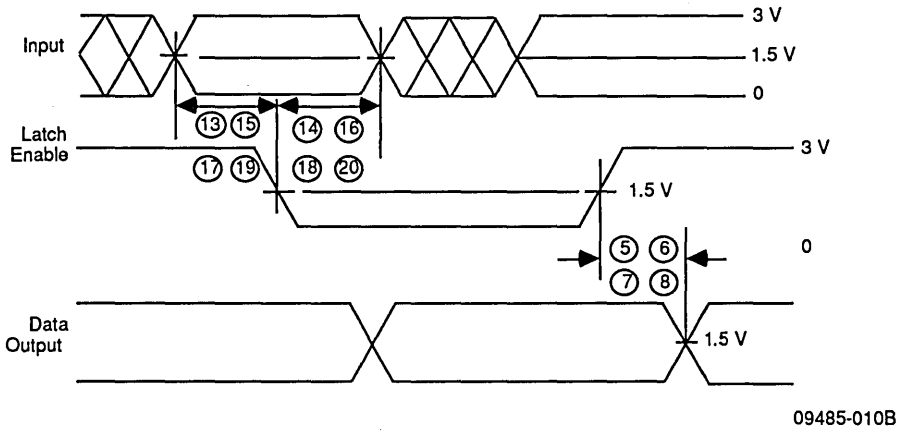
Propagation Delay—Port-to-Port 09485-008B



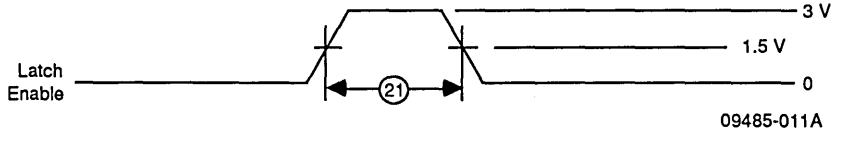
09485-009B

Propagation Delay—Select-to-Port

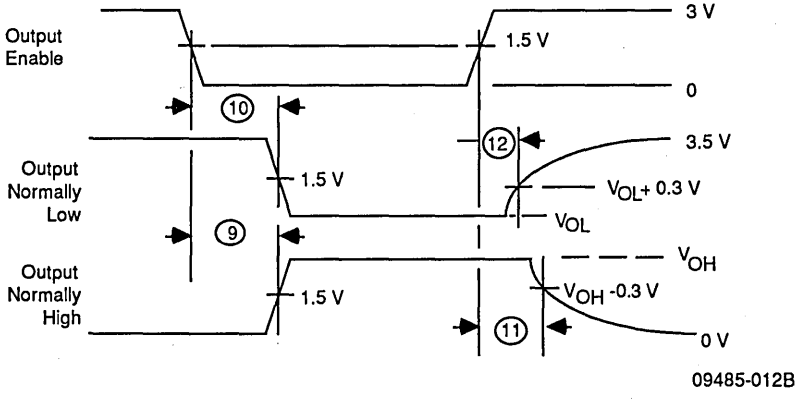
SWITCHING TEST WAVEFORMS (Continued)



Input and Output Latch Propagation Delay, Setup and Hold Times



Minimum Latch Enable Pulse Width



Enable and Disable Times

Am29C985

9-Bit x 4-Port Multiple Bus Exchange with Parity

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Four bidirectional I/O ports**
  - Replaces several bidirectional latched transceivers
  - Permits multiple bus communication
  - Allows two independent communication channels
  - TTL compatibility
- **9 bit-wide ports to handle byte parity**
- **Parity check/generate at all ports**
  - Odd parity
- **Additional output bus check**
  - Compares bus with driver inputs
- **Two selection inputs per port**
  - Independent port interconnect control
  - Increased flexibility in data routing
- **Matched port decoding**
  - Simplifies external decode logic
  - Easily cascadable for wider buses
- **Power-Up/Down disable**
  - No power-up sequencing needed
  - Ideal for card-edge interface
- **48 mA output drive**
  - High-capacitance bus driving
- **High-performance CMOS**
  - Low stand-by power consumption
  - 6 ns (typ.) port-to-port delay
  - 7 ns (typ.) select-to-port delay
- **Available in 68-pin PLCC package**
  - Significant savings in board space
- **Proprietary output circuit minmizes ground bounce**
- **3-State during power off condition**

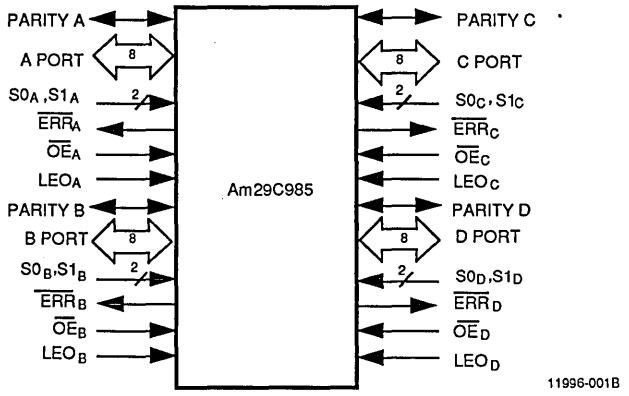
GENERAL DESCRIPTION

The Am29C985 is a high-speed Multiple Bus Exchange device. It is organized as four 9-bit wide TTL-compatible I/O ports with Output Enable control for each port. Any port can serve either as a source (Input) port or as a destination (Output) port. When the output drivers of a port are disabled (high-impedance state), the port serves as a source port. When the drivers are enabled, the port serves as a destination port. Source port selection is made by two independent Select inputs at each port. This organization offers flexibility in implementing the Am29C985 as a digital cross-point switch for multiple bus communication in a multiprocessing environment.

The Am29C985 incorporates parity check and generation capabilities on all four output ports. Each output port is capable of generating odd parity on byte-wide input data. Accordingly, parity check is accomplished at each output on incoming 9 bit parity data. A unique comparison scheme also performs a bus check by comparing the data driven onto the bus with the input data received at the internal multiplexers thus detecting stuck bus bits.

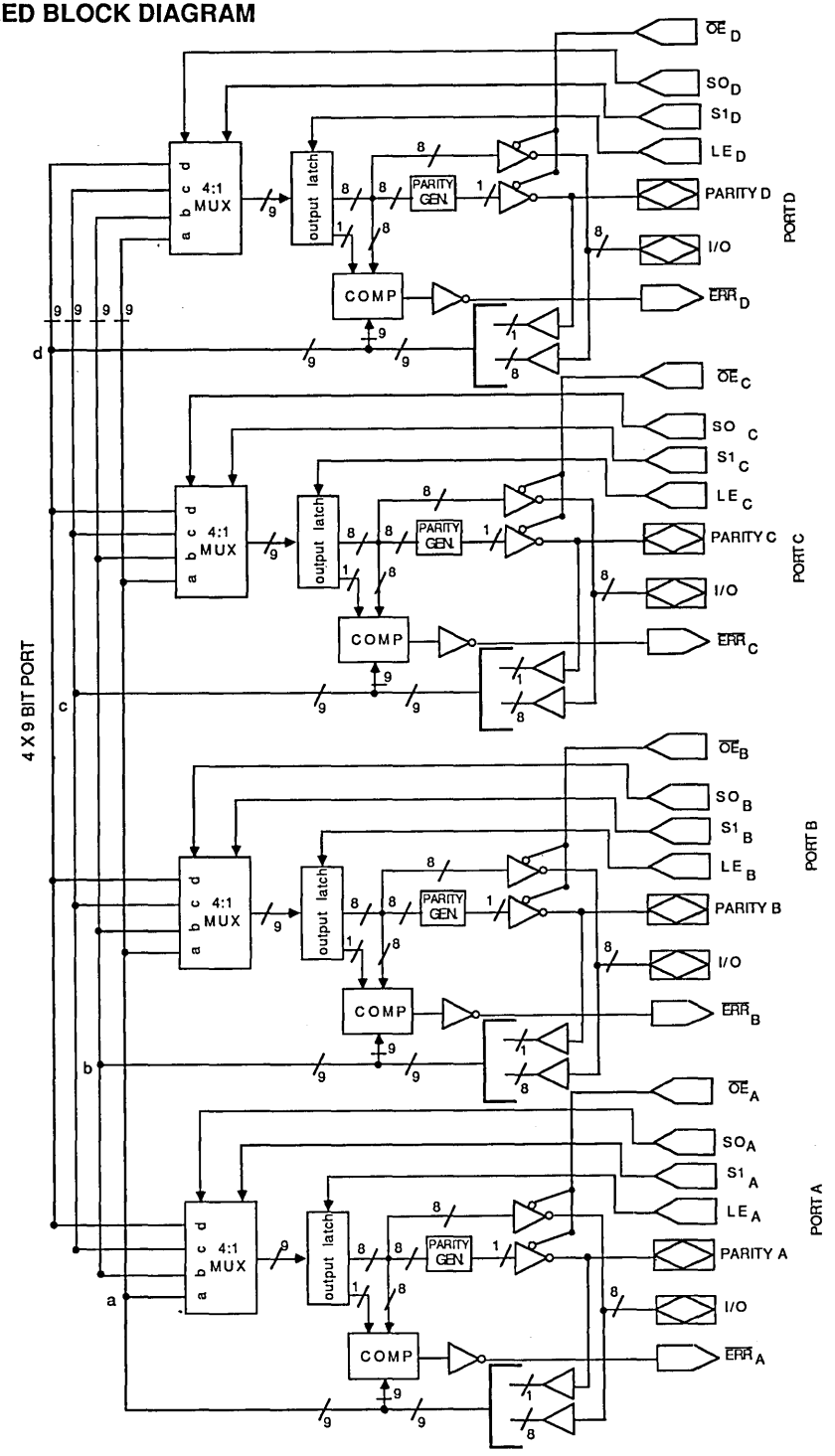
Each I/O port has an output latch to capture outgoing data. All output latches are independently controlled by active HIGH Output Latch Enable inputs. This feature can be used to perform stored operation for byte-word compression and expansion to communicate between buses of different widths. Independent port control permits cascading of Am29C985s for wide buses. All I/O ports go into high impedance state upon power down. This feature makes the device ideally suited for card-edge applications.

SIMPLIFIED BLOCK DIAGRAM



Publication # 11996 Rev. B Amendment /0
Issue Date: October 1990

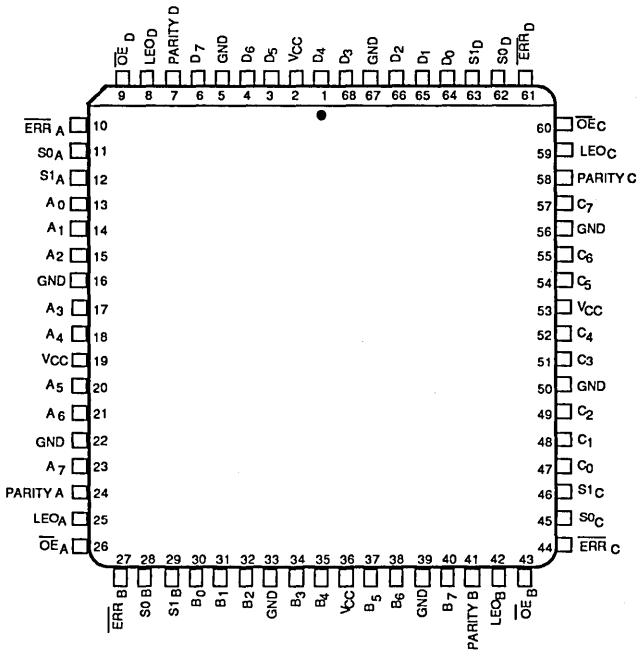
DETAILED BLOCK DIAGRAM



CONNECTION DIAGRAMS

PLCC

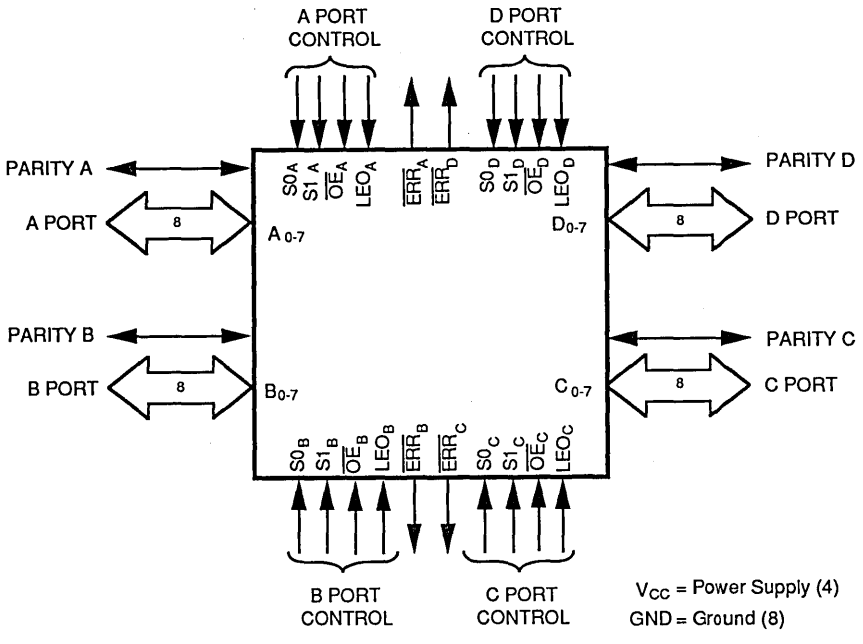
(Top View)



11996A-003A

Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL



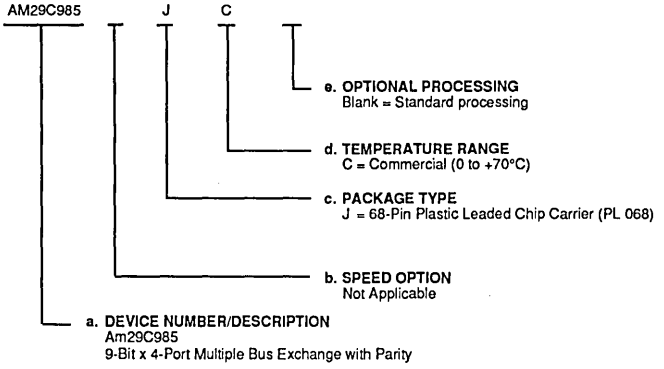
11996-005B

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM29C985	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A_I, B_I, C_I, and D_I (I = 0 through 7) Data Bus I/O Ports (Input/Output)
These four groups of eight I/O pins are defined as the A, B, C, and D ports respectively. Each port serves as a source (Input) or as a destination (Output).

PARITY A,PARITY B, PARITY C and PARITY D Parity Flag (Input/Output, Three-state)
As an input, parity and port are combined and checked for odd parity. As an output, parity is an active output indicating odd parity for port.

SI_A, SI_B, SI_C, and SI_D (I = 0, 1) Source Port Select (Inputs)
Each pair of inputs determines the source of data for the corresponding I/O port when used as a destination port.

$\overline{ERR}_A$, $\overline{ERR}_B$, $\overline{ERR}_C$ and $\overline{ERR}_D$ $\overline{ERROR}$ (Output, open drain)
Each output pin is used to flag Parity/Bus errors. Error is indicated by a LOW output.

LEO_A, LEO_B, LEO_C, and LEO_D Output Latch Enable (Inputs; Active HIGH)
Each LEO input controls a 9-bit wide latch on the output side of the corresponding I/O port. The latches are transparent when LEO is HIGH and are latched when LEO is LOW.

$\overline{OE}_A$, $\overline{OE}_B$, $\overline{OE}_C$, and $\overline{OE}_D$ Output Enable (Inputs; Active LOW)
Each $\overline{OE}$ input controls the bus drivers of the corresponding I/O port. When $\overline{OE}$ is LOW, data at the output of the Output latches is passed to the bus. When $\overline{OE}$ is HIGH, the bus outputs are in high-impedance state.

Am29C985 OPERATIONAL DESCRIPTION

Parity and bus checking are provided on the Am29C985. Parity checking and generation are both performed at the output. In order to preserve parity coverage through the part, the data driven onto the bus, including the generated parity, is compared to the data passing through the multiplexer, including the old parity. This has two effects: The comparison of the parity bits acts as a parity check. Also bus errors will be detected if the bus data does not agree with the data being driven.

Minimization of Ground Bounce through Output Edge-Rate Control

The Am29C985 incorporates AMD's proprietary edge controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in specified device propagation delay.

Power-Up/Down Disable

The Am29C985 contains a unique power up/down circuit to provide glitch free outputs during power-supply sequencing. This power-up circuit ensures that at low V_{CC} values (typically 0–2.0 V), the outputs are disabled and in 3-state. At V_{CC} values above this threshold, the outputs will remain disabled and not glitch to an active state if the appropriate output-enable inputs are conditioned for 3-state functionality. At V_{CC} values above the disable circuitry threshold, if the output-enable inputs are conditioned active (outputs enabled), the outputs will respond to a steady state input value. Additionally, the outputs will exhibit high impedance characteristics under power conditioning.

Input/Output Structures

Typical CMOS devices on the market today have maximum DC I/O voltage ratings that prevent some card edge applications, due to the uncertainty of the I/O voltage with respect to V_{CC}. This uncertainty occurs when extracting or replacing a card into a powered-on connector or when a powered-off device is sitting on an active bus. Under these conditions, the maximum rating of –0.5 V to V_{CC} + 0.5 V may be violated. This rating is derived from the presence of a parasitic diode from the input or output to V_{CC}. To prevent forward biasing the diode with an active signal, the 0.5 V limit above V_{CC} was adopted.

AMD has addressed this situation with unique input and output structures. These structures on the Am29C985 use an n-channel pull-up transistor. This results in a stacked n-channel output buffer and a proprietary ESD input cell.

These circuit modifications result in a maximum DC I/O voltage rating of –0.5 V to 7.0 V. The maximum rating is no longer a function of the V_{CC} voltage, thus allowing 3-state functionality under power off condition.

In addition, another benefit gained is that the n-channel pull-up reduces the output HIGH-level voltage for a lightly loaded output to 4.0 V, at V_{CC} = 5.0 Volts. This reduces switching noise and cross-talk associated with typical CMOS full rail-to-rail travel.

FUNCTIONAL DESCRIPTION

The Am29C985 Multiple Bus Exchange consists of four 9-bit I/O ports. Each port has a 9-bit output latch to capture outgoing data. There are four control pins associated with each port: two Select inputs for source port selection, one Output Latch Enable input (active HIGH) to control Output latches, and an active LOW Output Enable line to control the bus driver at the I/O port.

Port Selection and Control

Each port is independently controlled by these four control inputs. If the output drivers of a port are disabled (high-impedance state), that port is an input and can be used as a source port. At the same time, the data at one of the four internal buses can be transferred to the Output latch under the control of the appropriate Select inputs. If the output drivers are enabled, the port serves as a destination port, transporting the data at the output of its Output latch to the external bus connected to the I/O port. Independent control of the Output latch permits stored operation at any port.

Parity and Bus checking

In the Am29C985, parity checking and recognition are both performed at the output. To preserve parity coverage through the part, the data driven onto the bus, including the regenerated parity, is compared to the data passing through the switch, including the old parity. This has two effects: the comparison of parity bits acts as a parity check. Also bus errors will be detected if the bus data does not agree with data being driven to the output buffer.

Error Outputs

$\overline{ERR}$ pins are active LOW, open drain outputs. This allows easy combination of multiple bytes. When passing non-parity data through the part the output will have correct odd parity, but an error may be indicated due to the uncertainty of the 9th bit. Under this condition it is up to the user to ignore the error.

Multiple Bus Communication

Four internal buses serve as pathways for port-to-port connection. By proper choice of source select codes for the ports, the Am29C985 can be configured in different modes for multiple bus communication. In one mode of operation, two ports can be selected as source ports and the other two as destination ports; thus, two independent bidirectional communication channels are established. In another mode, one port can be selected as the source, and one or more of the other ports can serve as destination ports. Any port not intended as a destination port can be disabled (high-impedance state) by its Output Enable control.

A. Port Source Selection

$S1_n$	$S0_n$	Source
L	L	A Bus
L	H	B Bus
H	L	C Bus
H	H	D Bus

B. Output Latch Operation

LEO_n	Mode
H	Transparent
L	Latched

C. I/O Port Controls

LEO_n	$\overline{OE}_n$	I/O	Source of Data
L	L	Out	Contents of Output Latch
H	L	Out	Selected Source Port
X	H	In	

Key: n = A, B, C, or D
L = LOW
H = HIGH
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	−0.5 to 7.0 V
DC Input Diode Current	
(I_{IK}) (V_{IN} < 0 V)	−20 mA
(V_{IN} > V_{CC} if applicable)	+20 mA
DC Input Voltage (V_{IN})	−0.5 to 7.0 V
DC Output Diode Current	
(I_{OK}) (V_{OUT} < 0 V)	−50 mA
(V_{OUT} > V_{CC} if applicable)	+50 mA
DC Output Current per Output Pin:	
I_{SINK}	+70 mA
I_{SOURCE}	−30 mA
DC Output Voltage (V_{OUT})	−0.5 to 7.0 V
Total DC Ground Current (I_{GND})	1750 mA
Total DC V_{CC} Current (I_{CC})	575 mA
Storage Temperature	−65 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OH} = −15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 0 V			−10	µA
I_{IH}	Input HIGH Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0 V			−20	µA
I_{OZH}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−60		mA
I_{CCQ}	Quiescent Power Supply Current (Note 4)	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND, Outputs Open			1.5	mA
I_{CCT}	Power Supply Current TTL Input HIGH (Note 4)	V_{CC} = 5.5 V, V_{IN} = 2.4 V Other Inputs at V_{CC} or GND			3.0	mA/ Input

DC CHARACTERISTICS (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{CCD}	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)		500	µA MHz/Bit

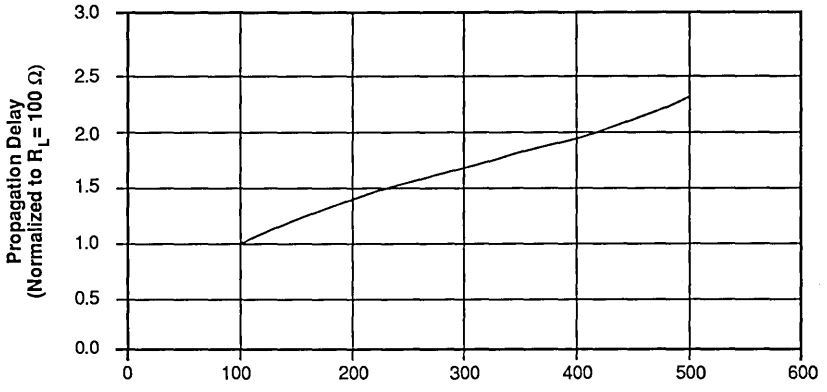
SWITCHING CHARACTERISTICS over operating range unless other specified.

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	1.5	12	ns
2	t_{PHL}	LEO = HIGH		1.5	12	ns
3	t_{PLH}	Propagation Delay Select Input to Port		1.5	12	ns
4	t_{PHL}	LEO = HIGH		1.5	12	ns
5	t_{PLH}	Propagation Delay Port to Parity		1.5	14	ns
6	t_{PHL}	LEO = HIGH		1.5	14	ns
7	t_{PLH}	Propagation Delay		1.5	10	ns
8	t_{PHL}	LEO to Port		1.5	10	ns
9	t_{PZH}	Output Enable Time		1	10	ns
10	t_{PZL}	$\overline{OE}$ to Port		1	10	ns
11	t_{PHZ}	Output Disable Time		0	9	ns
12	t_{PLZ}	$\overline{OE}$ to Port		0	9	ns
13	t_{PD}	Propagation Delay Port to $\overline{ERR}$ Valid (Note 5)		2.0	14	ns
14	t_{PLH}	Propagation Delay		2.0	15	ns
15	t_{PHL}	Select to Parity		2.0	15	ns
16	t_{PLH}	Propagation Delay		2.0	14	ns
17	t_{PHL}	LEO to Parity		2.0	14	ns
18	t_s	Port to LEO Setup		4.5		ns
19	t_h	Port to LEO Hold		0		ns
20	t_s	Select to LEO Setup		6.0		ns
21	t_h	Select to LEO Hold		0		ns
22	t_{PWH}	LEO Pulse Width HIGH		3		ns

Notes:

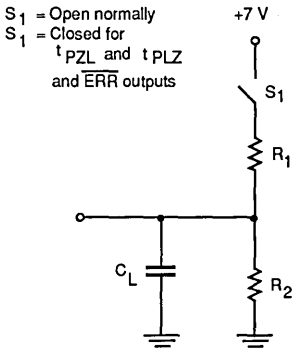
1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 ms.
3. Measured at a frequency of < 10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC}: $I_{CC} = I_{CCO} + I_{CCT}D_HN_T + I_{CCO}(f_{CP}/2 + f_iN_i)$
   Where: D_H = Duty cycle for each TTL input HIGH
   N_T = Number of inputs at D_H
   f_{CP} = Clock frequency for clocked devices (Zero for non-clocked devices)
   f_i = Input frequency of the i^{th} input
   N_i = Number of inputs at f_i
5. The propagation delay time is proportional to the output pull-up resistor to V_{CC}. In this case the measurment is done with the pull-up resistor = 100 Ω. Please refer to graph on the following page for more details

Am29C985 Port Out to $\overline{ERR}$ Valid
V_{CC} = 4.50 V, T_a = 70°C



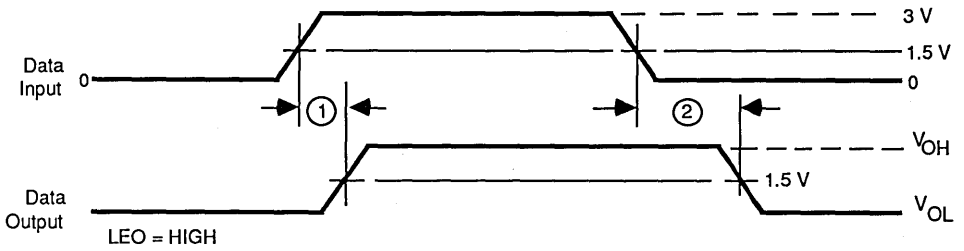
11996-015A

SWITCHING TEST CIRCUIT



11996-006A

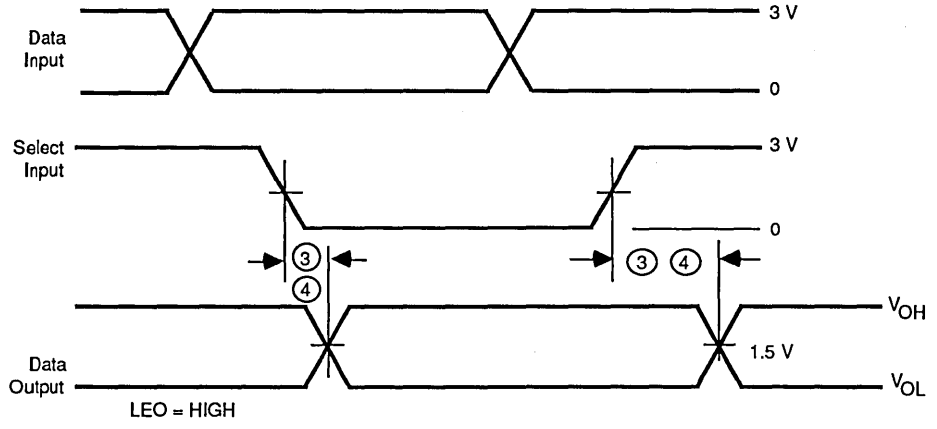
SWITCHING TEST WAVEFORMS



Propagation Delay—Port-to-Port

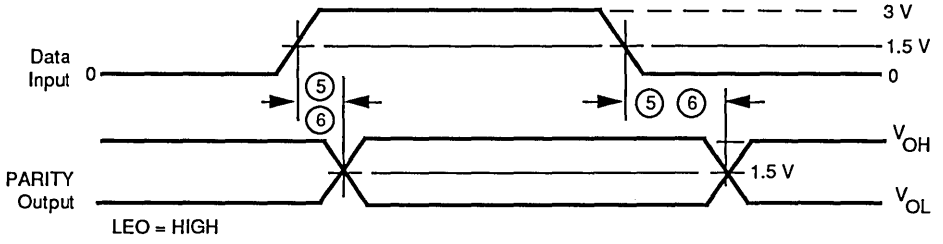
11996-007A

SWITCHING TEST WAVEFORMS (Cont'd.)



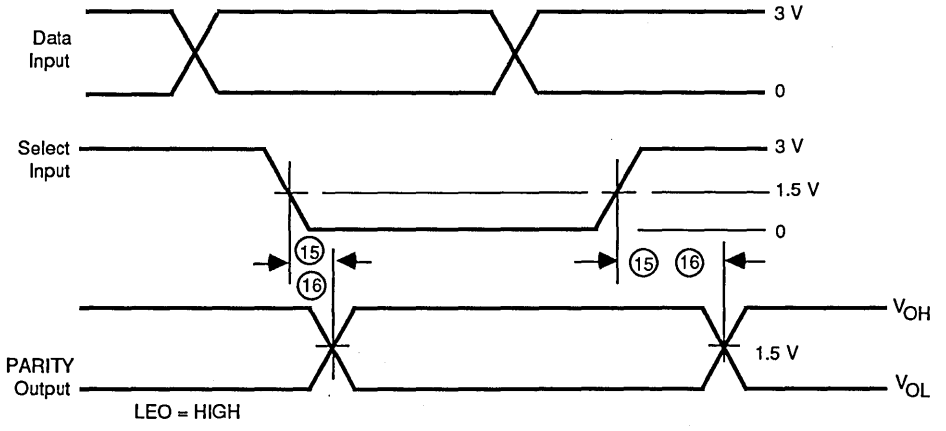
Propagation Delay—Select-to-Port

11996-008A



Propagation Delay — Port to Parity

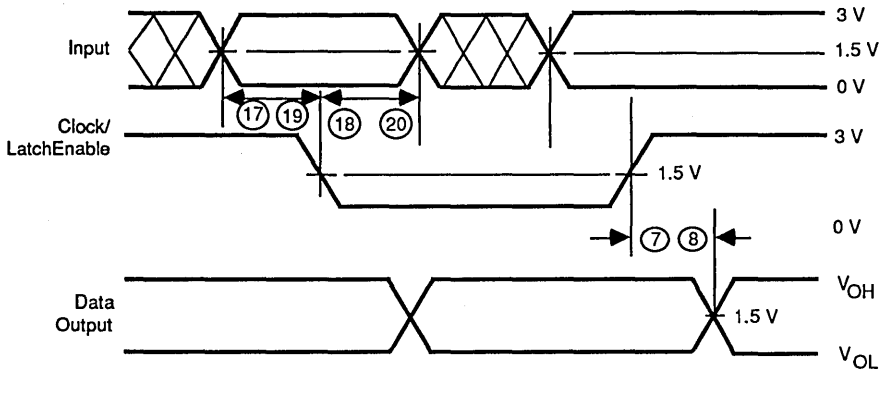
11996-009A



Propagation Delay — Select to Parity

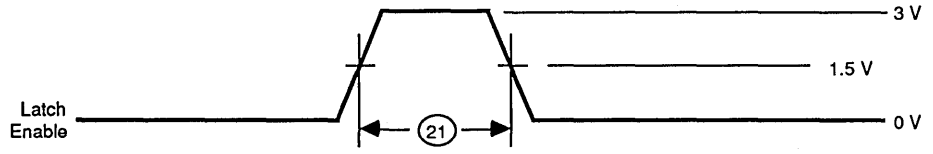
11996-010A

SWITCHING TEST WAVEFORMS (Cont'd.)



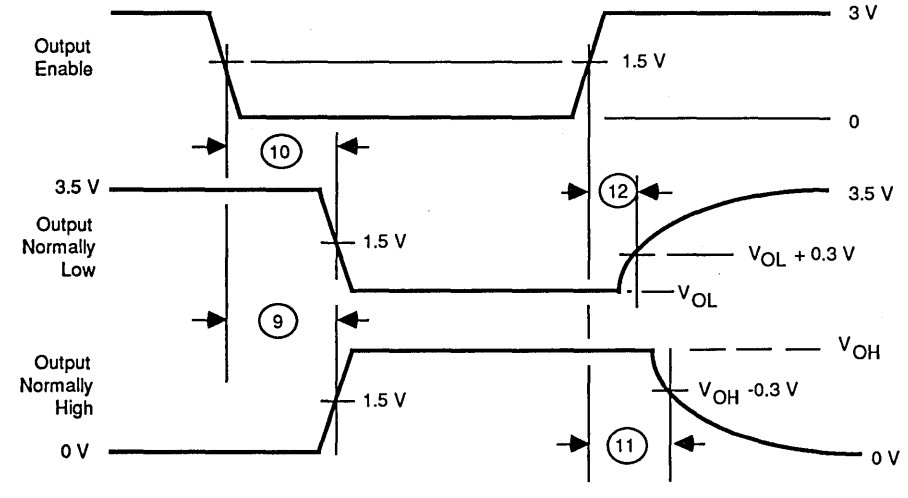
11996-011A

Output Latch Propagation Delay, Setup and Hold Times



Minimum Latch Enable

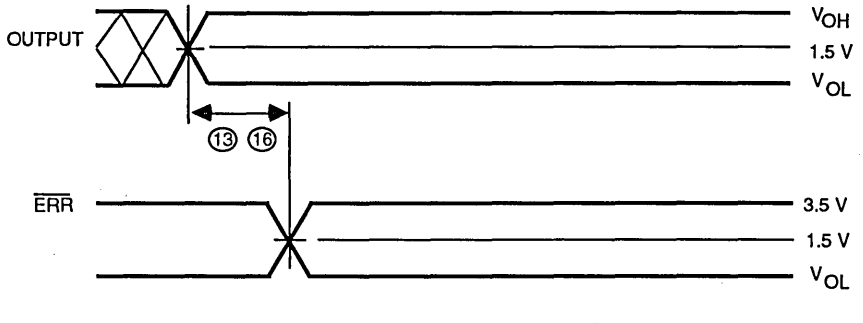
11996-012A



11996-013A

Enable and Disable Times

SWITCHING TEST WAVEFORMS (Cont'd.)

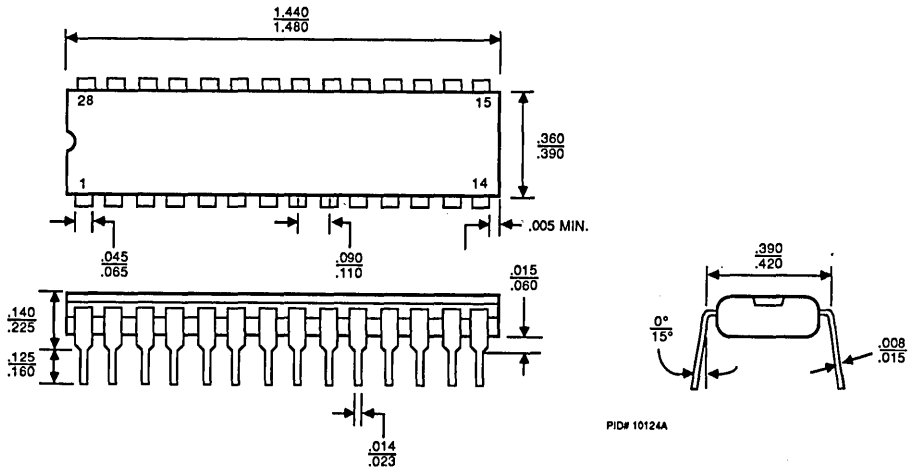


11996-014A

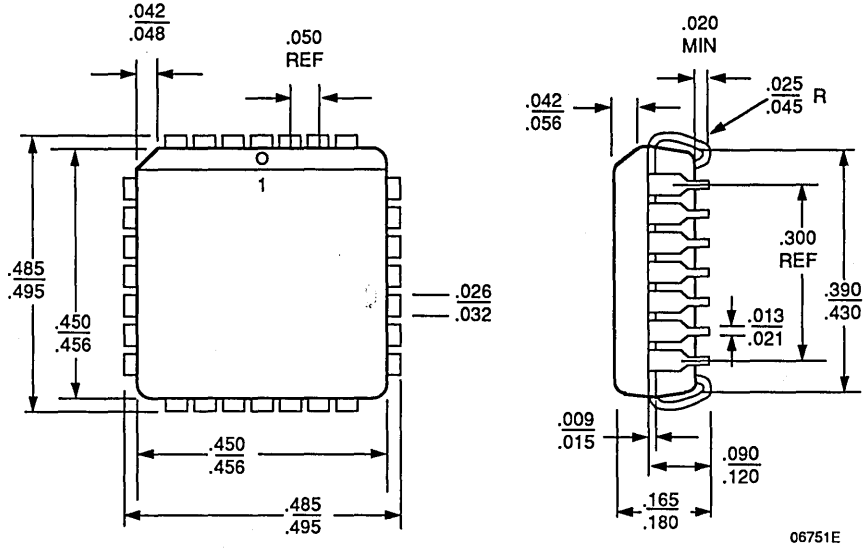
Propagation Delay—Output Port to $\overline{ERR}$

CHAPTER 6
Physical Dimensions

PD4028



PL 028



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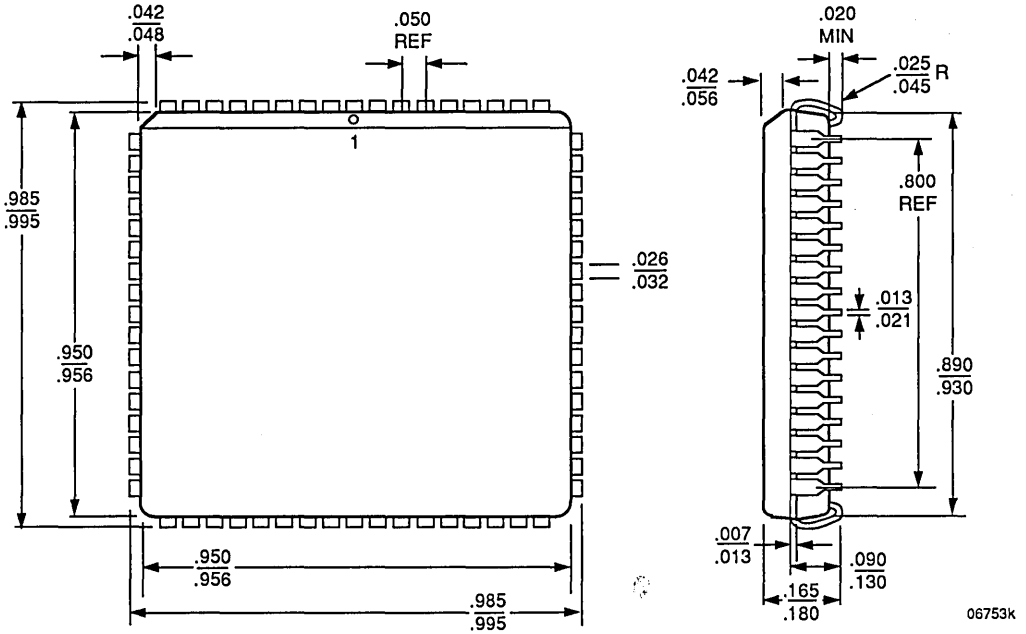
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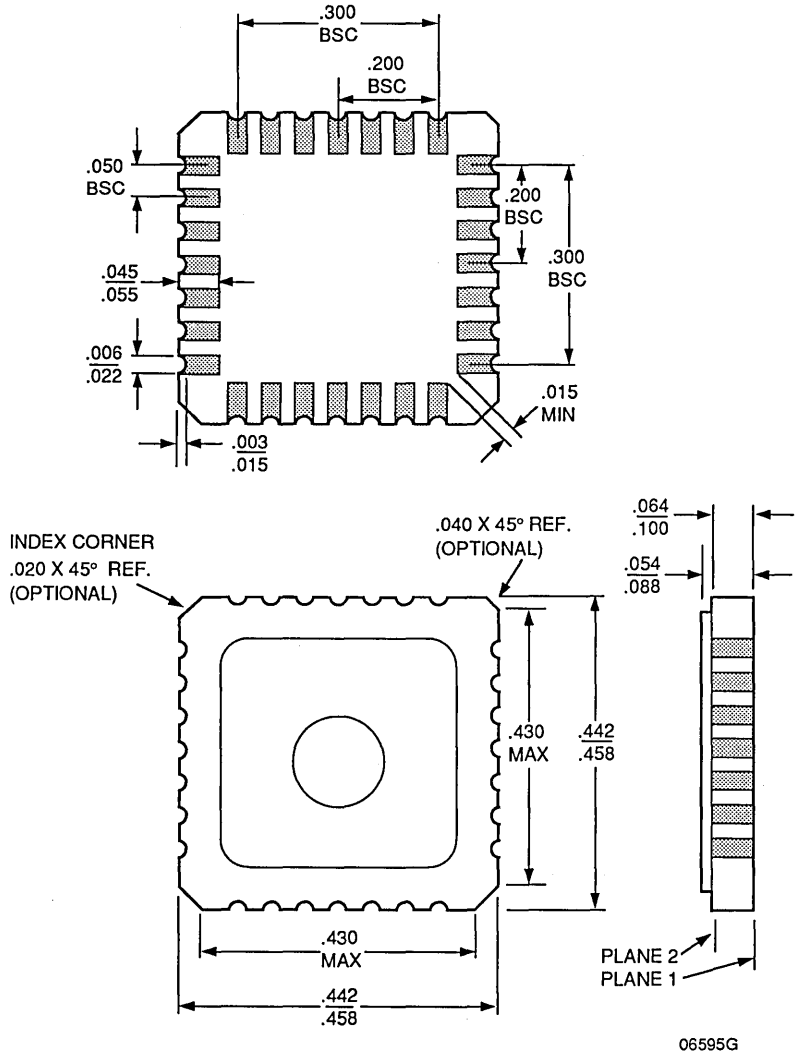
CL 028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(OPTIONAL)
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.054
.088
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MAX
.442
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.430
MAX
.442
.458
PLANE 2
PLANE 1
06595G

APPENDIX A
Electronic Design Automation Tools from OrCAD Systems Corporation

ELECTRONIC DESIGN AUTOMATION TOOLS FROM ORCAD SYSTEMS CORPORATION

With today's complex designs, the efficiency of Electronic Design Automation products is more than important, it's vital. Your company doesn't have the time or resources to redraw schematics, revise part lists and netlists using bad tools. For this reason, AMD has developed OrCAD® models of our most popular High Performance Bus Interface, Multiple Bus Exchange and Dynamic Memory Management products.

OrCAD is the world's largest volume producer of Electronic Design Automation tools. OrCAD/STD™ III is quick and easy to learn. Intuitive pop–up menus and quick keyboard commands let you start designing immediately. Work in OrCAD/SDT III flows logically in a progression of steps mirroring your own intuitive approach to design.

OrCAD/STD III includes everything you need to handle the most complex design challenges on your PC. In the package are powerful ways to automate:

- Bill of materials/parts list generation
- Electrical Rules Checking
- Forward and backward annotation
- Cross reference
- Netlist generation

High Performance Bus Interface devices supported include:

- Am29821, Am29823, Am29825, Am29827, Am29828, Am29841
- Am29843, Am29863
- Am29818A, Am29827A, Am29833A, Am29853A, Am29861A
- Am28C818A, Am29C821A, Am29C823A, Am29C827A, Am29C828A
- Am29C833A, Am29C841A, Am29C843A, Am29C853A, Am29C861A
- Am29C863A

Multiple Bus Exchange devices supported include:

- Am29C982
- Am29C983, Am29C983A
- Am29C985

Dynamic Memory Management devices supported include:

- Am29C668, Am29C668–1, Am29C676
- Am29C660, Am29C660A, Am29C660B, Am29C660C, Am29C660D, Am29C660E
- Am29C60, Am29C60–1, Am29C60A

OrCAD may be contacted for price and availability information, at the following address:

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OrCAD Systems Corporation
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APPENDIX B
Behavioral Simulation Models from Logic Automation Inc.

BEHAVIORAL SIMULATION MODELS FROM LOGIC AUTOMATION, INC.

- Fast and Accurate
- Extensive Usage and Timing Checks
- Over 5000 Devices Supported
- Compatible with Leading Simulators
- SmartModel Windows™, a System Emulation Capability for Viewing and Changing Register Contents

SmartModels® are behavioral language–simulation models with built–in expert assistance, used for board– and system–level simulation. Models of thousands of devices are available ranging from complex microprocessors to memories, PLDs, and TTL logic. Simulation provides several benefits to the user including faster design time, lower prototype costs, and higher quality product.

SmartModels increase designer productivity with extensive messages including usage checks and timing checks. The SmartModel usage checks look for undefined interrupts, uninitialized registers, illegal conditions—any misuse of the component that is likely to slow or stall the design process. These are reported as thoroughly as possible, pin–pointing the error by documenting the design sheet, part instance, pin name, and the time of occurrence, so the error can be eliminated immediately.

SmartModel timing checks look for violations of timing specifications like set–up, hold, and recovery. Messages cite the required specification as well as the violation, along with the pin location and simulation time. The result is that the designer need not interrupt the system verification to search component data books for specifications. The necessary data is right there, built into the simulation models.

Multiple Bus Exchange devices supported include:

- Am29C982
- Am29C983, Am29C983A
- Am29C985

High Performance Bus Interface devices supported include:

- Am29821, Am29823, Am29825, Am29827, Am29828, Am29841
- Am29843, Am29863
- Am29818A, Am29833A, Am29853A, Am29861A
- Am29C818A, Am29C821A, Am29C823A, Am29C827A, Am29C828A
- Am29C833A, Am29C841A, Am29C843A, Am29C853A, Am29C861A
- Am29C863A

Dynamic Memory Management devices supported include:

- Am29C668, Am29C668–1, Am29C676
- Am29C660, Am29C660A, Am29C660B, Am29C660C, Am29C660D, Am29C660E

Host Systems supported now include:

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- Valid Logic
- Gateway Design Automation
- HHB Systems
- Vantage
- Hewlett Packard
- AT&T (proprietary)
- GENRAD
- Cadence Design Systems
- Racal – Redac

Host Systems under development include:

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- Teradyne
- Viewlogic
- Silicon Compiler Systems

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Phone: (503) 690–6900 **FAX:** (503) 690–6906
Electronic Bulletin Board: (503) 690–6907

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Farley Hall, London Road
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United Kingdom
Phone: 44 (0) 344 863230 **FAX:** 44 (0) 344 863999
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APPENDIX C
Device Process and Package Information

28-PIN 4-BIT X 4-PORT MULTIPLE BUS EXCHANGE (Am29C982)

Process/Die Information

1. Process Name: CS11S
2. Process Technology: CMOS
3. Wafer Fabrication: Fab 15, Austin Texas
4. Device Number: Am29C982
5. Die Size: 151 x 155 mils
6. Last Overall Die Revision: "A"
7. Bond Pad Size: 125 x 125 µ
8. Number of Metal Layers: 2
9. Metal Thickness: 0.35µ/1.0µ
10. Content of Metalization: 1st level – Ti/TiN–0.5%Cu/Si/Al–MoSi
    2nd level – Al
11. Minimum Line/Spacing Width: 2µ width, 1.5µ spacing
12. Contact Dimensions (via's): 1.6µ x1.6
13. Passivation Material: 4% LTO/Nitride
14. Passivation Thickness: 7000 Å /8500 Å
15. ESD protection: 2000 V

Packaging Information

1. Assembly Location: Malaysia, Phillipines or Korea
2. Test Location: Malaysia or California

PLCC/PDIP Packages:

3. Resin Identification: Epoxy Novolac
4. Package Compound: Sumitomo 6300H
5. Filler Content: Fused Silicon
6. Thermal Conductivity: >13 x 10^{-4} calorie/cm °C sec
7. Glass Transition Temperature: 155 °C
8. Die Attach Material: Silver Filled Epoxy
9. Die Attach Vender: Dexter Hysol
10. Wire Bond Metal: 1.25 mil gold wire
11. Wire Bond Method: Thermosonic
12. Lead Frame Material: Copper
13. Lead Frame Finish: Solder Plate

Ceramic/LCC Packages for Military

14. Die Attach Material: Ag/Glass paste
15. Sealing Process: Gold Tin
16. Body Material: 90% Al_2O_3
17. Lid Material: ASTM–15–78 alloy (Kovar)
18. Die Attach Material: Silver Glass
19. Die Attach Vendor: Johnson Mathey Incorporated
20. Wire Bond Metal: A1 (99%) Silicon (1%)
21. Wire Bond Method: Ultra Sonic Wedge Bonding
22. Lead Fram Finish: Gold Plated

68-PIN 9-BIT X 4-PORT MULTIPLE BUS EXCHANGE (Am29C983A, Am29C983, Am29C985)

Process/Die Information

1. Process Name: CS21
2. Process Technology: CMOS
3. Wafer Fabrication: Fab 15, Austin Texas
4. Device Number: Am29C983/Am29C985/Am29C983A
5. Die Size: 178 x 183 mils
6. Last Overall Die Revision: "B"
7. Bond Pad Size: 112 x 112 µ
8. Number of Metal Layers: 2
9. Metal Thickness: 0.32µ/1.0µ
10. Content of Metalization: 1st level – Ti/TiN–0.5%Cu/Al–MoSi
    2nd level – Al
11. Minimum Line/Spacing Width: 2µ width, 1.6µ spacing
12. Contact Dimensions (via's): 1.4µ x 1.4µ
13. Passivation Material: 4% LTO/Nitride
14. Passivation Thickness: 7000 Å /8500 Å
15. ESD protection: 2000 V

Packaging Information

1. Assembly Location: Malaysia, Phillipines or Korea
2. Test Location: Malaysia or California

PLCC Packages:

3. Resin Identification: Epoxy Novolac
4. Package Compound: Sumitomo 6300H
5. Filler Content: Fused Silica
6. Thermal Conductivity: $>13 \times 10^{-4}$ calorie/cm °C sec
7. Glass Transition Temperature: 155 °C
8. Die Attach Material: Silver-Filled Epoxy
9. Die Attach Vender: Dexter Hysol
10. Wire Bond Metal: 1.25 mil gold wire
11. Wire Bond Method: Thermosonic
12. Lead Frame Material: Copper
13. Lead Frame Finish: Solder Plate

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	FAX	(1) 49-75-10-13
	TLX	263282F
WEST GERMANY,		
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	FAX	(0511) 721254
	TLX	922850
München	TEL	(089) 4114-0
	FAX	(089) 406490
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