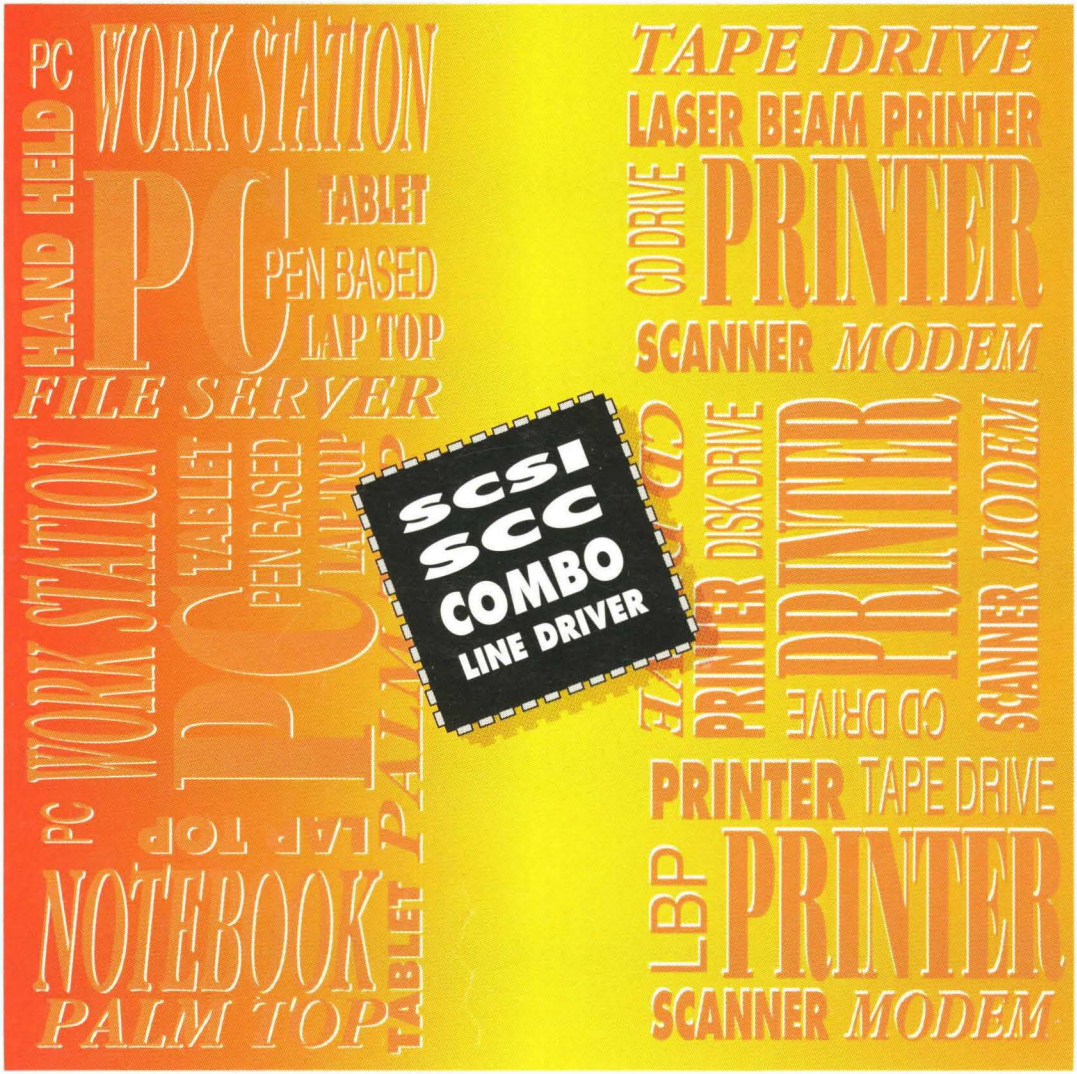
Data Communication Products

1992 Data Book/Handbook

Advanced
Micro
Devices



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Data Communication Products

1992 Data Book/Handbook

ADVANCED MICRO DEVICES

Advanced Micro Devices offers a complete line of Data Communications products. Optimized for industry standard protocols, these products allow CPU hosts to communicate with peripherals. Our Data Communication product family includes Small Computer System Interface (SCSI) Controllers, Enhanced Serial Communication Controllers (ESCC), Combination devices containing both SCSI and SCC blocks, and Interface Line Drivers and Receivers.

AMD's sub-micron CMOS process technology, advanced packaging programs and continued commitment to industry leading quality and reliability ensures that you are designing with high-value added ICs.

Remember, our partnership helps you gain and keep the competitive edge. We are not your competition.

Fred J. Roeder
Vice President
Standard Products Division

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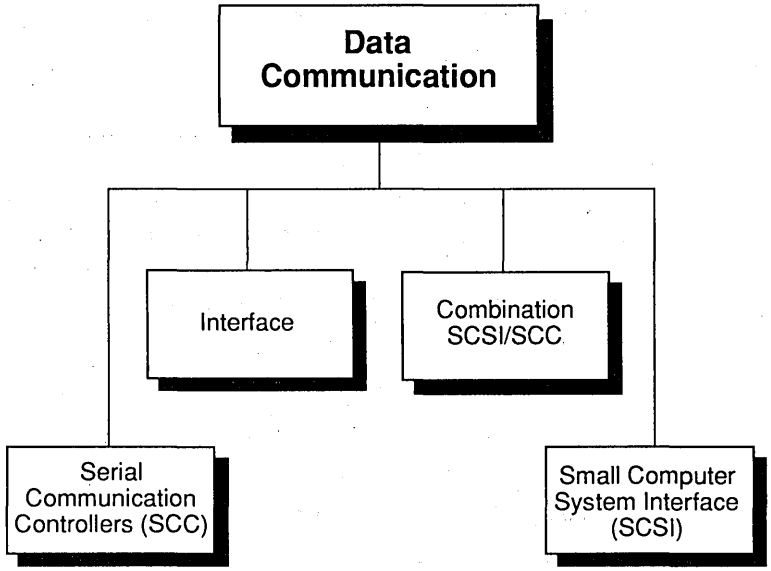
Data Communication Products



Introduction

AMD offers a complete line of Data Communications products which allow CPU hosts to communicate with peripherals using various industry standard protocols. AMD's Data Communications product family includes Small Computer System Interface (SCSI) Controllers, Serial Communications Controllers (SCC), Combination devices containing both SCC and SCSI blocks, and Interface Line Drivers and Receivers.

The Am53C94 and Am53C96 High Performance SCSI Controllers (HPSC) are plug-in replacements for the industry standard 53C94 and 53C96, respectively. The HPSC has a flexible three bus architecture. It has a 16 bit DMA interface, an 8 bit host data interface and an 8 bit SCSI data interface. The HPSC is designed to minimize host intervention by implementing common SCSI sequences in hardware. An on-chip state machine reduces protocol overheads by performing the required sequences in response to a single command from the host. Many SCSI-2 features are supported including Selection, Reselection, and Disconnection commands, which are directly supported.

Due to a popular move towards SCSI, AMD has second-sourced Western Digital's 33C93A second generation SCSI controller, enhancing it by fabricating the device on a submicron CMOS process technology. The 33C93A is the only second sourced SCSI controller in this category, allowing peripheral and host system manufacturers to build state-of-the-art systems, at low cost, while taking advantage of the 33C93A's 5MByte/second synchronous transfer rate.

The 53C80A first generation SCSI device has been improved by AMD with the addition of enhanced ESD protection and with proprietary "glitch eating" circuitry on the SCSI bus inputs, which increases the reliability of systems by filtering out noise Con the SCSI bus due to inadequate termination and high current swings.

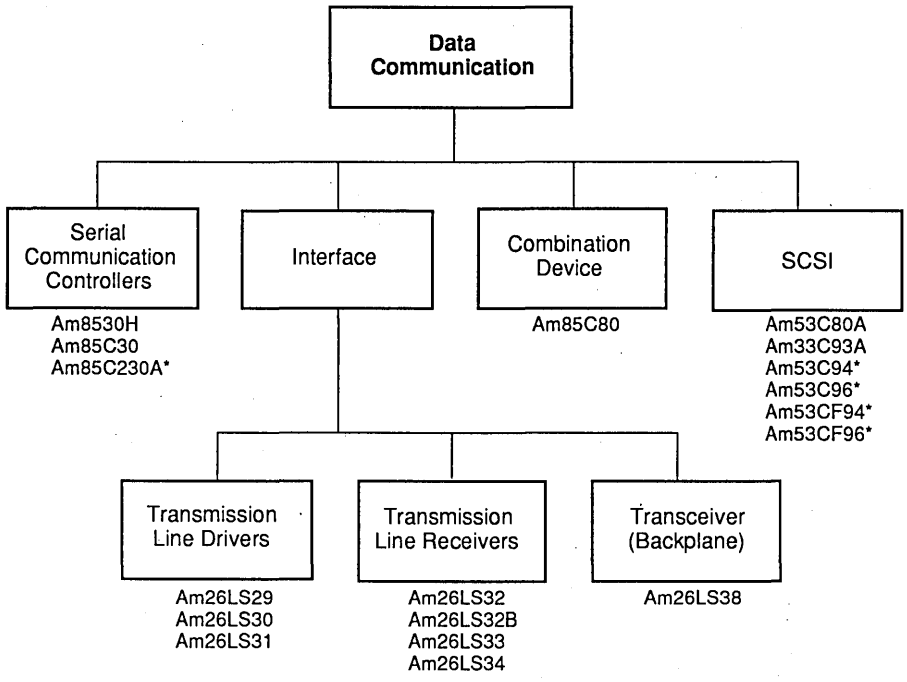
The Am8530H is the first generation of the serial communication controller family. It is designed for the use with the 8- and 16-bit microprocessors. The SCC is dual-channel and can be software configured to satisfy a wide variety of serial communication applications.

The Am85C30 ESCC is a high performance version of the industry-standard 8530 architecture. AMD's version incorporates enhancements which make CPU interfacing much easier, reducing software overhead, and increasing performance. As a result, the Am85C30 has become an industry standard serial interface on engineering workstations and many other high performance platforms.

The next generation of the SCC family is the Am85C230A. The Enhanced Serial Communication Controller with LocalTalk support. The Am85C230A is not only plug compatible to Z85230, it is a functional superset with LocalTalk enhancements; 4 deep transmit FIFO extension (total of 8 bytes), sleep mode, quieter Rx and Tx clock inputs, die revision information and ready signal to reflect write recovery time.

The Am85C80 Combination SCSI/SCC Controller is a unique device which incorporates an Am85C30 SCC and an Am53C80A SCSI ON ONE CHIP. This integration allows designers using both of these I/O functions to save valuable board space, power consumption, and manufacturing cost. Additionally, due to its fully-static CMOS design, the Am85C80 may be "put to sleep" when used with battery-powered systems, allowing a power consumption reduction of over 2000X, as compared with using two separate components.

AMD is the industry's leading supplier of standard interface devices including transmission line receivers, line drivers and backplane tranceivers.



Part Number	Description
Serial Communication Controllers	
Am8530H	Serial Communication Controller
Am85C30	Enhanced Serial Communication Controller
Am85C230A*	Enhanced Serial Communication Controller with LocalTalk Support
Interface	
Transmission Drivers	
Am26LS29	Quad RS-423 Line Driver
Am26LS30	Quad RS-422/423 Driver
Am26LS31	Quad RS-422 Line Driver
Transmission Line Receivers	
Am26LS32	Quad RS-422 Line Receiver
Am26LS32B	Quad RS-422/423 Line Receiver
Am26LS33	Quad High Vcm Line Receiver
Am26LS34	Quad Party Line Receiver
Transceiver (Backplane)	
Am26LS38	Quad Differential Backplane Transceiver

Part Number	Description
Combination SCSI/SCC	
Am85C80	CMOS SCSI/SCC Combo Chip
SCSI	
Am53C80A	CMOS SCSI Interface Controller (NCR Alternate Source)
Am33C93A	Enhanced CMOS SCSI Bus Interface Controller (Western Digital Second Source)
Am53C94*	High Performance CMOS SCSI Controller (Single-Ended; NCR Alternate Source)
Am53C96*	High Performance CMOS SCSI Controller (Single-Ended and Differential; NCR Alternate Source)
Am53CF94*	CMOS Fast SCSI-2 Chip (Emulex FAS216 Alternate Source; NCR Alternate Source)
Am53CF96*	CMOS Fast SCSI-2 Chip (Emulex FAS236 Alternate Source; NCR Alternate Source)

* In development

CHAPTER 1
Small Computer System Interface (SCSI) Controllers

Am33C93A

Enhanced SCSI-Bus Interface Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation/checking on both data ports, soft reset, and synchronous data transfers
- Synchronous offset selectable from 1 to 12 bytes, with selectable transfer period up to 5 Mbytes/s
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature
- Can be used as a host adapter (SCSI Initiator) or peripheral adapter (SCSI Target)
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (DBA Bus) transfers
- Includes 48-mA drivers for direct connection to the SCSI bus
- 24 bit transfer counter
- Programmable timeout for selection and reselection
- "Combination" commands greatly reduce interrupt-handling responsibilities
- Special "Translate Address" command performs the Logical- to-Physical address translation
- Single +5 V supply
- Available in 44-pin chip carrier or 40-pin DIP
- Low power CMOS design

GENERAL DESCRIPTION

The Am33C93A is a MOS/VLSI device implemented in Advanced Micro Devices' CMOS process. It operates from a single 5-Volt supply and is available in either a 44-pin chip carrier or a 40-pin dual-in-line package. All inputs and outputs are TTL compatible.

The Am33C93A is intended for use in systems which interface to the Small Computer System Interface (SCSI) Bus. The Am33C93A can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the Am33C93A interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor issues a command to the Am33C93A to select the desired Target. The Am33C93A then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying and notifies the host when it has succeeded by generating an interrupt. At this point, the Am33C93A is operating in the initiator role. When the peripheral requests a SCSI command from the host, the Am33C93A receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the Am33C93A. The Am33C93A transfers the SCSI command to the peripheral, and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The Am33C93A also offers high-level Select-and-Transfer commands which eliminate the interrupt handling otherwise required between each SCSI bus phase.

When the Am33C93A is used in a peripheral system, the Am33C93A will operate primarily in a Target role. It interfaces with a local processor and the SCSI bus in this environment just as it does when used as a host adapter. The Target-role command set enables the Am33C93A to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The Am33C93A has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

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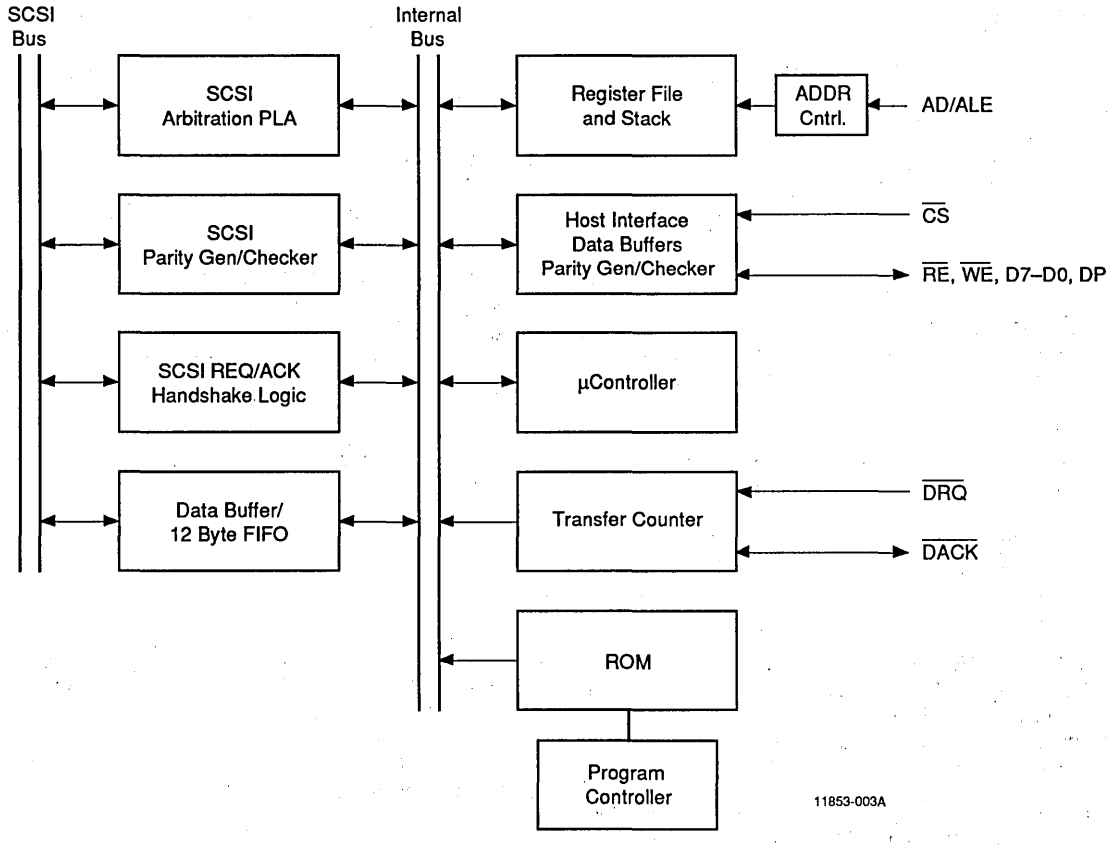
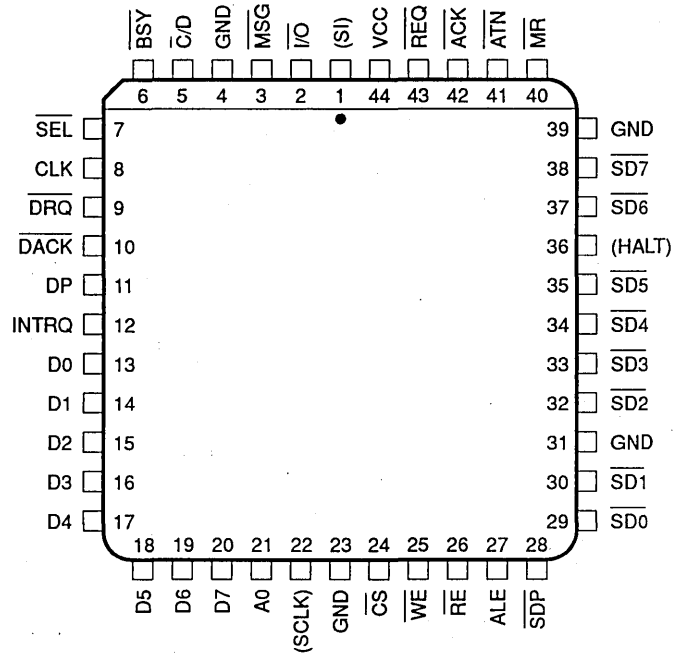
Issue Date: November 1991

BLOCK DIAGRAM



CONNECTION DIAGRAMS

44-PIN CHIP CARRIER



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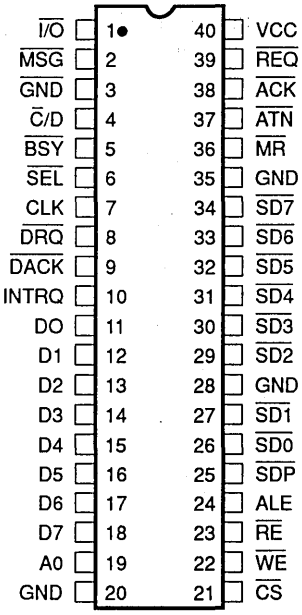
Note: Pins in parentheses are for test purposes only, and should be left unconnected for normal chip operation.

40-PIN DIP



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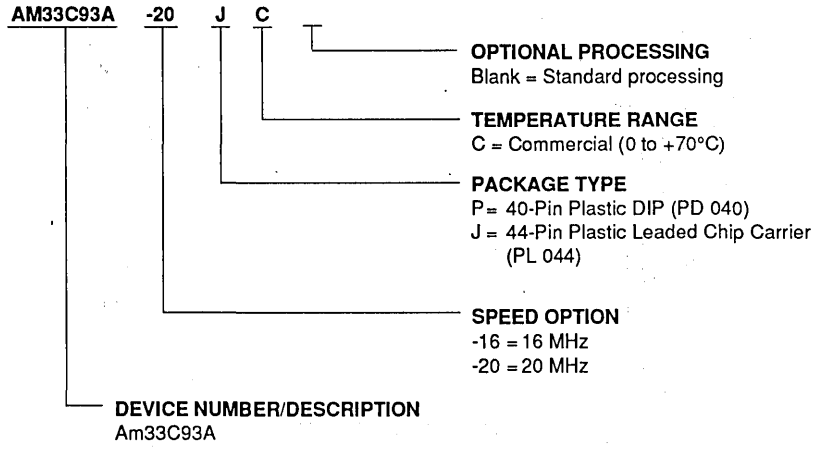
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid combination) is formed by a combination of:



Valid Combinations	
AM33C93A-16	JC, PC
AM33C93A-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

PIN DESCRIPTIONS

Processor/DMA Interface

Name	I/O	Function
CLK	I	8-20 MHz square wave clock.
$\overline{MR}$	I	Reset is an active-low input which forces the Am33C93A into an idle state. All SCSI signals are forced to the negated state.
INTRQ	O	Interrupt Request to external microprocessor indicates a command completion/termination or a need to service the SCSI interface. Reading the SCSI STATUS register clears this bit.
$\overline{RE}$	I/O	Read Enable is an active-low input which is used with $\overline{CS}$ to read a register or with $\overline{DACK}$ to access the DATA register in DMA mode. In DBA Bus mode, it is used as an output to read data from a sector buffer. (TRI-STATE)
$\overline{WE}$	I/O	Write Enable is an active-low input which is used with $\overline{CS}$ to write a register or with $\overline{DACK}$ to access the DATA register in DMA mode. In DBA Bus mode, it is used as an output to write data to a sector buffer. (TRI-STATE)
$\overline{CS}$	I	Chip Select is an active-low input which qualifies $\overline{RE}$ and $\overline{WE}$ when accessing a register. This signal must be inactive during a DMA cycle ($\overline{DACK}$ active in DMA and Burst DMA mode, or DRQ active in DBA Bus mode).
A0	I	Address pin A0 is used to access the internal registers for non-multiplexed address/data busses (i.e. the ALE pin is grounded). The address of the desired register is loaded into the ADDRESS register during a write cycle with A0=0. The selected register is then accessed when A0=1.
ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired Am33C93A register from the data bus. If indirect addressing is to be used, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
$\overline{DACK}$ ($\overline{RCS}$)	I/O	DMA acknowledge input used for interfacing to an external DMA controller (e.g. 8237). When $\overline{DACK}$ is low, all bus transfers are to/from the DATA register regardless of the contents of the ADDRESS register. In DBA Bus mode, this pin functions as a RAM chip select output to allow the Am33C93A to access a sector buffer. $\overline{RE}$ and $\overline{WE}$ are outputs when $\overline{RCS}$ (RAM Chip Select) is active. Since this pin can be an open drain output, a pullup resistor may be required when operating in DBA Bus mode.
$\overline{DRQ}$ (DRQ)	I/O	Data request is an output when interfacing to an external DMA controller, and an input when in DBA Bus mode. When used with an external DMA controller, $\overline{DRQ}$ and $\overline{DACK}$ form the handshake for the data-byte transfers. In Burst mode, $\overline{DRQ}$ remains low as long as there is data to transfer. In DBA Bus mode, the Am33C93A performs burst transfers while DRQ is high, and when DRQ is low, data transfers are inhibited, $\overline{RCS}$ is false, and the $\overline{RE}$ and $\overline{WE}$ outputs are disabled. Since this pin can be an open drain output, a pullup resistor may be required when operating in DMA or Burst mode.
D7–D0	I/O	Processor data bus.
DP	I/O	Data Parity, used only for checking/generating parity during data transfers.

SCSI Interface

Name	I/O	Function
$\overline{ATN}$	I/O	$\overline{ATN}$ is an output in the initiator role and an input in the target role. It is used to indicate the ATTENTION condition.
$\overline{ACK}$	I/O	$\overline{ACK}$ is an output in the initiator role and an input in the target role. It is used to indicate an acknowledgement for a REQ/ACK data transfer handshake.
$\overline{MSG}$	I/O	$\overline{MSG}$ is an input in the initiator role and an output in the target role. It is asserted during a MESSAGE phase.
$\overline{C}$/D	I/O	$\overline{C}$/D is an input in the initiator role and an output in the target role. It is used to indicate whether CONTROL or DATA information is on the SCSI data bus.
$\overline{REQ}$	I/O	$\overline{REQ}$ is an input in the initiator role and an output in the target role. It indicates a request for a REQ/ACK data transfer.

SCSI Interface (Cont.)

Name	I/O	Function
$\overline{I/O}$	I/O	$\overline{I/O}$ is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an Initiator.
$\overline{SD0–SD7}$	I/O	SCSI data bus.
$\overline{SDP}$	I/O	SCSI data bus parity signal.
$\overline{BSY}$	I/O	$\overline{BSY}$ is asserted when the Am33C93A is attempting to arbitrate for the SCSI bus or when connected as a Target.
$\overline{SEL}$	I/O	$\overline{SEL}$ is asserted when the Am33C93A is attempting to select or reselect another SCSI device.

Note: All pins have open-drain output drivers.

Am33C93A REGISTERS

Register Map

A0	R/W	Register Accessed		Address (HEX)
0	R	AUXILIARY STATUS REGISTER		XX
0	W	ADDRESS REGISTER		XX
1	R/W	OWN ID REGISTER	/CDB SIZE	00
1	R/W	CONTROL REGISTER		01
1	R/W	TIMEOUT PERIOD REGISTER		02
1	R/W	TOTAL SECTORS REGISTER	/CDB 1ST	03
1	R/W	TOTAL HEADS REGISTER	/CDB 2ND	04
1	R/W	TOTAL CYLINDERS REGISTER (MSB)	/CDB 3RD	05
1	R/W	TOTAL CYLINDERS REGISTER (LSB)	/CDB 4TH	06
1	R/W	LOGICAL ADDRESS (MSB)	/CDB 5TH	07
1	R/W	LOGICAL ADDRESS (2ND)	/CDB 6TH	08
1	R/W	LOGICAL ADDRESS (3RD)	/CDB 7TH	09
1	R/W	LOGICAL ADDRESS (LSB)	/CDB 8TH	0A
1	R/W	SECTOR NUMBER REGISTER	/CDB 9TH	0B
1	R/W	HEAD NUMBER REGISTER	/CDB 10TH	0C
1	R/W	CYLINDER NUMBER (MSB) REGISTER	/CDB 11TH	0D
1	R/W	CYLINDER NUMBER (LSB) REGISTER	/CDB 12TH	0E
1	R/W	TARGET LUN REGISTER		0F
1	R/W	COMMAND PHASE REGISTER		10
1	R/W	SYNCHRONOUS TRANSFER REGISTER		11
1	R/W	TRANSFER COUNT REGISTER (MSB)		12
1	R/W	TRANSFER COUNT REGISTER (2ND BYTE)		13
1	R/W	TRANSFER COUNT REGISTER (LSB)		14
1	R/W	DESTINATION ID REGISTER		15
1	R/W	SOURCE ID REGISTER		16
1	R	SCSI STATUS		17
1	R/W	COMMAND REGISTER		18
1	R/W	DATA REGISTER		19
1	R	AUXILIARY STATUS (DIRECT ADDRESSING MODE)		1F

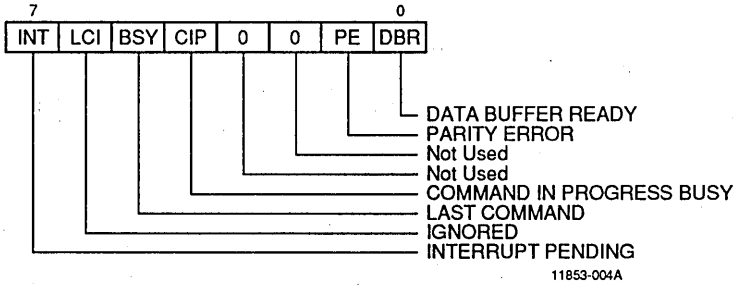
Notes:

1. *All unused bits of a defined register are reserved and must be zero.*
2. *Reading an undefined or unavailable register results in an all-ones data bus output.*
3. *Register addresses are determined by the ADDRESS register bits AR7 through AR0.*
4. *When using a multiplexed address/data bus with ALE, the A0 pin is ignored and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at hex 1F.*
5. *See Page 14 for a description of how reset affects the internal registers.*

Register Descriptions

AUXILIARY STATUS REGISTER (Address Hex 1F)

The AUXILIARY STATUS register is a read-only register which contains general status information not directly associated with the interrupt condition. The AUXILIARY STATUS register may be accessed at any time, except during DMA accesses (DACK asserted in DMA/Burst mode or DRQ asserted in DBA bus mode).



Bit	Name	Description
0	DBR	DATA BUFFER READY is used during programmed I/O to indicate to the processor whether or not the DATA register is available for reading or writing. During Send or Transfer commands which transmit data over the SCSI bus, the DBR bit is set when the Am33C93A is ready to take a byte from the host; the bit is reset when the processor writes the byte to the DATA register. During Receive or Transfer commands which receive data over the SCSI bus, the DBR is set when a byte is received; it is reset when the processor reads the byte from the DATA register.
1	PE	PARITY ERROR status indicates that even parity was detected on a data byte received during an information transfer. Parity is checked on data received from the host bus during transfers out to the SCSI bus and is checked on data received from the SCSI bus during transfers out to the host bus. Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTROL register. The PE bit is cleared when a new command is issued.
4	CIP	COMMAND IN PROGRESS, when set, indicates that the Am33C93A is interpreting the last command entered into the COMMAND register and therefore this register is unavailable. When this bit is reset, a command may be written to the COMMAND register.
5	BSY	BUSY indicates that a Level II command is currently executing and therefore only the COMMAND register (when CIP = 0), the DATA register, and the AUXILIARY STATUS register are accessible by the host. A Level II command may not be written to the COMMAND register when this bit is one.
6	LCI	LAST COMMAND IGNORED indicates that a command was issued by the host just prior to or concurrent with a pending interrupt, and therefore the command will be ignored.
7	INT	INTERRUPT PENDING indicates that the INTRQ pin is asserted. The host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

ADDRESS REGISTER (Address XX Hex)

The ADDRESS register is a write-only register which contains the address of the register to be accessed. Registers in the Am33C93A may be accessed in one of two ways:

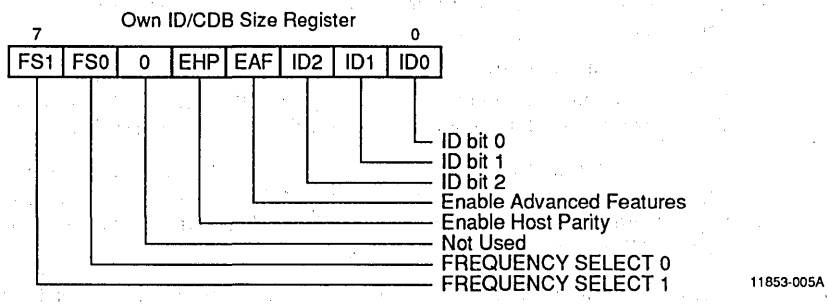
- Direct addressing (multiplexed address/data busses). In direct addressing, the falling edge of the ALE signal is used to latch the address into the ADDRESS register. The A0 pin should be connected to ground when using this method. The ALE is typically then followed by the $\overline{CS}$ and $\overline{WE}$ or $\overline{RE}$ signals that access the selected register. Also, in direct addressing, the AUXILIARY STATUS register is located at address 1F hex.
- Indirect addressing (separate address/data busses). In indirect addressing, the register access is performed in two separate cycles. This method is enabled by attaching ALE to ground. First, the ADDRESS register is loaded by performing a write of the desired address to the Am33C93A ($\overline{WE}$ and $\overline{CS}$ asserted) with A0=0. Then the register is accessed by asserting $\overline{CS}$ and $\overline{WE}$ or $\overline{RE}$, with A0=1. Also, following every access with A0=1, the ADDRESS register will automatically increment to point at the next register, with the exception of the following locations: AUXILIARY STATUS register, DATA register, and the COMMAND register. In indirect addressing, the AUXILIARY STATUS register is accessed by performing a read ($\overline{CS}$ and $\overline{RE}$ asserted) with A0=0.

OWN ID/CDB SIZE REGISTER (Address 00 Hex)

The OWN ID/CDB SIZE register, in its first mode, contains both the encoded ID of the Am33C93A on the SCSI bus and several control bits that are used to initially configure the device during the "Reset" command. These bits control 'advanced feature' selection, host bus parity enable, and selection of the divisor for the input clock. In its second mode (when advanced features are enabled, see p.16), this register is used during the combination commands to specify the SCSI CDB size if the command group is unknown to the Am33C93A.

In the first mode, this register (as defined below) is sampled and becomes effective only after a "Reset" command is issued to the device. This register must be initialized, and a "Reset" command must then be issued, following a hardware reset to set the SCSI bus ID, the clock divisor, and the operating modes before any other commands are issued.

In the second mode, bits 3-0 of this register are used during the Select-and-Transfer and Wait-for-Select commands to specify the SCSI Command Descriptor Block size if it is not a group 0, group 1, or group 5 command. This mode is enabled only when advanced features are enabled (see p.16).



Bit	Name	Description
0-2	IDn	SCSI ID Bits 0-2 set the SCSI bus ID number that the Am33C93A will use during arbitration and selection.
3	EAF	ENABLE ADVANCED FEATURES, when set to one, causes the Am33C93A to enable certain advanced features (see Page 16). When this bit is zero, those features are disabled.
4	EHP	ENABLE HOST PARITY, when set to one, enables odd parity checking on the host bus; the PE bit in the AUXILIARY STATUS register will indicate parity errors detected on the host bus, and the HHP bit in the CONTROL register will be used. When this bit is zero, no checking is performed on the host bus; the PE bit is not set when a parity error is detected on the host bus, and the HHP bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit	Name	Description
6–7	FSn	FREQUENCY SELECT 0–1 select the divisor that is applied to the input clock. The resulting clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. The correct divisor for the input clock must be used, or SCSI bus timing specifications may not be met.

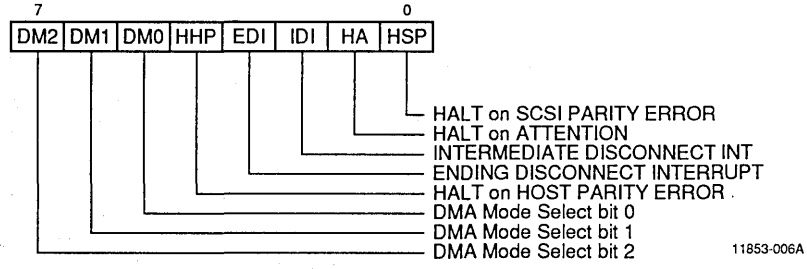
INPUT CLOCK FREQUENCY (MHZ)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
xx	1	1	Undefined

Note that an 11 MHZ clock rate should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is:

$$\text{Maximum SCSI Transfer Rate} = \frac{\text{Input Clock Fequency}}{\text{Clock Divisior}} \text{ [Mbyte/sec]}$$

CONTROL REGISTER
(Address 01 Hex)

The CONTROL register is used to enable/disable certain functions, such as response to parity errors and the SCSI attention condition, interrupt handling, and data transfer modes.



Bit	Name	Description
0	HSP	The HALT on SCSI PARITY ERROR bit enables the Am33C93A to immediately terminate a Receive or Transfer command if a parity error is detected on an incoming SCSI data byte. In the Initiator role, termination due to a SCSI parity error causes the $\overline{ACK}$ pin to be left in the active state in order to inhibit any additional data transfers (REQs) by the Target; this facilitates error handling with the Target. Synchronous data transfers check parity every 4096 bytes, or at the end of the remaining transfer count, whichever is less. Asynchronous transfers check parity on every byte.
1	HA	The HALT on ATTENTION bit (in Target mode only) enables the Am33C93A to terminate a Send or Receive command if the $\overline{ATN}$ input is asserted. This normally indicates that the Initiator detected a parity error while receiving data from the Am33C93A. The $\overline{ATN}$ input is tested before the start of a data transfer, every 4096 bytes if the transfer count is greater than 4096, and after the end of the transfer. These rules apply to both synchronous and asynchronous transfers.
2	IDI	The INTERMEDIATE DISCONNECT INTERRUPT bit, when set, enables the Am33C93A to generate an 85H interrupt and complete a Select-and-Transfer command if the Target disconnects according to the defined SCSI protocol. When this bit is reset, no interrupt is generated by a valid disconnect. This feature, when used with the Resume Select-and-Transfer command, provides support for overlapped SCSI operations. IDI is also used to select execution options in Target mode Combination commands that serve to reduce host system overhead. (Refer to COMMANDS, p.15 for more details.)

Bit	Name	Description
3	EDI	When the ENDING DISCONNECT INTERRUPT bit is set, the 16H interrupt which normally follows the COMMAND COMPLETE message during the execution of a Select-and-Transfer command will be suppressed until the Target disconnects from the SCSI bus. EDI is also used in the Target mode Combination commands to enable chaining between those commands, resulting in reduced host system overhead. Refer to COMMANDS p.15 for more details.
4	HHP	The HALT on HOST PARITY ERROR bit enables the Am33C93A to immediately terminate a Send or Transfer command if a parity error is detected on an incoming host data byte. Host parity errors are checked according to the rules for checking SCSI parity errors. However, a halt on a host parity error will not hold the $\overline{ACK}$ signal asserted when an error occurs. Host parity checking is performed at the same intervals as SCSI parity checking.
5-7	DMx	DMA MODE SELECT bits 2-0 are used to select the DMA mode of operation, which describes the host bus transfer mode used during Data In or Data Out phases. The following table describes the different DMA modes, and the state of these bits to select them:

DM2	DM1	DM0	DMA Mode Selected
0	0	0	POLLED MODE, or no DMA enabled. All data phase transfers are performed by polling for DBR in the AUXILIARY STATUS register, and then writing (reading) the data to (from) the DATA register.
0	0	1	BURST MODE selects a demand-mode DMA interface. In this mode, the $\overline{DRQ}$ signal will be active as long as there is data/space in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting $\overline{DACK}$ and $\overline{RE}$/$\overline{WE}$ as long as $\overline{DRQ}$ is active.
0	1	0	DBA BUS MODE is selected when the Am33C93A is connected to a DBA Bus. This mode also can be called Direct Buffer Access (DBA) mode. In this mode, the Am33C93A acts as a bus master, and all data access signals reverse their direction: The $\overline{DRQ}$ output signal becomes the DRQ input, which enables the Am33C93A to drive the buffer bus control signals. The $\overline{DACK}$ output signal becomes the $\overline{RCS}$ input, which is asserted as a chip select for the buffer. The $\overline{RE}$ and $\overline{WE}$ inputs become outputs which drive the read and write functions of the RAM buffer. As long as the DRQ signal is asserted, transfers will continue in a burst manner, until the transfer is complete or it decides to pause the transfer by negating the DRQ signal; one more transfer may occur after this transition, and then the $\overline{DACK}$, $\overline{RE}$, and $\overline{WE}$ signals are negated.
1	0	0	DMA MODE is selected when the Am33C93A is to be used with a DMA controller in single-byte transfer mode. In this mode, $\overline{DRQ}$ is asserted and then negated, and the DMA controller responds by asserting $\overline{DACK}$ and $\overline{WE}$ or $\overline{RE}$, for each data byte transferred to/from the Am33C93A.

TIMEOUT PERIOD REGISTER
(Address 02 Hex)

The TIMEOUT PERIOD register is an 8-bit register containing a preset value which determines the timeout period for Select and Reselect commands. This value may be calculated as a function of the input clock frequency and the desired timeout period, as shown in the following equation:

$$\text{register value} = \frac{\text{Tper} \cdot \text{Ficlk}}{80}$$

Where:

Tper = The desired timeout period in milliseconds;

Ficlk = The input clock frequency at the CLK pin in MHz (with no divisor applied).

The constant '80' scales the units of the equation, as is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the user's minimum timeout requirement is met.

The timeout period specifies how long the Am33C93A will wait for a response (indicated by assertion of the $\overline{BSY}$ signal) after it has begun the selection phase (assert $\overline{SEL}$ and negate $\overline{BSY}$) before terminating the command. The timeout function can be disabled by loading the TIMEOUT PERIOD register with zero.

NOTE: The following twelve registers are used exclusively by the Translate Address and/or "combination" commands. The function of each register is determined by the type of command issued.

TOTAL SECTORS REGISTER/CDB 1ST BYTE (Address 03 Hex)

Translate Address: The TOTAL SECTORS register should be set to the total number of sectors per track prior to issuing a Translate Address command.

Select-and-Transfer: This register should be loaded with the first byte of the COMMAND DESCRIPTOR BLOCK before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive: The Am33C93A will store the first byte of the received CDB in this register.

TOTAL HEADS REGISTER/CDB 2ND BYTE (Address 04 Hex)

Translate Address: This register holds the total number of heads during a Translate Address command.

Select-and-Transfer: This register should be loaded with the second byte of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive: The Am33C93A will store the second byte of the received CDB in this register.

TOTAL CYLINDERS REGISTER/CDB 3RD AND 4TH BYTES (Address 05, 06 Hex)

Translate Address: This is a 16-bit register which holds the total number of cylinders.

Select-and-Transfer: This register should be loaded with the third and fourth bytes of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive: The Am33C93A will store the third and fourth bytes of the received CDB in this register.

LOGICAL ADDRESS REGISTER/CDB 5TH–8TH BYTES (Address 06, 07, 08, 09, 0A Hex)

Translate Address: The LOGICAL ADDRESS register is a 32-bit register which should be loaded with the logical address to be translated prior to issuing the Translate Address command.

Select-and-Transfer: For six byte CDBs, only the first two bytes of this register are loaded with the fifth and sixth bytes of the CDB. For ten and twelve byte CDBs, this register is loaded with the fifth, sixth, seventh, and eighth bytes of the CDB.

Wait-for-Select-and-Receive: The Am33C93A will store the fifth, sixth, seventh (if any), and eighth (if any) bytes of the received CDB in this register.

SECTOR NUMBER REGISTER/CDB 9TH BYTE (Address 0B Hex)

Translate Address: This register will contain the resulting sector number following a Translate Address command.

Select-and-Transfer: This register should be loaded with the ninth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive: The Am33C93A will store the ninth byte of a ten or twelve byte received CDB in this register.

HEAD NUMBER REGISTER/CDB 10TH BYTE (Address 0C Hex)

Translate Address: The HEAD NUMBER register contains the resulting head number following a Translate Address command. If automatic compensation for spare sectors on a disk is to be performed by the Am33C93A, then the number of spare sectors per cylinder must be written into this register before issuing the Translate Address command. It should be noted that when compensation is used, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15. An initial value of zero in this register indicates that no compensation is to be performed.

Select-and-Transfer: This register should be loaded with the tenth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive: The Am33C93A will store the tenth byte of a ten or twelve byte received CDB in this register.

CYLINDER NUMBER REGISTER/CDB 11TH AND 12TH BYTES (Address 0D, 0E Hex)

Translate Address: The CYLINDER NUMBER register is a 16-bit register which contains the resulting cylinder number following execution of the Translate Address command. When a Translate Address command involving automatic compensation for spare sectors is issued (i.e. the HEAD NUMBER register initially contains a nonzero value), then this register must be loaded with total number of sectors per cylinder (total sectors/track • total heads – total spare sectors/cyl) before issuing the command.

Select-and-Transfer: This register should be loaded with the eleventh and twelfth bytes of a twelve byte CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive: The Am33C93A will store the eleventh and twelfth bytes of a twelve byte received CDB in this register.

Send-Status-and-Command-Complete: The CDB11 register is used to specify the returned status byte to be sent during a Send-Status-and-Command-Complete command. The CDB12 register is used to determine the type of Command-Complete message sent by the Am33C93A. If bit 0 of the CDB12 register is set to one,

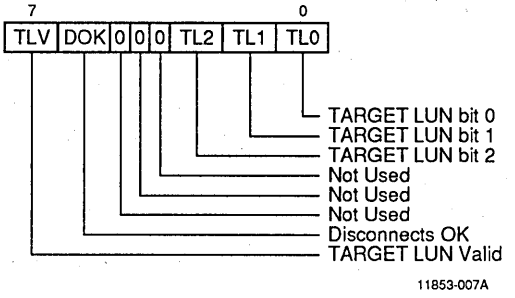
then a linked Command Complete message will be sent during command execution. In this case, bit 1 of the CDB12 register is used as a FLAG bit to determine whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) Linked Command Complete message is sent. If bit 0 is zero, then a simple Command Complete message (00 hex) is sent.

TARGET LUN REGISTER (Address 0F Hex)

The TARGET LUN register is used to hold both the Logical Unit Number (LUN) and Target status information during various Am33C93A commands and sequences. During a Select-and-Transfer or Reselect-and-Transfer command, the contents of this register (along with the SOURCE ID register) are used to generate and check the IDENTIFY messages transferred across the SCSI bus. In addition, the TARGET LUN register is used to hold the Target Status byte received during a Select-and-Transfer command.

During Wait-for-Select-and-Receive commands, this register may hold the image of the Identify message received from the Initiator. If the TLV bit is zero, there was no Identify message received. If the TLV bit is one, then a valid Identify message was received. The DOK bit will then indicate whether of not the Initiator has enabled disconnects.

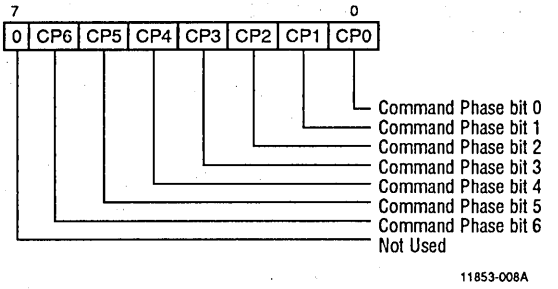
During Reselect-and-Transfer commands, this register is used to set the LUN to be used in the Identify message sent to the Initiator after Selection phase. The TLV and DOK bits are not used.



In advanced mode, during Select-and-Transfer commands, this register is used to handle reselection by an unexpected Target. In this case, this register will hold the logical unit number of the reselecting target. The TLV and DOK bits will be zero.

COMMAND PHASE REGISTER (Address 10 Hex)

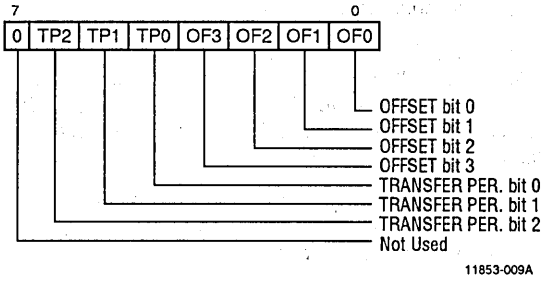
The COMMAND PHASE register is used during combination commands to indicate which phases of these



multi-phase commands have been completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and how to respond to it. This register is also used to resume combination commands by loading this register with a value that indicates the next desired or expected bus phase, and reissuing the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

SYNCHRONOUS TRANSFER REGISTER (Address 11 Hex)

The SYNCHRONOUS TRANSFER register is used to select between synchronous and asynchronous transfers, and is also used to define the maximum transfer rate. For information phases other than a "data" transfer phase, or when the selected offset is zero (OF3=OF2=OF1=OF0=0), asynchronous transfers will occur. Values greater than zero define a synchronous transfer mode and the offset is determined as shown below. This offset determines the effective FIFO depth for synchronous data transfers, and is typically determined by negotiation with the other SCSI device (as defined in the SCSI standard). The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI transfers and, if DBA Bus mode is used, the transfer period and the width of the $\overline{RE}/\overline{WE}$ strobes for host transfers. The period is defined in terms of the internal clock cycle time; the frequency of this clock is determined by the divisor selected in the OWN ID register.



Bit	Name	Description

0–3 OFx

The OFFSET bits are used to select the desired offset according to the following:

3	2	1	0	Selected Offset
0	0	0	0	0 (=Asynchronous data phase transfers)
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	X	Undefined

4–6 TPx

The TRANSFER PERIOD bits are used to select the desired transfer period according to the following table:

SCSI 6	SCSI 5	SCSI 4	DBA Bus Transfer Period	(SCSI REQ/ACK Synchronous Pulse Width and DBA Bus RE/WE Pulse Width)
0	0	X	8 cycles	(4 cycles)
0	1	0	2 "	(1 ")
0	1	1	3 "	(1 ")
1	0	0	4 "	(2 ")
1	0	1	5 "	(3 ")
1	1	0	6 "	(4 ")
1	1	1	7 "	(4 ")

The 'cycle' referred to above is the period of the internal data transfer clock after the divisor chosen in the OWN ID register is applied. This period is calculated by the following formula:

$$\text{CYCLE} = \frac{\text{DIVISOR (from OWN ID)}}{2 \cdot \text{INPUT CLOCK FREQUENCY (MHz)}} \text{ (µsec)}$$

TRANSFER COUNT REGISTER
(Address 12, 13, 14 Hex)

The TRANSFER COUNT register is a 24-bit register containing a preset value for the internal transfer counter. This preset value is loaded into the internal transfer counter when a Send, Receive, or Transfer command is issued. This counter is used to define command completion by decrementing as each data byte is transferred over the SCSI bus and causing a "successful completion" interrupt when the counter reaches zero. In Combination commands, this register specifies the number of bytes to be transferred during a Data phase.

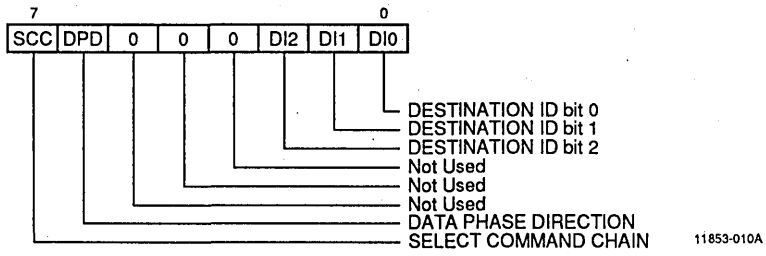
The counter function can be disabled by loading the TRANSFER COUNT register with zeros prior to issuing a command or by setting the SINGLE-BYTE TRANSFER bit in the COMMAND register concurrent with issuing the command. If the counter is disabled, the Send, Receive, or Transfer command will be completed when a single byte has been transferred.

After the completion of any successful transfer, the TRANSFER COUNT register will be zero. This includes commands issued in Single Byte Transfer mode.

When a transfer is interrupted by a halt on error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred to/from the SCSI bus, including any bytes left in the FIFO (see DATA register). This FIFO clearing process may cause the TRANSFER COUNT register to differ with the user's DMA controller count, because some bytes may have been transferred into the FIFO, but not to the SCSI bus; therefore, the TRANSFER COUNT should be used to determine the actual number of bytes transferred to/from the SCSI bus.

DESTINATION ID REGISTER
(Address 15 Hex)

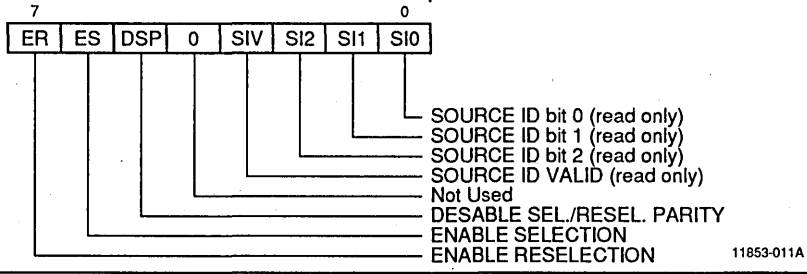
The DESTINATION ID register contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or Select command is issued. This register also contains control bits that affect the operation of certain combination commands.



Bit	Name	Description
6	DPD	DATA PHASE DIRECTION, when advanced features are enabled (see p.14), is used to specify the expected direction of the SCSI data phase, when it occurs. This allows the Am33C93A to verify the direction during Select-and-Transfer commands before beginning the transfer. When this bit is zero, the expected direction is out (to the Target). When this bit is one, the expected direction is in (from the Target). An unexpected information phase error will occur if the direction does not match the setting of this bit.
7	SCC	SELECT COMMAND CHAIN is used only when the Reselect-and-Transfer command is issued with EDI=1. This bit selects which command is chained to when the data transfer is completed. When this bit is zero, a Send-Status-and-Command-Complete command begins executing. When this bit is one, a Send-Disconnect-Message command begins executing.

SOURCE ID REGISTER
(Address 16 Hex)

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the Am33C93A. It also contains bits that enable and control response to selection and reselection.



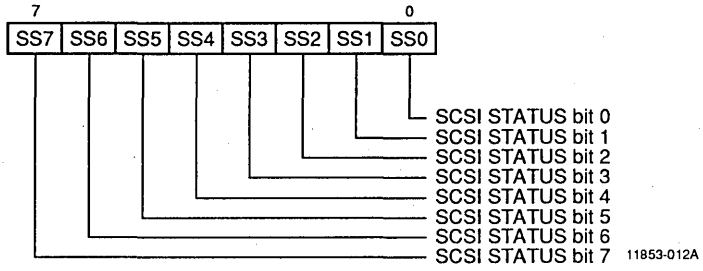
Bit	Name	Description
7	ER	ENABLE RESELECTION, when set to one, enables the Am33C93A to respond to a reselection by another device on the SCSI bus. When this bit is zero, any reselection is ignored.
6	ES	ENABLE SELECTION, when set to one, enables the Am33C93A to respond to a selection by another device on the SCSI bus. When this bit is zero, any selection is ignored.
5	DSP	DISABLE SELECT PARITY, when set to one, causes the Am33C93A to ignore the bus parity when responding to selection or reselection. When this bit is zero, any selection or reselection with a parity error is ignored.
3	SIV	SOURCE ID VALID is set to one after the Am33C93A is selected or reselected if the other SCSI bus device asserted its own bus ID bit (in addition to the bus ID bit of the Am33C93A) during the select/reselect phase. This bit is zero if only the bus ID bit of the Am33C93A was asserted.
2–0	SIx	SOURCE ID Bits 2–0 are valid only if the SIV bit is set to one. These bits indicate the SCSI bus ID of the device that selected or reselected the Am33C93A.

SCSI STATUS REGISTER (Address 17 Hex)

The SCSI STATUS register is a read-only register which indicated the cause of the most recent INTRQ assertion. INTRQ is asserted whenever a condition occurs within the Am33C93A that requires intervention by the host; for example:

- The Am33C93A has been reset;
- The command completed successfully;
- The bus phase changed;
- An error occurred.

Once INTRQ has been asserted, the contents of this register will not change until after the SCSI STATUS register has been read or until the Am33C93A has been reset.



Bit	Name	Description
0-3	SSx	SCSI STATUS bits 0-3 are status qualifiers whose meaning depends upon which upper (4–7) status bit is set.
4–7	SSx	SCSI STATUS bits 4–7 define the type of interrupt that occurred. The possible codes are defined in the following table:

Status	Code	Group Meaning
0000	xxxx	The Am33C93A is in a reset state.
0001	xxxx	A Am33C93A command has completed successfully.
0010	xxxx	A Am33C93A command has paused or was aborted by an Abort command.
0100	xxxx	A Am33C93A command has been terminated prematurely due to an error or other unexpected condition.
1000	xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the current state in which the Status Code can occur. Also, the MCI field refers to the signals that define a SCSI bus information transfer phase: MSG, $\overline{C}$/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus. A zero indicates negation. Whenever one of these Status Codes occurs, the $\overline{REQ}$ signal is asserted on the SCSI bus. The table below summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

Reset State Interrupts

Status	Code	State*	Specific Meaning
0000	0000	DTI	Am33C9A3 Reset. The device has been reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the Am33C93A is disconnected.
0000	0001	DTI	Am33C93A Reset. The device has successfully completed a Reset command with advanced features enabled. The new state of the Am33C93A is disconnected.

Successful Completion Interrupts

Status	Code	State*	Specific Meaning
0001	0000	D	A Reselect command completed successfully. The new state of the Am33C93A is connected as a Target.
0001	0001	D	A Select command completed successfully. The new state of the Am33C93A is connected as an Initiator.
0001	0010	—	Reserved for future use.
0001	0011	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect- Message command completed successfully ($\overline{ATN}$ is not asserted).
0001	0100	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully ($\overline{ATN}$ is asserted).
0001	0101	DT	A Translate Address command completed successfully.
0001	0110	DI	A Select-and-Transfer command completed successfully.
0001	0111	—	Reserved for future use.
0001	1MCI	I	A Transfer (non-MESSAGE IN phase) command completed successfully. MCI defines the new information type (SCSI bus phase) being requested.

Paused or Aborted Interrupts

Status	Code	State*	Specific Meaning
0010	0000	I	A Transfer Info (MESSAGE-IN phase) command has paused with $\overline{ACK}$ asserted. This allows the host to examine the message before accepting it.
0010	0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010	0010	D	A Select or Reselect command was aborted.
0010	0011	T	A Receive or Send command has halted by an error or was aborted ($\overline{ATN}$ is not asserted).
0010	0100	T	A Receive or Send command has halted by an error or by assertion of $\overline{ATN}$ or was aborted ($\overline{ATN}$ is asserted).
0010	0101	—	Reserved for future use.
0010	0110	—	Reserved for future use.
0010	0111	D	The Am33C93A has been reselected during a Select-and-Transfer (with IDI=0) by a Target that does not match the SCSI bus ID loaded into the DESTINATION ID register or the following Identify message did not match the LUN loaded into the TARGET LUN register. $\overline{ACK}$ has been left asserted following the Identify message, and the bus ID and LUN of the reselecting Target are available in the SOURCE ID and TARGET LUN registers.
0010	1MCI	I	A Transfer command was aborted. MCI define the new information type (SCSI bus phase) being requested.

** D = Disconnected*
T = Connected as a Target
I = Connected as an Initiator

Terminated Interrupts

Status	Code	State*	Specific Meaning
0100	0000	DTI	An invalid command was issued.
0100	0001	I	An unexpected disconnect (SCSI bus free) by the Target caused a command to terminate. The new state of the Am33C93A is disconnected.
0100	0010	D	A timeout occurred during a Select or Reselect command. The state of the Am33C93A is disconnected.
0100	0011	TI	A parity error caused a command to terminate ($\overline{ATN}$ is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0100	TI	A parity error caused a command to terminate ($\overline{ATN}$ is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100	0101	DT	The Logical Address exceeded the disk boundaries.
0100	0110	D	A Target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the Am33C93A during a Select-and-Transfer command (with IDI=0). This interrupt occurs when the Am33C93A is not in Advanced Mode. The new state of the Am33C93A is connected as an Initiator.
0100	0111	I	An incorrect status byte was received during a Select-and-Transfer command.
0100	1MCI	I	An unexpected information phase was requested. MCI define the SCSI bus phase which is requested. This is typically caused by a phase change before the Transfer Count has reached zero or by an unexpected phase sequence occurring during a Select-and- Transfer command.

Service Required Interrupts

Status	Code	State*	Specific Meaning
1000	0000	D	The Am33C93A has been reselected. The new state of the Am33C93A is connected as an Initiator. No Identify message transfer has yet occurred.
1000	0001	D	The Am33C93A has been reselected in Advanced Mode. The SCSI bus ID of the Target may be read from the SOURCE ID register. The Identify message from the Target may be read from the DATA register. The $\overline{ACK}$ signal is left asserted. The new state of the Am33C93A is connected as an Initiator.
1000	0010	D	The Am33C93A has been selected ($\overline{ATN}$ was not asserted). The new state of the Am33C93A is connected as a Target.
1000	0011	D	The Am33C93A has been selected ($\overline{ATN}$ was asserted). The new state of the Am33C93A is connected as a Target.
1000	0100	T	The $\overline{ATN}$ signal has been asserted.
1000	0101	I	A disconnect has occurred. The new state of the Am33C93A is disconnected.
1000	0110	—	Reserved for future use.
1000	0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not a known command group. The OWN ID register must be loaded with the CDB length, and the command resumed. The CDB1 register may be examined to determine the SCSI command group from the opcode. The new state of the Am33C93A is connected as a Target. (Advanced Mode only)
1000	1MCI	I	The REQ signal has been asserted following connection or when the Am33C93A is in the Initiator state and no command is executing. The information phase type should be examined. MCI define the information phase (SCSI bus phase) which is being requested.

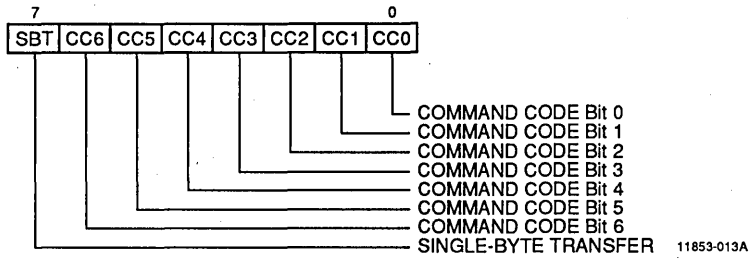
** D = Disconnected*
T = Connected as a Target
I = Connected as an Initiator

COMMAND REGISTER
(Address 18 Hex)

The COMMAND register is used to issue the AM33C93A commands. This register should never be loaded when the CIP or INT bits (in AUXILIARYSTATUS) are set to one, and a Level II command should never be loaded when the BSY bit is set to one.

The SINGLE-BYTE TRANSFER (SBT) bit in the COMMAND register is only used during information transfer type commands. When this bit is set in conjunction with one of these commands, the transfer counter is disabled and exactly one byte is to be transferred, regardless of the value in the TRANSFER COUNT register. The previous contents of the TRANSFER COUNT register are not preserved.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.



DATA REGISTER
(Address 19 Hex)

The DATA register is used to transfer data bytes between the host and the SCSI bus during the SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the processor during any type of information phase (simple Level II commands) or via the DMA/DBA Bus interface during a SCSI Data In phase or Data Out phase (simple and combination Level II commands).

The DATA register is actually a port for the host interface into the internal twelve byte FIFO of the Am33C93A. The FIFO is used for all transfers (synchronous and asynchronous) between the SCSI bus and the host bus, for both DMA and processor access transfers. If the Am33C93A is to be halted for any reason (through ABORT, for example), then data transfers with this FIFO must continue until an interrupt occurs. This must be done so that the FIFO is returned to a ready state for subsequent transfers, and to flush incoming data to the host bus.

The DATA register is accessed by the processor during a data phase when the CONTROL register DMA mode select bits are all reset (=0), and when the DBR bit in the AUXILIARY STATUS register is true. The processor writes (reads) the DATA register by loading the ADDRESS register with a hex value of 19 and asserting the $\overline{WE}$ ($\overline{RE}$) and $\overline{CS}$ pins. This access also occurs during non-data phases.

When the CONTROL register DMA mode select bits are set for DMA mode or BURST mode, the DMA interface is enabled. In this case, the DATA register is written (read) when the $\overline{DACK}$ and $\overline{WE}$ ($\overline{RE}$) pins are asserted in response to the assertion by the Am33C93A of the $\overline{DRQ}$ pin. When the DBA Bus is selected by the DMA mode select bits, the $\overline{RCS}$ pin functions as an external buffer chip select and the $\overline{WE}$ and $\overline{RE}$ pins become outputs, allowing the Am33C93A to automatically transfer data between its DATA register and the external buffer. In this mode, bus control can be returned to the external processor or any other device by negating the DRQ pin.

Reset Conditions

HARDWARE RESET

The following results occur when the Am33C93A is reset by the assertion of the $\overline{MR}$ signal:

- The AUXILIARY STATUS register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The OWN ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.
- The following host accessible registers are NOT affected by the $\overline{MR}$ signal:
- Registers 01 hex through 15 hex;
- SOURCE ID (16 hex) register bits 0-3;
- COMMAND register (18 hex);

Note: The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to cause a reset of the Am33C93A (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the $\overline{MR}$ signal to recover from the SCSI reset condition.

SOFTWARE RESET

The following results occur when the Am33C93A executes the Software Reset command:

- The DBR bit in the AUXILIARY STATUS register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The OWN ID register is interpreted and the clock divisor, host parity, and advanced mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set as commanded by the EAF bit in the OWN ID register.

COMMANDS

Command List

Command Code (HEX)	Valid Command	States	Level
00	Reset	D,T,I	I
01	Abort	D,T,I	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T,I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-$\overline{\text{ATN}}$ and-Transfer	D,I	II
09	Select-without-$\overline{\text{ATN}}$ and-Transfer	D,I	II
0A	Reselect-and-Receive-Data	D,T	II
0B	Reselect-and-Send-Data	D,T	II
0C	Wait-for-Select-and-Receive	D,T	II
0D	Send-Status-and-Command-Complete	T,I	I
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D,T,I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D,T	II
20	Transfer Info	I	II

Am33C93A states:
D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

Command Levels:
I = Level I command
II = Level II command

Am33C93A Command Types

There are two basic types of Am33C93A commands: Level I and Level II. Level I commands may be issued while a Level II command is in progress (indicated by an AUXILIARY STATUS of BSY=1,CIP=0) and, except for the "Abort" and "Reset" commands, do not generate an interrupt upon their completion. Level II command execution will always result in an interrupt. If a Level II command is issued while another Level II command is executing, unpredictable results may occur.

There are two types of Level II commands. 'Simple' Level II commands are associated with a single operation or phase (for example, selection or information transfer). 'Combination' Level II commands combine multiple phases into a single Am33C93A command to minimize interrupt overhead. The Initiator combination commands 'expect' certain SCSI bus phases at certain times during a sequence. These expected phases are based on common sequences performed by a Target on the SCSI bus; any deviation causes an interrupt. Target combination commands can be chained together to further minimize interrupt overhead by creating longer phase sequences.

NOTE: When using command chaining, care must be taken to ensure that all commands in the chain are initialized prior to issuing the command.

The Am33C93A will be in one of three "states" during operation: Disconnected, Connected as a Target, or Connected as an Initiator. Certain commands are valid only in particular states as indicated in the COMMAND LIST. An attempt to issue a Level II command which is invalid for the present Am33C93A state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

Advanced Mode Features

The Am33C93A has several new features included which add new functions to the original 33C93 design. Some of these features cause the Am33C93A to be incompatible with the 33C93. These features have been grouped together under the heading of 'Advanced Mode' features. These features are disabled when the Am33C93A is reset by the $\overline{MR}$ signal (hardware reset). They must be enabled by the host by issuing the 'Reset' command with the 'Enable Advanced Features' (EAR) bit set in the OWN ID register. The host can determine if advanced features have been enabled (thereby implying that a Am33C93A is installed) by examining the SCSI STATUS register after issuing the 'Reset' command.

The features enabled by this bit are described below.

UNEXPECTED RESELECTION

When in normal (33C93) mode, a reselection when idle (ER=1) or when disconnected during a Select-and-Transfer command (and the Target bus ID does not match the DESTINATION ID register) causes an immediate interrupt after the reselection handshake is complete. In Advanced Mode, the Am33C93A will continue to the Message In phase to fetch the Identify message. If the Am33C93A was idle, the SCSI STATUS register will be set to 81 hex, and the Identify message will be in the DATA register. If the Am33C93A was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the Identify message will be in the TARGET LUN register. In either case, the SOURCE ID register will contain the SCSI bus ID of the reselecting Target, and the ACK signal remains asserted so that the Identify message may be rejected.

UNKNOWN SCSI COMMAND GROUPS

When a SCSI Command Descriptor Block is transferred on the SCSI bus, the command length in bytes is determined by the group code, which is found in bits 7–5 of the first command byte, or opcode. Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands are defined by the SCSI standard (X3.131-1986) as six, ten, and twelve byte commands, respectively. All other command groups are undefined by that standard. In normal mode, the Am33C93A will assume that these undefined groups are six byte commands when executing Select-and-Transfer or Wait-for-Select-and-Receive commands. In Advanced Mode, the following events will occur:

Select-and-Transfer: When loading the CDB into the CDB registers prior to issuing the command, the host also loads the expected command length into the OWN ID register. The Am33C93A uses this value to make sure the correct number of bytes are then transferred in the command phase.

Wait-for-Select-and-Receive: When receiving the CDB from the Initiator, the Am33C93A will check the first CDB byte as soon as it is received. If the group is undefined, an interrupt will occur so that the host can examine the first command byte in the CDB 1ST register, and then load the TOTAL command length into the OWN ID register. The SCSI STATUS register is set to 87 hex, and the COMMAND PHASE register is set to 31 hex, when this interrupt occurs.

After the interrupt, the Am33C93A will only accept a Resume Wait-for-Select-and-Receive command, Abort, Disconnect, or Reset command. All other commands are invalid; during the interrupt processing, the Am33C93A will continue to transfer the first six bytes of the command into its internal FIFO.

DATA PHASE DIRECTION

During a Select-and-Transfer command in normal mode, the Data phase direction is determined solely by the Target; if this direction does not match the direction expected by the host, the Am33C93A will not detect this error but expects that the transfer will continue. In

Advanced Mode, the DPD bit in the DESTINATION ID register is compared with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with 'unexpected phase' status in the SCSI STATUS register.

Level I Commands

RESET (00 HEX)

The Reset command performs a similar function to the hardware reset caused by asserting the $\overline{MR}$ pin except that the OWN ID register is sampled for information concerning the operating configuration of the Am33C93A. The Am33C93A is also initialized as described in theRESET CONDITIONS section. The Reset command may be executed in any Am33C93A state and will force the Am33C93A into the Disconnected state, aborting any previously issued command in progress. Upon completion of the Reset command, an interrupt is generated the SCSI STATUS will be 00 hex or 01 hex, depending on the contents of the OWN ID register.

ABORT (01 HEX)

The Abort command is valid in the Disconnected and Connected-as-a-Target states.The Abort command has different effects depending on the state and the command that is currently executing, as described below:

Disconnected State: In the Disconnected state, the Abort command may be used to halt an attempted Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command. If the Abort command is issued following a Select or Reselect command and the Am33C93A has won arbitration, the Am33C93A releases the SCSI bus by removing the Bus ID bits while $\overline{SEL}$ is asserted and checking for a negated $\overline{BSY}$ signal. If after at least 200 µs, there is no $\overline{BSY}$ response, the Am33C93A goes to a Bus Free condition and generates a "paused/aborted" interrupt. If there is a response within this time period, then a "successful completion" interrupt will result instead. If the Am33C93A has not yet won arbitration, it immediately aborts the Select or Reselect command.

Target State: When the Am33C93A is in a Connected-as-a-Target state, the Abort command may be used to abort Receive, Send, or the data phase portion of a Target combination command. When issuing an Abort in the Connected-as-a-Target state, the following rules apply:

1. When a Abort command is issued to abort a Send or Reselect-and-Send command, the local processor must not service any data request (DBR, DRQ, etc.) from the Am33C93A until an interrupt from the Am33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the SCSI bus. The Am33C93A removes the data request at an arbitrary time during the Abort command processing and the data request is not valid once the Abort command is written to the COMMAND register.
2. When a Abort command is issued to abort a Receive or Reselect-and-Receive command, the local processor must CONTINUE to service any data request (DBR, DRQ, etc.) from the Am33C93A until an interrupt from the Am33C93A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the local processor.

After the Abort command is processed and the local processor has received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The Am33C93A remains in the Connected-as-a-Target state. The Am33C93A is now ready to receive any appropriate Target mode command, including a resume of the command that was aborted.

DISCONNECT (04 HEX)

The Disconnect command may be used in either the Target or the Initiator connected states. In the Target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the Initiator role, Disconnect can be used to release the bus following a timeout condition. The Disconnect command causes the immediate release of all bus signals and, in Target mode, returns the SCSI bus to the Bus Free phase. If the Disconnect command is issued during an active Level II command, the Level II command is immediately terminated and the Am33C93A transitions to the Disconnected state.

ASSERT ATN (02 HEX)

The Assert ATN command is only valid when Connected as an Initiator. It is normally used to allow the Initiator to inform a Target that it has a message pending (The Target is expected to respond by performing a Message Out Phase).

$\overline{ATN}$ is automatically negated:

- Before the last byte of a Transfer Info command issued in response to the Message Out phase;
- When the Identify message out is transferred to the Target during a Select-and-Transfer command;
- When a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the Am33C93A to automatically assert $\overline{ATN}$ prior to the release of $\overline{SEL}$ providing the bus arbitration is won.

NEGATE ACK (03 HEX)
The Negate ACK command causes $\overline{ACK}$ to be negated. It may be used in the following situations:

- after successful completion of a Message-In Transfer Info commands;
- after the Am33C93A has detected a parity error on any received SCSI information and the HALT on SCSI PARITY ERROR (HSP) bit is set;
- after unexpected reselection in advanced mode; and
- after a save-data-pointer message is received during a select-and-transfer command.

Host parity errors do not affect the $\overline{ACK}$ signal. For all other Initiator transfers, $\overline{ACK}$ negation is automatic.

In the case of a Message-In transfer, incoming messages may be rejected and the Initiator may indicate its intent to send either a "MESSAGE REJECT" or a "MESSAGE PARITY ERROR" Message by issuing the Assert ATN command prior to issuing the Negate Ack command. If the incoming message is to be accepted, only the Negate Ack command should be issued.

During non-Message-In transfers, if the Transfer command is terminated by a parity error, the Assert ATN command can again be issued prior to Negate ACK, this time indicating the Initiator's intent to send an "INITIATOR DETECTED ERROR" Message.

SET IDI (0F HEX)
The Set IDI command is used in the Initiator role to support overlapped SCSI operations. If a SCSI command is executing via a Select-and-Transfer command, then the Set IDI command may be used to set the IDI bit in the CONTROL register, which then causes an interrupt to occur upon a Target disconnection. This ability allows the IDI bit to be left reset when the first SCSI operation is started, which may reduce the number of Am33C93A interrupts, yet also allows a second operation to be started when needed without waiting for the first operation to be completed.

Simple Level II Commands

SELECT-WITH-ATN (06 HEX)
Select-with-ATN is valid only in the Disconnected state and when issued will cause the Am33C93A to select a Target. Before issuing this command, the SCSI Bus ID of the Target device should be written into the DESTINATION ID register. When the Select- with-ATN command is issued, the Am33C93A begins bus arbitration. If the Am33C93A is selected or reselected by another device during the arbitration, the Select-with-ATN command is aborted and a "service required" interrupt (8x hex) is generated.

Should the Am33C93A win the arbitration, $\overline{SEL}$ and $\overline{ATN}$ are asserted, the Target and Initiator Bus IDs are placed on the SCSI data bus, and then $\overline{BSY}$ is deasserted. At this time, a timeout sequence whose length is determined by the value in the TIMEOUT PERIOD register begins. If $\overline{BSY}$ is not asserted by the Target before a timeout occurs, the Am33C93A begins its selection abort sequence (as described in the Abort command description), and if there is no Target response the Select- with-ATN command is terminated and a "terminated" interrupt is generated. If the Target responds before the timeout period has elapsed or before the selection abort sequence is complete, the Am33C93A negates the $\overline{SEL}$ signal, putting the Am33C93A in a Connected-as-an-Initiator state. A "successful completion" interrupt indicates that the Select-with-ATN command has been completed successfully.

If the Am33C93A does not win the arbitration or there is no response from the Target and the timeout feature is disabled, the Select-with-ATN command can be aborted with an Abort command. When the Abort command is successfully executed under these circumstances, the Am33C93A is disconnected from the bus and a "paused/aborted" interrupt is generated.

SELECT-WITHOUT-ATN (07 HEX)
The Select-without-ATN command is identical to the Select-with-ATN command except that $\overline{ATN}$ is not set during the Selection Phase.

RESELECT (05 HEX)
The Reselect command is identical to the Select-without-ATN command except that the I/O signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the Am33C93A being Connected as a Target.

RECEIVE (10-13 HEX)
There are four Receive commands which are distinguished from each other only by the state of three SCSI interface signals and the type of data that is transferred. These commands, consisting of the Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out commands are valid only in the Connected-as-a-Target state. The type of the Receive command selected determines the state of the $\overline{I/O}$, C/$\overline{D}$, and $\overline{MSG}$ outputs during the command according to the following chart (1=asserted):

The Receive commands are information transferring commands and are therefore dependent on the SBT bit in the COMMAND register for determination of a suc-

Receive Command Type	OPCODE	MSG	C/D	I/O
Receive Command	10	0	1	0
Receive Data	11	0	0	0
Receive Message Out	12	1	1	0
Receive Unspecified Info Out	13	1	0	0

cessful completion. In addition to a termination caused by reset (via either a Reset command being issued or assertion of the $\overline{MR}$ pin), a Receive command completion or termination will occur under any of these conditions: (1) The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register; (2) The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred; (3) A parity error has been detected on one of the received data bytes (and HSP=1); (4) The $\overline{ATN}$ pin is asserted (and HA=1); (5) The Abort command is issued; or (6) A Disconnect command is issued.

When the Receive command is completed as a result of receiving the correct number of bytes, a "successful completion" interrupt will be generated. If a parity error has caused termination, a "terminated" interrupt will instead be generated. In this case, the TRANSFER COUNT register will contain the number of bytes yet to be transferred. After any completion or termination of the Receive commands except those due to a subsequent Disconnect command or reset, the Am33C93A is in the Connected-as-a-Target state.

As data transfer commands, the Receive commands are dependent on the DMA mode select bits in the CONTROL register for the DATA register accessing mode. These bits determine whether the DATA register accesses will be handled by the processor or through a DMA/Am interface. When the processor is required to read the DATA register (i.e. DMA mode select bits=0), it must monitor the DBR status bit (in AUXILIARY STATUS) to determine when a byte is available for reading. During Receive commands, this status bit will be reset when a byte is read from the DATA register and set when a byte is loaded into the DATA register via the SCSI interface. DBR is also reset when a Receive command is issued.

All information transfers involving other than data information are asynchronous. However, if the information phase involves data transfers, the SYNCHRONOUS TRANSFER register will be evaluated. In this case, any selected offset other than zero results in synchronous transfers. The minimum Transfer Period for both types of transfers is determined by the transfer period bits in this same register.

SEND (14-17 HEX)

As in the case of the Receive commands, there are four Send commands which are distinguished only by the state of the $\overline{I/O}$, $\overline{C}$/D, and $\overline{MSG}$ pins and the type of data that is transferred. The four Send commands, also valid in the Connected-as-a-Target state only, are the Send Status, Send Data, Send Message In, and Send Unspecified Info In commands. The SCSI pin states during the Send commands are determined by the particular command as follows (asserted=1):

Send Command Type	OPCODE	MSG	C/D	I/O
Send Status	14	0	1	1
Send Data	15	0	0	1
Send Message In	16	1	1	1
Send Unspecified Info In	17	1	0	1

The Send commands are also information transferring commands and as such are also dependent upon the SBT bit in the COMMAND register for command completion. In addition to that caused by reset (via either a Reset command being issued or assertion of the $\overline{MR}$ pin), a Send command completion or termination will occur under any of these conditions: (1) The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register; (2) The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred; (3) A parity error has been detected on one of the data bytes from the host (and HHP=1); (4) The $\overline{ATN}$ pin is asserted (and HA=1); (5) The Abort command is issued; or (6) A Disconnect command is issued. The Am33C93A remains Connected-as-a-Target following the Send command completion/termination unless the Disconnect command or reset was used to force a termination.

During a Send command, DATA register accessing is controlled by the DMA mode select bits in the CONTROL register. When these bits are set to the appropriate mode, loading of the DATA register is accomplished by a DMA controller or through the DBA Bus interface. If the DMA mode select bits are zero, the processor must poll the AUXILIARY STATUS register and can write to the DATA register only when the DATA BUFFER READY bit is set (DBR=1). Send commands cause the DBR bit to be reset every time the processor loads a byte into the DATA register and set when a byte is transferred from the DATA register onto the SCSI data bus. The DBR bit will also be set upon issuing a Send command.

As in the case of Receive commands, synchronous transfers will occur only when data transfers are involved and an offset other than zero is selected.

TRANSFER INFO (20 HEX)

The Transfer Info command is valid only when Connected as an Initiator and is used to send and receive data, command, status, and message information.

The first $\overline{REQ}$ assertion following connection as an Initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the Target, and then issue a Transfer Info command in response. While an Initiator, the Am33C93A will also generate an interrupt each time the Target device requests a new type of information transfer phase.

As in the case of the Send and Receive commands, when completion of the Transfer Info command depends upon the internal transfer counter, the processor should load the TRANSFER COUNT register prior to issuing this command. The DMA mode select bits in the CONTROL register, the offset and transfer period bits in the SYNCHRONOUS TRANSFER register, and the SBT bit in the COMMAND register are used during Transfer Info commands just as they are during the Send and Receive commands. However, for processor access of the DATA register during Transfer Info commands (when the DMA mode select bits are zero or the bus phase is other than Data phase), behavior of the DATA BUFFER READY (DBR) status bit is determined by the direction of information transfer as defined by the $\overline{I/O}$ pin. When the transfer is from Initiator to Target, the DBR bit is reset by writing to the DATA register and is set when the byte is transferred from the DATA register onto the SCSI data bus. When the transfer is from Target to Initiator, DBR is set when a byte is received over the SCSI data bus and transferred into the DATA register and is reset by reading the DATA register. DBR is also reset whenever a Transfer Info command is issued.

There are several causes of a Transfer Info command completion/termination in addition to a reset. Just as for a Send or Receive command, the Transfer Info command can be terminated by issuing a subsequent Disconnect or Abort command. The Abort command will cause a "paused/aborted" interrupt to be generated after execution (leaving the Am33C93A in a connected state), while the Disconnect command causes an immediate disconnect and does not generate an interrupt.

A Transfer Info command will either complete or pause when the specified number of bytes (either a single byte or multiple bytes as defined by the SINGLE-BYTE TRANSFER bit in the COMMAND register) has been sent or received. The Am33C93A generates a "successful completion" interrupt only after receiving another $\overline{REQ}$ from the Target during non-Message-In information phases but generates a "paused/aborted" interrupt for Message-In phases without waiting for an additional $\overline{REQ}$ (Note that when the completed Transfer Info command was a Message-In transfer phase, the $\overline{ACK}$ pin will be left asserted by the Am33C93A in the last REQ-ACK cycle of the command, and the processor is required to issue a Negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message).

If a parity error is detected on a data byte received from the SCSI bus (and HSP=1) or on a data byte byte received from the host (and HHP=1), then the Am33C93A will terminate the command and, for SCSI parity errors, will leave $\overline{ACK}$ asserted (to also halt the Target). In this case a "terminated" interrupt is generated. Finally, a negation of the $\overline{BSY}$ signal (i.e. the Target suddenly disconnects) or a transition in the $\overline{I/O}$, $\overline{C}$/D, and/or $\overline{MSG}$ pins during a Transfer command will also terminate the command and generate a "terminated" interrupt.

If a parity error is detected on a received byte but parity error command termination is disabled (HSP=0 or HHP=0, as appropriate), the Am33C93A will still set the PARITY ERROR status bit in the AUXILIARY STATUS register but will not terminate the command as a result of this error.

TRANSLATE ADDRESS (18 HEX)

The Translate Address Command performs a logical-address to physical-address translation. Certain SCSI commands involve a logical address which may be up to 32 bits in length. When a command is detected which requires address translation, the processor can reload the logical address into the Am33C93A LOGICAL ADDRESS register and then issue the Translate Address command to have the Am33C93A do the conversion. Upon receiving a "successful completion" interrupt, the processor can read the CYLINDER NUMBER, HEAD NUMBER, and SECTOR NUMBER registers to extract the logical address. The disk parameters contained in the TOTAL SECTORS, TOTAL HEADS, and TOTAL CYLINDERS registers must also be valid before issuing a Translate Address command.

If automatic compensation for spare sectors is to be performed by the Am33C93A, then the number of spare sectors per cylinder and total number of sectors per cylinder must also be loaded, respectively, into the HEAD NUMBER and CYLINDER NUMBER registers. A "terminated" interrupt will occur if any division operation performed during this command results in an overflow.

Combination Level II Commands

SELECT-AND-TRANSFER (08 AND 09 HEX)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the Am33C93A's internal microprocessor to manage the low-level SCSI protocol, resulting in as few as one interrupt per SCSI operation. Select-and-Transfer commands are used when in an Initiator role, and typically consist of at least the following SCSI phases: (1) Selection of a Target device; (2) Sending of a command; (3) Reception of status information; and (4) Reception of a COMMAND COMPLETE Message. These commands optionally consist of a Data Transfer phase and additional Message Transfer phases.

The Am33C93A will update the COMMAND PHASE register as the Select-and-Transfer command executes. Upon completion or termination of the command, the local processor can read this register to determine where the SCSI operation stopped.

The two Select-and-Transfer commands differ from each other only by whether or not the $\overline{ATN}$ pin is asserted during the Selection phase. The ability to assert

$\overline{ATN}$ during Selection supports the SCSI Message Protocol which calls for an IDENTIFY Message Out phase following the Selection. When executing a Select W/ATN-and-Transfer commands, the Am33C93A expects the Target to request a Message Out phase immediately following selection, whereas for a Select W/O ATN-and-Transfer command, it expects the Target to directly enter Command phase. The Select-and-Transfer commands, moreover, support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands.

When a Select-and-Transfer command is issued, the Am33C93A arbitrates for the bus and selects a Target just as during a Select command. If the Target does not respond before a timeout occurs, the Select-and-Transfer command halts and a "terminated" interrupt is generated. Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If the Selection is successful, no interrupt is generated, but the COMMAND PHASE register will be set to a hex 10.

After completing the Selection phase, the Am33C93A begins an information transfer phase. If $\overline{ATN}$ has been asserted (i.e. a Select W/ATN-and-Transfer command was issued), the Am33C93A expects the Target to respond with a Message Out phase. If the first information phase request is other than a Message Out request, the Am33C93A will terminate the command and generate a "terminated" interrupt. However, when the Target does request a Message Out phase, the Am33C93A will respond by automatically sending an IDENTIFY Message. This single byte message is of the binary form: 1r000ttt, where r=1 if the ENABLE RESELECTION bit in the SOURCE ID register is equal to 1, and ttt is the encoded Target LOGICAL UNIT NUMBER contained in the TARGET LUN register. Once the IDENTIFY Message has been sent, the Am33C93A will set the COMMAND PHASE register to hex 20.

Following the Message Out phase (or Selection phase when $\overline{ATN}$ was not asserted during Selection), a Command phase is expected by the Am33C93A. Again, and throughout the entire Select-and-Transfer command execution, if the Target requests an unexpected information phase type, the Am33C93A terminates the command and generates a "terminated" interrupt. If the Command phase is requested in this situation, the Am33C93A will extract the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and send the 6-, 10-, or 12-bytes of command information as determined by its evaluation of the SCSI command code in the CDB1 register. The COMMAND PHASE register is set to hex 30 before the first Command byte is sent and then increments with each byte transferred, so that for a 12-byte CDB command the COMMAND PHASE register will contain hex 3C when all bytes of the CDB have been transferred.

After the Command phase, the Am33C93A expects either a Data In phase, Data Out phase, Status phase, or Message In phase. If the Target is requesting a Message In phase, a pending disconnection is assumed. The Am33C93A therefore expects to receive either a Save-Data-Pointer message (hex 02) or a Disconnect message (hex 04). If either message is incorrect, or if a different message is received, a "terminated" interrupt will be generated to alert the processor of that fact and to allow the message to be read from the DATA register. A "terminated" interrupt will also be generated if the Target disconnects before sending the Disconnect message. When a correct Save-Data-Pointer message is received, a "paused/aborted" interrupt is generated and the Select-and-Transfer command terminated to allow the processor to save the SCSI data pointer. However, if a Disconnect message is received, the COMMAND PHASE register will be updated to hex 42 and command execution continues.

When the actual Target-disconnection does occur, the COMMAND PHASE register is updated to hex 43 and if the IDI bit is set, the Am33C93A terminates the Select-and-Transfer command by generating an 85H interrupt. However, if the IDI bit is reset, then instead the Am33C93A sits in an idle state, waiting for the Target to reconnect. If a different Target device Reselects the Am33C93A, a "terminated" interrupt is generated. However, if the original Target Reselects the Am33C93A, no interrupt is generated and the COMMAND PHASE register is set to hex 44.

Following the original Target Reselection, the Am33C93A expects a Message In phase which should consist of the Target sending an IDENTIFY Message. This single-byte message should be of the binary form: 10000ttt, where ttt is the Target LUN. If the data received by the Am33C93A is different or the Target LUN specified in this byte does not match the contents of the TARGET LUN register, a "terminated" interrupt is generated and the Message byte may be examined by the processor. A correct IDENTIFY Message In phase results in the COMMAND PHASE register being updated to hex 45.

After the IDENTIFY Message is received from the Target or immediately after the Command Out phase (when there is no disconnection), a Data In phase, Data Out phase, or Status phase should occur. If the TRANSFER COUNT register contains any non-zero value, then the Am33C93A will expect a Data Transfer phase. If Advanced Features are enabled, then the DPD bit will be examined to verify the correct data direction. If the data direction is incorrect, then a "terminated" interrupt is generated. In this phase, the Am33C93A will use the TRANSFER COUNT register to determine the number of bytes to be transferred, and all host-side DATA register accesses will be accomplished via the method selected by the DMA mode select bits in the CONTROL register. When the internal counter

reaches zero, the Data Transfer phase is complete and the COMMAND PHASE register is set to hex 46.

Note that any number of disconnection/reconnection cycles may occur during the Data Transfer phase so long as they are accomplished according to the defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41–45) with each disconnection and subsequent reconnection until all of the data has been transferred and the Data Transfer phase is complete.

A Status phase is expected by the Am33C93A following the Data Transfer phase (or instead of the Data Transfer phase when the TRANSFER COUNT register contains a value of zero). At the start of the Status phase, the COMMAND PHASE register is loaded with hex 47. Upon completion of the Status phase, the COMMAND PHASE register will be updated to hex 50, and the received status byte is stored in the TARGET LUN register where it can be read upon completion of the command.

Following completion of the status-byte transfer, a Message In phase is expected. The Am33C93A expects the Target to send a COMMAND COMPLETE Message (hex 00) to indicate that the SCSI command operation has been completed. After the Am33C93A receives this COMMAND COMPLETE Message, the COMMAND PHASE register advances to hex 60, and if the EDI bit is reset, a "successful completion" interrupt is generated. The processor should then read the TARGET LUN register to examine the Target status. An additional interrupt will then occur when the SCSI bus goes to the Bus Free state, or when another $\overline{REQ}$ is asserted to begin an information transfer phase (as in SCSI linked commands). If the EDI bit is set, the "successful completion" interrupt will be suppressed until the Target disconnects from the SCSI bus.

At any time during execution of the Select-and-Transfer commands, an abnormal or unexpected condition will cause the Am33C93A to terminate the command, set the appropriate status qualifiers, and generate a "terminated" interrupt. If the termination occurred during an information transfer phase, the Am33C93A will be left in a Connected-as-an-Initiator state (unless termination was due to a sudden Target disconnection). Command termination during any other phase will result in the Am33C93A being in a Disconnected state. Transfer commands may be used to handle the exception by transferring messages with the Target.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Select-and-Transfer commands, and their meanings relative to command termination:

Command Phase	Meaning
00	No SCSI bus device has been selected. The Am33C93A is in the disconnected state.
10	The Target has been selected. The Am33C93A is now in the connected as an Initiator state.
20	An Identify message has been sent to the Target.
30	Command phase has started, no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI bus free) following a successful transfer of a Disconnect message. The Am33C93A is now in the disconnected state.
44	The Am33C93A has been reselected by the Target whose SCSI bus ID matches the value in the DESTINATION ID register. The Am33C93A is now in the connected as an Initiator state.
45	The Am33C93A has received an Identify message from the Target whose Logical Unit Number matches the value in the TARGET LUN register.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to/from the Target during a Data Out/In phase.
47	The Target has begun a Receive Status phase.
50	The Am33C93A has successfully received a Status byte from the Target and stored it in the TARGET LUN register.
60	The Am33C93A has successfully received a Command Complete message from the Target.

A "Resume Select-and-Transfer" command is assumed whenever a normal "Select-and-Transfer" command is issued while the Am33C93A is in the Connected-Initiator state. When the "Resume" is issued, the Am33C93A examines the COMMAND PHASE register to determine where to restart the Select-and-Transfer command execution. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT enabled, allows support of multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

Command Phase	Meaning
10	Resume after Target selection is complete.
20	Resume after Identify message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun ($\overline{REQ}$ asserted).
41	Resume after Command phase or after Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a Target.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the data phase has been completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the Target; an implied Negate ACK occurs.

RESELECT-AND-TRANSFER (0A AND 0B HEX)

The Reselect-and-Transfer commands include the Reselect-and-Receive-Data and the Reselect-and-Send-Data commands. These commands cause the Am33C93A to execute certain common SCSI bus phase sequences as a Target following a Reselection phase. These phases are determined by which command is sent, and the setting of two bits: the EDI bit in the CONTROL register; and the SCC bit in the DESTINATION ID register. The SCSI bus phase sequences are summarized below. Refer to the command descriptions of the Send-Status-and-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

1. Reselect-and-Receive command, EDI=0, and SCC=don't care:
   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Completion interrupt.
2. Reselect-and-Send command, EDI=0, and SCC=don't care:
   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Completion interrupt.
3. Reselect-and-Receive command, EDI=1, and SCC=0:
   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Status-and-Command Complete;
4. Reselect-and-Send command, EDI=1, and SCC=0:
   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Status-and-Command-Complete;
5. Reselect-and-Receive command, EDI=1, and SCC=1:
   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Disconnect-Message;
6. Reselect-and-Send command, EDI=1, and SCC=1:
   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Disconnect-Message.

If the reselection attempt times out during a Reselect-and-Transfer command, $\overline{ATN}$ is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will be terminated and the appropriate status will be set. In this case, the COMMAND PHASE register should be evaluated to determine the last successfully completed phase. If none of these conditions occurs, all phases complete normally, and if EDI=0, then a "successful completion" interrupt would be generated at this point. However, if EDI=1, no interrupt is generated and command chain occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Reselect-and-Transfer commands, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Command Phase	Meaning
00	No SCSI bus device has been reselected. The Am33C93A is in the disconnected state.
10	The Am33C93A has successfully reselected the Initiator. The Am33C93A is now in the connected as a Target state.
20	The Identify message has been successfully sent to the Initiator.
46	The requested data transfer has been completed.

A "Resume Reselect-and-Transfer" command is assumed whenever a normal "Reselect-and-Transfer" command is issued while the Am33C93A is in the Connected-as-a-Target state. When the "Resume" is issued, the Am33C93A examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

Command Phase	Meaning
10	Resume after Initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

WAIT-FOR-SELECT-AND-RECEIVE (0C HEX)

The Wait-for-Select-and-Receive causes the Am33C93A to idle until it is selected by an Initiator, at which time the Am33C93A will enter the Target mode and message and command information will automatically be requested. As an option, the Am33C93A may be programmed to disconnect when a SCSI read command is received while executing a Wait-for-Select-and-Receive command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase, and results in very short bus-connect time during SCSI read commands.

If $\overline{ATN}$ was asserted by the Initiator during the selection phase, the Am33C93A will first execute an implied "Receive Message Out" command to get the Identify message from the Initiator, before continuing on with the implied "Receive Command" to receive the SCSI command information. The SCSI command information (CDB) will be stored in the CDB registers (hex addresses 03 to 0E), and if a valid IDENTIFY message is received, it will be saved in the TARGET LUN register (hex address 0F). The number of command bytes requested by the Am33C93A is determined by the SCSI group code in the first byte of the CDB.

After the Am33C93A is selected and receives all valid command and message information, a "successful completion" interrupt will normally be generated to allow the local processor to read out and interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the Am33C93A is enabled to perform an automatic disconnect when a SCSI read command is received. Therefore, when EDI=1 and the 1st CDB byte received contains a 6-, 10-, or 12-byte read command code, then the Am33C93A will temporarily suppress the interrupt and chain to begin execution of a Send-Disconnect-Message command. An interrupt will then be generated after completion of this command, which normally would indicate a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If during execution the message or command information received from the Initiator is invalid, the implied receive command will be terminated and the appropriate status reported. In this case, the COMMAND PHASE register should be read to determine which phase of the Wait-for-Select-and-Receive command was last completed before the error condition occurred. A COMMAND PHASE hex value of hex 10 indicates that the Am33C93A was successfully selected. A hex value of 20 indicates that a message was received from the Initiator, and when the Am33C93A begins receiving command bytes, the COMMAND PHASE is set to hex 30 and increments with each byte received (to a maximum of 3C for a 12-byte CDB command).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Wait-for-Select-and-Receive command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Command Phase	Meaning
00	The Am33C93A has not been selected. The Am33C93A is in the disconnected state.
10	The Am33C93A has been successfully selected by the Initiator. The Am33C93A is now in the connected as a Target state.
20	The Identify message has been successfully received from the Initiator.
30	The Am33C93A has begun command phase by setting the SCSI bus phase signals and asserting $\overline{REQ}$.
31	The Am33C93A has transferred one command byte from the Initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The Am33C93A has transferred x command bytes from the Initiator.

A "Resume Wait-for-Select-and-Receive" command is assumed whenever a normal "Wait-for-Select-and-Receive" command is issued while the Am33C93A is in the Connected-as-a-Target state. When the "Resume" is issued, the Am33C93A examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

Command Phase	Meaning
10	Resume after selection by the Initiator is complete; start with Identify Message Out if ATN is asserted, otherwise, start with command phase.
20	Resume after a message out; check the received message in the TARGET LUN register for a valid Identify message.
30	Resume after Identify message out. Start with command phase.
31	Resume after the Am33C93A has transferred 1 command byte from the Initiator. This resume point is used only when an unknown group code has been detected in Advanced Mode, and the command size has been loaded into the OWN ID register.

SEND-STATUS-AND-COMMAND-COMPLETE (0D HEX)

The Send-Status-and-Command-Complete command is valid in the Target role, and is used to complete a SCSI operation by transferring the appropriate status information to the Initiator prior to disconnection from the SCSI bus. This command also supports linked SCSI operations by optionally allowing a linked command-complete message to be sent after the status is transferred. Linked command complete messages are controlled by the CDB12 register with bits that correspond to the standard linked command control bits in the CDB.

Before a Send-Status-and-Command-Complete command is issued, the CDB11 register must be loaded with a status byte which will then be transferred across the SCSI bus. Also, the link control bits from the current CDB must be loaded into the CDB12 register to ensure that the correct sequence occurs. Note that the bits used by the Am33C93A are identical in meaning to the SCSI standard link control bits. The host processor may simply load the control byte from the current SCSI command into CDB12 to get the correct function. As the command execution progresses, the COMMAND PHASE register will be updated to indicate the last phase completed.

The possible sequences caused by this command are as follows:

1. CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex). A "successful completion" interrupt now occurs.
2. CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked Command Complete message (0A hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. Am33C93A command execution proceeds as described for that command.
3. CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked Command Complete with Flag message (0B hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. Am33C93A command execution proceeds as described for that command.

A Send-Status-and-Command-Complete command may be terminated by $\overline{ATN}$ asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Status-and-Command-Complete command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Command Phase	Meaning
00	No operation occurred; typically, $\overline{ATN}$ was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

A "Resume Send-Status-and-Command-Complete" command is assumed whenever a normal "Send-Status-and-Command-Complete" command is issued while the Am33C93A is in the Connected-as-a-Target state. When the "Resume" is issued, the Am33C93A examines the COMMAND PHASE register to determine where to restart the Send-Status-and-Command-Complete command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

Command Phase	Meaning
50	Resume after status phase. Start with command complete message. May chain to command fetch if commanded to do so.

SEND-DISCONNECT-MESSAGE (0E HEX)

The Send-Disconnect-Message command is a Target-role command which may be used to disconnect from the SCSI bus at any time during a SCSI command

sequence. This command consists of sending a Disconnect message byte, followed by physical disconnection from the bus (SCSI bus free). An interrupt is generated only after transition to bus free occurs. As an option, a Save-Data-Pointer message will automatically be sent before the Disconnect message whenever the IDI bit is set prior to issuing this command.

The COMMAND PHASE register is updated during execution of the Send-Disconnect-Message command to indicate bus phase status. After a Save-Data-Pointer message is sent, the COMMAND PHASE will be set to 41H. After the Disconnect message transfer, this register will be updated to 42H, and after disconnection the COMMAND PHASE register will contain a 43H.

A Send-Disconnect-Message command may be terminated by $\overline{ATN}$ asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Disconnect-Message, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

Command Phase	Meaning
00	No operation occurred; typically, $\overline{ATN}$ was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The Am33C93A is now in the disconnected state.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to GND	–0.5 V to +7.0 V
Operating temperature	0 to 70 deg. C
Storage temperature	–55 to +125 deg. C
Power dissipation	400 mW
Input Static Discharge Protection	2K V

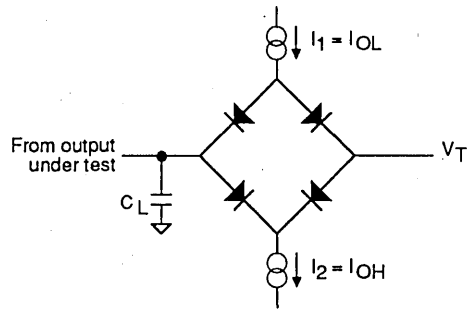
Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolutely maximum ratings for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS

Ta = 0 to 70°C, VCC = +5 V ±0.25 V, GND = 0 V

Symbol	Characteristic	Min	Max	Units	Conditions
IIL	Input Leakage		10	µA	VIN = .4 to VCC
IOL1	SCSI Output Leakage (Inactive)		50	µA	VOUT = .5 to VCC
IOL2	Output Leakage (Tri-State)		10	µA	VOUT = .4 to VCC
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		0.8	V	
VIHYS	Schmitt Trigger Input Hysteresis (All SCSI Pins)	0.2		V	
VOH	Output High Voltage	2.4		V	IO = –400 µA
VOL1	SCSI Output Low Voltage		0.5	V	IO = 48.0 mA
VOL2	Output Low Voltage (All Others)		0.4	V	IO = 4.0 mA
ICC	Supply Current		20	mA	Ta = +25°C

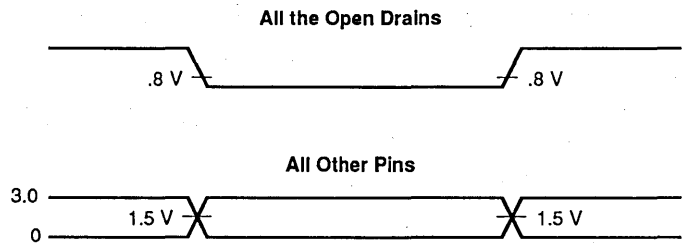
SWITCHING TEST CIRCUIT



Pins of the Device	*C_L	I_1	I_2
INTRQ, RE, WE	100 pF	4 mA	400 µA
D0–D7, DP	100 pF	4 mA	400 µA
DACK, DRQ	100 pF	4 mA	—
SD0–SD7, SDP BSY, SEL, I/O, C/D MSG, ATN, REQ, ACK	100 pF	20 mA	—

* Actual capacitance may vary ±20%.

SWITCHING TEST WAVEFORM



TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70°C) and voltage (4.75 to 5.25 V) ranges, and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 Volts. All outputs are assumed to have a load capacitance of 50 picofarads.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time that is determined by the input clock and the clock divisor selected in the OWN ID register. This cycle time is calculated as follows:

$$Tcyc = \frac{Tckin \bullet DIVISOR}{2}$$

Where:

Tcyc is the internal clock cycle time;

Tckin is the period of the clock at the CLK input;

DIVISOR is the clock divisor selected in the OWN ID register.

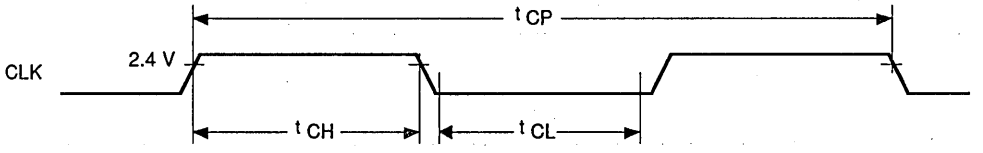
For example, with a 16 MHz clock input to the Am33C93A, the clock divisor selected would be 4. Therefore, the value of Tcyc would be:

$$Tcyc = \frac{62.5\ ns \bullet 4}{2} = 125\ ns$$

Processor/DMA Interface

CLK

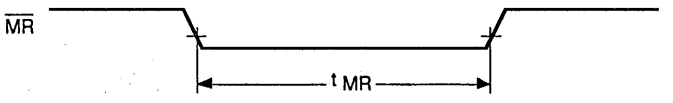
Symbol	Characteristic		Min	Max	Units
t_{CP}	Clock Period	16 MHz	62.5	125	ns
		20 MHz	50.0		ns
t_{CH}	Clock High	16 MHz	28.0		ns
		20 MHz	20.0		ns
t_{CL}	Clock Low	16 MHz	28.0		ns
		20 MHz	20.0		ns



11853-013A

$\overline{MR}$

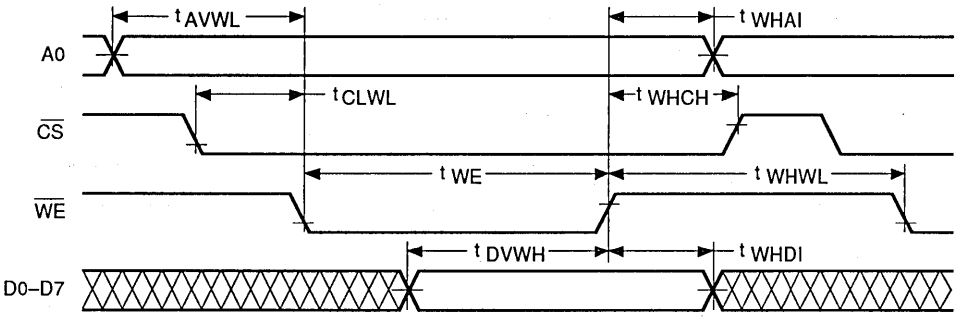
Symbol	Characteristic	Min	Max	Units
t_{MR}	$\overline{MR}$ Pulse Width	1		µs



11853-014A

PROCESSOR WRITE—INDIRECT ADDRESSING MODE

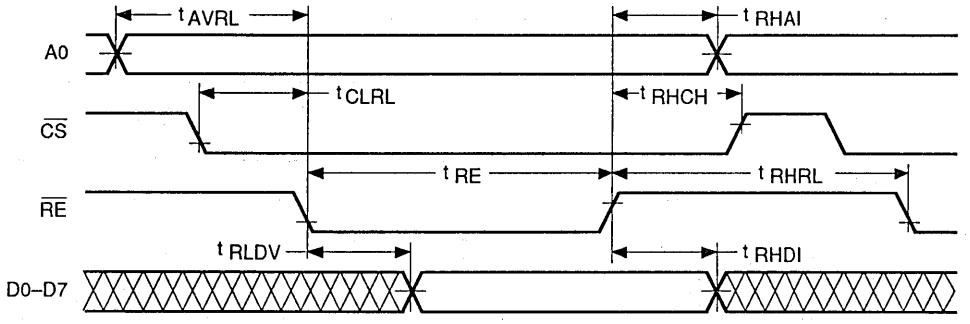
Symbol	Characteristic	Min	Max	Units
t_{AVWL}	A0 Valid to $\overline{WE}$ Low	0		ns
t_{CLWL}	$\overline{CS}$ Low to $\overline{WE}$ Low	0		ns
t_{WE}	$\overline{WE}$ Pulse Width	120		ns
t_{DVWH}	Data Valid to $\overline{WE}$ High	70		ns
t_{WHAI}	$\overline{WE}$ High to A0 Invalid	0		ns
t_{WHCH}	$\overline{WE}$ High to $\overline{CS}$ High	0		ns
t_{WHDI}	$\overline{WE}$ High to Data Invalid	0		ns
t_{WHWL}	$\overline{WE}$ High to $\overline{WE}$ or $\overline{RE}$ Low	100		ns



11853-015A

PROCESSOR READ—INDIRECT ADDRESSING MODE

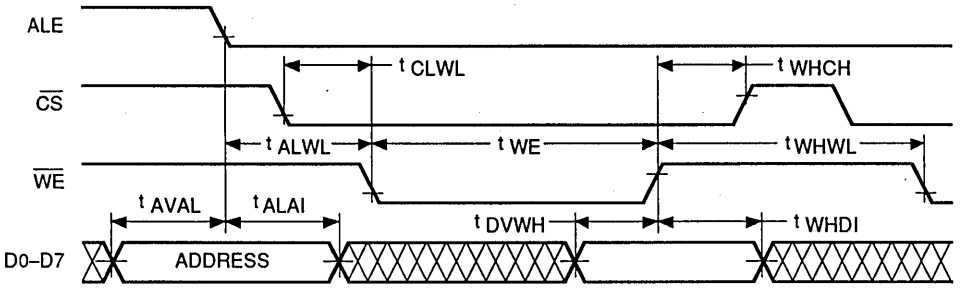
Symbol	Characteristic	Min	Max	Units
t_{AVRL}	A0 Valid to $\overline{RE}$ Low	0		ns
t_{CLRL}	$\overline{CS}$ Low to $\overline{RE}$ Low	0		ns
t_{RE}	$\overline{RE}$ Pulse Width	180	10000	ns
t_{RLDV}	$\overline{RE}$ Low to Data Valid		180	ns
t_{RHCH}	$\overline{RE}$ High to $\overline{CS}$ High	0		ns
t_{RHDI}	$\overline{RE}$ High to Data Invalid	10	40	ns
t_{RHRL}	$\overline{RE}$ High to $\overline{RE}$ or $\overline{WE}$ Low	100		ns
t_{RHAI}	$\overline{RE}$ High to A0 Invalid	0		ns



11853-016A

PROCESSOR WRITE—DIRECT ADDRESSING MODE

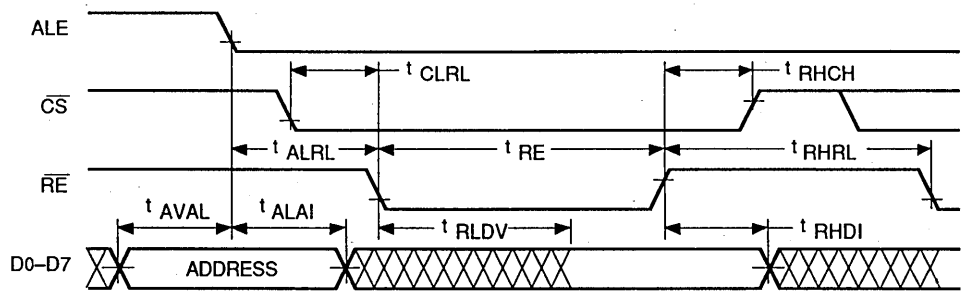
Symbol	Characteristic	Min	Max	Units
t_{AVAL}	ADDR Valid to ALE Low	40		ns
t_{ALAI}	ALE Low to ADDR Invalid	0		ns
t_{ALWL}	ALE Low to $\overline{WE}$ Low	90		ns
t_{CLWL}	$\overline{CS}$ Low to $\overline{WE}$ Low	0		ns
t_{WE}	$\overline{WE}$ Pulse Width	120		ns
t_{DVWH}	Data Valid to $\overline{WE}$ High	70		ns
t_{WHCH}	$\overline{WE}$ High to $\overline{CS}$ High	0		ns
t_{WHDI}	$\overline{WE}$ High to Data Invalid	0		ns
t_{WHWL}	$\overline{WE}$ High to $\overline{WE}$ or $\overline{RE}$ Low	100		ns



11853-017A

PROCESSOR READ—DIRECT ADDRESSING MODE

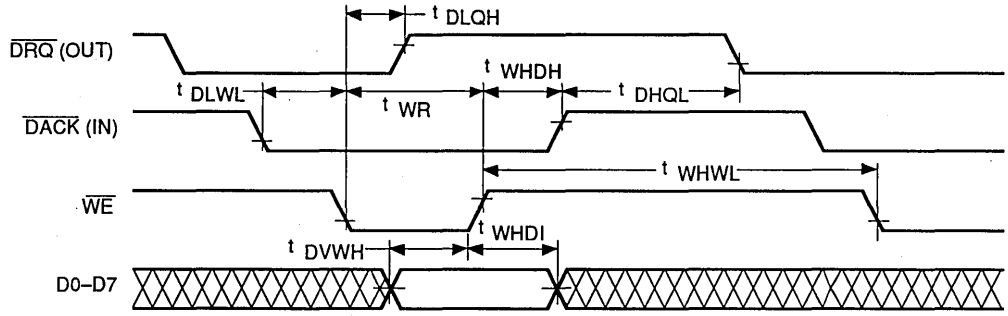
Symbol	Characteristic	Min	Max	Units
t_{AVAL}	ADDR Valid to ALE Low	40		ns
t_{ALAI}	ALE Low to ADDR Invalid	0		ns
t_{ALRL}	ALE Low to $\overline{RE}$ Low	30		ns
t_{CLRL}	$\overline{CS}$ Low to $\overline{RE}$ Low	0		ns
t_{RE}	$\overline{RE}$ Pulse Width	180	10000	ns
t_{RLDV}	$\overline{RE}$ Low to Data Valid		180	ns
t_{RHCH}	$\overline{RE}$ High to $\overline{CS}$ High	0		ns
t_{RHDI}	$\overline{RE}$ High to Data Invalid	10	40	ns
t_{RHRL}	$\overline{RE}$ High to $\overline{RE}$ or $\overline{WE}$ Low	100		ns



11853-018A

DMA WRITE

Symbol	Characteristic	Min	Max	Units
t_{DLWL}	$\overline{DACK}$ Low to $\overline{WE}$ Low	0		ns
t_{DLQH}	$\overline{DACK}$, $\overline{WE}$ Low to $\overline{DRQ}$ High		75	ns
t_{WR}	$\overline{WE}$ Pulse Width	50		ns
t_{WHWL}	$\overline{WE}$ High to $\overline{WE}$ Low	100		ns
t_{DVWH}	Data Valid to $\overline{WE}$ High	25		ns
t_{WHDH}	$\overline{WE}$ High to $\overline{DACK}$ High	0		ns
t_{WHDI}	$\overline{WE}$ High to DATA Invalid	5		ns
t_{DHQL}	$\overline{DACK}$ High to $\overline{DRQ}$ Low	0		ns

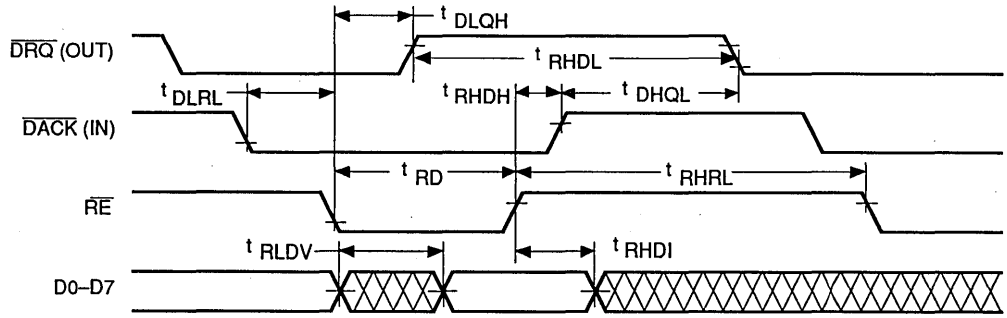


NOTE: External load on $\overline{DRQ}$ & $\overline{DACK}$ is assumed to be 1K Ω.

11853-019A

DMA READ

Symbol	Characteristic	Min	Max	Units
t_{DLRL}	$\overline{DACK}$ Low to $\overline{RE}$ Low	0		ns
t_{DLQH}	$\overline{DACK}$, $\overline{RE}$ Low to $\overline{DRQ}$ High		75	ns
t_{RD}	$\overline{RE}$ Pulse Width	80		ns
t_{RHRL}	$\overline{RE}$ High to $\overline{RE}$ Low	100		ns
t_{RLDV}	$\overline{RE}$ Low to Data Valid		70	ns
t_{RHDH}	$\overline{RE}$ High to $\overline{DACK}$ High	0		ns
t_{RHDI}	$\overline{RE}$ High to DATA Invalid	5	40	ns
t_{DHQL}	$\overline{DACK}$ High to $\overline{DRQ}$ Low	0		ns
t_{RHDL}	$\overline{DRQ}$ High to $\overline{DRQ}$ Low	100		ns

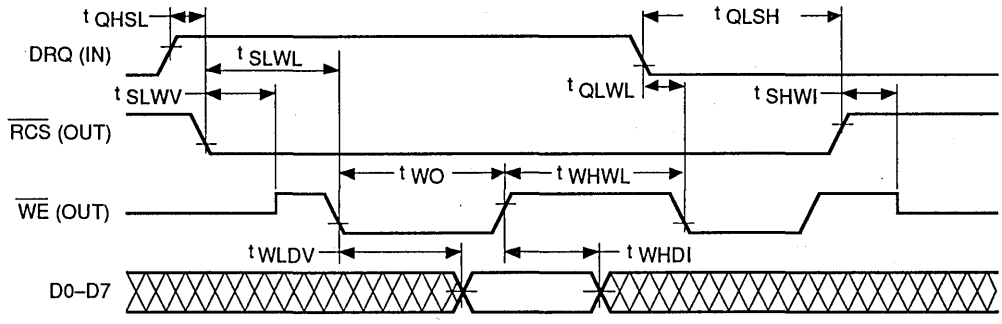


NOTE: External load on $\overline{DRQ}$ & $\overline{DACK}$ is assumed to be 1K Ω.

11853-020A

DIRECT BUFFER ACCESS WRITE

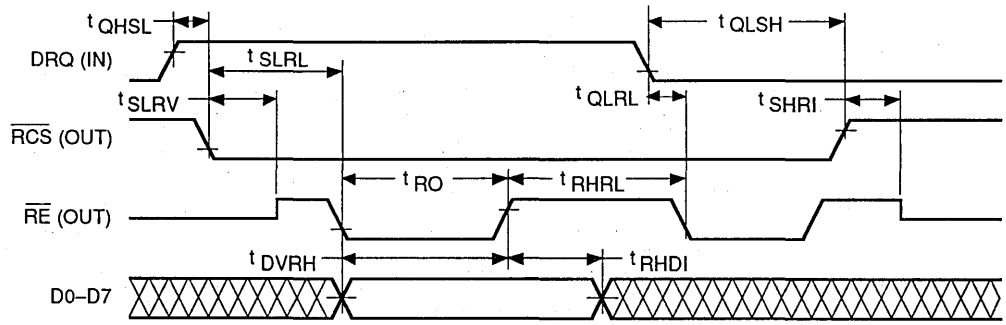
Symbol	Characteristic	Min	Max	Units
t_{QHSL}	DRQ High to $\overline{RCS}$ Low	0		ns
t_{SLWV}	$\overline{RCS}$ Low to $\overline{WE}$ Valid	0	20	ns
t_{WO}	$\overline{WE}$ Pulse Width	Tcyc-20		ns
t_{WLDV}	$\overline{WE}$ Low to Data Valid		50	ns
t_{WHDI}	$\overline{WE}$ High to Data Invalid	20		ns
t_{WHWL}	$\overline{WE}$ High to $\overline{WE}$ Low	Tcyc-20		ns
t_{QLSH}	DRQ Low to $\overline{RCS}$ High	8*Tcyc	10*Tcyc	ns
t_{SHWI}	$\overline{RCS}$ High to $\overline{WE}$ Invalid	0	100	ns
t_{SLWL}	$\overline{RCS}$ Low to $\overline{WE}$ Low	60		ns
t_{QLWL}	DRQ Low to $\overline{WE}$ Low (1)	0		ns



11853-021A

DIRECT BUFFER ACCESS READ

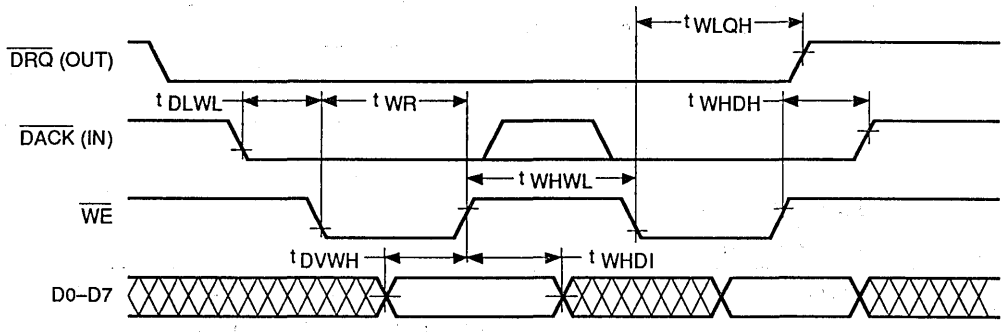
Symbol	Characteristic	Min	Max	Units
t_{QHSL}	DRQ High to $\overline{RCS}$ Low	0		ns
t_{SLRV}	$\overline{RCS}$ Low to $\overline{RE}$ Valid	0	20	ns
t_{RO}	$\overline{RE}$ Pulse Width	Tcyc-20		ns
t_{DVRH}	Data Valid to $\overline{RE}$ High	10		ns
t_{RHDI}	$\overline{RE}$ High to Data Invalid	10		ns
t_{RHRL}	$\overline{RE}$ High to $\overline{RE}$ Low	Tcyc-20		ns
t_{QLSH}	DRQ Low to $\overline{RCS}$ High	8*Tcyc	10*Tcyc	ns
t_{SHRI}	$\overline{RCS}$ High to $\overline{RE}$ Invalid		100	ns
t_{SLRL}	$\overline{RCS}$ Low to $\overline{RE}$ Low	60		ns
t_{QLRL}	DRQ Low to $\overline{RE}$ Low (1)	0		ns



11853-022A

BURST DMA WRITE

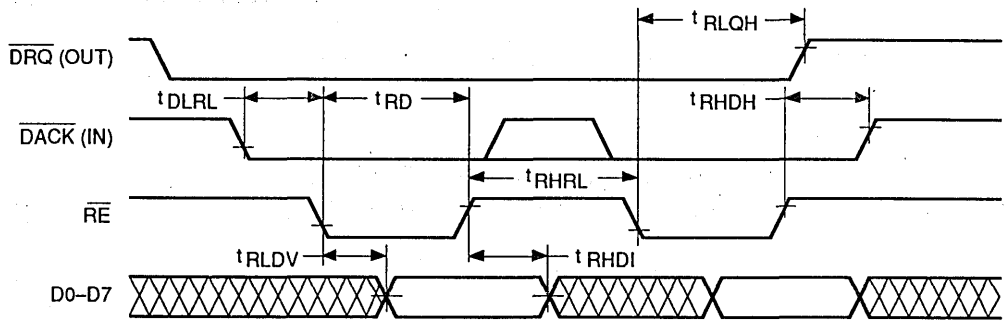
Symbol	Characteristic	Min	Max	Units
t_{DLWL}	$\overline{DACK}$ Low to $\overline{WE}$ Low	0		ns
t_{WLQH}	$\overline{WE}$ Low to $\overline{DRQ}$ High		75	ns
t_{WR}	$\overline{WE}$ Pulse Width	50		ns
t_{WHWL}	$\overline{WE}$ High to $\overline{WE}$ Low	80		ns
t_{DVWH}	Data Valid to $\overline{WE}$ High	25		ns
t_{WHDH}	$\overline{WE}$ High to $\overline{DACK}$ High	0		ns
t_{WHDI}	$\overline{WE}$ High to Data Invalid	5		ns



11853-023A

BURST DMA READ

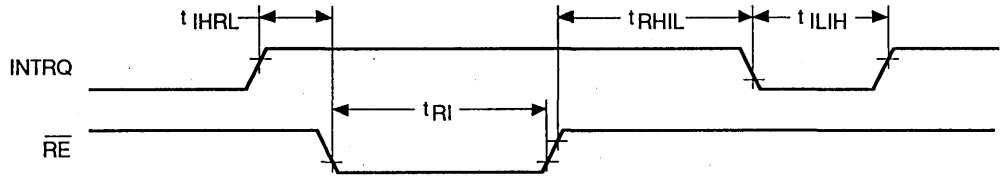
Symbol	Characteristic	Min	Max	Units
t_{DLRL}	$\overline{DACK}$ Low to $\overline{RE}$ Low	0		ns
t_{RLQH}	$\overline{RE}$ Low to $\overline{DRQ}$ High		75	ns
t_{RD}	$\overline{RE}$ Pulse Width	80		ns
t_{RHRL}	$\overline{RE}$ High to $\overline{RE}$ Low	80		ns
t_{RLDV}	$\overline{RE}$ Low to Data Valid		50	ns
t_{RHDH}	$\overline{RE}$ High to $\overline{DACK}$ High	0		ns
t_{RHDI}	$\overline{RE}$ High to Data Invalid	5	40	ns



11853-024A

INTRQ

Symbol	Characteristic	Min	Max	Units
t_{IHRL}	INTRQ High to $\overline{RE}$ Low	0		ns
t_{RI}	$\overline{RE}$ Pulse Width	180		ns
t_{RHIL}	$\overline{RE}$ High to INTRQ Low	0	100	ns
t_{ILIH}	INTRQ Low to INTRQ High	100		ns

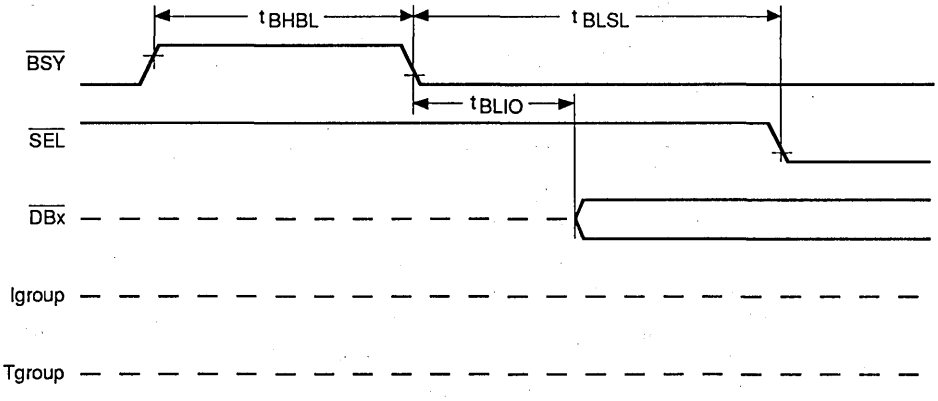


11853-025A

SCSI Interface

ARBITRATION

Symbol	Characteristic	Min	Max	Units
t_{BHBL}	$\overline{BSY}$, $\overline{SEL}$ In High to $\overline{BSY}$ Out Low	12*Tcyc	6*Tcyc	ns
t_{BLIO}	$\overline{BSY}$ Out Low to BUS ID Out	–50	50	ns
t_{BLSL}	$\overline{BSY}$ Out Low to $\overline{SEL}$ Out Low	2.2		µs

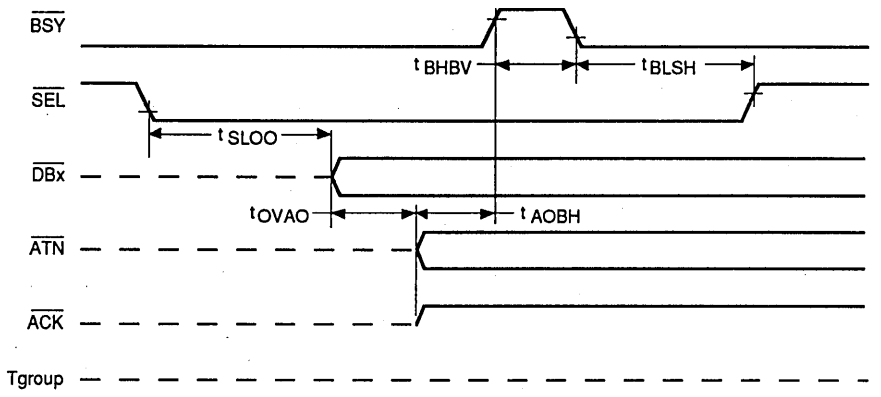


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

11853-026A

SELECTING A TARGET (AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SLOO}	$\overline{SEL}$ Out Low to "OR-ED" ID Out	1.2		us
t_{OVAO}	"OR-ED" ID Out Valid to $\overline{ACK}$, $\overline{ATN}$ Out	100		ns
t_{AOBH}	$\overline{ACK}$, $\overline{ATN}$ Out Valid to $\overline{BSY}$ Out High	100		ns
t_{BHBV}	$\overline{BSY}$ Out High to $\overline{BSY}$ In Low Valid	400		ns
t_{BLSH}	$\overline{BSY}$ In Low to $\overline{SEL}$ Out High	100		ns

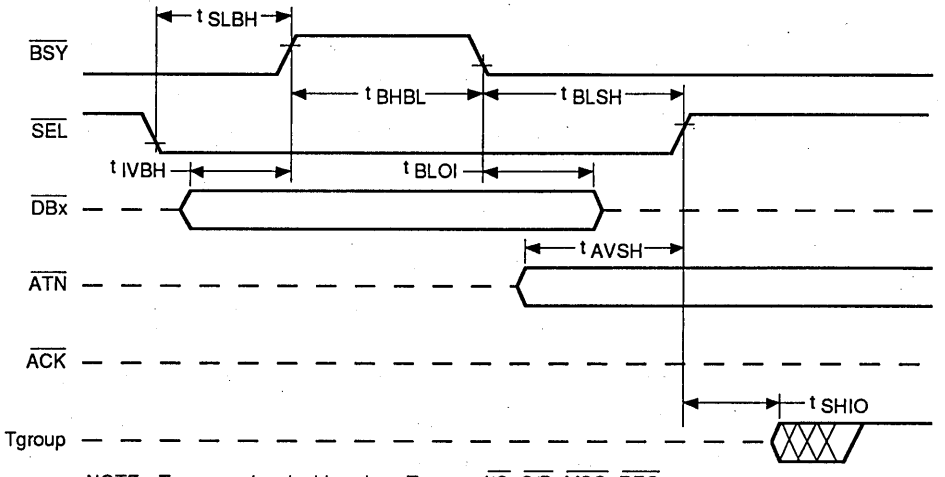


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

11853-027A

RESPONSE TO SELECTION (AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SLBH}	$\overline{SEL}$ In Low to $\overline{BSY}$ In High	0		ns
t_{IVBH}	"OR-ED" ID Valid In to $\overline{BSY}$ In High	0		ns
t_{BHBL}	$\overline{SEL}$ Low , ID Valid , $\overline{BSY}$ High to $\overline{BSY}$ Low	0.4	200	us
t_{BLOI}	$\overline{BSY}$ Out Low to "OR-ED" ID Invalid In	0		ns
t_{BLSH}	$\overline{BSY}$ Out Low to $\overline{SEL}$ In High	0		ns
t_{AVSH}	$\overline{ATN}$ Valid In to $\overline{SEL}$ In High	0		ns
t_{SHIO}	$\overline{SEL}$ In High to Tgroup Out	100		ns

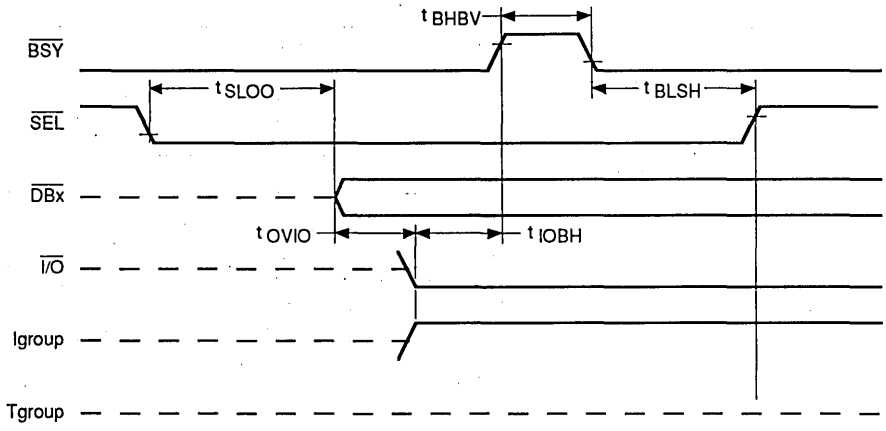


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$

11853-028A

RESELECTING AN INITIATOR (AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SLOO}	$\overline{SEL}$ Out Low to "OR-ED" ID Out	1.2		µs
t_{OVIO}	"OR-ED" ID Out Valid to I/O & Tgroup Out Valid	100		ns
t_{IOBH}	I/O & Tgroup Out Valid to $\overline{BSY}$ Out High	100		ns
t_{BHBV}	$\overline{BSY}$ Out High to $\overline{BSY}$ In Low Valid	400		ns
t_{BLSH}	$\overline{BSY}$ In Low to $\overline{SEL}$ Out High	100		ns

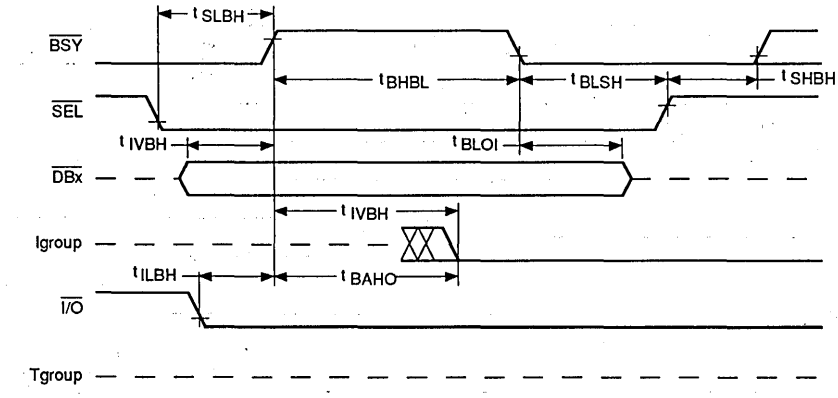


NOTE: Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

11853-029A

RESPONSE TO RESELECTION (AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SLBH}	$\overline{SEL}$ In Low to $\overline{BSY}$ In High	0		ns
t_{IVBH}	"OR-ED" ID Valid In to $\overline{BSY}$ In High	0		ns
t_{ILBH}	$\overline{I/O}$ In Low to $\overline{BSY}$ In High	0		ns
t_{BHAO}	$\overline{SEL}$ Low , ID Valid , $\overline{BSY}$ High to Igroup Out	100		ns
t_{AVBL}	Igroup Valid Out to $\overline{BSY}$ Out Low	100		ns
t_{BHBL}	$\overline{BSY}$ In High to $\overline{BSY}$ Out Low	0.4	200	µs
t_{BLOI}	$\overline{BSY}$ Out Low to "OR-ED" ID Invalid In	0		ns
t_{BLSH}	$\overline{BSY}$ Out Low to $\overline{SEL}$ In High	0		ns
t_{SHBH}	$\overline{SEL}$ In High to $\overline{BSY}$ Out High	0		ns

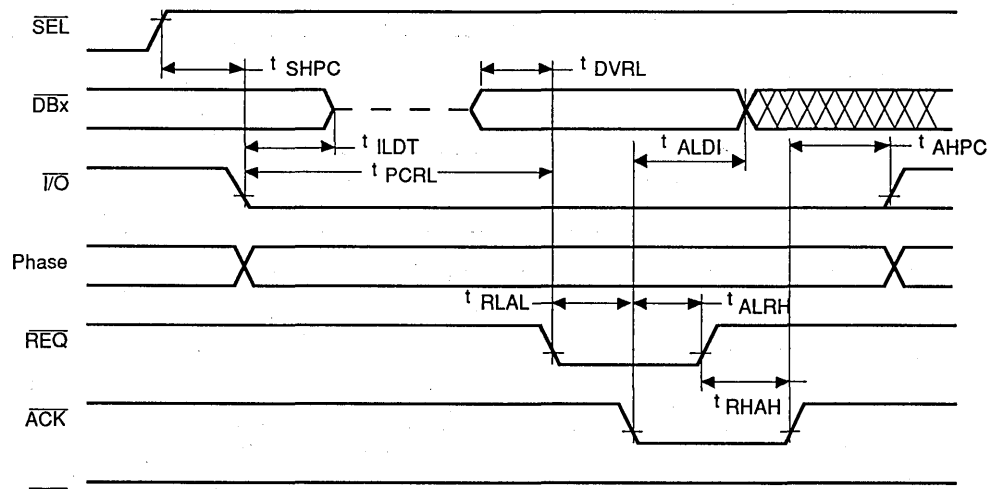


Tgroup = signals driven by a Target = $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$
*** $\overline{BSY}$ will still be driven by the reselecting target.

11853-030A

RECEIVE ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change In	0		ns
t_{ILDT}	$\overline{I/O}$ In Low to Data Bus TRISTATE	0	125	ns
t_{PCRL}	Phase Change In to $\overline{REQ}$ In Low	400		ns
t_{DVRL}	Data Valid In to $\overline{REQ}$ In Low	0		ns
t_{RLAL}	$\overline{REQ}$ In Low to $\overline{ACK}$ Out Low	0	175	ns
t_{ALDI}	$\overline{ACK}$ Out Low to Data Invalid In	0		ns
t_{ALRH}	$\overline{ACK}$ Out Low to $\overline{REQ}$ In High	0		ns
t_{RHAH}	$\overline{REQ}$ In High to $\overline{ACK}$ Out High	0	175	ns
t_{AHPC}	$\overline{ACK}$ Out High to Phase Change In	0		ns

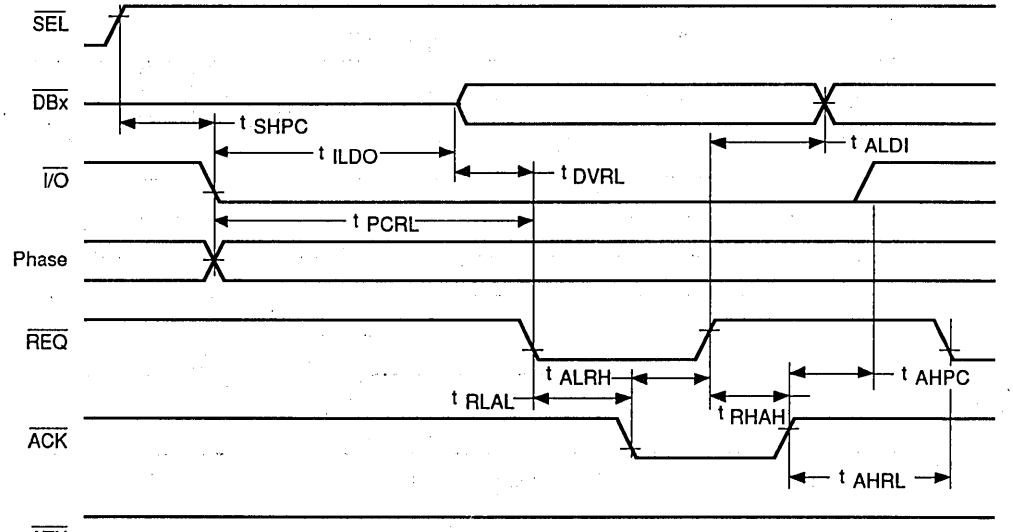


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-031A

SEND ASYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change Out	100		ns
t_{ILDO}	$\overline{I/O}$ Out Low to Data Out	800		ns
t_{DVRL}	Data Out Valid to $\overline{REQ}$ Out Low	55		ns
t_{PCRL}	Phase Change Out to $\overline{REQ}$ Out Low	500		ns
t_{RLAL}	$\overline{REQ}$ Out Low to $\overline{ACK}$ In Low	0		ns
t_{ALRH}	$\overline{ACK}$ In Low to $\overline{REQ}$ Out High	0	175	ns
t_{ALDI}	$\overline{ACK}$ In Low to Data Out Invalid	0		ns
t_{RHAH}	$\overline{REQ}$ Out High to $\overline{ACK}$ In High	0		ns
t_{AHPC}	$\overline{ACK}$ In High to Phase Change Out	100		ns
t_{AHRL}	$\overline{ACK}$ In High to $\overline{REQ}$ Out Low	0	175	ns

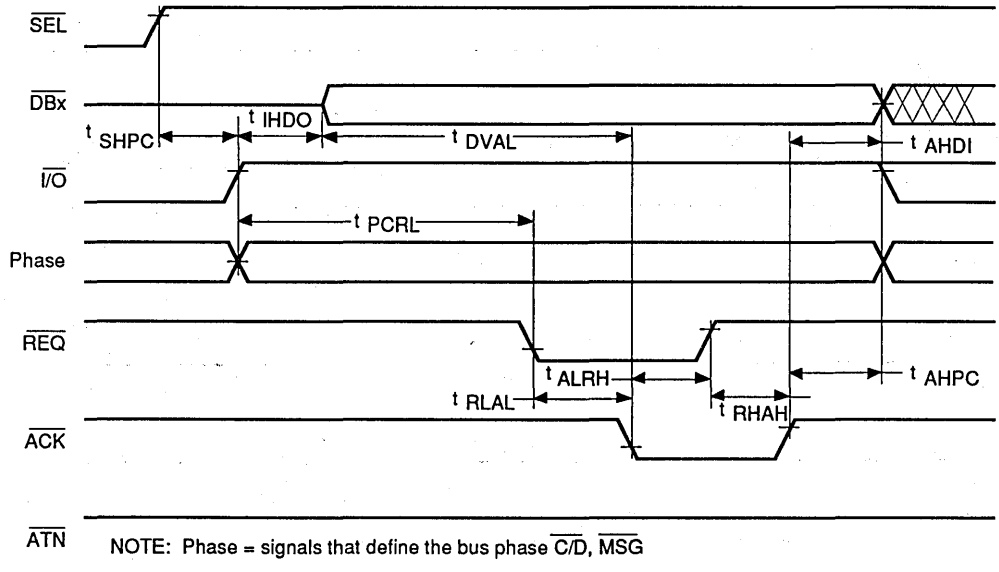


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-032A

SEND ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change In	0		ns
t_{IHDO}	$\overline{I/O}$ In High to Data Out	0		ns
t_{PCRL}	Phase Change In to $\overline{REQ}$ In Low	400		ns
t_{RLAL}	$\overline{REQ}$ In Low to $\overline{ACK}$ Out Low	0	175	ns
t_{DVAL}	Data Out Valid to $\overline{ACK}$ Out Low	55		ns
t_{ALRH}	$\overline{ACK}$ Out Low to $\overline{REQ}$ In High	0		ns
t_{RHAH}	$\overline{REQ}$ In High to $\overline{ACK}$ Out High	0	175	ns
t_{AHDI}	$\overline{ACK}$ In High to Data Out Invalid	0		ns
t_{AHPC}	$\overline{ACK}$ Out High to Phase Change In	0		ns

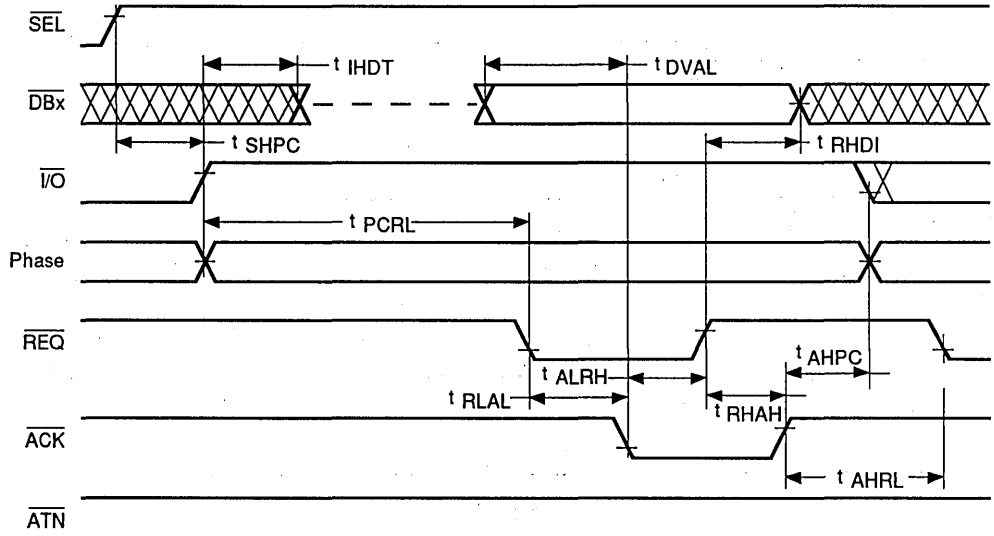


NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-033A

RECEIVE ASYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{SHPC}	$\overline{SEL}$ In High to Phase Change Out	100		ns
t_{IHDT}	$\overline{I/O}$ Out High to Data Bus TRISTATE	0		ns
t_{PCRL}	Phase Change to $\overline{REQ}$ Out Low	500		ns
t_{RLAL}	$\overline{REQ}$ Out Low to $\overline{ACK}$ In Low	0		ns
t_{DVAL}	Data In Valid to $\overline{ACK}$ In Low	5		ns
t_{ALRH}	$\overline{ACK}$ In Low to $\overline{REQ}$ Out High	0	175	ns
t_{RHDI}	$\overline{REQ}$ Out High to Data In Invalid	0		ns
t_{RHAH}	$\overline{REQ}$ Out High to $\overline{ACK}$ In High	0		ns
t_{AHPC}	$\overline{ACK}$ In High to Phase Change Out	0		ns
t_{AHRL}	$\overline{ACK}$ In High to $\overline{REQ}$ Out Low	0	175	ns



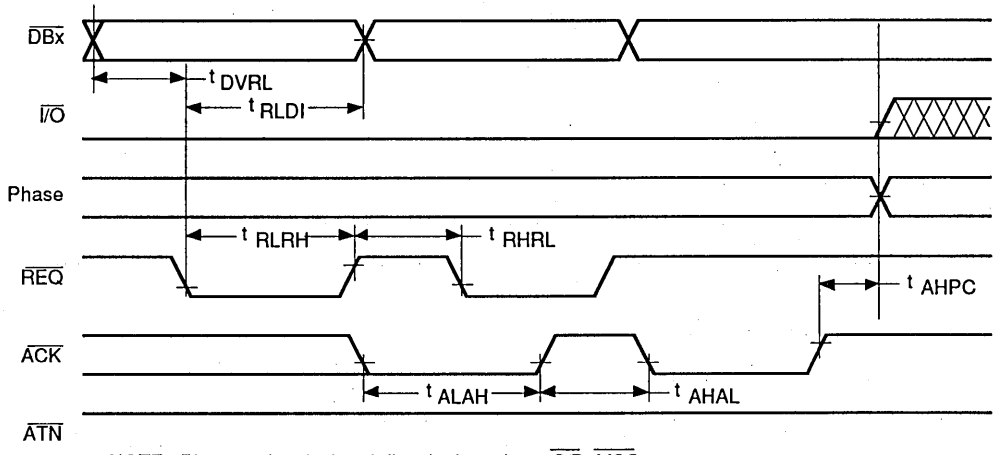
NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-034A

RECEIVE SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{DVRL}	Data Valid In to $\overline{REQ}$ In Low	0		ns
t_{RLDI}	$\overline{REQ}$ In Low to DATA Invalid	45		ns
t_{RLRH}	$\overline{REQ}$ In Low to $\overline{REQ}$ In High	50		ns
t_{RHRL}	$\overline{REQ}$ In High to $\overline{REQ}$ In Low	50		ns
t_{ALAH}	$\overline{ACK}$ Out Low to $\overline{ACK}$ Out High	Tcyc-10		ns
t_{AHAL}	$\overline{ACK}$ Out High to $\overline{ACK}$ Out Low	Tcyc-25		ns
t_{AHPC}	$\overline{ACK}$ Out High to Phase Change	0		ns

Parameters t_{SHPC}, t_{ILDT}, and t_{PCRL} are also applicable and are identical to those in Receive Asynchronous Information Transfer In (Acting as an Initiator), top of page 37.



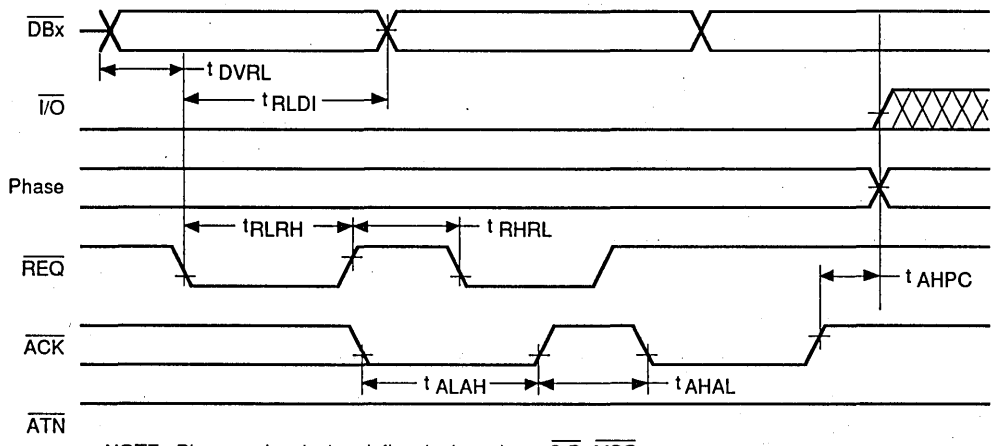
NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-035A

SEND SYNCHRONOUS INFORMATION TRANSFER IN (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{DVRL}	Data Valid Out to $\overline{REQ}$ Out Low	55		ns
t_{RLDI}	$\overline{REQ}$ Out Low to Data Invalid	100		ns
t_{RLRH}	$\overline{REQ}$ Out Low to $\overline{REQ}$ Out High	Tcyc-10		ns
t_{RHRL}	$\overline{REQ}$ Out High to $\overline{REQ}$ Out Low	Tcyc-25		ns
t_{ALAH}	$\overline{ACK}$ In Low to $\overline{ACK}$ In High	50		ns
t_{AHAL}	$\overline{ACK}$ In High to $\overline{ACK}$ In Low	50		ns
t_{AHPC}	$\overline{ACK}$ In High to Phase Change Out	0		ns

Parameters t_{SHPC}, t_{ILDO}, and t_{PCRL} are also applicable and are identical to those in Receive Asynchronous Information Transfer In (Acting as a Target), bottom of page 37.



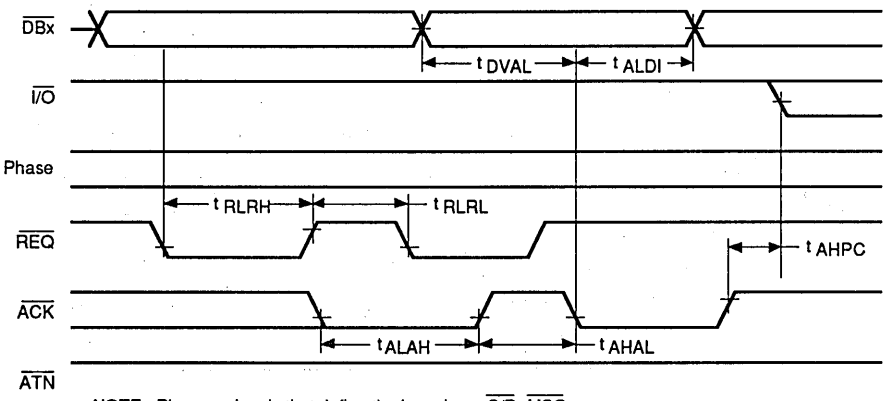
NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-036A

SEND SYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS AN INITIATOR)

Symbol	Characteristic	Min	Max	Units
t_{DVAL}	Data Valid Out to $\overline{ACK}$ Out Low	55		ns
t_{ALDI}	$\overline{ACK}$ Out Low to Data Invalid	100		ns
t_{RLRH}	$\overline{REQ}$ In Low to $\overline{REQ}$ In High	50		ns
t_{RHRL}	$\overline{REQ}$ In High to $\overline{REQ}$ In Low	50		ns
t_{ALAH}	$\overline{ACK}$ Out Low to $\overline{ACK}$ Out High	Tcyc-10		ns
t_{AHAL}	$\overline{ACK}$ Out High to $\overline{ACK}$ Out Low	Tcyc-25		ns
t_{AHPC}	$\overline{ACK}$ Out High to Phase Change In	0		ns

Parameters t_{SHPC}, t_{IHDO}, and t_{PCRL} are also applicable and are identical to those in Send Asynchronous Information Transfer In (Acting as a Target), bottom of page 39 and 40.



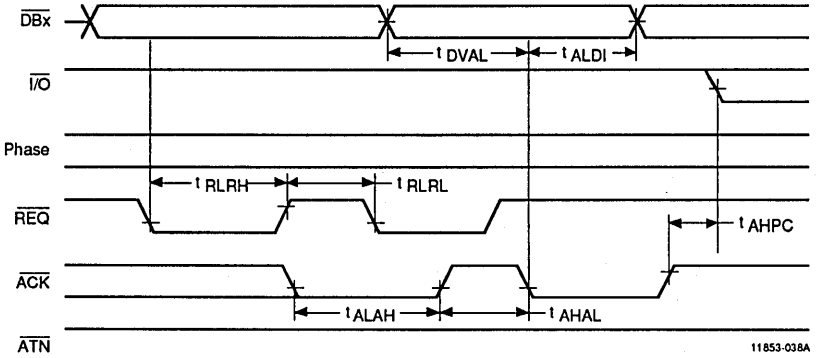
NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

11853-037A

RECEIVE SYNCHRONOUS INFORMATION TRANSFER OUT (ACTING AS A TARGET)

Symbol	Characteristic	Min	Max	Units
t_{DVAL}	Data Valid In to $\overline{ACK}$ In Low	0		ns
t_{ALDI}	$\overline{ACK}$ In Low to Data Invalid	45		ns
t_{RLRH}	$\overline{REQ}$ Out Low to $\overline{REQ}$ Out High	Tcyc-10		ns
t_{RHRL}	$\overline{REQ}$ Out High to $\overline{REQ}$ Out Low	Tcyc-25		ns
t_{ALAH}	$\overline{ACK}$ In Low to $\overline{ACK}$ In High	50		ns
t_{AHAL}	$\overline{ACK}$ In High to $\overline{ACK}$ In Low	50		ns
t_{AHPC}	$\overline{ACK}$ In High to Phase Change Out	0		ns

Parameters t_{shpc}, t_{ihdt}, and t_{pcrl} are also applicable and are identical to those in Send Synchronous Information Transfer Out (Acting as an Initiator), top of this page.

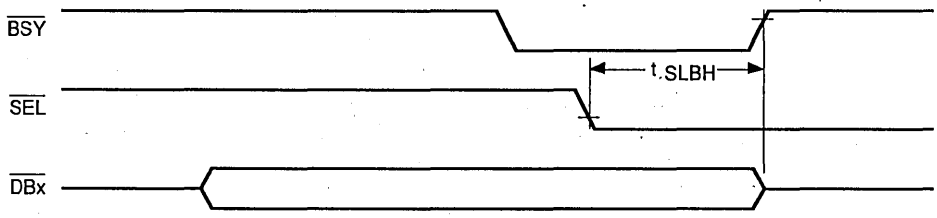


11853-038A

NOTE: Phase = signals that define the bus phase $\overline{C/D}$, $\overline{MSG}$

ARBITRATION TO BUS FREE

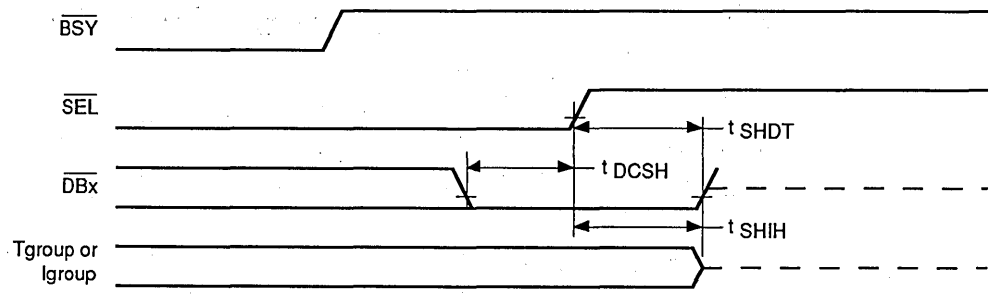
Symbol	Characteristic	Min	Max	Units
t_{SLBH}	$\overline{SEL}$ In Low to $\overline{BSY}$ High , Data TRI-STATE		8*Tcyc +75	ns



11853-039A

SELECTION (AS AN INITIATOR) OR RESELECTION (AS A TARGET) TO BUS FREE (SELECTION TIMEOUT)

Symbol	Characteristic	Min	Max	Units
t_{TADC}	Timeout or Abort to Data Bus Cleared	0		ns
t_{DCSH}	Data Bus Cleared to $\overline{SEL}$ Out High	200		µs
t_{SHDT}	$\overline{SEL}$ Out High to Data Bus TRISTATE		800	ns
t_{SHIH}	$\overline{SEL}$ Out High to CNTL TRISTATE		800	ns

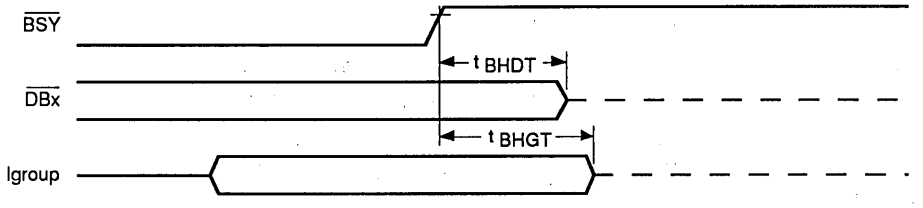


NOTE: Tgroup = signals driven by a Target = $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$
Igroup = signals driven by an Initiator = $\overline{ATN}$, $\overline{ACK}$

11853-040A

CONNECTED-AS-AN-INITIATOR TO BUS FREE

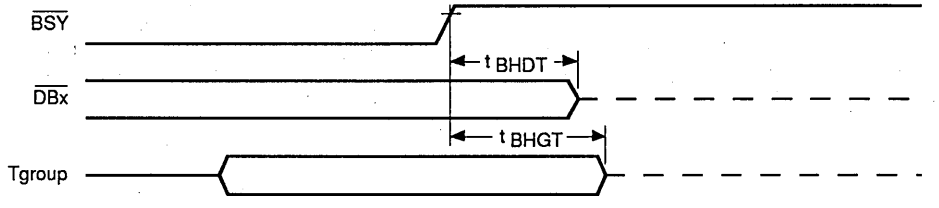
Symbol	Characteristic	Min	Max	Units
t_{BHDT}	$\overline{BSY}$ In High to Data Bus TRISTATE		8*Tcyc +75ns	ns
t_{BHGT}	$\overline{BSY}$ In High to Igroup TRISTATE		8*Tcyc +75ns	ns



11853-041A

CONNECTED-AS-A-TARGET TO BUS FREE

Symbol	Characteristic	Min	Max	Units
t_{BHDT}	$\overline{BSY}$ Out High to Data Bus TRISTATE		8*Tcyc +75ns	ns
t_{BHGT}	$\overline{BSY}$ Out High to Tgroup TRISTATE		8*Tcyc +75ns	ns



11853-042A

Am53C80A

SCSI Interface Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

SCSI Interface

- Asynchronous Interface to 4 megabytes per second
- Supports Initiator and Target roles
- Parity generation with optional checking
- Supports arbitration
- Direct control of all bus signals
- High-current outputs drive SCSI bus directly

CPU Interface

- Memory or I/O-mapped Interface
- DMA or programmed I/O
- Normal or Block mode DMA
- Optional CPU Interrupts

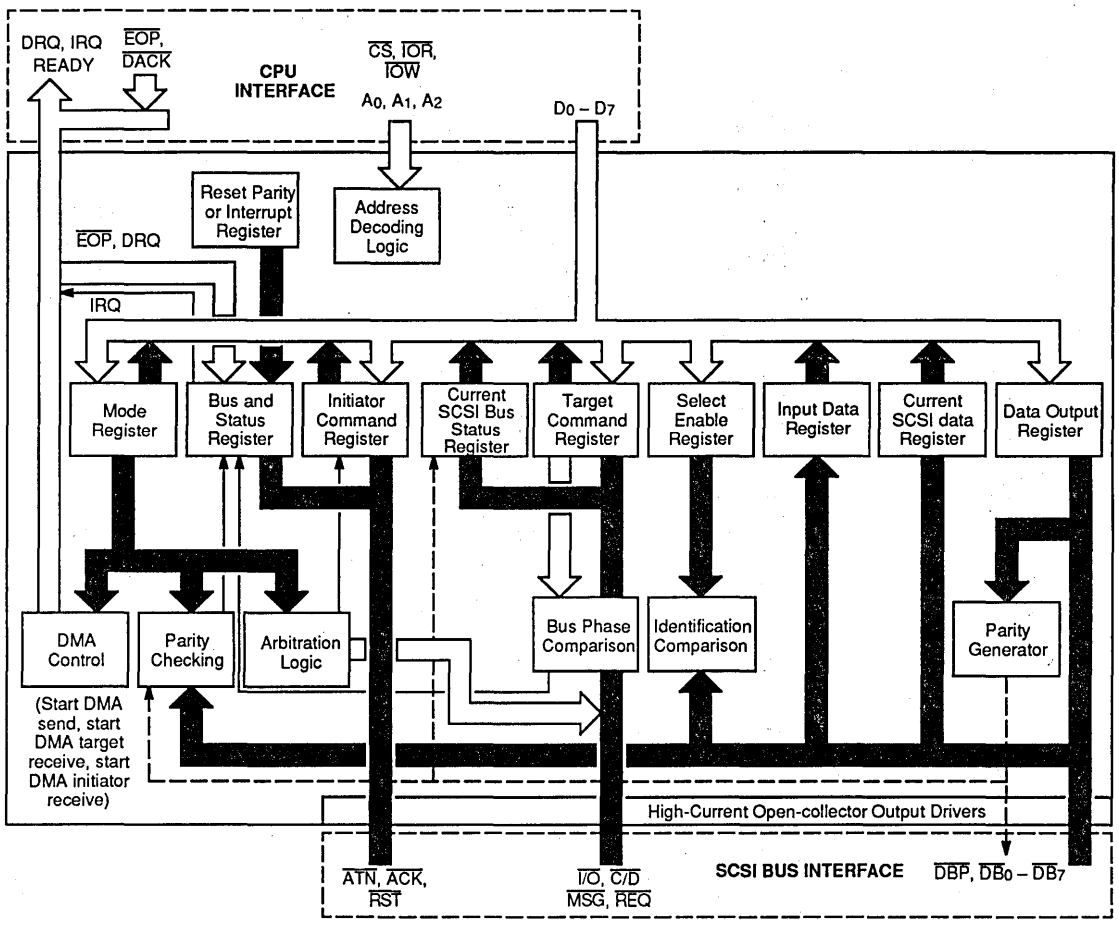
GENERAL DESCRIPTION

The Am53C80A Small Computer Systems Interface (SCSI) Controller is a CMOS device designed to accommodate the SCSI as defined by the ANSI X3T9.2 committee. The Am53C80A operates in both the Initiator and Target roles and can, therefore, be used in host adapter, host port, and formatter designs. This device supports Arbitration, including Reselection. Special high-current open-collector output drivers, capable of sinking 48 mA at 0.5 V, allow for direct connection to the SCSI Bus.

The Am53C80A communicates with the system microprocessor as a peripheral device. The chip is controlled by reading and writing several internal registers which may be addressed as standard or memory-mapped I/O. Minimal processor intervention is required for DMA transfers because the Am53C80A controls the necessary handshake signals. The Am53C80A interrupts the CPU when it detects a bus condition that requires attention. Normal and Block mode DMA is provided to match many popular DMA controllers.

Publication# 10665 Rev. B Amendment/0
Issue Date: November 1991

BLOCK DIAGRAM

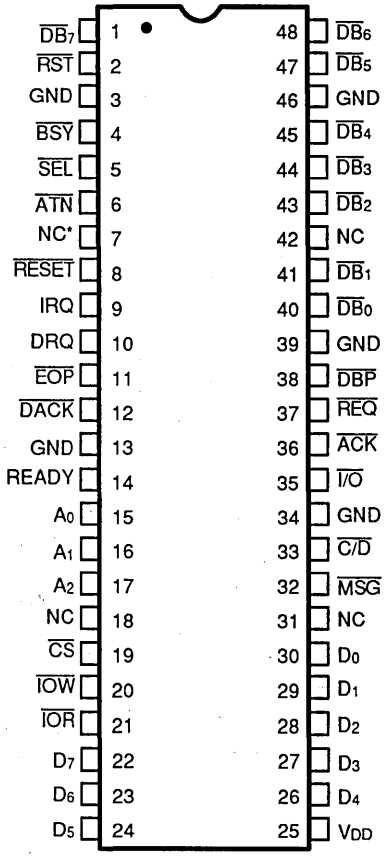


10665B-001A

CONNECTION DIAGRAMS

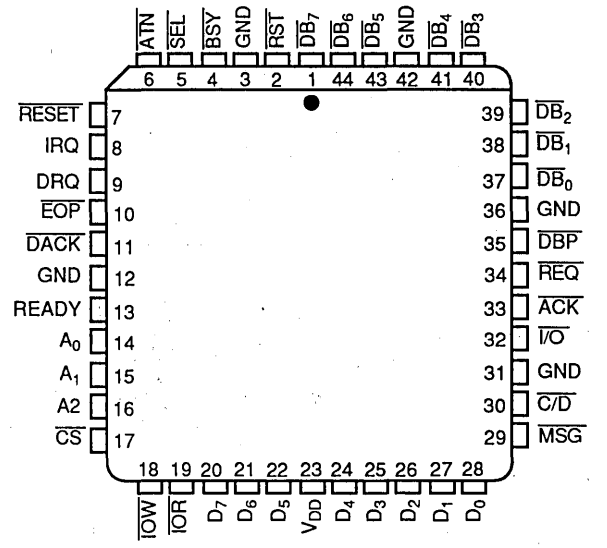
Top View

DIP



10665B-002A

PLCC

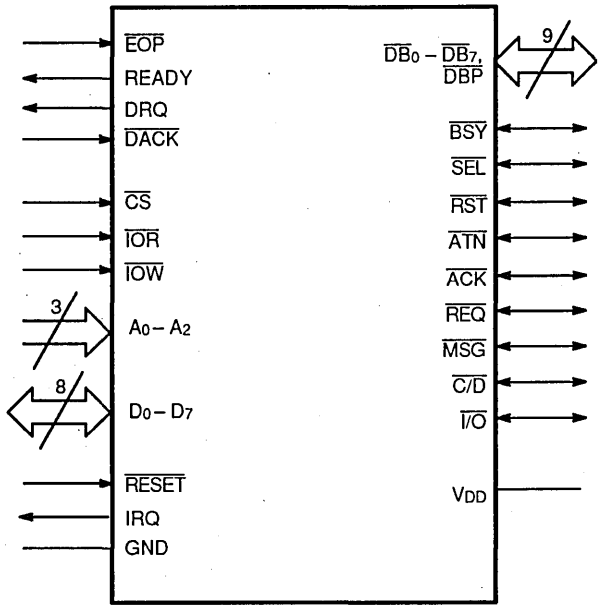


10665B-003A

Notes:

Pin 1 is marked for orientation.
*NC = No Connection

LOGIC SYMBOL

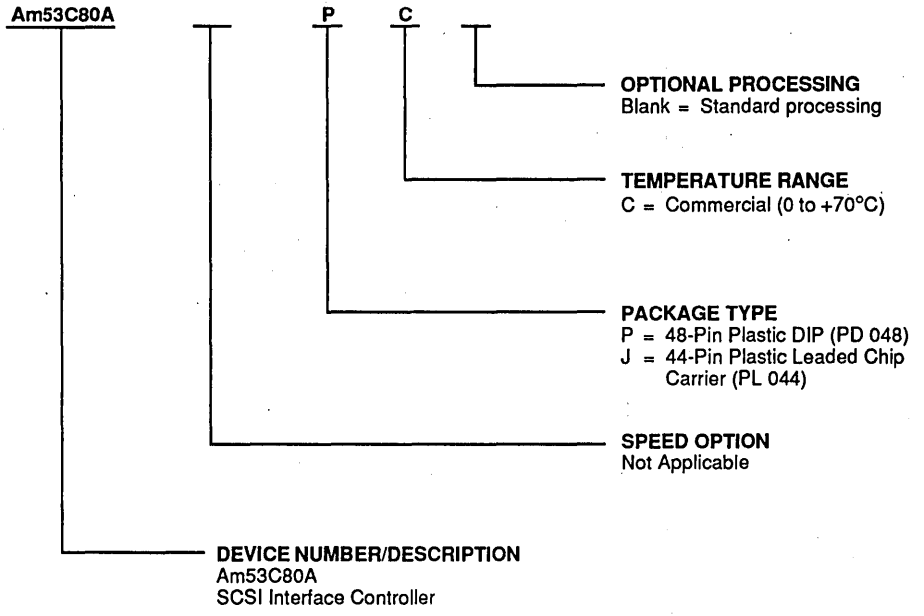


10665B-004A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am53C80A	PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

PIN DESCRIPTION

Microprocessor Interface Signals

A_0–A_2

Address Lines (Input)

These signals are used with $\overline{CS}$, $\overline{IOR}$ or $\overline{IOW}$ to address all internal registers.

$\overline{CS}$

Chip Select (Input, Active Low)

$\overline{CS}$ enables a read or write of the internal register selected by A_0–A_2.

$\overline{DACK}$

DMA Acknowledge (Input, Active Low)

$\overline{DACK}$ resets DRQ and selects the data register for input or output data transfers.

DRQ

DMA Request (Output)

DRQ indicates that the data register is ready to be read or written. DRQ occurs only if DMA mode is TRUE in the Command Register. DRQ is cleared by $\overline{DACK}$.

$D_0 - D_7$

Data Lines (Input/Output; Three-State, Active HIGH)

Bidirectional microprocessor data bus lines.

$\overline{EOP}$

End of Process (Input, Active Low)

$\overline{EOP}$ is used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred, but no additional bytes will be requested.

$\overline{IOR}$

I/O Read (Input, Active LOW)

$\overline{IOR}$ is used to aread asn internal register selected by $\overline{CS}$ and $A_0 - A_2$. It also selects the Input Data Register when used with $\overline{DACK}$.

$\overline{IOW}$

I/O Write (Input, Active LOW)

$\overline{IOW}$ is used to write an internal register selected by $\overline{CS}$ and $A_0 - A_2$. It also selects the Output Data Register when used with $\overline{DACK}$.

IRQ

Interrupt Request (Output)

IRQ alerts a microprocessor of an error condition or an event completion.

READY

Ready (Output)

READY can be used to control the speed of Block mode DMA transfers. This signal goes active to indicate the chip is ready to send/receive data and remains FALSE after a transfer until the last byte is sent or until the DMA MODE bit is reset.

$\overline{RESET}$

Reset (Input, Active Low)

$\overline{RESET}$ clears all the SCSI controller registers. It does not force the SCSI $\overline{RST}$ signal to the active state.

Power Signals

V_{DD}

+5-Volt Power Supply

GND

Ground

SCSI Interface Signals

The following signals are all bidirectional, active-Low, open-collector signals. With 48-mA sink capability, all pins interface directly with the SCSI Bus.

$\overline{ACK}$

Acknowledge (Input/Output; Open Collector, Active Low)

Driven by an Initiator, $\overline{ACK}$ indicates an acknowledgment for a $\overline{REQ}$/$\overline{ACK}$ data-transfer handshake. In the Target role, $\overline{ACK}$ is received as a response to the $\overline{REQ}$ signal.

$\overline{ATN}$

Attention (Input/Output; Open Collector, Active Low)

Driven by an Initiator, $\overline{ATN}$ indicates an Attention condition. This signal is received in the Target role.

$\overline{BSY}$

Busy (Input/Output; Open Collector, Active Low)

This signal indicates that the SCSI Bus is being used and can be driven by both the Initiator and the Target device.

$\overline{C/D}$

Control/Data (Input/Output; Open Collector, Active Low)

A signal driven by the Target, $\overline{C/D}$ indicates Control or Data information is on the Data Bus. This signal is received by the Initiator.

$\overline{I/O}$

Input/Output (Input/Output; Open Collector, Active Low)

$\overline{I/O}$ is a signal driven by a Target which controls the direction of data movement on the SCSI Bus. TRUE indicates input to the intitiator. This signal is also used to distinguish between Selection and Reselection phases.

$\overline{MSG}$

Message (Input/Output; Open Collector, Active Low)

$\overline{MSG}$ is a signal driven by the Target during the Message phase. This signal is received by the Initiator.

$\overline{REQ}$

Request (Input/Output; Open Collector, Active Low)

Driven by a Target, $\overline{REQ}$ indicates a request for a $\overline{REQ}$/$\overline{ACK}$ data-transfer handshake. This signal is received by the Initiator.

$\overline{RST}$

SCSI Bus RESET (Input/Output; Open Collector, Active Low)

The $\overline{RST}$ Signal indicates an SCSI Bus RESET condition. An internal 30 µA pull up transistor is built-in to prevent spurious interrupts.

$\overline{DB_0}$–$\overline{DB_7}$, $\overline{DBP}$

Data Bits, Parity Bit (Input/Output; Open Collector, Active Low)

These eight data bits ($\overline{DB_0}$–$\overline{DB_7}$), plus a parity bit ($\overline{DBP}$) form the Data Bus. $\overline{DB_7}$ is the most significant bit (MSB) and has the highest priority during the Arbitration phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during Arbitration.

$\overline{SEL}$

Select (Input/Output; Open Collector, Active Low)

$\overline{SEL}$ is used by an Initiator to select a Target, or by a Target to reselect an Initiator.

FUNCTIONAL DESCRIPTION

General

The Am53C80A Small Computer Systems Interface (SCSI) device appears as a set of eight registers to the controlling CPU. By reading and writing the appropriate registers, the CPU may initiate any SCSI Bus activity or may sample and assert any signal on the SCSI Bus. This allows the user to implement all or portions of the SCSI protocol in software. These registers are read (written) by activating $\overline{CS}$ with an address on A_0–A_2 and then issuing an $\overline{IOR}$ ($\overline{IOW}$) pulse. This section describes the operation of the internal registers.

Table 1. Register Summary

Address				
A_2	A_1	A_0	R/W	Register Name
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	R/W	Initiator Command
0	1	0	R/W	Mode
0	1	1	R/W	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupts
1	1	1	W	Start DMA Initiator Receive

Data Registers

The data registers are used to transfer SCSI commands, data, status, and message bytes between the microprocessor Data Bus and the SCSI Bus. The Am53C80A does not interpret any information that passes through the data registers. The data registers consist of the transparent Current SCSI Data Register, the Output Data Register, and the Input Data Register.

Current SCSI Data Register—Address 0 (Read Only)

The Current SCSI Data Register is a read-only register that allows the microprocessor to read the active SCSI Data Bus. This is accomplished by activating $\overline{CS}$ with an address on A_2–A_0 of 000 and issuing an $\overline{IOR}$ pulse. If parity checking is enabled, the SCSI Bus parity is checked at the beginning of the read cycle. This register is used during a programmed I/O data read or during Arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during Arbitration.

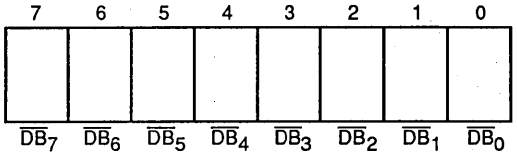


Figure 1. Current SCSI Data Register

Output Data Register—Address 0 (Write Only)

The Output Data Register is a write-only register that is used to send data to the SCSI Bus. This is accomplished by either using a normal CPU write, or under DMA control, by using $\overline{IOW}$ and $\overline{DACK}$. This register is also used to assert the proper ID bits or the SCSI Bus during the Arbitration and Selection phases.

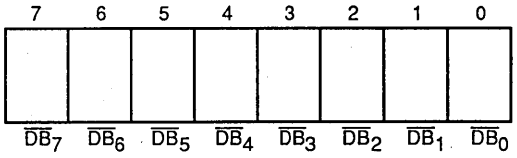


Figure 2. Output Data Register

Input Data Register—Address 6 (Read Only)

The Input Data Register is a read-only register that is used to read latched data from the SCSI Bus. Data is latched either during a DMA Target receive operation when $\overline{ACK}$ goes active or during a DMA Initiator receive when $\overline{REQ}$ goes active. The DMA Mode bit (port 2, bit 1) must be set before data can be latched in the Input Data Register. This register may be read under DMA control using $\overline{IOR}$ and $\overline{DACK}$. Parity is optionally checked when the Input Data Register is loaded.

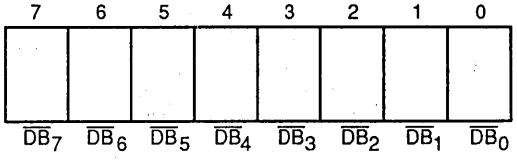


Figure 3. Input Data Register

Initiator Command Register—Address 1 (Read/Write)

The Initiator Command Register is a read/write register that is used to assert certain SCSI Bus signals, to monitor those signals, and to monitor the progress of bus arbitration. Many of these bits are significant only when being used as Initiators; however, most can be used during Target role operation.

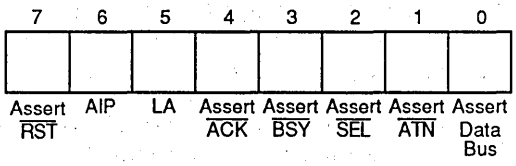


Figure 4-1.
Initiator Command Register—Register Read

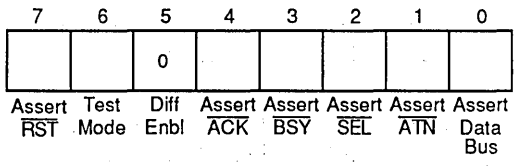


Figure 4-2.
Initiator Command Register—Register Write

The following describes the operation of all bits in the Initiator Command Register.

Bit 7—Assert RST

Whenever a one is written to bit 7 of the Initiator Command Register, the RST signal is asserted on the SCSI Bus. The RST signal will remain asserted until this bit is reset or until an external RESET occurs. After this bit is set (1), IRQ goes active and all internal logic and control registers are reset (except for the interrupt latch and the Assert RST bit). Writing a zero to bit 7 of the Initiator Command Register de-asserts the RST signal. Reading this register simply reflects the status of this bit.

Bit 6—AIP (Arbitration In Progress) (Read Bit)

This bit is used to determine if Arbitration is in progress. For this bit to be active, the Arbitrate bit (port 2, bit 0) must have been set previously. It indicates that a Bus-Free condition has been detected and that the chip has asserted BSY and the contents of the Output Data Register (port 0) onto the SCSI Bus. AIP will remain active until the Arbitrate bit is reset.

Bit 6—Test Mode (Write Bit)

This bit may be written during a test environment to disable all output drivers, effectively removing the Am53C80A from the circuit. Resetting this bit returns the part to normal operation.

Bit 5—LA (Lost Arbitration) (Read Bit)

This bit, when active, indicates that the Am53C80A detected a Bus-Free condition, arbitrated for use of the bus by asserting BSY and its ID on the Data Bus, and lost Arbitration due to SEL being asserted by another bus device. For this bit to be active, the Arbitrate bit (port 2, bit 0) must be active.

Bit 5—Diff Enbl (Differential Enable) (Write Bit)

This bit should be written with a zero for proper operation.

Bit 4—Assert ACK

This bit is used by the bus initiator to assert ACK on the SCSI Bus. In order to assert ACK, the Targetmode bit (port 2, bit 6) must be False. Writing a zero to this bit resets ACK on the SCSI Bus. Reading this register simply reflects the status of this bit.

Bit 3—Assert BSY

Writing a one (1) into this bit position asserts BSY onto the SCSI Bus. Conversely, a zero resets the BSY signal. Asserting BSY indicates a successful selection or reselection and resetting this bit creates a Bus-Disconnect condition. Reading this register simply reflects the status of this bit.

Bit 2—Assert SEL

Writing a one (1) into this bit position asserts SEL onto the SCSI Bus. SEL is normally asserted after Arbitration has been successfully completed. SEL may be de-asserted by resetting this bit to a zero. A read of this register simply reflects the status of this bit.

Bit 1—Assert ATN

ATN may be asserted on the SCSI Bus by setting this bit to a one (1) if the Targetmode bit (port 2, bit 6) is False. ATN is normally asserted by the initiator to request a Message Out bus phase. Note that since Assert SEL and Assert ATN are in the same register, a select with ATN may be implemented with one CPU write. ATN may be de-asserted by resetting this bit to zero. A read of this register simply reflects the status of this bit.

Bit 0—Assert Data Bus

The Assert Data Bus bit, when set, allows the contents of the Output Data Register to be enabled as chip outputs on the signals $\overline{DB_0}$–$\overline{DB_7}$. Parity is also generated and asserted on DBP.

When connected as an initiator, the outputs are only enabled if the Targetmode bit (port 2, bit 6) is False, the received signal I/O is False, and the phase signals (C/D, I/O, and MSG) match the contents of the Assert C/D, Assert I/O, and Assert MSG in the Target Command Register.

This bit should also be set during DMA send operations.

Mode Register—Address 2 (Read/Write)

The Mode Register is used to control the operation of the chip. This register determines whether the Am53C80A operates as an Initiator or a Target, whether DMA transfers are being used, whether parity is checked, and whether interrupts are generated on

various external conditions. This register may be read to check the value of these internal control bits. Figure 5 describes the operation of these control bits.

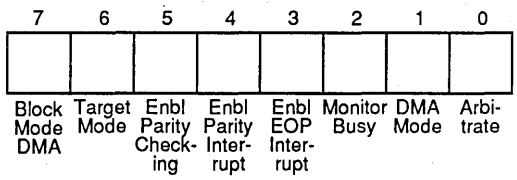


Figure 5. Mode Register

Bit 7—Block Mode DMA

The Block Mode DMA bit controls the characteristics of the DMA DRQ-$\overline{DACK}$ handshake. When this bit is reset (0) and the DMA Mode bit is active (1), the DMA handshake uses the normal interlocked handshake, and the rising edge of $\overline{DACK}$ indicates the end of each byte being transferred. In block mode operations, Block Mode DMA bit set (1), and DMA Mode bit set (1), the end of $\overline{IOR}$ or $\overline{IOW}$ signifies the end of each byte transferred and $\overline{DACK}$ is allowed to remain active throughout the DMA operation. Ready can then be used to request the next transfer.

Bit 6—Targetmode

The Targetmode bit allows the Am53C80A to operate as either an SCSI Bus Initiator, bit reset (0), or as an SCSI Bus Target device, bit set (1). In order for the signals $\overline{ATN}$ and $\overline{ACK}$ to be asserted on the SCSI Bus, the Targetmode bit must be reset (0). In order for the signals $\overline{C/D}$, $\overline{I/O}$, $\overline{MSG}$, and $\overline{REQ}$ to be asserted on the SCSI Bus, the Targetmode bit must be set (1).

Bit 5—Enable Parity Checking

The Enable Parity Checking bit determines whether parity errors will be ignored or saved in the parity error latch. If this bit is reset (0), parity will be ignored. Conversely, if this bit is set (1), parity errors will be saved.

Bit 4—Enable Parity Interrupt

The Enable Parity Interrupt bit, when set (1), will cause an interrupt (IRQ) to occur if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking bit (bit 5) is also enabled (1).

Bit 3—Enable EOP Interrupt

The Enable EOP Interrupt bit, when set (1), causes an interrupt to occur when the $\overline{EOP}$ (End of Process) signal is received from the DMA controller logic.

Bit 2—Monitor Busy

The Monitor Busy bit, when True (1), causes an interrupt to be generated for an unexpected loss of $\overline{BSY}$. When the interrupt is generated due to loss of $\overline{BSY}$, the lower six bits of the Initiator Command Register are reset (0) and all signals are removed from the SCSI Bus.

Bit 1—DMA Mode

The DMA Mode bit is normally used to enable a DMA transfer and must be set (1) prior to writing ports 5 through 7. Ports 5 through 7 are used to start DMA transfers. The Targetmode bit (port 2, bit 6) must be consistent with writes to port 6 and 7 [i.e., set (1) for a write to port 6 and reset (0) for a write to port 7]. The control bit Assert Data Bus (port 1, bit 0) must be True (1) for all DMA send operations. In the DMA mode, $\overline{REQ}$ and $\overline{ACK}$ are automatically controlled.

The DMA Mode bit is not reset upon the receipt of an $\overline{EOP}$ signal. Any DMA transfer may be stopped by writing a zero into this bit location; however, care must be taken not to cause $\overline{CS}$ and $\overline{DACK}$ to be active simultaneously.

Bit 0—Arbitrate

The Arbitrate bit is set (1) to start the Arbitration process. Prior to setting this bit, the Output Data Register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI Bus Arbitration. The Am53C80A will wait for a Bus-Free condition before entering the Arbitration phase. The results of the Arbitration phase may be determined by reading the status bits LA and AIP (port 1, bits 5 and 6, respectively).

Target Command Register—Address 3 (Read/Write)

When connected as a target device, the Target Command Register allows the CPU to control the SCSI Bus Information Transfer phase and/or to assert $\overline{REQ}$ simply by writing this register. The Targetmode bit (port 2, bit 6) must be True (1) for bus assertion to occur. The SCSI Bus phases are described in Table 2.

Table 2. SCSI Information Transfer Phases

Bus Phase	Assert $\overline{I/O}$	Assert $\overline{C/D}$	Assert $\overline{MSG}$
Data Out	0	0	0
Unspecified	0	0	1
Command	0	1	0
Message Out	0	1	1
Data In	1	0	0
Unspecified	1	0	1
Status	1	1	0
Message In	1	1	1

When connected as an Initiator with DMA Mode True, if the phase lines ($\overline{I/O}$, $\overline{C/D}$, and $\overline{MSG}$) do not match the phase bits in the Target Command Register, a phase-mismatch interrupt is generated when $\overline{REQ}$ goes active. In order to send data as an Initiator, the Assert $\overline{I/O}$, Assert $\overline{C/D}$, and Assert $\overline{MSG}$ bits must match the corresponding bits in the Current SCSI Bus Status Register (port 4). The Assert $\overline{REQ}$ bit (bit 3) has no meaning when operating as an Initiator.

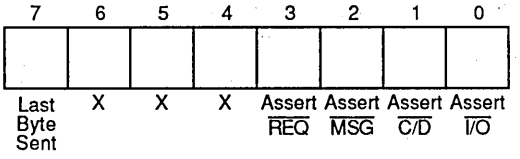


Figure 6. Target Command Register

The Am53C80A uses bit 7 of this register to determine when the last byte of a DMA transfer is sent to the SCSI Bus. This flag is necessary since the end of DMA bit in the Bus and Status Register only reflects when the last byte was received from the DMA.

Current SCSI Bus Status Register—Address 4 (Read Only)

The Current SCSI Bus Status Register is a read-only register that is used to monitor seven SCSI Bus control signals plus the Data Bus parity bit. For example, an Initiator device can use this register to determine the current bus phase and to poll REQ for pending data transfers. This register may also be used to determine why a particular interrupt occurred. Figure 7 describes the Current SCSI Bus Status Register.

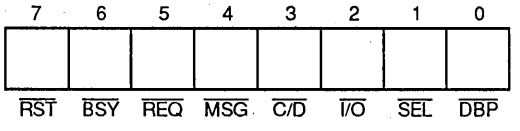


Figure 7. Current SCSI Bus Status Register

Select Enable Register—Address 4 (Write Only)

The Select Enable Register is a write-only register which is used as a mask to monitor a signal ID during a selection attempt. The simultaneous occurrence of the correct ID bit, BSY False, and SEL True will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the Enable Parity Checking bit (port 2, bit 5) is active (1), parity will be checked during selection.

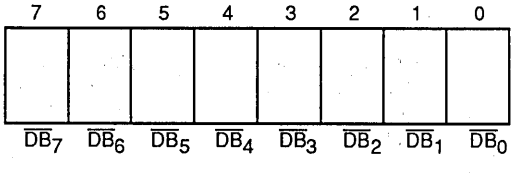


Figure 8. Select Enable Register

Bus and Status Register—Address 5 (Read Only)

The Bus and Status Register is a read-only register that can be used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status Register (ATN and ACK), as well as six other status bits. Individual descriptions of each bit of the Bus and Status Register follow.

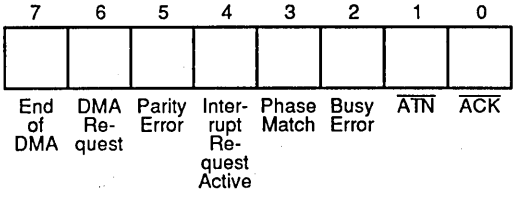


Figure 9. Bus and Status Register

Bit 7—End of DMA Transfer

The End of DMA Transfer bit is set if EOP, DACK, and either IOR or IOW are simultaneously active for at least 100 ns. Since the EOP signal can occur during the last byte sent to the Output Data Register (port 0), the REQ and ACK signals should be monitored to ensure that the last byte has been transferred. This bit is reset when the DMA Mode bit is reset (0) in the Mode Register (port 2).

Bit 6—DMA Request

The DMA Request bit allows the CPU to sample the output pin DRQ. DRQ can be cleared by asserting DACK or by resetting the DMA Mode bit (bit 1) in the Mode Register (port 2). The DRQ signal does not reset when a phase-mismatch interrupt occurs.

Bit 5—Parity Error

This bit is set if a parity error occurs during a data receive or a device selection. The Parity Error bit can only be set (1) if the Enable Parity Check bit (port 2, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 4—Interrupt Request Active

This bit is set if an enabled interrupt condition occurs. It reflects the current state of the IRQ output and can be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 3—Phase Match

The SCSI signals, MSG, C/D, and I/O, represent the current Information Transfer phase. The Phase Match bit indicates whether the current SCSI Bus phase matches the lower 3 bits of the Target Command Register. Phase Match is continuously updated and is only

significant when operating as a Bus Initiator. A phase match is required for data transfers to occur on the SCSI Bus.

Bit 2—Busy Error

The Busy Error bit is active if an unexpected loss of the $\overline{BSY}$ signal has occurred. This latch is set whenever the Monitor Busy bit (port 2, bit 2) is True and $\overline{BSY}$ is False. An unexpected loss of $\overline{BSY}$ will disable any SCSI outputs and will reset the DMA Mode bit (port 2, bit 1).

Bit 1—ATN

This bit reflects the condition of the SCSI Bus control signal $\overline{ATN}$. This signal is normally monitored by the Target device.

Bit 0—ACK

This bit reflects the condition of the SCSI Bus control signal $\overline{ACK}$. This signal is normally monitored by the Target device.

DMA Registers

Three write-only registers are used to initiate all DMA activity. They are Start DMA Send (port 5), Start DMA Target Receive (port 6), and Start DMA Initiator Receive (port 7). Simply writing these registers starts the DMA transfers. Data presented to the Am53C80A on signals D_0–D_7 during the register write is meaningless and has no effect on the operation. Prior to writing these registers, the Block Mode DMA bit (bit 7), the DMA Mode bit (bit 1) and the Targetmode bit (bit 6) in the Mode Register (port 2) must be appropriately set. The individual registers are briefly described as follows.

Start DMA Send—Address 5 (Write Only)

This register is written to initiate a DMA send, from the DMA to the SCSI Bus, for either Initiator or Target role operations. The DMA Mode bit (port 2, bit 1) must be set prior to writing this register.

Start DMA Target Receive—Address 6 (Write Only)

This register is written to initiate a DMA receive—from the SCSI Bus to the DMA—for Target operation only. The DMA Mode bit (bit 1) and the Targetmode bit (bit 6) in the Mode Register (port 2) must both be set (1) prior to writing this register.

Start DMA Initiator Receive—Address 7 (Write Only)

This register is written to initiate a DMA receive—from the SCSI Bus to the DMA, for Initiator operation only. The DMA Mode bit (bit 6) must be False (0) in the Mode Register (port 2) prior to writing this register.

Reset Parity/Interrupt—Address 7 (Read Only)

Reading this register resets the Parity Error bit (bit 5), the Interrupt Request bit (bit 4), and the Busy Error bit (bit 2) in the Bus and Status Register (port 5).

On-Chip SCSI Hardware Support

The Am53C80A is easy to use because of its simple architecture. The chip allows direct control and monitoring of the SCSI Bus by providing a latch for each signal. However, portions of the protocol define timings that are much too quick for traditional microprocessors to control. Therefore, hardware support has been provided for DMA transfers, bus arbitration, phase-change monitoring, bus disconnection, bus reset, parity generation, parity checking, and device selection/reselection.

Arbitration is accomplished using a Bus-Free filter to continuously monitor $\overline{BSY}$. If $\overline{BSY}$ remains inactive for at least 400 ns, then the SCSI Bus is considered free and Arbitration may begin. Arbitration will begin if the bus is free, $\overline{SEL}$ is inactive, and the Arbitration bit (port 2, bit 0) is active. Once arbitration has begun ($\overline{BSY}$ asserted), an arbitration delay of 2.2 µs must elapse before the Data Bus can be examined to determine if Arbitration has been won. This delay must be implemented in the controlling software driver.

The Am53C80A has no clock. Delays such as bus-free delay, bus-set delay, and bus-settle delay are implemented using gate delays. These delays may differ between devices because of inherent process variations, but are well within the proposed ANSI X3T9.2 specification.

Interrupts

The Am53C80A provides an interrupt output (IRQ) to indicate a task completion or an abnormal bus occurrence. The use of interrupts is optional and may be disabled by resetting the appropriate bits in the Mode Register (port 2) or the Select Enable Register (port 4).

When an interrupt occurs, the Bus and Status Register and the Current SCSI Bus Status Register must be read to determine which condition created the interrupt. IRQ can be reset simply by reading the Reset Parity/Interrupt Register (port 7) or by an external chip reset ($\overline{RESET}$ active for 200 ns).

Assuming the Am53C80A has been properly initialized, an interrupt will be generated if the chip is selected or reselected, if an $\overline{EOP}$ signal occurs during a DMA transfer, if an SCSI Bus reset occurs, if a parity error occurs during a data transfer, if a bus phase mismatch occurs, or if an SCSI Bus disconnection occurs.

Selection/Reselection

The Am53C80A can generate a select interrupt if $\overline{SEL}$ is True (1), its device ID is True (1), and $\overline{BSY}$ is False for at least a bus-settle delay (400 ns). If $\overline{I/O}$ is active, this should be considered a reselect interrupt. The correct ID bit is determined by a match in the Select Enable Register (port 4). Only a single bit match is required to generate an interrupt. This interrupt may be disabled by writing zeros into all bits of the Select Enable Register.

If parity is supported, parity should also be good during the selection phase. Therefore, if the Enable Parity bit (port 2, bit 5) is active, then the Parity Error bit should be checked to ensure that a proper selection has occurred. The Enable Parity Interrupt bit need not be set for this interrupt to be generated.

The proposed SCSI specification also requires that no more than two device IDs be active during the selection process. To ensure this, the Current SCSI Data Register (port 0) should be read.

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 10 and 11, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	X	0	X	0
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{ATN}$	$\overline{ACK}$

Figure 10. Bus and Status Register

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 11. Current SCSI Bus Status Register

End of Process (EOP) Interrupt

An End of Process ($\overline{EOP}$) signal which occurs during a DMA transfer (DMA Mode True) will set the End of DMA Status bit (port 5, bit 7) and will optionally generate an interrupt if the Enable EOP Interrupt bit (port 2, bit 3) is True. The $\overline{EOP}$ pulse will not be recognized (End Of DMA bit set) unless $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are concurrently active for at least 100 ns. DMA transfers can still occur if $\overline{EOP}$ was not asserted at the correct time. This interrupt can be disabled by resetting the Enable EOP Interrupt bit.

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for this interrupt are shown in Figures 12 and 13, respectively.

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	X
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{ATN}$	$\overline{ACK}$

Figure 12. Bus and Status Register

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 13. Current SCSI Bus Status Register

The End of DMA bit is used to determine when a block transfer is complete. Receive operations are complete when there is no data left in the chip and no additional handshakes occurring. The only exception to this is receiving data as an Initiator when the Target opts to send additional data for the same phase. In this case, $\overline{REQ}$ goes active and the new data is present in the Input Data Register. Since a phase-mismatch interrupt will not occur, $\overline{REQ}$ and $\overline{ACK}$ need to be sampled to determine that the Target is attempting to send more data.

For send operations, the End of DMA bit is set when the DMA finishes its transfer, but the SCSI transfer may still be in progress. If connected as a Target, $\overline{REQ}$ and $\overline{ACK}$ should be sampled until both are False. If connected as an Initiator, a phase change interrupt can be used to signal the completion of the previous phase. It is possible for the Target to request additional data for the same phase. In this case, a phase change will not occur and both $\overline{REQ}$ and $\overline{ACK}$ must be sampled to determine when the last byte was transferred.

SCSI Bus Reset

The Am53C80A generates an interrupt when the $\overline{RST}$ signal transitions to True. The device releases all bus signals within a bus-clear delay (800 ns) of this transition. This interrupt also occurs after setting the Assert $\overline{RST}$ bit (port 1, bit 7). This interrupt cannot be disabled. (Note: $\overline{RST}$ is not latched in bit 7 of the Current SCSI Bus Status Register and may not be active when this port is read. For this case, the Bus Reset interrupt may be determined by default.)

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 14 and 15, respectively.

7	6	5	4	3	2	1	0
0	X	0	1	X	0	X	X
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{ATN}$	$\overline{ACK}$

Figure 14. Bus and Status Register

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 15. Current SCSI Bus Status Register

Parity Error

An interrupt is generated for a received parity error if the Enable Parity Check (bit 5) and the Enable Parity Interrupt (bit 4) bits are set (1) in the Mode Register (port 2). Parity is checked during a read of the Current SCSI Data Register (port 0) and during a DMA receive operation. A parity error can be detected without generating an interrupt by disabling the Enable Parity Interrupt bit and checking the Parity Error flag (port 5, bit 5).

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 16 and 17, respectively.

7	6	5	4	3	2	1	0
0	X	1	1	1	0	X	X
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{ATN}$	$\overline{ACK}$

Figure 16. Bus and Status Register

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 17. Current SCSI Bus Status Register

Bus Phase Mismatch

The SCSI phase lines are composed of the signals $\overline{I/O}$, $\overline{C/D}$, and $\overline{MSG}$. These signals are compared with the corresponding bits in the Target Command Register: Assert $\overline{I/O}$ (bit 0), Assert $\overline{C/D}$ (bit 1), and Assert $\overline{MSG}$ (bit 2). The comparison occurs continually and is reflected in the Phase Match bit (bit 3) of the Bus and Status Register (port 5). If the DMA Mode bit (port 2, bit 1) is active and a phase mismatch occurs when $\overline{REQ}$ changes from False to True, an interrupt (IRQ) is generated.

A phase mismatch prevents the recognition of $\overline{REQ}$ and removes the chip from the bus during an initiator send operation [$\overline{DB_0}$–$\overline{DB_7}$ and $\overline{DBP}$ will not be driven even though the Assert Data Bus bit (port 1, bit 0) is active]. This interrupt is only significant when connected as an initiator and may be disabled by resetting the DMA Mode bit. (Note: It is possible for this interrupt to occur when connected as a Target if another device is driving the phase lines to a different state.)

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed in Figures 18 and 19, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	0	0	X	0
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{ATN}$	$\overline{ACK}$

Figure 18. Bus and Status Register

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{DBP}$

Figure 19. Current SCSI Bus Status Register

Loss of $\overline{BSY}$

If the Monitor Busy bit (bit 2) in the Mode Register (port 2) is active, an interrupt will be generated if the $\overline{BSY}$ signal goes False for at least a bus-settle delay (400 ns). This interrupt may be disabled by resetting the Monitor Busy bit. Register values are displayed in Figures 20 and 21.

7	6	5	4	3	2	1	0
0	0	0	1	X	1	0	0
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{ATN}$	$\overline{ACK}$

Figure 20. Bus and Status Register

7	6	5	4	3	2	1	0
0	0	0	X	X	X	0	0
RST	BSY	REQ	MSG	C/D	I/O	SEL	DBP

Figure 21. Current SCSI Bus Status Register

Reset Conditions

Three possible reset situations exist with the Am53C80A.

Hardware Chip Reset

When the signal RST is active for at least 200 ns, the Am53C80A device is re-initialized and all internal logic and control registers of SCSI are cleared. This is a chip reset only and does not create an SCSI Bus-Reset condition.

SCSI Bus Reset (RST) Received

When an SCSI RST signal is received, an IRQ interrupt is generated and a SCSI chip reset is performed. All internal logic and registers are cleared, except for the IRQ interrupt latch and the Assert RST bit (bit 7) in the Initiator Command Register (port 1). (Note: The RST signal may be sampled by reading the Current SCSI Bus Status Register (port 4); however, this signal is not latched and may not be present when this port is read.)

SCSI Bus Reset (RST) Issued

If the CPU sets the Assert RST bit (bit 7) in the Initiator Command Register (port 1), the RST signal goes active on the SCSI Bus and an internal reset is performed. Again, all internal logic and registers are cleared except for the IRQ interrupt latch and the Assert RST bit (bit 7) in the Initiator Command Register (port 1). The RST signal will continue to be active until the Assert RST bit is reset or until a hardware reset occurs.

Data Transfers

Data may be transferred between SCSI Bus devices in one of four modes: (1) Programmed I/O, (2) Normal DMA, (3) Block Mode DMA, or (4) Pseudo DMA. The following sections describe these modes in detail. (Note: For all data transfer operations, DACK and CS should never be active simultaneously.)

Programmed I/O Transfers

Programmed I/O is the most primitive form of data transfer. The REQ and ACK handshake signals are individually monitored and asserted by reading and writing the appropriate register bits. This type of transfer is normally used when transferring small blocks of data, such as command blocks or message and status bytes.

An Initiator send operation would begin by setting the C/D, I/O, and MSG bits in the Target Command Register to the correct state so that a phase match exists. In addition to the phase match condition, it is necessary for the Assert Data Bus bit (port 1, bit 0) to be True and the received I/O signal to be False for the Am53C80A to send data.

For each transfer, the data is loaded into the Output Data Register (port 0). The CPU then waits for the REQ bit (port 4, bit 5) to become active. Once REQ goes active, the Phase Match bit (port 5, bit 3) is checked and the Assert ACK bit (port 1, bit 4) is set. The REQ bit is sampled until it becomes False and the CPU resets the Assert ACK bit to complete the transfer.

Normal DMA Mode

DMA transfers are normally used for large block transfers. The SCSI chip outputs a DMA request (DRQ) whenever it is ready for a byte transfer. External DMA logic uses this DRQ signal to generate DACK and an IOR or an IOW pulse to the Am53C80A. DRQ goes inactive when DACK is asserted, and DACK goes inactive some time after the minimum read or write pulse width. This process is repeated for every byte. For this mode, DACK should not be allowed to cycle unless a transfer is taking place.

Block Mode DMA

Some popular DMA controllers such as the Am9517A provide a Block Mode DMA transfer. This type of transfer allows the DMA controller to transfer blocks of data without relinquishing the use of the Data Bus to the CPU after each byte is transferred; thus, faster transfer rates are achieved by eliminating the repetitive access and release of the CPU Bus.

If the Block Mode DMA bit (port 2, bit 7) is active, the Am53C80A will begin the transfer by asserting DRQ. The DMA controller then asserts DACK for the remainder of the block transfer. DRQ goes inactive for the duration of the transfer.

Non-Block Mode DMA transfers end when DACK goes False, whereas Block mode transfers end when IOR or IOW becomes inactive. Since this is the case, DMA transfers may be started sooner in a Block Mode transfer.

To obtain optimum performance in Block Mode operation, the DMA logic may optionally use the normal DMA mode interlocking handshake. READY is still available to throttle the DMA transfer, but DRQ is 30 to 40 ns faster than READY and may be used to start the cycle sooner.

The methods described under "Halting a DMA Operation" apply for all DMA operations.

Pseudo DMA Mode

To avoid the tedium of monitoring and asserting the request/acknowledge handshake signals for programmed I/O transfers, the system may be designed to implement a pseudo DMA mode. This mode is implemented by programming the Am53C80A to operate in the DMA mode, but using the CPU to emulate the DMA handshake.

DRQ may be detected by polling the DMA Request bit (bit 6) in the Bus and Status Register (port 5), by sampling the signal through an external port, or by using it to generate a CPU interrupt. Once DRQ is detected, the CPU can perform a read or write data transfer. This CPU read/write is externally decoded to generate the appropriate $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals.

Often, external decoding logic is necessary to generate the Am53C80A $\overline{CS}$ signal. This same logic may be used to generate $\overline{DACK}$ at no extra system cost and provide an increased performance in programmed I/O transfers.

Halting a DMA Operation

The $\overline{EOP}$ signal is not the only way to halt a DMA transfer. A bus phase mismatch or a reset of the DMA Mode bit (port 2, bit 1) can also terminate a DMA cycle for the current bus phase.

Using the $\overline{EOP}$ Signal

If $\overline{EOP}$ is used, it should be asserted for at least 100 ns while $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active. Note, however, that if $\overline{IOR}$ or $\overline{IOW}$ is not active an interrupt will be generated, but the DMA activity will continue. The $\overline{EOP}$ signal does not reset the DMA Mode bit. Since the $\overline{EOP}$ signal can occur during the last byte sent to the Output Data Register (port 0), the $\overline{REQ}$ and $\overline{ACK}$ signals should be monitored to ensure that the last byte has transferred.

Bus Phase Mismatch Interrupt

A bus phase mismatch interrupt may be used to halt the transfer if operating as an Initiator. Using this method frees the host from maintaining a data length counter and frees the DMA logic from providing the $\overline{EOP}$ signal. If performing an Initiator send operation, the Am53C80A requires $\overline{DACK}$ to cycle before $\overline{ACK}$ goes inactive. Since phase changes cannot occur if $\overline{ACK}$ is active, either $\overline{DACK}$ must be cycled after the last byte is sent or the DMA Mode bit must be reset in order to receive the phase mismatch interrupt.

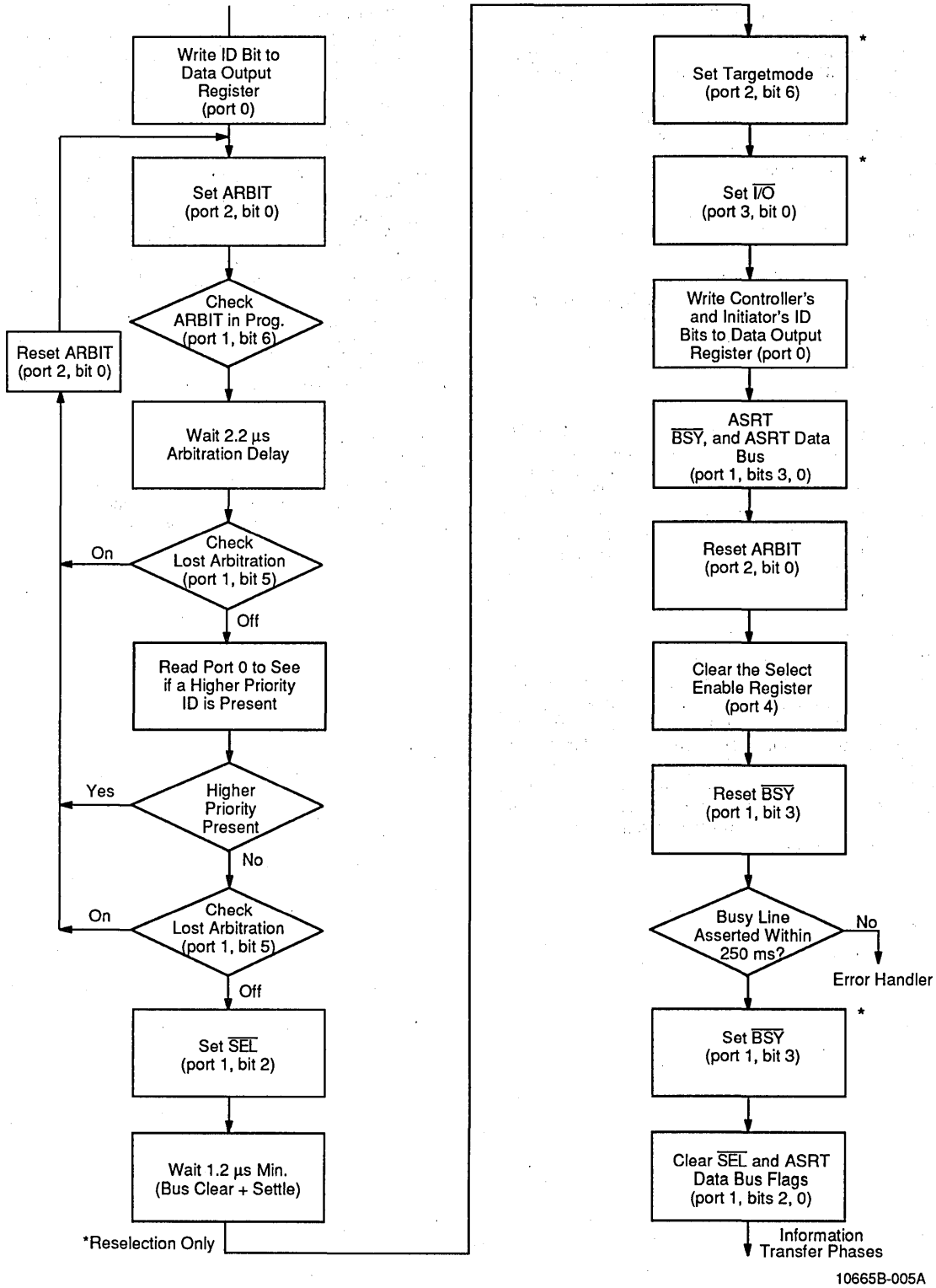
Resetting the DMA Mode Bit

A DMA operation may be halted at any time simply by resetting the DMA Mode bit. It is recommended that the DMA Mode bit be reset after receiving an $\overline{EOP}$ or bus phase-mismatch interrupt. The DMA Mode bit must then be set before writing any of the start DMA registers for subsequent bus phases.

If resetting the DMA Mode bit is used instead of $\overline{EOP}$ for Target role operation, then care must be taken to reset this bit at the proper time. If receiving data as a Target device, the DMA Mode bit must be reset once the last DRQ is received and before $\overline{DACK}$ is asserted to prevent an additional $\overline{REQ}$ from occurring. Resetting this bit causes DRQ to go inactive. However, the last byte received remains in the Input Data Register and may be obtained either by performing a normal CPU read or by cycling $\overline{DACK}$ and $\overline{IOR}$. In most cases $\overline{EOP}$ is easier to use when operating as a Target device.

Flowcharts

Flowcharts are provided (see Figures 22 through 25) as a guideline to facilitate your firmware development. Firmware will vary depending on the application and the level of the SCSI protocol being supported.



10665B-005A

Figure 22. Arbitration and (Re) Selection

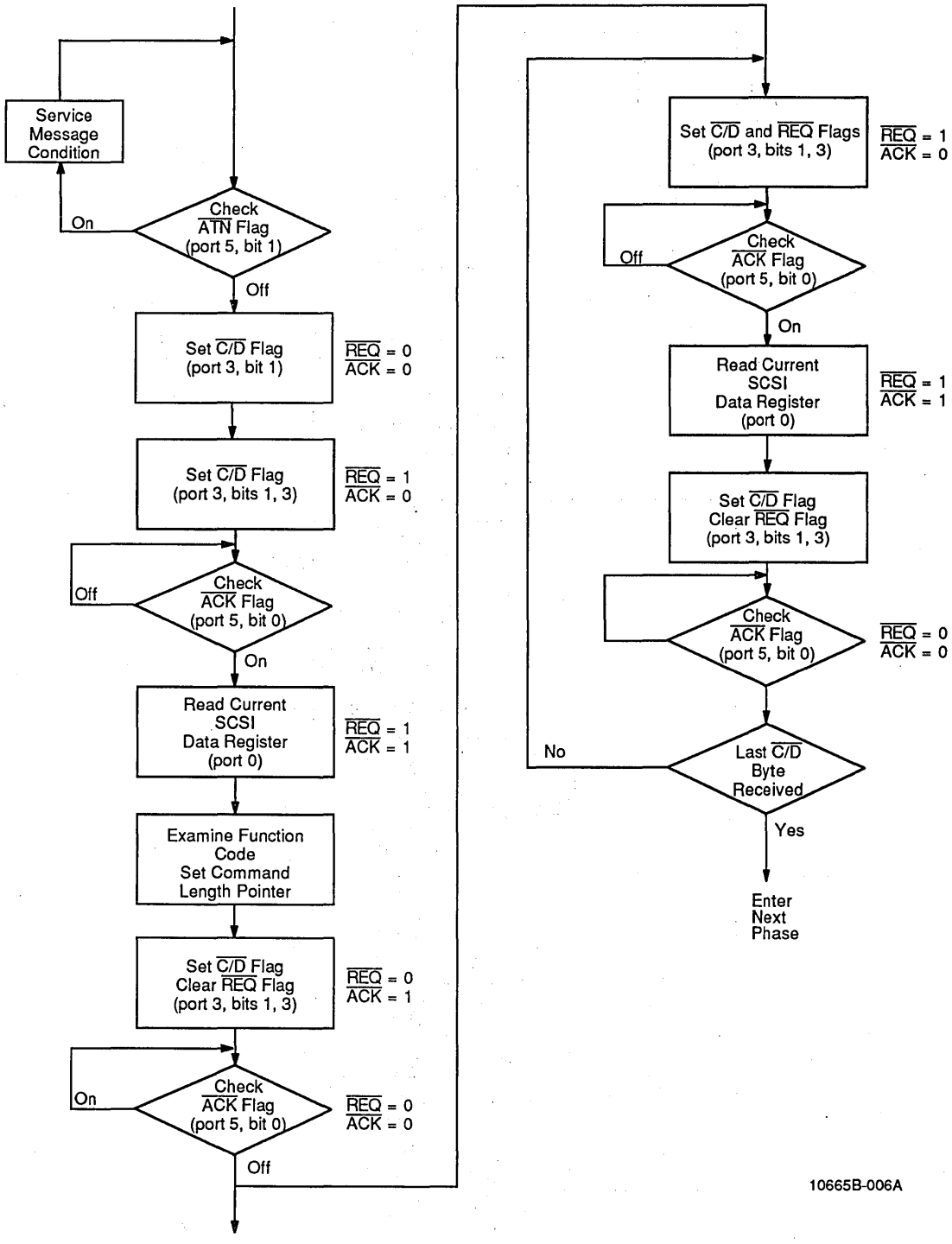


Figure 23. Command Transfer Phase (Target)

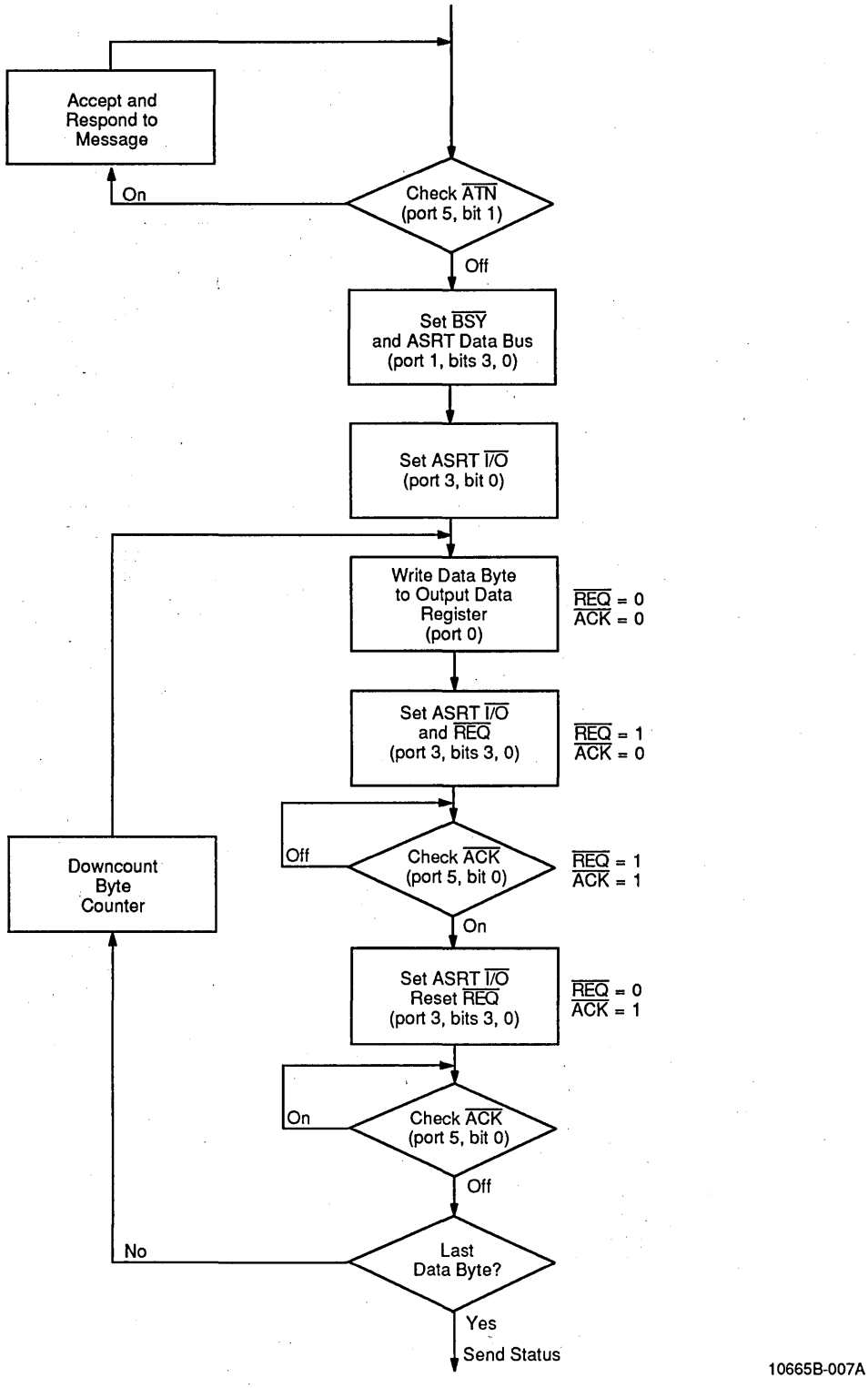


Figure 24. Data Transfer to Host via Programmed I/O

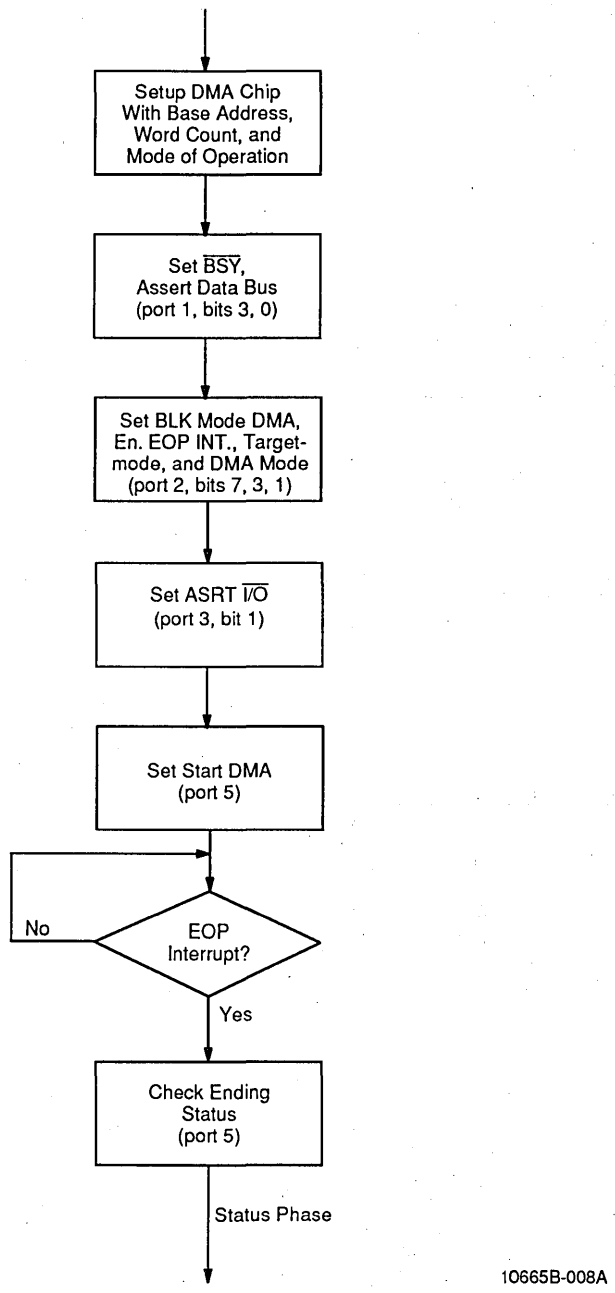


Figure 25. Data Transfer via DMA

Read **Write**

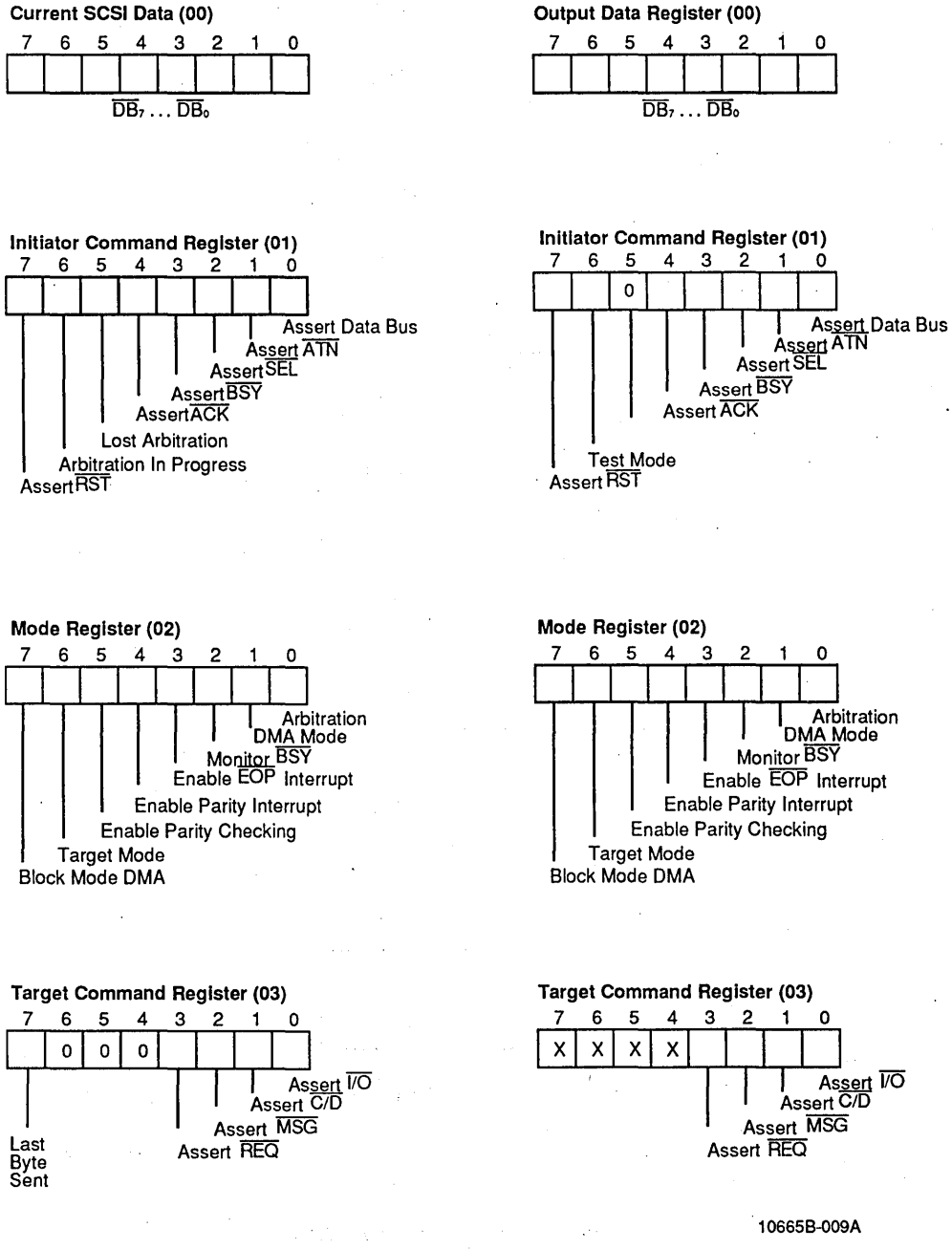
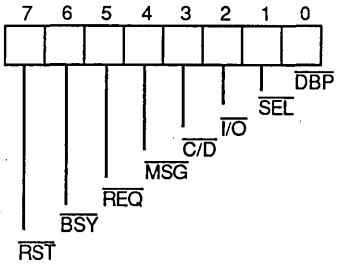


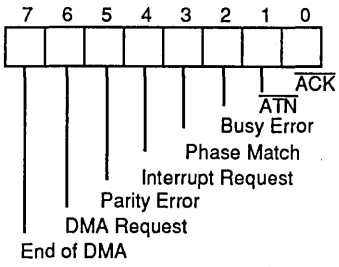
Figure 26. Register Reference Chart

Read

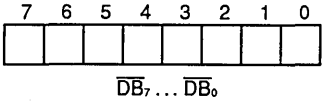
Current SCSI Bus Status (04)



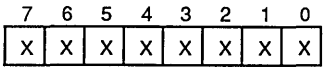
Bus and Status Register (05)



Input Data Register (06)

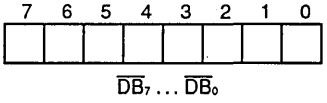


Reset Parity/Interrupt (07)

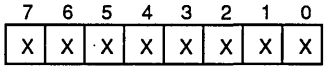


Write

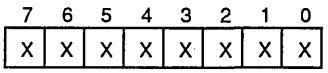
Select Enable Register (04)



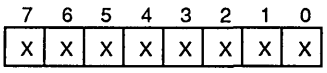
Start DMA Send (05)



Start DMA Target Receive (06)



Start DMA Initiator Receive (07)



10665B-010A

Note:
X = Don't Care

Figure 26. Register Reference Chart (continued)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Supply Voltage on Any Pin with Respect to Ground	−0.5 to +7.0 V
Power Dissipation	100 mW

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

Parameter Description	Test Conditions	Min.	Max.	Unit
Input Signal Requirements				
HIGH-Level, Input V_{IH}		2.0	5.25	V
LOW-Level, Input V_{IL}		−0.3	0.8	V
HIGH-Level Input Current, I_{IH}, on:				
SCSI Bus Pin except $\overline{RST}$	V_{IH} = 5.25 V, V_{IL} = 0		50	µA
All Other Pins			10	
LOW-Level Input Current, I_{IL}, on:				
SCSI Bus Pins except $\overline{RST}$	V_{IH} = 5.25 V, V_{IL} = 0		−50	µA
All Other Pins			−10	
Output Signal Requirements				
HIGH-Level Output on All Pins	V_{DD} = 4.75 V, I_{OH} = −3.0 mA	2.4		V
LOW-Level Output on:				
SCSI Bus Pins	V_{DD} = 4.75 V, I_{OL} = 48.0 mA		0.5	V
All Other Pins	V_{DD} = 4.75 V, I_{OL} = 7.0 mA		0.5	V

KEY TO SWITCHING WAVEFORMS

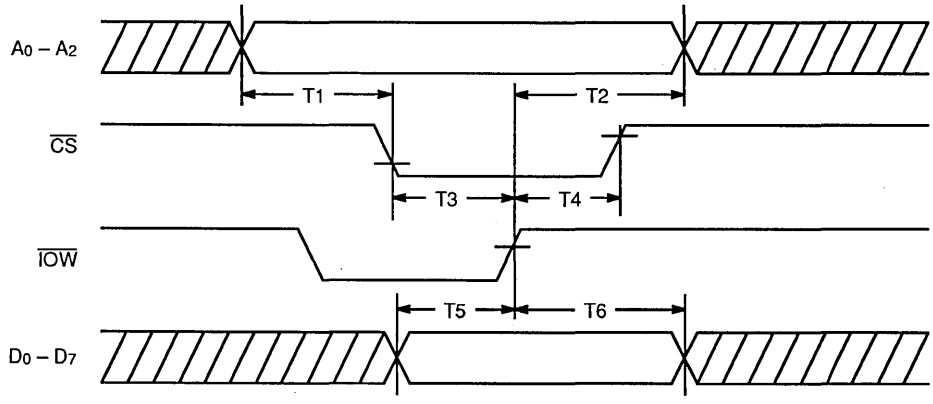
WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	Address Setup to Write Enable*	10		ns
T2	Address Hold from End Write Enable*	0		ns
T3	Write Enable Width*	10		ns
T4	Chip Select Hold from End of $\overline{IOW}$	0		ns
T5	Data Setup to End of Write Enable*	10		ns
T6	Data Hold Time from End of $\overline{IOW}$	10		ns

*Write Enable is the occurence of $\overline{IOW}$ and $\overline{CS}$.



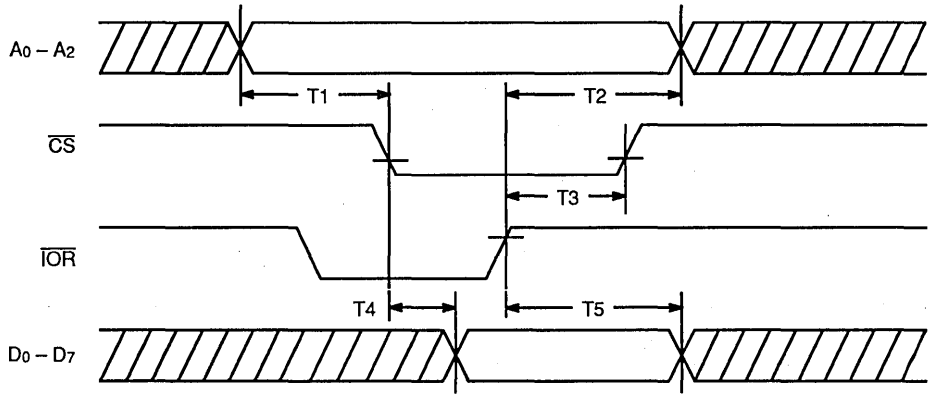
10665B-011B

CPU Write Cycle

SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	Address Setup to Read Enable*	10		ns
T2	Address Hold from End Read Enable*	0		ns
T3	Chip Select Hold from End of $\overline{IOR}$	0		ns
T4	Data Access Time from Read Enable*		40	ns
T5	Data Hold Time from End of $\overline{IOR}$	20		ns

*Read Enable is the occurence of $\overline{IOR}$ and $\overline{CS}$.



10665B-012A

CPU Read Cycle

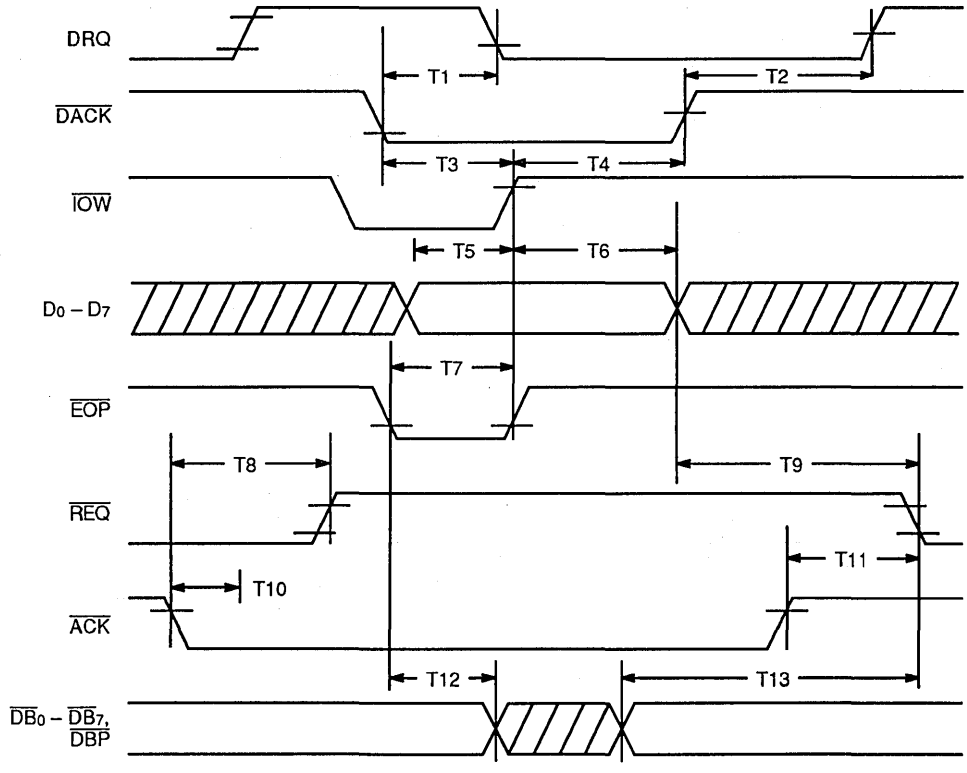
SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		35	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	Write Enable Width*	40		ns
T4	$\overline{DACK}$ Hold from End of $\overline{IOW}$	0		ns
T5	Data Setup to End of Write Enable*	5		ns
T6	Data Hold Time from End of $\overline{IOW}$	5		ns
T7	Width of $\overline{EOP}$ Pulse (Note 1)	40		ns
T8	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		85	ns
T9	$\overline{REQ}$ from End of $\overline{DACK}$ ($\overline{ACK}$ FALSE)		40	ns
T10	$\overline{ACK}$ TRUE to DRQ TRUE (Target)		90	ns
T11	$\overline{REQ}$ from End of $\overline{ACK}$ ($\overline{DACK}$ FALSE)		30	ns
T12	Data Hold from Write Enable	0		ns
T13	Data Setup to $\overline{REQ}$ TRUE (Target)	40		ns

*Write Enable is the occurence of $\overline{IOW}$ and $\overline{DACK}$.

Note:

1. $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$ must be concurrently TRUE for at least T7 for proper recognition of the $\overline{EOP}$ pulse.



10665B-013B

DMA Write (Non-Block Mode) Target Send Cycle

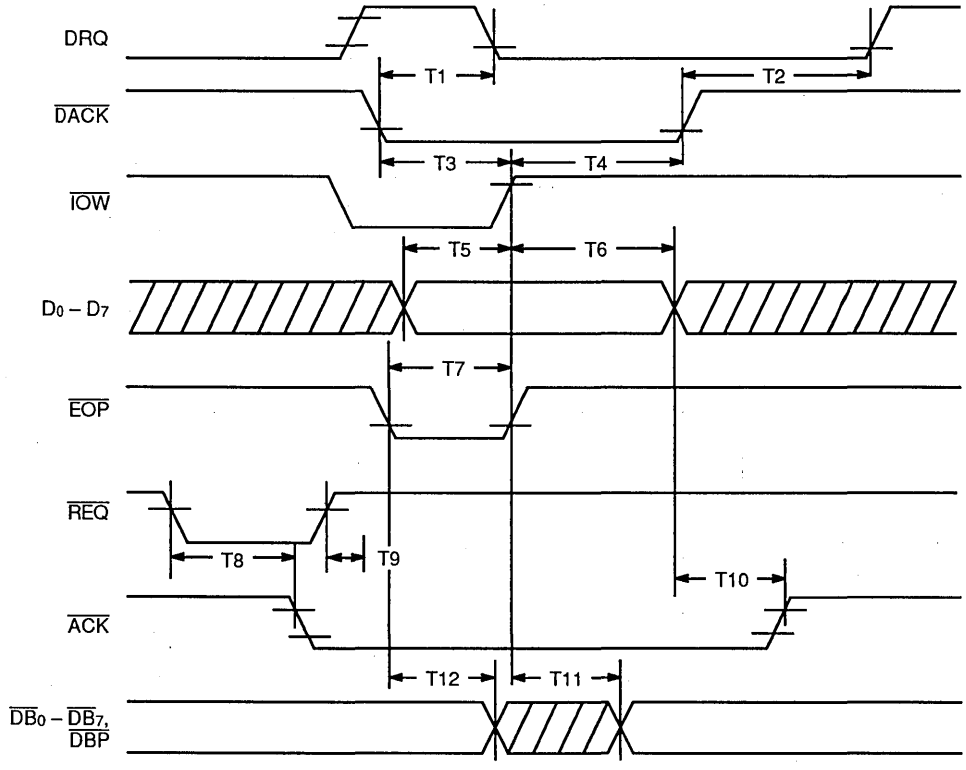
SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		35	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	Write Enable Width*	40		ns
T4	$\overline{DACK}$ Hold from End of $\overline{IOW}$	0		ns
T5	Data Setup to End of Write Enable*	10		ns
T6	Data Hold Time from End of $\overline{IOW}$	10		ns
T7	Width of $\overline{EOP}$ Pulse (Note 1)	40		ns
T8	$\overline{REQ}$ TRUE to $\overline{ACK}$ TRUE		85	ns
T9	$\overline{REQ}$ FALSE to DRQ TRUE		45	ns
T10	$\overline{DACK}$ FALSE to $\overline{ACK}$ FALSE		45	ns
T11	$\overline{IOW}$ FALSE to Valid SCSI Data		65	ns
T12	Data Hold from Write Enable	0		ns

*Write Enable is the occurence of $\overline{IOW}$ and $\overline{DACK}$.

Note:

1. $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$ must be concurrently TRUE for at least T7 for proper recognition of the $\overline{EOP}$ pulse.



10665B-014B

DMA Write (Non-Block Mode) Initiator Send Cycle

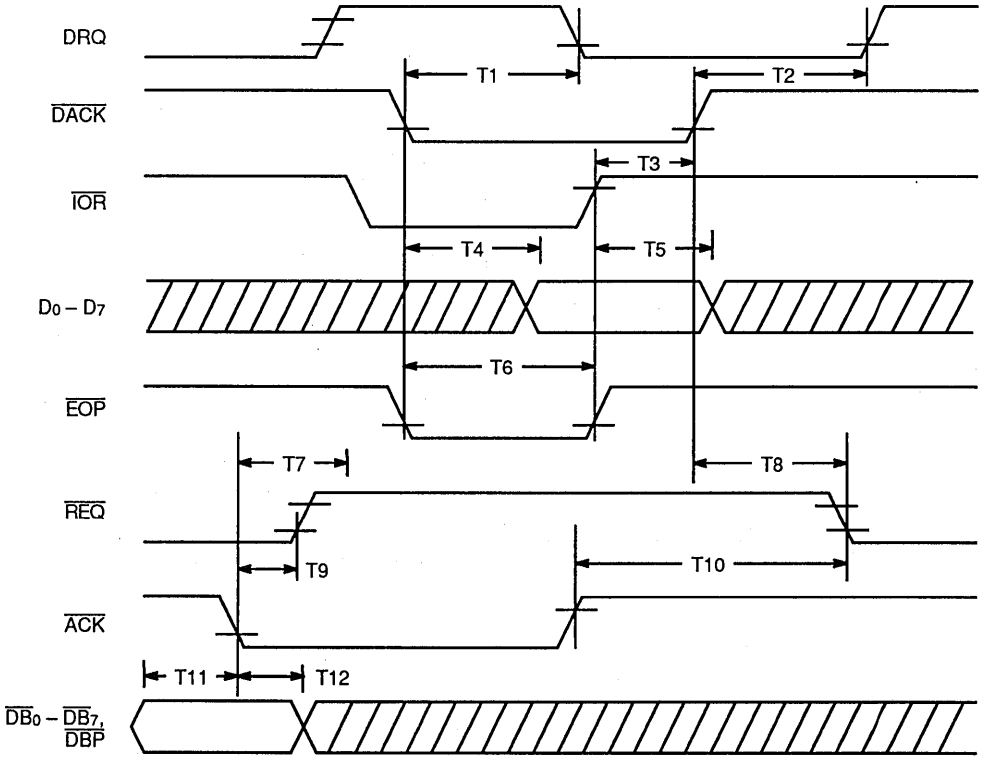
SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		35	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{IOR}$	0		ns
T4	Data Access Time from Read Enable*		20	ns
T5	Data Hold Time from End of $\overline{IOR}$	0		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	40		ns
T7	$\overline{ACK}$ TRUE to DRQ TRUE		90	ns
T8	$\overline{DACK}$ FALSE to $\overline{REQ}$ TRUE ($\overline{ACK}$ FALSE)		40	ns
T9	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		90	ns
T10	$\overline{ACK}$ FALSE to $\overline{REQ}$ TRUE ($\overline{DACK}$ FALSE)		35	ns
T11	Data Setup Time to $\overline{ACK}$	10		ns
T12	Data Hold Time from $\overline{ACK}$	65		ns

*Read Enable is the occurence of $\overline{IOR}$ and $\overline{DACK}$.

Note:

1. $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$ must be concurrently TRUE for at least T6 for proper recognition of the $\overline{EOP}$ pulse.



10665B-015B

DMA Read (Non-Block Mode)Target Receive Cycle

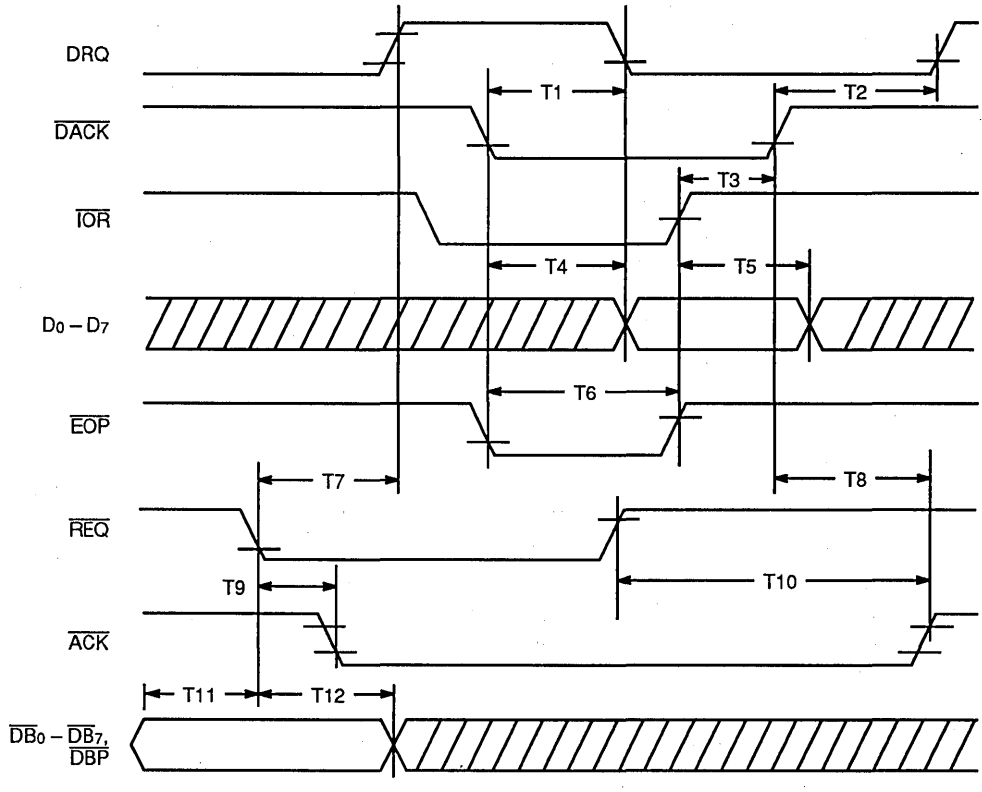
SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		35	ns
T2	$\overline{DACK}$ FALSE to DRQ TRUE	30		ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{IOR}$	0		ns
T4	Data Access Time from Read Enable*		20	ns
T5	Data Hold Time from End of $\overline{IOR}$	0		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	40		ns
T7	$\overline{REQ}$ TRUE to DRQ TRUE		95	ns
T8	$\overline{DACK}$ FALSE to $\overline{ACK}$ FALSE ($\overline{REQ}$ FALSE)		40	ns
T9	$\overline{REQ}$ TRUE to $\overline{ACK}$ TRUE		85	ns
T10	$\overline{REQ}$ FALSE to $\overline{ACK}$ FALSE ($\overline{DACK}$ FALSE)		35	ns
T11	Data Setup Time to $\overline{REQ}$	10		ns
T12	Data Hold Time from $\overline{REQ}$	65		ns

*Read Enable is the occurence of $\overline{IOR}$ and $\overline{DACK}$.

Note:

1. $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$ must be concurrently TRUE for at least T6 for proper recognition of the $\overline{EOP}$ pulse.



10665B-016B

DMA Read (Non-Block Mode) Initiator Receive Cycle

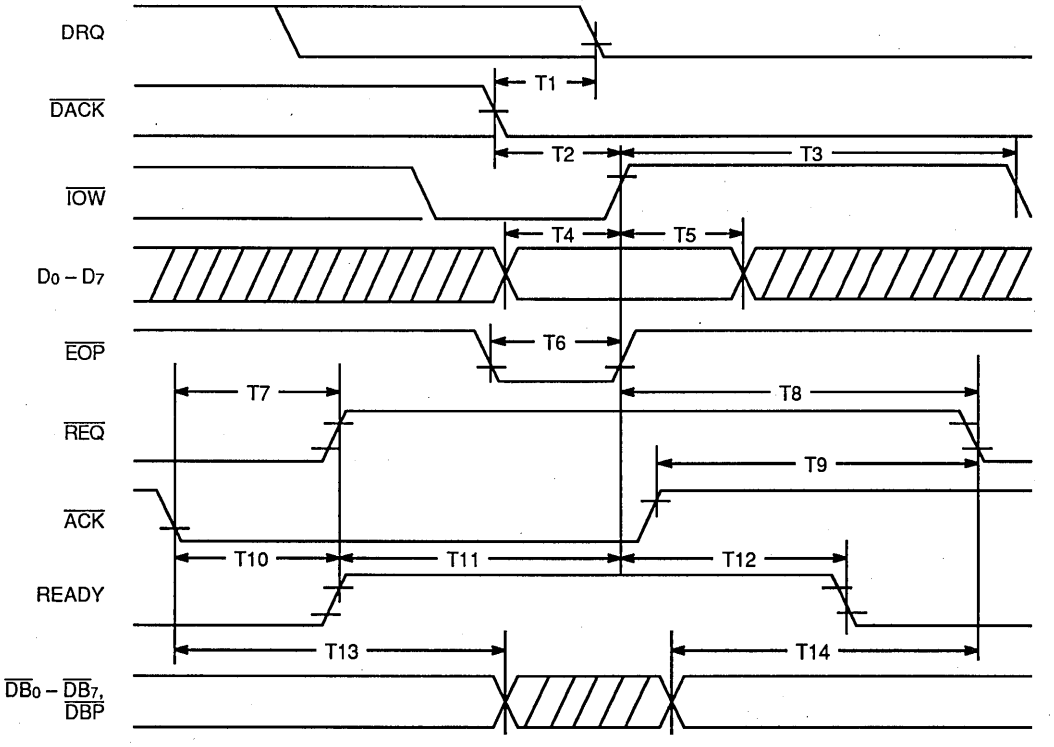
SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		35	ns
T2	Write Enable Width*	40		ns
T3	Write Recovery Time	80		ns
T4	Data Setup to End of Write Enable*	5		ns
T5	Data Hold Time from End of $\overline{IOW}$	5		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	40		ns
T7	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		85	ns
T8	$\overline{REQ}$ from End of $\overline{IOW}$ ($\overline{ACK}$ FALSE)		50	ns
T9	$\overline{REQ}$ from End of $\overline{ACK}$ ($\overline{IOW}$ FALSE)		40	ns
T10	$\overline{ACK}$ TRUE to READY TRUE		100	ns
T11	READY TRUE to $\overline{IOW}$ FALSE	45		ns
T12	$\overline{IOW}$ FALSE to READY FALSE	20	60	ns
T13	Data Hold to $\overline{ACK}$ TRUE	0		ns
T14	Data Setup to $\overline{REQ}$ TRUE	40		ns

*Write Enable is the occurence of $\overline{IOW}$ and $\overline{DACK}$.

Note:

1. $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$ must be concurrently TRUE for at least T6 for proper recognition of the $\overline{EOP}$ pulse.



10665B-017B

DMA Write (Block Mode) Target Send Cycle

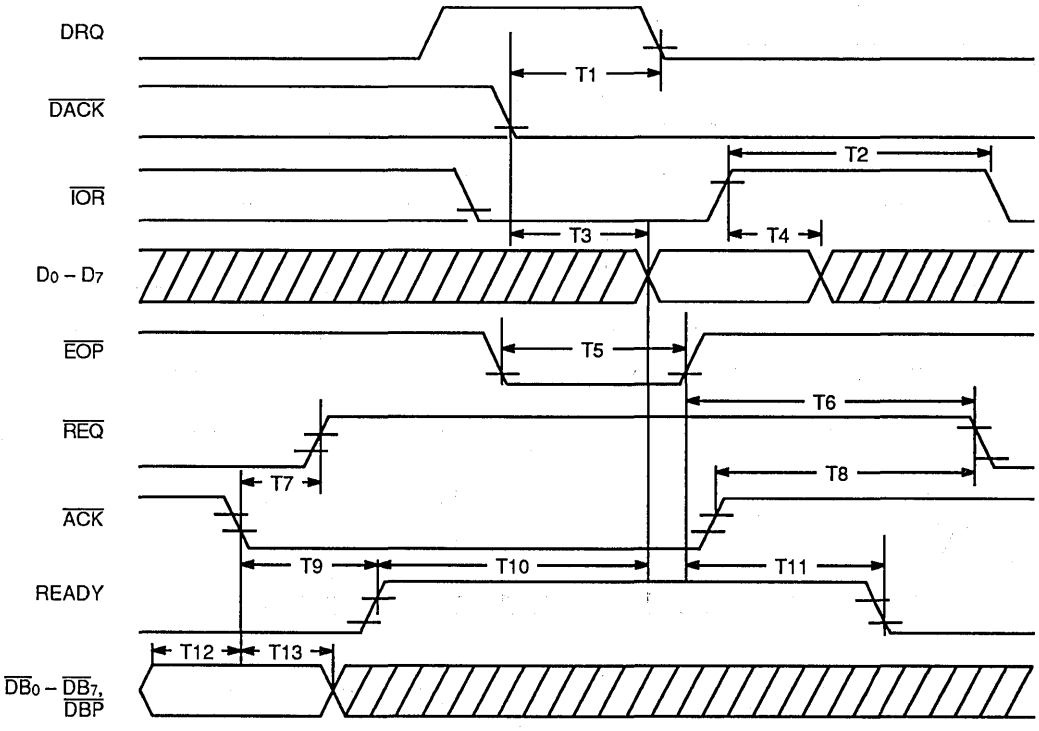
SWITCHING CHARACTERISTICS/WAVEFORMS

Name	Parameter Description	Min.	Max.	Unit
T1	DRQ FALSE from $\overline{DACK}$ TRUE		35	ns
T2	$\overline{IOR}$ Recovery Time	80		ns
T3	Data Access Time from Read Enable*		20	ns
T4	Data Hold Time from End of $\overline{IOR}$	0		ns
T5	Width of $\overline{EOP}$ Pulse (Note 1)	40		ns
T6	$\overline{IOR}$ FALSE to $\overline{REQ}$ TRUE ($\overline{ACK}$ FALSE)		45	ns
T7	$\overline{ACK}$ TRUE to $\overline{REQ}$ FALSE		90	ns
T8	$\overline{ACK}$ FALSE to $\overline{REQ}$ TRUE ($\overline{IOR}$ FALSE)		35	ns
T9	$\overline{ACK}$ TRUE to READY TRUE		100	ns
T10	READY TRUE to Valid Data		50	ns
T11	$\overline{IOR}$ FALSE to READY FALSE		40	ns
T12	Data Setup Time to $\overline{ACK}$	10		ns
T13	Data Hold Time from $\overline{ACK}$	65		ns

*Read Enable is the occurence of $\overline{IOR}$ and $\overline{DACK}$.

Note:

1. $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$ must be concurrently TRUE for at least T5 for proper recognition of the $\overline{EOP}$ pulse.

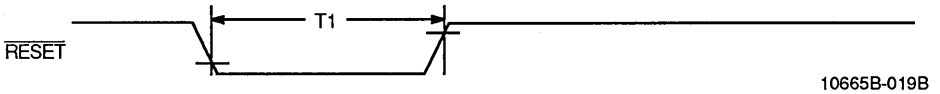


10665B-018B

DMA Read (Block Mode) Target Receive Cycle

SWITCHING CHARACTERISTICS/WAVEFORMS

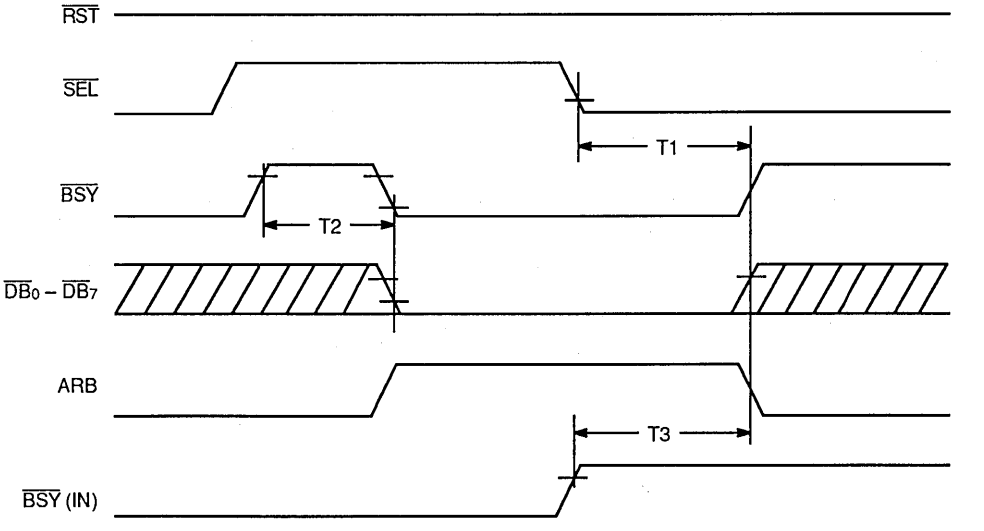
Name	Parameter Description	Min.	Max.	Unit
T1	Minimum Width of Reset	100		ns



10665B-019B

Reset

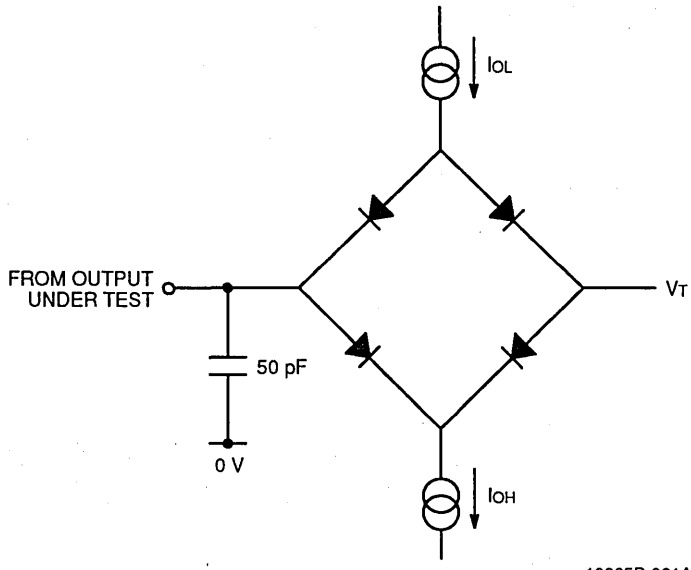
Name	Parameter Description	Min.	Max.	Unit
T1	Bus Clear from $\overline{SEL}$ TRUE		600	ns
T2	Arbitrate Start from $\overline{BSY}$ FALSE	1200	2400	ns
T3	Bus Clear from $\overline{BSY}$ FALSE		1100	ns



10665B-020A

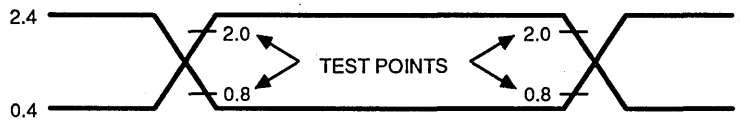
Arbitration

SWITCHING TEST CIRCUIT



10665B-021A

SWITCHING TEST WAVEFORM



10665B-022A

ADVANCE INFORMATION

Am53C94/Am53C96

High Performance SCSI Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Plug compatible with NCR 53C94/53C96
- 5 MB per second SCSI transfer rate
- 20 MB per second DMA transfer rate
- 16-bit DMA Interface plus 2 bits of parity
- Flexible bus architecture, supports a three bus architecture
- Single ended SCSI bus supported by Am53C94
- Single ended and differential SCSI bus supported by Am53C96
- Selection of multiplexed or non-multiplexed address and data bus
- High current drivers (48 mA) for direct connection to the single ended SCSI bus
- Supports Disconnect and Reselect commands
- Supports burst mode DMA operation with a threshold of 8
- Supports 3 byte tagged queuing as per the SCSI-2 specification
- Supports group 2 and 5 command recognition as per the SCSI-2 specification
- Advanced CMOS process for low power consumption
- Am53C94 available in 84 pin PLCC package
- Am53C96 available in 100 pin PQFP package

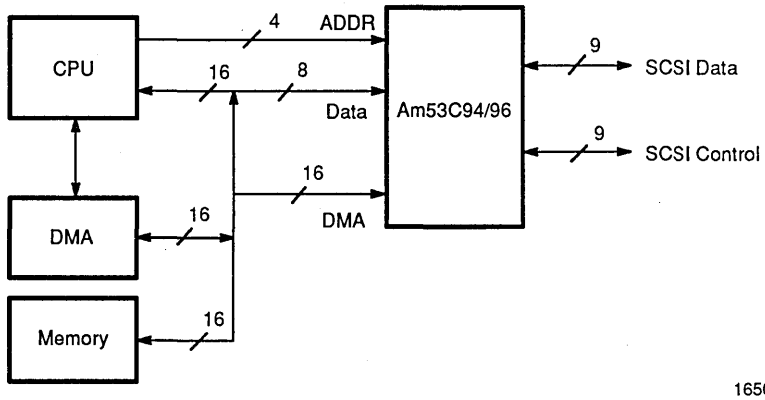
GENERAL DESCRIPTION

The High Performance SCSI Controller (HPSC) has a flexible three bus architecture. The HPSC has a 16 bit DMA interface, an 8 bit host data interface and an 8 bit SCSI data interface. The HPSC is designed to minimize host intervention by implementing common SCSI sequences in hardware. An on-chip state machine reduces protocol overheads by performing the required sequences in response to a single command from the host. Selection, Reselection, Information Transfer and Disconnection commands are directly supported.

The 16 byte internal FIFO further assists in minimizing host involvement. The FIFO provides a temporary storage for all command, data, status and message bytes as they are transferred between the 16 bit host data bus and the 8 bit SCSI data bus. During DMA operations the FIFO acts as a buffer to allow greater latency in the DMA channel. This permits the DMA channel to be suspended for higher priority operations such as DRAM refresh or reception of an ISDN packet.

Parity on the DMA bus is optional. Parity can either be generated and checked or it can be simply passed through.

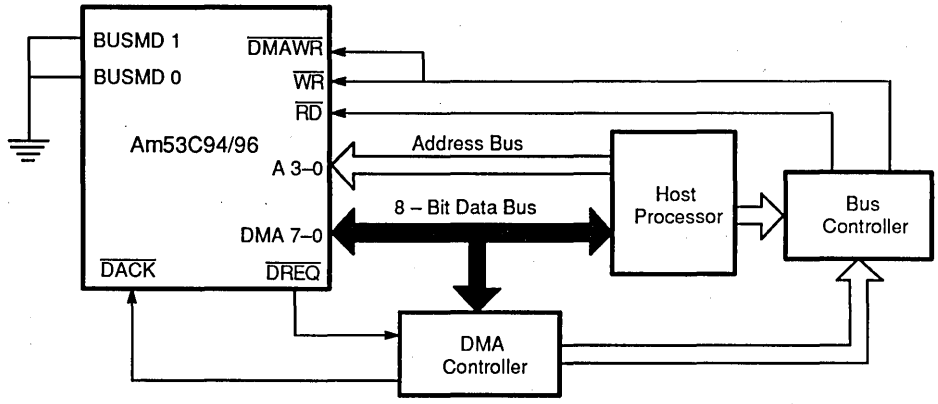
SYSTEM BLOCK DIAGRAM



16506A-001A

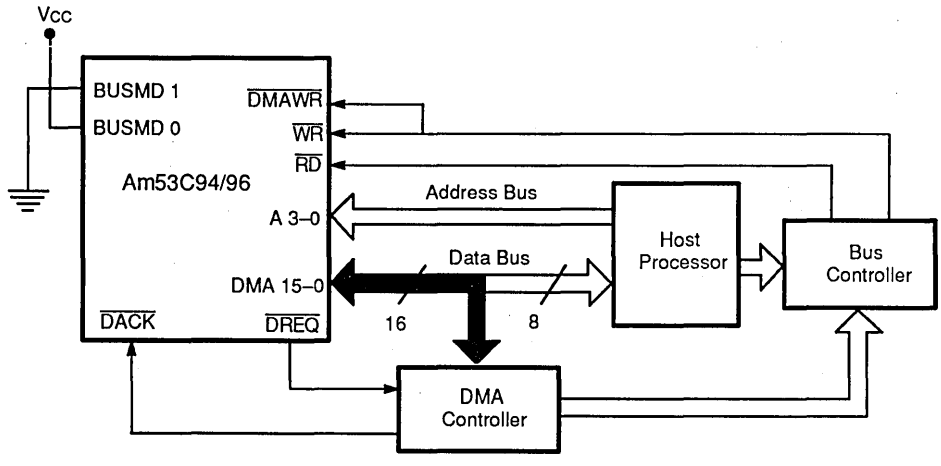
Publication# 16506 Rev. A Amendment/0
Issue Date: November 1991

SYSTEM BUS MODE DIAGRAMS



16506A-002A

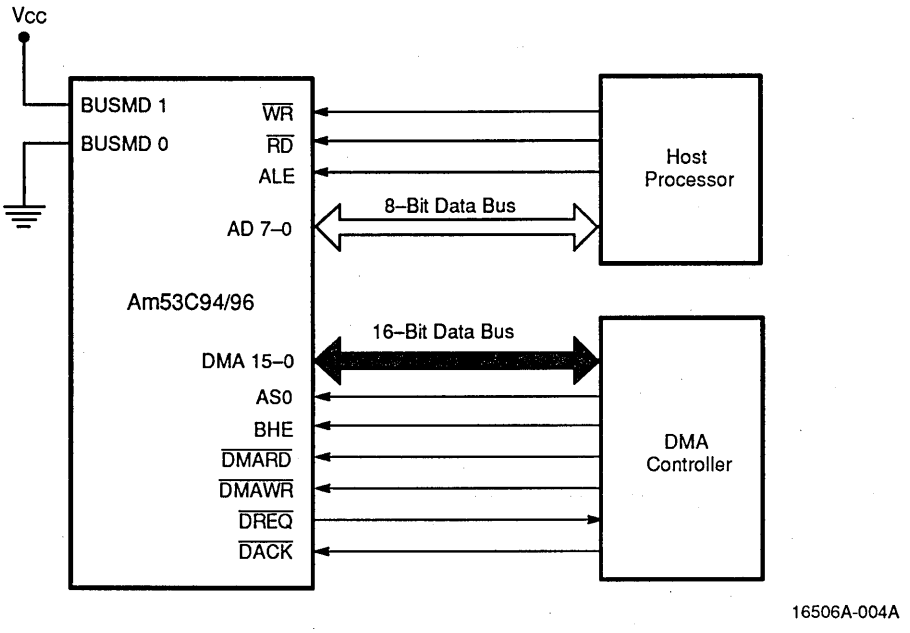
Bus Mode 0



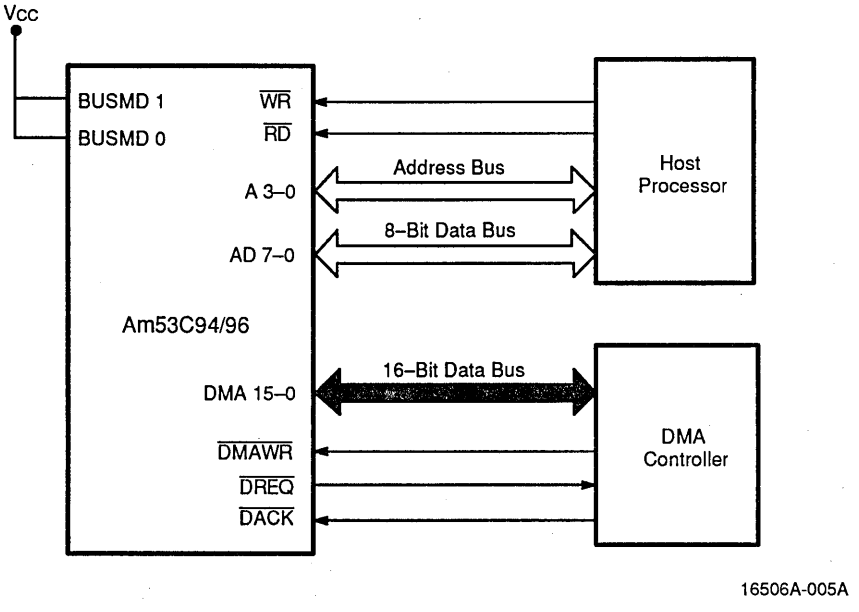
16506A-003A

Bus Mode 1

SYSTEM BUS MODE DIAGRAMS

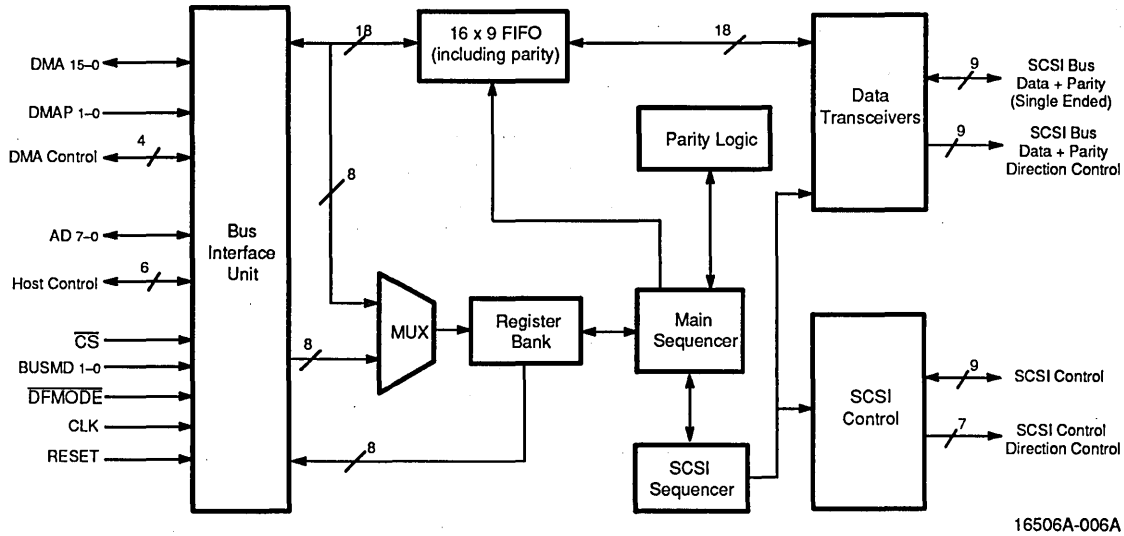


Bus Mode 2



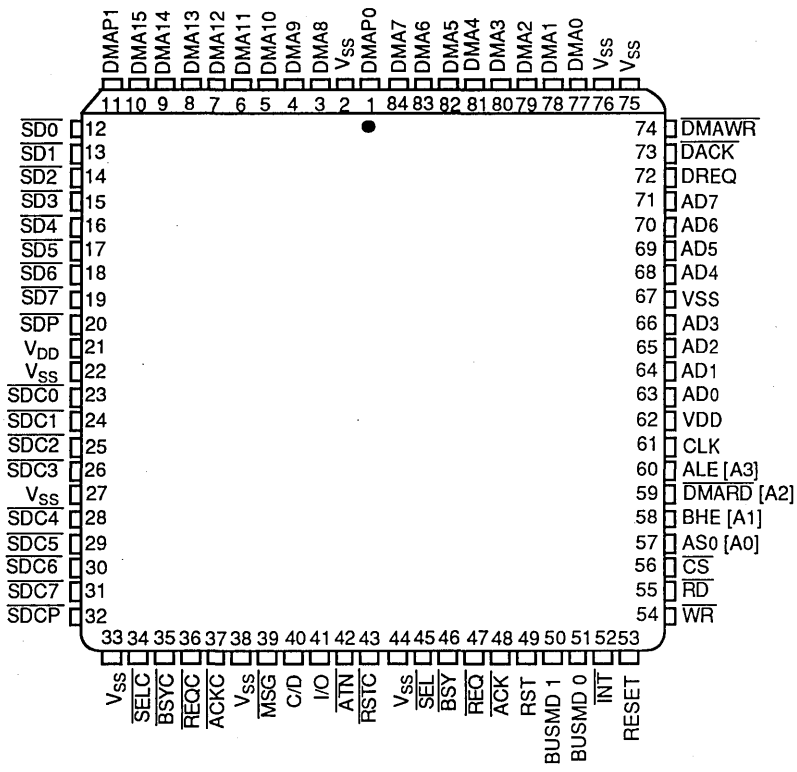
Bus Mode 3

BLOCK DIAGRAM



CONNECTION DIAGRAM
Am53C94 (Top View)

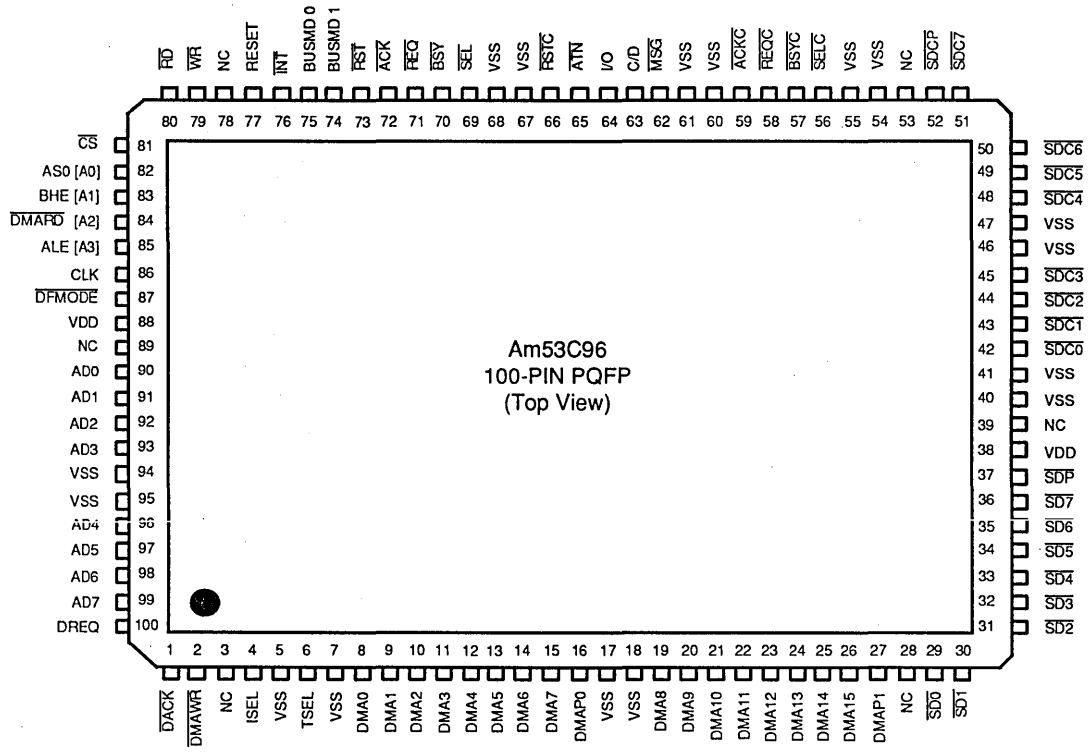
PLCC



16506A-007A

CONNECTION DIAGRAM
Am53C96 (Top View)

PQFP

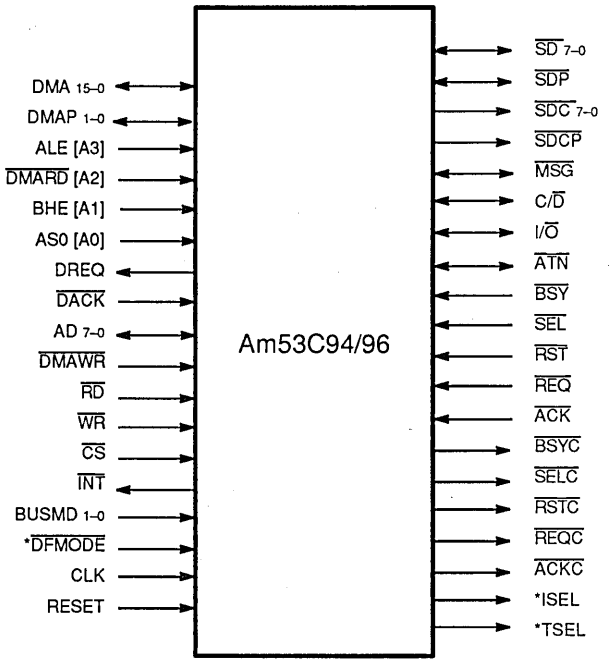


16506A-008A

RELATED AMD PRODUCTS

Part Number	Description
Am53C80A	4 MBytes/sec Asynchronous CMOS SCSI Controller
Am33C93A	5 MBytes/sec Async/Synchronous CMOS SCSI Controller
Am85C80	Combination SCSI Controller (Am53C80A) and ESCC (Am85C30)
Am85C30	Enhanced Serial Communications Controller (ESCC)

LOGIC SYMBOL

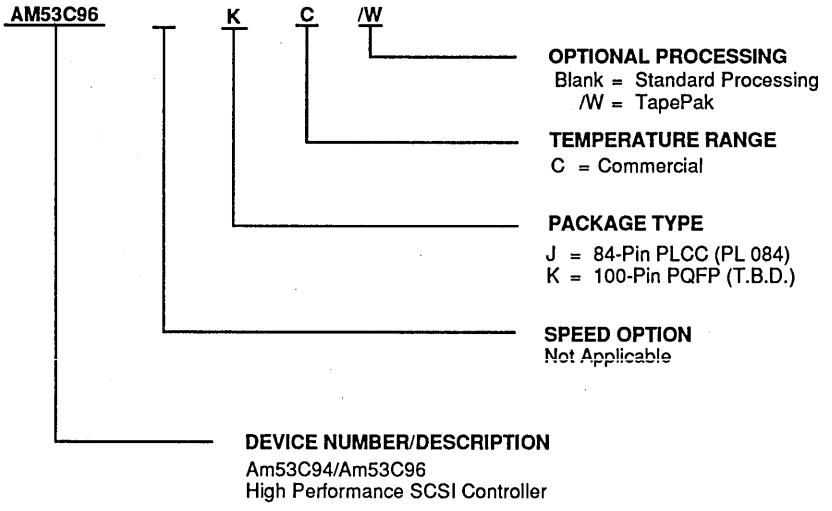


* Pins available on the Am53C96 only

16506A-009A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM53C94	JC
AM53C96	KC, KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Host Interface Signals

DMA 15-0

Data / DMA Bus (Input/Output, Active High, Internal Pullup)

The configuration of this bus depends on the Bus Mode 1-0 (BUSMD 1-0) inputs. When the device is configured for single bus operation, the host can access the internal register set on the lower eight lines and the DMA accesses can be made to the FIFO using the entire bus. When using the Byte Mode via the BHE and A0 inputs the data can be transferred on either the upper or lower half of the DMA 15-0 bus.

DMAP 1-0

Data/DMA Parity Bus (Input/Output, Active High, Internal Pullup)

These lines are odd parity for the DMA 15-0 bus. DMAP 1 is the parity for the upper half of the bus (DMA 15-8) and DMAP 0 is the parity for the lower half of the bus (DMA 7-0).

ALE [A3]

Address Latch Enable [Address 3] (Input, Active High)

This is a dual function input. When the device is configured for single bus operation this input acts as ALE. As ALE, this input latches the address on the AD 7-0 bus on its Low going edge. When the device is configured for dual bus operation this input acts as A3. As A3, this input is the third bit of the address bus.

$\overline{\text{DMARD}}$ [A2]

DMA Read [Address 2] (Input, Active Low [Active High])

This is a dual function input. When the device is configured for single bus operation this input acts as $\overline{\text{DMARD}}$. As $\overline{\text{DMARD}}$, this input is the read signal for the DMA 15-0 bus. When the device is configured for dual bus operation this input acts as A2. As A2, this input is the second bit of the address bus.

BHE [A1]

Bus High Enable [Address 1] (Input, Active High)

This is a dual function input. When the device is configured for single bus operation this input acts as BHE. As BHE, this input along with AS0 indicates on which lines the data transfer is to take place. When the device is configured for dual bus operation this input acts as A1. As A1, this input is the first bit of the address bus.

The following is the decoding for the BHE and AS0 inputs:

BHE	AS0	Bus Used
1	1	Upper Bus – DMA 15-8, DMAP 1
1	0	Full Bus – DMA 15-0, DMAP 1-0
0	1	Reserved
0	0	Lower Bus – DMA 7-0, DMAP 0

AS0 [A0]

Address Status [Address 0] (Input, Active High)

This is a dual function input. When the device is configured for single bus operation this input acts as AS0. As AS0, this input along with BHE indicates on which lines the data transfer is to take place. When the device is configured for dual bus operation this input acts as A0. As A0, this input is the zeroth bit of the address bus.

DREQ

DMA Request (Output, Active High, Tri-State)

This output signal to the DMA controller will be active during DMA read and write cycles. During a DMA read cycle it will be active as long as there is a word (or a byte in the byte mode) in the FIFO to be transferred to memory. During a DMA write cycle it will be active as long as there is an empty space for a word (or a byte in the byte mode) in the FIFO.

$\overline{\text{DACK}}$

DMA Acknowledge (Input, Active Low)

This input signal from the DMA controller will be active during DMA read and write cycles. The $\overline{\text{DACK}}$ signal is used to access the DMA FIFO only and should never be active simultaneously with the $\overline{\text{CS}}$ signal, which accesses the registers only.

AD 7-0

Host Address Data Bus (Input/Output, Active High, Internal Pullup)

This bus is used only in the dual bus mode. This bus allows the host processor to access the device's internal registers while the DMA bus is transferring data. When using the multiplexed bus mode, these lines can be used for address and data. When using a non-multiplexed bus mode these lines can be used for the data only.

$\overline{\text{DMAWR}}$

DMA Write (Input, Active Low)

This signal writes the data on the DMA 15-0 bus into the internal FIFO when DACK is also active. When in the single bus mode this signal must be tied to the WR signal.

$\overline{RD}$
Read (Input, Active Low)

This signal reads the internal device registers and places their contents on the data bus, when either $\overline{CS}$ signal or $\overline{DACK}$ signal is active.

$\overline{WR}$
Write (Input, Active Low)

This signal writes the internal device registers with the value present on the data bus, when the $\overline{CS}$ signal is also active.

$\overline{CS}$
Chip Select (Input, Active Low)

This signal enables the read and write of the device registers. $\overline{CS}$ enables access to any register (including the FIFO) while the $\overline{DACK}$ enables access only to the FIFO. $\overline{CS}$ and $\overline{DACK}$ should never be active simultaneously in the single bus mode, they may however be active simultaneously in the dual bus mode provided the $\overline{CS}$ signal is not enabling access to the FIFO.

$\overline{INT}$
Interrupt (Output, Active Low, Open Drain)

This signal is a non-maskable interrupt flag to the host processor. This signal is latched on the output on the high going edge of the clock. This flag may be cleared by reading the Interrupt Status Register (ISTAT) or by performing a device reset (hard or soft). This flag is not cleared by a SCSI reset.

BUSMD 1-0
Bus Mode (Input, Active High)

These inputs configure the device for single bus or dual bus operation and the DMA width.

BUSMD1	BUSMD0	Bus Configuration
1	1	Two buses: 8-bit Host Bus & 16-bit DMA Bus Register Address on A 3-0 & Data on AD Bus
1	0	Two buses: Multiplexed & byte control Register Address on AD 3-0 & Data on AD Bus
0	1	Single bus: 8-bit Host Bus & 16-bit DMA Bus Register Address on A 3-0 & Data on DMA Bus
0	0	Single bus: 8-bit Host Bus & 8-bit DMA Bus Register Address on A 3-0 & Data on DMA Bus

$\overline{DFMODE}$
Differential Mode (Input, Active Low)

This input is available only on the Am53C96. This input configures the SCSI bus to either single ended or differential. When this input is active, the device operates in the differential SCSI mode. The SCSI data is available on the SD 7-0 lines and the high active transceiver enables on the SDC 7-0 outputs. When this input is inactive, the device operates in the single-ended SCSI mode. The SCSI input data is available on SD 7-0 lines and the output data is available on SDC 7-0 lines. In the single-ended SCSI mode, the SD 7-0 and the SDC 7-0 buses can be tied together externally.

CLK
Clock (Input)

Clock input used to generate all the internal device timings. The maximum frequency of this input is 25 MHz. A minimum of 10MHz is required to maintain the SCSI bus timings.

RESET
Reset (Input, Active High)

This input when active resets the device. The RESET input must be active for at least two CLK periods after the voltage on the power inputs has reached Vcc minimum.

SCSI Interface Signals

$\overline{SD}$ 7-0
SCSI Data (Input/Output, Active Low, Schmitt Trigger)

When the device is configured in the Single-Ended SCSI Mode ($\overline{DFMODE}$ inactive) these pins are defined as inputs for the SCSI data bus. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) these pins are defined as a bidirectional SCSI data bus.

$\overline{SDP}$
SCSI Data Parity (Input/Output, Active Low, Schmitt Trigger)

When the device is configured in the Single-Ended SCSI Mode ($\overline{DFMODE}$ inactive) this pin is defined as the input for the SCSI data parity. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) this pin is defined as bidirectional SCSI data parity.

$\overline{SDC}$ 7-0
SCSI Data Control (Output, Active Low, Open Drain)

When the device is configured in the Single-Ended SCSI Mode ($\overline{DFMODE}$ inactive) these pins are defined as outputs for the SCSI data bus. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) these pins are defined as direction controls for the external differential transceivers. In this mode, a

signal High state corresponds to an output to the SCSI bus and a Low state corresponds to an input from the SCSI bus.

$\overline{\text{SDCP}}$
SCSI Data Control Parity (Output, Active Low, Open Drain)

When the device is configured in the Single-Ended SCSI Mode ($\overline{\text{DFMODE}}$ inactive) this pin is defined as an output for the SCSI data parity. When the device is configured in the Differential SCSI Mode ($\overline{\text{DFMODE}}$ active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal high state corresponds to an output to the SCSI bus and a low state corresponds to an input from the SCSI bus.

$\overline{\text{MSG}}$
Message (Input/Output, Active Low, Schmitt Trigger)

This is a bidirectional signal with a 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

C/$\overline{\text{D}}$
Command/Data (Input/Output, Schmitt Trigger)

This is a bidirectional signal with a 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

I/$\overline{\text{O}}$
Input/Output (Input/Output, Schmitt Trigger)

This is a bidirectional signal with a 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{\text{ATN}}$
Attention (Input/Output, Active Low, Schmitt Trigger)

This signal is a 48 mA output in the initiator mode and a Schmitt trigger input in the target mode. This signal will be asserted when the device detects a parity error or it can be asserted via certain commands. In the target mode this pin is an input.

$\overline{\text{BSY}}$
Busy (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{SEL}}$
Select (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{RST}}$
Reset (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{REQ}}$
Request (Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{ACK}}$
Acknowledge (Input, Active Low, Schmitt Trigger). This is a SCSI input signal with a Schmitt trigger.

$\overline{\text{BSYC}}$
Busy Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. When the device is configured in the Single-Ended SCSI Mode ($\overline{\text{DFMODE}}$ inactive) this pin is defined as a $\overline{\text{BSY}}$ output for the SCSI bus. When the device is configured in the Differential SCSI Mode ($\overline{\text{DFMODE}}$ active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal High state corresponds to an output to the SCSI bus and a Low state corresponds to an input from the SCSI bus.

$\overline{\text{SELC}}$
Select Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. When the device is configured in the Single-Ended SCSI Mode ($\overline{\text{DFMODE}}$ inactive) this pin is defined as a $\overline{\text{SEL}}$ output for the SCSI bus. When the device is configured in the Differential SCSI Mode ($\overline{\text{DFMODE}}$ active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal High state corresponds to an output to the SCSI bus and a Low state corresponds to an input from the SCSI bus.

$\overline{\text{RSTC}}$
Reset Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. The Reset SCSI command will cause the device to drive $\overline{\text{RSTC}}$ active for 25–40 microseconds, which will depend on the CLK frequency and the conversion factor. When the device is configured in the Single-Ended SCSI Mode ($\overline{\text{DFMODE}}$ inactive) this pin is defined as a $\overline{\text{RST}}$ output for the SCSI bus. When the device is configured in the Differential SCSI Mode ($\overline{\text{DFMODE}}$ active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal High state corresponds to an output to the SCSI bus and a Low state corresponds to an input from the SCSI bus.

$\overline{\text{REQC}}$
Request Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This signal is asserted only in the target mode.

$\overline{\text{ACKC}}$
Acknowledge Control (Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This signal is asserted only in the initiator mode.

ISEL
Initiator Select (Output, Active High)

This signal is available on the Am53C96 only. It is active whenever the device is in the initiator mode. In the differential mode this signal is used to enable the initiator signals $\overline{ACKC}$ and $\overline{ATNC}$ and the device also drives these signals.

TSEL
Target Select (Output, Active High)

This signal is available on the Am53C96 only. It is active whenever the device is in the target mode. In the differential mode this signal is used to enable the target signals $\overline{REQC}$, $\overline{MSG}$, C/$\overline{D}$ and I/$\overline{O}$ and the device also drives these signals.

FUNCTIONAL DESCRIPTION

Register Map

Address (Hex.)	Operation	Register
00	Read	Current Transfer Count Register LSB
00	Write	Start Transfer Count Register LSB
01	Read	Current Transfer Count Register MSB
01	Write	Start Transfer Count Register MSB
02	Read/Write	FIFO Register
03	Read/Write	Command Register
04	Read	Status Register
04	Write	SCSI Destination ID Register
05	Read	Interrupt Status Register
05	Write	SCSI Timeout Register
06	Read	Internal State Register
06	Write	Synchronous Transfer Period Register
07	Read	Current $\overline{FIFO}$ Internal State Register
07	Write	Synchronous Offset Register
08	Read/Write	Control Register 1
09	Write	Clock Factor Register
0A	Write	Forced Test Mode Register
0B	Read/Write	Control Register 2
0C	Read/Write	Control $\overline{Register\ 3}$ Rev. ID Register
0F	Write	Data Alignment Register

Not all registers in this device are both readable and writable. Some read only registers share the same address with write only registers. The registers can be accessed by asserting the $\overline{CS}$ signal and then asserting either $\overline{RD}$ or $\overline{WR}$ signal depending on the operation to be performed. Only the FIFO Register can be accessed by asserting either $\overline{CS}$ or $\overline{DACK}$ in conjunction with $\overline{RD}$ and $\overline{WR}$ signals or $\overline{DMARD}$ and $\overline{DMAWR}$ signals. The register address inputs are ignored when $\overline{DACK}$ is used but must be valid when $\overline{CS}$ is used.

COMMANDS

The device commands can be broadly divided into two categories, DMA commands and non-DMA commands. DMA commands are those which cause data movement between the host memory and the SCSI bus while non-DMA commands are those that cause data movement between the device FIFO and the SCSI bus. The MSB of the command byte differentiates DMA commands from non-DMA commands.

Summary of Commands

Command	Command Code (Hex.)	
	Non-DMA Mode	DMA Mode
Initiator Commands		
Information Transfer	10	90
Initiator Command Complete Steps	11	91
Message Accepted	12	-
Transfer Pad Bytes	18	98
Set $\overline{ATN}$	1A	-
Reset $\overline{ATN}$	1B	-
Target Commands		
Send Message	20	A0
Send Status	21	A1
Send Data	22	A2
Disconnect Steps	23	A3
Terminate Steps	24	A4
Target Command Complete Steps	25	A5
Disconnect	27	A7
Receive Message	28	A8
Receive Command Steps	29	A9
Receive Data	2A	AA
Receive Command Steps	2B	AB
Target Abort DMA	04	84

Command	Command Code (Hex.)	
	Non-DMA Mode	DMA Mode
Idle State Commands		
Reselect Steps	40	C0
Select without $\overline{ATN}$ Steps	41	C1
Select with $\overline{ATN}$ Steps	42	C2
Select with $\overline{ATN}$ and Stop Steps	43	C3
Enable Selection/Reselection	44	C4
Disable Selection/Reselection		45
Select with $\overline{ATN3}$	46	C6
General Commands		
No Operation	00	80
Clear FIFO	01	81
Reset Device	02	82
Reset SCSI bus	03	83

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–55 to +125°C
Ambient Operating Temperature	0 to +70°C
Maximum V_{CC}	–0.5 to +7.0 V
DC Voltage Applied to Any Pin	–0.5 to (V_{CC} + 0.3) V
Input Static Discharge Protection (Human body model: 100 pF at 1.5 K Ohms)	3000 V pin to pin

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.75 to +5.75 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

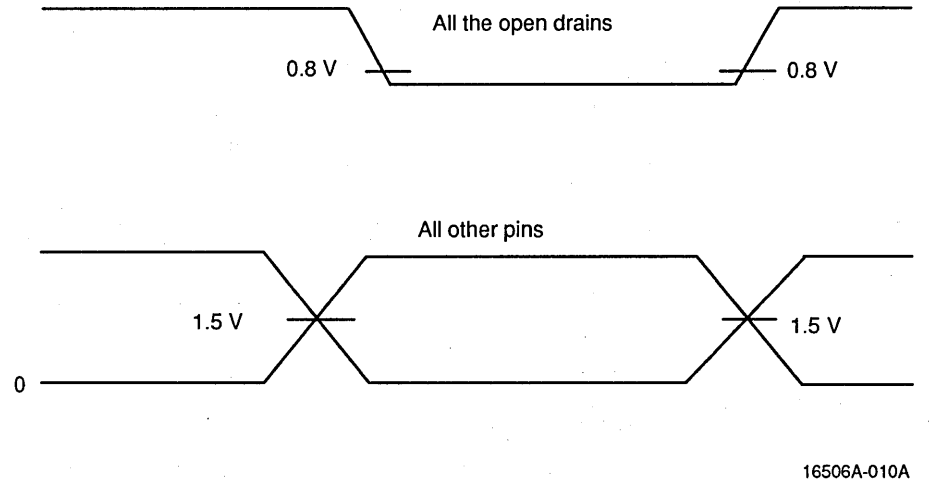
DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Pin Names	Test Conditions	Min.	Max.	Unit
I_{CCS}	Static Supply Current				8.0	mA
I_{CCD}	Dynamic Supply Current				50	mA
I_{LU}	Latch Up Current			–100	+100	mA
SCSI Pins						
V_{IH}	Input High Voltage	All SCSI Inputs		2.0		V
V_{IL}	Input Low Voltage	All SCSI Inputs			0.8	V
V_{IHST}	Input Hysteresis	All SCSI Inputs	4.75 V<V_{CC} <5.25 V	300		mV
V_{OH}	Output High Voltage	SD 7–0, SDP	I_{OH} = –2 mA	2.4	V_{CC}	V
V_{SOL1}	SCSI Output Low Voltage	SD 7–0, SDP	I_{OL} = 4 mA	V_{SS}	0.4	V
V_{SOL2}	SCSI Output Low Voltage	SDC 7–0, SDCP, MSG, C/$\overline{D}$, I/$\overline{O}$, ATN, RSTC, SELC, BSYC, ACKC and REQC	I_{OL} = 48 mA	V_{SS}	0.5	V
I_{IL}	Input Low Leakage	All SCSI Inputs	0.5 V < V_{IN} < 2.7 V	–10	+10	µA
I_{IH}	Input High Leakage	All SCSI Inputs	0.5 V < V_{IN} < 2.7 V	–10	+10	µA
I_{OZ}	High Impedance Leakage	All SCSI Inputs	0 V < V_{OUT} < V_{CC}	–10	+10	µA
Bidirectional Pins						
V_{IH}	Input High Voltage	DMA 15-0, DMAP 1-0 and AD 7-0		2.0	V_{CC} +0.5	V
V_{IL}	Input Low Voltage	DMA 15-0, DMAP 1-0 and AD 7-0		V_{SS}–0.5	0.8	V
V_{OH}	Output High Voltage	DMA 15-0, DMAP 1-0 and AD 7-0	I_{OH} = –2 mA	2.4	V_{CC}	V
V_{OL}	Output Low Voltage	DMA 15-0, DMAP 1-0 and AD 7-0	I_{OL} = 4 mA	V_{SS}	0.4	V
I_{IL}	Input Low Leakage	DMA 15-0, DMAP 1-0 and AD 7-0	V_{IN} = V_{IL}	–400	+10	µA
I_{IH}	Input High Leakage	DMA 15-0, DMAP 1-0 and AD 7-0	V_{IN} = V_{IH}	–10	+10	µA
I_{OZ}	High Impedance Leakage	DMA 15-0, DMAP 1-0 and AD 7-0		–100	400	µA
Output Pins						
V_{OH}	Output High Voltage	DRQ, ISEL, TSEL and INT	I_{OH} = –2 mA	2.4	V_{CC}	V
V_{OL}	Output Low Voltage	DRQ, ISEL, TSEL and INT	I_{OL} = 4 mA		0.4	V
I_{OZ}	High Impedance Leakage	DRQ, ISEL, TSEL and INT	0 V < V_{OUT} < V_{CC}	–10	+10	µA

DC CHARACTERISTICS over operating range unless otherwise specified (Continued)

Parameter Symbol	Parameter Description	Pin Names	Test Conditions	Min.	Max.	Unit
Input Pins						
V_{IH}	Input High Voltage	A 3-0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and DFMODE		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	A 3-0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and DFMODE		V_{SS} + 0.5	0.8	V
I_{IL}	Input Low Leakage	A 3-0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and DFMODE	$V_{IN} = V_{IL}$	−10	+10	µA
I_{IH}	Input High Leakage	A 3-0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and DFMODE	$V_{IN} = V_{IH}$	−10	+10	µA

SWITCHING TEST WAVEFORMS



16506A-010A

CHAPTER 2
Serial Communication Controllers

Am8530H

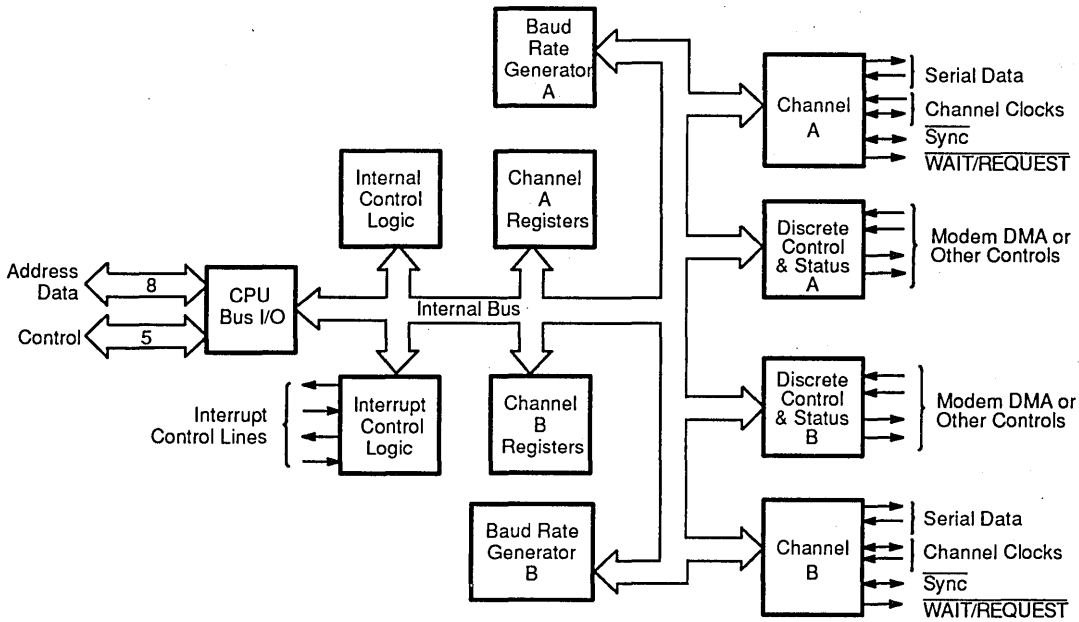
Serial Communications Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast data rate**
  - Up to 8 MHz/2 Mb/s
- **Two 0 to 2 Mb/s full duplex serial channels**
  - Each channel has independent oscillator, baud-rate generator, and PLL for clock recovery, dramatically reducing external components
- **Programmable protocols**
  - NRZ, NRZI, and FM data encoding supported under program control
- **Programmable asynchronous modes**
  - 5- to 8-bit characters with programmable stop bits, clock, break detect and error conditions
- **Programmable synchronous modes**
  - SDLC and HDLC and SDLC loop supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generator and checkers
- **Compatible with non-multiplexed bus**
  - The Am8530H interfaces easily to most other CPUs

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Serial Communications Control (SCC) is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats, synchronous byte-oriented protocols, such as IBM® Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC.

This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

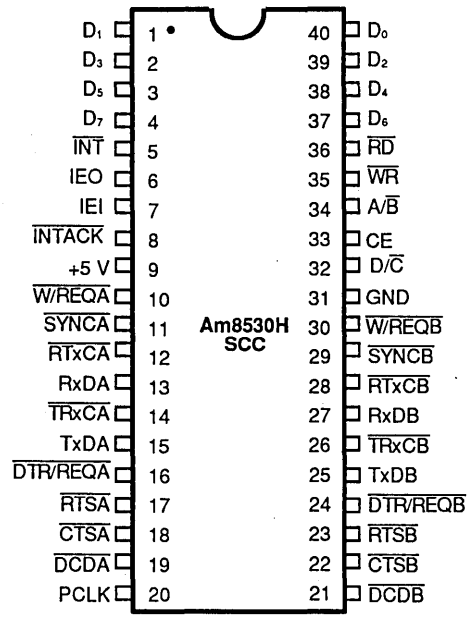
The Am8530H is designed for non-multiplexed buses and is easily interfaced with most other CPUs, such as 8080, Z80, 6800, 68000 and MULTIBUS™.

RELATED AMD PRODUCTS

Part Number	Description
Am79C12	Full Duplex 1200 bps Modem
Am7960	Coded Data Transceiver
80186	Highly Integrated 16-Bit Microprocessor
80286/80C286	High-Performance 16-Bit Microprocessor
8080A	8-Bit Microprocessor
Am9517A	DMA Controller
Am386™	High-Performance 32-Bit Microprocessor

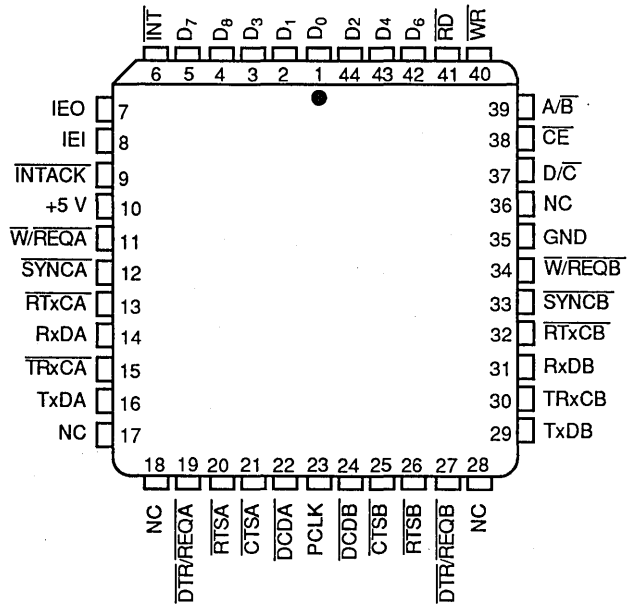
CONNECTION DIAGRAMS
Top View

DIPs



00970G-028B

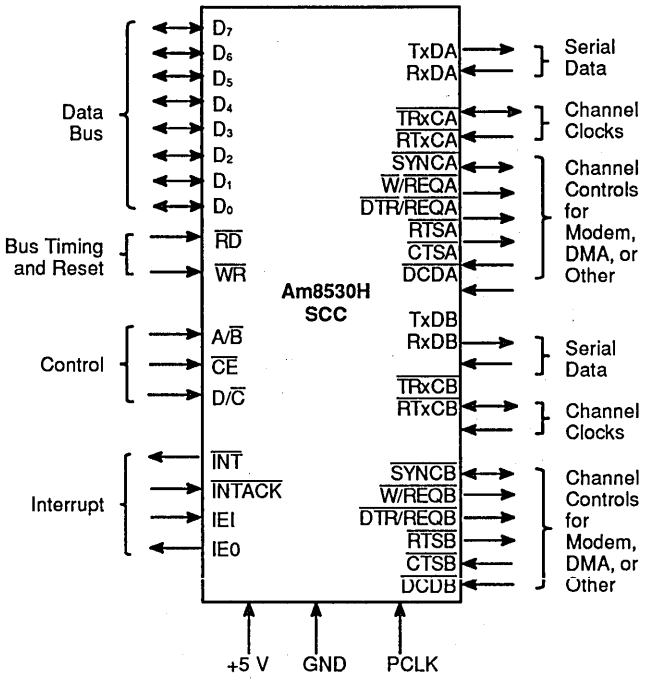
PLCC



00970G-002B

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

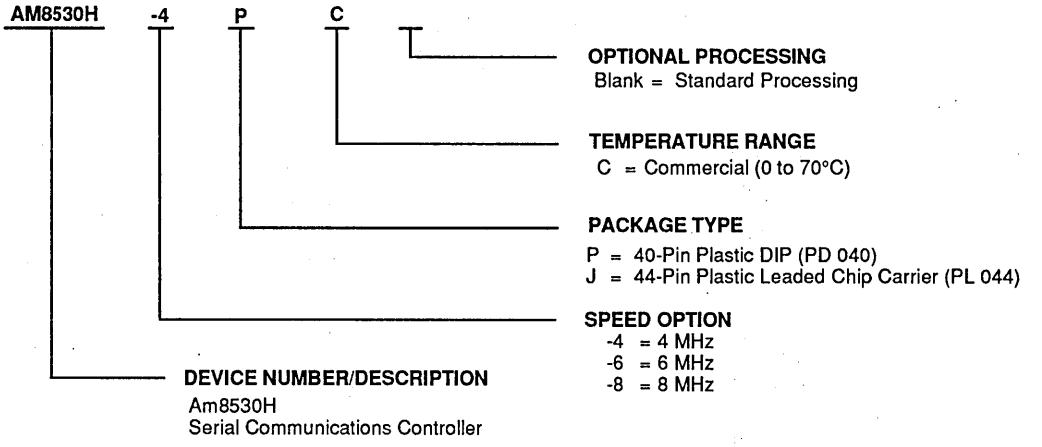


00970G–003

ORDERING INFORMATION

Commodity Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am8530H-4	PC, JC
Am8530H-6	
Am8530H-8	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A/$\overline{B}$
Channel A/Channel B Select (Input)

This signal selects the channel in which the Read or Write operation occurs.

$\overline{CE}$
Chip Enable (Input; Active Low)

This signal selects the SCC for a Read or Write operation.

$\overline{CTSA}$, $\overline{CTSB}$
Clear to Send (Inputs; Active Low)

If these pins are programmed as Auto Enables, a Low on these inputs enables their respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and may interrupt the CPU on both logic level transitions.

D/$\overline{C}$
Data/Control Select (Input)

This signal defines the type of information transferred to or from the SCC. A High means data is transferred; a Low indicates a command is transferred.

$\overline{DCDA}$, $\overline{DCDB}$
Data Carrier Detect (Inputs; Active Low)

These pins function as receiver enables if they are programmed as Auto Enables; otherwise, they may be used as general-purpose input pins. Both are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and may interrupt the CPU on both logic level transitions.

D7–D0
Data Bus (Inputs/Outputs; Three State)

These lines carry data and commands to and from the SCC.

$\overline{DTR/REQA}$, $\overline{DTR/REQB}$
Data Terminal Ready/Request (Outputs; Active Low)

These outputs follow the inverted state programmed into the DTR bit in WR5. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

GND
Ground

IEI
Interrupt Enable In (Input; Active High)

IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO
Interrupt Enable Out (Output; Active High)

IEO is High only if IEI is High and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$
Interrupt Request (Output; Active Low, Open Drain)

This signal is activated when the SCC requests an interrupt.

$\overline{INTACK}$
Interrupt Acknowledge (Input; Active Low)

This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of PCLK.

PCLK
Clock (Input)

$\overline{RD}$
Read (Input; Active Low)

This signal indicates a Read operation and, when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

$\overline{RTSA}$, $\overline{RTSB}$
Request to Send (Outputs; Active Low)

When the Request to Send (RTS) bit in Write Register 5 is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In SYNC mode, or in asynchronous mode with Auto Enable off, the $\overline{RTS}$ pins strictly follow the inverted state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{RTxCA}$, $\overline{RTxCB}$
Receive/Transmit Clocks (Inputs; Active Low)

These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

RxDA, RxDB
Receive Data (Inputs; Active High)

These input signals receive serial data at standard TTL levels.

$\overline{SYNCA}$, $\overline{SYNCB}$
Synchronization (Inputs/Outputs; Active Low)

These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Sync/

Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low two receive clock cycles after the last bit in the SYNC character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which SYNC characters are recognized. The SYNC condition is not latched, so these outputs are active each time a SYNC pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

$\overline{TRxCA}$, $\overline{TRxCB}$
Transmit/Receive Clocks
(Inputs/Outputs; Active Low)

These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

TxDA, TxDB
Transmit Data (Outputs; Active High)

These output signals transmit serial data at standard TTL levels.

This is the master SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock. PCLK is a TTL-level signal. Maximum transmit rate is 1/4 PCLK.

$\overline{WR}$
Write (Input; Active Low)

When the SCC is selected, this signal indicates a Write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.

$\overline{W/REQA}$, $\overline{W/REQB}$
Wait/Request (Outputs; Open drain when programmed for a Wait function, driven High or Low when programmed for a Request function)

These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

V_{CC}
+ 5-V Power Supply

ARCHITECTURE

The Am8530H internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to a non-multiplexed CPU bus. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface with modems or other external devices (Figure 1).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two synchronous character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the Interrupt Pending bits (A only).

The registers for each channel are designated as follows:

WR15–WR0—Write Registers 15 through 0.

RR0–RR3, RR10, RR12, RR13, RR15—Read Registers 0 through 3, 10, 12, 13, 15.

The following table lists the functions assigned to each read or write register. The SCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

Data Path

The transmit and receive data path illustrated in Figure 2 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

Table 1. Read and Write Register Functions

Read Register Functions		Write Register Functions	
RR0	Transmit/receive buffer status and external status	**WR0**	CRC initialize, initialization commands for the various modes, shift right/shift left command
RR1	Special receive condition status	**WR1**	Transmit/receive interrupt and data transfer mode definition
RR2	Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only)	**WR2**	Interrupt vector (accessed through either channel)
		WR3	Receive parameters and control
RR3	Interrupt pending bits (Channel A only)	**WR4**	Transmit/receive miscellaneous parameters and modes
RR8	Receive buffer	**WR5**	Transmit parameters and controls
RR10	Miscellaneous status	**WR6**	Sync character or SDLC address field
RR12	Lower byte of baud rate generator time constant	**WR7**	Sync character or SDLC flag
RR13	Upper byte of baud rate generator time constant	**WR8**	Transmit buffer
RR15	External/status interrupt information	**WR9**	Master interrupt control and reset (accessed through either channel)
		WR10	Miscellaneous transmitter/receiver control bits
		WR11	Clock mode control
		WR12	Lower byte of baud rate generator time constant
		WR13	Upper byte of baud rate generator time constant
		WR14	Miscellaneous control bits
		WR15	External/Status interrupt control

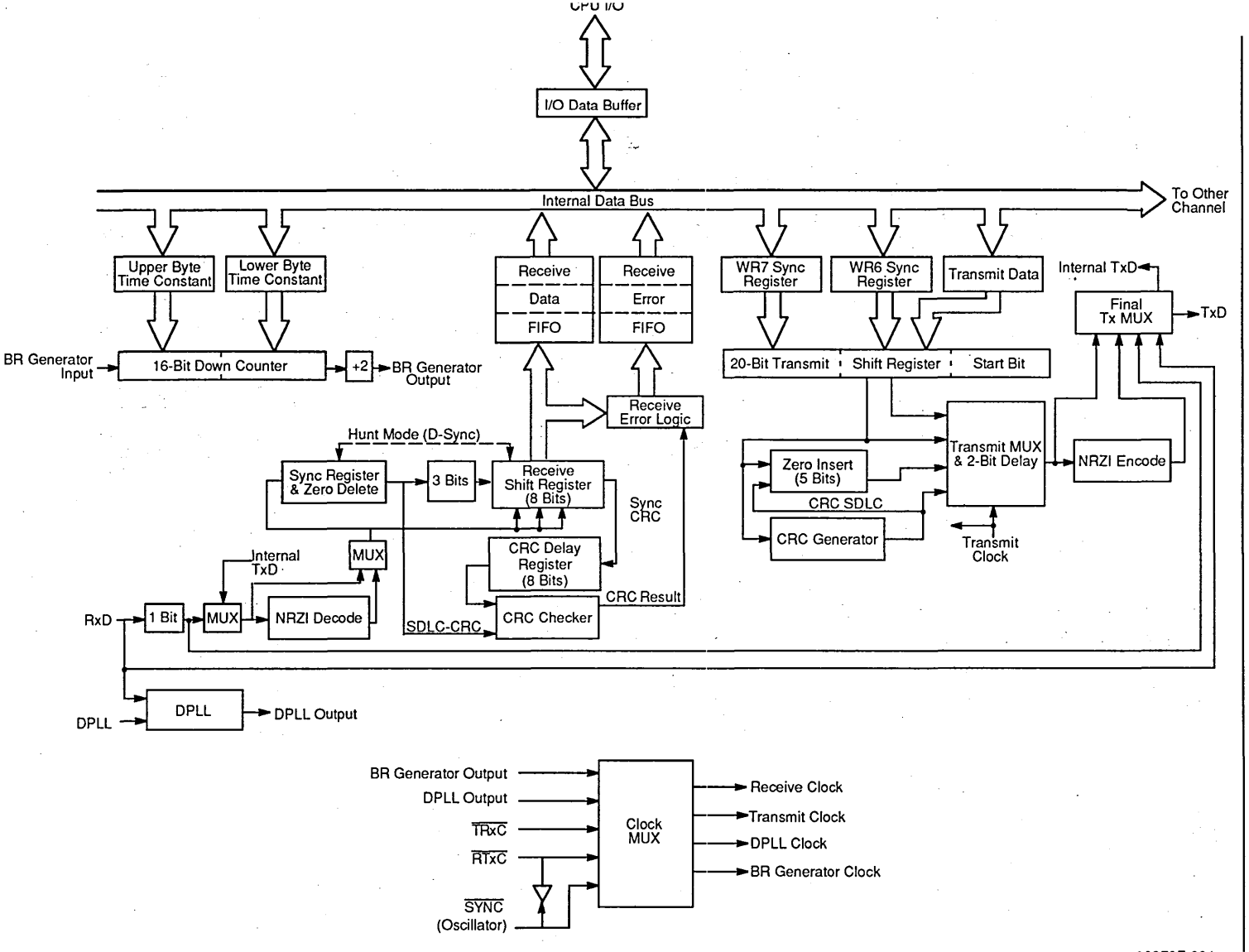


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Figure 1. Data Path

DETAILED DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

Data Communications Capabilities

The SCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data-communication protocol. Figure 2 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in the Am8530H Logic Symbol). If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The SCC does not require symmetric transmit and receive clock signals—a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input used for functions, such as monitoring a ring indicator.

Synchronous Modes

The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), any 12-bit synchronous pattern (Bisync), or with an external synchronous signal. Leading synchronous characters can be removed without interrupting the CPU.

5- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multiple incoming synchronous characters as shown in Figure 3.

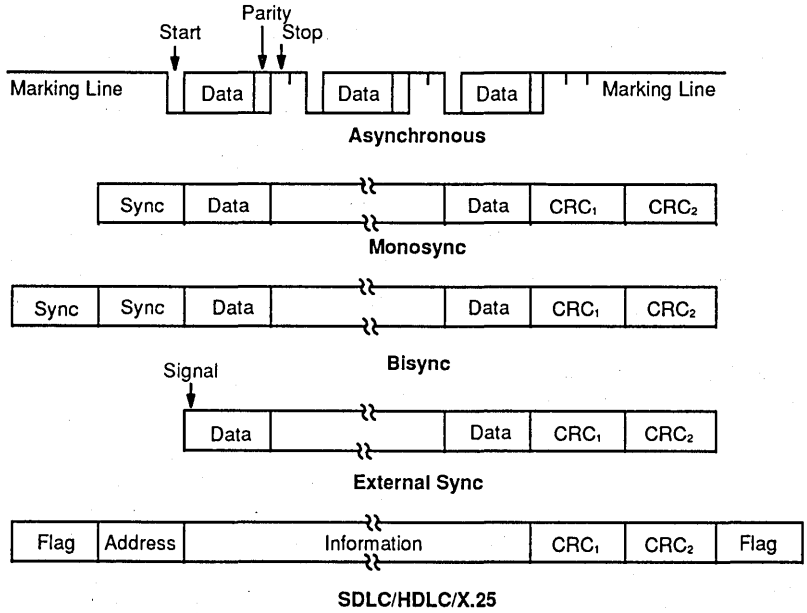

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Figure 2. SCC Protocols

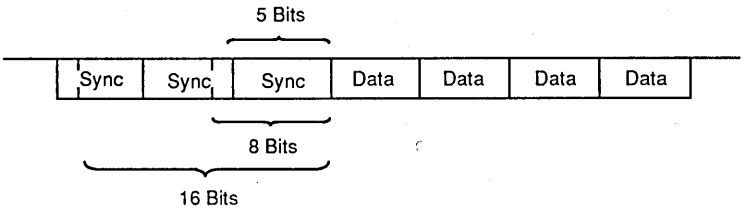

Figure 3. Detecting 5- or 7-Bit Synchronous Characters

00970F-006

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols, such as IBM Bisync.

Both CRC-16 ($X^{16}+X^{15}+X^2+1$) and CCITT ($X^{16}+X^{12}+X^5+1$) error checking polynomials are supported. Either polynomial may be selected in all synchronous modes. Users may preset the CRC generator and checker to all 1s or all 0s. The SCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, reliving the CPU of this task. One to eight bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{\text{SYNC}}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The SCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC Loop Mode

The SCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 4).

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop and, in fact, must pass these messages to the rest of the loop by retransmitting them with a one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110.

Because of zero insertion during messages, this bit pattern is unique and easily recognized.

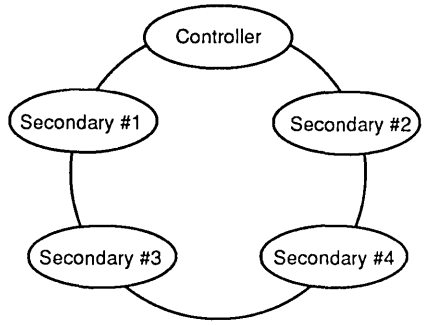

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Figure 4. An SDLC Loop

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary one of the EOP to a zero before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the SCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

Baud Rate Generator

Each channel in the SCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On start-up the flip-flop on the output is set in a High state; the value in the time constant register is loaded into the counter; and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero; the value in the time constant register is loaded into the counter; and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds.)

$$\text{baud rate} = \frac{1}{2\,(\text{time constant} + 2) \cdot (\text{BR clock period})}$$

Time Constant Values for Standard Baud Rates at BR Clock = 3.9936 MHz

Rate (Baud)	Time Constant (decimal/Hex notation)		Error
19200	102	(0066)	0
9600	206	(00CE)	0
7200	275	(0113)	0.12%
4800	414	(019E)	0
3600	553	(0229)	0.06%
2400	830	(033E)	0
2000	996	(03E4)	0.04%
1800	1107	(0453)	0.03%
1200	1662	(067E)	0
600	3326	(0CFE)	0
300	6654	(19FE)	0
150	13310	(33FE)	0
134.5	14844	(39FC)	0.0007%
110	18151	(46E7)	0.0015%
75	26622	(67FE)	0
50	39934	(98FE)	0

Digital Phase-Locked Loop

The SCC contains a digital phase-locked loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock or both.

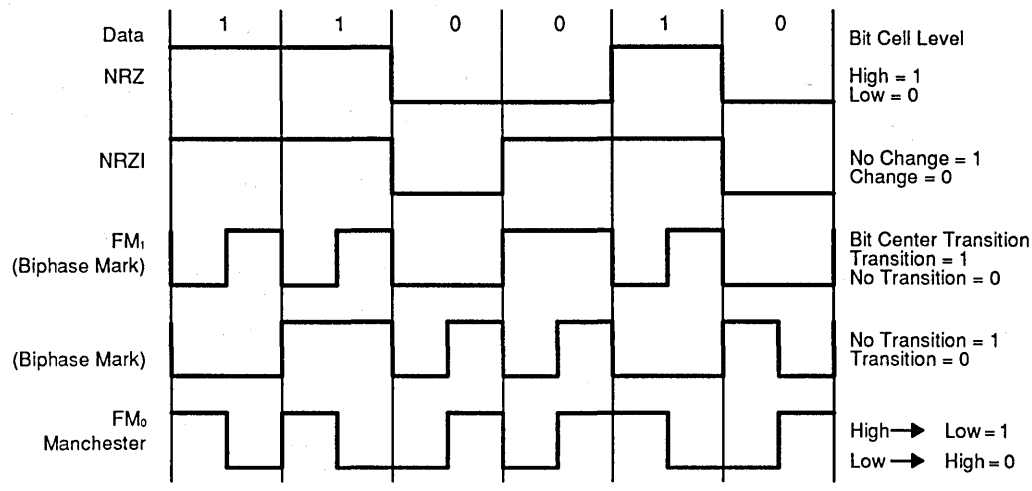

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Figure 5. Data Encoding Methods

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

Data Encoding

The SCC may be programmed to encode and decode the serial data in four different ways (Figure 5). In NRZ encoding, a 1 is represented by a High level, and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level, and a 0 is represented by a change in level. In FM_1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell, and a 0 is represented by no additional transition at the center of the bit cell. In FM_0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1, the bit is a 0. If the transition is 1/0, the bit is a 1.

Auto Echo and Local Loopback

The SCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes but works in synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed, and the programmer is responsible for disabling transmitter interrupts and $\overline{\text{WAIT/REQUEST}}$ on transmit.

The SCC is also capable of local loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data, and RxD is ignored (except to be echoed out via TxD). The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

I/O Interface Capabilities

The SCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

Polling

All interrupts are disabled. Three status registers in the SCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

Interrupts

When a SCC responds to an Interrupt Acknowledge signal ($\overline{\text{INTACK}}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 7 and 8).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other two bits are related to the Z-Bus interrupt priority chain (Figure 6). As a Z-Bus peripheral, the SCC may request an interrupt only when no higher priority device is requesting one; e.g., when IEI is High. If the device in question requests an interrupt, it pulls down $\overline{\text{INT}}$. The CPU then responds with $\overline{\text{INTACK}}$, and the interrupting device places the vector on the A/D bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the INT output is pulled Low, requesting an interrupt. In the SCC; if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the Receive can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition.
- Interrupt on all Receive Characters or Special Receive condition.
- Interrupt on Special Receive condition only.

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in asynchronous mode, End-of-Frame in SDLC mode, and optionally, a parity error. The Special Receive Condition Interrupt is different from an ordinary receive character available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive condition any time after the first receive character interrupt.

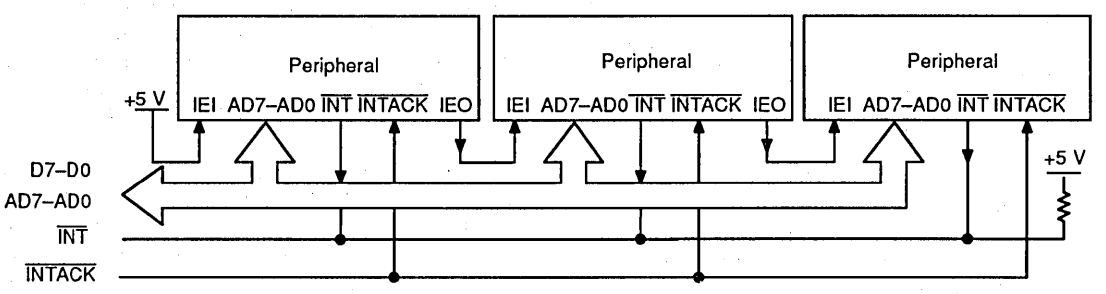


Figure 6. Z-Bus Interrupt Schedule

00970F-009

The main function of the External/Status Interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins; however, an External/Status Interrupt is also caused by a Transmit Underrun condition, a zero count in the baud rate generator, the detection of a Break (asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the SCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next, message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA Block Transfer

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{WAIT/REQUEST}$ output in conjunction with the $\overline{WAIT/REQUEST}$ bits in WR1. The WAIT/$\overline{REQUEST}$ output can be defined under software control as a $\overline{WAIT}$ line in the CPU Block Transfer mode or as a $\overline{REQUEST}$ line in the DMA Block Transfer mode.

To a DMA controller, the SCC $\overline{REQUEST}$ output indicates that the SCC is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{DTR/REQUEST}$ line allows full-duplex operation under DMA control.

PROGRAMMING INFORMATION

Each channel has 15 write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has 8 read registers from which the system can read status, baud rate, or interrupt information.

In the Am8530H only the four data registers (Read or Write for Channels A and B) are directly selected by a High on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$, and A/$\overline{B}$ pins. All other registers are addressable indirectly by the content of Write Register 0 in conjunction with a Low on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$, and A/$\overline{B}$ pins. If bit D3 in WR0 is 1 and bits 5 and 6 are 0, then bits 0, 1, 2 address the higher registers 8 through 15. If bits 4, 5, 6 contain a different code, bits 0, 1, 2 address the lower registers 0 through 7 as shown in Table 2.

Writing to or reading from any register except RR0, WR0 and the Data Registers thus involves two operations.

First, write the appropriate code into WR0, then follow this by a write or read operation on the register thus specified. Bits 0 through 4 in WW0 are automatically cleared after this operation, so that WW0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the A/D input (High = A, Low = B).

In Am8530H, the system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set and, finally, receiver or transmitter enable.

Read Registers

The SCC contains eight Read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt

Pending (IP) bits (Channel A). Figure 7 shows the formats for each Read register.

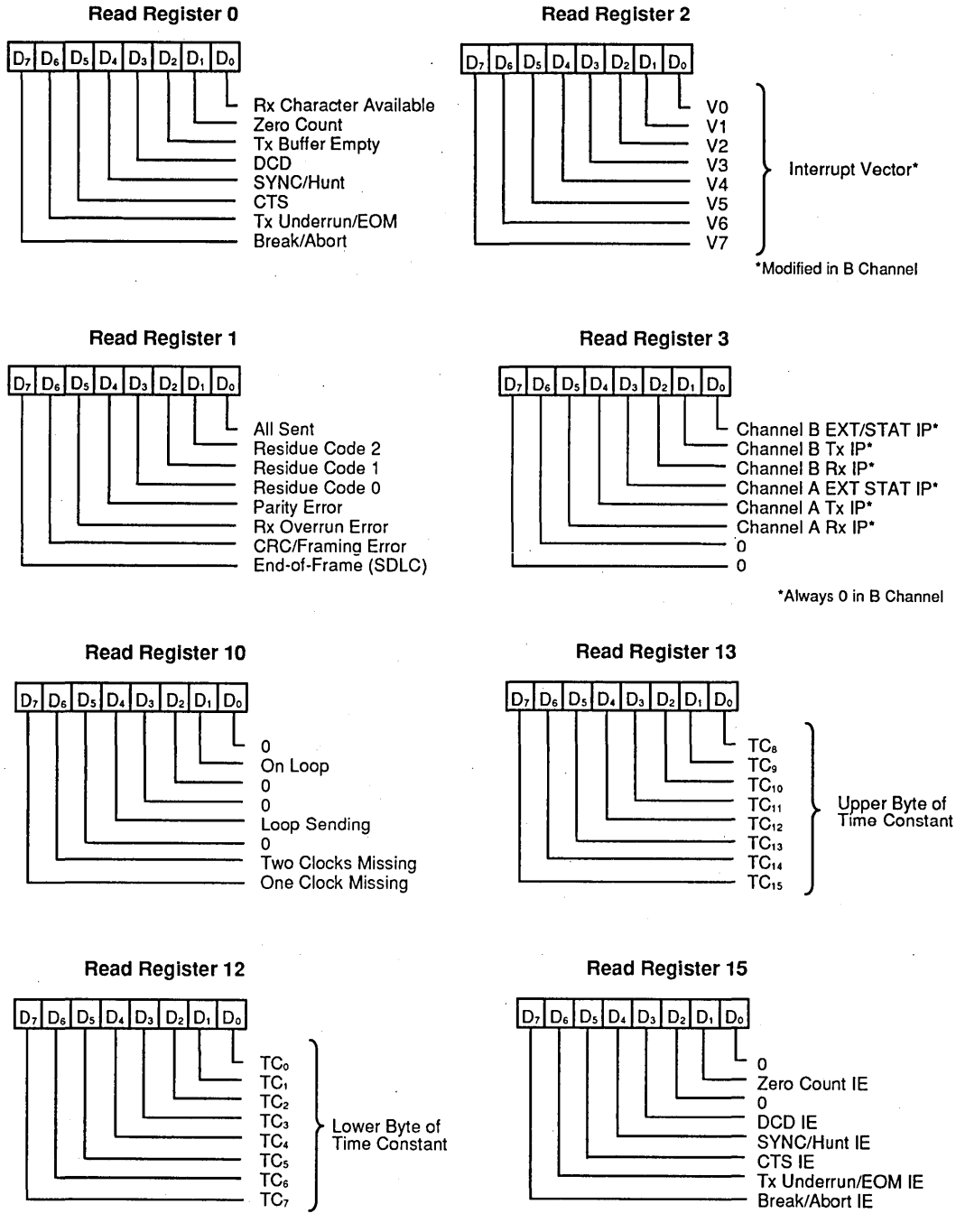
The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

Write Registers

The SCC contains 15 Write registers (16 counting WR8, the transmit buffer) in each channel. These Write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that can be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 8 shows the format of each Write register.

Table 2. Register Addressing

D/$\overline{C}$ "Point High" Code in WR0:		D2 In WR0:	D1 In WR0:	D0	Write Register	Read Register
High	Either Way	X	X	X	Data	Data
Low	Not True	0	0	0	0	0
Low	Not True	0	0	1	1	1
Low	Not True	0	1	0	2	2
Low	Not True	0	1	1	3	3
Low	Not True	1	0	0	4	(0)
Low	Not True	1	0	1	5	(1)
Low	Not True	1	1	0	6	(2)
Low	Not True	1	1	1	7	(3)
Low	True	0	0	0	Data	Data
Low	True	0	0	1	9	–
Low	True	0	1	0	10	10
Low	True	0	1	1	11	(15)
Low	True	1	0	0	12	12
Low	True	1	0	1	13	13
Low	True	1	1	0	14	(10)
Low	True	1	1	1	15	15



00970F-010

Figure 7. Read Register Bit Functions

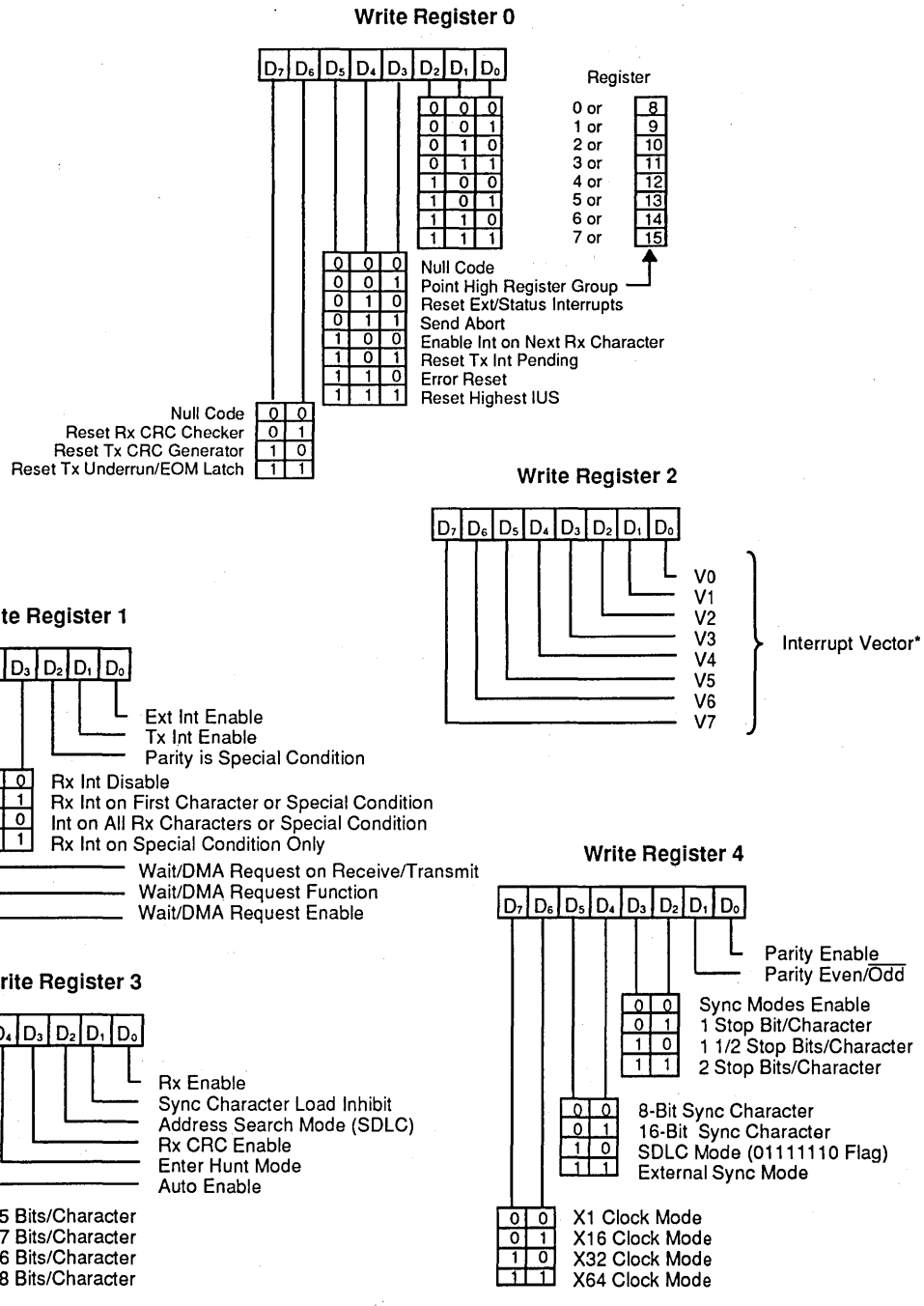
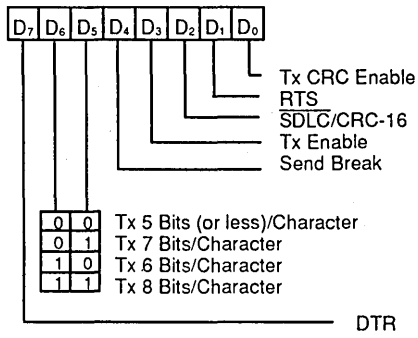


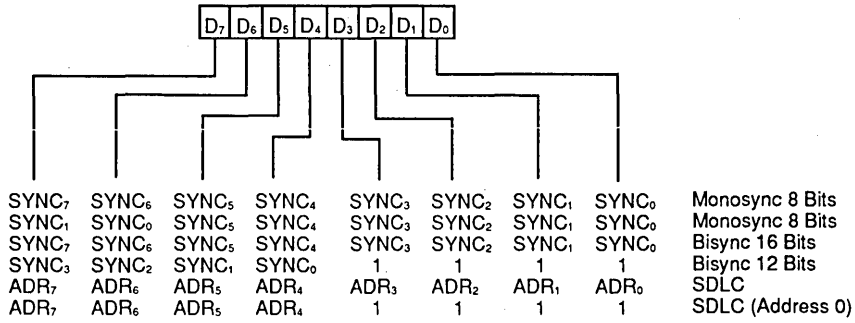
Figure 8. Write Register Bit Functions (Continued)

00970F-011B

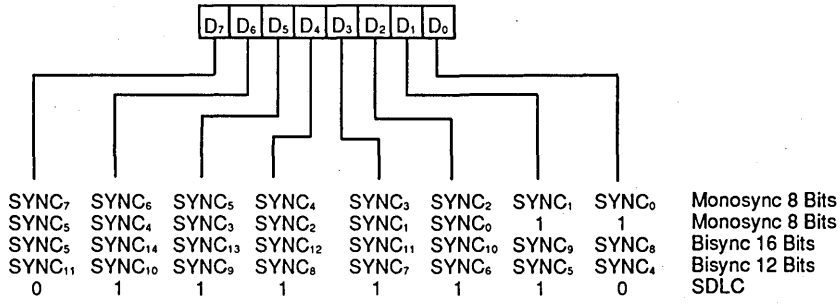
Write Register 5



Write Register 6

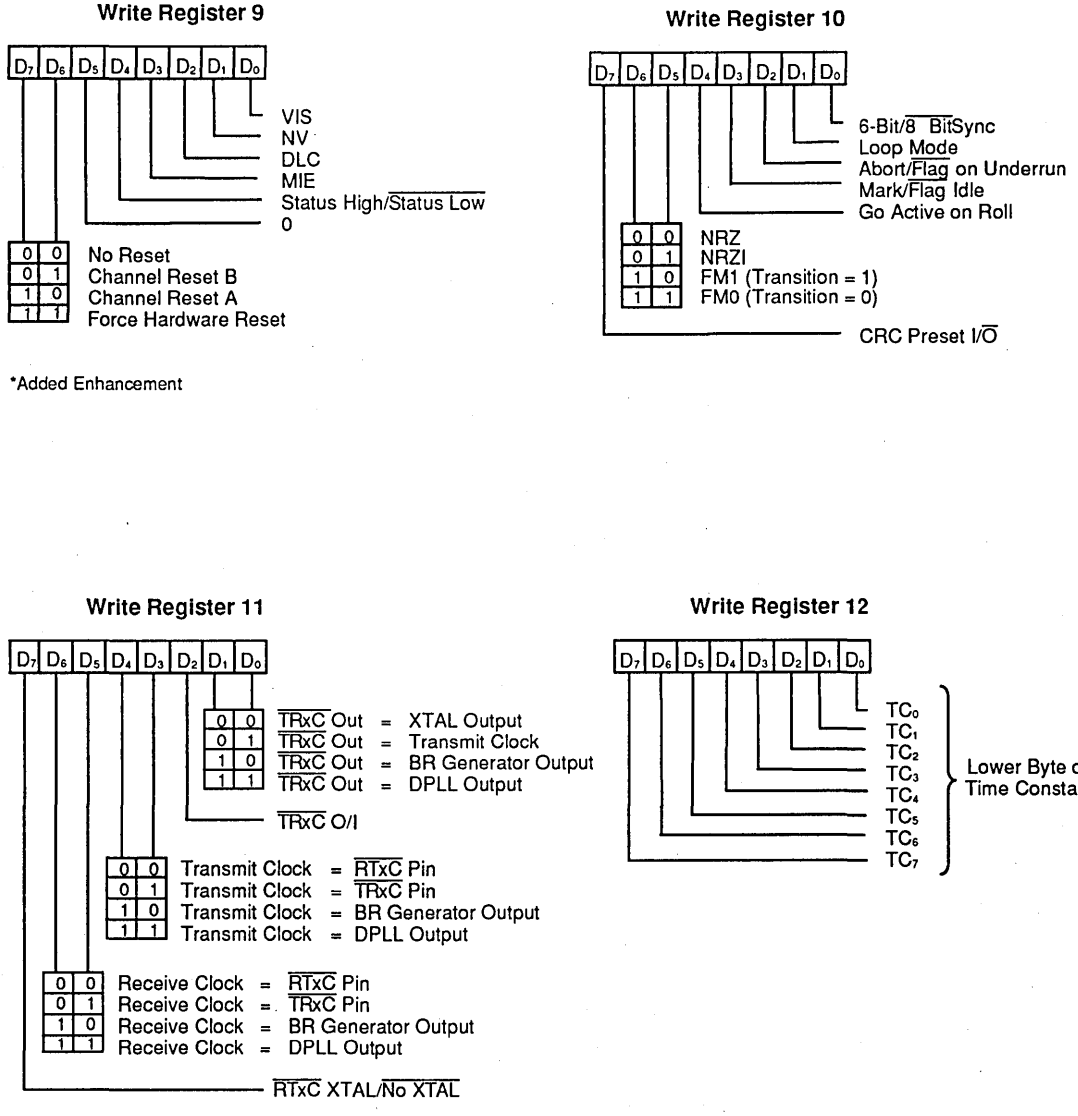


Write Register 7



00970F-011

Figure 8. Write Register Bit Functions (Continued)



*Added Enhancement

00970F-011

Figure 8. Write Register Bit Functions (Continued)

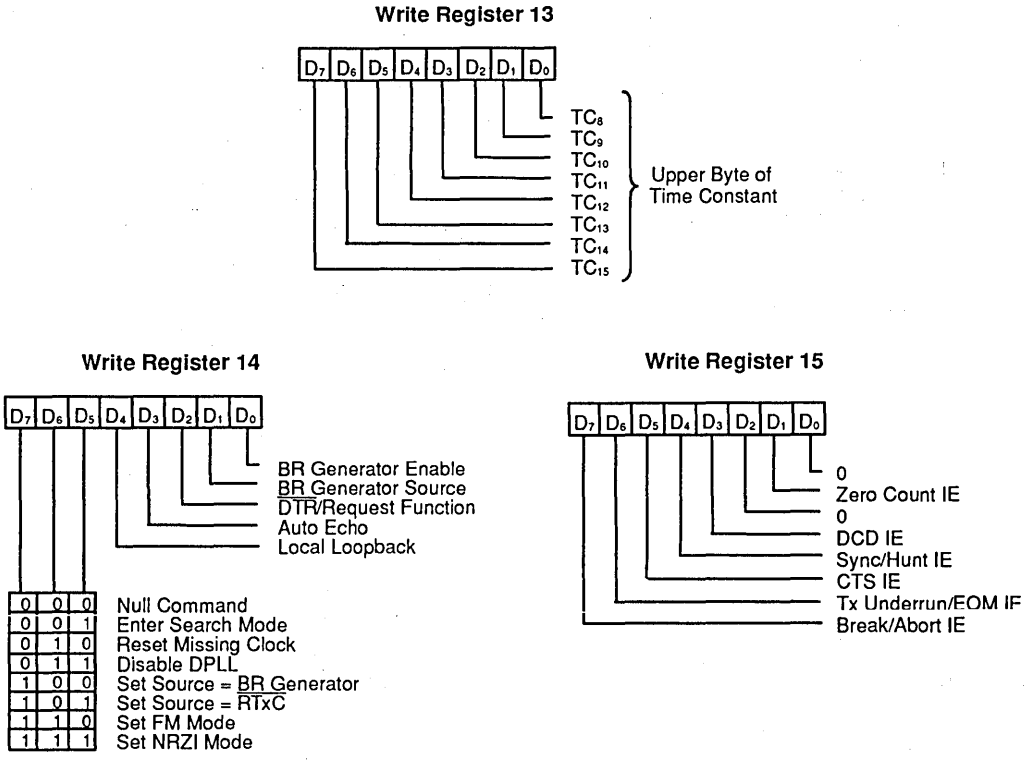


Figure 8. Write Register Bit Functions (Continued)

00970F-011

Am8530H Timing

The SCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC. The recovery time required for proper operation is specified from the rising edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the SCC to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the SCC. This time must be at least 6 PCLK cycles plus 200 ns.

Read Cycle Timing

Figure 9 illustrates Read cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

Write Cycle Timing

Figure 10 illustrates Write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened.

Interrupt Acknowledge Cycle Timing

Figure 11 illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{INTACK}$ goes Low and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is High when $\overline{RD}$ falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to $\overline{RD}$ Low by placing its interrupt vector on D7–D0; it then sets the appropriate interrupt-under-service latch internally.

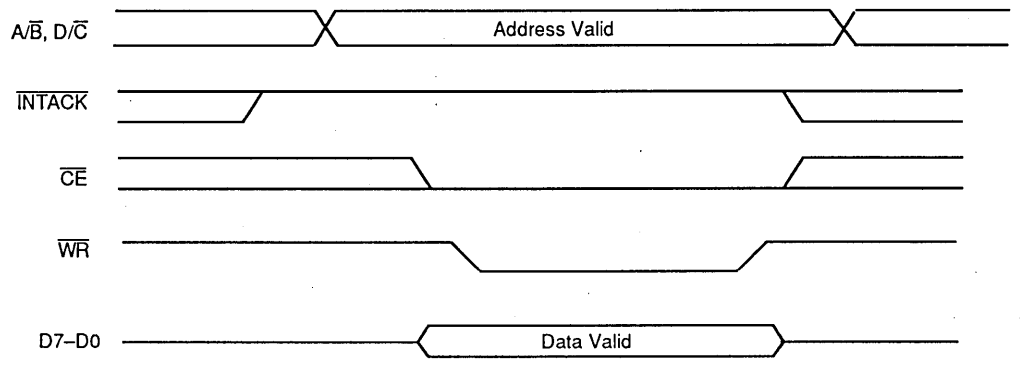


Figure 9. Read Cycle Timing

00970F-015

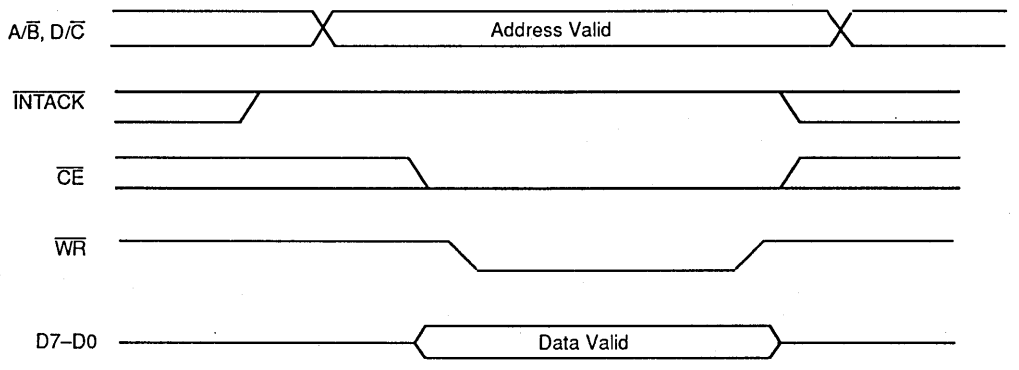


Figure 10. Write Cycle Timing

00970F-016

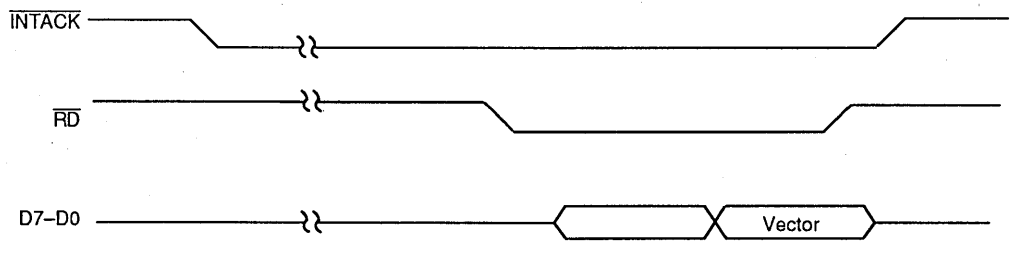


Figure 11. Interrupt Acknowledge Cycle Timing

00970F-017

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to + 150°C
Voltage at any Pin Relative to Vss	−0.5 to + 7.0 V
Power Dissipation	1.8 W

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to + 70°C
Supply Voltage (V_{CC})	5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IH}	Input High Voltage	Commercial	2.2	V_{CC} +0.3	V
V_{IL}	Input Low Voltage		−0.3	0.8	V
V_{OH}	Output High Voltage	I_{OH} = −250 µA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = +2.0 mA		0.4	V
I_{IL}	Input Leakage	0.4 V ≤ V_{IN} ≤ 2.4 V		±10.0	µA
I_{OL}	Output Leakage	0.4 V ≤ V_{OUT} ≤ 2.4 V		±10.0	µA
I_{CC}	V_{CC} Supply Current			250	mA
C_{IN}	Input Capacitance	Unmeasured pins returned		10	pF
C_{OUT}	Output Capacitance	to ground f = 1 MHz at		15	pF
C_{MO}	Bidirectional Capacitance	T_A = 25°C		20	pF

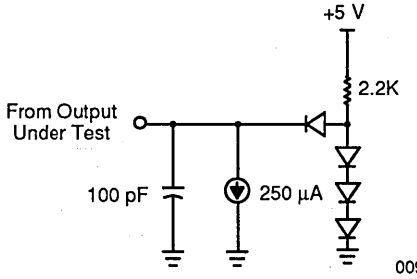
Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.5 V ≤ V_{CC} ≤ +5.5 V
GND = 0 V
0°C ≤ T_A ≤ 70°C

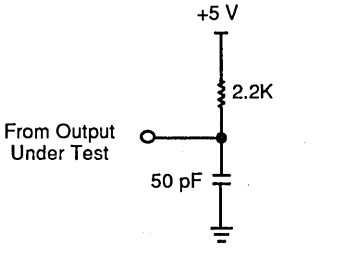
SWITCHING TEST CIRCUITS

Standard Test Load



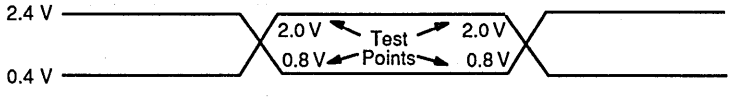
00970F-028

Open-Drain Test Load



00970F-029

Switching Test Input/Output Waveform



00970F-030

AC testing: Inputs are driven at 2.4 V for a logic 1 and 0.4 V for a logic 0.
Timing measurements are made at 2.0 V for a logic 1 and 0.8 V for logic 0.

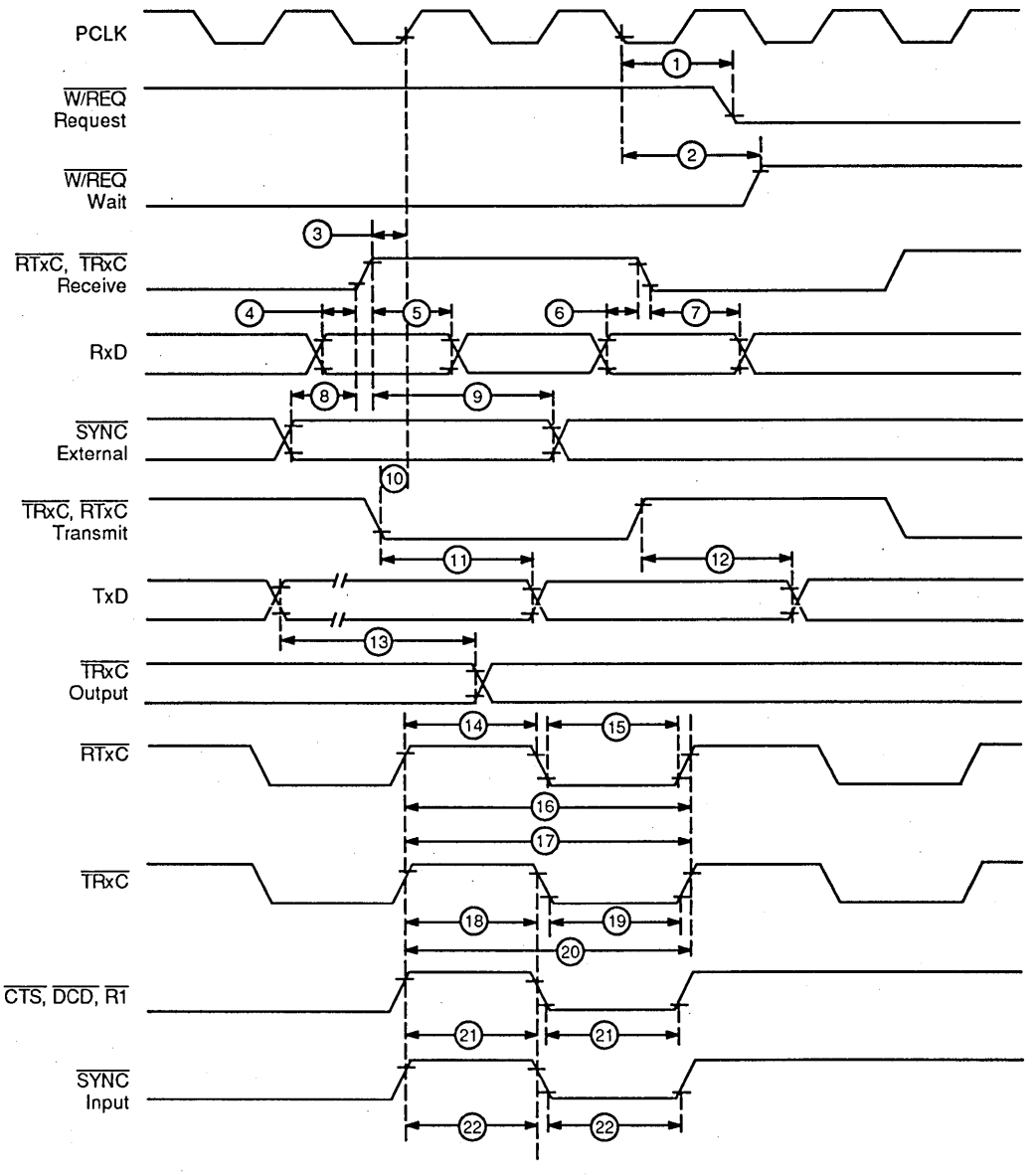
SWITCHING CHARACTERISTICS over operating range

General Timing

No.	Parameter Symbol	Parameter Description	4 MHz		6 MHz		8 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay		250		250		250	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		350		350	ns
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (Notes 1 & 4)	80	T_{WPCL}	70	T_{WPCL}	60	T_{WPCL}	ns
4	TsRXD(RXCr)	RxD to RxC ↑ Setup Time (XI Mode) (Note 1)	0		0		0		ns
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (XI Mode) (Note 1)	150		150		150		ns
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		0		ns
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (XI Mode) (Notes 1, 5)	150		150		150		ns
8	TsSY(RXC)	SYNC to RxC ↑ Setup Time (Note 1)	–200		–200		–200		ns
9	ThSY(RXC)	SYNC to RxC ↑ Hold Time (Note 1)	3TcPC +400		3TcPC +320		3TcPC +250		ns
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time (Notes 2, 4)	0		0		0		ns
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (XI Mode) (Note 2)		300		230		200	ns
12	TdTXCr(TXD)	TxC ↑ to TxD Delay (XI Mode) (Notes 2, 5)		300		230		200	ns
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200		200		200	ns
14	TwRTXh	RTxC High Width (Note 6)	180		180		150		ns
15	TwRTXl	RTxC Low Width (Note 6)	180		180		150		ns
16	TcRTX	RTxC Cycle Time (Notes 6, 7)	1000		660		500		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	250	1000	165	1000	125	1000	ns
18	TwTRXh	TRxC High Width (Note 6)	180		180		150		ns
19	TwTRXl	TRxC Low Width (Note 6)	180		180		150		ns
20	TcTRX	TRxC Cycle Time (Notes 6, 7)	1000		660		500		ns
21	TwEXT	DCD or CTS Pulse Width	200		200		200		ns
22	TwSY	SYNC Pulse Width	200		200		200		ns

Notes:

1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30-pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.



00970F-018

Figure 12. General Timing

SWITCHING CHARACTERISTICS over operating range (Continued)

System Timing

No.	Parameter Symbol	Parameter Description	4 MHz		6 MHz		8 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TdRXC(REQ)	$\overline{RXC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	8	12	TcPc
2	TdRXC(W)	$\overline{RXC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	8	14	8	14	TcPc
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	4	7	4	7	TcPc
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	10	16	10	16	TcPc
5	TdTXC(REQ)	$\overline{TxC}$ ↑ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	5	8	TcPc
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	5	11	5	11	TcPc
7	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	4	7	TcPc
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	6	10	6	10	TcPc
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	2	6	TcPc
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	2	6	TcPc

Notes:

1. Open-drain, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

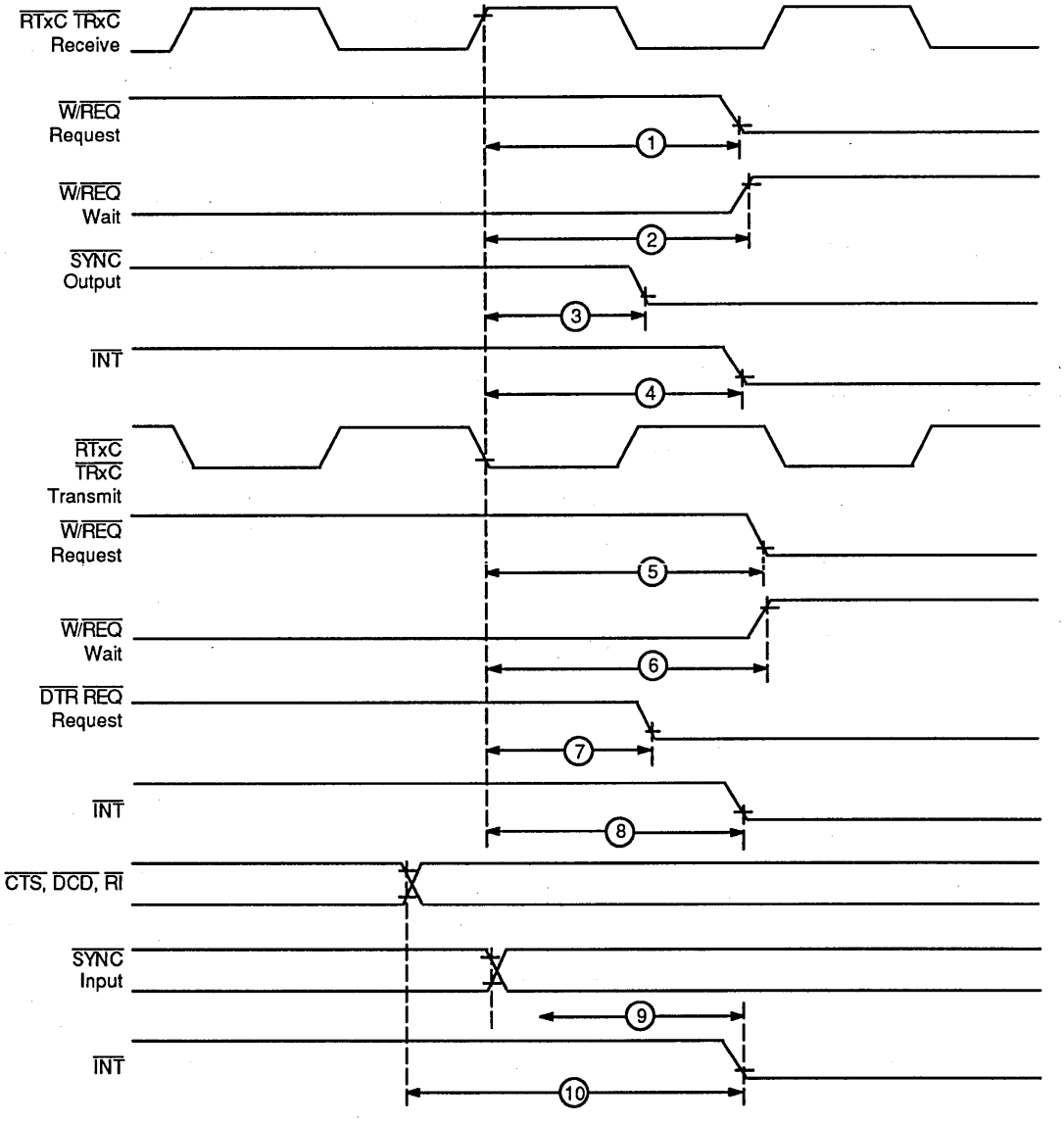


Figure 13. System Timing

00970F-019

SWITCHING CHARACTERISTICS over operating range

Read and Write Timing

No.	Parameter Symbol	Parameter Description	4 MHz		6 MHz		8 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TwPCl	PCLK Low Width	105	2000	70	1000	50	1000	ns
2	TwPCh	PCLK High Width	105	2000	70	1000	50	1000	ns
3	TfPC	PCLK Fall Time		20		10		10	ns
4	TrPC	PCLK Rise Time		20		10		10	ns
5	TcPC	PCLK Cycle Time	250	4000	165	2000	125	2000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Set-Up Time	80		80		70		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Set-Up Time	80		80		70		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Set-Up Time	10		10		10		ns
11	TsAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Set-Up Time (Note 1)	200		160		145		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
13	TsIAi(WR)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Set-Up Time (Note 1)	200		160		145		ns
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
15	TsCE(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Set-Up Time	80		80		70		ns
16	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
17	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Set-Up Time	100		70		60		ns
18	TsCE(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Set-Up Time	100		70		60		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Set-Up Time (Note 1)	0		0		0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Set-Up Time (Note 1)	100		70		60		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	240		200		150		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250		180		140	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		70		45		140	ns

Notes:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5 V change in the output with a maximum DC load and minimum AC load.

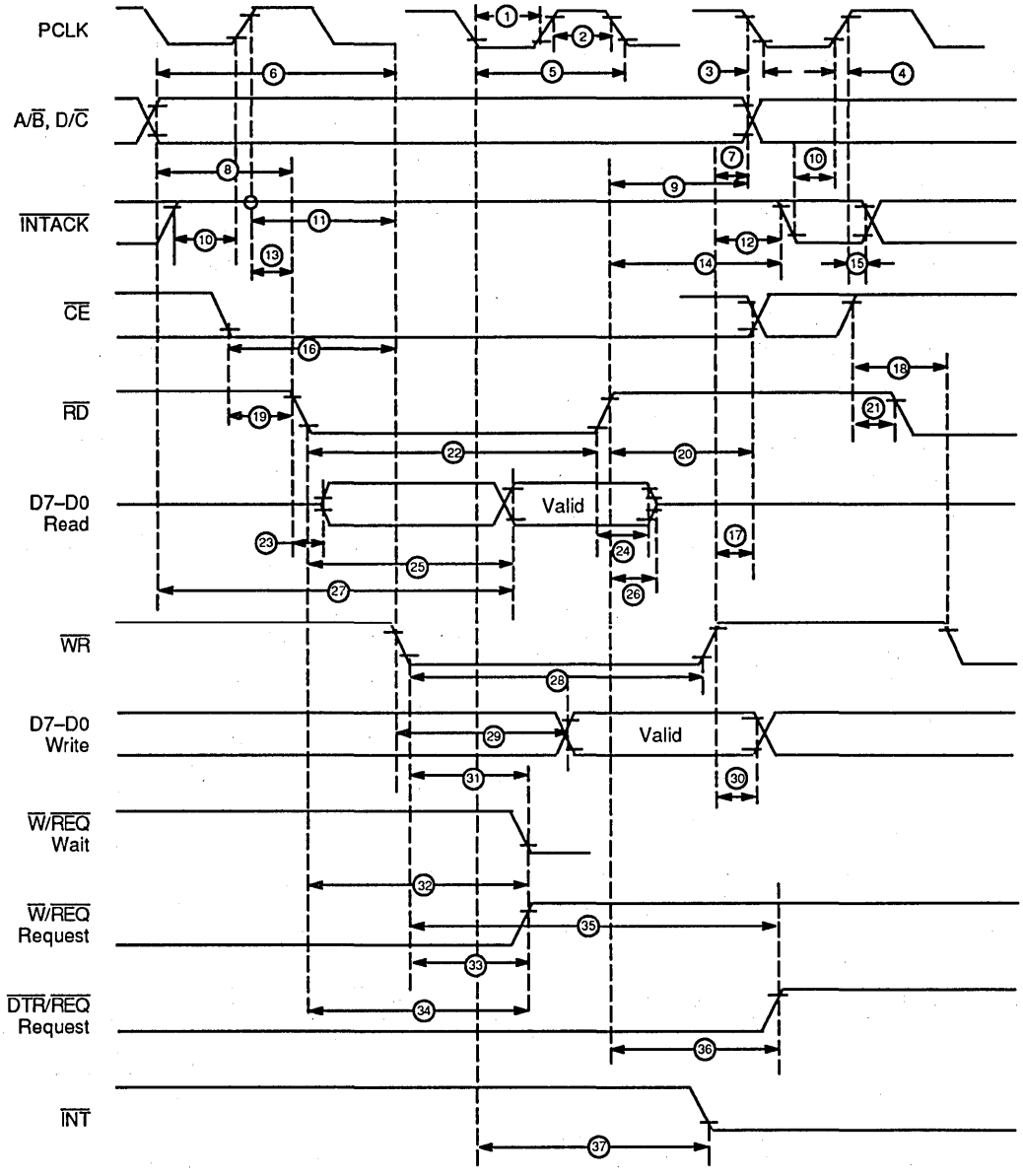


Figure 14. Read and Write Timing

00970F-021

SWITCHING CHARACTERISTICS over operating range

Interrupt Acknowledge Timing, Reset Timing, Cycle Timing

No.	Parameter Symbol	Parameter Description	4 MHz		6 MHz		8 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		300		280		220	ns
28	TwWRI	$\overline{WR}$ Low Width	240		200		150		ns
29	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Set-Up Time	10		10		10		ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 4)		240		200		170	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 4)		240		200		170	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200		170	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200		170	ns
35	TdWRr(REQ)	$\overline{WR}$ ↑ $\overline{DTR/REQ}$ Not Valid Delay		4TcPC		4TcPC		4TcPC	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ $\overline{DTR/REQ}$ Not Valid Delay		4TcPC		4TcPC		4TcPC	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 4)		500		500		500	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 5)	250		200		150		ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	250		200		150		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		250		180		140	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Set-Up Time	120		100		95		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Hold Time	0		0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100		95	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250		250		200	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 4)		500		500		450	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	30		15		15		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	30		30		20		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250		200		150		ns
49	Trc	Valid Access Recovery Time (Note 3)	4TcPC		4TcPC		4TcPC		ns

Notes:

3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAI(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

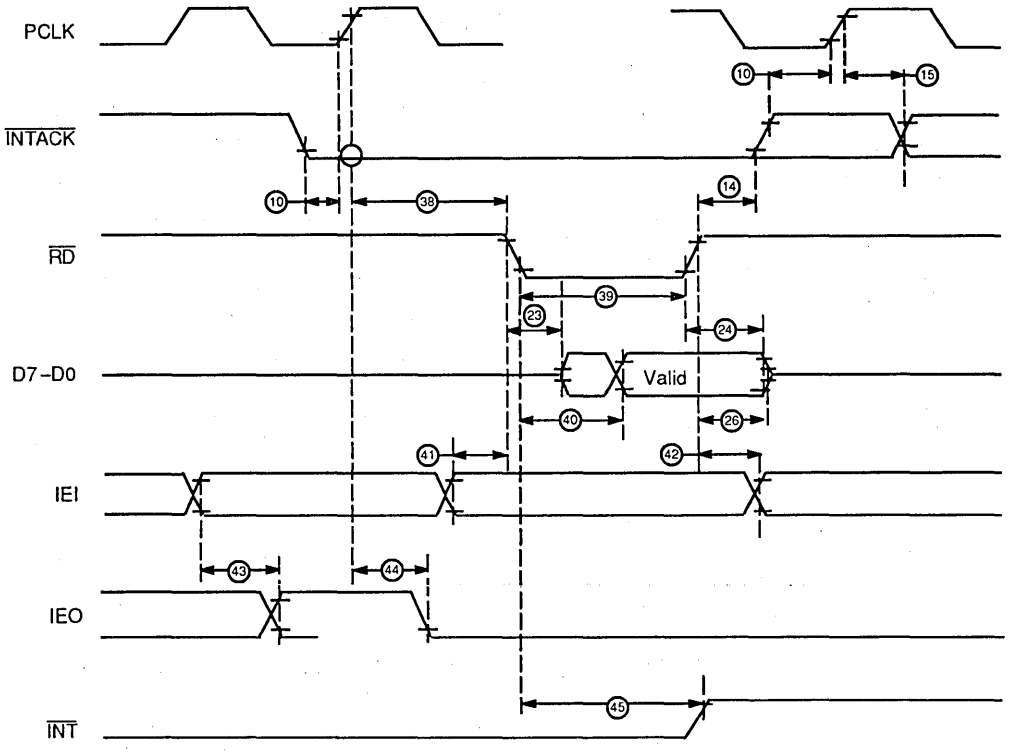


Figure 15. Interrupt Acknowledge Timing

00970F-025

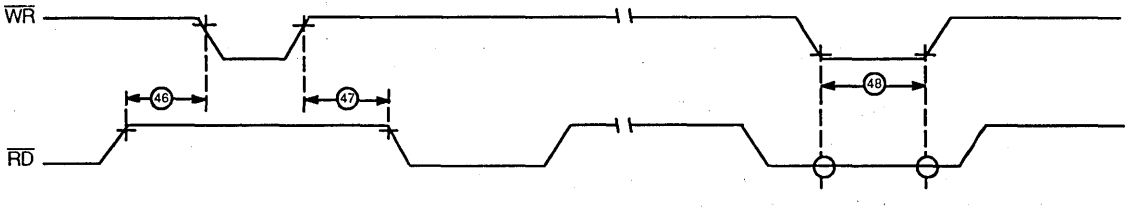


Figure 16. Reset Timing

00970F-026

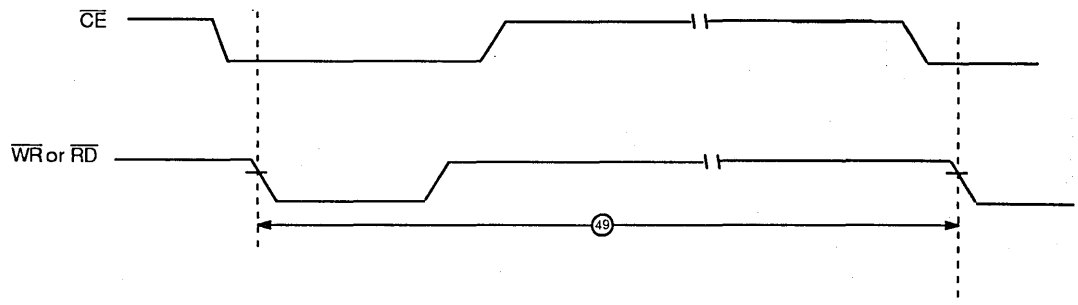


Figure 17. Cycle Timing

00970G–027

Am85C30

Enhanced Serial Communications Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fastest data rate of any Am8530**
  - 8.192 MHz / 2.048 Mb/s
  - 10 MHz / 2.5 Mb/s
  - 16.384 MHz / 4.096 Mb/s
- **Low-power CMOS technology**
- **Pin and function compatible with other NMOS and CMOS 8530s**
- **Easily interfaced with most CPUs**
  - Compatible with non-multiplexed bus
- **Many enhancements over NMOS Am8530H**
  - Allows Am85C30 to be used more effectively in high-speed applications
  - Improves interface capabilities
- **Two independent full-duplex serial channels**
- **Asynchronous mode features**
  - Programmable stop bits, clock factor, character length and parity
  - Break detection/generation
  - Error detection for framing, overrun, and parity
- **Synchronous mode features**
  - Supports IBM® BISYNC, SDLC, SDLC Loop, HDLC, and ADCCP Protocols
  - Programmable CRC generators and checkers
  - SDLC/HDLC support includes frame control, zero insertion and deletion, abort, and residue handling
- **Enhanced SCC functions support high-speed frame reception using DMA**
  - 14-bit byte counter
  - 10 × 19 SDLC/HDLC Frame Status FIFO
  - Independent Control on both channels
  - Enhanced operation does not allow special receive conditions to lock the 3-byte DATA FIFO when the 10 × 19 FIFO is enabled
- **Local Loopback and Auto Echo modes**
- **Internal or external character synchronization**
- **2-Mb/s FM encoding transmit and receive capability using internal DPLL for 16.384-MHz product**
- **Internal synchronization between RxC to PCLK and TxC to PCLK**
  - This allows the user to eliminate external synchronization hardware required by the NMOS device when transmitting or receiving data at the maximum rate of 1/4 PCLK frequency

GENERAL DESCRIPTION

AMD's Am85C30 is an enhanced pin-compatible version of the popular Am8530H Serial Communications Controller. The Enhanced Serial Communications Controller (ESCC) is a high-speed, low-power, multi-protocol communications peripheral designed for use with 8- and 16-bit microprocessors. It has two independent, full-duplex channels and functions as a serial-to-parallel, parallel-to-serial converter/controller. AMD's proprietary enhancements make the Am85C30 easier to interface and more effective in high-speed applications due to a reduction in software burden and the elimination of the need for some external glue logic.

The Am85C30 is easy to use due to a variety of sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic. The device can generate and check CRC codes in any SYNC mode, and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

This versatile device supports virtually any serial data transfer application such as networks, modems, cassettes, and tape drivers. The ESCC is designed for non-multiplexed buses and is easily interfaced with most CPUs, such as 80188, 80186, 80286, 8080, Z80, 6800, 68000 and MULTIBUS™.

Enhancements that allow the Am85C30 to be used more effectively in high-speed applications include:

- a 10 × 19 bit SDLC/HDLC frame status FIFO array
- a 14-bit SDLC/HDLC frame byte counter
- automatic SDLC/HDLC opening frame flag transmission
- TxD pin forced High in SDLC NRZI mode after closing flag
- automatic SDLC/HDLC Tx underrun/EOM flag reset

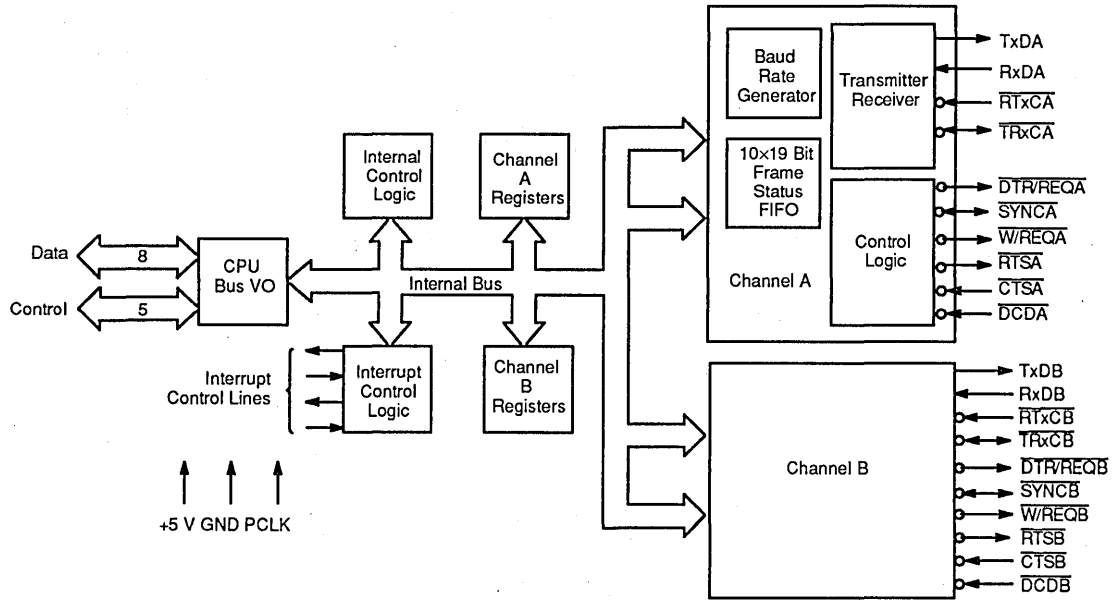
Publication # 10216 Rev. E Amendment /0
Issue Date: November 1991

- external PCLK to $\overline{RxC}$ or $\overline{TxC}$ synchronization requirement eliminated for PCLK divide-by-four operation

Other enhancements to improve the Am85C30 interface capabilities include:

- write data valid setup time to falling edge of $\overline{WR}$ requirement eliminated
- reduced $\overline{INT}$ response time
- reduced access recovery time (t_{RC}) to 3 PCLK best case (3 1/2 PCLK worst case)
- improved $\overline{Wait}$ timing
- Write Registers WR3, WR4, WR5, and WR10 made readable
- lower priority interrupt masking without $\overline{INTACK}$
- complete SDLC/HDLC CRC character reception

BLOCK DIAGRAM



10216A-001A

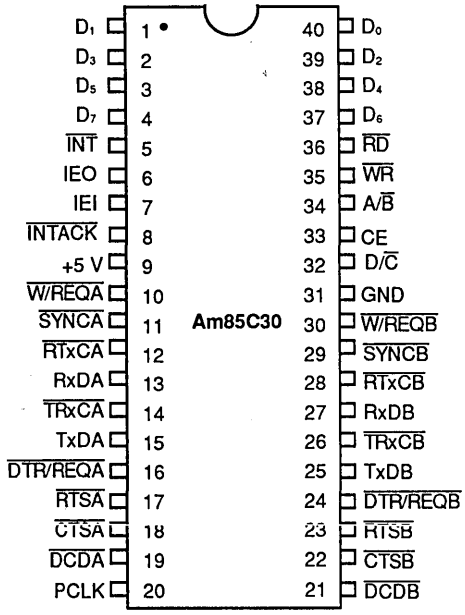
RELATED AMD PRODUCTS

Part No.	Description	Part No.	Description
Am7960	Coded Data Transceiver	Am9517A	DMA Controller
80186	Highly Integrated 16-Bit Microprocessor	5380, 53C80	SCSI Bus Controller
		80188	Highly Integrated 8-Bit Microprocessor
80286, 80C286	High-Performance 16-Bit Microprocessor	Am386™	High-Performance 32-Bit Microprocessor

CONNECTION DIAGRAMS

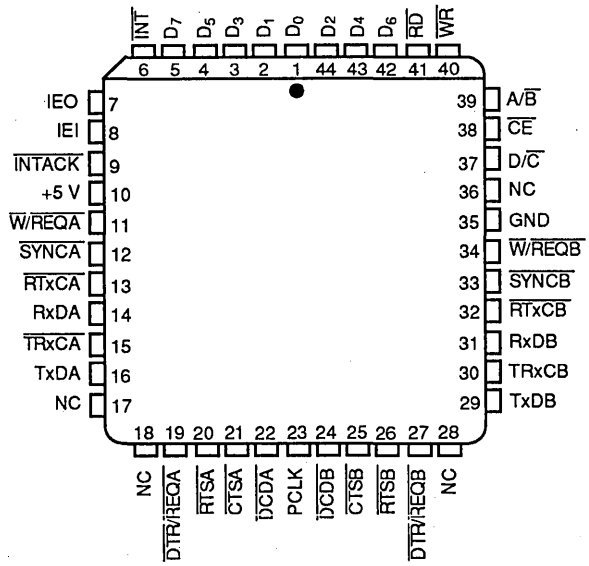
Top View

DIP



10216A-002A

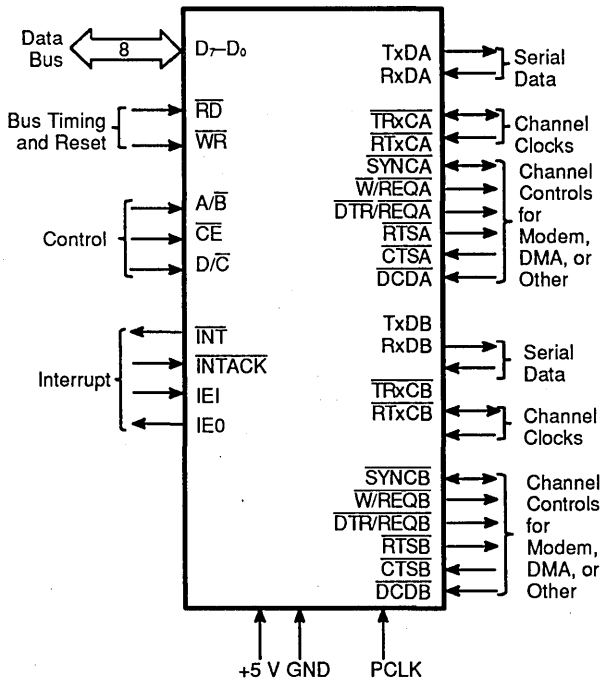
PLCC, LCC



10216A-003A

Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL

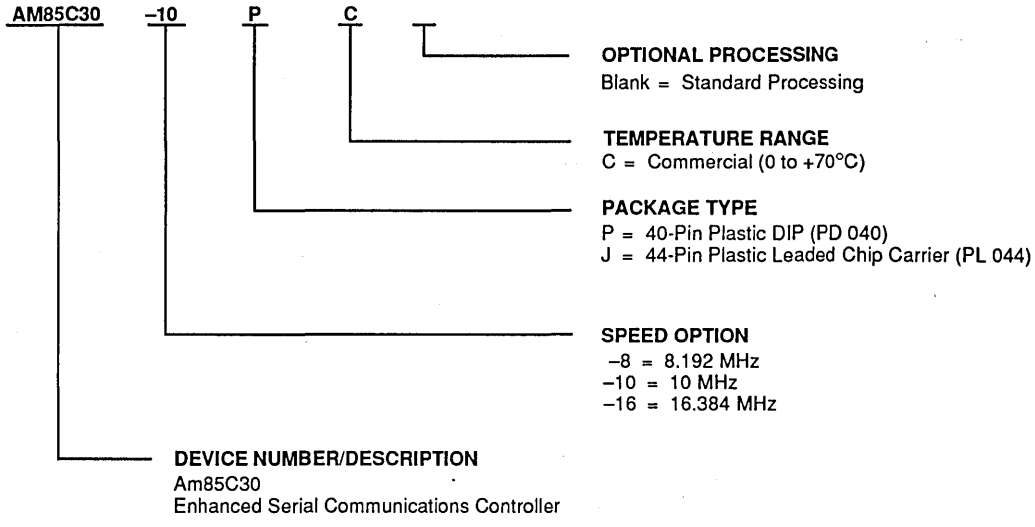


10216A-004A

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM85C30-8 AM85C30-10 AM85C30-16	PC, JC

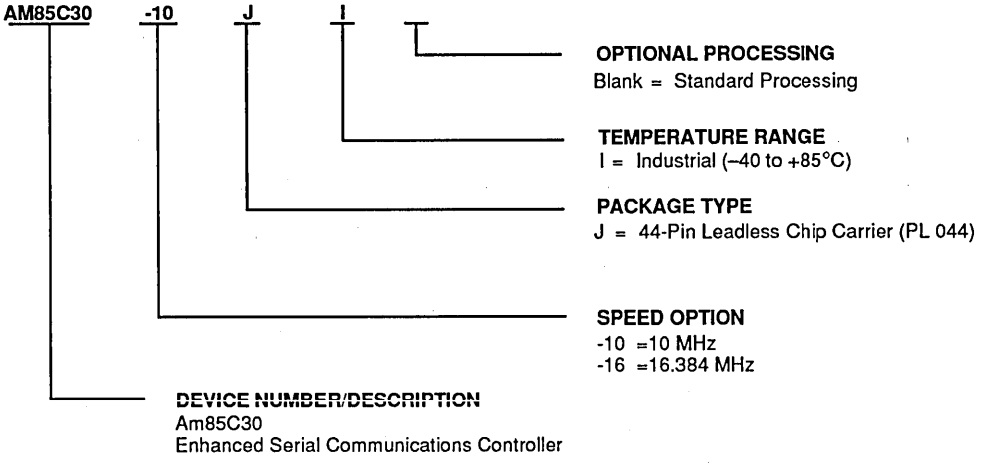
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

Industrial Products

AMD industrial products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM85C30-10 AM85C30-16	JI

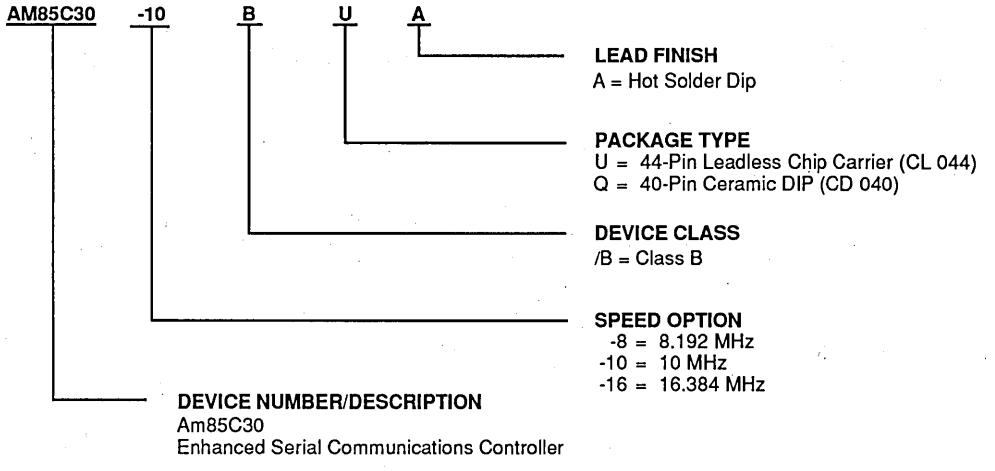
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM85C30-8 AM85C30-10 AM85C30-16	BQA, BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Bus Timing and Reset

$\overline{RD}$
Read (Input; Active Low)

This signal indicates a Read operation and, when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

$\overline{WR}$
Write (Input; Active Low)

When the SCC is selected, this signal indicates a Write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.

Channel Clocks

$\overline{RTxCA}$, $\overline{RTxCB}$
Receive/Transmit Clocks (Inputs; Active Low)

These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

$\overline{TRxCA}$, $\overline{TRxCB}$
Transmit/Receive Clocks (Inputs/Outputs; Active Low)

These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

Channel Controls for Modem, DMA, or Other

$\overline{CTSA}$, $\overline{CTSB}$
Clear to Send (Inputs; Active Low)

If these pins are programmed as Auto Enables, a Low on these inputs enables their respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and may interrupt the CPU on both logic level transitions.

$\overline{DCDA}$, $\overline{DCDB}$
Data Carrier Detect (Inputs; Active Low)

These pins function as receiver enables if they are programmed as Auto Enables; otherwise, they may be used as general-purpose input pins. Both are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and may interrupt the CPU on both logic level transitions.

$\overline{DTR/REQA}$, $\overline{DTR/REQB}$
Data Terminal Ready/Request (Outputs; Active Low)

These outputs follow the inverted state programmed into the DTR bit in WR5. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

$\overline{RTSA}$, $\overline{RTSB}$
Request to Send (Outputs; Active Low)

When the Request to Send (RTS) bit in Write Register 5 is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In SYNC mode, or in asynchronous mode with Auto Enable off, the $\overline{RTS}$ pins strictly follow the inverted state of the RTS bit. Both pins can be used as general-purpose outputs.

In SDLC mode, the AUTO RTS RESET enhancement described later in this document brings $\overline{RTS}$ High after the last 0 of the closing flag leaves the TxD pin.

$\overline{SYNCA}$, $\overline{SYNCB}$
Synchronization (Inputs/Outputs; Active Low)

These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low two receive clock cycles after the last bit in the SYNC character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which SYNC characters are recognized. The SYNC condition is not latched, so these outputs are active each time a SYNC pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

$\overline{W/REQA}$, $\overline{W/REQB}$
Wait/Request (Outputs; Open drain when programmed for a Wait function, driven High or Low when programmed for a Request function)

These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

Control

A/$\overline{B}$
Channel A/Channel B Select (Input)

This signal selects the channel in which the Read or Write operation occurs.

$\overline{CE}$
Chip Enable (Input; Active Low)

This signal selects the SCC for a Read or Write operation.

D/$\overline{C}$
Data/Control Select (Input)

This signal defines the type of information transferred to or from the SCC. A High means data is transferred; a Low indicates a command is transferred.

Data Bus

D_7–D_0
Data Bus (Input/Output; Three State)

These lines carry data and commands to and from the SCC.

Interrupt

IEI
Interrupt Enable In (Input; Active High)

IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO
Interrupt Enable Out (Output; Active High)

IEO is High only if IEI is High and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$
Interrupt Request (Output; Active Low, Open Drain)

This signal is activated when the SCC requests an interrupt.

$\overline{INTACK}$
Interrupt Acknowledge (Input; Active Low)

This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of PCLK.

Serial Data

RxDA, RxDB
Receive Data (Inputs; Active High)

These input signals receive serial data at standard TTL levels.

TxDA, TxDB
Transmit Data (Outputs; Active High)

These output signals transmit serial data at standard TTL levels.

Miscellaneous

GND
Ground

PCLK
Clock (Input)

This is the master SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock. PCLK is a TTL-level signal. Maximum transmit rate is 1/4 PCLK.

V_{CC}
+ 5 V Power Supply

ARCHITECTURE

The ESCC internal structure includes two full-duplex channels, two 10 × 19 bit SDLC/HDLC frame status FIFOs, two baud rate generators, internal control and interrupt logic, and a bus interface to a non-multiplexed bus. Associated with each channel are a number of Read and Write registers for mode control and status information, as well as logic necessary to interface with modems or other external devices (see Logic Symbol).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (Write) registers, two SYNC character (Write) registers, and four status (Read) registers. In addition, each baud rate generator has two (Read/Write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a Write register for the interrupt vector accessible through either channel, a Write-only Master Interrupt Control register, and three Read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the interrupt pending bits (A only).

The registers for each channel are designated as follows:

WR0–WR15—Write Registers 0 through 15. An additional Write register, WR7 Prime (WR7′), is available for enabling or disabling additional SDLC/HDLC enhancements if bit D_0 of WR15 is set.

RR0–RR3, RR10, RR12, RR13, RR15—Read Registers 0 through 3, 10, 12, 13, and 15.

If bit D_2 of WR15 is set, then two additional Read registers, RR6 and RR7, are available. These registers are used with the 10 × 19 bit Frame Status FIFO.

Table 1 lists the functions assigned to each Read and Write register. The ESCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

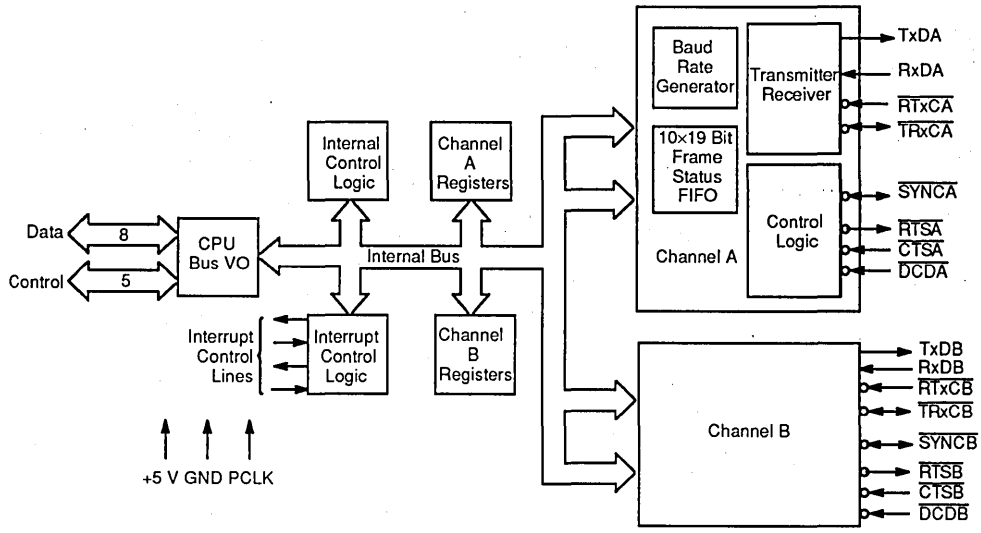


Figure 1. Block Diagram of ESCC Architecture

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Data Path

The transmit and receive data path illustrated in NO TAG is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data are routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data are routed through one of four main paths before they are transmitted from the Transmit Data output (TxD).

Table 1. Read and Write Register Functions

Read Register Functions		Write Register Functions	
RR0	Transmit/Receive buffer status and External status	**WR0**	Command Register, Register Pointers CRC initialize, initialization commands for the various modes, shift right/shift left command
RR1	Special Receive Condition status (also 10 × 19 bit FIFO Frame Reception Status if WR15 bit D_2 is set)	**WR1**	Interrupt conditions and data transfer mode definition
RR2	Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only)	**WR2**	Interrupt vector (accessed through either channel)
RR3	Interrupt Pending bits (Channel A only)	**WR3**	Receive parameters and control
RR6	LSB Byte Count (14-bit counter) (if WR15 bit D_2 set)	**WR4**	Transmit/Receive miscellaneous parameters and modes
RR7	MSB Byte Count (14-bit counter) and 10 × 19 bit FIFO Status (if WR15 bit D_2 is set)	**WR5**	Transmit parameters and controls
RR8	Receive buffer	**WR6**	Sync character or SDLC address field
RR10	Miscellaneous XMTR, RCVR status	**WR7**	Sync character or SDLC flag
RR12	Lower byte of baud rate generator time constant	**WR7′**	SDLC/HDLC enhancements (if bit D_0 of WR15 is set)
RR13	Upper byte of baud rate generator time constant	**WR8**	Transmit buffer
RR15	External/Status interrupt information	**WR9**	Master interrupt control and reset (accessed through either channel)
		WR10	Miscellaneous transmitter/receiver control bits, data encoding
		WR11	Clock mode control, Rx and Tx clock source
		WR12	Lower byte of baud rate generator time constant
		WR13	Upper byte of baud rate generator time constant
		WR14	Miscellaneous control bits, DPLL control
		WR15	External/Status interrupt control

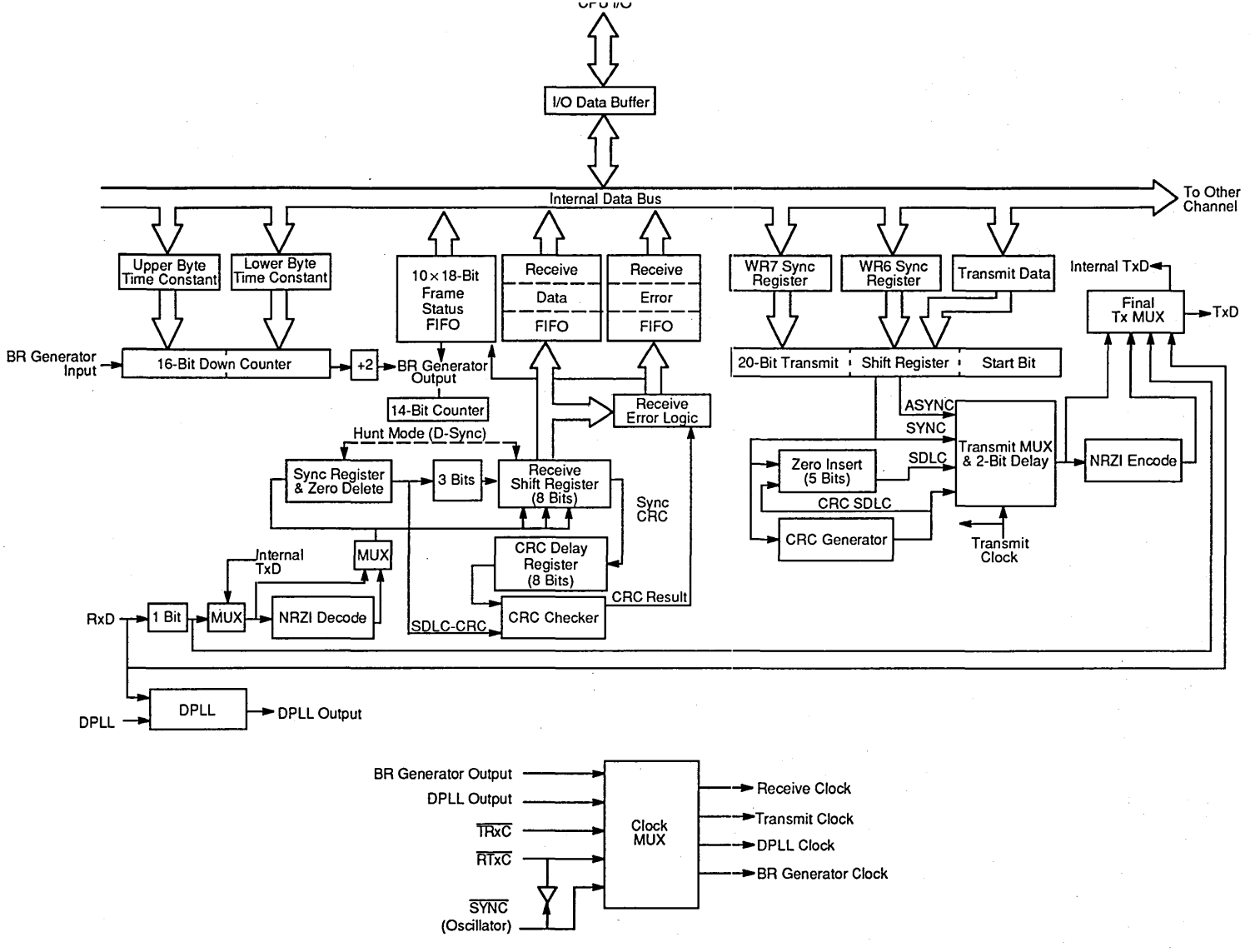


Figure 2. Data Path

DETAILED DESCRIPTION

The functional capabilities of the ESCC can be described from two different points of view: as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

Data Communications Capabilities

The ESCC provides two independent full-duplex channels programmable for use in any common asynchronous or SYNC data-communication protocol. Figure 3 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional even or odd parity. The transmitters can supply 1, 1 1/2, or 2 stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input. If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit; a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ESCC does not require symmetric transmit and receive clock signals—a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the $\overline{\text{SYNC}}$ pin may be programmed as an input used for functions, such as monitoring a ring indicator.

Synchronous Modes

The ESCC supports both byte-oriented and bit-oriented synchronous communication. SYNC byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit SYNC character (Monosync), any 12-bit or 16-bit SYNC pattern (Bisync), or with an external SYNC signal. Leading SYNC characters can be removed without interrupting the CPU.

5- or 7-bit SYNC characters are detected with 8- or 16-bit patterns in the ESCC by overlapping the larger pattern across multiple incoming SYNC characters as shown in Figure 4.

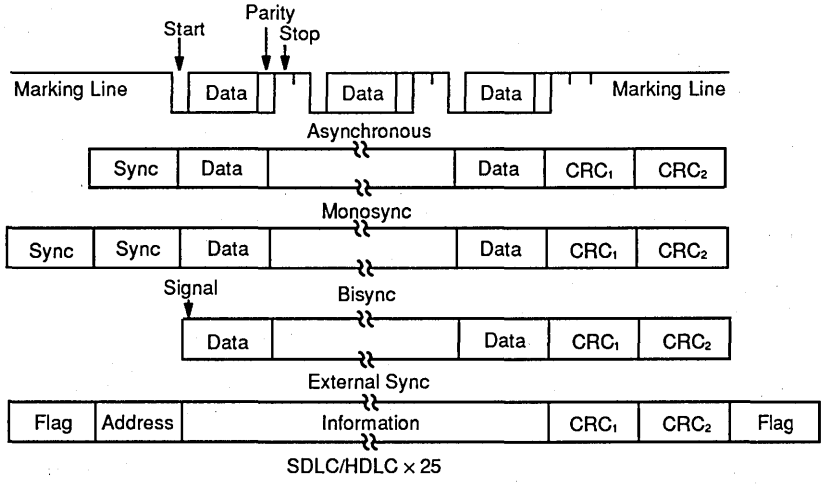


Figure 3. SCC Protocols

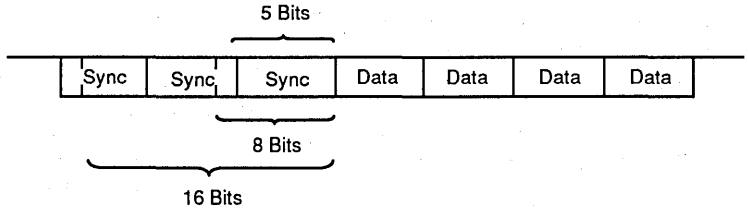


Figure 4. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols, such as IBM BISYNC.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error-checking polynomials are supported. Either polynomial may be selected in BISYNC and MONOSYNC modes. Users may preset the CRC generator and checker to all 1s or all 0s. The ESCC also provides a feature that automatically transmits CRC data when no other data are available for transmission. This allows for high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there are no data or CRC to send in SYNC modes, the transmitter inserts 6-, 8-, or 16-bit SYNC characters, regardless of the programmed character length.

The ESCC supports SYNC bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero-bit insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the ESCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The ESCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to 8 bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{\text{SYNC}}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or 4 bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the ESCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit. pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The ESCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the ESCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The ESCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the ESCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC Loop Mode

The ESCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the ESCC performs the functions of a secondary station while an ESCC operating in regular SDLC mode can act as a controller (Figure 5).

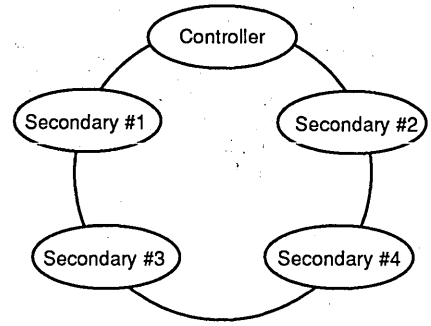


Figure 5. An SDLC Loop

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop and, in fact, must pass these messages to the rest of the loop by retransmitting them with a 1-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations farther down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the ESCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

Baud Rate Generator

Each channel in the ESCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On start-up, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero; the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate where PCLK or $\overline{RTxC}$ is the baud rate generator input frequency in Hz. The clock mode is X1, X16, X32, or X64 as selected in Write Register 4, bits D_6 and D_7. Synchronous operation modes should select X1 and asynchronous should select X16, X32, or X64.

$$\text{Time Constant} = \left[\frac{\text{PCLK or RTxC Frequency}}{2\,(\text{Baud Rate})(\text{Clock Mode})}\right] - 2$$

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds given by Clock Mode/Clock Frequency.)

$$\text{baud rate} = \frac{1}{2\,(\text{Time Constant} + 2) \times (\text{BR Clock Period})}$$

Time Constant Values for Standard Baud Rates at BR Clock = 3.9936 MHz

Rate (Baud)	Time Constant (decimal/Hex notation)		Error
19200	102	(0066)	0
9600	206	(00CE)	0
7200	275	(0113)	0.12%
4800	414	(019E)	0
3600	553	(0229)	0.06%
2400	830	(033E)	0
2000	996	(03E4)	0.04%
1800	1107	(0453)	0.03%
1200	1662	(067E)	0
600	3326	(0CFE)	0
300	6654	(19FE)	0
150	13310	(33FE)	0
134.5	14844	(39FC)	0.0007%
110	18151	(46E7)	0.0015%
75	26622	(67FE)	0
50	39934	(98FE)	0

Digital Phase-Locked Loop

The ESCC contains a digital phase-locked loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). As long as no transitions are detected, the DPLL output will be free running and its input clock source will be divided by 32, producing an output clock without any phase jitter. Upon detecting a transition the DPLL will adjust its clock output (during the next counting cycle) by adding or subtracting a count of 1, thus producing a terminal count closer to the center of the bit cell. The adding or subtracting of a count of 1 will produce a phase jitter of ±5.63° on the output of the DPLL. Because the SCC's DPLL uses both edges of the incoming signal to compare with its clock source, the mark-space ratio (50%) of the incoming signal should not deviate by more than ±1.5% if proper locking is to occur.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the $\overline{RTxC}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{TRxC}$ pin (if this pin is not being used as an input).

Crystal Oscillator

When using a crystal oscillator to supply the receive or transmit clocks to a channel of the SCC, the user should:

1. Select a crystal oscillator that satisfies the following specifications:
   - 30 ppm @ 25°C
   - 50 ppm over temperatures of –20° to 70°C
   - 5 ppm/yr aging
   - 5-MW drive level
2. Place crystal across $\overline{RTxC}$ and $\overline{SYNC}$ pins.
3. Place 30-pF capacitors to ground from both $\overline{RTxC}$ and $\overline{SYNC}$ pins.
4. Set bit D_7 of WR11 to 1.

Data Encoding

The ESCC may be programmed to encode and decode the serial data in four different ways (Figure 6). In NRZ encoding, a 1 is represented by a High level, and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level, and a 0 is represented by a change in level. In FM_1 (more properly, biphase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell, and a 0 is represented by no additional transition at the center of the bit cell. In FM_0 (biphase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the ESCC can be used to decode Manchester (biphase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1, the bit is a 0. If the transition is 1/0, the bit is a 1.

Auto Echo and Local Loopback

The ESCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes but works in SYNC and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the $\overline{CTS}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed, and the programmer is responsible for disabling transmitter interrupts and $\overline{WAIT/REQUEST}$ on transmit.

The ESCC is also capable of Local Loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data, and RxD is ignored (except to be echoed out via TxD). The $\overline{CTS}$ and $\overline{DCD}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, SYNC, and SDLC modes with NRZ, NRZI, or FM coding of the data stream.

I/O Interface Capabilities

The ESCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

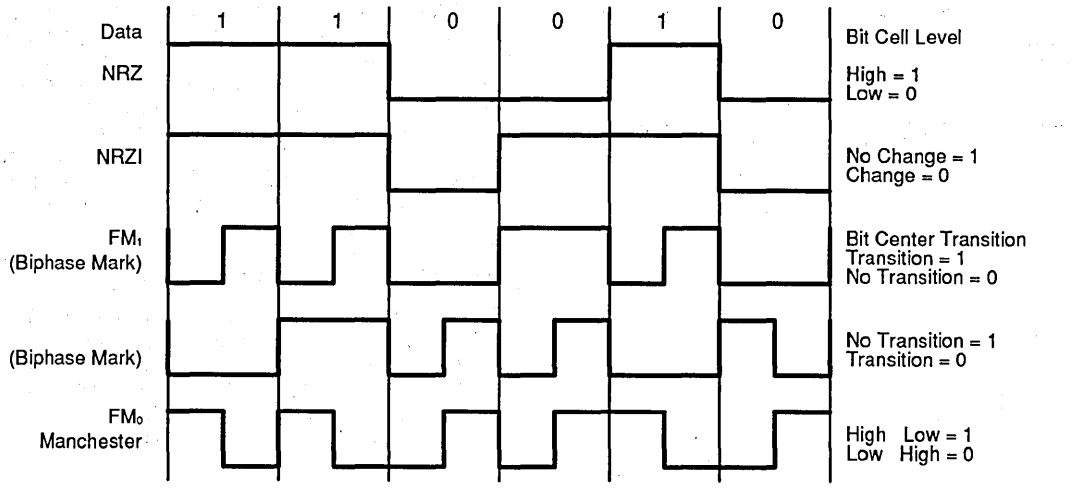


Figure 6. Data Encoding Methods

Polling

All interrupts are disabled. Three status registers in the ESCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

Interrupts

When an ESCC responds to an Interrupt Acknowledge signal (INTACK) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 8 and 9).

To speed interrupt response time, the ESCC can modify 3 bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ESCC (Transmit, Receive, and External/Status interrupts in both channels) has 3 bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

The other 2 bits are related to the Z-Bus interrupt priority chain (Figure 7). As a Z-Bus peripheral, the ESCC may request an interrupt only when no higher priority device is requesting one, for example, when IEI is High. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the A/D bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is set to 1 and the IEI input is High, the $\overline{INT}$ output is pulled Low, requesting an interrupt. In the ESCC, if the IE bit is set for an interrupt, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ESCC and external to the ESCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ESCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive, and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the Receive can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition
- Interrupt on all Receive Characters or Special Receive condition
- Interrupt on Special Receive condition only

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in asynchronous mode, end-of-frame in SDLC mode, and optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary Receive Character Available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive Conditions any time after the first Receive Character Interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins; however, an External/Status interrupt is also

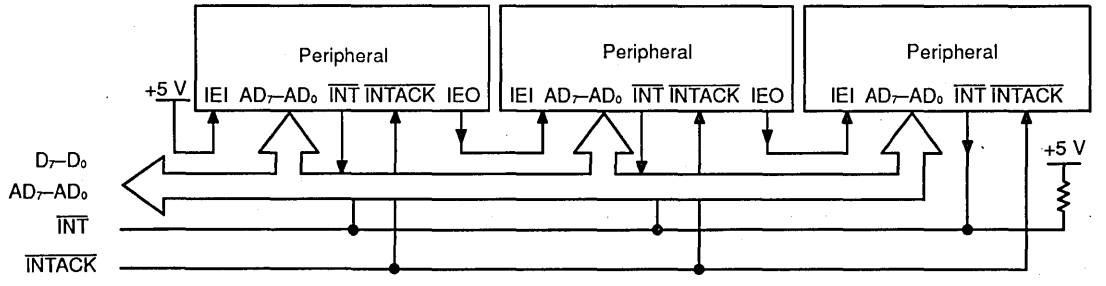


Figure 7. Z-Bus Interrupt Schedule

caused by a Transmit Underrun condition, a zero count in the baud rate generator, the detection of a Break (asynchronous mode), Abort (SDLC mode), or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the ESCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA Block Transfer

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{\text{WAIT/REQUEST}}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{\text{WAIT/REQUEST}}$ output can be defined under software control as a $\overline{\text{WAIT}}$ line in the CPU Block Transfer mode or as a $\overline{\text{REQUEST}}$ line in the DMA Block Transfer mode.

To a DMA controller, the ESCC $\overline{\text{REQUEST}}$ output indicates that the ESCC is ready to transfer data to or from memory. To the CPU, the $\overline{\text{WAIT}}$ line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{\text{DTR/REQUEST}}$ can be used as the transmit request line, thus allowing full-duplex operation under DMA control.

PROGRAMMING INFORMATION

Each channel has fifteen Write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has eight Read registers from which the system can read Status, Baud rate, or Interrupt information.

On the Am85C30, only four data registers (Read and Write for Channels A and B) are directly selected by a High on the D/$\overline{\text{C}}$ input and the appropriate levels on the $\overline{\text{RD}}$, $\overline{\text{WR}}$, and A/$\overline{\text{B}}$ pins. All other registers are addressed indirectly by the content of Write Register 0 in conjunction with a Low on the D/$\overline{\text{C}}$ input and the appropriate levels on the $\overline{\text{RD}}$, $\overline{\text{WR}}$, and A/$\overline{\text{B}}$ pins. If bit D_3 in WR0 is 1 and bits 5 and 6 are 0, then bits 0, 1, and 2 address the higher registers 8 through 15. If bits 4, 5, and 6 contain a different code, bits 0, 1, and 2 address the lower registers 0 through 7 as shown in Table 2.

Writing to or reading from any register except RR0, WR0, and the data registers thus involves two operations:

First, write the appropriate code into WR0, then follow this by a Write or Read operation on the register thus specified. Bits 0 through 4 in WR0 are automatically cleared after this operation, so that WR0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the A/$\overline{\text{B}}$ input (High = A, Low = B).

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set and, finally, receiver or transmitter enable.

Table 2. Register Addressing

D/$\overline{\text{C}}$	"Point High" Code In WR0:	D_2, D_1, D_0 In WR0:			Write Register	Read Register
High	Either Way	X	X	X	Data	Data
Low	Not True	0	0	0	0	0
Low	Not True	0	0	1	1	1
Low	Not True	0	1	0	2	2
Low	Not True	0	1	1	3	3
Low	Not True	1	0	0	4	(0)
Low	Not True	1	0	1	5	(1)
Low	Not True	1	1	0	6	(2)
Low	Not True	1	1	1	7	(3)
Low	True	0	0	0	Data	Data
Low	True	0	0	1	9	–
Low	True	0	1	0	10	10
Low	True	0	1	1	11	(15)
Low	True	1	0	0	12	12
Low	True	1	0	1	13	13
Low	True	1	1	0	14	(10)
Low	True	1	1	1	15	15

Read Registers

The ESCC contains eight Read registers [actually nine, counting the receive buffer (RR8) in each channel]. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). In addition, if bit D_2 of WR15 is set, RR6 and RR7 are available for providing frame status from the 10 × 19 bit Frame Status FIFO. Figure 8 shows the formats for each Read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring, for example, when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

Write Registers

The ESCC contains 15 Write registers (16 counting WR8, the transmit buffer) in each channel. These Write registers are programmed separately to configure the functional "personality" of the channels. Two registers (WR2 and WR9) are shared by the two channels that can be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. In addition, if bit D_0 of WR15 is set, Write Register 7 prime (WR7′) is available for programming additional SDLC/HDLC enhancements. When bit D_0 of WR15 is set, executing a write to WR7 actually writes to WR7′ to further enhance the functional "personality" of each channel. Figure 8 shows the format of each Write register.

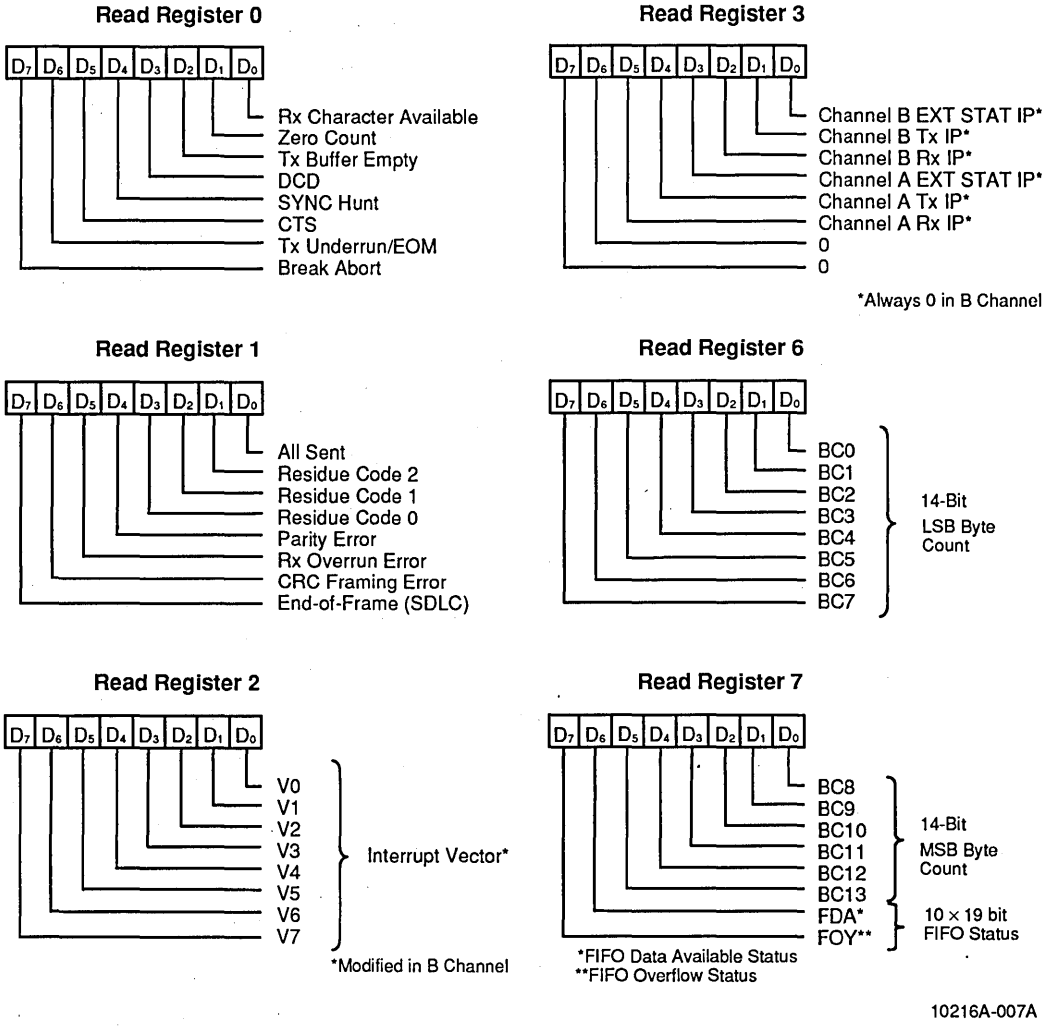


Figure 8. Read Register Bit Functions

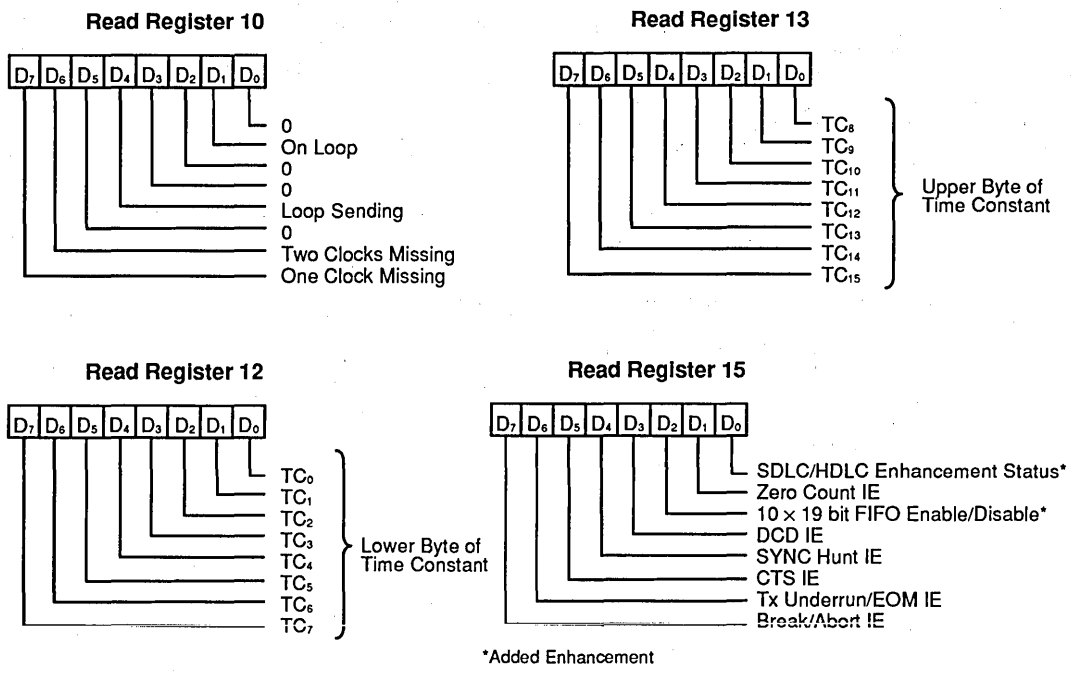


Figure 8. Read Register Bit Functions (continued)

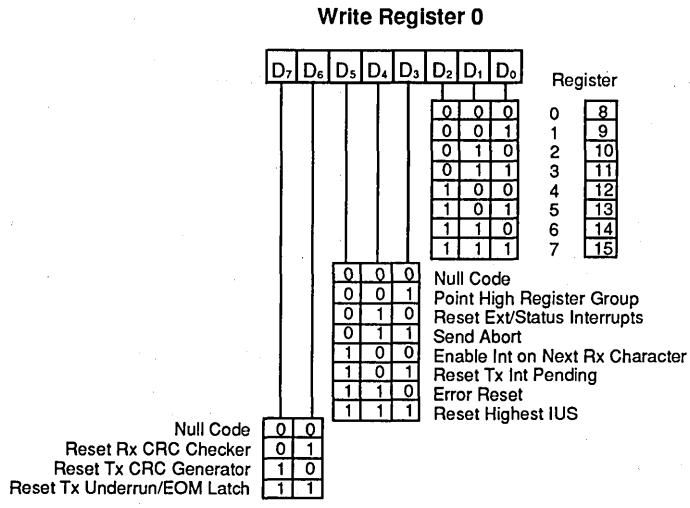


Figure 9. Write Register Bit Functions

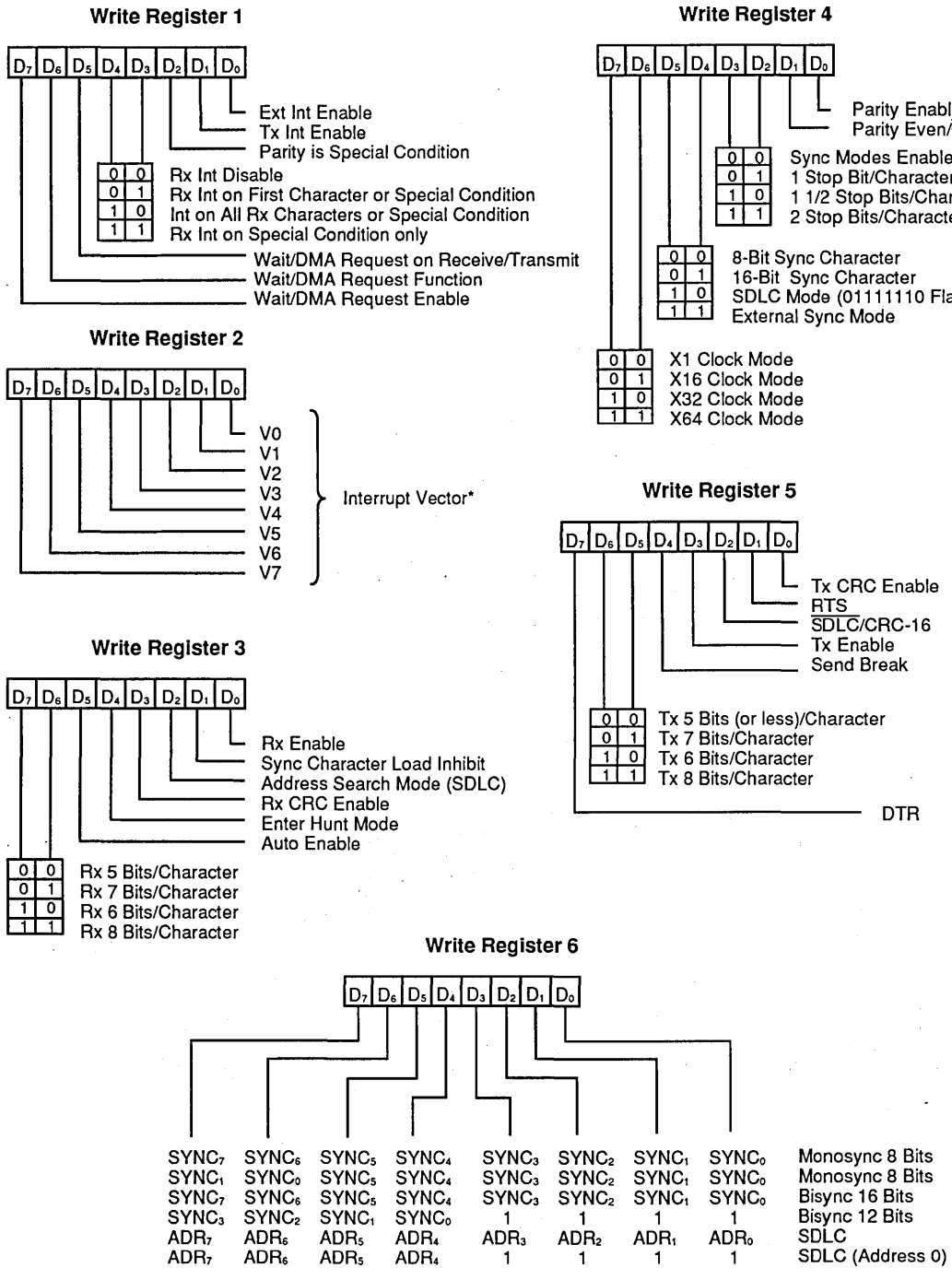
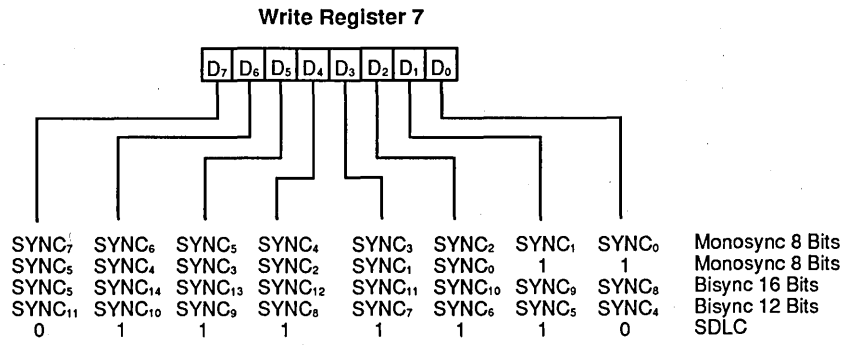
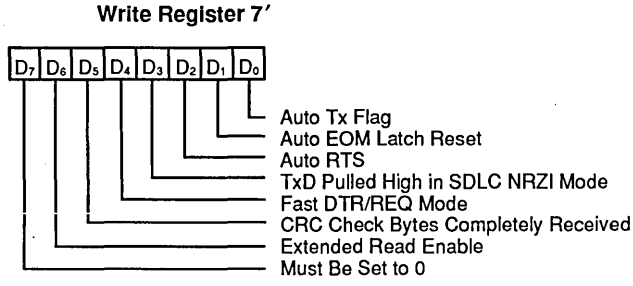
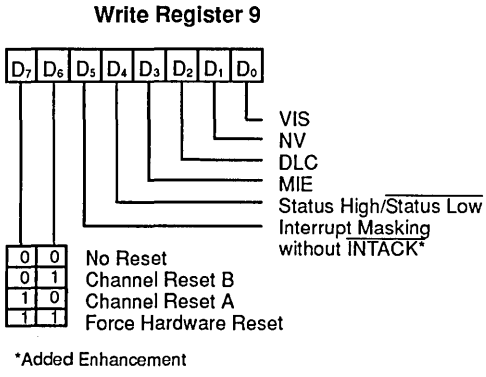


Figure 9. Write Register Bit Functions (continued)







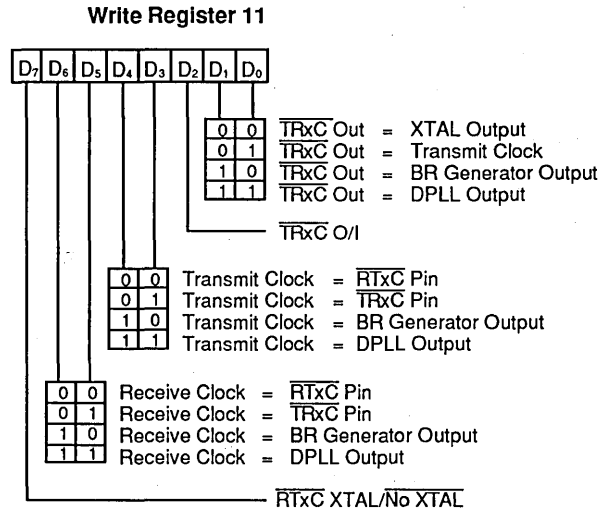


Figure 9. Write Register Bit Functions (continued)

10216A-008A

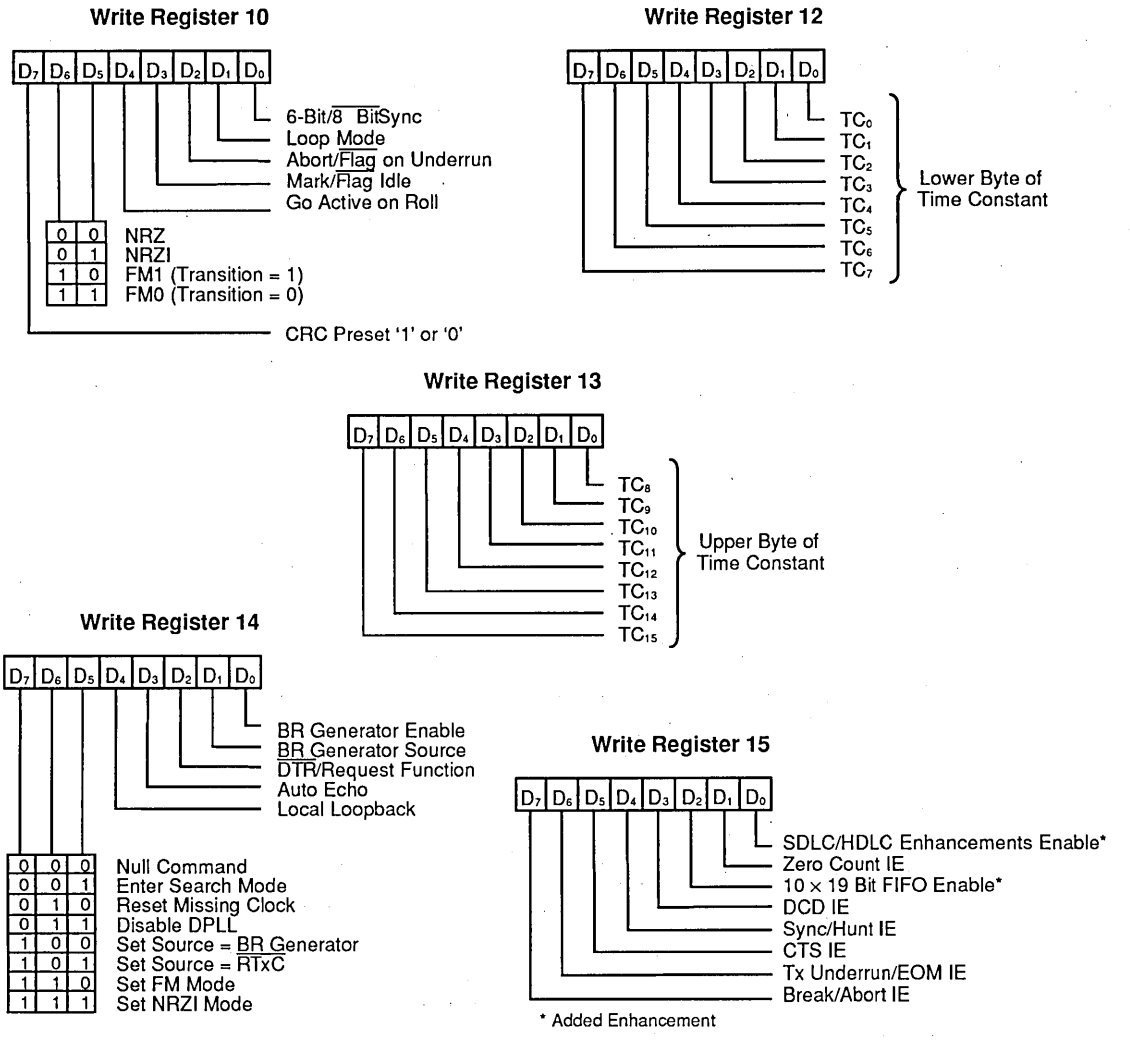


Figure 9. Write Register Bit Functions (continued)

Am85C30 Timing

The ESCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ESCC. The recovery time required for proper operation is specified from the falling edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the ESCC, to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the ESCC. This time must be at least 3 1/2 PCLK regardless of which register or channel is being accessed.

Read Cycle Timing

Figure 10 illustrates Read cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

Write Cycle Timing

Figure 11 illustrates Write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened. Data must be valid before the rising edge of $\overline{WR}$.

Interrupt Acknowledge Cycle Timing

NO TAG illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{INTACK}$ goes Low and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ESCC and IEI is High when $\overline{RD}$ falls, the Acknowledge cycle is intended for the SCC. In this case, the ESCC may be programmed to respond to $\overline{RD}$ Low by placing its interrupt vector on D_7–D_0 ; it then sets the appropriate Interrupt-Under-Ser-vice latch internally.

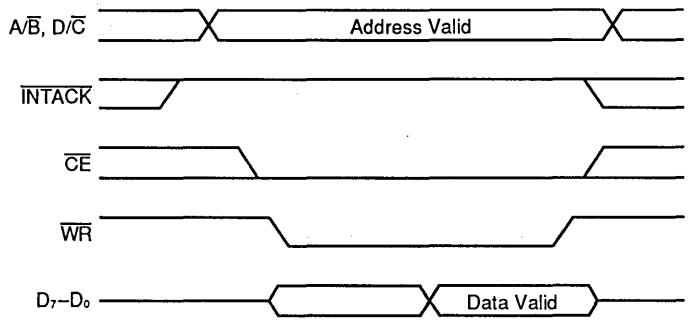


Figure 10. Read Cycle Timing

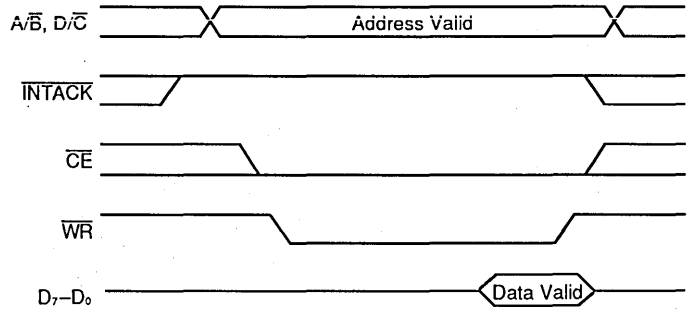


Figure 11. Write Cycle Timing

10216A-010A

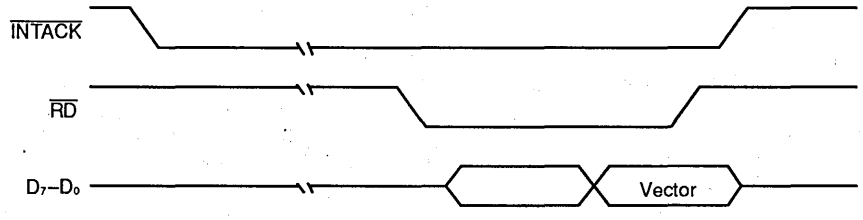


Figure 12. Interrupt Acknowledge Cycle Timing

FIFO

FIFO Enhancements

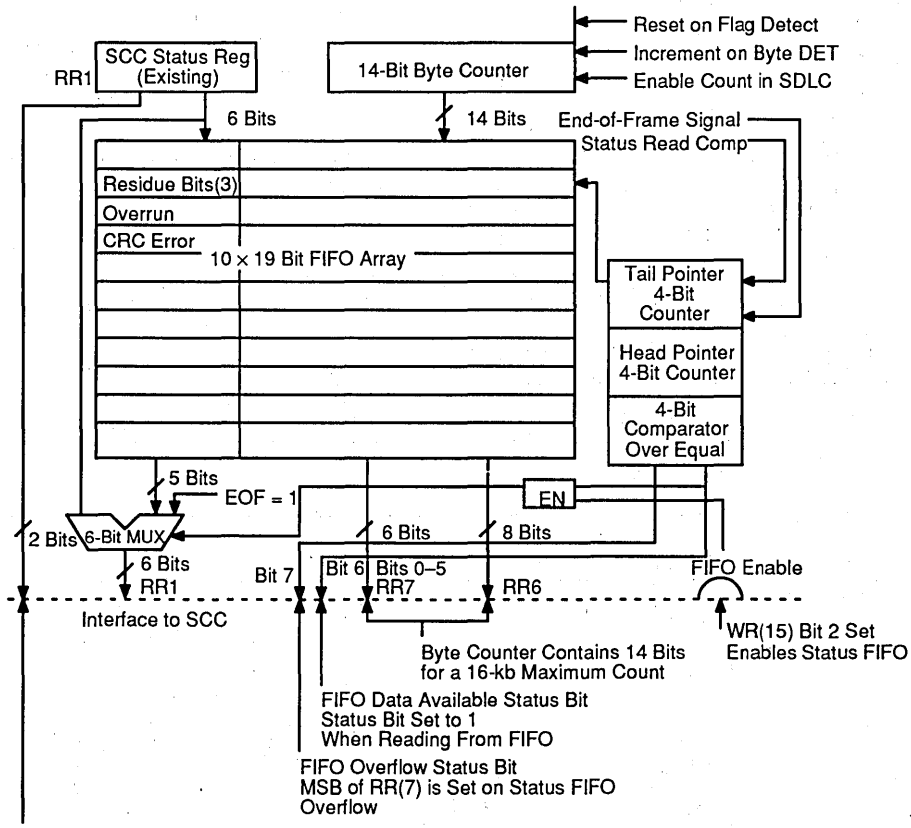
When used with a DMA controller, the Am85C30 Frame Status FIFO enhancement maximizes the ESCC's ability to receive high-speed back-to-back SDLC messages while minimizing frame overruns due to CPU latencies in responding to interrupts.

Additional logic was added to the industry-standard NMOS SCC consisting of a 10-deep by 19-bit status FIFO, a 14-bit receive byte counter, and control logic as shown in Figure 13. The 10 × 19 bit status FIFO is separate from the existing 3-byte receive data and error FIFOs.

When the enhancement is enabled, the status in Read Register 1 (RR1) and byte count for the SDLC frame will be stored in the 10 × 19 bit status FIFO. This allows the DMA controller to transfer the next frame into memory while the CPU verifies that the message was properly received.

Summarizing the operation, data is received, assembled, and loaded into the 3-byte receive FIFO before being transferred to memory by the DMA controller. When a flag is received at the end of an SDLC frame, the frame byte count from the 14-bit counter and 5 status bits are loaded into the status FIFO for verification by the CPU. The CRC checker is automatically reset in preparation for the next frame, which can begin immediately. Since the byte count and status are saved for each frame, the message integrity can be verified at a later time. Status information for up to 10 frames can be stored before a status FIFO overrun could occur.

If receive interrupts are enabled while the 10 × 19 FIFO is enabled, an SDLC end-of-frame special condition will not lock the 3-byte receive data FIFO. An SDLC end-of-frame still locks the 3-byte receive data FIFO in "Interrupt on first Receive Character or Special Condition" and "Interrupt on Special Condition Only" modes when the 10 × 19 FIFO is disabled. This feature allows



In SDLC mode, the following definitions apply:
- All Sent bypasses MUX and equals contents of SCC Status Register.
- Parity bits bypass MUX and do the same.
- EOF is set to 1 whenever reading from the FIFO.

Figure 13. SCC Status Register Modifications 10216A-011A

the 10×19 SDLC FIFO to accept multiple SDLC frames without CPU intervention at the end of each frame.

FIFO Detail

For a better understanding of details of the FIFO operation, refer to the block diagram contained in NO TAG.

Enable/Disable

This FIFO is implemented so that it is enabled when WR15 bit 2 is set and the ESCC is in the SDLC/HDLC mode, otherwise the status register contents bypass the FIFO and go directly to the bus interface (the FIFO pointer logic is reset either when disabled or via a channel or power-on reset). When the FIFO mode is disabled, the ESCC is completely downward-compatible with the NMOS Am8530. The FIFO mode is disabled on power-up (WR15 bit 2 is set to 0 on reset). The effects of backward compatibility on the register set are that RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2, and RR7 is an image of RR3. For the details of the added registers, refer to Figure 15. The status of the FIFO Enable signal can be obtained by reading RR15 bit 2. If the FIFO is enabled, the bit will be set to 1; otherwise, it will be reset.

Read Operation

When WR15 bit 2 is set and the FIFO is not empty, the next read to status register RR1 or the additional registers RR7 and RR6 will actually be from the FIFO. Reading status register RR1 causes one location of the FIFO to be emptied, so status should be read after reading the byte count, otherwise the count will be incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to be read directly from the status register, and reads from RR7 and RR6 will contain bits that are undefined. Bit 6 of RR7 (FIFO Data Available) can be used to determine if status data is coming from the FIFO or directly from the status register, since it is set to 1 whenever the FIFO is not empty.

Because not all status bits are stored in the FIFO, the All Sent, Parity, and EOF bits will bypass the FIFO. The status bits sent through the FIFO will be Residue Bits (3), Overrun, and CRC Error.

The sequence for proper operation of the byte count and FIFO logic is to read the registers in the following order, RR7, RR6, and RR1 (reading RR6 is optional). Additional logic prevents the FIFO from being emptied by multiple reads from RR1. The read from RR7 latches the FIFO empty/full status bit (bit 6) and steers the status multiplexer to read from the SCC megacell instead of the status FIFO (since the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO was empty, logic is added to prevent a FIFO underflow condition).

Write Operation

When the end of an SDLC frame (EOF) has been received and the FIFO is enabled, the contents of the status and byte-count registers are loaded into the FIFO. The EOF signal is used to increment the FIFO. If the FIFO overflows, the MSB of RR7 (FIFO Overflow) is set to indicate the overflow. This bit and the FIFO control logic are reset by disabling and reenabling the FIFO control bit (WR15 bit 2). For details of FIFO control timing during an SDLC frame, refer to Figure 14.

Byte Counter Detail

The 14-bit byte counter allows for packets up to 16K bytes to be received. For a better understanding of its operation, refer to Figures 13 and 14.

Enable

The byte counter is enabled when the SCC is in the SDLC/HDLC mode and WR15 bit 2 is set to 1.

Reset

The byte counter is reset whenever an SDLC flag character is received. The reset is timed so that the contents of the byte counter are successfully written into the FIFO.

Increment

The byte counter is incremented by writes to the data FIFO. The counter represents the number of bytes received by the SCC, rather than the number of bytes transferred from the SCC. (These counts may differ by

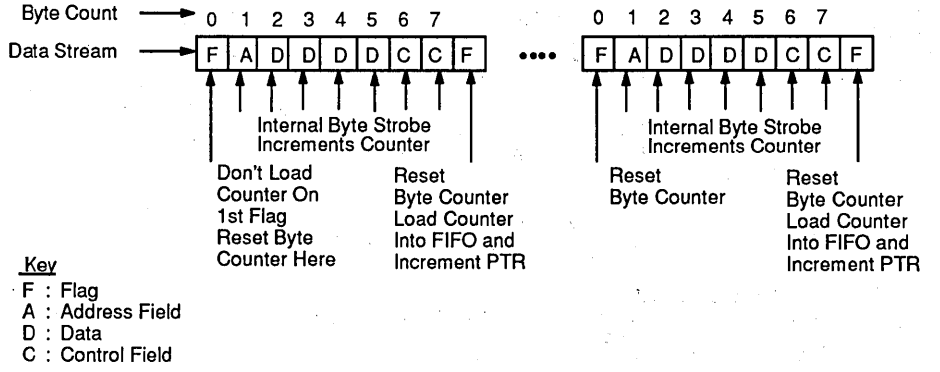
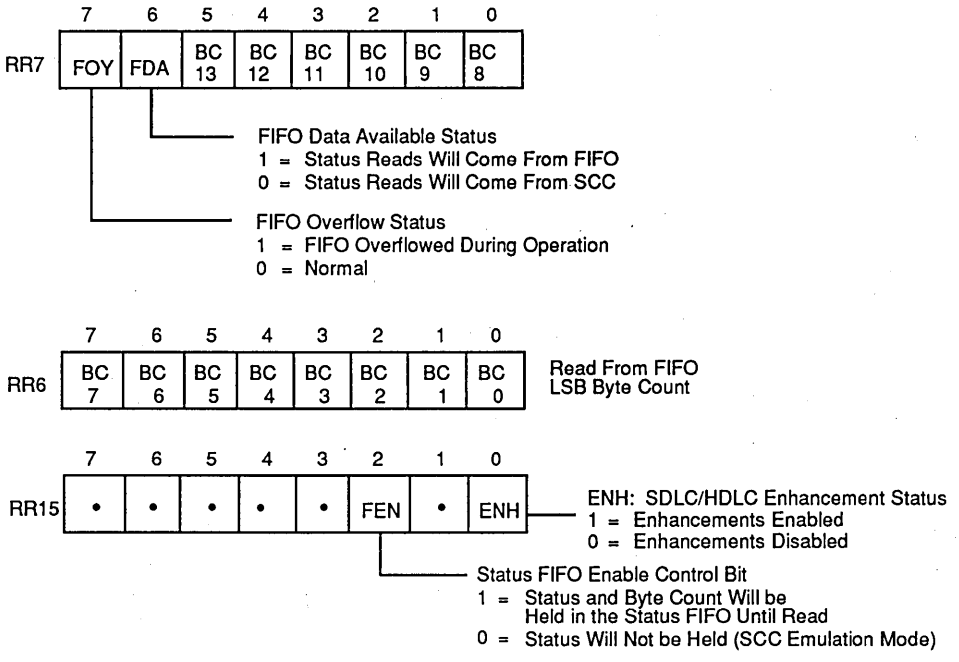


Figure 14. SDLC Byte Counting Detail



• = No Change From NMOS SCC DFN

10216A-013A

Figure 15. SCC Additional Registers

up to the number of bytes in the receive data FIFO contained in the SCC.)

Am85C30 SDLC/HDLC Enhancement Register Access

SDLC/HDLC enhancements on the Am85C30 are enabled or disabled via bits D_2 or D_0 in WR15. Bit D_2 determines whether or not the 10 × 19 bit SDLC/HDLC frame status FIFO is enabled while bit D_0 determines whether or not other enhancements are enabled via WR7′. Table 3 shows what functions on the Am85C30 are enabled when these bits are set.

When bit D_2 of WR15 is set to 1, two additional registers (RR6 and RR7) per channel specific to the 10 × 19 bit Frame Status FIFO are made available. The Am85C30

Table 3. Enhancement Options

WR15 Bit D_2 10 × 19 Bit FIFO Enabled	WR15 Bit D_0 SDLC/HDLC Enhancement Enabled	WR7′ Bit D_6 Extended Read Enabled	Functions Enabled
1	0	x	10 × 19 bit FIFO enhancement enabled only
0	1	0	SDLC/HDLC enhancements enabled only
0	1	1	SDLC/HDLC enhancements enabled with extended read enabled
1	1	0	10 × 19 bit FIFO and SDLC/HDLC enhancements enabled
1	1	1	10 × 19 bit FIFO and SDLC/HDLC enhancements with extended read enabled

register map when this function is enabled is shown in Table 4.

Bit D_0 of WR15 determines whether or not other enhancements pertinent only to SDLC/HDLC mode operation are available for programming via WR7′ as shown below. Write Register 7 prime (WR7′) can be written to when bit D_0 of WR15 is set to 1. When this bit is set, writing to WR7 (flag register) actually writes to WR7′. If bit D_6 of this register is set to 1, previously unreadable registers WR3, WR4, WR5, and WR10 are readable by the processor. In addition, WR7′ is also readable by having this bit set. WR3 is read when a bogus RR9 register is accessed during a read cycle. WR10 is read by accessing RR11, and WR7′ is accessed by executing a read to RR14. The Am85C30 register map with bit D_0 of WR15 and bit D_6 of WR7′ set is shown in Table 5.

If both bits D_0 and D_2 of WR15 are set to 1 and D_6 of WR7′ is set to 1, then the Am85C30 register map is as shown in Table 6.

Auto RTS Reset

On the CMOS ESCC, if bit D_0 of WR15 and bit D_2 of WR7′ are set to 1 and the channel is in SDLC mode, the $\overline{RTS}$ pin may be reset early in the Tx Underrun routine and the $\overline{RTS}$ pin will remain active until the last 0 bit of the closing flag leaves the TxD pin as shown in Figure 16. Note that

Table 4. 10×19 Bit FIFO Enabled

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	(RR0B)
0	1	0	1	WR5B	(RR1B)
0	1	1	0	WR6B	RR6B
0	1	1	1	WR7B	RR7B
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	(RR0A)
1	1	0	1	WR5A	(RR1A)
1	1	1	0	WR6A	RR6A
1	1	1	1	WR7A	RR7A
				With the Point High command:	
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR13B
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	(RR15B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	(RR10B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	(RR13A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	(RR15A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	(RR10A)
1	1	1	1	WR15A	RR15A

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Must Be Set to 0	Ext. Read Enable	Rx comp. CRC	$\overline{DTR/REQ}$ Fast Mode	Force TxD High	SDLC/HDLC Auto $\overline{RTS}$ Turnoff	SDLC/HDLC Auto EOM Reset	SDLC/HDLC Auto Tx Flag

WR7′—SDLC/HDLC Programmable Enhancements*

*Note: Options 3, 4, 5, and 6 may be used regardless of whether SDLC/HDLC mode is selected.

Table 5. SDLC/HDLC Enhancements Enabled

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	RR4B (WR4B)
0	1	0	1	WR5B	RR5B (WR5B)
0	1	1	0	WR6B	(RR2B)
0	1	1	1	WR7B	(RR3B)
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	RR4A (WR4A)
1	1	0	1	WR5A	RR5A (WR5A)
1	1	1	0	WR6A	(RR2A)
1	1	1	1	WR7A	(RR3A)
				With the Point High command:	
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR9 (WR3B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	RR11B (WR10B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	RR14B (WR7'B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	RR9A (WR3A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	RR11A (WR10A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	RR14A (WR7A)
1	1	1	1	WR15A	RR15A

in order for this to function properly, bits D_3 and D_2 of WR10 must be set to 1 and 0, respectively.

CRC Character Reception

NMOS Am8530H

On the NMOS Am8530H, when the end-of-frame flag is detected, the contents of the Receive Shift Register are transferred to the Receive Data FIFO regardless of the number of bits accumulated. Because of the 3-bit delay between the Receive SYNC Register and Receive Shift Register, the last 2 bits of the CRC check character received are never transferred to the Receive Data FIFO. Thus, the received CRC characters are unavailable for use.

CMOS Am85C30

On the Am85C30, the option of being able to receive the complete CRC characters generated by the transmitter is provided when both bit D_0 of WR15 and bit D_5 of WR7′ are set to 1. When these 2 bits are set and an end-of-frame flag is detected, the last 2 bits of the CRC will be clocked into the Receive Shift Register before its contents are transferred to the Receive Data FIFO. The data-CRC boundary and CRC character bit formats for each Residue Code provided are shown in Figures 17A through 17D for each character length selected.

Table 6. SDLC/HDLC Enhancements and 10×19 Bit FIFO Enabled

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	RR4B (WR4B)
0	1	0	1	WR5B	RR5B (WR5B)
0	1	1	0	WR6B	RR6B
0	1	1	1	WR7B	RR7B
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	RR4A (WR4A)
1	1	0	1	WR5A	RR5A (WR5A)
1	1	1	0	WR6A	RR6A
1	1	1	1	WR7A	RR7A
				With the Point High command:	
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR9 (WR3B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	RR11B (WR10B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	RR14B (WR7'B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	RR9A (WR3A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	RR11A (WR10A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	RR14A (WR7'A)
1	1	1	1	WR15A	RR15A

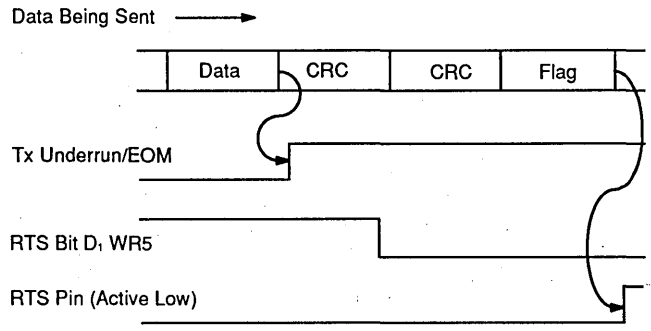


Figure 16. Auto $\overline{RTS}$ Reset Mode

Residue Code 012 = 001

D	D	D	D	D	C_0	C_1	C_2
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 101

D	D	D	D	D	D	C_0	C_1
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 100

D	D	D	D	D	D	D	C_0
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 010

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 110

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Figure 17A. 5 Bits/Character

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Residue Code 012 010

D	D	D	D	D	D	C_0	C_1
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 110

D	D	D	D	D	D	D	C_0
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 001

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 101

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 011

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 100

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Figure 17B. 6 Bits/Character

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Residue Code 012/111

D	D	D	D	D	D	D	C_0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/100

D	D	D	D	D	D	D	D
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/010

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/110

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/001

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/101

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/011

D	D	D	D	D	D	D	D
D	D	D	D	D	D	C_0	C_1
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Figure 17C. 7 Bits/Character

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Residue Code 012 = 011

(No Residue)

D	D	D	D	D	D	D	D
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 111

(1 Residue Bit)

D	D	D	D	D	D	D	D
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 000

(2 Residue Bits)

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 100

(3 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 010

(4 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 110

(5 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 001

(6 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	D	C_0	C_1
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 = 101

(7 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	C_0
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Figure 17D. 8 Bits/Character

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Auto Flag Mode

On the NMOS Am8530H, if the transmitter is actively mark idling and a frame of data is ready to be transmitted, the Mark/Flag Idle bit must be set to 0 before data is written to WR8, otherwise the opening flag will not be sent properly. However, care must be exercised in doing this because the mark idle pattern (eight 1 bits) is transmitted 8 bits at a time, and all 8 bits must have transferred out of the Transmit Shift Register before a flag may be loaded and sent. If data is written into the Transmit Buffer (WR8) before the flag is loaded into the Transmit Shift Register, the data character written to WR8 will supersede flag transmission and the opening flag will not be transmitted.

On the CMOS Am85C30, if bit D_0 of WR15 is set to 1 and the ESCC is programmed for SDLC operation, an option is provided via bit D_0 of WR7′ that eliminates this requirement. If bit D_0 of WR7′ is set to 1 and a character is written to the Transmit Buffer while the transmitter is mark idling, the Mark/Flag Idle bit in WR10 need not be reset to 0 in order to have the opening flag sent because the transmitter will automatically send it before commencing to send data.

In addition, as long as bit D_0 of WR15 and bit D_1 of WR7′ are set to 1, the CRC transmit generator will be automatically preset to the initial state programmed by bit D_7 of WR10 (so the Reset Tx CRC Generator command is also not necessary), and the Tx Underrun/EOM latch will be reset automatically on every new frame sent. This ensures that an opening flag and proper CRC generation and transmission will always be sent without processor intervention under varying bus latency conditions.

Auto Transmit CRC Generator Preset

The NMOS Am8530H does not automatically preset the CRC generator prior to frame transmission. This must be done in software, usually during the initialization routine. This is accomplished by issuing the Reset Tx CRC Generator Command via WR0. For proper results, this command must be issued while the transmitter is enabled and idling and before any data are written to the Transmit Buffer.

In addition, if CRC is to be used, the transmit CRC generator must be enabled by setting bit D_0 of WR5 to 1. CRC is normally calculated on all characters between opening and closing flags, so this bit should be set to 1 at initialization and never changed.

On the CMOS Am85C30, setting bit D_0 of WR15 to 1 will cause the transmit CRC generator to be preset automatically every time an opening flag is sent, so the Reset Tx CRC Generator Command is not necessary.

Auto Tx Underrun/EOM Latch Reset

On the ESCC, the transmission of the CRC check characters is controlled by the Transmit CRC Enable bit in WR5 (D_0) and the Tx Underrun/EOM bit in RR0 (D_6). However, if the Transmit Enable bit is set to 0 when a transmit underrun (i.e., both the Transmit Buffer and Transmit Shift Register become empty) occurs, the CRC check characters will not be sent regardless of the state of the Tx Underrun/EOM bit.

If the Transmit Enable bit is set to 1 when an underrun occurs, then the state of the Tx Underrun/EOM bit and the Abort/Flag on Underrun bit in WR10 (D_2) determine the action taken by the transmitter. The Abort/Flag on Underrun bit may be set or reset by the processor, whereas the Tx Underrun/EOM bit is set by the transmitter and can only be reset by the processor via the Reset Tx Underrun/EOM Command in WR0.

If the Tx Underrun/EOM bit is set to 1 when an underrun occurs, the transmitter will close the frame by sending a flag; however, if this bit is set to 0, the frame data will be appended with either the accumulated CRC characters followed by a flag or an abort pattern followed by a flag, depending on the state of the Abort/Flag on Underrun bit in the WR10 (D_2). In either case, after the closing flag is sent, the transmitter will idle the transmission line as specified by the Mark/Flag Idle bit D_3 in WR10.

Hence, if the CRC check characters are to be properly appended to a frame, the Abort/Flag on Underrun bit must be set to 0, and the Reset Tx Underrun/EOM Command must be issued after the first but before the last character is written to the Transmit Buffer. This will ensure that either an abort or the CRC will be transmitted if an underrun occurs. Normally, the Abort/Flag on Underrun bit in WR10 should be set to 1 around the same time that the Tx Underrun/EOM bit is reset so that an abort will be sent if the transmitter accidentally underruns, and then set to 0 near the end of the frame to allow the correct transmission of CRC.

On the Am85C30, if bit D_0 of WR15 is set to 1, the option of having the Tx Underrun/EOM bit reset automatically at the start of every frame is provided via bit D_1 of WR7′. This helps alleviate the software burden of having to respond within one character time when high-speed data are being sent.

SDLC/HDLC NRZI Transmitter Disabling

On the NMOS Am8530H, if NRZI encoding is being used and the transmitter is disabled, the state of the TxD pin will depend on the last bit sent. That is, the TxD pin may either idle in a Low or High state as shown in Figure 18.

On the CMOS Am85C30, an option is provided that allows setting the TxD pin High when operating in SDLC mode with NRZI encoding enabled. If bit D_0 of WR15 is set to 1, then bit D_3 of WR7′ can be used to set the TxD pin High. Note that the operation of this bit is independent of the Tx Enable bit in WR5. The Tx Enable bit in WR5 is used to disable and enable the transmitter, whereas bit D_3 of WR7′ acts as a pseudo transmitter disable and enable by just forcing the TxD pin High when set even though the transmitter may actually be mark or flag idling. Care must be used when setting this bit because any character being transmitted at the time this bit is set will be "chopped off," and data written to the Transmit Buffer while this bit is set will be lost.

When the transmit underrun occurs and the CRC and closing flag have been sent, bit D_3 can be set to pull TxD High. When ready to start sending data again this bit must be reset to 0 before the first character is written to the Transmit Buffer. Note that resetting this bit causes the TxD pin to take whatever state the NRZI encoder is in at the time, so synchronization at the receiver may take longer because the first transition seen on the TxD pin may not coincide with a bit boundary. Note that in order

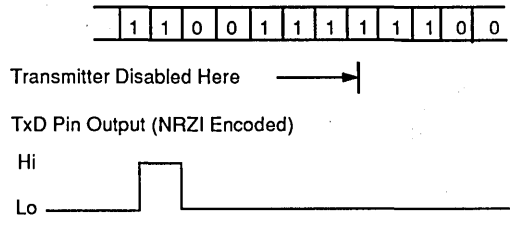


Figure 18. Transmitter Disabling with NRZI Encoding 10216A-019A

for this to function properly, bits D_3 and D_2 of WR10 must be set to 1 and 0, respectively.

Interrupt Masking Without $\overline{\text{INTACK}}$

The NMOS Am8530H's ability to mask lower priority interrupts is done via the IUS bit. This bit is internal to the SCC and is not observable by the processor. Being able to automatically mask lower priority interrupts allows a modular approach to coding interrupt routines. However, using the masking capabilities of the NMOS SCC requires that the $\overline{\text{INTACK}}$ cycle be generated. In standalone applications, having to generate $\overline{\text{INTACK}}$ through external hardware in order to use this capability is an unnecessary expense.

On the CMOS Am85C30, if bit D_5 in WR9 is set to 1, the $\overline{\text{INTACK}}$ cycle does not need to be generated in order to have the IUS bit set. This allows the user to respond to ESCC interrupt requests with a software acknowledgment through RR2. When bit D_5 in WR9 is set and an interrupt occurs, a read to RR2 emulates a hardware Interrupt Acknowledge cycle as it functions in Vectored mode. In this case the CPU must first read RR2 to determine the internal interrupt source and then jump to the appropriate interrupt routine. Reading RR2 sets the IUS bit for the highest priority IP. After the interrupting condition is cleared, the routine can then read RR3 to determine if any other IPs are set and clear them. At the end of the interrupt routine, a Reset IUS command must be issued to unlock the internal daisy chain.

Since the CPU can acknowledge the ESCC of highest priority with a read of its RR2 interrupt vector, there is no need for an external daisy chain. IEI for all ESCC devices should be tied active High. When acknowledging an ESCC interrupt request, the CPU must issue one read to RR2 per interrupt request. The modified interrupt vector can be read from Channel B, or the original vector stored in WR2 can be read from Channel A. Either action will produce the same internal actions on the IUS logic. Note that the No Vector and Vector Includes Status bits in WR9 are ignored when bit D_5 in WR9 is set to 1.

2-Mb/s FM Data Transmission and Reception

The 16-MHz version of the CMOS Am85C30 (Am85C30-16) is capable of transmitting and receiving FM-encoded data at the rate of 2 Mb/s. This is accomplished by applying a 32-MHz clock to the $\overline{\text{RTxC}}$ pin and assigning this waveform to drive the Internal Digital Phase-Locked Loop (DPLL) clock. This feature allows the user to send both clock and data information over the same line at 2 Mb/s and can eliminate external DPLLs required for high-speed NRZ data clock generation.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Voltage at any Pin	
Relative to V_{SS}	−0.5 to +7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+5 V ± 10%
Industrial (I) Devices	
Ambient Temperature (T_A)	−40 to +85°C
Supply Voltage (V_{CC})	5 V ±10%
Military (M) Devices	
Case Temperature (T_C)	−55° to 125°
Supply Voltage (V_{CC})	5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IH}	Input High Voltage	Commercial	2.2	V_{CC} +0.3*	V
V_{IL}	Input Low Voltage		−0.3*	0.8	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	2.4		V
V_{OH2}	Output High Voltage	I_{OH} = −250 µA	V_{CC} −0.8		V
V_{OL}	Output Low Voltage	I_{OL} = +2.0 mA		0.4	V
I_{IL}	Input Leakage	0.4 V ≤ V_{IN} ≤ 2.4 V		±10.0	µA
I_{OL}	Output Leakage	0.4 V ≤ V_{OUT} ≤ 2.4 V		±10.0	µA
I_{CC1}	V_{CC} Supply Current	8.192 MHz		18	mA
		10 MHz Inputs at		18	mA
		12 MHz voltage rails,		22	mA
		16.384 MHz output unloaded		22	mA
		20 MHz		30	mA
C_{IN}	Input Capacitance	Unmeasured pins returned		10	pF
C_{OUT}	Output Capacitance	to ground = 1 MHz over		15	pF
C_{MO}	Bidirectional Capacitance	specified temperature range		20	pF

*V_{IH} Max and V_{IL} Min not tested. Guaranteed by design.

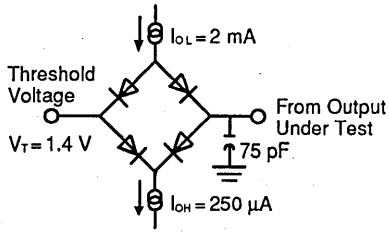
Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

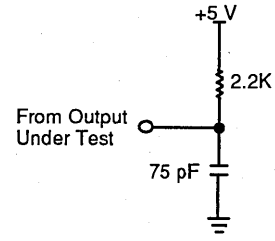
+4.5 V ≤ V_{CC} ≤ +5.5 V
GND = 0 V
0°C ≤ T_A ≤ 70°C

SWITCHING TEST CIRCUITS

Standard Test Dynamic Load Circuit



Open-Drain Test Load



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SWITCHING CHARACTERISTICS over COMMERCIAL operating range

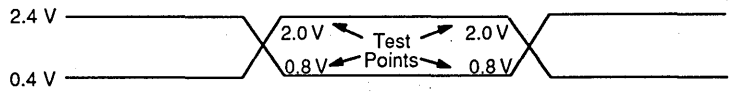
General Timing (see Figure 19)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TdPC(REQ)	PCLK ↓ to $\overline{W/REQ}$ Valid Delay		250		150		80	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		250		180	ns
3	TsRXC(PC)	$\overline{RxC}$ ↑ to PCLK ↑ Setup Time (Notes 1, 4 & 8)	NA	NA	NA	NA	NA	NA	
4	TsRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Setup Time (XI Mode) (Note 1)	0		0		0		ns
5	ThRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Hold Time (XI Mode) (Note 1)	150		125		50		ns
6	TsRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		0		ns
7	ThRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Hold Time (XI Mode) (Notes 1, 5)	150		125		50		ns
8	TsSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Setup Time (Note 1)	–200		–150		–100		ns
9	ThSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Hold Time (Note 1)	5TcPC		5TcPC		5TcPc		ns
10	TsTXC(PC)	$\overline{TxC}$ ↓ to PCLK ↑ Setup Time (Notes 2, 4 & 8)	NA		NA		NA		
11	TdTXCf(TXD)	$\overline{TxC}$ ↓ to TxD Delay (XI Mode) (Note 2)		200		150		80	ns
12	TdTXCr(TXD)	$\overline{TxC}$ ↑ to TxD Delay (XI Mode) (Notes 2, 5)		200		150		80	ns
13	TdTXD(TRX)	TxD to $\overline{TRxC}$ Delay (Send Clock Echo)		200		140		80	ns
14a	TwRTXh	$\overline{RTxC}$ High Width (Note 6)	150		120		80		ns
14b	TwRTxh(E)	$\overline{RTxC}$ High Width (Note 9)	50		40		15.6		ns
15a	TwRTXl	$\overline{RTxC}$ Low Width (Note 6)	150		120		80		ns
15b	TwRTXl(E)	$\overline{RTxC}$ Low Width (Note 9)	50		40		15.6		ns
16a	TcRTX	$\overline{RTxC}$ Cycle Time (Notes 6, 7)	488		400		244		ns
16b	TcRTx(E)	$\overline{RTxC}$ Cycle Time (Note 9)	125		100		31.25		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	125	1000	100	1000	62	1000	ns
18	TwTRXh	$\overline{TRxC}$ High Width (Note 6)	150		120		80		ns
19	TwTRXl	$\overline{TRxC}$ Low Width (Note 6)	150		120		80		ns
20	TcTRX	$\overline{TRxC}$ Cycle Time (Notes 6, 7)	488		400		244		ns
21	TwEXT	$\overline{DCD}$ or $\overline{CTS}$ Pulse Width	200		120		70		ns
22	TwSY	$\overline{SYNC}$ Pulse Width	200		120		70		ns

Notes:

1. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
3. Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30-pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and PCLK or $\overline{TxC}$ and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.
8. External PCLK to $\overline{RxC}$ or $\overline{TxC}$ synchronization requirement eliminated for PCLK divide-by-four operation.
   $\overline{TRxC}$ and $\overline{RTxC}$ rise and fall times are identical to PCLK. Reference timing specs Tfpc and Trpc.
   Tx and Rx input clock slow rates should be kept to a maximum of 30 ns. All parameters related to input CLK edges should be referenced at the point at which the transition begins or ends, whichever is the worst case.
9. ENHANCED FEATURE—$\overline{RTxC}$ used as input to internal DPLL only.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



AC testing: Inputs are driven at 2.4 V for a logic 1 and 0.4 V for a logic 0.
Timing measurements are made at 2.0 V for a logic 1 and 0.8 V for logic 0.

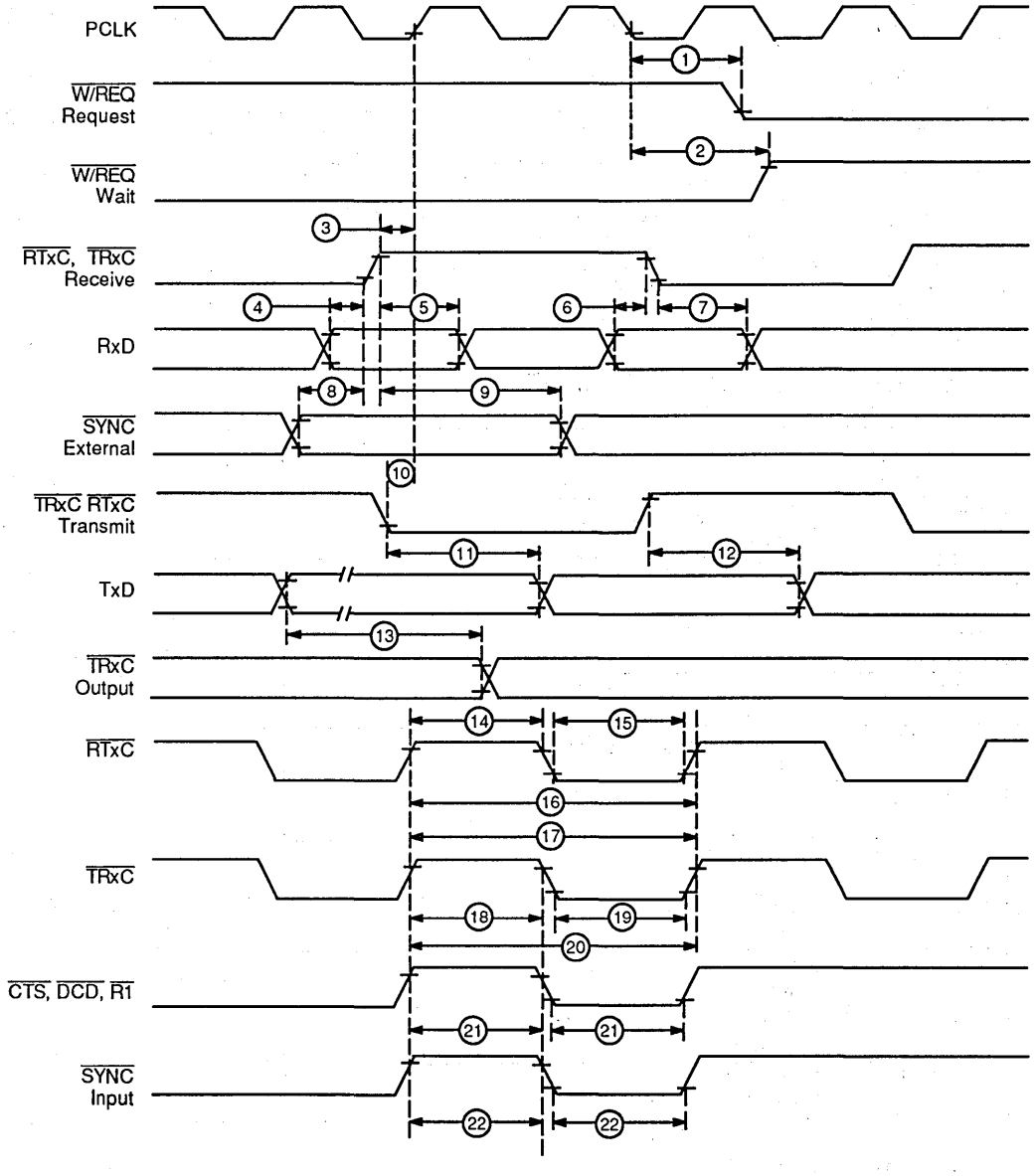


Figure 19. General Timing

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

System Timing (see Figure 20)

No.	Parameter Symbol	Parameter Description	8.192 MHz Min.	8.192 MHz Max.	10 MHz Min.	10 MHz Max.	Unit
1	TdRXC(REQ)	$\overline{RXC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	TcPc
2	TdRXC(W)	$\overline{RXC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	8	14	TcPc
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	4	7	TcPc
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPc
5	TdTXC(REQ)	$\overline{TxC}$ ↑ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	TcPc
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Notes 3, 4)	5	8	5	8	TcPc
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPc
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPc
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPc

No.	Parameter Symbol	Parameter Description	16.384 MHz Min.	16.384 MHz Max.	Unit
1	TdRXC(REQ)	$\overline{RXC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	TcPc
2	TdRXC(W)	$\overline{RXC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	TcPc
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	TcPc
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	TcPc
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	TcPc
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Notes 3, 4)	5	8	TcPc
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	TcPc
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	TcPc
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	TcPc

Notes:

1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
4. Parameter applies to Enhanced Request mode only.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

Read and Write Timing (see Figure 21)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TwPCl	PCLK Low Width	50	2000	40	2000	26	2000	ns
2	TwPCh	PCLK High Width	50	2000	40	2000	26	2000	ns
3	TfPC	PCLK Fall Time		15		12		8	ns
4	TrPC	PCLK Rise Time		15		12		8	ns
5	TcPC	PCLK Cycle Time	122	4000	100	4000	61	4000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	70		50		35		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	70		50		35		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	20		20		15		ns
11	TsIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time (Note 1)	145		120		70		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
13	TsIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	145		120		70		ns
14	ThIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	40		30		15		ns
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		0		ns
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	60		50		30		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note1)	0		0		0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	60		50		30		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	150		125		75		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		140		120		70	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		40		35		20	ns

Notes:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time at which the data bus is released from its drive state with a maximum DC load and minimum AC load.

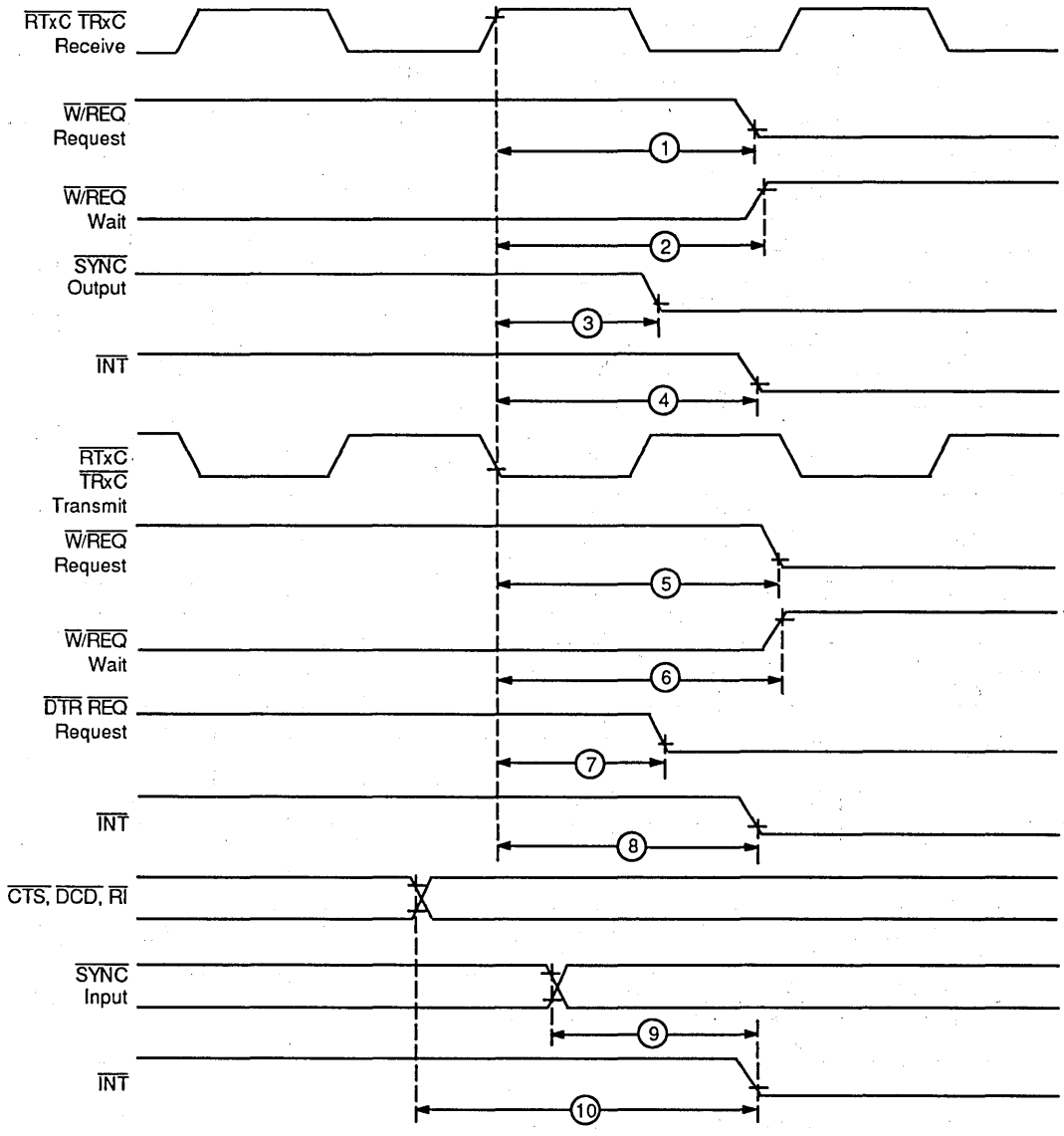


Figure 20. System Timing

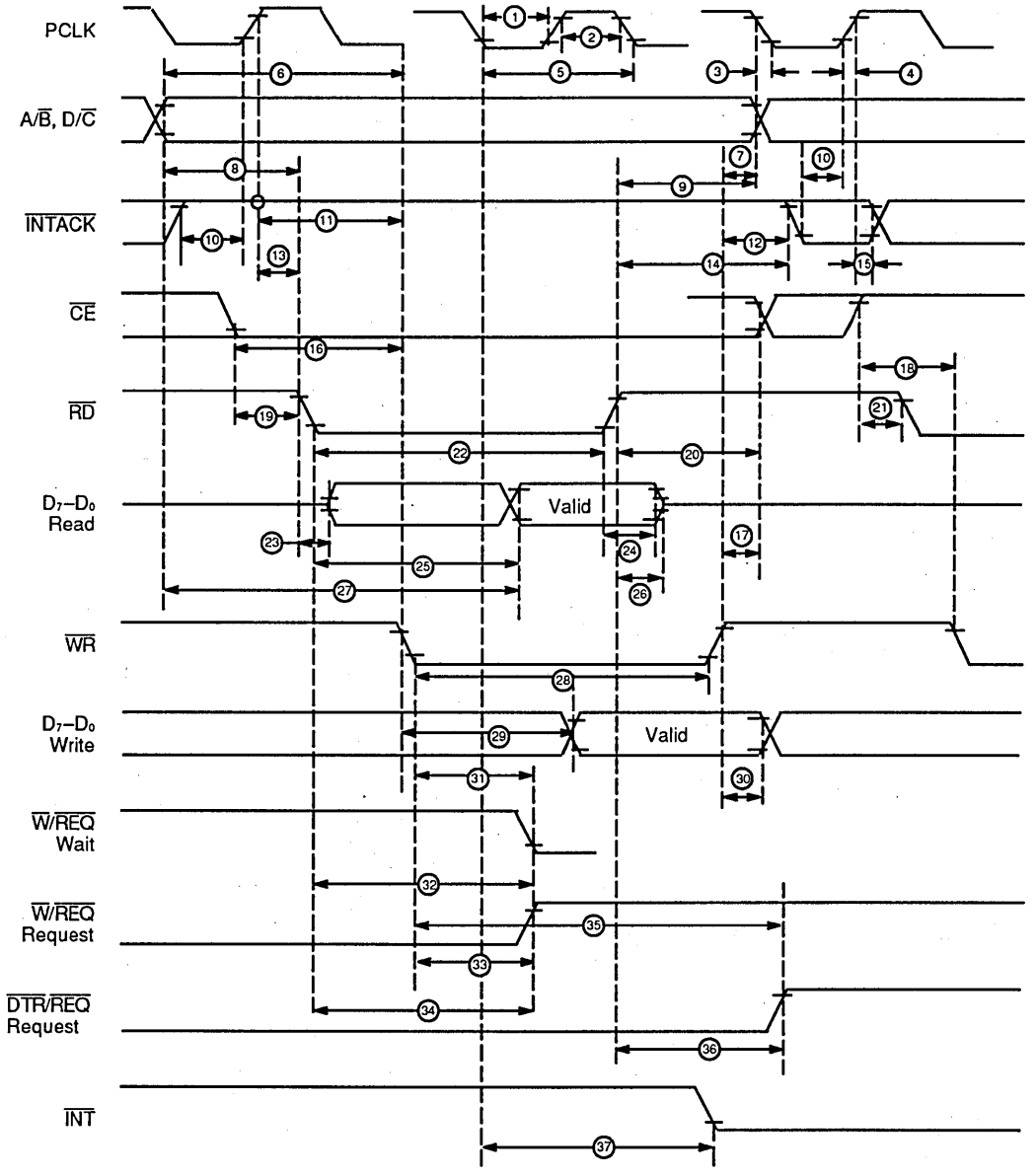


Figure 21. Read and Write Timing

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Continued)

Interrupt Acknowledge Timing, Reset Timing, Cycle Timing (see Figures 22–24)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		220		160		100	ns
28	TwWRI	$\overline{WR}$ Low Width	150		125		75		ns
29	TdWRf(DW)	$\overline{WR}$ ↓ to Write Data Valid		35		35		20	ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 2)		170		100		50	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 2)		170		100		50	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		120		70	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		120		70	ns
35a	TdWRr(REQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		4.0TcPc		4.0TcPc		4.0TcPc	ns
35b	TdWRr(EREQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		120		120		70	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		NA		NA		NA	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 2)		500		400		175	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 3)	150		125		50		ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	150		125		75		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		140		120		70	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	95		80		50	45	ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		95		80		45	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		200		175		80	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 2)		450		320		200	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	15		15		10		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	15		15		10		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	150		100		75		ns
49	Trc	Valid Access Recovery Time (Note 1)	3.5		3.5		3.5		TcPc

Notes:

1. Parameter applies only between transactions involving the ESCC, if $\overline{WR}/\overline{RD}$ falling edge is synchronized to PCLK falling edge, then TrC = 3TcPc.
2. Open-drain output, measured with open-drain test load.
3. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of DdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEI(IEO) for each device separating them in the daisy chain.
4. Parameter applies to Enhanced Request mode only.

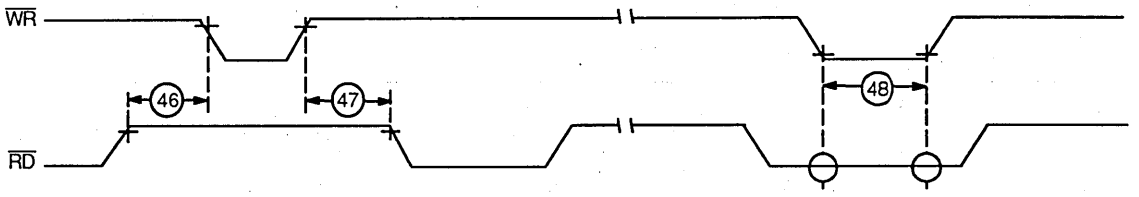


Figure 22. Reset Timing

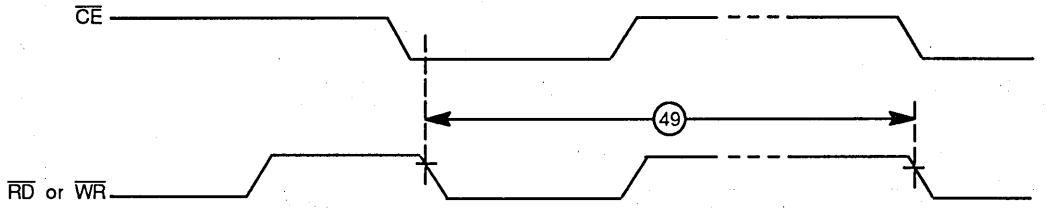


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Figure 23. Cycle Timing

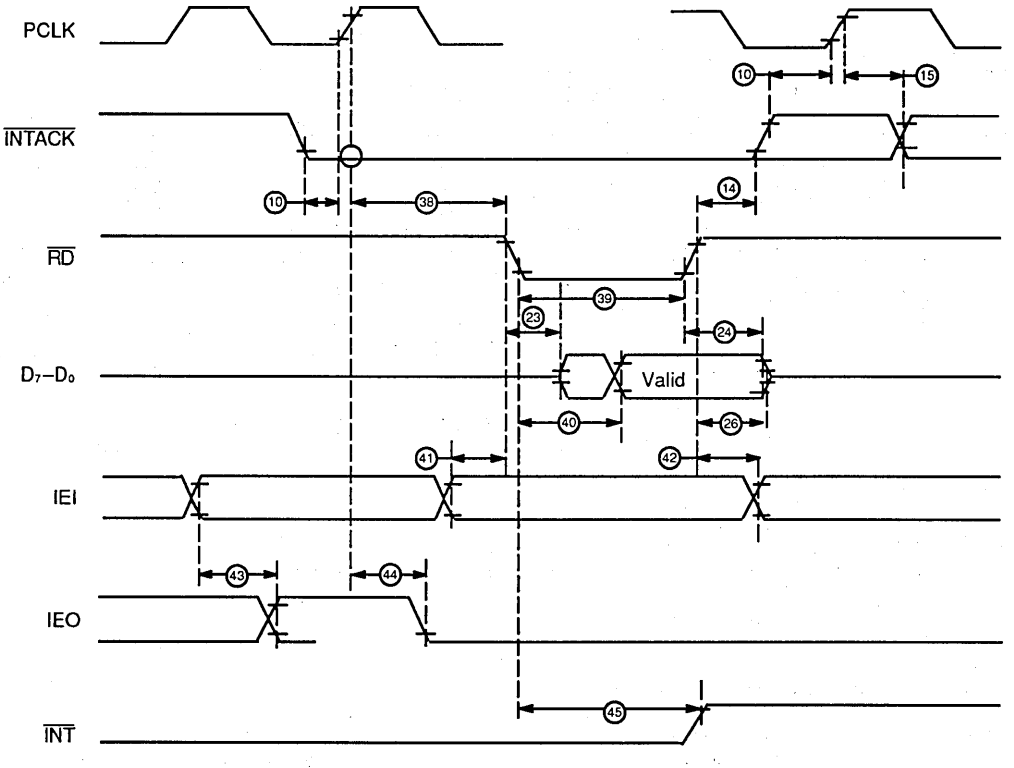


Figure 24. Interrupt Acknowledge Timing

SWITCHING CHARACTERISTICS over MILITARY/INDUSTRIAL operating range

General Timing (see Figure 19)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay		250		150		80	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		250		180	ns
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (Notes 1, 4 & 8)	NA	NA	NA	NA	NA	NA	
4	TsRXD(RXCr)	RxD to RxC ↑ Setup Time (XI Mode) (Note 1)	0		0		0		ns
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (XI Mode) (Note 1)	150		125		50		ns
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		0		ns
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (XI Mode) (Notes 1, 5)	150		125		50		ns
8	TsSY(RXC)	SYNC to RxC ↑ Setup Time (Note 1)	–200		–150		–100		ns
9	ThSY(RXC)	SYNC to RxC ↑ Hold Time (Note 1)	5TcPC		5TcPC		5TcPc		ns
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time (Notes 2, 4 & 8)	NA		NA		NA		
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (XI Mode) (Note 2)		200		150		80	ns
12	TdTXCr(TXD)	TxC ↑ to TxD Delay (XI Mode) (Notes 2, 5)		200		150		80	ns
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200		140		80	ns
14a	TwRTXh	RTxC High Width (Note 6)	150		120		80		ns
14b	TwRTxh(E)	RTxC High Width (Note 9)	50		40		15.6		ns
15a	TwRTXl	RTxC Low Width (Note 6)	150		120		80		ns
15b	TwRTXl(E)	RTxC Low Width (Note 9)	50		40		15.6		ns
16a	TcRTX	RTxC Cycle Time (Notes 6, 7)	488		400		244		ns
16b	TcRTx(E)	RTxC Cycle Time (Note 9)	125		100		31.25		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	125	1000	100	1000	62	1000	ns
18	TwTRXh	TRxC High Width (Note 6)	150		120		80		ns
19	TwTRXl	TRxC Low Width (Note 6)	150		120		80		ns
20	TcTRX	TRxC Cycle Time (Notes 6, 7)	488		400		244		ns
21	TwEXT	DCD or CTS Pulse Width	200		120		70		ns
22	TwSY	SYNC Pulse Width	200		120		70		ns

Notes:
1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30-pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.
8. External PCLK to RxC or TxC synchronization requirement eliminated for PCLK divide-by-four operation. TRxC and RTxC rise and fall times are identical to PCLK. Reference timing specs Tfpc and Trpc. Tx and Rx input clock slow rates should be kept to a maximum of 30 ns. All parameters related to input CLK edges should be referenced at the point at which the transition begins or ends, whichever is the worst case.
9. ENHANCED FEATURE—RTxC used as input to internal DPLL only.

SWITCHING CHARACTERISTICS over MILITARY/INDUSTRIAL operating range (Continued)

System Timing (see Figure 20)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TdRXC(REQ)	$\overline{RXC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	TcPc
2	TdRXC(W)	$\overline{RXC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	8	14	TcPc
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	4	7	TcPc
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPc
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	TcPc
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Notes 3, 4)	5	8	5	8	TcPc
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPc
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPc
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPc

No.	Parameter Symbol	Parameter Description	16.384 MHz		Unit
			Min.	Max.	
1	TdRXC(REQ)	$\overline{RXC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	TcPc
2	TdRXC(W)	$\overline{RXC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	TcPc
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	TcPc
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	TcPc
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	TcPc
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Notes 3, 4)	5	8	TcPc
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	TcPc
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	TcPc
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	TcPc

Notes:
1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
4. Parameter applies to Enhanced Request mode only.

SWITCHING CHARACTERISTICS over MILITARY/INDUSTRIAL operating range (Continued)

Read and Write Timing (see Figure 21)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	TwPCl	PCLK Low Width	50	1000	40	1000	26	1000	ns
2	TwPCh	PCLK High Width	50	1000	40	1000	26	1000	ns
3	TfPC	PCLK Fall Time		15		12		8	ns
4	TrPC	PCLK Rise Time		15		12		8	ns
5	TcPC	PCLK Cycle Time	122	2000	100	2000	61	2000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	70		50		35		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	70		50		35		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	20		20		15		ns
11	TsIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time (Note 1)	145		120		70		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
13	TsIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	145		120		70		ns
14	ThIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		0		ns
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	40		30		15		ns
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		0		ns
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	60		50		30		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note1)	0		0		0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	60		50		30		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	150		125		75		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		140		125	90	70	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		40		35	25	20	ns

Notes:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time at which the data bus is released from its drive state with a maximum DC load and minimum AC load.

SWITCHING CHARACTERISTICS over MILITARY/INDUSTRIAL operating range (Continued)

Interrupt Acknowledge Timing, Reset Timing, Cycle Timing (see Figures 22–24)

No.	Parameter Symbol	Parameter Description	8.192 MHz		10 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		220		160		100	ns
28	TwWRI	$\overline{WR}$ Low Width	150		125		75		ns
29	TdWRf(DW)	$\overline{WR}$ ↓ to Write Data Valid		35		35		20	ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 2)		170		100		50	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 2)		170		100		50	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		120		70	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		120		70	ns
35a	TdWRr(REQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		4.0TcPc		4.0TcPc		4.0TcPc	ns
35b	TdWRr(EREQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		120		120		70	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		NA		NA		NA	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 2)		500		400		175	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 3)	150		125		50		ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	150		125		75		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		140		120		70	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	95		80		50		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		0		0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		95		80		45	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		200		175		80	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 2)		450		320		200	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	15		15		10		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	15		15		10		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	150		100		75		ns
49	Trc	Valid Access Recovery Time (Note 1)	3.5		3.5		3.5		TcPc

Notes:

1. Parameter applies only between transactions involving the ESCC, if $\overline{WR/RD}$ falling edge is synchronized to PCLK falling edge, then TrC = 3TcPc.
2. Open-drain output, measured with open-drain test load.
3. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of DdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEI(IEO) for each device separating them in the daisy chain.
4. Parameter applies to Enhanced Request mode only.

ADVANCE INFORMATION

Am85C230A

Enhanced Serial Communication Controller with LocalTalk™ Support (ESCC/LT)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

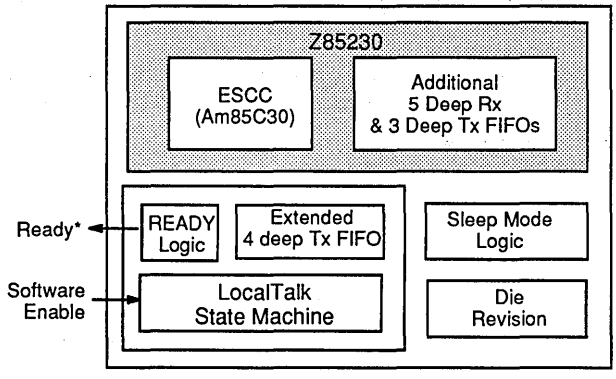
- **Plug compatible with Zilog Z85230**
  - Deactivation of $\overline{RTS}$ pin after the SDLC ending flag
  - Automatic transmission of the SDLC beginning flag
  - Automatic reset of Tx underrun/EOM latch
  - Complete CRC reception
  - TxD pin automatically forced high in NRZI encoding mode
  - Rx FIFO unlock after special condition interrupt when Status FIFO is used
  - Write registers WR3, WR4, WR5 and WR10 being readable
  - DTR/REQ pin timing reduced
  - Faster interrupt response
  - Software interrupt acknowledge mode
  - Addition of new register WR7'
  - Modified Databus Timing (Parameter #29)
  - Additional Rx and Tx FIFO
  - Tx Clock divider (X16 & X32) in Synchronous modes
  - Latching of RR0 during Read Cycle
- **Implements the following LocalTalk requirements:**
  - Generation of SYNC pulse before the SDLC opening FLAG
  - Generation of two SDLC opening FLAGs
  - Generation of an abort sequence at the end of LocalTalk packet
  - Automatic Receive Disable during Transmit
- **8-byte Receive and 4-byte (extendable to 8-byte) Transmit FIFO**
- **Generation of 'End of Packet' DMA Request**
- **Fast data rates; up to 20 MHz / 5Mb/s**
- **Sleep mode for reduced power**
- **Addition of Schmitt Trigger Circuit on Rx and Tx clock inputs**
- **Ready function added to reflect valid access recovery time**
- **Availability of the die revision ID information**
- **Available in both 40-pin DIP and 44-pin PLCC packages**

GENERAL DESCRIPTION

The Am85C230A is pin and software compatible and a functional superset of Z85230. Enhancements to the Z85230 include, hardware implementation of Apple LocalTalk protocol, 4 deep Transmit FIFO extension to total 8-byte Rx and 8-byte Tx FIFOs, Ready signal to reflect the write recovery time, sleep mode for reduced power, addition of Schmitt trigger circuitry on Rx and Tx clock inputs, and the availability of die revision information.

At power up, Am85C230A will look like the Z85230. The LocalTalk enhancements, TX FIFO extension and the die revision ID can be enabled using the new WR6' register.

BLOCK DIAGRAM



*Option on PLCC Package only

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Publication# 16505 Rev. A Amendment/0
Issue Date: November 1991

Interfacing the Am8530H and Am85C30 Serial Communications Controllers to the 80186 Microprocessor

by John Langlois

INTRODUCTION

A simple interface between the 80186 Microprocessor and 8530 Serial Communications Controller (SCC) can now be realized, due to the enhancements achieved with the Am8530H and Am85C30 Serial Communications Controllers. Previous application notes have required eight 74LS devices to meet the 8530 timing requirements. This document describes solutions that can be implemented in a single chip. Depending on system constraints, the interface can be as simple as a single inverter (Am85C30 in enhanced mode), but is never more than a PAL16L8 (Am8530H) device.

The timing requirements of each version of the 8530 are examined in the next section. The original 8530 is discussed only to provide a reference point. Solutions for each interface problem are then presented. If a particular feature is not required, that circuit obviously need not be implemented. Timing analysis for the complete interfaces follow the solutions. PAL, equations are also included.

For the purposes of this document, it is assumed that the reader is familiar with the 8530 SCC and 80186 microprocessor. The following data sheets are applicable:

AMD 80186 High Integration 16-Bit Microprocessor (Order #03551)

AMD Am85C30 Enhanced Serial Communications Controller (Order #10216)

AMD Am8530H Serial Communications Controller (Order #00970)

AMD Am85C30 Technical Manual (Order #07513)

TIMING REQUIREMENTS

8530 SCC

The original 8530/80186 interface is complicated by several factors, the most difficult being the access recovery time (T_{rc}). The minimum time from the trailing edge of one command to the leading edge of the next is six clock cycles + 130 ns for the 6 MHz part. This necessitates the use of extensive wait state generation circuitry to hold off back-to-back accesses. It is possible to meet the requirement in software by inserting NOPs. This practice is generally frowned upon, since the processor clock speed would affect the software. Also, DMA transfers at high rates have no way of inserting NOPs. The solution to this has already been addressed and is not part of this discussion (EDN, April 4, 1985, pp. 274–275).

Interrupt acknowledge cycles with the 8530 don't match the 80186. While the 80186 generates two pulses on the INTA line, reading the vector on the second pulse, the 8530 expects to see one long INTA pulse, with a read strobe near the end to read the interrupt vector. Note that it is possible to read the interrupt vector from Read Register 2 of the 8530. This will not, however, set the IUS bit and mask off lower priority interrupts; a hardware cycle must occur to accomplish that.

Data is expected to be valid at the leading edge of write during a write cycle. Consequently, write must be delayed to the 8530 until the next rising edge of the processor clock. This may or may not be a problem, depending on how the wait state circuitry is implemented.

The read strobe must also be delayed by one-half clock to meet the address setup time requirements.

Direct Memory Access (DMA) transfers are supported by the 8530. The $\overline{W/REQ}$ pin may be programmed as a DMA request for either transmit or receive. $\overline{DTR/REQ}$ can be used as a DMA request for transmit only. It is possible to support single-channel full-duplex or dual-channel half-duplex DMA with the DMA controller resident on the 80186. While the $\overline{W/REQ}$ timing does not present a problem, it is always possible to generate erroneous requests on the $\overline{DTR/REQ}$ interface. This is due to $\overline{DTR/REQ}$ going to its inactive state timed from the trailing edge of the command, which is too late to prevent an additional DMA request from being recognized by the 80186. $\overline{DTR/REQ}$ must therefore be negated at the beginning of the cycle servicing the request.

A reset of the 8530 is accomplished by asserting read and write simultaneously. A software reset command can also be issued by reading Read Register 0 and writing the reset command to Write Register 9. This is a choice left to the designer.

Am8530H SCC

A major improvement was made in the access recovery time with the Am8530H. T_{rc} is now measured from the leading edge of one command to the leading edge of the next. It is also reduced from six clocks + 130 ns to four clocks. The increased clock speed (8.192 MHz) allows it to be clocked from the 80186 CLKOUT in many systems. This improvement eliminates the wait state generation circuitry, allowing the 80186's internal wait state generator to be used.

The other 8530 timing requirements are still valid.

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Am85C30 ESCC

The Am85C30 provides many additional improvements. With this device, it is possible to interface to the 80186 with three inverters and still have interrupt and DMA support.

Access recovery time is improved to three clock cycles if the commands are synchronized to PCLK. This is the case here, since CLKOUT from the 80186 is driving PCLK. As in the Am8530H, it is measured from leading edge to leading edge of the command.

With the Am85C30, it is not necessary to use hardware interrupt acknowledge sequences. An additional feature has been added that will emulate a hardware cycle when the vector is read from Read Register 2. As with the hardware cycle, the IUS bit is set and all lower priority interrupts within the device are masked. Bit D5 of Write Register 9 controls this enhancement.

Data does not need to be valid prior to the leading edge of write. The timing has been relaxed so that data can become valid a short time after write. To take advantage of this, the Am85C30 data pins must be connected directly to the 80186, as the additional buffer delay would violate this parameter. This is not a problem in most systems. If it is, write must be delayed.

The read strobe need not be delayed, due to improved address setup time parameters.

The last enhancement of the Am85C30 that affects the 80186 interface is $\overline{DTR}/\overline{REQ}$ timing. The extended Write Register 7, or WR7', is enabled by setting bit D0 of Write Register 15. Bit D4 of WR7' then controls whether $\overline{DTR}/\overline{REQ}$ is de-asserted at the leading edge, like $\overline{W}/\overline{REQ}$, or the trailing edge, as in the 8530.

SOLUTIONS

Delayed Write

Write to the 8530 must be delayed in the case of the Am8530H, and may need to be delayed with the Am85C30. Two signals enter into the delayed write equation: WRITE from the 80186 and CLKOUT. The PAL equation is:

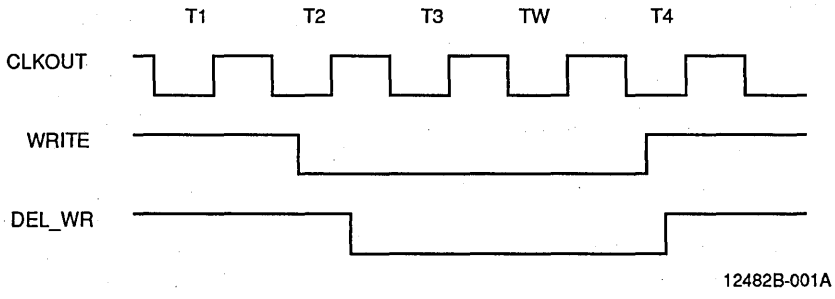
```
DEL_WR   =   WRITE * DEL_WR + CLKOUT *
             WRITE
```

This equation is read as: DEL_WR will be active (low) if WRITE is active (low) and DEL_WR is active (low), or CLKOUT is active (high) and WRITE is active (low).

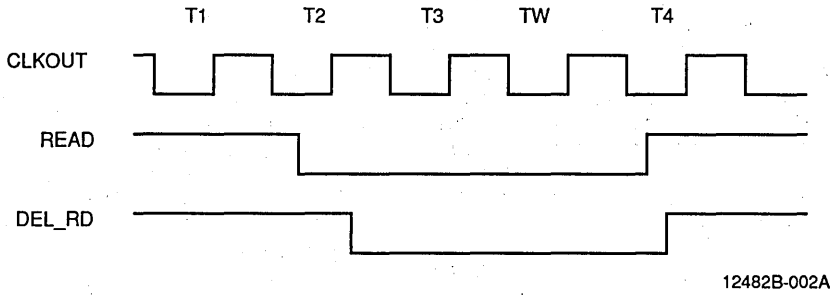
Delayed Read

The read strobe may need to be delayed to meet address setup requirements. The same equation used for delayed write applies.

```
DEL_RD   =   READ * DEL_RD + CLKOUT * READ
```



Delayed Write



Delayed Read

Interrupt Acknowledge Generation

This circuit generates the required interrupt acknowledge pulse and read strobe to the 8530 during an interrupt acknowledge sequence. Inputs are CLKOUT and INTA0, both generated by the 80186. ZINTACK and ZRD are outputs driving INTA and READ of the 8530, respectively. ZINTACK is simply INTA0 divided by 2, set to its inactive state on reset. This is easily done with a positive edge-triggered flip-flop, but that's not being used. To perform the same function in a combinatorial PAL device, two macrocells are used.

ZRD is merely the logical AND of INTA0 and ZINTACK. ZS0, ZINTACK and ZRD are defined as active low signals. RESET is active high and initializes the two cells.

```
ZS0      =  RESET + (ZS0 * /INTA0 + ZS0 *
            ZINTACK + INTA0 * ZINTACK)
ZINTACK  =  /RESET * (/ZS0 * /INTA0 + /ZS0
            * ZINTACK + INTA0 * ZINTACK)
ZRD      =  ZINTACK * INTA0
```

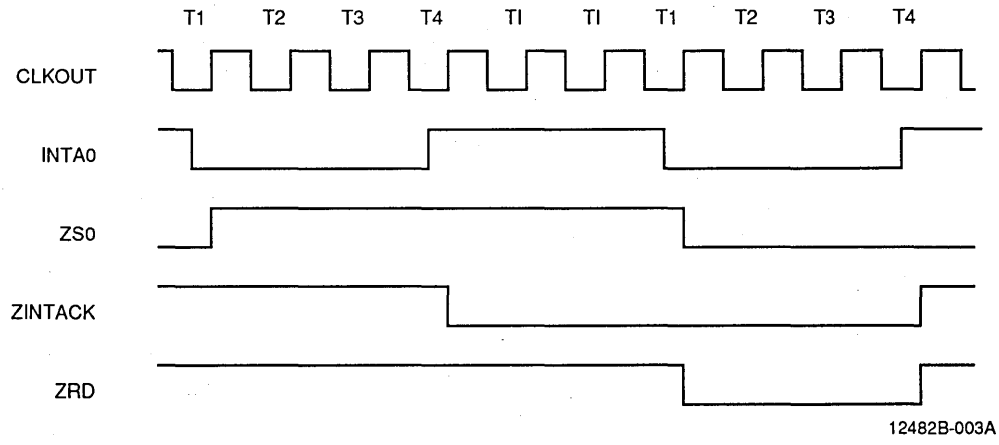
Hardware Reset

A hardware reset is generated by asserting a read and write to the 8530 simultaneously. RESET is an active high output from the 80186.

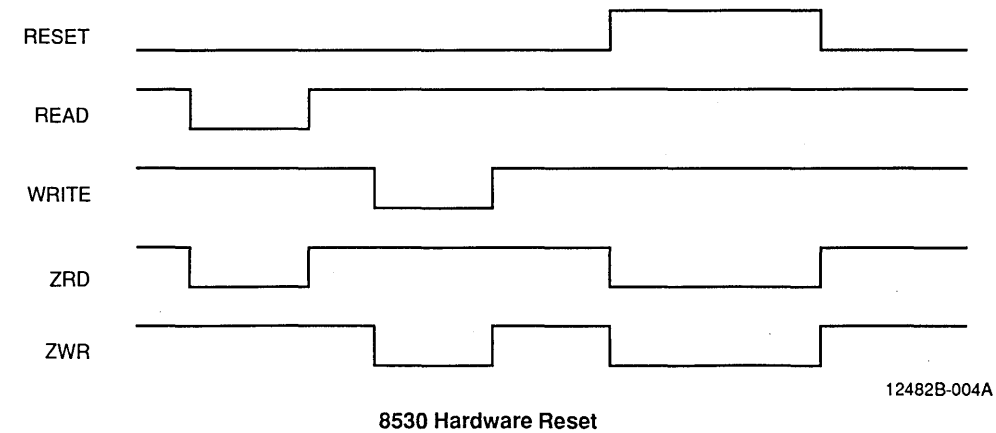
```
ZRD      =  READ + RESET
ZWR      =  WRITE + RESET
```

DTR/REQ Removal

There are two solutions to the DTR/REQ removal problem. One solution uses a separate Peripheral Chip Select for transfers associated with the request. The other solution requires delayed write and S6 (A19) of the 80186, which indicates whether the current bus cycle is DMA or processor. Write must be delayed, since S6 is not guaranteed valid at its leading edge. Write will be combined with one of these inputs to clear the request. DTR/REQ only supports transmit data, consequently, read is irrelevant.



Interrupt Acknowledge Sequence



8530 Hardware Reset

It is not necessary to decode A/B to determine which channel of the 8530 is being accessed. If $\overline{DTR/REQ}$ is used, then that channel is full-duplex, expending both 80186 DMA request inputs; the other channel cannot be supported. If the channel is half-duplex, then $\overline{W/REQ}$ would be utilized because it goes both ways.

The following solution uses delayed write and S6. With a separate chip select, merely substitute it for S6 and use the normal write (not that the delayed write is abnormal). This circuit could also be implemented using a standard flip-flop, but it can easily be realized with two cells in the PAL device.

Define CLEAR as the logical AND of the 8530's chip select, delayed write, and S6. Assume PCS0 from the processor is the chip select. DRQ1 is the DMA request to the 80186. DS0 is the output of the second cell. All signals are active low, with the exception of RESET. RESET initializes the two cells to their correct state.

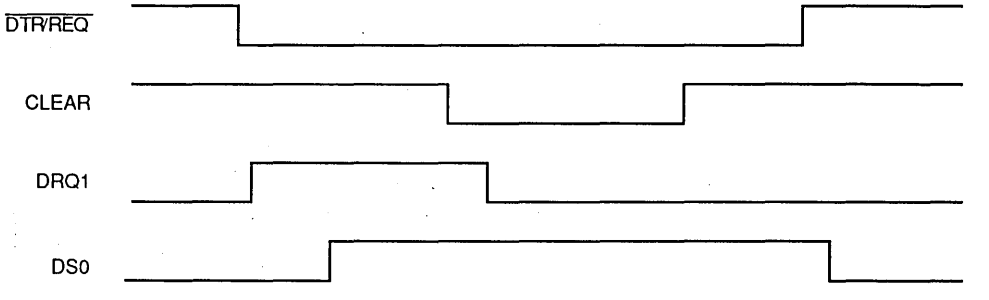
```
DS0     =   DS0 * DRQ1 + /DTR_REQ * DRQ1 +
            RESET

DRQ1    =   /DS0 * DRQ1 + CLEAR * /DS0 +
            /DS0 * /DTR_REQ  + DRQ1 *
            /DTR_REQ + RESET
```

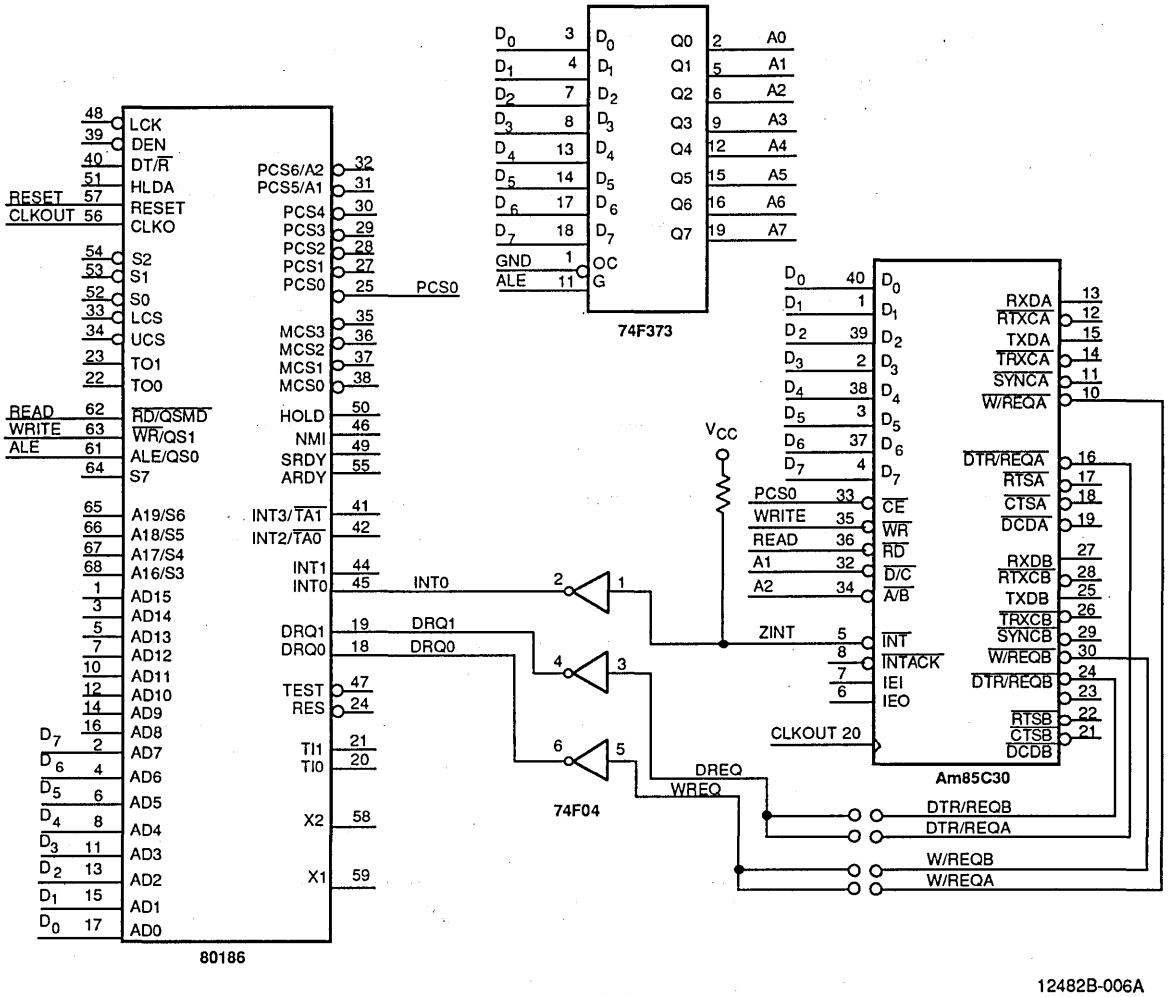
COMPLETE SOLUTIONS

Am85C30 Enhanced Mode

If using the Am85C30 in enhanced mode without hardware interrupt vector transfer, the 80186 interface is trivial. The interrupt and DMA request lines must be inverted, for which 1/2 of a 74F04 is adequate. It is assumed that a data buffer is not placed between the Am85C30 and the 80186, otherwise, WRITE must be delayed. RESET is performed in software and the clock rate is 10 MHz.



$\overline{DTR/REQ}$ Removal



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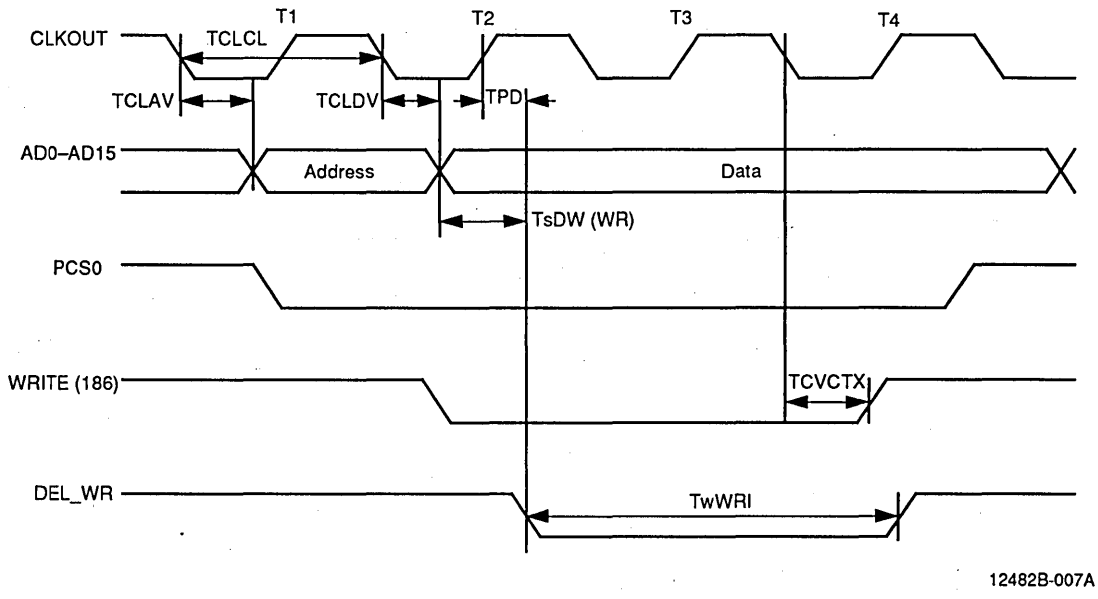
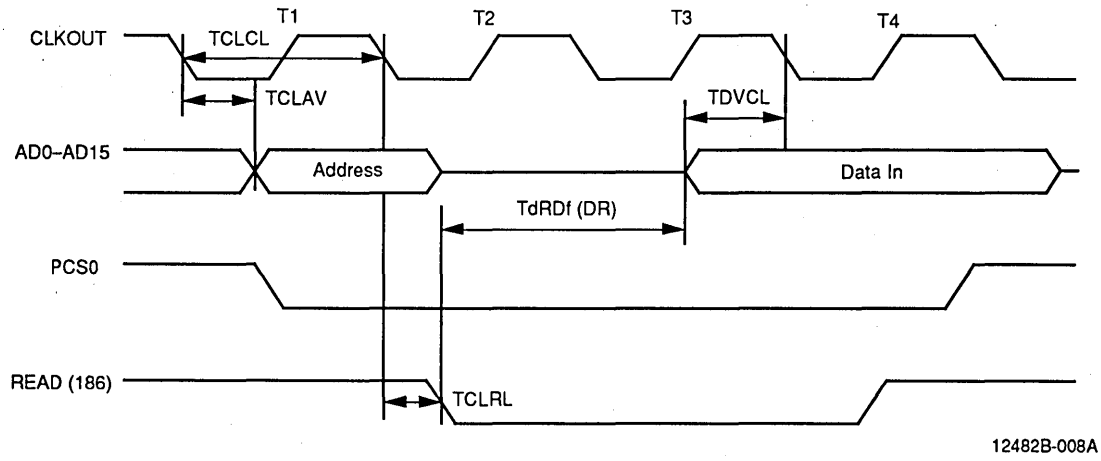
Am85C30/80186 Schematic



Am8530H Write Cycle Timing Diagram



Am85C30 Read Cycle Timing Diagram

Write Cycle Timing

The Am85C30 required address setup time is 50 ns.

$T_{sA(WR)} = T_{CLCL} - T_{CLAV} - T_{F373} + T_{CVCTV}$
$= 100 - 44 - 8 + 5$
$= 53$ ns

Data to the Am85C30 must be valid within 35 ns of WRITE being active.

$T_{dWRf(DW)} = T_{CLDV}(max) - T_{CVCTV}(min)$
$= 40 - 5$
$= 35$ ns

WRITE is to be active for a minimum of 125 ns.

$T_{wWRI} = 2\,T_{CLCL} - T_{CVCTV} + T_{CVCTX}$
$= 200 - 56 + 5$
$= 149$ ns

The access recovery time of three clocks is easily satisfied.

Read Cycle Timing

Data must be valid at the 80186 15 ns prior to the beginning of state T4. Data valid from READ active for the Am85C30 is 120 ns.The Am85C30 required address setup time is 50 ns.

$T_{DVCL} = T_{CLCL} - T_{CLRL} - T_{dRDf(DR)}$
$= 200 - 40 - 120$
$= 40$ ns

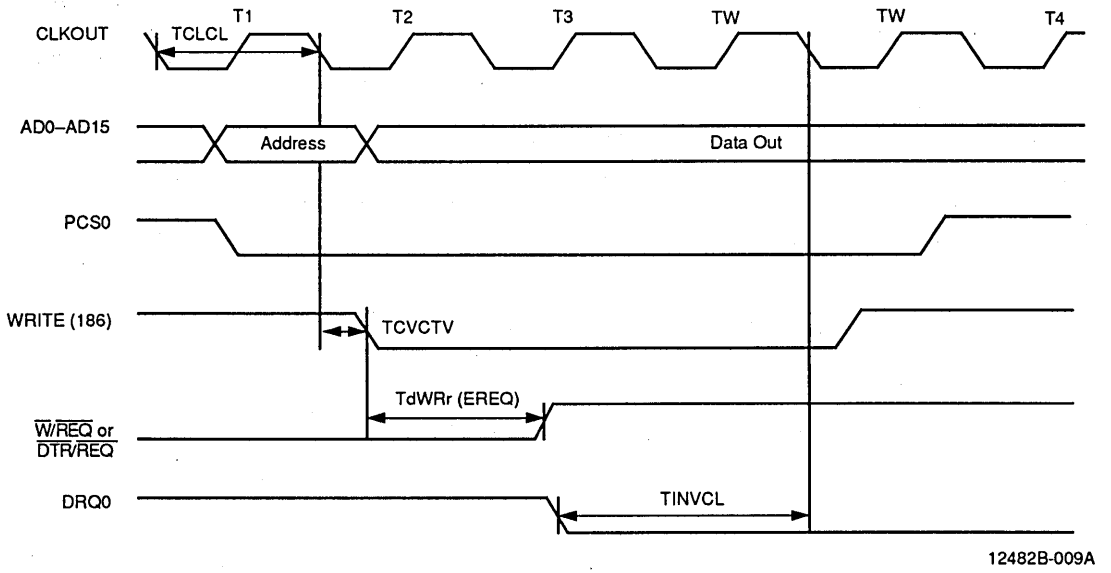
Address setup for READ is the same as WRITE, 50 ns.

$T_{sA(RD)} = T_{CLCL} - T_{CLAV} - T_{F373} + T_{CLRL}$
$= 100 - 44 - 8 + 10$
$= 58$ ns

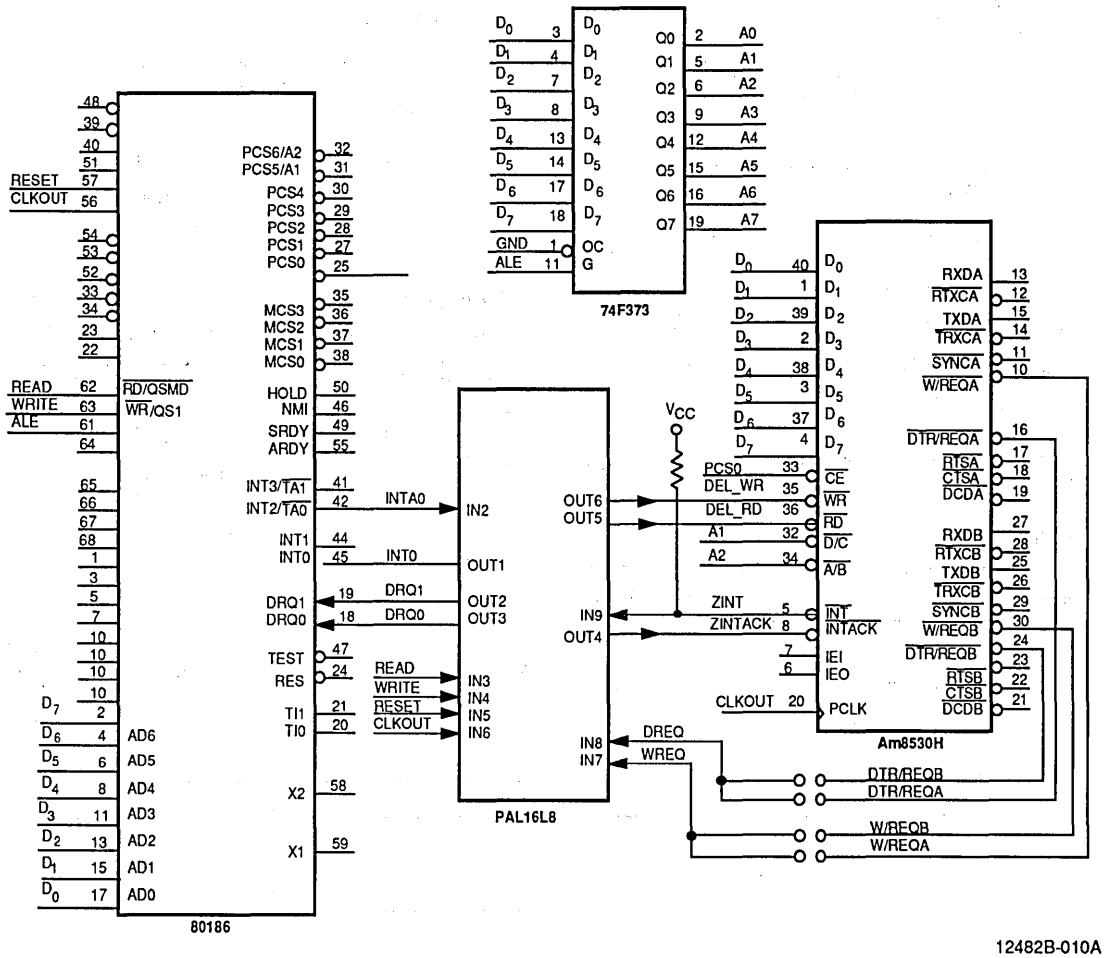
DMA Timing

To prevent a false DMA cycle, the request must be deasserted two clock periods prior to the end of the current bus cycle. The required setup time for DRQ into the 80186 is 20 ns. With one wait state, the specification is missed by 2 ns, therefore, two wait states are required.

$T_{INVCL} = 3\,T_{CLCL} - T_{CVCTV} - T_{dWRr(EREQ)} - T_{F04}$
$= 300 - 56 - 120 - 6$
$= 118$ ns



Am85C30 DMA Cycle Timing Diagram



Am8530H/80186 Schematic

Am8530H

This analysis applies to the 8.192 MHz Am8530H, but the design works with the Am85C30 as well. All of the solutions in the "SOLUTIONS" section are utilized to provide a complete interface. Included are hardware interrupt acknowledge cycles, full DMA support with removal of $\overline{DTR}/\overline{REQ}$, hardware reset, and delayed reads and writes.

Write Cycle Timing

The required address setup time for the 8.192-MHz Am8530H is 70 ns.

$T_{sA(WR)} = T_{CLCL} + T_{CLCH} - T_{F373} - T_{CLAV}$
$= 125 + 56.5 - 8 - 55$
$= 118.5$ ns

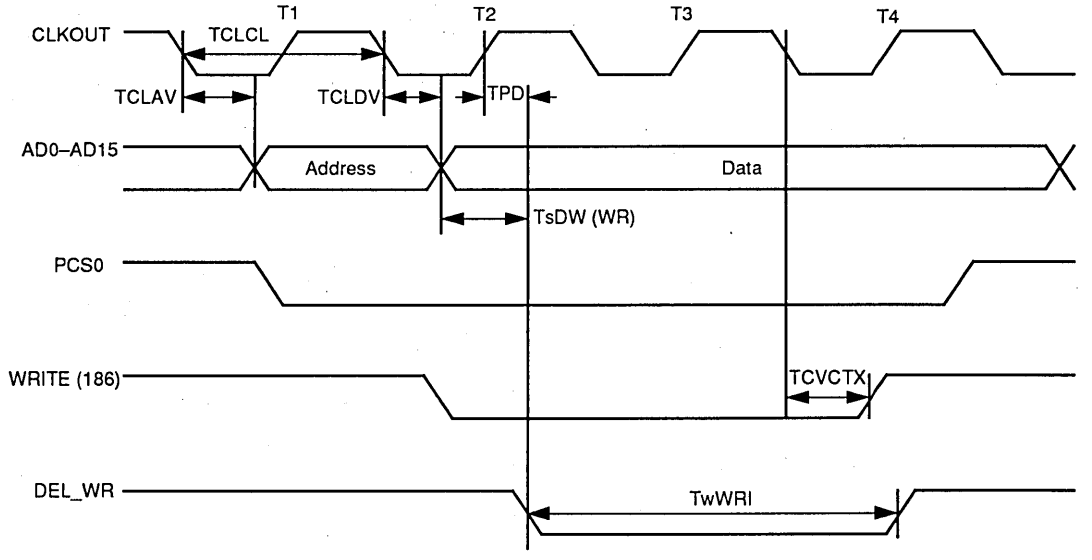
Data has to be valid 10 ns before the falling edge of WRITE to the Am8530H.

$T_{sDW(W)} = T_{CLCH} - T_{CLDV}$
$= 56.5 - 44$
$= 12.5$ ns

WRITE must be low for 150 ns.

$T_{wWR} = T_{CLCL} + T_{CLCH} - T_{PD} + T_{CVCTX}$
$= 181.5 - 15 + 5$
$= 171.5$ ns

Four clock edges occur between leading command edges. This satisfies the access recovery time.



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Am8530H Write Cycle Timing Diagram

Read Cycle Timing

Data must be valid at the 80186 20 ns prior to the beginning of state T4. Data valid from READ active for the Am8530H is 140 ns.

T_{DVCL} = $T_{CLCL} + T_{CLCH} - T_{PD} - T_{dRDf(DR)}$
= 181.5 – 15 – 140
= 26.5 ns

The required address setup time for the 8.192 MHz Am8530H is 70 ns.

$T_{sA(RD)}$ = $T_{CLCL} + T_{CLCH} - T_{F373} - T_{CLAV}$
= 181.5 – 8 – 55
= 118.5 ns

DMA Timing

To prevent a false DMA cycle, the request must be deasserted two clock periods prior to the end of the current bus cycle. The required setup time for DRQ into the 80186 is 25 ns.

$\overline{W/REQ}$

T_{INVCL} = $2T_{CLCL} + T_{CLCH} - T_{PD} - T_{dWRf(REQ)} - T_{PD}$
= 306.5 – 15 – 170 – 15
= 106.5 ns

$\overline{DTR/REQ}$

T_{INVCL} = $2T_{CLCL} + T_{CLCH} - 2T_{PD}$
= 306.5 – 30
= 276.5 ns

Thus, two wait states are necessary to meet the $\overline{W/REQ}$ timing.

Interrupt Acknowledge Cycle Timing

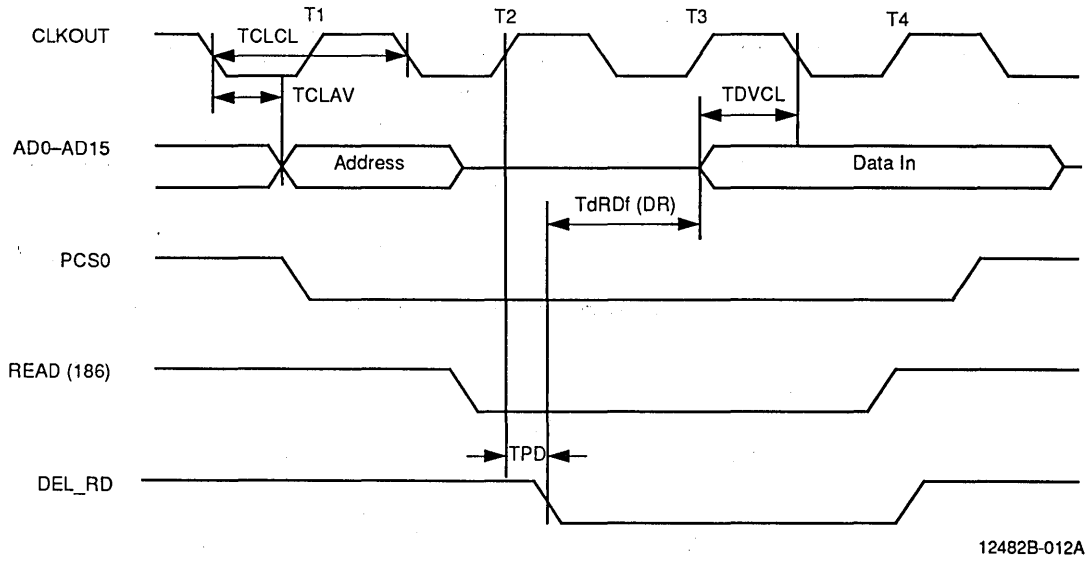
Interrupt acknowledge to the Am8530H is to be valid 150 ns prior to READ becoming active. ZINTACK is guaranteed to be recognized by the Am8530H at the middle of the first idle state between the interrupt acknowledge pulses.

$T_{dIAi(RD)}$ = $T_{CLCL} + T_{CLCH} + T_{CVCTV}$
= 181.5 + 10
= 191.5 ns

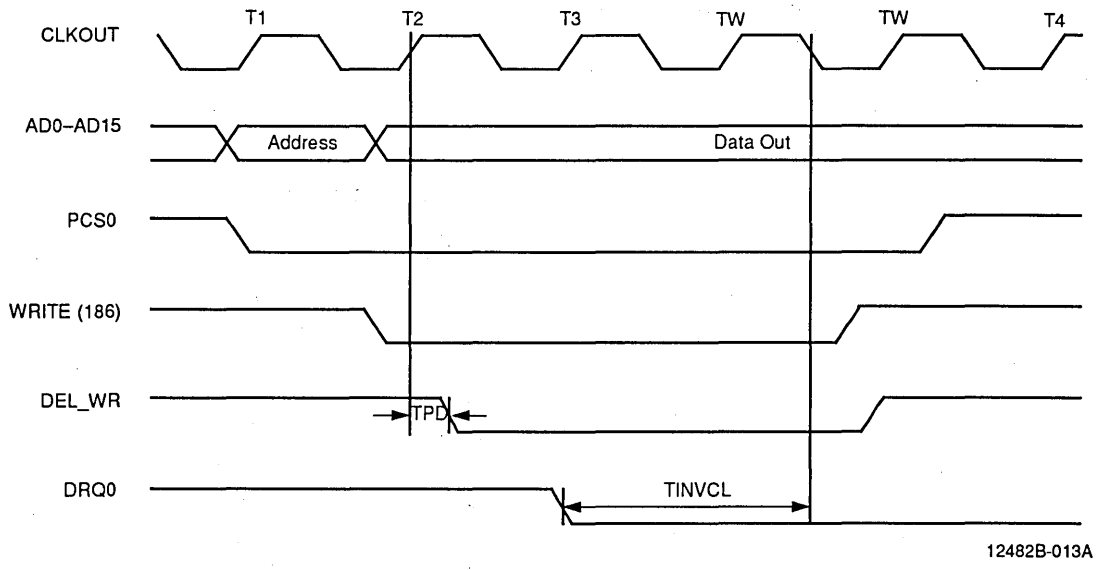
There is not enough delay between ZINTACK and DEL_RD to allow daisy-chained interrupts. Equations are given in the following "Am8530H INTERFACE PAL EQUATIONS" section to assert ZINTACK at the beginning of the first INTA0 cycle.

The interrupt vector must be valid 25 ns prior to T4.

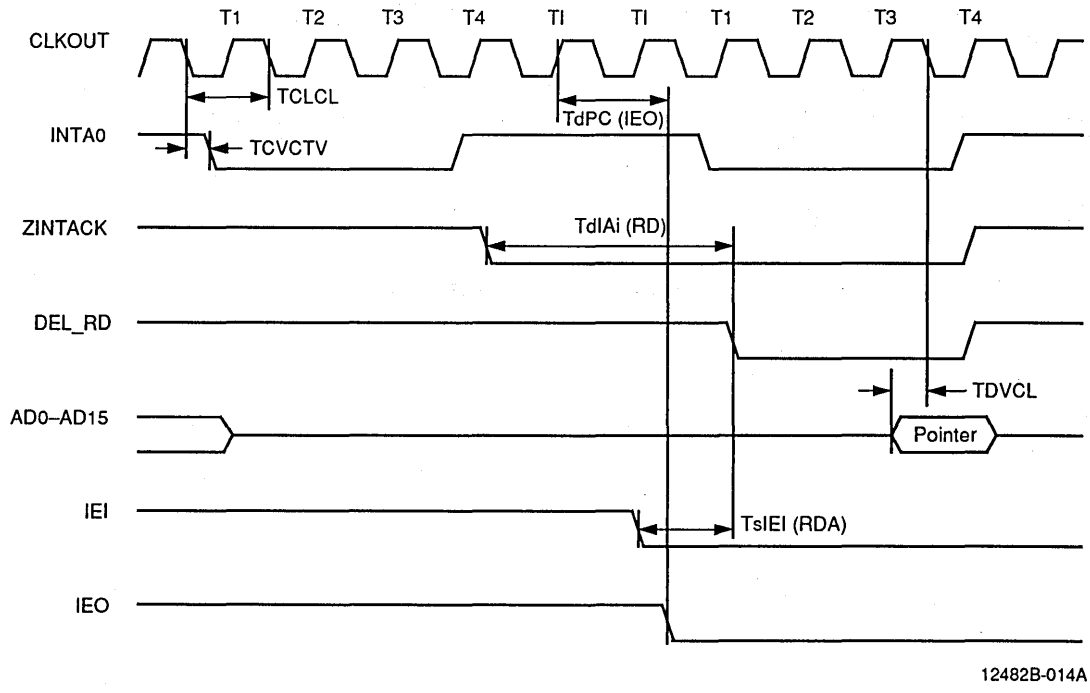
T_{DVCL} = $3T_{CLCL} - T_{CVCTV} - T_{PD} - T_{dRDA(DR)}$
= 375 – 70 – 15 – 140
= 150 ns



Am8530H Read Cycle Timing Diagram



Am8530H DMA Cycle Timing Diagram



Am8530H Interrupt Acknowledge Timing Diagram

Am8530H INTERFACE PAL EQUATIONS

Note: Do not minimize these equations.

Device Am8530H (P16L8)

```
PIN
        RESET           = 1             (INPUT COMBINATORIAL)
        /READ           = 2             (INPUT COMBINATORIAL)
        /WRITE          = 3             (INPUT COMBINATORIAL)
        CLKOUT          = 4             (INPUT COMBINATORIAL)
        /INTA0          = 5             (INPUT COMBINATORIAL)
        /DTR_REQ        = 6             (INPUT COMBINATORIAL)
        /WREQ           = 7             (INPUT COMBINATORIAL)
        /ZINT           = 8             (INPUT COMBINATORIAL)
        A19             = 9             (INPUT COMBINATORIAL)
        /INT0           = 12            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /DS0            = 13            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /ZS0            = 14            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /ZINTACK        = 15            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /DEL_RD         = 16            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /DEL_WR         = 17            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /DRQ1           = 18            (OUTPUT ACTIVE_LOW COMBINATORIAL)
        /DRQ0           = 19            (OUTPUT ACTIVE_LOW COMBINATORIAL);
BEGIN
ENABLE (INT0, ZS0, ZINTACK, DEL_RD, DEL_WR, DRQ1, DRQ0);
ZS0      =  RESET + (ZS0 * /INTA0 + ZS0 * ZINTACK + INTA0 * ZINTACK);
ZINTACK  =  /RESET * (/ZS0 * /INTA0 + /ZS0 * ZINTACK + INTA0 * ZINTACK);
DRQ1     =  /DS0 * DRQ1 + A19 * DEL_WR * /DS0 + /DS0 * /DTR_REQ + DRQ1 * /DTR_REQ + RESET;
DS0      =  DS0 * DRQ1 + /DTR_REQ * DRQ1 + RESET;
DRQ0     =  /WREQ;
INT0     =  /ZINT;
DEL_WR   =  WRITE * DEL_WR + CLKOUT * WRITE + RESET;
DEL_RD   =  READ * DEL_RD + CLKOUT * READ + ZINTACK * INTA0 + RESET;
END.
```

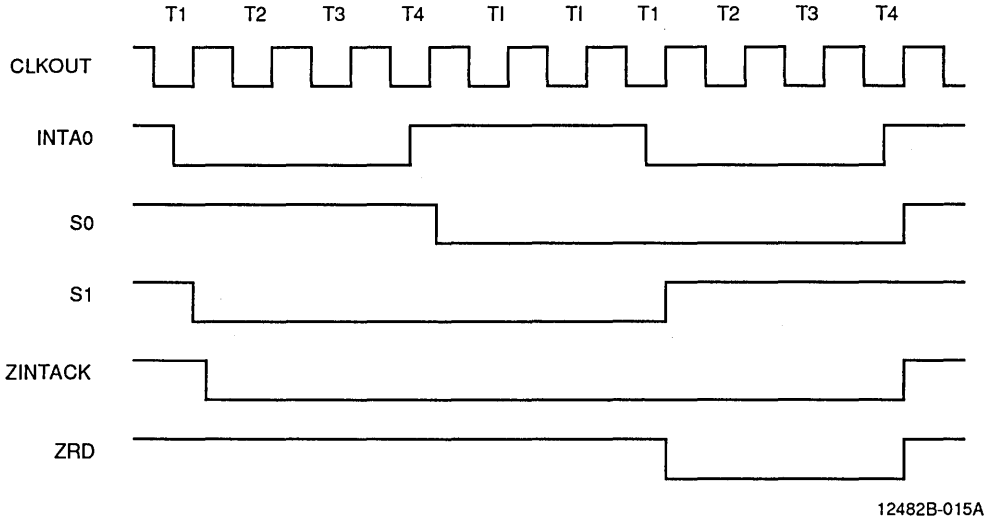
To support a daisy-chained interrupt structure, an extra output is required. This precludes using a 16L8 to implement the complete interface. A 22V10 could easily be utilized. The following equations would generate ZINTACK beginning at the start of the first INTA0 pulse. All signals are combinatorial active low.

```
S0       =  (S0*S1 + /INTA0*S1 +
            INTA0*S0)*/RESET;

S1       =  (/S0*S1 + /INTA0*S1 +
            INTA0*/S0)*/RESET;

ZINTACK  =  S0 + S1;

DEL_RD   =  READ * DEL_RD + CLKOUT * READ
            + S0 * INTA0 + RESET;
```



Daisy-Chained Interrupt Acknowledge Sequence

CHAPTER 3
Combination SCSI/SCC Controller

PRELIMINARY

Am85C80

Combined SCSI Controller and Serial Communications Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **The Am85C80 is an Enhanced Serial Communications Controller (ESCC) and Small Computer Systems Interface (SCSI) Controller**
  - This chip replaces both the 85C30 Serial Communications Controller (SCC) and the 53C80 SCSI Controller in functionality, while combining the two chips into a single package
  - The sleep mode feature consumes very little power; this feature may be used in notebook computer and other battery operated portable systems

ESCC

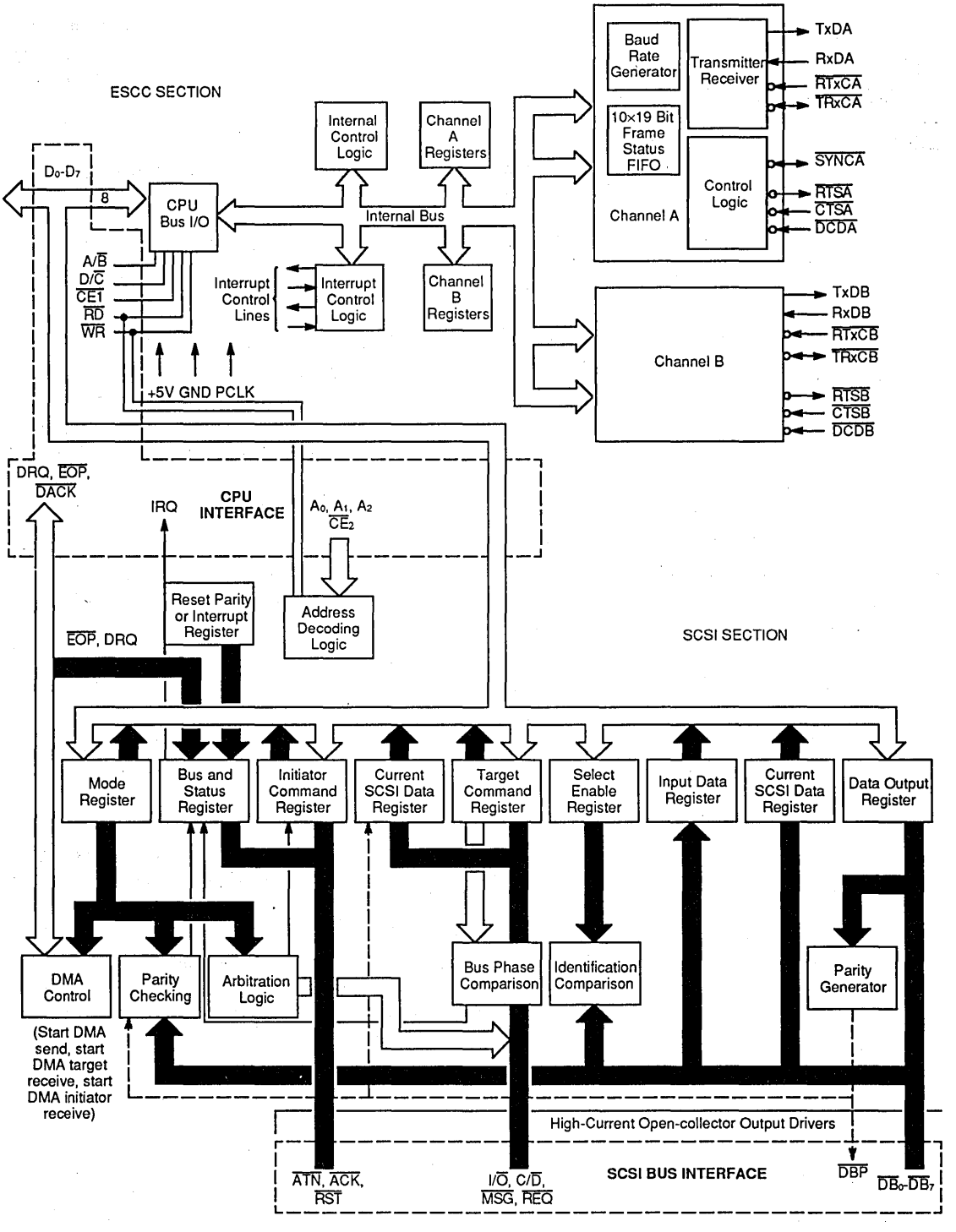
- **Fast Data Rate**
  - 8.192 MHz/2.048 Mb/s
  - 16.384 MHz/4.096 Mb/s
- **Low Power CMOS Technology**
- **Easily interfaced with most CPUs**
  - Compatible with non-multiplexed bus
- **Two Independent Full-duplex Serial Channels**
- **Asynchronous Mode Features**
  - Programmable stop bits, clock divider, character length and parity
  - Break detection/divider
  - Error detection for framing, overrun and parity
- **Synchronous Mode Features**
  - Supports IBM BISYNC, SDLC, SDLC Loop, HDLC and ADCCP Protocols
  - Programmable CRC generators and checkers
  - SDLC/HDLC support includes frame control, zero insertion and deletion, abort, and residue handling
  - External sync mode is supported on Channel A only
- **Enhanced ESCC functions support high-speed frame reception using DMA**
  - 14-bit frame byte counter
  - 10 × 19 SDLC/HDLC Frame Status FIFO
  - Independent Control on both channels
  - Enhanced operation does not allow special receive conditions to lock the three-byte DATA FIFO when the 10 × 19 FIFO is enabled
- **Local Loopback and Auto Echo Modes**
- **Internal or External Character Synchronization**
- **2 Mb/s FM Encoding Transmit and Receive capability using Internal DPLL for 16.384 MHz product**
- **Internal Synchronization between RxC to PCLK and TxC to PCLK**
  - This allows the user to eliminate external sychronization hardware required by the NMOS device when transmitting or receiving data at the maximum rate of 1/4 PCLK frequency

SCSI Interface

- **Asynchronous interface to 1.5 megabytes per second**
- **Supports Initiator and Target roles**
- **Parity generation with optional checking**
- **Supports Arbitration**
- **Direct control of all bus signals**
- **High-current outputs drive SCSI Bus directly**
- **Implements Glitch Eater circuitry that filters glitches upto 30 ns on the SCSI Bus**
- **CPU Interface Supports**
  - Memory or I/O-mapped interface
  - DMA or programmed I/O
  - Normal or Block mode DMA
  - Optional CPU interrupts

Publication # 12582 Rev. C Amendment /0
Issue Date: November 1991

BLOCK DIAGRAM



Block Diagram

12582C-096B

GENERAL DESCRIPTION

The Am85C80 is an Enhanced Serial Communications Controller and SCSI Interface Controller. The chip replaces both Am85C30 and Am53C80 in functionality, while combining the two chips into a single package.

ESCC

The Enhanced Serial Communications Controller (ESCC) is a high-speed, low-power, multi-protocol communications peripheral designed for use with 8- and 16-bit microprocessors. It has two independent, full duplex channels and functions as a serial-to-parallel, parallel-to-serial converter/controller. AMD's proprietary enhancements make the ESCC easier to interface and more effective in high-speed applications by reducing software overhead and eliminating the need for some external glue logic.

The ESCC is easy to use due to a variety of sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops and crystal oscillators which dramatically reduce the need for external logic. The device can generate and check CRC codes in any SYNC mode, and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

This versatile device supports virtually any serial data transfer application such as laser beam printers, networks, modems, cassettes and tape drives. The ESCC is designed for non-multiplexed buses and is easily interfaced with most CPUs, such as 80188, 80186, 80286, 8080, Z80, 6800, 68000 and MULTIBUS.

Enhancements which allow the ESCC to be used more effectively in high-speed applications include:

- a 10 × 19 bit SDLC/HDLC frame status FIFO array
- a 14-bit SDLC/HDLC frame byte counter
- automatic SDLC/HDLC opening frame flag transmission
- TxD pin forced High in SDLC NRZI mode after closing flag
- automatic SDLC/HDLC Tx underrun/EOM flag reset
- automatic SDLC/HDLC Tx CRC generator reset/preset
- $\overline{RTS}$ synchronization to closing SDLC/HDLC flag
- $\overline{DTR}/\overline{REQ}$ deactivation delay significantly reduced
- external PCLK to $\overline{RxC}$ or $\overline{TxC}$ synchronization requirement eliminated for PCLK divide-by-four operation
- 16 MHz operation

Other enhancements to improve the ESCC interface capabilities include:

- write data valid setup time to falling edge of $\overline{WR}$ requirement eliminated
- reduced $\overline{INT}$ response time
- reduced access recovery time (t_{RC}) to 3 PCLK best case (3 1/2 PCLK worst case)
- improved $\overline{Wait}$ timing
- write registers WR3, WR4, WR5, and WR10 made readable
- lower priority interrupt masking without $\overline{INTACK}$
- complete SDLC/HDLC CRC character reception
- Sleep mode feature saves all ESCC registers

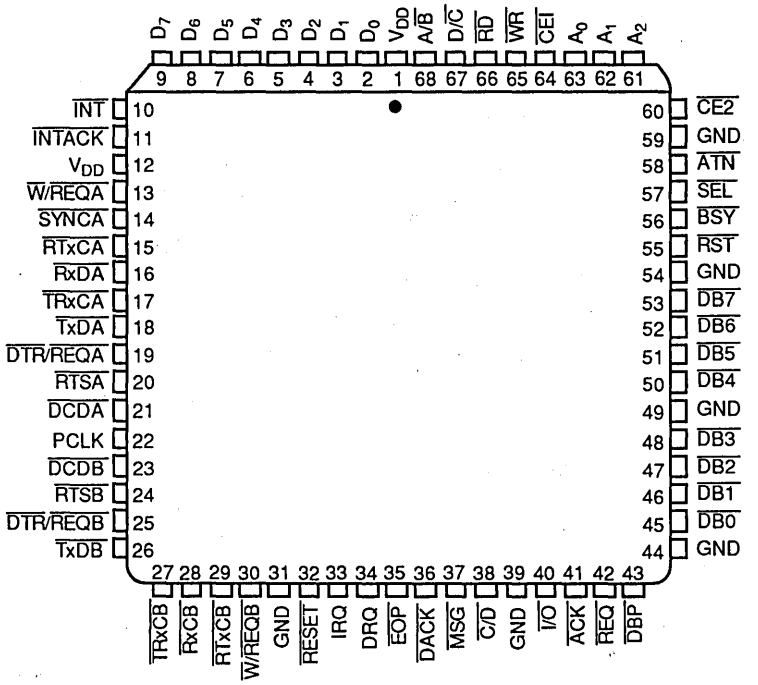
SCSI

The Small Computer Systems Interface (SCSI) Interface Controller is a CMOS device designed to accommodate the SCSI as defined by the ANSI X3T9.2 committee. The Am85C80 operates in both the Initiator and Target roles and can, therefore, be used in host adaptor, host port, disk drive, and formatter designs. This device supports Arbitration, including Reselection. Special high-current open-collector output drivers, capable of sinking 48 mA at 0.5 V, allow for direct connection to the SCSI Bus.

The Am85C80 communicates with the system microprocessor as a peripheral device. The chip is controlled by reading and writing several internal registers which may be addressed as standard or memory-mapped I/O. Minimal processor intervention is required for DMA transfers because the Am85C80 controls the necessary handshake signals. The Am85C80 interrupts the CPU when it detects a bus condition that requires attention. Normal and Block mode DMA is provided to match many popular DMA controllers.

CONNECTION DIAGRAM
Top View

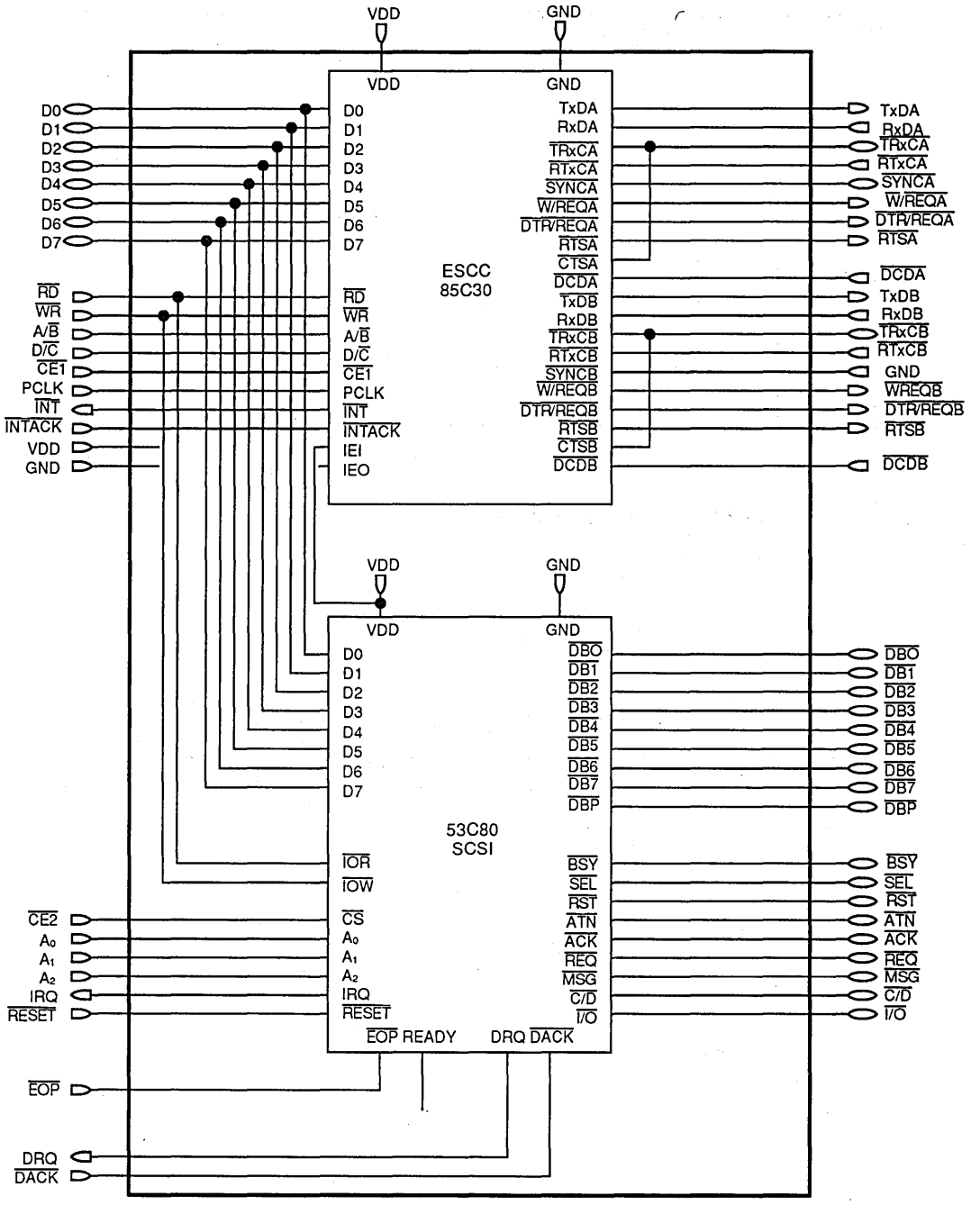
PLCC



Note:
Pin 1 is marked for orientation.

12582C-097A

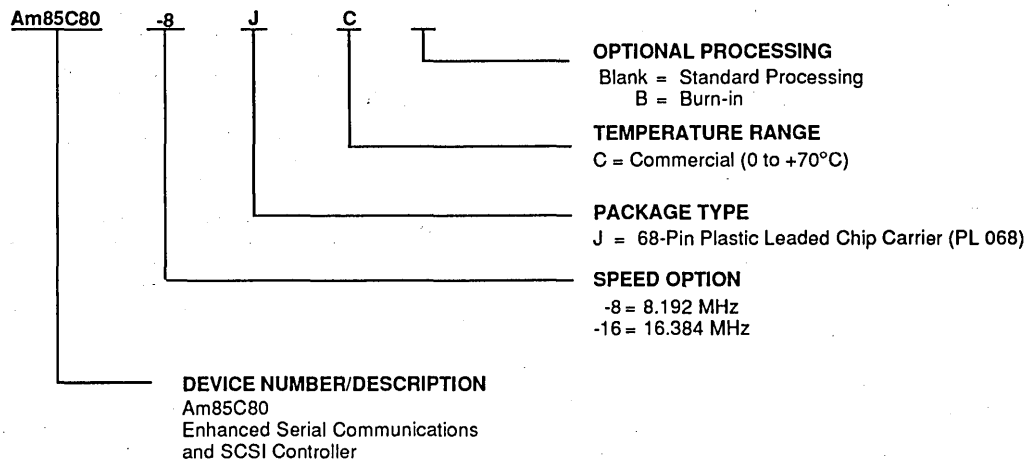
CONNECTION DIAGRAM
Detailed Internal



12582C-098B

ORDERING INFORMATION
Commodity Products

AMD commodity products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am85C80-8 Am85C80-16	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

ESCC

$\overline{RTxCA}$, $\overline{RTxCB}$

Receive/Transmit Clocks (Inputs; Active Low)

These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the digital phase-locked loop. $\overline{RTxCA}$ can also be programmed for use with the $\overline{SYNCA}$ pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

$\overline{TRxCA}$, $\overline{TRxCB}$

Transmit/Receive Clocks (Inputs/Outputs; Active Low)

These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

Channel Controls for Modem, DMA, or Other

$\overline{DCDA}$, $\overline{DCDB}$

Data Carrier Detect (Inputs; Active Low)

These pins function as receiver enables if they are programmed as Auto Enables; otherwise, they may be used as general-purpose input pins. Both are Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects pulses on these pins and may interrupt the CPU on both logic level transitions.

$\overline{DTR}/\overline{REQA}$, $\overline{DTR}/\overline{REQB}$

Data Terminal Ready/Request (Outputs; Active Low)

These outputs follow the inverted state programmed into the DTR bit in WR5. They can also be used as general-purpose outputs or as Request Lines for a DMA controller.

$\overline{RTSA}$, $\overline{RTSB}$

Request to Send (Outputs; Active Low)

When the Request to Send RTS bit in Write Register 5 is set, the $\overline{RTS}$ signal goes Low. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In SYNC mode or in asynchronous mode with Auto Enable off, the $\overline{RTS}$ pins strictly follow the inverted state of the RTS bit. Both pins can be used as general-purpose outputs.

$\overline{SYNCA}$

Synchronization (Input/Output; Active Low)

This pin can act either as input, output, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), this pin is input similar to $\overline{DCD}$. In this mode, transitions on this line affect the state of the Sync/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, this line also acts as an input. In this mode, $\overline{SYNCA}$ must be driven Low two receive clock cycles after the last bit in the SYNC character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNCA}$.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, this pin acts as an output and is active only during the part of the receive clock cycle in which SYNC characters are recognized. The SYNC condition is not latched, so this output is active each time a SYNC pattern is recognized (regardless of character boundaries). In SDLC mode, this pin acts as an output and is valid on receipt of a flag.

$\overline{W}/\overline{REQA}$, $\overline{W}/\overline{REQB}$

Wait/Request (Outputs; Open drain when programmed for a Wait function, driven High or Low when programmed for a Request function)

These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the ESCC data rate. The reset state is Wait.

Control

A/$\overline{B}$

Channel A/Channel B Select (Input)

This signal selects the channel in which the read or write operation occurs.

$\overline{CE1}$

Chip Enable (Input; Active Low)

This signal selects the ESCC for a read or write operation.

D/$\overline{C}$

Data/Control Select (Input)

This signal defines the type of information transferred to or from the ESCC. A High means data is transferred; a Low indicates a command is transferred.

PIN DESCRIPTION (continued)

Interrupt

$\overline{INT}$
Interrupt Request (Output; Active Low, Open Drain)

This signal is activated when the ESCC requests an interrupt.

$\overline{INTACK}$
Interrupt Acknowledge (Input; Active Low)

This signal indicates an active interrupt acknowledge cycle. When $\overline{RD}$ becomes active, the ESCC places an interrupt vector on the data bus. $\overline{INTACK}$ is latched by the rising edge of PCLK.

Serial Data

RxDa, RxDB
Receive Data (Inputs; Active High)

These input signals receive serial data at standard TTL levels.

TxDA, TxDB
Transmit Data (Outputs; Active High)

These output signals transmit serial data at standard TTL levels.

Miscellaneous

GND
Ground

VDD
+5 Volts

PCLK
Clock (Input)

This is the master ESCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock. PCLK is a TTL-level signal. Maximum transmit rate is 1/4 PCLK.

PIN DESCRIPTION (Continued)

SCSI

Microprocessor Interface Signals

A_0–A_2
Address Lines (Input)

These signals are used with $\overline{CE2}$, $\overline{RD}$ or $\overline{WR}$ to address all internal registers.

$\overline{CE2}$
Chip Enable (Input, Active Low)

$\overline{CE2}$ enables a read or write of the SCSI controller internal register selected by A_0–A_2.

$\overline{DACK}$
DMA Acknowledge (Input, Active Low)

$\overline{DACK}$ resets DRQ and selects the data register for input or output data transfers.

DRQ
DMA Request (Output)

DRQ indicates that the data register is ready to be read or written. DRQ occurs only if DMA mode is TRUE in the Command Register. DRQ is cleared by $\overline{DACK}$.

$\overline{EOP}$
End of Process (Input, Active Low)

$\overline{EOP}$ is used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred, but no additional bytes will be requested.

IRQ
Interrupt Request (Output)

IRQ alerts a microprocessor of an error condition or an event completion.

$\overline{RESET}$
Reset (Input, Active Low)

$\overline{RESET}$ clears all the SCSI controller registers. It does not force the SCSI $\overline{RST}$ signal to the active state.

SCSI Interface Signals

The following signals are all bidirectional, active-Low, open-collector signals. With 48-mA sink capability, all pins interface directly with the SCSI Bus.

$\overline{ACK}$
Acknowledge (Input/Output; Open Collector, Active Low)

Driven by an Initiator, $\overline{ACK}$ indicates an acknowledgment for a $\overline{REQ}$/$\overline{ACK}$ data-transfer handshake. In the Target role, $\overline{ACK}$ is received as a response to the $\overline{REQ}$ signal.

$\overline{ATN}$
Attention (Input/Output; Open Collector, Active Low)

Driven by an Initiator, $\overline{ATN}$ indicates an Attention condition. This signal is received in the Target role.

$\overline{BSY}$
Busy (Input/Output; Open Collector, Active Low)

This signal indicates that the SCSI Bus is being used and can be driven by both the Initiator and the Target device.

$\overline{C/D}$
Control/Data (Input/Output; Open Collector, Active Low)

A signal driven by the Target, $\overline{C/D}$ indicates Control or Data information is on the Data Bus. This signal is received by the Initiator.

$\overline{I/O}$
Input/Output (Input/Output; Open Collector, Active Low)

$\overline{I/O}$ is a signal driven by a Target which controls the direction of data movement on the SCSI Bus. TRUE indicates input to the intitiator. This signal is also used to distinguish between Selection and Reselection phases.

$\overline{MSG}$
Message (Input/Output; Open Collector, Active Low)

$\overline{MSG}$ is a signal driven by the Target during the Message phase. This signal is received by the Initiator.

$\overline{REQ}$
Request (Input/Output; Open Collector, Active Low)

Driven by a Target, $\overline{REQ}$ indicates a request for a $\overline{REQ}$/$\overline{ACK}$ data-transfer handshake. This signal is received by the Initiator.

$\overline{RST}$
SCSI Bus RESET (Input/Output; Open Collector, Active Low)

The $\overline{RST}$ Signal indicates an SCSI Bus RESET condition. An internal 30 µA pull up transistor is built-in to prevent spurious interrupts.

$\overline{DB_0}$-$\overline{DB_7}$, $\overline{DBP}$
Data Bits, Parity Bit (Input/Output; Open Collector, Active Low)

These eight data bits ($\overline{DB_0}$-$\overline{DB_7}$), plus a parity bit ($\overline{DBP}$) form the Data Bus. $\overline{DB7}$ is the most significant bit (MSB) and has the highest priority during the Arbitration phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during Arbitration.

$\overline{SEL}$
Select (Input/Output; Open Collector, Active Low)

$\overline{SEL}$ is used by an Initiator to select a Target, or by a Target to reselect an Initiator.

PIN DESCRIPTION (continued)

Common CPU Interface Signals

$\overline{RD}$

Read (Input; Active Low)

This signal indicates a read operation and when Am85C80 is selected, enables the Data Bus Drivers. During the interrupt acknowledge cycle for ESCC, this signal gates the interrupt vector onto the bus if the ESCC is the highest priority device requesting an interrupt. It also selects the SCSI input data register when used with $\overline{DACK}$.

$\overline{WR}$

Write (Input; Active Low)

When Am85C80 is selected, along with either $\overline{CE1}$ or $\overline{CE2}$, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset for ESCC. It also selects the SCSI output data register when used with $\overline{DACK}$.

D_0–D_7

Data (Input/Output; Active High)

Common data lines for ESCC and SCSI. These lines transfer data into and out of the Am85C80.

SCSI FUNCTIONAL DESCRIPTION

General

The Small Computer Systems Interface (SCSI) device appears as a set of eight registers to the controlling CPU. By reading and writing the appropriate registers, the CPU may initiate any SCSI Bus activity or may sample and assert any signal on the SCSI Bus. This allows the user to implement all or portions of the SCSI protocol in software. These registers are read (written) by activating $\overline{CE2}$ with an address on A_0–A_2 and then issuing an $\overline{RD}$ ($\overline{WR}$) pulse. This section describes the operation of the internal registers.

Table 1. Register Summary

Address				
A_2	A_1	A_0	R/W	Register Name
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	R/W	Initiator Command
0	1	0	R/W	Mode
0	1	1	R/W	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupts
1	1	1	W	Start DMA Initiator Receive

Data Registers

The data registers are used to transfer SCSI commands, data, status, and message bytes between the microprocessor Data Bus and the SCSI Bus. The Am85C80 does not interpret any information that passes through the data registers. The data registers consist of the transparent Current SCSI Data Register, the Output Data Register, and the Input Data Register. User note: a one in a register means the pin is Low. For example, when the $\overline{ATN}$ Pin is Low, $\overline{ATN}$ in the bus and status register will be High.

Current SCSI Data Register—Address 0 (Read Only)

The Current SCSI Data Register is a read-only register that allows the microprocessor to read the active SCSI Data Bus. This is accomplished by activating $\overline{CE2}$ with an address on A_2–A_0 of 000 and issuing an $\overline{RD}$ pulse. If parity checking is enabled, the SCSI Bus parity is checked at the beginning of the read cycle. This register is used during a programmed I/O data read or during Arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during Arbitration.

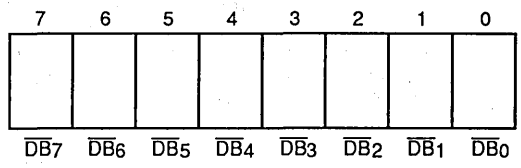


Figure 1. Current SCSI Data Register

Output Data Register—Address 0 (Write Only)

The Output Data Register is a write-only register that is used to send data to the SCSI Bus. This is accomplished by either using a normal CPU write, or under DMA control, by using $\overline{WR}$ and $\overline{DACK}$. This register is also used to assert the proper ID bits or the SCSI Bus during the Arbitration and Selection phases.

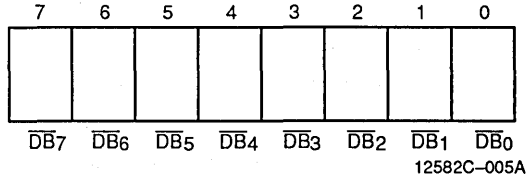


Figure 2. Output Data Register

Input Data Register—Address 6 (Read Only)

The Input Data Register is a read-only register that is used to read latched data from the SCSI Bus. Data is latched either during a DMA Target receive operation when $\overline{ACK}$ goes active or during a DMA Initiator receive when $\overline{REQ}$ goes active. The DMA Mode bit (port 2, bit 1) must be set before data can be latched in the Input Data Register. This register may be read under DMA control using $\overline{RD}$ and $\overline{DACK}$. Parity is optionally checked when the Input Data Register is loaded.

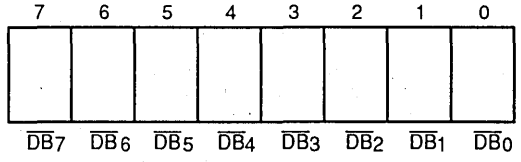


Figure 3. Input Data Register

Initiator Command Register—Address 1 (Read/Write)

The Initiator Command Register is a read/write register that is used to assert certain SCSI Bus signals, to monitor those signals, and to monitor the progress of bus arbitration. Many of these bits are significant only when being used as Initiators; however, most can be used during Target role operation.

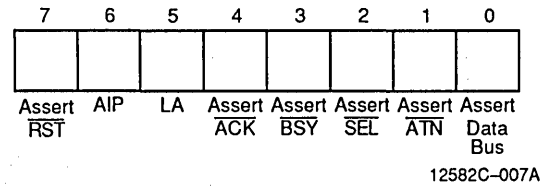


Figure 4-1. Initiator Command Register—Register Read

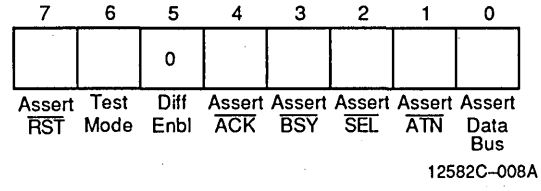


Figure 4-2. Initiator Command Register—Register Write

The following describes the operation of all bits in the Initiator Command Register.

Bit 7—Assert RST

Whenever a one is written to bit 7 of the Initiator Command Register, the RST signal is asserted on the SCSI Bus. The RST signal will remain asserted until this bit is reset or until an external RESET occurs. After this bit is set (1), IRQ goes active and all internal logic and control registers are reset (except for the interrupt latch and the Assert RST bit). Writing a zero to bit 7 of the Initiator Command Register de-asserts the RST signal. Reading this register simply reflects the status of this bit.

Bit 6—AIP (Arbitration In Progress) (Read Bit)

This bit is used to determine if Arbitration is in progress. For this bit to be active, the Arbitrate bit (port 2, bit 0) must have been set previously. It indicates that a Bus-Free condition has been detected and that the chip has asserted BSY and the contents of the Output Data Register (port 0) onto the SCSI Bus. AIP will remain active until the Arbitrate bit is reset.

Bit 6—Test Mode (Write Bit)

This bit may be written during a test environment to disable all output drivers, effectively removing the Am85C80 from the circuit. Resetting this bit returns the part to normal operation.

Bit 5—LA (Lost Arbitration) (Read Bit)

This bit, when active, indicates that the Am85C80 detected a Bus-Free condition, arbitrated for use of the bus by asserting BSY and its ID on the Data Bus, and lost Arbitration due to SEL being asserted by another bus device. For this bit to be active, the Arbitrate bit (port 2, bit 0) must be active.

Bit 5—Diff Enbl (Differential Enable) (Write Bit)

This bit should be written with a zero for proper operation.

Bit 4—Assert ACK

This bit is used by the bus initiator to assert ACK on the SCSI Bus. In order to assert ACK, the Targetmode bit (port 2, bit 6) must be False. Writing a zero to this bit resets ACK on the SCSI Bus. Reading this register simply reflects the status of this bit.

Bit 3—Assert BSY

Writing a one (1) into this bit position asserts BSY onto the SCSI Bus. Conversely, a zero resets the BSY signal. Asserting BSY indicates a successful selection or reselection and resetting this bit creates a Bus-Disconnect condition. Reading this register simply reflects the status of this bit.

Bit 2—Assert SEL

Writing a one (1) into this bit position asserts SEL onto the SCSI Bus. SEL is normally asserted after Arbitration has been successfully completed. SEL may be de-asserted by resetting this bit to a zero. A read of this register simply reflects the status of this bit.

Bit 1—Assert ATN

ATN may be asserted on the SCSI Bus by setting this bit to a one (1) if the Targetmode bit (port 2, bit 6) is False. ATN is normally asserted by the initiator to request a Message Out bus phase. Note that since Assert SEL and Assert ATN are in the same register, a select with ATN may be implemented with one CPU write. ATN may be de-asserted by resetting this bit to zero. A read of this register simply reflects the status of this bit.

Bit 0—Assert Data Bus

The Assert Data Bus bit, when set, allows the contents of the Output Data Register to be enabled as chip outputs on the signals $\overline{DB_0}$–$\overline{DB_7}$. Parity is also generated and asserted on DBP.

When connected as an initiator, the outputs are only enabled if the Targetmode bit (port 2, bit 6) is False, the received signal I/O is False, and the phase signals (C/D, I/O, and MSG) match the contents of the Assert C/D, Assert I/O, and Assert MSG in the Target Command Register.

This bit should also be set during DMA send operations.

Mode Register—Address 2 (Read/Write)

The Mode Register is used to control the operation of the chip. This register determines whether the Am85C80 operates as an Initiator or a Target, whether DMA transfers are being used, whether parity is checked, and whether interrupts are generated on various external conditions. This register may be read to check the value of these

internal control bits. Figure 5 describes the operation of these control bits.

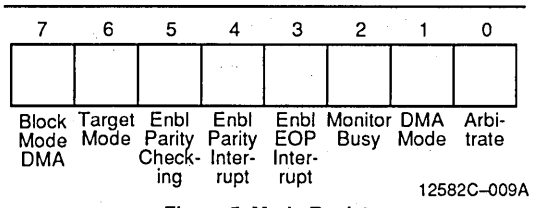


Figure 5. Mode Register

Bit 7—Block Mode DMA

The Block Mode DMA bit controls the characteristics of the DMA DRQ-DACK handshake. When this bit is reset (0) and the DMA Mode bit is active (1), the DMA handshake uses the normal interlocked handshake, and the rising edge of DACK indicates the end of each byte being transferred. In block mode operations, Block Mode DMA bit set (1), and DMA Mode bit set (1), the end of RD or WR signifies the end of each byte transferred and DACK is allowed to remain active throughout the DMA operation. Ready can then be used to request the next transfer.

Bit 6—Target Mode

The Targetmode bit allows the Am85C80 to operate as either an SCSI Bus Initiator, bit reset (0), or as an SCSI Bus Target device, bit set (1). In order for the signals ATN and ACK to be asserted on the SCSI Bus, the Targetmode bit must be reset (0). In order for the signals C/D, I/O, MSG, and REQ to be asserted on the SCSI Bus, the Targetmode bit must be set (1).

Bit 5—Enable Parity Checking

The Enable Parity Checking bit determines whether parity errors will be ignored or saved in the parity error latch. If this bit is reset (0), parity will be ignored. Conversely, if this bit is set (1), parity errors will be saved.

Bit 4—ENABLE PARITY INTERRUPT

The Enable Parity Interrupt bit, when set (1), will cause an interrupt (IRQ) to occur if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking bit (bit 5) is also enabled (1).

Bit 3—Enable EOP Interrupt

The Enable EOP Interrupt bit, when set (1), causes an interrupt to occur when the EOP (End of Process) signal is received from the DMA controller logic.

Bit 2—Monitor Busy

The Monitor Busy bit, when True (1), causes an interrupt to be generated for an unexpected loss of BSY. When the interrupt is generated due to loss of BSY, the lower six bits of the Initiator Command Register are reset (0) and all signals are removed from the SCSI Bus.

Bit 1—DMA Mode

The DMA Mode bit is normally used to enable a DMA transfer and must be set (1) prior to writing ports 5 through 7. Ports 5 through 7 are used to start DMA transfers. The Targetmode bit (port 2, bit 6) must be consistent with writes to port 6 and 7 [i.e., set (1) for a write to port 6 and reset (0) for a write to port 7]. The control bit Assert Data Bus (port 1, bit 0) must be True (1) for all DMA send operations. In the DMA mode, REQ and ACK are automatically controlled.

The DMA Mode bit is not reset upon the receipt of an EOP signal. Any DMA transfer may be stopped by writing a zero into this bit location; however, care must be taken not to cause CE2 and DACK to be active simultaneously.

Bit 0—Arbitrate

The Arbitrate bit is set (1) to start the Arbitration process. Prior to setting this bit, the Output Data Register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI Bus Arbitration. The Am85C80 will wait for a Bus-Free condition before entering the Arbitration phase. The results of the Arbitration phase may be determined by reading the status bits LA and AIP (port 1, bits 5 and 6, respectively).

Target Command Register—Address 3 (Read/Write)

When connected as a target device, the Target Command Register allows the CPU to control the SCSI Bus Information Transfer phase and/or to assert REQ simply by writing this register. The Targetmode bit (port 2, bit 6) must be True (1) for bus assertion to occur. The SCSI Bus phases are described in Table 2.

Table 2. SCSI Information Transfer Phases

Bus Phase	Assert I/O	Assert C/D	Assert MSG
Data Out	0	0	0
Unspecified	0	0	1
Command	0	1	0
Message Out	0	1	1
Data In	1	0	0
Unspecified	1	0	1
Status	1	1	0
Message In	1	1	1

When connected as an Initiator with DMA Mode True, if the phase lines (I/O, C/D, and MSG) do not match the phase bits in the Target Command Register, a phase-mismatch interrupt is generated when REQ goes active. In order to send data as an Initiator, the Assert I/O, Assert C/D, and Assert MSG bits must match the corresponding bits in the Current SCSI Bus Status Register (port 4). The Assert REQ bit (bit 3) has no meaning when operating as an Initiator.

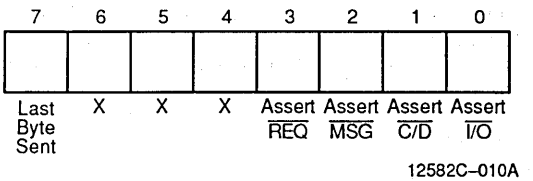


Figure 6. Target Command Register

The Am85C80 uses bit 7 of the SCSI Target Command Register to determine when the last byte of a DMA

transfer is sent to the SCSI bus. This flag is necessary since the end of DMA bit in the Bus and Status Register only indicates when the last byte was received from the DMA.

Current SCSI Bus Status Register—Address 4 (Read Only)

The Current SCSI Bus Status Register is a read-only register that is used to monitor seven SCSI Bus control signals plus the Data Bus parity bit. For example, an Initiator device can use this register to determine the current bus phase and to poll $\overline{REQ}$ for pending data transfers. This register may also be used to determine why a particular interrupt occurred. Figure 7 describes the Current SCSI Bus Status Register.

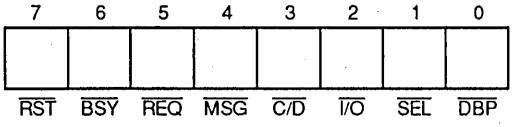


Figure 7. Current SCSI Bus Status Register

The Am85C80 uses bit 7 of this register to determine when the last byte of a DMA transfer is sent to the SCSI bus. This flag is necessary since the end of DMA bit in the Bus and Status Register only reflects when the last byte was received from the DMA.

Select Enable Register—Address 4 (Write Only)

The Select Enable Register is a write-only register which is used as a mask to monitor a signal ID during a selection attempt. The simultaneous occurrence of the correct ID bit, $\overline{BSY}$ False, and $\overline{SEL}$ True will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the Enable Parity Checking bit (port 2, bit 5) is active (1), parity will be checked during selection.

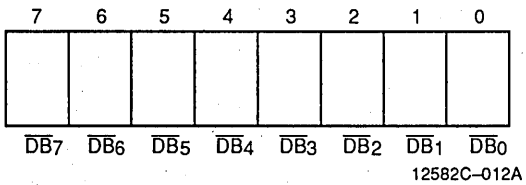


Figure 8. Select Enable Register

Bus and Status Register—Address 5 (Read Only)

The Bus and Status Register is a read-only register that can be used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status Register ($\overline{ATN}$ and $\overline{ACK}$), as well as six other status bits. Individual descriptions of each bit of the Bus and Status Register follow.

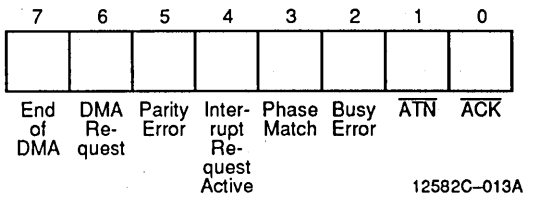


Figure 9. Bus and Status Register

Bit 7—End of DMA Transfer

The End Of DMA Transfer bit is set if $\overline{EOP}$, $\overline{DACK}$, and either $\overline{RD}$ or $\overline{WR}$ are simultaneously active for at least 100 ns. Since the $\overline{EOP}$ signal can occur during the last byte sent to the Output Data Register (port 0), the $\overline{REQ}$ and $\overline{ACK}$ signals should be monitored to ensure that the last byte has been transferred. This bit is reset when the DMA Mode bit is reset (0) in the Mode Register (port 2).

Bit 6—DMA Request

The DMA Request bit allows the CPU to sample the output pin DRQ. DRQ can be cleared by asserting $\overline{DACK}$ or by resetting the DMA Mode bit (bit 1) in the Mode Register (port 2). The DRQ signal does not reset when a phase-mismatch interrupt occurs.

Bit 5—Parity Error

This bit is set if a parity error occurs during a data receive or a device selection. The Parity Error bit can only be set (1) if the Enable Parity Check bit (port 2, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 4—Interrupt Request Active

This bit is set if an enabled interrupt condition occurs. It reflects the current state of the IRQ output and can be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 3—Phase Match

The SCSI signals, $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$, represent the current Information Transfer phase. The Phase Match bit indicates whether the current SCSI Bus phase matches the lower 3 bits of the Target Command Register. Phase Match is continuously updated and is only significant when operating as a Bus Initiator. A phase match is required for data transfers to occur on the SCSI Bus.

Bit 2—Busy Error

The Busy Error bit is active if an unexpected loss of the $\overline{BSY}$ signal has occurred. This latch is set whenever the Monitor Busy bit (port 2, bit 2) is True and $\overline{BSY}$ is False. An unexpected loss of $\overline{BSY}$ will disable any SCSI outputs and will reset the DMA MODE bit (port 2, bit 1).

Bit 1—$\overline{ATN}$

This bit reflects the condition of the SCSI Bus control signal $\overline{ATN}$. This signal is normally monitored by the Target device.

Bit 0—$\overline{ACK}$

This bit reflects the condition of the SCSI Bus control signal $\overline{ACK}$. This signal is normally monitored by the Target device.

DMA Registers

Three write-only registers are used to initiate all DMA activity. They are Start DMA Send (port 5), Start DMA Target Receive (port 6), and Start DMA Initiator Receive (port 7). Simply writing these registers starts the DMA transfers. Data presented to the Am85C80 on signals D_0–D_7 during the register write is meaningless and has no effect on the operation. Prior to writing these registers, the Block Mode DMA bit (bit 7), the DMA Mode bit (bit 1) and the Targetmode bit (bit 6) in the Mode Register (port 2) must be appropriately set. The individual registers are briefly described as follows.

Start DMA Send—Address 5 (Write Only)

This register is written to initiate a DMA send, from the DMA to the SCSI Bus, for either Initiator or Target role operations. The DMA Mode bit (port 2, bit 1) must be set prior to writing this register.

Start DMA Target Receive—Address 6 (Write Only)

This register is written to initiate a DMA receive—from the SCSI Bus to the DMA—for Target operation only. The DMA Mode bit (bit 1) and the Targetmode bit (bit 6) in the Mode Register (port 2) must both be set (1) prior to writing this register.

Start DMA Initiator Receive—Address 7 (Write Only)

This register is written to initiate a DMA receive—from the SCSI Bus to the DMA, for Initiator operation only. The DMA Mode bit (bit 6) must be False (0) in the Mode Register (port 2) prior to writing this register.

Reset Parity/Interrupt—Address 7 (Read Only)

Reading this register resets the Parity Error bit (bit 5), the Interrupt Request bit (bit 4), and the Busy Error bit (bit 2) in the Bus and Status Register (port 5).

On-Chip SCSI Hardware Support

The Am85C80 is easy to use because of its simple architecture. The chip allows direct control and monitoring of the SCSI Bus by providing a latch for each signal. However, portions of the protocol define timings that are much too quick for traditional microprocessors to control. Therefore, hardware support has been provided for DMA transfers, bus arbitration, phase-change monitoring, bus disconnection, bus reset, parity generation, parity checking, and device selection/reselection.

Arbitration is accomplished using a Bus-Free filter to continuously monitor $\overline{BSY}$. If $\overline{BSY}$ remains inactive for at least 400 ns, then the SCSI Bus is considered free and Arbitration may begin. Arbitration will begin if the bus is free, $\overline{SEL}$ is inactive, and the Arbitration bit (port 2, bit 0) is active. Once arbitration has begun ($\overline{BSY}$ asserted), an arbitration delay of 2.2 µs must elapse before the Data Bus can be examined to determine if Arbitration has been won. This delay must be implemented in the controlling software driver.

The Am85C80 has no clock. Delays such as bus-free delay, bus-set delay, and bus-settle delay are implemented using gate delays. These delays may differ between devices because of inherent process variations, but are well within the proposed ANSI X3T9.2 specification.

Interrupts

The Am85C80 provides an interrupt output (IRQ) to indicate a task completion or an abnormal bus occurrence. The use of interrupts is optional and may be disabled by resetting the appropriate bits in the Mode Register (port 2) or the Select Enable Register (port 4).

When an interrupt occurs, the Bus and Status Register and the Current SCSI Bus Status Register must be read to determine which condition created the interrupt. IRQ can be reset simply by reading the Reset Parity/Interrupt Register (port 7) or by an external chip reset ($\overline{RESET}$ active for 100 ns).

Assuming the Am85C80 has been properly initialized, an interrupt will be generated if the chip is selected or reselected, if an $\overline{EOP}$ signal occurs during a DMA transfer, if a SCSI Bus reset occurs, if a parity error occurs during a data transfer, if a bus phase mismatch occurs, or if a SCSI Bus disconnection occurs.

Selection/Reselection

The Am85C80 can generate a select interrupt if $\overline{SEL}$ is True (1), its device ID is True (1), and $\overline{BSY}$ is False for at least a bus-settle delay (400 ns). If $\overline{I/O}$ is active, this should be considered a reselect interrupt. The correct ID bit is determined by a match in the Select Enable Register (port 4). Only a single bit match is required to generate an interrupt. This interrupt may be disabled by writing zeros into all bits of the Select Enable Register.

If parity is supported, parity should also be good during the selection phase. Therefore, if the Enable Parity bit (port 2, bit 5) is active, then the Parity Error bit should be checked to ensure that a proper selection has occurred. The Enable Parity Interrupt bit need not be set for this interrupt to be generated.

The proposed SCSI specification also requires that no more than two device IDs be active during the selection process. To ensure this, the Current SCSI Data Register (port 0) should be read.

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for Selection/Reselection interrupt are displayed in Figures 10 and 11, respectively.

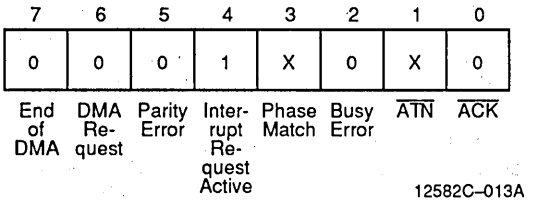


Figure 10. Condition of Bus and Status Register for Select Interrupt to Occur

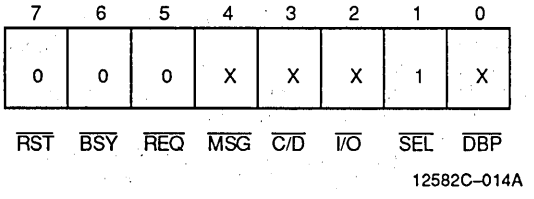


Figure 11. Condition of Current SCSI Bus Status Register for Select Interrupt to Occur

End of Process (EOP) Interrupt

An End of Process signal ($\overline{EOP}$) that occurs during a DMA transfer (DMA Mode True) will set the End Of DMA Status bit (port 5, bit 7) and will optionally generate an interrupt if the Enable $\overline{EOP}$ Interrupt bit (port 2, bit 3) is True. The $\overline{EOP}$ pulse will not be recognized (End Of DMA bit set) unless $\overline{EOP}$, $\overline{DACK}$, and either $\overline{RD}$ or $\overline{WR}$ are concurrently active for at least 100 ns. DMA transfers can still occur if $\overline{EOP}$ was not asserted at the correct time. This interrupt can be disabled by resetting the Enable $\overline{EOP}$ Interrupt bit (port 2, bit 3).

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for this interrupt are shown in Figures 12 and 13, respectively.

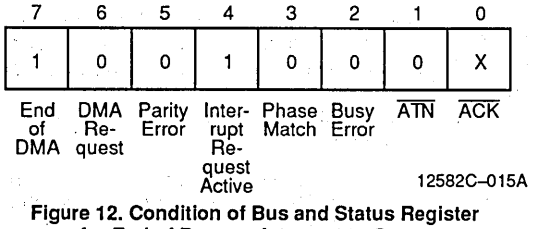


Figure 12. Condition of Bus and Status Register for End of Process Interrupt to Occur

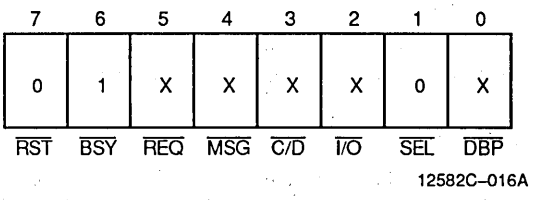


Figure 13. Condition of Current SCSI Bus Status Register for End of Process Interrupt to Occur

The End Of DMA bit (port 5, bit 7) is used to determine when a block transfer is complete. Receive operations are complete when there are no data left in the chip and no additional handshakes occurring. The only exception to this is receiving data as an Initiator when the Target opts to send additional data for the same phase. In this case, $\overline{REQ}$ goes active and the new data is present in the Input Data Register (port 6). Since a phase-mismatch interrupt will not occur, $\overline{REQ}$ and $\overline{ACK}$ need to be sampled to determine that the Target is attempting to send more data.

For send operations, the End Of DMA bit (port 5, bit 7) is set when the DMA finishes its transfer, but the SCSI transfer may still be in progress. If connected as a Target, $\overline{REQ}$ and $\overline{ACK}$ should be sampled until both are False. If connected as an Initiator, a phase change interrupt can be used to signal the completion of the previous phase. It is possible for the Target to request additional data for the same phase. In this case, a phase change will not occur and both $\overline{REQ}$ and $\overline{ACK}$ must be sampled to determine when the last byte was transferred.

SCSI Bus Reset

The Am85C80 generates an interrupt when the $\overline{RST}$ signal transitions to True. The device releases all bus signals within a bus-clear delay (800 ns) of this transition. This interrupt also occurs after setting the Assert $\overline{RST}$ bit (port 1, bit 7). This interrupt cannot be disabled. (Note: $\overline{RST}$ is not latched in bit 7 of the Current SCSI Bus Status Register (port 4) and may not be active when this port is read. For this case, the Bus Reset interrupt may be determined by default.)

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for this interrupt are displayed in Figures 14 and 15, respectively.

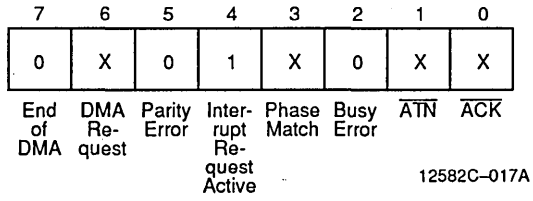


Figure 14. Condition of Bus and Status Register for SCSI Bus Reset to Occur

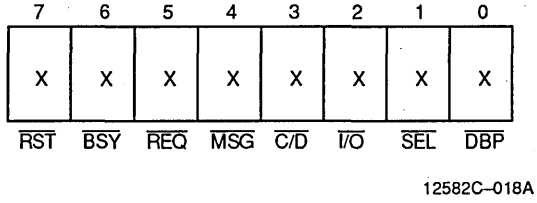


Figure 15. Condition of Current SCSI Bus Status Register for SCSI Bus Reset to Occur

Parity Error

An interrupt is generated for a received parity error if the Enable Parity Check (bit 5) and the Enable Parity Interrupt (bit 4) bits are set (1) in the Mode Register (port 2). Parity is checked during a read of the Current SCSI Data Register (port 0) and during a DMA receive operation. A parity error can be detected without generating an interrupt by disabling the Enable Parity Interrupt bit (port 2, bit 4) and checking the Parity Error flag (port 5, bit 5).

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for Parity Error interrupt are displayed in Figures 16 and 17, respectively.

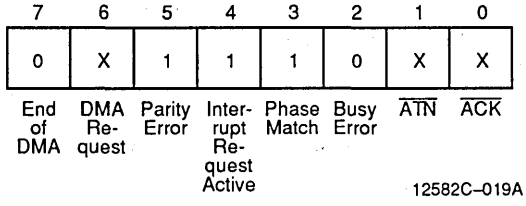


Figure 16. Condition of Bus and Status Register for Parity Error Interrupt to Occur

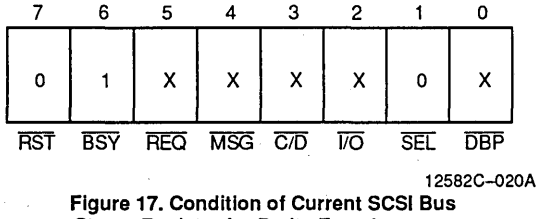


Figure 17. Condition of Current SCSI Bus Status Register for Parity Error Interrupt to Occur

Bus Phase Mismatch

The SCSI phase lines are composed of the signals $\overline{I/O}$, $\overline{C/D}$, and $\overline{MSG}$. These signals are compared with the corresponding bits in the Target Command Register: Assert $\overline{I/O}$ (bit 0), Assert $\overline{C/D}$ (bit 1), and Assert $\overline{MSG}$ (bit 2). The comparison occurs continually and is reflected in the Phase Match bit (bit 3) of the Bus and Status Register (port 5). If the DMA Mode bit (port 2, bit 1) is active and a phase mismatch occurs when $\overline{REQ}$ changes from False to True, an interrupt (IRQ) is generated.

A phase mismatch prevents the recognition of $\overline{REQ}$ and removes the chip from the bus during an initiator send operation [$\overline{DB_0}$–$\overline{DB_7}$ and $\overline{DBP}$ will not be driven even though the Assert Data Bus bit (port 1, bit 0) is active]. This interrupt is only significant when connected as an initiator and may be disabled by resetting the DMA Mode bit. (Note: It is possible for this interrupt to occur when connected as a Target if another device is driving the phase lines to a different state.)

The proper values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for Bus Phase Mismatch interrupt to occur are displayed in Figures 18 and 19, respectively.

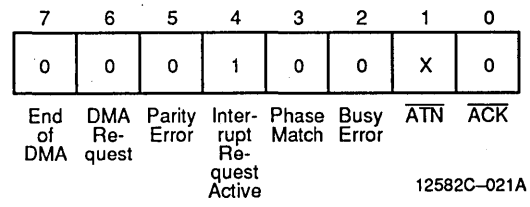


Figure 18. Condition of Bus and Status Register for Bus Phase Mismatch Interrupt to Occur

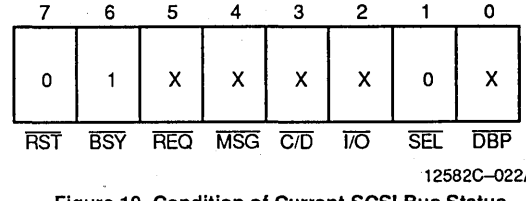


Figure 19. Condition of Current SCSI Bus Status Register for Bus Phase Mismatch Interrupt to Occur

Loss of $\overline{BSY}$

If the Monitor Busy bit (bit 2) in the Mode Register (port 2) is active, an interrupt will be generated if the $\overline{BSY}$ signal goes False for at least a bus-settle delay (400 ns). This interrupt may be disabled by resetting the Monitor Busy bit. Register values are displayed in Figures 20 and 21.

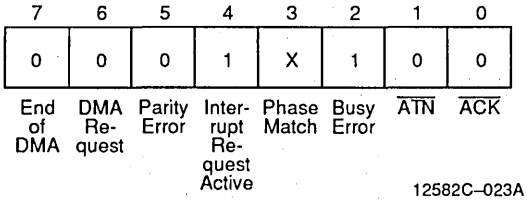


Figure 20. Bus and Status Register

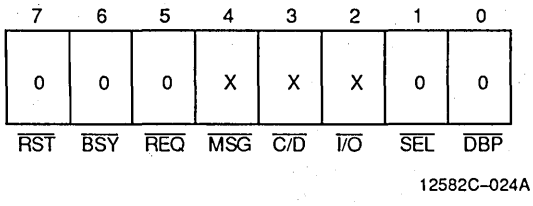


Figure 21. Current SCSI Bus Status Register

Reset Conditions

Three possible reset situations exist with the Am85C80.

Hardware Chip Reset

When the signal $\overline{RST}$ is active for at least 200 ns, the SCSI device is re-initialized and all internal logic and control registers of SCSI are cleared. This is a chip reset only and does not create an SCSI Bus-Reset condition.

SCSI Bus Reset ($\overline{RST}$) Received

When an SCSI $\overline{RST}$ signal is received, an IRQ interrupt is generated and a SCSI chip reset is performed. All internal logic and registers are cleared, except for the IRQ interrupt latch and the Assert $\overline{RST}$ bit (bit 7) in the Initiator Command Register (port 1). (Note: The $\overline{RST}$ signal may be sampled by reading the Current SCSI Bus Status Register (port 4); however, this signal is not latched and may not be present when this port is read.)

SCSI Bus Reset ($\overline{RST}$) Issued

If the CPU sets the Assert $\overline{RST}$ bit (bit 7) in the Initiator Command Register (port 1), the $\overline{RST}$ signal goes active on the SCSI Bus and an internal reset is performed. Again, all internal logic and registers are cleared except for the IRQ interrupt latch and the Assert $\overline{RST}$ bit (bit 7) in the Initiator Command Register (port 1). The $\overline{RST}$ signal will continue to be active until the Assert $\overline{RST}$ bit is reset or until a hardware reset occurs.

Data Transfers

Data may be transferred between SCSI Bus devices in one of four modes: (1) Programmed I/O, (2) Normal DMA, (3) Block Mode DMA, or (4) Pseudo DMA. The following sections describe these modes in detail. (Note: For all data transfer operations, $\overline{DACK}$ and $\overline{CE2}$ should never be active simultaneously.)

Programmed I/O Transfers

Programmed I/O is the most primitive form of data transfer. The $\overline{REQ}$ and $\overline{ACK}$ handshake signals are individually monitored and asserted by reading and writing the appropriate register bits. This type of transfer is normally used when transferring small blocks of data, such as command blocks or message and status bytes.

An Initiator send operation would begin by setting the $\overline{C/D}$, $\overline{I/O}$, and $\overline{MSG}$ bits in the Target Command Register to the correct state so that a phase match exists. In addition to the phase match condition, it is necessary for the Assert Data Bus bit (port 1, bit 0) to be True and the received I/O signal to be False for the Am85C80 to send data.

For each transfer, the data is loaded into the Output Data Register (port 0). The CPU then waits for the $\overline{REQ}$ bit (port 4, bit 5) to become active. Once $\overline{REQ}$ goes active, the Phase Match bit (port 5, bit 3) is checked and the Assert $\overline{ACK}$ bit (port 1, bit 4) is set. The $\overline{REQ}$ bit is sampled until it becomes False and the CPU resets the Assert $\overline{ACK}$ bit to complete the transfer.

Normal DMA Mode

DMA transfers are normally used for large block transfers. The SCSI chip outputs a DMA request (DRQ) whenever it is ready for a byte transfer. External DMA logic uses this DRQ signal to generate $\overline{DACK}$ and an $\overline{RD}$ or an $\overline{WR}$ pulse to the Am85C80. DRQ goes inactive when $\overline{DACK}$ is asserted, and $\overline{DACK}$ goes inactive some time after the minimum read or write pulse width. This process is repeated for every byte. For this mode, $\overline{DACK}$ should not be allowed to cycle unless a transfer is taking place.

Block Mode DMA

Some popular DMA controllers such as the Am9517A provide a Block Mode DMA transfer. This type of transfer allows the DMA controller to transfer blocks of data without relinquishing the use of the Data Bus to the CPU after each byte is transferred; thus, faster transfer rates are achieved by eliminating the repetitive access and release of the CPU Bus.

If the Block Mode DMA bit (port 2, bit 7) is active, the Am85C80 will begin the transfer by asserting DRQ. The DMA controller then asserts $\overline{DACK}$ for the remainder of the block transfer. DRQ goes inactive for the duration of the transfer.

Non-Block Mode DMA transfers end when $\overline{DACK}$ goes False, whereas Block mode transfers end when $\overline{RD}$ or $\overline{WR}$ becomes inactive. Since this is the case, DMA transfers may be started sooner in a Block Mode transfer.

The methods described under "Halting a DMA Operation" apply for all DMA operations.

Pseudo DMA Mode

To avoid the tedium of monitoring and asserting the request/acknowledge handshake signals for programmed I/O transfers, the system may be designed to implement a pseudo DMA mode. This mode is implemented by programming the Am85C80 to operate in the DMA mode, but using the CPU to emulate the DMA handshake. DRQ may be detected by polling the DMA Request bit (bit 6) in the Bus and Status Register (port 5), by sampling the signal through an external port, or by using it to generate a CPU interrupt. Once DRQ is detected, the CPU can perform a read or write data transfer. This CPU read/write is externally decoded to generate the appropriate $\overline{DACK}$ and $\overline{RD}$ or $\overline{WR}$ signals.

Often, external decoding logic is necessary to generate the Am85C80 $\overline{CE2}$ signal. This same logic may be used to generate $\overline{DACK}$ at no extra system cost and provide an increased performance in programmed I/O transfers.

Halting a DMA Operation

The $\overline{EOP}$ signal is not the only way to halt a DMA transfer. A bus phase mismatch or a reset of the DMA Mode bit (port 2, bit 1) can also terminate a DMA cycle for the current bus phase.

Using the $\overline{EOP}$ Signal

If $\overline{EOP}$ is used, it should be asserted for at least 100 ns while $\overline{DACK}$ and $\overline{RD}$ or $\overline{WR}$ are simultaneously active. Note, however, that if $\overline{RD}$ or $\overline{WR}$ is not active an interrupt will be generated, but the DMA activity will continue. The $\overline{EOP}$ signal does not reset the DMA Mode bit. Since the $\overline{EOP}$ signal can occur during the last byte sent to the Output Data Register (port 0), the $\overline{REQ}$ and $\overline{ACK}$ signals should be monitored to ensure that the last byte has transferred.

Bus Phase Mismatch Interrupt

A bus phase mismatch interrupt may be used to halt the transfer if operating as an Initiator. Using this method frees the host from maintaining a data length counter and frees the DMA logic from providing the $\overline{EOP}$ signal. If performing an Initiator send operation, the Am85C80 requires $\overline{DACK}$ to cycle before $\overline{ACK}$ goes inactive. Since phase changes cannot occur if $\overline{ACK}$ is active, either $\overline{DACK}$ must be cycled after the last byte is sent or the DMA Mode bit must be reset in order to receive the phase mismatch interrupt.

Resetting the DMA Mode Bit

A DMA operation may be halted at any time simply by resetting the DMA Mode bit. It is recommended that the DMA Mode bit be reset after receiving an $\overline{EOP}$ or bus phase-mismatch interrupt. The DMA Mode bit must then be set before writing any of the start DMA registers for subsequent bus phases.

If resetting the DMA Mode bit is used instead of $\overline{EOP}$ for Target role operation, then care must be taken to reset this bit at the proper time. If receiving data as a Target device, the DMA Mode bit must be reset once the last DRQ is received and before $\overline{DACK}$ is asserted to prevent an additional $\overline{REQ}$ from occurring. Resetting this bit causes DRQ to go inactive. However, the last byte received remains in the Input Data Register and may be obtained either by performing a normal CPU read or by cycling $\overline{DACK}$ and $\overline{RD}$. In most cases $\overline{EOP}$ is easier to use when operating as a Target device.

Flowcharts

Flowcharts are provided (see Figures 22 through 25) as a guideline to facilitate your firmware development. Firmware will vary depending on the application and the level of the SCSI protocol being supported.

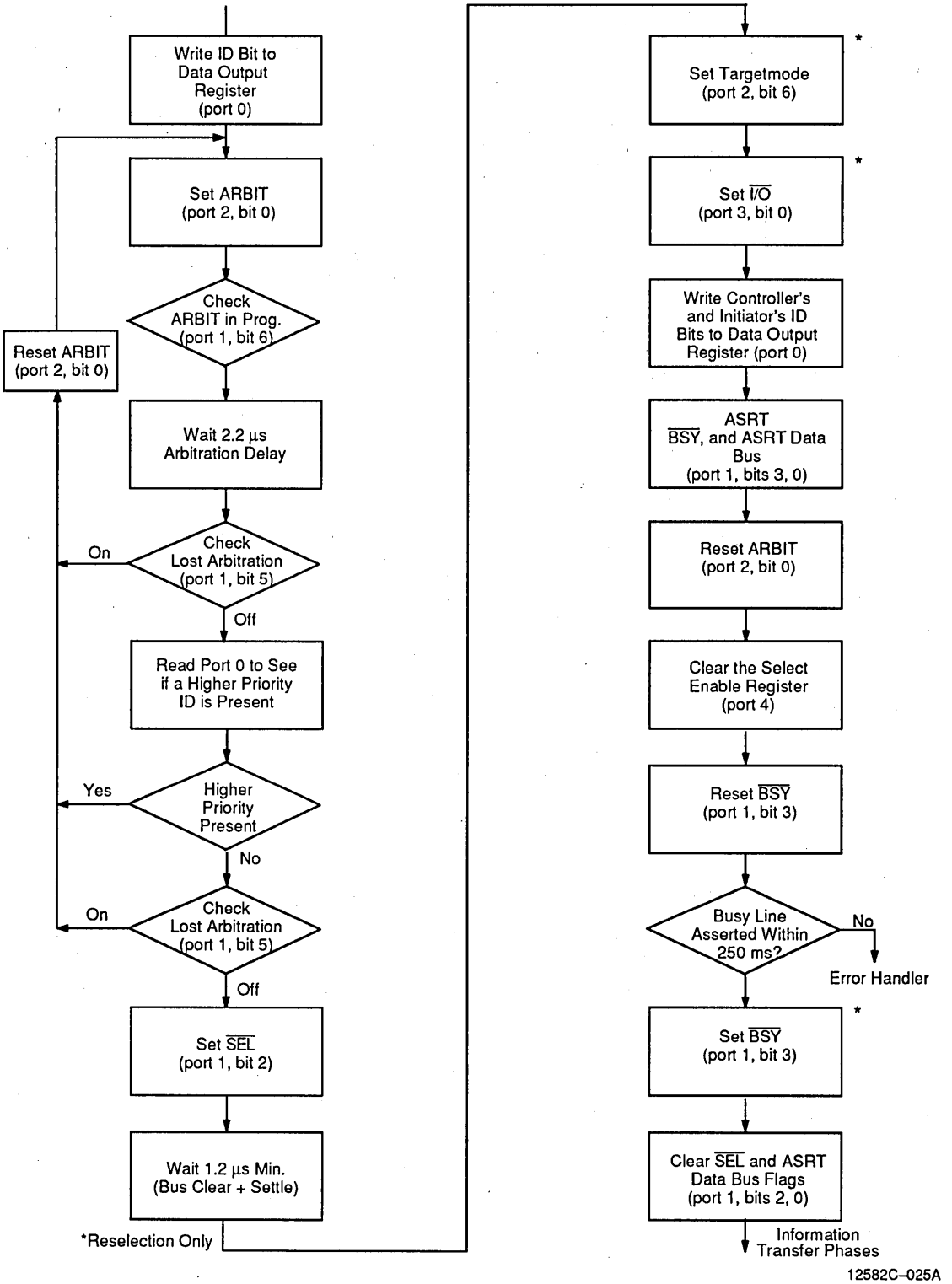


Figure 22. Arbitration and (Re) Selection

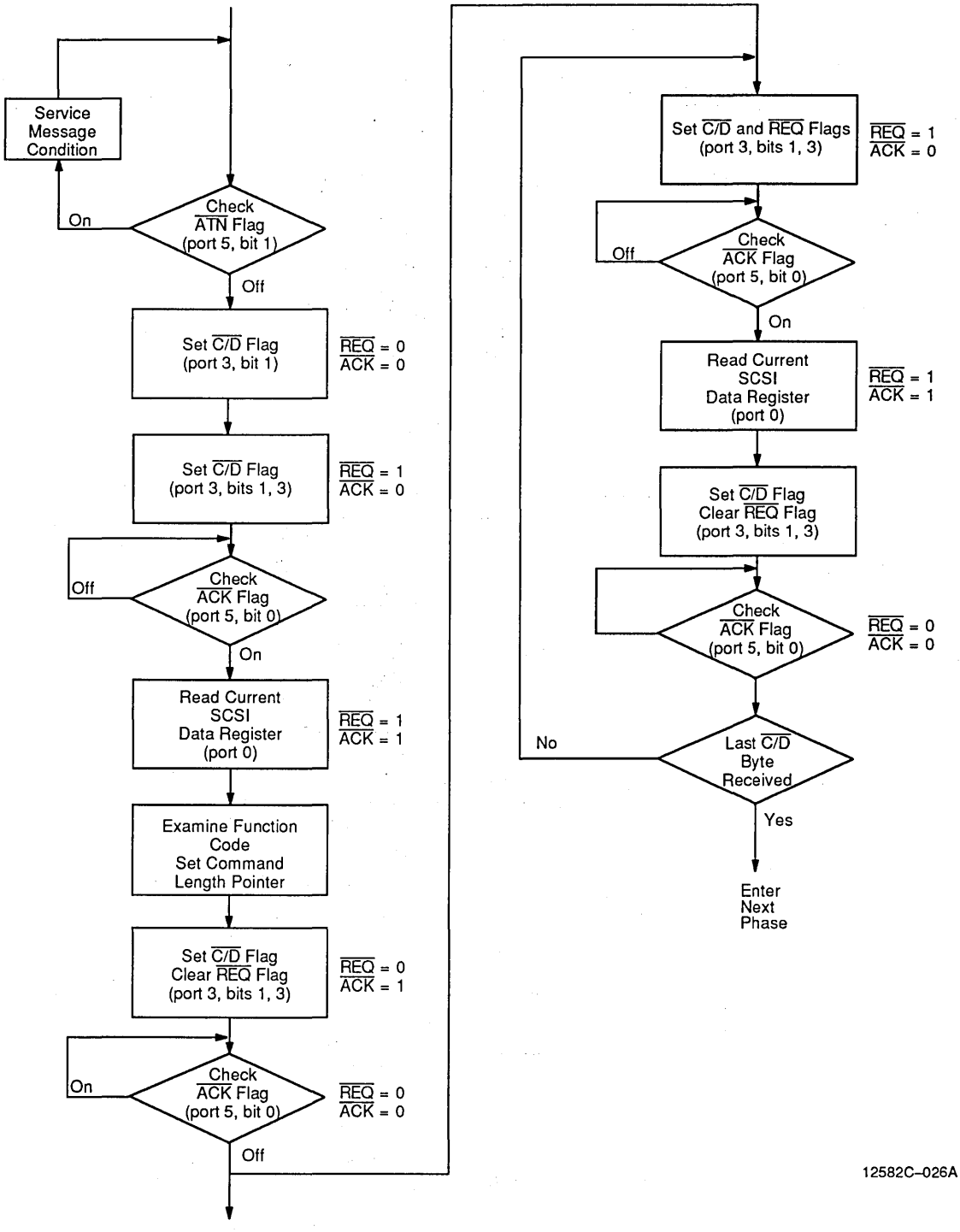


Figure 23. Command Transfer Phase (Target)

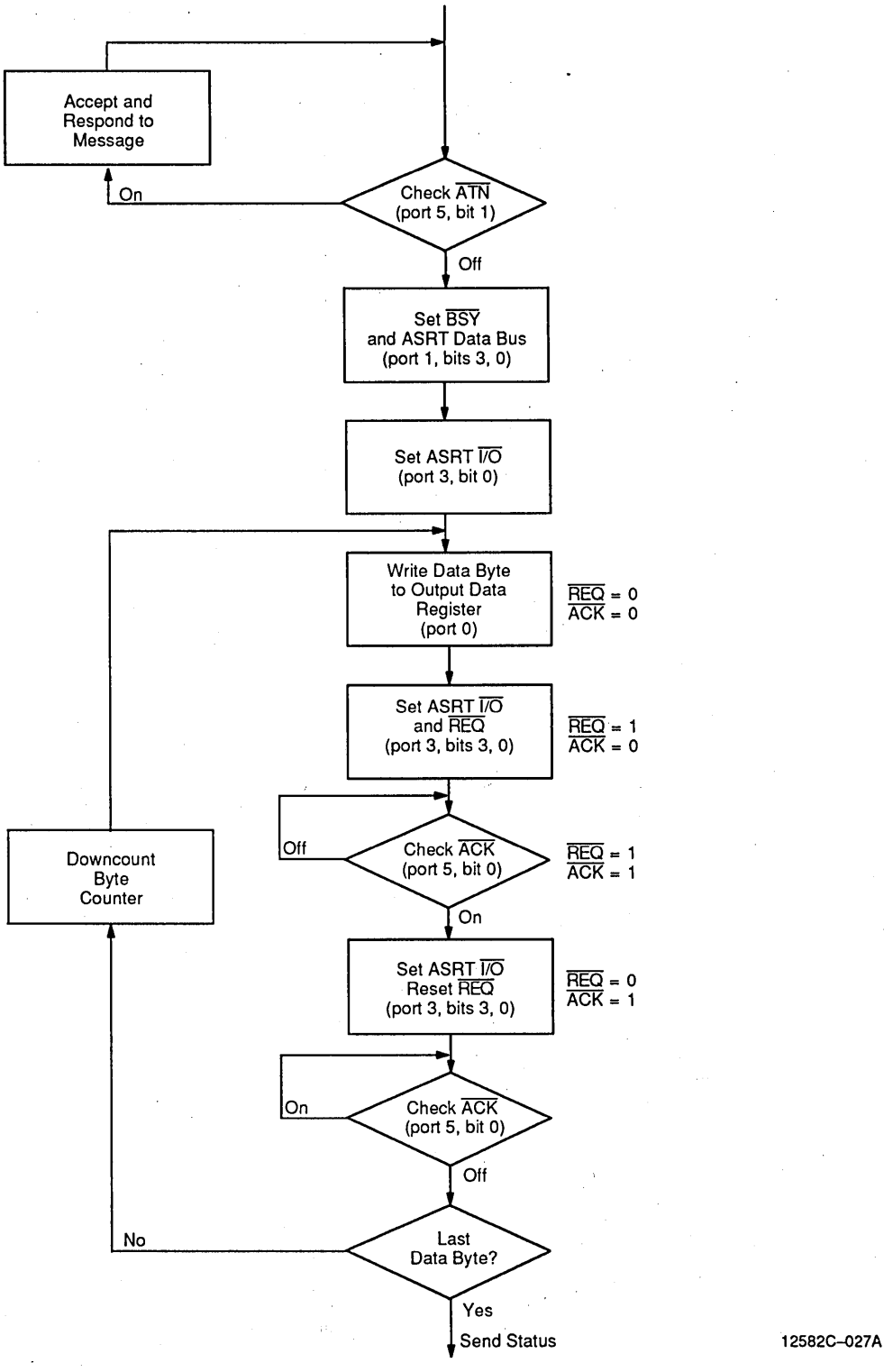


Figure 24. Data Transfer to Host via Programmed I/O

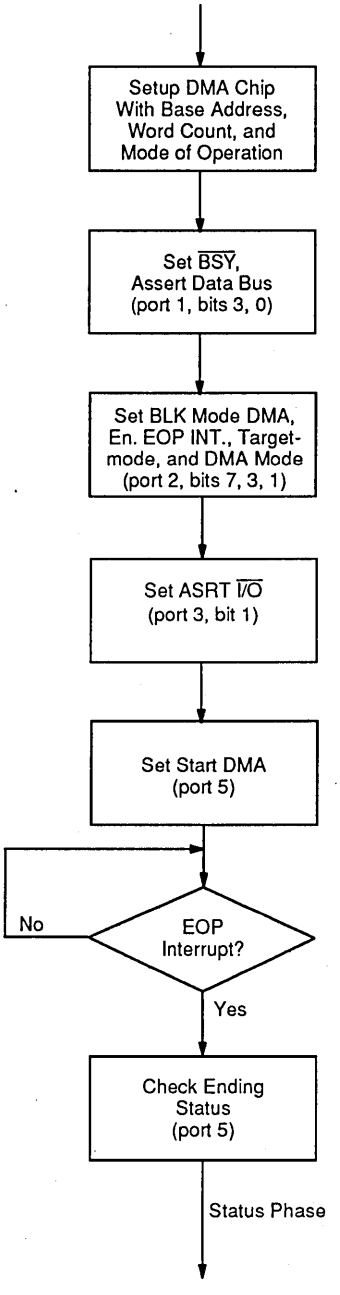


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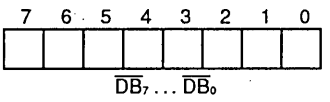
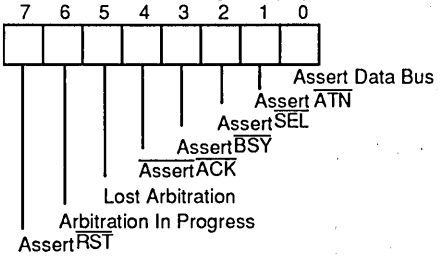
Figure 25. Data Transfer via DMA

Read

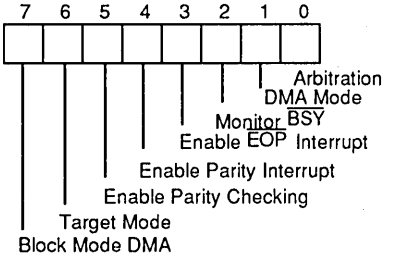
Current SCSI Data (00)



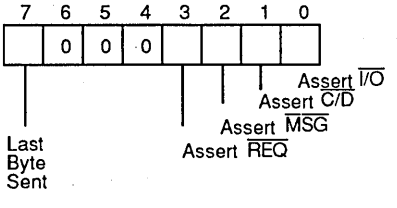
Initiator Command Register (01)



Mode Register (02)

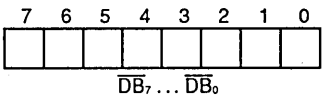


Target Command Register (03)

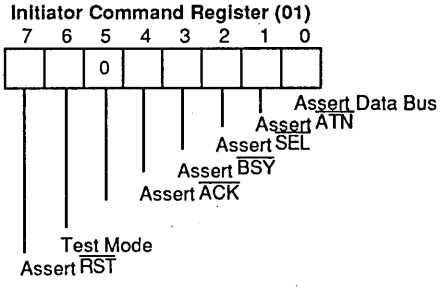


Write

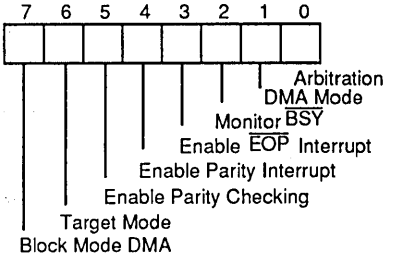
Output Data Register (00)



Initiator Command Register (01)



Mode Register (02)



Target Command Register (03)

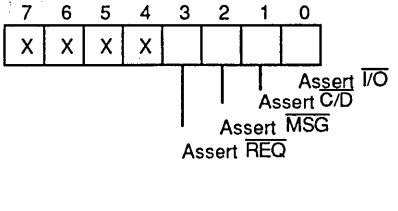


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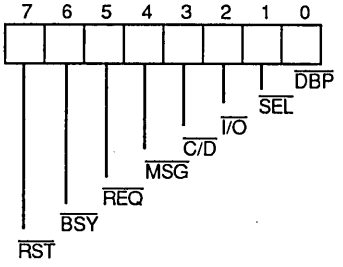
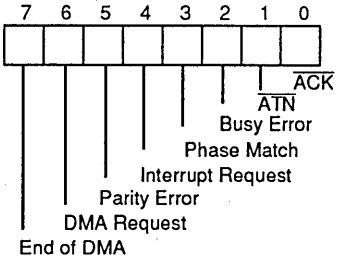
Figure 26. Register Reference Chart

Read

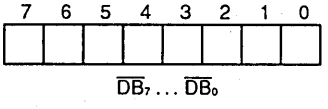
Current SCSI Bus Status (04)



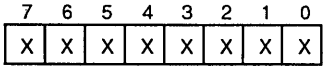
Bus and Status Register (05)



Input Data Register (06)



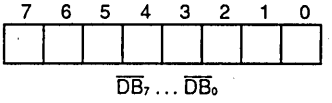
Reset Parity/Interrupt (07)



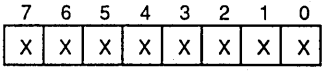
DF006090

Write

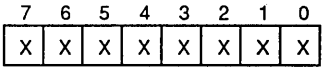
Select Enable Register (04)



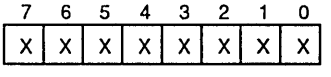
Start DMA Send (05)



Start DMA Target Receive (06)



Start DMA Initiator Receive (07)



Note: X= Don't Care

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Figure 26. Register Reference Chart (continued)

ESCC ARCHITECTURE

The ESCC internal structure includes two full-duplex channels, two 10 × 19 bit SDLC/HDLC frame status FIFOs, two baud rate generators, internal control and interrupt logic, and a bus interface to a non-multiplexed bus. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface with modems or other external devices (see Logic Symbol).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally be used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two SYNC character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write-only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (A only), and one containing the interrupt Pending bits (A only).

The registers for each channel are designated as follows:

WR0–WR15—Write Registers 0 through 15. An additional write register, WR7 Prime (WR7′), is available for enabling or disabling additional SDLC/HDLC enhancements if bit D0 of WR15 is set.

RR0–RR3, RR10, RR12, RR13, RR15—Read Registers 0 through 3, 10, 12, 13, 15.

If bit D2 of WR15 is set, then two additional Read Registers, RR6 and RR7, are available. These registers are used with the 10 × 19 bit Frame Status FIFO.

Table 3 lists the functions assigned to each read and write register. The ESCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

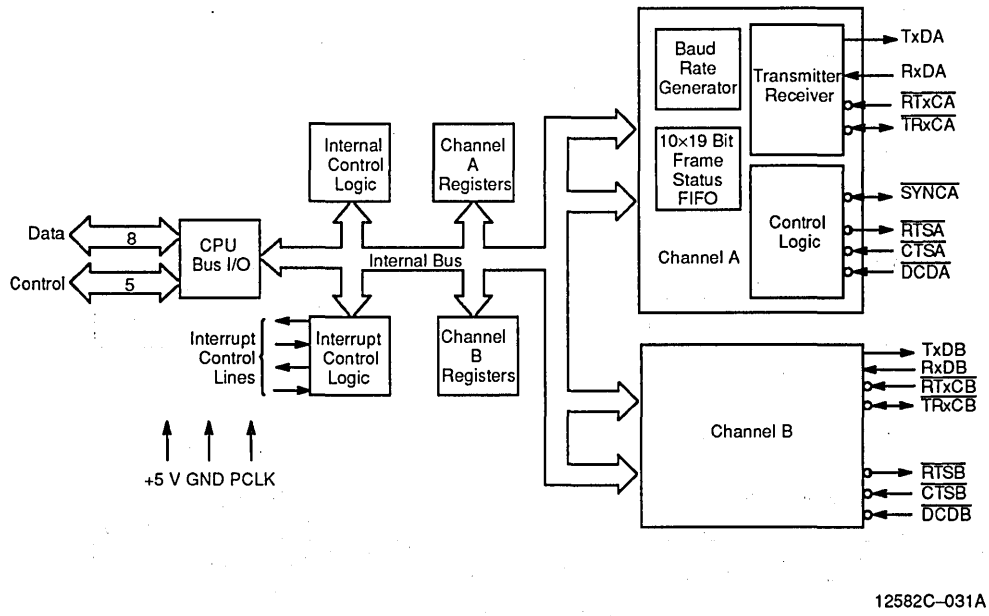

Figure 27. Block Diagram of ESCC Architecture

Data Path

The transmit and receive data path illustrated in Figure 28 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data are routed through one of several paths (data or CRC) depending on the selected mode (the character length in asynchronous modes also determines the data path).

The transmitter has an 8-bit transmit data buffer register loaded from the internal data bus and a 20-bit transmit shift register that can be loaded either from the sync-character registers or from the transmit data register. Depending on the operational mode, outgoing data are routed through one of four main paths before they are transmitted from the Transmit Data output (TxD).

Table 3. Read and Write Register Functions

Read Register Functions		Write Register Functions	
RR0	Transmit/Receive buffer status and External status	**WR0**	Command Register, Register Pointers CRC initialize, initialization commands for the various modes, shift right/shift left command
RR1	Special Receive Condition status (also 10 × 19 bit FIFO Frame Reception Status if WR15 bit D2 is set)	**WR1**	Interrupt conditions and data transfer mode definition
RR2	Modified interrupt vector (Channel B only) Unmodified interrupt vector (Channel A only)	**WR2**	Interrupt vector (accessed through either channel)
RR3	Interrupt Pending bits (Channel A only)	**WR3**	Receive parameters and control
RR6	LSB Byte Count (14-bit counter) (if WR15 bit D2 set)	**WR4**	Transmit/Receive miscellaneous parameters and modes
RR7	MSB Byte Count (14-bit counter) and 10 × 19 bit FIFO Status (if WR15 bit D2 is set)	**WR5**	Transmit parameters and controls
RR8	Receive buffer	**WR6**	Sync character or SDLC address field
RR10	Miscellaneous XMTR, RCVR status	**WR7**	Sync character or SDLC flag
RR12	Lower byte of baud rate generator time constant	**WR7′**	SDLC/HDLC enhancements (if bit D0 of WR15 set)
RR13	Upper byte of baud rate generator time constant	**WR8**	Transmit buffer
RR15	External/Status interrupt information	**WR9**	Master interrupt control and reset (accessed through either channel)
		WR10	Miscellaneous transmitter/receiver control bits, data encoding
		WR11	Clock mode control, Rx and Tx clock source
		WR12	Lower byte of baud rate generator time constant
		WR13	Upper byte of baud rate generator time constant
		WR14	Miscellaneous control bits, DPLL control
		WR15	External/Status interrupt control

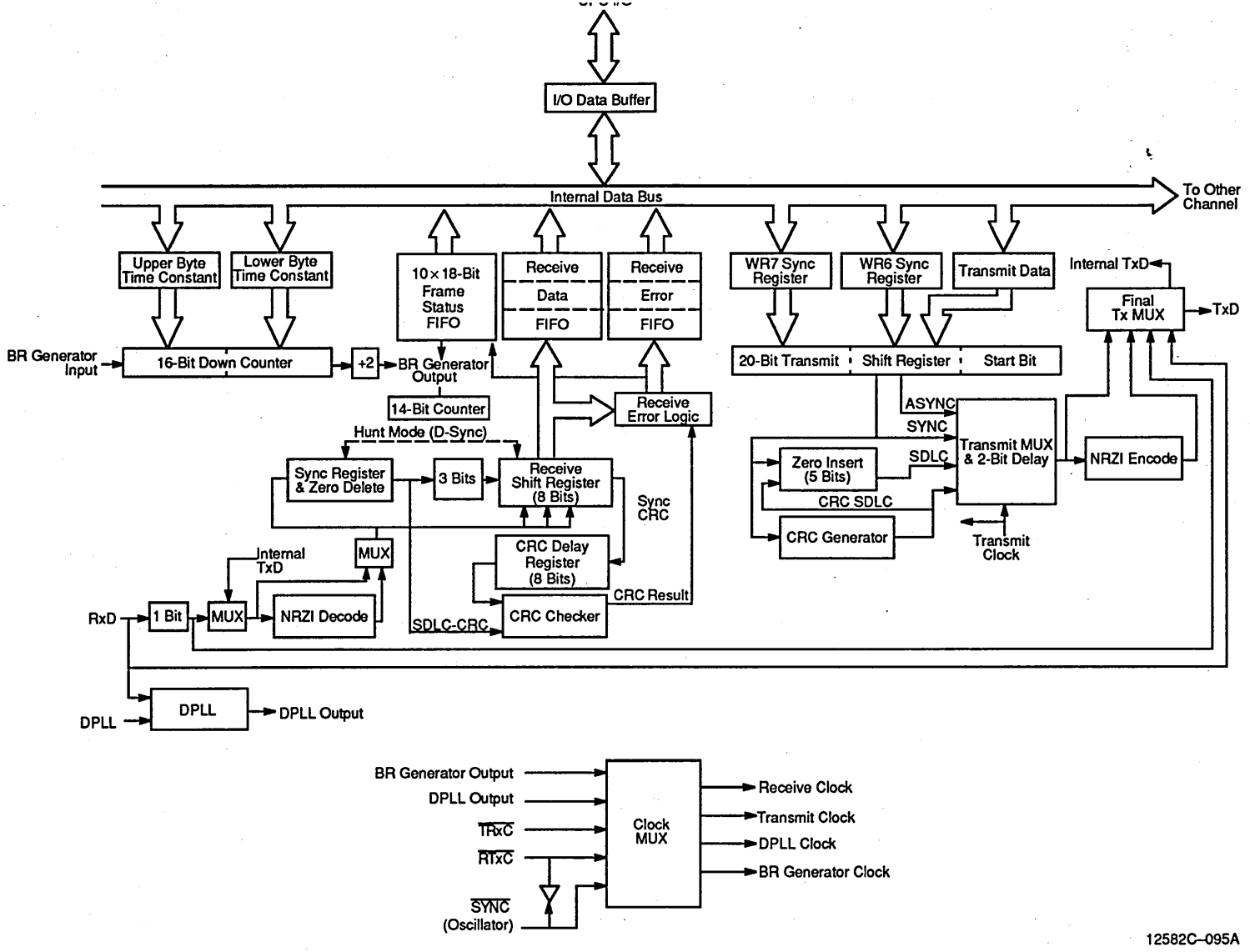

Figure 28. Data Path

DETAILED DESCRIPTION

The functional capabilities of the ESCC can be described from two different points of view; as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, it interacts with the CPU and provides vectored interrupts and handshaking signals.

Data Communications Capabilities

The ESCC provides two independent full-duplex channels programmable for use in any common asynchronous or SYNC data-communication protocol. Figure 29 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input. If the Low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of framing error as a new start bit; a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ESCC does not require symmetric transmit and receive clock signals—a feature allowing use of a wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the $\overline{SYNC}$ pin may be programmed as an input used for functions, such as monitoring a ring indicator.

Synchronous Modes

The ESCC supports both byte-oriented and bit-oriented synchronous communication. SYNC byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit SYNC character (Monosync), any 12-bit or 16-bit SYNC pattern (Bisync), or with an external SYNC signal. Leading SYNC characters can be removed without interrupting the CPU.

Five- or 7-bit SYNC characters are detected with 8- or 16-bit patterns in the ESCC by overlapping the larger pattern across multiple incoming SYNC characters as shown in Figure 30.

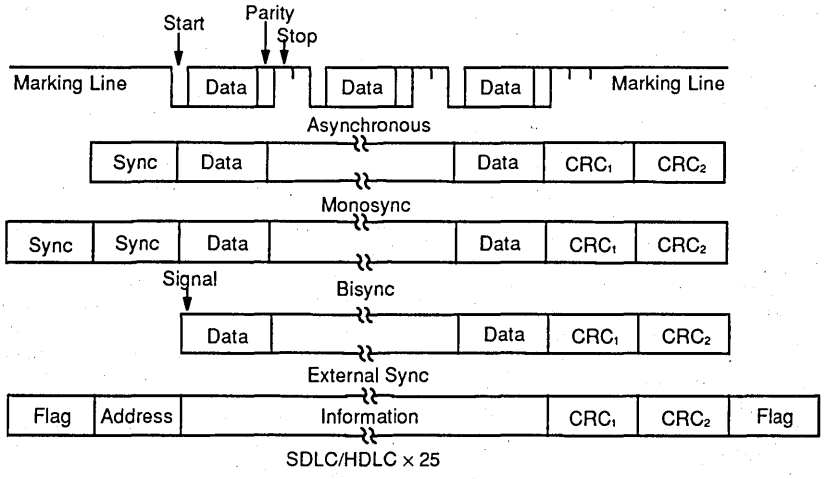

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Figure 29. ESCC Protocols

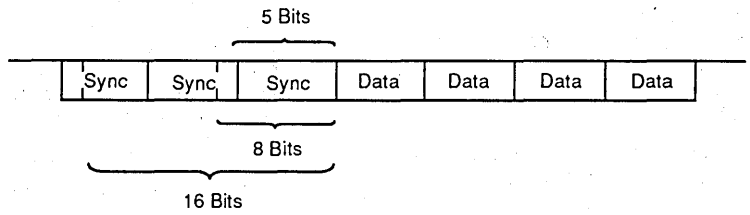

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Figure 30. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols, such as IBM BISYNC.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in BISYNC and MONOSYNC modes. Users may preset the CRC generator and checker to all "1"s or all "0"s. The ESCC also provides a feature that automatically transmits CRC data when no other data are available for transmission. This allows for high-speed transmissions under DMA control with no need for CPU intervention at the end of a message. When there are no data or CRC to send in SYNC modes, the transmitter inserts 6-, 8-, or 16-bit SYNC characters, regardless of the programmed character length.

The ESCC supports SYNC bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero bit insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the ESCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The ESCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{SYNC}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all "0"s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the ESCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all "1"s or all "0"s. The CRC is inverted before transmission and the receiver checks against the bit pattern "0001110100001111."

NRZ, NRZI or FM coding may be used in any 1X mode. The parity options available in asynchronous modes are available in synchronous modes.

The ESCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the ESCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The ESCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the ESCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC Loop Mode

The ESCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow and any number of secondary stations. In SDLC Loop mode, the ESCC performs the functions of a secondary station while an ESCC operating in regular SDLC mode can act as a controller (Figure 31).

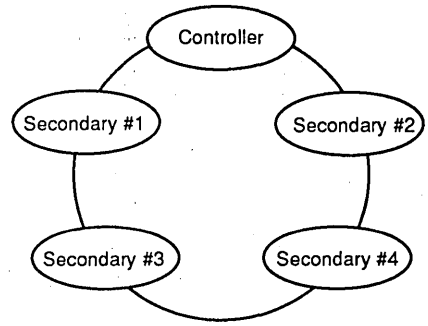

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Figure 31. An SDLC Loop

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop and, in fact, must pass these messages to the rest of the loop by retransmitting them with a 1-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern "11111110." Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary one of the EOP to a zero before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send

merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the ESCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

Baud Rate Generator

Each channel in the ESCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On start-up, the flip-flop on the output is set in a High state; the value in the time constant register is loaded into the counter; and the counter starts counting down. The output of the baud rate generator toggles upon reaching zero; the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate where PCLK or $\overline{RTxC}$ is the baud rate generator input frequency in Hz. The clock mode is X1, X16, X32, or X64 as selected in Write Register 4, bits D6 and D7. Synchronous operation modes should select X1 and Asynchronous should select X16, X32, or X64.

$$\text{Time Constant} = \left[\frac{\text{PCLK or RTxC Frequency}}{2\,(\text{Baud Rate})(\text{Clock Mode})}\right] - 2$$

The following formula relates the time constant to the baud rate. (The baud rate is in bits/second and the BR clock period is in seconds given by Clock Mode/Clock Frequency.)

$$\text{baud rate} = \frac{1}{2\,(\text{Time Constant} + 2) \times (\text{BR Clock Period})}$$

Time Constant Values for Standard Baud Rates at BR Clock = 3.9936 MHz			
Rate (Baud)	Time Constant (decimal/Hex notation)		Error
19200	102	(0066)	0
9600	206	(00CE)	0
7200	275	(0113)	0.12%
4800	414	(019E)	0
3600	553	(0229)	0.06%
2400	830	(033E)	0
2000	996	(03E4)	0.04%
1800	1107	(0453)	0.03%
1200	1662	(067E)	0
600	3326	(0CFE)	0
300	6654	(19FE)	0
150	13310	(33FE)	0
134.5	14844	(39FC)	0.0007%
110	18151	(46E7)	0.0015%
75	26622	(67FE)	0
50	39934	(98FE)	0

Digital Phase-Locked Loop

The ESCC contains a digital phase-locked loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the ESCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32X clock to create nominal bit times. As the 32X clock is counted, the DPLL is searching the incoming data stream for edges (either 1/0 or 0/1). As long as no transitions are detected, the DPLL output will be free running and its input clock source will be divided by 32, producing an output clock without any phase jitter. Upon detecting a transition the DPLL will adjust its clock output (during the next counting cycle) by adding or subtracting a count of 1, thus producing a terminal count closer to the center of the bit cell. The adding or subtracting of a count of 1 will produce a phase jitter of ±5.63° on the output of the DPLL. Because the ESCC's DPLL uses both edges of the incoming signal to compare with its clock source, the mark-space ratio (50%) of the incoming signal should not deviate by more than ±1.5% if proper locking is to occur.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15/16 counting transition.

The 32X clock for the DPLL can be programmed to come from either the $\overline{RTxC}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ESCC via the $\overline{TRxC}$ pin (if this pin is not being used as an input).

Crystal Oscillator

When using a crystal oscillator to supply the receive or transmit clocks to a channel of the ESCC, the user should:

1. Select a crystal oscillator which satisfies the following specifications:
   - 30 ppm @ 25°C
   - 50 ppm over temperature of –20° to 70°C
   - 5 ppm/yr aging
   - 5 mW drive level
2. Place crystal across $\overline{RTxC}$ and $\overline{SYNC}$ pins
3. Place 30 pF capacitors to ground from both $\overline{RTxC}$ and $\overline{SYNC}$ pins
4. Set bit D_7 of WR11 to "1."

Data Encoding

The ESCC may be programmed to encode and decode the serial data in four different ways (Figure 6). In NRZ encoding, a "1" is represented by a High level, and a "0" is represented by a Low level. In NRZI encoding, a "1" is represented by no change in level, and a "0" is represented by a change in level. In FM_1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A "1" is represented by an additional transition at the center of the bit cell, and a "0" is represented by no additional transition at the center of the bit cell. In FM_0 (bi-phase space), a transition occurs at the beginning of every bit cell. A "0" is represented by an additional transition at the center of the bit cell, and a "1" is represented by no additional transition at the center of the bit cell. In addition to these four methods, the ESCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0/1, the bit is a "0." If the transition is 1/0, the bit is a "1."

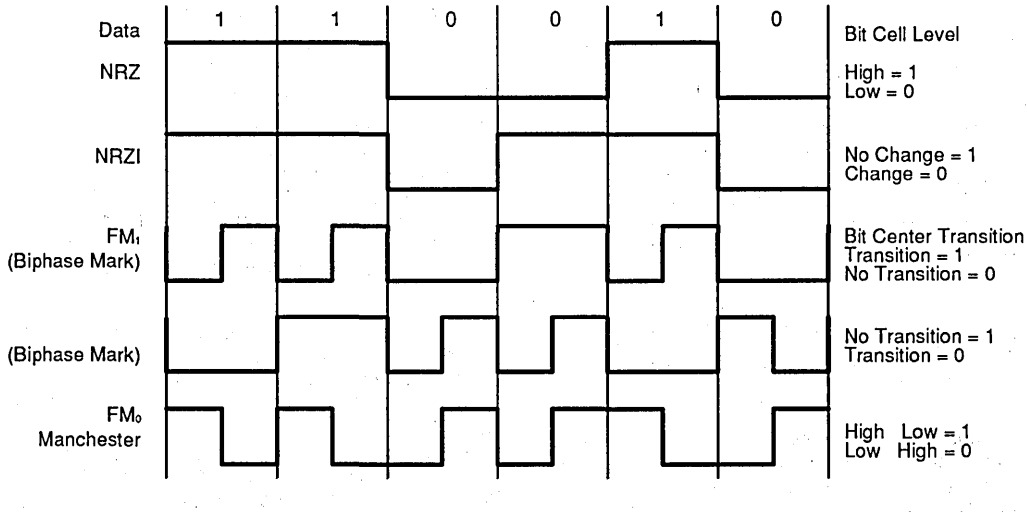


Figure 32. Data Encoding Methods

Auto Echo and Local Loopback

The ESCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes but works in SYNC and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In this mode, the transmitter is actually bypassed, and the programmer is responsible for disabling transmitter interrupts and $\overline{WAIT}$/$\overline{REQUEST}$ on transmit.

The ESCC is also capable of Local Loopback. In this mode, TxD is RxD just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data, and RxD is ignored (except to be echoed out via TxD). The $\overline{DCD}$ input is also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, SYNC and SDLC modes with NRZ, NRZI or FM coding of the data stream.

I/O Interface Capabilities

The ESCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

Polling

All interrupts are disabled. Three status registers in the ESCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

Interrupts

When an ESCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 34 and 35).

To speed interrupt response time, the ESCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ESCC (Transmit, Receive and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write-only.

In the ESCC, the IP bit signals a need for interrupt servicing. When an IP bit is set to "1" and the IEI input is High, the $\overline{INT}$ output is pulled Low, requesting an interrupt. In the ESCC, if the IE bit is set for an interrupt, then the IP for that source can never be set. The IP bits are readable in RR3A.

There are three types of interrupts: Transmit, Receive and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the Receive can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive condition
- Interrupt on all Receive Characters or Special Receive condition
- Interrupt on Special Receive condition only

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in asynchronous mode, end-of-frame in SDLC mode, and optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary Receive Character Available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In Interrupt on First Receive Character, an interrupt can occur from Special Receive Conditions any time after the first Receive Character Interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{DCD}$, and $\overline{SYNCA}$ pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, a zero count in the baud rate generator, the detection of a Break (asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the ESCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA Block Transfer

The ESCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the $\overline{WAIT/REQUEST}$ output in conjunction with the Wait/Request bits in WR1. The $\overline{WAIT/REQUEST}$ output can be defined under software control as a $\overline{WAIT}$ line in the CPU Block Transfer mode or as a $\overline{REQUEST}$ line in the DMA Block Transfer mode.

To a DMA controller, the ESCC $\overline{REQUEST}$ output indicates that the ESCC is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ line indicates that the ESCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{DTR/REQUEST}$ can be used as the transmit request line, thus allowing full-duplex operation under DMA control.

PROGRAMMING INFORMATION

Each channel has fifteen Write registers that are individually programmed from the system bus to configure the functional personality of each channel. Each channel also has eight Read registers from which the system can read Status, Baud rate, or Interrupt information.

On the ESCC, only four data registers (Read and Write for Channels A and B) are directly selected by a High on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$ and A/$\overline{B}$ pins. All other registers are addressed indirectly by the content of Write Register 0 in conjunction with a Low on the D/$\overline{C}$ input and the appropriate levels on the $\overline{RD}$, $\overline{WR}$ and A/$\overline{B}$ pins. If bit D3 in WR0 is 1 and bits 5 and 6 are 0, then bits 0, 1, 2 address the higher registers 8 through 15. If bits 4, 5, 6 contain a different code, bits 0, 1, 2 address the lower registers 0 through 7 as shown in Table 4.

Writing to or reading from any register except RR0, WR0 and the Data Registers thus involves two operations:

First, write the appropriate code into WR0, then follow this by a write or read operation on the register thus specified. Bits 0 through 4 in WR0 are automatically cleared after this operation, so that WR0 then points to WR0 or RR0 again.

Channel A/Channel B selection is made by the A/$\overline{B}$ input (HIGH = A, Low = B)

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set and, finally, receiver or transmitter enable.

Table 4. Register Addressing

D/$\overline{C}$	"Point High" Code In WR0:	D2, D1, D0 In WR0:			Write Register	Read Register
HIGH	Either Way	x	x	x	Data	Data
LOW	Not True	0	0	0	0	0
LOW	Not True	0	0	1	1	1
LOW	Not True	0	1	0	2	2
LOW	Not True	0	1	1	3	3
LOW	Not True	1	0	0	4	(0)
LOW	Not True	1	0	1	5	(1)
LOW	Not True	1	1	0	6	(2)
LOW	Not True	1	1	1	7	(3)
LOW	True	0	0	0	Data	Data
LOW	True	0	0	1	9	–
LOW	True	0	1	0	10	10
LOW	True	0	1	1	11	(15)
LOW	True	1	0	0	12	12
LOW	True	1	0	1	13	13
LOW	True	1	1	0	14	(10)
LOW	True	1	1	1	15	15

Read Registers

The ESCC contains eight read registers [actually nine, counting the receive buffer (RR8) in each channel]. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). In addition, if bit D2 of WR15 is set, RR6 and RR7 are available for providing frame status from the 10 × 19 bit Frame Status FIFO. Figure 33 shows the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring, for example, when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

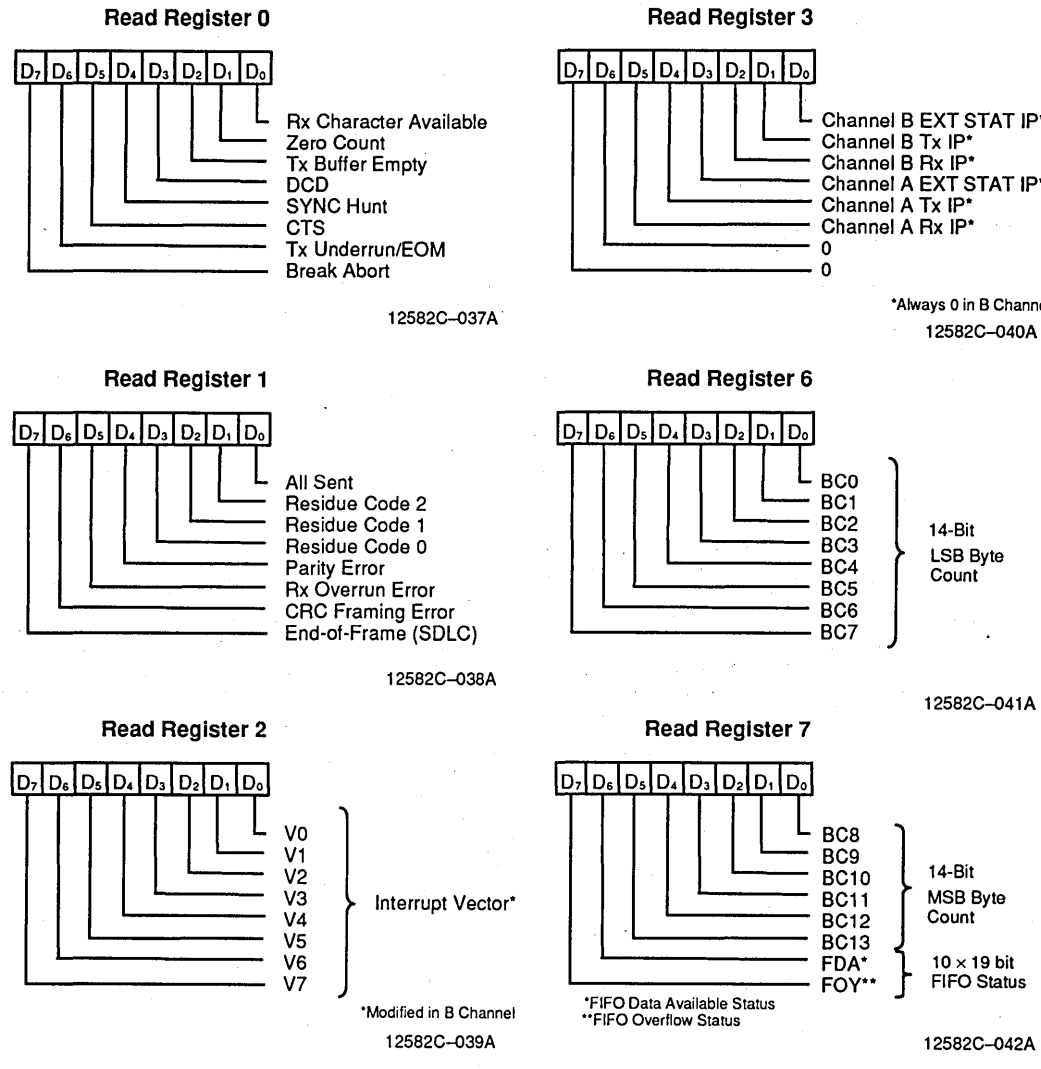


Figure 33. Read Register Bit Functions

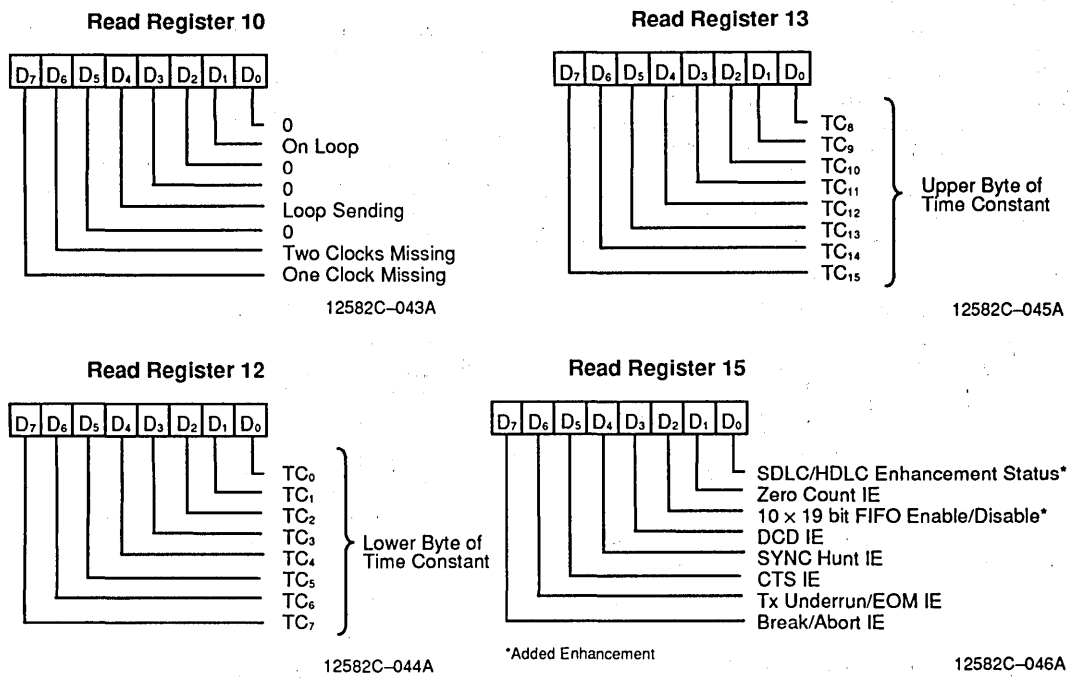


Figure 33. Read Register Bit Functions (continued)

Write Registers

The ESCC contains 15 write registers (16 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. Two registers (WR2 and WR9) are shared by the two channels that can be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. In addition, if bit D0 of WR15 is set, write register seven prime (WR7′) is available for programming additional SDLC/HDLC enhancements. When bit D0 of WR15 is set, executing a write to WR7 actually writes to WR7′ to further enhance the functional "personality" of each channel. Figure 34 shows the format of each write register.

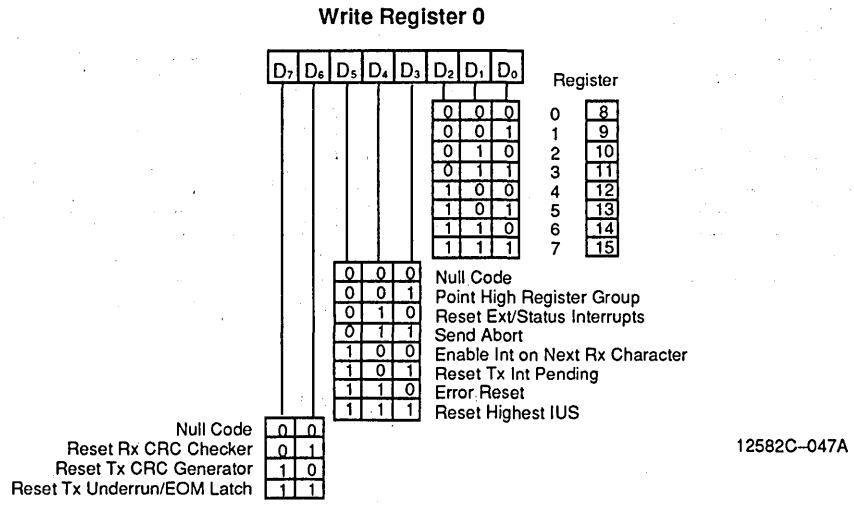


Figure 34. Write Register Bit Functions

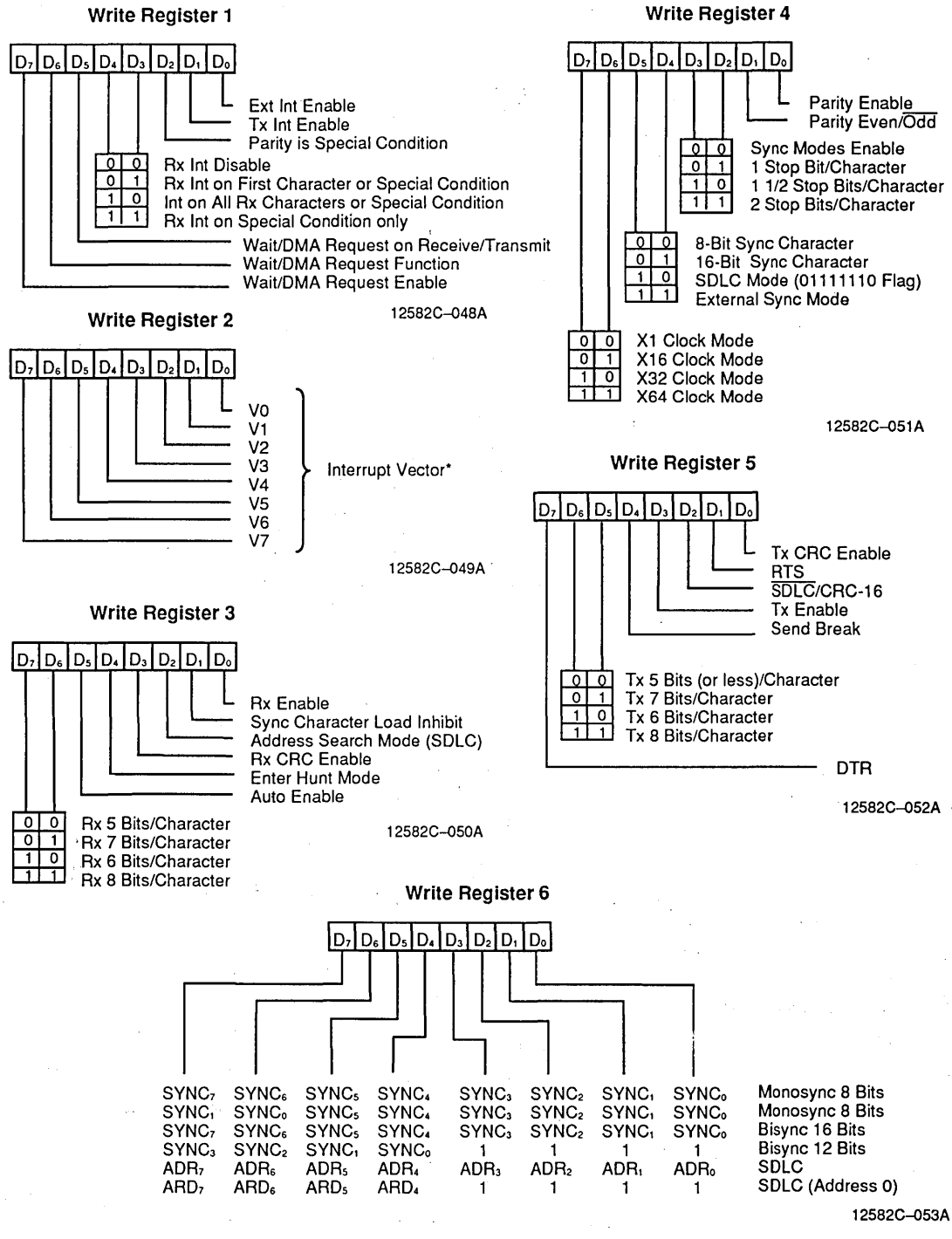
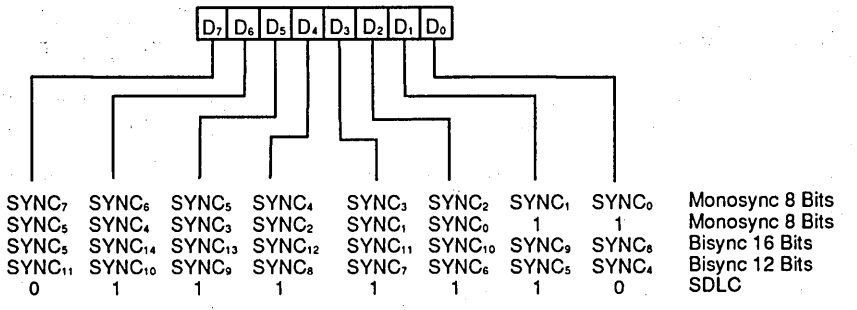


Figure 34. Write Register Bit Functions (continued)

Write Register 7



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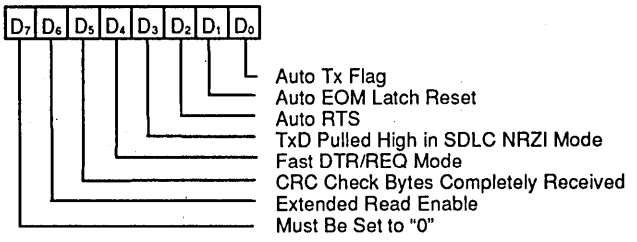
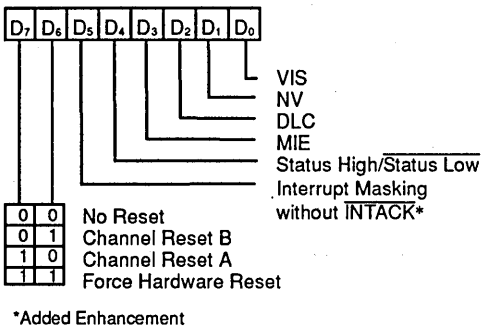
Write Register 7′



12582C–055A

Write Register 9



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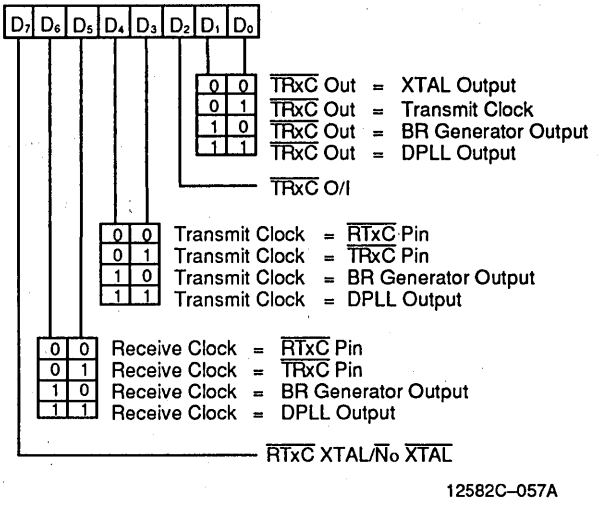
Write Register 11



12582C–057A

Figure 34. Write Register Bit Functions (continued)

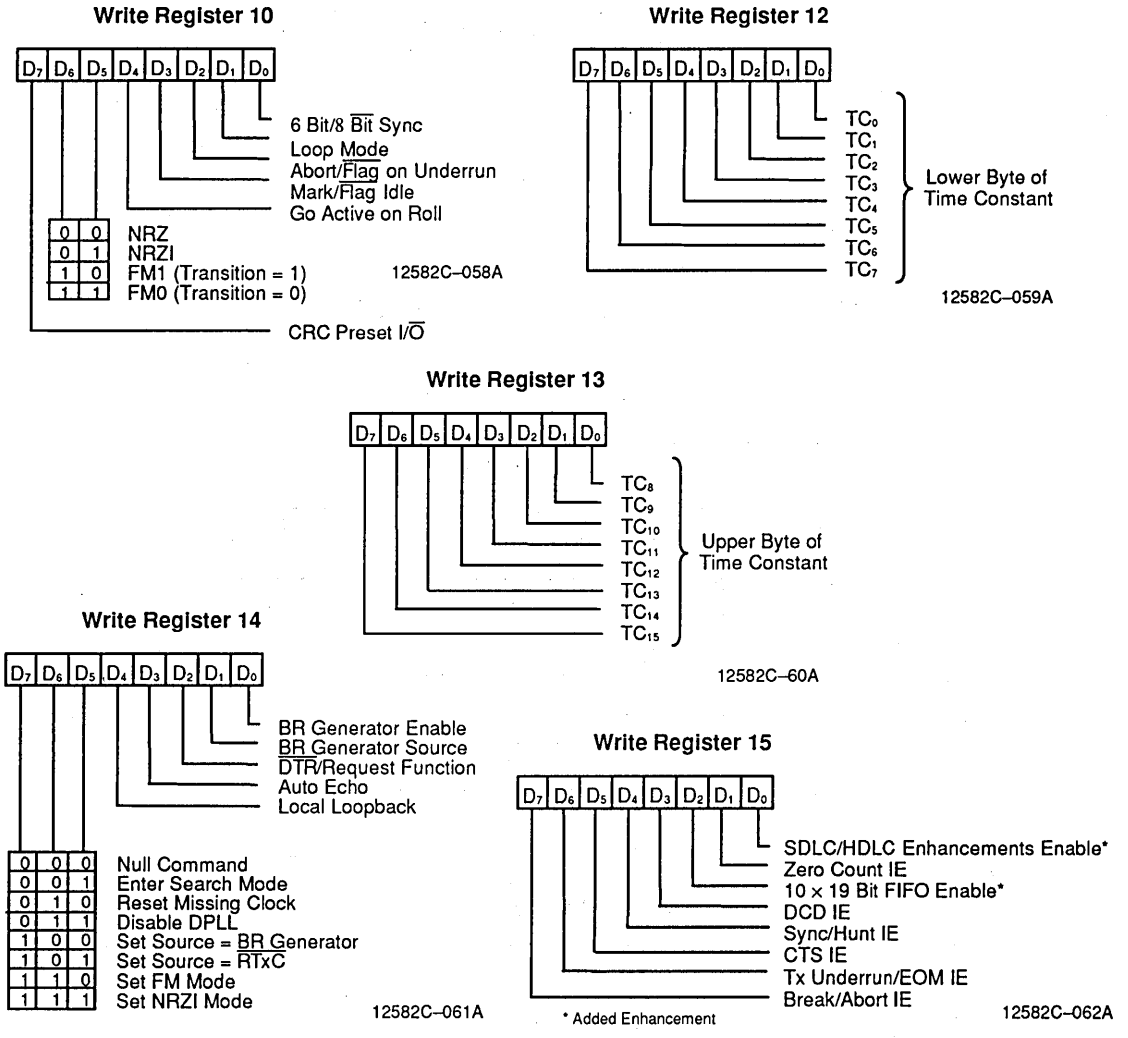


Figure 34. Write Register Bit Functions (continued)

ESCC Timing

The ESCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ESCC. The recovery time required for proper operation is specified from the falling edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the ESCC, to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the ESCC. This time must be at least 3 1/2 PCLK regardless of which register or channel is being accessed.

Interrupt Acknowledge Cycle Timing

Figure 37 illustrates Interrupt Acknowledge cycle timing. The ESCC may be programmed to respond to $\overline{RD}$ Low by placing its interrupt vector on D0–D7 and it then sets the appropriate Interrupt-Under-Service latch internally.

Read Cycle Timing

Figure 35 illustrates Read cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE1}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened. $\overline{CE2}$ and $\overline{DACK}$ must be inactive.

Write Cycle Timing

Figure 36 illustrates Write Cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE1}$ falls after $\overline{WR}$ falls or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened. Data must be valid before the rising edge of $\overline{WR}$. $\overline{CE2}$ and $\overline{DACK}$ must be inactive.

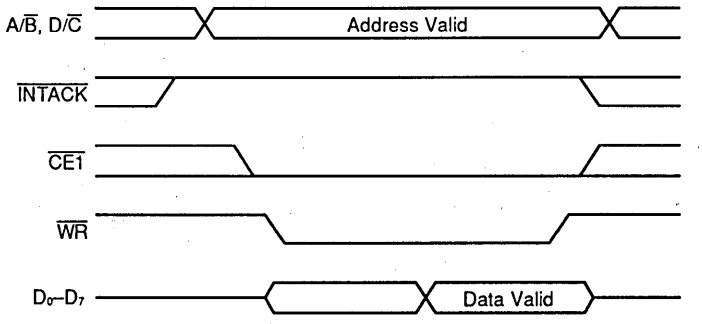


Figure 35. Read Cycle Timing

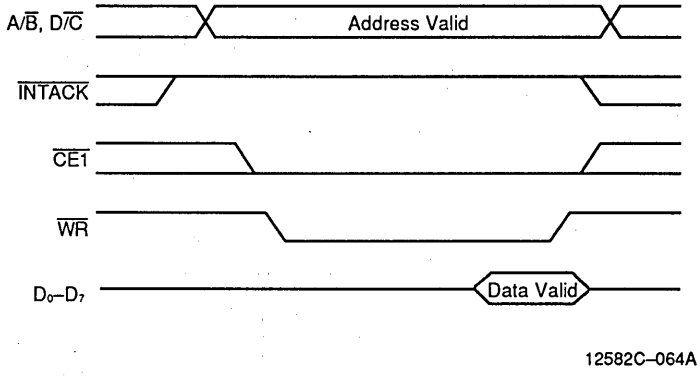


Figure 36. Write Cycle Timing

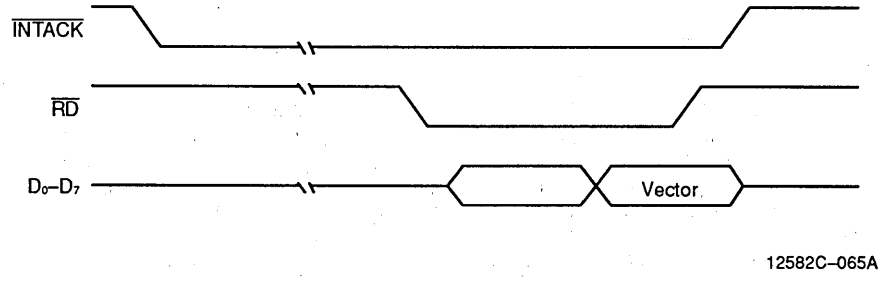


Figure 37. Interrupt Acknowledge Cycle Timing

FIFO

FIFO Enhancements

When used with a DMA controller, the ESCC Frame Status FIFO enhancement maximizes the ESCC's ability to receive high-speed back-to-back SDLC messages while minimizing frame overruns due to CPU latencies in responding to interrupts.

Additional logic was added to the industry-standard NMOS Am8530H consisting of a 10-deep by 19-bit status FIFO, a 14-bit receive byte counter, and control logic as shown in Figure 38. The 10 × 19 bit status FIFO is separate from the existing three-byte receive data and Error FIFOs.

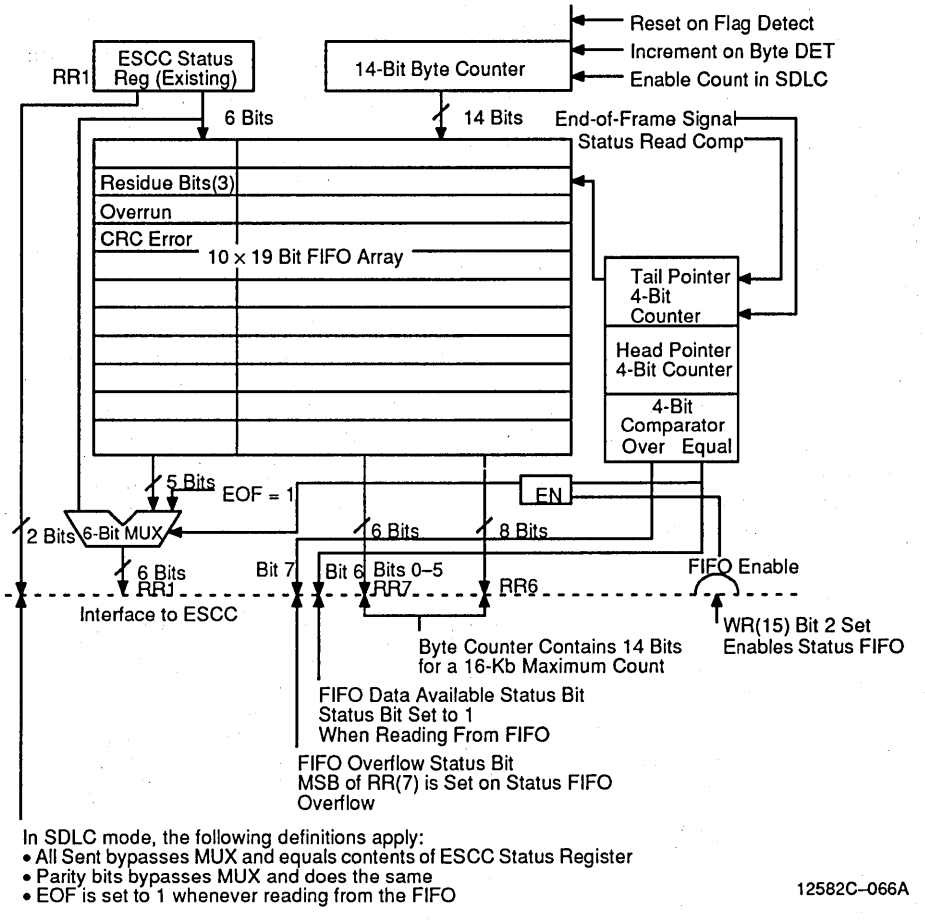


Figure 38. ESCC Status Register Modifications

When the enhancement is enabled, the status in Read Register 1 (RR1) and byte count for the SDLC frame will be stored in the 10 × 19 bit status FIFO. This allows the DMA controller to transfer the next frame into memory while the CPU verifies that the message was properly received.

Summarizing the operation, data is received, assembled, and loaded into the three-byte receive FIFO before being transferred to memory by the DMA controller. When a flag is received at the end of an SDLC frame, the frame byte count from the 14-bit counter and five status bits are loaded into the status FIFO for verification by the CPU. The CRC checker is automatically reset in preparation for the next frame which can begin immediately.

Since the byte count and status are saved for each frame, the message integrity can be verified at a later time. Status information for up to 10 frames can be stored before a status FIFO overrun could occur.

If receive interrupts are enabled while the 10 × 19 FIFO is enabled, an SDLC end-of-frame special condition will not lock the three-byte Receive data FIFO. An SDLC end-of-frame still locks the three-byte Receive data FIFO in "Interrupt on first Receive Character or Special Condition" and "Interrupt on Special Condition Only" modes when the 10 × 19 FIFO is disabled. This feature allows the 10 × 19 SDLC FIFO to accept multiple SDLC frames without CPU intervention at the end of each frame.

FIFO Detail

For a better understanding of details of the FIFO operation, refer to the block diagram contained in Figure 38.

Enable/Disable

This FIFO is implemented so that it is enabled when WR15 bit 2 is set and the ESCC is in the SDLC/HDLC mode, otherwise the status register contents bypass the FIFO and go directly to the bus interface (the FIFO pointer logic is reset either when disabled or via a channel or power-on reset). When the FIFO mode is disabled, the ESCC is completely downward-compatible with the NMOS Am8530H. The FIFO mode is disabled on power-up (WR15 bit 2 is set to "0" on reset). The effects of backward compatibility on the register set are that RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2, and RR7 is an image of RR3. For the details of the added registers, refer to Figure 15. The status of the FIFO Enable signal can be obtained by reading RR15 bit 2. If the FIFO is enabled, the bit will be set to "1"; otherwise, it will be reset.

Read Operation

When WR15 bit 2 is set and the FIFO is not empty, the next read to status register RR1 or the additional registers RR7 and RR6 will actually be from the FIFO. Reading status register RR1 causes one location of the FIFO to be emptied, so status should be read after reading the byte count, otherwise the count will be incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to be read directly from the status register, and reads from RR7 and RR6 will contain bits that are undefined. Bit 6 of RR7 (FIFO Data Available) can be used to determine if status data is coming from the FIFO or directly from the status register, since it is set to "1" whenever the FIFO is not empty.

Because not all status bits are stored in the FIFO, the All Sent, Parity, and EOF bits will bypass the FIFO. The status bits sent through the FIFO will be Residue Bits (3), Overrun, and CRC Error.

The sequence for proper operation of the byte count and FIFO logic is to read the registers in the following order, RR7, RR6, and RR1 (reading RR6 is optional). Additional logic prevents the FIFO from being emptied by multiple reads from RR1. The read from RR7 latches the FIFO empty/full status bit (bit 6) and steers the status multiplexer to read from the ESCC megacell instead of the status FIFO (since the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO was empty, logic is added to prevent a FIFO underflow condition).

Write Operation

When the end of an SDLC frame (EOF) has been received and the FIFO is enabled, the contents of the status and byte-count registers are loaded into the FIFO. The EOF signal is used to increment the FIFO. If the FIFO overflows, the MSB of RR7 (FIFO Overflow) is set to indicate the overflow. This bit and the FIFO control logic is reset by disabling and re-enabling the FIFO control bit (WR15 bit 2). For details of FIFO control timing during an SDLC frame, refer to Figure 39.

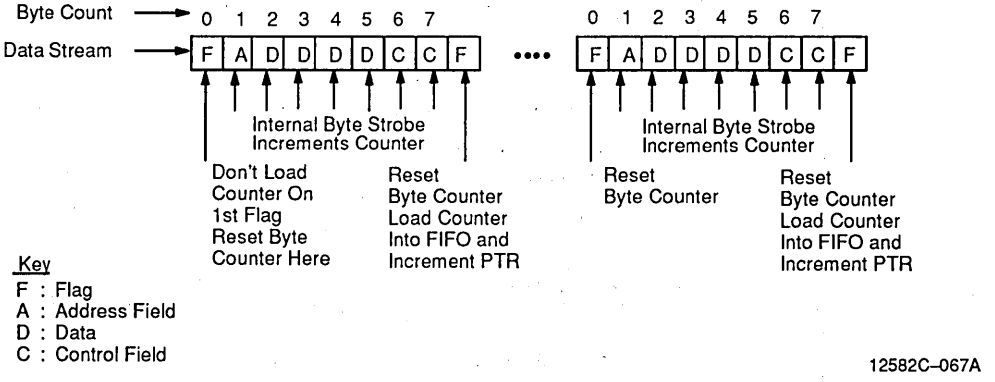


Figure 39. SDLC Byte Counting Detail

Byte Counter Detail

The 14-bit byte counter allows for packets up to 16K bytes to be received. For a better understanding of its operation, refer to Figures 38 and 39.

Enable

The byte counter is enabled when the ESCC is in the SDLC/HDLC mode and WR15 bit 2 is set to "1."

Reset

The byte counter is reset whenever an SDLC flag character is received. The reset is timed so that the contents of the byte counter are successfully written into the FIFO.

Increment

The byte counter is incremented by writes to the data FIFO. The counter represents the number of bytes received by the ESCC, rather than the number of bytes transferred from the ESCC. (These counts may differ by up to the number of bytes in the receive data FIFO contained in the ESCC.)

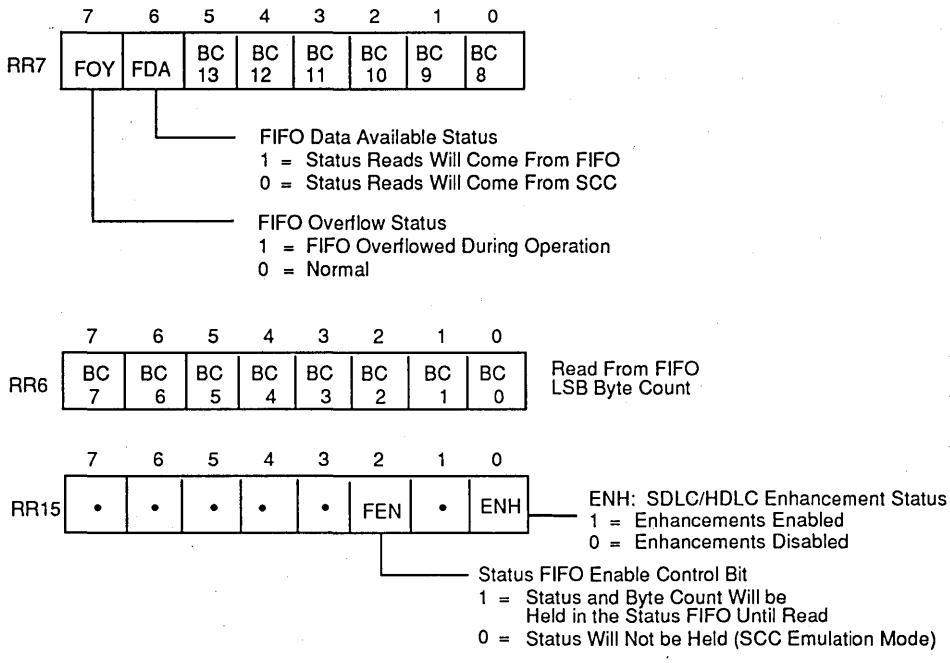


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Figure 40. ESCC Additional Registers

ESCC SDLC/HDLC Enhancement Register Access

SDLC/HDLC enhancements on the ESCC are enabled or disabled via bits D2 or D0 in WR15. Bit D2 determines whether or not the 10 × 19 bit SDLC/HDLC frame status FIFO is enabled while bit D0 determines whether or not other enhancements are enabled via WR7′. Table 5 shows what functions on the ESCC are enabled when these bits are set.

Table 5. Enhancement Options

WR15 Bit D2 10 × 19 Bit FIFO Enabled	WR15 Bit D0 SDLC/HDLC Enhancement Enabled	WR7′ Bit D6 Extended Read Enabled	Functions Enabled
1	0	x	10 × 19 bit FIFO enhancement enabled only
0	1	0	SDLC/HDLC enhancements enabled only
0	1	1	SDLC/HDLC enhancements enabled with extended read enabled
1	1	0	10 × 19 bit FIFO and SDLC/HDLC enhancements enabled
1	1	1	10 × 19 bit FIFO and SDLC/HDLC enhancements with extended read enabled

When bit D2 of WR15 is set to "1," two additional registers (RR6 and RR7) per channel specific to the 10 × 19 bit Frame Status FIFO are made available. The ESCC register map when this function is enabled is shown in Table 6.

Table 6. 10 × 19 Bit FIFO Enabled

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	(RR0B)
0	1	0	1	WR5B	(RR1B)
0	1	1	0	WR6B	RR6B
0	1	1	1	WR7B	RR7B
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	(RR0A)
1	1	0	1	WR5A	(RR1A)
1	1	1	0	WR6A	RR6A
1	1	1	1	WR7A	RR7A
With the Point High command:					
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR13B
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	(RR15B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	(RR10B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	(RR13A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	(RR15A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	(RR10A)
1	1	1	1	WR15A	RR15A

Bit D0 of WR15 determines whether or not other enhancements pertinent only to SDLC/HDLC Mode operation are available for programming via WR7′ as shown below. Write Register 7 prime (WR7′) can be written to when bit D0 of WR15 is set to "1." When this bit is set, writing to WR7 (flag register) actually writes to WR7′. If bit D6 of this register is set to "1," previously unreadable registers WR3, WR4, WR5, and WR10 are readable by the processor. In addition, WR7′ is also readable by having this bit set. WR3 is read when a bogus RR9 register is accessed during a read cycle. WR10 is read by accessing RR11, and WR7′ is accessed by executing a read to RR14. The ESCC register map with bit D0 of WR15 and bit D6 of WR7′ set is shown in Table 7.

D7	D6	D5	D4	D3	D2	D1	D0
Must Be Set to 0	Ext. Read Enable	Rx comp. CRC	$\overline{DTR}/\overline{REQ}$ Fast Mode	Force TxD High	SDLC/HDLC Auto $\overline{RTS}$ Turnoff	SDLC/HDLC Auto EOM Reset	SDLC/HDLC Auto Tx Flag

WR7′—SDLC/HDLC Programmable Enhancements*

***Note:**
Options 3, 4, 5, and 6 may be used regardless of whether SDLC/HDLC mode is selected.

Table 7. SDLC/HDLC Enhancements Enabled

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	RR4B (WR4B)
0	1	0	1	WR5B	RR5B (WR5B)
0	1	1	0	WR6B	(RR2B)
0	1	1	1	WR7B	(RR3B)
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	RR4A (WR4A)
1	1	0	1	WR5A	RR5A (WR5A)
1	1	1	0	WR6A	(RR2A)
1	1	1	1	WR7A	(RR3A)
With the Point High command:					
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR9 (WR3B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	RR11B (WR10B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	RR14B (WR7′B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	RR9A (WR3A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	RR11A (WR10A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	RR14A (WR7A)
1	1	1	1	WR15A	RR15A

If both bits D0 and D2 of WR15 are set to "1" and D6 of WR7′ is set to "1," then the ESCC register map is as shown in Table 8.

Table 8. SDLC/HDLC Enhancements and 10 × 19 Bit FIFO Enabled

A/$\overline{B}$	PNT_2	PNT_1	PNT_0	Write	Read
0	0	0	0	WR0B	RR0B
0	0	0	1	WR1B	RR1B
0	0	1	0	WR2	RR2B
0	0	1	1	WR3B	RR3B
0	1	0	0	WR4B	RR4B (WR4B)
0	1	0	1	WR5B	RR5B (WR5B)
0	1	1	0	WR6B	RR6B
0	1	1	1	WR7B	RR7B
1	0	0	0	WR0A	RR0A
1	0	0	1	WR1A	RR1A
1	0	1	0	WR2	RR2A
1	0	1	1	WR3A	RR3A
1	1	0	0	WR4A	RR4A (WR4A)
1	1	0	1	WR5A	RR5A (WR5A)
1	1	1	0	WR6A	RR6A
1	1	1	1	WR7A	RR7A
With the Point High command:					
0	0	0	0	WR8B	RR8B
0	0	0	1	WR9	RR9 (WR3B)
0	0	1	0	WR10B	RR10B
0	0	1	1	WR11B	RR11B (WR10B)
0	1	0	0	WR12B	RR12B
0	1	0	1	WR13B	RR13B
0	1	1	0	WR14B	RR14B (WR7'B)
0	1	1	1	WR15B	RR15B
1	0	0	0	WR8A	RR8A
1	0	0	1	WR9	RR9A (WR3A)
1	0	1	0	WR10A	RR10A
1	0	1	1	WR11A	RR11A (WR10A)
1	1	0	0	WR12A	RR12A
1	1	0	1	WR13A	RR13A
1	1	1	0	WR14A	RR14A (WR7'A)
1	1	1	1	WR15A	RR15A

Auto $\overline{RTS}$ Reset

On the CMOS ESCC, if bit D0 of WR15 and bit D2 of WR7′ are set to "1" and the channel is in SDLC Mode, the $\overline{RTS}$ pin may be reset early in the Tx Underrun routine and the $\overline{RTS}$ pin will remain active until the last zero bit of the closing flag leaves the TxD pin as shown in Figure 16. Note that in order for this to function properly, bits D3 and D2 of WR10 must be set to "1" and "0" respectively.

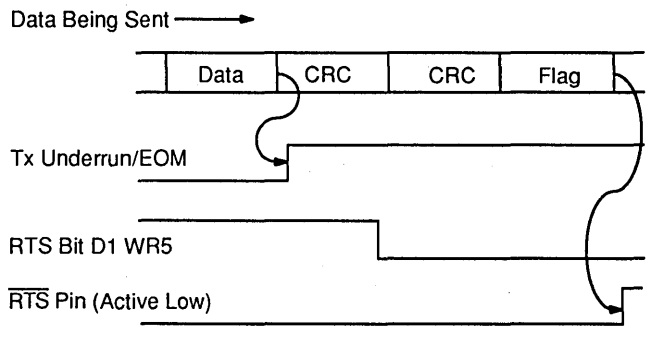

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Figure 41. Auto $\overline{RTS}$ Reset Mode

CRC Character Reception

NMOS Am8530H

On the NMOS Am8530H , when the end-of-frame flag is detected, the contents of the Receive Shift Register are transferred to the Receive Data FIFO regardless of the number of bits accumulated. Because of the 3-bit delay between the Receive SYNC Register and Receive Shift Register, the last two bits of the CRC check character received are never transferred to the Receive Data FIFO. Thus, the received CRC characters are unavailable for use.

CMOS ESCC

On the ESCC, the option of being able to receive the complete CRC characters generated by the Transmitter is provided when both bit D0 of WR15 and bit D5 of WR7' are set to "1." When these two bits are set and an end-of-frame flag is detected, the last two bits of the CRC will be clocked into the Receive Shift Register before its contents are transferred to the Receive Data FIFO.The data-CRC boundary and CRC character bit formatsfor each Residue Code provided is shown in Figures 42A through 42D for each character length selected.

Residue Code 012/001

D	D	D	D	D	C_0	C_1	C_2
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/101

D	D	D	D	D	D	C_0	C_1
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/100

D	D	D	D	D	D	D	C_0
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/010

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/110

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 42A. 5 Bits/Character

Residue Code 012 010

D	D	D	D	D	D	C_0	C_1
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 110

D	D	D	D	D	D	D	C_0
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 001

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 101

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 011

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012 100

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 42B. 6 Bits/Character

Residue Code 012/111

D	D	D	D	D	D	D	C_0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/100

D	D	D	D	D	D	D	D
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/010

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/110

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/001

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/101

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/011

D	D	D	D	D	D	D	D
D	D	D	D	D	D	C_0	C_1
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 42C. 7 Bits/Character

Residue Code 012/011 (No Residue)

D	D	D	D	D	D	D	D
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/111 (1 Residue Bit)

D	D	D	D	D	D	D	D
D	C_0	C_1	C_2	C_3	C_4	C_5	C_6
C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/000 (2 Residue Bits)

D	D	D	D	D	D	D	D
D	D	C_0	C_1	C_2	C_3	C_4	C_5
C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/100 (3 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	C_0	C_1	C_2	C_3	C_4
C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/010 (4 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	C_0	C_1	C_2	C_3
C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/110 (5 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	C_0	C_1	C_2
C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/001 (6 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	D	C_0	C_1
C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

Residue Code 012/101 (7 Residue Bits)

D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	C_0
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

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Figure 42D. 8 Bits/Character

Auto Flag Mode

On the NMOS Am8530H, if the transmitter is actively mark idling and a frame of data is ready to be transmitted, the MARK/FLAG idle bit must be set to "0" before data is written to WR8, otherwise the opening flag will not be sent properly. However, care must be exercised in doing this because the mark idle pattern (eight "1" bits) is transmitted eight bits at a time, and all eight bits must have transferred out the Transmit Shift Register before a flag may be loaded and sent. If data is written into the Transmit Buffer (WR8) before the flag is loaded into the Transmit Shift Register, the data character written to WR8 will supersede flag transmission and the opening flag will not be transmitted.

On the CMOS ESCC, if bit D0 of WR15 is set to "1," and the ESCC is programmed for SDLC operation, an option is provided via bit D0 of WR7′ that eliminates this requirement. If bit D0 of WR7′ is set to "1" and a character is written to the Transmit Buffer while the Transmitter is mark idling, the Mark/Flag Idle bit in WR10 need not be reset to "0" in order to have the opening flag sent because the Transmitter will automatically send it before commencing to send data.

In addition, as long as bit D0 of WR15 and bit D1 of WR7′ are set to "1," the CRC transmit generator will be automatically preset to the initial state programmed by bit D7 of WR10 (so the Reset Tx CRC Generator command is also not necessary), and the Tx Underrun/EOM latch will be reset automatically on every new frame sent. This ensures that an opening flag and proper CRC generation and transmission will always be sent without processor intervention under varying bus latency conditions.

Auto Transmit CRC Generator Preset

The NMOS Am8530H does not automatically preset the CRC generator prior to frame transmission. This must be done in software, usually during the initialization routine. This is accomplished by issuing the Reset Tx CRC Generator Command via WR0. For proper results, this command must be issued while the transmitter is enabled and idling and before any data are written to the Transmit Buffer.

In addition, if CRC is to be used, the transmit CRC generator must be enabled by setting bit D0 of WR5 to "1." CRC is normally calculated on all characters between opening and closing flags, so this bit should be set to "1" at initialization and never changed.

On the CMOS ESCC, setting bit D0 of WR15 to "1" will cause the transmit CRC generator to be preset automatically every time an opening flag is sent, so the Reset Tx CRC Generator Command is not necessary.

Auto Tx Underrun/EOM Latch Reset

On the ESCC, the transmission of the CRC check characters is controlled by the Transmit CRC Enable bit in WR5 (D0) and the Tx Underrun/EOM bit in RR0 (D6). However, if the Transmit Enable bit is set to "0" when a transmit underrun (i.e., both the Transmit Buffer and Transmit Shift Register go empty) occurs, the CRC check characters will not be sent regardless of the state of the Tx Underrun/EOM bit.

If the Transmit Enable bit is set to "1" when an underrun occurs, then the state of the Tx Underrun/EOM bit and the Abort/Flag on Underrun bit in WR10 (D2) determine the action taken by the Transmitter. The Abort/Flag on Underrun bit may be set or reset by the processor, whereas, the Tx Underrun/EOM bit is set by the Transmitter and can only be reset by the processor via the Reset Tx Underrun/EOM Command in WR0.

If the Tx Underrun/EOM bit is set to "1" when an underrun occurs, the Transmitter will close the frame by sending a flag; however, if this bit is set to "0," the frame data will be appended with either the accumulated CRC characters followed by a flag or an abort pattern followed by a flag, depending on the state of the Abort/Flag on Underrun bit in the WR10 (D2). In either case, after the closing flag is sent, the Transmitter will idle the transmission line as specified by the Mark/Flag Idle bit D3 in WR10.

Hence, if the CRC check characters are to be properly appended to a frame, the Abort/Flag on Underrun bit must be set to "0," and the Reset Tx Underrun/EOM Command must be issued after the first but before the last character is written to the Transmit Buffer. This will ensure that either an abort or the CRC will be transmitted if an underrun occurs. Normally, the Abort/Flag on Underrun bit in WR10 should be set to "1" around the same time that the Tx Underrun/EOM bit is reset so that an abort will be sent if the transmitter accidentally underruns, and then set to "0" near the end of the frame to allow the correct transmission of CRC.

On the ESCC, if bit D0 of WR15 is set to "1," the option of having the Tx Underrun/EOM bit reset automatically at the start of every frame is provided via bit D1 of WR7′. This helps alleviate the software burden of having to respond within one character time when high-speed data are being sent.

SDLC/HDLC NRZI Transmitter Disabling

On the NMOS Am8530H, if NRZI encoding is being used and the Transmitter is disabled, the state of the TxD pin will depend on the last bit sent. That is, the TxD pin may either idle in a Low or High state as shown in Figure 43.

On the CMOS ESCC, an option is provided that allows setting the TxD pin High when operating in SDLC Mode with NRZI encoding enabled. If bit D0 of WR15 is set to "1," then bit D3 of WR7′ can be used to set the TxD pin High. Note that the operation of this bit is independent of the Tx Enable bit in WR5. The Tx Enable bit in WR5 is used to disable and enable the transmitter, whereas bit D3 of WR7′ acts as a pseudo transmitter disable and enable by just forcing the TxD pin High when set even though the transmitter may actually be mark or flag idling. Care must be used when setting this bit because any character being transmitted at the time this bit is set will be "chopped off," and data written to the Transmit Buffer while this bit is set will be lost.

When the transmit underrun occurs and the CRC and closing flag have been sent, bit D3 can be set to pull TxD High. When ready to start sending data again this bit must be reset to "0" before the first character is written to the Transmit Buffer. Note that resetting this bit causes the TxD pin to take whatever state the NRZI encoder is in at the time so synchronization at the Receiver may take longer because the first transition seen on the TxD pin may not coincide with a bit boundary. Note that in order for this to function properly, bits D3 and D2 of WR10 must be set to "1" and "0" respectively.

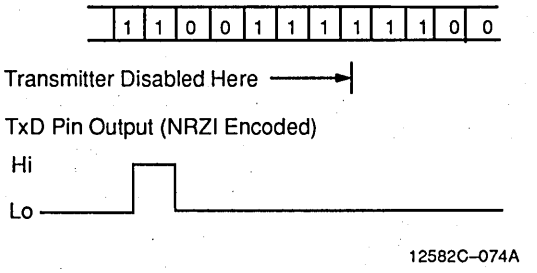


Figure 43. Transmitter Disabling with NRZI Encoding

Interrupt Masking Without $\overline{\text{INTACK}}$

The NMOS Am8530H's ability to mask lower priority interrupts is done via the IUS bit. This bit is internal to the ESCC and is not observable by the processor. Being able to automatically mask lower priority interrupts allows a modular approach to coding interrupt routines. However, using the masking capabilities of the NMOS ESCC requires that the $\overline{\text{INTACK}}$ cycle be generated. In stand-alone applications, having to generate $\overline{\text{INTACK}}$ through external hardware in order to use this capability is an unnecessary expense.

On the CMOS ESCC, if bit D5 in WR9 is set to "1," the $\overline{\text{INTACK}}$ cycle does not need to be generated in order to have the IUS bit set. This allows the user to respond to ESCC interrupt requests with a software acknowledgment through RR2. When bit D5 in WR9 is set and an interrupt occurs, a read to RR2 emulates a hardware Interrupt Acknowledge cycle as it functions in Vectored Mode. In this case the CPU must first read RR2 to determine the internal interrupt source and then jump to the appropriate interrupt routine. Reading RR2 sets the IUS bit for the highest priority IP. After the interrupting condition is cleared, the routine can then read RR3 to determine if any other IPs are set and clear them. At the end of the interrupt routine, a Reset IUS Command must be issued to unlock the internal daisy chain.

Since the CPU can acknowledge the ESCC of highest priority with a read of its RR2 interrupt vector, there is no need for an external daisy chain. When acknowledging an ESCC interrupt request, the CPU must issue one read to RR2 per interrupt request. The modified interrupt vector can be read from Channel B, or the original vector stored in WR2 can be read from Channel A. Either action will produce the same internal actions on the IUS logic. Note that the No Vector and Vector Includes Status bits in WR9 are ignored when bit D5 in WR9 is set to "1."

1 Mb/s FM Data Transmission and Reception

The 8-MHz version of the CMOS ESCC (ESCC-8) is capable of transmitting and receiving FM-encoded data at the rate of 1 Mb/s. This is accomplished by applying a 16-MHz clock to the $\overline{\text{RTxC}}$ pin and assigning this waveform to drive the Internal Digital Phase Locked Loop (DPLL) clock. This feature allows the user to send both clock and data information over the same line at 1 Mb/s and can eliminate external DPLLs required for high-speed NRZ data clock generation.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Voltage at any Pin	
Relative to V_{SS}	−0.5 to +7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+5 V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IH}	Input High Voltage	Commercial	2.2	V_{CC} +0.3*	V
V_{IL}	Input Low Voltage		−0.3*	0.8	V
V_{OH1}	Output High Voltage	I_{OH} = −3.0 mA	2.4		V
V_{OH2}	Output High Voltage	I_{OH} = −250 µA (Note 2)	V_{CC}−0.8		V
V_{OL1}	Output Low Voltage	I_{OL} = +2.4 mA		0.5	V
V_{OL2}	Output Low Voltage	I_{OL} = +48 mA (Note 1)		0.5	V
I_{IL}	Input Leakage	0.4 V ≤ V_{IN} ≤ 2.4 V		±10.0	µA
	SCSI Bus Pins Except $\overline{RST}$	V_{IH} = 5.25 V, V_{IL} = 0		±50	µA
I_{OL}	Output Leakage	0.4 V ≤ V_{OUT} ≤ 2.4 V		±10.0	µA
I_{CC}	V_{CC} Supply Current	CLK = 8 MHz, inputs at voltage rails, output unloaded		40	mA
C_{IN}	Input Capacitance	Unmeasured pins returned to ground. f = 1 MHz over specified temperature range		10	pF
C_{OUT}	Output Capacitance			15	pF
C_{MO}	Bidirectional Capacitance Except SCSI Bus Pins			20	pF

* V_{IH} Max. and V_{IL} Min. not tested. Guaranteed by design.

Notes:

1. SCSI Bus Pins only.
2. SCC outputs only.

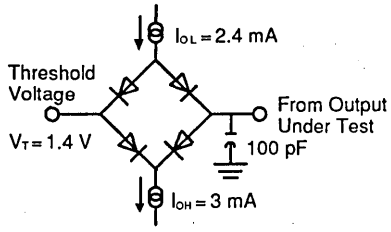
Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75 V ≤ V_{CC} ≤ +5.25 V
GND = 0 V
0°C ≤ T_A ≤ 70°C

SWITCHING TEST CIRCUITS

Standard Test Dynamic Load Circuit



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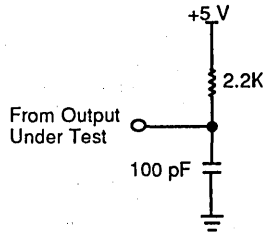
Open-Drain Test Load



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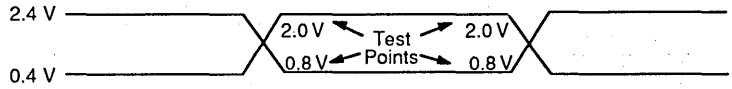
SWITCHING TEST INPUT/OUTPUT WAVEFORM



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AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for logic "0."

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

ESCC SWITCHING CHARACTERISTICS over COMMERCIAL operating range
General Timing (see Figure 44)

No.	Parameter Symbol	Parameter Description	8.192 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay		250		80	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		180	ns
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (Notes 1, 4 & 8)	NA	NA	NA	NA	
4	TsRXD(RXCr)	RxD to RxC ↑ Setup Time (XI Mode) (Note 1)	0		0		ns
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (XI Mode) (Note 1)	150		50		ns
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (XI Mode) (Notes 1, 5)	0		0		ns
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (XI Mode) (Notes 1, 5)	150		50		ns
8	TsSY(RXC)	SYNCA to RxC ↑ Setup Time (Note 1)	–200		–100		ns
9	ThSY(RXC)	SYNCA to RxC ↑ Hold Time (Note 1)	5TcPc		5TcPc		ns
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time (Notes 2, 4 & 8)	NA		NA		
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (XI Mode) (Note 2)		200		80	ns
12	TdTXCr(TXD)	TxC ↑ to TxD Delay (XI Mode) (Notes 2, 5)		200		80	ns
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200		80	ns
14a	TwRTXh	RTxC High Width (Note 6)	150		80		ns
14b	TwRTxh(E)	RTxC High Width (Note 9)	50		15.6		ns
15a	TwRTXl	RTxC Low Width (Note 6)	150		80		ns
15b	TwRTXl(E)	RTxC Low Width (Note 9)	50		15.6		ns
16a	TcRTX	RTxC Cycle Time (Notes 6, 7)	488		244		ns
16b	TcRTx(E)	RTxC Cycle Time (Note 9)	125		31.25		ns
17	TcRTXX	Crystal Oscillator Period (Note 3)	125	1000	62	1000	ns
18	TwTRXh	TRxC High Width (Note 6)	150		80		ns
19	TwTRXl	TRxC Low Width (Note 6)	150		80		ns
20	TcTRX	TRxC Cycle Time (Notes 6, 7)	488		244		ns
21	TwEXT	DCD Pulse Width	200		70		ns
22	TwSY	SYNCA Pulse Width	200		70		ns

Notes:

1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNCA have 30-pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver, DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.
8. External PCLK to RxC or TxC synchronization requirement eliminated for PCLK divide-by-four operation.
   TRxC and RTxC rise and fall times are identical to PCLK. Reference timing specs Tfpc and Trpc.
   Tx and Rx input clock slow rates should be kept to a maximum of 30 nsec. All parameters related to input CLK edges should be referenced at the point at which the transition begins or ends, whichever is worst case.
9. ENHANCED FEATURE— RTxC used as input to internal DPLL only.

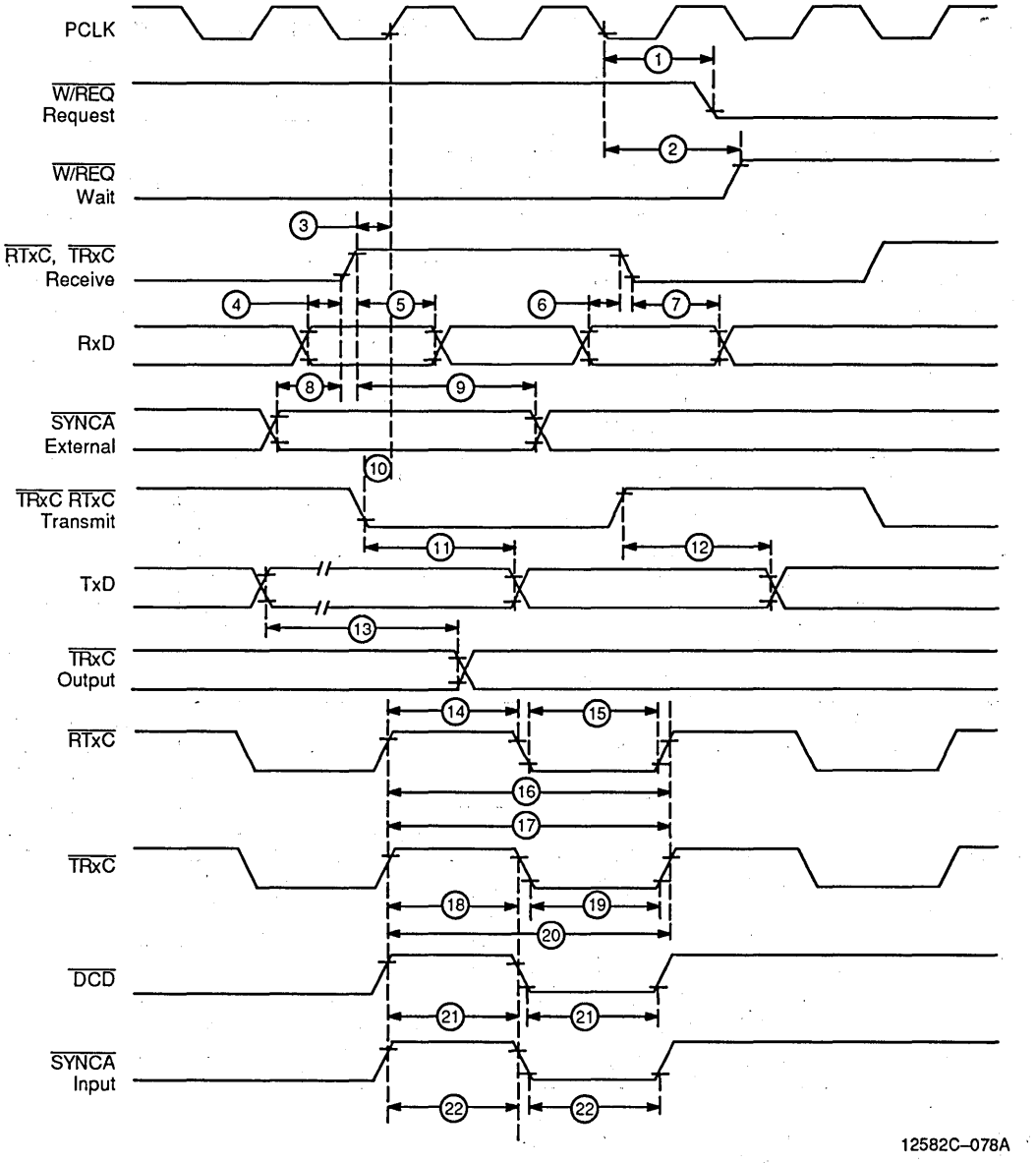

Figure 44. General Timing

ESCC SWITCHING CHARACTERISTICS over COMMERCIAL operating range (continued)
System Timing (see Figure 45)

No.	Parameter Symbol	Parameter Description	8.192 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TdRXC(REQ)	$\overline{RXC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	8	12	TcPc
2	TdRXC(W)	$\overline{RXC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	8	14	TcPc
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	4	7	TcPc
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	10	16	TcPc
5	TdTXC(REQ)	$\overline{TxC}$ ↑ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	5	8	TcPc
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	5	11	TcPc
7a	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	4	7	TcPc
7b	TdTXC(EDRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Notes 3, 4)	5	8	5	8	TcPc
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	6	10	TcPc
9	TdSY(INT)	$\overline{SYNCA}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPc
10	TdEXT(INT)	$\overline{DCD}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	2	6	TcPc

Notes:

1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
4. Parameter applies to Enhanced Request mode only.

ESCC SWITCHING CHARACTERISTICS over COMMERCIAL operating range (continued)
Read and Write Timing (see Figure 46)

No.	Parameter Symbol	Parameter Description	8.192 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TwPCl	PCLK Low Width	50	2000	26	2000	ns
2	TwPCh	PCLK High Width	50	2000	26	2000	ns
3	TfPC	PCLK Fall Time		15		8	ns
4	TrPC	PCLK Rise Time		15		8	ns
5	TcPC	PCLK Cycle Time	122	4000	61	4000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	70		35		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	70		35		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		ns
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	20		15		ns
11	TsIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time (Note 1)	145		70		ns
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
13	TsIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time (Note 1)	145		70		ns
14	ThIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		ns
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	40		15		ns
16	TsCEI(WR)	$\overline{CE1}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		ns
17	ThCE(WR)	$\overline{CE1}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns
18	TsCEh(WR)	$\overline{CE1}$ High to $\overline{WR}$ ↓ Setup Time	60		30		ns
19	TsCEI(RD)	$\overline{CE1}$ Low to $\overline{RD}$ ↓ Setup Time (Note 1)	0		0		ns
20	ThCE(RD)	$\overline{CE1}$ to $\overline{RD}$ ↑ Hold Time (Note1)	0		0		ns
21	TsCEh(RD)	$\overline{CE1}$ High to $\overline{RD}$ ↓ Setup Time (Note 1)	60		30		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	150		75		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		140		70	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		40		20	ns

Notes:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time at which the data bus is released from its drive state with a maximum DC Load and minimum AC load.

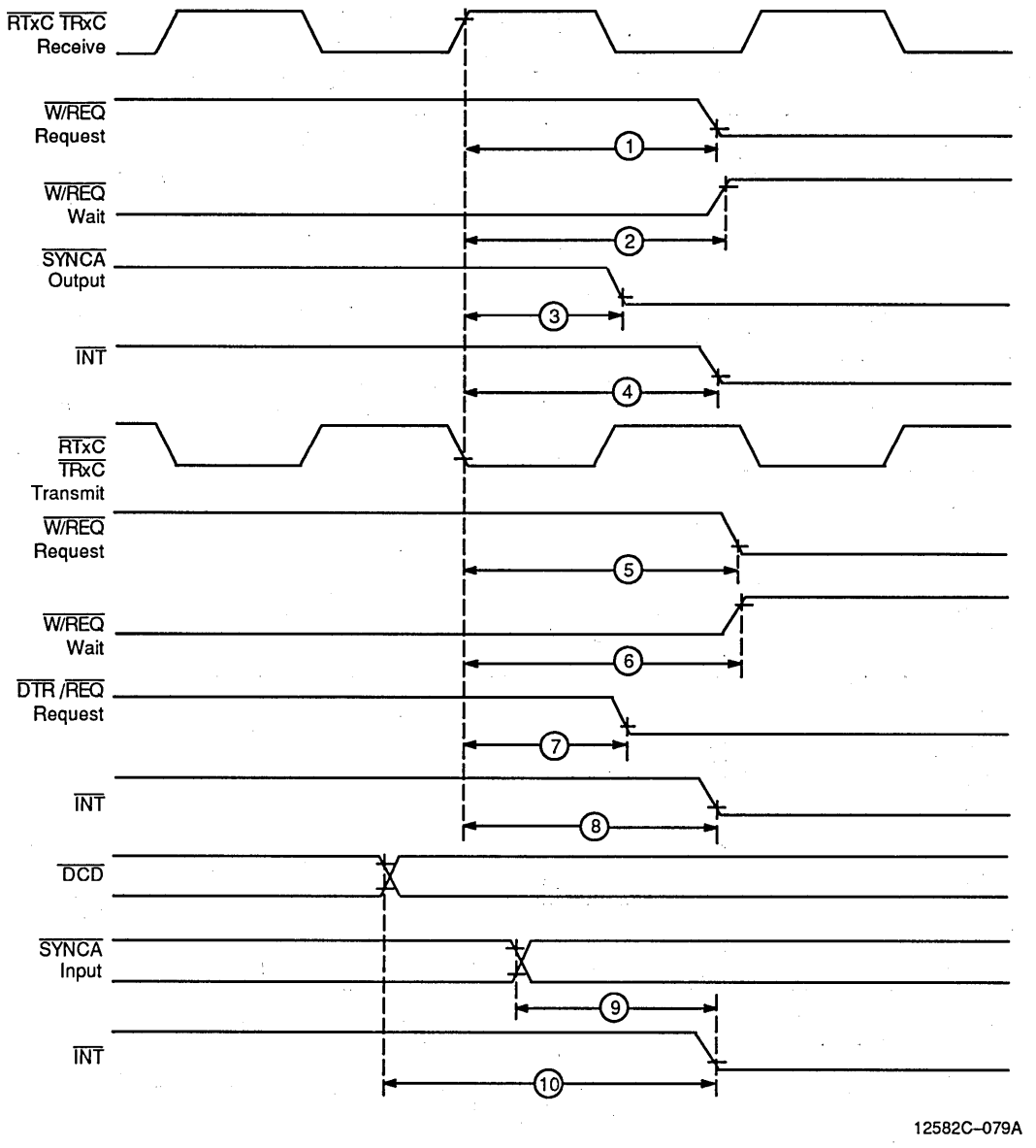

Figure 45. System Timing

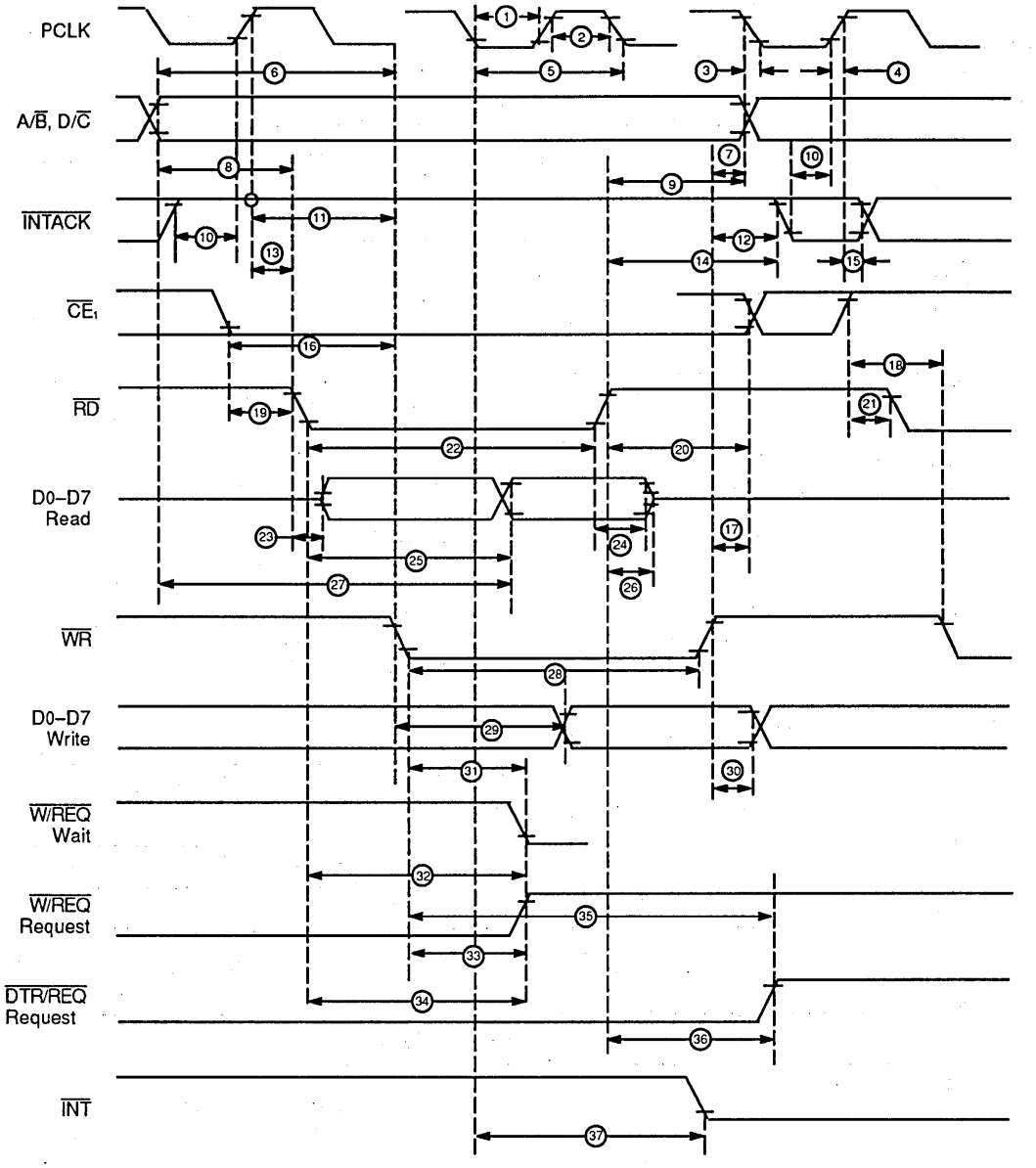

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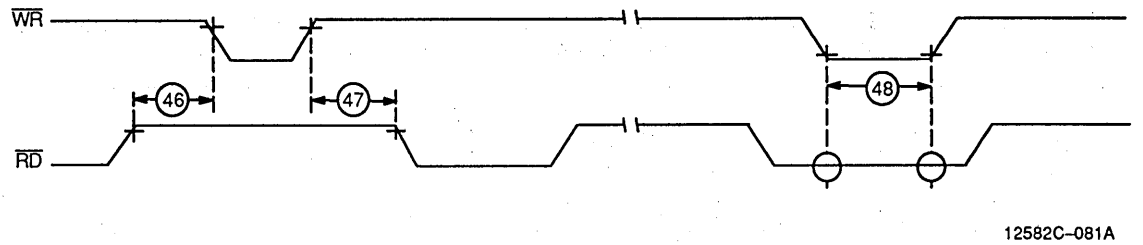
Figure 46. Read and Write Timing

ESCC SWITCHING CHARACTERISTICS over COMMERCIAL operating range (continued)
Interrupt Acknowledge Timing, Reset Timing, Cycle Timing (see Figures 47–49)

No.	Parameter Symbol	Parameter Description	8.192 MHz		16.384 MHz		Unit
			Min.	Max.	Min.	Max.	
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		220		100	ns
28	TwWRI	$\overline{WR}$ Low Width	150		75		ns
29	TdWRf(DW)	$\overline{WR}$ ↓ to Write Data Valid		35		20	ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		10		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 2)		170		50	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 2)		170		50	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		70	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		170		70	ns
35a	TdWRr(REQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		4.0TcPc		4.0TcPc	ns
35b	TdWRr(EREQ)	$\overline{WR}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		120		70	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ $\overline{DTR/REQ}$ Not Valid Delay		NA		NA	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 2)		500		175	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay	150		50		ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	150		75		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		140		70	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time			50		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time			0		ns
43	TdIE(IEO)	IEI to IEO Delay Time				45	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay				80	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 2)		450		200	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	15		10		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	15		10		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	150		75		ns
49	Trc	Valid Access Recovery Time (Note 1)	3.5		3.5		TcPc

Notes:

1. Parameter applies only between transactions involving the ESCC, if $\overline{WR}/\overline{RD}$ falling edge is synchronized to PCLK falling edge, then TrC = 3TcPc.
2. Open-drain output, measured with open-drain test load.



12582C–081A

Figure 47. Reset Timing

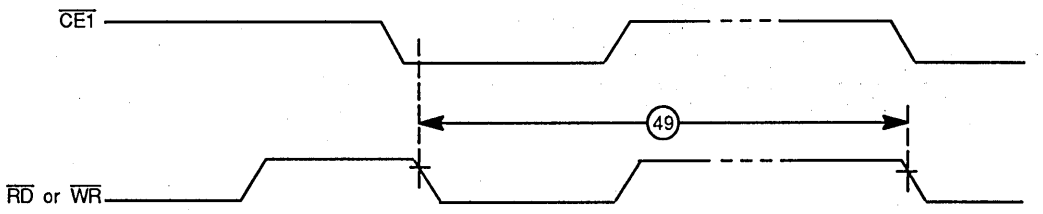


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Figure 48. Cycle Timing

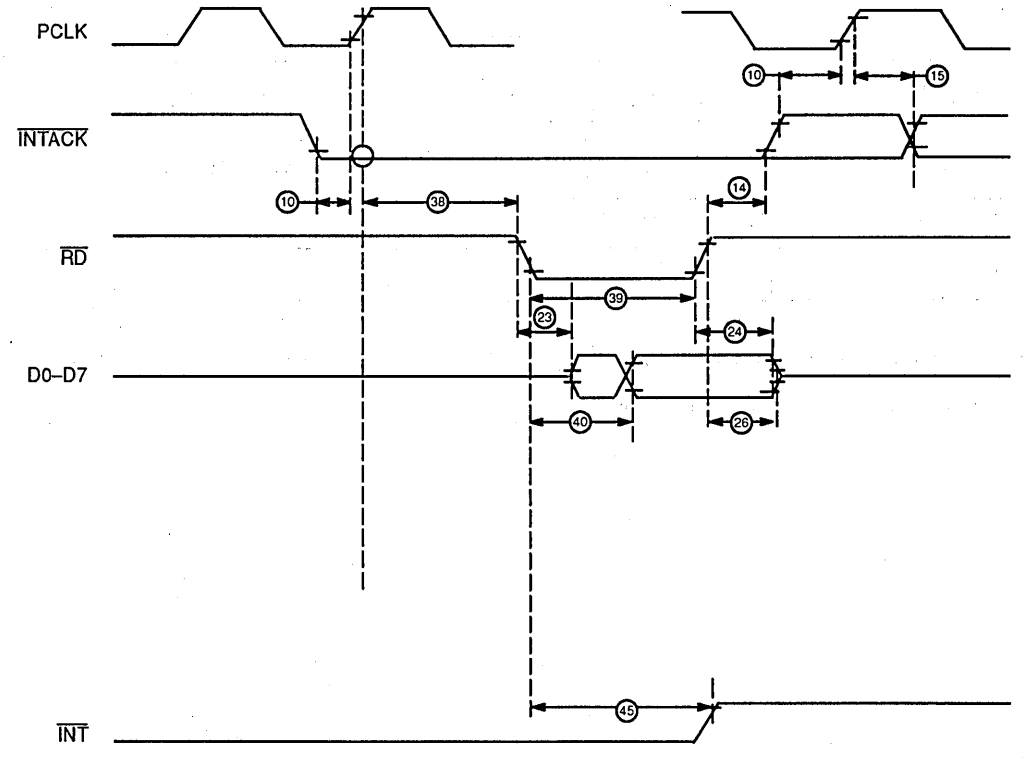

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Figure 49. Interrupt Acknowledge Timing

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS
DMA Write (Non-Block Mode) Target Send Cycle (see Figure 50)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	DRQ False from $\overline{DACK}$ True		100	ns
T2	$\overline{DACK}$ False to DRQ True	30		ns
T3	Write Enable Width*	70		ns
T4	DACK Hold from End of $\overline{WR}$	0		ns
T5	Data Setup to End of Write Enable*	30		ns
T6	Data Hold Time from End of $\overline{WR}$	40		ns
T7	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T8	$\overline{ACK}$ True to $\overline{REQ}$ False		125	ns
T9	$\overline{REQ}$ from End of $\overline{DACK}$ ($\overline{ACK}$ False)		120	ns
T10	$\overline{ACK}$ True to DRQ True (Target)		110	ns
T11	$\overline{REQ}$ from End of $\overline{ACK}$ ($\overline{DACK}$ False)		120	ns
T12	Data Hold from Write Enable	*0		ns
T13	Data Setup to $\overline{REQ}$ True (Target)	60		ns

*Write Enable is the occurrence of $\overline{WR}$ and $\overline{DACK}$

Note:

1. $\overline{EOP}$, $\overline{WR}$, and $\overline{DACK}$ must be concurrently True for at least T7 for proper recognition of the $\overline{EOP}$ pulse.

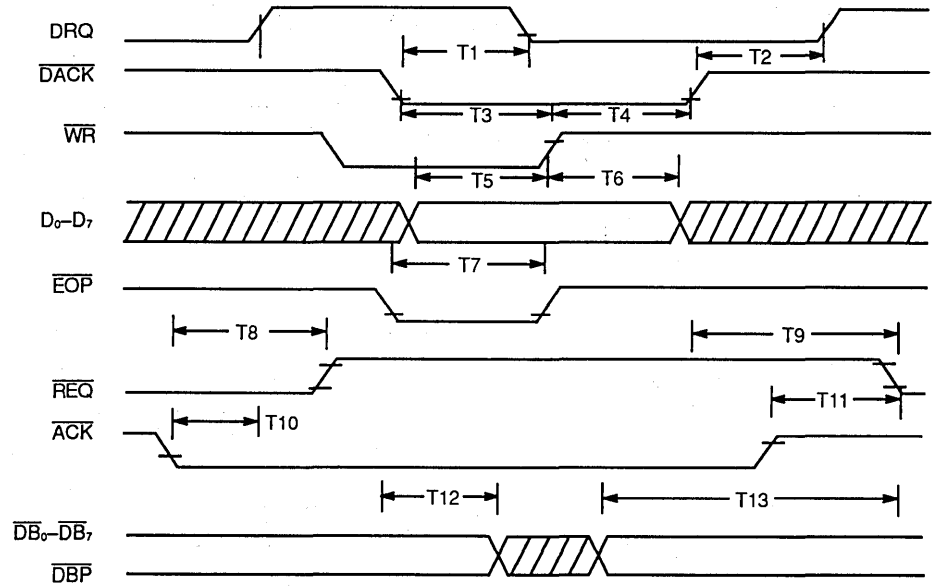

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Figure 50. DMA Write (Non-Block Mode) Target Send Cycle

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)
DMA Write (Non-Block Mode) Initiator Send Cycle (see Figure 51)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	DRQ False from $\overline{DACK}$ True		100	ns
T2	$\overline{DACK}$ False to DRQ True	30		ns
T3	Write Enable Width*	70		ns
T4	$\overline{DACK}$ Hold from End of $\overline{WR}$	0		ns
T5	Data Setup to End of Write Enable*	30		ns
T6	Data Hold Time from End of $\overline{WR}$	40		ns
T7	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T8	$\overline{REQ}$ True to $\overline{ACK}$ True		110	ns
T9	$\overline{REQ}$ False to DRQ True		110	ns
T10	$\overline{DACK}$ False to $\overline{ACK}$ False		130	ns
T11	$\overline{WR}$ False to Valid SCSI Data		100	ns
T12	Data Hold from Write Enable	*0		ns

*Write Enable is the occurrence of $\overline{WR}$ and $\overline{DACK}$

Note:

1. $\overline{EOP}$, $\overline{WR}$, and $\overline{DACK}$ must be concurrently True for at least T7 for proper recognition of the $\overline{EOP}$ pulse.

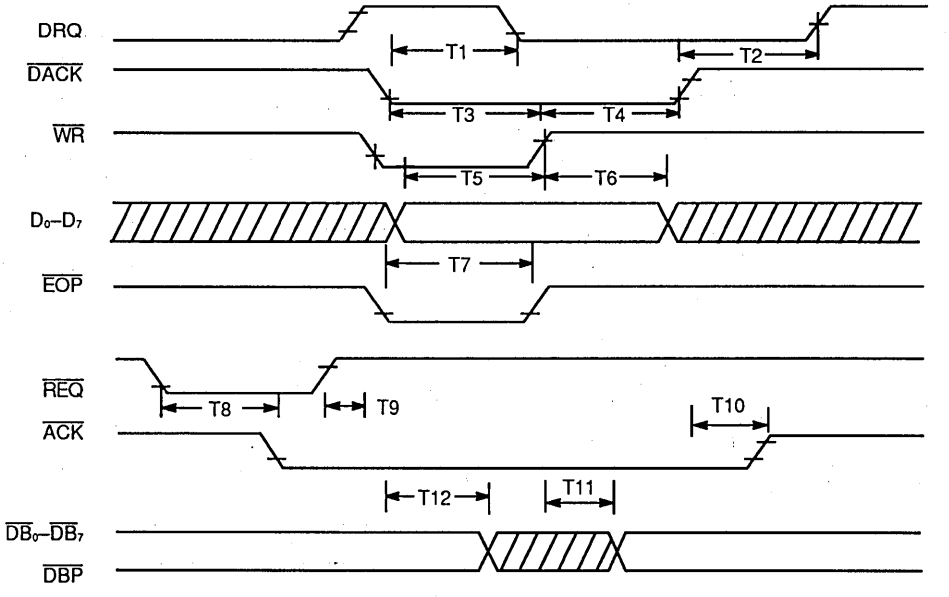

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Figure 51. DMA Write (Non-Block Mode) Initiator Send Cycle

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)
DMA Read (Non-Block Mode) Target Receive Cycle (see Figure 52)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	DRQ False from $\overline{DACK}$ True		100	ns
T2	$\overline{DACK}$ False to DRQ True	30		ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{RD}$	0		ns
T4	Data Access Time from Read Enable*		100	ns
T5	Data Hold Time from End of $\overline{RD}$	0		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T7	$\overline{ACK}$ True to DRQ True		110	ns
T8	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		120	ns
T9	$\overline{ACK}$ True to $\overline{REQ}$ False		125	ns
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		120	ns
T11	Data Setup Time to $\overline{ACK}$	10		ns
T12	Data Hold Time from $\overline{ACK}$	65		ns

*Read Enable is the occurrence of $\overline{RD}$ and $\overline{DACK}$

Note:

1. $\overline{EOP}$, $\overline{RD}$, and $\overline{DACK}$ must be concurrently True for at least T6 for proper recognition of the $\overline{EOP}$ pulse.

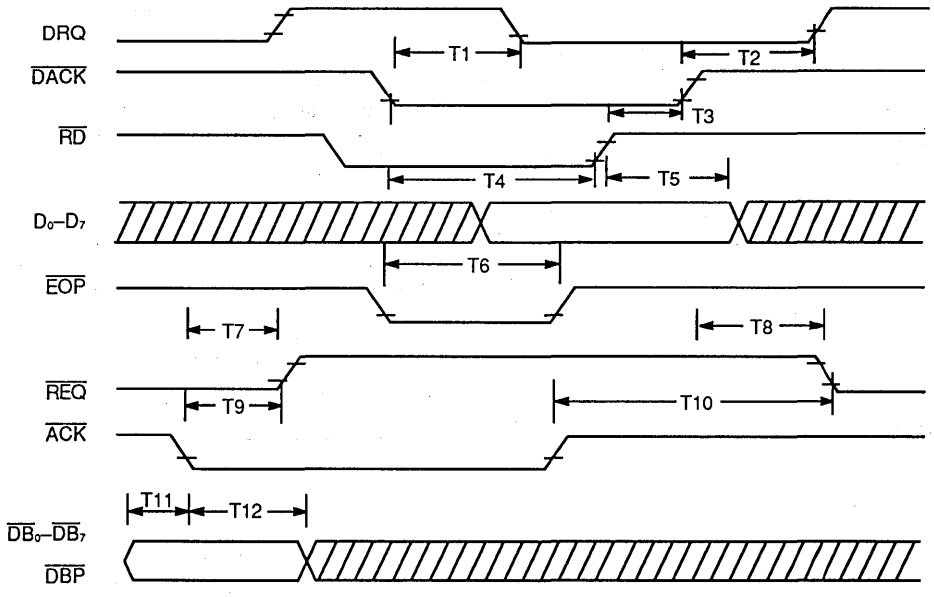

Figure 52. DMA Read (Non-Block Mode) Target Receive Cycle

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)
DMA Read (Non-Block Mode) Initiator Receive Cycle (see Figure 53)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	DRQ False from $\overline{DACK}$ True		100	ns
T2	$\overline{DACK}$ False to DRQ True	30		ns
T3	$\overline{DACK}$ Hold Time from End of $\overline{RD}$	0		ns
T4	Data Access Time from Read Enable*		100	ns
T5	Data Hold Time from End of $\overline{RD}$	0		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T7	$\overline{REQ}$ True to DRQ True		140	ns
T8	$\overline{DACK}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		100	ns
T9	$\overline{REQ}$ True to $\overline{ACK}$ True		110	ns
T10	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)		100	ns
T11	Data Setup Time to $\overline{REQ}$	10		ns
T12	Data Hold Time from $\overline{REQ}$	65		ns

*Read Enable is the occurrence of $\overline{RD}$ and $\overline{DACK}$

Note:

1. $\overline{EOP}$, $\overline{RD}$, and $\overline{DACK}$ must be concurrently True for at least T6 for proper recognition of the $\overline{EOP}$ pulse.

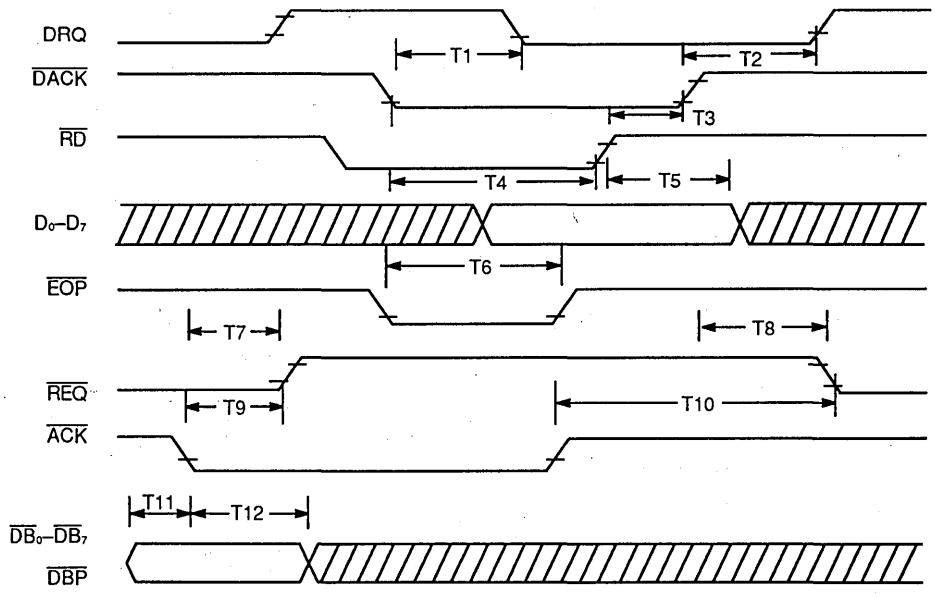

Figure 53. DMA Read (Non-Block Mode) Initiator Receive Cycle

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)
DMA Write (Block Mode) Target Send Cycle (see Figure 54)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	DRQ False from $\overline{DACK}$ True		100	ns
T2	Write Enable Width*	70		ns
T3	Write Recovery Time	120		ns
T4	Data Setup to End of Write Enable*	30		ns
T5	Data Hold Time from End of $\overline{WR}$	40		ns
T6	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T7	$\overline{ACK}$ True to $\overline{REQ}$ False		125	ns
T8	$\overline{REQ}$ from End of $\overline{WR}$ ($\overline{ACK}$ False)		130	ns
T9	$\overline{REQ}$ from End of $\overline{ACK}$ ($\overline{WR}$ False)		110	ns
T13	Data Hold from $\overline{ACK}$ True	0		ns
T14	Data Setup to $\overline{REQ}$ True	60		ns

*Write Enable is the occurrence of $\overline{WR}$ and $\overline{DACK}$

Note:

1. $\overline{EOP}$, $\overline{WR}$, and $\overline{DACK}$ must be concurrently True for at least T6 for proper recognition of the $\overline{EOP}$ pulse.

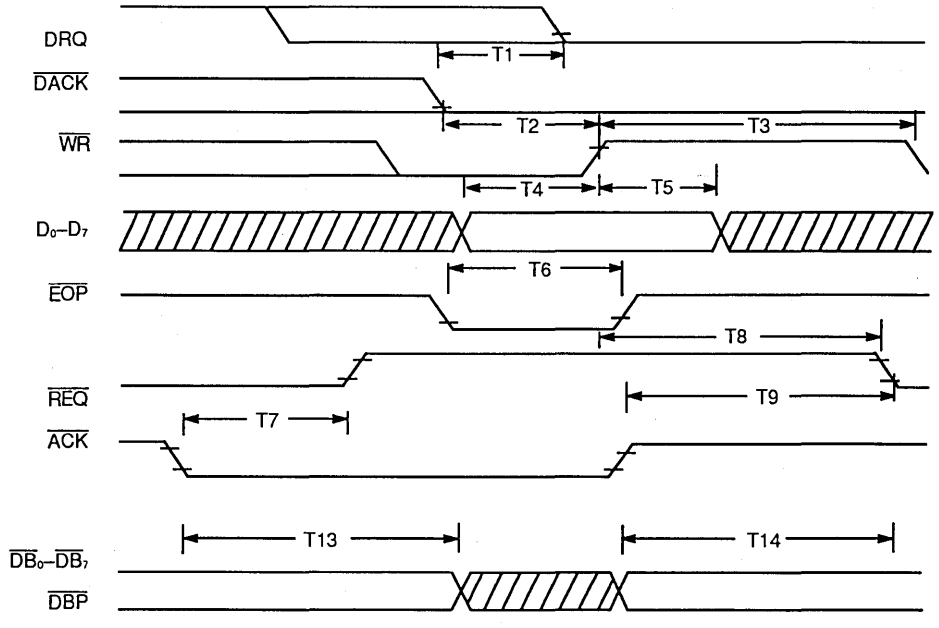

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Figure 54. DMA Write (Block Mode) Target Send Cycle

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)
DMA Read (Block Mode) Target Receive Cycle (see Figure 55)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	DRQ False from $\overline{DACK}$ True		100	ns
T2	$\overline{RD}$ Recovery Time	120		ns
T3	Data Access Time from Read Enable*		100	ns
T4	Data Hold Time from End of $\overline{RD}$	0		ns
T5	Width of $\overline{EOP}$ Pulse (Note 1)	70		ns
T6	$\overline{RD}$ False to $\overline{REQ}$ True (ACK False)		130	ns
T7	$\overline{ACK}$ True to $\overline{REQ}$ False		125	ns
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{RD}$ False)		110	ns
T12	Data Setup Time to $\overline{ACK}$	*10		ns
T13	Data Hold Time from $\overline{ACK}$	65		ns

*Read Enable is the occurrence of $\overline{RD}$ and $\overline{DACK}$

Note:

1. $\overline{EOP}$, $\overline{RD}$, and $\overline{DACK}$ must be concurrently True for at least T5 for proper recognition of the $\overline{EOP}$ pulse.

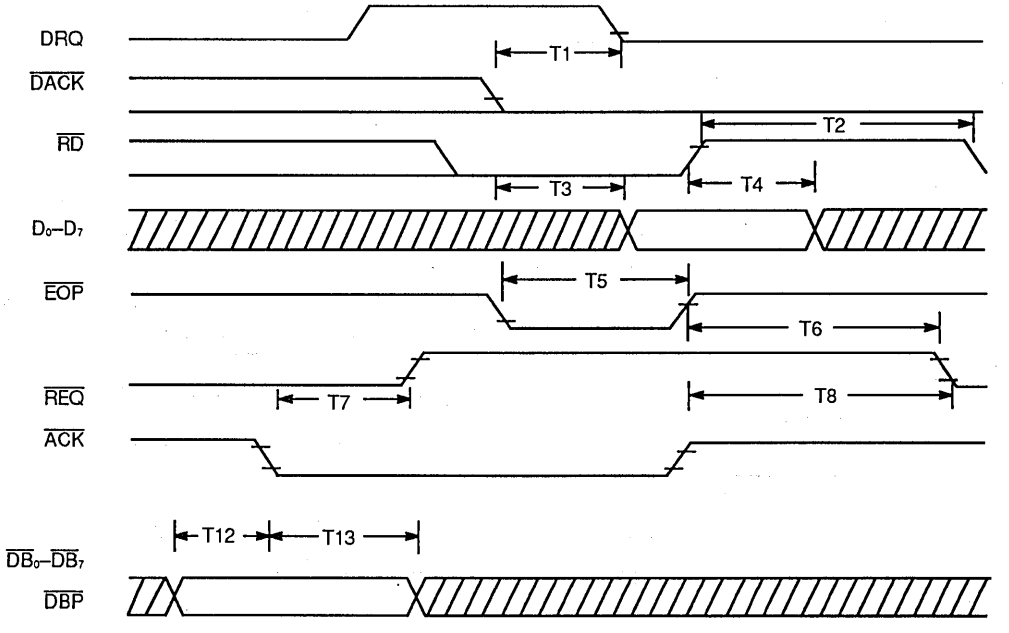
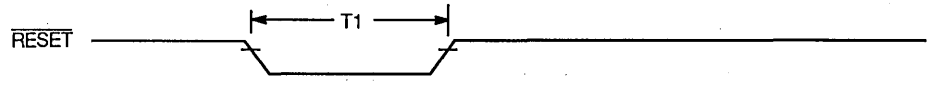


Figure 55. DMA Read (Block Mode) Target Receive Cycle

SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)

Reset

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	Minimum Width of $\overline{\text{RESET}}$	100		ns



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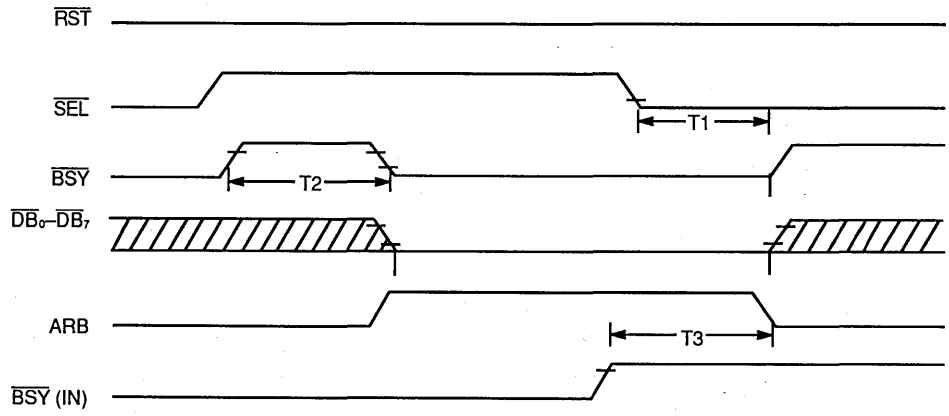
Arbitration

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	Bus Clear from $\overline{\text{SEL}}$ True		600	ns
T2	Arbitrate Start from $\overline{\text{BSY}}$ False	1200	2400	ns
T3	Bus Clear from $\overline{\text{BSY}}$ False		1100	ns



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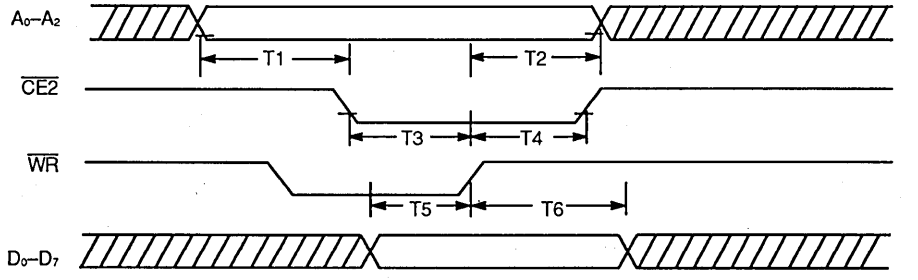
SCSI SWITCHING CHARACTERISTICS/WAVEFORMS (Continued)

CPU Write Cycle

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	Address Setup to Write Enable*	10		ns
T2	Address Hold from End Write Enable*	0		ns
T3	Write Enable Width*	40		ns
T4	Chip Select Hold from End of $\overline{WR}$	0		ns
T5	Data Setup to End of Write Enable*	20		ns
T6	Data Hold Time from End of $\overline{WR}$	30		ns

*Write Enable is the occurrence of $\overline{WR}$ and $\overline{CE2}$.



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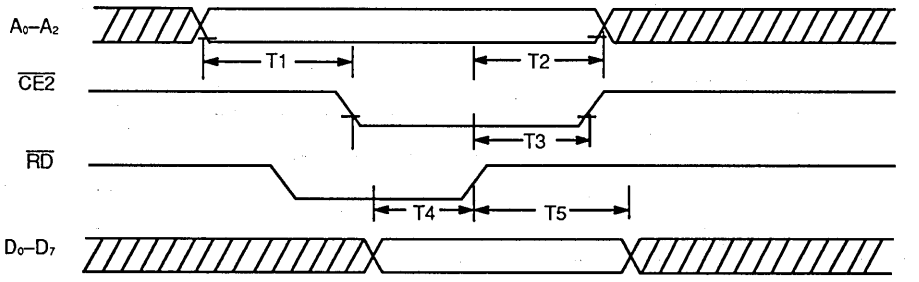
CPU Read Cycle

Parameter Symbol	Parameter Description	Min.	Max.	Unit
T1	Address Setup to Read Enable*	10		ns
T2	Address Hold from End Read Enable*	0		ns
T3	Chip Select Hold from End of $\overline{RD}$	0		ns
T4	Data Access Time from Read Enable*		100	ns
T5	Data Hold Time from End of $\overline{RD}$	0		ns

*Read Enable is the occurrence of $\overline{RD}$ and $\overline{CE2}$.



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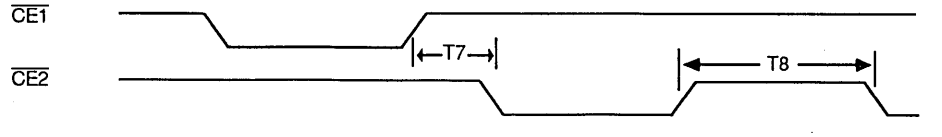
Parameter Symbol	Parameter Description	Min.	Max.	Unit
T7	$\overline{CE1}$ to $\overline{CE2}$ Recovery	100		ns
T8	$\overline{CE2}$ to $\overline{CE2}$ Recovery	100		ns



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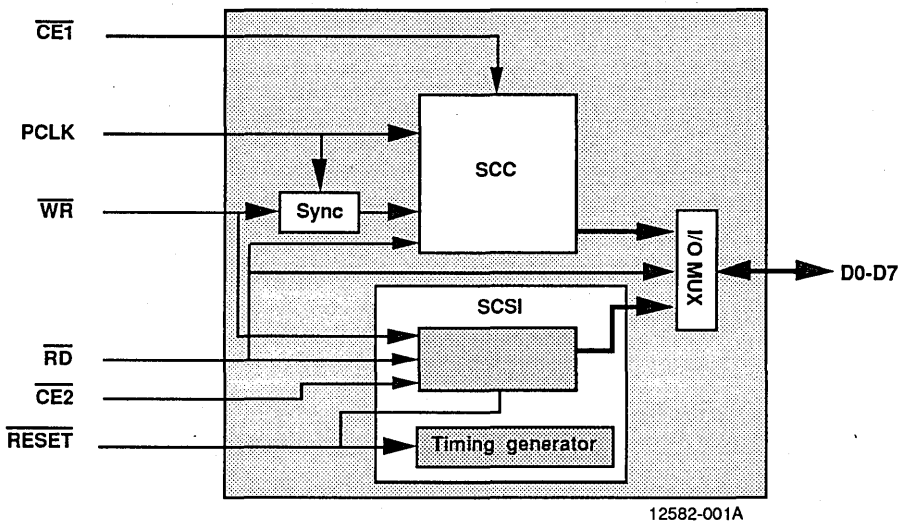
SLEEP MODE

The Am85C80 has a "sleep mode" feature which is extremely desirable in designing low power systems such as laptop, notebook and tablet PCs. Basically, the "sleep mode" feature saves power consumption by shutting down all the active circuitries when they are not in use, while keeping the necessary register values. While in "sleep mode," any incoming clock has to be stopped, all internal Voltage Controlled Oscillators and Ring Oscillators should be disabled, and to avoid driving any resistive load, the outputs have to be in tri-state. System designers should take necessary precautions to ensure no glitches occur when the system clock is being stopped or started. This is a key design issue for systems with clock stop/start capability.

The Am85C80's sleep mode has been designed so that the two different portions of the device (SCSI and SCC) may be powered down separately or together, depending on user needs. For example, a SCSI disk can be shut down while serial communication is active, or the serial ports can be shut down while data is transferring to/from the disk. To utilize the least current (typical 80 μA), both the SCSI and SCC can be powered down, and this state is called "Deep Sleep." If a user exercises a shut down and wake up session into and out of "Deep Sleep," the Am85C80 will save all its SCC register values. On the other hand, its SCSI register values will be destroyed, and the user has to program the SCSI portion once the device is out of the "sleep mode."

From the design point of view, the clock and host interface of the Am85C80 are crucial. The SCSI timing generator has an internal oscillator that is used for Arbitration and Selection timing defined in the ANSI X3.131-1986 standard. Because $\overline{WR}$ is synchronized with PCLK, the SCC writing registers are blocked when PCLK is stopped. However, any read and write to SCSI is unaffected by PCLK since it is still asynchronous. This feature enables SCSI and SCC portions of Am85C80 to be in "sleep mode" separately or together. Typically, only the SCSI or SCC portion of a Am85C80 will be active. The diagram below is a simplified block diagram of the Am85C80 drawn to address the power down mode.



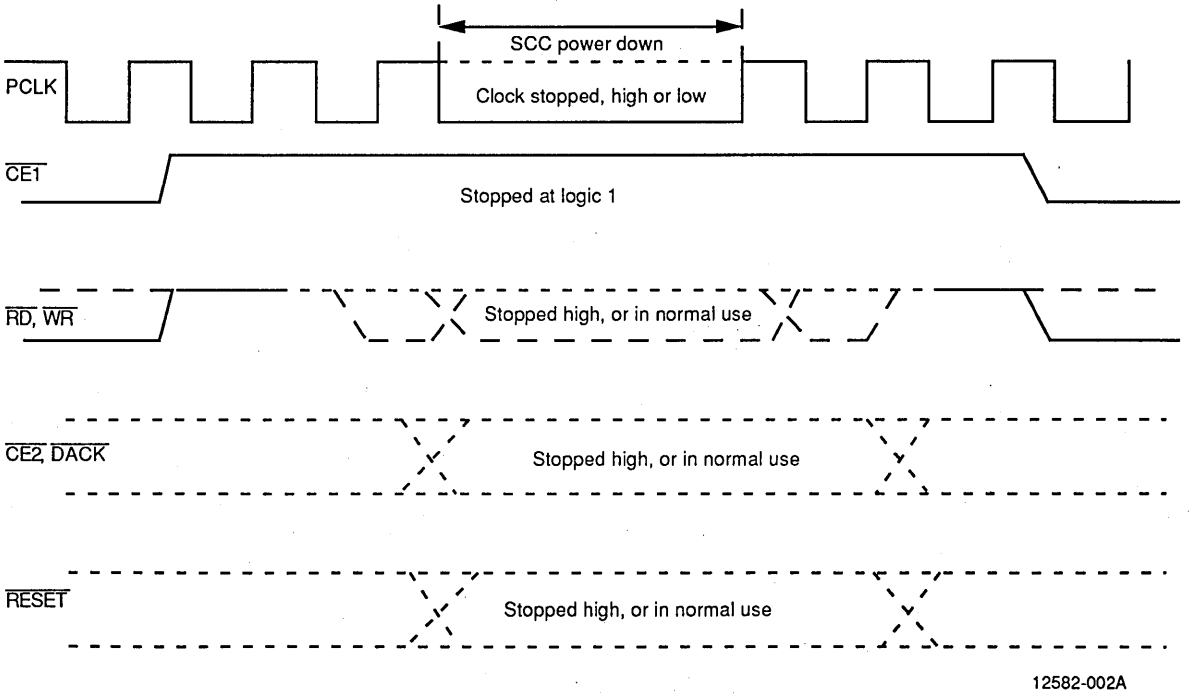
Simplified Block Diagram of the Am85C80

Guidelines for Designing Battery Powered Computers Using the Am85C80:

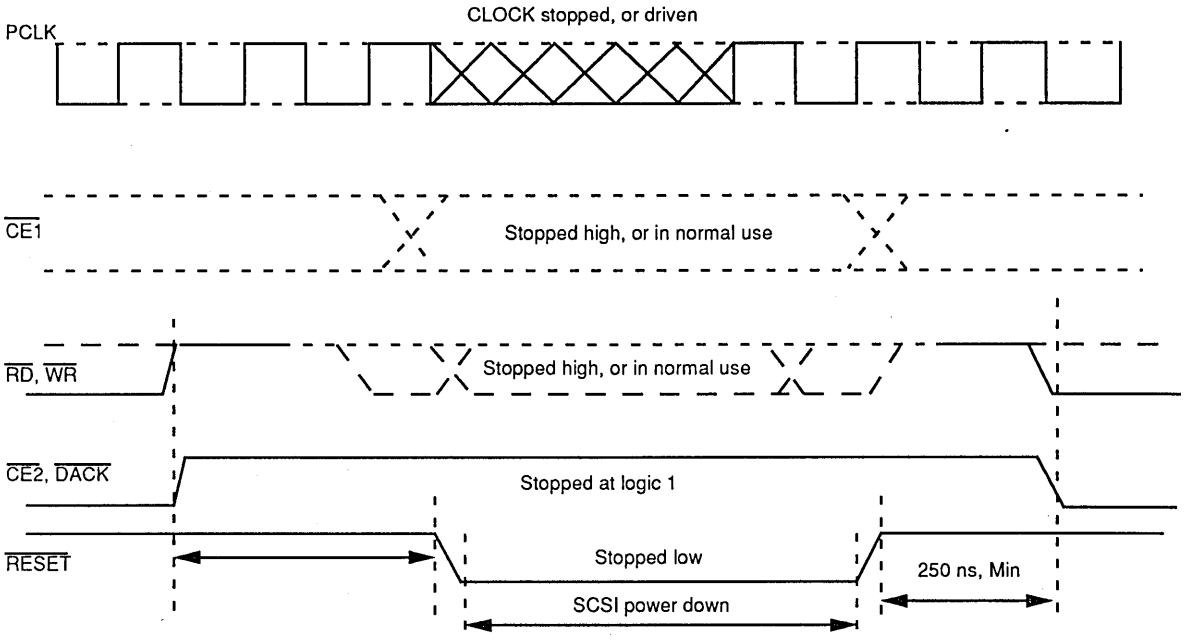
1. To save power, power-on reset (POR) circuitry is not implemented in the Am85C80. A user needs to do a soft reset, or assert both $\overline{RD}$ and $\overline{WR}$ simultaneously to cause a hard reset to the SCC portion.
2. In order to ensure the outputs (data lines) are inactive, either:

   a) $\overline{RD}$ should be kept at logic 1, or
   b) $\overline{CE1}$ and $\overline{CE2}$ should be kept at logic 1.
3. In order to put the SCC portion into "sleep mode," PCLK should be stopped at a logic 1 or 0 level. Users should ensure PCLK is stopped and started cleanly, with no double clocking or glitches. PCLK should be stopped a minimum of two cycles of PCLK before and after the access to the SCC.
4. In order to put the SCSI portion into "sleep mode," $\overline{RESET}$ should be asserted logic 0 to stop internal timing generator as shown on the diagram. $\overline{RESET}$ signal, which affects only the SCSI portion, can be asserted any time even in the middle of a CPU read or write. (Attention should be given to the software to first terminate any SCSI bus activity by going into bus free phase to avoid troubles on the SCSI bus when $\overline{RESET}$ is asserted.)
5. In order to put the Am85C80 into "Deep Sleep" mode, the user should put both the SCC and SCSI portion into their respective "sleep modes." This is done by both stopping PCLK and asserting $\overline{RESET}$.

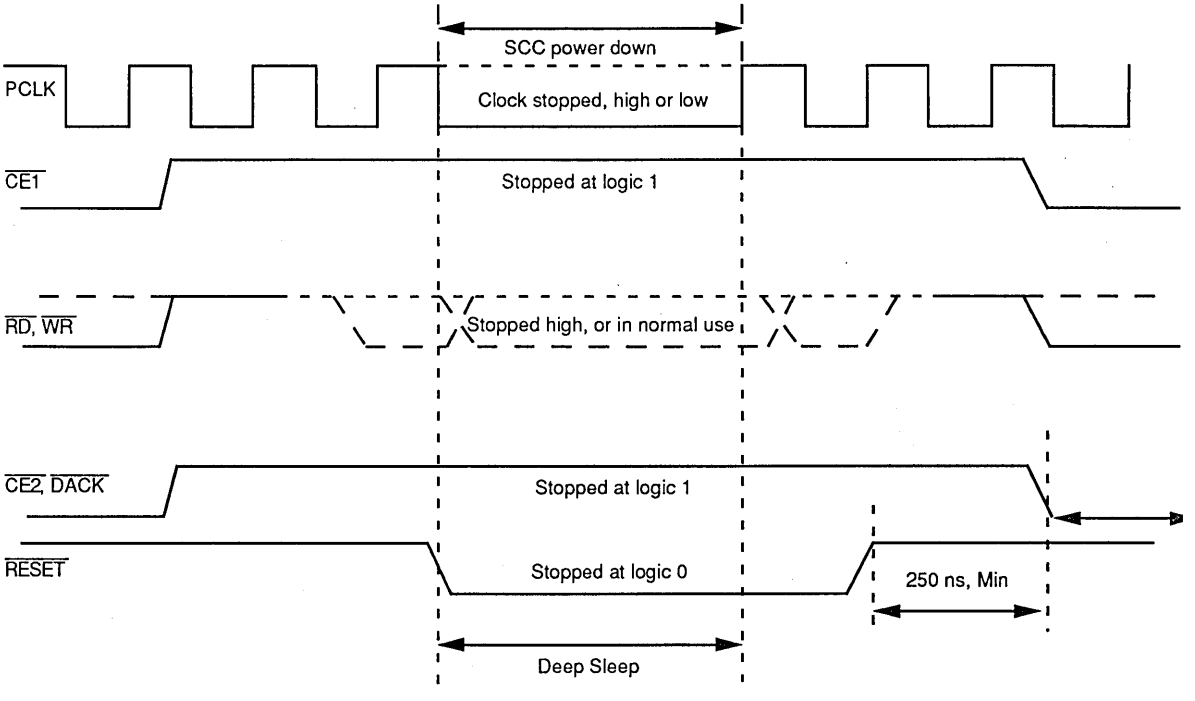
The above guide lines are for designing the laptop computers using Am85C80. The following is a typical timing diagram the one could use. It is recommended that while the chip is in "Deep Sleep" mode, $\overline{CE1}$, $\overline{CE2}$, $\overline{RD}$, and $\overline{WR}$ are at logic 1.



SCC Power Down Mode (SCC PCLK Stopped)



SCSI Power Down (RESET Held Low)



Power Down Mode: "Deep Sleep"

CHAPTER 4
Interface Products

Am26LS29

Quad Three-State Single Ended RS-423 Line Driver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off. Outputs are in high-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing

GENERAL DESCRIPTION

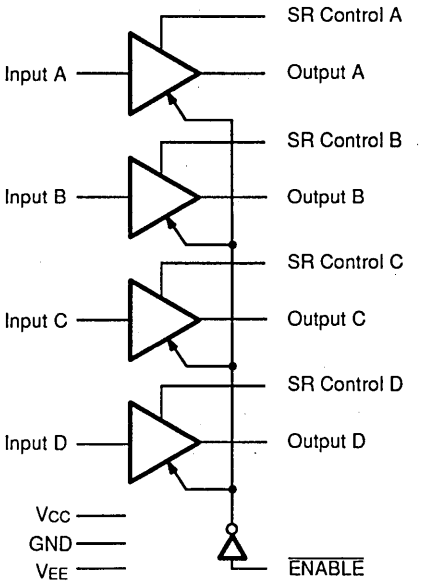
The Am26LS29 is a quad single ended line driver, designed for digital data transmission. The Am26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS29 has three-state outputs for bus oriented systems. The outputs in the high-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the Am26LS29 line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

The Am26LS29 is constructed using advanced low-power Schottky processing.

BLOCK DIAGRAM



04599-001A

Publication# 04599 Rev. B Amendment/0
Issue Date: May 1991

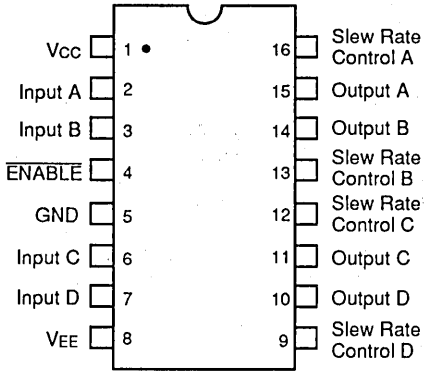
RELATED PRODUCTS

Part Number	Description
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS32	Quad Differential Line Receiver
26LS33	Quad Differential Line Receiver

CONNECTION DIAGRAMS

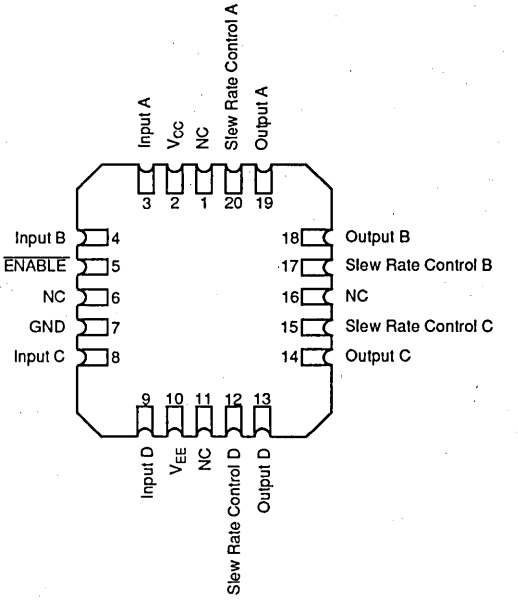
Top View

DIP



04599-003A

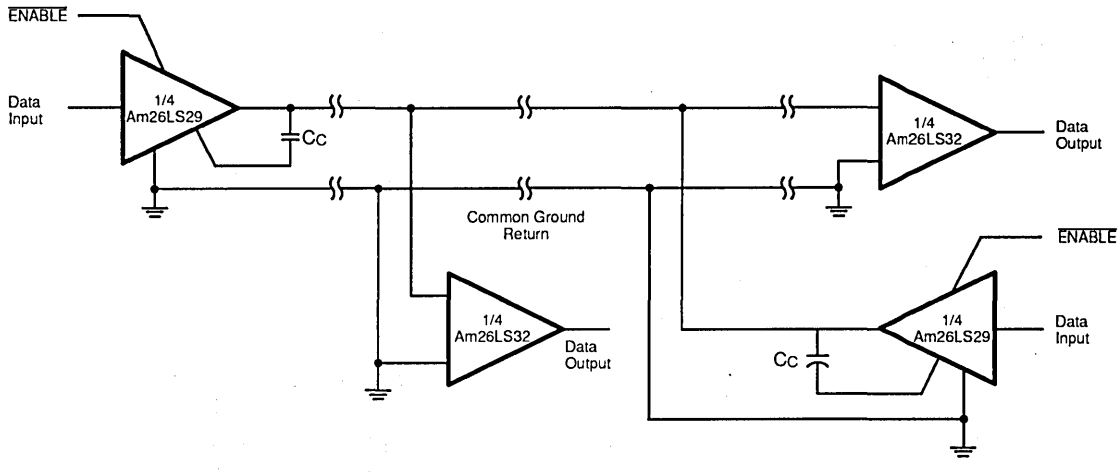
LCC



04599-002A

Note:
Pin 1 is marked for orientation

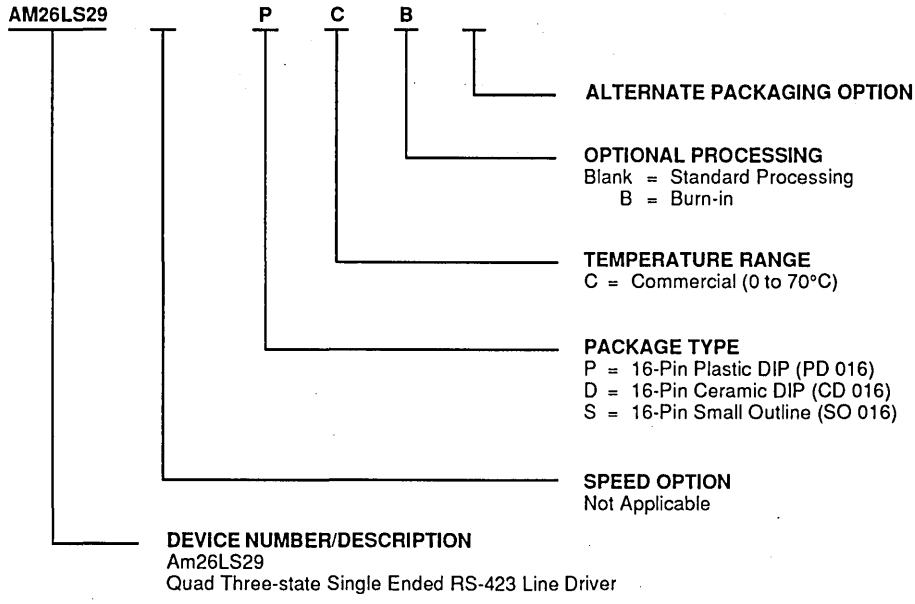
TYPICAL APPLICATION



04599-005A

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



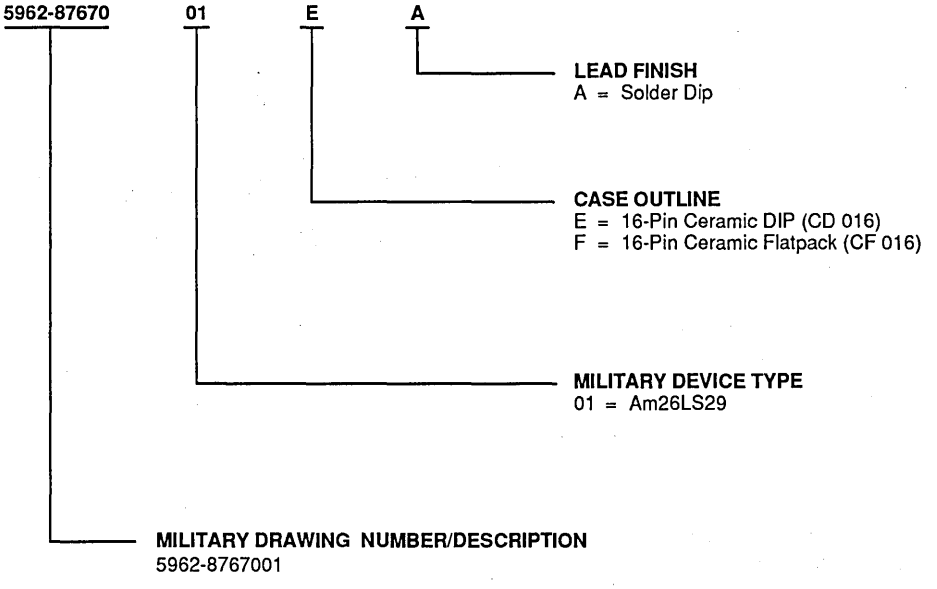
AM26LS29	PC, PCB, DC, DCB, SC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION
Standard Military Drawing Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The ordering number for SMD/DESC (Valid Combination) is formed by a combination of:



5962-8767001	EA, FA

Valid Combinations

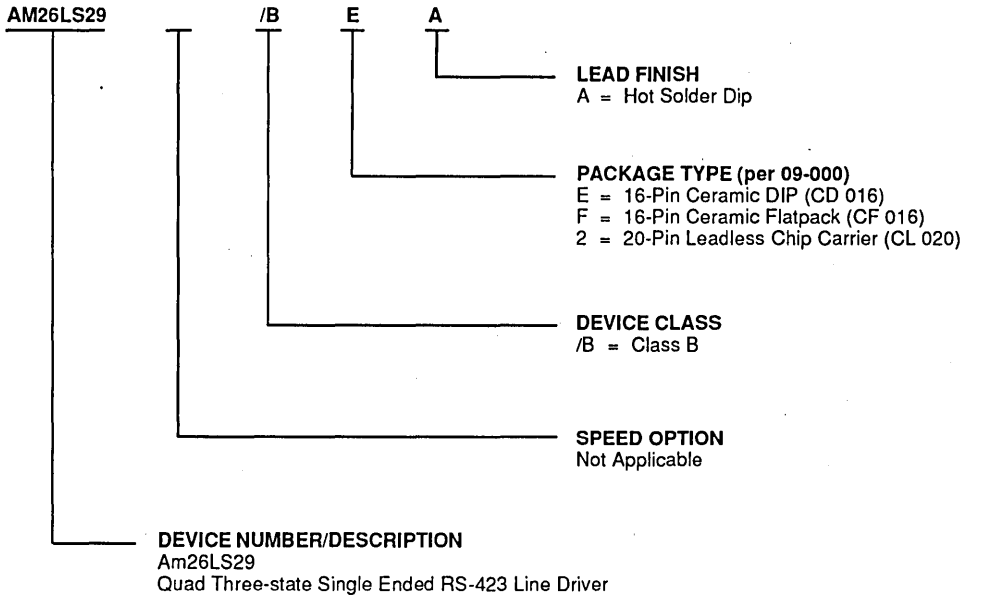
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The ordering number (Valid Combination) is formed by a combination of:



AM26LS29	/BEA /BFA /B2A

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	−65°C to +165°C
Supply Voltage:	
V+	7.0 V
V−	−7.0 V
Power Dissipation	165 mW
Input Voltage	−1.5 to +15 V
Enable Voltage	±15 V
Output Sink Current	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	+4.75 V to +5.25 V
(V_{EE})	−4.75 V to −5.25 V

Military (M) Devices

Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V
(V_{EE})	−4.75 V to −5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Unit
V_O	Output Voltage	$\|V_{CC}\| = \|V_{EE}\|$ = Min.	V_{IN} = 2.4 V	4.0	4.4	6.0	V
$\overline{V_O}$		$R_L = \infty$ (Note 3)	V_{IN} = 0.4 V	−4.0	−4.4	−6.0	V
V_T	Output Voltage (Note 4)	$\|V_{CC}\| = \|V_{EE}\|$ = Min.	V_{IN} = 2.4 V	3.6	4.1		V
$\overline{V_T}$		R_L = 450 Ω	V_{IN} = 0.4 V	−3.6	−4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance (Note 4)	$\|V_{CC}\| = \|V_{EE}\|$, R_L = 450 Ω			0.02	0.4	V
I_{X+}	Output Leakage Power Off	$V_{CC} = V_{EE}$ = 0V	V_O = 10 V			100	µA
I_{X-}			V_O = −10 V			−100	µA
I_{S+}	Output Short Circuit Current (Note 6)	$\|V_{CC}\| = \|V_{EE}\|$ = Max.	V_{IN} = 2.4 V	−20	−80	−150	mA
I_{S-}		V_O = 0 V	V_{IN} = 0.4 V	20	80	150	mA
I_{CC}	Positive Supply Current	V_{IN} = 0.4 V, $R_L = \|\infty$, $\|V_{CC}\| = \|V_{EE}\|$ = Max.			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4 V, $R_L = \|\infty$, $\|V_{CC}\| = \|V_{EE}\|$ = Max.			−10	−22	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 10 V			100	µA
		$\|V_{CC}\| = \|V_{EE}\|$ = Max.	V_O = −10 V			−100	µA
V_{IH}	High Level Input Voltage	(Note 7)		2.0			V
V_{IL}	Low Level Input Voltage	(Note 7)				0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4 V, $\|V_{CC}\| = \|V_{EE}\|$ = Max.				40	µA
		$V_{IN} \le 15$ V, V_{CC} = 5.5 V, V_{EE} = −5.0 (Note 5)				100	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V, $\|V_{CC}\| = \|V_{EE}\|$ = Max.			−30	−200	µA
V_I	Input Clamp Voltage	I_{IN} = −12mA, V_{CC} = Min., V_{EE} = Max.				−1.5	V

Notes:

1. Typical limits are at V_{CC} = 5.0 V, V_{EE} = −5.0 V, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9 V minimum and −3.9 V minimum at −55°C.
4. This parameter is tested by forcing an equivalent current.
5. V_{EE} = −5.0 V due to tester limitation.
6. Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
7. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.

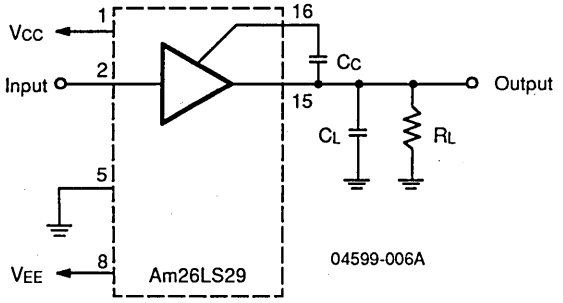
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
t_r	Rise Time	R_L = 450 Ω, C_L = 500 pF, Fig. 1	C_C = 50 pF		3.0		µs
			C_C = 0 pF		120	300	ns
t_f	Fall Time	R_L = 450 Ω, C_L = 500 pF, Fig. 1	C_C = 50 pF		3.0		µs
			C_C = 0 pF		120	300	ns
t_{pdh}	Output Propagation Delay	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF			180	300	ns
t_{pdl}	Output Propagation Delay	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF			180	300	ns
t_{LZ}	Output Enable to Output	R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF, Fig. 2			180	300	ns
t_{HZ}					200	350	
t_{ZL}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF, Fig. 2			200	350	
t_{ZH}					180	300	

AC CHARACTERISTICS (T_A = –55°C to +125°C, V_{CC} = 4.75 V to 5.5 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Rise Time	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF			450	µs
t_f	Fall Time	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF			450	µs
t_{pdh}	Output Propagation Delay	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF			450	ns
t_{pdl}	Output Propagation Delay	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF			450	ns
t_{LZ}	Output Enable to Output	R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF			400	ns
t_{HZ}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF			400	ns
t_{ZL}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF			400	ns
t_{ZH}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF			400	ns

SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORM

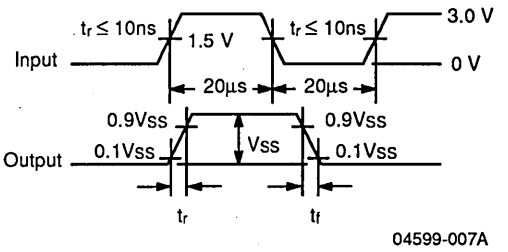
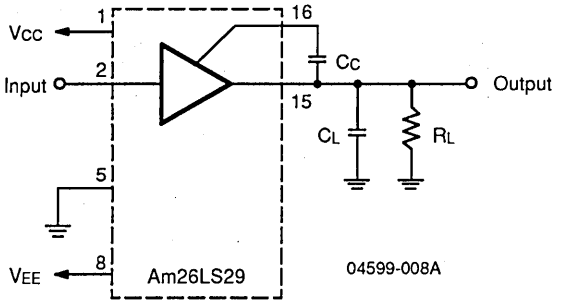


Figure 1. Rise Time Control

SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORM

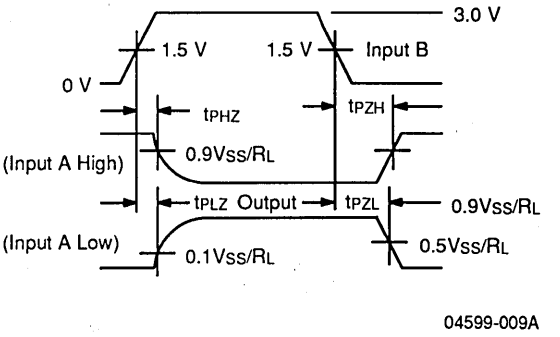
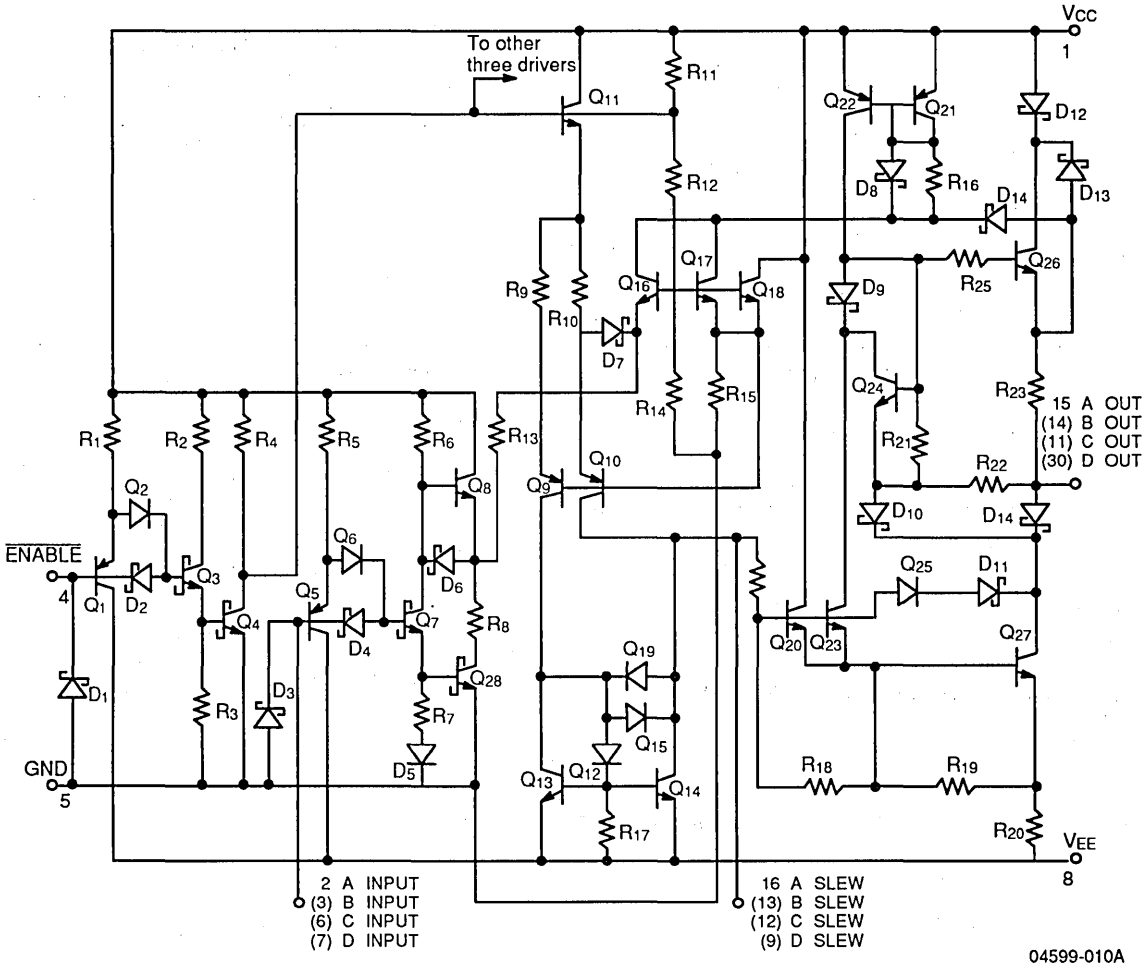


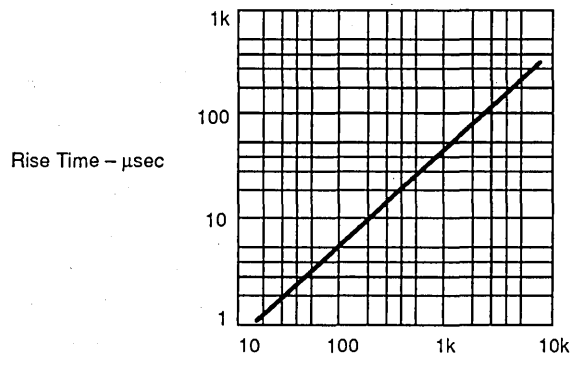
Figure 2. Three-State Delays

Am26LS29 EQUIVALENT CIRCUIT



TYPICAL PERFORMANCE CURVES

**Slew Rate (Rise or Fall Time)
Versus External Capacitor**



04599-011A

Am26LS30

Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in hi-impedance state
- Independent output control in the differential mode
- Low I_{CC} and I_{EE} power consumption
  RS-422 differential mode; 35 mW/driver typ.
  RS-423 single-ended mode; 26 mW/driver typ.
- Individual slew rate control for each output
- 50 Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- Advanced low power Schottky processing

GENERAL DESCRIPTION

The Am26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all of the requirements of EIA Standard RS-422 or four independent single-ended RS-423 line drivers.

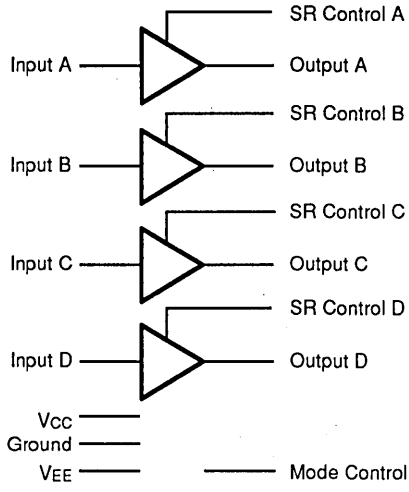
In the differential mode the outputs have individual three-state controls. In the hi-impedance state these outputs will not clamp the line over a common mode transmission line voltage of ±10 V. A typical full duplex system would be the Am26LS30 differential line driver and up to twelve Am26LS32 line receivers or a Am26LS32 line receiver and up to thirty-two Am26LS30 differential drivers.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS30 is constructed using Advanced Low Power Schottky processing.

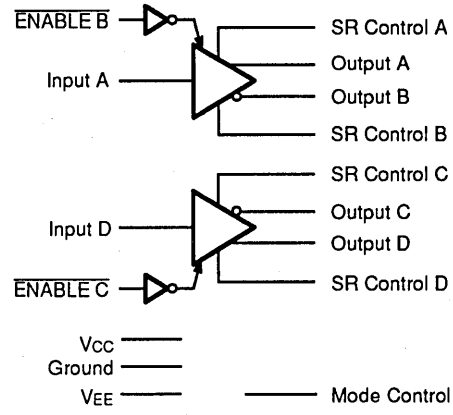
BLOCK DIAGRAM

Logic for Am26LS30 with Mode Control HIGH (RS-423)



04600-001A

Logic for Am26LS30 with Mode Control LOW (RS-422)



04600-002A

Publication# 04600 Rev. B Amendment/0
Issue Date: May 1991

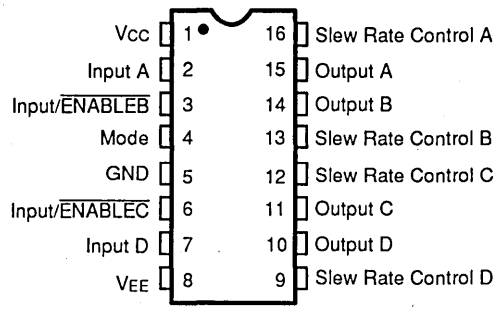
RELATED AMD PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS32	Quad Differential Line Receiver
26LS33	Quad Differential Line Receiver

CONNECTION DIAGRAMS

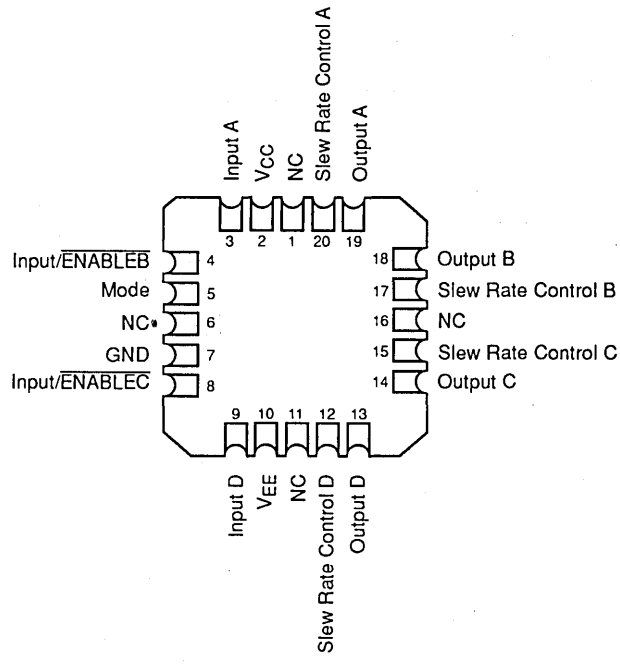
Top View

DIP



04600-003A

LCC

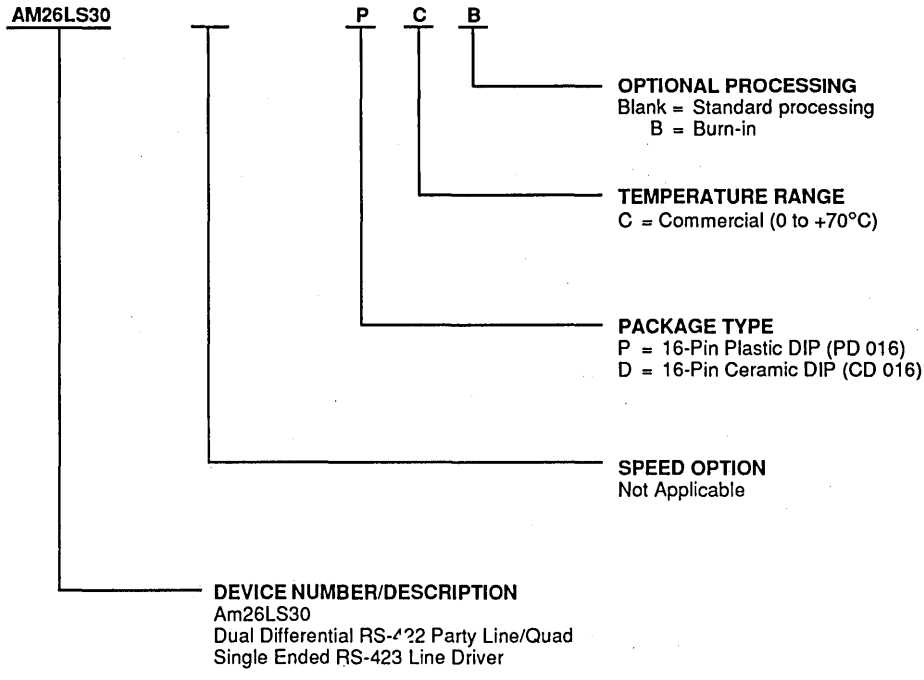


04600-004A

Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS30	PC, PCB DC, DCB

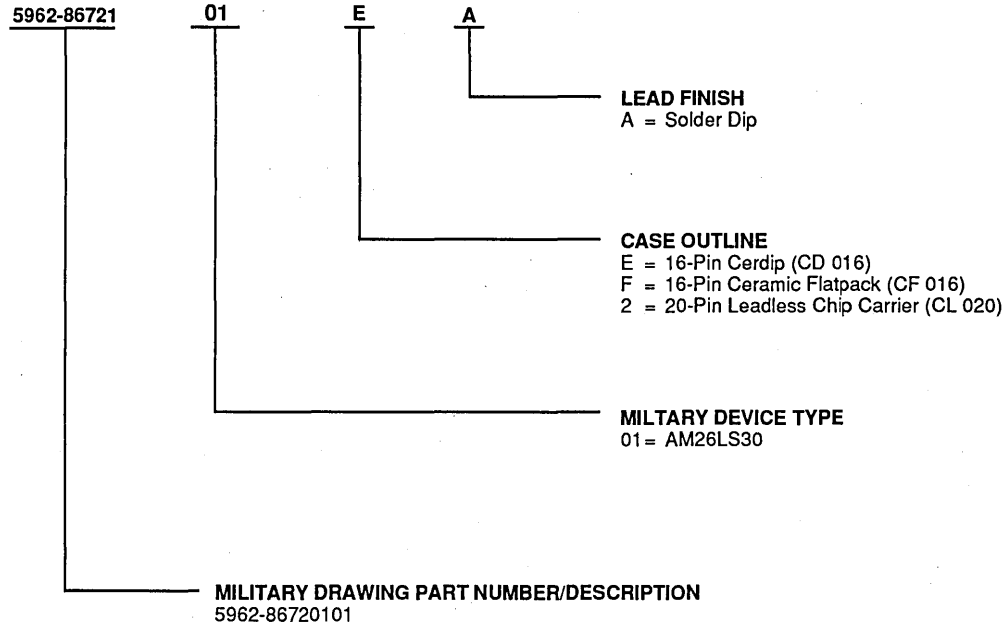
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:



Valid Combinations	
5962-8672101	EA, FA, 2A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

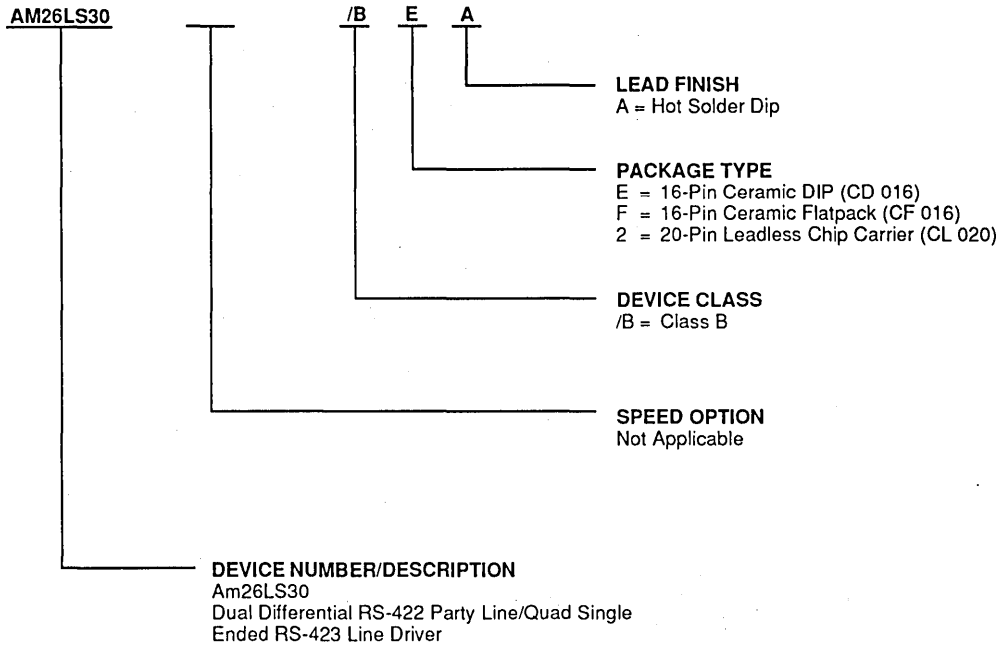
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS30	/BEA, /BFA, /B2A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

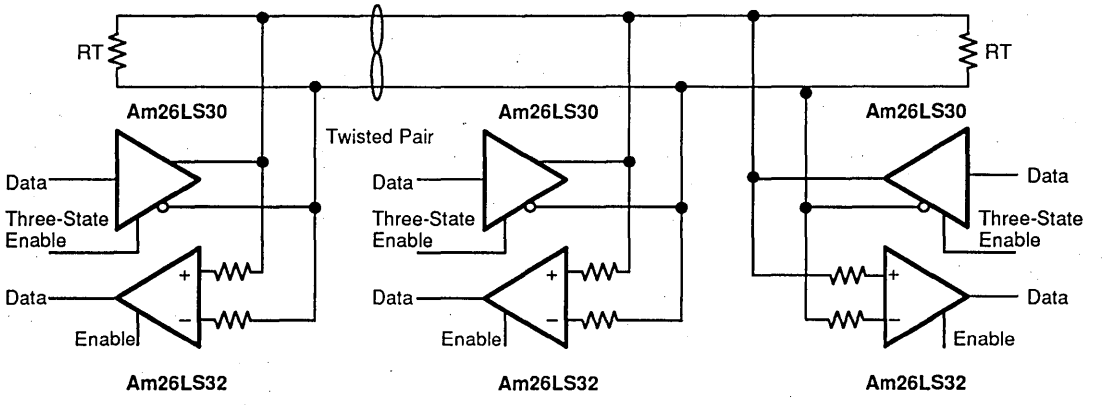
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Am26LS30 FUNCTION TABLE

Mode	Inputs		Outputs	
	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

TYPICAL APPLICATION



04600-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	–65 to +150°C
Supply Voltage	
V+	7.0 V
V–	–7.0 V
Power Dissipation	600 mW
Input Voltage	–1.5 to +15.0 V
Output Voltage (Power Off)	±15 V
Lead Soldering Temperature (10 seconds)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0 to +70°C
Supply Voltage (V_{CC})	+4.75 V to +5.25 V
Supply Voltage (V_{EE}) RS422	GND
Supply Voltage (V_{EE}) RS423	–4.75 V to –5.25 V

Military (M) Devices

Temperature	–55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V
Supply Voltage (V_{EE}) RS422	GND
Supply Voltage (V_{EE}) RS423	–4.75 V to –5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified
EIA RS-422 Connection, Mode Voltage ≤ 0.8 V, V_{CC} = +4.75 V to +5.5 V, V_{EE} = GND

Parameter Symbol	Parameter Description	Test Conditions (Note 3)		Min.	Typ. (Note 1)	Max.	Unit
V_O	Differential Output Voltage,	$R_L = \infty$	V_{IN} = 2.0 V		3.6	6.0	V
$\overline{V_O}$	$V_{A, B}$		V_{IN} = 0.8 V		–3.6	–6.0	
V_T	Differential Output Voltage,	R_L = 100 Ω	V_{IN} = 2.0 V	2.0	2.4		V
$\overline{V_T}$	$V_{A, B}$		V_{IN} = 0.8 V	–2.0	–2.4		
V_{OS}, $\overline{V_{OS}}$	Common Mode Offset Voltage	R_L = 100 Ω			2.5	3.0	V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output Voltage	R_L = 100 Ω			0.005	0.4	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Difference in Common Mode Offset Voltage	R_L = 100 Ω			0.005	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T}\rvert$	R_L = 100 Ω		4.0	4.8		V
V_{CMR}	Output Voltage Common Mode Range	$V_{\overline{ENABLE}}$ = 2.4 V		±10			V
I_{XA}	Output Leakage Current	V_{CC} = 0 V	V_{CMR} = 10 V			100	µA
I_{XB}			V_{CMR} = –10 V			–100	
I_{OX}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_{CMR} = 10 V			100	µA
			V_{CMR} = –10 V			–100	
I_{SA}, I_{SB}	Output Short Circuit Current	V_{CC} = Max.	V_{OA} = 6.0 V	20	80	150	mA
		V_{IN} = 2.4 V	V_{OB} = 0 V	–20	–80	–150	
		V_{CC} = Max.	V_{OA} = 0 V	–20	–80	–150	mA
		V_{IN} = 0.4 V	V_{OB} = 6.0 V	20	80	150	
I_{CC}	Supply Current	V_{IN} = .4 V, V_{CC} = Max.			18	30	mA
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max.	V_{IN} = 2.4 V			40	µA
			V_{IN} = 15 V			100	
I_{IL}	Low Level Input Current	V_{CC} = Max.	V_{IN} = 0.4 V		–30	–200	µA
V_{IC}	Input Clamp Voltage	V_{CC} = Min.	I_{IN} = –12 mA			–1.5	V

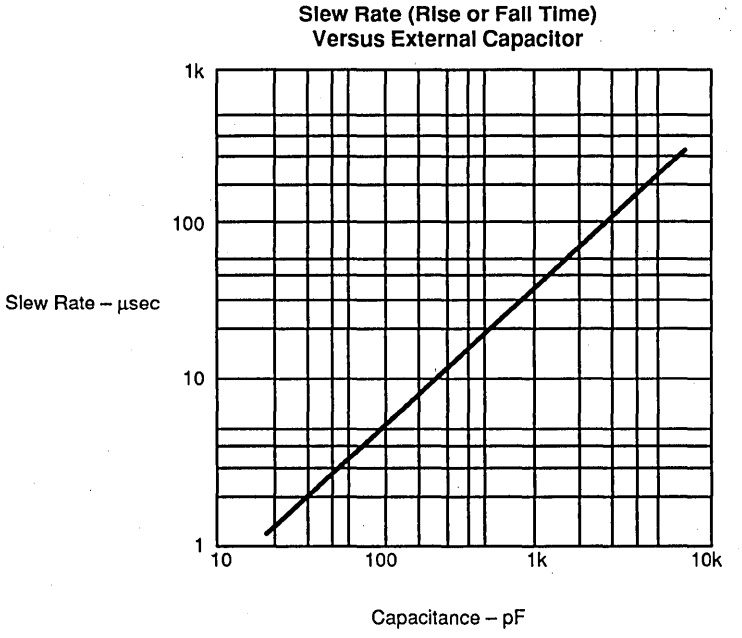
DC CHARACTERISTICS over operating ranges unless otherwise specified
EIA RS-423 Connection, Mode Voltage ≥ 2.0 V

Parameter Symbol	Parameter Description	Test Conditions (Note 4)		Min.	Typ. (Note 1)	Max.	Unit
V_O	Output Voltage	$R_L = \infty$ (Note 3)	V_{IN} = 2.4 V	4.0	4.4	6.0	V
$\overline{V_O}$		$\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=4.75 V	V_{IN} = 0.4 V	−4.0	−4.4	−6.0	
V_T	Output Voltage (Note 7)	R_L = 450 Ω	V_{IN} = 2.4 V	3.6	4.1		V
$\overline{V_T}$		$\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=4.75 V	V_{IN} = 0.4 V	−3.6	−4.1		
$\lvert V_T\rvert-\lvert\overline{V_T}\rvert$	Output Unbalance (Note 7)	$\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=4.75 V, R_L = 450 Ω			0.02	0.4	V
I_{X+}	Output Leakage Power Off	$V_{CC} = V_{EE}$ = 0 V	V_O = 6.0 V			100	µA
I_{X-}			V_O = −6.0 V			−100	
I_{S+}	Output Short Circuit Current	V_O = 0 V	V_{IN} = 2.4 V	−20	−80	−150	mA
I_{S-}		$\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=Max. (Note 5)	V_{IN} = 0.4 V	20	80	150	
I_{SLEW}	Slew Control Current	$V_{SLEW} = V_{EE}$	V_{IN} = 2.7 V		−230		µA
I_{CC}	Positive Supply Current	V_{IN} = 0.4 V, $R_L = \infty$, $\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=Max.			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4 V, $R_L = \infty$, $\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=Max.			−10	−22	mA
V_{IH}	High Level Input Voltage	Note 6		2.0			V
V_{IL}	Low Level Input Voltage	Note 6				0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4 V, $\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=Max.				40	µA
		V_{IN} = 15 V, V_{CC} = 5.5 V, V_{EE} = −5.0 V				100	
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V, $\lvert V_{CC}\rvert=\lvert V_{EE}\rvert$=Max.			−30	−200	µA
V_{IC}	Input Clamp Voltage	I_{IN} = −12 mA, V_{CC} = Min., V_{EE} = Max.				−1.5	V

Notes:

1. Typical limits are at V_{CC} = 5.0 V, V_{EE} = −5.0 V, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9 V minimum and −3.9 V minimum at −55°C.
4. R_L connected between each output and its complement.
5. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
6. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
7. This parameter is tested by forcing an equivalent current.

PERFORMANCE CURVE



SWITCHING CHARACTERISTICS

EIA RS-422 Connection, V_{CC} = 5.0 V, V_{EE} = GND, Mode = 0.4 V, T_A = 25°C

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Differential Output Rise Time	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_f	Differential Output Fall Time	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_{PDH}	Output Propagation Delay	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_{PDL}	Output Propagation Delay	Fig. 2, R_L = 100 Ω, C_L = 500 pF		120	200	ns
t_{LZ}	Output Enable to Output	R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF, Fig. 3		180	300	ns
t_{HZ}				200	300	
t_{ZL}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF, Fig. 3		200	300	
t_{ZH}				180	300	

SWITCHING CHARACTERISTICS (Continued)

EIA RS-422 Connection, V_{CC} = 4.5 V to 5.5 V, V_{EE} = GND, Mode = 0.4 V, T_A = 55°C to 125°C

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Differential Output Rise Time	R_L = 100 Ω, C_L = 500 pF see Rise Time Control for RS-422			300	ns
t_f	Differential Output Fall Time	R_L = 100 Ω, C_L = 500 pF see Rise Time Control for RS-422			300	ns
t_{PDH}	Output Propagation Delay	R_L = 100 Ω, C_L = 500 pF see Rise Time Control for RS-422			300	ns
t_{PDL}	Output Propagation Delay	R_L = 100 Ω, C_L = 500 pF see Rise Time Control for RS-422			300	ns
t_{LZ}	Output Enable to Output	R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-422			400	ns
t_{HZ}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-422			400	ns
t_{ZL}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-422			400	ns
t_{ZH}		R_L = 100 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-422			400	ns

SWITCHING CHARACTERISTICS

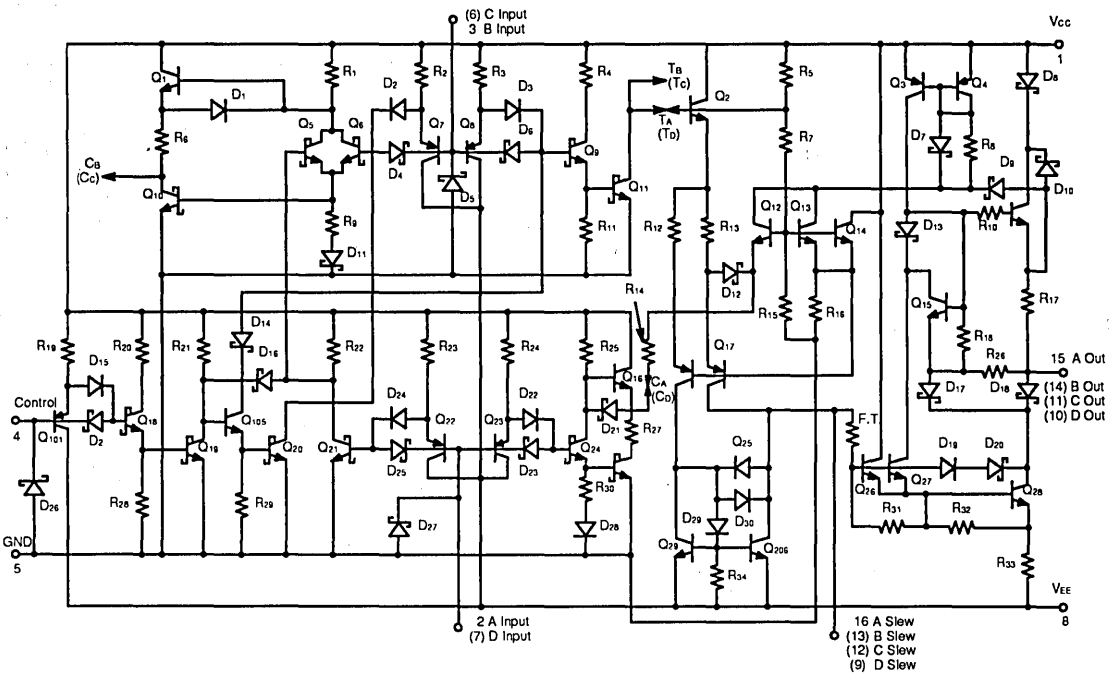
EIA RS-423 Connection, V_{CC} = 5.0 V, V_{EE} = –5.0 V, Mode = 2.4 V, T_A = 25°C

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
t_r	Rise Time	Fig. 1, R_L = 450 Ω,	C_C = 50 pF		3.0		µs
		C_L = 500 pF	C_C = 0		120	300	ns
t_f	Fall Time	Fig. 1, R_L = 450 Ω,	C_C = 50 pF		3.0		µs
		C_L = 500 pF	C_C = 0		120	300	ns
Src	Slew Rate Coefficient	Fig. 1, R_L = 450 Ω, C_L = 500 pF			.06		µs/pF
t_{PDH}	Output Propagation Delay	Fig. 1, R_L = 450 Ω, C_L = 500 pF, C_C = 0			180	300	ns
t_{PDL}	Output Propagation Delay	Fig. 1, R_L = 450 Ω, C_L = 500 pF, C_C = 0			180	300	ns

EIA RS-423 Connection, V_{CC} = 4.75 V to 5.5 V, V_{EE} = –4.75 V to –5.5 V, Mode = 2.4 V, T_A = –55°C to 125°C

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Rise Time	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-423			450	ns
t_f	Fall Time	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-423			450	ns
t_{PDH}	Output Propagation Delay	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-423			450	ns
t_{PDL}	Output Propagation Delay	R_L = 450 Ω, C_L = 500 pF, C_C = 0 pF see Rise Time Control for RS-423			450	ns

Am26LS30 EQUIVALENT CIRCUIT



04600-007A

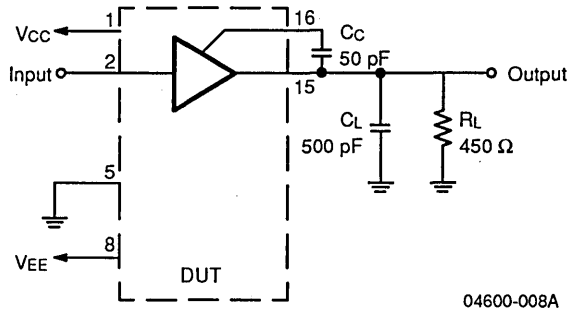
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

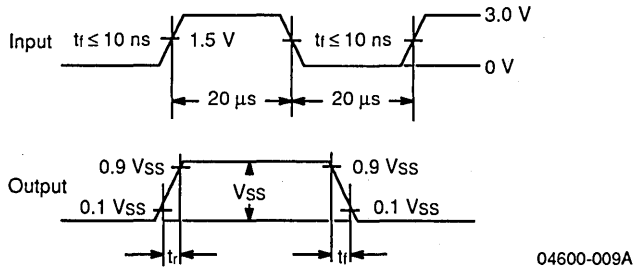
EIA RS-423 CONNECTION

Switching Test Circuit
(Mode Control = 0)



04600-008A

Switching Test Waveform

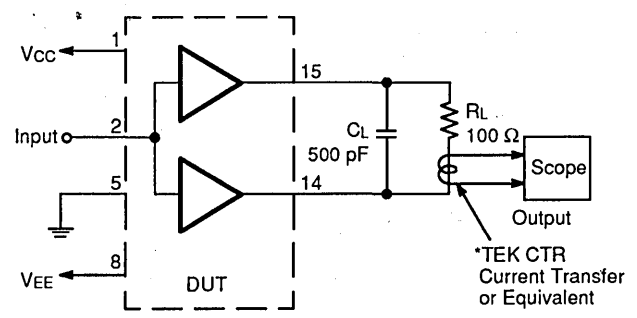


04600-009A

Figure 1. Rise Time Control for RS-423

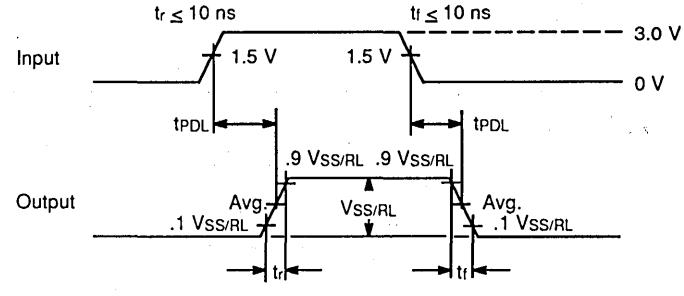
RS-422 CONNECTION

Switching Test Circuit
(Mode Control = 0)



04600-010A

Rise Time Control for RS-422

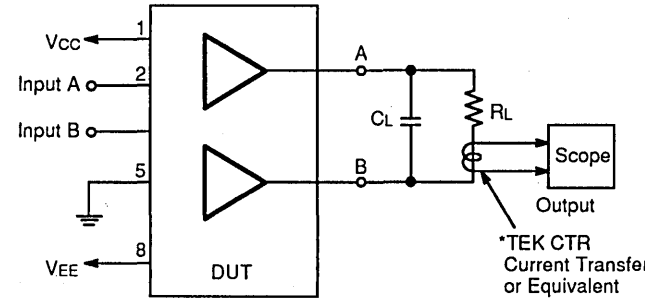


04600-011A

Figure 2.

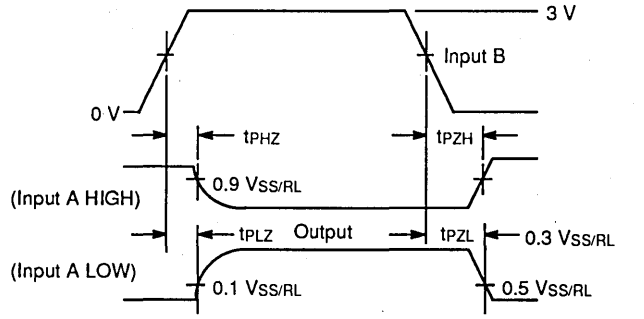
RS-422 CONNECTION (Continued)

Switching Test Circuit
(Mode Control = 0)



04600-012A

Switching Test Waveform



04600-013A

*Current probe is the easiest way to display a differential waveform

Figure 3. Three-State Delays

Am26LS31

Quad High Speed Differential Line Driver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0 ns typical
- Input to output delay – 12 ns
- Operation from single +5 V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when V_{CC} = 0
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100 Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing

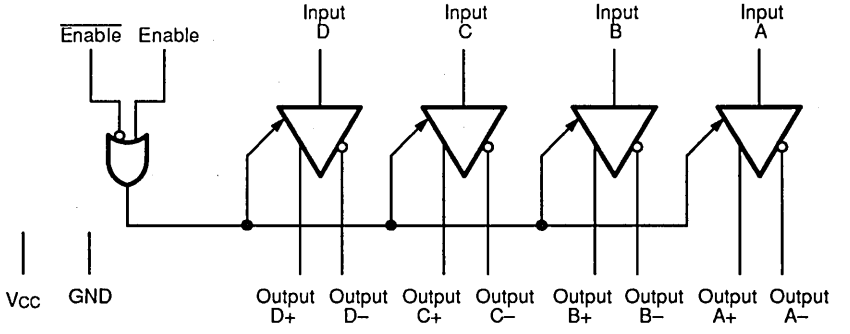
GENERAL DESCRIPTION

The Am26LS31 is a quad-differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

BLOCK DIAGRAM



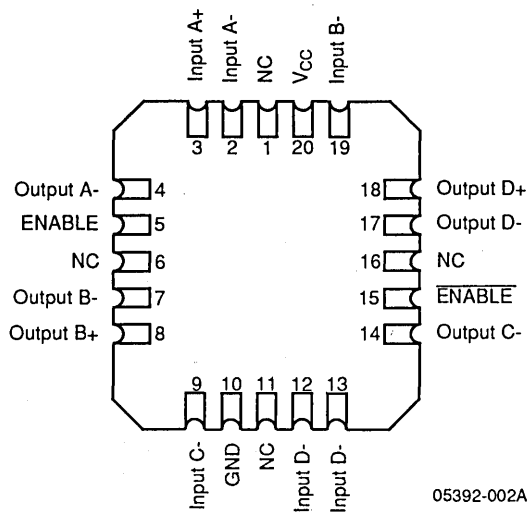
05392-001A

RELATED PRODUCTS

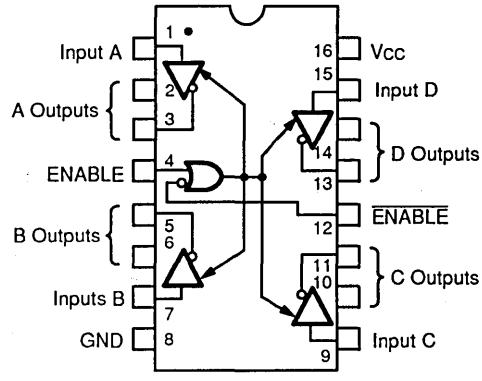
Part No.	Description
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS32	Quad Differential RS-422 Line Receiver

Publication# 05392 Rev. B Amendment/0
Issue Date: May 1991

CONNECTION DIAGRAMS
Top View



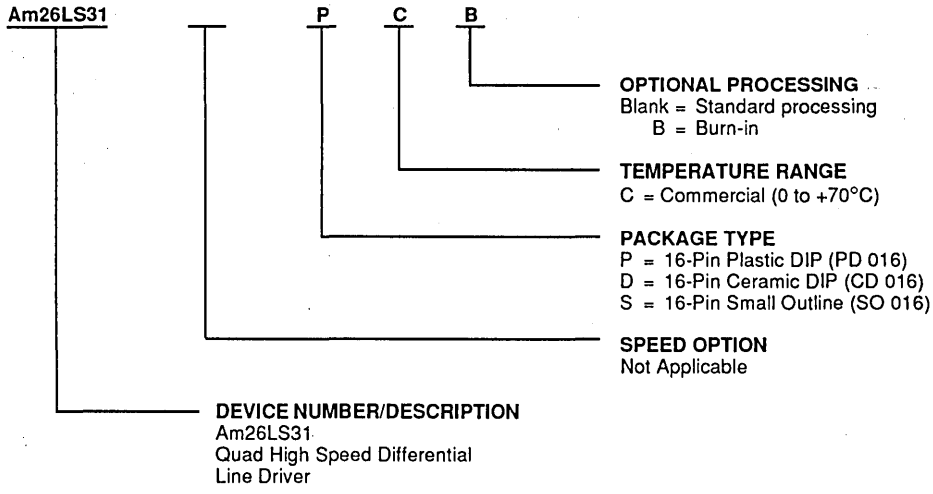
05392-002A



05392-003B

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS31	PC, PCB DC, DCB SC

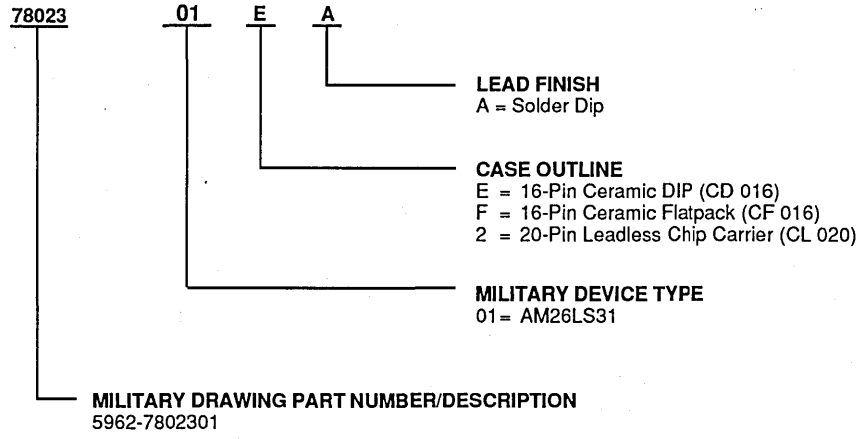
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

SMD/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
5962-7802301	MEA, MFA, M2A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

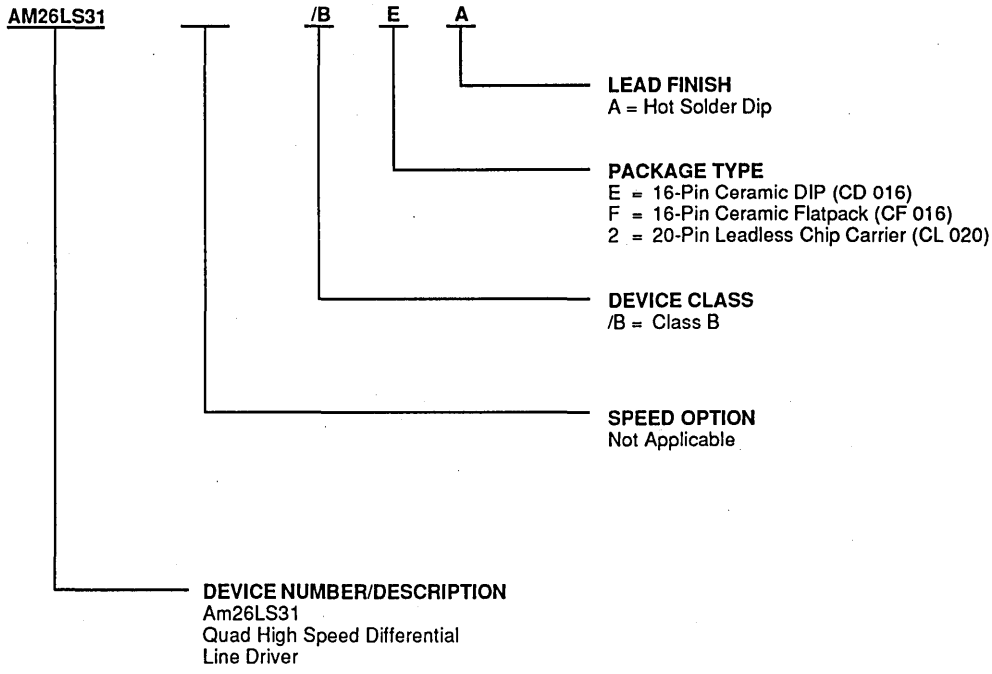
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am26LS31	/BEA, /BFA, /B2A

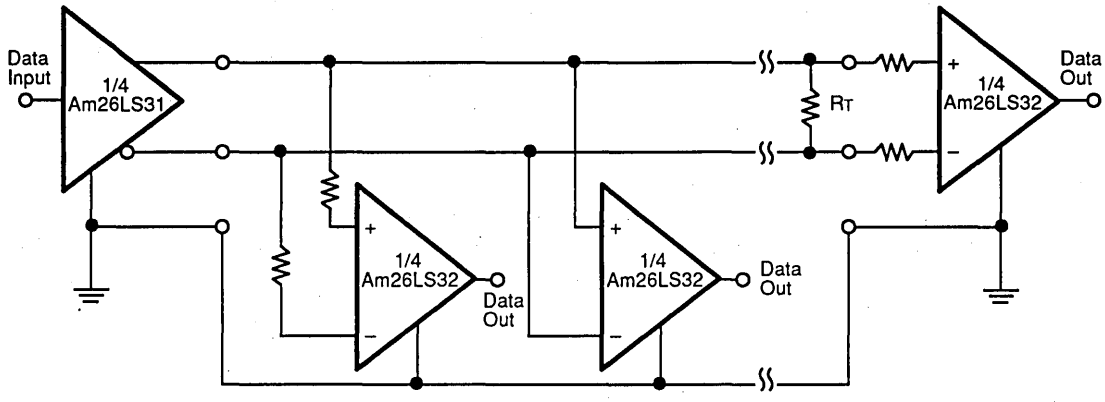
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

TYPICAL APPLICATION



05392-004A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Supply Voltage	−0.5 to 7.0 V
DC Input Voltage	−1.5 to 7.0 V
DC Output Voltage	−0.5 to V_{CC} max

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V

Military (M) Devices

Temperature	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 2)		Min.	Typ. (Note 1)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min; I_{OH} = −20 mA		2.5	3.2		V
V_{OL}	Output LOW Voltage	V_{CC} = Min; I_{OL} = 20 mA			0.32	0.5	V
V_{IH}	Input HIGH Voltage	V_{CC} = Min; (Note 3)		2.0			V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 3)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−0.20	−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			0.5	20	µA
I_I	Input Reverse Current	V_{CC} = Max., V_{IN} = 7.0 V				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = Max.	V_O = 2.5 V			20	µA
			V_O = 0.5 V			−20	
V_I	Input CLAMP Voltage	V_{CC} = Min., I_{IN} = −18 mA			−0.8	−1.5	V
I_{OFF}	Power off leakage Current	V_{CC} = 0 V	V_{OUT} = 6 V			100	µA
			V_{OUT} = −.25 V			−100	
I_{SC}	Output Short Circuit Current	V_{CC} = Max., (Note 4)		−30	−60	−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., all outputs disabled			60	80	mA
AC Parameters V_{CC} = 5.0 V, T_A = 25°C							
t_{PLH}	Input to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, C_L = 10 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, C_L = 10 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			30	40	ns

Notes:

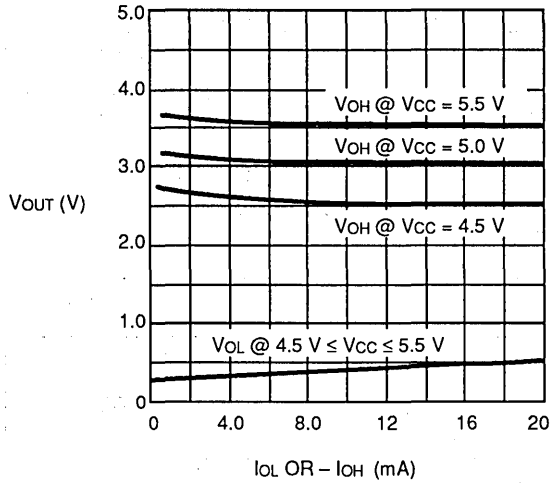
1. All typical values are V_{CC} = 5.0 V, T_A = 25°C.
2. C_L = 30 pF, V_{IN} = 1.3 V to V_{OUT} = 1.3 V, V_{PULSE} = 0 V to +3.0 V, R_{L1} = 180 Ω, R_{L2} = 75 Ω.
3. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Unit
AC Parameters (Commercial) V_{CC} = 4.75 V – 5.25 V; T_A = 0°C – 70°C						
t_{PLH}	Propagation Delay from Input to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		18	30	ns
t_{PHL}	Propagation Delay from Input to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		18	30	ns
t_{SKEW}	Output to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		3.0	9.0	ns
t_{PLZ}	Propagation Delay from Enable to Output	C_L = 10 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		35	53	ns
t_{PHZ}	Propagation Delay from Enable to Output	C_L = 10 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		25	45	ns
t_{PZL}	Propagation Delay from Enable to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		53	68	ns
t_{PZH}	Propagation Delay from Enable to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		45	60	ns
AC Parameters (Military) V_{CC} = 4.75 V – 5.25 V; T_A = –55°C – +125°C						
t_{PLH}	Propagation Delay from Input to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		18	30	ns
t_{PHL}	Propagation Delay from Input to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		18	30	ns
t_{SKEW}	Output to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		3.0	9.0	ns
t_{PLZ}	Propagation Delay from Enable to Output	C_L = 10 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		35	53	ns
t_{PHZ}	Propagation Delay from Enable to Output	C_L = 10 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		25	45	ns
t_{PZL}	Propagation Delay from Enable to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		53	68	ns
t_{PZH}	Propagation Delay from Enable to Output	C_L = 30 pF, R_{L1} = 180 Ω, R_{L2} = 75 Ω		45	60	ns

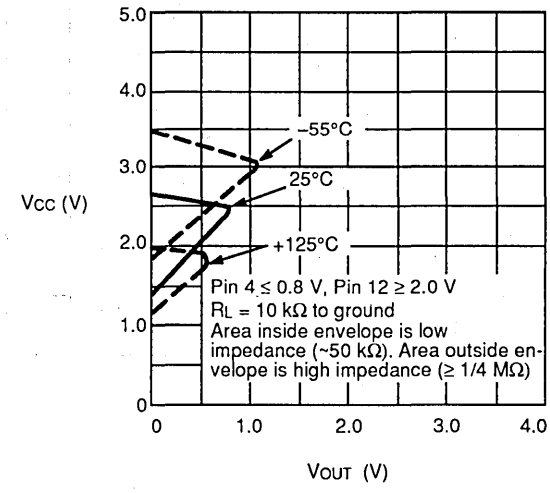
PERFORMANCE CURVES

Guaranteed V_{OH} and V_{OL}
(T_A = –55°C to +125°C)



05392-005A

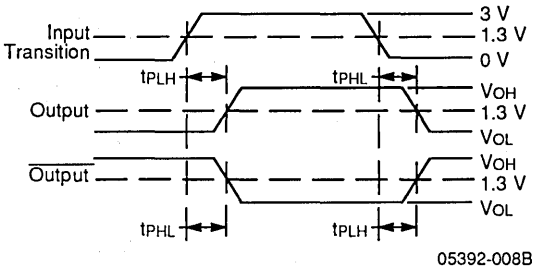
V_{OUT} Versus V_{CC}



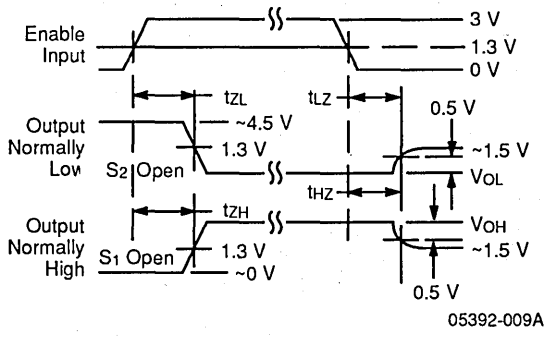
05392-006A

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State



Propagation Delay
(Notes 1 and 3)

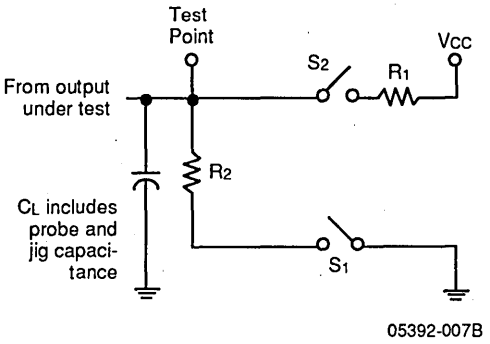


Enable and Disable Times
(Notes 2 and 3)

Notes:

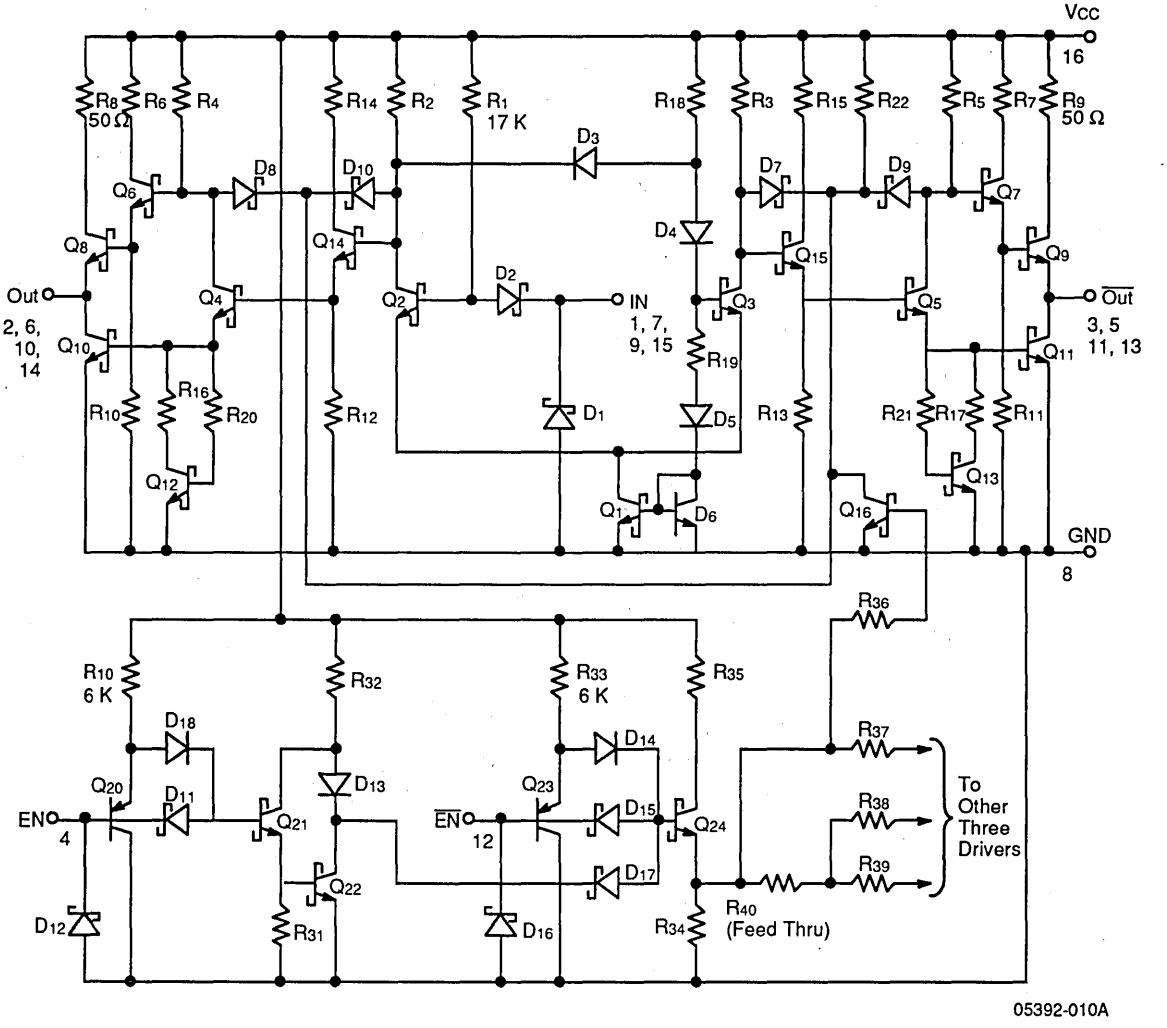
1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω; t_r ≤ 15 ns; t_f ≤ 6.0 ns.

SWITCHING TEST CIRCUIT



Three-State Outputs

EQUIVALENT CIRCUIT (1/4 Am26LS31)



05392-010A

Am26LS32/Am26LS33

Quad Differential Line Receivers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Input voltage range of 15 V (differential or common mode) on Am26LS33; 7 V (differential or common mode) on Am26LS32**
  - 200 mV sensitivity over the input voltage range on Am26LS32;
  - 500 mV sensitivity on Am26LS33
- **6k minimum input impedance with 30 mV input hysteresis**
- **The Am26LS32 meets all the requirements of RS-422 and RS-423**
- **Operation from single +5 V supply**
- **Fail safe input-output relationship. Output always high when inputs are open**
- **Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus**

GENERAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

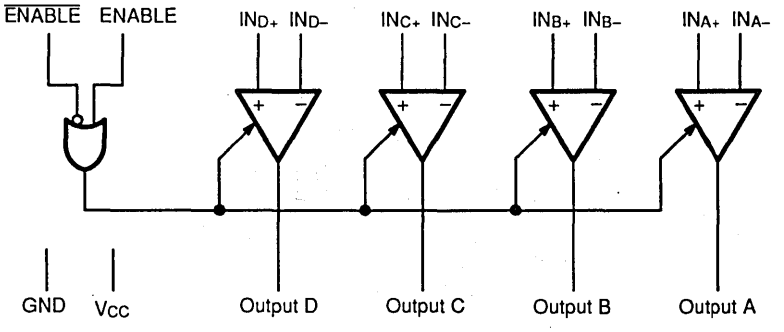
The Am26LS32 features an input sensitivity of 200 mV over the input voltage range of ±7 V.

The Am26LS33 features an input sensitivity of 500 mV over the input voltage range of ±15 V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8 mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

BLOCK DIAGRAM



05393-001B

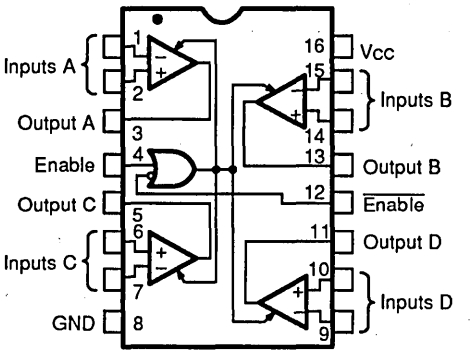
RELATED AMD PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS31	Quad High Speed Differential Line Driver

Publication# 05393 Rev. B Amendment/0
Issue Date: May 1991

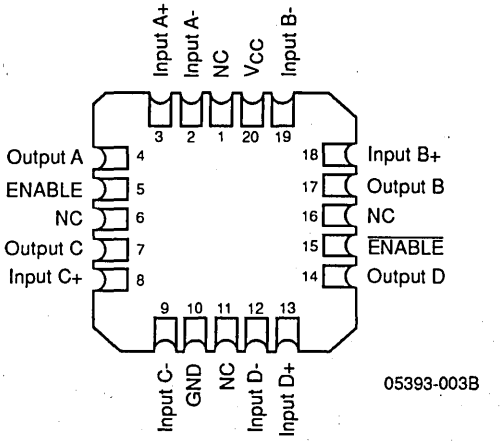
CONNECTION DIAGRAMS
Top View

DIP



05393-002B

LCC

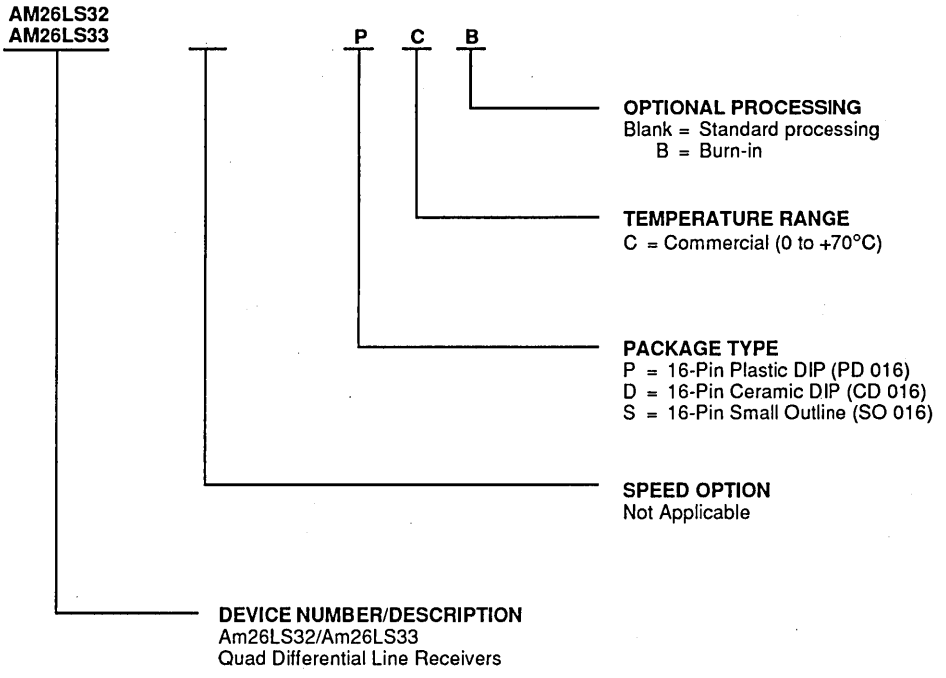


05393-003B

Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS32	PC, PCB, DC, DCB, SC
AM26LS33	

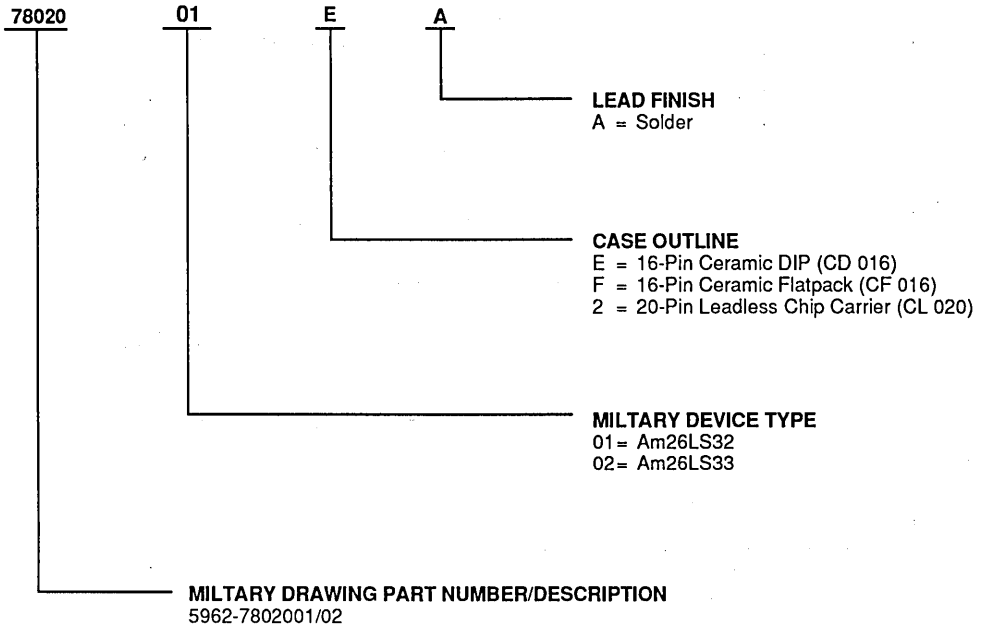
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:



Valid Combinations	
5962-7802001	MEA, MFA, M2A
5962-7802002	

Valid Combinations

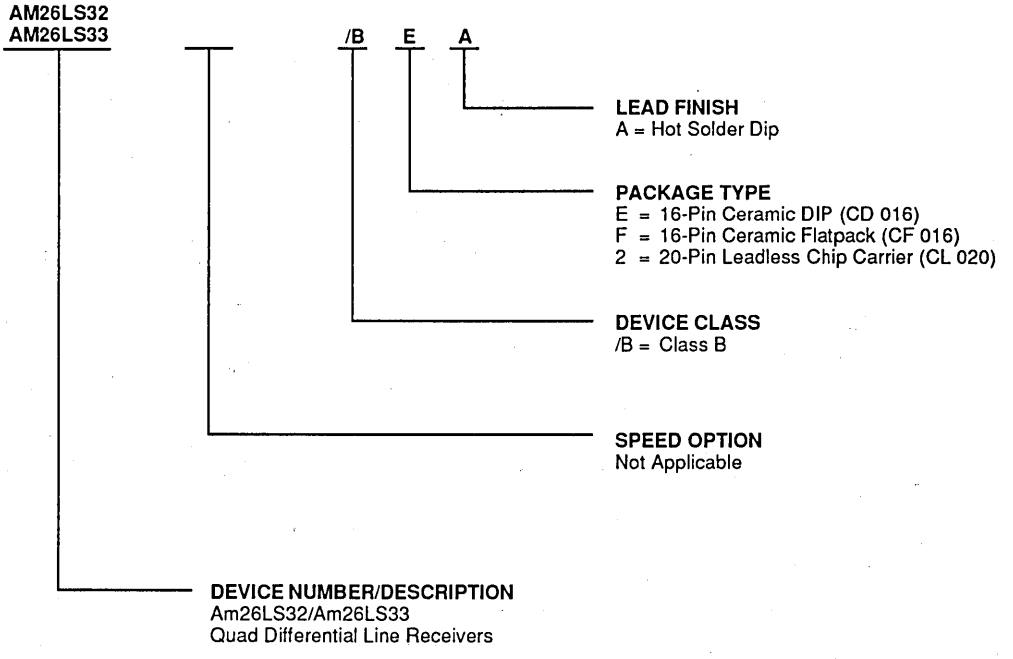
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS32	/BEA, /BFA, /B2A
AM26LS33	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Range	±25 V
Differential Input Voltage	±25 V
Enable Voltage	7.0 V
Output Sink Current	50 mA
Storage Temperature Range	−65 to +165°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0 to +70°C
Supply Voltage	+4.75 V to +5.25 V

Military (M) Devices

Temperature	−55 to +125°C
Supply Voltage	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Unit
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH} (Note 5)	Am26LS32, −7 V ≤ V_{CM} ≤ +7 V	−0.2	±0.06	+0.2	V
			Am26LS33, −15 V ≤ V_{CM} ≤ +15 V	−0.5	±0.12	+0.5	
R_{IN}	Input Resistance	−15 V ≤ V_{CM} ≤ +15 V (One input AC ground) (Note 4)		6.0	9.8		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +15 V, Other Input −15 V ≤ V_{IN} ≤ +15 V				2.3	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −15 V, Other Input −15 V ≤ V_{IN} ≤ +15 V				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., ΔV_{IN} = +1.0 V	COM'L	2.7	3.4		V
		$V_{\overline{ENABLE}}$ = 0.8 V, I_{OH} = −440 µA	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., ΔV_{IN} = −1.0 V	I_{OL} = 4.0 mA			0.4	V
		$V_{\overline{ENABLE}}$ = 0.8 V	I_{OL} = 8.0 mA			0.45	
V_{IL}	Enable LOW Voltage	(Note 2)				0.8	V
V_{IH}	Enable HIGH Voltage	(Note 2)		2.0			V
V_{IC}	Enable Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.5	V
I_O	Off-state (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V			20	µA
			V_O = 0.4 V			−20	
I_{IL}	Enable LOW Current	V_{IN} = 0.4 V, V_{CC} = Max.			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max.				20	µA
I_I	Enable Input High Current	V_{IN} = 5.5 V, V_{CC} = Max.				100	µA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = Max., ΔV_{IN} = +1.0 V (Note 3)		−15	−50	−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5.0 V, V_{CM} = 0 V			30		mV

Notes:

1. All typical values are V_{CC} = 5.0 V, T_A = 25°C.
2. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
3. Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
4. R_{IN} is not directly tested but is correlated. (See Attachment I)
5. Input voltage is not tested directly due to tester accuracy limitation but is threshold correlated. (See Attachment II)

SWITCHING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Unit
AC Parameters (T_A = +25°C)						
t_{PLH}	Propagation Delay From Input to Output	C_L 15 pF, R_{L1} =.5 kΩ, R_{L2} = 2 kΩ, V_{CC} = 5.0		17	25	ns
t_{PHL}	Propagation Delay From Input to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ, V_{CC} = 5.0		17	25	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0, C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		20	30	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0, C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		15	22	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0, C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		15	22	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0, C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		15	22	ns
AC Parameters (–55°C to +125°C)						
t_{PLH}	Propagation Delay From Input to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ,		23	38	ns
t_{PHL}	Propagation Delay From Input to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		22	38	ns
t_{PZH}	Propagation Delay From Enable to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		17	33	ns
t_{PZL}	Propagation Delay From Enable to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		25	33	ns
t_{PHZ}	Propagation Delay From Enable to Output	C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		18	33	ns
t_{PLZ}	Propagation Delay From Enable to Output	C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		24	45	ns
Tristate Delays for $\overline{\text{Enable}}$ (T_A = +25°C)						
t_{PZH}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		16	32	ns
t_{PZL}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		23	33	ns
t_{PHZ}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		14	24	ns
t_{PLZ}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		14	32	ns
Tristate Delays for $\overline{\text{Enable}}$ (–55°C to +125°C)						
t_{PZH}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		23	48	ns
t_{PZL}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 15 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		35	50	ns
t_{PHZ}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		20	36	ns
t_{PLZ}	Propagation Delay From $\overline{\text{Enable}}$ to Output	C_L 5 pF, R_{L1} = 5 kΩ, R_{L2} = 2 kΩ		22	48	ns

Note:

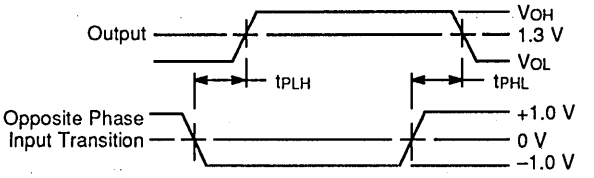
1. All typical values are V_{CC} = 5.0 V, T_A = 25°C.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

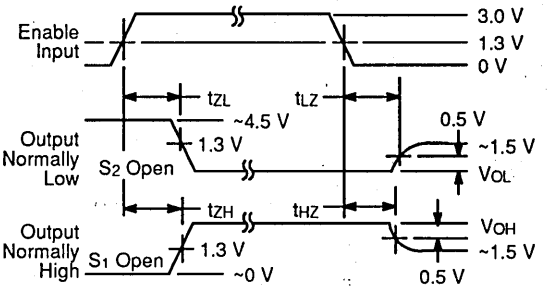
KS000010

SWITCHING WAVEFORMS



Propagation Delay (Notes 1 and 3)

05393-004B



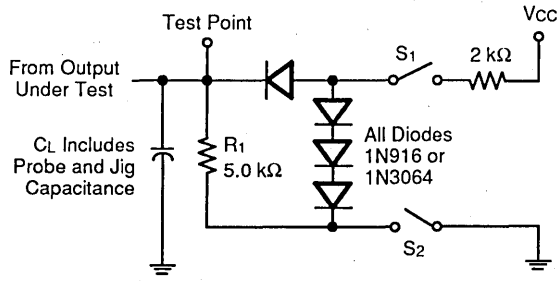
Enable and Disable Times (Notes 2 and 3)

05393-005B

Notes:

1. Diagram shown for $\overline{\text{ENABLE}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω; t_r ≤ 15 ns; t_f ≤ 6.0 ns.

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



05393-006B

Am26LS32/32B/33/34 Input Resistance and Input Current (Attachment I)

Input resistance measurement for differential inputs on line receivers are generally not measured directly. Instead they are correlated to an input current measurement and to the process resistor temperature coefficient. The assumptions made include 1) Process resistor temperature coefficient is known and 2) The open input bias voltage for the input is known or measured within the same test sequence.

Under the above assumptions R_{IN} can be correlated to the input current measured. The expression

$$R_{IN} = \frac{(V_{ICM} - V_{IN})\,(R_T)}{(I_{IN})\,(R25)},$$

where V_{ICM} is the open input bias voltage of the Line Receiver. When applying this correlation to the 26LS32 die, the following criteria have been set.

1) V_{ICM} and I_{IN} are the values screened at wafer sort.
2) Temperature coefficients are for 800 ohm/square which gives 0.96 at 0°C and 0.93 at –55°C.

When setting limits, characterized values for V_{ICM} have been used instead of the test programmed limit value. R_{IN} (dif) is R_{IN} (dif) = 2 R_{IN}.

For the Am26LS32/32B/33/34

$$R_{IN}\ \text{Min.} = \frac{(2.56 - -15)\ 0.96}{I_{IN}\ (\text{Max.})} = 16.8/I_{IN}\ (\text{Max.})\ \text{Comm.},$$

and

R_{IN} Min. = 16.3/I_{IN} (Max.) Mil.

Worst Case Measurement for Input Current

Two considerations have been used to determine the test condition for input current of the data path for the Am26LS32 Line Receiver.

1) Input current is tested on the 26LS32 with the pin under test at one end of the range (+15 V for example) and the untested pin at the opposite extreme of the input range under test. If both pins were at the same test voltage the internal bias generator would have a lower output voltage for tests at –15 V V_{IN} and a higher output voltage at +15 V V_{IN}. This would produce test currents less than maximum.
2) For the 26LS32, breakdown of the differential inputs is the primary failure to the data sheet specification. Hence, both breakdown voltage and input current are tested during the input current tests.

Test Documentation For Am26LS32/32B/34 V_{TH} (Attachment II)

Input threshold (V_{TH}) for the Am26LS32/32B/34 is described by the equation,

V_{TH} = (N+1) (1+R1/R) K*T/Q ((1+Rh/(m (Rc+Rh))) /(1–Rh/ (M(Rc+Rh))).

Where N+1 is the attenuator ratio, R1/R is the attenuator ratio mismatch, M is the ratio of the input stage current to hysteresis stage current, and Rh and Rc are input stage loads. For Am26LS32 – 34 devices which pass function tests, V_{OH} and V_{OL} tests, thresholds for all inputs within the operating range of the circuit.

The Test system is unable to force input thresholds within the accuracy required for the Am26LS32 – 34 specifications. Figure 1 plots the expected values for V_{TH}, the worst case values at 25°C and 155°C. Also shown are the test values for V_{TH} at the –1.5 V input (V_{IN}). In addition, the test voltage at –7 V V_{IN} is shown. For the figure it is seen that the worst case value for the test limit shown would be +/–165 mV, where +/– 102 mV is expected for process parameters and the equation for V_{TH}. Further the 25 mV negative guardband used for –7 V testing is less than half the machine uncertainty of 60 mV.

When QA testing for Am26LS32/32B/34 is done, thresholds are screened for V_{CM} other than –1.5 V. These additional tests are considered functional tests only, and the precision threshold tests which insure compliance with data sheet limits are those tests performed where the inputs are tested near –1.5 V.

The actual threshold tests are done as a sequence where a setup is performed which preconditions the DUT to a logic one state, then the threshold correlation for a logic zero is tested followed by a threshold correlation for logic one to complete the sequence. The limit values for the setup (Vt SET), logic zero test (Vt "–"), and logic one test (Vt "+") are listed under V_{TH} for supply value of 5.0 V.

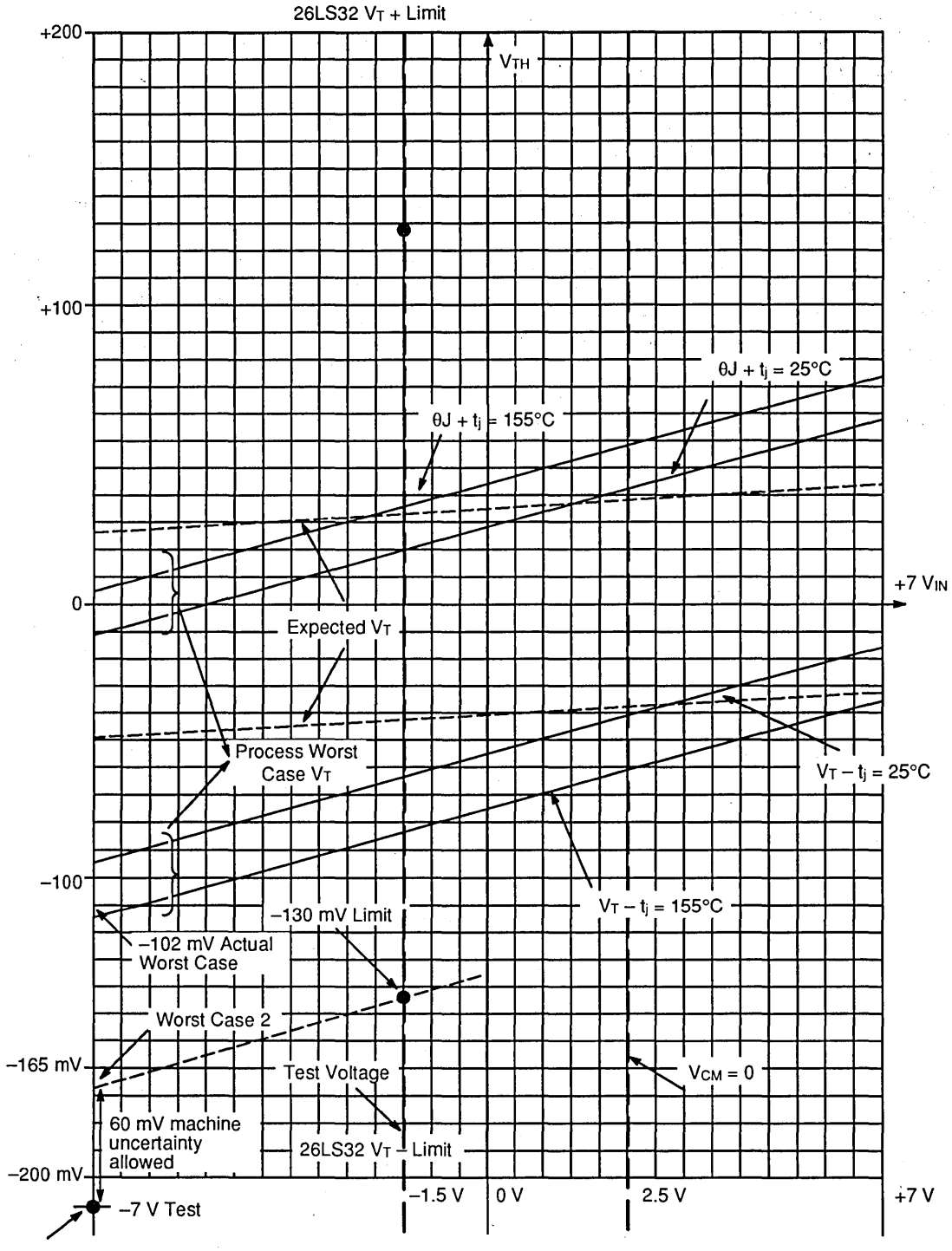


Figure 1. 26LS32 Input Threshold V_T vs. Input Voltage V_{IN}

Am26LS32B

Quad Differential Line Receiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- ±120 mV sensitivity over V_{IN} range of 0 V to 5 V
- ±200 mV sensitivity over V_{CM} range
- –7 V to +12 V input voltage range – differential or common mode
- Guaranteed input voltage hysteresis limits
  - 65 mV minimum
  - 240 mV maximum
- 3 V maximum open circuit input voltage
- Three-state outputs disabled during power-up and power-down
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over COM'L and MIL operating temperature ranges
- Single +5 V supply
- Advanced low-power Schottky processing

GENERAL DESCRIPTION

The Am26LS32B is a quad line receiver designed to meet the requirements of RS-422 and RS-423, CCITT V.10 and V.11, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

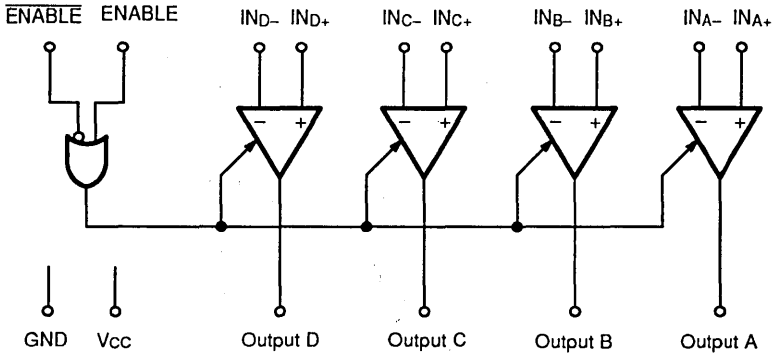
The Am26LS32B features an input sensitivity of 200 mV over the common mode input voltage range of –7 V to +12 V.

The Am26LS32B is the first device in the Am26LS32 configuration to guarantee minimum hysteresis and propagation delay skew while maintaining better propagation delay guarantees than the Am26LS32. This allows a more critical analysis of performance in high noise environments and better performance in terms of signal quality, resulting in better system performance.

The Am26LS32B provides an enable and disable function common to all four receivers. It features three-state outputs with 24 mA sink capability and incorporates a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32B is contructed using Advanced Low-Power Schottky processing.

BLOCK DIAGRAM



01024-001B

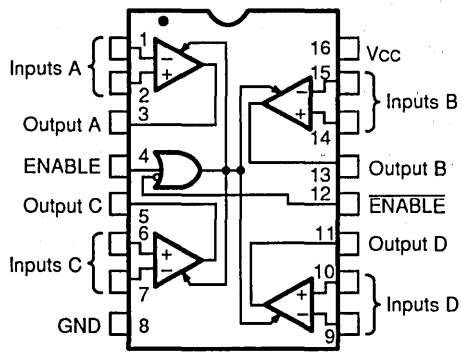
RELATED AMD PRODUCTS

Part No.	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS33	Quad Differential Line Receiver

Publication# 01024 Rev. B Amendment/0
Issue Date: May 1991

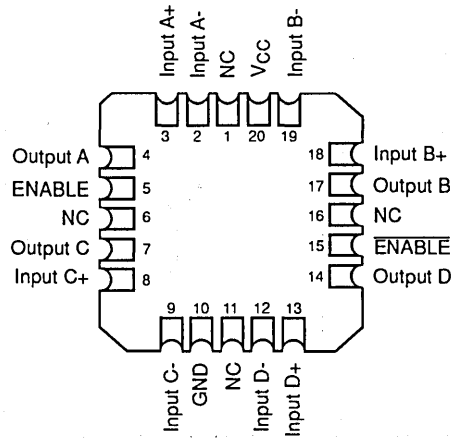
CONNECTION DIAGRAMS
Top View

DIP



01024-002A

LCC

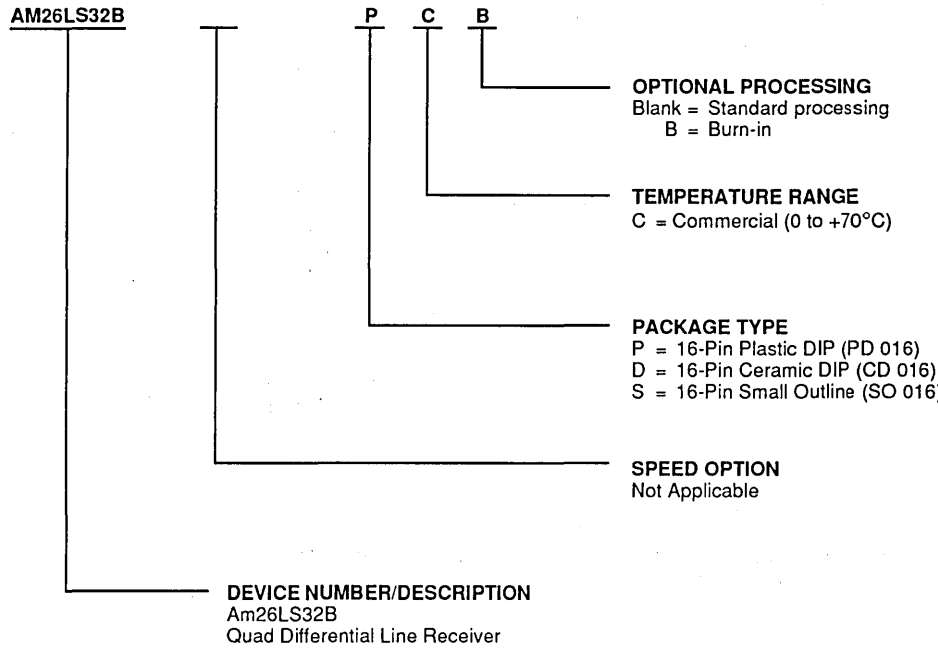


01024-003A

Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS32B	PC, PCB, DC, DCB, SC

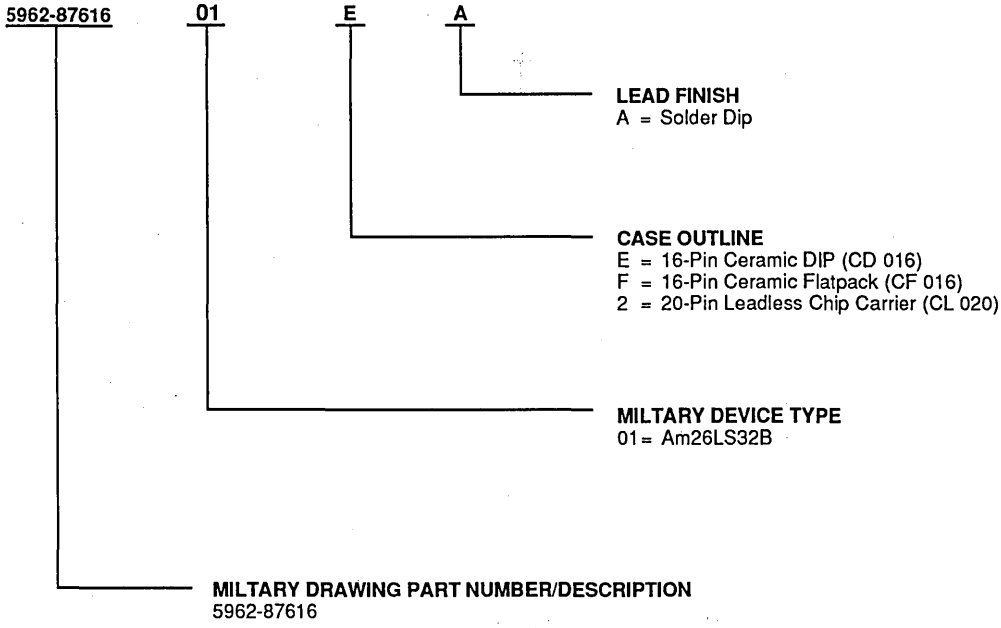
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:



Valid Combinations	
5962-8761601	EA, FA, 2A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

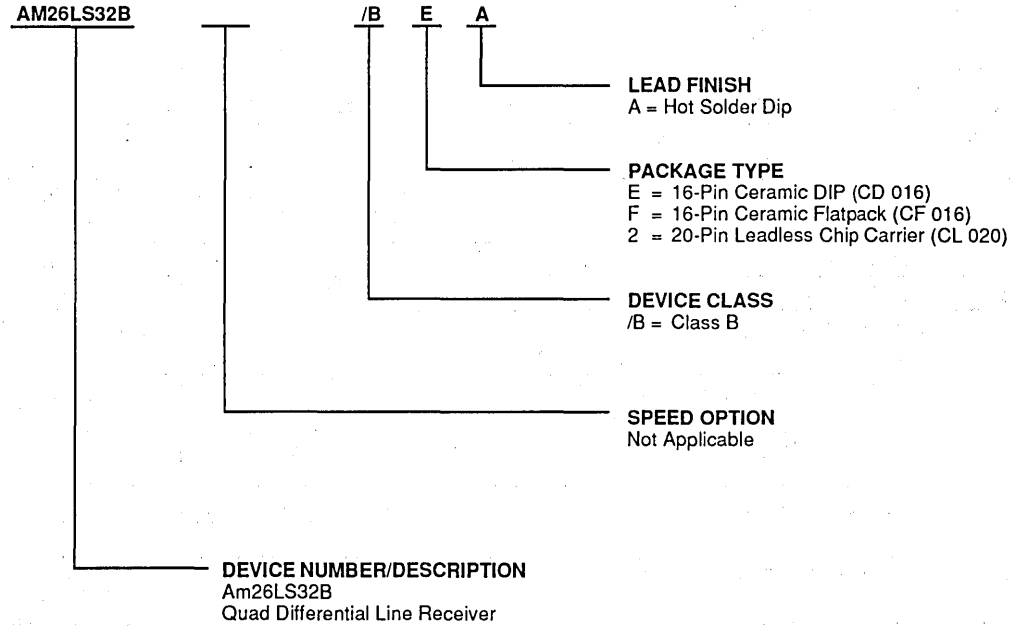
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS32B	/BEA, /BFA, /B2A

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Range	±25 V
Differential Input Voltage	±25 V
Enable Voltage	7.0 V
Output Sink Current	50 mA
Storage Temperature Range	−65 to +165°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0 to +70°C
Supply Voltage	+4.5 V to +5.5 V

Military (M) Devices

Temperature	−55 to +125°C
Supply Voltage	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Unit
V_{TH}	Differential Input Voltage (Note 5)	$V_{OUT} = V_{OL}$ or V_{OH}	$0 \le V_{CM} \le +5$ V	−100	±60	100	mV
			-7 V $\le V_{CM} \le +12$ V	−200		200	
V_{HYST}	Input Hysteresis	V_{CC} = 5.0 V		65		240	mV
V_{IOC}	Open Circuit Input Voltage			1.5		3.0	V
R_{IN}	Input Resistance (Note 4)	-15 V $\le V_{CM} \le +15$ V (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +15 V, Other Input -15 V $\le V_{IN} \le +15$ V				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15$ V, Other Input -15 V $\le V_{IN} \le +15$ V				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., ΔV_{IN} = +1.0 V	$I_{OH} = -12$ mA	2.0			V
		$V_{\overline{ENABLE}}$ = 0.8 V	$I_{OH} = -1$ mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0$ V	I_{OL} = 16 mA			0.4	V
		$V_{\overline{ENABLE}}$ = 0.8 V	I_{OL} = 24 mA			0.5	
V_{IL}	Enable LOW Voltage	(Note 2)				0.8	V
V_{IH}	Enable HIGH Voltage	(Note 2)		2.0			V
V_{IC}	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18$ mA				−1.5	V
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V			50	µA
			V_O = 0.4 V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4 V, V_{CC} = Max.			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max.				20	µA
I_I	Enable Input High Current	V_{IN} = 5.5 V, V_{CC} = Max.				100	µA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = Max., ΔV_{IN} = +1.0 V (Note 3)		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA

Notes:

1. All typical values are V_{CC} = 5.0 V, T_A = 25°C.
2. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
3. Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
4. R_{IN} is not directly tested but is correlated. (See Attachment I)
5. Input voltage is not tested directly due to tester accuracy limitations but is tester correlated. (See Attachment II)

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay, Input to Output	C_L = 50 pF See test circuit		16	21	ns
t_{PHL}				17	21	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			1.5	3.0	ns
t_{ZL}	Output Enable Time, ENABLE to Output			16	22	ns
t_{ZH}				10	16	ns
t_{LZ}	Output Disable Time, ENABLE to Output	C_L = 5 pF See test circuit		11	18	ns
t_{HZ}				13	18	ns

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Input to Output	C_L = 50 pF See test circuit		26		26	ns
t_{PHL}				26		26	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			4.0		4.0	ns
t_{ZL}	Output Enable Time, ENABLE to Output			33		33	ns
t_{ZH}				22		22	ns
t_{LZ}	Output Disable Time, ENABLE to Output	C_L = 5 pF See test circuit		27		27	ns
t_{HZ}				27		27	ns

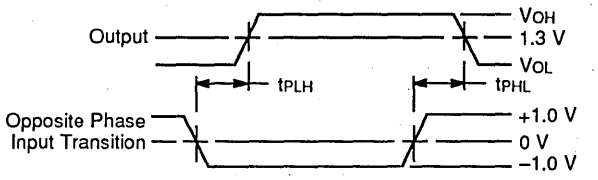
Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
Tristate Delays for $\overline{\text{ENABLE}}$ (T_A = +25°C)						
t_{PZH}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			26	ns
t_{PZL}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			33	ns
t_{PHZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			20	ns
t_{PLZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			20	ns
Tristate Delays for $\overline{\text{ENABLE}}$ (–55°C to +125°C)						
t_{PZH}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			39	ns
t_{PZL}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 50 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			49	ns
t_{PHZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			30	ns
t_{PLZ}	Propagation Delay From $\overline{\text{ENABLE}}$ to Output	C_L 5 pF, R_{L1} = 1 kΩ, R_{L2} = 280 Ω			30	ns

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

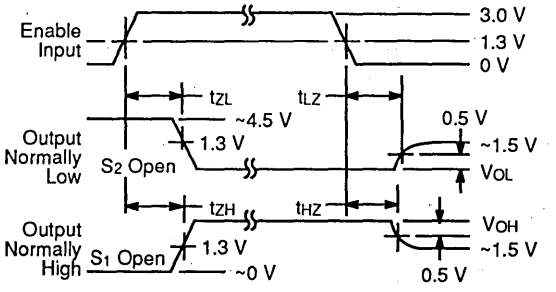
KS000010

SWITCHING WAVEFORMS



Propagation Delay (Notes 1 and 3)

01024-005A



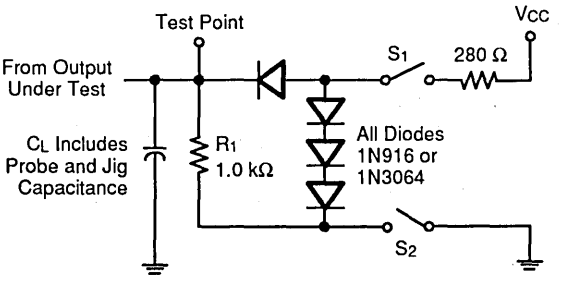
Enable and Disable Times (Notes 2 and 3)

01024-006A

Notes:

1. Diagram shown for ENABLE LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

SWITCHING TEST CIRCUIT FOR THREE-STATE OUTPUTS



01024-007A

Am26LS32/32B/33/34 Input Resistance and Input Current (Attachment I)

Input resistance measurement for differential inputs on line receivers are generally not measured directly. Instead they are correlated to an input current measurement and to the process resistor temperature coefficient. The assumptions made include 1) Process resistor temperature coefficient is known and 2) The open input bias voltage for the input is known or measured within the same test sequence.

Under the above assumptions R_{IN} can be correlated to the input current measured. The expression

$$R_{IN} = \frac{(V_{ICM} - V_{IN})\ (R_T)}{(I_{IN})\ (R25)},$$

where V_{ICM} is the open input bias voltage of the Line Receiver. When applying this correlation to the 26LS32 die, the following criteria have been set.

1) V_{ICM} and I_{IN} are the values screened at wafer sort.
2) Temperature coefficients are for 800 ohm/square which gives 0.96 at 0°C and 0.93 at –55°C.

When setting limits, characterized values for V_{ICM} have been used instead of the test programmed limit value. R_{IN} (dif) is R_{IN} (dif) = 2 R_{IN}.

For the Am26LS32/32B/33/34

$$R_{IN}\ \text{Min.} = \frac{(2.56 - -15)\ 0.96}{I_{IN}\ (\text{Max.})} = 16.8/I_{IN}\ (\text{Max.})\ \text{Comm.},$$

and

R_{IN} Min. = 16.3/I_{IN} (Max.) Mil.

Worst Case Measurement for Input Current

Two considerations have been used to determine the test condition for input current of the data path for the Am26LS32 Line Receiver.

1) Input current is tested on the 26LS32 with the pin under test at one end of the range (+15 V for example) and the untested pin at the opposite extreme of the input range under test. If both pins were at the same test voltage the internal bias generator would have a lower output voltage for tests at –15 V V_{IN} and a higher output voltage at +15 V V_{IN}. This would produce test currents less than maximum.
2) For the 26LS32, breakdown of the differential inputs is the primary failure to the data sheet specification. Hence, both breakdown voltage and input current are tested during the input current tests.

Test Documentation For Am26LS32/32B/34 V_{TH} (Attachment II)

Input threshold (V_{TH}) for the Am26LS32/32B/34 is described by the equation,

V_{TH} = (N+1) (1+R1/R) K*T/Q (1+Rh/(m (Rc+Rh))) /(1–Rh/ (M(Rc+Rh))).

Where N+1 is the attenuator ratio, R1/R is the attenuator ratio mismatch, M is the ratio of the input stage current to hysteresis stage current, and Rh and Rc are input stage loads. For Am26LS32 – 34 devices which pass function tests, V_{OH} and V_{OL} tests, thresholds for all inputs within the operating range of the circuit.

The Test system is unable to force input thresholds within the accuracy required for the Am26LS32 – 34 specifications. Figure 1 plots the expected values for V_{TH}, the worst case values at 25°C and 155°C. Also shown are the test values for V_{TH} at the –1.5 V input (V_{IN}). In addition, the test voltage at –7 V V_{IN} is shown. For the figure it is seen that the worst case value for the test limit shown would be +/–165 mV, where +/– 102 mV is expected for process parameters and the equation for V_{TH}. Further the 25 mV negative guardband used for –7 V testing is less than half the machine uncertainty of 60 mV.

When QA testing for Am26LS32/32B/34 is done, thresholds are screened for V_{CM} other than –1.5 V. These additional tests are considered functional tests only, and the precision threshold tests which insure compliance with data sheet limits are those tests performed where the inputs are tested near –1.5 V.

The actual threshold tests are done as a sequence where a setup is performed which preconditions the DUT to a logic one state, then the threshold correlation for a logic zero is tested followed by a threshold correlation for logic one to complete the sequence. The limit values for the setup (Vt SET), logic zero test (Vt "–"), and logic one test (Vt "+") are listed under V_{TH} for supply value of 5.0 V.

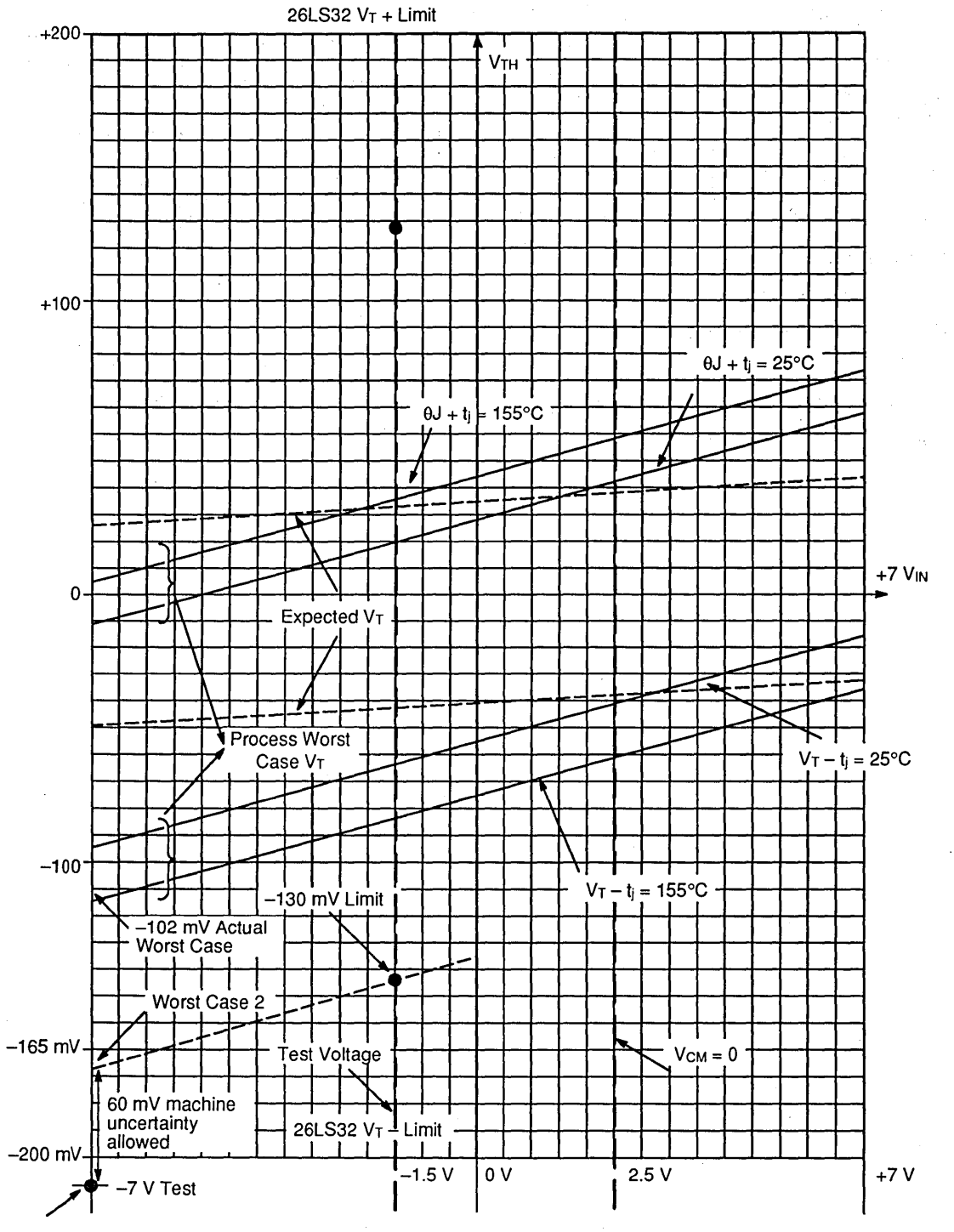


Figure 1. 26LS32 Input Threshold V_T vs. Input Voltage V_{IN}

Am26LS34

Quad Differential Line Receiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Meets all requirements of EIA Standards RS-442, RS-423, CCITT V.10 and V.11, and the new party line standard in development under EIA Project Number 1360.
- ±200 mV sensitivity over input voltage range.
- ±150 mV sensitivity for V_{CM} = 0.
- –7 V to + 12 V common mode input voltage range.
- 12 kΩ minimum input impedance.
- Maximum guarantees for t_{PD} skew.
- All AC and DC parameters guaranteed over military and commercial temperature ranges.
- Guaranteed input voltages hysteresis limits.
  - 120mV minimum
  - 300mV maximum
- No internal failsafe.
- Pin compatible with Am26LS32/32B/33

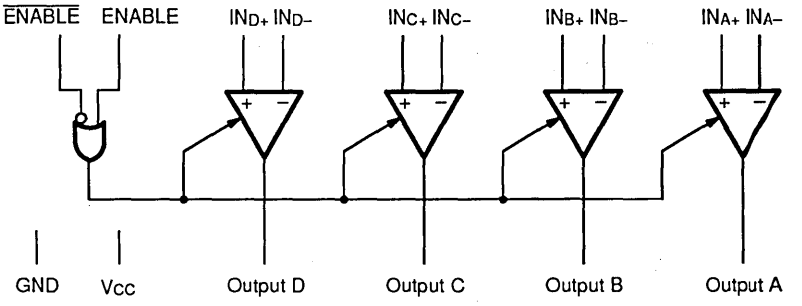
GENERAL DESCRIPTION

The Am26LS34 is a high performance, quad, differential line receiver. It has higher impedance and higher input voltage hysteresis than the similar Am26LS32B. The Am26LS34 also does not have internal fail-safe to allow greater user flexibility.

Input threshold sensitivity is specified for three different V_{CM} ranges. The improved sensitivity, guaranteed hysteresis and skew limits allow a more critical analysis of system performance in high noise environments and better system performance capability.

All performance parameters are guaranteed over ±10% supplies and over the operating temperature range. In addition; I_{OL} is specified to 24 mA for easy system bus interfacing.

BLOCK DIAGRAM



01025-001A

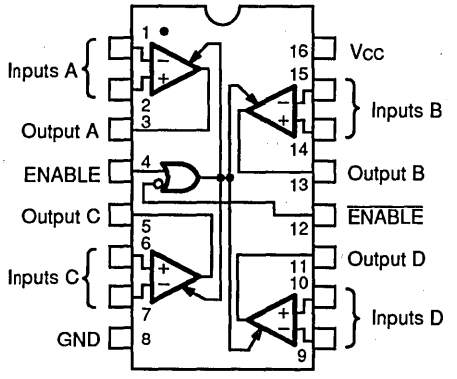
RELATED PRODUCTS

Part Number	Description
26LS29	Quad Three-State Single Ended RS-423 Line Driver
26LS30	Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver
26LS32	Quad Differential Line Receiver
26LS33	Quad Differential Line Receiver

Publication# 01025 Rev. B Amendment/0
Issue Date: May 1991

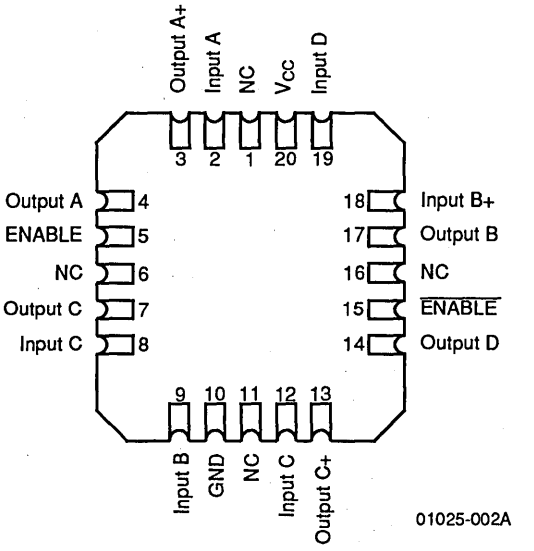
CONNECTION DIAGRAMS
Top View

DIP



01025-003A

LCC

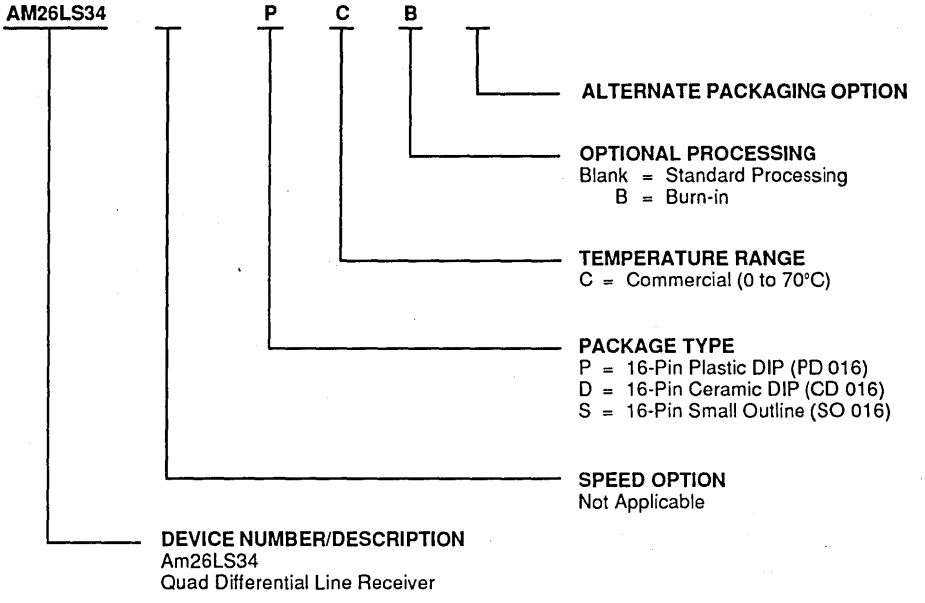


01025-002A

Note:
Pin 1 is marked for orientation

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



AM26LS34	PC, PCB, DC, DCB, SC

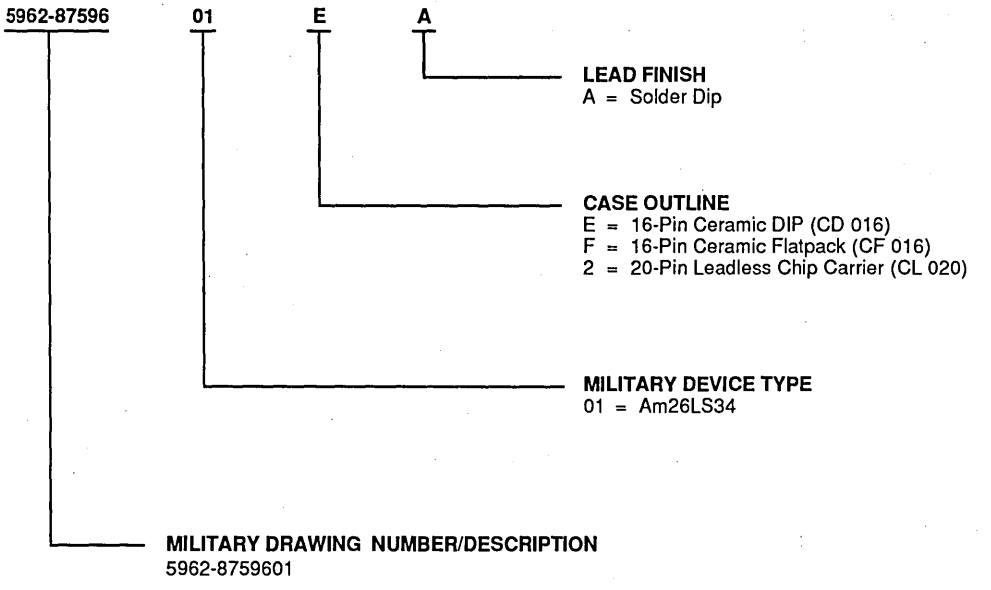
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

Standard Military Drawing Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The ordering number for SMD/DESC (Valid Combination) is formed by a combination of:



5962-8759601	EA, FA, 2A

Valid Combinations

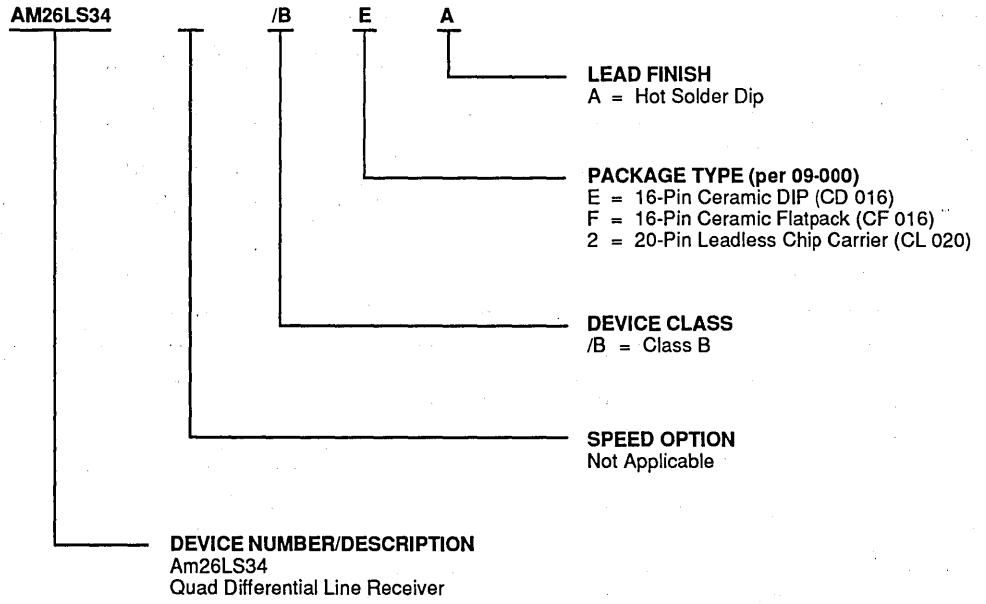
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The ordering number (Valid Combination) is formed by a combination of:



AM26LS34	/BEA, /BFA, /B2A

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Voltage	±25 V
Differential Input Voltage	±30 V
Enable Voltage	7.0 V
Output Sink Current	50mA
Storage Temperature Range	−65°C to +165°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	+4.75 V to +5.25 V

Military (M) Devices

Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH} (Note 5)	$0V < V_{CM} < +5$ V	−100	±90	+100	mV
			$-7V \le V_{CM} \le +12$ V	−200		+200	
			$-15V \le V_{CM} \le +15$ V	−400		+400	
V_{HYST}	Input Hysteresis	V_{CC} = 5.0 V		120	180	300	mV
R_{IN}	Input Resistance	−15 V ≤ V_{CM} ≤ + 15 V (One input AC ground) (Note 4)		12k	20k	40k	Ω
I_{IN}	Input Current (Under Test)	V_{IN} = +12 V			0.7	1.0	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −7 V			−0.5	−0.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., Δ V_{IN} = +1.0 V, $V_{\overline{ENABLE}}$ = 0.8 V	−12 mA	2.0			V
			−1 mA	2.4		3.4	
V_{OL}	Output LOW Voltage	V_{CC} = Min., Δ V_{IN} = −1.0 V, $V_{\overline{ENABLE}}$ = 0.8 V	I_{OH} = 16 mA			0.4	V
			I_{OL} = 24 mA			0.5	
V_{IL}	Enable LOW Voltage	(Note 2)				0.8	V
V_{IH}	Enable HIGH Voltage	(Note 2)		2.0			V
V_I	Enable CLAMP Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.5	V
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	V
I_O	Off-State (High impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4 V			−0.03	−0.2	mA
I_{IH}	Enable HIGH Current	V_{IH} = 2.7 V			0.5	20	μA
I_I	Enable Input High Current	V_{IN} = 5.5 V			1	100	μA
I_{SC}	Output Short Circuit Current	V_O = 0 V, V_{CC} = Max., Δ V_{IN} = +1.0 V (Note 3)		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA

Notes:

1. All typical values are V_{CC} = 5.0 V, T_A = 25°C.
2. Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
3. Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
4. R_{IN} is not directly tested but is correlated. (See Attachment I)
5. Input voltage is not tested directly due to tester accuracy limitations but is tester correlated. (See Attachment II)

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Commercial Am26LS34 Min.	Commercial Am26LS34 Max.	Military Am26LS34 Min.	Military Am26LS34 Max.	Units
t_{PLH}	Propagation Delay, Input to Output	C_L = 50 pF See test circuit		30		30	ns
t_{PHL}				30		30	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$			±5		±5	ns
t_{ZL}	Output Enable Time, ENABLE to Output			33		33	ns
t_{ZH}				22		22	ns
t_{LZ}	Output Disable Time, ENABLE to Output	C_L = 5 pF See test circuit		27		27	ns
t_{HZ}				27		27	ns

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

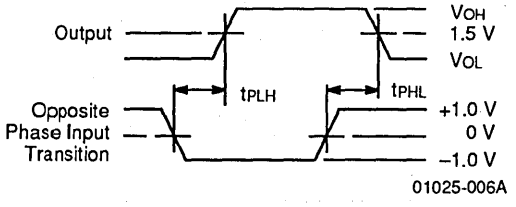
Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay, Input to Output	C_L = 50 pF See test circuit		18	24	ns
t_{PHL}				20	24	ns
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$					
				2	4	ns
t_{ZL}	Output Enable Time, ENABLE to Output			16	22	ns
t_{ZH}				10	16	ns
t_{LZ}	Output Disable Time, ENABLE to Output	C_L = 5 pF See test circuit		11	18	ns
t_{HZ}				13	18	ns
Tristate Delays For Enable Bar						
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{PZH}	Propagation Delay From ENABLE BAR to Output	C_L = 50 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			26	ns
t_{PZL}	Propagation Delay From ENABLE BAR to Output	C_L = 50 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			33	ns
t_{PHZ}	Propagation Delay From ENABLE BAR to Output	C_L = 5 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			20	ns
t_{PLZ}	Propagation Delay From ENABLE BAR to Output	C_L = 5 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			20	ns
t_{PZH}	Propagation Delay From ENABLE BAR to Output	C_L = 50 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			39	ns
t_{PZL}	Propagation Delay From ENABLE BAR to Output	C_L = 50 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			49	ns
t_{PHZ}	Propagation Delay From ENABLE BAR to Output	C_L = 5 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			30	ns
t_{PLZ}	Propagation Delay From ENABLE BAR to Output	C_L = 5 pF, R_{L1} = 1 KΩ, R_{L2} = 280 Ω			30	ns

KEY TO SWITCHING WAVEFORMS

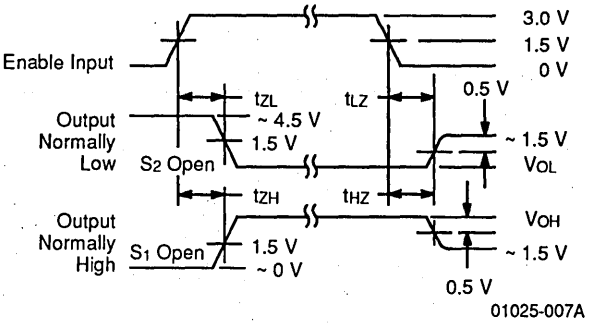
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



Propagation Delay
(Notes 1 and 3)

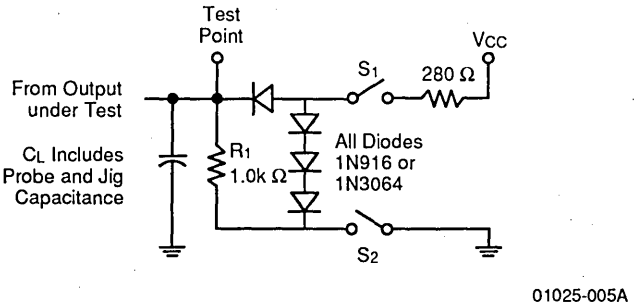


Enable And Disable Times
(Notes 2 and 3)

Notes:

1. Diagram shown for $\overline{\text{ENABLE}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator Rate ≤ 1.0 MHz; $Z_0 = 50\Omega$; t_r; $t_f \leq 2.5$ns.

SWITCHING TEST CIRCUIT



Three-State Outputs

ATTACHMENT I

Am26LS32/32B/33/34 Input Resistance and Input Current

Input resistance measurement for differential inputs on line receivers are generally not measured directly. Instead they are correlated to an input current measurement and to the process resistor temperature coefficient. The assumptions made include 1) Process resistor temperature coefficient is known and 2) The open input bias voltage for the input is known or measured within the same test sequence.

Under the above assumptions R_{IN} can be correlated to the input current measured. The expression

$$R_{IN} = \frac{(V_{ICM} - V_{IN})\ (R_T)}{(I_{IN})\ (R25)},$$

where V_{ICM} is the open input bias voltage of the Line Receiver. When applying this correlation to the 26LS32 die, the following criteria have been set.

1) V_{ICM} and I_{IN} are the values screened at wafer sort.
2) Temperature coefficients are for 800 ohm/square which gives 0.96 at 0°C and 0.93 at –55°C.

When setting limits, characterized values for V_{ICM} have been used instead of the test programmed limit value. R_{IN} (dif) is R_{IN} (dif) = 2 R_{IN}.

For the Am26LS32/32B/33/34

$$R_{IN}\ \text{Min.} = \frac{(2.56 - -15)\ 0.96}{I_{IN}\ (\text{Max.})} = 16.8/I_{IN}\ (\text{Max.})\ \text{Comm.},$$

and

R_{IN} Min. = 16.3/I_{IN} (Max.) Mil.

Worst Case Measurement for Input Current

Two considerations have been used to determine the test condition for input current of the data path for the Am26LS32 Line Receiver.

1) Input current is tested on the 26LS32 with the pin under test at one end of the range (+15 V for example) and the untested pin at the opposite extreme of the input range under test. If both pins were at the same test voltage the internal bias generator would have a lower output voltage for tests at –15 V V_{IN} and a higher output voltage at +15 V V_{IN}. This would produce test currents less than maximum.
2) For the 26LS32, breakdown of the differential inputs is the primary failure to the data sheet specification. Hence, both breakdown voltage and input current are tested during the input current tests.

ATTACHMENT II

Test Documentation For Am26LS32/32B/34 V_{TH}

Input threshold (V_{TH}) for the Am26LS32/32B/34 is described by the equation,

V_{TH} = (N+1) (1+R1/R) K*T/Q ((1+Rh/(m (Rc+Rh))) /(1–Rh/ (M(Rc+Rh))).

Where N+1 is the attenuator ratio, R1/R is the attenuator ratio mismatch, M is the ratio of the input stage current to hysteresis stage current, and Rh and Rc are input stage loads. For Am26LS32 – 34 devices which pass function tests, V_{OH} and V_{OL} tests, thresholds for all inputs within the operating range of the circuit.

The Test system is unable to force input thresholds within the accuracy required for the Am26LS32 – 34 specifications. Figure 1 plots the expected values for V_{TH}, the worst case values at 25°C and 155°C. Also shown are the test values for V_{TH} at the –1.5 V input (V_{IN}). In addition, the test voltage at –7 V V_{IN} is shown.

For the figure it is seen that the worst case value for the test limit shown would be +/–165 mV, where +/– 102 mV is expected for process parameters and the equation for V_{TH}. Further the 25 mV negative guardband used for –7 V testing is less than half the machine uncertainty of 60 mV.

When QA testing for Am26LS32/32B/34 is done, thresholds are screened for V_{CM} other than –1.5 V. These additional tests are considered functional tests only, and the precision threshold tests which insure compliance with data sheet limits are those tests performed where the inputs are tested near –1.5 V.

The actual threshold tests are done as a sequence where a setup is performed which preconditions the DUT to a logic one state, then the threshold correlation for a logic zero is tested followed by a threshold correlation for logic one to complete the sequence. The limit values for the setup (Vt SET), logic zero test (Vt "–"), and logic one test (Vt "+") are listed under V_{TH} for supply value of 5.0 V.

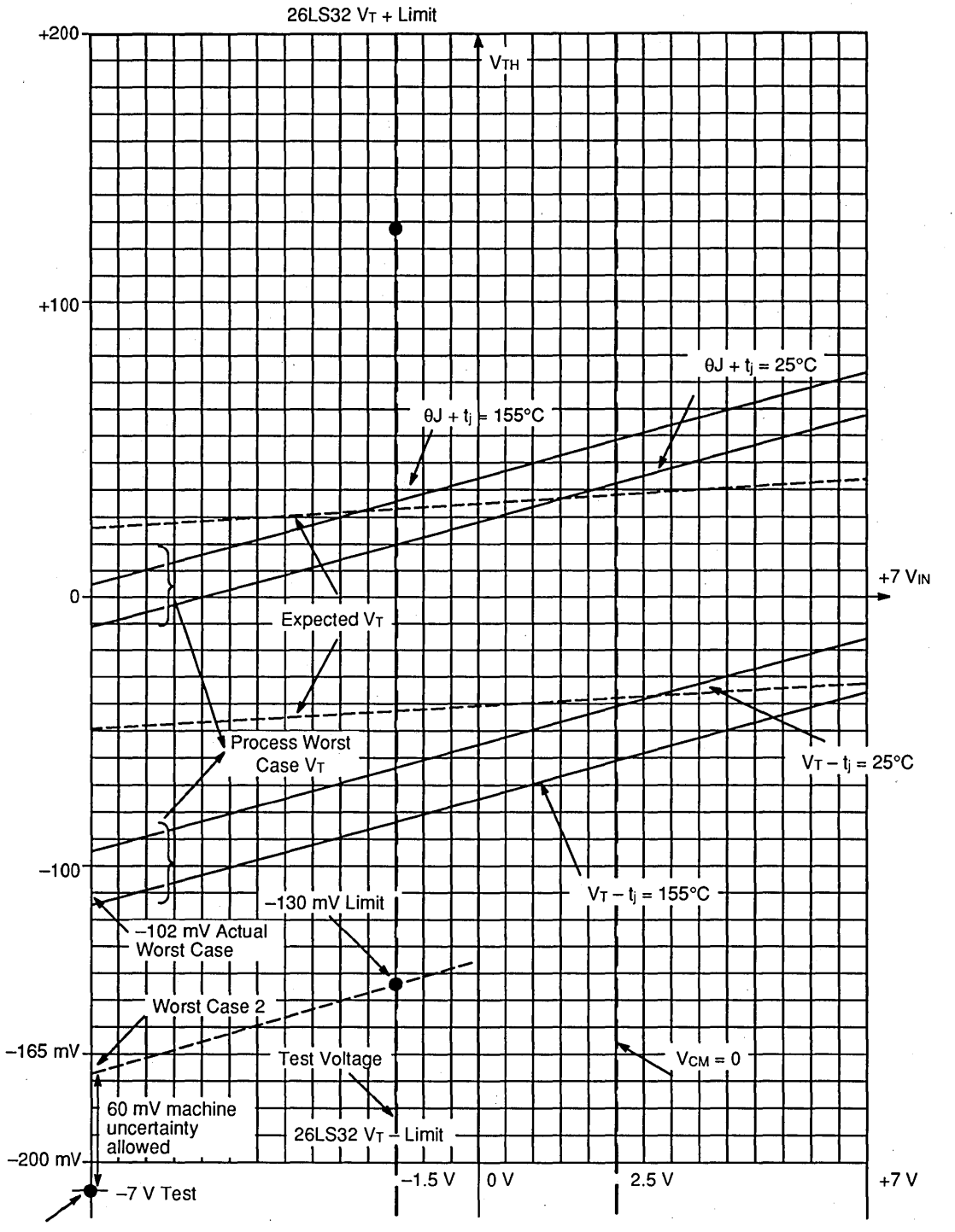


Figure 1. 26LS32 Input Threshold V_T vs. Input Voltage V_{IN}

Am26LS38

Quad Differential Backplane Transceiver

Advanced Micro Devices

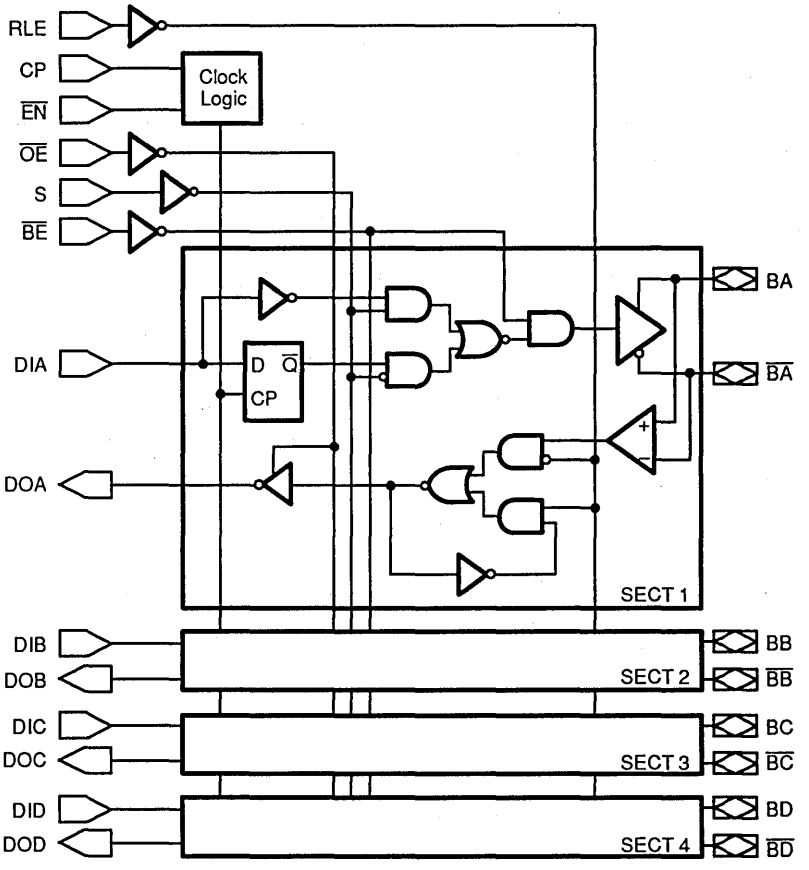
DISTINCTIVE CHARACTERISTICS

- 10 Mb data rate
- 0.45 V DC noise margin
- Biasing line terminations allow low voltage swing while maintaining high noise margin
- Pair delay 55 ns maximum
- Controlled driver skew to minimize noise
- Driver register and receiver latch with register bypass mode
- Driver output short-circuit protected to V_{CC} limits
- Outputs disabled during power-up and down
- Three-state receiver outputs maintain Hi-Z during power-up and down and over V_{CC} range

GENERAL DESCRIPTION

The Am26LS38 is a high performance backplane transceiver designed to integrate Schottky TTL performance, high noise immunity and wired logic capability into a low cost differential backplane structure. The resulting backplane can have up to 24 receiver unit loads in a party-line, wired-OR logic configuration, with a guaranteed fail-safe state, and operates from a single 5 V power supply.

BLOCK DIAGRAM

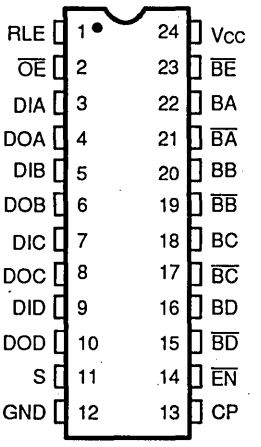


02163-001C

Publication# 02163 Rev. C Amendment/0
Issue Date: May 1991

CONNECTION DIAGRAM
Top View

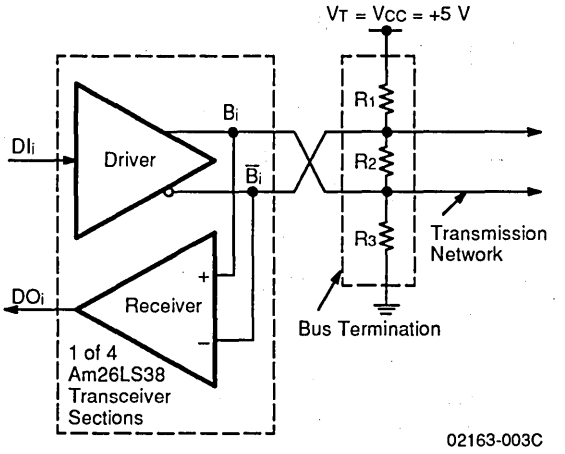
DIP



02163-002C

Note:
Pin 1 is marked for orientation.

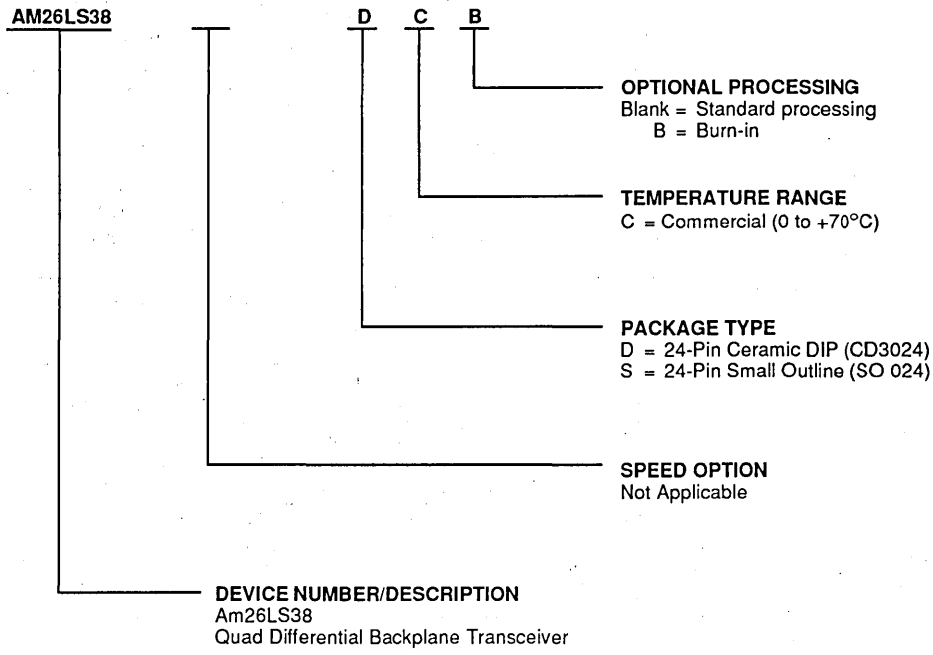
SYSTEM CONFIGURATION DIAGRAM



02163-003C

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM26LS38	DC, DCB, SC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
22, 20 18, 16, 21, 19, 17, 15	BA, BB, BC, BD (B_i), $\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$ ($\overline{B_i}$)	I/O	Paired open emitter (B_i)/ open collector ($\overline{B_i}$) driver outputs and receiver inputs. The driver outputs are either simultaneously active or simultaneously inactive. In the inactive state (DI_i = LOW) both drivers (B_i and $\overline{B_i}$) are turned off and the voltage differential representing the OFF state is determined by the line terminating resistor networks. In the active state (DI_i = HIGH), both drivers are driven on and act to reverse the voltage differential across the line to produce the ON state. The open-emitter/open-collector outputs are always connected in a wried-OR (or wired-AND) configuration. A driver is disabled by making its outputs inactive.
23	$\overline{BE}$	I	Bus Enable operates to enable or disable all output drivers by making them inactive when $\overline{BE}$ = HIGH and controlled by data input when $\overline{BE}$ = LOW.
13	CP	I	Clock Pulse input to the driver register enters data on the LOW-to-HIGH transition.
3, 5, 7, 9	DIA, DIB, DIC, DID (DI_i)	I	Data inputs each driver's buffer or register. A HIGH input to DI_i will result in an active (ON) output. A LOW input will cause an inactive (OFF) output.
4, 6, 8, 10	DOA, DOB, DOC, DOD (DO_i)	O	Receiver data latch outputs. An inactive bus (OFF state) will produce a LOW DO_i output and an active bus (ON state) will produce a HIGH DO_i output.
14	$\overline{EN}$	I	Clock Enable for the driver registers. $\overline{EN}$ = LOW enables DI_i data to be clocked into the respective register. $\overline{EN}$ = HIGH acts to hold previous data in each register regardless of the state of CP.
2	$\overline{OE}$	I	Output Enable for the receiver latch output buffer. When $\overline{OE}$ is LOW the outputs are enabled. When $\overline{OE}$ is HIGH all receiver outputs are in the high impedance state.
1	RLE	I	Receiver Latch Enable for the receiver latches. When RLE is HIGH the latches are transparent. When RLE is LOW received data meeting the setup and hold requirements relative to the HIGH-to-LOW transition of RLE will be stored.
11	S	I	Select input control for the drivers. When S is HIGH driver data from the registers will be selected (Register Mode). When S is LOW (Buffer Mode) the drivers respond to the DI_i inputs directly, bypassing the driver registers.

Inputs									Outputs			
RLE	CP	$\overline{EN}$	$\overline{OE}$	S	$\overline{BE}$	DI_i	B_i	$\overline{B_i}$	B_i	$\overline{B_i}$	DO_i	Function
H	X	X	L	L	L	L	NA	NA	L	H	L	Driver buffer mode (loop test)
H	X	X	L	L	L	H	NA	NA	H	L	H	
H	↑	L	L	H	L	L	NA	NA	L	H	L	Driver register mode
H	↑	L	L	H	L	H	NA	NA	H	L	H	
H	X	X	L	X	H	X	L	H	NA	NA	L	Receiver latch mode
H	X	X	L	X	H	X	H	L	NA	NA	H	
L	X	X	L	X	H	X	X	X	X	X	DO_{in-1}	Receiver in circulation
X	X	X	H	X	H	X	X	X	X	X	Z	Receiver output in high impedance state

H = HIGH

L = LOW

↑ = LOW-to-HIGH transition of clock

DO_{in-1} = Previous state of DO_i

Z = High impedance

X = Don't care

NA = Not applicable

FUNCTIONAL DESCRIPTION

The Am26LS38 represents a new approach in backplane transceiver design. Its unipolar differential signaling scheme minimizes problems associated with crosstalk and the loss of noise immunity due to common mode voltage while providing high speed, party line and wired logic capabilities.

A good ground system and shielding are the best methods for limiting noise on the backplane. Ground planes can significantly reduce inductive ground voltage ringing. Where multilayer PC backplane are not a reasonable choice, a differential bus can be created using the Am26LS38 and twisted pair or any balanced transmission medium.

A backplane designed with an Am26LS38 has 3 main elements; 1) a driver section, 2) a receiver section, 3) and a controlled impedance differential line with a pre-biasing line termination. The scheme for driver, receiver, and termination resistors is shown in Figure A.

System Operation

The system has two operational states.

1. Active – driver outputs on
2. Passive – driver outputs off

This 2-state (active/passive) operation makes passive or wired logic functions possible. In the passive state, the lines assume a known polarity and voltage (pre-biased bus). The passive bus state may be assigned either the false (wired-OR) or true (wired-AND) sense, potentially reducing the number of backplane signal lines.

The 2-state driver employs active pull-down (open collector) and active pull-up (open emitter) output stages (Figure A). When a driver is active, both output stages turn on. This impresses a 0.5 V minimum voltage differential on the bus, reversing the voltage across R_2. In the passive mode both output stages are off. The voltage levels and polarities return to the conditions set by the pre-biasing resistive network. In either state the voltage across the differential lines are symmetrical about $V_{CC}/2$. The system achieves high speeds because the voltage levels required to change state are very close together.

The receiver is designed with a ±50 mV threshold voltage. This low threshold level combined with a driver output greater than 500 mV provides a high degree of tolerance to attenuation and reflection effects in the cable. Receiver hysteresis provides differential noise immunity. Without hysteresis, a small amount of noise around the switching threshold could cause errors.

Propagation delay skew ($t_{PHL} - t_{PLH}$) is controlled. The system allows up to 1.5 V of common mode voltage.

Terminating the Transmission Line or Bus

Common mode reflections in the line can be reduced significantly by symmetrically terminating the bus. This increases the tolerance to common mode noise. Centering the network at $V_{CC}/2$ ($R_1 = R_3$) further improves the performance by causing all induced noise and reflections to appear as a common mode signal (Figure B).

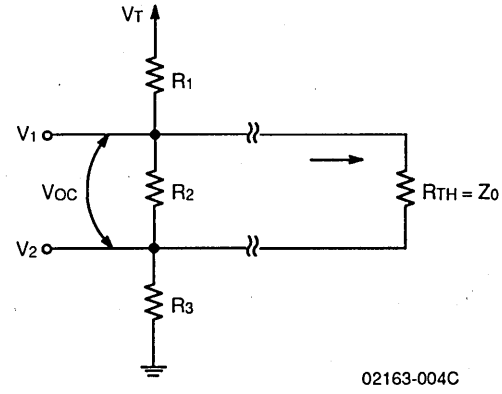


Figure B. Termination Circuit

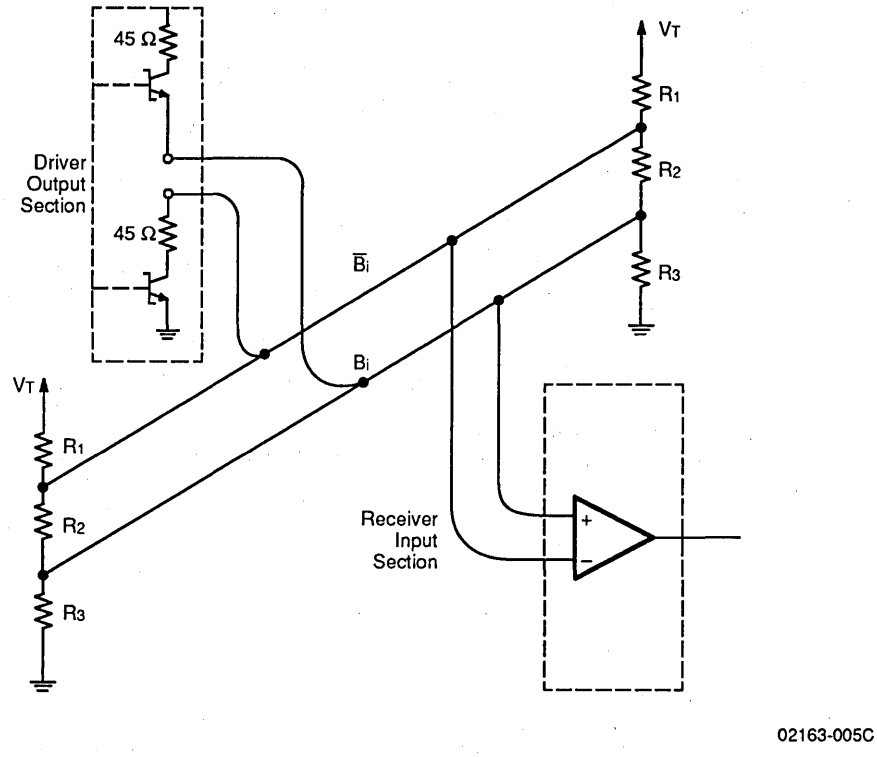


Figure A. The Scheme for Driver, Receiver, and Termination Resistors

A first order approximation of resistor values may be developed by letting the ratio of R_1 to R_2 be 2:1, and the Thevenin equivalent resistance of the termination equal the characteristic impedance of the line (Z_0).

Then:

$$(1)\ V_{OC} = V_T \frac{R_2}{R_2 + 2R_1}$$

$$(2)\ R_{TH} = \frac{2R_1R_2}{2R_1 + R_2}$$

From equation (1) and (2),

$$(3)\ R_1 = \frac{V_T R_{TH}}{2V_{OC}}$$

$$(4)\ R_2 = \frac{V_T R_{TH}}{V_T - V_{OC}}$$

If $V_T = 5$ V, $V_{OC} = 1.0$ V, and $R_{TH} = 90\Omega = Z_0$, we can derive that $R_1 \sim 220\Omega$, $R_2 \sim 110\Omega$.

Second order adjustments require attention to unit loading factors (receiver differential input resistance is in parallel with R_2), transmission rates and a host of other factors.

Data Path

Figure C shows the data path from one driver to another receiver for one bit of the bus interface.

The transmit register or buffer and receiver latch are configured to provide two modes of operation. The register and latch can provide local storage for output and input data. In the non-storage mode the buffer input to the driver can be selected and the receiver can be wired transparent. Incorporating storage on-chip provides improved speed and lower package count without significant penalty in the non-storage mode.

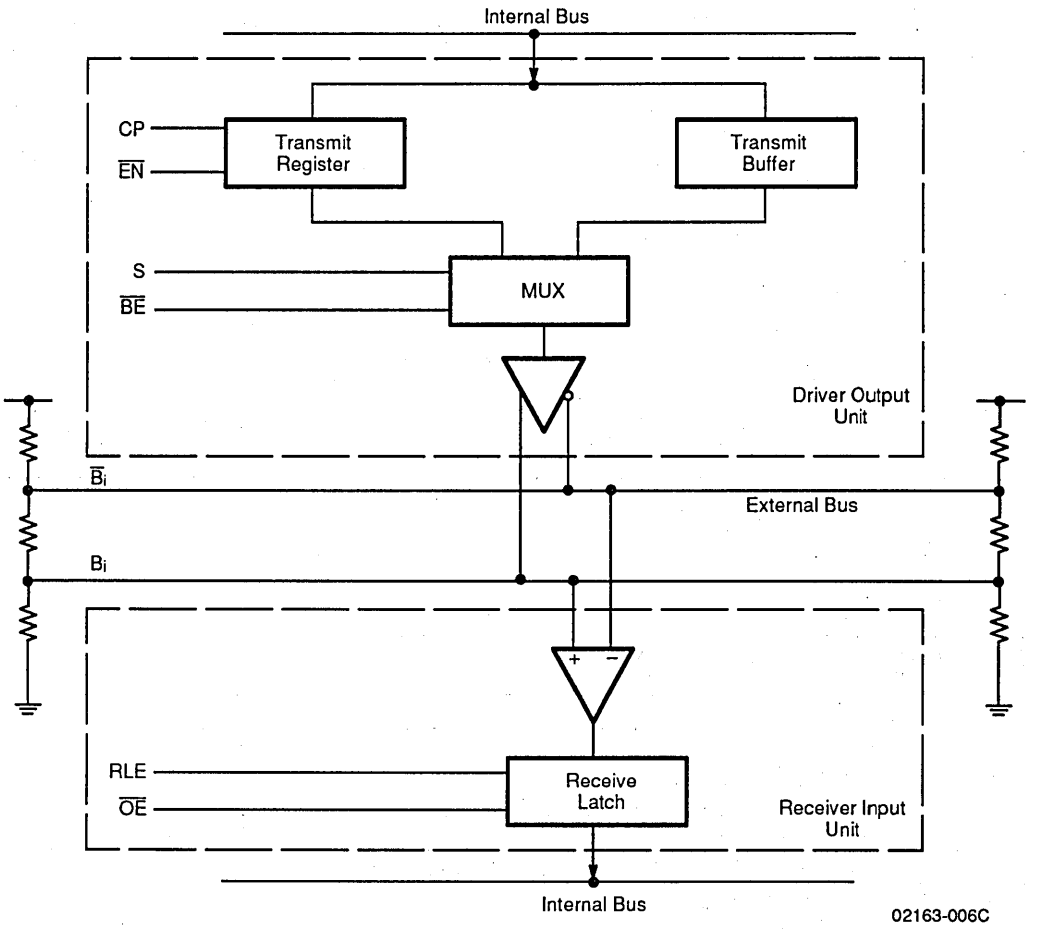
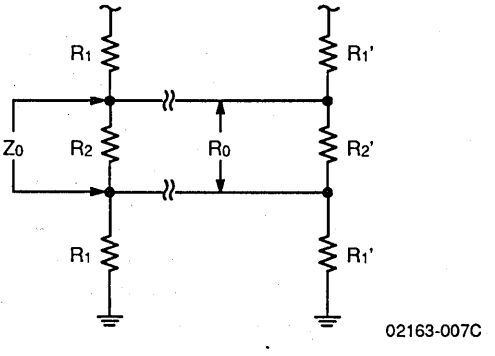


Figure C. The Data Path for One Bit of the Bus Interface



Equivalent Circuit Recommended Termination

Termination Resistors and Equivalent Impedance

Z_0	$R_1 = R_1'$	$R_2 = R_2'$
90Ω	220Ω	110Ω
120Ω	300Ω	150Ω

Minimum line V_0 (differential voltage) = 0.5 V

Equivalent Termination Versus DC Resistance

Z_0	R_0
88.0Ω	44.0Ω
120.0Ω	60.0Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0 V
Common Mode Range	0 to Vcc
Differential Mode Range (REC)	0 to Vcc
Logic Inputs	5.5 V
Storage Temperature Range	−65 to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0 to +70°C
Supply Voltage	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
Bus Driver Output							
V_O	Output Differential Voltage (Driver Active) $V_{Bi} - \overline{V}_{Bi}$	$\overline{BE}$ = LOW DI_i = HIGH Test Circuit #1		0.5			V
I_{SS}	Output Current	DI_i = HIGH Test Circuit #2 $\overline{BE}$ = LOW	Ia	−22.5	−55	−115	mA
			Ib	+22.5	+55	+115	
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5 V		−75	−150	−250	mA
Bus Receiver Input							
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 to Vcc V_{OUT} = V_{OL} or V_{OH}		−50	±10	+50	mV
R_{IN}	Input Resistance to GND	0 ≤ Vcc ≤ Vcc Max.		4	5.7		kΩ
R_{IN}	Differential Input Resistance	0 ≤ Vcc ≤ Vcc Max.		8	11.4		kΩ
V_{OS}	Center Voltage	Test Circuit #3 Active and Passive		2.0	Vcc/2	3.0	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Center Voltage Difference (Active vs Passive)	Test Circuit #3			90	300	mV
Non-Bus Input and Outputs							
V_{OH}	Output HIGH Voltage	ΔV_{IN} = +0.1 V	I_{OH} = −15 mA	2.4	3.4		V
			I_{OH} = −24 mA	2.0	3.3		
V_{OL}	Output LOW Voltage	ΔV_{IN} = −0.1 V	MIL, I_{OL} = 32 mA			0.5	V
			COM'L, I_{OL} = 48 mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	Data		−275	−400	µA
			Control		−0.65	−1.0	mA
			Clock		−0.65	−1.0	mA
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			0.1	+50	µA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5 V		−75	−150	−250	mA
I_I	Input Leakage Current	V_{IN} = 5.5 V				1	mA
V_{IC}	Input Clamp Voltage	I_{IN} = −18 mA			−0.75	−1.2	V
I_{OZ}	Leakage Current Passive	V_O = 2.4 V				+50	µA
		V_O = 0.4 V				−50	
I_{CC}	Power Supply Current	$\overline{BE}$, $\overline{OE}$ = HIGH				145	mA

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description		Test Conditions		Min.	Typ.	Max.	Unit
t_{DBA}	DI_i to $Bi/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW, S = LOW	Test Circuit #1		7	10	ns
t_{DBP}		Passive				7	10	
t_{CBA}	CP to $Bi/\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW, S = HIGH	Test Circuit #1		10.5	16	ns
t_{CBP}		Passive				13	16	
t_{PA}	$\overline{BE}$ to $Bi/\overline{B}_i$ Propagation Delay	Active	DI_i = HIGH, S = LOW	Test Circuit #1		8.5	12	ns
t_{PP}		Passive				4	8	
t_S	DI_i to Clock Setup Time		$\overline{BE}$ = LOW		5	2.5		ns
t_H	DI_i to Clock Hold Time				2	0		
t_S	$\overline{EN}$ to Clock Setup Time				8	4		
t_H	$\overline{EN}$ to Clock Hold Time				0	–4		
t_S	$Bi/\overline{B}_i$ to RLE Setup Time				5	2.5		
t_H	$Bi/\overline{B}_i$ to RLE Hold Time				2	0.7		
t_{PLZ}/t_{PHZ}	$\overline{OE}$ to DO_i Disable Time		C_L = 50 pF	Test Circuit #4			20	ns
t_{PLZ}/t_{PHZ}			C_L = 5 pF	Test Circuit #4			13	
t_{PZL}	$\overline{OE}$ to DO_i Disable Time		Test Circuit #4				17	ns
t_{PZH}							17	
t_{PLH}	RLE to DO_i		$\overline{OE}$ = LOW	Test Circuit #4		11	13	ns
t_{PHL}						14	17	
t_{PRX}	$Bi/\overline{B}_i$ to DO_i		RLE = HIGH, $\overline{OE}$ = LOW	Test Circuit #4		12	17	ns
t_{PLH}	$\overline{BE}$ to DO_i Propagation Delay		RLE = HIGH, $\overline{OE}$ = LOW	Test Circuits #1, #4		15	25	ns
t_{PLH}	DI_i to DO_i (Buffer Mode)		S = LOW, RLE = HIGH, $\overline{OE}$ = LOW	Test Circuits #1, #4		18	25	ns
t_{PHL}								
t_{PLH}	CP to DO_i (Register Mode)		S = HIGH, RLE = HIGH, $\overline{OE}$ = LOW	Test Circuits #1, #4		22	28	ns
t_{PHL}								
t_{PWL}	Clock Pulse Width	LOW			10	3		ns
t_{PWH}		HIGH			10	5		
t_{PWH}	RLE Pulse Width	HIGH			10	6		ns
t_{SKEW}	Propagation Delay Skew ($t_{PLH} - t_{PHL}$)		V_{CC} = 5 V, C_L = 50 pF, Measurement $V_{CC}/2$	Test Circuit #1		±1	±5	ns

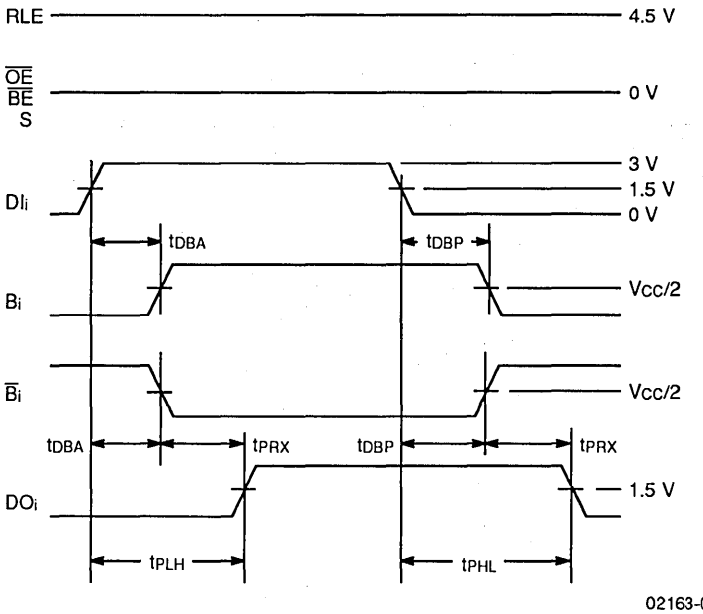
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions		T_A = 0 to +70°C, V_{CC} = 5.0 V ±10% Min.	Max.	Unit
t_{DBA}	DI_i to B_i/$\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW	Test Circuit #1		12	ns
t_{DBP}		Passive	S = LOW			12	
t_{CBA}	CP to B_i/$\overline{B}_i$ Propagation Delay	Active	$\overline{BE}$ = LOW	Test Circuit #1		20	ns
t_{CBP}		Passive	S = HIGH			20	
t_{PA}	$\overline{BE}$ to B_i/$\overline{B}_i$ Propagation Delay	Active	DI_i = HIGH	Test Circuit #1		17	ns
t_{PP}		Passive	S = LOW			12	
t_S	DI_i to Clock Setup Time		$\overline{BE}$ = LOW		7		ns
t_H	DI_i to Clock Hold Time				3		
t_S	$\overline{EN}$ to Clock Setup Time				10		
t_H	$\overline{EN}$ to Clock Hold Time				0		
t_S	B_i/$\overline{B}_i$ to RLE Setup Time				7		
t_H	B_i/$\overline{B}_i$ to RLE Hold Time				3		
t_{PLZ}/t_{PHZ}	$\overline{OE}$ to DO_i Disable Time		C_L = 50 pF	Test Circuit #4		17	ns
t_{PLZ}/t_{PHZ}			C_L = 5 pF	Test Circuit #4		10	
t_{PZL}	$\overline{OE}$ to DO_i Enable Time		Test Circuit #4			15	ns
t_{PZH}						15	
t_{PLH}	RLE to DO_i		$\overline{OE}$ = LOW	Test Circuit #4		15	ns
t_{PHL}						20	
t_{PRX}	B_i/$\overline{B}_i$ to DO_i		RLE = HIGH $\overline{OE}$ = LOW	Test Circuit #4		21	ns
t_{PLH}	$\overline{BE}$ to DO_i Propagation Delay		RLE = HIGH $\overline{OE}$ = LOW	Test Circuits #1, #4		32	ns
t_{PHL}							
t_{PLH}	DI_i to DO_i (Buffer Mode)		S = LOW RLE = HIGH $\overline{OE}$ = LOW	Test Circuits #1, #4		30	ns
t_{PHL}							
t_{PLH}	CP to DO_i (Register Mode)		S = HIGH RLE = HIGH $\overline{OE}$ = LOW	Test Circuits #1, #4		35	ns
t_{PHL}							
t_{PWL}	Clock Pulse Width	LOW			10		ns
t_{PWH}		HIGH			10		
t_{PWH}	RLE Pulse Width	HIGH			13		ns
t_{SKEW}	Propagation Delay Skew (t_{PLH} – t_{PHL})		V_{CC} = 5 V C_L = 50 pF Measurement V_{CC}/2	Test Circuit #1		±7	ns

KEY TO SWITCHING WAVEFORMS

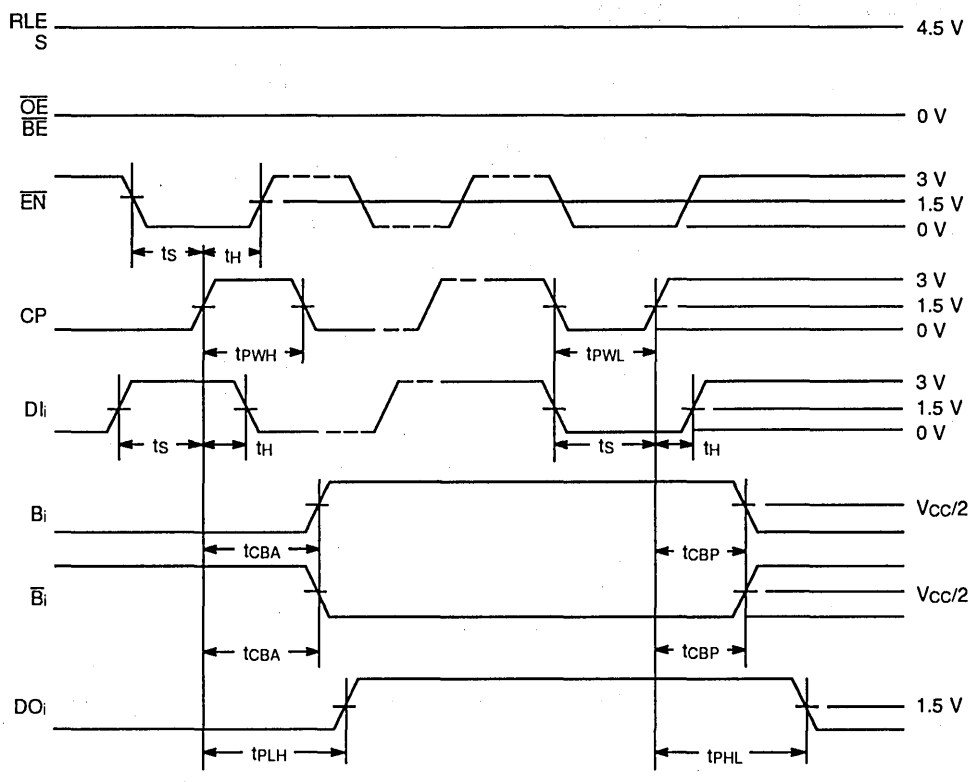
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010



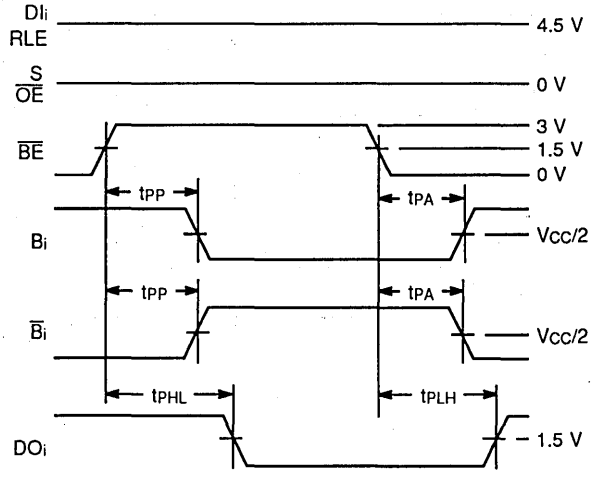
02163-008C

DIi to Bi,Bi, DOi (Buffer Mode)



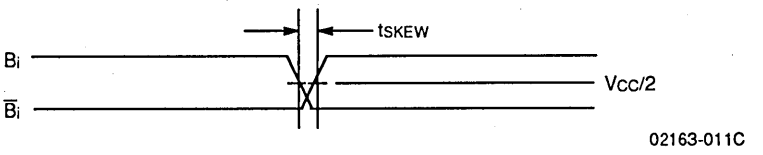
02163-009C

CP to B_i,$\overline{B}_i$, DO_i (Register Mode)

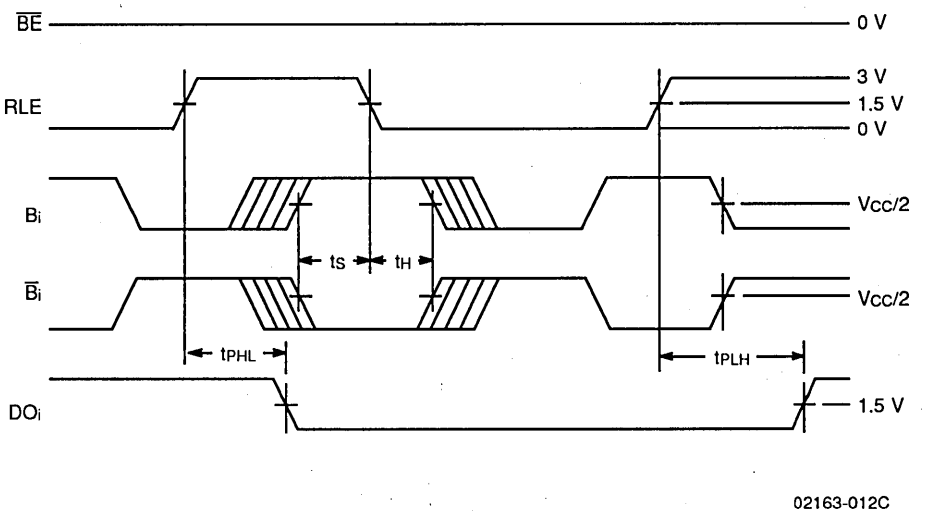


02163-010C

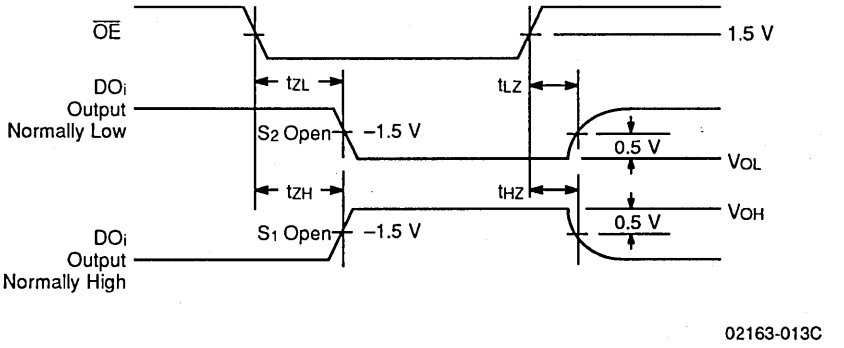
$\overline{BE}$ to B_i,$\overline{B}_i$, DO_i (Passive and Active)



Output to Output

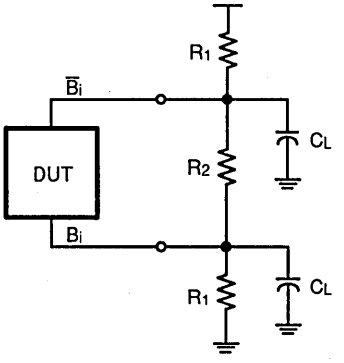


RLE to DO_i



$\overline{OE}$ to DO_i

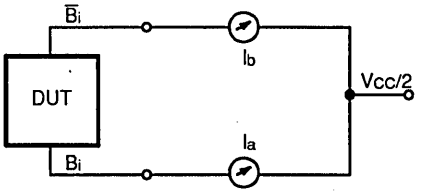
SWITCHING TEST CIRCUITS



R1 = 200Ω
R2 = 50Ω
CL = 50pF

02163-014C

Test Circuit #1



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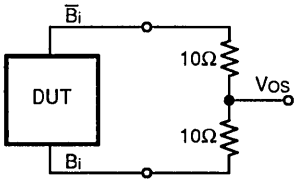
Test Circuit #2



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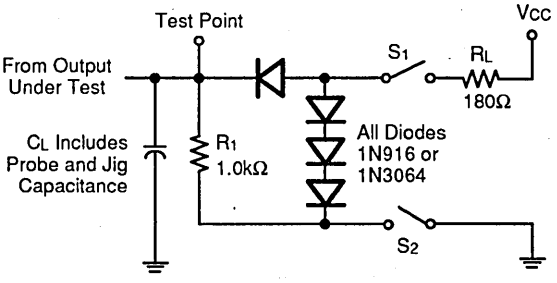
Test Circuit #3



02163-017C

Test Circuit #4

Notes:

1. C_L = 50 pF unless otherwise specified.
2. S_1 and S_2 are closed except where shown.

Use of the Am26LS29, 30, 31 and 32 Quad Driver/Receiver Family in EIA RS-422 and 423 Applications

INTRODUCTION

EIA RS-423 is an unbalanced, bipolar voltage specification designed to interface with RS-232C, while greatly enhancing its operation. It permits the communication of digital information over distances of up to 2000 feet and at data rates of up to 300 Kilobaud. EIA RS-422 is a balanced voltage digital interface for communication of digital data over distances of 4000 feet or data rates of up to 10 megabaud.

Advanced Micro Devices has developed a family of monolithic Low-power Schottky quad line drivers and receivers to meet the requirements of these specifications.

The Am26LS29 and 30 line drivers and the Am26LS32 receiver meet all requirements of RS-423 while the Am26LS31 differential line driver and the Am26LS32 receiver meet the requirements of RS-422.

A second receiver element, the Am26LS33 is available for use in high common mode noise environments, exceeding the common mode voltage requirements of RS-411 and RS-423.

This application note reviews the use of these devices in implementing the EIA RS-422 balanced interface.

EIA STANDARD SPECIFICATION

Two basic forms of operation are available for transmission of digital data over interconnecting lines. These are the single ended and differential techniques.

The single-ended form uses a single conductor to carry the signal with the voltage referenced to a single return conductor. This may also be the common return for other signal conductors Figure 1a.

The single-ended form is the simplest way to send data as it requires only one signal line per circuit. This simplicity, however, is often offset by the inability of this form to allow discrimination between a valid signal produced by the driver, and the sum of the driver signal plus externally induced noise signals.

A solution to some of the problems inherent in the single-ended form of operation is offered by the differential form of operation. Figure 1b. This consist of a differential driver (essentially two single-ended drivers with one driver always producing the complementary output signal level to the other driver), a twisted pair transmission

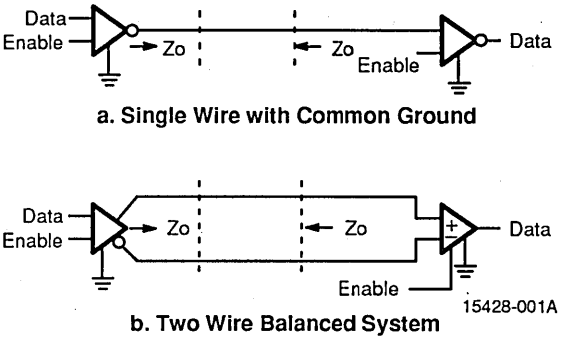


Figure 1. Data Communication Techniques

line and a differential line receiver. The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a common mode signal. The two signals, therefore, can be discriminated by a line receiver with a sufficient common mode voltage operating range.

The Electronic Industries Association, EIA, has defined a number of specifications standardizing the interface between data terminal equipment and data circuit terminating equipment based on both single-ended and differential operation.

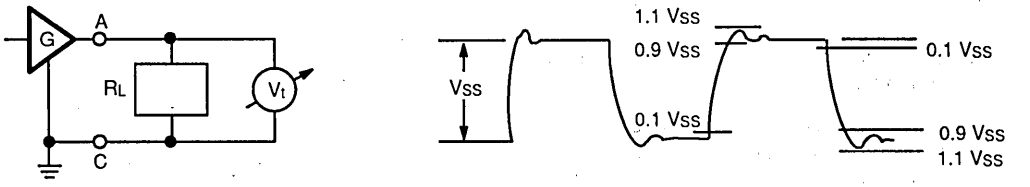
The RS-232C electrical interface is a single-ended, bipolar-voltage, unterminated circuit. This specification is for serial binary data interchange over short distances (up to 50 feet) at low rates (up to 20 Kilobaud). It is a protocol standard as well as an electrical standard, specifying hand shaking signals and functions between terminal and the communications equipment. As already noted, single-ended circuits are susceptible to all forms of electromagnetic interference. Noise and cross talk susceptibility are proportional to length and bandwidth. RS-232C places restrictions on both. It limits slew rate of the drivers (30 V/μs) to control radiated emission on neighboring circuits and allows bandwidth limiting on the receivers to reduce susceptibility to cross talk. The length and slew rate limits can adequately control reflections on unterminated lines, and the length and bandwidth limits are more than adequate to reduce susceptibility to noise.

Like EIA RS-232C, EIA RS-423 is also a single-ended, bipolar-voltage unterminated circuit. It extends the dis-

Publication #	Rev.	Amendment	Issue Date
15428	A	/0	5/91

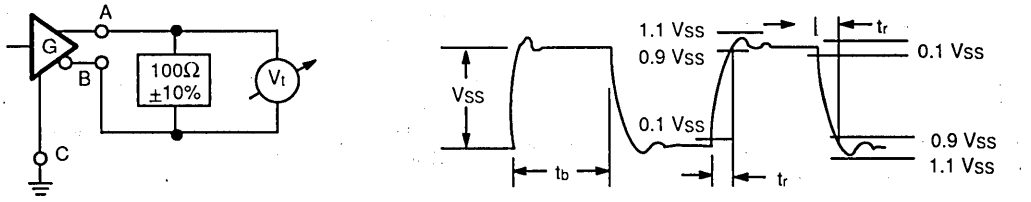
tance and data rate capabilities of this technique to distances of up to 4000 feet at data rates of 3000 baud, or at higher rates of up to 300 Kilobaud over a maximum distance of 40 feet.

EIA RS-422 is a differential, balanced voltage interface capable of significantly higher data rates over longer distances. It can accommodate rates of 100 Kilobaud over a distance of 4000 feet or rates of up to 10 megabaud. These performance improvements stem from the advantages of a balanced configuration which is isolated from ground noise currents. It is also immune to fluctuating voltage potentials between system ground references and to common mode electromagnetic interference. Figure 2 compares the driver output waveforms for the three EIA standard configurations, while Table 1 compares the key characteristics required by drivers and receivers intended for these applications. Since RS-232C has been in use for many years, RS-422 and 423 parameter values have been selected to facilitate an orderly transition from existing designs to new equipment.



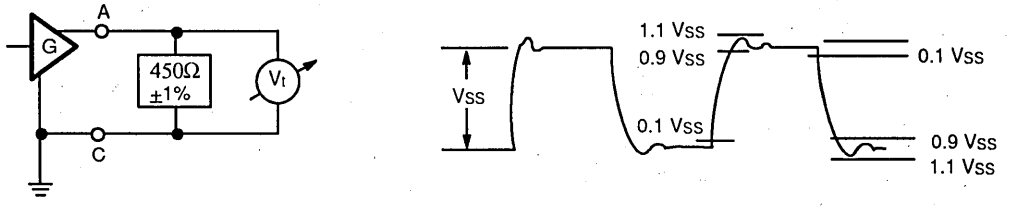
$V_{SS} = |V_t - \overline{V_t}|$
V_{SS} = Differences in steady state voltages
R_L = 3KΩ to 7KΩ
V_{SS} min. = ±5 V; V_{SS} max. = ±25 V

a. EIA RS-232C Generator Output



t_D = Time duration of the unit interval at the applicable modulation rate
$t_r \leq 0.1\ t_D$ when $t_D \geq 200ns$
$t_r \leq 20ns\ t_D$ when $t_D < 200ns$
V_{SS} = Differences in steady state voltages
$V_{SS} = |V_t - \overline{V_t}|$
V_{SS} min. = 2 V; V_{SS} max. = 6 V

b. EIA RS-422 Generator Output



$V_{SS} = |V_t - \overline{V_t}|$
V_{SS} = Difference in steady state voltages
V_{SS} min. = ±3.6 V; V_{SS} max. = ±6 V

c. EIA RS-423 Generator Output

Figure 2. Driver Output Waveforms

Table 1. Key Parameters Of EIA Specifications

Characteristics	EIA RS–232C	EIA RS–423	EIA RS–422	Units
Form of Operation Max. cable length Max. data rate	Single Ended 50 20K	Single Ended 2000 300K	Differential 4000 10M	 Feet Baud
Driver output voltage, open circuit*	±25	±6	6 volts between outputs	Volts (Max.)
Driver output voltage, loaded output*	±5 to ±15	±3.6	2 volts between outputs	Volts (Min.)
Driver output resistance power off	Ro = 300Ω	100μA between −6 to +6 V	100μA between +6 and −.25 V	Min.
Driver output short circuit current ISC	±500	±150	±150	mA (Max.)
Driver output slew rate	30 V/μsec Max.	Slew rate must be controlled based upon cable length and modulation rate	No control necessary	
Receiver input resistance Rin	3K to 7K	≥4K	≥4K	Ω
Receiver input thresholds	−3 to +3	−0.2 to +0.2	−0.2 to +0.2	Volts (Max.)
Receiver input voltage	−25 to +25	−12 to +12	−12 to +12	Volts (Max.)

* ± indicates polarity switched output.

INTEGRATED CIRCUIT CHARACTERISTICS

The Am26LS29, 30, 31 and 32 are a family of quad drivers and receivers designed specifically to meet the EIA standards. These products utilize Low-Power Schottky technology to incorporate four drivers or four receivers, together with control logic, in standard 16-pin package outlines.

The Am26LS29/30 and the Am26LS32 are driver and receiver pairs designed to implement the single-ended EIA RS-423 standard. The Am26LS31 is a differential line driver designed for use with the Am26LS32 receiver in a differential mode to meet EIA RS-422.

AM26LS29 AND AM26LS30 QUAD RS-423 LINE DRIVERS

The Am26LS29 and 30 consist of four single-ended line drivers designed to meet or exceed the requirements of RS-423. The buffered driver outputs are provided with sufficient source and sink current capability to drive 50 ohm to a virtual ground transmission line and high capacitive loads. The Am26LS29 has a three-state output control while the Am26LS30 has a Mode control input that allows it to operate as a dual RS-422 driver (with suitable power supply changes), Figure 3.

Each of the four driver inputs, as well as the $\overline{\text{Enable}}$/Mode Control input is a PNP Low-Power Schottky input for reduced input loading, one-half the normal fan-in. Since there are two inverters from each input to output, the driver is non-inverting. When operating in the RS-423 mode, the Am26LS29 and 30 require both +5 V and −5 V nominal value power supplies. This allow the outputs to swing symmetrically about ground—producing a true bipolar output. The mode Control (Pin 4) of the Am26LS30 should be HI or tied to V_{CC}. Each output is designed to drive the RS-423 load of 50 ohms with an output voltage equal or greater than +3.6 V in the HI state and −3.6 V in the LO state. Each output is current limited to 150 mA max. in either logic state. A Slew Rate control pin is brought out separately for each output to allow output ramp rate (rise and fall time) control. This provides suppression of near end cross talk to other receivers in the cable. Connecting a capacitor from this node to that driver's respective output will produce a ramp (10% to 90%) of 50 ns typical for each picofarad of capacitance in that capacitor. RS-423 establishes recommended ramp rates versus length of line driven and modulation rate, Figure 4.

Table 2. Advanced Micro Devices' EIA Compatible Devices

EIA Standard	Drivers	Receivers
RS-422	Am26LS31 Quad Differential with three-state control gating	AM26LS32 Quad Differential Driver single-ended Receiver
RS-423	Am26LS29 Quad Driver with three-state output Am26LS30 Quad Driver with slew rate control	Am26LS32 Quad single-ended/ Differential Receiver

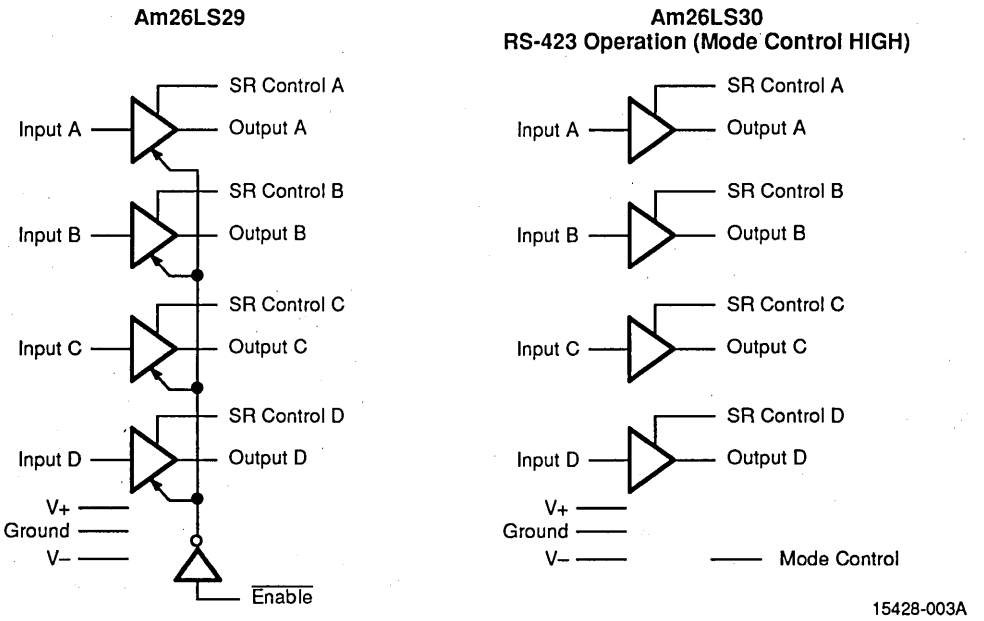
The Am26LS30 can be use at low data rates as a dual EIA RS-422 driver with three-state outputs by connecting the V_{EE} supply and the mode control input to ground.

AM26LS31 QUAD RS-422 DRIVER

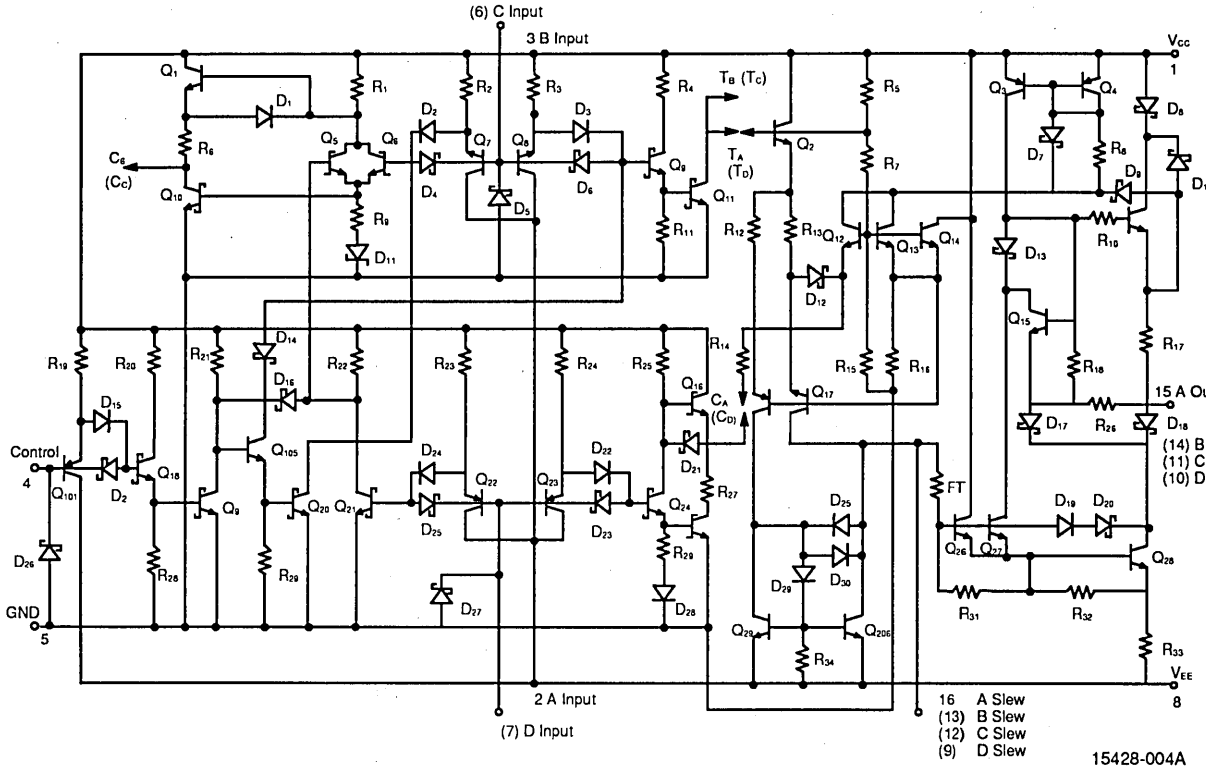
The Am26LS31 is a quad differential line driver designed to meet the RS-422 specification while operating with a single +5 V supply. A common enable and disable function controls all four drivers, Figure 5. The driver features high speed, de-skewed differential outputs with typical propagation delays of 12 ns and residual skew of 2 ns. Both differential line outputs are designed for three-state operation to allow two-way half duplex and multiplex, data bus applications.

Table 3 is a summary of the essential requirements of the RS-422 standard. Section A describes the key characteristics satisfied by the Am26LS31 driver.

The balanced differential line driver consists of two halves, each of which is similar to a Low-power Schottky TTL gate with equal source and sink current capability. The two halves are emitter coupled in a differential input configuration. One side of the input circuit is tied to a fixed TTL bias threshold and the other side is tied to a sink diode in normal DTL/TTL fashion. This configuration offers complementary outputs with very low skew, dependent only upon component matching a necessity to meet RS-422.



a. Logic Diagrams



b. Circuit Diagram for Am26LS30

Figure 3. Am26LS29 and Am26LS30 Drivers.

The circuit diagram of the driver is shown in Figure 6. The emitter-coupled input circuit is formed by Q2 and Q3, which are biased by a current source. This source is a current mirror, formed by Q1 which supplies the current, and D6 which is diode connected transistor matched to Q1. The fixed bias for Q3, formed by D5 and D6, is 2VBE. A 2VBE bias, less the D2 Schottky diode drop, provides the normal Low-power Schottky TTL threshold, V_{IL} = 0.7 V. R19 provides a boost to 0.8V for a full 400 mV TTL noise margin. The differential outputs of the emitter coupled stage, A and $\overline{A}$, drive emitter followers Q14 and Q15, which provide the required speed and matching characteristics. The emitter followers, drive phase splitters Q4 and Q5, which in turn drive totem-pole outputs. The outputs at the line interface are of standard Low-power Schottky TTL configuration, except that circuits values are modified to provide high sourcing capability. The outputs are designed to source or sink 20 mA each, so that they can generate a voltage of at least 2.0 V across a 100 ohm load, as required by RS-422. Additional circuitry has been included to make the line outputs three-state for two-way bus applications. The Am26LS31 meets the RS-422 requirement that the driver not load the line in the powered down condition ($I_X \leq 100\ \mu A$) or if the power supply to that device should fail.

AM26LS32 QUAD RS-422 AND 423 RECEIVER

The Am26LS32 is a quad line receiver which, operating from a single 5 volt supply, can be used in either differential or single-ended modes to satisfy RS-422 and 423 applications respectively. A complementary enable and disable feature, similar to that on the driver, controls all four receivers, Figure 7. The device's three-state outputs, which can sink 8 mA, incorporate a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 meets the receiver input specification of Table 3, a 200 mV threshold sensitivity with common mode rejection exceeding the supply line potentials, (greater than 7 V). The same design feature of the input circuit which provides the common mode rejection also insures excellent power supply ripple rejection, which is important when switching the high currents involved in a system's interfaces. Furthermore, unlike operational amplifiers, where the DC common mode and power

supply rejection ratios roll off with open loop gain, the full rejection capability of this line receiver is maintained at high frequencies. The receiver hysteresis of typically 30 mV, provides differential noise immunity. Signals received on long lines can have slow transition times, and without hysteresis, a small amount of noise around the switching threshold can cause errors in the receiver output.

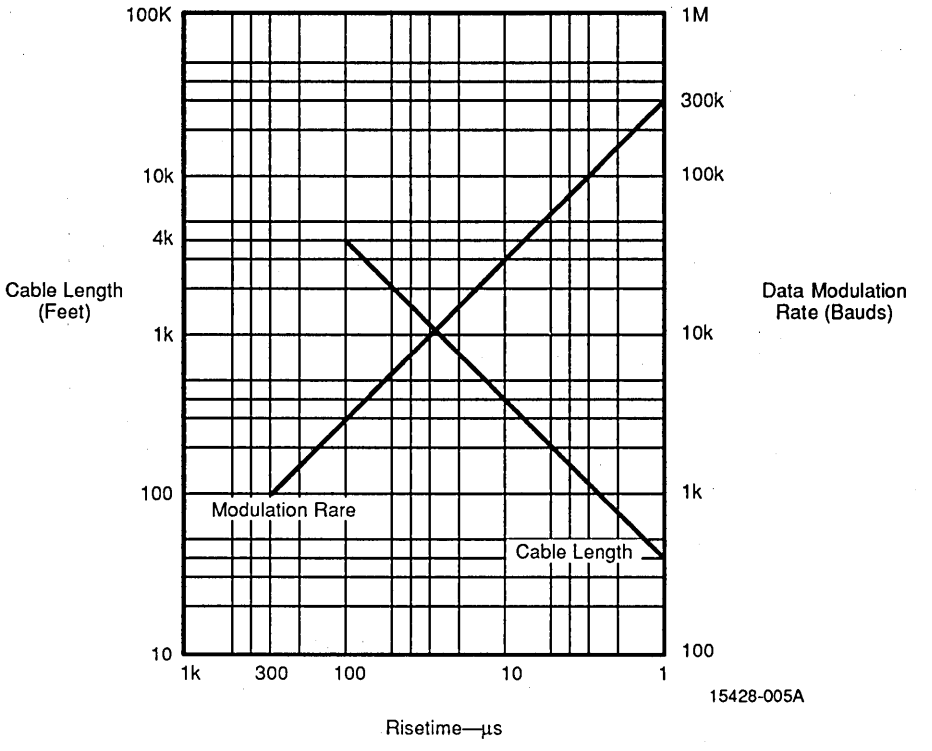


Figure 4. Data Modulation Rate or Cable Length Versus Risetime for EIA RS-423

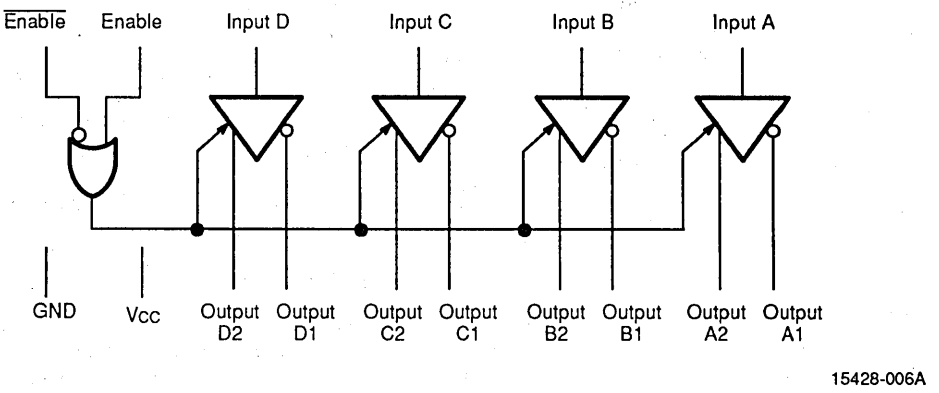


Figure 5. Am26LS31 Logic Diagram

Table 3. Summary Of EIA RS-422 Standard For A Balanced Differential Interface

A. Line Driver

Open Circuit Voltage (either logic state)
- Differential: $|V_{do}| \leq 6.0$ V
- Common Mode: $|V_{cmo}| \leq 3.0$ V

Differential Output Voltage (across 100 ohm load)
- Either logic state: $|V_d| \geq$ max. $|0.5\ V_{do}, 2.0\ V|$

Output Impedance
- Either logic state: $R_G \leq 100$ ohms

Mark-Space Level Symmetry (across 100 ohm load)
- Differential: $|V_{dS}| - |V_{dM}| \leq 0.4$ V
- Common Mode: $|V_{cmS}| - |V_{cmM}| \leq 0.4$ V

Output Short Circuits Current (to ground)
- Either Output: $|I_{SC}| \leq 150$ mA

Output Leakage Current (power off)
- Voltage Range: $-0.25\ V \leq V_x \leq +6.0$ V
- Either Output at V_X: $|I_X| \leq 100\ \mu A$

Rise and Fall Times (across 100 ohm load)
- T = Baud Interval: $(t_r, t_f) \leq$ max. (0.1T, 20 ns)

Ringing (across 100 ohm load)
- Definitions
- $V_{dSS} = V_{dd}$ (steady state)
- $V_{SS} = V_{dS} - V_{dM}$ (steady state)
- Limits (either logic state)
- Percentage: $|V_d - V_{dSS}| \leq 0.1\ V_{SS}$
- Absolute: $2.0\ V \leq |V_d| \leq 6.0$ V

B. Line Receiver

Signal Voltage Range
- Differential: $|V_d| \leq 6.0$ V
- Common Mode: $|V_{CM}| \leq 7.0$ V

Single-Ended Input Current (power ON or OFF)
- Either Input at V_X: $|V_x| = 10$ V
- Other Input Grounded: $|I_V| \leq 3.25$ mA

Single-Ended Input Bias Voltage (other input grounded)
- Either Input Open Circuit: $|V_B| \leq 3.0$ V

Single-Ended Input Impedance (other input grounded)
- Either Input: $R_L \geq 4000$ ohms

Differential Threshold Sensitivity
- Common Mode Voltage Range: $|V_{cm}) \leq 7.0$ V
- Either Logic State: $|V_T| \leq 200$ mV

Absolute Maximum Input Voltage
- Differential: $|V_d| \leq 12$ V
- Single-Ended: $|V_x| \leq 10$ V

Input Balance (threshold shift)
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0$ V
- Differential Threshold (500 ohms in series with each input)
- Either Logic State: $|V_t| \leq 400$ mV

Termination (optional)
- Total Load Resistance (differential): $R_T > 90$ ohms

Multiple Receivers (bus applications)
- Up to 10 receivers allowed. Differential threshold sensitivity of 200 mV must be maintained.

Hysteresis (optional)
- As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)
- As required by application to provide a steady MARK or SPACE condition under open connector or driver.

power
- OFF condition.

C. Interconnecting Cable

Type
- Twisted Pair Wire or Flat Cable Conductor Pair

Conductor Size
- Copper Wire (solid or stranded) 24 AWG or larger
- Other (per conductor): R ≤ 30 ohms/1000 ft.

Capacitance
- Mutual Pair: C ≤ 20 pF/ft.
- Stray: C ≤ 40 pF/ft.

Pair-to-Pair Cross Talk (balanced)
- Attenuation at 150 KHz: A ≥ 40 dB

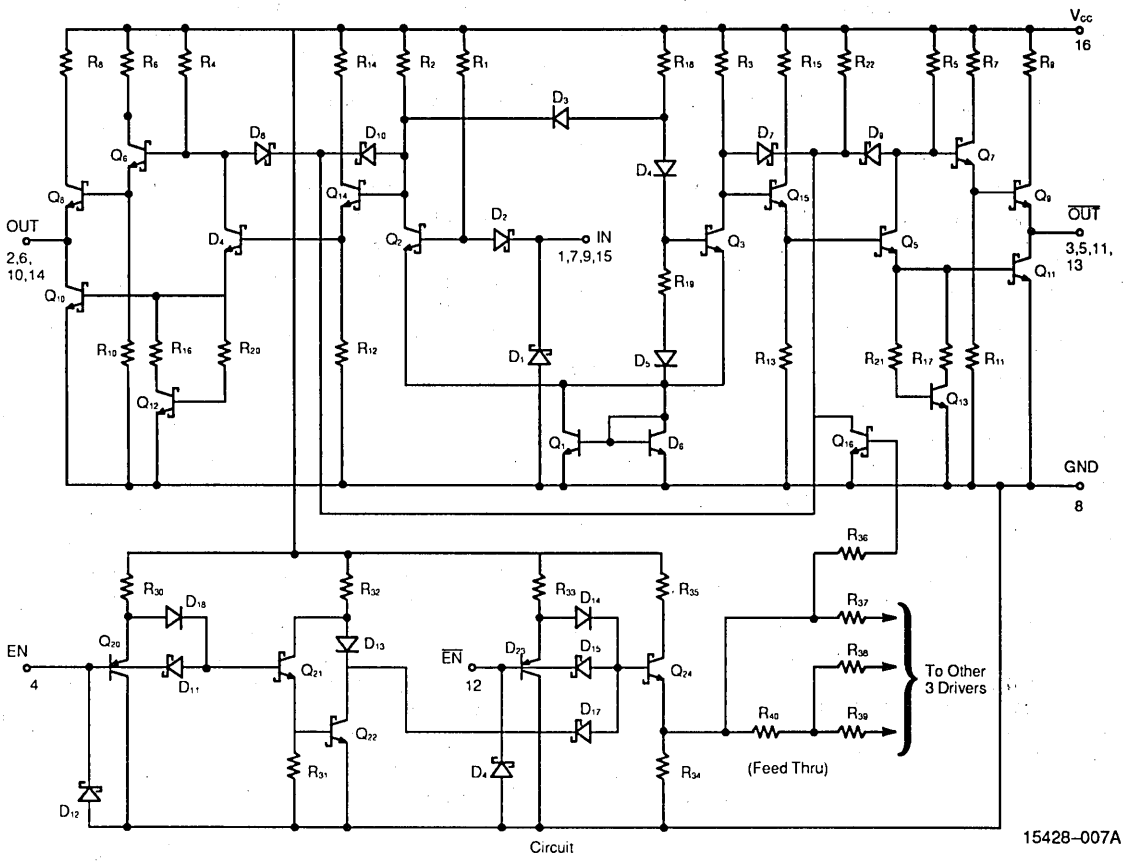


Figure 6. Am26LS31 Circuit Diagram (Only One Driver Shown)

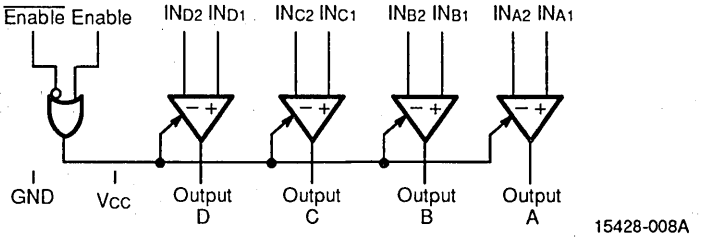
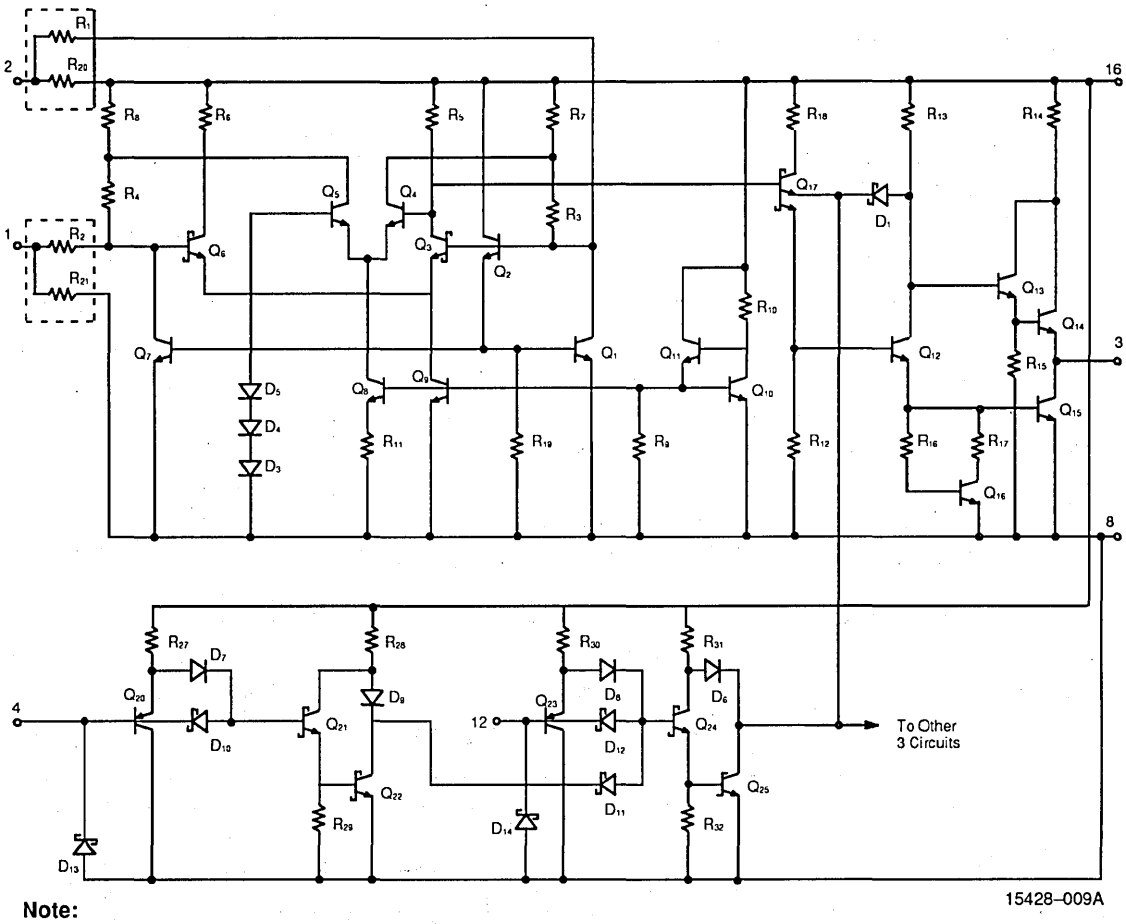


Figure 7. Am26LS32 Logic Diagram

The balanced differential line receiver is a three-stage circuit. The input stage consists of a low-impedance differential current amplifier with series resistor inputs to convert line signal voltage to current and provide a moderate input impedance. The input resistors provide impedance greater than 6K on each input, power on or power off, which exceeds the requirements of RS-422 and RS-423. This is one advantage of the current amplifier input circuit. Another advantage is that it can operate with immunity to common mode voltages above Vcc and below ground. The differential threshold sensitivity of this circuit is 200 mV, as required by RS-422. The second stage is a differential voltage amplifier, which interfaces to the single-ended output stage through an emitter follower. The output stage is a standard Low-power Schottky TTL totem-pole output with three-state capability.



Note:
R3 and R4 values for Am26LS32 are half the Am26LS33 values.

Figure 8. Am26LS32 and Am26LS33 Circuit Diagram (Only One Receiver Shown).

The full circuit is shown in Figure 8. Resistors R_{20} and R_{21}, which connect the non-inverting input to V_{CC} and the inverting input to ground, provide the fail-safe feature, which guarantees a HIGH logic state for the receiver output when there is no signal on the line. The differential voltage amplifier in the second stage is formed by Q_6 and Q_3 which are biased by current source Q9. The hysteresis in the receiver switching characteristic is provided by Q_4 and Q_5, a differential pair biased by current source Q_6, whose collectors are connected in positive feedback to the input pull-up circuits. A small amount of current is switched by Q_4 and Q_5, which must be overcome by the different voltage signal, resulting in the hysteresis. The output stage is driven from one side of the differential second stage by emitter follower Q_{17}, which is a multiple emitter transistor. The second emitter is the control point for the three-state output. Q_{17} drives the phase splitter Q_{12}, which in turn drives the three-state totempole output. The remainder of the circuit is the output enable control logic. This three-state capability on the receiver TTL side of the interface is a useful feature for modularizing two-way bus design.

A mask option of the input resistors (R_1, R_2, R_{20} and R_{21}) modifies the receiver characteristics to improve operation in high common mode noise environments. This device, known as the Am26LS33, has these resistors at twice the value of the Am26LS32. An input differential or common mode voltage range of ±15 V is achieved at the expense of a minor decrease of input threshold sensitivity, to ±500 mV from ±200 mV.

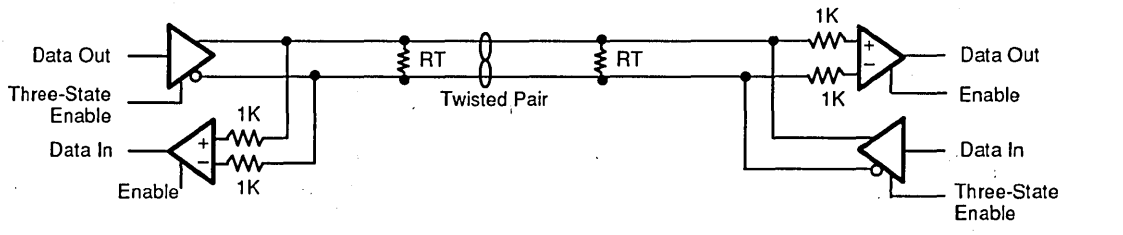


Figure 9. Bidirectional RS-422

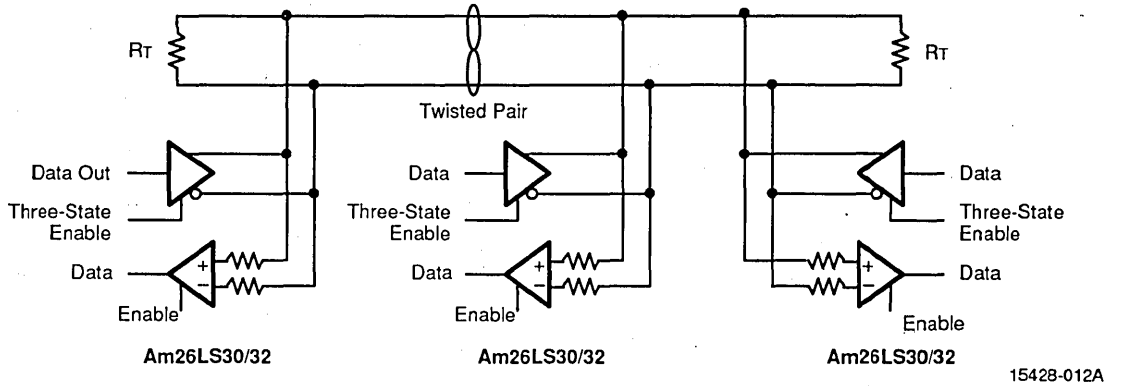


Figure 10. Party Line Configuration

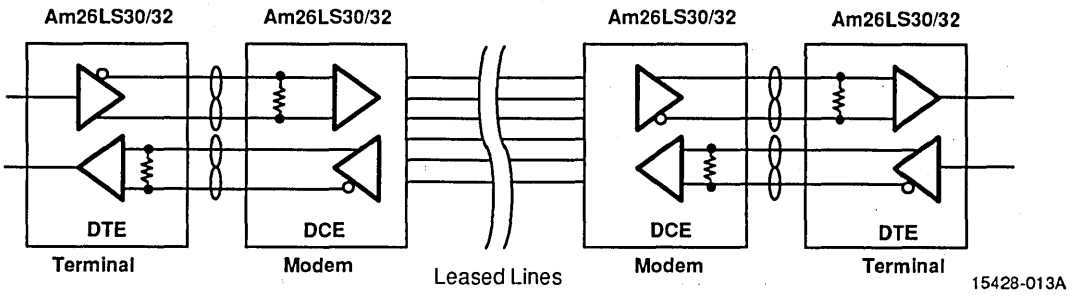


Figure 11. Full Duplex Four-Wire Data Communication RS-422 Interface (with Data Modem)

LINE TERMINATION TUTORIAL

It is important in a digital communication system to have the minimum amount of noise generated by undesired reflections at the driver and receiver. There are numerous ways of matching to the line. The line can be matched at the driver, at the receiver or both, each method has advantages and disadvantages. Generally for any but the longest lines it is sufficient to match at one place, and only when there are discontinuities in the line, party line operation, or lack of reasonable match at the opposite end of the line is the extra hardware of matching at both ends justified. The majority of transmission lines have fairly low characteristic impedances (in the range of 50 to 200 ohms) and the currents involved for a reasonable voltage swing are quite large. It is more difficult to couple noise into this low impedance, but it is also more difficult to drive, and line drivers must have the ability to supply large currents.

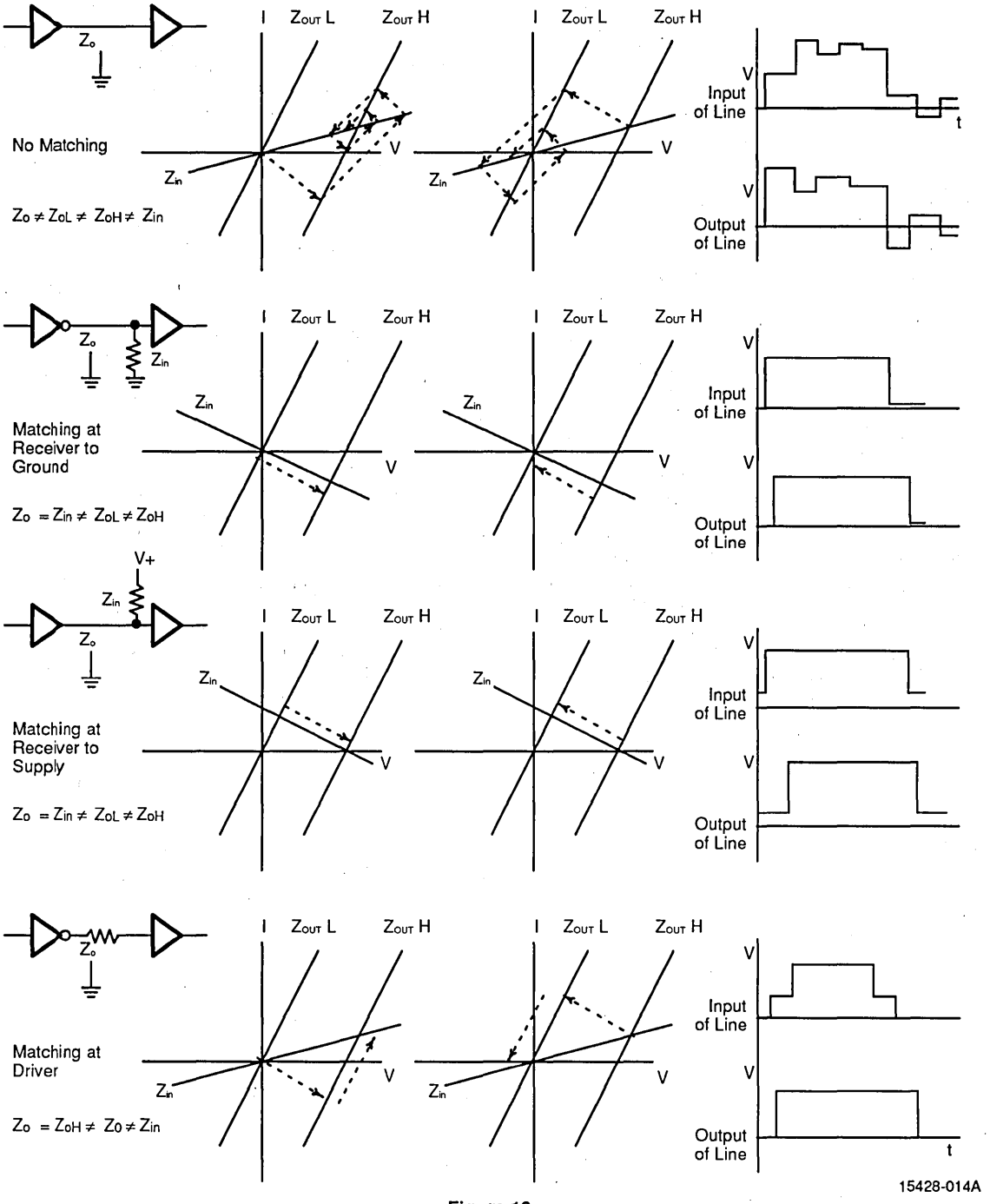
Various matching techniques that can be employed are shown in Figure 1. These impedance charts are useful in showing what happens to wave fronts traveling down a line, when the line delay is longer than the wave front transition. The DC input characteristic of the receiver, including any external components, is plotted on the V–I

graph together with the output characteristic of the driver, including any external components used at the driving end. There are always quiescent points—points where the driver and receiver characteristics cross. These points represent the DC voltage/current conditions, which must eventually be satisfied. To determine the effect of switching from one quiescent point to the other, a line with a slope equal to the characteristic impedance of the transmission line is plotted, starting at the initial quiescent point and ending at the applicable output impedance characteristic. The point of intersection gives the voltage and current at the output of the driver (and the input of the transmission line immediately after the driver switched states). From this point a line having an equal but opposite slope is drawn to the input characteristic and, at the intersection shows the voltage/current conditions of the wave front at the input of the receiver. This procedure is repeated to the output characteristic and so on at each intersection of the characteristic, the voltage/current relationship for a particular reflection is given. The resulting time/voltage relationships for the traveling wavefront at the two ends of the transmission line are shown alongside.

From the graphs several important features can be seen. If the line is not matched at either end considerable transient voltage swings can occur. In fact if the input and output characteristics are at right angles to one another, the reflections continue for an infinite time if the line is assumed to have zero loss. Most lines have extremely low losses, and, therefore, a very undesirable situation exists if the line is not matched at either end.

If the line is matched at the receiver, a voltage wave of constant amplitude travels down the line and is absorbed at the termination. Note whether the line is terminated to ground or to the power supply the system consumes DC power, either in the HIGH logic level or in the LOW logic level. In order to reduce the power dissipation, a blocking capacitor can be used in series with the receiver termination. The capacitor can be chosen to look like a short circuit to the voltage wavefront but stop DC (current) flow. Since the capacitor must be charged and discharged through the line, the data rate is reduced, when this technique is employed.

If the line is matched with a series resistor at the driver, then the line input initially rises to one half the final voltage. This wave front travels down the line and is reflected at the receiver. When the reflection reaches the driver the voltage at the driver rises to its final amplitude. The receiver, however, sees on transition from the initial to the final amplitude. When the driver switches from HIGH to LOW a similar situation occurs, in which the input of the line delays later, the final LOW condition. This back matching mode of operation consumes no DC power if the input impedance of the receiver is infinite. The advantage of the method is that if the input impedance of the receiver is high, very little power is dissipated and current only flows during the transition time, which is twice the line delay time. If back matching is used in a balanced system the terminating series resistance must be divided into two equal resistances with resistors inserted in series with each wire in order to maintain a balanced system.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Zo ≠ ZoL ≠ ZoH ≠ Zin
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Zin
V
Input of Line
Output of Line
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Matching at Receiver to Ground
Zo = Zin ≠ ZoL ≠ ZoH
V+
Matching at Receiver to Supply
Matching at Driver
Zo = ZoH ≠ Zo ≠ Zin
15428-014A

Figure 12.

CHAPTER 5
Physical Dimensions*

CD 016	16-Pin Ceramic DIP
CD 040	40-Pin Ceramic DIP
CD3024	24-Pin Ceramic DIP
CF 016	16-Pin Ceramic Flatpack
CL 020	20-Pin Leadless Chip Carrier
CL 044	44-Pin Leadless Chip Carrier
PD 016	16-Pin Plastic DIP
PD 040	40-Pin Plastic DIP
PD 048	48-Pin Plastic DIP
PL 044	44-Pin Plastic Leaded Chip Carrier
PL 068	68-Pin Plastic Leaded Chip Carrier
PL 084	84-Pin Plastic Leaded Chip Carrier
SO 016	16-Pin Plastic Small Outline Package
SO 024	24-Pin Plastic Small Outline Package

* All Dimensions are measured in inches, unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

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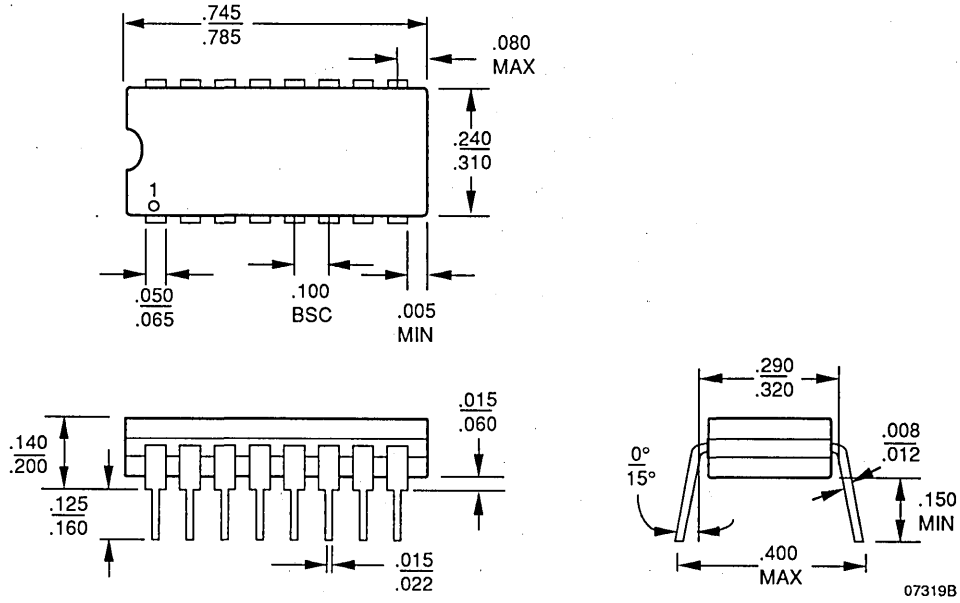

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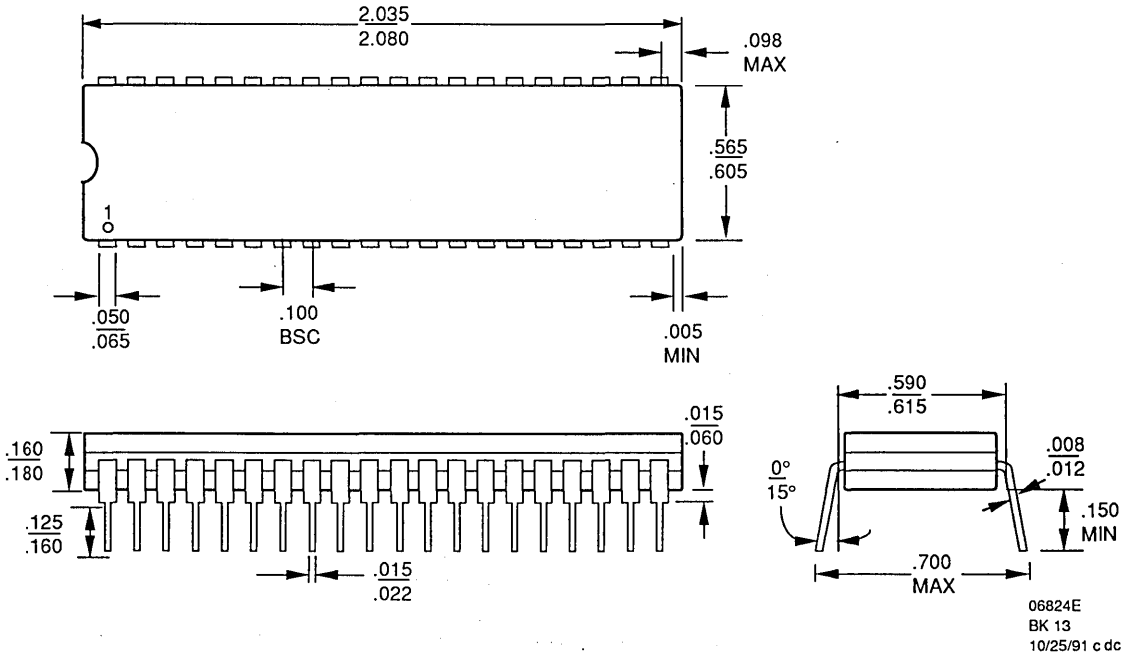

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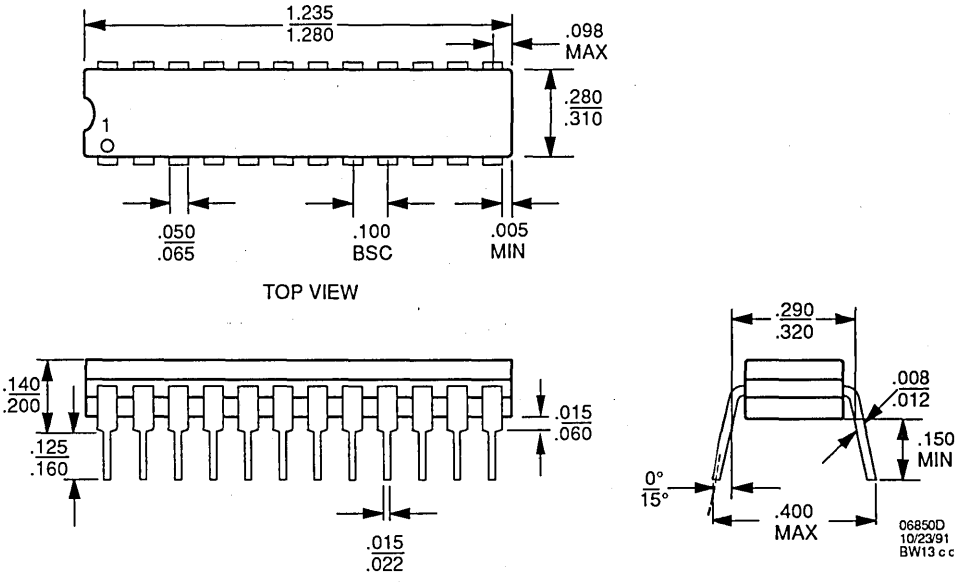

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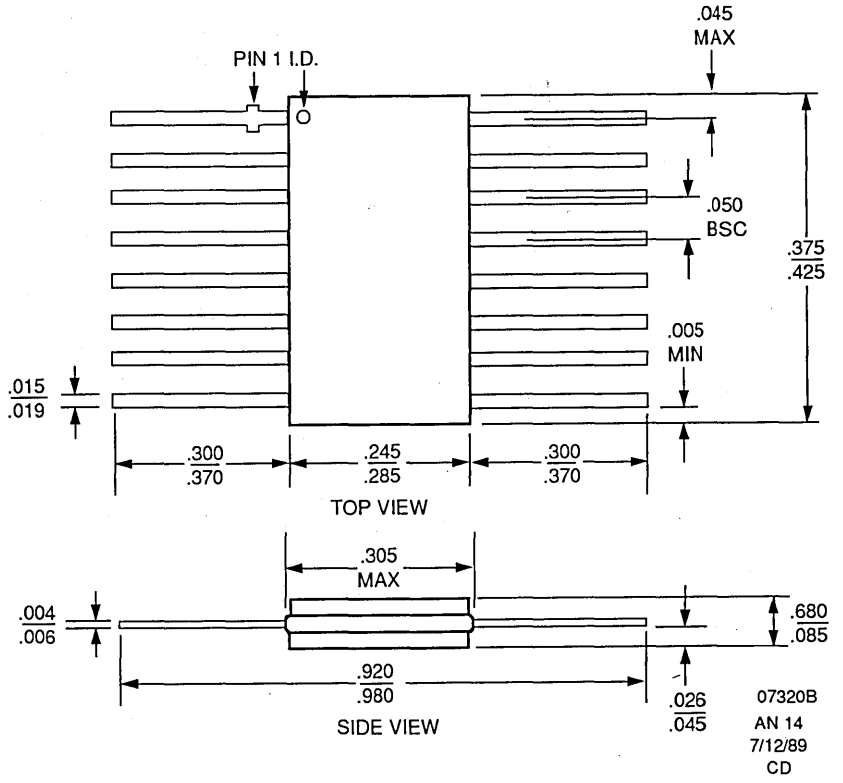

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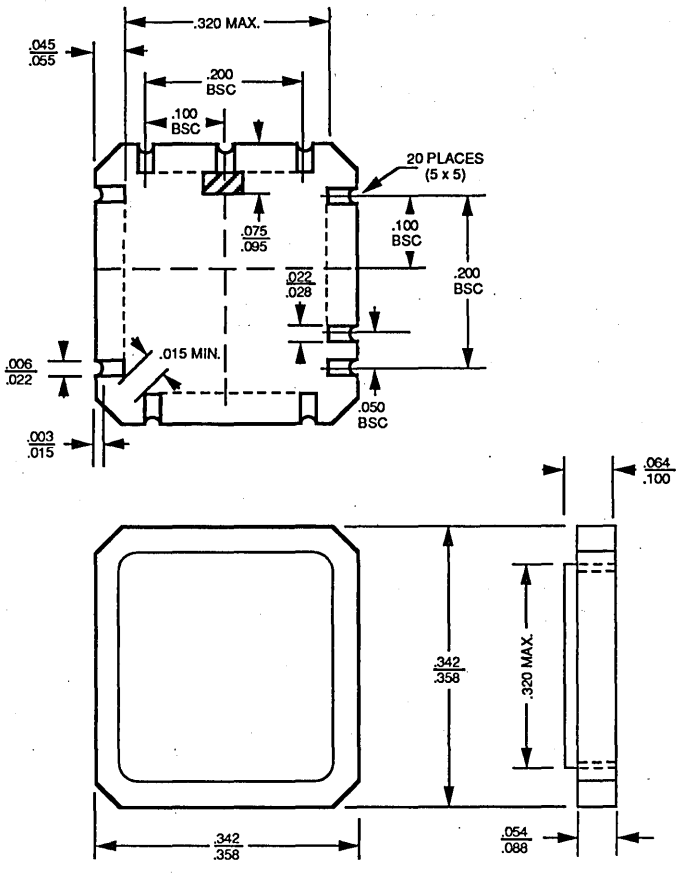

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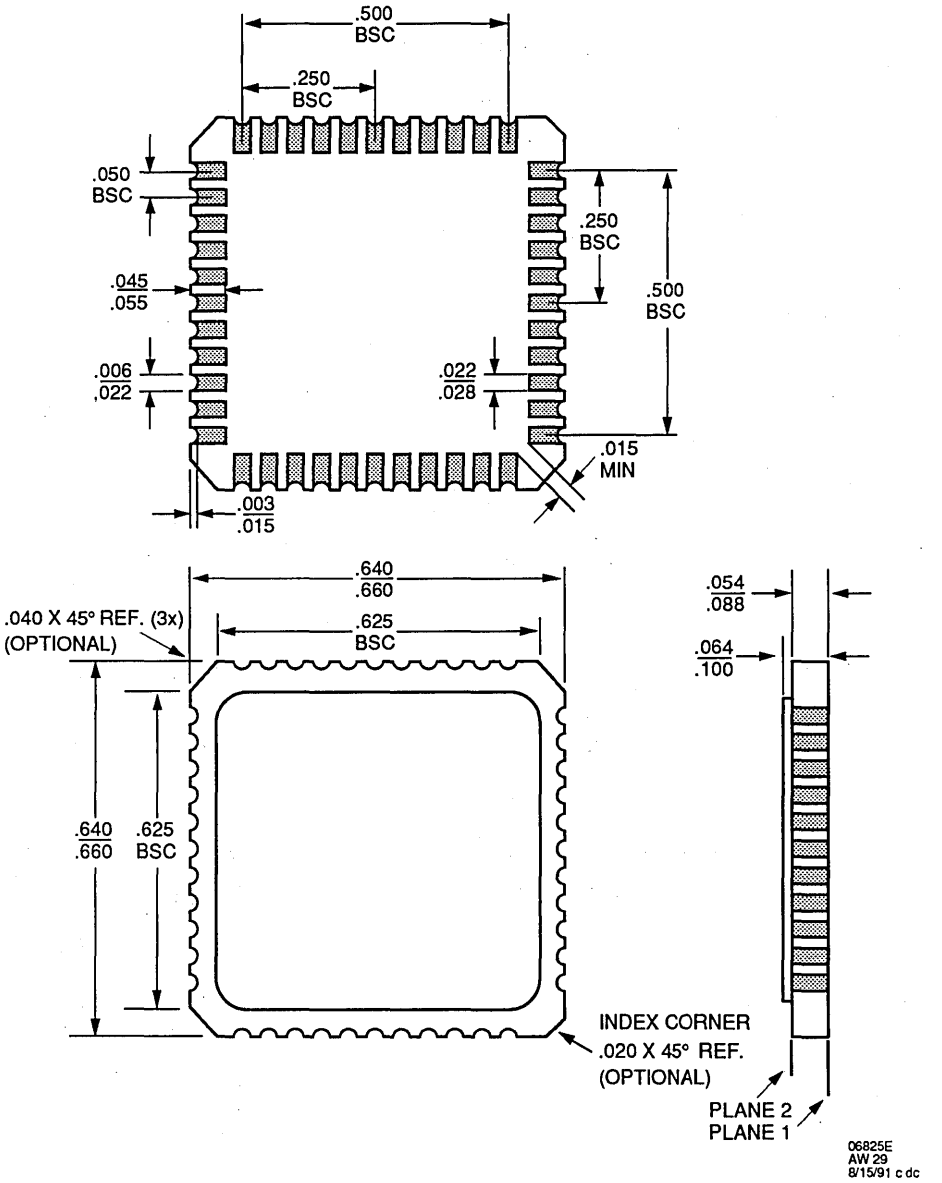
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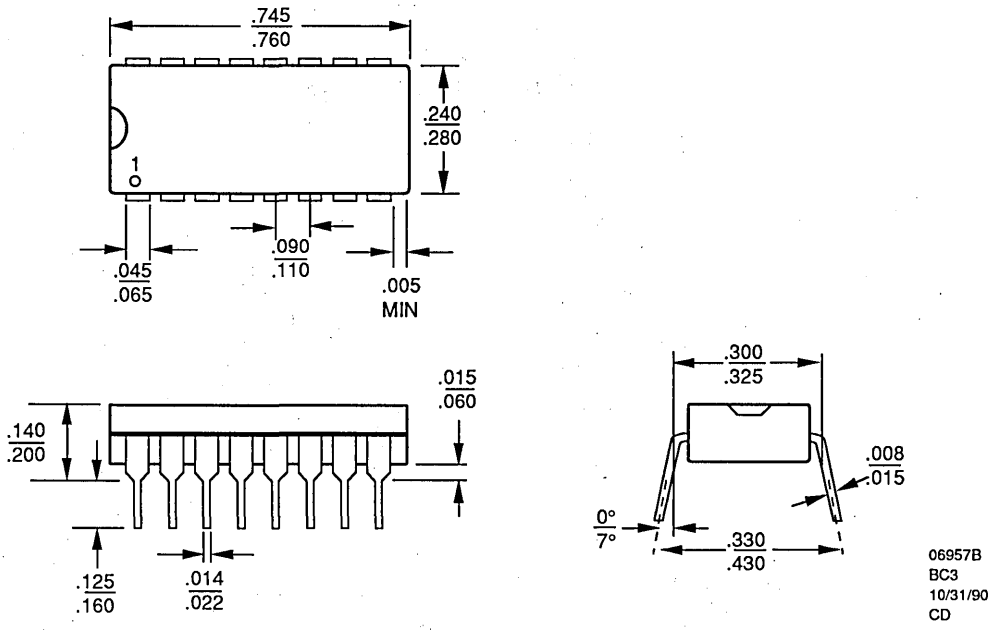

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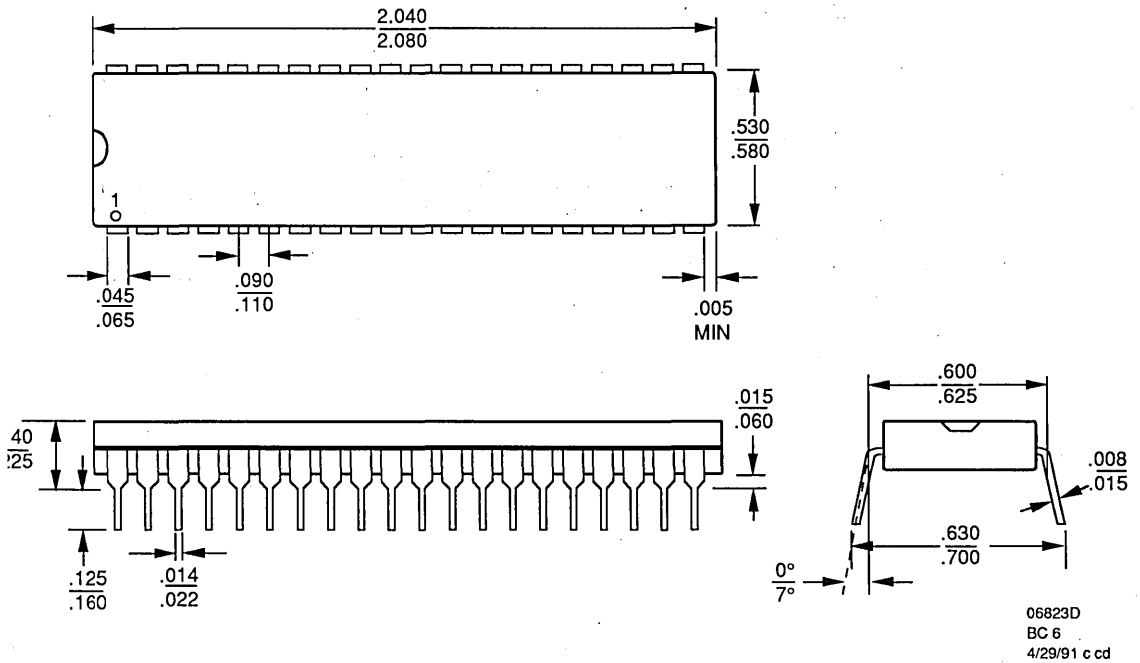

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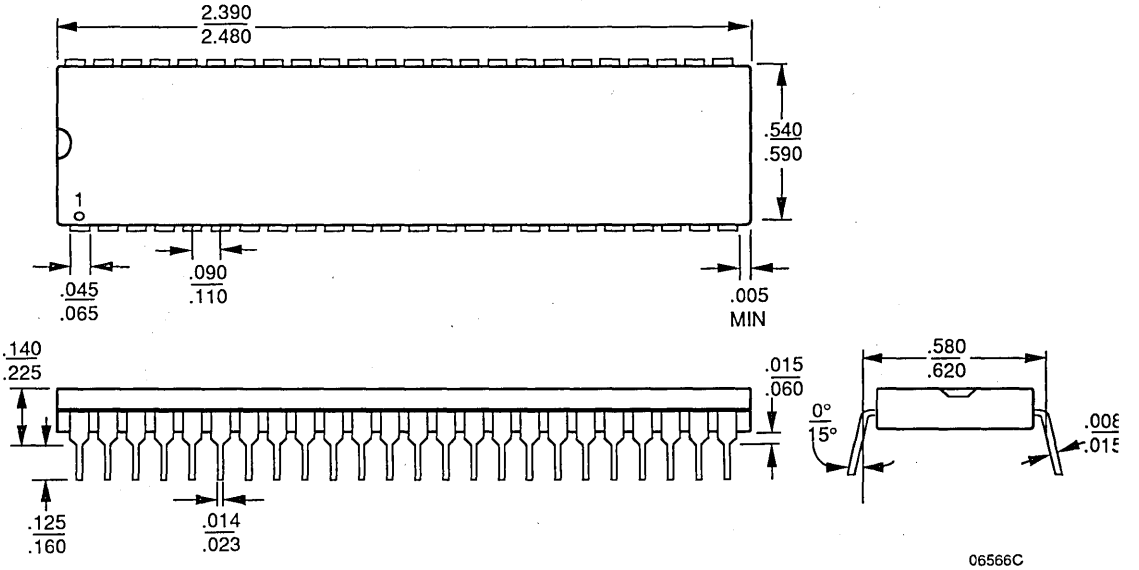

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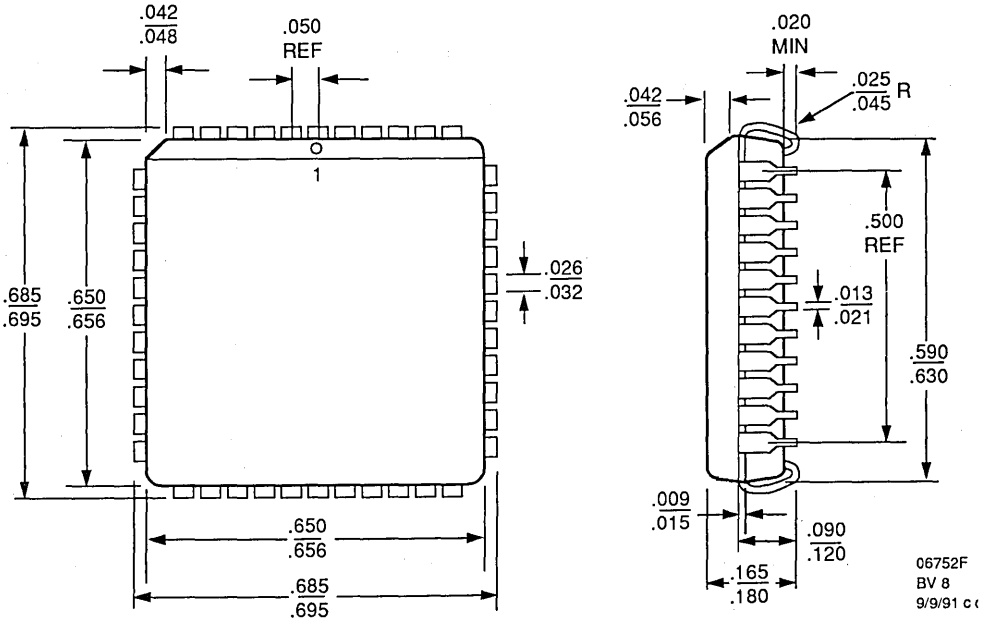

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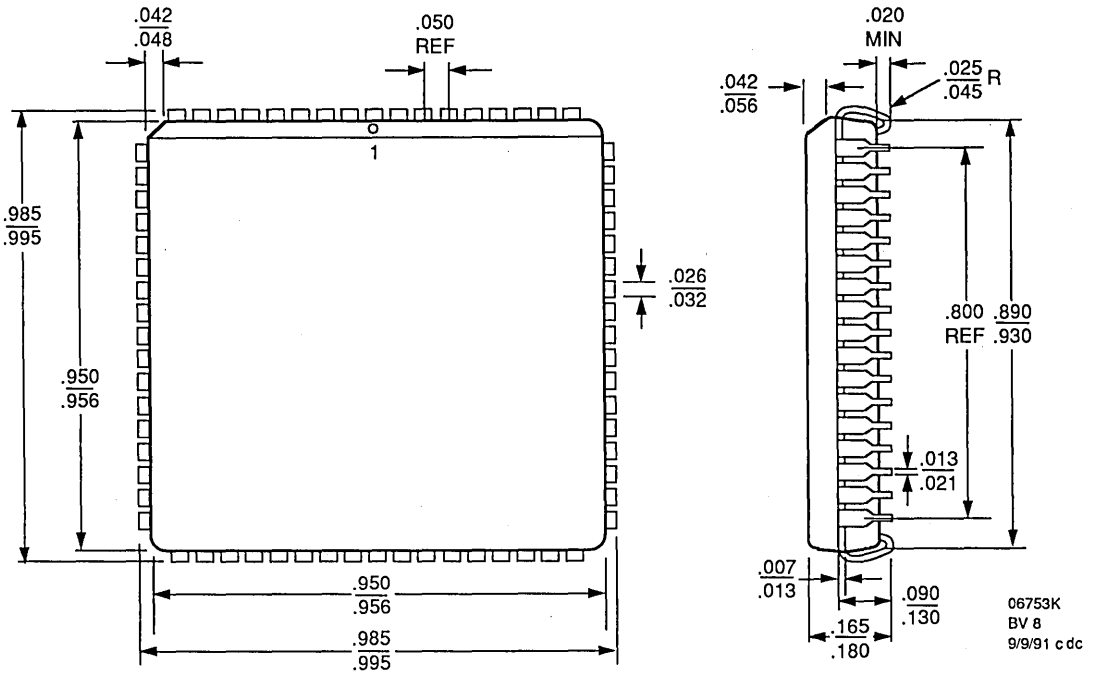
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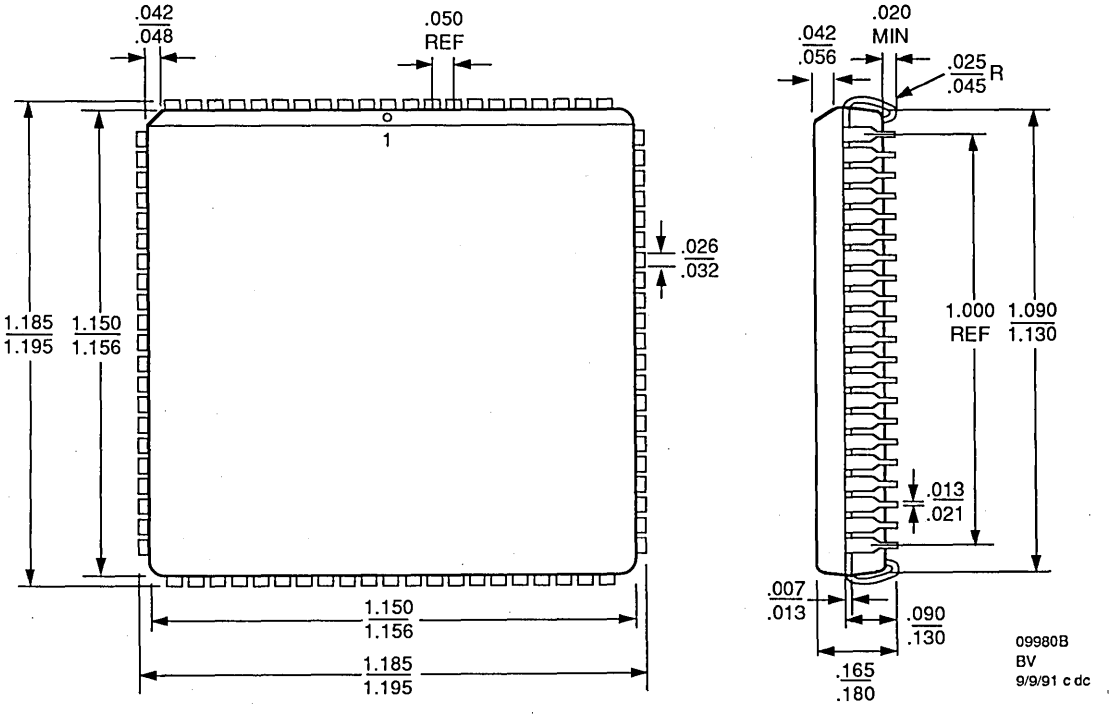
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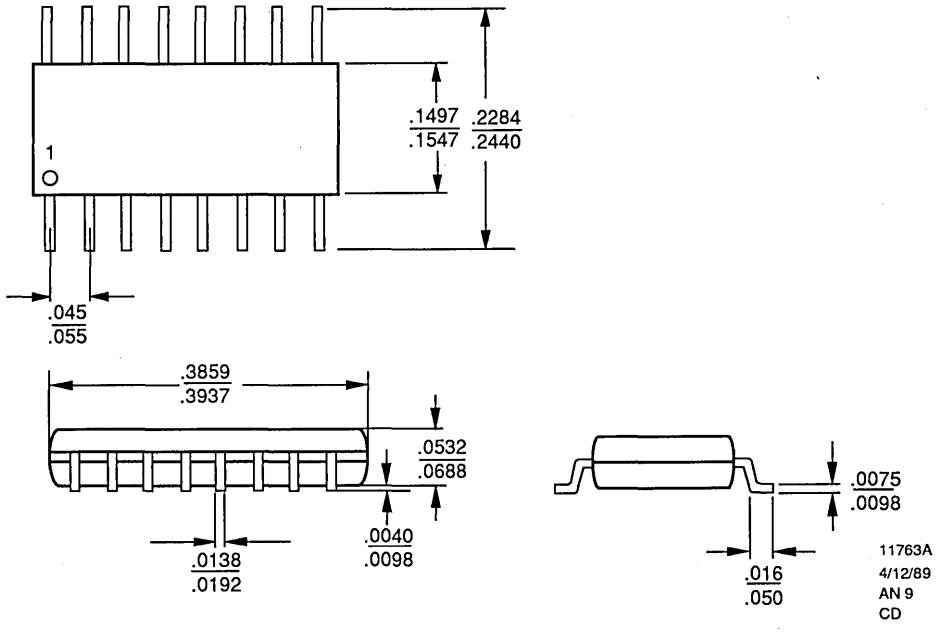
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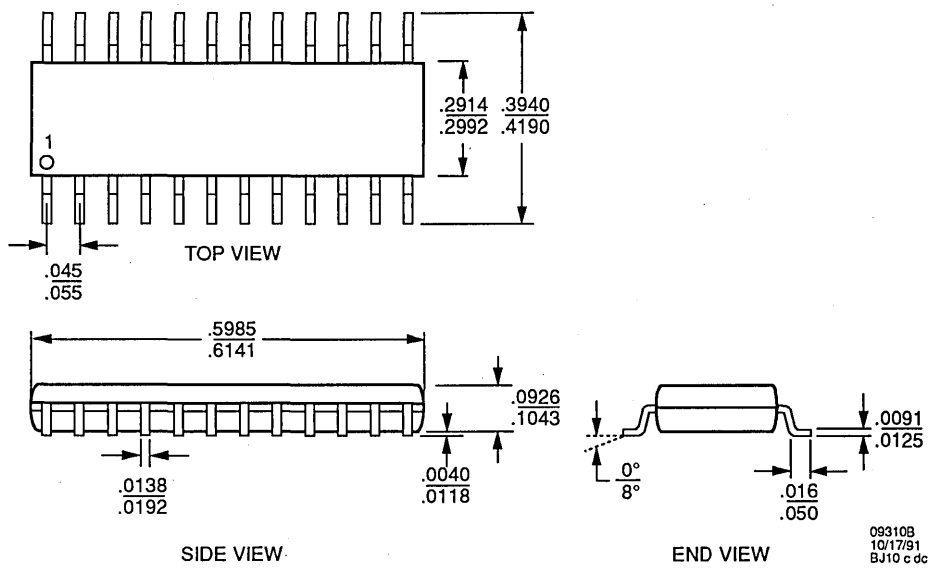
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APPENDICES

Am33C93A Qualification Information

The following qualification information summary has been included to aid the user with component evaluation and production release.

DEVICE PROCESS/DIE INFORMATION

1. Process Name: CS21
2. Process Technology: CMOS
3. Wafer Fabrication: Fab 15, Austin, Texas
4. Die Size: 209 x 183 mils
5. Last Overall Die Revision: "B"
6. Bond Pad Size: 125 µm x 125 µm
7. Substrate: N– epi over N+, P– well
8. Gate Oxide Thickness: 200 Angstroms
9. Number of Metal Layers: 2
10. Metal Thickness: 0.32 µm/1.0 µm
11. Content of Metalization:
    1st level – Ti/TiN–0.5%Cu/Al–MoSi
    2nd level – Al
12. Minimum Metal Line/Spacing Width:
    Metal 1 – 1.6 µm width, 1.2 µm spacing
    Metal 2 – 2.0 µm width, 1.6 µm spacing
13. Contact Dimensions (via's):
    Contact 1 – 1.2 µm x 1.2 µm
    Contact 2 – 1.4 µm x 1.4 µm
14. Passivation Material: 4% LTO/Nitride
15. Passivation Thickness: 7000 Angstroms/12500 Angstroms
16. ESD protection: > 2000 volts

Assembly/Package Information

1. Assembly Location: Korea, Malayasia, and Thailand
2. Test Location: Malaysia or Santa Clara, California

For PLCC/PDIP Packages:

3. Resin Identification: Epoxy Novolac
4. Package Compound: Sumitomo 6300H
5. Filler Content: Fused Silica
6. Thermal Conductivity: >13 x 10^{-4} calorie/cm°C sec
7. Glass Transition Temperature: 155°C
8. Die Attach Material: Silver Filled Epoxy
9. Die Attach Material Vendor: Dexter Hysol
10. Wire Bond Metal: 1.25 mil gold wire
11. Wire Bond Method: Thermosonic
12. Lead Frame Material: Copper
13. Lead Frame Finish: Solder Dip (PDIP), Solder Plate (PLCC)

Am53C80A Qualification Information

The following qualification information summary has been included to aid the user with component evaluation and production release.

DEVICE PROCESS/DIE INFORMATION

1. Process Name: CS11S
2. Process Technology: CMOS
3. Wafer Fabrication: Fab 15, Austin, Texas
4. Die Size: 150 x 170 mils
5. Last Overall Die Revision: "B"
6. Bond Pad Size: 125 µm x 125 µm
7. Substrate: N– epi over N+, P– well
8. Gate Oxide Thickness: 200 Angstroms
9. Number of Metal Layers: 2
10. Metal Thickness: 0.32 µm/1.0 µm
11. Content of Metalization:
    1st level – Ti/TiN–0.5%Cu/Al–MoSi
    2nd level – Al
12. Minimum Metal Line/Spacing Width:
    Metal 1 – 2.4 µm width, 1.44 µm spacing
    Metal 2 – 4.16 µm width, 1.76 µm spacing
13. Contact Dimensions (via's):
    Contact 1 – 1.28 µm x 1.28 µm
    Contact 2 – 1.6 µm x 1.6 µm
14. Passivation Material: 4% LTO/Nitride
15. Passivation Thickness: 7000 Angstroms / 8500 Angstroms
16. ESD protection: > 2000 volts

Assembly/Package Information

1. Assembly Location: Korea, Malayasia, and Thailand
2. Test Location: Malaysia or Santa Clara, California

For PLCC/PDIP Packages:

3. Resin Identification: Epoxy Novolac
4. Package Compound: Sumitomo 6300H
5. Filler Content: Fused Silica
6. Thermal Conductivity: >13 x 10^{-4} calorie/cm°C sec
7. Glass Transition Temperature: 155°C
8. Die Attach Material: Silver Filled Epoxy
9. Die Attach Material Vendor: Dexter Hysol
10. Wire Bond Metal: 1.25 mil gold wire
11. Wire Bond Method: Thermosonic
12. Lead Frame Material: Copper
13. Lead Frame Finish: Solder Dip (PDIP), Solder Plate (PLCC)

APPENDIX C

Am85C30 Qualification Information

1. Process Name: CS21S
2. Process Technology: CMOS
3. Wafer Fabrication: Fab 15, Austin, Texas
4. Production Date: December, 1991
5. Die Size: 152 X 208 mils
6. Die Thickness: 20 mils
7. Last Overall Die Revision: "B"
8. Gate Length: 0.8 µm
9. Number of Metal Layers: 2
10. Die Passivation 1/2: LTO/Nitride
11. Die Coating: None
12. Die Junction Temperature (Tjmax): 77°C for commercial product
13. Fab Flow:
    Well Definition
    Source/Drain Definition
    VT Implants
    Poly Deposition
    Contact 1
    Metal 1
    Planarization
    Contact 2
    Metal 2
    Topside

Statistical process control (SPC) is utilized at all fabrication steps. SPC is computer-based and is controlled by manufacturing.

All additional information on wafer fabrication is AMD proprietary.

PACKAGE DATA

For PLCC/PDIP Packages:

1. Assembly Location: Penang, Manila or Bangkok
2. Test Location: Singapore or Sunnyvale, California
3. Package Compound: Sumitomo 6300H
4. Glass Transition Temperature: 150°C
5. Die Attach Material: Silver Epoxy
6. Die Attach Material Vendor: Kyocera
7. Wire Bond Metal: 1.25 mil gold wire
8. Wire Bond Method: Thermosonic gold ball wirebond
9. Lead Frame Material: Copper Alloy
10. Lead Frame Finish: Solder Plate
11. Theta ja (Oja): 43°C/Watt for PDip package
    41°C/Watt for PLCC package

Ceramic/LCC Packages:

1. Assembly Location: Penang, Manilla or Bangkok
2. Test Location: Singapore or Sunnyvale, California
3. Sealing Glass Material: (CDip only) LS0113
4. Glass Transition Temperature: (CDip only) 150°C
5. Die Attach Material: Silver Glass
6. Die Attach Material Vendor: Kyocera
7. Wire Bond Metal: Aluminum
8. Wire Bond Method: Ultrasonic
9. Lead Frame Material: (CDip only) Alloy 42
10. Lead Frame Finish: (CDip only) Matte Tin Plate
11. Theta ja (Oja): 30°C/Watt for CDip package
    42°C/Watt for LCC package

Statistical process control (SPC) is utilized at all fabrication steps. SPC is computer-based and is controlled by manufacturing.

Am85C80 Qualification Information

The following qualification information summary has been included to aid the user with component evaluation and production release.

DEVICE PROCESS/DIE INFORMATION

1. Process Name: CS21
2. Process Technology: CMOS
3. Wafer Fabrication: Fab 15, Austin, Texas
4. Die Size: 213 x 258 mils
5. Last Overall Die Revision: "B"
6. Bond Pad Size: 125 µm x 125 µm
7. Substrate: N– epi over N+, P– well
8. Gate Oxide Thickness: 200 Angstroms
9. Number of Metal Layers: 2
10. Metal Thickness: 0.32 µm/1.0 µm
11. Content of Metalization:
    1st level – Ti/TiN–0.5%Cu/Al–MoSi
    2nd level – Al
12. Minimum Metal Line/Spacing Width:
    Metal 1 – 1.6 µm width, 1.2 µm spacing
    Metal 2 – 2.0 µm width, 1.6 µm spacing
13. Contact Dimensions (via's):
    Contact 1 – 1.2 µm x 1.2 µm
    Contact 2 – 1.4 µm x 1.4 µm
14. Passivation Material: 4% LTO/Nitride
15. Passivation Thickness: 7000 Angstroms/12500 Angstroms
16. ESD protection: > 2000 volts

Assembly/Package Information

1. Assembly Location: Korea, Malayasia, and Thailand
2. Test Location: Malaysia or Santa Clara, California

For PLCC Package:

3. Resin Identification: Epoxy Novolac
4. Package Compound: Sumitomo 6300H
5. Filler Content: Fused Silica
6. Thermal Conductivity: >13 x 10^{-4} calorie/cm°C sec
7. Glass Transition Temperature: 155°C
8. Die Attach Material: Silver Filled Epoxy
9. Die Attach Material Vendor: Dexter Hysol
10. Wire Bond Metal: 1.25 mil gold wire
11. Wire Bond Method: Thermosonic
12. Lead Frame Material: Copper
13. Lead Frame Finish: Solder Plate

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